Local poly-SiO_x carrier-selective contacts deposited through a hard mask

Simplified fabrication technique for local poly-SiO_x finger formation

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by

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Abstract

Passivating contacts in the front-rear contacted c-Si solar cells enhances the device performance by quenching the contact recombination and enabling sufficient carrier transport. Tunneling oxide passivating contact (TOPCon) which consists of an interfacial oxide and a poly-SiO_x layer is one of the most promising contact techniques in passivating both surfaces of the silicon wafer. However, the full area poly-SiO_x layer is absorptive when it is applied at the front side which has become an efficiency limiting factor. In this project, an advanced local poly-SiO_x passivating contact architecture is proposed and presented. The local poly-SiO_x passivating contacts, so-called "poly-SiO_x finger", is deposited through a hard mask at predefined locations which will be only placed underneath the metal contacts. The formation of poly-SiO_x finger and its application in the solar cells are discussed.

First, a silicon wafer hard mask is fabricated by a lithography process followed by a KOH wet chemical etch-back process. Specified openings down to 38.7 μm are established which isolate sections of the substrate for the poly-SiO_x finger formation. P^+ doped a-SiO_x:H is deposited using PECVD with SiO_x p^+ diffused emitter commercial Cz wafers through the hard mask. By investigating the influence of deposition parameters during the PECVD, specifically the power and pressure, decent uniformity of the finger deposition is achieved. An optimized deposition condition of the doped a-SiO_x:H is established for the poly-SiO_x finger formation: an RF power source at 15 Watt, a chamber pressure of 1.5 mbar, and a substrate temperature of 180 °C. A narrow poly-SiO_x finger with a width of 40.0 μm has been demonstrated.

Second, the passivation properties of the symmetrical samples are examined by varying the poly-SiO_x and Al_2O_3 thickness for the hole carrier selective contacts. A full area p^+ TOPCon and Al_2O_3 symmetric samples were coated on the textured diffused p^+ surface with an n-type c-Si substrate to investigate the process parameters on the passivation properties. The optimal iV_{oc} of p^+ TOPCon samples is 662 mV and a corresponding J_0 of 156 fA/cm^2 which is obtained with a poly-SiO_x thickness of 50 nm when annealed at 850 °C. The optimal thickness for the Al_2O_3 passivation layer is achieved by depositing a 20 nm thick layer followed by FGA, with an iV_{oc} of 692 mV and a J_0 of 22.4 fA/cm^2.

Finally, a process flowchart has been created to fabricate c-Si solar cells with the local p^+ TOPCon on the front p^+ diffused emitter and a full area n^+ TOPCon on the rear side. A localized polished area is made by a poly-etch process for the alignment between the substrate and the pattern in the lithography mask. Using the ascertained parameters during the optimization, NAOS-SiO_x combining with 50 nm-thick doped p^+ a-SiO_x:H fingers are applied on the p^+ diffused surface and 100 nm-thick n^+a-SiO_x:H on the rear side. A annealing step is performed for the crystallization. A 20 nm-thick Al_2O_3 followed by a 75 nm SiN_x layer are deposited on the front side and 100 nm SiN_x layer is applied on the rear side. Lithography, wet chemical etch-back together with Al/Ag(front/rear) evaporation are utilized for solar cells metallization. The fabricated c-Si solar cells with poly-SiO_x fingers has a champion efficiency with an efficiency of 7.91 %, with a iV_{oc} of 562 mV, $_{int}J_{sc}$ of 34.7 mA/cm^2 and fill factor of 40.5 %. The limited performance originates from the poor passivation in the poly-SiO_x local contact area and severe iV_{oc} drop after the metallization process. For further improvement, good performing c-Si solar cells by minimizing the recombination in the poly-SiO_x local fingers contacts area and optimizing metallization steps are expected to be fabricated .

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Nomenclature

Abbreviations

Abbreviation	Definition
a-SiO_x:H	Hydrogenated amorphous silicon oxide
ALD	Atomic layer deposition
ARC	Anti-reflection coating
BOE	Buffer oxide etch
BSF	Back surface field
c-Si	Crystalline silicon
CVD	Chemical vapor deposition
Cz	Czochralski
ECV	Electrochemical capacitance–voltage
EQE	External quantum efficiency
IR	Infrared
J-V	Current density and voltage
MFC	Metal finger coverage
NAOS	Nitric acid oxidation of silicon
NMP	N-methylpyrrolidon
PCE	Power conversion efficiency
PECVD	Plasma enhanced chemical vapor deposition
PERC	Passivated emitter and rear cells
PERL	Passivated emitter locally diffused cells
poly-SiO_x	Polycrystalline silicon oxide
PV	Photovoltaics
RCA	Radio corporation of America
RTA	Rapid thermal annealing
SEM	Scanning electron microscope
SPC	Solid-phase crystallization
SRH	Shockley-Read Hall
STC	Standard test conditions
TLM	Transmission line method
TOPCon	Tunnel oxide passivated contact

Symbols

Symbol	Definition	Unit
A	Surface area	$[cm^2]$
c	Speed of light *in vacuo*	$[m/s]$
E	Energy	$[eV]$
FF	Fill factor	$[\%]$
G	Photogeneration rate	$[cm^{-3}s^{-1}]$
h	Planck constant	$[m^2 * kg/s]$
I_{sc}	Short-circuit current	$[mA]$
J_0	Saturation current density	$[mA/cm^2]$
$_{int}J_{sc}$	Integrated short-circuit current density	$[mA/cm^2]$
J_{mpp}	Maximum power point current density	$[mA/cm^2]$
J_{ph}	Photogenerated current density	$[mA/cm^2]$
J_{sc}	Short-circuit current density	$[mA/cm^2]$
k_B	Boltzmann constant	$[JK^{-1}]$
L_T	Transfer length	$[\mu m]$
N_{sT}	Surface trap density	$[cm^{-2}]$
n	Electron density	$[cm^{-3}]$
P	Power density	$[W/cm^2]$
R_c	Contact resistance	$[\Omega]$
R_s	Sheet resistance	$[\Omega/\square]$
R_{sh}	Shunt resistance	$[\Omega]$
S_r	Surface recombination velocity	$[cm/s]$
T	Temperature	$[K]$
V_{mpp}	Maximum power point voltage	$[mV]$
V_{oc}	Open-circuit voltage	$[mV]$
W	Width	$[\mu m]$
λ	Wavelength	$[nm]$
ρ_c	Contact resistivity	$[\Omega * cm^2]$
σ	Capture cross section	$[cm^2]$
τ	Lifetime	$[\mu s]$
v_{th}	Thermal velocity	$[cm/s]$

1
Introduction

1.1. Silicon solar cells

Solar energy is an indispensable building block for a renewable and neutral energy-system both in the Netherlands and worldwide. The current cumulative installed capacity of PV modules in the Netherlands at the end of 2022 exceeded 19 GW, worldwide this number is 700 GW [1, 2]. Given that the large-scale usage of fossil fuels and the excessive CO_2 emissions that come with it are the most important, but not the only, cause of climate change, the implementation of Photovoltaic (PV) Technology will only increase [3]. There are promising incentives to continue the development and implementation of PV. The abundance of materials provides a good supply to fabricate PV modules, and the long-term stability of crystalline silicon (c-Si) ensures a long lifetime of the PV modules. The expectation is that the role of electricity generated from solar PV will strongly increase, potentially up to 90% of the total energy supply in 2050 [4]. In order to make PV more affordable, it is important to increase the power conversion efficiency (PCE) of semiconductor materials. Higher efficiencies lead to higher yields which in turn results in lower module costs. Figure 1.1 shows the progression of efficiencies from various companies and institutions over the years.

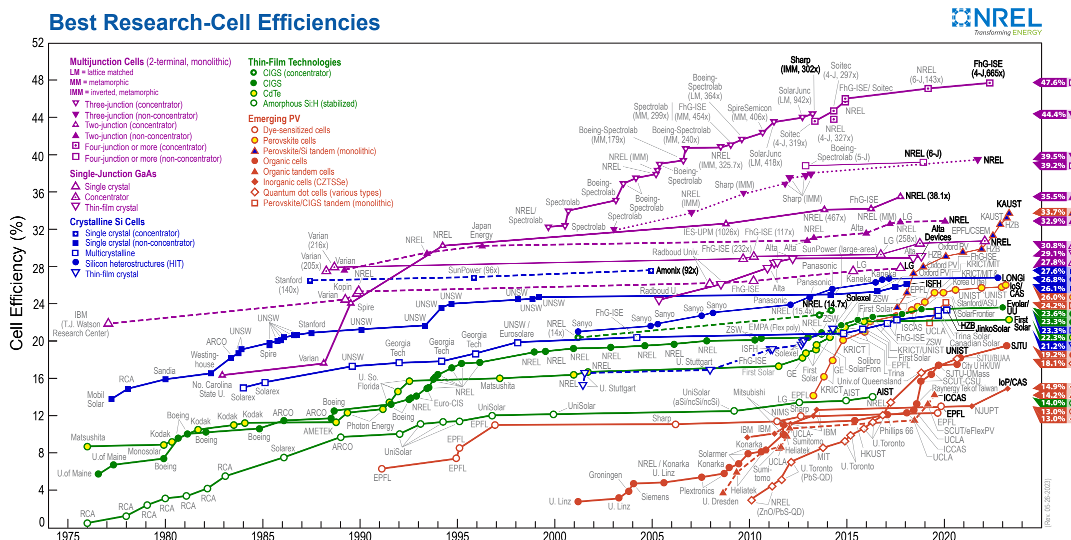

Figure 1.1: Timeline of research solar cell energy conversion efficiencies since 1976 [5].

As figure 1.1 illustrates, there are many types of solar cells, and all of them are made of semiconductor materials. Semiconductor materials come from different groups in the periodic table and they share certain qualities. A conductor is a material that has the ability to conduct electricity. An insulator is a material that has a poor conduction of electricity. A semiconductor is a material that has a moderate

conductivity that sits between a conductor and an insulator. At low temperatures the semiconductors will behave as insulators, and at higher temperatures they start to behave as conductors. There are numerous elements and compounds that can be used as semiconductor material. Silicon (Si) however is the most used material due to the low material costs, its ease of fabrication and a high abundance [6].

When a semiconductor is at an elevated temperature, such as the temperature where solar cells operate, electrons that are present in the semiconductor lattice potentially start to move. Only if an electron gains enough energy to move around the lattice it can participate in conduction. The minimum amount of energy that is required for an electron to break free is called the bandgap of a semiconductor. The energy and quantity of free electrons participating in conduction is crucial to the operation of solar cells. Due to an electron moving around the lattice a space is left vacant. This space is called a hole and appears as a positive charge in contrast to the electron. A good method to visualize the bandgap is with a schematic showing the energy bands for electrons in a solid, as shown in figure 1.2. When an electron attains enough energy it can excite from the valence band into the conduction band. The minimum required amount of energy for this process has to be greater than or equal to the bandgap energy. This energy varies per semiconductor material, for silicon it is equal to 1.12 eV [7]. When an electron-hole pair is generated and separated the final step is to collect them. This will take place at metal contacts that form a connection with the semiconductor. The metal contacts are commonly designed as a so-called finger grid designed to conduct the photogenerated current. A connection to an external circuit allows the charge carriers to be transported out and perform electrical work. The carrier behaviors can be summarized in four steps:

1. The absorption of photons in the semiconductor with energy greater than the bandgap energy ($E > E_{gap}$).
2. Formation of an electron-hole pair, with the electron moving from the valence band to the conduction band.
3. Movement of the charge carriers through the semiconductor material.
4. Collection of the charge carriers at the contacts attached to both sides of the semiconductor surface.

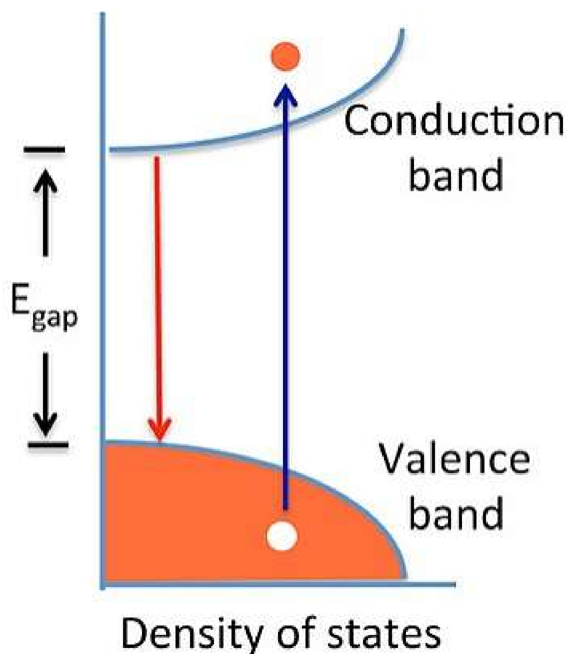

Figure 1.2: An electron-hole pair is created when supplied sufficient energy (blue arrow). The electron-hole pair recombines to release energy [8].

For the separation of the charge carriers solely pure silicon will not be sufficient. A p-n junction has to be created in the semiconductor which allows for both types of charge carriers to relocate to

one specific side of the semiconductor material. The process which provides the materials required to form a p-n junction is called doping. During the doping process the number of electrons and holes is varied. Once there is a dopant present in the semiconductor material the charge carriers can be referred to as either majority or minority charge carriers. The n-type doping increases the number of available electrons, the electrons are now called the majority charge carriers and hole are the minority charge carriers. For p-type doping it is the exact opposite; the number of available holes is increased, holes become the majority charge carriers and electrons the minority charge carriers. The p-n junction is established by joining n-type and p-type material, leading to the separation of charge carriers.

Figure 1.3 shows a simplified representation of a high efficiency solar cell. It is composed of the front contacts, a thin anti-reflection coating (ARC), a n-type emitter layer, a p-type absorber layer, a p-type back surface field and full-area back contacts. The bulk material of the solar cell is the absorber layer, this layer is also called the base and will absorb the majority of the incident photons and excites charge carriers to the conduction band [9]. The top layer of the solar cell is referred to as the emitter, together with the base it forms the p-n junction. The back surface field (BSF) is a highly doped region, the interface's highly and low doped regions behave similar to a p-n junction despite being the same dopant type. The purpose of the BSF is to prevent minority carriers from reaching the back contacts, this promotes the solar cell efficiency.

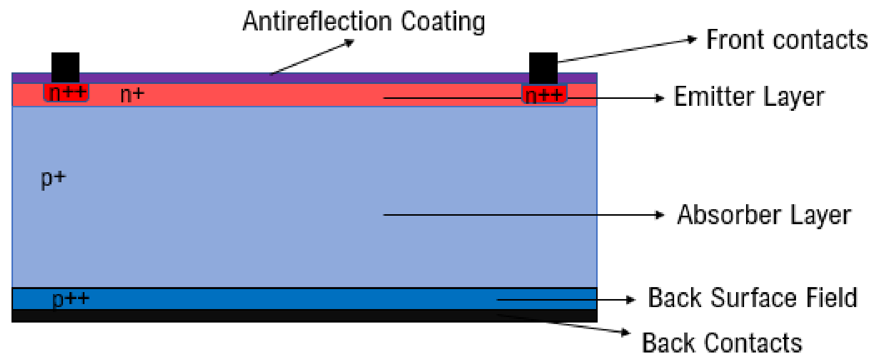

Figure 1.3: A schematic visualization of a typical crystalline silicon solar cell [10].

The efficiency of solar cells is characterized by various parameters indicating the performance. Most importantly the current-voltage parameters include the short-circuit current (I_{sc}), the open-circuit voltage (V_{oc}) and the fill factor (FF) [11]. The I_{sc} is the current flowing through the solar cell when the electrodes are short circuited, and it expresses the maximum collection of photogenerated charge carriers. The I_{sc} is dependent on the solar cell area, a more common manner to express this property is the short circuit current density J_{sc} by using equation 1.1. The maximum current that the solar cell can deliver depends on the optical properties of the solar cell which include the absorption in the absorber layers and the reflection.

$$J_{sc} = \frac{I_{sc}}{A} \tag{1.1}$$

where A is the surface area of the solar cell in cm^2.

The V_{oc} is the maximum amount of voltage that the solar cell can deliver, it is obtained when no current flows through the solar cell. It is dependent on the photogenerated current density and can be calculated using equation 1.2:

$$V_{oc} = \frac{k_B * T}{q} * ln(\frac{J_{ph}}{J_0} + 1) \approx \frac{k_B * T}{q} * ln(\frac{J_{ph}}{J_0}) \tag{1.2}$$

where K_B is the Boltzmann constant , T is the temperature, q is the elementary charge, J_{ph} is the

photogenerated current and J_0 is the saturation current density.

The power output of a solar cell can be calculated by multiplying the current and the voltage, the fill factor is the ratio of the maximum power output of the solar cell and the product of J_{sc} and V_{oc}. The maximum power point (MPP) denotes the point when plotting the J-V characteristics of the solar cell where the power output is the highest. The current and voltage of the MPP will always be lower than those of the J_{sc} and V_{oc}, thus the FF is never higher than 1. Calculating the FF is achieved by using equation 1.3:

$$FF = \frac{J_{mpp} * V_{mpp}}{J_{sc} * V_{oc}} \tag{1.3}$$

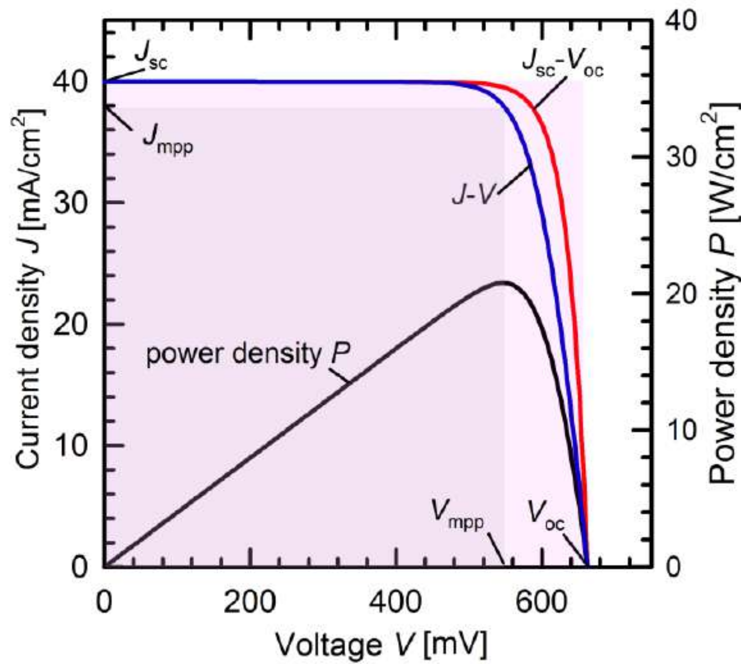

Figure 1.4: Graph visualizing the J-V curve of a solar cell given in blue and the power density of given in black. The fill factor can be presented as the light-grey square box below the J-V curve [12].

Various factors influence the losses which accumulate throughout the solar cells, section 1.2 will discuss the types of losses.

1.2. Solar cell power loss mechanisms

In order to further increase the performance of solar cells while approaching the maximum theoretical efficiency it is important to minimize the losses. When analyzing the loss mechanisms occurring in the semiconductor material they can be categorized in two groups: optical losses and electrical losses. Section 1.2.1 discusses the optical losses and section 1.2.2 the electrical losses. Section 1.2.3 introduces another source of recombination which is that between the semiconductor material and the metal contacts.

1.2.1. Optical losses

Optical losses affect the power generated by the solar cell by lowering the short-circuit current. The short-circuit current, usually written as I_{sc}, is the largest possible current that a solar cell can reach. The optical losses influence this property because light can reflect from the solar cell surface. The photons, of which the light consists, will not participate in the potential excitation of electrons from the valance band into the conduction band. There are solutions to reducing the reflection incident on the solar cell

surface, such as the inclusion of an ARC and texturing the semiconductor surface. An ARC is a small dielectric material deposited on top of the semiconductor surface as a thin layer with a specific thickness. The ARC ensures that light reflected from the surface is minimized. The theory is that the presence of a double interface from the ARC can produce two reflected waves, one from the ARC coating and one from the ARC/c-Si interface, these waves are out of phases with each other and this results in destructive interference [13]. This means that the waves can partially or totally cancel each other out. A single layer ARC can often reduce the majority of the reflections, and an ARC consisting of multiple layers can improve the effectiveness even further.

Surface texturing is a common technique for solar cell fabrication by which the surface morphology is changed. If the surface is flat then it is easy for light to reflect away from the surface, a textured surface introduces the possibility for light reflected away from the surface to interact with the surface at another location. The texturing can be performed by etching along the crystal planes of the c-Si lattice, the surface morphology changes to randomized pyramids in the order of microns. Figure 1.5 shows an example of the pyramids. Having light interact with multiple surfaces of the c-Si will improve that chance that light passes into the semiconductor, rather than reflect away from it.

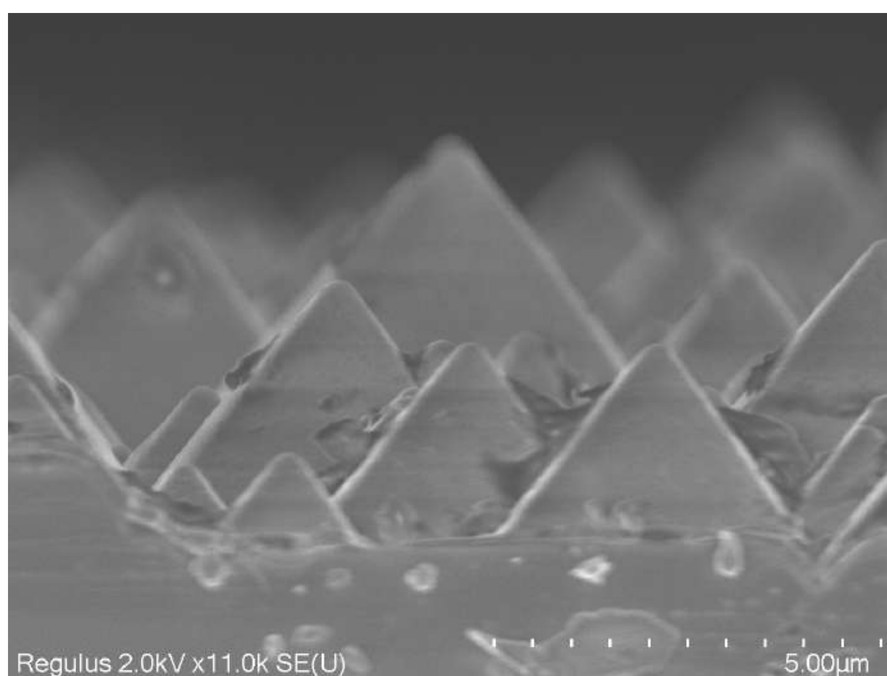

Figure 1.5: Side-view of randomized pyramids on a c-Si surface, image taken using the SEM.

Not all of the photons that are absorbed by the semiconductor material contribute to the attainable photocurrent, and this loss mechanism is referred to as parasitic absorption. All the layers present in the solar cell structure are potential sources of parasitic absorption [14]. This is especially relevant for photons in the infrared (IR) wavelength range which spans from 780 nm upwards. The IR photons that do not leave the semiconductor material contribute to heating up the temperature of the cell and this phenomenon needs to be minimized.

Shading is separate mechanism leading to a lower efficiency, this is caused by the front side metallization. The inevitable collection of charge carriers requires a portion of the surface area to be deposited with conductive material for the collection. The magnitude of the shading loss is proportional to the metallization surface area and affects the performance for all wavelengths.

Transmission of photons present another challenge for reducing the optical losses, and any photon not being absorbed by the absorber layer is undesirable. At IR wavelengths the photons will not have

enough energy to interact with the semiconductor material and excite an electron. The relationship between the energy (E) of an electron and the wavelength is given by equation 1.4.

$$E = \frac{h * c}{\lambda} \tag{1.4}$$

where h is the Plank constant, c the speed of light *in vacuo* and λ the wavelength.

Making the rear surface reflective can increase the path length of photons present in the cell, thus having a higher chance of absorption. Figure 1.6 shows over the relevant solar cell wavelength range the various contributions to the current loss [15].

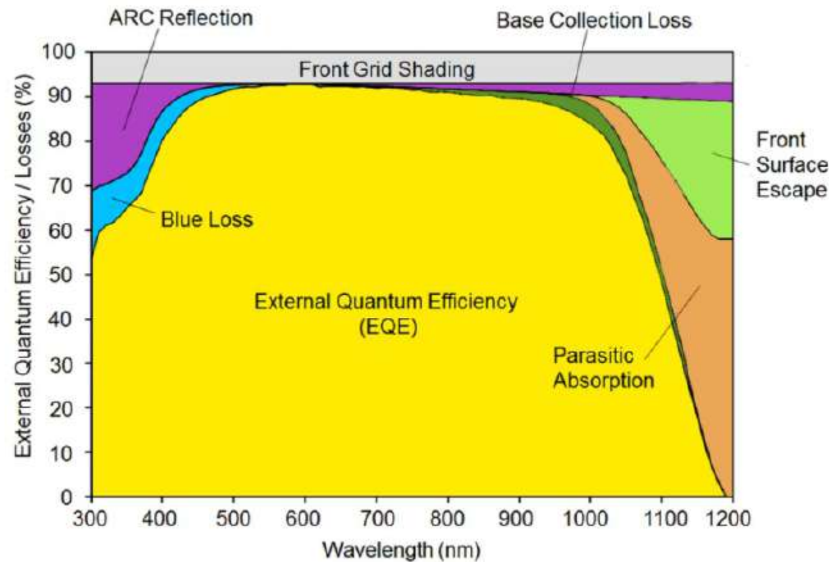

Figure 1.6: EQE spectrum dependent analysis of photon losses of a pyramid-textured solar cell. Adapted from [16].

1.2.2. Electrical losses

Once an electron-hole pair is generated they are able to recombine, this mechanism is referred to as recombination. Recombination is a process by which the electron interacts with a hole and reverts back to its original state [17]. The rate of recombination plays a key role in the performance of solar cells. There are three basic types of recombination that can occur in the bulk of the semiconductor material, there are:

- Radiative recombination. This is a recombination mechanism dominant in direct bandgap semiconductors. A direct bandgap signifies that a the highest point of the valence band is aligned with the lowest point in the conduction band. The alternate indirect bandgap will have a misalignment between these two points, and this will require an excited electron to have a momentum provided from the vibrations of the crystal lattice. Silicon happens to be an indirect bandgap material, this limits this type of recombination and can be considered negligible. During this recombination an electron in the conduction band recombines with a hole in the valence band.
- Auger recombination. This is an important recombination mechanism for indirect bandgap material. Auger recombination is a process which involves three particles, the momentum and energy of a recombining electron-hole pair is transferred to another hole or electron. If an electron received the transferred energy and momentum it excites into a higher level in the conduction band. For a hole, it excites into a deeper level of the valence band. This third particle will eventually transfer the energy in the form of heat. Auger recombination limits the lifetime of the charge carriers and thus the efficiency.
- Shockley-Read-Hall (SRH) recombination. SRH recombination is facilitated by an impurity atom or lattice defects, and these elements can introduce trap states. Electrons that are excited to the

conduction band can be trapped at the defects expedited by the trap states and subsequently recombine. This recombination mechanisms is the most dominant process in semiconductors. The energy released from the recombination is also in the form of heat. Figure 1.7 shows a visual representation of all the recombination mechanisms.

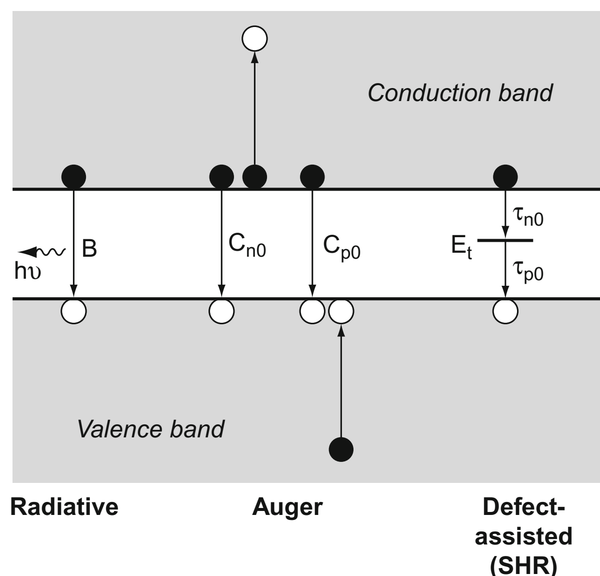

Figure 1.7: Schematic diagram of the three recombination processes in semiconductors, the direction of arrows indicates electron transitions [18].

A parameter indicative of the recombination between electrons and holes is the saturation current density J_0. This parameters depends on fundamental semiconductor parameters, ideally this parameter is as low as possible [11]. J_0 is able to express the charge carrier recombination in both equilibrium and under external illumination [19].

The surface of the semiconductor material also participates in defect-assisted recombination, the abrupt discontinuation of the crystal lattice introduces dangling bonds. Dangling bonds are unpaired electrons at the surface and are essentially trap states which will induce the SRH recombination. The recombination at the dangling bonds is very high, and a technique for reducing the recombination at the surface is by passivation. Passivation implies that a thin layer of material is deposited which can form a bond with the dangling bonds. These new bonds result in a lower trap state density and reduce the recombination. Section 1.3 will go into more detail regarding the passivation.

1.2.3. Metal-induced recombination

Significant recombination can occur between the semiconductor and metal contact interface. During the application of the metal contacts a so-called firing step is included which allow the contacts to form. This process occurs at higher temperatures which causes metal to penetrate the diffused doping region and depassivates the interface [20]. Properties of the metals used for the contacts can also result in a sub-optimal work function difference at the interface, resulting in an increased minority carrier concentration.

1.3. Passivating contacts

Quenching the surface recombination can be achieved reducing the surface defect density. Chemical passivation by applying an ultra-thin layer of SiO_2 or a-SiO_x:H will form either Si-O or Si-H bonds, respectively [21, 22]. These bonds will saturate the surface and passivate the dangling bonds. Layers such as these two can be deposited through a chemical vapor deposition (CVD), during this process

the surface reacts with gasses brought at an elevated temperature. Alternative means for applying an ultra-thin layer of SiO_x is through nitric acid oxidation of silicon (NAOS) [23]. In this process the layer is grown by the immersion of the silicon substrate in a high concentration of nitric acid (HNO_3).

Electric field passivation is an alternate method to achieve passivation; this process involves electrostatically shielding the charge carriers from the interface by an internal electric field [24]. Putting a barrier in place is how this can be achieved. This barrier is formed by a placing a highly doped region beneath the surface. For both methods of passivation the ultimate goal is to reduce the surface recombination velocity (S_r). Equation 1.5 shows how this parameter can be defined:

$$S_r = v_{th} * \sigma_{p/n} * N_{sT} \tag{1.5}$$

where v_{th} is the thermal velocity in cm/s, σ is the capture cross section in cm^2 and N_{sT} the surface trap density in cm^{-2}. The lower this value is, the lower the recombination.

The limiting factor for solar cell efficiency is due to the effectiveness of photogenerated carriers collection at the metal contacts [25, 26]. An additional material positioned between the semiconductor and metal can reduce area of direct contact, and this is facilitated by local contacts. Local contacts can be found in structures such as the passivated emitter and rear cells (PERC) and passivated emitter locally diffused cells (PERL) [27]. Figure 1.8 shows how these structures are built with the local contacts, with the local contact shown in green. This local contact is a doped area which reduces the minority carrier density by reducing the equilibrium concentration of minority charge carriers caused by the doping concentration thus resulting in a difference in chemical potential with respect to the c-Si bulk [28]. Furthermore the minority carrier mobility is also reduced [29]. The consequence of adding local contacts to the structure is an increase in processing complexity, and a compromise between the V_{oc} and FF due to an increase in ohmic losses [30].

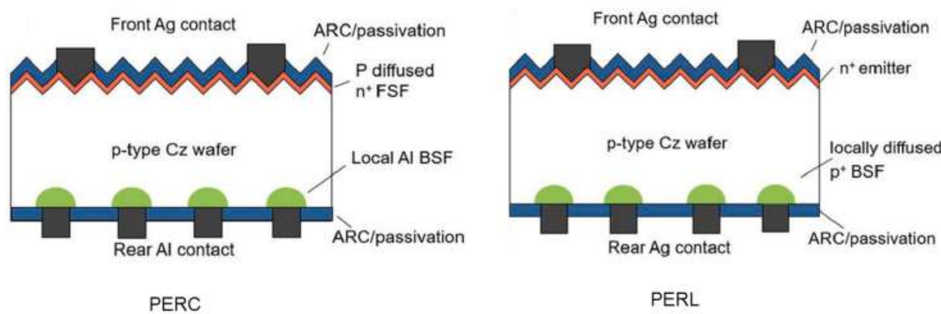

Figure 1.8: Schematic side view of the PERC and PERL solar cell structure [27].

1.3.1. Local poly-SiO_x passivating contacts

A specific material used for the local contacts is doped polycrystalline silicon (poly-SiO_x) [31]. The doped poly-SiO_x is the material which facilitates the carrier selectivity. Poly-SiO_x can be fabricated by depositing the surface with hydrogenated amorphous silicon (a-SiO_x:H) and subsequently performing an annealing process which converts the a-SiO_x:H to poly-SiO_x via solid-phase crystallization (SPC) [32]. The doped poly-SiO_x can be used to form a connection with a metal contact to extract the charge carriers. In combination with a chemical passivation by ultra-thin SiO_x and a metal contact, a passivating contact can be created. This manner of contact has already been implemented in tunnel oxide passivated contact (TOPCon) structures. Figure 1.9 shows a TOPCon stricture featuring a full tunnel oxide passivated rear contact and a diffused p^+ boron doped emitter.

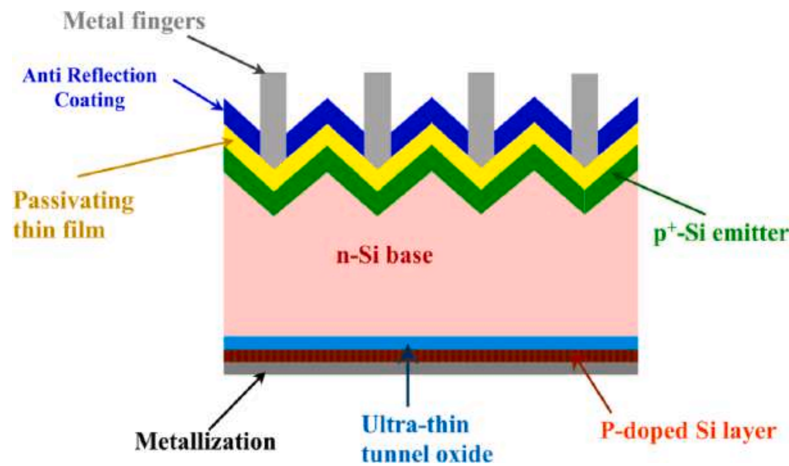

Figure 1.9: Schematic structure of a TOPCon solar cell [33].

1.4. Motivation and objectives

A shortcoming of using full-area poly-SiO$_x$ for the carrier-selective contacts is the increase of parasitic absorption losses [34]. In the TOPCon structure shown in figure 1.9 the poly-SiO$_x$ layer is placed at the rear side, this induces much less parasitic absorption losses resulting in a higher overall J_{sc}. In this project the poly-SiO$_x$ will be applied on the front surface of a TOPCon structure solar cell, however to prevent the photo generated current loss induced by the parasitic absorption losses it will only be applied locally. The locally applied doped poly-SiO$_x$ will function as a carrier-selective contact. One approach for the local contact deposition is using a hard mask to deposit doped a-SiO$_x$:H through specified openings [35]. During a deposition process this mask will allocate the positions where the a-SiO$_x$:H may be deposited on the semiconductor substrate. In order to fabricate local passivating contacts solar cells the poly-SiO$_x$ finger through the hard mask will have to be investigated. Furthermore applying all the necessary layers for a TOPCon structure needs to be optimized in order to properly function with the local carrier-selective contacts. The research questions that are posed for this project are:

- How do the PECVD deposition conditions affect the local poly-SiO$_x$ fingers formation through a hard mask?
- What is the influence when tuning the process parameters on the surface passivation of textured p$^+$ diffused c-Si and local poly-SiO$_x$ fingers?
- Can a flowchart be created for poly-SiO$_x$ finger solar cell fabrication?

1.5. Thesis outline

The report is structured in six chapters. Chapter 1 contains an introduction to solar cells and a description of the recombination that can occur, as well as introducing the passivating contacts. In chapter 2 all the necessary equipment and techniques that are required to make the eventual local poly-SiO$_x$ solar cells are described and explained. This chapter also introduces the equipment used to analyze the performance of the fabricated solar cells and its precursors. Chapter 3 focuses on the method to fabricate the local poly-SiO$_x$, first discussing how to make the hard mask and subsequently how to optimize the depositions that are applied by implementing the hard mask. In chapter 4 the experimental procedures for the surface passivation are described and analyzed, with a section dedicated to the doping profile of the c-Si precursor. Chapter 5 discusses the fabrication of the local carrier-selective solar cells, followed by the measured performance of the finalized local poly-SiO$_x$ carrier-selective solar cells and gives an explanation for the power loss that was measured. Conclusions and recommendations for a follow-up project are finally presented in chapter 6.

2
Experimental method

This chapter discusses equipment located in the EKL, Kavli and ESP lab that allows for either fabricating parts or defining the quality of applied features of the local poly-SiO_x solar cells. Section 2.1 explains how to go from a semiconductor to a functional solar cell, section 2.2 introduces equipment used to analyze the poly-SiO_x solar cells at various steps in the overall process. In section 2.3 a technique to map the concentration of dopants is briefly introduced.

2.1. Equipment for the fabrication of local poly-SiO_x solar cells

2.1.1. Laser cutter

The ability to create any shape out of a c-Si substrate is provided by the laser cutter. This machine allows the user to draw shapes in the software which it will trace in the chamber containing the c-Si substrate. Unconventional shapes can be cut to the standard 4-inch wafer size. A single trace of the shape with the laser will never be sufficient to cut the c-Si substrate, the shape is always looped several times. The cutting speed and power may also be changed to optimize the process. Generally the best cuts and sharpest edges are obtained when the speed of the laser is at least 200 mm/sec and looped for 100 cycles. If the thickness of the substrate increases then the number of loops will have to be increased proportionally. Between each cutting process the chamber requires cleaning to remove any shards that broke off from the surface. Figure 2.1 shows the chamber is where the wafers are positioned below the laser, on the top and right side of the wafer are extrusions in the chamber's table. Positioning the wafer against both these reference points provides the functionality to produce repeatable results.

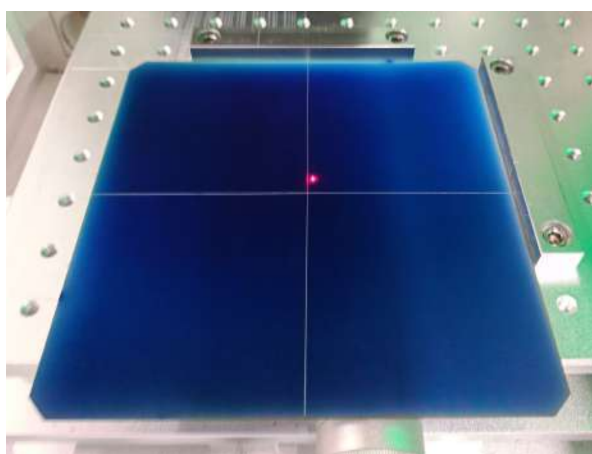

Figure 2.1: Process of a large square wafer being laser cut into four smaller wafers.

2.1.2. RCA cleaning

Contamination is a significant issue for silicon wafers during solar cells manufacturing. Any contaminant, whether it is organic or inorganic, can reduce the performance of the eventual solar cell. Thankfully a cleaning process can be carried out which will get rid of the majority of the contaminants when performed correctly, and subsequently apply a thin protective layer on the semiconductor surface. This cleaning process is called RCA cleaning and it consists of two steps [36]:

RCA 1

First is the RCA 1 cleaning process, the purpose of RCA 1 is to remove organic contamination and particles for the c-Si surface. RCA 1 requires a solution consisting of deionized water, ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) heated up to a temperature of 70 °C. Prior to submerging the wafers that need to be cleaned, a rinsing bath in deionized water is required. Another bath is vital for a successful cleaning process, which is a bath for a so-called hydrogen fluoride (HF) dip. This bath consists of mostly deionized water and a small concentration of HF. The purpose of the HF dip is to remove native oxide which naturally grows on the semiconductor surface. A concentration of 0.55 % should be enough when performing the HF dip for a single minute. It should be apparent if the HF dip is successful, because when the silicon wafers are removed from the bath the surface should be hydrophobic. For safety reasons and to prevent the unwanted and potentially dangerous mixture of chemicals, a rinsing step is obligated between every soaking process. When all solutions are prepared and at the proper temperature, the order of the RCA 1 is as follows:

1. Rinse for 5 minutes in deionized water
2. HF dip for at least 1 minute
3. Rinse for 5 minutes in deionized water
4. RCA 1 bath for 10 minutes
5. Rinse for 5 minutes in deionized water

The result is a surface free of organic particles and a thin oxide on the surface of the wafer.

RCA 2

Second is the RCA 2 cleaning process, this is a further cleaning step and is a procedure for removing metal ions from the silicon wafer surface. A slightly different combination of chemicals is used for RCA 2. This solution also consists of deionized water and hydrogen peroxide, but additionally uses hydrochloric acid (HCl) heated up to a temperature of 80 °C. For RCA 2 the hydrogen peroxide is added after the solution has reached the required temperature. This is because the solution becomes active after the hydrogen peroxide is mied into the solution and only is effective for no longer than 30 minutes. Given the waiting time required for the solution to reach 80 °C, it would be ineffective to add the hydrogen peroxide prior. The order of the RCA 2 is as follows:

1. Rinse for 5 minutes in deionized water
2. HF dip for at least 1 minute
3. Rinse for 5 minutes in deionized water
4. RCA 2 bath for 10 minutes
5. Rinse for 5 minutes in deionized water

The result when performing these steps is clean wafers free of contamination that would hinder the solar cell performance. RCA cleaning is performed in the wet bench located in the EKL C10000. Appliances that provide the chemical baths with heat to increase the temperature are the built-in sink and hotplate. The built-in sink provides heat via bain-marie, which is a heated bath used to gently heat up the chemical bath. The RCA bath is placed in a room-temperature water bath, heat is then supplied to the water bath and is transferred to the RCA bath. When using the hotplate to heat the RCA bath, heat is directly supplied to the bottom of the RCA bath.

2.1.3. Local doped poly-SiO_xOx formation

To create the doped poly-SiO_x two processes will have to be used: plasma-enhanced chemical vapor deposition (PECVD) and annealing. PECVD deposits materials based on predefined gases, these react with electrodes in a deposition chamber which creates a plasma. Figure 2.2 depicts the working principle for PECVD. The PECVD has many degrees of freedom when performing depositions, such as temperature and deposition power [37]. The PECVD is performed using the AMOR located in the EKL C10000. The AMOR contains several chambers that are hooked up to particular gasses, some chambers can only be used to deposit n-type material while another chamber can only deposit p-type. The chambers are kept at a constant temperature of approximately 180 °C. Singular substrates are positioned inside of a holder, the substrate is clamped in the holder to prevent it from falling in the machine. The hard mask and a substrate can be positioned in the same holder for a hard mask deposition. Inserting a substrate in any chamber requires the use of a load-lock capable of pumping down to a low pressure environment in the AMOR. The chambers in the AMOR can remain at a low pressure environment while the load-lock is able to be brought to atmospheric pressure for inserting the holders. A robotic arm facilitates the movement of the holder to any of the chambers. It is not possible to perform a deposition for more than one wafer at a time, making the PECVD quite time-intensive. Using a combination of silane (SiH_4), hydrogen and boron, the doped a-SiO_x:H can be deposited. Holders that are removed from the AMOR will first have to cool down for further processing.

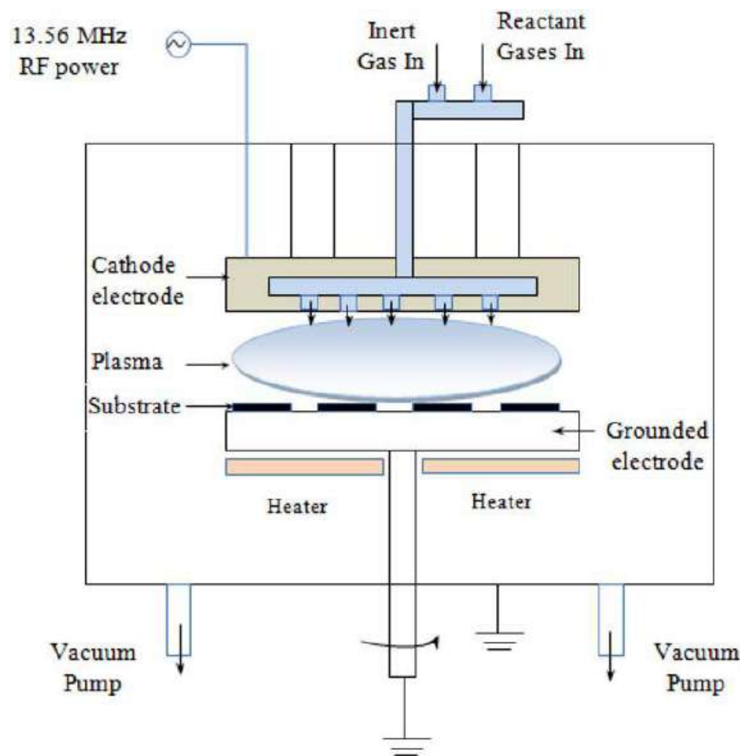

Figure 2.2: Schematic representation of the working principle of a PECVD reactor [38].

Annealing is the process which transfers the doped a-SiO_x:H to the poly-SiO_x [39]. The annealing process takes place in a furnace located in the EKL C100. Samples are placed in a holder located in the furnace tube. With the samples in place the tube retracts into the furnace and is heated up to the required annealing temperature. Once this temperature is reached it remains there for a specified duration before cooling down. Annealing temperatures for poly-SiO_x are between 800 °C and 1100 °C, too high annealing temperatures results in the interfacial oxide from the chemical passivation deteriorating leading to higher recombination characteristics [31]. An example of the progress from an intrinsic semiconductor material to a single side doped semiconductor is shown in figure 2.3.

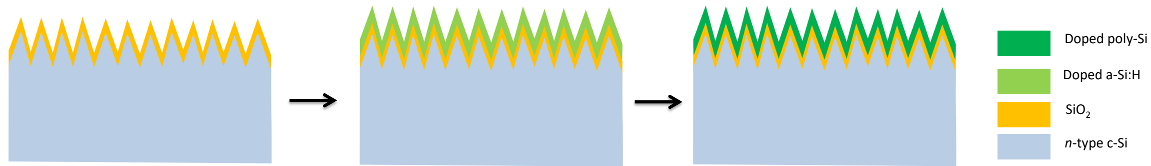

Figure 2.3: Schematic structures the progression of a chemical passivated precursor, to PECVD deposited a-SiO_x:H, to annealed doped poly-SiO_x.

2.1.4. Atomic Layer Deposition

An essential layer when fabricating poly-SiO_x passivating contacts is a hydrogen-rich capping layer, Al_2O_3 is such a layer. Al_2O_3 functions as a reservoir for hydrogen. Performing an annealing step after Al_2O_3 has been deposited on p^+ poly-SiO_x and the Si/SiOx interface will provide this hydrogen to the layers below the Al_2O_3 [40]. Atomic layer deposition (ALD) is a suitable method to provide the c-Si surface of Al_2O_3. ALD can produce thin films of atomic-scale precision with the ability to modify the film thickness and the material composition with wonderful conformity [41]. The ALD is a sequential process, this means that multiple reactants do not interact with the surface simultaneously. The reactants, the so-called precursors, interact with the surface in non-overlapping pulses. The process is visualized in figure 2.5. The precursors used for the Al_2O_3 are $Al(CH_3)_3$, also known as Trimethylaluminium or simply abbreviated as TMA, and water. A purge of TMA enters the chamber containing the sample in a low-pressure environment, then the TMA is brought into contact with the surface's dangling bonds. The TMA reacts with the dangling bonds, this is a self-limiting reaction because when the number of free dangling bonds decrease the TMA doesn't react. The excess TMA is purged from the chamber, afterwards a purge of water enters the chamber and reacts with the methyl group (CH_3) of the TMA, the result are new OH bonds capable of reacting with a subsequent TMA purge. This process repeats for a predefined number of cycles. The higher the number cycles, the thicker the Al_2O_3 will become. Figure illustrates the ALD deposition on a p^+ diffused emitter wafer. The ALD was performed using the ALD Oxford located in the Kavli Nanolab. The process in the ALD Oxford takes place at 105 °C at a pressure of approximately 3.00^{-6} Torr. The ALD Oxford is a temporal ALD, this implies that the position of sample onto which the ALD will deposit is fixed [42]. The alternative to this is a spatial ALD. The spatial variant ALD has a constant supply of precursors going to separate chambers, providing a constant deposition rate.

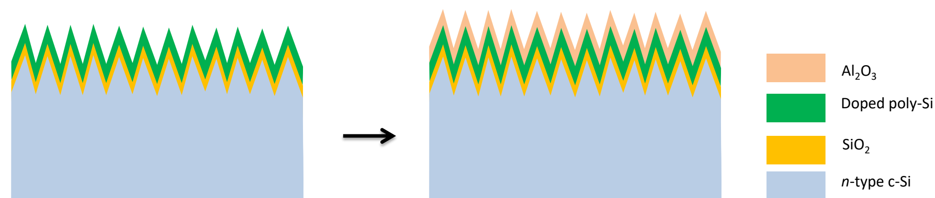

Figure 2.4: Schematic structures the progression of a single side doped sample to a ALD deposited passivated sample.

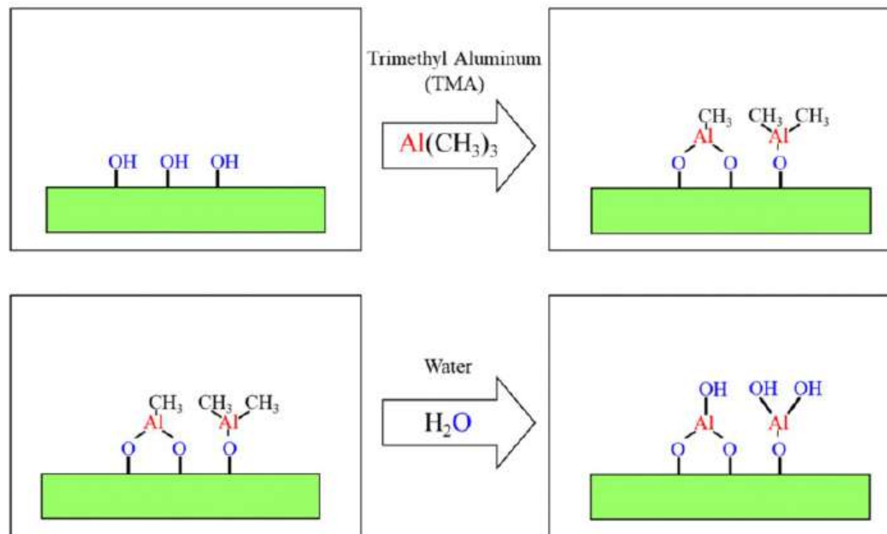

Figure 2.5: Schematic representation of the ALD cycle [43].

2.1.5. ARC application

The topmost layer of the solar cell will function as an ARC to promote the optical performance, a typical material using for this application is SiN_x. SiN_x is a dielectric material which can cause destructive interference, it typically is deposited using PECVD [44]. The machine used for the SiN_x deposition is the Plasmalab80+ located in the Kavli Nanolab[45]. This machine is capable of depositing on multiple wafers at a high wafer loading and unloading rate with an accurate control of deposition. Wafers are placed on a heating table which is at 400 °C. The chamber lid is brought down and the machine is pumped down to perform the deposition in a low pressure environment. Once the proper pressure is achieved a preheating step fill the chamber with nitrogen for a single minute. For the deposition two extra gases are added into the chamber: silane (SiH_4) and ammonia (NH_3). Once the power is turned on the plasma is created between electrodes present in the chamber and the deposition begins. The specified amount of time determines the thickness of the deposited layer. Uniformity is lower when samples are positioned near the edge of the chamber where the distance to the electrodes are the highest, it is important to place the wafers as close to the center of the table without overlapping each other. Following a successful deposition, the chamber is pumped down to remove any excess gases for one minute. The chamber is finally brought back to atmospheric pressure so that the chamber may be opened and the wafers removed. Figure 2.7 shows how this deposition is performed.

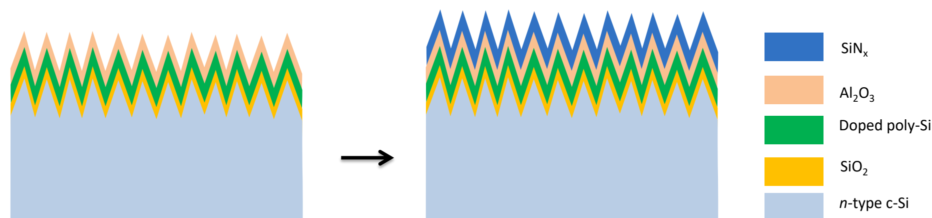

Figure 2.6: Schematic structures the progression of a single side doped ALD passivated sample to a single side doped passivated ARC protected sample.

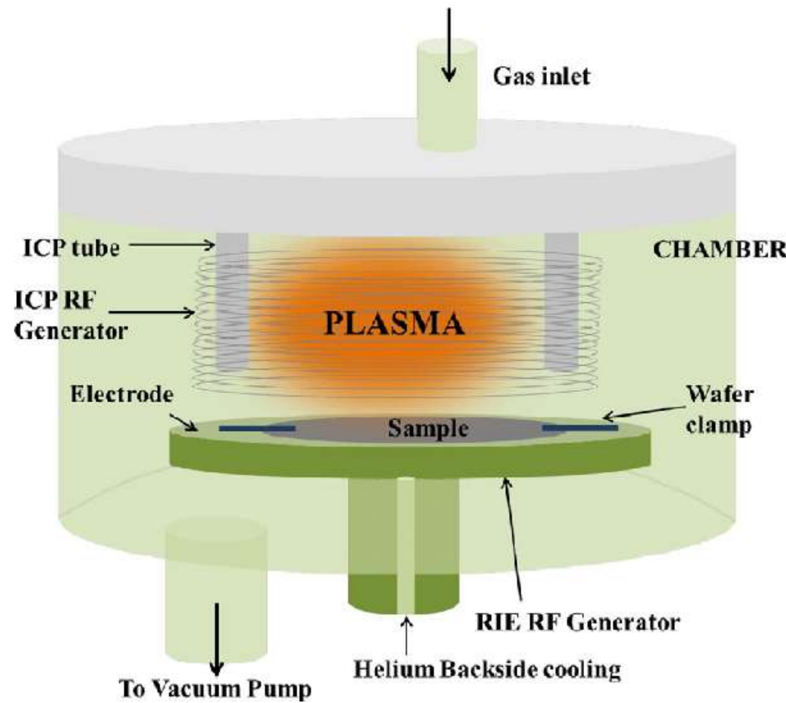

Figure 2.7: Schematic representation of the SiN_x PECVD deposition [46].

2.1.6. Metallization

Collecting the charge carriers is the final step for the solar cell design, this step involves the localized application of a metal on the semiconductor. The metallization is applied on both sides of the semiconductor. Two possible methods are available for the metal formation: thermal evaporation and E-beam evaporation. For both methods the wafers are present in a low pressure environment placed in a rotating holder. This holder typically rotates at a rotation speed of 20 rpm, its purpose being to improve the uniformity of the deposited metal. Thermal evaporation is achieved by having the metal heated up to a sufficient temperature to for it to start vaporizing. The heating process is provided by having the container in which the metal is placed receiving a high current, resulting in the temperature of the container to rise. The vapor will condense on the wafer substrate to form a high purity metallic layer [47]. E-beam evaporation uses a high energy electron beam to heat up the metal. Metal from the container will evaporate if the electrons from the beam provide enough energy [48]. Figure 2.8 visualizes both these techniques. The Provac PRO500S in the EKL C10000 is capable both metallization processes [49].

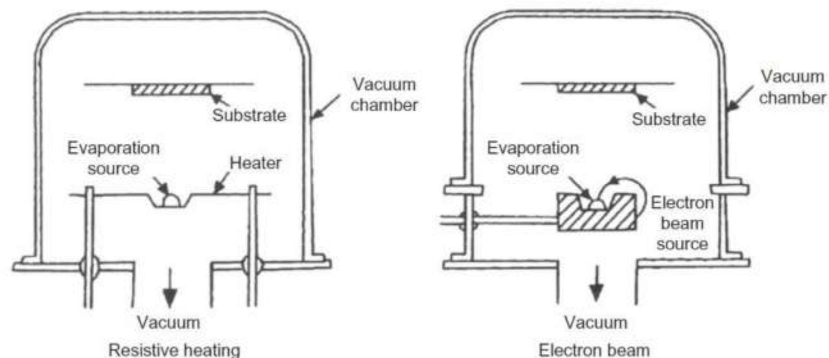

Figure 2.8: schematic drawing for the metallization processes, left image is thermal evaporation and right image is E-beam evaporation [50].

2.1.7. Forming gas annealing

Forming gas annealing (FGA) is an additional annealing process that is performed following the metallization. Not only is the FGA capable of providing the semiconductor surface with hydrogen to passivate the dangling bonds, it can also supply the bulk with hydrogen to fill voids caused by hydrogen abstraction, plus it can also activate the metal contacts to lower the specific contact resistance [51, 52]. The FGA is performed in a furnace located in the Kavli Nanolab. Forming gas is a mixture of primarily nitrogen with a smaller concentration of hydrogen. The annealing is performed at 400 °C for 30 minutes.

2.1.8. Rapid thermal processing

The usage of rapid thermal annealing (RTA) is implemented during the optimization for the passivation layers, specifically the influence on the Al_2O_3 layers deposited through ALD. Thermal treatments at higher temperatures ($\approx$ 800 °C) have shown to sometimes improve the surface passivation quality [53]. The possibility for a degradation in passivation quality might also occur following RTA. Al_2O_3 passivation layers may not always improve or degrade progressively with an increase in annealing temperatures. To investigate the implementation of the RTA the SSI Solaris located in the Kavli Nanolab is used [54]. This machine is capable of reaching the high temperatures required for the RTA in less than a minute, once the required temperature is reached it remains there briefly before reverting to lower temperatures. Recipes have to be optimized by changing the parameters of the PID controller, these parameters define the ramping speed and time of the temperature increase. Without the optimization process the preferred temperatures are easily overshot leading to excessive annealing temperatures. The heat is supplied by a lamp positioned above the sample inserted in the annealing chamber, only a single wafer can be processed per RTA recipe. Depending on the preferences for the gases supplied to the annealing chamber, either a pure nitrogen or a forming gas environment is present during RTA. Figure 2.9 shows how the RTA is performed.

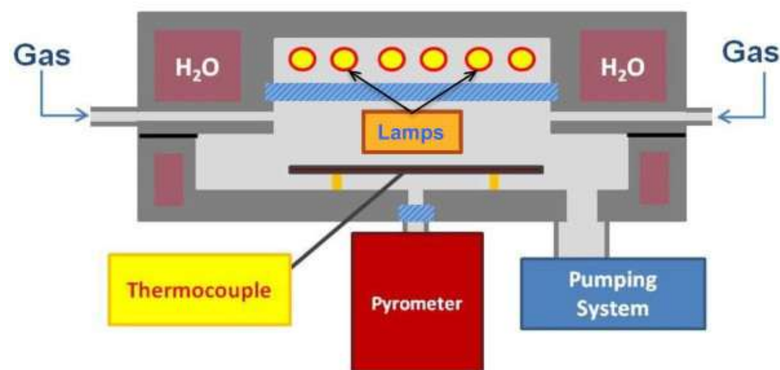

Figure 2.9: Schematic overview of the RTA system [55].

2.1.9. Photolithography

Patterning is an important process step for the fabrication of solar cells, lithography is the process which facilitates the patterning process. Lithography is an photographic process during which a light sensitive polymer, referred to as a photoresist (PR), is exposed to ultraviolet light through a photoresist mask creating a structure on the substrate. Ideally the photoresist which remains after the exposure will replicate the pattern that is present in the mask on the exposed substrate. Afterwards an etching process might be implemented which will remove some of the material not exposed to the photoresist, since this now acts as a protection layer. Two types of photoresist can be used for the lithography: positive photoresist and negative photoresist. The difference between these two types is how they interact with the ultraviolet light; positive photoresist will disappear after the exposure and negative photoresist will remain after the exposure. Figure 2.10 shows the difference between the two processes.

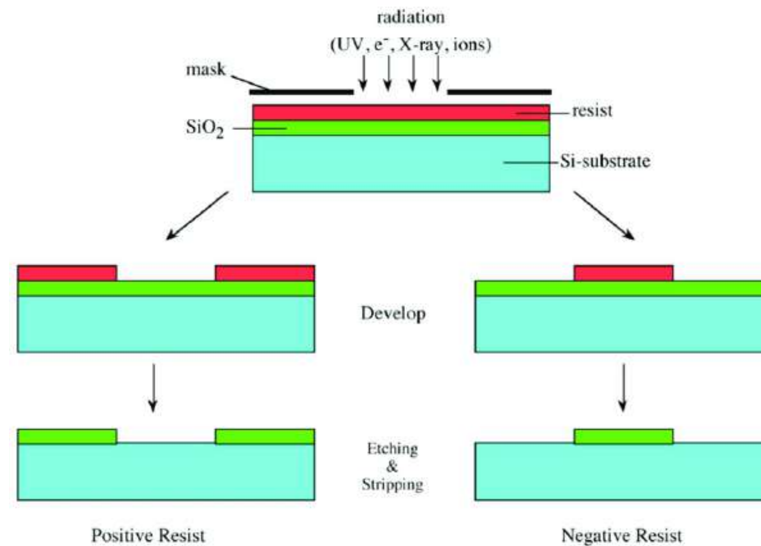

Figure 2.10: Lithography process showing the difference between positive and negative photoresist [56].

The lithography process as a whole consists of several steps to properly create structures with the photoresist, these include:

1. **Photoresist coating**. The photoresist comes as a liquid, in order to uniformly apply it to the substrate surface spin-coating is utilized. A wafer is positioned on a turntable which uses a vacuum to keep it in place. Due to the vacuum the turntable is able to reach high RPMs while keeping the wafer centered. This is important if a photoresist has a high viscosity. Depending on the photoresist viscosity, spin duration and spin speed the thickness of the photoresist can be optimized. The substrate morphology also plays a role since flat and textured surfaces do not interact the same with the coating. Coatings are applied in the polymer lab in the EKL C100.
2. **Post-coating softbake**. The photoresist will contain solvent which helps with the coating, once the coating is applied this solvent has to be removed. A baking process in either an oven or on top of a hotplate removes the solvent by evaporation, changing the properties of the coating and improving the quality. This process also has to be optimized, excessive baking time or baking temperatures may cause the photoresist to decompose. If the wafers are a standard size and do not contain any features that will negatively affect the vacuum suction then the coating and baking can be automated, if the wafers are of an unconventional size it has to be performed manually.
3. **Exposure**. During the exposure step the photoresist coated substrate is subjected to ultraviolet light for a predefined duration with a mask separating the substrate and the light. A mask is a square glass pane with a pattern design on it which stops the light from reaching the substrate. To ensure a good exposure the substrate and the mask have to be aligned. If no pattern is present on the substrate centering the wafer to the mask is the priority, however some wafers might already have patterns from previous lithographic processes. Most masks will contain markers, which are small objects in the order of a few hundred micron. These markers will have to be matched to each other to ensure a good alignment of the mask's features. This is a critical step in the lithography process since bad alignment could lead to a poor solar cell performance. The exposure will generally take second, thicker coating require a higher exposure time to fully imbue to pattern of the mask onto the coating. For all exposures the SUSS MicroTec MA/BA8 mask aligner located in the EKL C100 is used [57].
4. **Post-exposure bake**. A post-exposure bake will increase the quality of the pattern now present in the coating. The purpose of this baking step is to smoothen out the pattern created by the exposure. Without this baking step the structures formed from the resist will have irregular sidewall leading to a decrease of pattern accuracy. This baking step is usually done using the a small convection oven [58].
5. **Development**. The development process is the final step of the lithography process, during this step the pattern will become visible through removing part of the photoresist. For positive

photoresist the exposed area will be removed, for negative photoresist the unexposed area will be removed. This is achieved by pouring a developer solution on the photoresist, the developer is an aqueous base such as Tetramethylammoniumhydroxide (TMAH). After the pattern is clearly visible the wafer is rinsed with water and dried.

Following a successful application of a lithography pattern on a substrate an etching step usually follows. This etching step consists of the wafer being submerged into a chemical that reacts with the area not protected by the photoresist. This will etch the pattern from the lithography mask into the substrate. Finally the photoresist coating has to be removed. For positive photoresist acetone can be used, negative photoresist is more resilient to acetone and requires something stronger such as N-methylpyrrolidon (NMP).

2.2. Characterization

2.2.1. Surface morphology

During the process of fabricating solar cells, numerous layers are applied on top of each other. It is important to measure the performance and quality of each layer whenever possible, however being able to visually inspect a layer is tremendously helpful. Section 2.2.1 will explain some equipment that has been used to observe layers applied on c-Si surface.

Dektak 8

The Dektak 8 [59] is a stylus profilometer, it analyzes topographical data of a pre-defined surface section. The deposited materials on the c-Si surface will have a particular height that can be calculated or approximated prior to the deposition based on the process parameters, this devices allows to investigate the height afterwards. A silicon wafer is loaded onto the sample stage and locked in position using a vacuum on the rear surface side. Once the stage has moved in position beneath the stylus, the stylus descends towards the wafer and halting before making contact. A camera is attached to the stylus which gives visual support when allocating the portion of the wafer that should be investigated. A path length and sample steps can be assigned to the stylus, once the measurement starts the stylus will initiate contact with the wafer and move in a horizontal direction along the wafer taking a topographic measurement for each sample step. The stylus ensures that a scratch-free analysis is performed. A cross-sectional profile of the surface is generated in real-time, the resulting data can be exported to the preferred file type. Based on the step size and the assigned time for the measurement, the measurement can reach a high degree of detail. Figure 2.11 visualizes how the Dektak 8 performs the morphology measurements.

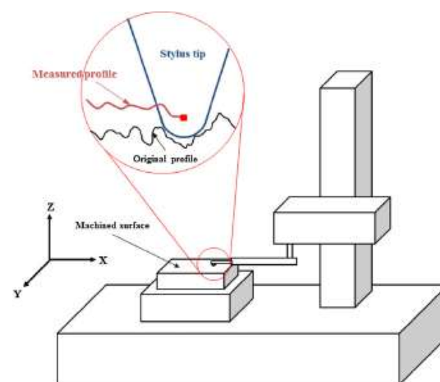

Figure 2.11: Schematic illustration of the working principle of a stylus-type profilometer[60].

Optical microscope

The advantage of using an optical microscope is that small details otherwise invisible to the naked eye can be observed quick and with relative ease. During processes which involve lithography the microscope is especially useful since it shows if alignment has been performed successfully. The optical microscopes situated in the EKL also allows for images to be taken of the samples, measurements of

features can also be performed. Several lenses are available to cycle through to find the most suitable magnification for the observed sample, with the resolution reaching magnitudes of up to 200 times. Figure 2.12 shows the basic principle of the optical microscope.

Scanning electron microscope

The fabrication of solar cells on semiconductors is a process that focuses on a small scale, occasionally on a nano-scale level. To study how a certain fabrication technique affects the semiconductor a tool is required that can properly characterize and visualize the structure on said level. A scanning electron microscope (SEM) is a powerful microscope that offers all these capabilities. The specific SEM used in the EKL is called a Hitachi Regulus 8230 [61]. The SEM works by firing a beam of electrons at a specimen, these electrons interact with the sample, reflect from the sample and subsequently are collected by detectors. Through the information of these detectors an image is generated on the screen. Based on the surface topology of the wafer the differences in surface heights, materials and textures should be able to be identified. The samples will not be damaged or deformed by the beam. Figure 2.13 illustrates the working principle of the SEM.

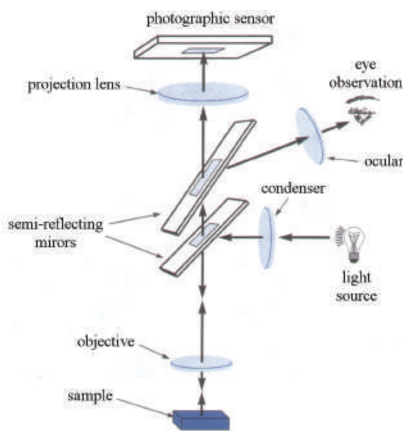

Figure 2.12: Schematic illustration of the working principle of an optical microscope [62].

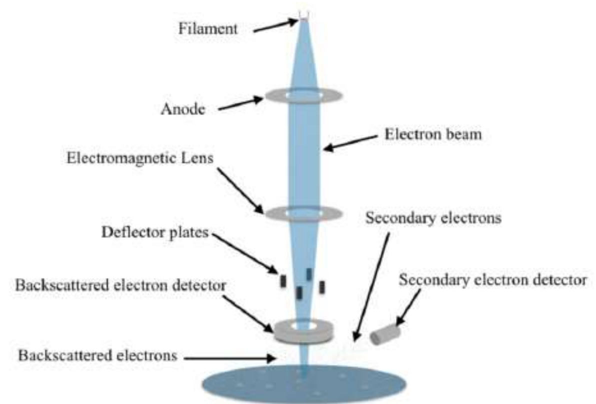

Figure 2.13: Schematic illustration of the working principle of a scanning electron microscope [63].

2.2.2. Solar cell performance

To express the performance of the test samples and the solar cells, several tools are used that can characterize the operation. The following section will introduce and explain the tools used for this purpose.

Photoconductance decay of carrier lifetimes

Being able to measure the passivation quality is essential when optimizing the solar cell, this can be achieved by measuring the wafer minority carrier lifetime. A device which provides this measurement is the Sinton WCT-120 lifetime test instrument [64]. This device uses an eddy-current conductance sensor and a filtered xenon flash lamp to measure the carrier lifetime. Figure 2.14 shows an example of a Sinton setup. Under illumination, the excess carrier density is calculated from the conductivity of the sample [65]. As input it requires the wafer thickness, resistivity, doping type and an optical constant based on the top layer of the solar cell. Besides the minority carrier lifetime the implied open-circuit voltage (iV_{oc}) and the saturation current density (J_0) are also calculated. These values are of use since they are a measure of the passivation quality for symmetrically passivated wafers [66]. The lifetime expressed by the Sinton in calculated using equation 2.1.

$$\tau = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}} \tag{2.1}$$

where Δn is the change in carrier density and is $G(t)$ is the photogeneration rate.

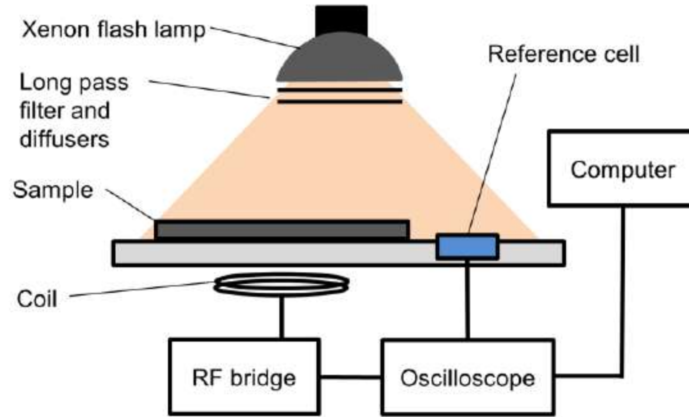

Figure 2.14: Schematic illustration of a Sinton photoconductance measurement setup [65].

J-V

For a reliable analysis of the J-V characteristics of a solar cell the WACOM solar simulator is utilized [67]. Through the use of a xenon and halogen lamp sunlight can be imitated for standard test conditions (STC). The requirements for the STC are an irradiance of 1000 W/m^2, the spectrum resembles an AM1.5 spectrum and the temperature should be 25 °C. Due to the temperature emitted from the lamps an active cooling element is preventing the solar cells from reaching excessive temperatures. Figure 2.15 shows a schematic for a basic solar cell J-V measurement setup. The solar cell needs to be positioned beneath the lamps and connections are made with several pins to the metal contacts. Prior to the measurement a voltage range and the solar cell surface area have to be specified. Since wafers may include multiple cells black segments are used to cover the cells that will not be measured so that no charge carriers may be generated on those surfaces. Besides the J-V curve as an output, other external parameters that are measured include the J_{sc}, V_{oc}, FF η, R_s and R_{sh}. The efficiency is determined as the ratio of the incident power that can be converted into electricity, using the parameters measured from the J-V characteristics the power and efficiency can be expressed as:

$$P_{max} = J_{sc} * V_{oc} * FF \tag{2.2}$$

$$\eta = \frac{J_{sc} * V_{oc} * FF}{P_{in}} = \frac{P_{max}}{P_{in}} \tag{2.3}$$

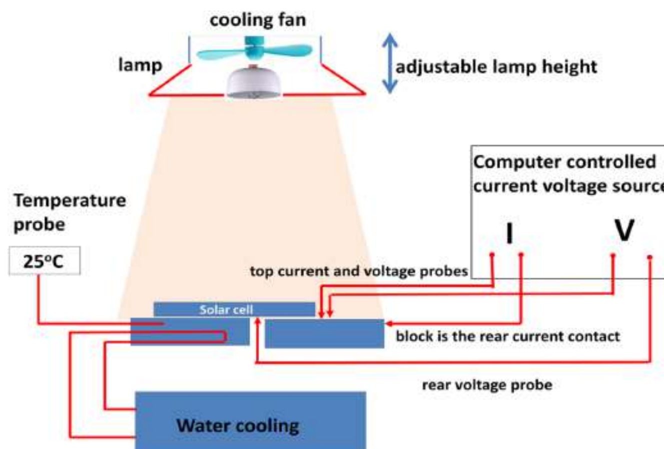

Figure 2.15: Schematic illustration of the setup to measure the J-V characteristics [68].

EQE

The External Quantum Efficiency (EQE) of a solar cells is the ratio of the collected electron-hole pairs at the metal contacts of the solar cells to the number of photons incident on the solar cell. It can be expressed using equation 2.4 [11]:

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q * \phi(\lambda)} \tag{2.4}$$

where $I_{ph}(\lambda)$ is the photocurrent measured in the solar cell, q is the elementary charge and $\phi(\lambda)$ is the spectral photon flow incident on the solar cell. It is also possible to calculate an integrated J_{sc} from the EQE, equation 2.5 shows how:

$$_{int}J_{sc} = q * \int_{\lambda_1}^{\lambda_2} EQE(\lambda) * \phi(\lambda) d\lambda \tag{2.5}$$

The EQE is presented in a graph with the wavelength of light on the x-axis and the percentage of the collected electron-hole pairs to the incident number of photons on the y-axis. The wavelength range typically used is 300 nm to 1200 nm. This is because 300 nm is the lower limit of the AM1.5 spectrum and above 1200 nm most photons will not interact with the semiconductor. The EQE is measured by positioning the solar cell in a chamber in front of a Xenon lamp with a wavelength range from 200 nm to 2500 nm. At specified wavelength intervals that collected charge carriers are measured over the wavelength range. The output is a graph that shows for each wavelength the EQE percentage. This graph can assist in identifying major optical loss mechanisms in the solar cell. If the EQE is low for short wavelengths, the photons are absorbed prior to reaching the absorber layer which leads to parasitic absorption. If the EQE is low for high wavelengths, the light passes through the absorber layer and subsequently leaves the solar cell.

TLM

Characterizing the contact resistance of solar cells can be determined by using the transmission line method (TLM). TLM is implemented on test samples with variable spacing between metal contacts deposited on the semiconductor surface [69]. The metal contacts are of identical dimensions and as many contacts as possible are preferred for measuring the contact resistance (R_c) between them. An example of a TLM structure is presented in figure 2.16. Measuring the R_c between the different lengths of the semiconductor area provides values that can be plotted in a graph, with increased semiconductor surface lengths the R_c increases given the longer distances carriers will travel. A line can be plotted over the measured R_c from which it is possible to extrapolate the sheet resistance (R_s), this property indicates the resistivity over the thickness of a layer.

The contact resistance is dependent on the size of the metal contacts, a property more suited for the comparison of contact formation is the contact resistivity (ρ_c). A phenomenon referred to as current crowding, which is a uneven flow of current to and from the contacts, is also considered in the when calculating the ρ_c by using the transfer length (L_T). The L_T is defined as the average distance a carrier will travel between contacts. Equation 2.6 describes the calculation for the contact resistivity:

$$\rho_c = R_c * L_T * W \tag{2.6}$$

where $L_T W$ can be considered the effective area of the contact.

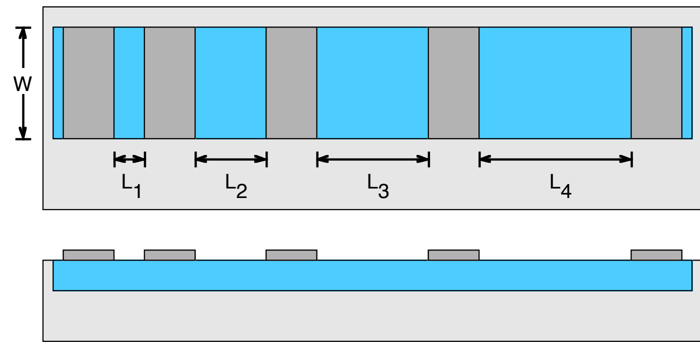

Figure 2.16: Schematic illustration of a typical arrangement of a TLM pattern, the semiconductor surface is given in blue and the metal contacts in grey [69].

2.3. Elements profiling

Electrochemical capacitance–voltage (ECV) measurements are performed to measure active carrier concentrations in the semiconductor material. Specifically, the carrier concentrations refer to the doping profile close to the surface of the material. The capacitance of the solar cell is measured whilst it is positioned against an electrochemical cell [70]. The electrochemical cell uses an electrolyte to create a depletion region , by etching the semiconductor surface the capacitance measurements are performed as a function of depth. After every etching step the capacitance is measured and this process is repeated in a cycle until the concentrations of dopants have reached intrinsic values. The resulting values can be inserted into a logarithmic plot given the variation in the order of magnitude when considering doping profiles.

3

Local poly-SiO_x finger fabrication and optimization

For this project the local poly-SiO_x will be deposited through a hard mask, this chapter will first explain how this mask is fabricated and subsequently implemented for the deposition process in section 3.1. A morphology optimization has also been performed for the a-SiO_x:H deposited through the hard mask which is discussed in section 3.2. Finally section 3.3 shows the cell designs that are used for the fabrication process.

3.1. Fabrication of the hard mask

Making the hard mask is a rather straightforward process. This mask will function as a cover for the substrate when a PECVD deposition is performed. The mask has certain requirements:

- The openings widths of the mask have to be close to the calculated dimensions, this ensures that the design can be optimized for the various solar cell patterns. The edges of the mask will have to be straight and not irregular which might result in inaccurate depositions.
- The mask requires a good durability. One of the advantages of the hard mask is the ability to re-use it for multiple depositions, a fragile mask might break after a single deposition. The mask must not break when it is clamped into the PECVD holder, survive the PECVD deposition numerous times and not shatter during a cleaning process.
- The size of the mask has to be close to that of the wafer used for the deposition, and the surface of the mask that is in contact with the wafer should be flat. When the mask is positioned in the PECVD holder it can not exceed the holder's border. A too small mask will fall out of the holder if it is not in contact with all of the holder's edges. The flat surface is important because the space between the mask and the wafer has to be minimized; any leftover space will influence the PECVD deposition. Some material could slip between the substrate and the mask opening resulting in uneven finger depositions.

The masks are fabricated using standard silicon wafers that are double side polished with a thickness between 280 ± 25 μ. The orientation of the wafer is <100>, this relates to the direction of the silicon crystal lattice. Making the mask openings requires an etching step that will fully etch through the wafer. A layer has to be deposited on the wafer surface that is able to resist the etching solution, otherwise the entire wafer is etched and will be destroyed. This resistant layer will have to be patterned using lithography in order to preserve certain areas of the wafer. Once the etching process is finished this protective layer will have to be removed. The entire process consists of the following steps:

1. Silicon nitride deposition of the front side of the mask. This layer will function as the material resistant to the etching step. The silicon nitride layer is deposited at a temperature of 400 °C and is a few hundred of nm thick, approximately 240 nm.

2. Lithography on the front side of the mask. This step will add a layer of photoresist on top of the silicon nitride layer, the pattern of the photoresist will correspond to the design of the hard mask.
3. Silicon nitride removal on the front side of the open area. For the wet etching step some areas of the mask have to be exposed, currently it is fully covered by silicon nitride and some closed areas with photoresist. An etching step of the silicon nitride will remove this layer up to the silicon bulk material.
4. Photoresist removal. The photoresist has served its purpose now that a pattern has been created in the silicon nitride layer, removing the photoresist is required for the steps which follow. The photoresist has to be stripped from the surface.
5. Cleaning of the wafer masks. To prevent contamination possible obtained from the previous processes a cleaning step is included to prevent the risk of contamination to machinery. This cleaning process consists of first a nitric acid bath with a concentration of 99% at the room temperature, second a nitric acid bath with a 69% concentration at 110 °C. Rinsing is performed before and after each bath for safety reasons and to prevent contamination of the masks. Drying the wafers is the final step of the cleaning process to remove any residual water.
6. Silicon nitride deposition of the rear side of the mask. The rear side of the mask does not yet have a silicon nitride layer, without this layer the etching step will fully etch the rear side and destroy the mask. A full area silicon nitride layer is deposited at 400 °C that also is about 240 nm in thickness.
7. Wet etching of the mask. The wet etching will be performed using a potassium hydroxide (KOH) solution. Silicon nitride has a high selectivity to KOH, the etch rate will be below 1 nm/h [71]. The etching rate of silicon in KOH varies depending on the temperature and concentration of the solution. Reported KOH etching rates when the solution has a concentration of 30% and a temperature of 80 °C are approximately 80 μm/h [72]. Given that the thickness of the wafer is at least 255 μm, the etching process will take at least 3 hours. The KOH will etch away at the silicon at an angle of 54.74 °, which corresponds with the <100> orientation of the wafer. Once the wafer has been fully etched through and opening are visible of both the front and rear side, it is removed from the solution and rinsed.
8. Silicon nitride removal from both sides of the mask. The mask now has been fabricated, removing the silicon nitride is the final step. Any solution that can etch away silicon nitride is suitable for this step. A buffer oxide etch (BOE 1:7) at room temperature is the most convenient chemical to properly remove the silicon nitride, depending on the quality of the silicon nitride the removal will take several minutes. The complete mask fabrication process is visualized in figure 3.1. An example of a hard mask fabricated with this process is shown in figure 3.2.

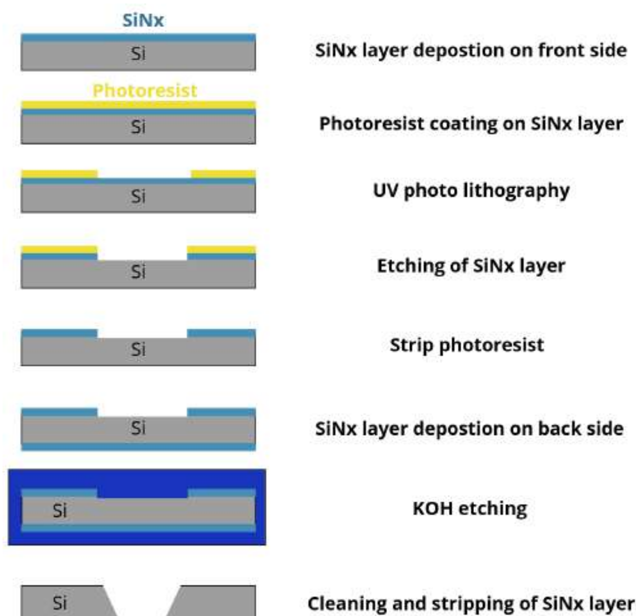

Figure 3.1: Schematic overview of the hard mask fabrication.

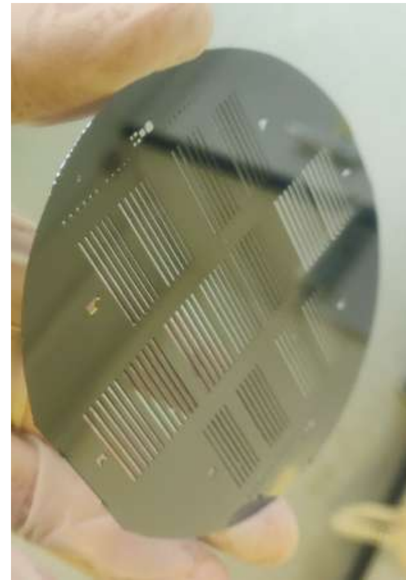

Figure 3.2: Hard mask with openings of various dimensions.

3.2. Poly-SiO$_x$ finger surface morphology optimization

This section investigates the deposition through the hard mask using the PECVD. Section 3.2.1 will discuss how the hard mask affects the shape of the deposition and section 3.2.2 introduces the parameters of the PECVD deposition that influence the deposition. Section 3.2.3 briefly explains another method for the poly-SiO$_x$ finger fabrication which does not use a hard mask.

3.2.1. Influence of the hard mask

The hard mask fully determines the dimensions of the PECVD deposited a-SiO$_x$:H fingers. Materials will be deposited through the openings and attach to the c-Si substrate. In order to minimize the parasitic absorption caused by the poly-SiO$_x$ it is important to have narrow fingers. These fingers do have to be wide enough in order for metal contacts to be deposited on top of them. In order to optimize the a-SiO$_x$:H deposition a test mask was fabricated that allowed for a wide range of finger widths. The mask fabricated for this purpose is shown in figure 3.3.

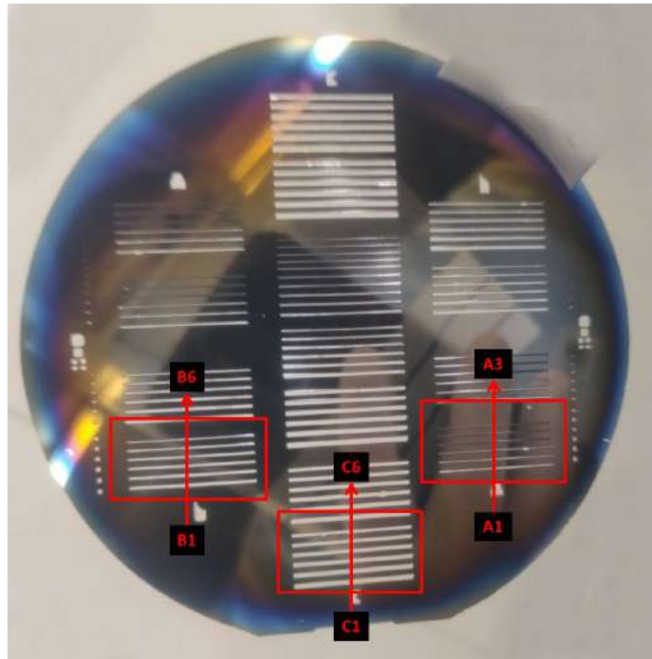

Figure 3.3: Hard mask used for investigating the opening width, three groups of opening widths are indicated.

This mask has three mains groups based on the mask opening widths, going from smallest to largest they are group A, B and C. These groups consist of a number of openings, group A has three openings and both group B and C have six openings. The groups are of similar magnitude in opening, however the minimal finger opening width is different. Group A has the smallest width and C has the widest, group B is in between the two. In each group the fingers given a number based on number to differentiate them. Each opening in a group has a 50 μm width difference. If both the opening of the mask on the front side, the thickness of the mask wafer and the crystal orientation of the wafer is known then the theoretical opening on the rear side of the wafer can be calculated. The optical microscope or the SEM can be used to measure the openings. Both the calculated and the measured width openings are presented in tables 3.1, 3.2 and 3.3.

Table 3.1: Width openings of group A.

	A1	A2	A3
Design width [μm]	130	80.0	30.0
Measured width [μm]	136	85.3	38.7

Table 3.2: Width openings of group B.

	B1	B2	B3	B4	B5	B6
Design width [μm]	330	280	230	180	130	80.0
Measured width [μm]	333	285	235	186	133	82.4

Table 3.3: Width openings of group C.

	C1	C2	C3	C4	C5	C6
Design width [μm]	630	580	530	480	430	380
Measured width [μm]	636	587	541	491	438	387

All of the measured widths are slightly larger than what the calculated width had anticipated them to be. Several reasons can be the cause for these deviations, such as that the wafers spent a few minutes too

long in the KOH bath during the etching process. Another reason could be that the concentration, the temperature, or a combination of both were slightly higher than the assumed values in the calculation for the KOH bath. The thickness of the wafer also could be lower than the reporter thickness, leading to the etch through the wafer being finished earlier than expected. Nevertheless, given the number of variables to consider the measured width openings are close enough to the calculated values. All these opening serve as pathway for the a-SiO$_x$:H deposited during the PECVD to pass through, figure 3.4 shows a 2D schematic lay-out of this process.

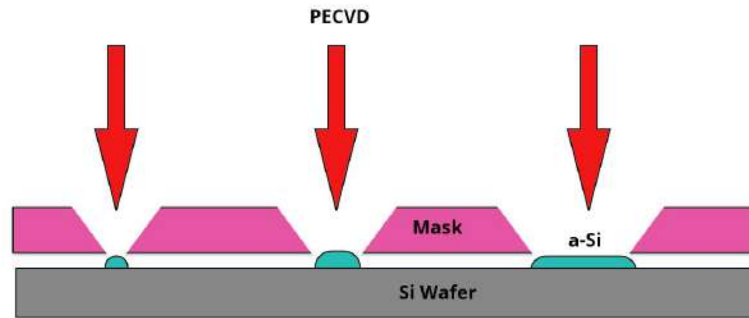

Figure 3.4: Schematic representation of the PECVD process when a hard mask is included.

3.2.2. Influence of the a-SiO$_x$:H layer deposition parameters

The PECVD allows for various parameters to be altered for the depositions, this section will discuss some of the investigated parameters and their effects. These parameters include:

- Gas flow rate
- Power density
- Working pressure
- Substrate temperature
- Deposition time

During the optimization process the influence of the power, pressure and deposition time were investigated. The temperature was not changed due to the PECVD chamber being kept at a constant temperature, the substrate when deposited reach a temperature of 180 °C after waiting 30 minutes. The gas flow rate was not investigated to reduce the complexity of the optimization. Several recipes were established to deposit the a-SiO$_x$:H through the hard mask, table 3.4 shows the specifications of the recipes.

Table 3.4: Recipes investigated for the PECVD showing the parameters which were varied.

	Power [W]	Pressure [mbar]	Deposition time [min]
Recipe 1	5	1.0	60
Recipe 2	15	1.0	60
Recipe 3	25	1.0	60
Recipe 4	5	1.0	12
Recipe 5	5	1.5	12
Recipe 6	5	2.0	12
Recipe 7	15	1.0	12
Recipe 8	25	1.0	12
Recipe 9	15	1.5	12
Recipe 10	25	1.5	12

This list of recipes provides a good combination between the influence of the power and pressure on the morphology of the a-SiO$_x$:H. All recipes were deposited through the hard mask on a flat wafer.

For the solar cells fabrication the a-SiO$_x$:H will be deposited on textured wafer, however to investigate the morphology flat wafers are more suitable to be used with the Dektak 8. The a-SiO$_x$:H will be tens-to-hundreds of nanometers in scale and this is difficult to measure on the randomized pyramids of a textured surface which is in the order of microns.

Recipe 4 deposits the a-SiO$_x$:H at low power, pressure and a short deposition time, figure 3.5 shows the morphology of a select number of fingers from group C. The morphology of these fingers appears rough and irregular. The majority of the deposited material has not accumulated in the center of the opening width through the mask, this location being at 0 on the x-axis. Furthermore the surface of all the fingers show a constant unevenness with some measurements shooting upwards several nm. This occasional spike could be a measurement irregularity of the Dektak 8, however the small deviations which fill the surface certainly are not. The low power and moderate pressure show promise for the a-SiO$_x$:H deposition but the morphology preferably is more constant throughout.

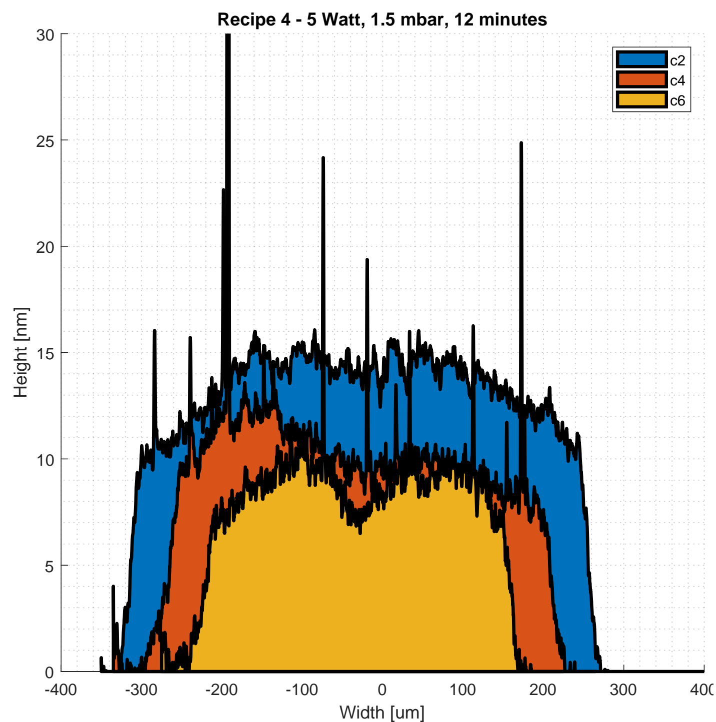

Figure 3.5: Doped a-SiO$_x$:H deposition through the hard mask at 5 Watt, 1.5 mbar and 12 minutes.

It can be observed that the morphology in terms of uniformity drastically improves with a higher power, as shown in figure 3.6. For this recipe the power has increased from 5 to 25 Watt, this should improve the uniformity of the a-SiO$_x$:H fingers because of the higher deposition rate of the a-SiO$_x$:H [73]. The surface still has small nanometer scale irregularities, however given the larger dimensions of these fingers they become less noticeable in the given figure. The uniformity has drastically improved when compared to recipe 4 with the increase in deposition power. The center of the fingers are distinctly located at the center of the x-axis and its shape is clearly that of a finger.

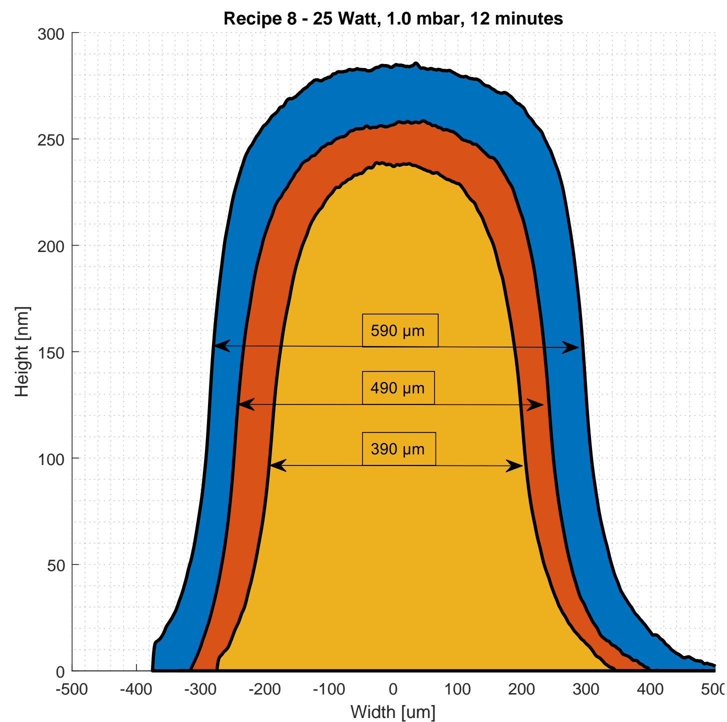

Figure 3.6: Doped a-SiO$_x$:H deposition through the hard mask at 25 Watt, 1.5 mbar and 12 minutes.

Another deposition is given in figure 3.7. This deposition is performed at a power of 15 Watt and at a pressure of 1.5 mbar. A significant difference with this a-SiO$_x$:H finger deposition compared to the deposition in figure 3.6 is the variation of the finger height for each hard mask opening. Each of the fingers from the previous graphs are from the same group of the hard mask, the deposition from recipe 9 shows the highest deviation between each finger height. When the opening width decreases 100 μm, the height of the finger deposition decreases approximately 35 nm. Despite this discrepancy between the finger heights, the lower power shows that at a lower deposition rate there is still uniformity for the fingers. The lower deposition rate provides a higher control of the deposition in terms of the deposited finger thickness.

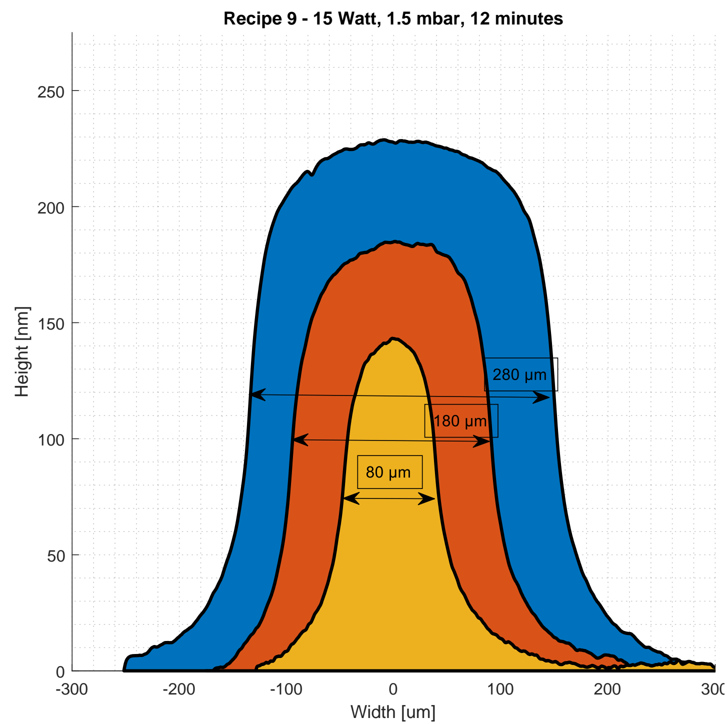

Figure 3.7: Doped a-SiO$_x$:H deposition through the hard mask at 15 Watt, 1.5 mbar and 12 minutes.

One aspect of the finger deposition is that material can pass between the mask and the substrate if there is a small gap, a-SiO$_x$:H will subsequently accumulate beyond the hard mask openings as illustrated in figure 3.8. Figure 3.8 includes 2 vertical black lines, these lines indicate the opening of the hard mask through which the finger is deposited, which is 38 μm in total width. Past these black lines it can be observed that a slight amount of a-SiO$_x$:H is measured. The a-SiO$_x$:H which slips past the hard mask opening will accrue and potentially could results in parasitic absorption losses. Clamping the hard mask to the semiconductor substrate does not seems to resolve this issue, the textured surface of the substrate is several orders of magnitudes larger than the a-SiO$_x$:H slipping through. This excess material will always be present when depositing through the hard mask.

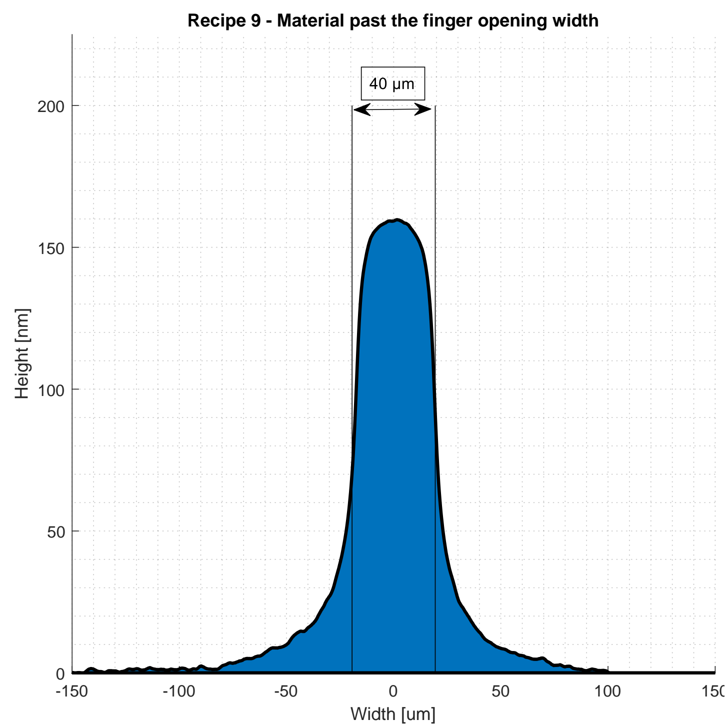

Figure 3.8: Doped a-SiO$_x$:H deposition through the hard mask at 15 Watt, 1.5 mbar and 12 minutes, showing the overshoot of material.

Only several of the measurements were discussed in this section, and ultimately the recipe deemed most suitable for the poly-SiO$_x$ finger fabrication is recipe 9. The parameters used for the deposition of a-SiO$_x$:H through the hard mask with recipe 9 result in a uniform deposition, while having a controllable deposition rate and not overly degrading the quality of the hard mask. When depositing using a power 5 Watt there is little uniformity, at a power of 25 Watt there is plenty uniformity however this is paired with a higher deposition rate. For a better control of the a-SiO$_x$:H finger thickness, a power of 15 Watt provides decent uniformity while having a higher control of the deposition rate. The influence of the pressure has not resulted in any measurable changes.

3.2.3. Etch-back method

Till now the only method for depositing the poly-SiO$_x$ fingers that has been discussed is the hard mask method. An alternative method for fabricating local poly-SiO$_x$ fingers is implementing an etch-back method. This process involves lithography steps after a full-area poly-SiO$_x$ layer has been deposited on the c-Si surface. This purpose of the lithography step is to protect certain parts of the poly-SiO$_x$ that we want to preserve, these parts being the narrow poly-SiO$_x$ fingers. The process is visualized in figure 3.9.

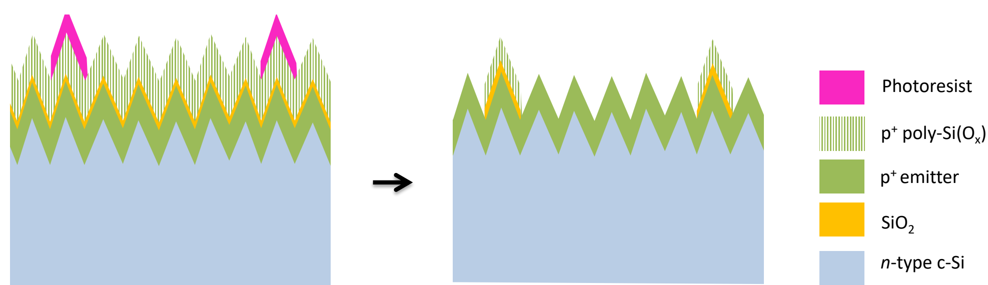

Figure 3.9: Visual representation of the etch-back method.

3.3. Design of the poly-SiO$_x$ fingers

The design of a localized poly-SiO$_x$ finger solar cell requires several masks to make the complete structure. For lithography purposes a design is needed to make a new hard mask that allows for the placement of the poly-SiO$_x$ finger on a solar cell structure. A second design is required for the metallization on the front side of the wafer, this design has to include the metal fingers that will be placed on top of the poly-SiO$_x$ fingers and busbars which go around the solar cell's edge. Finally a design is required for the rear side metallization which can facilitate a metal deposition covering each cell present on the wafer, while not coming into contact with each other. Figure 3.10 shows the masks used for the local poly-SiO$_x$ solar cell fabrication process.

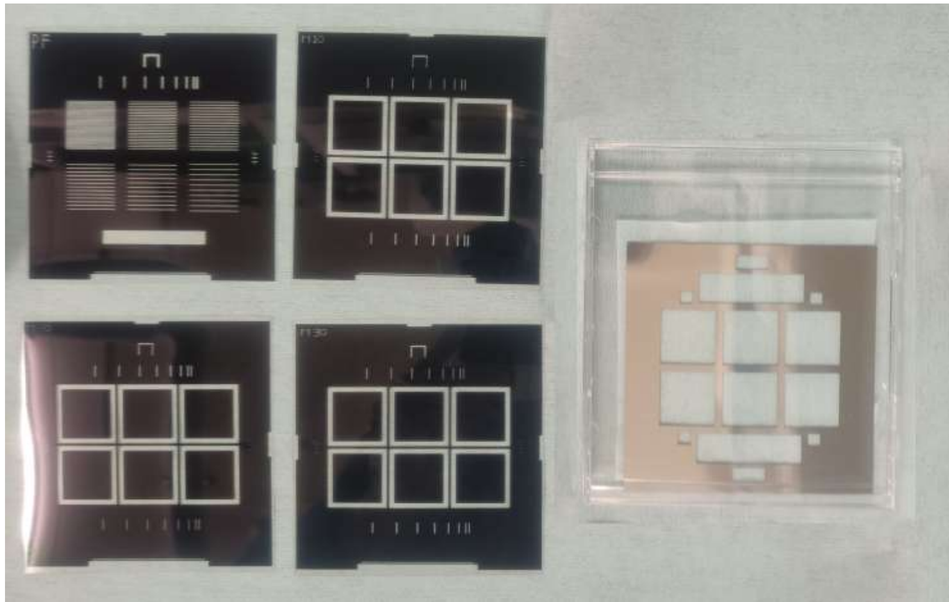

Figure 3.10: Four black lithography masks and a full area metallization mask for the local poly-SiO$_x$ finger application.

The top-left black lithography mask in figure 3.10 is used for the hard mask design, the other three are used for the metallization. The openings on the hard mask approximately 40 μm. The difference between the three metallization masks is the width of the fingers on the cells, which are 10, 20 and 30 μm. The metal mask on the right side is used for the rear side metallization. Ideally a lithography mask with the same design as the rear side metallization mask is also used, unfortunately such a mask was not available. The purpose of the extra mask would be do perform a front side cell isolation prior to the local poly-SiO$_x$ finger deposition to prevent a cross connection of the doping layers of the cells.

The six cells depicted on the masks are comprised of a varying amount of fingers, meaning that they have a different metal finger coverage (MFC) per solar cell. The MFC is a percentage which expresses the percentage of the solar cell area covered with metal fingers relative to the entire solar cell surface area. A thicker metal finger width subsequently leads to a higher MFC. Table 3.5 gives an overview of the differences of the six solar cells.

Table 3.5: Number of fingers for each solar cell (SC) and MFC for each cell given a specific metal finger width.

	Fingers	**MFC for 10 μm [%]**	**MFC for 20 μm [%]**	**MFC for 30 μm [%]**
SC-1	33	1.65	3.30	4.95
SC-2	22	1.10	2.20	3.30
SC-3	17	0.85	1.70	2.55
SC-4	13	0.65	1.30	1.95
SC-5	11	0.55	1.10	1.65
SC-6	10	0.50	1.00	1.50

Figure 3.11 shows a detailed close-up of the markers of the mask. These markers are located on both sides of all the mask, these are relevant for aligning the poly-SiO_x fingers to the metal fingers. These markers are the essential structures for the alignment of the structures displayed on the lithography masks. Either of the two markers in located on beside the solar cell structures in lithography mask. The alignment utilizes two microscope lenses during the alignment, one lens for each marker. The usage of two reference points increases the accuracy when trying to overlay a structure on top of another. Although in theory the alignment might come across as trivial it is rather intricate given the small scale. The markers in figure 3.11 are not larger than 300 μm in width and length, potential misalignments will surely occur. Figure 3.12 highlights several misalignments. It is important to use the optical microscope as often as possible to ensure that alignments are carried out accurately.

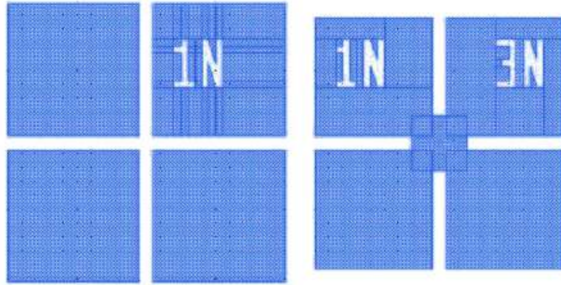

Figure 3.11: Markers located on all the black lithography masks, the left marker is of the hard mask design and the right markers is present in the three metallization masks.

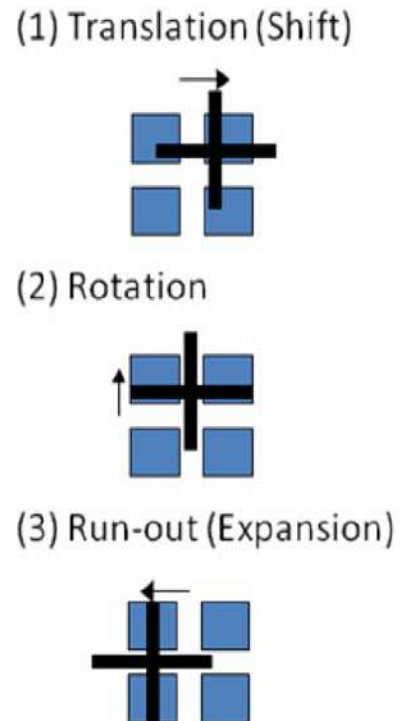

Figure 3.12: Schematic of various misalignments [74].

4
Poly-SiO_x passivating contact optimization

Fabricating the poly-SiO_x finger solar cells requires many depositions to establish all the layers that constitute the solar cells. This chapter focuses on the optimization of the processes involved in the fabrication process. In section 4.1 the surface passivation is optimized, separated in three subsections that investigate the front side poly-SiO_x, the passivation layers and the rear side doping layer. Section 4.2 investigates the doping profiles of the doping layers deposited for the local poly-SiO_x finger solar cells fabrication.

4.1. Surface passivation

The passivation for the doped poly-SiO_x passivating contacts includes the chemical passivation from the ultra-thin tunneling SiO_x layer positioned between the doping layer and the doped poly-SiO_x, and the field-effect passivation to prevent minority carriers from diffusing towards the surface. This section will first investigate the doped poly-SiO_x deposited on the front side of which the poly-SiO_x fingers will be fabricated. The majority of the surface area will however not contain the poly-SiO_x fingers, thus the passivation layer of bulk surface area is investigated as well. Finally the rear side doping layer is briefly examined.

In order to have separation of the charge carriers a p-n junction should be present. Initially for this project the p-type and n-type doping layers would've been created using ion implantation, this is a fabrication technique which through ion acceleration changes the chemical and electrical properties of a semiconductor [75]. Unfortunately the machine which provides the ion implantation turned to be defective and was no longer functional. An alternative for the p-n junction formation is thermal diffusion of doping atoms into the semiconductor surface. This can be achieved through either BBr_3 or $POCl_3$ diffusion, BBr_3 providing a p-type layer and $POCl_3$ a n-type layer. These respective diffusion methods consist of an initial deposition of the required material and afterwards a drive-in of to move doping atoms deeper into the substrate [76, 77]. With the equipment available in the lab it is not possible to use thermal diffusion to create a p-type doping layer, because there is no active furnace to facilitate the diffusion. The only option left was to build the poly-SiO_x finger solar cells on wafers that already have a p-type doping layer. For this project commercial p^+ diffused Cz wafers are utilized. These wafers are the staring material for the poly-SiO_x finger solar cells. These wafers are commercial grade n-type c-Si quasi-square Cz wafers. They have a thickness of approximately 150 μm with a resistivity ranging between 0.5 - 3.0 Ωm, the front side is textured and the rear side is flat. The square dimensions are about 182 mm and the lattice is a <100> orientation. On the front side is a p^+ diffused doping layer while the rear side is intrinsic. Figure 4.1 shows the structure of the commercial Cz wafer.

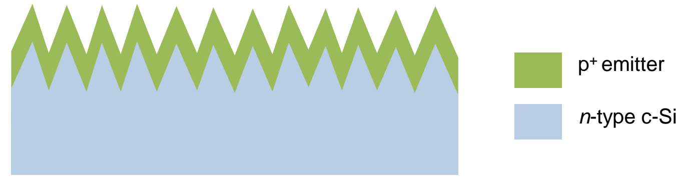

Figure 4.1: Schematic structure of the commercial p^+ diffused Cz wafer used for the poly-SiO_x finger fabrication.

To investigate the optimization of the various process used throughout, symmetrical test samples will have to be constructed. The reason being is that when characterizing the test samples the measurements are unreliable in the front side and rear side are not identical. Surfaces which contain different layers to each other will inherently give different results. Symmetrical samples will avoid this issue.

4.1.1. Doped poly-SiO_x on the front side

In section 3 an optimization for the poly-SiO_x finger morphology was performed, this section will discuss the optimization of the poly-SiO_x finger properties. Symmetrical samples containing full area poly-SiO_x were fabricated using the optimal PECVD deposition parameters previously determined. For examining the properties both the poly-SiO_x thickness and annealing temperature were investigated. The commercial Cz wafers were first cleaned using RCA cleaning, a low concentration HF bath was subsequently used to remove the native oxide layer. The SiO_x was formed in a 69.5 % nitric acid solution on both sides. Full area a-SiO_x:H was deposited using the PECVD, with thicknesses of 20, 50, 100 and 150 nm on individual wafers. Each wafer is laser cut into four pieces. The annealing process which follows takes place at 850, 875, 900 and 900 °C, with each different poly-SiO_x thickness wafer piece being annealed at a different annealing temperatures. This results in sixteen unique test samples. The passivation is performed by applying a 75 nm thick SiN_x layer and subsequent FGA. Figure 4.2 shows the schematic structure of the symmetrical p^+ doped poly-SiO_x sample.

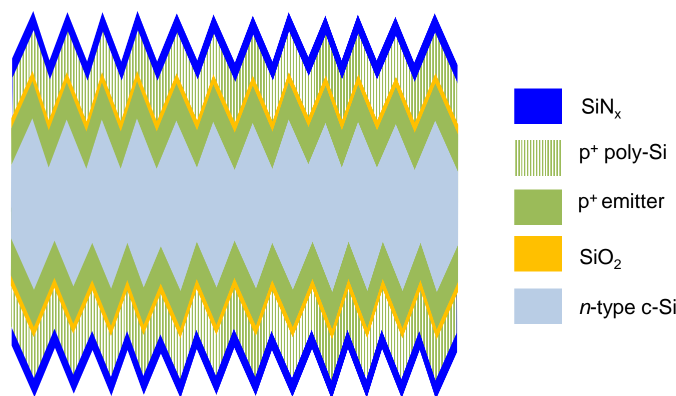

Figure 4.2: Schematic structure of the doped poly-SiO_x symmetrical test sample.

The Sinton WCT-120 was utilized at various points in the process to measure, among other parameters, the implied open-circuit voltage (iV_{oc}), the minority carrier lifetime (τ) and the saturated current density (J_0). These measurements were taken after the annealing, after the SiN_x deposition, after the FGA and after removing the SiN_x layer on both sides. Figures 4.3, 4.4, 4.5 and 4.6 show the progression of the iV_{oc} for the test samples when the a-SiO_x:H fingers with various thicknesses is annealed at specific temperatures.

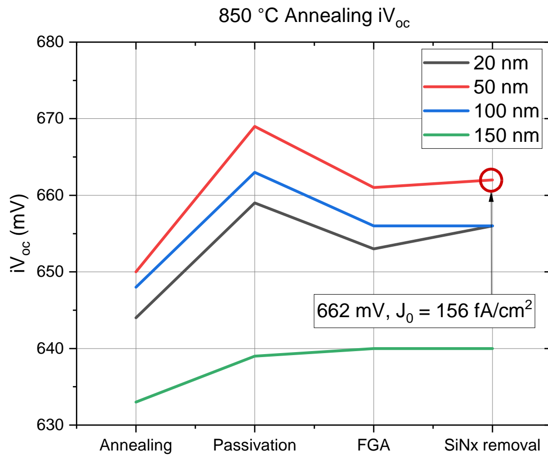

Figure 4.3: iV_{oc} of doped poly-SiO$_x$ test samples annealed at 850 °C.

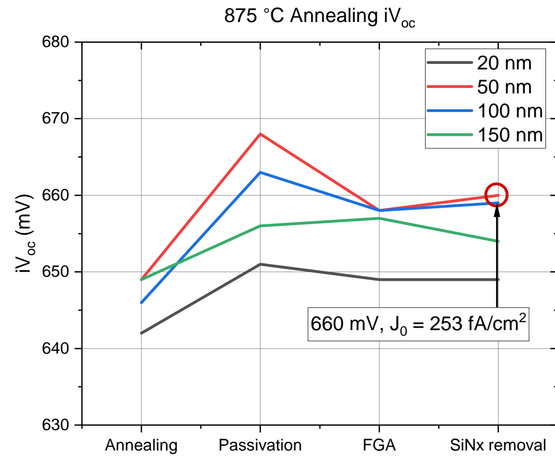

Figure 4.4: iV_{oc} of doped poly-SiO$_x$ test samples annealed at 875 °C.

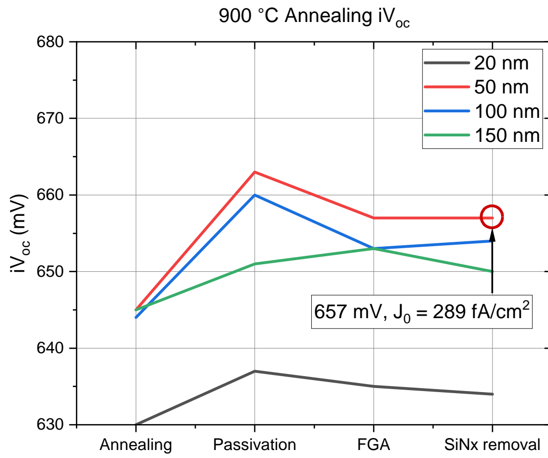

Figure 4.5: iV_{oc} of doped poly-SiO$_x$ test samples annealed at 900 °C.

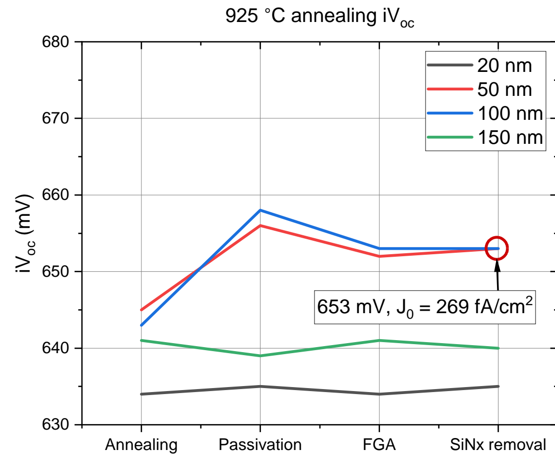

Figure 4.6: iV_{oc} of doped poly-SiO$_x$ test samples annealed at 925 °C.

For the majority of the samples the iV_{oc} increases when the SiN$_x$ passivation layer is applied following the full-area poly-SiO$_x$ annealing. The highest rise of the iV_{oc} occurs for the 50 nm thick poly-SiO$_x$ layer, it increases from 637 mV to 663 mV after the SiN$_x$ is deposited. Following the FGA annealing the iV_{oc} decreases for the 20, 50 and 100 nm thickness samples, however for the 150 nm thickness is seems to slightly increase. Removing the SiN$_x$ layer results in small irregular changes to the iV_{oc}, for some samples there appears to be no change when performing this operation. Poly-SiO$_x$ layers that are too thin or too thick show the lower obtained iV_{oc} measurements. During the annealing process some of the p-dopants present in the a-SiO$_x$:H layer might diffuse into the c-Si bulk material. A decrease of the dopants from the poly-SiO$_x$ reduces the intensity of the field-effect passivation resulting in a decrease of the passivation properties [78].

For the symmetrical samples the saturation current density J_0 is also obtained, these values will have to be halved to account for the symmetric structure. Similar to the iV_{oc} the smallest J_0 is obtained for 50 nm poly-SiO$_x$ layer thicknesses. For an iV_{oc} of 662 mV the value of J_0 156 is fA/cm^2, for the same finger thickness the J_0 becomes 289 fA/cm^2 when annealing at 900 °C. These results imply that the higher annealing temperatures result in a higher J_0, thus a higher recombination.

The lifetimes of the doped poly-SiO$_x$ test samples are given in figures 4.7, 4.8, 4.9 and 4.10. As was the case for the iV_{oc}, the 50 and 100 nm thick finger have obtained the highest values. The highest lifetime that was measured after the SiN$_x$ removal is for the 50 nm thick finger annealed at 850 °C with

155.64 μs. This also happens to be the finger that showed the lowest J_0. Following the application of the SiN_x layer on the doped poly-SiO_x, the majority of the test sampled increase in measured lifetime. The 150 nm thick doped poly-SiO_x is the only thickness which decreases after the passivation of the doped poly-SiO_x layer, these figures all show a similar trend for all annealing temperatures. The FGA procedure results in lower lifetimes for all investigated samples, a similar decrease is seen when looking at the iV_{oc}. The inclusion of the FGA to the overall process causes a decrease in passivation quality.

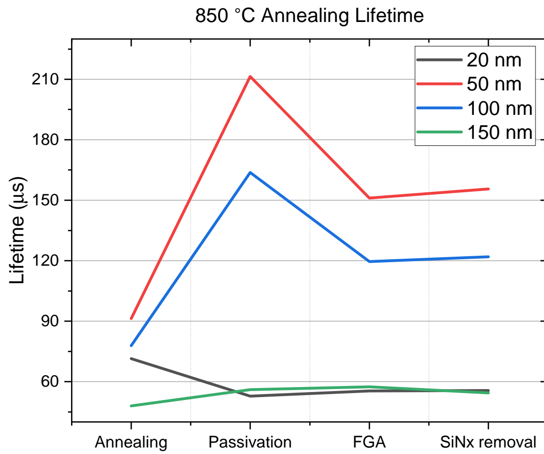

Figure 4.7: Lifetimes of doped poly-SiO_x test samples annealed at 850 °C.

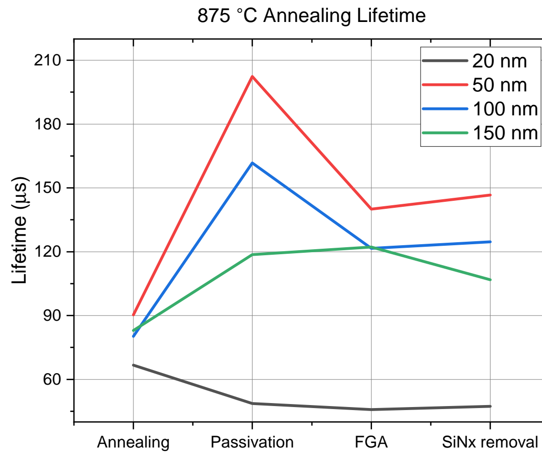

Figure 4.8: Lifetimes of doped poly-SiO_x test samples annealed at 875 °C.

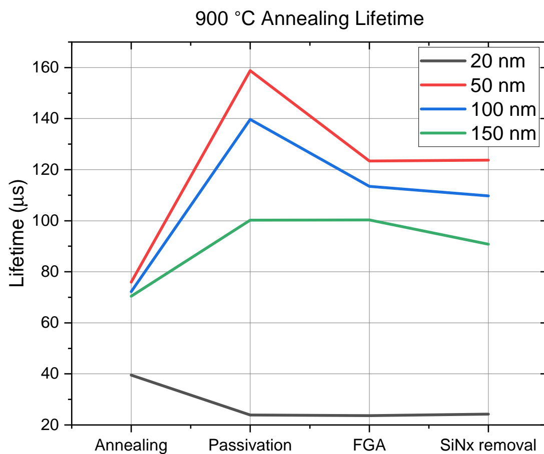

Figure 4.9: Lifetimes of doped poly-SiO_x test samples annealed at 900 °C.

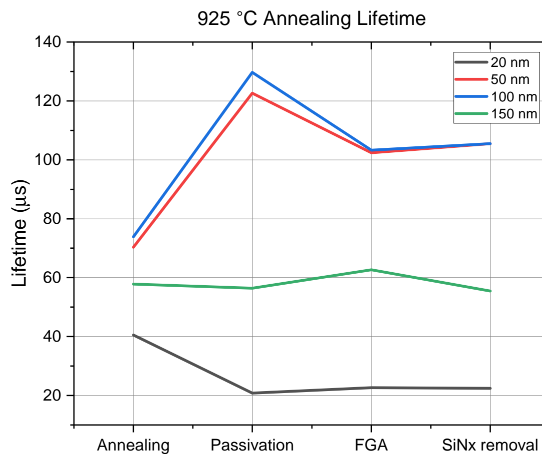

Figure 4.10: Lifetimes of doped poly-SiO_x test samples annealed at 925 °C.

Given the results for the iV_{oc}, τ and J_0 of the investigated samples the preferred conditions for the doped poly-SiO_x fingers would be a 50 nm thickness annealed at a temperature of 850 °C. The sample which was fabricated according to these parameters presented the highest iV_{oc} with a values of 662 mV and a corresponding J_0 of 156 fA/cm^2.

4.1.2. Passivation layer on the front side

The majority of the doped poly-SiO_x finger solar cell will have the surface passivated by a Al_2O_3 and SiN_x layer, this section will investigate the influence of the Al_2O_3 thickness and the annealing temperature used to "active" the passivation layer. The ALD deposited Al_2O_3 layer has to be specified by the amount of cycles that are allowed for the deposition. Three different amounts of cycles are considered for the test samples: 60, 120 and 240 cycles. These cycles correspond to deposited Al_2O_3 thicknesses of approximately 5, 10 and 20 nm, respectively. The annealing process is categorized by FGA at 400 °C for 30 minutes and three RTA processes. The RTA takes place at 760, 780

and 800 °C for 1 minute also in a forming gas environment. The structure of the passivated test sample is presented in figure 4.11, a double side textured diffused p^+ emitter wafer is chemically passivated by a thermally grown SiO_x layer. The Al_2O_3 layer is deposited next, followed by the SiN_x capping layer. The test sampled are subsequently laser cut into smaller pieces to perform the annealing processes. The measured iV_{oc} of the passivated test samples are shown in figures 4.12, 4.13, 4.14 and 4.15.

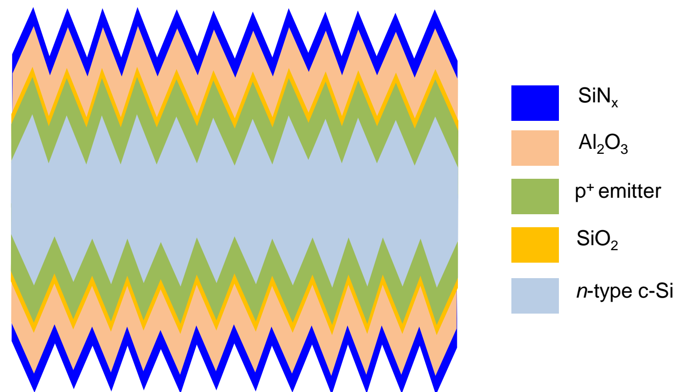

Figure 4.11: Schematic structure of the passivated symmetrical test sample.

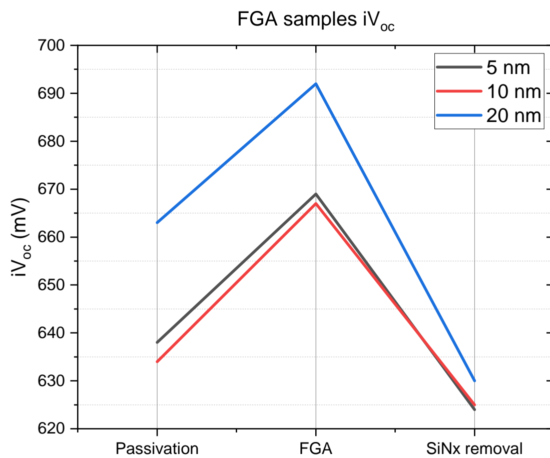

Figure 4.12: iV_{oc} of passivated test samples annealed using FGA.

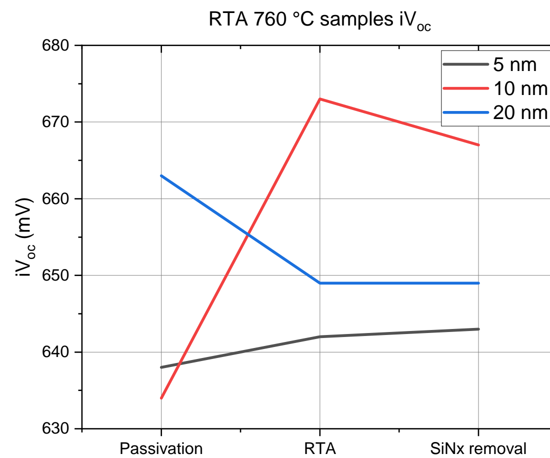

Figure 4.13: iV_{oc} of passivated test samples annealed using RTA at 760 °C.

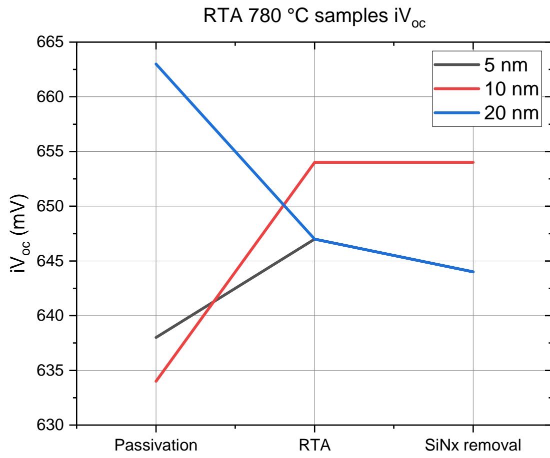

Figure 4.14: iV_{oc} of passivated test samples annealed using RTA at 780 °C.

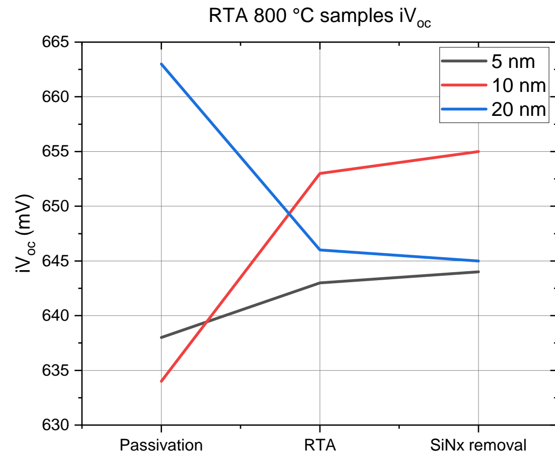

Figure 4.15: iV_{oc} of passivated test samples annealed using RTA at 800 °C.

From these four iV_{oc} figures it can be observed that the FGA test samples provide the highest iV_{oc} measurements. Following the FGA for the 20 nm thick Al_2O_3 passivation layer, the measured iV_{oc} increases from 663 mV to 692 mV with a J_0 of 22.4 fA/cm^2. The slightly thinner Al_2O_3 layer of 20 nm has a lower iV_{oc} of 669 mV and a J_0 of 74 fA/cm^2. The thinnest Al_2O_3 of 10 nm has an even lower iV_{oc} of 667 mV, however it has a slightly lower J_0 of 63 fA/cm^2.

The measurements for all the RTA samples generally do not surpass the iV_{oc} of the FGA samples, or have lower J_0 than that of the FGA samples. The highest obtained iV_{oc} for any of the RTA samples is 673 mV for a 20 nm thick Al_2O_3 layer annealed at 760 °C for one minute. The J_0 corresponding to this measurement is 81 fA/cm^2. This samples seems to be an outlier when compared to the remainder of the RTA samples, since none of the other samples reach and iV_{oc} that exceeds 655 mV. It has been mentioned that high annealing temperatures can cause the passivation quality to degrade, which could be a plausible explanation for the measurements of the RTA samples. Regarding the RTA samples, the 10 nm thick Al_2O_3 layer samples perform the best when compared to the 5 and 20 nm samples. The 5 and 10 nm thick Al_2O_3 samples provide higher iV_{oc} measurements after the RTA process, with the 10 nm thickness resulting is steeper increases. The lifetimes for these samples have also been measured and are presented in figures 4.16, 4.17, 4.18 and 4.19.

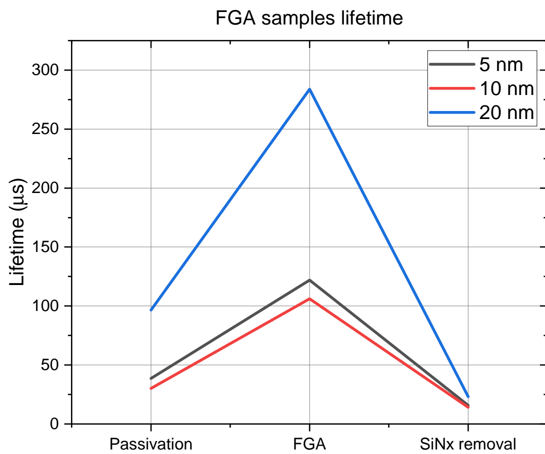

Figure 4.16: Lifetimes of doped poly-SiO_x test samples annealed at 850 °C.

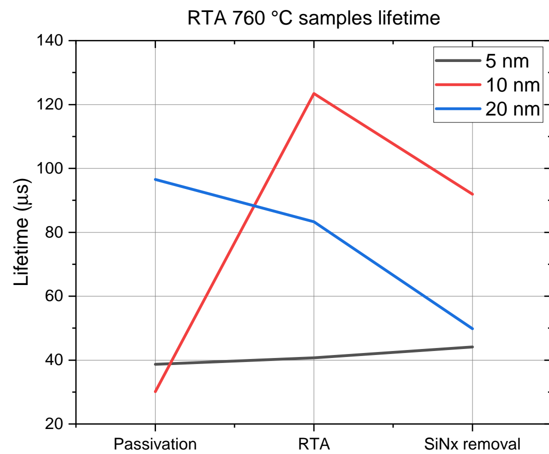

Figure 4.17: Lifetimes of doped poly-SiO_x test samples annealed at 875 °C.

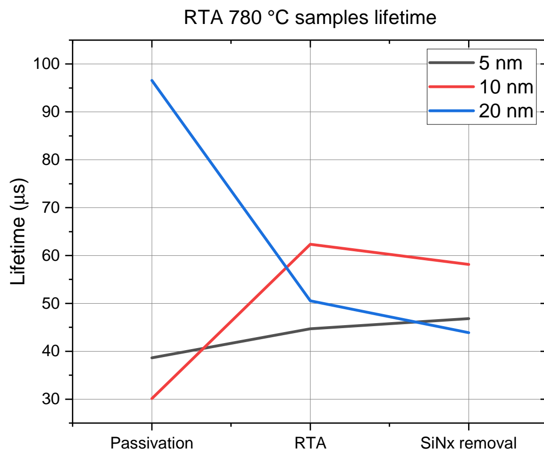

Figure 4.18: Lifetimes of doped poly-SiO_x test samples annealed at 900 °C.

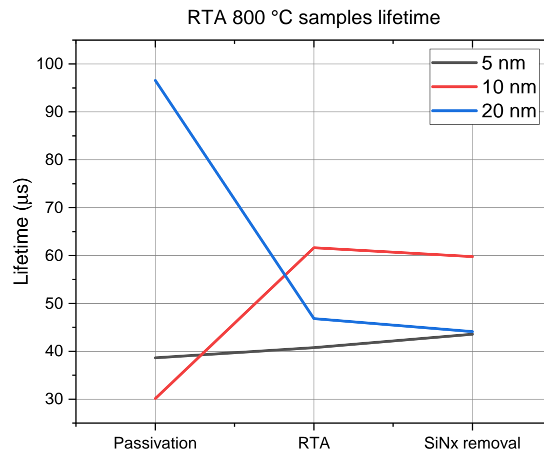

Figure 4.19: Lifetimes of doped poly-SiO_x test samples annealed at 925 °C.

The values of the lifetimes corroborate what the iV_{oc} measurements suggest; the optimal annealing process following the passivation of the p^+ diffused textured surface is FGA. The highest measured lifetime is for the 20 nm thick Al_2O_3 with a value of 283.89 μs. The lifetimes for the other FGA samples are 106.04 μs for the 10 nm thick Al_2O_3 sample and 121.87 μs for the 5 nm thick Al_2O_3 sample. The RTA samples fail to reach these high lifetime values, apart from the 10 nm thick Al_2O_3 layer annealed at 760 °C. This RTA sample has a lifetime of 123.43 μs, however this is the same RTA sample that happened to be the exception to the majority of the RTA measurements and is the only sample with a higher measurement.

The passivated test samples suggest that the best parameters for applying the passivation is depositing a 20 nm thick Al_2O_3 layer, followed by FGA. The highest attainable iV_{oc} and τ for investigated test samples were achieved when these parameters where selected, with an iV_{oc} of 692 mV and a J_0 of 22.4 fA/cm^2.

4.1.3. n-type poly-SiO_x on the rear side

This project does not focus on the optimization on the rear side doping layer, however this layer will have to be fabricated to obtain functional solar cells. A single test wafer was created with the intent to deposit n-type doping and observe the influence of the annealing temperature on the performance. The symmetrical samples that was fabricated is shown in figure 4.20. The commercial Cz wafer currently has a p^+ diffused front side textured surface, to turn this layer into an intrinsic flat surface a potassium hydroxide (KOH) solution is implemented. During this etching step the surface loses the p^+ diffused doping layer and becomes flat. Chemical passivation is performed using a 69.5 % nitric acid solution and with PECVD a 100 nm thick n-type doping layer is deposited on both sides. The doping layer is a-SiO_x:H for the first 10 nm, then phosphor is introduced to form doped a-SiO_x:H. The samples are annealed at 850, 875, 900 and 925 °C for 30 minutes. An HF dip follows the annealing process to remove native grown oxide with a SiN_x deposition and FGA afterwards. In figure 4.21 and 4.22 the iV_{oc} and lifetime of this sample is presented.

Figure 4.20: Schematic structure of the symmetrical rear side n-type doping test sample.

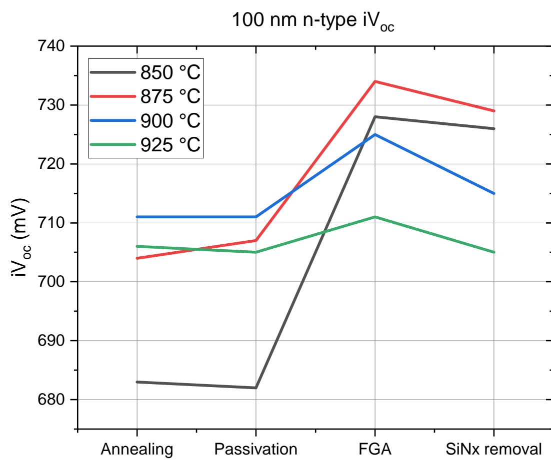

Figure 4.21: iV_{oc} of 100 nm n-type flat test samples.

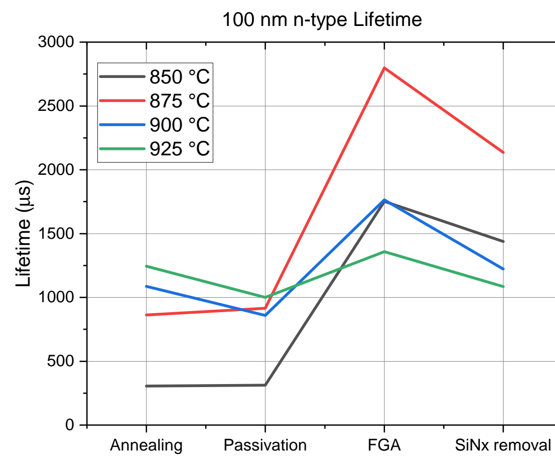

Figure 4.22: Lifetimes of 100 nm n-type flat test samples.

The iV_{oc} of the different annealing temperature samples range between 711 to 734 mV. The highest measurement is obtained for the sampled annealed at 875 °C, which is the 734 mV with a J_0 of 3.9 fA/cm^2. The lowest iV_{oc} is obtained when annealing at 925 °C with 711 mV and a J_0 of 7.3 fA/cm^2. The highest measured lifetime is obtained for the 875 °C annealed sample also, with a corresponding value of 2798 μs. The lifetimes are slightly lower for the 850 and 900 °C annealed temperatures, which are 1752 and 1763 μs, respectively. Again, the lowest measured values are obtained for the 925 °C annealing temperature and is 1358 μs. For the rear side n-type layer the annealing temperature that shows the best performance is 30 minutes at 875 °C.

4.2. ECV measurements

The doping profiles for the samples discussed in the previous section were investigated by fabricating unique test samples and performing ECV measurements. Being able to observe the doping profiles is helpful for visualizing the diffusion of the dopants into the semiconductor material.

The first ECV sample is shown in figure 4.23, this structure is the basic commercial Cz wafer with a chemical passivation, a 20 nm thick Al_2O_3 layer followed by a 75 nm thick SiN_x capping layer. During the local carrier-selective contact solar cell fabrication an annealing step is performed after the doped a-SiO_x:H deposition. The majority of the semiconductor's surface will not be in contact with the doped a-SiO_x:H, this sample investigates what happens to the p^+ diffused doping layer during the annealing for these areas. The RCA cleaned sample is cut into four pieces and annealed at 850, 875, 900 and 925 °C for 30 minutes prior to the application of the passivation layers. After the passivation an FGA step is performed followed by removal of the SiN_x layer. The ECV doping profiles of these samples are shown in figure 4.24.

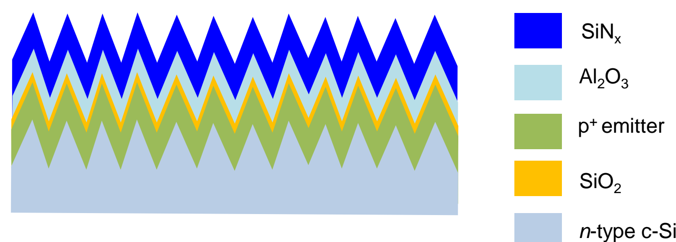

Figure 4.23: Schematic structure of the commercial Cz wafer with a passivation layer.

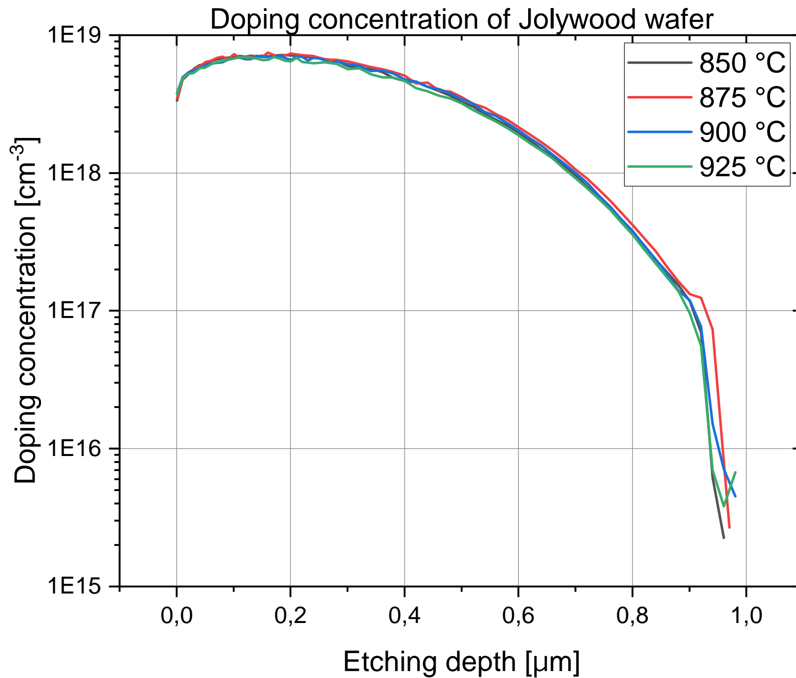

Figure 4.24: Logarithmic visualization for the doping profile of an annealed and passivated commercial Cz wafer.

It is clear that the dopants present near the surface of the wafer have diffused further into the semiconductor bulk material, since the doping concentration at an etching depth of 0.20 μm is higher that directly at the surface. At 0.50 μm into the semiconductor material the doping concentration is equal to that of the surface. The highest obtained doping concentration over this domain is 7.18 x 10^{19} cm^{-3}. When approaching a depth of 1.00 μm the doping concentration has decreased several orders of magnitude. There is little noticeable difference for the various annealing temperatures up until an etching depth of about 0.90 μm, it appears that for 875 °C the diffusion has reached slightly further than the others. The final local carrier-selective solar cells' area will primarily consist of this type of surface, where the highest doping concentration will not be directly at the semiconductor surface.

The second ECV test sample investigates the how the doping profile changes when the p^+ doped poly-SiO_x is applied on the surface. An RCA cleaned sample is chemically passivated and p^+ doped a-SiO_x:H with a thickness of 100 nm is deposited on the front side. Annealing takes place at 850, 875, 900 and 925 °C for 30 minutes and a SiN_x capping layer is deposited afterwards. The structure of this sample is given in figure 4.25. The measured doping profile is shown in figure 4.26.

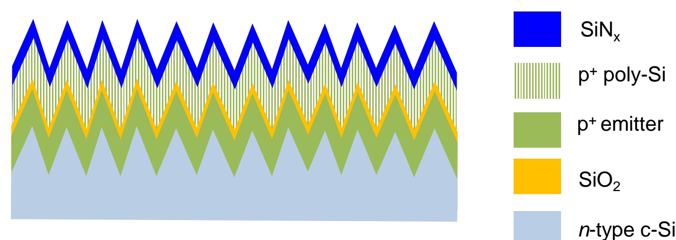

Figure 4.25: Schematic structure of the commercial Cz wafer with a p^+ doped poly-SiO_x.

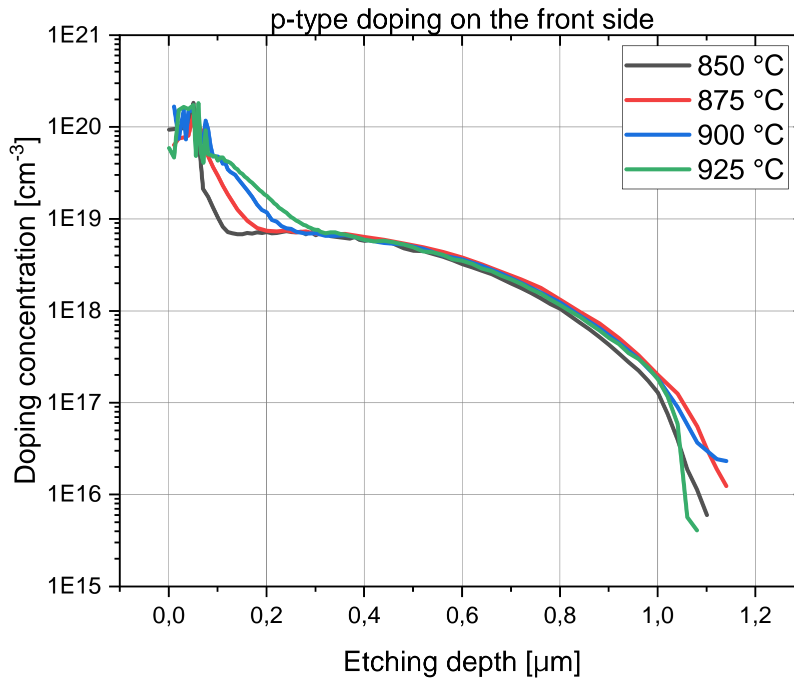

Figure 4.26: Logarithmic visualization for the doping profile of a p^+ doped poly-SiO_x commercial Cz wafer.

The difference of the doping profile between this p^+ doped poly-SiO_x sample and the previous passivated wafer is seen in the first 0.20 μm of the measurements. The deposited doped poly-SiO_x reached carrier concentrations upwards of 1.00 x 10^{20} cm^{-3}, albeit very irregular. The first 0.10 μm of the measurements show a high level of fluctuation for the measured carrier concentration for all four samples, there is no clear annealing temperature providing a uniform doping profile. The influence of the annealing temperature is more visible in the 0.10 to 0.30 μm etching depth range, where there is an apparent difference in the carrier concentration. These doping profiles suggest that a higher annealing temperature promotes further diffusion into the semiconductor bulk. At an annealing temperature of 850 °C the doping concentration deceases the most rapidly and earliest when compared to the other annealing temperatures. At 0.10 μm the doping profile for the 850 °C annealing p^+ doped poly-SiO_x sample is equal to that of the passivated wafer without added doping. The next doping profile to decrease in doping concentration is that of the 875 °C annealed sample. The diffusion gain of the dopants is higher than that of the 850 °C, but lower than that of 900 and 925 °C annealed sample. At an etching depth of 0.20 μm the doping profile for the 875 °C sample is at the same value to the non-doped passivated wafer. This also is the case for the 900 °C annealed sample at and etching depth of 0.25 μm, and at 0.30 μm for the 925 °C sample. The doping profiles for these annealing temperatures will most likely be present at the local carrier-selective contacts depending on the annealing temperature used following the PECVD.

The n-type on the rear side is deposited according to the structure shown in figure 4.27. A commercial wafer is KOH polished to remove the p^+ diffused doping layer and changed from a textured surface to flat. The wafers are RCA cleaned and chemically passivated, subsequently a n-type doping layer is deposited by PECVD. Four samples are annealed at 850, 875, 900 and 925 °C for 30 minutes, followed by the deposition of a SiN_x layer. The measured doping profiles for these samples are shown in figure 4.28

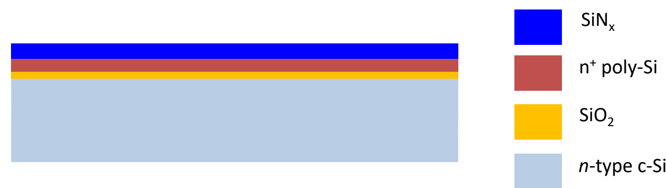

Figure 4.27: Schematic structure of the commercial Cz wafer with a n-type doping on a flat surface.

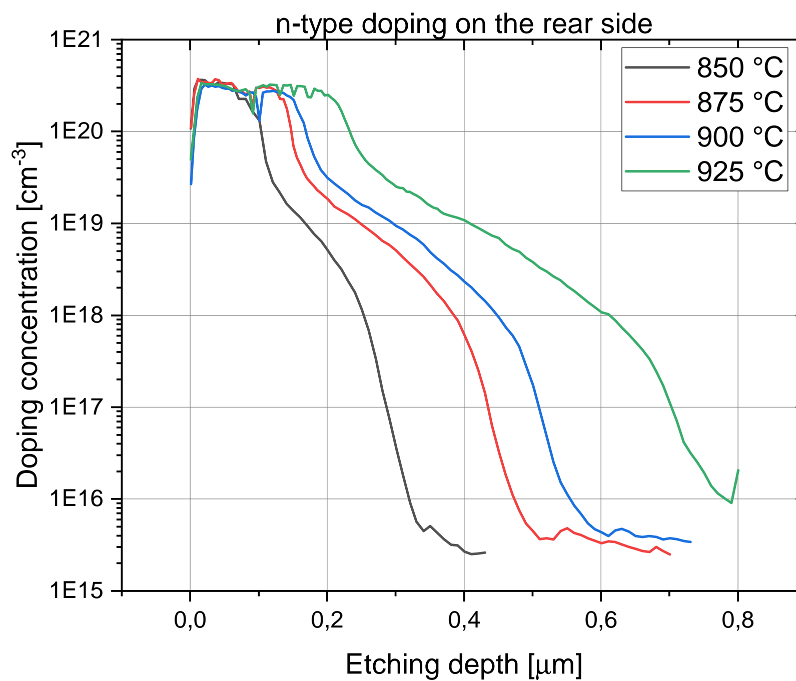

Figure 4.28: Logarithmic visualization for the doping profile of a n-type doped KOH polished commercial Cz wafer.

These four measurements show the most deviation between when compared to the previous profile shown in figure 4.24 and 4.26. A similar trend for the diffusion depth can be observed: a higher annealing temperature results in a further diffusion of the dopants into the semiconductor bulk. At the lower etching depth there is more consistency in the doping concentration when compared to figure 4.26. For the lowest annealing temperature of 850 °C the doping profile starts to rapidly decrease at an etching depth of about 0.10 μm, for the highest temperature of 925 °C this happens at approximately 0.25 μm. Most of the doping profiles decrease several order of magnitude after an etching depth between 0.25 to 0.60 μm. Depending on the annealing temperature used for the local carrier-selective solar cell fabrication, doping profiles on the rear side of the wafer are expected to follow similar doping profiles as seen in figure 4.28.

5

Poly-SiO_x finger solar cell fabrication and performance

The fabrication process for the local poly-SiO_x finger solar cell is given in this chapter. The optimization processes described in previous chapters are applied for various steps throughout the process. Section 5.1 describes the fabrication process for the local poly-SiO_x finger solar cells and visualizes the entire process in a flowchart. The performance of the local poly-SiO_x finger solar cells were characterized by measuring the J-V curves and the EQE. Section 5.2 shows these results and section 5.3 explains some of the observed power loss.

5.1. Poly-SiO_x finger solar cell fabrication

The optimization processes described in previous chapters are applied for various steps throughout the fabrication. For several steps it is possible to process multiple wafers, however some processes have to be performed one wafer at a time thus making it quite time intensive. The solar cell structure that should be the result of the fabrication process is given in figure 5.1. This structure shows the p^+ local poly-SiO_x fingers deposited on top of the p^+ diffused doping layer, with the poly-SiO_x finger also in contact with the metal contact. The remaining surface area is deposited with a passivation layer. The rear side has a n-type doping layer and a full metal back contact. The process can be divided into general segments:

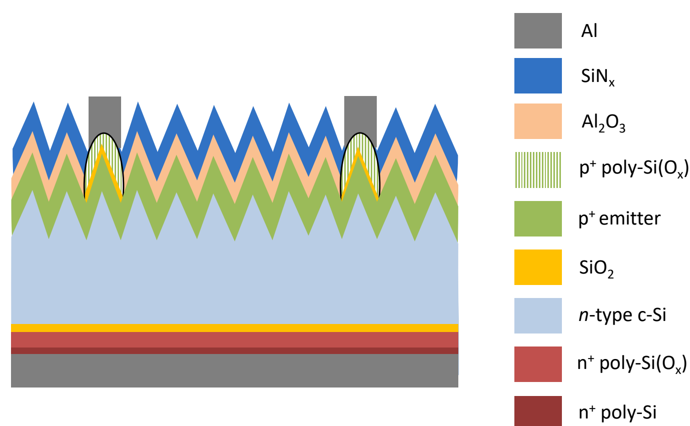

Figure 5.1: Proposed p^+ poly-SiO_x finger solar cell structure.

1. **Wafer preparation**. The commercial Cz wafers are too large for processing. Using the laser cutter located in the ESP lab basement, square wafers are cut from the larger wafer that are approximately 90 mm by 90 mm. Alternatively the dimensions of standard circular 4-inch wafers can be used to

cut into the larger commercial Cz wafer, however this will result in more waste material. For the 180 μm thick wafers a speed of 200 mm/sec and a loop count of 100 should be sufficient. RCA cleaning is subsequently implemented for cleaning the wafers since the surface potentially holds contaminants, this consists of an RCA 1 and RCA 2 bath in which the wafers are deposited for 10 minutes each. Rinsing baths are used between every soak in a chemical bath. The wafers have to be dried using a nitrogen gun one separately. Square laser cut wafers do not properly fit in automated drying tools, and circular laser cut wafers are too fragile and will not survive the high rotation speed. To ensure that future lithography processes can be performed without any impediment a localized polishing of the wafers is required, this consists of a lithography step and a wet etching step.

By far the most difficult aspect of the poly-SiO_x fingers is the alignment. The alignment is performed with the alignment markers, as shown in figure 3.11. The issue arises from the substrate surface that is used for the poly-SiO_x finger deposition. The commercial Cz wafers are front side textured, thus the markers are deposited through the hard mask on the textured surface. One of the properties of the textured surface is that it reduces reflection. During the alignment it becomes very difficult to observe the markers, the purpose of the alignment is now obsolete since no suitable reference points are available. Given the very small room for error the alignment becomes a gamble when it is attempted. Figure 5.2 shows several examples of the misalignment. During the alignment the line going through the four images has to be positioned exactly in the black gap between the two white structures and should end at the edges of the white structures. The black gap indicates the placement of the poly-SiO_x finger, the white area are structures from the alignment mask.

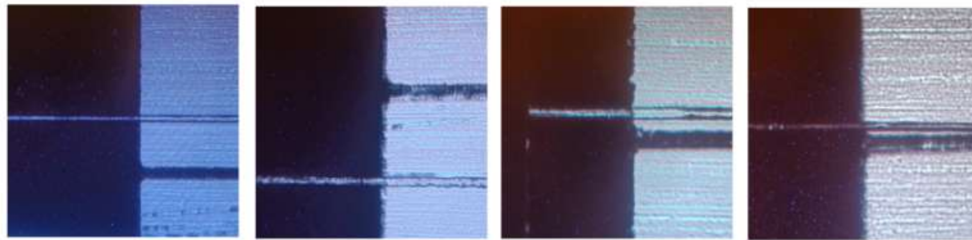

Figure 5.2: Examples of misalignment. From left to right: high vertical overshoot and high horizontal overshoot, high vertical undershoot and high horizontal overshoot, slight vertical overshoot and slight horizontal overshoot, slight vertical overshoot and slight tilt.

The misalignment becomes a problem when the lithography step is applied. At a certain point in the process an Al_2O_3 and SiN_x layer are deposited on top of the poly-SiO_x fingers, applying photoresist on all areas but the poly-SiO_x fingers is required to etch away these layers covering the poly-SiO_x. Otherwise when applying the metallization there is no contact between the poly-SiO_x finger and the metal contacts. A solution has to be applied before the Al_2O_3 and SiN_x layers are deposited which will preserve the functionality of the alignment, with this solution being localized polishing of the commercial Cz wafer. Flat surfaces are more desirable when performing the alignment; there is more reflection from the flat surface than the textured surface. By introducing localized polishing prior to all the depositions the area suited for the marker placement can be transformed from textured to flat. Figure 5.3 shows a schematic structure of a commercial Cz wafer that has been locally polished.

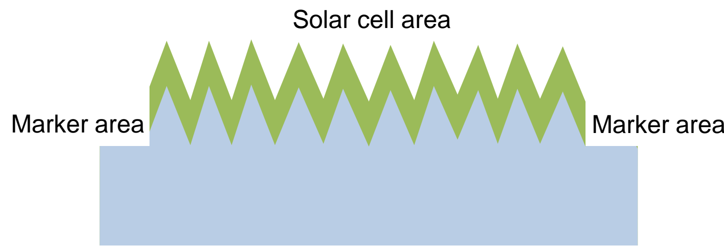

Figure 5.3: Schematic structure of the localized polished commercial Cz wafer to define the textured area for the solar cells and flat area for the markers.

This locally polished wafer still has the textured p$^+$ diffused doping layer on the front side and now on the edges of the wafer the doping layer is removed to make the surface flat. Lithography is used for specifying the area that is protected during the localized polishing. There is no lithography mask available to define the area for the localized polishing, but it is possible to create a makeshift mask. Using lithography mask scraps, a glass plate and some tape a mask suitable for localized polishing can be constructed that will preserve the p$^+$ diffused doping layer for the solar cells, but will polish the area used for the marker placement. Figure 5.4 shows the localized polishing mask.

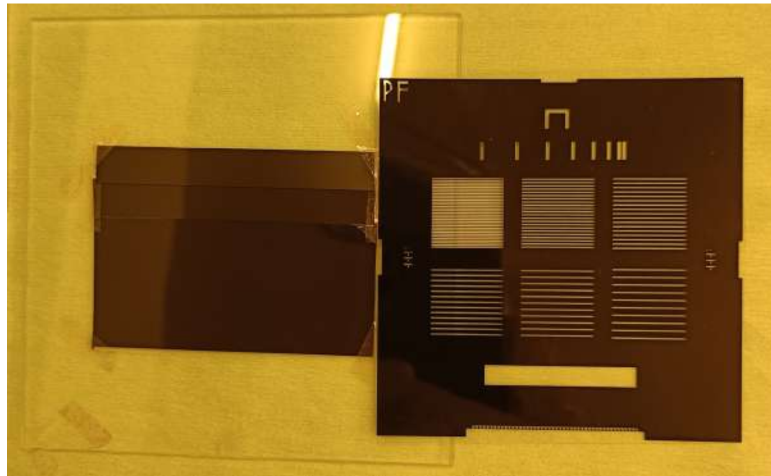

Figure 5.4: The localized polishing mask (right) besides the poly-SiO$_x$ finger solar cell mask.

A photoresist layer with a 4 μm thickness is deposited on the commercial Cz wafers to preserve the area where the poly-SiO$_x$ finger cells will be deposited. The localized polishing is performed using a poly-etch solution, this solution is a mixture of 69.9 % HNO_3, water and 40.0 % HF in [500:500:15] proportions. Given that the amount of HF present in the solution is relatively little, stirring the mixture prior to etching is desirable for creating a homogeneous solution. The wafers are etched for 10 minutes, longer than 10 minutes will cause the photoresist to degrade and separate from the wafer surface. The localized polished wafer used for further processing in shown in figure 5.5. The markers deposited on the polished surface are significantly more observable during the alignment process with an Al_2O_3 and SiN_x layer deposited on top of it, as shown in figure 5.6. Without localized polishing the alignment was arduous and tedious, however with localized polishing the alignment can be carried out effortlessly and resolved the majority of the alignment issues.

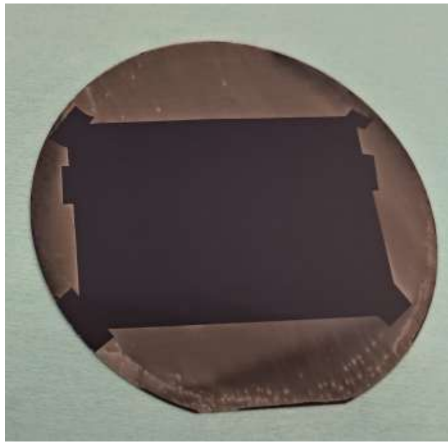

Figure 5.5: Localized polished commercial Cz wafer.

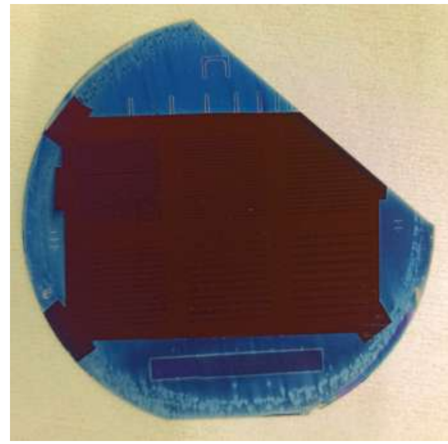

Figure 5.6: Localized polished wafer after passivation.

The application for both the positive photoresist and negative photoresist are similar. This localized polishing has to be performed using positive photoresist specifically the AZ ECI 3012 photoresist [79]. The wafer is placed on the spin coater as centered as possible. If the spin rotation of the wafer is not centralized, or if the photoresist is not situated in the center of the wafer, the distribution of the photoresist coating might not be uniform or some parts of the wafer might not receive any photoresist at all. A vacuum connection is made between the chuck on which the wafer is situated and with the wafer itself. The recipe for positive photoresist consists of two steps:

(a) A 5 seconds rotation at 500 rpm.
(b) A 20 seconds rotation at 3450 rpm.

The first step broadly distributes the photoresist over the wafer surface, the second step increases the rotation speed significantly in order to obtain the desired thickness. The desirable thickness for every lithography step utilized in fabrication process is 4 μm. A hotplate heated up to a temperature of 90 °C facilitates the post-coating softbake, the wafer is placed on the hotplate for 4 minutes. The general rule of thumb for the bakes for photoresist coating is 1 minute for every μm of photoresist. The exposure is performed for 19 seconds using a standard front soft contact alignment. The mask utilized for the exposure has a rectangle shape with the intent to preserve this area for the localized polishing. After removing the wafer from the aligner the pattern should be slightly visible in the photoresist. The post-exposure bake following the exposure takes place in a small heating oven for 4 minutes at 125 °C. The final step uses standard MF-322 developer for a single minute deposited on top of the wafer, with the wafer placed on top of a beaker. It is problematic to fully submerge the wafer in a bath filled with the MF-322 developer, not only is it a waste of developer but the wafer might break when removing it from the bath. The excess developer is carefully rinsed from the surface and the wafer is dried with the nitrogen gun. The front side of the wafer now has an area on the front side defined for the localized polishing. This entire process is now repeated for the rear side, but without the exposure step. The purpose of this photoresist deposition is to protect the rear side of the wafer from the wet etching step which will follow. The surface of the rear side is flat, as opposed to the textured front side, however the coating recipe is still suitable to fabricate a decent protective layer.
The commercial Cz wafer currently has a front side isolated photoresist layer and a rear side full area photoresist layer, the localized polishing now has to be performed. Rinsing the wafer with DI water and removing the photoresist using IPA is the final step after the localized polishing, figure 5.7 shows how the commercial Cz wafer looks after this process.

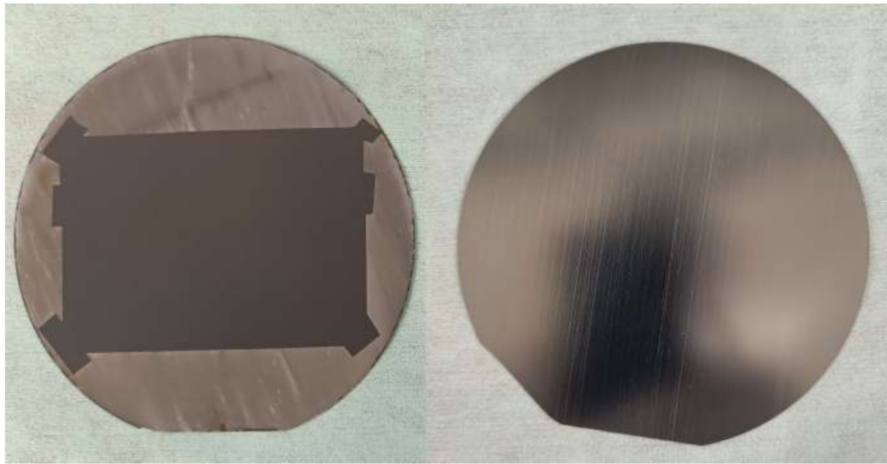

Figure 5.7: Front side (left) and rear side (right) of the commercial Cz wafer following the localized polishing.

The next step is to perform the RCA cleaning for removing any unwanted particles from the surfaces. Given the amount of chemicals involved in the cleaning process, preferably multiple wafers can be cleaned simultaneously. RCA 1 is performed for 10 minutes at 70 °C and RCA also for 10 minutes at 80 °C shortly after completing the RCA 1. Once the RCA cleaning is finished, the wafers are prepared for the first depositions. The schematic structure of the wafer after these steps is that of the *structure 1)* in figure 5.15.

2. **PECVD depositions**. Applying the local carrier-selective contacts through the hard mask starts with the PECVD deposition of the a-SiO$_x$:H. Prior to the deposition the native oxide present on the wafer surface is removed by using a low concentration HF bath. This process is followed by the chemical passivation through a nitric acid solution of 69.5 % at room temperature. The wafer is submerged in this solution for 30 minutes to form a ultra-thin SiO$_x$ layer.
The PECVD depositions will first deposit the doped a-SiO$_x$:H through the hard mask on the textured front side, shortly after the n-type a-SiOx will be deposited on the flat rear side. Figure 5.8 gives an example of the commercial Cz wafer and hard mask together in the holder. There is a possibility that both the commercial Cz wafer and the hard mask can move during the placement in the holder, thus it is essential to be extra careful to avoid any misalignment when placing the holder in the AMOR load lock. The hard mask has to be lined up with the isolated area of the locally polished wafer. Waiting for thirty minutes is required for the substrate to heat up to the deposition chamber temperature of 180 °C. The sample is inserted in the first chamber of the AMOR, this chamber will have access to the boron gas to create a p-type doping. The doped a-SiO$_x$:H is deposited for 5 minutes and 22 seconds at a power 15 Watt and a pressure 1.5 mbar, the plasma is guided through the hard mask and this results in 50 nm thick doped a-SiO$_x$:H fingers. Figure 5.8 shows an example of the hard mask PECVD deposition. Next the holder is removed from the chamber, the wafer and hard mask removed from the holder and the wafer is placed in the holder again upside down. Directly after the front side deposition the rear side n-type a-SiOx will be deposited. To create the n-type doping, the holder is placed in the second chamber which has access to phosphine gas. A 100 nm thick n^+ a-siOx layer is deposited with a power of 5 Watt and a pressure of 1.0 mbar, given the low power the deposition will take 23 minutes and 40 seconds. During the last 2 minutes of the deposition the CO_2 present in the chamber is turned off, the deposition will change to an n^+ a-Si layer. This part of the deposition will function as a protective layer for the rear-side doping. Following a successful deposition of the front side textured p^+ doped a-SiO$_x$:H fingers and rear side flat full area n^+ a-siOx annealing is performed at 850 °C for 30 minutes. During the annealing process solid-phase crystallization will take place and transfer the a-SiO$_x$:H to poly-SiO$_x$. The schematic structure of the current wafer is that of *structure 2)* presented in figure 5.15.

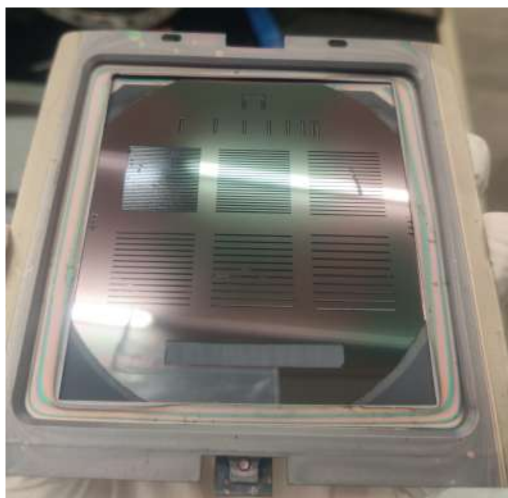

Figure 5.8: The hard mask with a square locally polished commercial Cz wafer below it placed in the holder for the PECVD deposition.

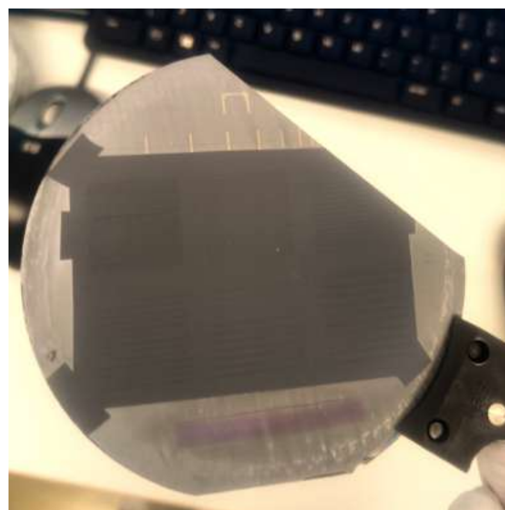

Figure 5.9: Deposition of a-SiO_x:H fingers through the hard mask on a locally polished commercial Cz wafer.

3. **Passivation**. Providing the front surface with passivating layers are the next depositions, both will be performed in the Kavli Nanolab. Prior to entering the lab, a short HF dip is performed to remove the native oxide which has grown on the surface. The Al_2O_3 layer which will be deposited using ALD will be 20 nm thick, this is achieved by depositing for 240 cycles at a temperature of 105 °C. Given that the rear side of the wafer is flat, an issue that could present itself whilst the load lock of the ALD Oxford is pumping down is that the wafer might move out of position. There is little friction between the rear side of the wafer and the moving platform onto which the wafer is positioned. During the pumping down procedure to reduce the pressure in the chamber, the air between the moving platform and the wafer causes the wafer to slide from its place. An solution to this issue is employing a dummy wafer onto which the commercial Cz wafer is positioned. If this dummy wafer has a textured surface there is a higher chance of the wafer maintaining its position. When the pressure in the load lock is sufficient the moving platform transfers the wafer to the deposition chamber, this all occurs automatically when the recipe is selected in the software. Once finished, the wafer is transferred back to the load lock for further processing. The SiN_x layer is deposited on both sides of the wafer next, however only one surface can be processed per deposition. The wafer is placed on a heated table at a temperature of 400 °C. For the textured front side the PECVD deposition is performed for 5 minutes and 36 second, resulting in a SiN_x layer approximately 75 nm thick. For the flat rear side the PECVD deposition is performed for 8 minutes, resulting in a SiN_x layer approximately 100 nm thick. The different thickness for the SiN_x layer is relevant when performing a simultaneous wet etch for both the front and rear side SiN_x removal, the flat surface etching rate is higher than that of the textured surface. The structure of the current wafer is that of *structure 3)* given in figure 5.15, the front side and rear side of the wafer are presented in figure 5.10 and 5.11.

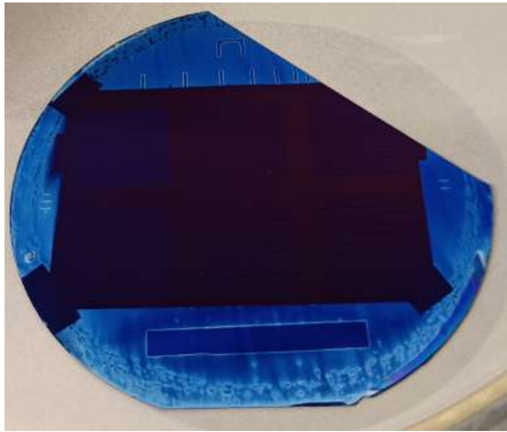

Figure 5.10: Al_2O_3 and SiN_x deposited on the textured localized polished front side of the commercial Cz wafer with local doped poly-SiO_x fingers.

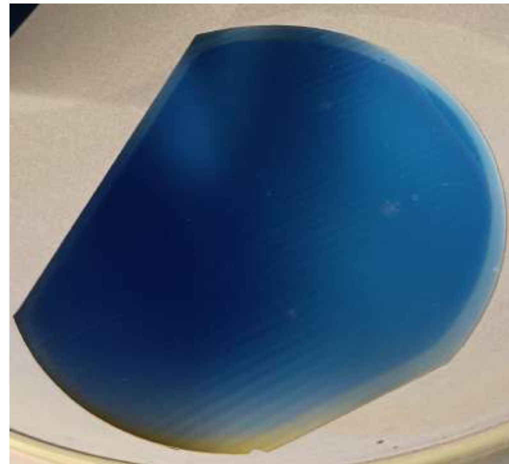

Figure 5.11: SiN_x deposited on the flat rear side of the commercial Cz wafer.

4. **Lithography**. At the moment there is unwanted material present on top of the local doped poly-SiO_x fingers, a 20 nm Al_2O_3 and a 75 nm SiN_x layer. Removing this material is the next step, isolating the area which needs to be removed is required. Using lithography a pattern that is of the same design as that of the doped poly-SiO_x fingers is created. Negative lithography is used to form an opening directly on top of the local poly-SiO_x finger, the negative photoresist which is used is the AZ nLOF 2020 [80]. The coating recipe for the negative photoresist is different than that of the positive photoresist, the steps are:

   (a) A 10 seconds rotation at 700 rpm.
   (b) A 30 seconds rotation at 1060 rpm.

   A 4 μm thick negative photoresist coating is established when following this recipe. Furthermore, with other the differences of the negative photoresist application is a double exposure time of 28 seconds and a double post-coating baking time of 8 minutes for the protective rear side coating. An extended exposure is required to properly apply the pattern of the isolation into the coating. The extended post-coating bake increases the strength of the coating for the rear side. This is required for the wet etching process that follows, if the extended post-coating bake is not performed then the photoresist will detach during the wet etching and areas that should be preserved will be subjected to the etching process. This lithography process is also the reason why the initial localized polishing was performed. The markers used as reference points for the lithography alignment of below a Al_2O_3 and SiN_x layer. Fortunately on the flat surface they are visible, however if they are deposited on the textured surface this become impossible to locate and a proper alignment can not be conducted. The structure of the wafer once the lithography is performed is that of *structure 4)* in figure 5.15.

5. **Wet etching**. A short wet etching step will remove the 20 nm Al_2O_3 and 75 nm SiN_x layers. Two chemicals are used for the wet etching: BOE 1:7 and an HF dip. The etching rate of BOE 1:7 is typically between 30 to 80 nm/min, depending on the quality of the layer that will be etched. The etching rate of the HF dip, which is at a concentration of approximately 0.55 %, is only a few nm/min. Experimentally the etching times were determined by etching away the Al_2O_3 and SiN_x layers on dummy wafers. The etching process is performed using the following etching times:

   (a) 1 minute and 30 seconds BOE 1:7 wet etch.
   (b) 3 minutes 0.55 % HF dip.

   Following the wet etching, the excess Al_2O_3 and SiN_x material which was present on top of the doped poly-SiO_x finger has now been removed. The structure of the wafer following this process is that of *structure 5* shown in figure 5.15.

6. **Metallization**. Applying the metal contacts on the front and the rear side is the final step, front side metallization is applied using one of the lithography masks as shown in figure 3.10, and the rear side metallization is deposited through the metallization mask. Once again, negative lithography is applied to isolate an area on the front side through which a thermal evaporation of aluminium may be deposited. The recipe for the negative photoresist is used to provide a 4 μm thick pattern on the front surface that has an opening of 10 μm for the fingers and 2 mm thick busbars surrounding every individual solar cell. A protective rear side coating is also applied to prevent any of the evaporated aluminium from reaching the rear side of the wafer during the metallization. The recipe of the front side metallization is a 700 nm thick aluminium layer deposited at a pressure of 2.00 $^{-5}$ $mbar$. The aluminium is deposited on top of the doped poly-SiO$_x$ finger and on the protective photoresist. All the excessive aluminium can be removed through a lift-off process. The lift-off is a technique which allows the transfer of a pattern on a substrate using a sacrificial material, the photoresist in this case will be that material. The process is visualized in figure 5.12.

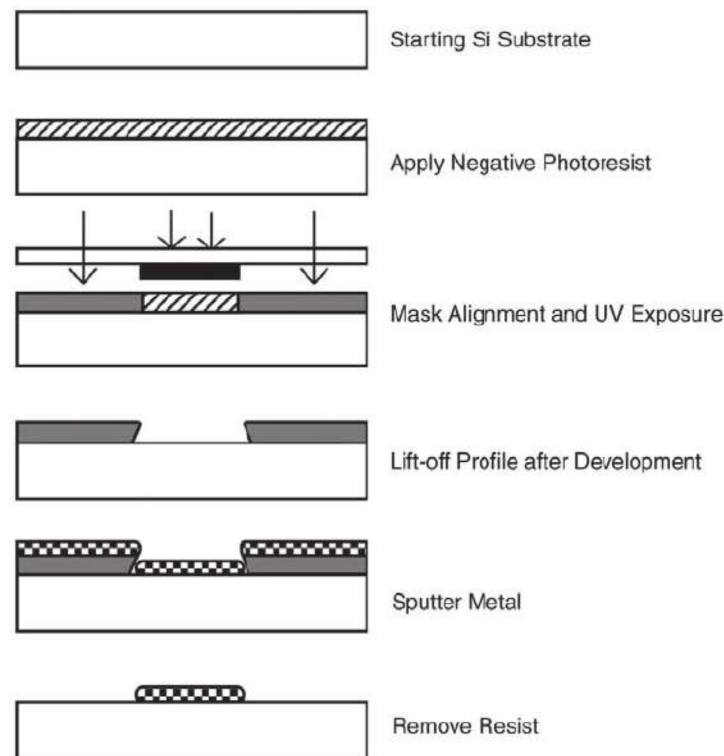

Figure 5.12: Schematic procedure of the lift-off process [81].

Removing the negative photoresist from the substrate requires NMP and an ultrasonic bath. The NMP will over time decrease the strength of the negative photoresist and cause it to detach from the substrate surface. The ultrasonic bath promotes the removal of the sacrificial layer since it can only be reached from the sides of the openings on the wafer. Eventually all the photoresist will have been removed from the substrate and what is left is a front side metallization of 700 nm thick aluminium metal contacts on the textured surface. FGA is performed after the front side metal contacts are in place, the FGA will provide hydrogen to the dangling bonds in the passivation layer to reduce the interface surface trapping density. Additionally a low ohmic contact is formed between the doped poly-SiO$_x$ fingers and the aluminium on the front side.
Currently the rear side is still covered with the SiN$_x$ capping layer, the rear side metallization can not be performed with this layer still present. Removing the SiN$_x$ layer requires the front side of the wafer to be covered with a positive photoresist protection layer and a subsequent BOE 1:7 wet etching and HF dip. The etching times for the rear side have also been determined experimentally using dummy wafers, with the two steps as follows:

(a) 2 minutes BOE 1:7 wet etch.
(b) 3 minutes 0.55 % HF dip.

The rear side n-type poly-SiO$_x$Ox is now exposed and full area silver is deposited using thermal evaporation through the metallization mask. The recipe for the rear side metallization deposits 1 μm of silver at a pressure of 5.00 $^{-5}$ mbar. The finalized local carrier-selective solar cell is that of *structure 6* shown in figure 5.15, and the physical version is shown in figures 5.13 and 5.14.

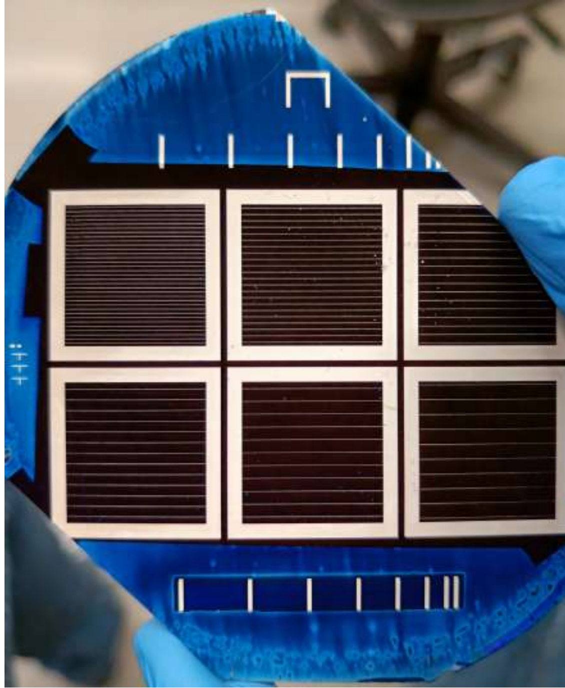

Figure 5.13: Six poly-SiO$_x$ finger solar cells.

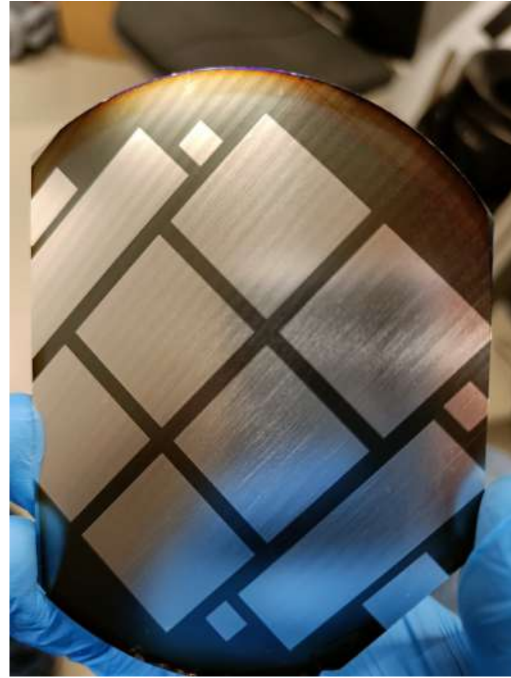

Figure 5.14: Rear side of the poly-SiO$_x$ finger solar cells.

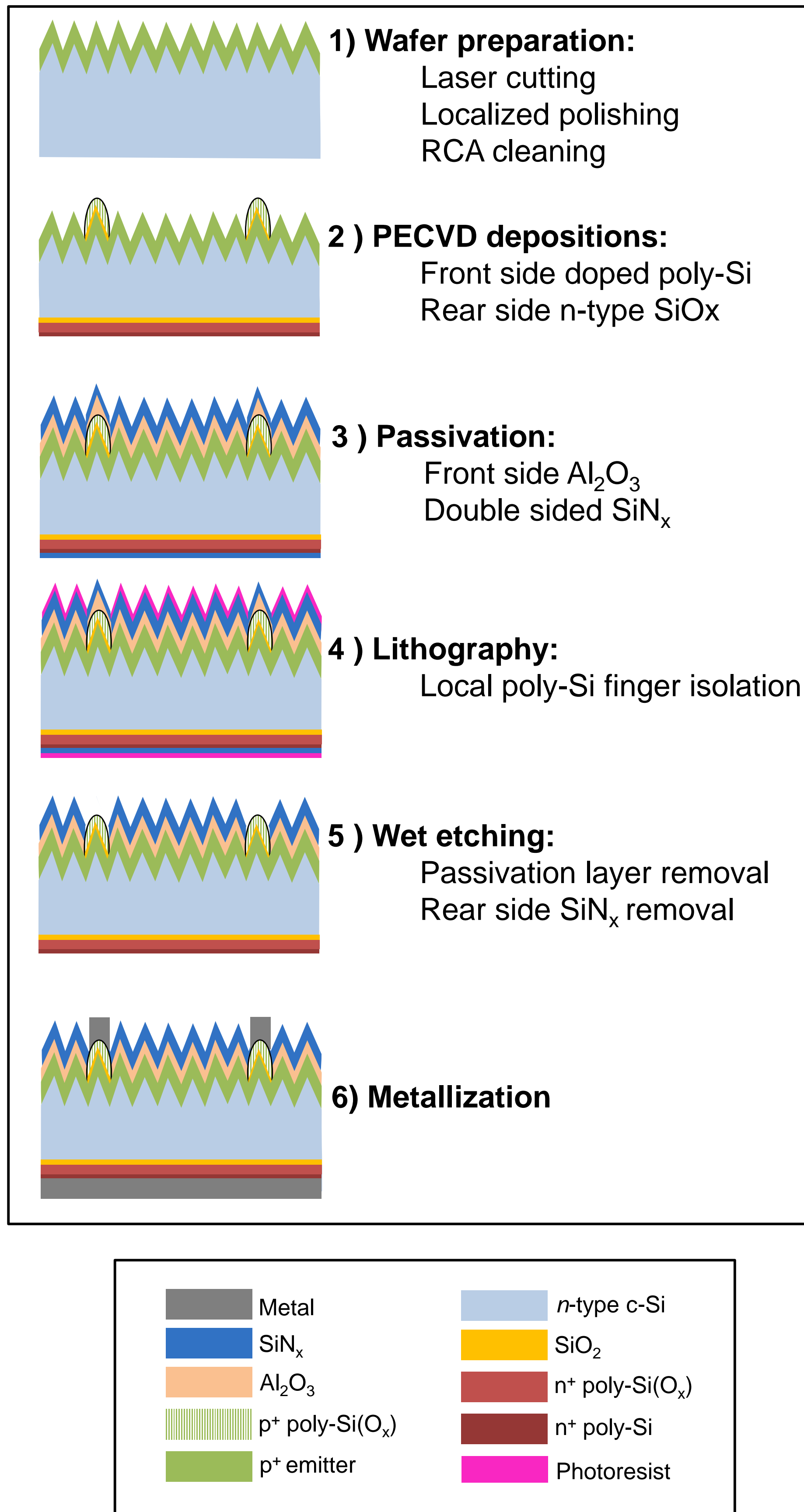

Figure 5.15: Visual flowchart for the local carrier-selective contacts wafers deposited through the hard mask.

5.2. Poly-SiO$_x$ finger solar cell performance

The J-V measurements were carried out using the WACOM solar simulator. The voltage range over which the measurements were performed ranged from -1.00 to 1.00 V. Measurements are taken for every 0.04 V resulting in 52 data points from which a graph can be plotted. Figure 5.16 shows the J-V curves for the poly-SiO$_x$ finger cells, relevant parameters for the poly-SiO$_x$ finger cells are shown in table 5.1.

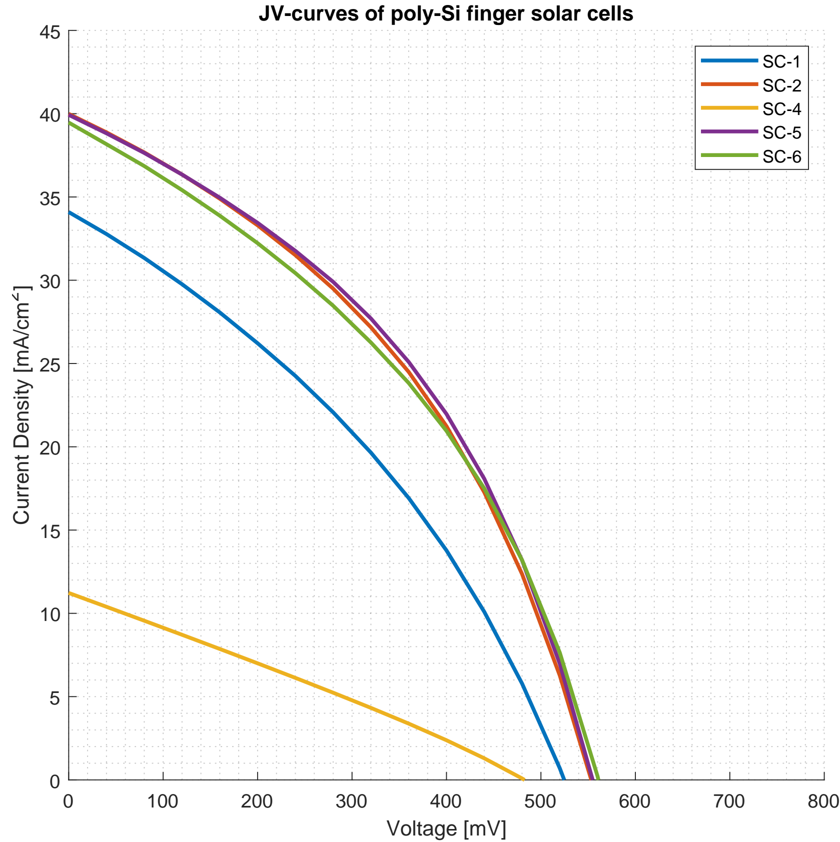

Figure 5.16: JV curves for five poly-SiO$_x$ finger cells.

Table 5.1: External parameters of the poly-SiO$_x$ finger solar cells.

	SC-1	**SC-2**	**SC-4**	**SC-5**	**SC-6**
J_{sc} $[mA/cm^2]$	34.09	39.98	11.23	39.93	35.67
V_{oc} $[mV]$	525.0	553.0	483.0	555.0	562.0
FF [%]	35.1	39.9	27.1	40.8	40.5
Efficiency [%]	6.29	8.82	1.47	9.03	8.12

Despite six poly-SiO$_x$ finger cells present on the wafer only five plots are present in figure 5.16. Because SC-3 has the top-right of the cell broken off it is not possible to take measurements of its performance, which is why this cell has not been included. SC-4 has a lower V_{oc} and significantly lower J_{sc} than the other measured cells, this can also be explained by breakage of the wafer. The bottom-left corner of the busbars have suffered a break creating a bridge between charge carriers on the front and rear side of the wafer, thus resulting in significant recombination. The final cell showing a lower performance of is SC-1, this cell has an issue with the continuity of the front side metallization fingers. Near the left side of busbars, the connection between the fingers and the busbar is broken along the length of the busbar. The interruption of the finger formation prevents charge carriers from taking the shortest route to the external circuit for charge carrier collection. The longer travel time of the charge carriers increases

the chance of recombination in the metal contacts, leading to a lower performing solar cell. The origin of this disruption in the metal fingers is most likely a faulty area of the lithography implemented for the metal finger isolation. If the isolated finger area was not well defined then it is possible photoresist was present on top of the doped poly-SiO$_x$, during the lift-off process the aluminium on these location was removed. Alternatively, the aluminium deposited during thermal evaporation might have separated during the lift-off process in the event that a low level of uniformity was present at these specific locations.

The three cells that show similar V_{oc} and J_{sc} measurements are SC-2, SC-5 and SC-6. These are the solar cells with 22, 11 and 10 fingers, respectively. SC-5 has the highest measured efficiency with 9.03 %, with a corresponding V_{oc} of 555 mV, J_{sc} of 39.93 mA/cm^2 and fill factor of 40.8 %. Second is SC-2 with an efficiency of 8.82 %, with slightly a lower V_{oc} of 553 mV but a higher J_{sc} of 39.98 mA/cm^2 and fill factor of 39.9 %. Finally SC-6 has an efficiency of 8.12 %, V_{oc} of 562 mV, J_{sc} of 35.67 mA/cm^2 and fill factor of 40.5 %. There does not seem to be a direct correlation between the MFC and the external parameters, since the measured efficiency is the highest when 11 fingers are implemented in SC-5. Apart from the J-V characteristics, the EQE performance of the solar cells were also measured, these are presented in figure 5.17.

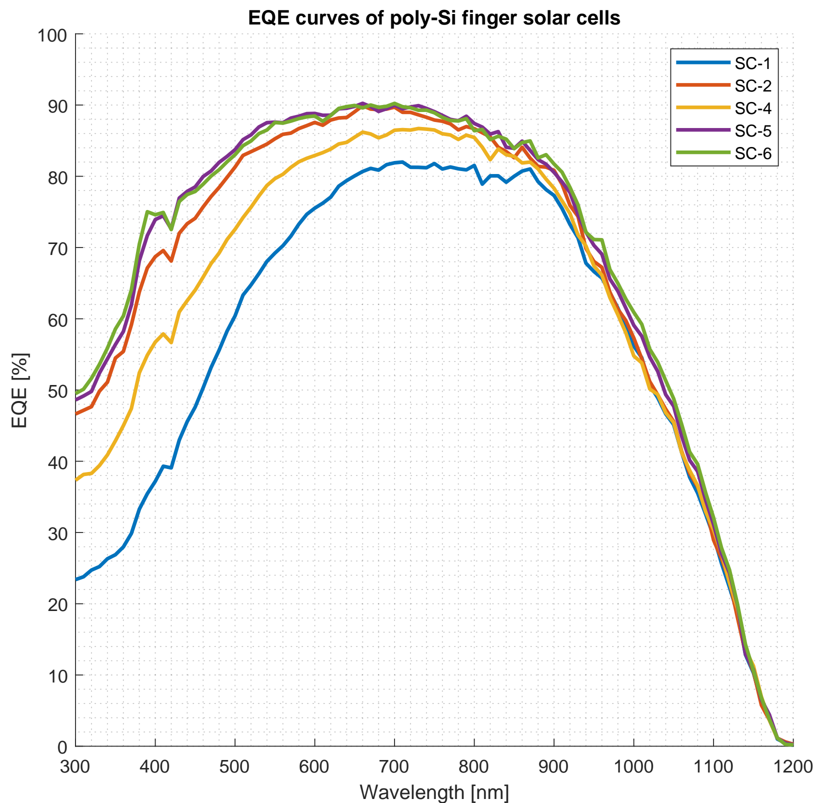

Figure 5.17: EQE curves for five poly-SiO$_x$ finger cells.

Similar to the J-V measurements, SC-1 and SC-4 given the mechanical defects present in the solar cells. There remaining solar cells that showed similar trends for the J-V curve also have similar EQE curves. At low photon wavelengths the number of collected charge carriers is approximately 50 %, with the highest obtained values reaching 90 % for wavelengths between 500 to 900 nm. Using the EQE values it is possible to calculate the $_{int}J_{sc}$ by using equation 2.5, the values of these calculations are presented in table 5.2.

Table 5.2: Integrated short-circuit current density of the poly-SiO$_x$ finger solar cells.

	SC-1	**SC-2**	**SC-4**	**SC-5**	**SC-6**
$_{int}J_{sc}$ $[mA/cm^2]$	29.61	33.91	32.27	34.70	34.79

The $_{int}J_{sc}$ shows lower values for the better performing poly-SiO$_x$ finger solar cells when compared to the J-V measurements. These values for the J_{sc} can be considered more accurate than those of the J-V measurements due to the EQE measurement being independent from the contact area of the solar cells. The solar cell area may not be properly defined during the J-V measurements thus giving inaccurate results. These new $_{int}J_{sc}$ values would suggest that the performance of the poly-SiO$_x$ finger solar cells is even lower. By combining the $_{int}J_{sc}$ from the EQE measurements with the V_{oc} and FF from the J-V measurements new efficiencies for the solar cells can be calculated as shown in table 5.3:

Table 5.3: External parameters of the poly-SiO$_x$ finger solar cells by combining the J-V and EQE measurements.

	SC-1	**SC-2**	**SC-4**	**SC-5**	**SC-6**
$_{int}J_{sc}$ $[mA/cm^2]$	29.61	33.91	32.27	34.70	34.79
V_{oc} $[mV]$	525.0	553.0	483.0	555.0	562.0
FF [%]	35.1	39.9	27.1	40.8	40.5
Efficiency [%]	5.46	7.48	4.22	7.86	7.92

The champion cell using the $_{int}J_{sc}$ calculated using the EQE measurements is SC-6 which has 10 poly-SiO$_x$ fingers. It has a champion efficiency of 7.91 %, iV_{oc} of 562 mV, $_{int}J_{sc}$ of 34.7 mA/cm^2 and fill factor of 40.5 %.

5.3. Power loss of poly-SiO$_x$ solar cells

The poor performance of the local carrier-selective contacts would suggest that there still is significant recombination taking place. Observations made during the fabrication process might explain some of the loss of power loss.

5.3.1. Auger recombination in the fingers

During the optimization of the full area doped poly-SiO$_x$ it may be noted that the obtained values for the iV_{oc} are lower and the J_0 are significantly higher than those for the passivation layers or the rear side n-type doping. The higher J_0 implies that after the p$^+$ doped poly-SiO$_x$ deposition on the p$^+$ diffused emitter of the commercial wafer there already is significant recombination occurring. The highest measured lifetime during the optimization was 155.64 μs, the low lifetime implies that charge carriers decay quickly due to recombination. Specifically, the recombination causing the low lifetime of the charge carriers in Auger recombination. When the doping concentration is higher, the Auger recombination lifetime is lower. For the structure built using the p$^+$ doped poly-SiO$_x$ deposition on the p$^+$ diffused emitter there is one highly doped region on top of another highly doped region, the high dopant concentration facilitates the high Auger recombination in this area.

5.3.2. Metal contact shunting

With the formation of the front side metallization, a significant amount of shunting is introduced. Shunting occurs when an alternate current path is introduced for the induced photogenerated current [82]. Given the available masks for the metallization, the front side aluminium contacts are in direct contact with the p$^+$ diffused emitter surrounding the poly-SiO$_x$ finger solar cells. This specifically applies for the metal busbars that surround the metal fingers. Figure 5.18 shows an image taken with the SEM that shows the interface between the busbars with the textured p$^+$ diffused emitter surface. The solution for this specific problem would be to produce new lithography mask which will facilitate the metallization by preventing the connection between the p$^+$ diffused emitter and the busbars.

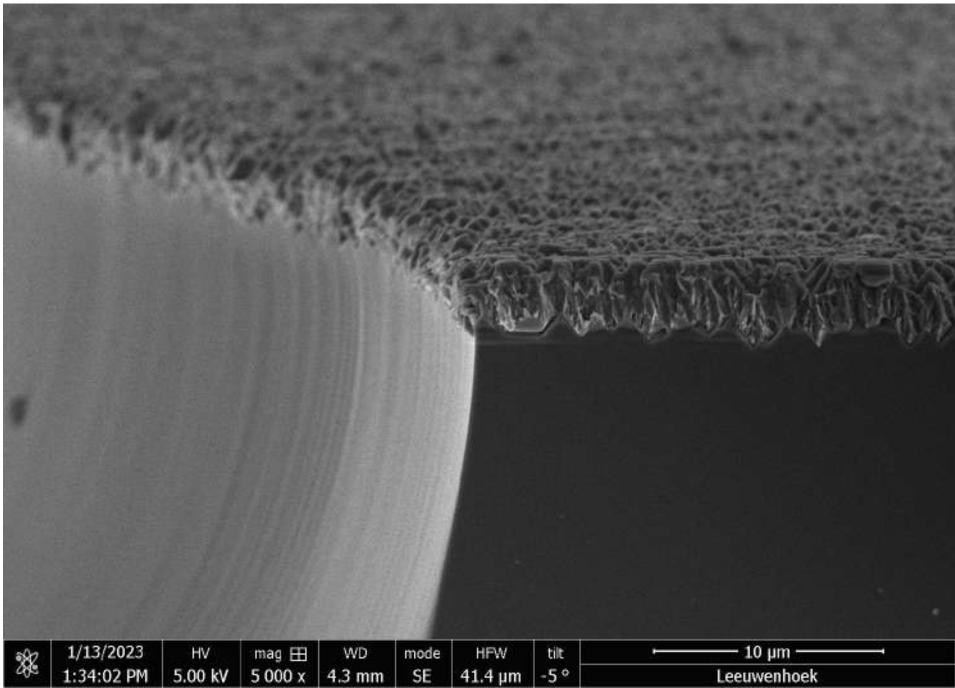

Figure 5.18: SEM image of the busbars in contact with the p^+ diffused emitter.

6

Conclusions and outlook

6.1. Conclusion

The objective of this project is to fabricate local carrier-selective contacts that are deposited through a hard mask, and the local contacts are placed only below the metal contacts with the intent to increase the passivation by lowering the parasitic absorption losses.

The formation of the PECVD deposited a-SiO_x:H was optimized experimentally by investigating the influence of the deposition power and pressure. The power has the most significant influence for the finger formation, a lower power results in irregular fingers while higher power improves the uniformity. A larger power also provides a higher deposition rate. The variation for the pressure shows little influence on the finger formation. The poly-SiO_x fingers deposited for the solar cell fabrication were deposited at a medium power of 15 Watt at a pressure of 1.5 mbar, these parameters provide a manageable deposition controls while also ensuring satisfactory uniformity of the deposited finger through the hard mask. A poly-SiO_x finger with a width of 40 μm is obtained.

The local carrier-selective contacts are deposited on commercial wafers with a p^+ diffused doping layer. An investigation regarding the process parameters affecting the surface passivation was performed by creating symmetrical samples of full-area doped poly-SiO_x and full area Al_2O_3. The full area doped poly-SiO_x with a chemical passivated ultra-thin SiO_2 layer shows the best performance when a PECVD deposited 50 nm thick layer of p^+ doped a-SiO_x:H is annealed at a temperature of 850 °C. The iV_{oc} of this sample has a value of 662 mV and a corresponding J_0 of 156 fA/cm^2. The optimal thickness for the Al_2O_3 passivation layer is achieved by depositing 20 nm thick layer followed by FGA, with an iV_{oc} of 692 mV and a J_0 of 22.4 fA/cm^2.

The results from the optimization were implemented for the carrier-selective solar cell fabrication. A chemical passivation was implemented to provide the surface of the laser-cut commercial wafers with an ultra-thin SiO_2 layer and subsequently 50 nm thick a-SiO_x:H was deposited through the hard mask and annealed at 850 °C to form the poly-SiO_x through solid-phase crystallization. An Al_2O_3 layer deposited by ALD was deposited with a thickness of approximately 20 nm which induces a negative charge density on the surface, repelling minority carrier thus reducing the recombination. A 75 nm thick SiNx layer was deposited by PECVD which functions as a protective layers and reduces the reflection from the solar cell surface. A lithography step was implemented to remove current materials deposited on the carrier-selective contacts, the locally isolated area of the wafer ensures that the alignment can be performed with little difficulty. Front side aluminium contacts and silver full metal back contacts were deposited with thermal evaporation, followed by FGA to passivate remaining dangling bonds to reduce the recombination induce by trap states. A flowchart was created specifically for the fabrication of the hard mask and for the fabrication of local carrier-selective contacts on the commercial wafers.

J-V and EQE measurements of showed that the best performing local carrier-selective solar cell achieved a champion efficiency of 7.91 %, iV_{oc} of 562 mV, ${}_{int}J_{sc}$ of 34.7 mA/cm^2 and fill factor of 40.5

%. The limited performance suggests that despite attempting to reduce the recombination from the parasitic absorption losses there remains much recombination in the solar cells.

6.2. Outlook for future improvements

During the fabrication process and after measuring the external parameters of the local carrier-selective contacts it has become apparent that there is a lot of potential for improvement, this section will highlight some of the recommendations for improving the fabrication and the performance.

Wafer fragility

The aspect which hindered most of the fabrication process has been the fragility of the commercial wafers. Given their 180 μm thickness they are slightly thinner than most silicon wafers used in the lab, which are primarily around 280 μm. Because of the thickness of the commercial Cz wafers and them having a rough laser cut edge, being extra careful is paramount during the poly-SiO_x finger solar cell fabrication. Slight mishandling of the wafer, whether it be putting too much force on the tweezer when holding the wafer, drying the wafer when using the nitrogen gun for removing excess water from the wafer, clamping the wafer in a holder during a deposition process or even taking the wafer out of a wafer case can result in a fracture. This problem has been the most setback since it can occur at any step in the process. Smoothing the edge of the wafer by means of a dicing process to remove the outer edge of the cut wafer could potentially increase the endurance of the wafers.

At a certain point in the process the decision was made to shift from using square wafers to circular wafers. Initially during the optimization process all the test samples and the initial poly-SiO_x finger solar cells were fabricated on square substrates. The circular wafers were cut using the laser cutter out of the square wafers. When shifting to the circular wafers the breakage of wafers increased. An explanation for the increased fragility could be the influence of the laser, the power of the laser can affect the strength of the silicon [83]. The circular wafers are fully cut by the laser cutter, while the square wafers only have the laser cut on two sides. In total the square wafers have a shorter exposure to the laser cutter and this could explain their higher survival rate.

Poly-SiO_x finger formation

The hard mask can be used multiple times if it doesn't break during the PECVD process or when it is cleaned between depositions. Over time more material will accumulate on the mask and gradually reduce the openings of the hard mask. Investigations into the potential lifetime for the hard mask con be conducted by performing many PECVD deposition on the same mask. Deposited poly-SiO_x fingers that become too narrow from built-up material reducing the hard mask openings may not form a good contact with the metallization.

The etch-back method was briefly eluded to in chapter 3, this alternative method for finger formation would not utilize the hard mask but lithography instead. Full area doped poly-SiO_x is deposited and subsequently etched away partly to form the finger. This method could potentially resolve the issue of doped a-SiO_x:H being deposited between the gap of the hard mask and the substrate, since the dimensions of the finger would be exactly that of the lithography mask. The poly-SiO_x finger following a wet-etching step would be more rectangular shaped as opposed to a finger, given that the quality of the photoresist protective layer survives the wet etching process.

Alignment of poly-SiO_x finger

An alternative to the localized polishing would be to use the flat rear side for the marker reference, since the rear side of the commercial wafers have a flat surface. To perform a proper alignment with the rear side the markers on the lithography mask have to be perfectly mirrored. Attempts to align a lithography mask to the poly-SiO_x fingers have been made during this project, however the accuracy was never sufficient due to the pattern-shift observed on the rear side.

Recombination near the doped poly-SiO_x finger

The high concentration of dopants caused significant recombination due to the dopants in the poly-SiO_x finger and the p^+ diffused emitter on which it is deposited. A localized etching step can be performed

prior to the doped a-SiO_x:H PECVD deposition to remove the p^+ diffused emitter, then the poly-SiO_x can be deposited at these locations. The intention of this etching step is to mitigate the Auger recombination by having the dopants from the doped a-SiO_x:H diffuse into the c-Si bulk, rather than into the p^+ diffused emitter. This might potentially increase the carrier lifetimes due to lower Auger recombination present in the local carrier-selective contacts.

TLM

During the optimization process TLM samples were fabricated from the 32 symmetrical samples, silver and aluminium contacts where deposited in linear configurations with the distances between the metal contacts spanning from 650 to 3350 μm. Prior to the metallization the SiN_x layers were removed to create the interface between the metal contact and semiconductor doped areas. Fourteen measurements were taken for each sample with seven measurements for both types of metal. Regrettably the measurements were inconsistent for the majority of the samples, thus they have been ignored during the optimization of the process. The measurements were flawed due to not having cut the samples into thin pieces to prevent the carriers traveling away from the contacts. Future investigations into the contact resistivity of samples will have to include the cutting of the samples.

Metallization

A combination of metals for the front side contacts that has not been investigated include copper and titanium, both of which are available in the lab. By applying a thin titanium seed layer on top of the aluminium contacts and then applying copper contacts via plating can potentially be beneficial given the higher conductivity and lower cost of copper. The facilities available in the lab that provide the copper plating only allow for circular 4-inch wafer to be processed, this in turn interferes with the problem of the commercial wafer's fragility. Either the local carrier-selective contacts are made on initially laser-cut 4-inch circular wafers, or an laser-cut square wafers and prior to the copper plating the wafer is cut to a circular 4-inch wafer size.

New mask have since been designed which could potentially resolve the issues described in this section, the masks are shown in figure 6.1. The blue-colored isolation mask can be utilized to properly isolate active area for the solar cells, as opposed to the makeshift isolation mask. The red metallization mask is designed for the front side metallization of the fingers, to deposit metal fingers only on the poly-SiO_x fingers. The purple mask is subsequently used to deposit another layer of metal on top of the metal fingers to form the busbars.

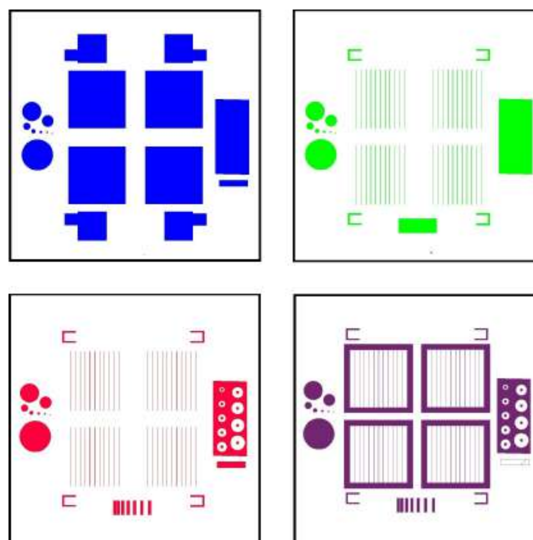

Figure 6.1: New lithography mask usable for the local carrier-selective solar cell fabrication. The masks include an active-area isolation mask (blue), poly-SiO_x finger mask (green), metal finger metallization mask (red) front contact finger and busbars mask (purple).

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In addition, many thanks are also given to everyone in the EKL, ESP and Kavli laboratories for their kind help. The expertise of the staff and other users has helped me gain confidence in my ability to build photovoltaic devices.

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