Design of a Bias Power Supply for GaN Switch Based Multilevel Traction Inverter

by

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TU Delft Delft University of Technology

I have never let my schooling
interfere with my education

Mark Twain

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Abstract

There has been significant research into the use of multilevel inverter topologies using Wide Band Gap (WBG) semiconductors in Electric Vehicle (EV) powertrains. This combination promises an increased power density and efficiency which should boost the viability and adoption of EVs. However, a reliable power supply is required for the inverter switches, which counters some of the challenges presented by these topologies. These challenges include the issue of high side power supply and Electromagnetic Interference (EMI) mitigation.

To begin with, certain requirements for a high side power supply are drawn up and various architectures are compared based on their merits and demerits. Based on this comparison, the LLC resonant converter is chosen as the most suitable topology due to its high efficiency, power density and potential for EMI mitigation.

The operating principles of this topology are examined and used to optimally design a one output LLC converter. These principles are then further extrapolated to the design of a LLC converter with six isolated outputs which are required for a multilevel converter. Both these designs are then prototyped and tested to verify their performance. It is found that the multi output converter performs at par or better than the commercially available solutions, while fulfilling the design requirements.

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I would like to thank my parents from the bottom of my heart for guiding me to this opportunity and trusting me to do them proud. I will always be there for you as you have for me.

Finally, I would like to thank my friends who have made this journey worthwhile. Anay, Aman, Suraj, and Utkarsh, you have been the constants and I genuinely look up to you. The poker nights with the EPE gang (and Souri) will weigh heavy in my pocket but always light in my heart. And to my Ravers van Delft, I will cherish our bond for the rest of my life.

Lick the stamp and we send it!

Naman Agarwal
Delft, July 2023

List of Abbreviations

GaN Gallium Nitride

FCML Flying Capacitor Multi Level

EV Electric Vehicle

SEV Solar Electric Vehicle

THD Total Harmonic Distortion

MLC Multi Level Converter

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

IGBT Insulated Gate Bipolar Transistor

FET Field Effect Transistor

SiC Silicon Carbide

CM Common Mode

EMC Electromagnetic Compatibility

EMI Electromagnetic Interference

WBG Wide Band Gap

PWM Pulse Width Modulation

FHA First Harmonic Approximation

ZVS Zero Voltage Switching

FEA Finite Element Analysis

PCB Printed Circuit Board

IC Integrated Circuit

BoM Bill of Materials

RMS Root Mean Square

1

Introduction

The transport sector is responsible for 25% of the global emissions. About 80% of these emissions can be attributed to passenger cars and other road vehicles [1]. Thus, it is of utmost importance to make this sector sustainable as quickly as possible. A great way to do this is the electrification of vehicles. This would allow the vehicles to be powered by electricity generated via renewable energy sources, thereby eliminating the carbon emissions from burning fossil fuels. Moreover, with Vehicle to Grid technology, these vehicles can also act as a battery pack to store energy when excess renewable energy is generated. The stored energy can then be used when the cost of electricity is higher or during the night when the availability of renewable energy sources is relatively lower. Thus, these vehicles can also prove to balance the diurnal nature of solar energy.

To facilitate speedy adoption of Electric Vehicles (EVs), it is crucial that their costs be reduced and convenience increased to justify the transition from the customers' perspective. One of the biggest barriers to the adoption of EVs is range anxiety among customers. This issue can be addressed by improving charging infrastructure or by increasing the range of the EVs itself. This can be done by improving the backbone of EV technology, which is the power electronics components and converters which drive the whole car.

In a conventional EV, a two-level inverter (Figure 1.1) is used as the interface to power the motors from batteries. This inverter converts the direct current of the battery into the three-phase alternating current required to power the motors.

Typically, these two-level inverters generally employ Si Insulated Gate Bipolar Transistors (IGBTs) as the choice of switch in the converter. However, as we approach the performance limits of these technologies, alternative topologies and devices are being explored to further improve the performance, range, and adoption of EVs [2]. These are discussed in the following sections.

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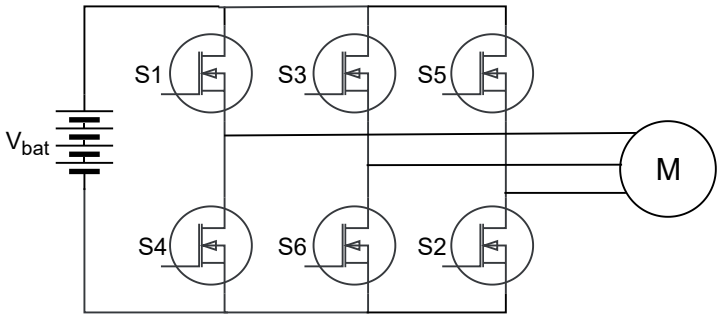


Figure 1.1: Two level inverter in EV powertrain

1.1. Multilevel Inverter

Multilevel inverters present several advantages over the typical two-level inverters. Some of these include decreased Total Harmonic Distortion (THD) in the motor current which improves the performance and efficiency of the traction motors. With the market trending towards 800V battery packs, it also enables the use of cheaper lower voltage rated switches which have lower switching and conduction losses compared to the singular high rating switch used in two-level inverters [3], [4]. In the specific niche of solar electric vehicles such as the Lightyear, which look to optimise the efficiency of each aspect of the car to enable long ranges on solar power, the multilevel inverters present a great potential benefit due to the aforementioned advantages.

Several topologies of multi-level inverters can be found in literature. One such converter under consideration is the Flying Capacitor Multi Level (FCML) inverter as seen in Figure 1.2. This topology allows for the use of lower voltage rated switches which are cheaper and more efficient. Compared to other multilevel topologies it also requires fewer switches and gate drive stages.

However, the use of FCML inverters also presents certain challenges. These include the use of complicated modulation strategies, capacitor charge balancing, and high side gate driving of the switching device. This thesis specifically looks at the gate driving challenge, which is exacerbated in a Multi Level Converter (MLC) compared to a conventional two-level converter due to the higher number of switching stages.

Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) (n-type) are fairly simple in their operation. They require a gate-source voltage higher than their threshold voltage to turn on by forming a conducting channel from the drain to the source. However, as the power rating of the switches increase, typically there is also an increase in the gate-source capacitance. Effectively turning them on and off at a high speed, while ensuring minimal switching losses requires a significant amount of gate current. To ensure efficient turn on/off of the MOSFETs, gate driver circuits are employed [5]. However, powering these gate drivers is a major challenge as the series connected switches have a floating source terminal.

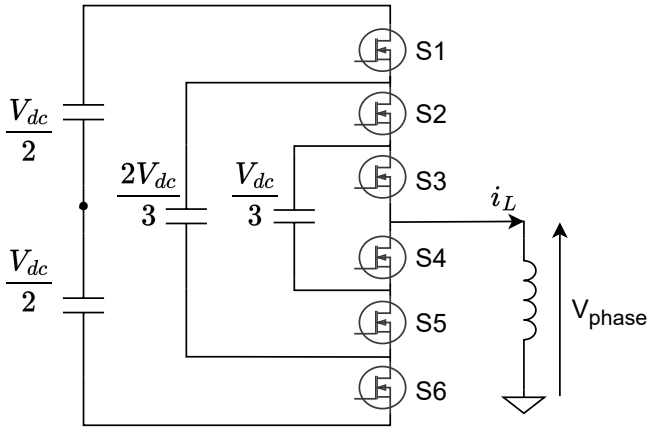


Figure 1.2: One leg of a four level FCML inverter

This is highlighted for a two-level converter in Figure 1.3 .

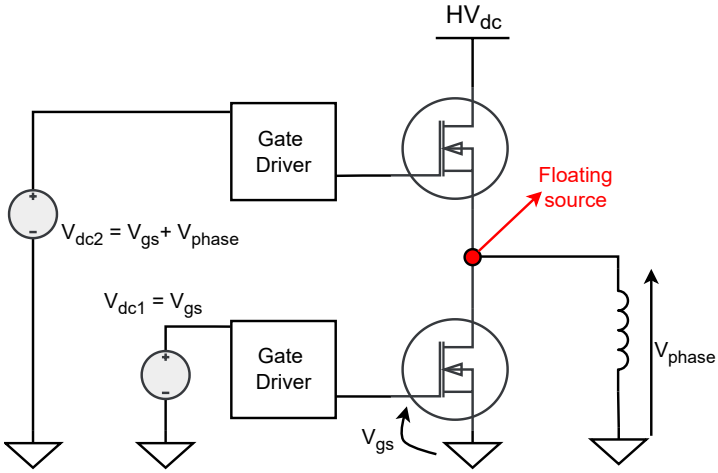


Figure 1.3: Floating source at the switching node of an inverter leg

Hence, a typical ground referenced power supply can not be used to provide the required voltage to all the switches as the required voltage for each DC source will keep increasing with the number of levels.

Further, the gate drive and power supply circuitry for these switches can quickly become a major barrier to the power density of MLCs as the number of levels increases. For instance, in a four-level FCML inverter, the total number of switches

1

across three phases is eighteen, compared to the six switches in a conventional two-level inverter. Hence, it is desirable to have a compact power supply and gate drive stages to achieve high power density. Several methodologies to implement this power supply solution exist in literature. These have been examined in Chapter 2.

1.2. GaN Transistors

Gallium Nitride (GaN) and Silicon Carbide (SiC) devices are ushering in a new era of power electronics. These Wide Band Gap (WBG) devices offer several benefits over conventional silicon based devices including lower switching and conduction losses. Further, GaN switches have no body diode which eliminates the reverse recovery losses. This enables them to switch at higher frequencies, thereby reducing the volume and cost of filtering elements of a converter and improving the power density [6]. In the context of electric drives, this also translates to improved motor efficiency due to reduced current ripple and improved sinusoidal current supplied to the motor [7], [8].

However, use of these high switching frequency devices with fast on/off transients introduces EMI into the system due to the high magnitude of dv/dt (upto 100V/ns) at the switching node which can be modelled as a pulsed voltage source as seen in Figure 1.4.

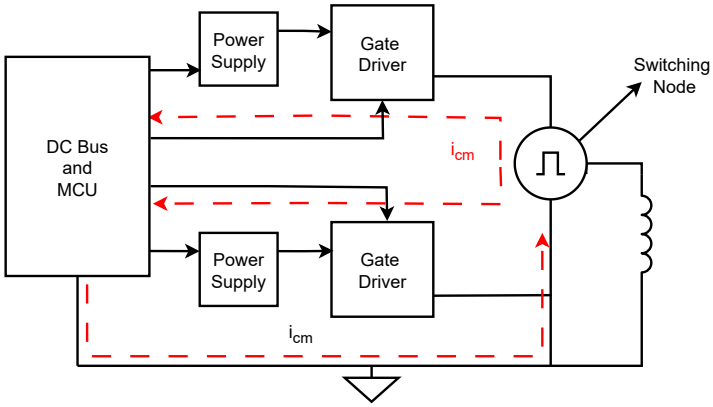


Figure 1.4: Generation of common mode currents due to fast switching transitions

This noise can couple into the system through the parasitic capacitances in the form of Common Mode (CM) currents, causing extra losses, malfunction of the control logic, and other low voltage systems.

$$i_{CM} = C_{par} * \frac{dv}{dt} \tag{1.1}$$

Further, a large loop of the CM currents also causes radiated emissions in the system. The mitigation of these undesirable emissions is necessary to comply with the various Electromagnetic Compatibility (EMC) standards imposed upon commercial automotives. One way to reduce these CM currents is by using active or passive EMI filters in the system [9]. This, however, adds to the cost, complexity, and weight of the system which are all undesirable.

Another approach is to suppress the EMI at source and hinder its propagation by reducing the parasitic capacitances in the system. As seen in (1.1), the CM current is linearly dependent on the parasitic capacitance. For instance, for a switching transition of $dv/dt = 50$V/ns, a reduction of C_{par} from 20pF to 5pF reduces the CM current from 1A to 0.25A. Hence, this thesis also investigates the best power supply architectures to minimise the EMI in a GaN switched multilevel inverter.

1.3. Research Question

The use of GaN devices in a multilevel topology may prove to be a potent combination in pushing the efficiency and power density of electric powertrains to the next level. However, to make such a system viable, a reliable high side power supply must be designed which addresses the various issues highlighted in Sections 1.1 and 1.2. Based on these requirements, this thesis aims to answer the following questions:

- What architectures are capable of providing a **continuous power supply** to the high side gate drivers to support a variety of modulation schemes for the inverter?
- Which power supply architecture is the most compact to achieve a **high power density** in MLCs?
- Which topology can **mitigate the EMI** in a fast switching GaN inverter?
- Which topology would be the most **efficient** for the required specifications?

The objective of this thesis is to identify, design and prototype the best topology of a high side power supply for a FCML inverter which meets the aforementioned requirements.

1.4. Structure of Thesis

The thesis answers each of these research questions in the following chapters:

- **Chapter 1** introduces the research topic and provides some context into the issues which need to be addressed in GaN switched FCML inverters.
- **Chapter 2** explores the various high side power supply architectures found in literature to examine them in context of the requirements and determine the best candidate.

- **Chapter 3** describes the working principles of the LLC converter which justify its selection for this application. The design of the power electronics stages are further discussed in this chapter.
- **Chapter 4** discusses the design procedure from analytical modelling to Printed Circuit Board (PCB) design for the planar isolation transformer of a single and multi output LLC converter.
- **Chapter 5** deals with the testing and performance of the designed prototype.
- **Chapter 6** summarizes the thesis and suggests some points for future research into this topic.

2

High Side Power Supplies

The gate driver is a critical part of any power electronics circuit. It provides the necessary gate to source voltage to the power switches to turn them on and off based on the low voltage control signals received from the controller. It serves several functions such as:

- Source and sink sufficient gate current to efficiently turn the MOSFET on or off through the four stages of switching [10]. This is crucial to ensure fast switching and minimise switching losses.
- Prevent false triggering of the switches due to fast dv/dt spikes [11]. Negative gate voltages may be applied to prevent accidental turn on of the switch.
- They may provide additional functionality such as over-current protection, undervoltage lockout, and galvanic isolation.

However, these gate drivers need a bias voltage supply to function which is typically in the range of 4 to 20V depending on the type of power device to be switched. Supplying this voltage to the gate drivers becomes increasingly challenging in the case of series connected switches as they have floating grounds as discussed in Section 1.1. This is exacerbated in multi level topologies where several switches are connected in series and all of them must be controlled independently of each other to fit the desired modulation scheme. Several methodologies to power the high side gate drivers have been proposed in literature. This chapter analyses their feasibility in context of a FCML inverter.

2.1. Pulse Transformer

One of the most common solutions is the pulse transformer for high side driving. The transformer simultaneously provides gate drive to the MOSFETs and galvanic isolation between the control and power stages [12]. This fairly simple and economical solution with few components is illustrated in 2.1.

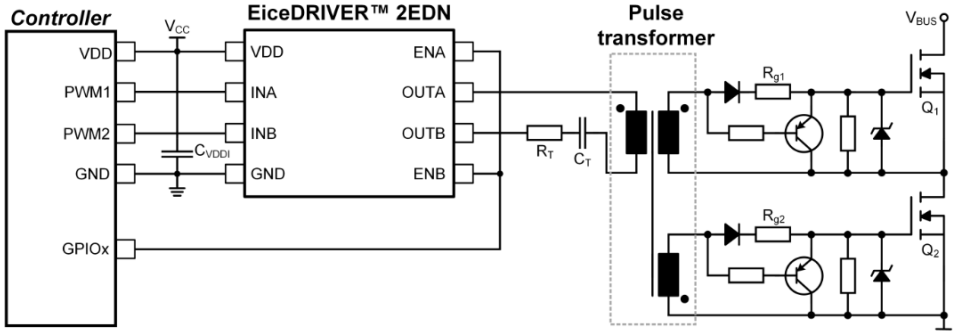


Figure 2.1: Pulse Transformer [12, p. 6]

However, the parasitics of the transformer present significant drawbacks. The leakage inductance can cause a mismatch in the propagation delays of the switching signals which leads to cross conduction of the inverter switches. The high di/dt flowing through the leakage inductance might also cause significant ringing across the drain-source terminals which can damage the switch. To minimize the leakage inductance, the windings may be interleaved at the cost of increasing the interwinding capacitance of the transformer. However, in high frequency applications with fast dv/dt transitions at the inverter side, the high interwinding capacitance offers a path to the common mode currents leading to spurious turn-on of the switch and EMI issues. These are amplified when fast switching GaN devices are used, thereby rendering this solution infeasible. Furthermore, there are issues with core saturation, especially in cases where the duty cycle of the inverter is above 50% [12], which restricts the possible modulation schemes for the inverter.

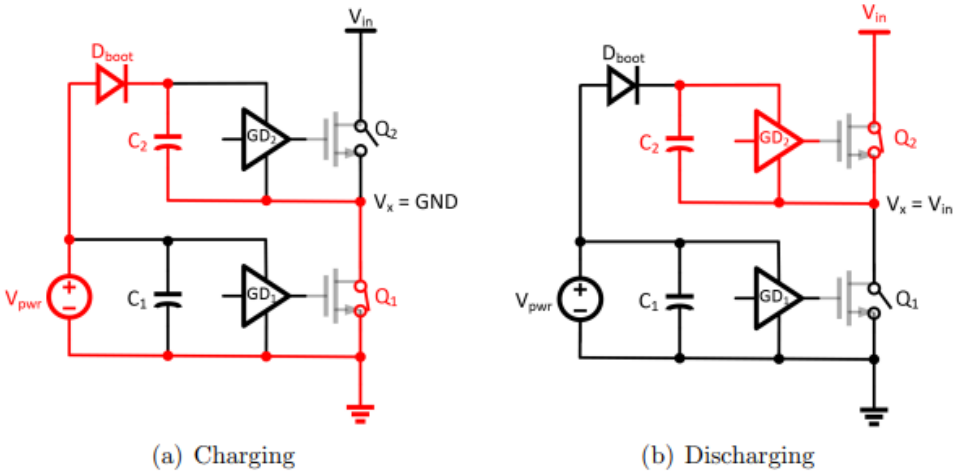
2.2. Cascaded Bootstrap

Another commonly used technique for two-level converters is the bootstrap method. Here the bootstrap capacitor is charged from the power supply when the low side switch is turned on. The charge on the capacitor is used to power the high side switch in the next cycle. This mechanism is highlighted in Figure 2.2.

This method is cheap and simple as it utilises a few additional components. However, the on time and duty cycle of the switch are limited by the charge on the bootstrap capacitor, which must be refreshed to a minimum level every cycle to ensure stable operation. This constraint renders it non-viable for use in inverters where a switch may have to be constantly on across multiple switching cycles in operation schemes such as overmodulation.

The cascaded bootstrap method as seen in Figure 2.3 builds upon this principle where several bootstrap stages are connected to one another.

It uses the forward drop of the power switch body diode to charge the capacitor above the input voltage. This requires sufficient inductor current and a dead time for charging to an appropriate level each cycle.



(a) Charging (b) Discharging

Figure 2.2: Bootstrap operation [5, p. 14]

However, this method carries the same flaws highlighted earlier, and may not work suitably during startup and light load conditions when there is not enough current to charge the bootstrap capacitor to a suitable voltage [5]. Further, fast switching converters with overmodulation constraints will suffer from failed turn on of the switches. Thereby, even this archetype of high side power supply is omitted from the potential solutions for a FCML inverter.

2.3. Charge Pump

The charge pump typically utilises a pulsed voltage to charge the high side capacitor and allows for a continuously on switch operation which is beneficial for inverters [13]. Building on this concept is the gate driven charge pump, unique to the flying capacitor family of multilevel converters [5]. It aims to utilise the flying capacitor connected between a low and high side switch to pump charge into the high side capacitor through the gate drive circuitry of the low side switch. The operation is illustrated in Figure 2.4. This a minimal solution that exploits the converter topology to simplify the power supply circuitry.

However, it suffers several demerits which make it unsuitable for use in a FCML inverter. Firstly, like the bootstrap method, it relies on the off time of the lower switch to charge the upper capacitor, which constrains the duty cycle and thereby the potential modulation schemes. Secondly, it requires the lower capacitor (C3) to be independently charged, either through a bootstrap or an isolated DC-DC stage. The use of the bootstrap method again brings the problems mentioned in Section 2.2. Finally, depending on the sizing of the respective capacitors, this method may cause an imbalance in the charge of the flying capacitors which would have to be compensated using a complication of the modulation strategies [14]. Hence, this

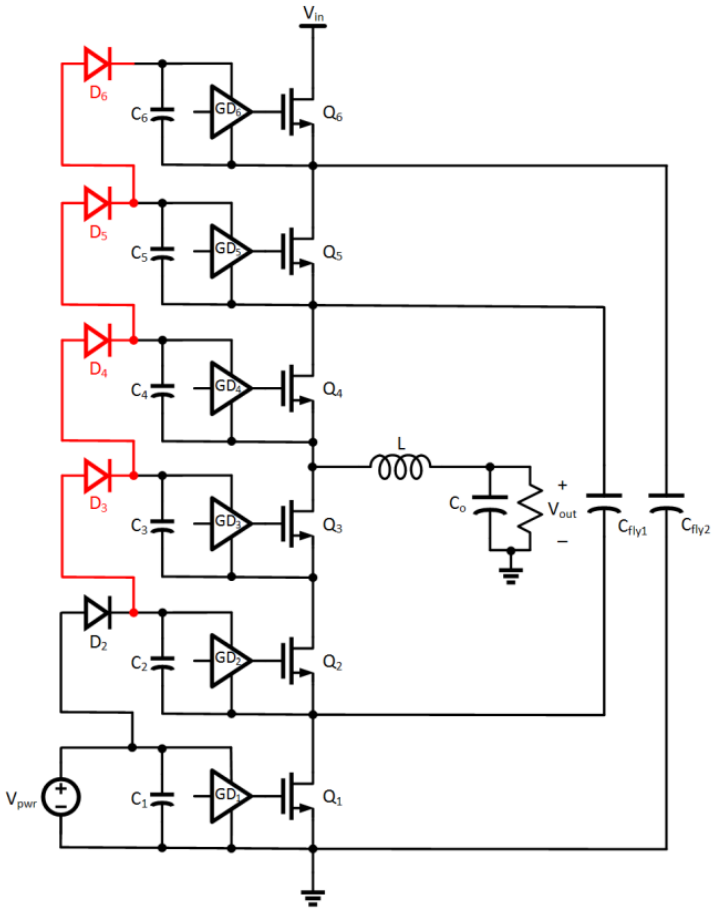


Figure 2.3: Cascaded bootstrap circuit [5, p. 17]

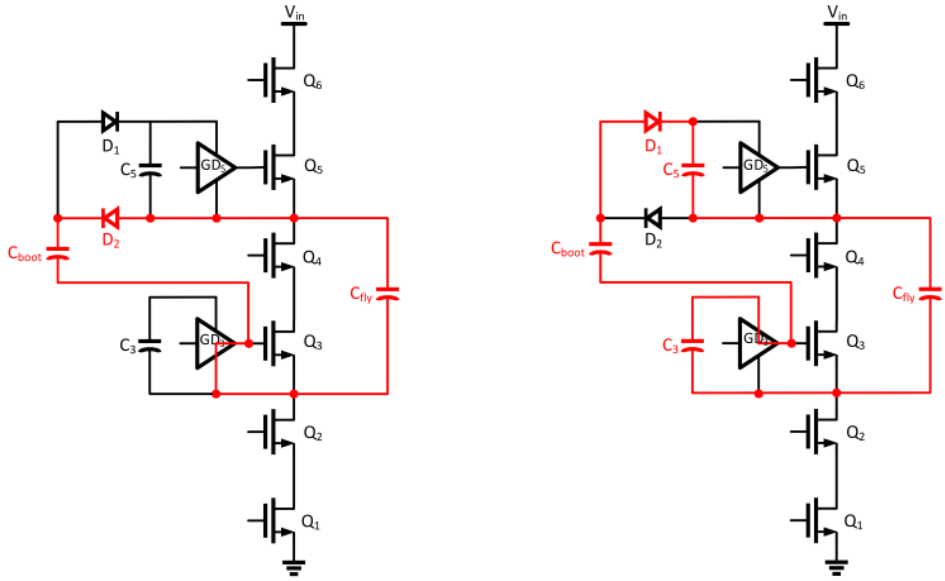


Figure 2.4: Gate driven charge pump operation [5, p. 45]

strategy is also omitted from consideration due to its pitfalls.

Another variation on this concept is the oscillator driven charge pump for FCML converters [15]. This solution is a combination of the aforementioned charge pump solutions. It utilises an oscillator on the low side to pump charge to the high side through the connected flying capacitor as seen in Figure 2.5. It is a relatively cheap and modular solution and overcomes some of the drawbacks of the gate driven charge pump, by allowing for full duty cycle operation of the switches as it does not rely on the low side switch to replenish the charge on the high side capacitor.

However, it also suffers from similar drawbacks as earlier, in that it assumes the low side stages are already powered from a DC source. In a four level FCML inverter, this means that only two of the six driving stages will benefit from this solution, and the other four will require either bootstrapping or isolated power stages. This may save some space and cost but increases design complications as multiple solutions need to be deployed in the system. However, this solution might make more sense for a multilevel configuration with a higher number of stages. Due to the presented drawbacks, this solution is not favourable for a FCML inverter.

2.4. Isolated Power Stages

Isolated power stages are the most commonly used power supply solutions for multilevel converters. They present a reliable and modular solution that has been employed in various multilevel converter implementations in literature [16], [17].

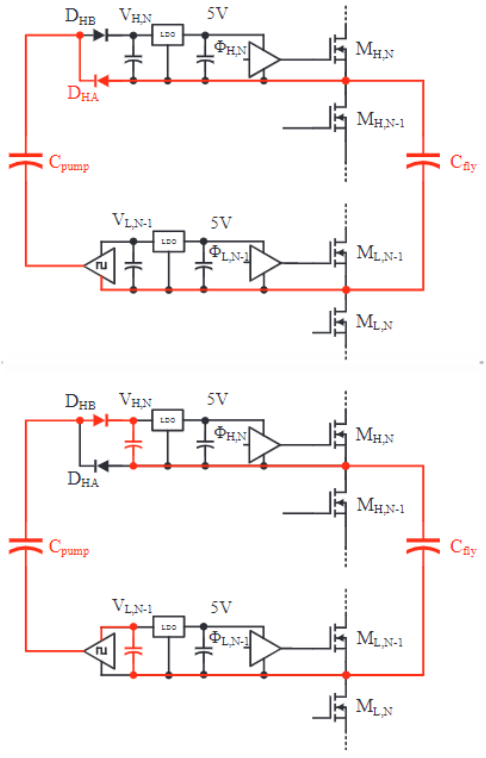


Figure 2.5: Oscillator charge pumping mechanism for FCML converters [15, p. 3]

A typical isolated power supply is shown in Figure 2.6. The input of the DC/DC converter is connected to a regulated DC bus, which can be derived from the high voltage battery using an isolated step down converter, or by connecting to a low voltage battery of 12V or 24V. The transformer or coupled inductor isolates the low voltage DC bus from the power stage. The secondary windings of the transformer then provide floating output voltages that are not referenced to the system ground, thereby overcoming the issue of floating grounds as discussed in Section 1.1.

This architecture allows for a continuous power supply to the switches. Hence, there is no constraint on the possible modulation schemes on the inverter side. Further, a tightly regulated output voltage can be obtained which is critical for GaN devices as they can get damaged if the gate voltage exceeds maximum rating [18]. This solution is also modular and can be easily scaled to the required number of stages. However, deploying isolated power stages for each switch can make the overall system somewhat bulky and expensive compared to the other solutions.

Based on the preceding analysis which is summarised in Table 2.1, it is found that isolated DC/DC converters present the most feasible solution. The charge pump seems like a feasible candidate as well, but it requires isolated power sup-

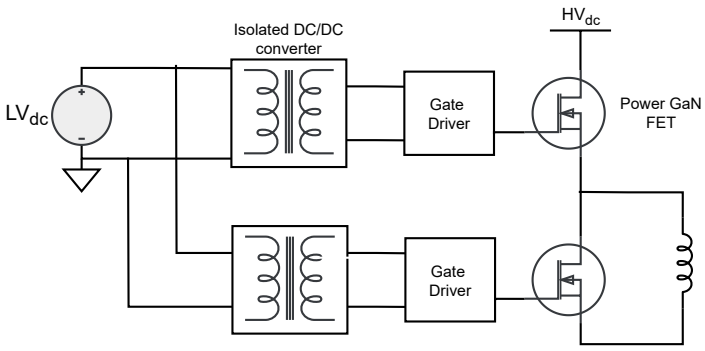


Figure 2.6: Isolated power supply solution

plies for more than half of the switching stages as described in Section 2.3. Hence, utilising only isolated power stages simplifies the design as it is a modular solution that can be easily scaled to the required number of levels.

Revisiting the system level requirements in Section 1.2, they can be mapped to the characteristics of an isolated DC/DC converter as follows:

- The EMI and CM noise currents can be mitigated by reducing the inter-winding capacitance ($C_{pri-sec}$) of the isolation transformer as seen in Figure 2.7. However, this inherently increases the leakage inductance ($L_{lk,pri}$ and $L_{lk,sec}$) of the transformer due to loose coupling of the windings [19],[20].
- Must be compact as there are multiple switching stages and the volume of the power supply can reduce the overall power density of the system. Hence multiple isolated outputs from the same converter would be preferred.
- Must be able to provide a continuous, constant voltage to the gate driver to allow for flexibility in inverter modulation schemes.
- Open loop operability would make the system cheaper and more compact. It would also reduce the parasitic effects of the feedback loop elements such as the optocoupler [19].

The possible DC/DC topologies are further examined in the context of these requirements.

2.4.1. Switch Mode Power Supplies

Switch mode power supplies are the status quo for bias power supplies in the industry due to their simple design and low component count while providing isolation. This archetype of converters includes the flyback (or flybuck), push-pull and forward converter topologies [21], [22], [23]. Further, it is possible to have multiple

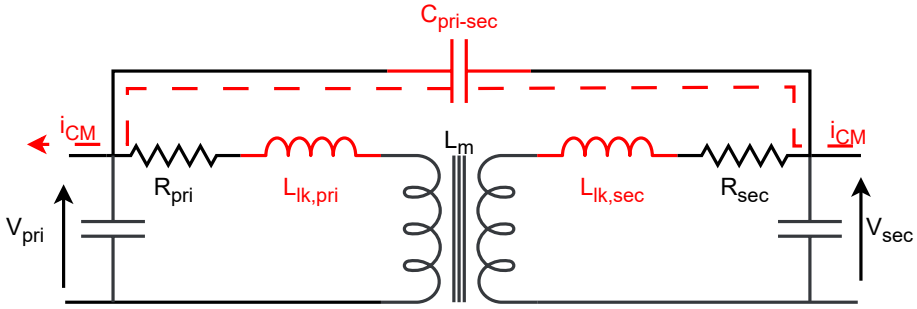


Figure 2.7: Interwinding capacitance in a transformer

isolated outputs which allows for a compact system design.
However, one of the main drawbacks of this archetype is the presence of leakage inductance inherent to any transformer (or coupled inductor). The presence of this parasitic causes voltage ringing at the drain of the switching device which increases losses and device stress and also introduces EMI into the system [24],[25]. These issues are further exacerbated if a transformer with lower inter-winding capacitance is desired, which increases the leakage inductance. Hence, this archetype of power supplies may not be the most suitable option for the given FCML inverter with GaN switches.

2.4.2. Resonant Converters

Resonant converters are another broad archetype of DC/DC converters. They can be generalized into cascaded blocks consisting of an inverter bridge, a resonant tank, and an output rectifier as highlighted in Figure 2.8. Typically, the output voltage of a resonant converter is regulated by varying the switching frequency of the inverter bridge at a fixed duty cycle of 50%. Resonant converters are known to have high efficiency and low EMI due to soft switching while providing multiple isolated outputs [26], [27], [28].

The input DC source is connected to the inverter bridge which is usually in a half or a full bridge configuration. This inverter produces the square voltage pulses of the desired frequency to regulate the output voltage. The resonant tank consists of an inductor and capacitor network. This network also includes the various parasitic components of the transformer [29].

Resonant converters can be classified into series resonant, parallel resonant, and series-parallel resonant converters based on the configuration of the resonant tank. The series and parallel resonant circuits present several difficulties with load regulation and high circulating currents [30]. Hence, to overcome these drawbacks, the series-parallel (or third order) resonant converters are preferred for most applications.

As discussed in [29], there are thirty-six possible third order resonant tank con-

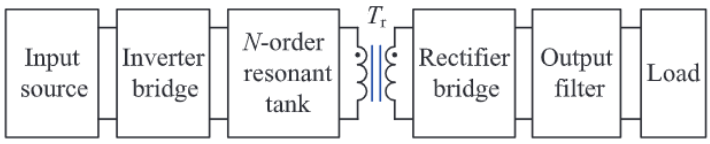


Figure 2.8: General block diagram of an resonant converter [29, p. 2].

verters. Out of all the possibilities, the LLC configuration (as seen in Figure 2.9) allows for fully benefiting from integrating the leakage inductance and magnetizing inductance of the transformer as resonant elements in the resonant tank of the converter. This makes for a compact design while mitigating the undesirable effects of having a high leakage inductance as with switch mode power supplies. Hence, the transformer can be designed with a low parasitic capacitance to reduce the CM currents, without compromising the performance of the system.

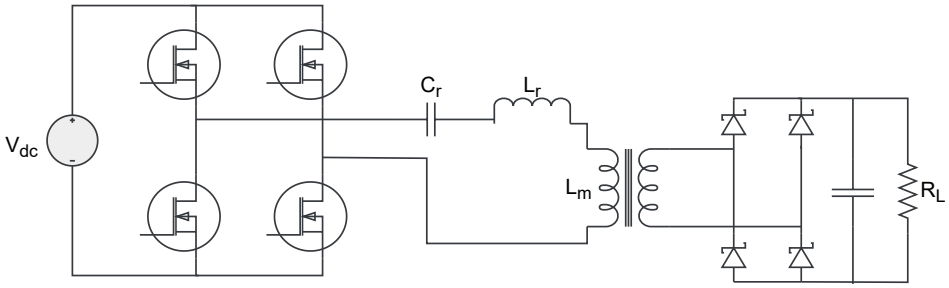


Figure 2.9: LLC resonant converter

A comparable topology to the LLC is the active bridge. However, this has issues with increased core losses and saturation due to the absence of a DC blocking capacitor in the circuit [31].

Due to the high theoretical efficiency, the possibility of a high leakage yet compact design, and the ability to have multiple outputs, the LLC resonant converter is chosen as the desired topology for isolated DC/DC power supply. The detailed functioning of the LLC converter is further discussed in Chapter 3.

2.5. Literature Overview

The comparison of the various high side power supply architectures as seen in literature are summarized in Table 2.1.

Based on this comparison, it is decided that the isolated power supplies provide the most feasible solution as there is no restriction on the inverter side duty cycle and they provide a higher efficiency.

Isolated power supplies for modular multilevel converters have been reported in [21], [33]. The former utilizes the flyback topology which brings the issues

Table 2.1: Comparison of various high side power supply methods

	Duty Cycle	Efficiency	Volume	Cost
Pulse Transformer [12]	<50%	50%	High	Medium
(Cascaded) Bootstrap [5]	<100%	88%	Low	Low
Gate Driven Charge Pump [5]	<100%	90%	Low	Low
Oscillator Charge Pump [15]	100%	50%	Low	Medium
Isolated Power Supply [32]	100%	80%	Medium	High

highlighted in Section 2.4.1. The latter design utilizes the LLC topology focused on high voltage isolation. Both these solutions are focused on power supply for IGBT based systems and do not consider the EMI mitigation required in a GaN switched converter.

A dual output power supply for GaN half bridges using an active clamp flyback circuit is proposed in [34]. However, it requires a PCB embedded transformer core which can be difficult to manufacture. It also utilizes GaN switches and requires active control for soft switching which makes the solution expensive.

Another solution for SiC systems proposed in [35] utilizes modified forward converters to obtain soft switching. It aims to utilize the parasitic inductor and capacitor of the converter to determine the switching frequency, which makes the optimal magnetics design rather complicated.

Apart from these, there are several bias power supplies available in the market in the power range of 1W to 3W. These typically have one to three outputs and offer around 80% efficiency. Further, an isolation capacitance of 20 to 80pF appears to be the industry standard. The parameters of these solutions have been summarized in Table 2.2.

Table 2.2: Comparison of some existing bias power supplies

Outputs	Solution	Power (W)	$C_{pri-sec}$ (pF)	Efficiency (%)
2	Sun Et al. [34]	2	1.6	85
4	Serban Et al. [35]	4	14	85
1	IEB01 [32]	1	20	80
2	PDME2-S[36]	2	20	80

The commercially available solutions use the flyback topology which itself can increase the EMI of the system. Furthermore, none of these solutions offer six isolated outputs in a single package which is required for a four level FCML converter. Hence, this thesis aims to design a six output LLC converter with high efficiency and low parasitic capacitance to bridge this gap.

3

LLC Converter Working and Design

3.1. Working Principles

As described in Section 2.4.2, the LLC resonant converter is ideal for the presented application due to the integration of leakage inductance and high efficiency. The working principles and intricacies of the LLC converter will be discussed in this section.

3.1.1. Circuit Description

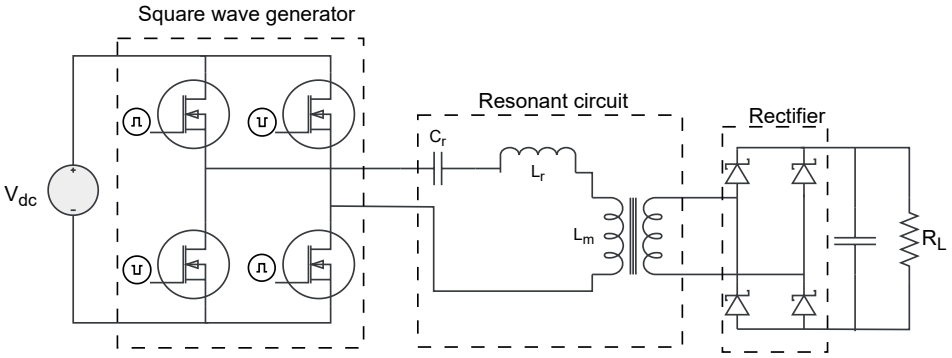


Figure 3.1: Full bridge LLC resonant converter

As seen in Figure 3.1, the square wave generator consists of two legs with series connected MOSFETs. The MOSFETs are driven by complementary Pulse Width Modulation (PWM) pulses at a duty cycle of 50%. This generates the square wave pulses at the desired frequency across the resonant circuit. A dead time is often

included to ensure both the switches in the bridge are not simultaneously turned on to prevent shoot-through. As detailed in Section 3.1.3, this dead time can also be used for ZVS of the switches which eliminates the switching losses of the device. The varying frequency of the applied pulses varies the effective impedance of the resonant tank which consists of a resonant capacitor (C_r), resonant inductor (L_r), and the magnetizing inductance (L_m). The intrinsic leakage inductance (L_{lk}) of the isolation transformer can be used as the resonant inductor, eliminating the need for an additional component. Finally, on the secondary side, a diode bridge rectifies the voltage which is smoothed by the output capacitor to provide a regulated output voltage to the load. The effective circuit can be seen in Figure 3.2. The impedance of the resonant tank varies with the frequency of applied square pulses and the output load as described in [30].

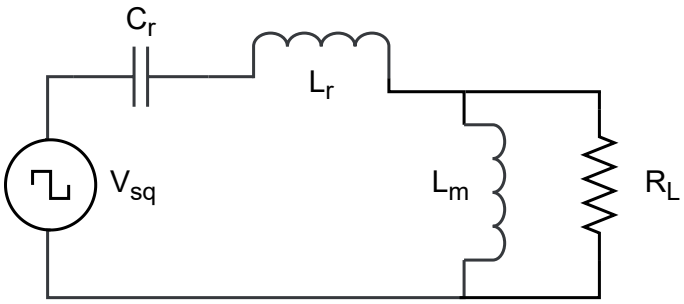


Figure 3.2: Effective circuit for LLC converter

3.1.2. First Harmonic Approximation

For analysis of the presented circuit, the First Harmonic Approximation (FHA) is often employed. For simplification, it assumed that the first harmonic (f_{sw}) of the square wave pulse is the dominant frequency and the effect of the other harmonics can be neglected [37],[38], [39].

The resonant frequency (f_0) and pole frequency (f_p) are defined as:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.1}$$

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{3.2}$$

The FHA simplifies the non-linear circuit into a linear and sinusoidal circuit while also providing accurate results, especially if the converter is operated in the vicinity of the resonant frequency f_0 [30].

Based on the FHA, the gain of the circuit due to the resonant tank may be calculated using (3.3).

$$Gain_{FHA} = \sqrt{\frac{1}{(\frac{1}{\omega_{sw}^2 L_m C_r})^2(\frac{\omega_{sw}^2}{\omega_p^2} - 1)^2 + (\frac{1}{\omega_{sw} C_r n^2 R_L})^2(1 - \frac{\omega_{sw}^2}{\omega_0^2})^2}} \tag{3.3}$$

Where $\omega_{sw} = 2\pi f_{sw}$, $\omega_0 = 2\pi f_0$, $\omega_p = 2\pi f_p$ and $n = \frac{N_{pri}}{N_{sec}}$.

For a full bridge configuration on the primary side, the input and output voltages are related by 3.4.

$$\frac{V_{out}}{V_{in}} = Gain_{FHA} * \frac{1}{n} \tag{3.4}$$

If the switching frequency is equal to the resonant frequency, the gain of the tank is unity. This means that the output and input voltage are related only by transformer turns ratio irrespective of the load.

3.1.3. Zero Voltage Switching

ZVS across a switch (in this case MOSFET) may be obtained by ensuring the voltage across the switch is zero before it is turned on. This ensures that it is softly switched and the switching losses are minimized. The ability of the LLC converters to have ZVS on the primary side is one of its greatest benefits as it allows for low losses even at high switching frequencies, thereby enabling an efficient and compact system [37]. To ZVS a MOSFET in practice, it is required that a current discharge the output MOSFET capacitance (C_{oss}) before it is turned on. In the LLC converter, this is done using the current flowing in the resonant tank as seen in Figure 3.3

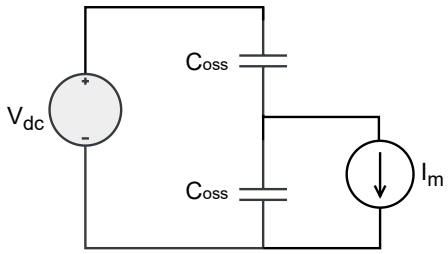


Figure 3.3: Effective circuit for ZVS operation

The converter may be operated below, at, or above the resonant frequency by varying the switching frequency (f_{sw}) of the primary side MOSFETs. To obtain soft switching of these switches, it is necessary that the current in the resonant tank lags the voltage. This implies that the impedance of the resonant tank, as seen by the voltage source is inductive in nature. This is possible when the converter is switched above the resonant frequency i.e. $f_n = \frac{f_{sw}}{f_0} > 1$, presenting the first condition required for effective ZVS. This region of operation is highlighted in Figure 3.4. Further, operating below the resonant frequency is undesirable as it increases the losses in the conductor due to higher circulating currents [30].

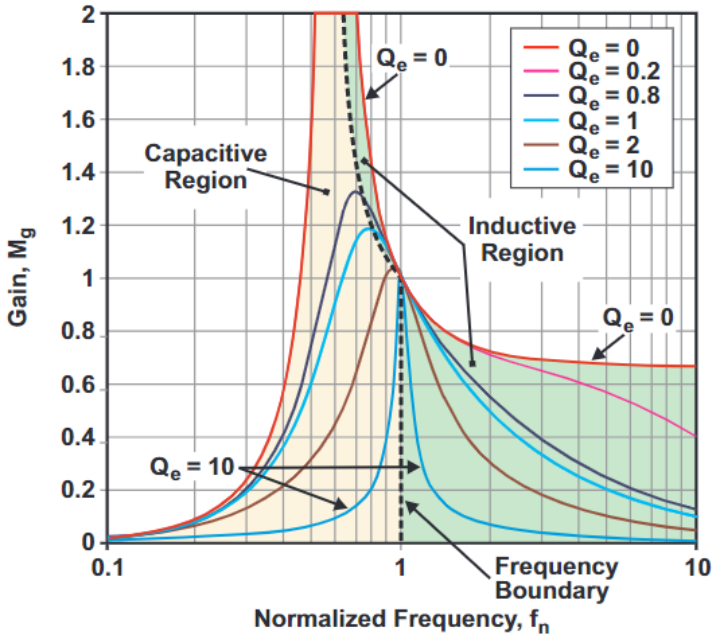


Figure 3.4: Resonant tank gain curves for various loading conditions [30, p. 14]

The second condition to ensure ZVS is based on the energy required to charge and discharge the capacitors. Since the resonant tank current is used for this purpose, the tank energy must be greater than the capacitive energy of the MOSFET. This may be represented by (3.5).

$$\frac{1}{2}(L_m + L_r)I_{peak}^2 \geq \frac{1}{2}(2C_{oss})V_{in}^2 \tag{3.5}$$

The final condition is that there must be sufficient time between switching transitions for this tank current to (dis)charge the capacitors. This is ensured by including a dead time between the complementary square pulses used to drive the MOSFETs. This can be quantified using (3.6).

$$t_{dead} \geq 32 * C_{oss} * f_{sw} * L_m \tag{3.6}$$

3.1.4. Open Loop Operation

As highlighted in Section 2.4, one of the desirable qualities of the isolated DC/DC is the ability to operate in open loop to reduce system complexity, cost, and parasitics. For the given application, where the input DC bus of the converter is well regulated and the required output voltage is constant and predefined, it is actually feasible to design a robust open loop system. The LLC converter especially proves itself rather beneficial in such an application. As described in Section 3.1.2, the gain of

the resonant tank approaches unity as the switching frequency (f_{sw}) approaches the resonant frequency (f_0) of the tank. This can also be observed in Figure 3.4.

Here Q is defined as:

$$Q = \frac{\sqrt{L_r/C_r}}{R_L} \tag{3.7}$$

and the increasing value of Q represents a higher load at the output. However, it can be seen that at the normalized frequency (f_n) of one, all the curves meet at the resonant tank gain of one. This implies at the resonant frequency the output voltage is independent of the load and the voltage gain is purely dictated by the turns ratio of the isolation transformer as described by (3.4).

Hence, it is possible to design an LLC converter that operates just above but in the vicinity of the resonant frequency. This would allow it to operate in open loop with a fixed gain for all loads while also being in the inductive region which is necessary for ZVS as discussed in Section 3.1.3.

Revisiting the research objectives highlighted in Section 1.3, it is seen that they align very well with the characteristics of the LLC converter:

- **EMI mitigation:** The operation of the LLC converter is not deteriorated by a high leakage inductance thereby making a low interwinding capacitance design viable as highlighted in Section 2.4.2.
- **Volume:** It is possible to operate the converter at a high frequency without incurring significant switching loss and also have the resonant tank integrated into the isolation transformer. Further, it is also possible to have multiple outputs in the same LLC converter. This allows for compact magnetics and improves the power density of the system.
- **Continuous supply:** The isolated resonant converter is capable of providing a regulated output voltage to keep the switch on continuously.
- **Efficiency:** As discussed in Section 3.1.3, it is possible to soft switch the semiconductors by operating in the inductive region which mitigates losses. Further, optimized design of the magnetics to be covered in Chapter 4 improves system efficiency.

3.2. Converter Design

The design of the input and output LLC converter stages will be discussed in this section. The detailed transformer design is discussed in Chapter 4.

3.2.1. Initial Specifications

The first step in designing the system is to define the specifications:

- The input voltage from the regulated DC bus is constant at 12V.

- The GaN switch used in the inverter is the *EPC2304* which has a maximum gate-source voltage (V_{gs}) of 6V [40]. This is the voltage that needs to be supplied to the output side of the gate driver.
- The *BAS3007A* barrier rectifier array from Infineon are chosen as diodes in the output side rectifier of the power supply. They are used as they have a low forward voltage drop of 0.5V, and include four diode in one package which reduces the Bill of Materials (BoM) and board space [41]. Hence, the output voltage of the converter can be set to $6 + 0.5 + 0.5 = 7V$.
- The gate driver for the GaN switch is chosen to be *UCC5304* from Texas Instruments [42]. This requires an average current of about 50mA to function at full load conditions.
- The total power of the converter for one output, after accounting for stray losses can be estimated to be about $7\text{V} * 0.05\text{A} + \text{losses} = 0.5\text{W}$.

The converter specifications are summarised in Table 3.1.

Table 3.1: Converter specifications

Vin	12V
Vout	7V
Power	0.5W

3.2.2. Input Side Full Bridge

The full bridge on the input side is required to convert the 12V DC voltage to square pulses to feed into the resonant tank. It can be constructed using four MOSFETs with their respective bootstrapped drivers. However, to reduce the bill of materials, complexity, and the size of the system, the MAX22258AUD IC from Analog Devices is chosen [43]. A typical application circuit of the IC is shown in Figure 3.5. The resonant tank is connected across the ST1 and ST2 pins of the IC. A square pulse at twice the desired converter switching frequency can be supplied to the CLKI pin to determine the switching period.

This IC has the four switches of the full bridge built into it, along with additional circuity which offers several benefits:

- A reduction in the BoM, board space and design complexity.
- The dead time can be set by using a resistor between the DTC pin and ground which allows for flexible prototyping. In the designed prototype, a potentiometer is used for this purpose to dynamically vary the dead time.
- The IC includes additional useful features such as adjustable current limit and fault detection which improve the safety and reliability of the system.

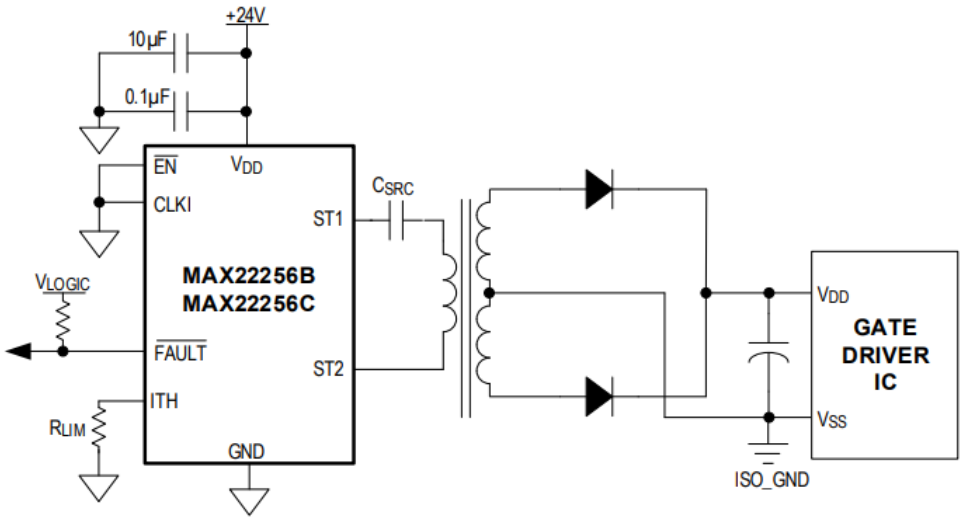


Figure 3.5: Typical application circuit using the MAX2258AUD IC [43, p. 1]

The final schematic using this IC can be seen in Figure 3.6. It must be noted that a 'capacitor bank' has been included instead of a single resonant capacitor. This adds an extra degree of freedom during prototyping to optimally tune the resonant tank. The final designed PCB is seen in Figure 3.8. Further, an op-amp based current sensing circuit has been added to measure the resonant tank currents.

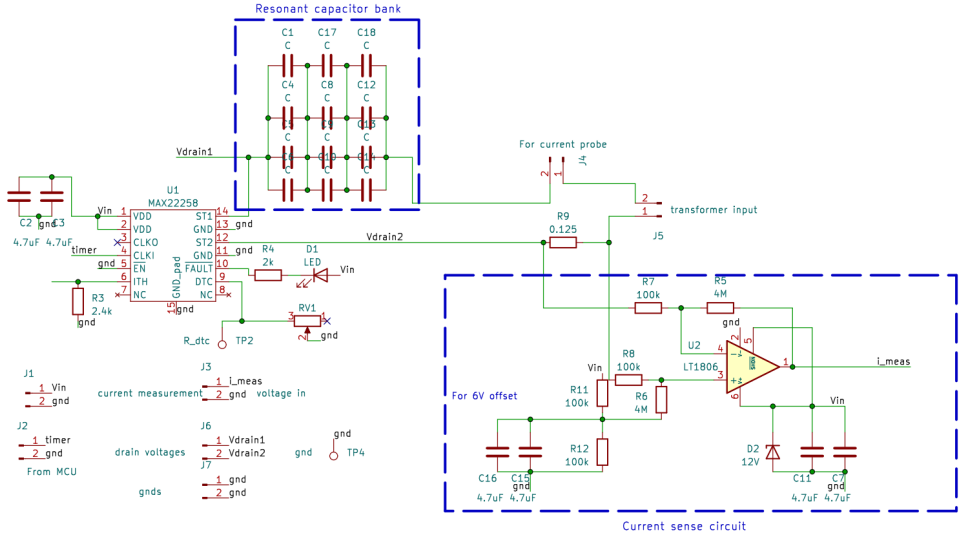


Figure 3.6: Input full bridge schematic

Both of these features are only required for the prototyping and testing phase and are not required for the proper functioning of this design.

Since the specs of the internal MOSFETs on MAX22258AUD are unknown, the RA1C030LD MOSFET from ROHM [44] is chosen to model the primary side full bridge in the analytical calculation and simulations in the following sections.

3.2.3. Output Stage

The output stage is responsible for rectifying the AC currents of the resonant tank into the DC current required at the output. The schematic for a single output stage can be seen in Figure 3.7. The same design is replicated for the remaining five outputs as well and can be seen on the PCB in Figure 3.8.

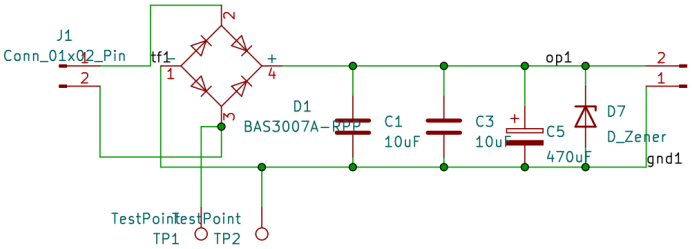


Figure 3.7: Output rectifier stage schematic

The BAS3007A Schottky diode array from Infineon is used to form the full bridge rectifier [41]. Two ceramic bypass capacitors and a bulk electrolytic capacitor are connected to give a smooth DC voltage. Further, a 6V Zener diode is included to limit the output voltage and protect the sensitive GaN devices in case of voltage spikes.

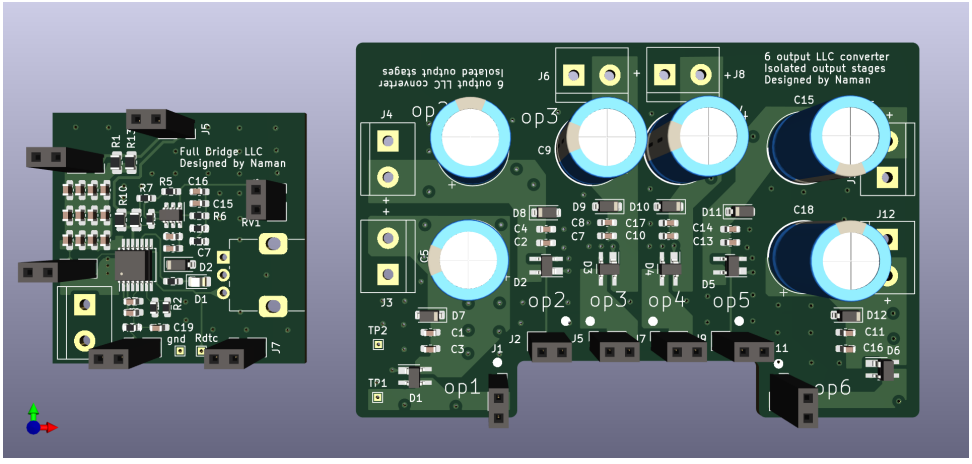


Figure 3.8: Renders of designed input and output stages of the converter

4

Transformer Design

Based on the theory discussed in Chapter 3, it is now possible to design a LLC converter for the stated requirements. To make a compact design, the leakage inductance (L_{lk}) of the isolation transformer will be utilized as the resonant inductor (L_r) of the LLC converter. Initially, a one input to one output transformer will be designed according to the circuit in Figure 4.1. This design can further be extrapolated to a LLC converter with multiple outputs.

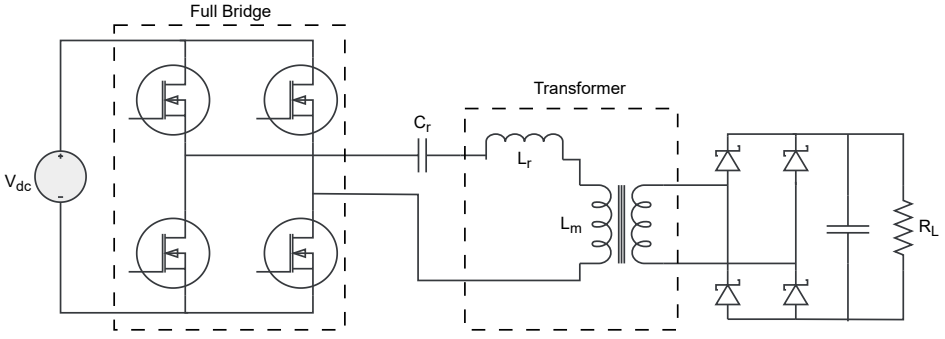


Figure 4.1: Full bridge LLC converter

4.1. Single Output Transformer Design

Once the specifications are determined, the next step is to design the isolation transformer for the given LLC converter. As described in Section 3.1.3, the converter is capable of soft switching, and designing an optimal transformer would further improve the efficiency of the system.

4.1.1. Core Selection

It is decided that a planar transformer would be ideal for this application as it improves the power density of the system, can be accurately modelled due to consistent winding positions and the design is repeatable [45]. The "core geometry" method as described in [46] is used to determine the required core. The value of the factor "K_g" is calculated to be 0.00004878 cm^{-5} at a frequency of 200kHz. A conservatively lower frequency is used for this calculation to ensure the core is big enough for the application. Based on this the E8.8 core from TDK is chosen [47]. Two halves of this core will be placed in the EE configuration to form the transformer core. Based on the available magnetic materials, the N87 ferrite is chosen as it performs optimally around $100°C$ and in the frequency range of up to 500kHz.

4.1.2. Transformer Optimization

Once the core and its material are chosen, the next step is to determine the optimal working parameters of the transformer and the converter. This section describes the objective of the optimization, the various parameters that influence it, and how they interact.

4.1.2.1. Optimization Objective

The goal of the design is to minimize the losses and the inter-winding capacitance of the transformer as discussed in Section 4. The inter-winding capacitance is highly influenced by geometry and placement of the windings hence it is not included in the optimization problem and will be discussed in Section 4.1.3. The losses, however, can be modelled fairly accurately. There are two main mechanisms of losses in the transformer: **Core loss** and **Copper loss**.

The core loss per unit volume is calculated using the Steinmetz equation [48]:

$$P_v = C_m * f_{sw}^x * B^y * (Ct_2 * T^2 - Ct_1 * T + Ct) \tag{4.1}$$

$$P_{core} = P_v * V_{core} \tag{4.2}$$

where the C_m, x, y are the Steinmetz coefficients of the material, T is the temperature in degrees Celsius, Ct_2, Ct_1 and Ct are the temperature modifiers and V_{core} is the core volume. f_{sw} and B are the switching frequency and maximum flux density respectively.

The copper loss is caused due to the I^2R losses in the conductors. However, at high frequencies of the AC current, there are eddy currents generated in the conductors which reduces their effective cross section area, thereby increasing the resistance and the losses [45]. These are often separated into skin and proximity effects. Skin effect causes the increased AC resistance of the wire by effectively causing the current to flow only in the outer peripheries of the conductor. The available cross section can be quantified by calculating the skin depth of the conductor which is given by (4.3).

$$\delta = \sqrt{\frac{\rho}{\pi f_{sw} \mu}} \tag{4.3}$$

Here ρ is the conductivity and μ is the permeability of the material.

Meanwhile, the proximity effect is caused due to the eddy currents induced by adjacent conductors. Both of these effects are modelled by calculating the effective AC resistance of the conductor. The ratio of AC to DC resistance for the m^{th} layer of a transformer winding using (4.4) and (4.5) [49], [50]:

$$R_{ac,m} = R_{dc,m} * \frac{\xi}{2}\left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2.\frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right] \tag{4.4}$$

$$m = \frac{F(h)}{F(h) - F(0)} \tag{4.5}$$

Here ξ is the ratio of conductor height and skin depth, m is given by (4.5) and F(h) and F(0) are the magnetomotive force (MMF) at the limits of a given layer as described in [45].

From (4.2) and (4.4), it is possible to evaluate the total transformer loss using (4.6)

$$P_{tf} = P_{core} + i_{pri,rms}^2 * R_{ac,pri} + i_{sec,rms}^2 * R_{ac,sec} \tag{4.6}$$

The objective of the optimization is to minimize the value of this function, henceforward referred to as the objective function.

4.1.2.2. Optimization Parameters

There are several parameters in the design space that determine the performance characteristics of the transformer and the converter. These include the switching frequency (f_{sw}), magnetizing inductance (L_m), dead time (t_{dead}) required for soft switching and the primary (N_{pri}) and secondary turns (N_{sec}). All of these variables are interdependent, bound by constraints and also influence the objective function. Further, these parameters also influence the primary current ($i_{pri,rms}$) flowing in the windings and hence the copper losses in the transformer. This interdependence can be visualized using Figure 4.2.

(3.5) and (3.6) which dictate ZVS, form the relation between L_m, f_{sw} and $i_{pri,rms}$. Further, using the first harmonic approximation, the primary RMS current is related to L_m and f_{sw} by (4.7)

$$i_{pri,rms} = \frac{4}{\pi} * \frac{V_{in}}{2} * \frac{1}{2\pi f_{sw} L_m} \tag{4.7}$$

Also, N_{pri} and L_m are related by (4.8)

$$L_m = \frac{N_{pri}^2 A_e \mu}{l_e} \tag{4.8}$$

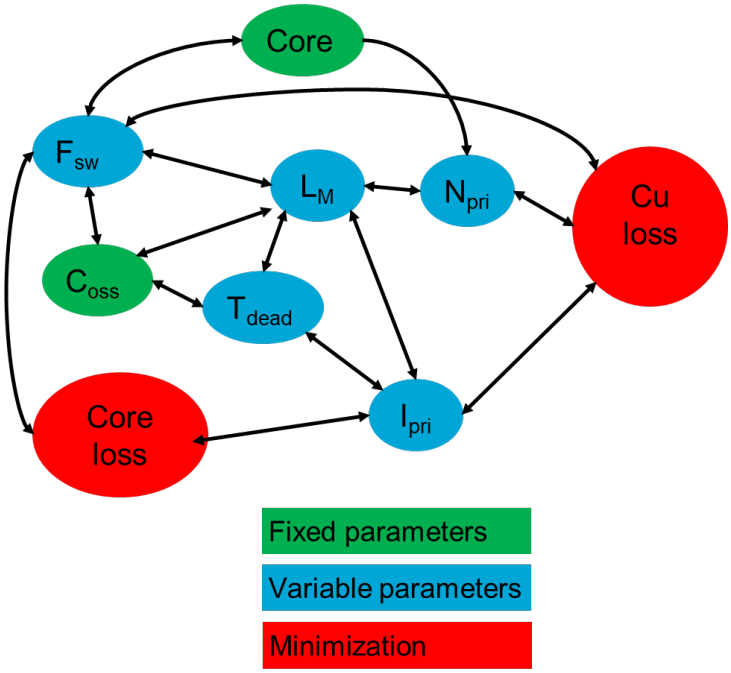


Figure 4.2: Interdependence of the various transformer design parameters

where A_e is the core area, l_e is the effective length and μ is the core permeability.

Further, the value of f_{sw} and N_{pri} also effect the magnitude of R_{ac} through (4.3) and (4.5).

Finally, several constraints are imposed on these parameters:

- Core material determines the limits on switching frequency ($< 500kHz$) and flux density ($< 0.4T$).
- Input and output voltages from the specifications determine the relation of the primary and secondary turns.
- Current density ($< 4A/mm^2$) limits the current through the transformer windings for a given trace width.
- Maximum of eight layer PCB can be used for the windings as the manufacturing cost increases significantly for more layers.

Using these relations, the total loss from Equation 4.6 can now be represented in terms of these parameters. A MATLAB script has been developed to capture this complex web of interdependencies and constraints and perform the optimization.

4.1.2.3. Optimization Results

The optimization is carried out with the objective of minimizing the value of (4.6) subject to the various constraints highlighted in Section 4.1.2.2. The optimal values

of the various parameters at the minimum value of the objective function are found and summarized in Table 4.1. The leakage inductance (L_{lk}) is not a part of the optimization problem but is calculated from the obtained results using the methods employed in [51]. Further, it may be noted that the dead time can be tuned to suit the needs of the hardware implementation.

Table 4.1: Transformer optimization results

Parameter	Symbol	Value
Primary inductance	L_m	30.5uH
Leakage inductance	L_{lk} or L_r	0.75uH
Switching frequency	f_{sw}	500kHz
Dead time	t_{dead}	50ns
Primary turns	N_{pri}	8
Secondary turns	N_{sec}	10
Core loss	P_{core}	76mW
Cu loss	P_{Cu}	34.9mW

4.1.3. FEA Modelling and Comparison

Based on the initial transformer specifications obtained from the optimization, finite element models of the transformer are created in Ansys Maxwell. This is done to verify the findings and obtain other important parameters such as the leakage inductance and interwinding capacitance, which were not considered in the optimization problem. Both these parameters are crucial as the leakage inductance is used as the resonant inductor of the LLC converter and the interwinding capacitance must be minimized to suppress the EMI.

Three possible configurations of the windings on the transformer are discussed in the following sections. Their results are quantified in Table 4.2. It may be noted that the windings in blue are primary and windings in yellow represent the secondary in the respective figures.

4.1.3.1. Interleaved

Here the primary and secondary windings are both wound around the center leg in an alternating fashion as seen in Figure 4.3. The primary side has two windings on four layers each to make a total of eight turns.

Due to the tight coupling of the windings, this configuration would have high interwinding capacitance which is undesirable. It is also expected to have low leakage inductance due to interleaving, which also mitigates the proximity loss caused in transformers by flux cancellation in the opposing windings.

4.1.3.2. Secondary on one side leg

Here the primary winding is wound around the center leg while the secondary windings are placed around one side leg of the core as seen in Figure 4.4. The primary is again wound with two windings on four layers each to keep the analysis consistent with the interleaved case. However, it is also possible to have a configuration

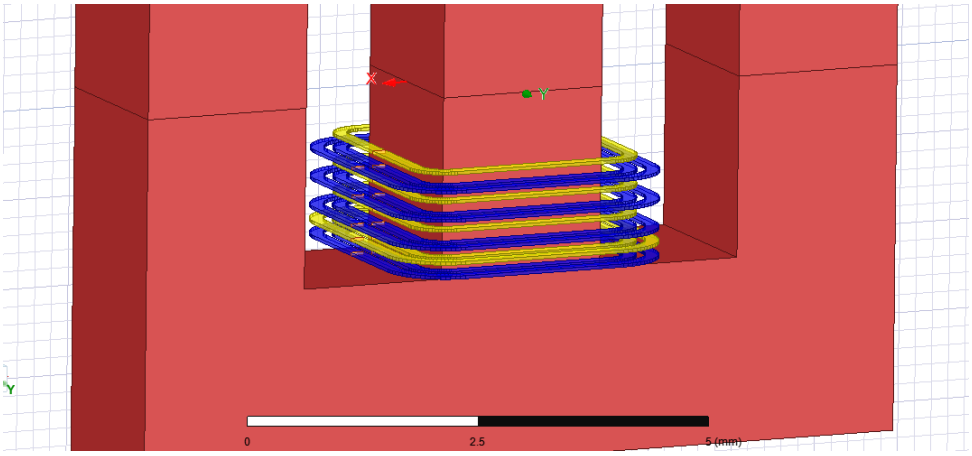


Figure 4.3: Interleaved winding configuration

where there is one turn on each of the eight layers of the PCB. This configuration will be discussed further in Section 4.1.6.1.

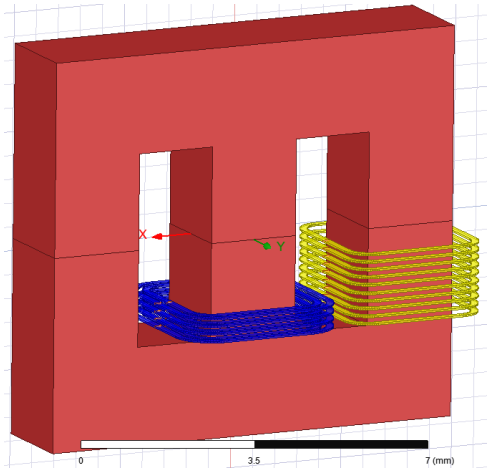


Figure 4.4: Secondary winding on one transformer leg

It is found that in this case, the leakage inductance is very high. This is because only half the flux generated from the primary winding links to the secondary coils, causing the magnitude of leakage inductance to be comparable to that of the magnetizing inductance. Hence this design is also unviable for the converter.

4.1.3.3. Secondary split across side legs

The primary windings are on the center leg while the secondary winding is split across the two side legs and connected in series as seen in Figure 4.5.

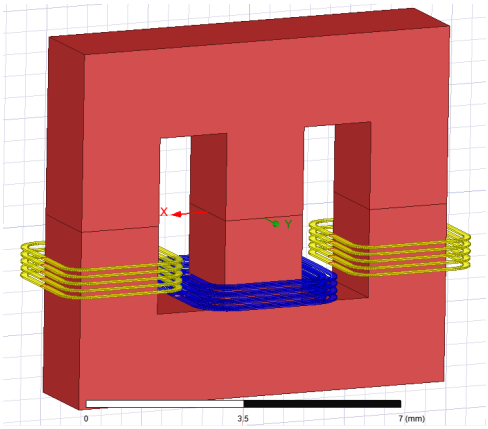


Figure 4.5: Secondary windings split across transformer legs

This configuration has a higher coupling than the previous case but less than the interleaved windings. Further, it maximizes the distance between the primary and secondary sides, thereby minimizing the capacitance linking them. This is also evident from Equation 4.9.

$$C = \frac{\epsilon A}{d} \tag{4.9}$$

Table 4.2: FEA results of the three configurations

	Coupling	$L_m(\mu\text{H})$	$L_{lk}(\mu\text{H})$	$C_{pri-sec}$ (pF)	Remarks
Interleaved	0.9995999	80.14	0.032	9.3	Interwinding capacitance is high
One Leg	0.59	80.27	32.91	2.2	Coupling is very low
Two Legs	0.993373	80.28	0.532	0.88	Low capacitance and high coupling

The results of the FEA are summarized in Table 4.2. Based on this analysis, the split winding configuration is chosen for the transformer design. A discrepancy can be seen in the analytical and FEA calculations of the primary inductance (L_m). The reason for this was only identified after a hardware prototype was developed and will be addressed in Section 4.1.6.2. For now, the results obtained from the FEA are assumed correct and a SPICE simulation is conducted to verify the functioning of the converter.

4.1.4. SPICE Verification

Using the results obtained from the analytical and finite element analysis, it is now possible to electrically model the transformer and determine how the whole system performs. This is done using a circuit simulation in LTspice. The schematic used can be seen in Figure 4.6

Firstly, the output voltage regulation is observed in Figure 4.7 .

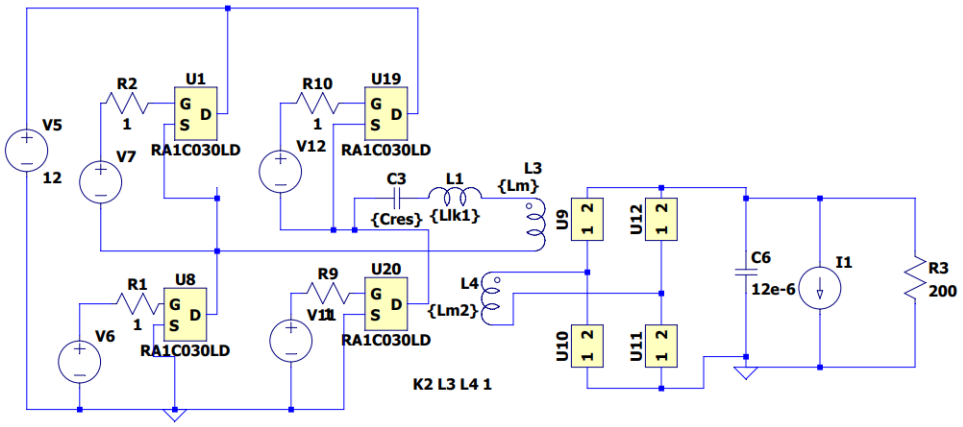


Figure 4.6: LTspice schematic used for circuit simulation

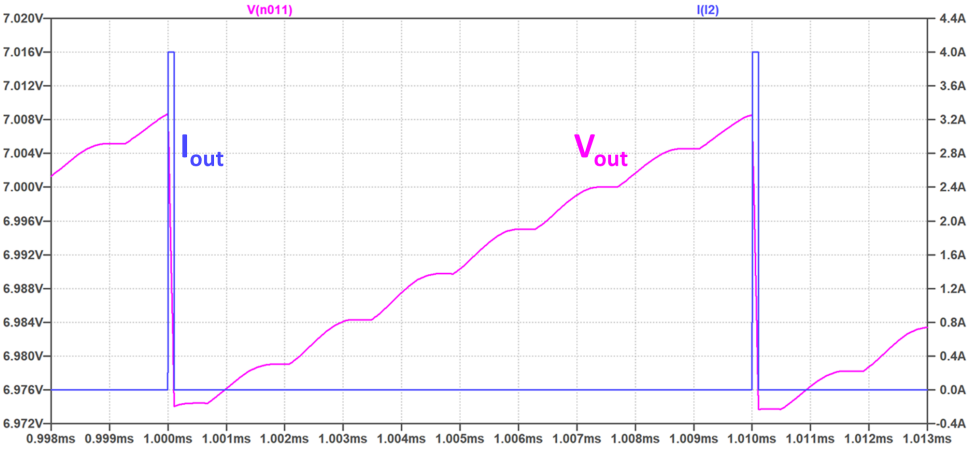


Figure 4.7: Output voltage regulation

Pulses of 4A are applied at the output to emulate the functioning of the GaN gate driver. It can be seen that the output voltage is tightly regulated even in an open loop setup. Further, the soft switching can be seen in Figure 4.8.

Overall, the losses are minimized due to soft switching and a tightly regulated output voltage is obtained, thereby verifying that the designed converter fulfills the design requirements.

4.1.5. Design summary

The important parameters obtained from various analyses are summarized in Table 4.3

The efficiency of the system is estimated to be 72.55% using (4.10). Overall,

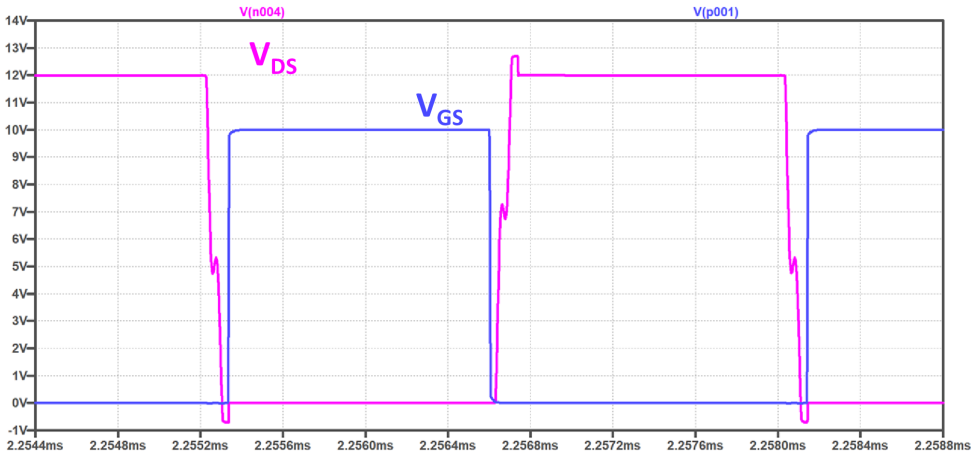


Figure 4.8: ZVS across primary MOSFETs

Table 4.3: Design Summary

Parameter	Symbol	Source	Value
Magnetizing inductance	L_m	FEA	80.28μH
Leakage inductance	L_{lk} or L_r	FEA	0.532μH
Interwinding capacitance	$C_{pri-sec}$	FEA	0.88pF
Core loss	P_{core}	FEA	59.3mW
Cu loss	P_{Cu}	FEA	1.4mW
Input Power	P_{in}	SPICE	497.87mW
Output Power	P_{out}	SPICE	405.25mW

it is seen that the system performance and parameters are satisfactory, hence the planar transformer for this configuration is designed in the following section.

$$\eta = \frac{P_{out}}{P_{in} + P_{core} + P_{Cu}} * 100\% \tag{4.10}$$

4.1.6. Planar Transformer Design

Three variants of the planar transformer are constructed for the one output converter to validate the design. A eight layer PCB is used to accommodate the required number of turns as higher layer counts significantly increase the production costs.

4.1.6.1. Configurations

As highlighted in Section 4.1.3, the transformer has eight primary turns on the center leg and five secondary turns each on the side legs. The windings on each layer are connected to the next layer using vias to form a series connection. Further, the manufacturing tolerances of the PCB vendor are taken into account to create

a manufacturable design [52]. Based on this setup, three variants of the planar transformer are designed to compare the parameters. These configurations are:

- **Interleaved:** Here the primary and secondary windings are both wound around the center leg of the transformer. The respective windings are wound on alternate layers to maximize the coupling between the two sides as seen in Figure 4.3. This configuration is expected to have the highest interwinding capacitance and lowest leakage inductance due to the maximum overlap of the two windings. It must be noted that this setup is only used for comparison and will not be employed in the converter.
- **4x2 Primary:** The primary windings consists of two turns on each layer across four layers of the PCB as seen in Figure 4.5. The secondary windings consist of one winding on each layer around both side legs which are connected in series to form a total of ten turns.
- **8x1 Primary:** The primary winding consists of one winding for each layer, which are then connected in series. The secondary winding configuration is the same as before. This configuration is expected to have a lower leakage inductance than the 4x2 configuration due to the tighter coupling of the primary windings with the core.

The PCB windings for the three configurations can be seen in Figure 4.9.

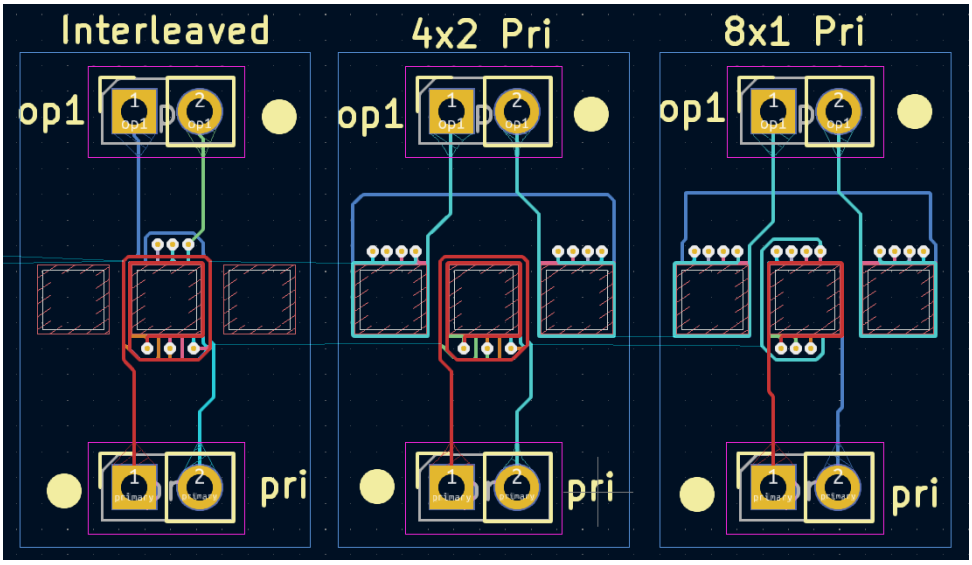


Figure 4.9: PCB winding variations

Measurements of the primary inductance (L_m), leakage inductance (L_{lk}), and interwinding capacitance ($C_{pri-sec}$) are conducted using the Bode100 vector network analyzer using the methods described in [53]. The measurements can be

seen in Figure 4.10 and the values at a frequency of 350kHz and are summarized in Table 4.4.

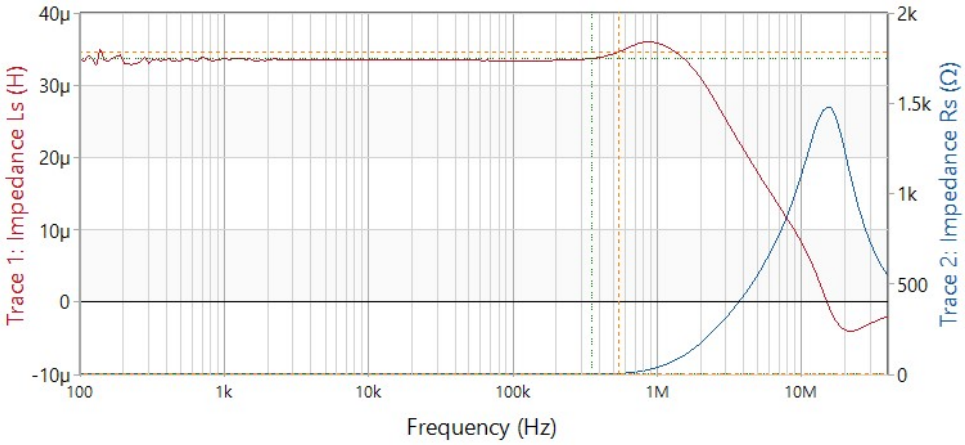


Figure 4.10: Primary winding measurement

Table 4.4: Measured parameters of the three transformer configurations

	L_m (μH)	L_{leak} (μH)	$C_{pri-sec}$ (pF)	$R_{ac}(\Omega)$
Interleaved	35.2	0.74	9.36	3.135
4x2	36.8	1.58	2.1	1.82
8x1	34	1.34	2.65	1.9

As expected, the interleaved case has the highest interwinding capacitance. The parameters of the 4x2 and 8x1 configurations are quite similar and both can be employed for the design. Further, it is seen that the inductance of the coil starts increasing after a frequency of about 400kHz and peaks around 900kHz. This may be attributed to the frequency dependent permeability of the N87 magnetic material as seen in the datasheet [54].

4.1.6.2. Parameter Discrepancy

It is seen here that the measured primary inductance of the transformer (36μH) is significantly lower than that of the FEA model (80μH), from Section 4.1.5. This is a considerable difference between the designed and physically realized values. This difference can be attributed to the presence of a non-zero air gap between the two core halves even when they are properly aligned with each other, as illustrated in Figure 4.11.

This non-ideality was not considered in the original FEA model. This hypothesis is verified by introducing a known airgap of 40μm and 80μm between the two core halves by placing a piece of paper and measuring the inductance. A new FEA is

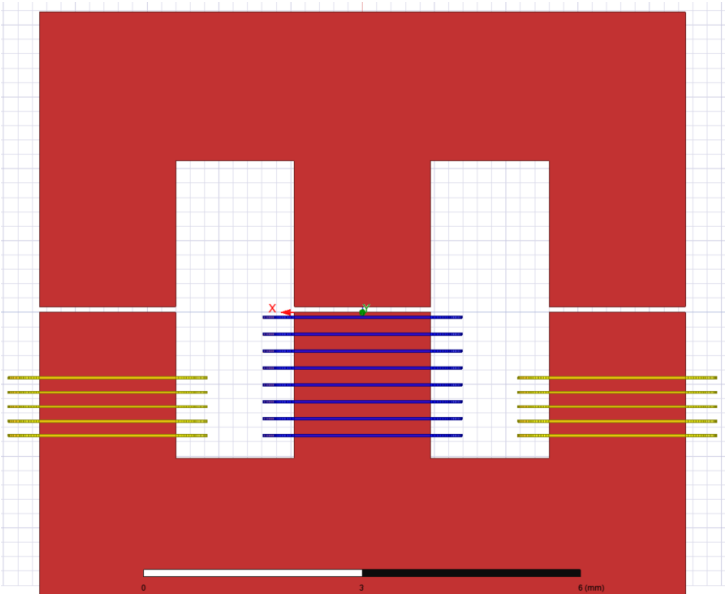


Figure 4.11: FEA model of transformer with a non-zero airgap

conducted with the same airgap values to validate the model and the results are compared as seen in Table 4.5.

Table 4.5: Comparison of transformers with air gap

Airgap	Configuration	$L_m(\mu\mathrm{H})$	$L_{lk}(\mu\mathrm{H})$
$40\mu\mathrm{m}$	Hardware	6.2	1.31
	FEA	5.8	0.36
$80\mu\mathrm{m}$	Hardware	4.05	1.41
	FEA	3.33	0.34
$4\mu\mathrm{m}$	Hardware	33.71	1.34
	FEA	33.67	0.387

This analysis confirmed that it was indeed the air gap that causes the discrepancy. A FEA sweep is conducted with various values of air gaps and the primary inductance values are recorded to determine the actual air gap in the hardware. It is found that an air gap of approximately $4\mu\mathrm{m}$ exists between the two core halves, which causes the drift from the anticipated values. This is likely caused due to the surface roughness of the cores, causing imperfect contact between the two halves. These results also align with the analytical calculations conducted in Section 4.1.2.

4.1.6.3. SPICE verification

Now that the real parameters of the transformer are known, a LTspice simulation is conducted using the circuit in Figure 4.6 to verify the functioning of the system.

Firstly, the output voltage regulation for both the outputs is observed in Figure 4.12 .

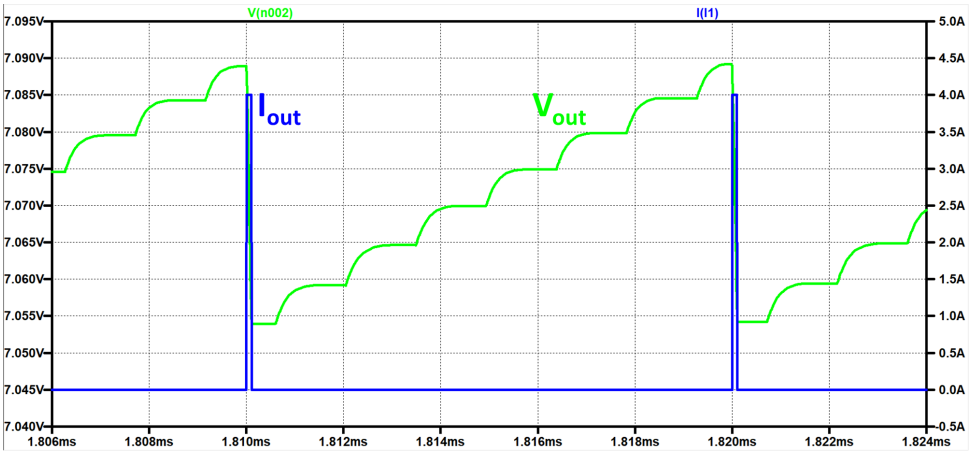


Figure 4.12: Output voltage regulation

Further the soft switching can be seen in Figures 4.13

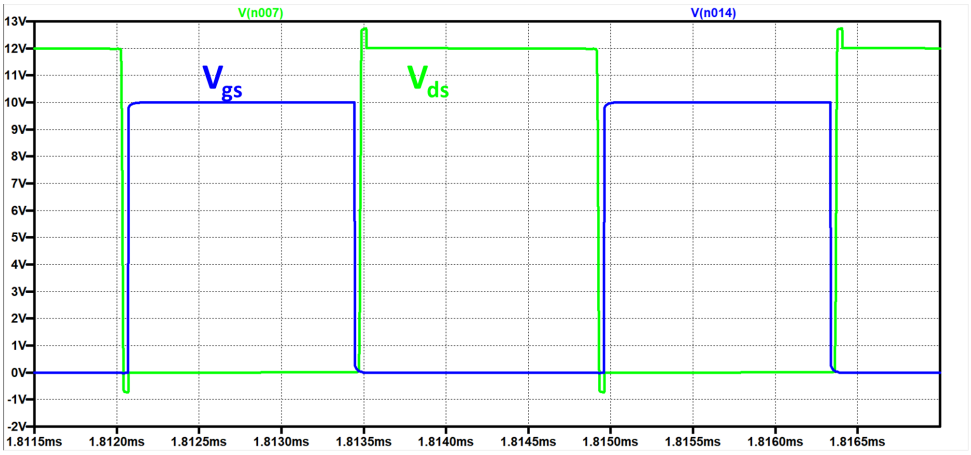


Figure 4.13: ZVS across primary MOSFETs

An increase in the resonant tank current is expected due to the lower inductance, which will increase the conduction losses of the system. The efficiency of the system is estimated to be 75.29% using (4.10).

Overall, it is seen that the system will still meet the desired specifications. Hence, this methodology discussed in this chapter is extended to the design of the multiple output transformer.

Table 4.6: Design Summary

Parameter	Symbol	Source	Value
Magnetizing inductance	L_m	Hardware	33.71uH
Leakage inductance	L_{lk} or L_r	Hardware	1.34uH
Interwinding capacitance	$C_{pri-sec}$	Hardware	2.65pF
Core loss	P_{core}	FEA	59.4mW
Cu loss	P_{Cu}	FEA	4mW
Input Power	P_{in}	SPICE	483.2mW
Output Power	P_{out}	SPICE	411.56mW

4.2. Multi Output Transformer Design

A four level FCML inverter has six switches in each leg (Figure 1.2). Hence, a multi-output converter with one input and six isolated outputs would be ideal as only one power supply could be used for each switching leg of the inverter. The converter may now look like Figure 4.14.

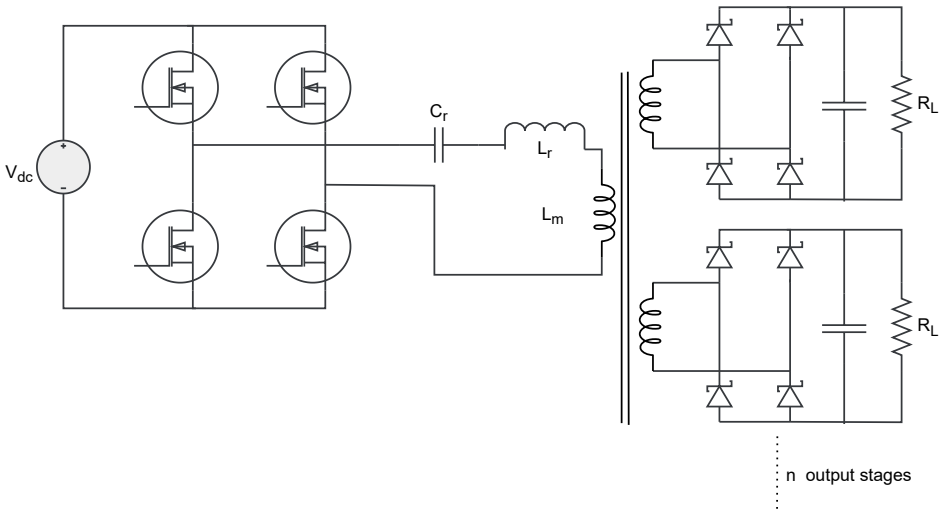


Figure 4.14: Multiple output LLC converter

4.2.1. FEA Modelling

The design procedure used for the single output converter discussed in Section 4.1 may be extrapolated for this design. The same core, E8.8 from TDK is used and a FEA model as seen in Figure 4.15 is created to verify the transformer parameters. The primary winding is in red around the center leg. The corresponding series connected output windings around the side legs are of the same colour. It can be seen that the output windings which are close to the core on one leg are placed far away

from the other leg. This is done to balance the coupling and leakage inductance across the various outputs and obtain a uniform output voltage. It is determined that a total of four PCBs can be stacked in the chosen planar transformer. The bottom PCB would have the input winding around the center leg and the other three PCBs would have two output windings each. Hence, the overall system would consist of one input and six output windings on the same core. These windings can then be interfaced to their respective electronics to obtain the input and output stages. This configuration is determined after considering the manufacturing tolerances from the PCB vendor [52], which limited the minimum distance required between two traces and also the minimum distance between the trace and the hole cutout for the core.

The leakage inductance is found to be around 0.86 μH for the various windings and is slightly higher than the single output case due to looser coupling of the windings. The interwinding capacitance is estimated to be 0.35pF.

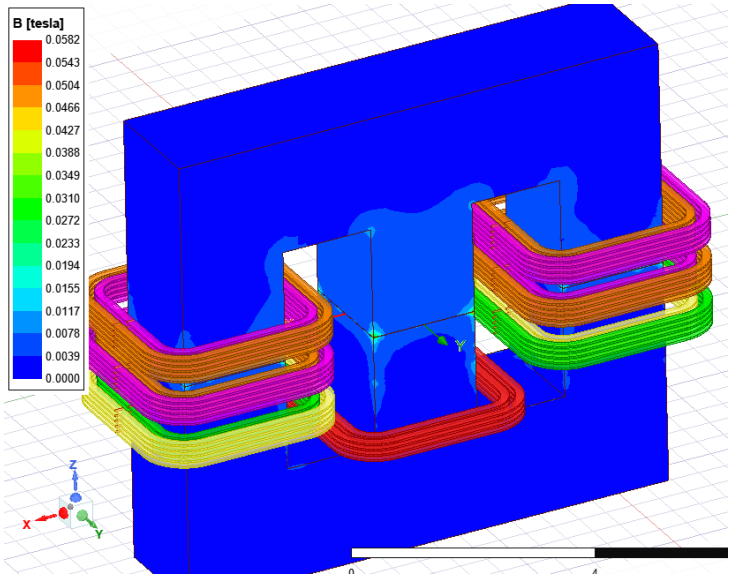


Figure 4.15: FEA model of six output transformer

4.2.2. Planar Transformer Design

Four PCBs of 0.8mm thickness and eight copper layers each would be stacked in the core window to form the transformer, which has a total height of about 4mm [47].

As seen in Figure 4.16, the first PCB would consist only of the primary winding. Both the output boards have the same copper windings pattern around the core legs. The first output side PCB has an output on the left and right extremities. The topside output PCB can be flipped upside-down to create another two outputs in the stack for a total of six outputs as seen in Figure 4.17. The copper traces have

been hidden for clarity.

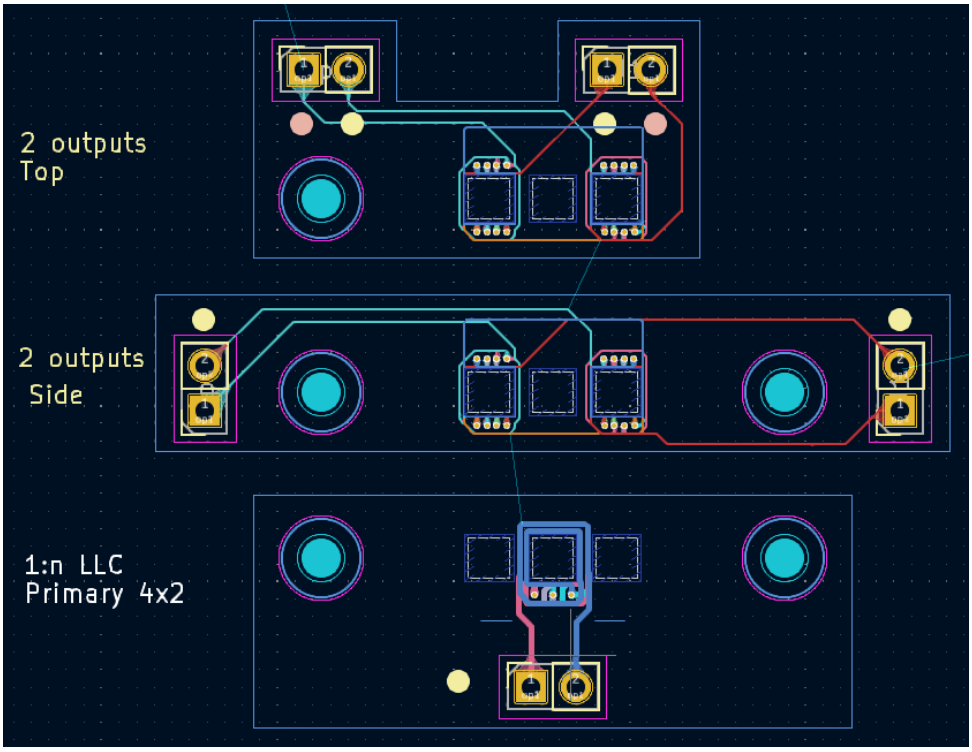


Figure 4.16: Primary and secondary windings of the multiple output transformer

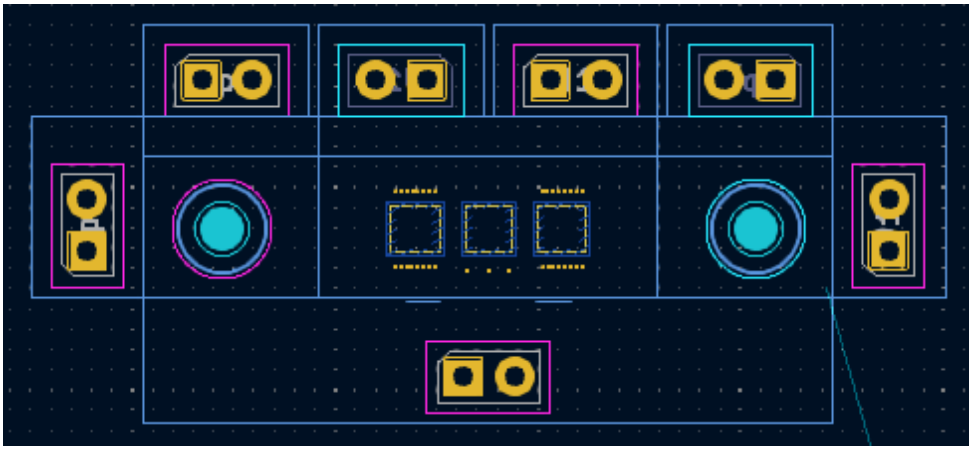


Figure 4.17: Visualisation of multi-output transformer stack

This configuration is modular, as the output stage PCBs can be added or removed from the stack to achieve the required number of outputs. Further, a reduction in interwinding capacitance is expected as compared to the previous single output transformer, as there is physically no overlap between the primary and secondary windings due to them being on entirely different PCBs.

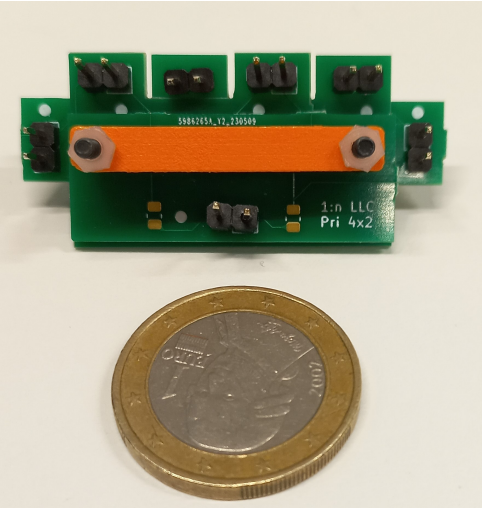


Figure 4.18: Prototype of the multiouput transformer with a coin for scale

The parameter measurements are made for this transformer and summarised in Table 4.7. Here $L_{lk}-pri$ is the leakage inductance of the output winding as seen from the primary side.

Table 4.7: Measured parameters from the six output transformer

Winding	$L_m(\mu\text{H})$	$L_{lk}-pri(\mu\text{H})$	$C_{pri-sec}$ (pF)
Primary	36.8	-	-
Output 1	13.703	1.710	2.21
Output 2	13.624	1.627	2.55
Output 3	11.620	4.802	2.95
Output 4	11.549	4.905	2.97
Output 5	13.640	1.697	2.54
Output 6	11.500	5.087	2.52

The interwinding capacitance ($C_{pri-sec}$) is less than 3pF which is significantly smaller than the 15 to 80pF value found in commercially available solutions as highlighted in Section 2.5. A wide variation in the leakage and magnetizing inductances across the windings is also observed. The reason for this is found to be two-fold:

1. The winding of one of the outputs had to be a partial turn to allow for ease

in the routing of the PCB traces. This can be seen as the red copper trace in Figure 4.19.

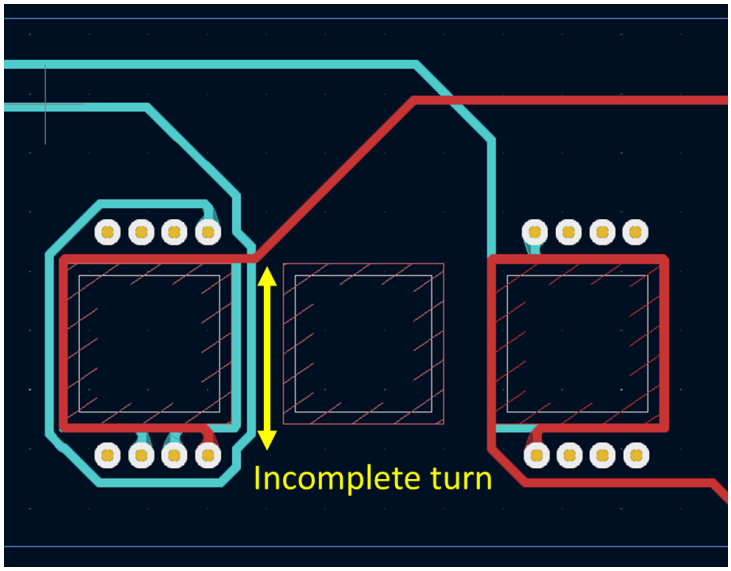


Figure 4.19: Incomplete turn in output 6

2. There is a difference in the way the windings are routed to their respective outputs which creates an area of extra leakage energy to be stored. This is highlighted in Figure 4.20.

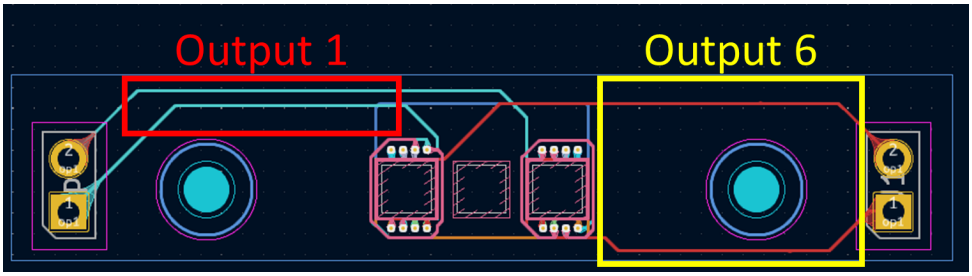


Figure 4.20: Extra winding area in the output 6 storing extra leakage energy

Both of these characteristics are replicated across the three output boards and can be observed in Table 4.7.

4.2.3. SPICE Verification

A SPICE simulation is conducted using the measured transformer parameters to verify the functioning of the multi output converter. To simplify the simulation,

only two output windings with the minimum and maximum leakage inductances are considered. The simulation schematic can be seen in Figure 4.21.

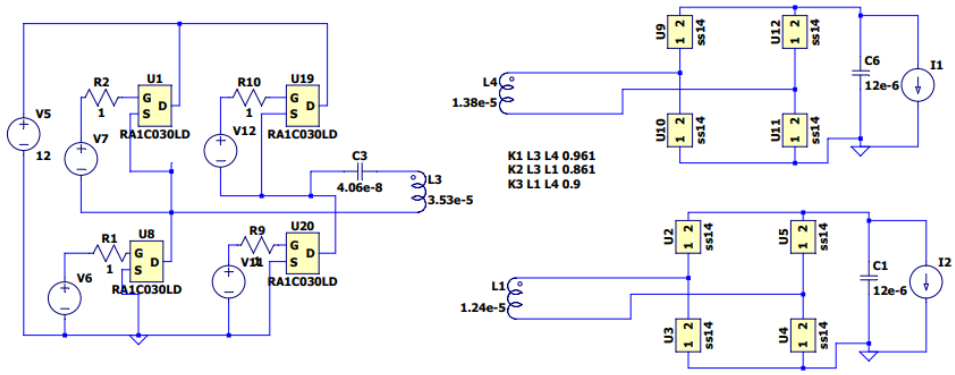


Figure 4.21: Simulation schematic of multi output converter

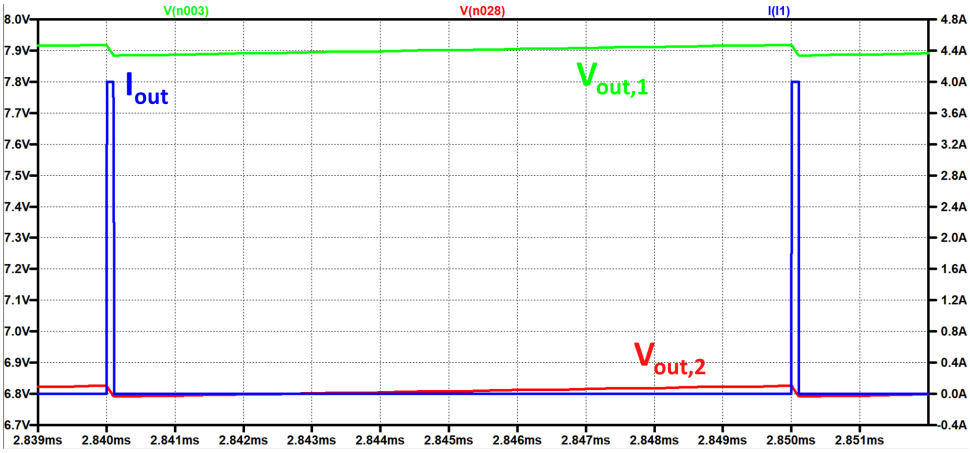


Figure 4.22: Output voltage of two output windings

It is seen that the output voltage is higher for the winding with lower leakage inductance due to lower impedance. Hence, a variation in winding voltages can be expected. However, the voltages are still tightly regulated for the given load.

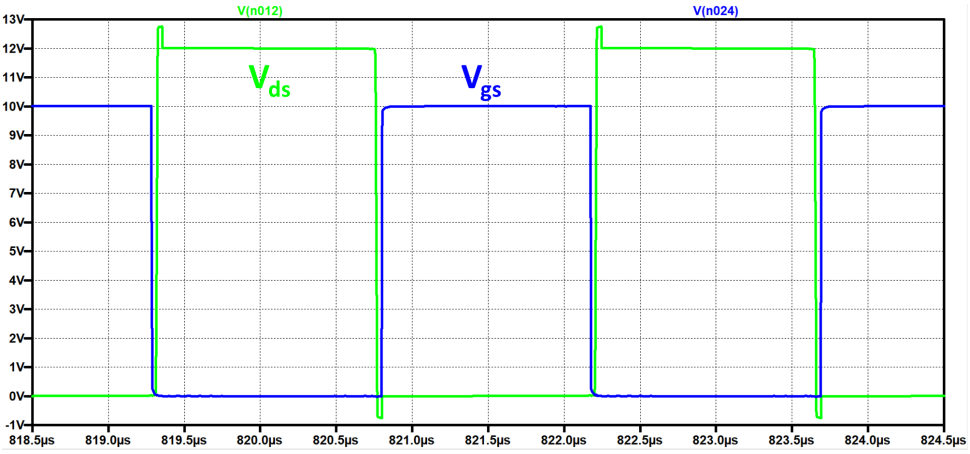


Figure 4.23: Primary side ZVS in the multi output converter

5

Results

The PCBs designed in Chapter 3 are populated and tested for both, the single and multi-output converters. The results obtained from this testing will be discussed in this chapter.

5.1. Experimental Setup

The assembled converter with the respective input and output stages and the multioutput transformer can be seen in Figure 5.1.

For both, the single and multi-output configurations, the same PCBs are used for the input and output stages. Only the transformer is changed between the two converters. The converter is tested using the following setup:

- The primary side full bridge is connected to a capacitor bank as seen in Figure 3.6. For a given leakage inductance, this allows for flexibility in the choice of resonant frequency (f_{res}) based on (3.1).
- The regulated input 12V is provided using a DC power supply.
- The converter load is varied using axial resistors. 120 Ω is used on the output side to emulate the fully loaded condition of approximately 0.3W per output stage.
- The PWM pulses of the desired frequency are provided using a signal generator to control the switching frequency (f_{sw}) of the converter.

5.2. Single Output Converter

5.2.1. Soft Switching

One of the main advantages of the LLC converter is its ability to minimize losses through soft switching. The voltage and current through the resonant tank at the

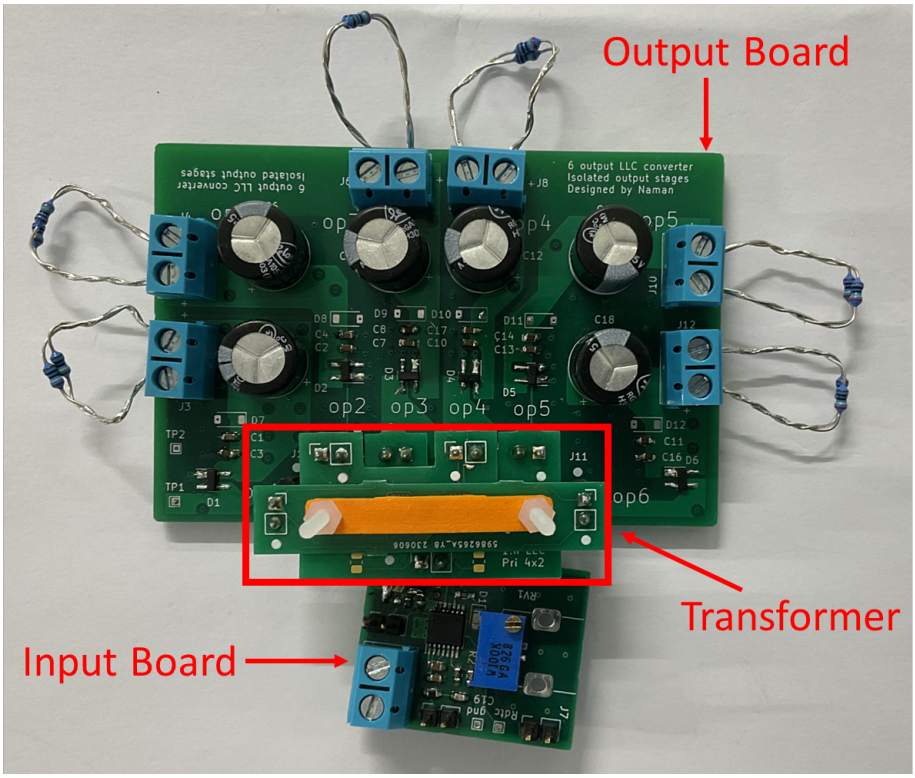


Figure 5.1: Multi output converter prototype

resonant frequency of 452kHz and switching frequency of 470kHz can be seen in Figure 5.2.

It can be observed that the current in the tank lags the voltage applied across it, implying that the converter operates in the inductive region and ensuring ZVS operation as discussed in Section 3.1.3.

5.2.2. Efficiency

The efficiency of the single output system is measured by finding the ratio of output and input powers using the WT500 Power Analyzer. The dead time is varied from 40 to 180ns for various switching frequencies, but no noticeable variation in efficiency is observed. Hence the dead time for the converter is set to a nominal value of 100ns for the measurements.

The signal generator is used to vary the converter's switching frequency from 300kHz to 1200khz for various resonant frequency values to find the most efficient operating points. The resonant frequency is varied using the discrete values of the capacitor in the resonant tank. The variation in efficiency can be seen in Figure 5.3a.

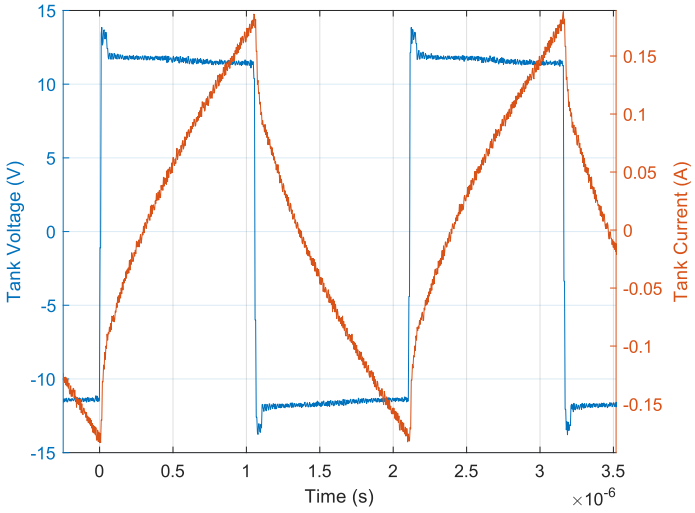
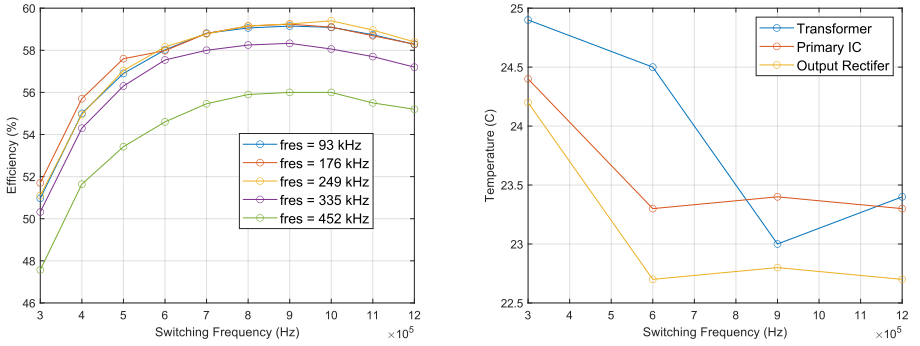


Figure 5.2: Resonant tank voltage and current



(a) Single output converter efficiency **(b)** Temperature of various components

Figure 5.3: Full load efficiency analysis of single output converter

A peak efficiency of approximately 59.4% is measured for the single output converter at a full load of 0.3W. While this value may be on the lower side, it is expected as the system is designed for a higher power level.

To understand the relative distribution of losses, the temperatures of the primary full bridge (MAX2258AUD IC), the transformer, and the output rectifier are measured for various switching frequencies at a resonant frequency of 452kHz. The temperature of each component can be seen in Figure 5.3b.

It can be seen that the losses in the switching elements are relatively higher below the resonant frequency due to hard switching. Once above the resonant

frequency, the switch losses decrease as reflected by the temperature. Further, the transformer temperature is minimum at 900kHz, implying the lowest losses and hence the highest efficiency.

The reason for this behaviour is twofold. Firstly, the increasing switching frequency reduces the Root Mean Square (RMS) current in the resonant tank as seen in Figure 5.4. Further, as seen in Figure 4.10, the inductance of the coil is maximum at approximately 900kHz, which minimizes the magnetizing current in the circuit. Both of these factors reduce the conduction losses in the transformer.

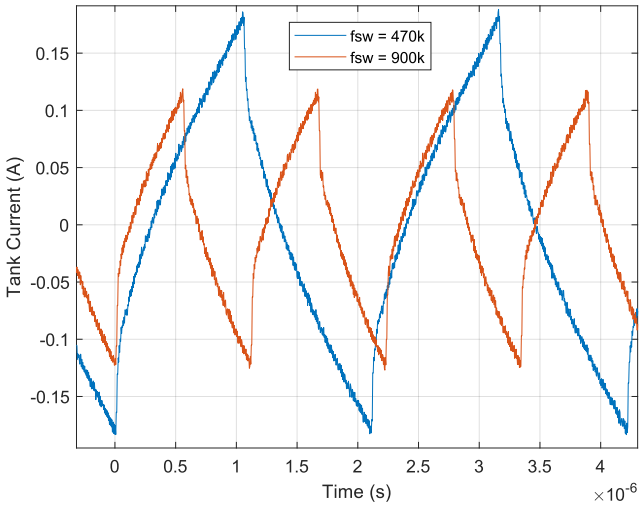


Figure 5.4: Current ripple for different switching frequencies

However, beyond the 900kHz, the inductance starts to decrease again and the transformer core losses start to dominate according to (4.1), leading to a reduction in efficiency.

5.2.3. Voltage Regulation

The output voltage of the converter is observed for various loading levels. The measurements are conducted at a switching frequency of 260kHz and 900kHz for a resonant frequency of 250kHz.

It is seen that the output voltage is fairly well regulated between low load and full load conditions. However, at no load conditions, the output voltage increases drastically due to the resonant current in the switching transition. This is not expected to be an issue in the intended application as there is always a quiescent load from the gate driver. Several methodologies to mitigate this phenomenon have been investigated in literature [55], however, these are beyond the scope of this thesis. Further, a lower output voltage is measured for the higher switching frequency as expected according to (3.3).

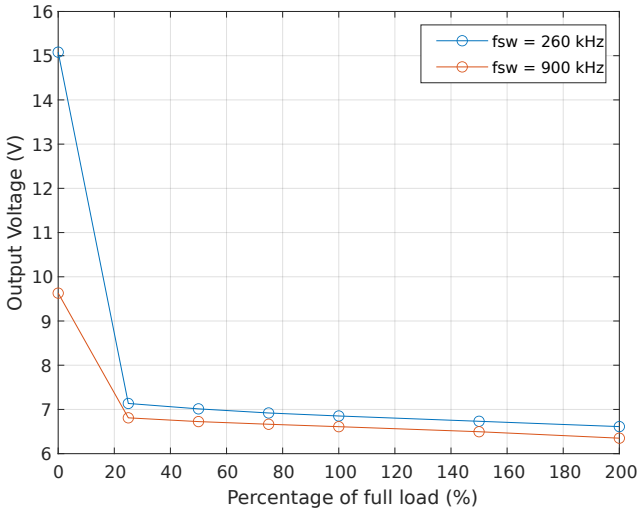


Figure 5.5: Single output voltage for various loads at f_{res} = 250kHz

The quality factor (Q) of the converter can be calculated from (3.7). For a resonant frequency of 250kHz, $Q = 0.0081$, which is a relatively low loaded condition. As seen in Figure 3.4, the converter gain at low loads is quite flat with increasing switching frequency. Hence, similar output voltages are obtained for a $f_{sw} = 260kHz$ and $f_{sw} = 900kHz$. This allows for higher switching frequencies which reduces losses without affecting the output voltage.

5.3. Multi-output converter

The multi-output converter consists of six isolated outputs for one leg of the FCML inverter. The final prototype can be seen in Fig 5.1.

5.3.1. Soft Switching

The resonant tank current for the multi-output convert can be seen in Figure 5.6. Compared to the waveform of the single output converter in Figure 5.2, it is seen that the current magnitude is greater than the single output case. Further, the current is more sinusoidal as the ratio of the load current to the magnetizing current is increased.

5.3.2. Efficiency

The efficiency of the converter is measured at full load conditions for various switching frequencies. The total combined output power of the converter is approximately 1.8W. The resonant frequencies of the various windings vary from 220kHz to 380kHz based on the respective leakage inductances as seen in Table 4.7. These can be seen in Figure 5.7.

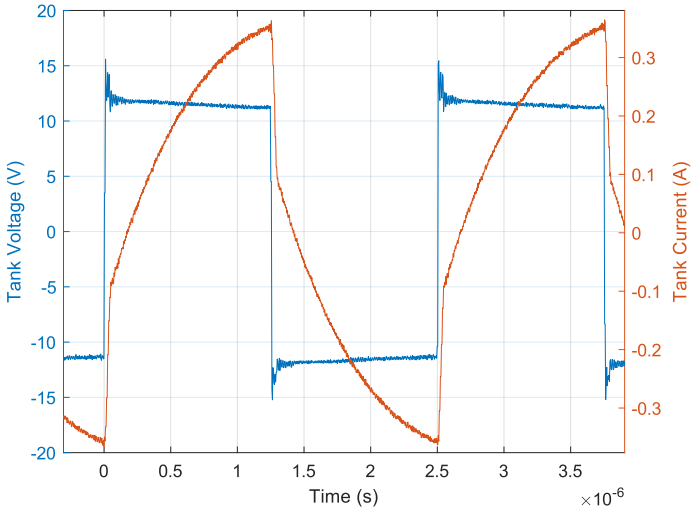


Figure 5.6: Resonant tank voltage and current in the multi output converter

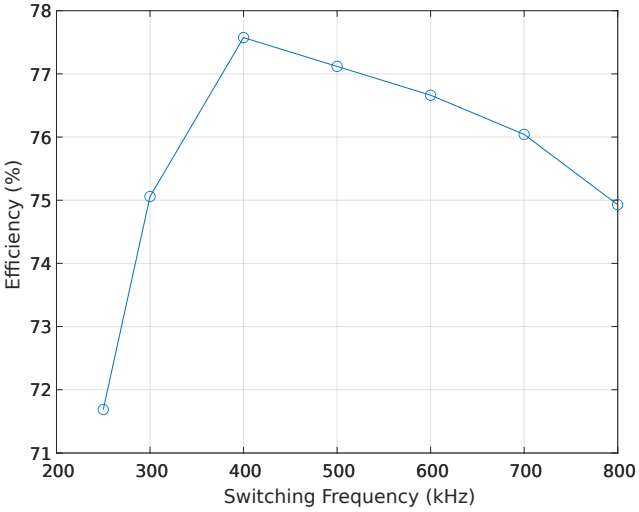


Figure 5.7: Multi output converter efficiency for various switching frequencies at full load

A peak efficiency of 77.5% is measured at a switching frequency of 400kHz, after which it drops rapidly due to an increase in transformer losses as discussed previously.

5.3.3. Voltage Regulation

The effect of change in load in one of the outputs on the other outputs is examined to measure the cross-regulation performance. The load on output one is varied from no load to twice the full load. The measured voltages can be seen in Figure 5.8. The difference in output voltage across the windings can be attributed to the varying value of leakage inductance, where by the outputs with the higher leakage have a lower output voltage.

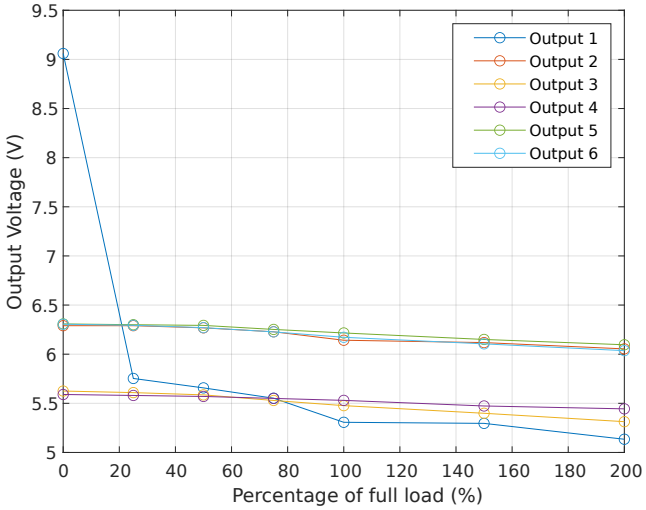


Figure 5.8: Multi-output converter cross regulation performance at f_{sw} = 400kHz

It is seen that the other outputs are still tightly regulated with a load variation on output 1, thereby providing good cross voltage regulation characteristics.

5.4. Testing Summary

The designed prototypes have been tested and their performance has been analyzed. The following characteristics are observed:

- The peak efficiency of the multi-output converter (77.5%) is comparable to the conventionally available solutions.
- The interwinding capacitance (<3pF) is better than the commercially available solution and at par with the benchmarks in literature.
- The primary switches undergo ZVS, thereby minimizing losses.
- There is some variation in the output voltage across different windings due to different magnetizing and leakage inductance values. However, the converter displays good self and cross-regulation characteristics.

6

Conclusions

6.1. Discussion

The use of multi-level inverters utilizing WBG devices appears to be the next breakthrough in boosting the performance and adoption of EVs. However, this transition also brings several challenges. One of the crucial barriers, the high side bias power supplies for such converters was researched and designed in this thesis.

- **Chapter 1** introduced the research topic and provided some context into the issues which need to be addressed in GaN switched FCML inverters.
- **Chapter 2** explored the various high side power supply architectures found in literature to examine them in context of the requirements and determine the best candidate.
- **Chapter 3** described the working principles of the LLC converter which justify its selection for this application. The design of the power electronics stages are further discussed in this chapter.
- **Chapter 4** discussed the design procedure from analytical modelling to PCB design for the planar transformer of a single and multi-output LLC converter.
- **Chapter 5** dealt with the testing and performance of the designed prototype.

The thesis aimed at answering the following research questions:

1. **What architectures are capable of providing a continuous power supply to the high side gate drivers to support a variety of modulation schemes for the inverter?**

   The various bias power supply architectures were examined. It was found that the isolated DC stages provide the most reliable and efficient solution for an FCML inverter.

2. **Which power supply architecture is the most compact to achieve a high power density in MLCs?**

   Of all the isolated converter topologies, it is possible to operate the LLC converter at a high frequency without incurring significant switching loss and also have the resonant tank integrated into the isolation transformer. Further, it is also possible to have multiple outputs in the same LLC converter. This allows for compact magnetics and improves the power density of the system.

3. **Which topology can mitigate the EMI in a fast switching GaN inverter?**

   Various topologies of isolated power stages were compared. It was found that the LLC converter proved best in EMI mitigation due to its ability to operate with a high leakage inductance in the transformer which is in an inherent trade-off to reduce the CM current coupling through the interwinding capacitance of the isolation transformer and hence mitigate the EMI.

4. **Which topology would be the most efficient for the required specifications?**

   The LLC converter is capable of soft switching without extra circuitry. This drastically reduces losses and improves efficiency, while still having a simple and cheap design.

Based on these requirements, a multiple output LLC converter was designed, prototyped, and tested in this thesis. The design methodology of the multiple output isolation transformer has been detailed from an initial analytical model to the final prototype.

The tested prototype has a peak efficiency of about 77.5% and an interwinding capacitance of less than 3pF, which are all at par or better than the commercially available solutions.

Finally, the converter provides six isolated output stages required for a 4-level FCML inverter, which improves power density and reduces the design complexity of the overall system.

6.2. Future Scope

This thesis looked into the prototyping of multiple output LLC converter for a high side bias power supply application. The final prototype demonstrates good functionality, however, there are several improvements that can be made to the design which are discussed below.

1. The initial design of the transformer was inaccurate as it did not account for the intrinsic air gap between the two core halves. The lower magnetizing inductance permits a higher current in the windings which reduces the efficiency of the system due to higher conduction losses. Optimizing the transformer parameters with the inclusion of air gap effects can further increase the system efficiency.

2. This thesis focused specifically on the reduction of interwinding capacitance for EMI mitigation. This was done by maximizing the distance between the input and output windings. However, other methodologies can also be explored and combined.

3. There is a wide variation in the leakage inductance of the different windings of the multi-output transformer. This causes a variation in the output voltages of the different isolated stages. An updated design can be created to have identical output voltages.

4. The converter is a proof of concept and was designed with a bias towards ease of prototyping and testing. The final converter can be designed to be much more compact and power dense by using smaller components and eliminating the potentiometer, op-amp circuit, and the current sense and power connectors.

5. A post-regulation stage can be designed and cascaded with the presented converter to obtain a negative gate voltage and prevent spurious turn in the inverter switches.

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