24 GHz Receiver Design

By Simonetta Rampu

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Delft University of Technology, the Netherlands

Approval

Name: Simonetta Rampu

Degree: Master of Science

Title of Thesis: 24 GHz Receiver Design

Committee in Charge of Approval:

Chair:

_____

Professor John R. Long
Department of Electrical Engineering

Committee Members:

_____

Professor R.A.C.M.M. van Swaaij
Department of Electrical Engineering

_____

Marco Spirito
Department of Electrical Engineering

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Chapter 1. Introduction and Motivation

The world of wireless sensor networks (WSN) has grown in the past years by showing potential for independent and robust functioning in extreme conditions. Ever since it emerged as a low cost, low power option to traditional wired sensors, many improvements have been developed, further upgrading the attainable specifications. Applications for wireless sensor networks are as broad as environment monitoring, military surveillance and smart homes [1, 2]. The main advantage of the sensor nodes is that they can be deployed in a variety of environments in a large number, such as hundreds or even thousands of nodes. Their miniature size (< 1 cm^3) and extended lifetime function (>5 years) require them to be dependent on battery operation or energy scavenging [2]. Consequently, additional limits are placed on the design and structure of the sensor node for constraining power consumption. Solutions have been investigated in both networking algorithms and physical implementations of RF transceivers, which represent the main power hungry constituent of the sensor node. Further examination in the direction of optimizing the power consumed by the radio is much needed [1, 3].

This work presents a low power receiver front-end which focuses on the two basic requirements for WSN radios: bringing down the power consumption and simplifying the RF architecture. In this thesis, an overview of the system design is presented and discussed, followed by the circuit design and implementation of a 24 GHz receiver in a CMOS 65 nm technology.

1.1 Introduction to Wireless Sensor Networks

As the name suggests, wireless sensor networks are a network of closely spaced sensor nodes communicating in between each other via a wireless link. The sensor performs several functions: it detects information in the environment, processes the gathered data and further transmits it through a wireless data path. The network

k can consist of a large number of sensors. For example, tens to thousands of sensors deployed around the area of interest being able to function autonomously are envisaged. Their multitude and small size are advantageous for a number of applications, including: environmental monitoring, smart buildings, and body area networks [4-6].

Each wireless sensor node has a certain system architecture, as shown in Fig.1.1. They include: sensing, processing, transceiver, and power units. The sensing unit provides two functions. It senses the environmental parameters and transforms the information of interest into digital signals using an analog to digital converter (ADC). Storing the signals of interest and managing the assigned tasks to be performed is performed by the processing unit. The transceiver unit sends and receives information to or from other nodes. The power unit provides the power for all the other units to perform their required assignments. The node may have other units attached depending on its application, such as the power generator unit [1]. All the units are integrated in a system-on-chip fashion, requiring them to occupy a small space and to be power aware [7].

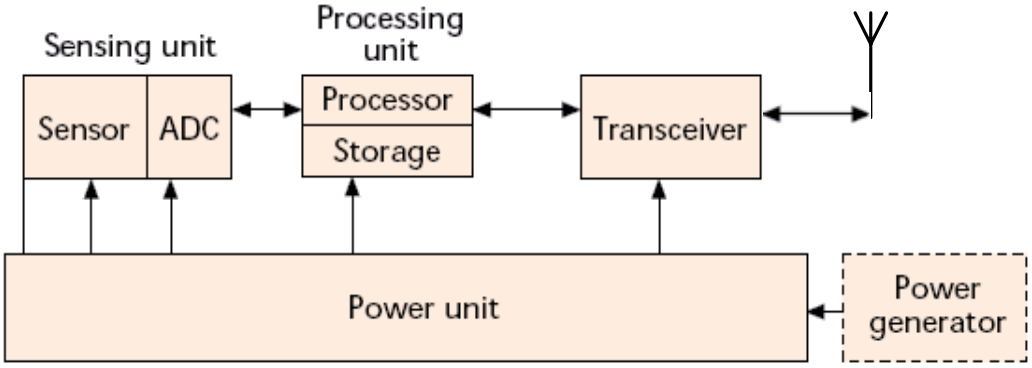

Fig.1. 1 Structure of a sensor node [1]

Yet another way to characterize a WSN is by the open systems interconnection (OSI) model. This model takes several so called layers into consideration and assigns different protocols to each layer. This protocol stack manages the sensor network's functioning. The protocols, shown in Fig. 1.2, enable the administration of power distribution, routing configuration, networking, and wireless communication.

The physical layer approaches ways to implement the radio taking in consideration modulation techniques, data rate, receiving and transmitting in an efficient manner. The

data link layer takes care of the data frame detection, medium access control and ensuring safe communication between the nodes. The medium access control (MAC) protocol is an integral part of the data link layer which sets a communication link for data transfer between the multitude of sensor nodes. The power, mobility and task management planes supply an integrated view on how the sensor nodes can manage and coordinate their power consumption, movement and task distribution [1].

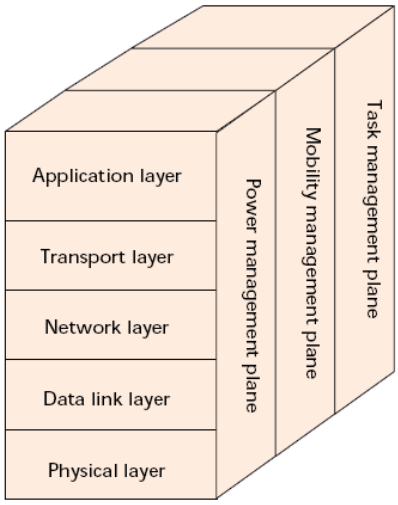

Fig.1. 2 WSN protocol stack [1]

Among the layers presented, the implementation of the transceiver for the physical layer is focused upon in this work. This layer, as mentioned before, is the wireless communication enabling technology.

1.2 Physical Layer Optimization

The sensitive issues regarding the physical layer within wireless sensor networks surround power consumption, high data rate transmission, and the modulation scheme used to encrypt the data. Among these, power consumption plays a significant role in terms of the structure of WSNs.

As mentioned above, the main characteristic of the sensor nodes is their capacity to manage tasks and further transmit the collected data on a limited power supply. They need to perform these tasks for a long time without the possibility of replenishing the power supply.

When defining a “long time”, one should understand 1 to 5 years or even more. To further realize this, one can take the classic example of powering the sensor with a 1.5 V alkaline battery voltage, which has a 2000 mAh capacity and 30 μA of leakage current. The lifetime of such a battery is defined by the following equation:

$$Lifetime = \frac{Capacity \cdot voltage}{I_{leak} \cdot voltage + P_{AVE}} \tag{1-1}$$

If the average power, P_{AVE}, is around 10 μW to 100 μW, the lifetime becomes 3 to 6 years. It is therefore the task of the sensor node to achieve this average power consumption [3]. In the following, several methods of realizing this daunting goal will be highlighted.

When figuring out the power distribution in the sensor node, it is found that the transceiver requires the most energy. The radio consumes generally more power than any other component in the sensor node. In [8], 76% of the total power is consumed by the transmitter of the transceiver. Therefore, optimizing the radio has been the attraction of much research. However, for true power optimization, the focus should be set not only on the physical layer level, but also on the MAC layer level. Radio optimization will not lead to lower power consumption if the routing, networking and data link layer of the sensor network do not have efficient algorithms to take care of the power distribution among the sensor’s different components [3]. Nevertheless, the subject of this paper will only deal with constructing a power- aware radio.

As sensor nodes send and receive data packets on a set amount of time over an idle length of time or sporadically, these are therefore considered to be duty cycled, on the order of 0.1 to 1%. Duty cycling represents the ratio between the sleeping and active modes of the sensor nodes’ radio. By employing such a low duty cycle, it is ensured that the radio will be woken up to perform its tasks for a very short period of time, thereby saving power. Hence, the P_{AVE} considered is based on this duty cycling, determined by limiting the time that the radio is turned on, which sets the requirements of the sensor node’s overall power

consumption. Duty cycling is used by almost every WSN and has become a standard modality to achieve the average power [1, 3, 9].

Another way to reduce the power consumption is to design power-aware transceivers. Most transceivers use up to tens to hundreds of milliwatts of power when turned on. They cannot be integrated in small sensors even when duty cycling is performed. This implies that several components which consume more power have to be removed from the circuit architecture. Research has shown that one of the most power hungry components of transceivers is the phase-locked loop (PLL) synthesizer, which is required for start-up of the radio and power amplifiers, and needed for transmission of data. The PLL needs time to lock to the desired frequency before the data can be demodulated (for a receiver) or modulated (for a transmitter). Within this start-up time, the radio consumes significant amounts of power relative to the power dissipated during the active mode. For example, in [9], 38% of the active power is consumed during start-up time. When transmitting data, power amplifiers also require much energy. Transceivers based on architectures that can do without these components should be employed for a reduction in power on the order of a few mWs to less than 1mW.
Within the physical layer, power consumption is also dependent on the data bit rate required for the application and the modulation scheme chosen. Consequently, by selecting a certain data rate and modulation scheme, power optimization can be achieved as well.

Common modulation schemes implemented to limit power dissipation need to be of the simplest kind, such as: On/off keying (OOK), frequency shift keying (FSK), and M-ary modulation abound in literature [3, 9, 10]. Moving towards higher data rates, such as 5 to 10 Mbps can be used to reduce the energy per bit, which is the energy consumed by the sensor node in order to transmit or receive one bit of data [11]. These issues are discussed in chapter 2 of this work.

1.3 Design objectives and approaches

The above solutions to the WSN radio design address the power consumption problem on different levels. This goal is better accomplished if a combination of the aforementioned approaches is implemented. A radio which employs duty cycling, a simple architecture, and a simple modulation scheme can ensure low power consumption. This is the direction that this work will also follow.

However, architectural simplification is the subject of this work. Choosing a low power architecture together with reducing the number of RF blocks can cut power consumption in order to achieve less than or about a mW. The traditional blocks in frequency translation architectures are reduced by selecting a different strategy for downconversion, employing frequency demodulators. Nonetheless, using frequency demodulators at 24 GHz with limited power requirements is a challenging task. Therefore, the aim of this work is to investigate whether it is possible to use frequency demodulators for downconversion at a relatively high frequency in a low power CMOS technology (with its inherent limitations). Thus, several trade-offs between power consumption, gain, linearity, and noise which are usually investigated are not emphasized in this work. Aspects such as gain and current consumption are focused upon.

In summary, this work considers the design of a 24 GHz receiver front-end employing a frequency discriminator as the downconversion block, using an FSK modulation scheme for a data rate of 5 Mbps.

1.4 Thesis Outline

Chapter 2 will present a qualitative overview of the state of the art receivers within the WSN context as well as frequency detectors. A discussion on architecture, modulation scheme, and data rate is held and a selection for each is made.

Chapter 3 provides the theoretical background, design and simulation results of the 24 GHz receiver consisting of an LNA, mixer, and phase shifter.

Chapter 4 provides information about the physical layout of the receiver test chip, post layout simulations and includes a discussion of the changes made to the receiver due to layout considerations.

Chapter 5 provides measurement results of the tested receiver and discusses what testing setup has been provided.

Finally, Chapter 6 presents a summary of what has been achieved in this thesis and presents insights for future work.

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Chapter 2. Low Power Architectures and FM Detectors

The issues regarding the physical layer optimization highlighted in the previous chapter are further discussed in this chapter. First, trade-offs between different modulation schemes and data rates are presented. Second, several state of the art receivers are presented and their architectures highlighted. Third, a discussion on frequency detectors is held and the role within the present work is displayed. Fourth, a link budget is derived presenting the system requirements. Finally, the chosen architecture, demodulator, data rate, and modulation scheme are discussed.

2.1 Modulation Schemes

As mentioned in the previous chapter, the choice of modulation scheme impacts the power performance of the receiver. The modulation directly influences the kind of receiver architecture that can be employed. For low power consumption, only the simplest architectures should be used. Therefore, higher level modulation schemes which require complex modulation and demodulation circuitry, are not considered for implementation. Such modulation schemes are
M-ary Phase Shift Keying (M-PSK), M-ary Quadrature Amplitude Modulation (M-QAM), and M-ary Frequency Shift Keying (M-FSK). M-ary modulation reduces the transmit time of the radio since it sends multiple bits per symbol, but the lower energy is not attained since the architecture requires complex analog-to-digital converters [1, 2]. A comparison between M-ary and binary modulation schemes is given in [3].

Thus, binary modulation schemes are most energy efficient, since they allow for simple analog demodulation. For example, by utilizing a continuous phase modulation system such as the binary scheme, the VCO in the transmitter can be directly modulated, removing the I and Q mixers needed in M-ary schemes [1]. The modulation schemes that are reviewed are on/off keying (OOK) and frequency-shift keying (FSK).

With an OOK modulation, the transmitter is turned on only while sending data, digital 1, while for a digital 0, the transmitter is off. This saves half of the power consumption. On the other hand, the oscillator needs to settle in less than a bit's period, which might not be fast enough in comparison to the data rate employed [2]. Furthermore, OOK is known for having poor spectral inefficiency due to varying amplitudes in the carrier wave and for being very susceptible to interferers [4].

FSK is another simple modulation scheme which can be also used in direct downconversion architectures. As OOK, FSK has simple modulation and demodulation circuitry, being ideal for low power applications. Unlike OOK, the transceiver is turned on at all times-for sending both digital 1s and 0s. An advantage of FSK which provides a solution to the flicker noise problem in direct downconversion receivers is that, for a sufficiently high FSK tone frequency, the downconverted signal is away from DC [5]. Furthermore, FSK is less responsive to interferers as the sensitivity is diminished.

Fig. 2.1 shows the spectrum of the two modulation schemes examined above. OOK exhibits a single peak, implying that only one tone is available at a single time. FSK displays two tones at a single time as the frequency is shifted from one to another.

Due to the susceptibility to interferers, on-off keying is not selected for the receiver in this work. Instead, orthogonal FSK (OFSK) is the modulation scheme choice. OFSK has the advantage that the two keyed frequencies have no correlation: they are orthogonal to each other. Moreover, the bandwidth is higher, thus better discriminating between one tone and another.

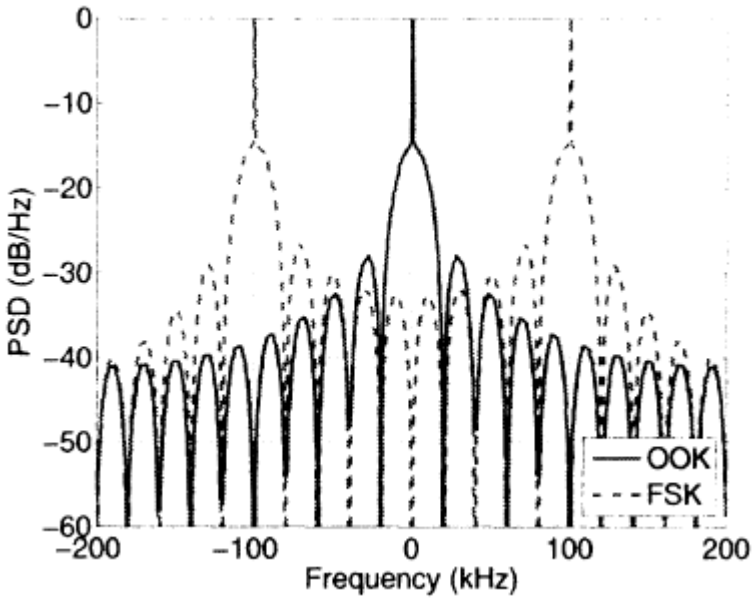


Fig.2. 1 Spectra of OOK and FSK [2]

2.2 Data Rate

Data rate selection is another issue that influences power consumption. Data rates used in WSN radios are predominantly in the order of tens to hundreds of kbps [8-12]. The common belief is that low data rate is associated with low power consumption. This statement also depends on the kind of transceiver architecture and RF blocks employed. Papers on low power radios report data rates below 1Mbps. However, energy per bit is a better metric for low power radios. Data rate evaluation can be interpreted within the total energy consumption of the radio node during active time. In [6], a model for calculating the total energy consumption of the radio node is given based on the start-up, receive and transmit times. A formula for calculating the energy per bit, *Eb/No*, is derived, as in Eq. 2-1. This energy is a WSN figure of merit, as it shows how much energy is required by the radio to transmit one bit.

$$E_{bit} = \frac{P_{LO} \cdot \left(t_{start} + t_{switch}\right)}{2 \cdot L_{pkt}} + \frac{1}{2 \cdot \eta} \cdot \gamma_{PA} \cdot d^{n} + \frac{P_{LO} + \frac{1}{2} \cdot P_{RX}}{r} \qquad (2\text{-}1)$$

Where P_{LO} is the power consumption of the synthesizer; t_{start}, the settling time; t_{switch}, the time between the receive and the transmit mode; L_{pkt}, the length of the packet; η, the power efficiency of the power amplifier; d, the transmission distance; γ_{PA}, the factor depending on

the transmit/receive antenna gains; r, the data rate; P_{RX}, the power consumption of the receiver.

Since the energy per bit is inversely proportional to the data rate, a higher data rate results in lower energy per bit. For the same transceiver architecture, the derivation in [6] concludes that using higher data rate leads to lower energy per bit. To reduce the transmit time, the data can be sent in high bursts during the active time of the transmitter.

2.3 The frequency band

The International Telecommunication Union issues free unlicensed bands for industrial, scientific, and medical (ISM) purposes. For the implementation of this receiver, the frequency of operation was chosen to be 24 GHz. It has a 250 MHz bandwidth, with a center frequency of 24.125 GHz. The choice of the ISM band also gives more degrees of freedom since the design does not need to adhere to any frequency, modulation, or data rate requirement specific to a certain standard. For example, the IEEE 802.15.4a standard created for the purpose of low cost low power applications, such as WSN, requires the use of BPSK or O-QPSK as modulation schemes. The data rates are limited to 20 kbit/s or 250 kbit/s, respectively, while the operation frequencies are constrained to 900MHz and 2.4GHz [7].

The choice of 24 GHz is both for research and practical reasons. Ever since the first working implementation concerning wireless sensor networks, the operation frequency has increased. The most successful projects were the “PicoRadio” from the UC Berkeley group which used a 100 kbit/s data rate at 1.9 GHz [8], the WiseNet transceivers which used less than 100 kbit/s data rate at frequencies less than 1 GHz [9], and a variety of other implementations at 2.4 GHz [10-12]. As shown in Fig 2.2, these low frequencies do not allow for higher data rate due to low bandwidth and SNR, independent of the modulation scheme employed. Furthermore, Fig.2.2 confirms that for higher frequencies, more capacity is available.

Another reason for moving up to the 24 GHz ISM band is the lack of interferers to corrupt the channel. At this frequency, signals can't penetrate through walls, thus reducing interference to a great extent. This is an advantage since, in comparison to the 2.4 GHz ISM band, there are significantly less interferers from other licensed bands such as WLAN and Bluetooth whose signals can go through walls.

The standard also allows for extra bandwidth. In the present system, OFSK modulation scheme is used. The extra bandwidth allows for a better signal detection. A higher channel bandwidth permits the two frequency tones in the spectrum to be farther away from each other making them easily recognizable than if they were closer to one another, as shown in Fig.2.1. The potential for an even higher data rate exists, as can be noted in Fig 2.2. One can see that for at 24 GHz, the potential data rate can be as high as 10 Mbit/s for a propagation range of 25 m. Furthermore, higher bandwidth allows more transmission of data, which can reduce the energy per bit, which is a key aspect for low power consumption.

From a circuit design point of view, the 24 GHz frequency band facilitates the miniaturization of circuit components. Passive components, such as on-chip microstrip inductors, are greatly reduced in value and thus in size. The antennas used in transceiver designs at this frequency are also diminished in size since the wavelength at 24 GHz is small-0.0125m.

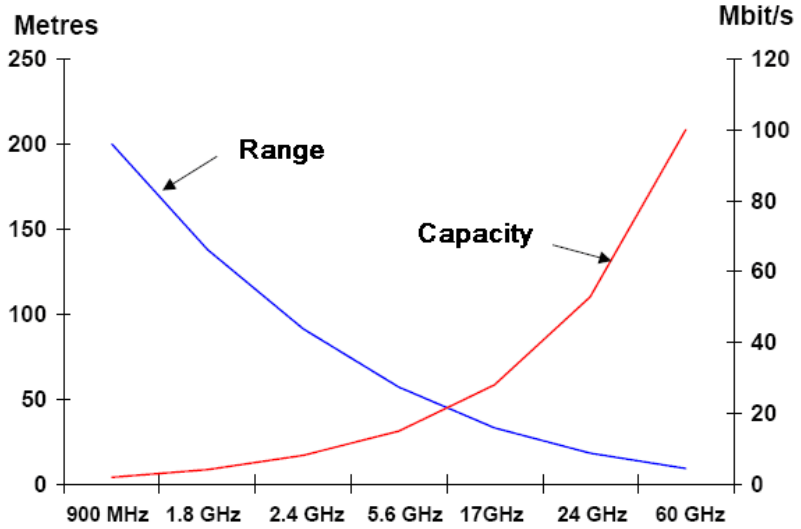


Fig.2. 2 Range vs. channel capacity of WLAN technology

2.4 Architecture review

The most significant power reduction can be achieved at the transceiver architecture level. As mentioned in Chapter 1, the architecture should not have power hungry components such as a frequency synthesizers, complicated modulation and demodulation circuits or even power amplifiers. The simplest kind of architectures should be aimed for. The following discussion reviews what possible architectures are wise to be employed for the application of WSNs.

2.4.1 Direct conversion Architecture

The homodyne architecture, shown in Fig.2.3, is also known as a direct conversion or zero IF. The receiver consists of a band select filter followed by a low noise amplifier (LNA) as in the classical heterodyne receiver. Since the intermediate frequency is set to zero, it allows image rejection by signal cancellation in two parallel-operating channels I and Q. The channel select filter is implemented via low pass filters which allow for easy tuning. Also, this is an easily integrated low cost solution in comparison to the bulky heterodyne receiver. The low number of chip components allows for flexibility and for integration possibility which ultimately saves power and chip area.

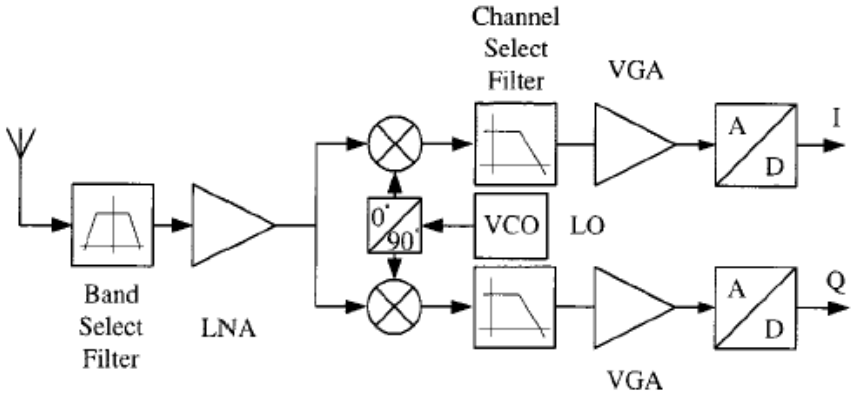


Fig.2. 3 Typical homodyne/zero-IF receiver [13]

Some weaknesses are observed in this architecture. Since the downconverted signal extends to DC, offset voltages might corrupt the signal. Another issue is the mismatch of the in-

phase/quadrature phase of the signal, which might alter the constellation diagram of the baseband signal. Flicker noise also constitutes a problem if CMOS is used for implementation. [13] Nevertheless, proper solutions have addressed these problems proving this architecture a viable candidate for many applications. Furthermore, many modulation schemes and data rates are applicable to this architecture.

An example for this architecture is the implementation in [14]. A direct conversion receiver is designed for the 802.15.4 standard developed especially for low power, low cost and low rate applications such as WSN. The receiver operates at 2.4GHz, and is applicable for binary phase- shift keying (BPSK), Offset quadrature phase-shift keying (O-QPSK) and parallel sequence spread spectrum (PSSS) modulation types. The LNA is designed using the inductive degeneration cascode amplifier with an extra gate source capacitor. The passive mixer converts the RF directly to baseband, dissipating no DC current. With the main focus on low power and low noise figure, the receiver achieves a NF of 3 dB, a 30 dB conversion gain, an IIP3 of -5 dBm and an IIP2 of 45 dBm. It consumes 2 mA from a 1.8 V power supply.

2.4.2 Low-IF Architecture

Another architecture used in receivers is the low-IF, showed in Fig.2.4. It combines the advantages offered by the heterodyne and homodyne receivers. Here, the intermediate frequency is not zero, but one or two times the channel bandwidth. There are several advantages for choosing a low intermediate frequency rather than zero. The final downconversion is performed in the baseband circuitry. Due to the digital implementation, the image reject downconversion is done without mismatch in the I/Q components of the signal, a problem that occurred in the direct conversion receiver. Since the IF is on the order of MHz, also the requirements for the ADC are lowered. Another advantage over the zero-IF receiver is that DC offsets are no longer significant since the digital image reject down conversion is not sensitive to self-mixing or signal leakage. However, there is a disadvantage to this architecture: the resulting image signal can be stronger than the wanted signal. To keep up with the high linearity requirements, the ADC must then sample both the

wanted and the image signal. Along with this problem, in terms of power consumption, the number of components is higher [13].

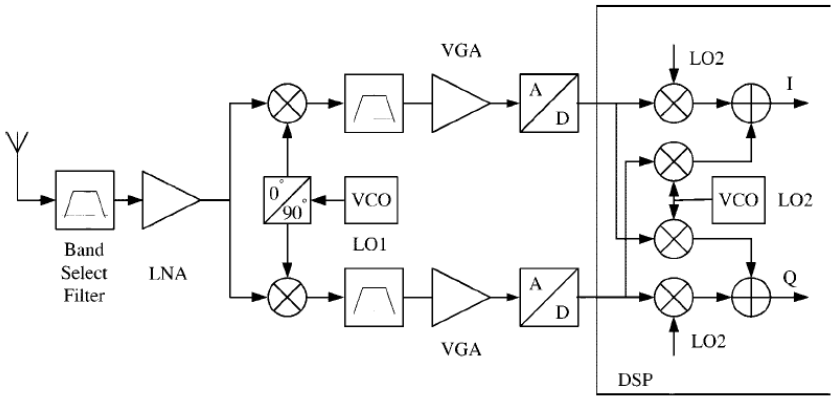


Fig.2. 4Typical low-IF receiver [13]

An example for this architecture is the low IF transceiver given in [11]. It achieves very low power consumption, 2.5 mA in the maximum mode, from a 400 mV power supply operating at 2.4 GHz. It sacrifices image rejection in exchange for halving the power. The typical LNA is eliminated and the RF signal is directly fed to the I/Q passive mixers, which consume zero DC current. The highest power is dissipated by the VCO which produces both in-phase and quadrature outputs to drive the mixers with a high LO amplitude. In the maximum mode, the receiver achieves a noise figure of 11.8 dB, and an IIP3 of -7.5 dBm. The transmitter uses a PA with 44% efficiency, while the VCO has a phase noise of -106 dBc/Hz at 1 MHz offset.

2.4.3 Super-Regenerative Architecture

The third reviewed architecture is the super regenerative, shown in Fig. 2.5. It consists of an LNA, followed by an oscillator which is stopped periodically with a quenching signal. The oscillator is held near oscillation, which, in this mode, provides very high gain. By quenching the oscillator, the presence of RF signals can be distinguished. The result is fed to an envelope detector which demodulates the RF. This very simple architecture is mostly suited for low power and low cost applications such as WSN. An advantage is that a simple modulation scheme such as OOK or FSK can be employed as well. A big disadvantage to this architecture is that due to its high sensitivity (even -100 dBm) it is prone to interferers.

Also the oscillator might suffer from slow settling behavior which hinders high data rates to be used [5].

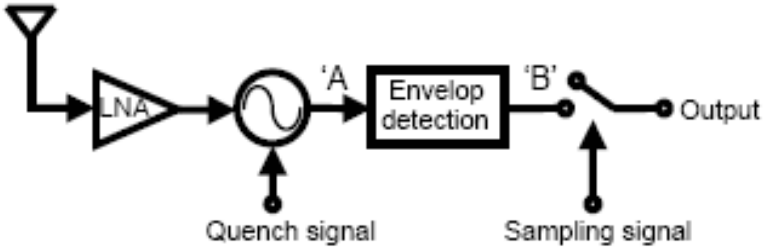


Fig.2. 5Typical Super regenerative receiver [5]

An example for this architecture is the transceiver in [15]. BAW resonators are used to reduce power consumption. The receiver consists of an isolation amplifier which converts the RF power to current and injects it to the detector oscillator. This further samples the RF input as the start-up condition for its oscillation, modifying the start-up envelope. The signal is sampled directly at RF, providing a large gain of over 55 dB. The envelope of the oscillation is detected by a nonlinear filter, while finally an OOK analog signal is formed. The receiver consumes a total of 400 μA from a 1 V power supply and operates at 1.9 GHz. It achieves a sensitivity of -100.5 dBm. The efficiency of the low power amplifier in the transmitter is 27.5% while delivering 380 μW.

Based on the wireless sensor network application, a receiver architecture is selected which is compatible with low power consumption, minimal number of RF blocks, and suitable modulation scheme. Even though all the architectures can achieve minimum power consumption as described in the references given, a different conversion architecture is chosen for the possibility of its simple implementation. The low-IF architecture is rejected due to the abundance of power-hungry components. Double downconversion can be accepted with a higher power consumption but not with 1 mA. Super regeneration is also affordable, but the sensitivity to interferers is too high to be finally considered.

2.5 Frequency Detectors

Frequency detectors are reviewed in this section in order to provide an alternative to standard frequency translation approaches and to provide a possible way to avoid the power hungry RF blocks that compose the architectures.

Frequency detectors are devices that recover the information content of a modulated wave. To receive FM signals, the receiver is made sensitive for frequency variations and insensitive to amplitude modulations. The response of such a frequency detector is a linear voltage to frequency characteristic.

Throughout the history of FM modulation and demodulation techniques, different classes of FM demodulators have been encountered. Early demodulators were based on slope detection which combined AM and FM detection. Later demodulators focused only on FM detectors which offered higher linearity and lower noise level.

The detectors reviewed in this section are the quadricorrelator, the Foster-Seeley discriminator and the quadrature detector. Their performance is analyzed and compared in the following sections.

2.5.1 The Quadricorrelator

The quadricorrelator, first presented by Sheaffer in 1942, provides frequency discrimination without being dependent on tuned circuits [16]. The quadricorrelator in itself is a frequency difference detector. Fig.2.6 shows the architecture of this FM detector. It consists of two mixers which convert the input passband signal into the I and Q components by multiplying them with an LO. The LO was first provided by a crystal oscillator which had a very stable frequency, as well as a stable voltage at the output of the discriminator. Thereafter, the difference terms resulting from the mixer multiplication pass through the low pass filters (LPF). The output of one of the LPF is differentiated, providing a 90^{o} phase shift, while the other is left as is. Further on, the differentiated signal and the remaining signal are multiplied once more. The result is a DC component proportional to the frequency difference and a ripple component at twice the operation frequency. The DC component is used for FM demodulation, while the ripple component should be limited. An advantage of

this system is that the differentiator can be a high pass filter, a low pass filter, or a delay line, since the way the phase shift occurs is intrinsic to the functioning of the quadricorrelator. Also, since the phase shift is not provided by any tuned circuit, the system is very stable to temperature or process variation. Many improvements have been made to the original circuit. One version is the balanced quadricorrelator which cancels the mentioned ripple by adding another differentiator unit in the other circuit branch, and two more multipliers for cross multiplication with the low pass filtered signal [17].

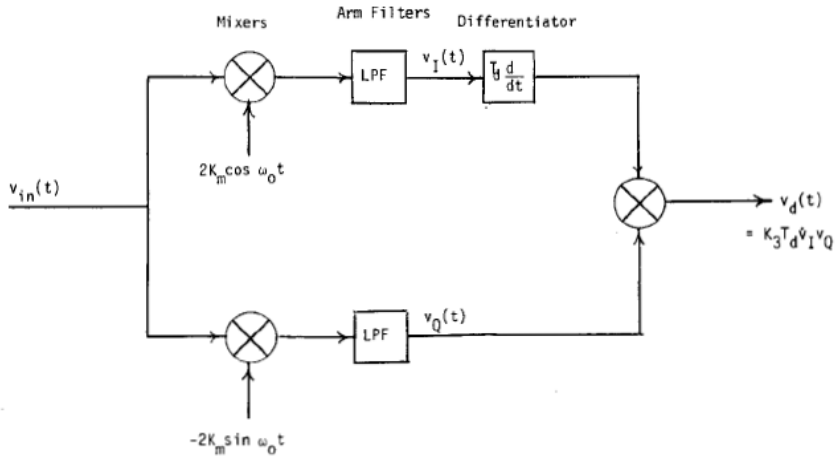


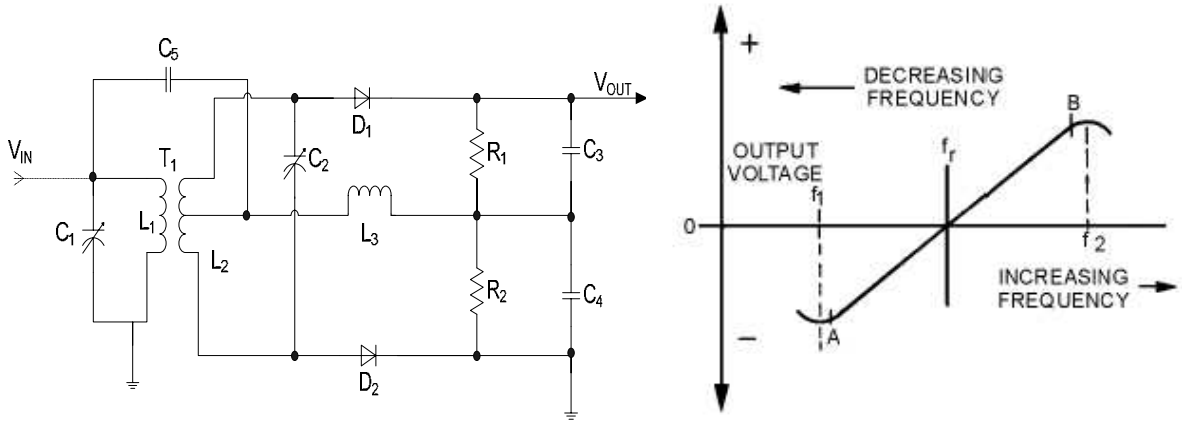
Fig.2. 6 Quadricorrelator architecture [17]

A disadvantage of this detector is the number of components required for demodulation. Even though the balanced version presents more advantages in terms of cancelling the ripple and providing acceptable noise levels, it requires additional circuit blocks, which increase power consumption.

2.5.2 Foster-Seeley Discriminator

Another very popular frequency detector was presented by Foster and Seeley in 1937 [18]. Fig. 2.7a shows a schematic implementation of the detector. At first, the Foster Seeley discriminator is similar to the slope detector, since it consists of two LC tanks tuned slightly below or above the center frequency. The detector is composed of a double tuned transformer in which the primary and secondary turns are tuned to the carrier frequency [19]. These convert frequency variations to amplitude variations, which are then rectified using a full wave DC rectifier and filtered to provide a DC output voltage. The output

varies in amplitude and polarity as the input varies in frequency, as shown in Fig.2.7b. For example, when the input frequency equals the carrier frequency, the output voltage is equal in amplitude but opposite in polarity; therefore it cancels out to 0. When the input frequency is higher than the center frequency the output voltage increases in the positive direction. In this case, the tank circuit acts more like an inductor, allowing more voltage on the upper branch and more voltage drop across resistor R_1.When the input frequency is lower than the center frequency, the opposite happens and the output voltage increases in the negative direction.



(a) **(b)**

Fig.2. 7a) Schematic implementation of Foster- Seeley detector; b) Frequency characteristic of the detector [19]

The main disadvantage of the Foster-Seeley detector is the sensitivity to amplitude variations in the carrier signal, which appear at the detector output [19]. Moreover, a monolithic integrated circuit version is greatly hindered by the presence of the area consuming transformer.

2.5.3. Quadrature detector

The final FM detector presented in this review is the quadrature detector. Bilotti presented a new detector based on an analog multiplier [20]. The multiplier can be used for different applications including an FM detector. Fig. 2.8 shows a schematic implementation of the discriminator. The input to the quadrature detector is split in two signals of which one is fed to a tuned circuit and another to the input of a phase detector. The tuned circuit is

composed of a high reactance capacitor, which shifts the signal by 90º, and an LC tank which is resonant at the carrier frequency. In the original paper, the phase detector was an analog multiplier, which in later versions was replaced by a mixer. The mixer takes the two quadrature signals and multiplies them, producing an output proportional to the phase difference between them. The result of the multiplication is afterwards low pass filtered. In the case of an unmodulated signal, the downconverted result is an average of 0. For the case of a modulated FM signal, the total phase difference will be the sum of 90º plus the negative or positive phase change due to frequency deviation from the LC tank resonant frequency. If the frequency deviation is more positive, the voltage output increases; for the more negative deviation, the voltage output decreases. [20]

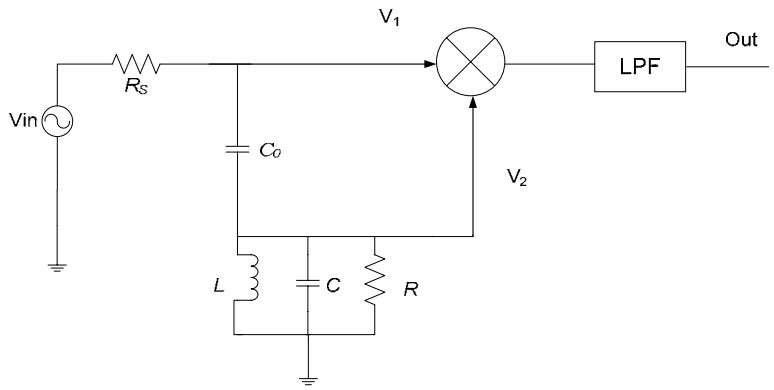


Fig.2. 8 Schematic implementation of the quadrature detector

The quadrature detector is more appropriate for IC integration, unlike the other detectors presented in this review. However, since it consists of a tuned circuit, the detector is liable to process and temperature variations. Nevertheless, its simplicity is appropriate for the WSN application.

2.6 Final choices

Upon reviewing architectures most applicable to low power applications and several FM demodulators, a decision can be made as to what implementation is best in terms of the WSN requirements. The choice for the direct conversion architecture has already been made in the previous section. To reduce the power consumption and to provide a simple way to detect the OFSK signals, FM demodulators have been examined. While the

quadricorrelator and Foster Seeley detector equally present advantages in terms of performance, the quadrature detector is the only one that provides both reduced levels of power consumption and simplicity for IC integration. The implemented receiver uses the chosen demodulator and integrates it into the direct conversion architecture. As shown in Fig.2.9, the designed front end consists of an LNA, the FM demodulator and an IF amplifier.

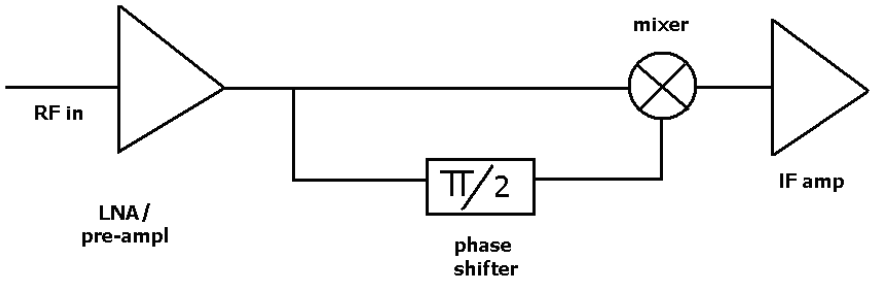


Fig.2. 9 Receiver architecture

2.7 System requirements and possible link budget

The most important performance characteristics for a receiver are its sensitivity and dynamic range. The receiver sensitivity is found by calculating the noise floor and the signal to noise ratio- SNR. This is given by Eq. 2.2 [21]:

$$SNR = \frac{E_B}{N_0} \cdot \frac{R}{B} \qquad (2\text{-}2)$$

where E_B/N_0 is the energy per bit to noise power spectral density ratio, R is the system data rate and B is the system bandwidth. Additionally, E_B/N_0 depends on the modulation scheme and the desired system BER. Assuming bit error rate is 10^{-3} and the modulation scheme is OFSK for a coherent detector, according to Fig. 2.10, the energy per bit to noise power spectral density ratio is 9 dB or 8 in magnitude. If the data rate is 5 Mbps and the system bandwidth 10 MHz, in view of Eq. 2-2, the SNR is 4 or 6 dB. An additional 2 dB margin is taken for extra losses.

The receiver sensitivity can be calculated by adding the SNR to the noise floor. The noise floor is found from Eq. 2-3 [21]:

$$Noisefloor = k_B T\Delta f = 1.38 \cdot 10^{-23} \, {}^{J}\!/_{K} \cdot \Delta f \qquad (2\text{-}3)$$

$$= -174dBm + 10\log(\Delta f)$$

where Δf is the bandwidth of the desired signal, indicated by approximately twice the chosen data rate. Therefore, the noise floor is -104dBm.

Receiver sensitivity without the addition of Noise Figure (NF) is given in Eq. 2-4:

$$P_r = Noisefloor + SNR = -104dBm + 8dB = -96dBm \qquad (2\text{-}4)$$

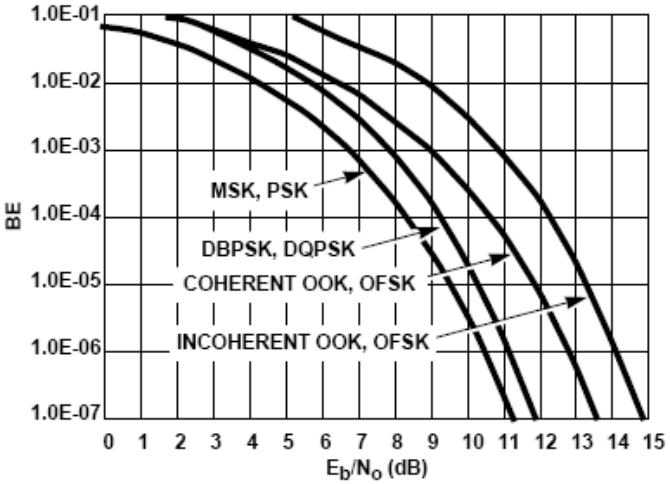


Fig.2. 10 Probability of bit error for common modulation schemes [21]

Additionally, the minimum detectable signal is:

$$MDS = Noisefloor + SNR + NF \qquad (2\text{-}5)$$

The transmit power equals [21]:

$$P_T = MDS - G_{TX} - G_{TR} + L_{fs} + Fade\ Margin \qquad (2\text{-}6)$$

where G_{TX} and G_{RX} are the transmit antenna gain and receive antenna gain, respectively and L_{fs} the propagation loss. The fade margin represents the extra power the transmitter has to radiate to overcome the multipath interference. The fade margin is usually taken as 20 to 30 dB depending on link reliability. The antenna transmit and receive gain is taken as 5 dBi since patch antennas which provide high gain at these frequencies can be used. The λ/4 patch antennas are furthermore small in size-3mm*3mm- since the wavelength at 24 GHz is only 0.0125 m. The propagation loss is determined by Eq. 2-7 [21]:

$$L_{fs} = 20 \cdot \log\left(\frac{4 \cdot \pi \cdot d}{\lambda}\right) \qquad (2\text{-}7)$$

where d is the distance between receiver and transmitter and λ is the wavelength. Given the wavelength of 0.0125 m and the distance between the sensor nodes is 1 m, L_{fs} is 60 dB. The transmitter specification for the transmit power is -10 dBm.

In view of Eq. 2-6:

$$MDS = P_T - Fade\ Margin - L_{fs} + G_{TX} + G_{RX} = -20-60-10+10 = -80\ dB.$$

From Eq. 2-5, the Noise Figure is estimated to be:

$$NF = MDS - Noisefloor - SNR = -80+96 = 16\ dB$$

The receiver sensitivity is given then by:

$$P_r = Noisefloor + SNR + NF + FM = -104+8+16+20 = -60\ dB$$

Although the previous derivation regarding receiver sensitivity leads to a usual result, it is expected that the input power is too small. This is due to the inherent functioning of the FM demodulator and the restricted 1 mA current consumption. As explained in section 2.5.3, the signal swing at the detector input determines the value of the downconverted signal. The signal swing is limited by the gain of the LNA prior to the detector, which in turn is limited by the current restriction. This is imposed as a figure of merit for the front-end design to examine whether the goal of this work can be accomplished. Also, linearity calculations for the link budget are not performed since the receiver inputs are small amplitude signals, posing limited distortion problems. Intermodulation distortion is not calculated since limited interferers are present for the frequency band: the ones from other sensor nodes. For these interferers, IIP3 can be sufficiently low to accommodate them. [22]

Table 2. 1 Receiver specifications

RF frequency	24 GHz
RF bandwidth	250 MHz
RF input impedance	50 Ω
Receiver sensitivity	<-60 dBm
NF	<16 dB
Data rate	5 Mbps
Transmit power	-10 dBm
Data link	<1 m
Current consumption	<1 mA
Supply voltage	1.2 V

2.8 Conclusions

This chapter reviewed the receiver architectures that lend themselves to the application of wireless sensor networks. A set of FM detectors as an alternative to the high power consuming RF downconversion blocks was also examined. Ideas with regard to limiting power dissipation such as choosing simple modulation schemes and a high data rate were also investigated. The next chapter presents the design strategy of the receiver based on the chosen architecture and FM detector. Two receiver implementations are presented from which one is selected for tape out.

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Chapter 3. 24 GHz WSN Front End design

This chapter presents the theory, design and simulation results of the front end. The concept behind the design is initially presented. Afterwards, the receiver is presented, discussing specifications and drawbacks. The individual RF blocks are presented and discussed in terms of the receiver specifications obtained in the last section of the previous chapter.

3.1 Possible challenges

Decreasing power consumption and simplifying the architecture, regarded as design goals in Chapter 1, face some considerable challenges. Firstly, the 1 mA current consumption greatly restricts the kind of architecture, as discussed in Chapter 2. Secondly, at an operation frequency of 24 GHz, each circuit component has added parasitic behavior.

The low current constraint limits the amount of current distributed among the different blocks of the receiver. Therefore, for a feasible implementation, the number of RF blocks used should be minimized. The current consumption also limits the voltage gain achieved by transistors. As mentioned in the last section of chapter 2, gain is a key parameter in the front-end design, since it determines the signal amplitude at the mixer input. Therefore, it is important to keep this as high as possible.

Due to the high frequency operation, parasitic behavior of components have major influence on the overall circuit performance, such as decreasing the gain and providing an extra path by which the RF signal is lost. Furthermore, the high frequency selection also implies that for any small changes in component values, the entire AC behavior changes. Therefore, these changes must be properly taken into consideration.

Another effect of high frequency operation is that more current is needed for a specified gain. At low frequencies, high gain amplifiers are easily designed, but for high gain, more current is needed to obtain the same.

3.2 Detection Concept and System Design

In this section, the quadrature detector is examined in terms of performance. The detector produces a maximum output when two 90º phase shifted signals are multiplied by the mixer. The output is proportional to the frequency shift from the central frequency. The detection concept is outlined in the block diagram of Fig. 3.1.

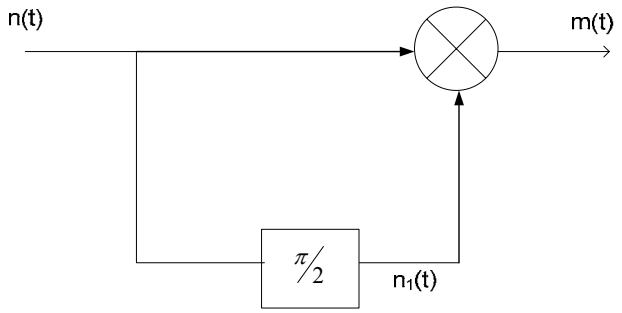


Fig.3. 1 Block diagram

Signal n(t) and $n_1(t)$ are multiplied by the mixer to result in the output signal m(t). The two input signals can be described according to (3-1) and (3-2):

$$n(t) = A \cdot \sin\left(\omega \cdot t + \frac{\Delta f}{f_1} \cdot \sin(\omega_1 \cdot t) \right) \tag{3-1}$$

$$n_1(t) = A \cdot \sin\left(\omega \cdot t + \frac{\Delta f}{f_1} \cdot \sin(\omega_1 \cdot t) + \phi \right) \tag{3-2}$$

where A is the input signal amplitude, ω is the operating frequency, $\Delta f / f_1$ is the frequency deviation from the carrier frequency, and ϕ is the phase shift. This signal representation is a particular form of FM modulated signals. The standard FM modulated signal is described by:

$$s(t) = A \cdot \left[2\pi \cdot f_c \cdot t + 2\pi \cdot k_f \cdot \int_0^t m(\tau) d\tau \right] \tag{3-3}$$

where k_f represents the frequency sensitivity of the modulator and *m(t)* represents the message signal.

Multiplying the two signals lead to the following:

$$m(t) = n(t) \cdot n_1(t) = A^2 \cdot \sin\left(\omega \cdot t + \frac{\Delta f}{f_1} \cdot \sin(\omega_1 \cdot t) \right) \cdot \sin\left(\omega \cdot t + \frac{\Delta f}{f_1} \cdot \sin(\omega_1 \cdot t) + \varphi \right)$$

$$= \frac{A^2}{2} \cdot \left(\cos\phi - \cos\left(2 \cdot \omega \cdot t + 2 \cdot \frac{\Delta f}{f_1} + \varphi \right) \right) \tag{3-4}$$

When φ is a linear function of the input signal n(t), then: $\varphi = -\frac{\pi}{2} + \alpha \cdot x(t)$ (3-5)

where α is a proportionality factor.

After low pass filtering, the output signal *m(t)* becomes:

$$LPF(m(t)) = \frac{\mathrm{A}^2}{2} \cdot \cos\phi = \frac{\mathrm{A}^2}{2} \cdot \cos\left(-\frac{\pi}{2} + \alpha \cdot x(t) \right) = -\frac{\mathrm{A}^2}{2} \cdot \sin\left(\alpha \cdot x(t) \right) \tag{3-6}$$

Also, if $\left(\alpha \cdot n(t) \right) << 1$ then

$$LPF(m(t)) \approx -\frac{A^2}{2} \cdot \alpha \cdot x(t) \tag{3-7}$$

Once the low pass filtered output is determined, it is important to understand how to obtain the proportionality factor α. This is further investigated in the phase shifter. To obtain a phase shifting action, the filter circuit shown in Fig 3.2 is determined.

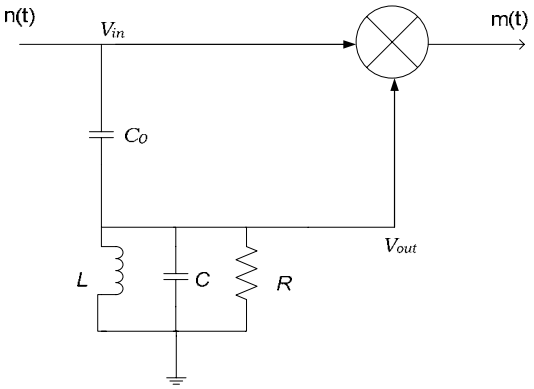


Fig.3. 2 System design with phase shifter diagram

The transfer function of such a system is described by:

$$\frac{V_{out}}{V_{in}} = \frac{C_0}{C + C_0} \cdot \frac{L \cdot \left(C + C_0 \right) \cdot s^2}{L \cdot \left(C + C_0 \right) \cdot s^2 + \frac{L}{R} \cdot s + 1} \tag{3-8}$$

Given that:

$$\omega_0 = \frac{1}{\sqrt{L \cdot (C + C_0)}} \tag{3-9}$$

$$Q = \frac{R}{L \cdot \omega_0} = R \cdot \sqrt{\frac{C + C_0}{L}} = R \cdot \left(C + C_0 \right) \cdot \omega_0 \tag{3-10}$$

The frequency response of the system is:

$$H(j\omega)=\left(-\frac{C_0}{C+C_0}\cdot\frac{\omega^2}{\omega_0^2}\right)\cdot\frac{1}{\left(1-\frac{\omega^2}{\omega_0^2}\right)+j\cdot\frac{\omega}{Q\cdot\omega_0}} \tag{3-11}$$

The phase of *H(jω)* can be found from:

$$\varphi=\arctan\left(\frac{-\frac{\omega}{Q\cdot\omega_0}}{1-\frac{\omega^2}{\omega_0^2}}\right) \tag{3-12}$$

When $\omega\approx\omega_0$, then $\varphi=-\frac{\pi}{2}$.

If one further denotes, $\varphi=-\frac{\pi}{2}+\alpha$, with $\alpha<<1$, then $\tan\alpha\approx\alpha$. (3-13)

Since $\alpha=\varphi+\frac{\pi}{2}$, then

$$\alpha=\tan\alpha=\frac{1-\frac{\omega^2}{\omega_0^2}}{\frac{\omega}{Q\cdot\omega_0}} \tag{3-14}$$

which leads to:

$$\alpha=\frac{Q\cdot(\omega_0-\omega)\cdot(\omega_0+\omega)}{\omega\cdot\omega_0} \tag{3-15}$$

When $\omega\approx\omega_0$,

$$\alpha=\frac{2\cdot Q(\omega_0-\omega)}{\omega_0} \tag{3-16}$$

Therefore,

$$\varphi=-\frac{\pi}{2}+\frac{2\cdot Q\cdot\Delta\omega}{\omega_0} \tag{3-17}$$

Inserting (3-16) into (3-7) leads to:

$$LPF(m(t))\approx-\frac{A^2}{2}\cdot\frac{2\cdot Q\cdot\Delta f}{f_0} \tag{3-18}$$

Equation (3-18) shows that the output is proportional to the frequency shift from the central frequency ω_0. This is the idea highlighted at the beginning of this section. One can also notice that the output will be proportional to the square of the signal amplitude and to the inductor quality factor. Therefore, a high inductor quality factor and a high voltage swing at the input of the mixer leads to a high voltage output.

An example of the presented concept now follows. The characteristic of the detector is determined by inputting signals at different frequencies, 200 MHz apart. The phase shifter is designed to provide a 90 degrees phase shift at 24 GHz. This leads to a maximum voltage output at this frequency. Signals at other frequencies will lead to a lower output. Fig.3.3 shows a typical detector system output characteristic. For signals with a frequency closer to the center frequency, the output voltage is higher, while farther apart frequency signals are rejected. As seen in Fig.3.3, over a bandwidth of 800 MHz, from 23.6 to 24.4 GHz, the FM detector can detect signals higher than 1.2 mV. Aside from this bandwidth the detector rejects the signals. This shows a high selectivity of the entire system.

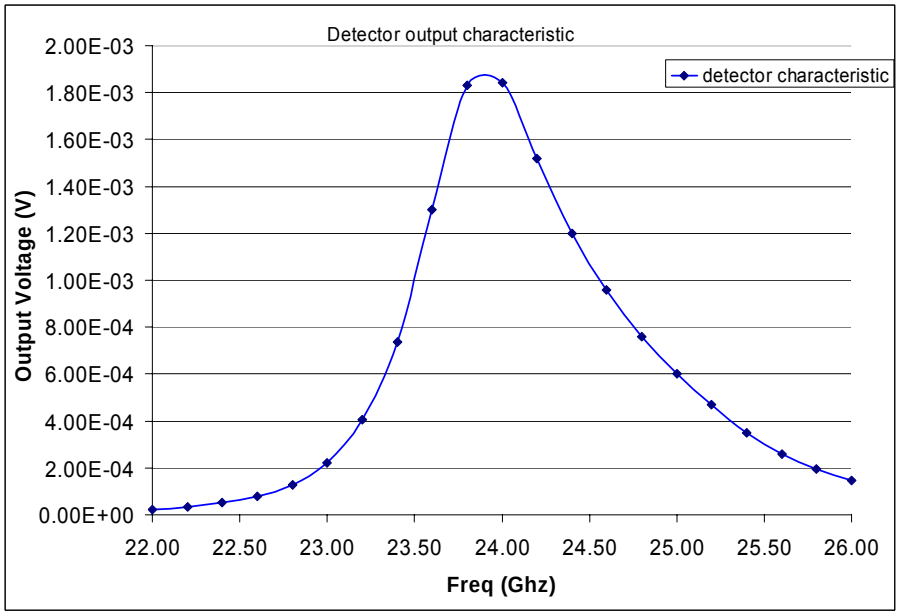


Fig.3. 3 Simulated system output characteristic

For the detector design, the aim is to achieve a DC output of 5 to 10mV, for an input level of -50dBm. Even though in Chapter 2 a derivation for the receiver sensitivity of -60 dBm

was made, the detector needs more input power to account for the relatively high signal swing to the mixer input.

3.3 Double stage receiver

This section presents the architecture of the implemented receiver. The system overview is shown in Fig 3.4. The first block consists of a cascoded low noise amplifier or preamplifier with a resonant tank. The signal is then fed to the phase shifter and to the dual gate mixer. Following downconversion, the signal is amplified by the IF amplifier which produces a digital signal. Each individual block will be discussed in the following sections providing a theoretical background and the simulations performed.

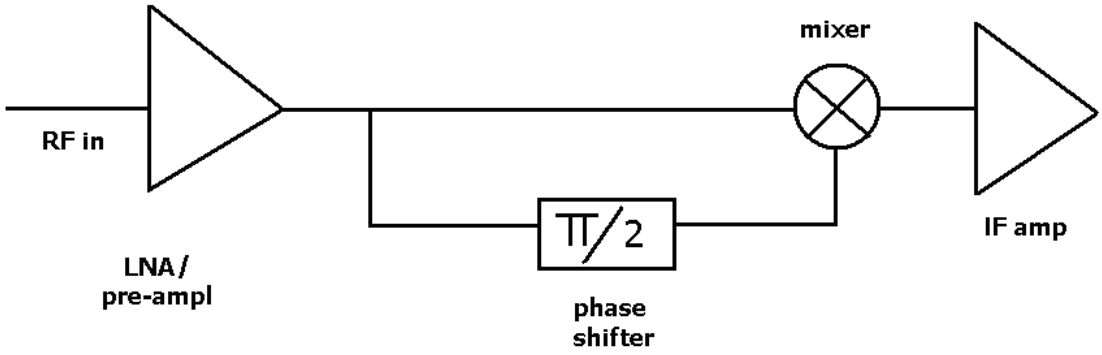


Fig.3. 4 System overview of double stage receiver

Unless otherwise specified, the simulations are performed at a more realistic temperature of 60ºC with a -50 dBm signal power.

3.3.1 Low Noise Amplifier Design

The low noise amplifier is the first circuit block the signal encounters coming from the antenna. Its function is to provide amplification in order to surpass the noise of the other receiver blocks while at the same time limiting the injection of its own noise. It must also sustain large signals with sufficient linearity, and provide a 50 Ω impedance match to the input source.

The most important requirements on the LNA's part are to provide conjugate matching, that is simultaneous noise and power match. Power matching is achieved by displaying the same impedance to the transistor's input as the one the source provides. In this way, it is ensured that the signal power is preserved without loss or reflections throughout the receiver blocks.

Noise matching, according to two port network theory, can be achieved when the noise figure is minimum. The noise figure is represented as [1]:

$$\mathrm{F}= 1+\left|\frac{v_A \cdot \left(Y_{cor}+Y_G\right)+i_u}{i_G}\right|^2 \tag{3-19}$$

$$i_A = Y_{cor} \cdot v_A + i_u \tag{3-20}$$

where v_A and i_A are the noise sources of the network represented by a noise correlation matrix, Y_{cor}; i_g is the generator noise current source; i_u is the uncorrelated noise current source and Y_G is the source admittance.

A further simplification of the equation, due to the fact that i_u and v_A are uncorrelated, leads to an expression for the noise figure in terms of impedances:

$$F = 1+\frac{R_u}{R_G}+\frac{G_n}{R_G}\cdot\left[\left(R_G+R_{cor}\right)^2+\left(X_G+X_{cor}\right)^2\right] \tag{3-21}$$

,where R_u is the uncorrelated noise resistance, G_n, the noise conductance, R_G, the generator resistor, R_{cor}, the correlation resistance, X_G, the generator reactance, and X_{cor}, the correlation reactance. From this expression, a minimum noise figure can be achieved when the derivative of F with respect to R_G, and X_G, is zero. This yields an optimum resistance for which noise is minimum: $R_{opt} = \sqrt{\frac{R_u}{G_n}+R_{cor}^{\ 2}}$

and an optimum reactance: X_{opt}= - $X_{cor.}$

More generally, the noise figure expression can be found under the following form in terms of the generator admittance [1]:

$$F = F_{\min}+\frac{R_n}{G_g}\left[\left(G_{opt}-G_g\right)^2+\left(B_{opt}-B_g\right)^2\right] \tag{3-22}$$

where Y_{opt} is the optimum admittance noise match; Y_G, the generator admittance; F_{min}, the minimum noise figure when Y_{opt} equals Y_G; and R_n, the noise resistance which gives the sensitivity of the noise figure F to the source admittance.

It is well known that a noise match does not imply also an impedance match, therefore, a conjugate match is harder to obtain. For narrowband applications, conjugate matching is achieved by the inductive degenerative technique [2]. This technique has been quite popular in many LNA designs [3, 4].

Nevertheless, for wideband matching, it is not that useful. For the purpose of wideband input matching, the inductive degeneration is not employed in this work. A solution capable of spreading the input reflection coefficient over a wider frequency range, and also providing decent noise figure is aimed for. As mentioned in section 3.1, in this work, the LNA is meant to provide enough signal swing for the mixer to produce a good downconverted output voltage. Achieving a good noise figure is not a goal in this design. Primarily, voltage gain, wideband input matching, and limiting current consumption are emphasized as design goals.

3.3.1.1 LNA topologies

As mentioned in the previous section, the inductive degeneration technique which employs a common source amplifier and connects an inductor to both the gate and source, will not be used because of its narrowband application.

For a wideband application, several implementations were investigated. Wideband input matching has been achieved in [3] by employing a matching network consisting of an input LC ladder network which provides a larger tuning range. A transformer based matching network also has been implemented in [6], which achieves a conjugate match over the UWB range.

Wideband matching is desired in this receiver due to potential mismatch in the inductors from the resonant tank and from the input impedance matching network. Due to process variation in TSMC technology, the impedance matching inductors required for tuning away C_{GS} of the input transistor might produce an input reflection coefficient, S_{11}, shifted at a different frequency than was designed for. This will render operation at the LC tank design frequency useless. For a wideband match, this problem is not encountered since the

reflection coefficient is designed to be lower than -10dB for a 7% variation of the operation frequency.

When considering LNA topologies, generally two transistor configurations are used to aim for the conjugate match: the common source (CS) and the common gate (CG) stage. These are shown in Fig.3.5.

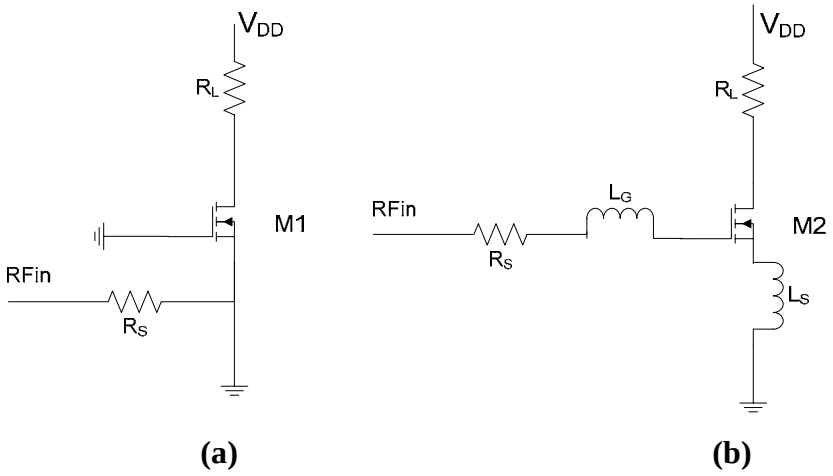


Fig.3. 5 LNA topologies: common gate (a) and common source with inductive degeneration (b)

The advantage of the CG LNA is that it provides an input impedance of 1/gm for a wide range of frequencies. Furthermore, it is less sensitive to parasitic effects and process or voltage variations. This is due to the fact that the matching network for this amplifier is a parallel resonant network attaining lower Q. Also, it performs better in terms of reverse isolation and stability in comparison to the CS LNA [7].

On the other hand, achievable noise figures with this topology are higher than with the common source stage, defined as:

$$F\min = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{w_0}{w_T}\right)^2 \qquad (3\text{-}23)$$

where γ is the channel thermal noise coefficient which increases to a value of 1-2 for short channel devices, while $\alpha = \frac{g_m}{g_{d0}}$ with g_{d0} being the drain source conductance at $V_{DS}=0$, and $\delta=2\gamma$. This equation does not include the gate current noise effect, even though it has been shown in [8] that this contribution is minimal in CG stages. The behavior of the noise figure at high frequencies is superior to the common source stage since the dependence on

the frequency ratio, ω_0 / ω_T is very weak, making it only dependent on bias dependent variables.

Nevertheless, the common source stage delivers higher gain and a lower overall noise figure. This occurs when the inductive degeneration technique is used. In a CS stage, the matching network is a series resonant network exhibiting a higher Q than in the parallel case of the CG stage. The common source stage is preferred because of its intrinsic gain delivered by the higher transconductance, defined as:

$$G_M = \frac{1}{2R_S} \cdot \frac{\omega_T}{\omega_0} \tag{3-24}$$

The frequency ratio factor induces a higher gain than in the CG stage.

Furthermore, the series resonant network also allows to find an optimum quality factor at which the noise figure is minimum [7].

The derivation of the optimum Q is significant since an expression of the noise figure is obtained:

$$F = F\min + \left[\frac{\gamma}{\alpha \cdot g_m \cdot R_S}\right]\left[1 - \frac{Q_{opt}}{Q_S}\right]^2 \tag{3-25}$$

where Qs= $\frac{1}{\omega_0 \cdot R_S \cdot C_{GS}}$ and Qopt= $\alpha \cdot \sqrt{\frac{\delta}{5\gamma} \cdot \left(1 - |c|^2\right)}$

where c is a correlation factor between the current noise sources.

For the inductive degeneration technique, the noise figure (NF) is lower at lower frequencies, but it degrades at higher frequencies, since the NF is dependent on the frequency ratio factor, ω_0 / ω_T .

The last issue of discussion within the CS stage is its reverse isolation. By itself, the C_{GD} feedback path is present and the CS LNA is prone to oscillation. To combat this, a cascode transistor is employed which practically nullifies the Miller effect. Nevertheless, the cascode does add noise to the whole LNA.

In comparison, even though the CG has more strong points, the CS stage provides advantages in the most important points within LNA design: gain and low noise figure.

Therefore, even though the inductive degeneration technique will not be used, the common source stage will be employed in this work.

3.3.1.2 Input Impedance Design

The LNA topology used in this design is a common source stage with a cascoded transistor. The input matching network is achieved by using two inductors which establish a voltage ratio to provide a higher voltage at the gate of the LNA, emulating the optimum Q behavior identified in the last section. Fig.3.6 shows the schematic of the small signal circuit of the LNA.

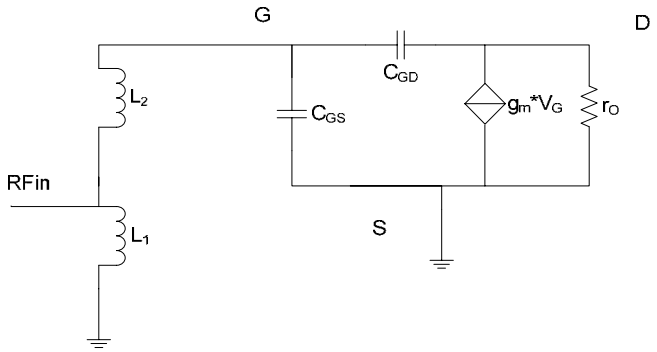


Fig.3. 6 Small signal circuit of designed LNA

The input impedance of this stage is defined as:

$$Zin = \frac{1}{s \cdot C_{GS}} + s(L_1 + L_2) \qquad (3\text{-}26)$$

Since this is purely imaginary, we can already define a requirement for the input impedance match such as $Im(Z_{in})=0$. Equation (3-26) then becomes:

$$\omega^2 \cdot (L_1 + L_2) \cdot C_{GS} = 1 \qquad (3\text{-}27)$$

The relation by which the real part of the input impedance can be set to 50 Ohm, is obtained by selecting the ratio of the inductors to provide the impedance transformation.
First, the input impedance of the transistor, *Zin*, is found. Thereafter, the ratio is found by using the following:

$$\frac{L_2}{L_1} = \sqrt{\frac{\mathrm{Re}(Z_{in})}{R_S}} \tag{3-28}$$

By using these two expressions, it is ensured that 50 Ohm input impedance matching is achieved. This impedance transformation also sets the Q_{opt}. In the previous section, an expression for the noise figure was given based on the quality factor of the source and that of the optimum admittance. In the CS LNA, the gate noise is enhanced by the RLC series tank adding to the noise figure, while a higher quality factor of the input resonant circuit reduces the contribution of channel noise. Thus, care must be taken to achieve a value that brings the balance between these two contributions [7].

3.3.1.3 Simulation results

The schematic of the LNA and the component parameters are provided in Fig.3.7.

The DC bias was first chosen to set the current consumption. Since more gain is desired from this LNA, a tentative current of 600 μA is decided for, leaving 400 μA for the mixer. With this current, the *gm* of transistor M1 is obtained as:

$$gm = \frac{2 \cdot Pd}{V_{DD}\left(V_{GS} - V_T\right)} \tag{3-29}$$

Based on (3-29), and assuming an overdrive voltage of 200mV, *gm* has a value of 6mS. According to this initial evaluation, transistor M1 is biased by a current mirror supplying 450μA, and a V_{GS1} of 400mV. This combination induces a current of 603μA flowing in the LNA, when M1 has an aspect ratio of 20/0.065 and M2 of 30/0.065.

Dimensioning the LC tank sets the voltage gain of the LNA, which provides the voltage swing of the signals at the mixer input. The inductor is chosen to be 300 pH having a Q of 26.8, while the capacitor is chosen to be 74 fF. The capacitance of the LNA needs to be interpreted within the whole receiver since the capacitance in further stages affects the AC behavior with respect to voltage gain and resonance frequency. This is discussed within the coupled filter section 3.3.3 of this chapter. The simulated AC voltage gain is given in Fig.3.8.

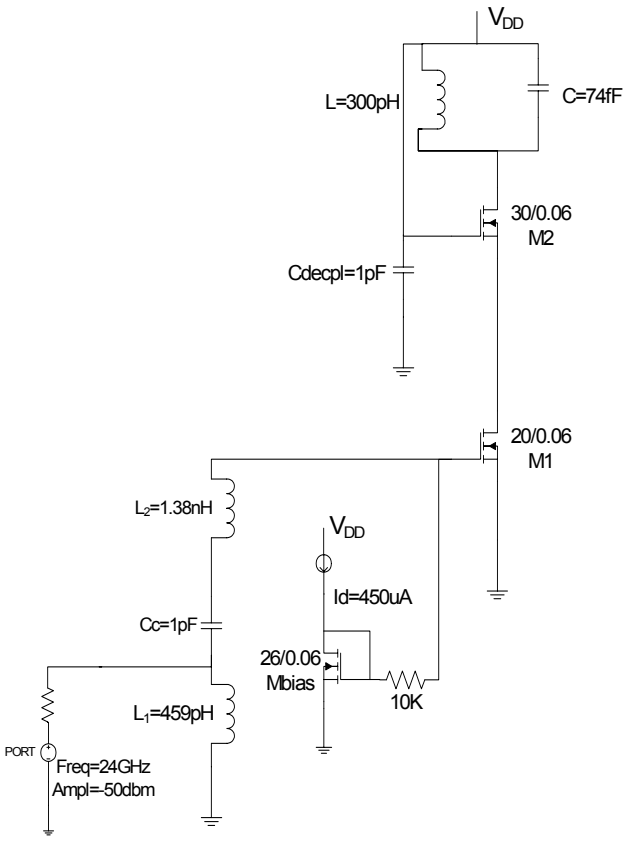


Fig.3. 7 Schematic of LNA

The gain achieves a value of 22.18 dB at 24 GHz, while its 3dB bandwidth is 1.1 GHz. This is enough for the ISM band specification, which required a 250 MHz bandwidth. Over this bandwidth, the gain decreases by 0.5 dB.

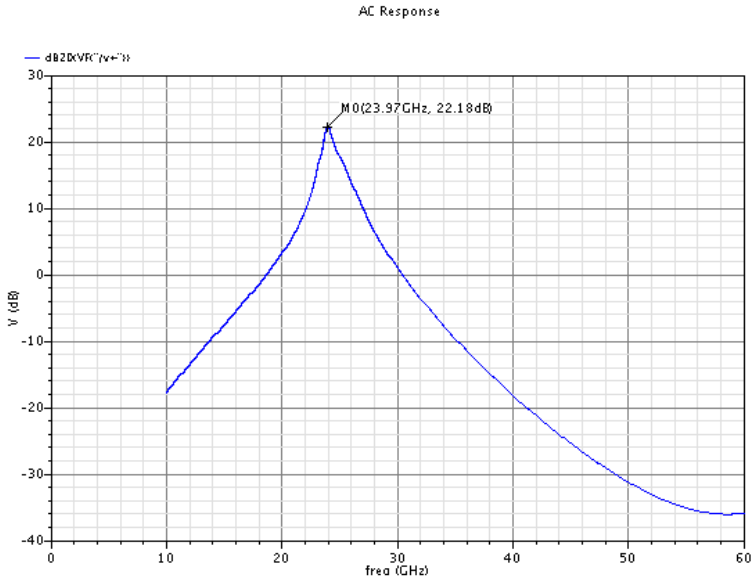


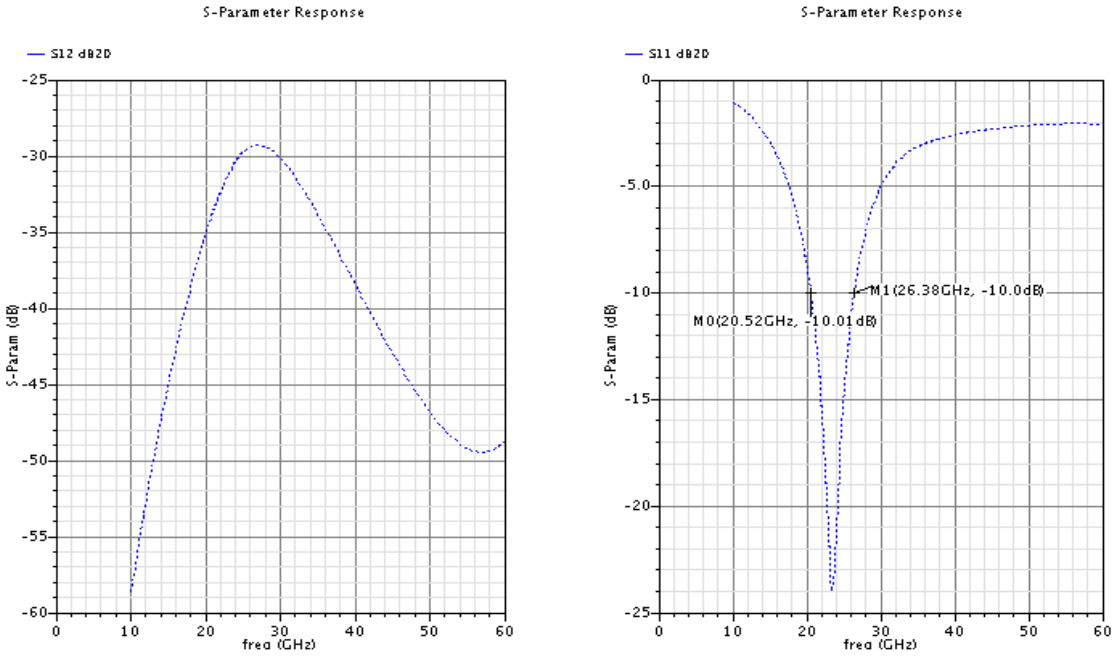
Fig.3. 8 Simulated voltage gain

To achieve an input impedance match, the strategy described in the LNA design section is adopted.

Using (3-27), the sum of the inductors is solved for, knowing that the value of C_{GS} is 23.7 fF at 24 GHz. The imaginary part of the input impedance will disappear with a value of 1.85 nH. For the real part of the impedance, first the input impedance of the transistor is simulated. This is found to be 250 Ω.

Using (3-28), an inductor ratio of 2.23 is found. This results to L_2=1.27 nH and L_1=572 pH. Due to the fact that the values found belong to ideal inductors, certain modifications are made to incorporate the resistance losses. Comparing with Fig.3.14, the resulting values are not far from the ideal case, even though the quality factor of L_2 is only 4, while that of L_1 is 16.

Using these inductances, the input reflection coefficient, S_{11}, and the reverse isolation, S_{12}, are shown in Fig. 3.9. S_{11} shows a wideband match with a bandwidth of 6 GHz, between 20.5GHz and 26.4 GHz. S_{12} shows an attenuation of more than -28 dB, at a frequency of 28 GHz, which is the resonant frequency of the standalone LNA, when it is presented with an impedance of 1.2 kΩ from an output port. This is the impedance of the resonant tank.



(a) **(b)**

Fig.3. 9 a) Reverse isolation, S_{12}; b) Input reflection coefficient, S_{11}

The real and imaginary part of the input impedance are shown in Fig.3.10. The imaginary impedance is close to 0 over the 6 GHz band where S_{11} is lower than -10dB. Although the real part of Z_{IN} is not 50 Ω, for S_{11} being less than -10dB over the band, it provides an acceptable wideband match.

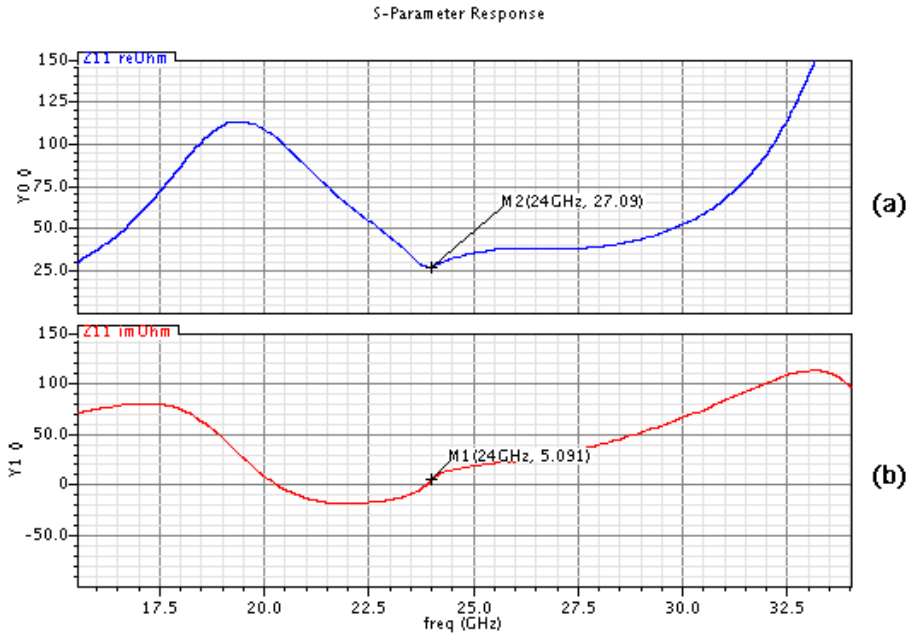


Fig.3. 10 Simulated real (a) and imaginary part (b) of input impedance, Z_{11}

The noise figure has been simulated as well. Fig. 3.11 shows that a NF of 6.8dB is achieved which is also the NF_{MIN}. This shows that we are close to the best achievable NF, for this current consumption. The frequency range for which NF is +/-0.3 dB of this value is also quite large: 4GHz. In comparison to the NF values achieved with the inductive degenerative common source configuration, reported to be less than 5 dB [10, 11], this NF is quite large. Due to the reasons mentioned in the LNA design, this high value is quite expected.

A noise analysis of this LNA configuration will not be performed since the accuracy will never be the same as the one obtained by the simulator. Cadence MOSFET models are ultimately much more intricate than any model apparent in literature from which a noise description could be performed. Furthermore, noise contributions from other sources such as induced gate noise, substrate resistances or channel thermal noise can occur [13]. A basic

overview of the noise processes within the CS LNA configuration is abundant in literature [1, 7, 8-9, 13].

As a final simulation, the LNA stability has been checked. It is important to see that the LNA does not oscillate at any frequencies. This is checked by Rollet's stability factor K, defined as in (3-30). For K>1 and Δ <1, the amplifier is unconditionally stable over the shown frequency range. Fig. 3.19 shows that indeed these factors meet the requirements.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} \cdot S_{21}|}, \Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \qquad (3\text{-}30)$$

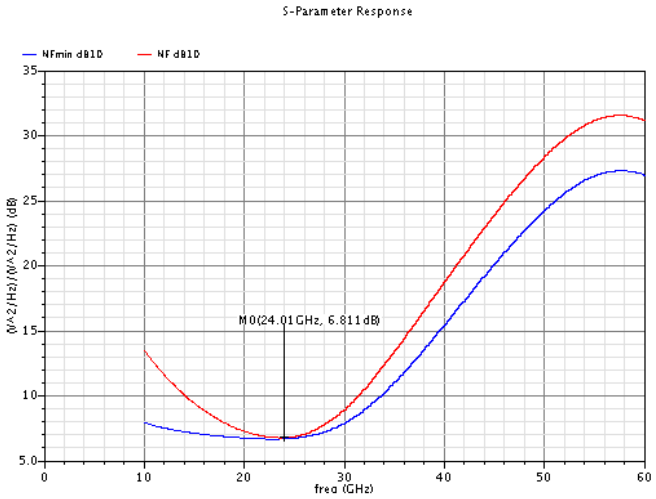


Fig.3. 11 Simulated noise figure and minimum noise figure

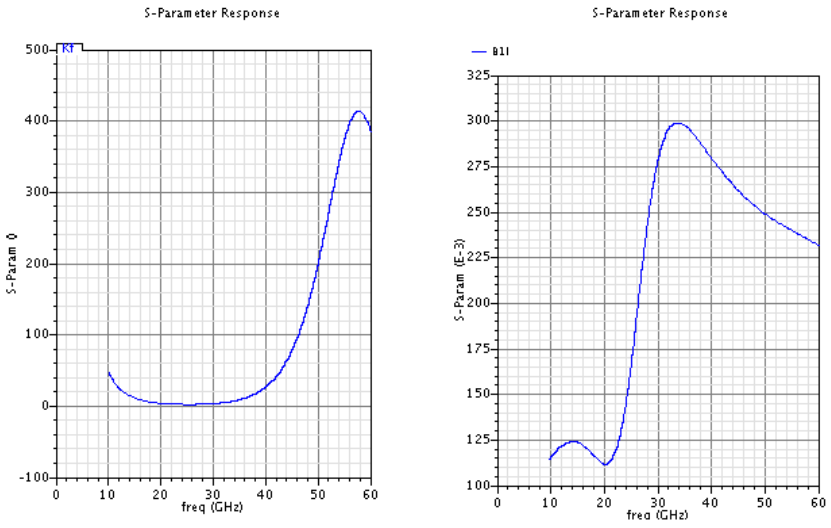


Fig.3. 12 Stability factors

A summary of the LNA simulated results is given in Table 3.1. The simulations have not taken into account parasitics from the input wire connecting the bond-pad to the matching network, which will add an inductance. Also, more inductance will be added due to the line connecting the cascode transistor to the LC tank. A discussion about these issues will be held in Chapter 5 regarding the layout.

Table 3. 1 LNA simulated results.

V_{DD}	1.2 V
Current consumption	600 μA
Maximum Voltage gain at 24 GHz	22.2 dB
NF at 24 GHz	6.81 dB
S_{11} (from 20.5-26.4GHz)	<-10 dB
S_{12}	<-30 dB
Stability	Unconditionally stable

3.3.2 Mixer Design

There are two classes of mixers employed in IC design: passive and active mixers. At the expense of more power consumption, active mixers are preferred since they provide gain and thereby reduce noise present in the system [1]. Even though passive mixers have the advantage of speed and higher linearity, more gain and less noise is favored for this receiver.

A further categorization of active mixers leads to balanced and single-ended mixers. Among the balanced mixers, the double-balanced topology is commonly used since it provides high gain, low noise, and less even-order harmonic distortion all at the expense of power [1]. In comparison to the balanced version, single-ended mixers are much simpler in structure, but also attain lesser specifications such as the ones mentioned above. Nevertheless, they consume less power.

The phase shifter presented in the system design section is better suited for a single-ended LO input. Therefore, a mixer with only two inputs would be desired, one RF input and one LO input. A review of the possible single-ended mixer topologies in [13] shows that a mixer topology with these specifications is fulfilled by the dual gate mixer, shown in Fig. 3.14a.

3.3.2.1 Theory and Mixing Concept

Dual gate mixers are a type of active single-ended FET mixers. Depending on where the LO signal is fed into a FET based mixer, three kind of nonlinearities can be employed for frequency mixing: the gate source capacitance, the transconductance, and the drain resistance. Moreover, the MOSFET can be biased at different bias points to take advantage of these nonlinearities. Fig.3.13 shows the biasing points and the way the LO signal moves these points during mixing. The typical Gilbert cell topology is a gate fed mixer which takes advantage of the varying transconductance while the LO switches the FET from the saturation to the cutoff region. The dual gate mixer is a drain fed mixer which uses the drain source conductance and the transconductance variation as the LO varies the FET from the saturation to the linear region [13].

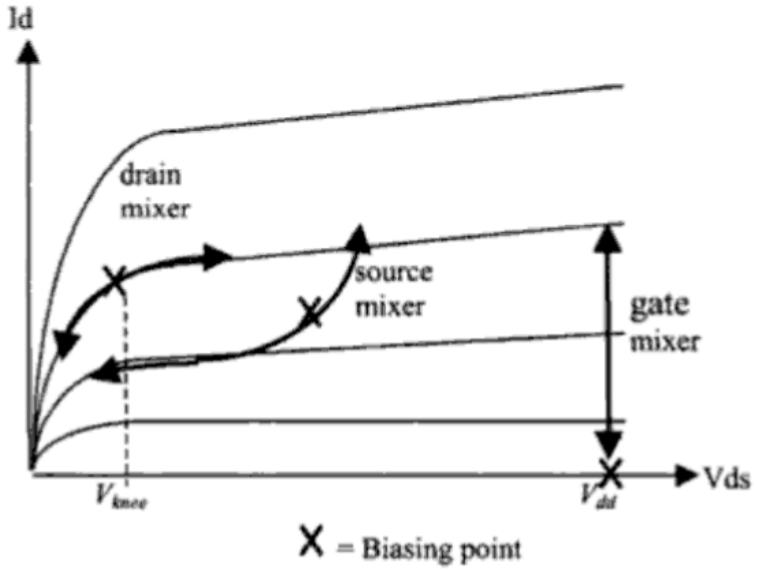
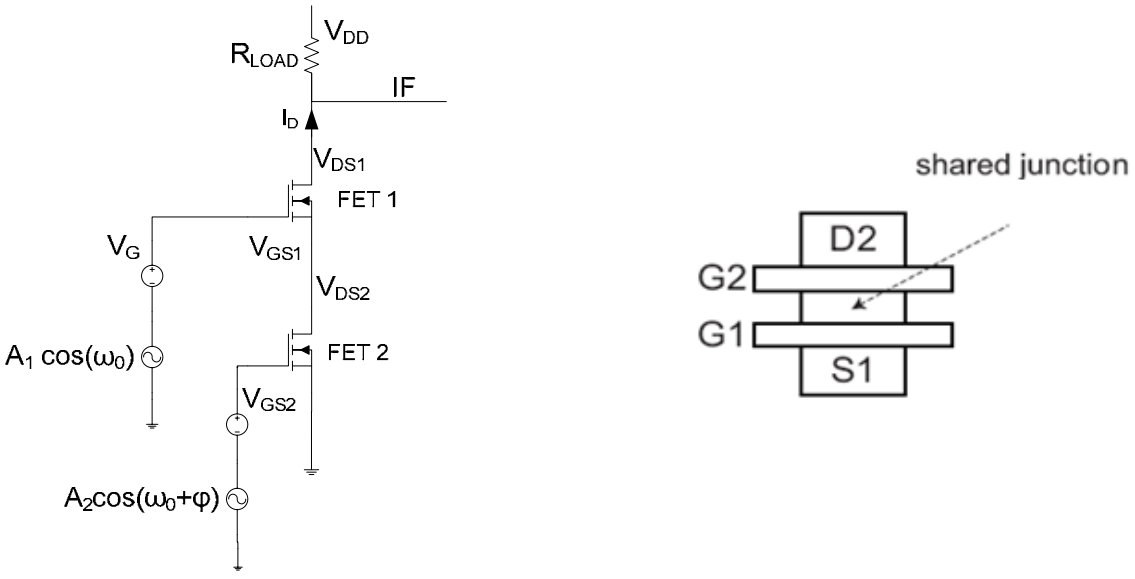


Fig.3. 13 Bias points for gate, drain and source mixers and their paths while mixing. [13]

Compared to the Gilbert cell topology, the conversion gain of the dual gate mixer is lower. This is because the drain-source nonlinearity is lower than the gate source one. By using this nonlinearity, the dual gate mixer requires a higher LO amplitude for a higher conversion gain. On a first view this might be a disadvantage, but a higher LO power and less conversion gain implies better linearity performance in terms of intermodulation and cross modulation [14]. Another advantage, in comparison to single FET mixers, is that dual gate mixers have the LO and RF inputted from separate ports, therefore adding inherent signal isolation without filtering [15].

Applications for dual gate mixers were in UHF television receivers and direct broadcasting satellite reception. They were also employed within microwave MMIC circuits when GaAs was not commercially available [14]. This is where the "dual gate" term originates from. The source of upper FET and the drain of the lower FET are shared, as shown in Fig. 3.14. In MMIC circuits, this was a great advantage since it provided LO to IF isolation and did not require complicated matching circuits for both inputs at the same node.



(a) **(b)**

Fig.3. 14 a) Schematic of dual gate mixer; b) shared junction

3.3.2.2 Mixer Operation

The operation of dual gate mixers has been extensively treated by Tsironis in [16]. From these investigations, it is apparent that dual gate mixers operate best in the low noise mode, when the lower transistor (FET2) is biased in the linear region while the top one (FET1) is in saturation. The assumption under this statement is only when the LO is an order of magnitude higher than the RF in order to drive the FET from the saturation region to the linear one. In the present receiver, the LO and RF have quite similar amplitudes since they both originate from the LNA. This implies that the LO does not have such high swing to be able to switch the lower FET completely from the saturation regime to the linear regime. That is why the lower FET has to be biased at the border of the active region. Had the LO been much higher in amplitude than the RF, FET2 could have been biased in the linear region. Fig.3.15 provides an explanation for this behavior.

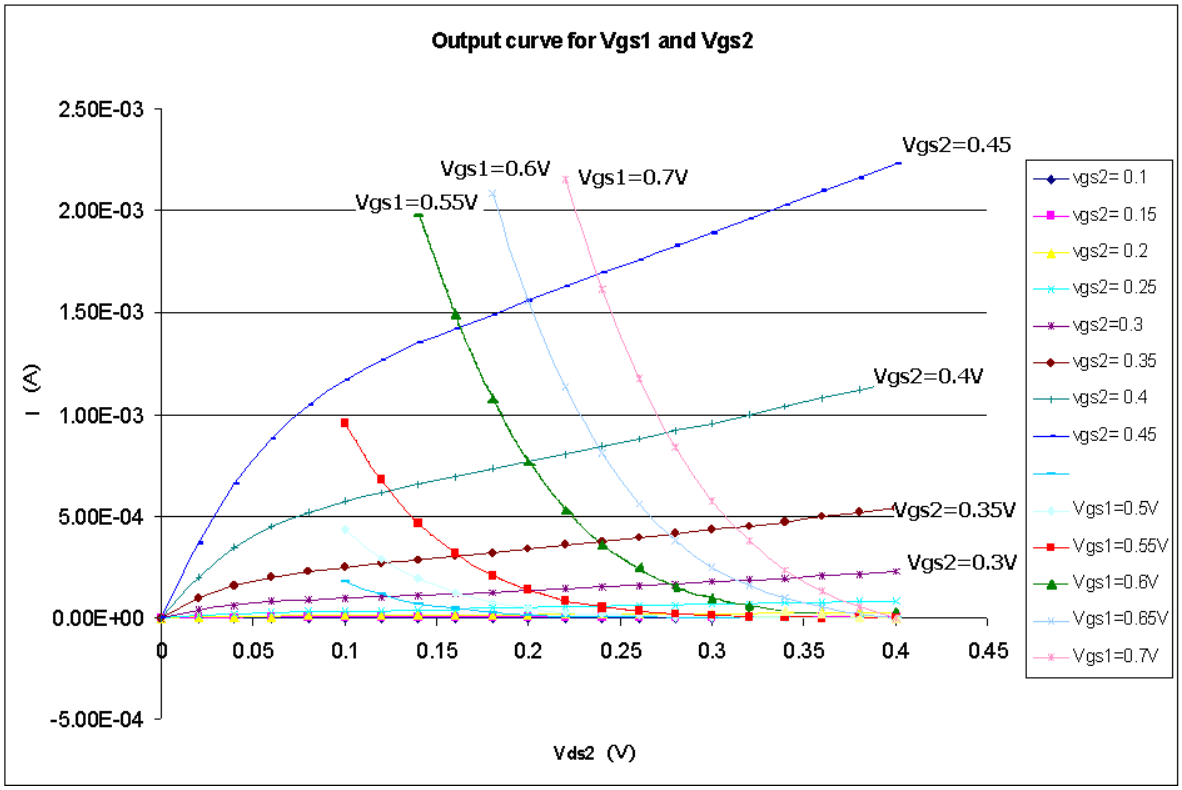


Fig.3. 15 Lower FET drain voltage modulation by LO signal

Fig.3.15 shows the drain current flowing through both FETs as a function of the drain source voltage of the lower FET (Vds2) and the gate-source voltage of the lower (Vgs2) and upper FET (Vgs1). One can see that based on different Vgs1 (Vgs1=0.6V, Vgs1=0.55V), these push or pull the lower FET (i.e. Vgs2=0.45V, Vgs2=0.4V or lower) out of the saturation region in the linear region. Therefore, if an LO signal is superimposed on the DC value of V_{GS1}, it will be able to modulate the drain source voltage of FET2, or to modulate its transconductance. This is why the LO signal should have high amplitude in general in order to switch the lower FET. In the present situation, since the LO signal does not have sufficient amplitude, the lower FET has to be biased at the border of the saturation region.

Moreover, the gate to source voltage of the lower transistor, V_{GS2}, needs to be selected such as to allow sufficiently high slope in the triode region, for the modulation of the transconductance to be high enough.

Putting all these observations into perspective leads to the conclusion that the bias point should be chosen when the conversion transconductance is highest with respect to the varying V_{DS2}. This point is chosen by plotting *gm* versus V_{DS2}. Fig. 3.16 shows the different slopes that *gm* obtains while V_{DS2} changes, for a certain V_{GS2}. The highest slope should be chosen for the highest conversion transconductance. Vgs2 is chosen to be 400mV as it provides a high slope: $5.5*10^{-3}$ mS/mV.

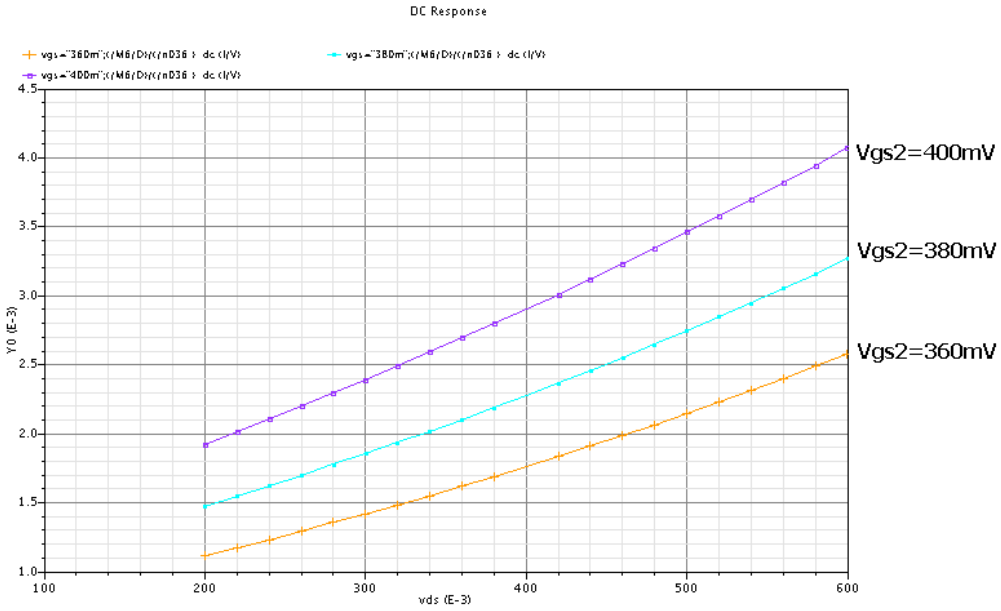


Fig.3. 16 *gm* as a function of V_{DS2} for different V_{GS2}

Once the functionality of the dual gate mixer has been presented, a description of the mixing process from a theoretical approach can be shown. To assist in the component terminology, Fig. 3.14 shows the DC voltages and AC signals. The two input signals have the same frequencies, but a different phase, as highlighted in Section 3.2 which presented the detection concept. Also, the signals should have the same amplitude, but for simplicity, it is assumed they are different.

Therefore, the input signals are:

$$m_1(t) = A_1 \cdot \cos(\omega_0 t) \tag{3-31}$$

$$m_2(t) = A_2 \cdot \cos(\omega_0 t + \varphi) \tag{3-32}$$

Since FET 2 operates in between the linear and active region, both cases will be treated: FET2 in the linear region and FET2 in the active region.

The transconductance *g(t)* of the lower FET is described as:

$$g(t) = \mu \cdot Cox \cdot \frac{W}{L} \cdot \left(V_G - V_{GS1} + A_1 \cos(\omega_0 t)\right) \qquad V_{DS2} \le V_{GS2} - V_T \rightarrow linear \tag{3-33}$$

$$g(t) = \mu \cdot Cox \cdot \frac{W}{L} \cdot \left(A_2 \cos(\omega_0 t + \varphi) + V_{GS2} - V_T\right), \quad V_{DS2} \ge V_{GS2} - V_T \rightarrow saturation \tag{3-34}$$

where $\left(V_G - V_{GS1} + A_1 \cos(\omega_0 t)\right)$ equals $V_{DS2.}$

A. FET2 in the linear region

In the case that FET2 is in the linear region, mixing happens in the following way:

$$io = g(t) \cdot v_{RF} = \mu \cdot Cox \cdot \frac{W}{L} \cdot \left(V_G - V_{GS1} + A_1 \cos(\omega_0 t)\right) \cdot \left(A_2 \cdot \cos(\omega_0 t + \varphi) + V_{GS2}\right) \tag{3-35}$$

,where *io* is the AC current at the IF output.

If $\mu \cdot Cox \cdot \frac{W}{L}$ is denoted by k, and $V_G - V_{GS1}$ and V_{GS2} are factorized, the following is obtained:

$$io = g(t) \cdot v_{RF} = k \cdot \left(1 + \frac{A_1}{V_G - V_{GS1}} \cos(\omega_0 t)\right) \cdot \left(1 + \frac{A_2}{V_{GS2}} \cdot \cos(\omega_0 t + \varphi)\right) \tag{3-36}$$

This leads to a downconverted output of:

$$i_0 = \frac{k}{2} \cdot \frac{A_1}{V_G - V_{GS1}} \cdot \frac{A_2}{V_{GS2}} = \frac{k}{2} \frac{A_1 \cdot A_2}{V_{DS1} \cdot V_{GS1}} \tag{3-37}$$

The conversion transconductance is then:

$$gc = \frac{i_0}{A_2} = \frac{k}{2} \frac{A_1}{V_{DS1} \cdot V_{GS1}} \tag{3-38}$$

B. FET2 in saturation

In the case that FET2 is in the saturation region, mixing happens in the following way:

$$io = g(t) \cdot v_{LO} = \mu \cdot Cox \cdot \frac{W}{L} \cdot \left(A_2 \cos(\omega_0 t + \varphi) + V_{GS2} - V_T\right) \cdot \left(A_1 \cdot \cos(\omega_0 t) + V_G\right) \tag{3-39}$$

If $\mu \cdot Cox \cdot \frac{W}{L}$ is denoted by k, and $V_{GS2} - V_T$ and V_G are factorized, the following is obtained:

$$io = g(t) \cdot v_{RF} = k \cdot \left(1 + \frac{A_2}{V_{GS2} - V_T} \cos(\omega_0 t + \varphi)\right) \cdot \left(1 + \frac{A_1}{V_G} \cdot \cos(\omega_0 t)\right) \tag{3-40}$$

This leads to a downconverted output of:

$$i_0 = \frac{k}{2} \cdot \frac{A_1}{V_G} \cdot \frac{A_2}{V_{GS2} - V_T} \tag{3-41}$$

The conversion transconductance is then:

$$gc = \frac{i_0}{A_1} = \frac{k}{2} \frac{A_2}{V_{DS1} \cdot V_{GS1}} \tag{3-42}$$

This theoretical approach is valid when there is a clear delineation in which regime FET2 works. Since the transistor operates in between the two regions, it cannot be asserted that the conversion gain will have a certain value based on these equations. The equations modeling the transconductance at the strong inversion point are very complicated and cannot be fully represented by the square law model of the MOSFET.

3.3.2.3 Simulation results

As discussed in Section 3.3.2.2, for the mixer to produce the highest conversion transconductance, it has to be biased at the border of the active region. This is achieved by setting V_{GS1}=V_{GS2} and by dividing the drain to source voltage to both transistors in an equal manner. However, the current consumption has to also be taken into account. Since the LNA consumes 600 μA to set the gain, a remaining 400 μA for the mixer is left. A favorable compromise between the voltage distribution and current consumption has to be decided for.

Fig.3.14 presented the drain to source and gate to source voltages that need to be determined. It is important to note that the variation of V_G influences every bias voltage and changes the current. Important relationships between the voltages are:

$V_{GS1} = V_G - V_{DS2}$ and $V_{DS1} = V_{load} - V_{DS2}$.

Another constraint on the distribution of voltages is the value of R_{LOAD}. This resistor sets the voltage at the mixer output by the following equation:

$$V_{OUT} = I_D \cdot R_{LOAD} \tag{3-43}$$

R_{LOAD} is chosen to leave 400mV at the mixer output, which is enough to provide a bias voltage to the gate of initial transistor in the IF amplifier. Therefore, R_{LOAD} is 2.1kΩ. Furthermore, the value is an optimum for defining the conversion gain.

A concurrent simulation has been performed taking into account all these relationships, by sweeping V_G, I_D and R_{LOAD}. The lower FET, with an aspect ratio of 40/0.065, is biased by a current mirror which sets V_{GS2} at 381 mV and the current through the two transistors. Fig. 3.17 shows only the V_G sweep and its effect on the other parameters. FET 1 also has an aspect ratio of 40/0.065.

Fig. 3.17 shows that both drain-source voltages vary significantly as I_D increases. If a lower V_{DS2} were chosen such as to push the transistor into the linear region, the DC current would be too small to convey a higher conversion gain. Moreover, as V_{DS2} increases, V_{DS1}

decreases showing that an almost equal distribution of the voltages should be striven for. Additionally, by choosing different bias points it has been noticed that a DC current of around 370-400 μA, taking care of the bias voltages at the same time, results in a good downconverted output voltage (not shown in this figure).

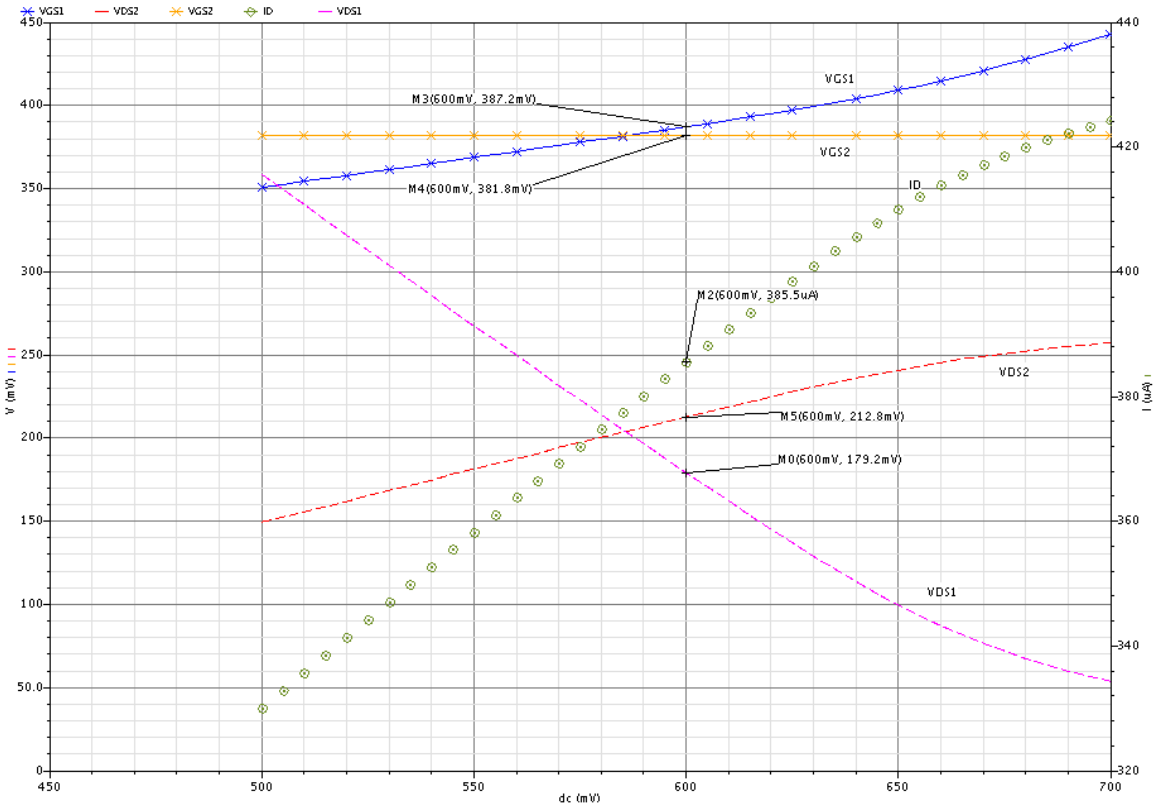


Fig.3. 17 Simulated DC bias points

The conversion loss has been simulated for the dual gate mixer. Fig.3.18 shows that the highest gain is reached when *plo* is -0.1 dBm for a conversion gain of -1.48 dB. The input power required for the highest gain is much higher than the signal amplitudes obtained from the LNA, therefore the conversion gain is indeed a loss. Nevertheless, the next simulation shows that the mixer operated at -22.3 dBm achieves a 1.8 mV output voltage. LO to RF feedthrough has also been checked and is lower than -70 dB. The noise figure of the mixer is simulated to be 12.2 dB at 24 GHz.

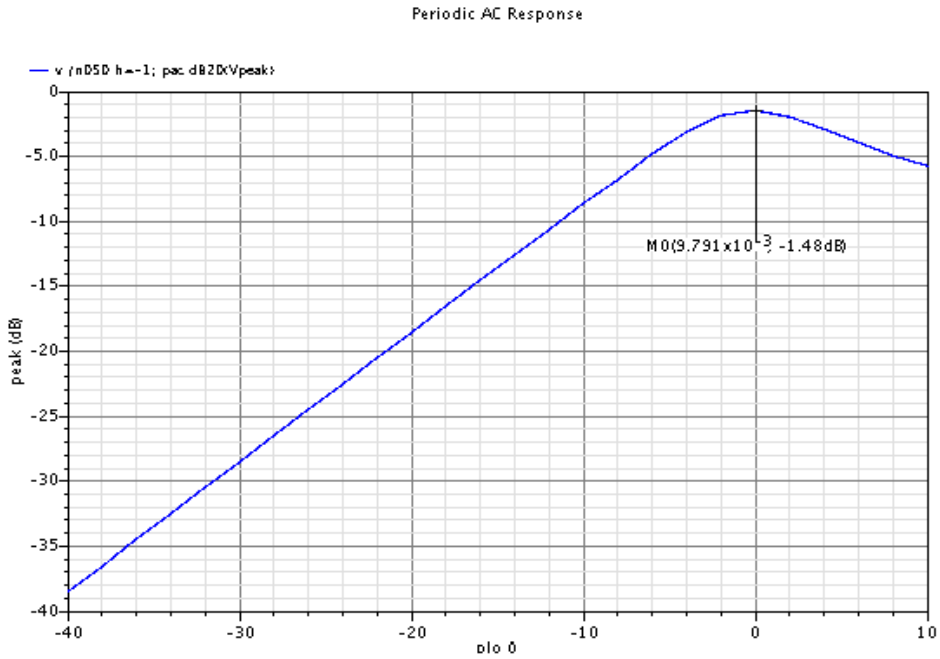
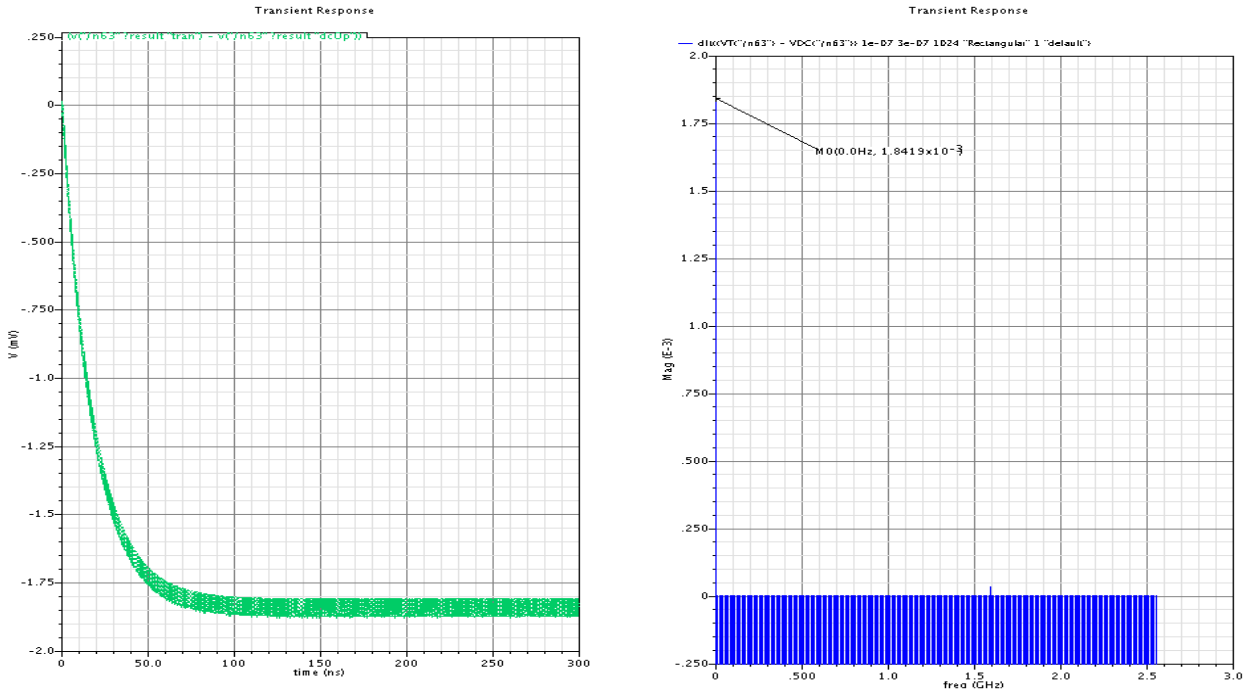


Fig.3. 18 Conversion loss of the dual gate mixer

A transient simulation is run for 300 ns to check the downconverted output voltage. The simulation is performed not on the mixer alone, but on the whole receiver-LNA, mixer and phase shifter- taking in consideration all coupling effects and impedance loading. The signals entering the mixer gates attain LO=24.1 mVpk-pk and RF=16.6 mVpk-pk. Fig. 3.19 shows the value of the downconverted output voltage of 1.84 mV at 0 Hz. The value is not high in comparison to what was suggested in the system design section, which was at least 5 mV. Still, due to the fact that this is the output of the whole receiver considering all non ideal effect, the output value is acceptable. Furthermore, a high gain IF amplifier can be designed to raise the downconverted voltage level to V_{DD} level, with a gain of around 55 dB.



(a) **(b)**

Fig.3. 19 a) Downconverted output signal; b) DFT transform performed on output voltage

Fig. 3.20 shows a plot of the receiver characteristic over a frequency range of 22 GHz to 26 GHz. The receiver reaches a maximum voltage level of 1.84 mV at 23.8 and 24 GHz and then decreases to lower values. The output level drops at a slower rate towards lower frequencies than towards the higher ones. This implies that the amplitude difference between the higher frequencies is higher than between lower frequencies. If two signals are chosen with a 400 MHz frequency difference- 24 GHz and 23.6 GHz- the amplitude obtained between these two frequencies is lower than the one obtained between other 2 signals with 24GHz and 24.4 GHz. From a digital design point of view, if 24 GHz represents a digital 1, and any other frequency is a digital 0, the rejection rate between a 1 and 0 is higher if signals with frequencies on the right side of Fig. 3.20 are chosen.

A further discussion regarding this topic will be presented when simulations on the entire receiver are performed, in Section 3.3.5.

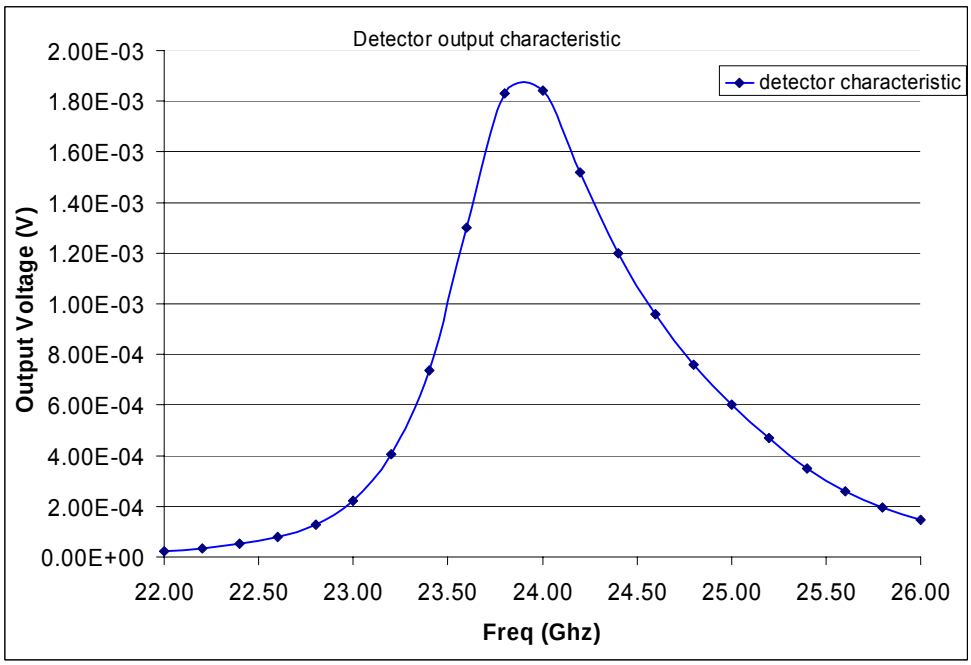


Fig.3. 20 Simulated downconverted output level for a range of frequencies

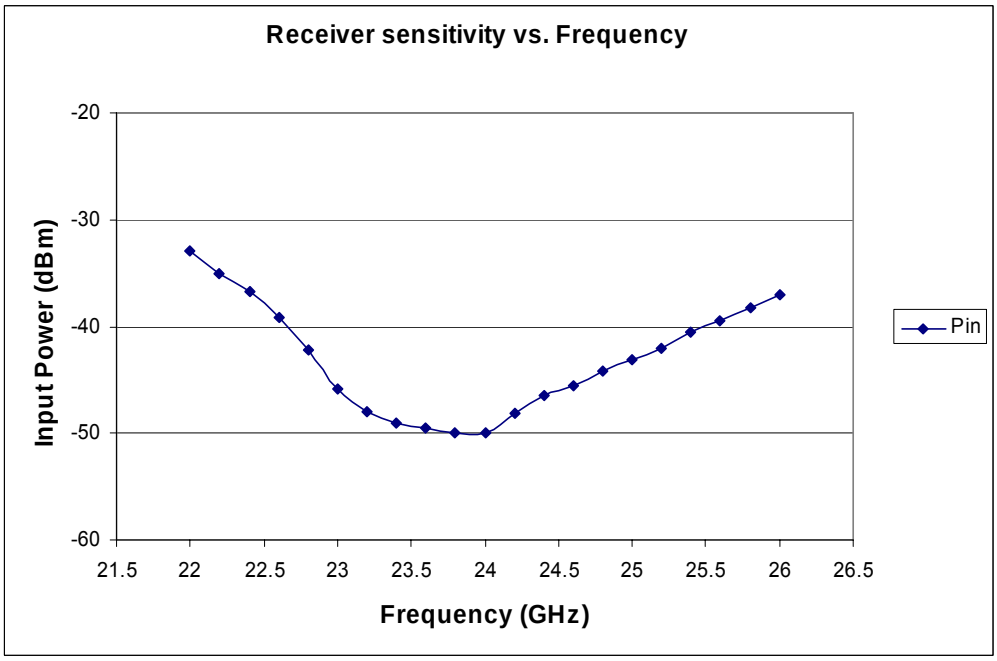


Fig.3. 21 Simulated receiver sensitivity for different frequencies.

Another simulation is performed to test the receiver sensitivity. Fig. 3.21 shows the input power the receiver needs in order to attain the same downconverted output as the one

achieved at 24 GHz. The downconverted output voltage reached was 1.8 mV at 24 GHz. To see how much more power the receiver requires in order to produce the same output level, the input power is varied and plotted. As the signal's frequency deviates from the central frequency, the receiver needs higher input power.

3.3.3 Coupled Filter Design within Complete Receiver

This section considers the interaction between the LNA, phase shifter, and mixer, in order to understand the overall system behavior. The circuit blocks designed independently have a different characteristic than when connected together. Impedance loading is the more serious effect of combining different circuit blocks together, in case they have different output or input impedances than the following or previous circuit blocks.
In the present design, the output impedance of the LNA differs from the input impedance of the mixer. The output impedance of the LNA is in the range of kΩ, while the input impedance of the mixer is a few ohms. Furthermore, impedance loading relates also to the imaginary parts of the components, changing their reactance/susceptance, thus also changing the resonance frequency.

For the current receiver, there are two LC resonant tanks present which interact with each other, changing their susceptances. The first LC tank is present in the LNA, while the other in the implementation of the phase shifter. The interaction can be interpreted within the context of coupled resonance filters, as shown in Fig. 3.22.

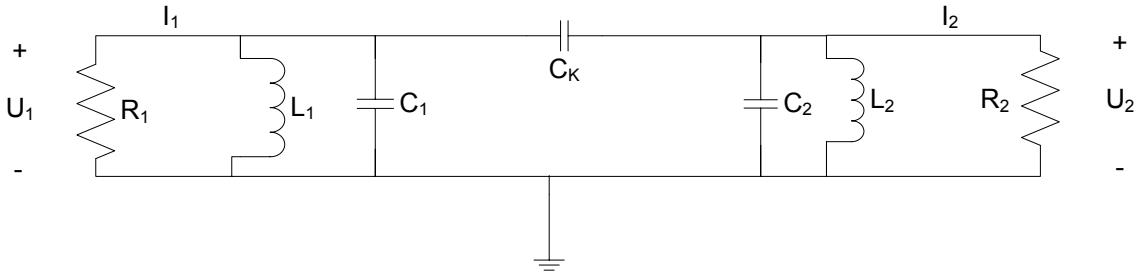


Fig.3. 22 Schematic of coupled resonance filter

It is characterized by having two resonant tanks coupled together via a coupling capacitor C_K. A derivation of the admittance matrix and the Z_{21} term that is important to determine the influence of C_K, can be found in [17]. Z_{21} is reproduced below, as:

$$Z_{21} = \frac{s^3 \cdot C_K \cdot L^2}{\left(s^2 LC + \frac{sL}{R} + 1\right)\left(s^2 L \cdot \left(C + 2C_K\right) + \frac{sL}{R} + 1\right)} \tag{3-44}$$

The first denominator term $\left(s^2 LC + \frac{sL}{R} + 1\right)$ produces a set of poles at a central frequency $\omega_0^2 = \frac{1}{L \cdot C}$. The other term $\left(s^2 L \cdot \left(C + 2C_K\right) + \frac{sL}{R} + 1\right)$ produces poles at the frequency $\omega_1^{\,2} = \frac{1}{L \cdot \left(C + 2C_K\right)}$. The resonant tanks have the same resonance frequencies, therefore, the equality between the components is assumed, such as C_1=C_2=C and L_1=L_2=L.

The set of poles formed by each frequency split away from each other based on the coupling capacitance. Therefore, for a high C_K, one set of poles are farther from the other. The result is a band pass filter response peaking where the poles are located with a local minimum at ω_0. For a lower C_K, the band pass filter response is smoother since the poles are closer to each other. The ratio between C_K and the capacitance of one tuned circuit represents the coupling coefficient, k_C, which determines how far apart the set of poles are. The following relation is presented in [17] and is valid if k_C is small enough:

$$\omega_1 = \omega_0 \cdot \left(1 - k_C\right) \tag{3-45}$$

The relation implies that the smaller the coupling coefficient, the closer the two resonant frequencies are. This is a point that is focused in the phase shifter design.

In the context of the present work, the coupled resonance filter can be recognized from the simplified schematic of the receiver which is shown in Fig.3.23.

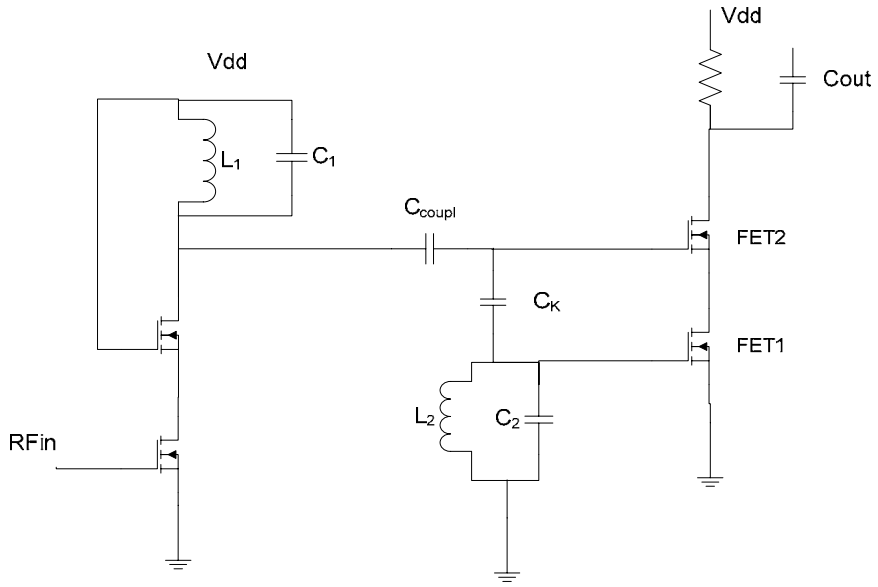


Fig.3. 23 Simplified schematic of the receiver

The coupled filter with transistor capacitances is shown in Fig. 3.24 together with the component values.

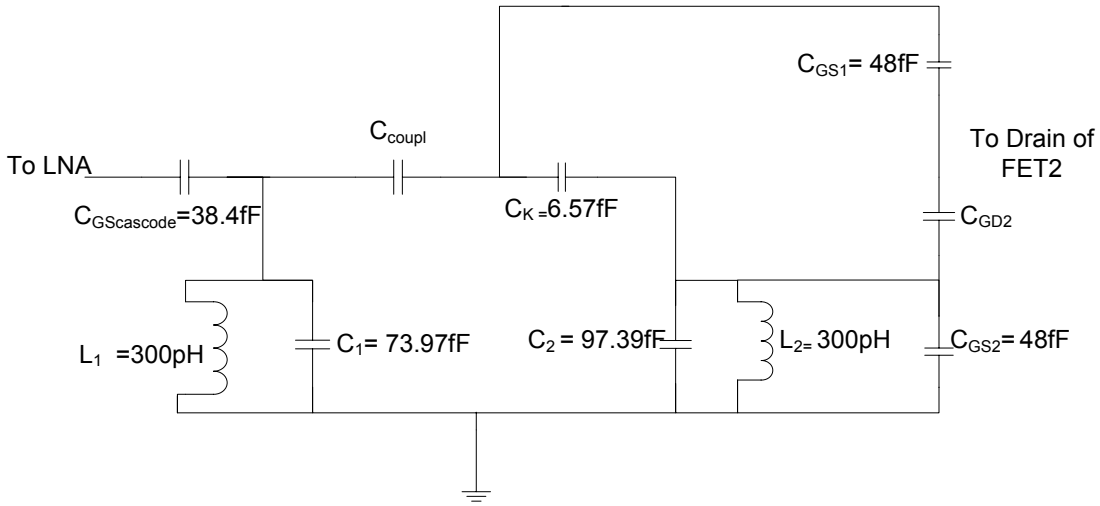


Fig.3. 24 Coupled resonance filter within the receiver

3.3.3.1 Phase Shifter Design

In the context of the coupled resonance filter, the phase shifter is designed. It is important to notice the focus for equality of the summed capacitances in the two tuned circuits to achieve a resonance at 24 GHz. Capacitances on one side of C_K amount to 160.4fF: $C_{GScascode}+C_1+C_{GS1}$, while on the other side they are 144.2fF: $C_{GS2}+C_2$. The coupling

capacitance influence is small, since kc= 0.04. From (3-45), the additional frequency that is created lies at 23.04 GHz.

The phase shifter was presented in Section 3.2.

To obtain a 90 degrees phase shift, the filter has to fulfill the following condition:

$$\omega_0 = \frac{1}{\sqrt{L \cdot (C_2 + C_K)}} \tag{3-46}$$

The inductor is chosen with the same value, 300pH, as in the design of the LNA, since its quality factor with the assigned width, inner radius and guard ring distances proved to be highest (Q=26.8). Capacitor C_2 is selected to be 96.2 fF, while C_k is chosen to be as small as possible to provide the least coupling between the two filters. Since the technology does not provide capacitors with a value less than 19.72 fF, a series combination of three capacitors has been chosen. The series capacitance has a value of: 19.72 fF/ 3= 6.5743 fF. According to (3-46), these values result in an operating frequency of 28.67 GHz. Due to the influence of the coupled filter, it is expected that the simulated attainable frequency decreases. Fig. 3.25 shows the phase shift attained between the signals entering the mixer. This figure also depicts the 3.4 dB difference between the signals, which amounts to a transient voltage discrepancy of 4 mV. The discrepancy does not influence the downconverted output. However, over a bandwidth of 250 MHz, the phase shift changes 11º from 95.8º for 23.875 GHz to 84.4º for 24.125 GHz. This behavior does have an influence on the RF signal of the lower FET. At 23.875 GHz, the RF= 16.8 mVpk-pk and LO=25.3 mVpk-pk. At 24.125 GHz, the RF= 16.8 mVpk-pk and LO=15.3 mVpk-pk. Nevertheless, the downconverted output does not change drastically: it ranges from 1.60 mV for 24.125GHz to 1.82 mV for 23.875GHz. Note that in the receiver characteristic shown in Fig. 3.20, the output level was the same for 23.8 and 24GHz.

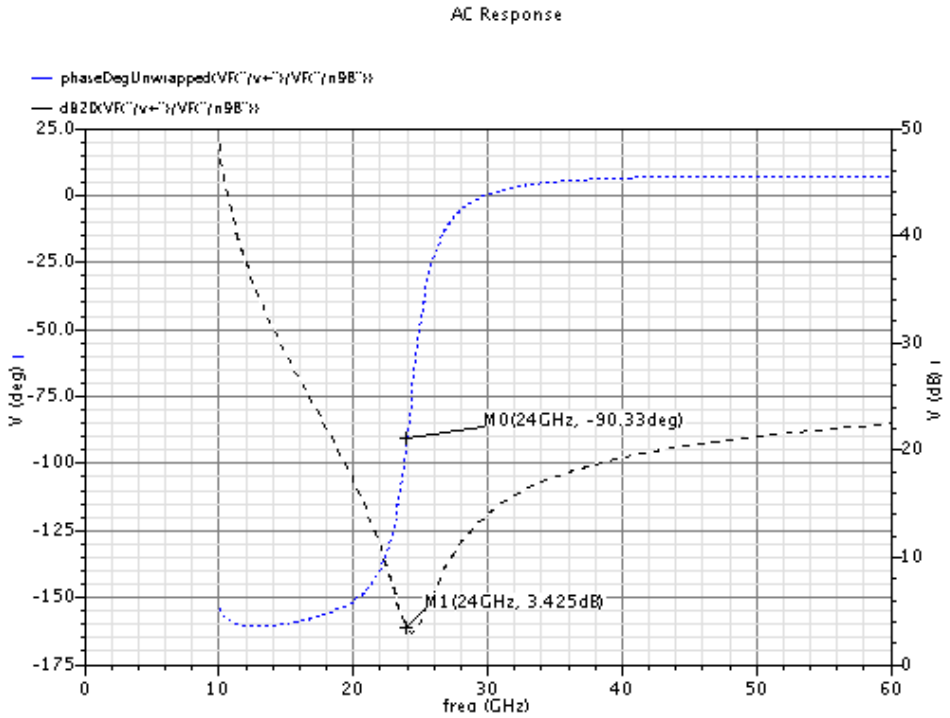


Fig.3. 25 Simulated Phase Shift between the LO and RF signals

3.3.4 Receiver Discussion

Since the RF circuit blocks influence each other in an intricate way, a discussion is held on how they impact the receiver performance. These effects are examined based on Fig.3.24.

First, it is important to note that the coupled filter influences the phase shifter design. Capacitor C_K plays a double role in the receiver: it produces the phase shift and defines the coupling between the two tuned circuits.

Second, the coupled filter influences the LNA design, since $C_{GS\text{-}cascode}$ and the LNA LC tank influence the resonant frequency. The LNA LC tank resonates alone at 28 GHz. This can be seen in the peak of S_{12} shown in Fig. 3.9a. By connecting the mixer to the LNA output, C_{GS1} adds to the total capacitance of the LNA, bringing down the resonance frequency. Furthermore, the gain of the receiver influences the signal swing at the input of the mixer which directly affects the conversion gain.

To see how the coupled resonance filter impacts the performance of the whole receiver, equal values of the capacitances in the two tuned circuits are selected and the coupling capacitance C_K is increased to 19 fF in order to see its influence on the AC response.

Fig.3.26 shows the AC response for three cases: a) C_2 is initially 96.2 fF (blue line) and C_K is 19 fF; b) C2 is changed to 79 fF (red line) and C_K is 19 fF; c) C_2 is 96.2 fF (green line) and C_K is 6.57 fF. In case b), C_2 is chosen to be smaller to account for the caused phase shift. The two maxima are seen clearly in the case when coupling capacitor C_K was increased. The maxima are shifted at frequencies close to the calculated resonant frequencies of the individual tuned circuits, while the minima in case b) with C_2 being 79fF, is close to 24 GHz, as expected from theory. The response of case c, when C_K is small, is also plotted to see the original gain characteristic.

As a conclusion to the RF design sections, the LNA, mixer and phase shifter have been designed. The LNA as specified in section 3.3.1 achieves a NF of 6.8 dB and 22.1 dB of voltage gain at the designed frequency. As specified in section 3.3.2, for an input power of -50 dBm, the mixer together with the phase shifter achieves a downconverted output voltage of 1.8 mV. Investigations regarding the influence of the two LC tanks within the coupled filter are performed. It can be stated that the receiver produces a recognizable output that can be processed by the IF amplifier. The next section presents the design of this amplifier such that a 1.2 V output voltage can be attained.

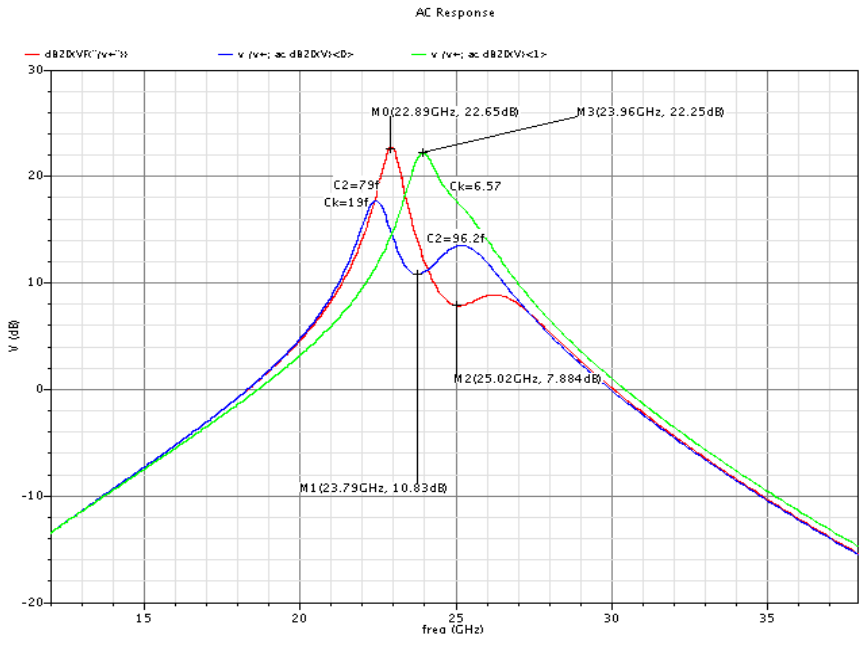


Fig.3. 26 Coupled filter responses when C_K is small (green line) and C_K is larger (blue and red curves)

3.3.5 IF amplifier

This section discusses the design of the IF amplifier. The design concentrates on the generation of a 5 MHz bandwidth and amplifying the FM detector output to produce a high swing voltage for giving digital 1s and 0s. As the output of the mixer is just a couple of mV, the amplifier should have a gain of around 55 dB. For this reason, the amplifier consists of two stages. Each of them are explained and discussed below.

The signal amplitude is increased by means of an operational amplifier with feedback. The feedback loop includes a high impedance amplifier and a capacitor to ground, as shown in Fig.3.27. The high impedance amplifier adjusts the output of the first stage to the bias voltage, V_{BIAS}. This amplifier sets the average DC value at the input of the feedback amplifier to its DC value from the detector output. In fact, it corrects any slow varying DC voltage as the input signal can be smaller than its own offset. Furthermore, the output of the high impedance amplifier is in the order of GΩs. Such a large value cannot be easily realizable on an IC by a resistor. The output of the feedback amplifier is fed to the folded cascode amplifier which supplies a high swing signal and further feeds it to the inverter.

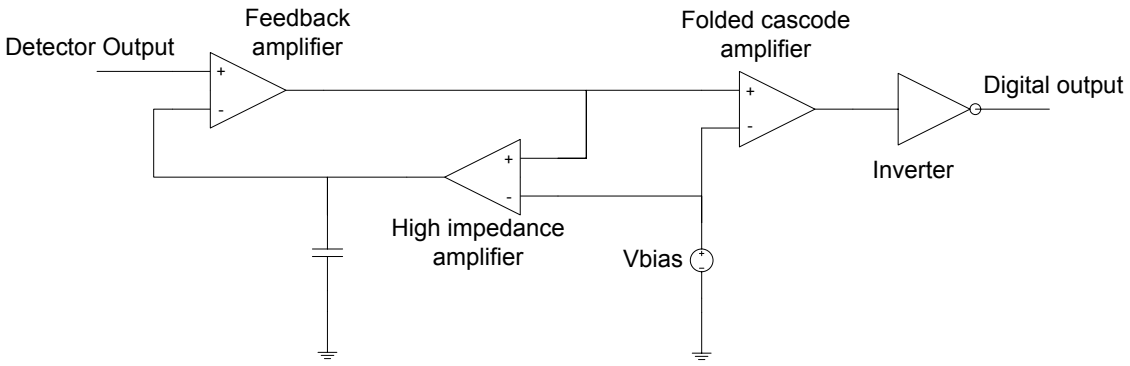


Fig.3. 27 System level schematic of IF amplifier

Fig 3.28 shows the transistor level implementation of the first stage of Fig.3.27. The feedback amplifier consists of the M1 and M2 differential pair with cascoded PMOS transistors. The high impedance amplifier consists of differential PMOS pair, M3 and M4, with triple NMOS cascode transistors to provide high output impedance.

The first stage, M1 and M2, provides offset correction for the inputs of the high impedance amplifier. Also, the offset of differential pair M1 and M2 may be larger than the detector output of 2mV. An offset correction mechanism is used which makes the amplifier sensitive enough to distinguish the 2mV input. It performs this detection by setting the M2 drain and M3 gate to the voltage of Vbias by means of the feedback loop. The selection of 600 mV for Vbias was done based on the range of M2's drain voltage. In the same way, the offset correction sets the same gate voltage on both M1 and M2. In this case, the DC value of the detector output is 391 mV. Therefore, both the inputs adjust to 391 mV. When a signal is detected, the input of M1 decreases by 2mV. This triggers the offset correction mechanism to go back to the normal 391 mV.

The feedback amplifier itself consumes 14 μA, which is enough to raise the detector output voltage and to charge/discharge the capacitance.

Bias control can be achieved by increasing the loop gain of the high impedance amplifier. This is done by increasing the cascode impedance. The widths of these transistors are 8 μm each, to ensure more resistance. The current consumption of the high impedance amplifier is 10nA. By ensuring sufficiently high impedance, the offset voltage at the input is reduced, to 2mV in the final design, which is acceptable.

The feedback amplifier's stability is investigated by breaking the feedback loop and checking the open loop gain and phase. The phase margin in this case must be positive and at least 45 degrees. The phase margin is 72 degrees at a frequency of 156 kHz, while the open loop gain has a value of 63 dB. To increase the gain, in this design, one can increase the capacitor size, increase the length of the cascode transistors or decrease the current flowing through the high impedance amplifier.

The second stage of the IF amplifier provides a high bandwidth and a high voltage swing for driving the output CMOS inverter. This stage takes the output of the feedback amplifier and a reference voltage V_{BIAS} of 600mV. The transistor level implementation of the folded amplifier is shown in Fig.3.29. The output signal swing of a source coupled pair such as the one formed by M1 and M2 is not able to provide a high swing. The uppermost PMOS transistors M3 and M5, and M4 and M6 form a folded cascode so that output swing can be from rail to rail. . The node connecting transistor M5 and M8 provides the possibility for a

high voltage swing since, in principle, the voltage can go from 100mV (needed by M5) to ground. This high impedance node is connected further to the CMOS inverter through a diode connected transistor, M7. This transistor limits the speed of the CMOS so that the DC current flowing through it is not too high (only 112nA).

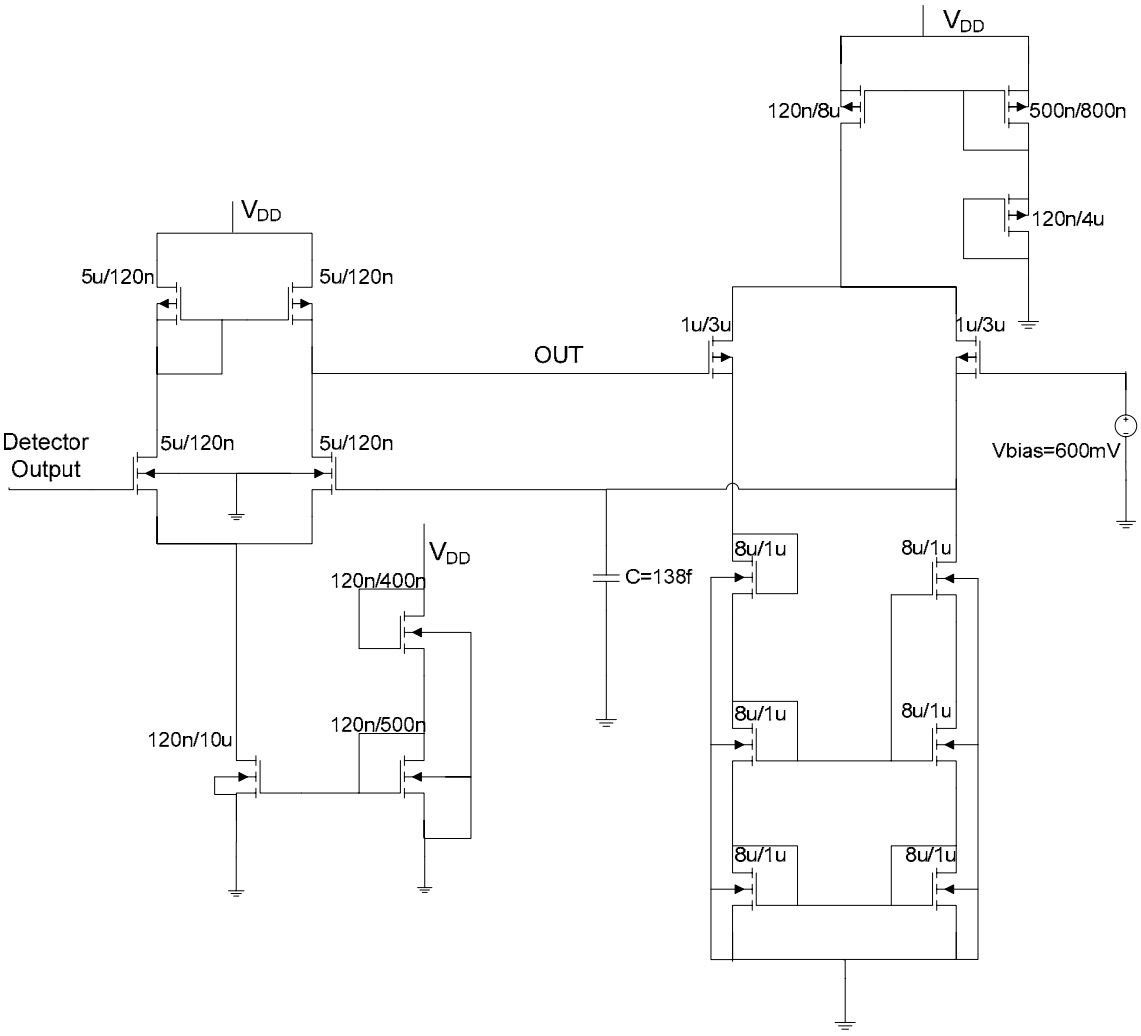


Fig.3. 28 Transistor level schematic of feedback amplifier

The bandwidth of the folded amplifier is limited only by the roll-off given by the pole resulting from the high impedance node and the input capacitance of the CMOS inverter. The bandwidth should be more than 5 MHz. This ensures that a high data rate for the receiver can be sustained.

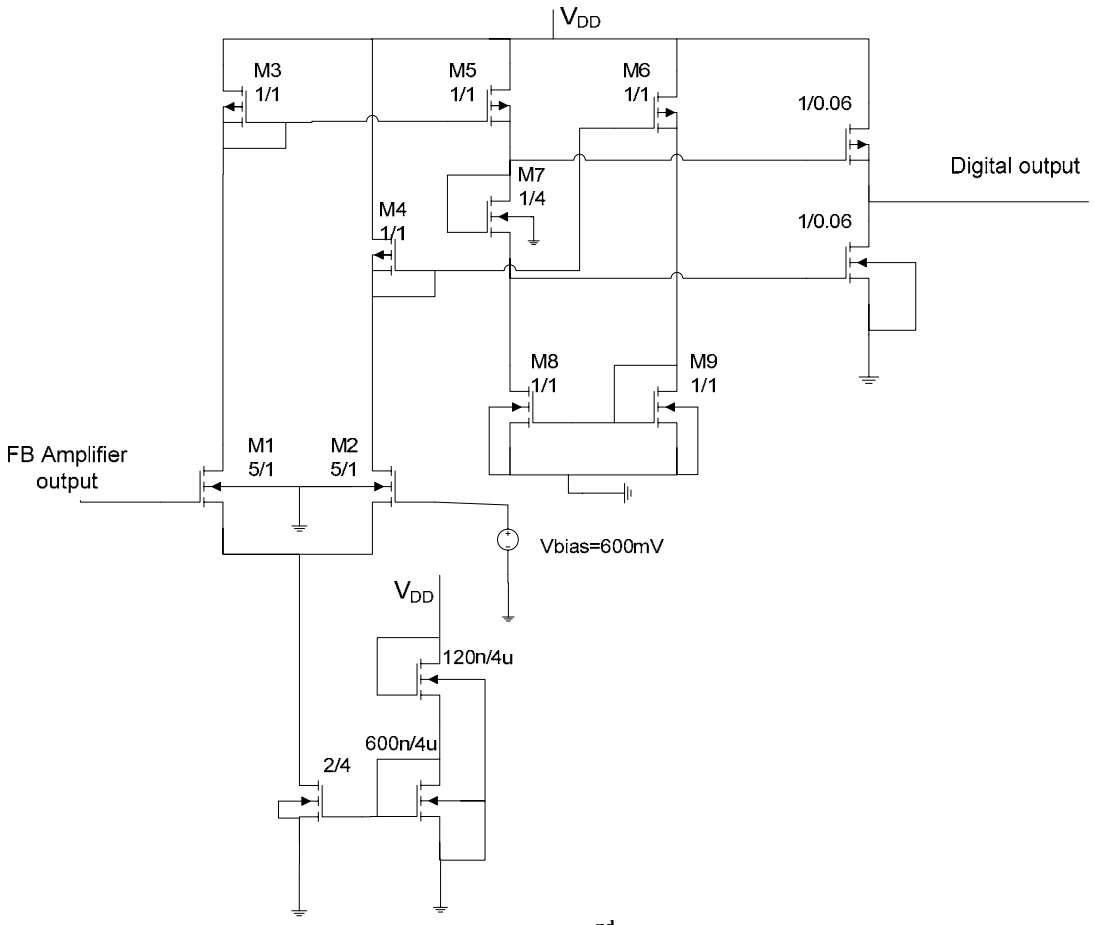


Fig.3. 29 Transistor level schematic of 2nd stage of IF amplifier

3.3.5.1 Simulation Results

The amplifier's frequency response has been simulated over a 1 GHz bandwidth. Fig 3.30 shows that at low frequency (less than 50 kHz), signals are greatly attenuated while for frequencies higher than 100 kHz, signals are amplified. Signals ranging in frequency from 500 kHz to 6 MHz are amplified correctly producing signals with little delays and distortion.

In view of the frequency response, there is a certain type of signal encoding the amplifier can use. Non-return-to-zero (NRZ) codes or Manchester codes should be employed. A falling or rising edge indicates a digital 0 or a 1, respectively. The reason for using NRZ

codes is because signals should not return to the average DC value as seen in return-to-zero (RZ) codes. By inserting a DC level in the encoding, the amplifier would have to deal with three DC levels, when only two can be sustained.

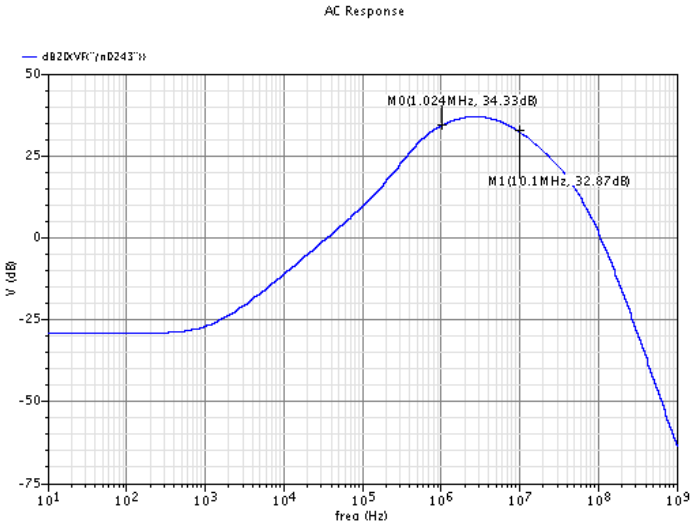


Fig.3. 30 Frequency response of IF amplifier

Simulation results of the IF amplifier with an input signal of 1.8 mV are given in Fig. 3.31. The amplifier has been simulated by emulating the behavior of the detector output. A transient voltage source switching between 0 and -1.81 mV and biasing the first stage with 391 mV has been chosen. The voltage source has been set with a period of 200 ns to set the 5 MHz data rate, with a 25 ns rise and fall times. The resulting transient characteristic of the IF amplifier is shown in Fig 3.31. Fig. 3.31 shows the input while second one shows the output of the IF amplifier. The difference between the output and input for a digital 0 is of 8 ns. The difference between the output and input for a digital 1 is of 10ns. Furthermore, there is a general input output delay, on the order of 27 ns.

The delay is caused by the time constant of the high impedance amplifier and capacitor. For a larger input amplitude, the delays become smaller.

Another simulation is performed with the following data pattern: 101001011010. This test checks the response for a sequence of 1s or 0s. The IF amplifier recognizes the sequences and it faithfully reproduces them with the appropriate intrinsic delays caused by the RC time constant.

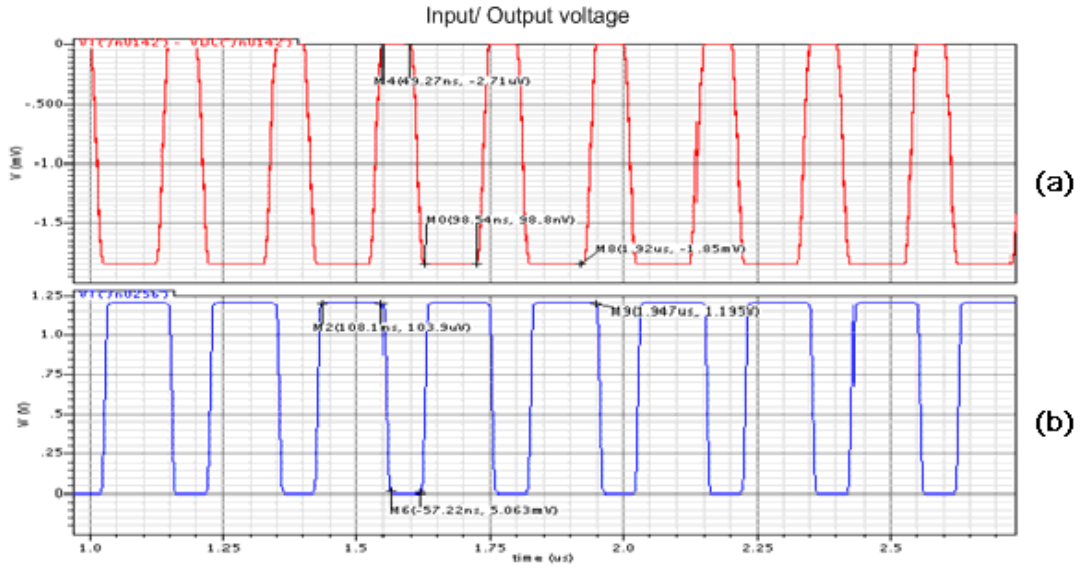


Fig.3. 31Transient operation of IF amplifier (a) input and (b) output voltage

3.3.6 Final receiver simulation results

The past sections described the receiver individual blocks and their performance. Typical figures of merit for each block have been reported, such as voltage gain, noise figure, current consumption, and downconverted output voltage. A last simulation is performed for an OFSK modulation in order to check for the demodulated signal at the receiver output

The simulation is set for 3 μs as in the IF amplifier testing. The first simulation is performed with two input tones at 23.6 GHz and 24 GHz. The 400 MHz difference is 150 MHz higher than required by the standard. The key rate is set at 5 Mbps. The simulation results are shown in Fig 3.32.

Fig. 3.32 (a) shows the frequency variation of the two tones- between 24 GHz and 24.4 GHz. The digital 1s and 0s have a duration of 75 ns and 125 ns, as shown by M2 and M0 respectively. Fig. 3.32 (b) shows the downconverted detector output. As in the previous simulation, the 0 and 1 bits have similar durations as the input waveform. The mixer output in this case is smaller than in the previous case, 1.7 mV, resembling the output value simulated in Fig. 3.19.

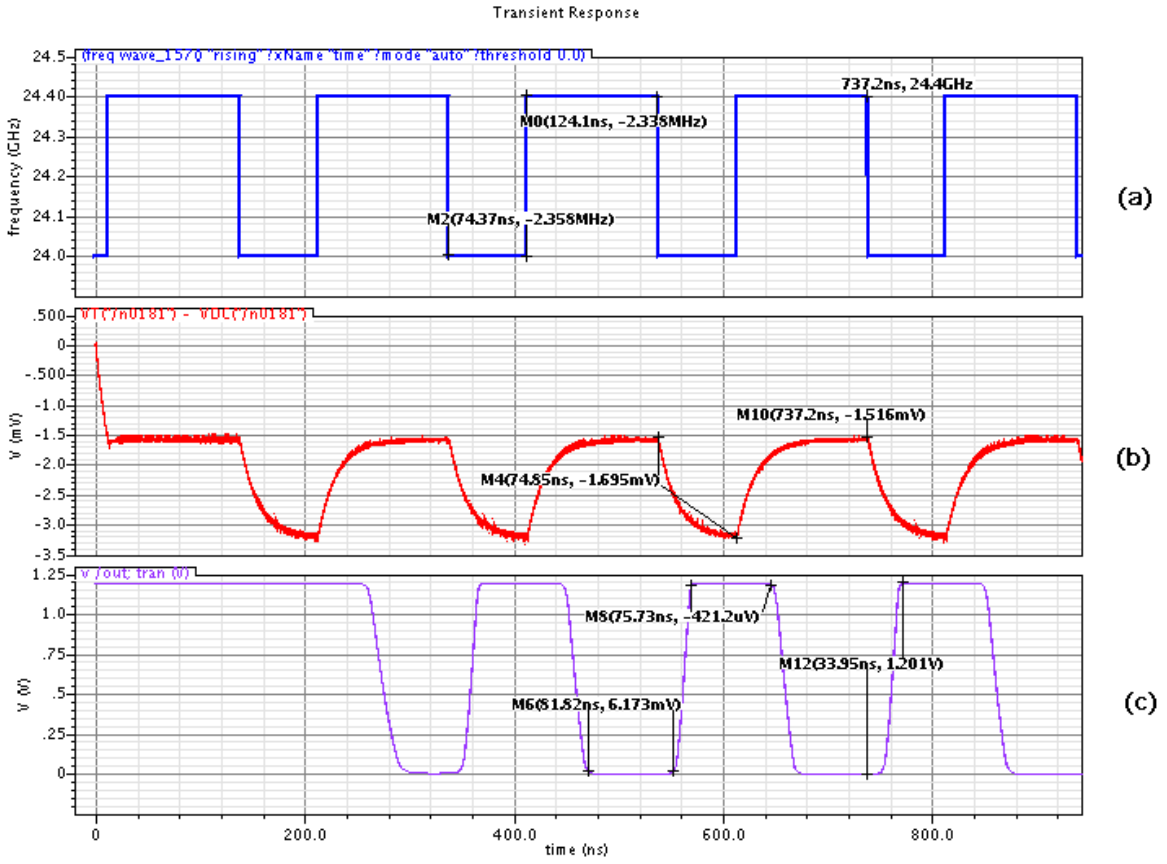


Fig.3. 32 Receiver response at 24GHz and 24.4GHz with -50dBm input power (a) input signal (b) detector output voltage (c) IF amplifier output voltage

Since the frequency deviation for the OFSK modulated signal is 400 MHz, the detector characteristic presented in Fig. 3.20 accounts for the difference in output signal level for the respective frequencies. Fig. 3.32 (c) shows the CMOS inverter result. The duration of the 0 bit is 100ns while that of a 1 is 75.7 ns, not too different from the ideal case. The delay between the output and input in the duration of bit 1 is of 34 ns. The same value is found for bit 0. In this case, the start-up time of the receiver is 300 ns.

As a second case, two input signals with the same frequency are set with a different power level: -50 dBm and -95 dBm. Fig.3.33 shows the rejection rate at these two different power levels. The DC bias is subtracted from the transient voltage.

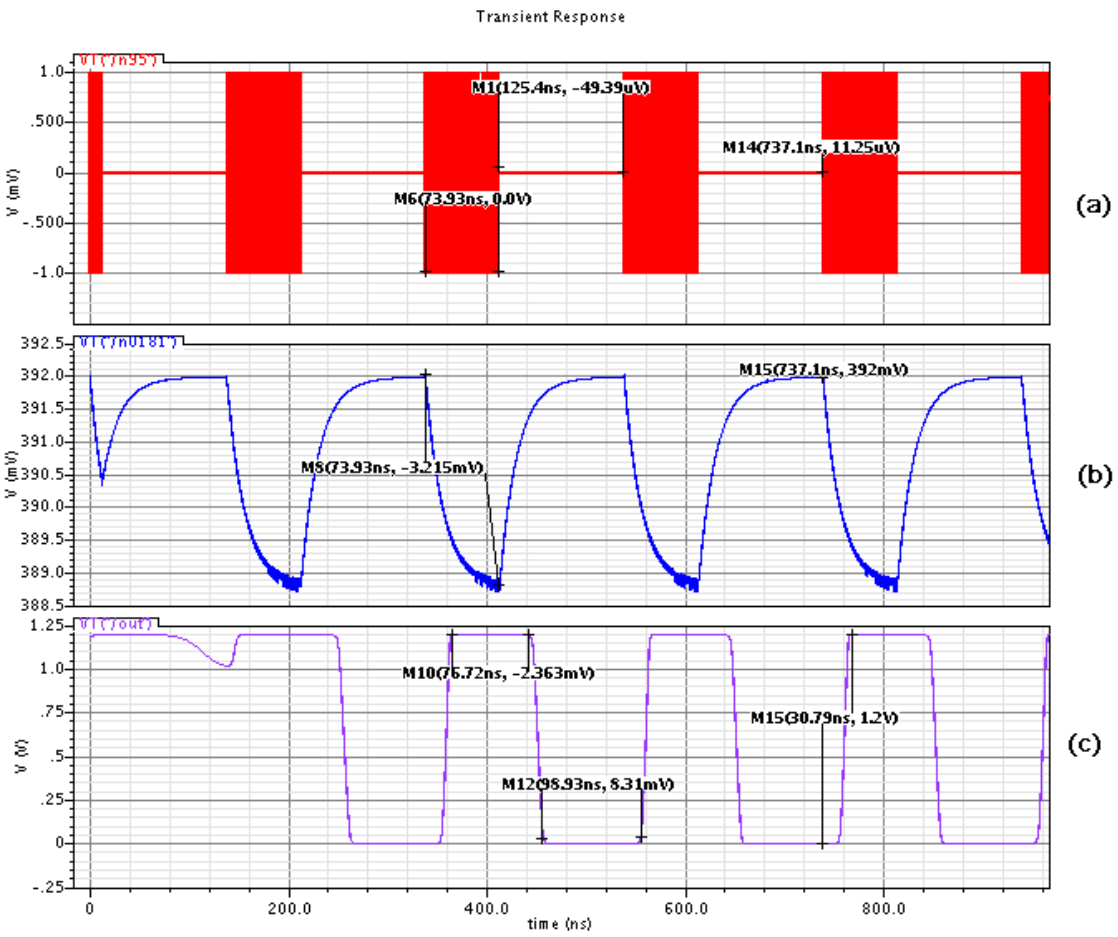


Fig.3. 33 Receiver response at 24GHz with -50dBm and -95dBm input power (a) input signal (b) detector output voltage (c) IF amplifier output voltage

Fig. 3.33 (a) shows the multiplexed input frequencies with the -95 dBm and -50 dBm power levels. The duration of a digital 1 is of 74 ns, while that of a 0 is 125 ns, shown by M6 and M1 respectively. Fig. 3.33 (b) shows the output of the quadrature detector for the different power levels. The plot shows no delay between switching from one power level to another, as can be seen from marker M8. The digital 0s and 1s have similar durations as the input waveform. When a tone with a power level in the receiver's range is detected, there is an output voltage- this is noticed by a decreasing slope. For a 0 bit, the output increases and returns to the initial DC value. The downconverted detector output is 3.215 mV in this case. Fig. 3.33 (c) shows the output of the receiver. The duration of a single 0 is 100.9 ns while that of a 1 is 76.7 ns, as can be seen from markers M10 and M8 respectively. For a digital 1, the output correctly presents a 1 but with a delay of 30.8 ns as can be seen from marker M15. A similar delay is found for digital 0. The start-up time of the receiver is 300 ns.

This simulation presents the receiver with a signal similar to an on-off keying modulated signal. The receiver interprets the -95 dBm amplitude as a 0 bit with no amplitude and practically 0 Hz. Therefore, looking at the detector characteristic presented in Fig.3.20, the output voltage difference between the maximum point corresponding to 24 GHz and the lowest point, which is closest to 0 Hz, accounts for the 3.215 mV difference. Therefore, the receiver works with an OOK modulated signal as well, although the specified modulation scheme is OFSK.

As a conclusion, it can be stated that the receiver performs within specifications: it achieves both the 1 mA current consumption and the 5 Mbps data rate, while correctly demodulating both OFSK. Although it is intended for OFSK modulation, the receiver demodulates OOK signals as well. Table 3.2 and 3.3 provides the main receiver results. Table 3.3 shows the noise figure and gain attained by the individual RF blocks.

Table 3. 2 Simulated receiver results

V_{DD}	1.2 V
Current consumption	1 mA
Sensitivity	-50 dBm
Data rate	5 Mbit/s
S11 (from 20.5-26.4GHz)	<-10 db
Detector output	1.8 mV
Receiver output voltage swing	1.2 V

Table 3. 3 Gain and NF of receiver RF blocks

	LNA (dB)	Mixer (dB)
NF	6.8	12.2
Voltage Gain	22.14	-21

Fig. 3.34 shows the schematic of the designed receiver with biasing as well. The implementation of the IF amplifier can be seen in Fig. 3.27- 3.29.

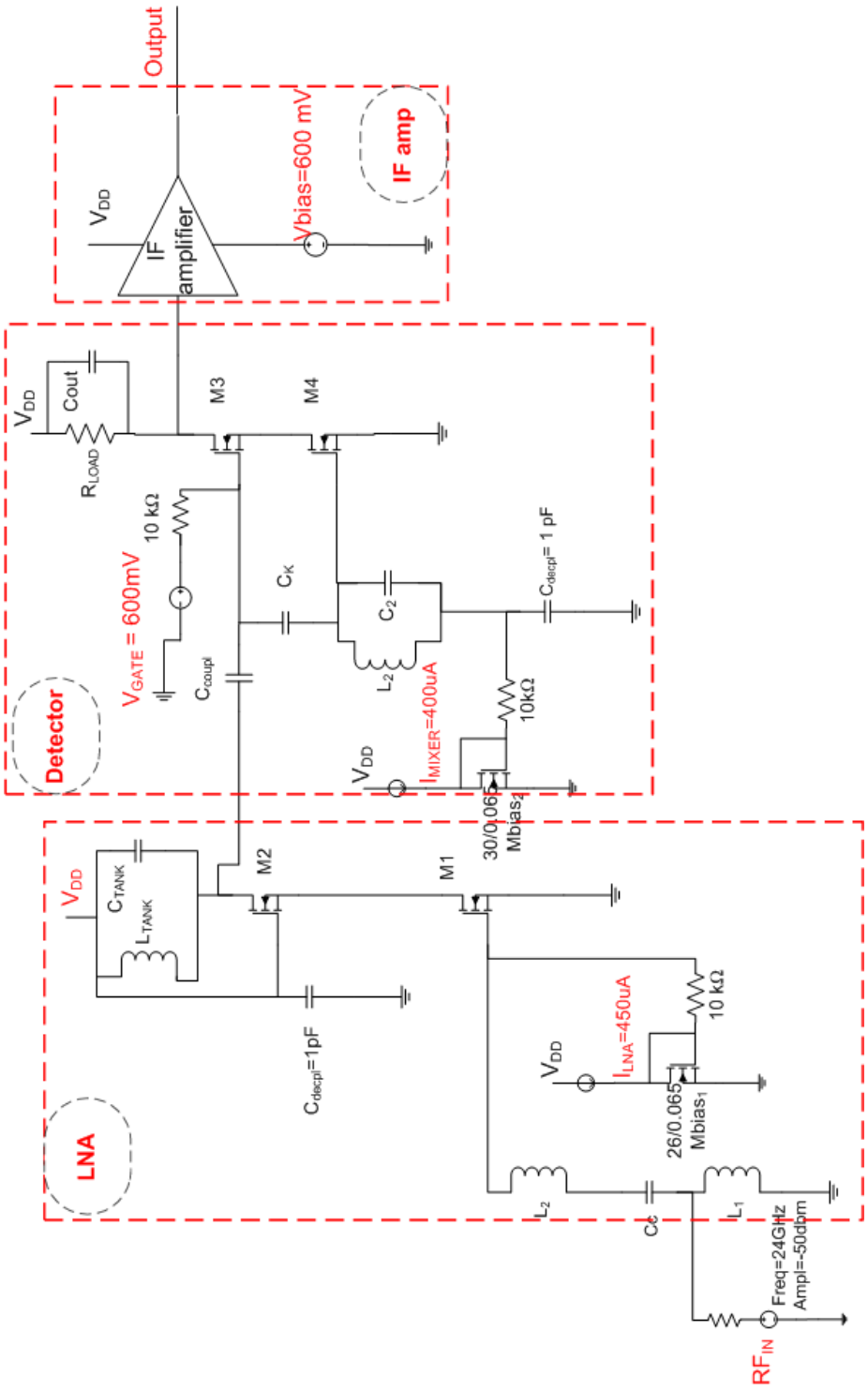


Fig.3. 34 Schematic of LNA-detector

3.4 Common Gate Input Detector

Another version of the receiver has been designed. This stage eliminates the common source LNA and leaves only the FM detector to be sent for tape out.

Section 3.3.1 highlighted the need for wideband input matching. For the case that there is potential mismatch in the inductors from the resonant tank and from the input impedance matching network, a wideband match would suppress this variation and leave the input reflection coefficient below the required value of -10dB. Also in this section, common gate (CG) low noise amplifiers are described in comparison to the common source ones. One of the conclusions was that CG LNAs have an inherent wideband input matching equal to $1/gm$. This fact will be used in the design of the second version of the receiver.

To overcome the possibility of mismatch between the inductors, a common gate version of the LNA is designed. The schematic of the second version of the receiver is shown in Fig.3.35. Transistor M1 assumes the role of the CG LNA and is the former cascode transistor used in the design of the CS LNA. It has the same aspect ratio. Biasing is provided by resistor R_2 which sets a current of 600 μA through the branch. Input matching is performed by resistor R_1 which sets the required 50 Ω input impedance seen by the transistor. All other dimensions of the front-end are left the same. The full schematic of this receiver is the same as Fig. 3.34, excepting the input stage.

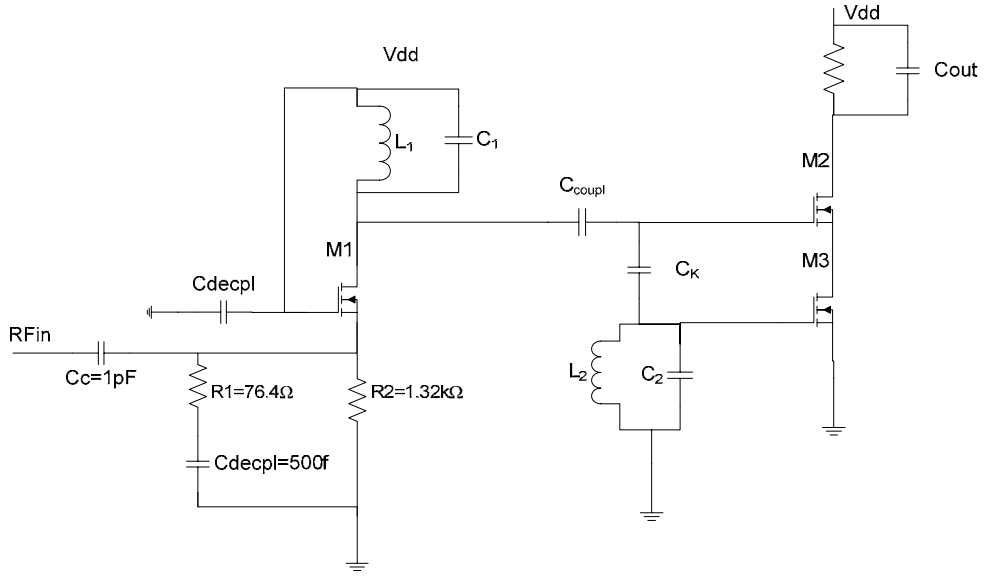


Fig.3. 35 Transistor level schematic of common gate detector

3.4.1 Simulation results

A first simulation checks the voltage gain of the common gate stage. The gain is not as high as that of the CS LNA, as the common gate stage transconductance is [7]:

$$G_M = \frac{1}{2} \cdot g_m = \frac{1}{2 \cdot R_S} \tag{3-47}$$

where Rs is the input impedance. Figure 3.36 shows that the voltage gain is 9.6 dB at 24 GHz. With a -50dBm input power, this value is not be able to provide a sufficient swing for the signals entering the mixer: RF=3.86 mVpk-pk and LO=5.49 mVpk-pk. This indicates that the input power has to be increased. To achieve the same downconverted output voltage of 1.81 mV as in the first version of the receiver, the input power has to be raised to -37dBm.

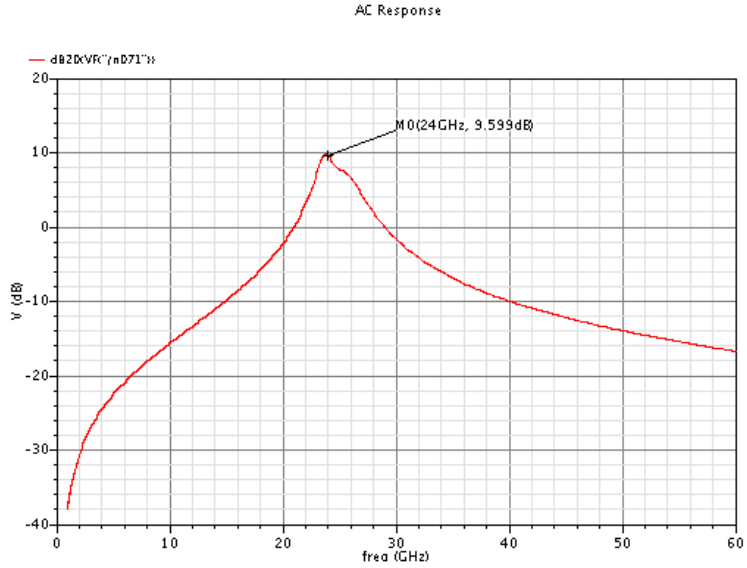
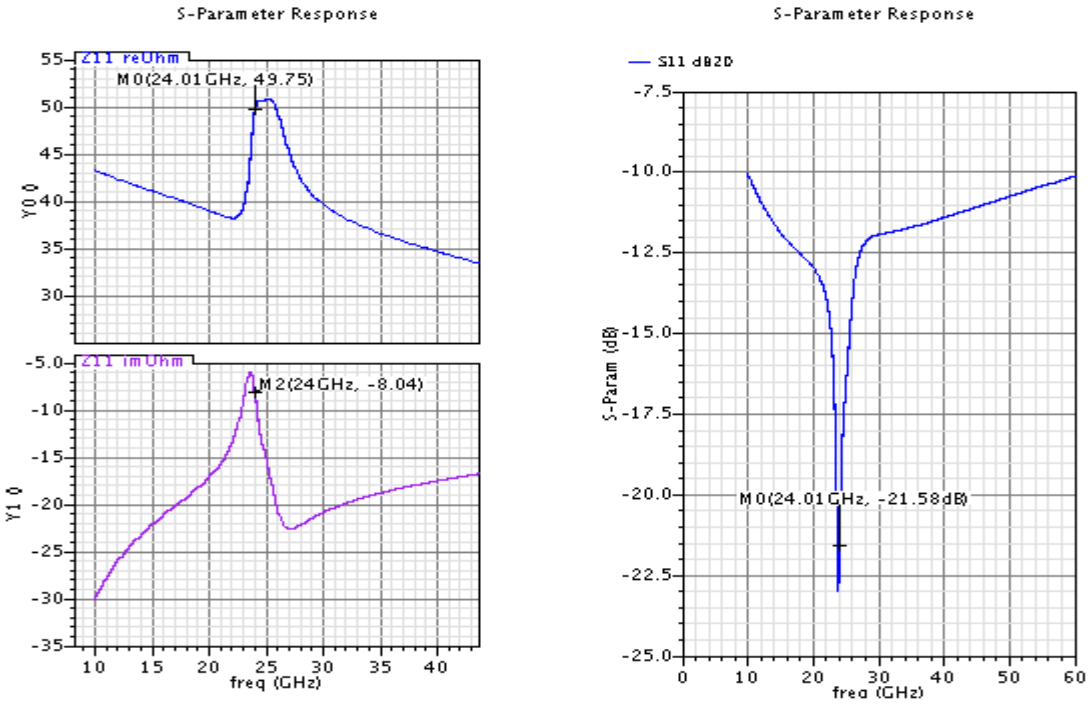


Fig.3. 36 Simulated gain of the common gate detector

Fig 3.37 (a), (b) shows the real and imaginary parts of Z_{IN} in addition to the input reflection coefficient. S_{11} is smaller than -10dB for a wide range of frequencies ensuring the input matching requirement. Furthermore, the real part of the impedance is 49.75 Ω at 24GHz, and ranges between 40 and 50 Ω over a 10 GHz bandwidth. The imaginary part also is capacitive.

With a -37dBm input power, the mixer has a resulting input RF signal of 12.26 mVpk-pk and an equivalent input LO signal of 8.7 mVpk-pk peak. A downconverted output of 1.8 mV is also achieved with this receiver.

This section examined a second version of the receiver. The common gate input stage was implemented in this version in order to eliminate any mismatches between the inductor from the LC tank and the input matching network. The CG stage transistor does not perform as an LNA since it does not minimize noise. The achieved noise figure is 11.3 as reported in Table.3.4 and 3.5. All other receiver blocks perform the same as reported in Table 3.3. The circuit provides a minimal amplification of approximately 10 dB. Therefore, the input power needs to be increased. Apart from these changes, the quadrature detector has not been changed. Consequently, it can be measured individually without the influence of the LNA.



(a) ,(b) **(c)**

Fig.3. 37 (a), (b) Simulated Z_{IN} and (c) S_{11}

Table 3. 4 Common gate input-detector simulated receiver results

V_{DD}	1.2 V
Current consumption	1 mA
Sensitivity	-37 dBm
Data rate	5 Mbit/s
S_{11} (from 10-40 GHz)	<-10 dB
Detector output	1.8 mV
Receiver output voltage swing	1.2 V

Table 3. 5 Gain and NF of CG input- detector RF blocks

	LNA (dB)	Mixer (dB)
NF	11.3	12.2
Voltage Gain	9.6	-21

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Chapter 4. IC Layout

4.1 Introduction to CMOS65 Technology

The TSMC CLN65LP technology lends itself to low power applications combining digital, native and RF MOS transistors and passive components. It accommodates 1.2 V, 2.5 V and 3.3 V input/output voltages. It has several front end features, such as dual gate oxide process providing a range of gate voltages and multiple threshold voltage (low, standard and high V_T) for low leakage and high performance requirements [1]. The transit frequency f_T for the transistors used in this work varies between 160 GHz[1] and 84 GHz[2], while f_{max} ranges between 170 GHz and 138 GHz, respectively.

The mixed signal CMN65 pack included in the TSMC 65 PDK features high resistance resistors, MOS varactors, metal fringe capacitors (MoM), and Metal-Insulator-Metal (MiM) capacitors. The RF components provided by the PDK and used in this work are well described at high frequencies. The models which enable high precision analog and RF designs include 1/f noise model and CMOS RF model. The inductors available (standard, symmetrical and center-tapped structures) attain a relatively high Q, due to the use of thick copper top metals [1]. One of the only disadvantages of this technology is that the minimum RF MIM capacitor value is not smaller than 19.7fF, requiring a series connection to be used.

4.2 Receiver Floor Plan

The receiver floor plan is discussed in this section. The general schematic for the floor plan is given in Fig. 4.1. For the RF input, a Ground Signal Ground (GSG) bond pad is used. For

[1] f_T and fmax measured at V_{GS}=0.6V, for a 40u width transistor
[2] f_T and fmax measured at V_{GS}=0.4V for a 20u width transistor

the output, a Ground-Power-4xLogic (GP4L) bond pad is used. Both bond-pads have 125 μm pitch, with a bond-pad length and width of 70 μm. The Signal pad of the GSG bond pad, is composed only of metal 6 and metal 5, to shield the RF from ground. The other pads contain all the metals for easy contacting. These standard Philips bond pads are compatible with the probe station used in wafer probing. The single Logic bond pads are connected to DC needles supplied within the measurement setup.

There are two separate power supplies: one for the RF and IF amplifier circuits and one for the output buffers. In order to detect the signal, the load represented by the oscilloscope is driven by a pair of buffers implemented with CMOS inverters placed at the output of the IF amplifier. The load is modeled as a 1 MΩ and a 100 pF capacitor. The output buffers are supplied by a separate power supply which draws a maximum of 10 mA, as seen in transient simulations. This current is not included in the link budget derived in chapter 2 since it is not required for the functioning of the front-end.

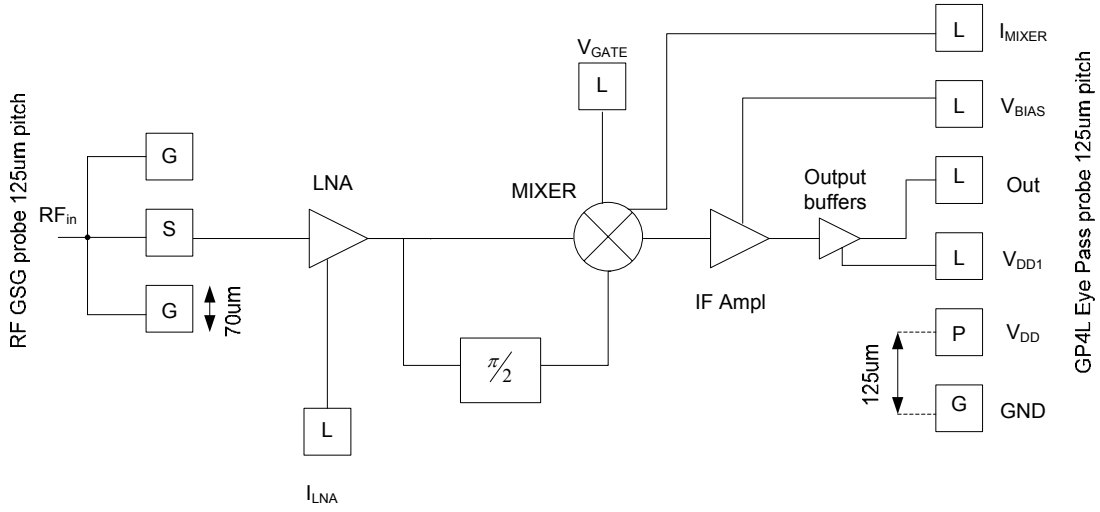


Fig.4. 1 Floor plan for the LNA-detector receiver

The floor plan of the common gate standalone detector is similar, except for one of the Logic bond pads which is removed since it supplied the current to the LNA.

4.3 LNA-Detector Layout

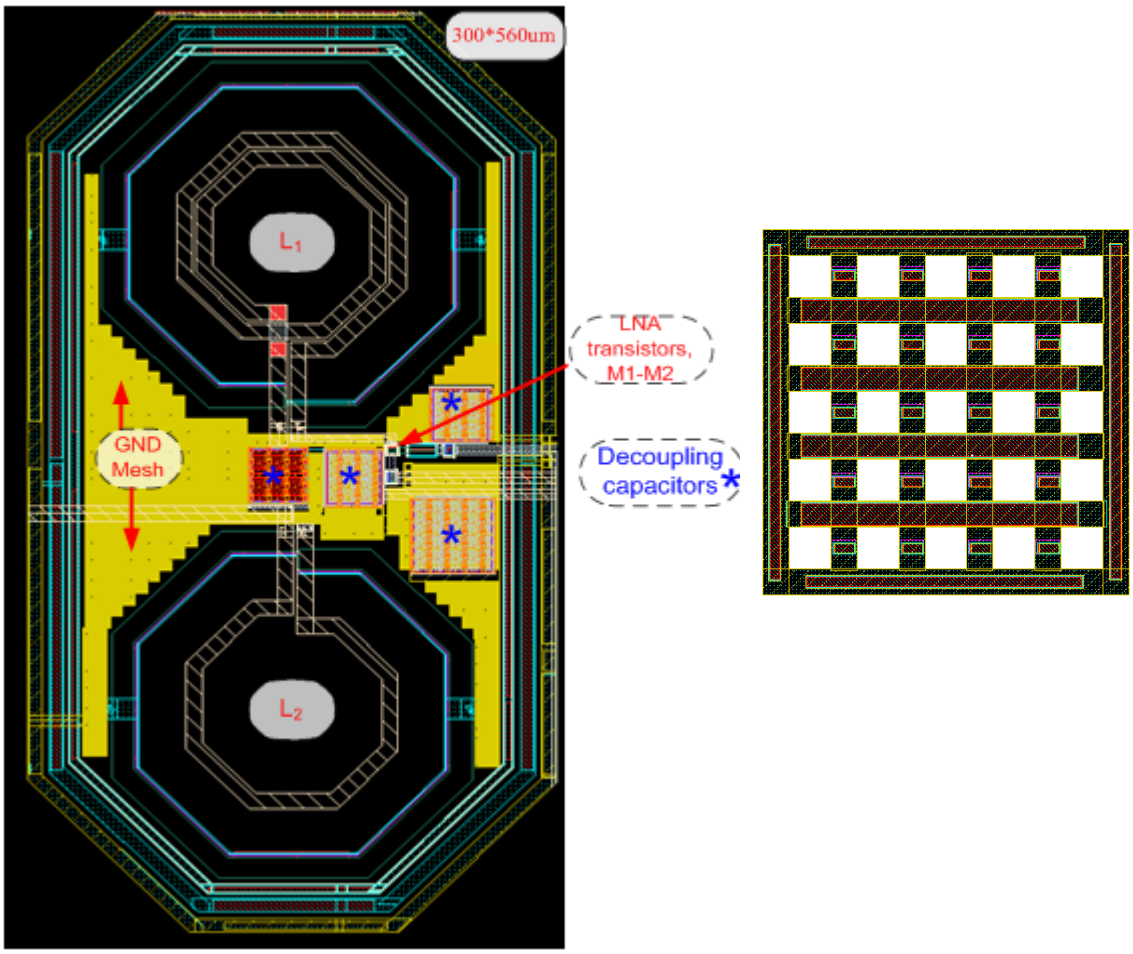
The layout of the LNA-detector is performed first. Since the inductors cover most of the chip area, the layout is focused on fitting them together with the other smaller RF components. The layout of the LNA and the detector are made afterwards.

The LNA-detector receiver includes 4 inductors. To make sure they have no mutual coupling, input matching inductors, L_1 and L_2 from Fig. 3.7, are shielded from the LNA and detector inductors. For this, guard rings are placed around the inductors of the input matching network of the LNA (see Fig. 4.2(a)) The first guard ring connects the underlying N-well to $V_{DD.}$ The second one connects the substrate to ground. The third one is a superposition of metal 1 (M1) and metal 2 (M2) which are connected together to ground. The guard rings ensure that the magnetic field of the inductors of the matching network is contained in the enclosed area and does not extend to the inductors from the LC tank and from the detector. Instead of using wires for the ground connection, which adds impedance, a ground mesh is opted for. The ground mesh provides shielding from the substrate. It provides connections through vias from M1 and M2 to the substrate. Fig 4.2(b) also shows the mesh structure which covers the empty areas around the inductors and provides a ground connection for other components. The mesh connects to the ground bond pads through M1 (blue) and M2 (yellow). The LNA in figure 4.2a measures 300 μm*560 μm.

Figure 4.3 shows the layout of the entire receiver. The chip measures 695 μm*720 μm. The 3.4 μm thick top metal 6 is chosen for the RF signal to pass through. V_{DD} flows through the top metal, DC bias voltages use metal 5 and metal 4.

Power supply decoupling capacitors of 50 pF are placed around the active area. A rule of thumb is that 1 μm of line contributes 0.5pH. Following this rule and adding that V_{DD} runs through the whole length and width of the chip at least once, large capacitance is needed for DC decoupling.

Decoupling the RF from V_{DD} or bias voltages is performed with 500fF or 1pF capacitors (where space permits). The decoupling capacitors are placed close to the active circuit so as not to lose RF signal and to provide a low impedance connection to ground.



(a) **(b)**

Fig.4. 2 LNA layout (a) and ground mesh structure (b)

Fig. 4.3 shows the connection from the input RF signal pad to the input inductors which measures 180 µm. The connection is this long since the inductors are 220 µm large in diameter. Another 180 µm strip line connects the drain of the LNA cascode transistor to the LC tank. The LC tank was chosen to be close to the detector active area such that the detector layout is compact. Modeling and simulations with ADS Momentum™ have been performed for the line and are discussed in Section 4.4. A stack of metals, connected to the ground mesh through vias from metal 6, is placed on either side of the transmission line in order to make it behave like a coplanar waveguide. This arrangement also facilitates the chip tiling process. By covering the empty parts of the chip with a metal stack, chances are diminished that the tiling algorithm will place random metals in sensitive active areas of the receiver.

The inductors in the receiver were chosen with high self resonance frequency and with a high Q. As previously mentioned in Chapter 3, the Q of the LC tank and the detector inductor is 26.8, while the quality factor in the input matching inductors is smaller (4 for the 1.38 nH inductor and 16 for the 460pH one). In addition, the large valued inductor has 2 turns lowering the self resonance frequency to 33.2 GHz. To minimize the inductor size, the guard ring distances were decreased from the standard 50 μm to 30 μm. The changes due to this decrease have been taken into consideration in simulations in Chapter 3. As a last point of concern, all connections to the inductors are maintained through M6 in order to minimize RF losses.

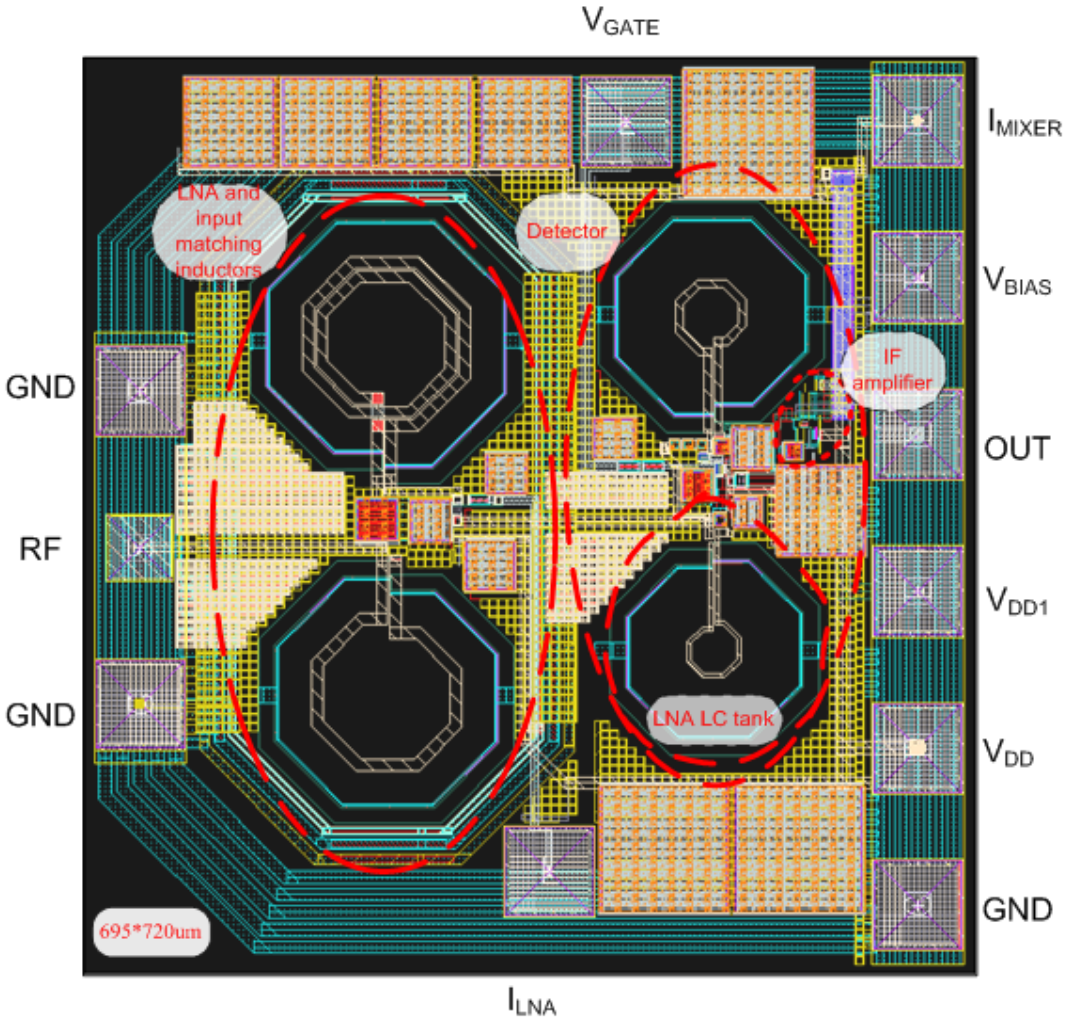


Fig.4. 3 LNA-detector layout

4.4 Common Gate Input Detector

This section presents the standalone detector layout. As mentioned in the Section 3.4 of Chapter 3, this version of the receiver was realized in order to remove any inductor mismatch as presented in Fig.3.34. This version allows testing the functioning of the detector itself, albeit at the expense of 13 dBm more power.

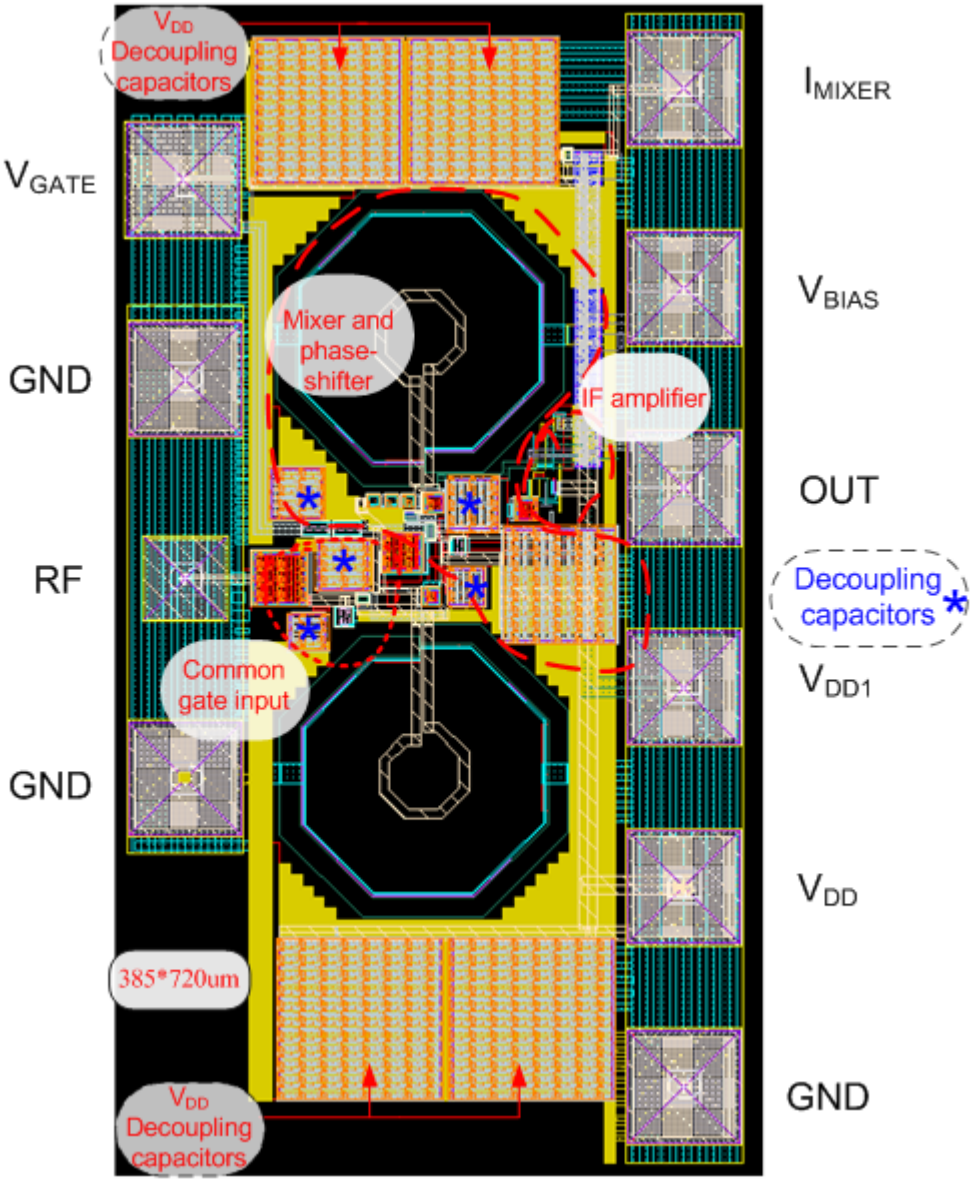


Fig.4. 4 Common gate input detector

The layout for the standalone detector is shown in Fig. 4.4. The chip measures a total of 385µm x 720µm. It is more compact and features very short connecting transmission lines. The phase shifter, mixer, and LC tank are chosen to be very close to each other such as to minimize parasitic capacitance. Simulations showed that due to the detector's sensitivity, small extra capacitance influences the circuit's performance, more specifically the voltage gain and the phase shift which in turn changes the signal amplitude entering the mixer. V_{DD} and the RF signal still flow through M6. DC bias voltages also flow in metal 5 and metal 4. Due to a decrease in chip size, power supply decoupling capacitors are 38 pF instead of 50 pF. RF decoupling capacitors are placed close to the active area, as shown in Fig.4.4.
Both layouts pass DRC (design rule check), antenna effect of MIM capacitors and LVS (layout vs. schematic) checks and are sent for fabrication.

4.5 ADS Momentum™ Simulations

This section discusses the simulations performed on the 180 µm long line connecting the RF input bond pad to the input inductors and the LNA cascode to the LC tank, as seen in Fig. 4.3. The TSMC metal stack characteristics are imported in ADS Momentum. The 180 µm line is drawn and shown in Fig. 4.5. The line is matched at both ports to 50 Ω.

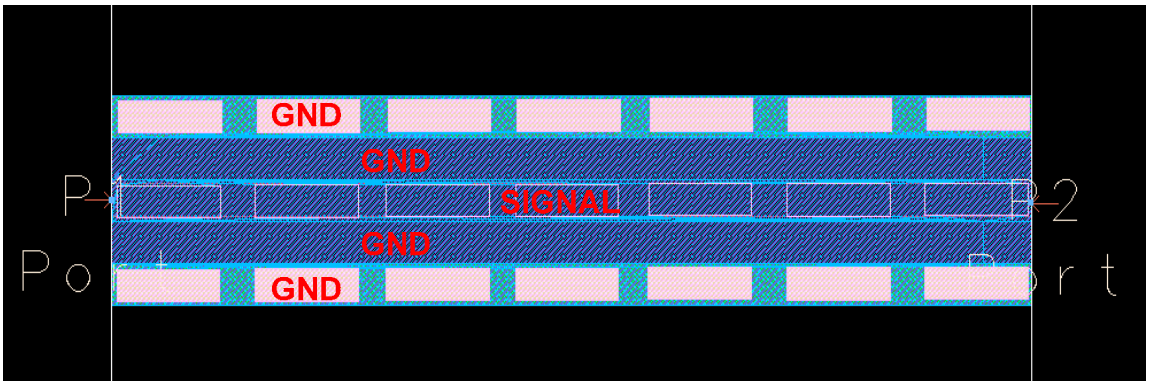


Fig.4. 5 180 µm line in Momentum

The line is designed as a coplanar waveguide (CPW) with the signal flowing through M6. The trace width is 7µm, chosen to be in accordance with the distance from M6 to ground. The width of the ground spacing and the metal stack connected to ground are also 7µm. The metal stack is formed of metals 6 through 1 and connected to each other and to a ground sheet through vias as shown in Fig. 4.6. While defining the layers and their characteristics for the Momentum simulation, the substrate is not included in the definition.

This is because the structure is embedded in the ground plane. By supplying a substrate and specifying its thickness, ground would be moved deeper in the silicon than it actually is.

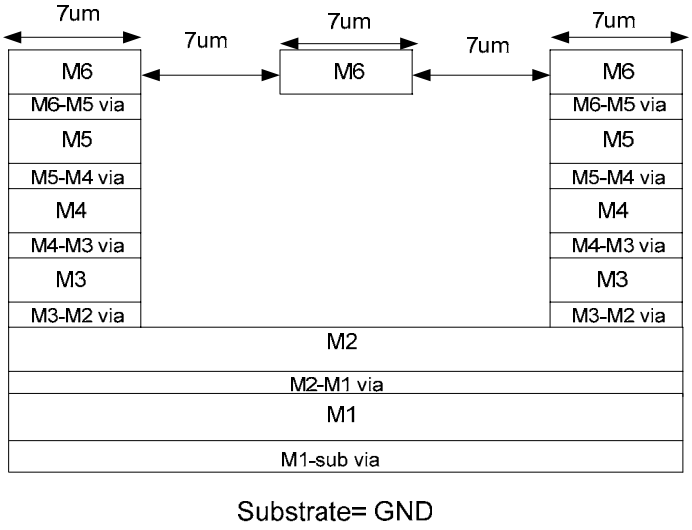
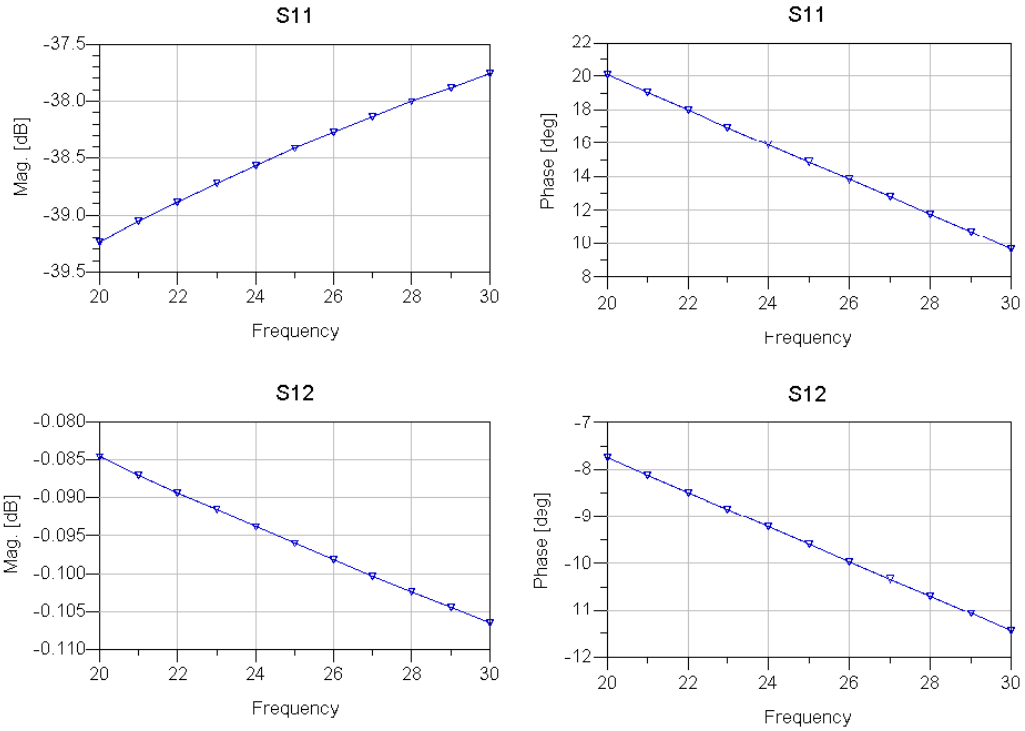


Fig.4. 6 Metal layer stack for Momentum simulation on 180 µm line



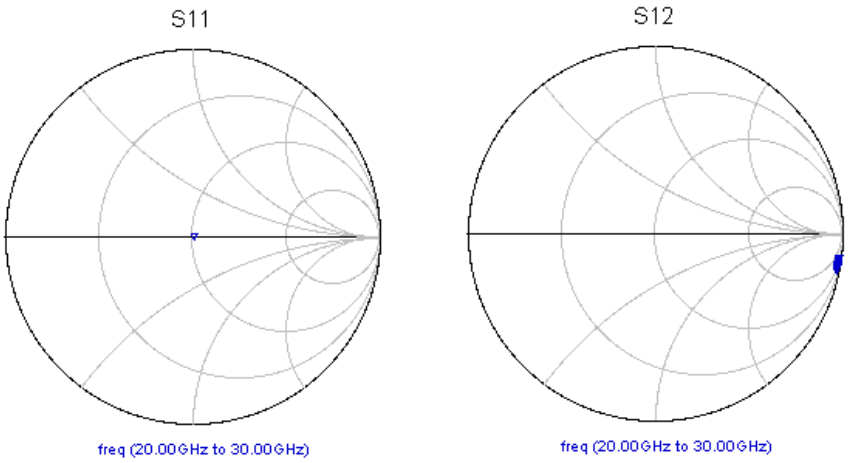
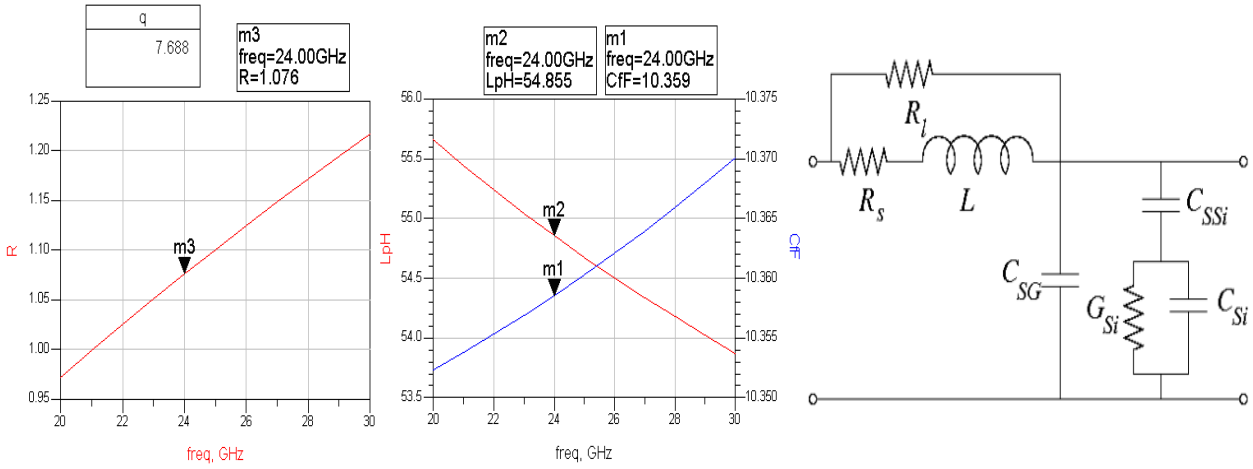


Fig.4. 7 Rectangular and Smith chart view of S parameters



(a) **(b)**

Fig.4. 8 (a) Inductance, capacitance and resistance of 180µm line (b) Coplanar waveguide equivalent circuit [2]

A Momentum simulation is set up to run between 20 and 30 GHz. The results are shown in Fig 4.7-8. Fig. 4.7 shows that the input and output reflection coefficient of the line is less than -38 dB. The losses of the line are also minimal, less than -0.1 dB. The signal undergoes 9º phase shift at 24 GHz as seen by the phase of S_{12}. The Smith chart view shows that the line is well matched to 50 Ω for the whole 10 GHz frequency range. Fig.4.8a shows the inductance, capacitance and Q the line attains. Fig. 4.8b shows the equivalent circuit of the CPW implemented on a silicon substrate, where R_s is series ohmic resistance, R_l, longitudinal current flow in substrate, C_{SG}, capacitance between the signal line and the coplanar grounds, C_{SSi}, capacitance between signal and substrate, C_{Si}, displacement current

flow in the substrate and G_{Si}, perpendicular current flow in the substrate. The line adds an inductance of L=54.8pH with a Q of 7.68, C_{SG} =10.3 fF and Rs=1.076 at 24 GHz.

4.6 Post Layout Simulations

Extra capacitance should also be considered while adding the influence of the line. At the time the chip was taped out, the Assura™ parasitic extraction tool was not available. Therefore, based on [3], calculations were performed knowing what capacitances different metal lines have. In comparison to the ADS Momentum simulations, the calculation method in [3] uses the deducted parasitic capacitances from the Assura™ tool, which gives more realistic capacitance values. Together, the s2p file and the parasitic capacitances from [3] provide a parasitic behavior description in the absence of a functioning parasitic extraction tool. In this work, there are two cases to be considered: the capacitances of metal lines to the ground plate and the capacitance from one metal line to a stack of metals. The first case relates to the intrinsic capacitances metals have to ground. Parasitic extraction is most relevant regarding the metals which carry the signal. In this case, this is M6. According to [3], the capacitance of M6 over a plate of M2 (such as the RF signal flowing over the ground shield) is:

$$C_{M6} = Ca \cdot l \cdot w + 2 \cdot C_f \cdot l \tag{4-1}$$

where Ca=13 aF/μm^2 , the fringe capacitance C_f=55 aF/μm^2, l and w are the length and width of the line. For a 180 μm line, with 7μm width, C_{M6}=34.27 fF.

The second case relates to the fringe capacitance from a metal to a stack of metals. M6 is taken with respect to metal 1-6 wall. The capacitance obtained is given as:

$$C_{fM6} = \frac{C_0 \cdot l}{d + \sqrt{d}} \tag{4-2}$$

where C_0= 0.46 fF and l is the length of the line and d is the distance between the strips. For a 180 μm line, with 7 μm distance to the stack of metals, C_{fM6} = 10.8 fF.

Additionally, extra capacitances are placed at the sensitive nodes of the active part (such as at the phase shifter nodes). The result of these additional capacitances has little effect on the voltage gain, but does influence the phase shifting action. Therefore, the capacitor responsible for obtaining the 24 GHz phase shift is decreased from 96.2 to 93 fF.

The s2p file containing the S parameters of the line along with the previously calculated capacitance results are inserted in the receiver schematic to see the influence.

The additional inductance and capacitance changes the input matching frequency range such that S_{11} <-10 dB from 22.08 to 27.4 GHz. The resonance frequency of the tank decreases by 1.78 GHz to 22.35 GHz while the gain increases by 7 dB.

To compensate for these added parasitics, the inductors in the input impedance matching network are changed to L_1=410 pH (Q=17.6) and L_2 =1.52 nH (Q=3.84). The tank components are changed to L_{tank}=269 pH (Q=26.2) and C_{tank}= 54.5 fF. With these changes, the voltage gain is maximum at 24 GHz giving 21.2 dB. The frequency range for which S_{11}<-10dB extends from 20.91 to 27.15 GHz. The amplitude of the signals at the mixer gates decreases to 17 mVpp from 24 mVpp and to 8 mVpp from 16.6 mVpp. Therefore, the downconverted output also decreases to 300 uV. This implies that the input power has to be increased to -40 dBm in order to have the same result as seen in Chapter 3.

Changes to component values in the standalone detector are only made to the capacitor C_2 from Fig.3.23, which is responsible for the 90º phase shift. It is changed from 96.2 to 93 fF.

In view of these modifications, the chips are sent for tape out.

Before the chips returned from fabrication, the Assura™ parasitic extraction tool started functioning. Nevertheless, it did not produce correct results. It computes the parasitic behavior by taking twice the capacitance value of the MIM capacitors.

Table 4. 1 Schematic vs. Post layout simulations results

Receiver versions		Voltage gain (dB)	S_{11}<-10dB range (GHz)	90º Phase Shift at	Freq (GHz)	Input power (dBm)	Detector Output (mV)
LNA-det.	Schem.	22.14	20.5-26.4	24GHz	24	-50	1.81mV
	Parasitic Extr.	20	17-22	15.48 GHz	17.36	-50	350uV
CG - input det.	Schem.	9.6	10- 40	24GHz	24	-37	2mV
	Parasitic Extr.	8.46	14.73-15.5	15.48 GHz	15.19	-37	2.2mV

The results of parasitic extraction in comparison to the schematic simulations for both receivers are reported in Table 4.1. The table shows a dramatic decrease of operating frequency. As mentioned in Section 3.3.3.1 of Chapter 3, the capacitance which sets the operating frequency is the sum of the gate to source capacitors and the tank capacitance. If the tank capacitance is doubled, the resonance frequency already shifts to 19.44 GHz. The difference to 17.36GHz is then 2 GHz. The other important issue is the phase shift. According to Table 4.1, the 90º phase shift is obtained at 15.48GHz. Due to the error in Assura, the coupling capacitor (C_K) now changes to 13.14fF, the gate to source capacitance of the lower FET remains the same and the phase shifter capacitance doubles. This leads to a resonance frequency of 18.3GHz. This is 3 GHz higher than reported in Table 4.1. Considering that the influence of the line is not taken into account in the post layout simulation, it is expected that the additional inductance changes the respective frequencies. The line will add also losses.

The detector output voltage of 300 uV is obtained with an input signal of -50 dBm 17.36 GHz. The LC tanks resonate at different frequencies as observed from Table 4.1. A signal with a different frequency than the one for which 90º phase shift is achieved does not produce a high amplitude signal at the lower FET mixer input. Thus, although the signal at the upper FET of the mixer is acceptable, the signal at the lower FET is low; therefore, the output differs from the result achieved in schematic simulations.

The frequency bandwidth for which S_{11} <-10 dB decreases to 4.9 GHz. Minimum reflection occurs at 17.74 GHz. The long connection at the input is expected to increase this frequency range since it will add inductance.

Table 4.1 also shows the post layout simulation results of the common gate input detector. The operating frequency shifts lower to 15.2 GHz. It is approximately the same frequency at which there is a 90º phase shift.

The detector output voltage is obtained with an input signal at the 15.2GHz operating frequency and with -37dBm input power. The result is slightly higher than obtained in schematic simulations.

The biggest difference is observed in the S_{11} response. As presented in Section 3.4 of Chapter 3, the input reflection coefficient is less that -10 dB over a very wide range with minimal reflection occurring at 24 GHz. Parasitic simulation reveals that the range greatly

decreases to only 1.5% of the schematic simulated bandwidth. Investigations showed that the main component which deteriorates input impedance matching is the bond pad capacitance. Fig. 4.9 shows that adding at least 60 fF to the input of the detector dramatically decreases the reflection coefficient by 10 dB. The bond pad capacitance was not included in simulations when the common gate input was designed.

Parasitic extraction was also performed on the IF amplifier layout block. The result is similar to the schematic simulation with 21 ns delay between the pulses.

This section concludes the discussion about the physical layout and post layout simulations. The layout of both chips was described and some features were highlighted. Momentum simulations for the 180µm line were presented and the effect of the line is included in post layout simulations. The results of RCX simulations on both chips were compared to the schematic simulation results. The measurement results of the fabricated receiver ICs will be presented in the next chapter.

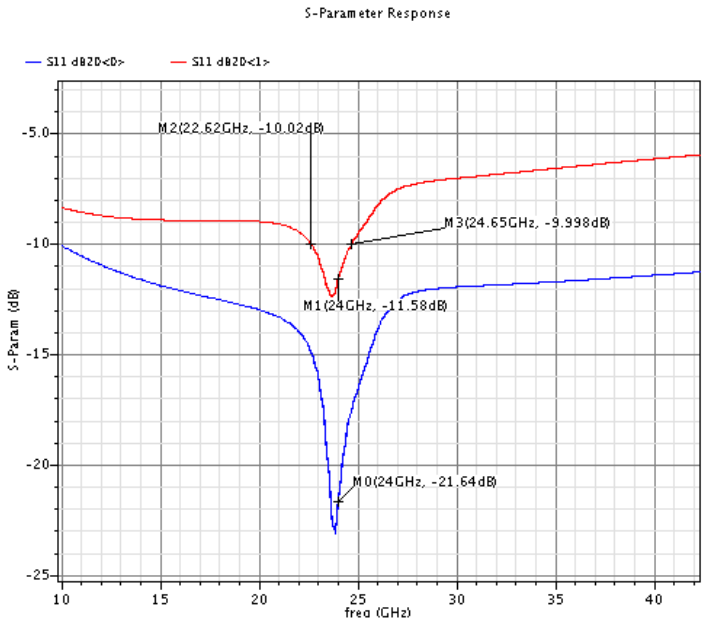


Fig.4. 9 Input impedance matching with (red line) and without bond pad capacitance (blue)

References

[1] TSMC "55 and 65 Nanometer Process Technology", April 2008, last retrieved on 10.09.2008 from http://www.tsmc.com/download/english/a05_literature

[2] B. Frank, "Transmission Line Design on Silicon" ELEC 853 course, Queens University, 2007

[3] P. van Zeijl, "TSMC 65nm extraction: Calibre and Assura" February 2008, Philips Research

Chapter 5. Measurement results

This chapter presents the measurement results obtained from testing the receiver. Two circuits were designed for tape out: the detector itself as described in Chapter 3, Section 3.4, and the LNA and detector, as described in the same chapter in Section 3.3.

5.1 24 GHz WSN Receiver Measurement Considerations

Circuit micrographs of the two chips are shown in Fig 5.1 (a), (b). Fig.5.1 (a) shows the complete receiver: the LNA and the detector, as presented in Fig.3.34-schematic view and Fig. 4.3-layout view. Fig. 5.1 (b) shows the detector with the common gate input stage as presented in Fig.3.35-schematic view and Fig. 4.4-layout view. In both cases, the input RF is supplied through a single-ended GSG RF probe (Ground-Signal-Ground).

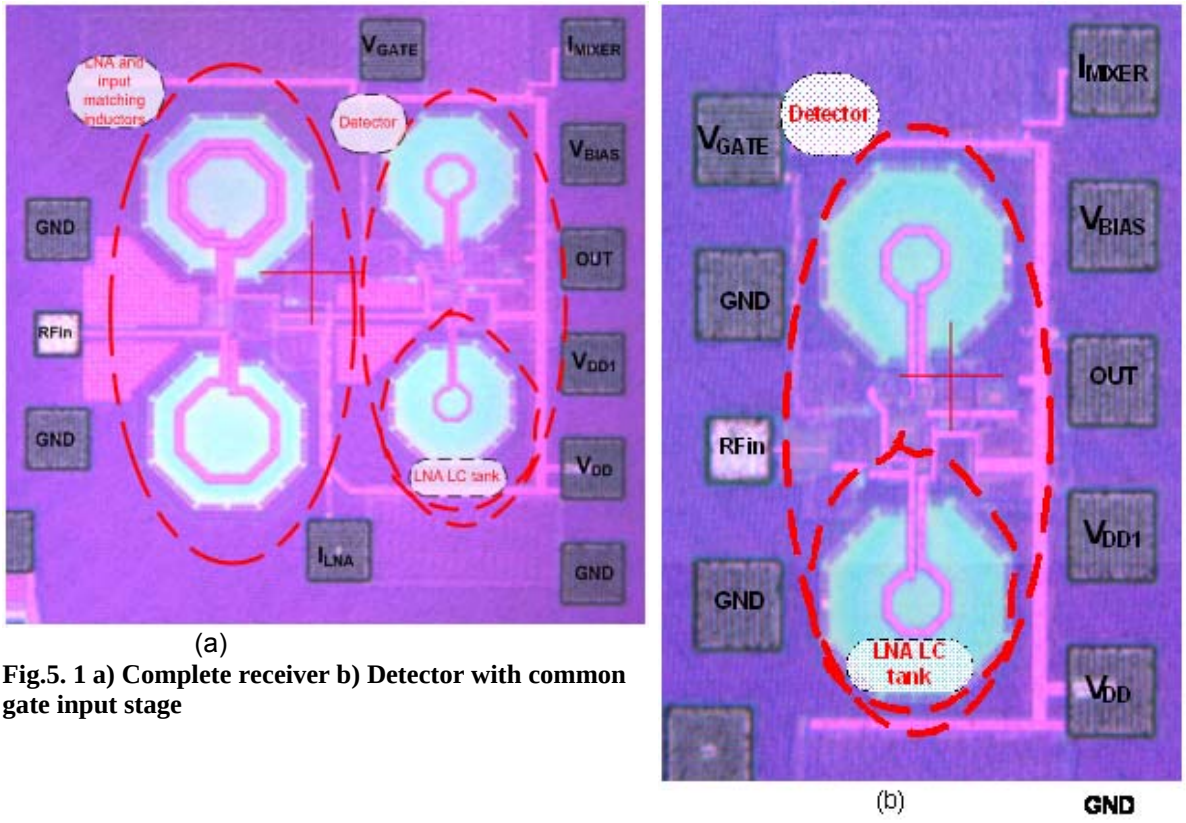


Fig.5. 1 a) Complete receiver b) Detector with common gate input stage

The Eye-Pass GP4L probe (Ground, Power, 4 times Logic signal) supplies the DC biasing. The output signal is also taken from the Eye-Pass probe.

The measurement set up is made so as to test both the chips with two switching tones for OFSK. For this purpose, a high frequency multiplexer was intended to be used which takes two tones and a 5 MHz pulse which switches them on or off. Due to the fact that there was a delay with the delivery of the multiplexer, the RF input signal was generated with a signal generator that could produce on-off keying signals and FM signals.

The design of the chips allow for a limited set of measurements to be performed. Since the detector output is a couple of mV, a bond-pad connection cannot be made at the mixer output. The bond-pad and the additional probe would load the node. Therefore, the detector is a black box, whose performance can be analyzed only through the output of the IF amplifier. It is expected that for the operation frequency and for a certain input power, a series of digital 1s and 0s will be seen at the output pin. Moving further away from the operation frequency should induce an output response of distorted, blurry or noisy bits. The output can be judged based on the bit rise and fall time, the duty cycle and by its general aspect. A clear signal indicates that the detector output voltage is high, while a blurry one indicates that the output is lower. The receiver can be also tested for sensitivity and input matching.

5.2 Common gate input-detector measurements

The common gate input-detector is measured first. The measurement setup is described in Fig. 5.2. In this figure, the ground pad is not seen. The RF signal is fed from the Agilent PSG Analog Signal Generator E8257D through a single ended GSG probe. The output is taken from the GP4L probe and inputted to the Agilent DS06034A oscilloscope. DC biasing is provided through the other bond-pads. The two power supplies, V_{DD} and $V_{DD1,}$ which supply the receiver and the output buffers respectively, are supplied via the Agilent B1500A Semiconductor Device Analyzer and via the Hewlett Packard E3631 Triple Output DC power supply. The current through the mixer, I_{MIXER}, is supplied by the Keithley 220 Programmable current source. The DC gate voltage of the mixer, V_{GATE}, is given by the same Agilent B1500A Semiconductor Device Analyzer. The bias voltage for the IF amplifier, V_{BIAS}, is supplied by the Hewlett Packard E3631 Triple Output DC power.

When DC biasing is provided, before the RF is turned on, an unexpected oscillation is detected in the output. A detailed discussion on the cause of oscillation is provided in Section 5.4. Unfortunately, due to this oscillation, higher levels of input power need to be applied to the receiver for detection of signal.

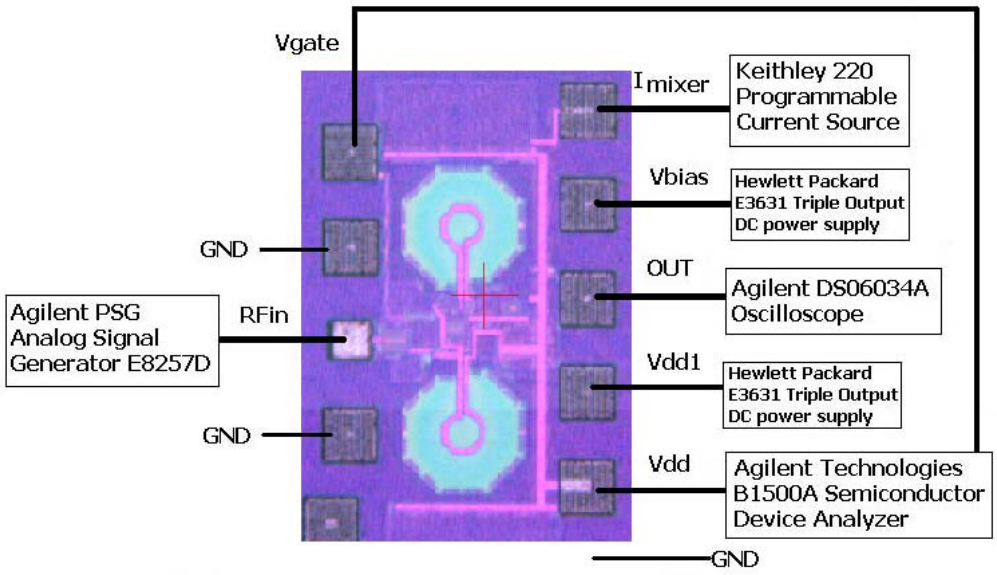


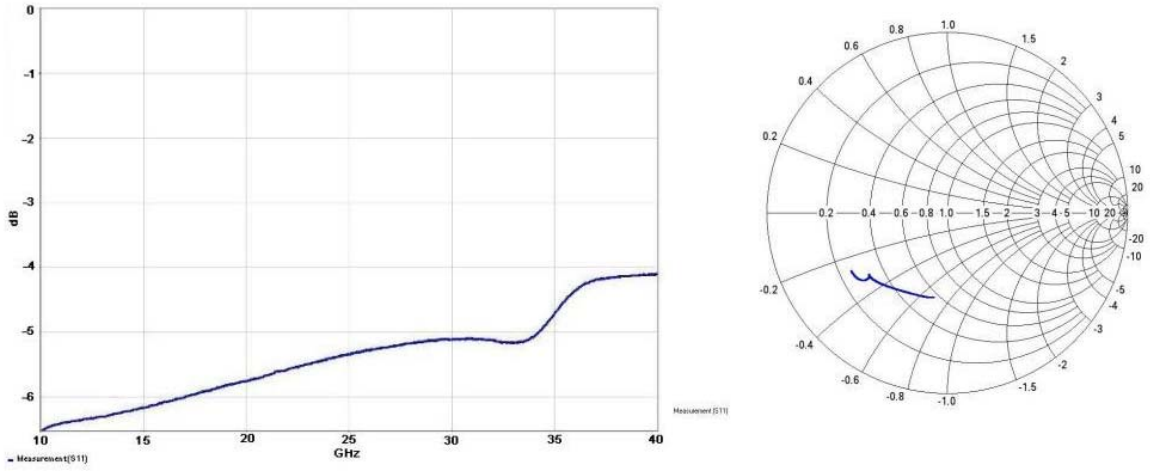
Fig.5. 2 Measurement setup for common gate input detector

5.2.1 Input impedance and sensitivity measurement results

Input matching was tested for the common gate input detector by means of the Agilent PNA Network Analyzer E8361A. The result of this test is reproduced in Fig. 5.3 (a), (b). Fig. 5.3 (a) shows the S_{11} range is above -10 dB for the whole frequency range. Parasitic extraction simulations provided in Table 4.1 and Fig. 4.9 are in accordance with this result though. This loss is mainly due to the capacitive impedance presented to the receiver input by the bond pad, as discussed in Chapter 4, Section 4.5.

The chip has been tested with both OOK and FM signals. From Section 3.3.5 in Chapter 3, it is known that the detector output is higher when receiving OOK modulated signals. For the FM signal, the frequency deviation of the signal is not as high as the difference used in the simulation of the receiver. A deviation of 64 MHz is the maximum produced in comparison with 400 MHz used in simulation. Another limitation is that the maximum FM rate (which sets the data rate) is 1 MHz. The receiver can detect both OOK and FM modulated signals. In the following, only results with FM modulation are provided since

measurements with OOK signals lead to very similar results.

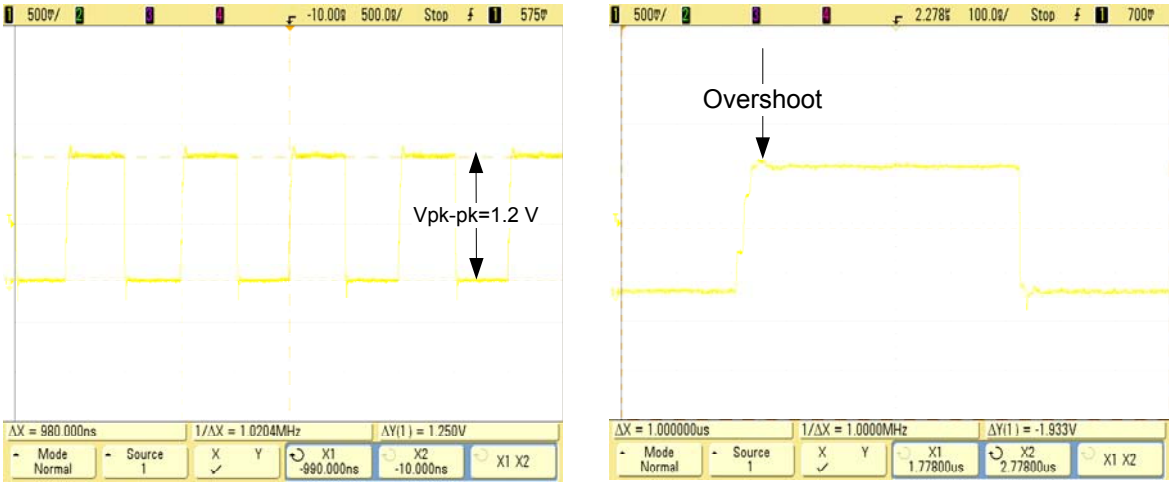


(a) **(b)**

Fig.5. 3 Detector input reflection coefficient in (a) rectangular and (b) smith chart view

The DC biasing points are: V_{DD1}=1.2 mV, V_{DD}=1.2, V, $I_{MIXER=}$300uA, V_{GATE}=600mV and V_{BIAS}=495 mV. The value of V_{BIAS} can range from 300 to 900mV. The IF amplifier functions for this voltage range even though it was designed at 600 mV.

Fig. 5.4 shows the output of the receiver when tested with an FM modulated signal. The FM deviation is 64 MHz while the FM rate is 1 MHz. The output is quite clear, with an overshoot at the transition point between a digital 1 and 0. The output voltage measures 1.2 V. The 1 MHz data rate and the 50% duty cycle are also observed.



(a) **(b)**

Fig.5. 4 Output signal (a) with zoomed in view for FM modulated input (b)

Fig. 5.5 shows the rise and fall time of the output signal. It can be seen that the rise time is 26ns, while the fall time is very small, 1.6ns.

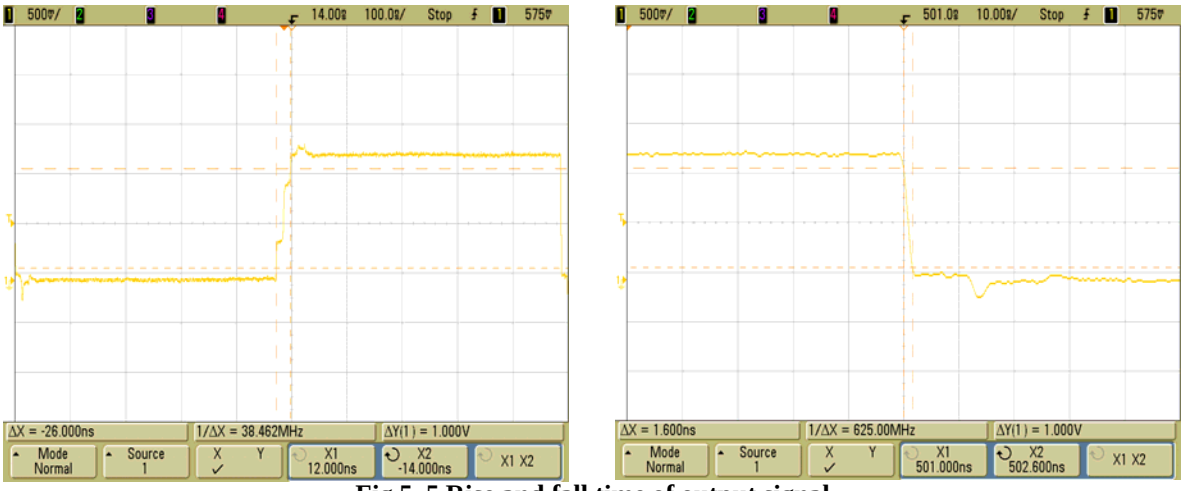


Fig.5. 5 Rise and fall time of output signal

With an FM modulated signal, the sensitivity of the receiver can be better characterized. The frequency at which detection worsens can be more readily seen, since the FM deviation is small in this case and since the detector output is smaller than with an OOK signal. The receiver provides an output for a wide range of frequencies, from 15 GHz to 28GHz. In the range between 22 and 23 GHz, the output is clearest indicating the detector output voltage is high. The results provided in Fig. 5.4 and 5.5 are taken at 22.7 GHz with a signal power of 18 dBm. This high power is needed to overcome the above mentioned oscillation. At an input power of 14 dBm there is no more detection. At the border frequencies of 15 and 28 GHz, the output becomes distorted and fades into the characteristic oscillation. The large frequency range is not expected in comparison to simulation results. The detector should not detect signals lower than 18 GHz even if parasitic simulation results from Chapter 4 Table 4.1 are taken in consideration. The amended resonance frequency of the phase shifter according to Table 4.1 is 18.3 GHz. This would indicate that below and above this value, a reasonable swing can still be obtained for the mixer lower FET of Fig. 3.14 (a). Nevertheless, the upper bound of 28 GHz is unexpected and can only be explained by the high input power level that provides high input signals to the mixer, of around 0 dBm. This value induced the highest conversion loss for the dual gate mixer as shown in Fig. 3.18.

5.3 LNA-Detector receiver measurements

The measurement setup for the full receiver is the same as for the common gate input detector, as shown in Fig.5.6. An extra bond-pad supplies current for the LNA biasing by means of a Keithley 220 programmable current source supplying 450 μA.
Upon providing DC biasing, the same 5 MHz oscillation is detected in the output.

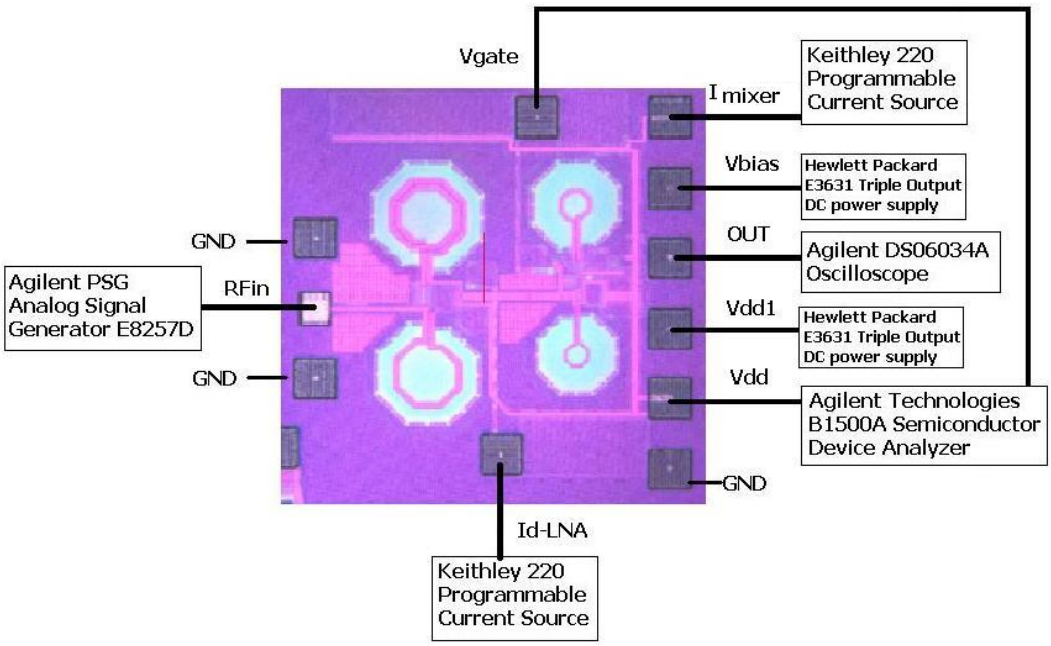
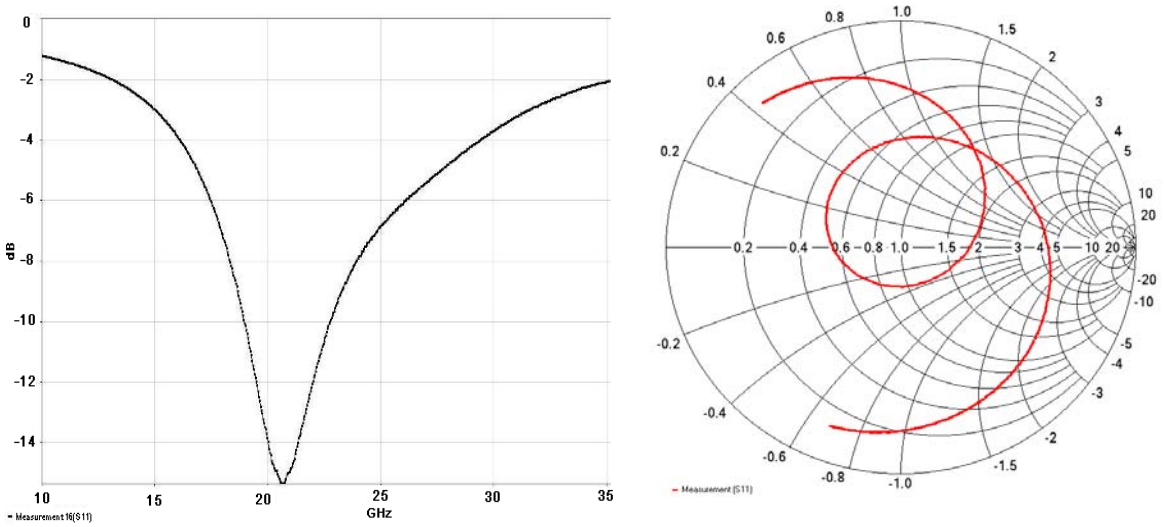


Fig.5. 6 Measurement setup for the LNA-detector

5.3.1 Input impedance and sensitivity measurement results

Input matching was tested for the LNA-Detector receiver, the result of which is reproduced in Fig. 5.7. Input matching was tested with 300 and 400 μA current through the LNA. Fig. 5.7 shows the result with 400 μA. For 300 μA, S_{11} shifts 100 MHz lower. The S_{11} characteristic shown in Fig. 5.7 (a) is more similar to the simulation results as shown in Fig.3.16 (b) than to the parasitic extraction performed in Chapter 4, which does not include the inductive effect of the 180 μm input line. Fig. 5.6 shows an input matching of more than -14 dB at 20.6 GHz, and an S_{11}< -10 dB over the frequency range of 18.9 to 22.7 GHz. In comparison to simulations, the frequency range is shifted 3.1 GHz lower from 23.7 to 20.6 GHz and the frequency range where S_{11}<-10dB is decreased from 6 to 3.8 GHz.



(a) (b)

Fig.5. 7 Complete receiver input reflection coefficient in a) rectangular and b) Smith chart view

The complete receiver was tested with OOK and FM signals. For FM signals though, the receiver cannot recognize the RF anymore. The cause can be that due to parasitics, the 90º phase shift occurs at a frequency different than the one where the LNA provides the highest amplification. The different phase shift also implies a lower signal to the lower FET of Fig.3.14 (a). Another reason could be due to the restricted 64 MHz FM signal deviation which is insufficient for producing a reasonable detector output voltage. In the following, results with OOK modulation will be provided.

The DC biasing points are: V_{DD1}=1.2 V, V_{DD}=1.2, V, $I_{MIXER=}$300 μA, I_{LNA}=450 μA V_{GATE}=600 mV and V_{BIAS}=618 mV. Fig. 5.8 shows the output of the receiver when tested with an OOK modulated signal. The pulse width is 1 MHz.

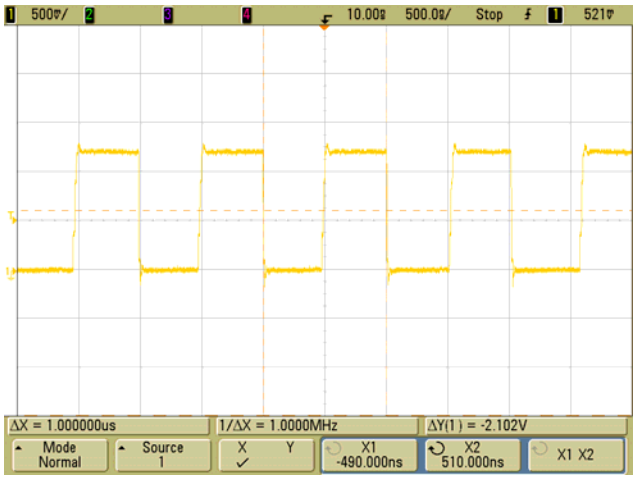
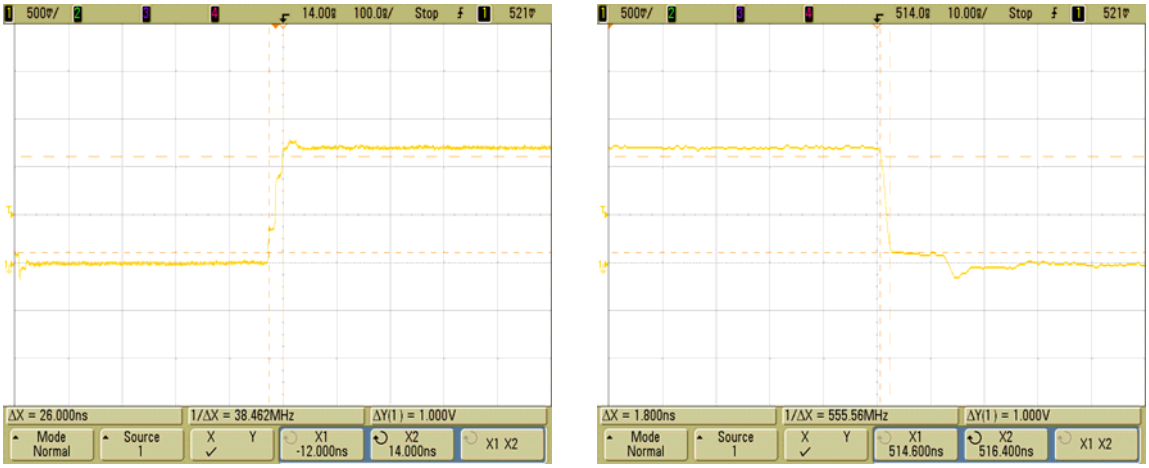


Fig.5. 8 Output signal for OOK modulated input

Fig. 5.9 shows the rise and fall time of the output. The rise time is 26ns, while the fall time is 1.8ns, which is very similar to the output of the standalone detector.



(a) **(b)**

Fig.5. 9 (a) Rise and (b) fall time of output signal

As with the standalone detector, the receiver provides an output for a range of operating frequencies, from 17 to 25 GHz. Upon sweeping the frequency, it was noticed that the output is clear between 19-23 GHz. The results provided in Fig. 5.8 and 5.9 are taken at 21.8 GHz at an input signal power of -1 dBm. The receiver sensitivity reaches a minimum of -8 dBm, after which there is no more recognizable output. The sensitivity increases in comparison to the standalone detector due to the 20 dB LNA gain. In comparison to the receiver sensitivity derived in Fig.3.21 which showed -50 dBm input power, the increased input power is needed in measurements to suppress the unwanted oscillation.

The measurement results provided in the last two sections can be subject to some criticism. Although there is a detectable output, the input power is so large that linearity concerns appear. It is not clear whether the LNA in the complete receiver front-end acts like a switch or if it still amplifies linearly. For this reason, another set of measurements was performed. Due to the existence of the oscillation, input power has to be greatly increased in order to detect the RF signal. It is found that the oscillation can be reduced by limiting the power supply of the output buffers to 650 mV. This increases sensitivity to around -20 dBm for the LNA-detector. Measurements are taken with an OOK modulated signal, by varying the

pulse rate, pulse width, frequency at which the detector is more sensitive, and input power. The DC biasing points are: V_{DD1}=650 mV, V_{DD}=1.2 V, I_{MIXER}=400 μA, I_{LNA}=450 μA, V_{GATE}=600 mV and V_{BIAS}=600-700 mV. The mixer current as well as the LNA current is increased from previous measurements. The results are reported in Table 5.1.

Table 5. 1 LNA-detector results with OOK modulated signal

Sample	Pulse rate (μs)		Pulse width (μs)		Frequency (GHz)		Sensitivity (dBm)	
1	Worst case	Best case	Worst case	Best case	Worst case	Best case	Worst case	Best case
2	1.56	2.62	0.77	1.6	19, 25	20-24	-22	-15
3	1.5	2.42	0.64	1.11	18.7, 24.9	19-23.8	-21	-15
4	1.62	2.39	0.6	1.27	18.9, 24.9	19.8-22.6	-20	-15.6
5	1.63	2.83	0.5	1.46	18.9, 23.8	20.5-22.5	-21	-14.8

Table 5.1 shows results in the worst case, at detection limit and in the best case, when the signal's aspect is best, as defined in Section 5.1. Table 5.1 shows that the receiver works best with a data rate ranging from 3.5 to 4.2 MHz and worst with 666 kHz. This is in accordance to the result of Fig. 3.37 showing the AC behavior of the IF amplifier. The figure shows at what frequency the IF amplifier attains the highest gain, which is in the range of the data rates exhibited above. The pulse width shows an approximately 50% duty cycle. As in the previous measurements, the frequency at which the receiver is most sensitive ranges from 19-20 GHz to 23- 24GHz. This is also acceptable considering the parasitic extraction tools predicted a worse scenario. The frequency at which the signal is clearest is at 22.7 GHz. The input power decreases due to minimizing $V_{DD1,}$ which decreases the oscillation. This has an influence on the measured signal: since the current flowing is limited by the reduced power supply, it is not enough to charge the capacitive load. Therefore, the output is no longer a pulse. Also, the amplitude decreases to 300 mVpk-pk since the output buffers have limited swing. Nevertheless, while the sensitivity

has been improved, viable measurements have been provided which prove that the receiver functions.

5.4 Oscillation Discussion

As mentioned in the previous sections, there is an unwanted oscillation when DC biasing is turned on and the RF is not switched on. This section provides some reasons for its occurrence.

The oscillation frequency is 5 MHz. A first possibility for its occurrence is due to improper power supply decoupling for low frequencies. The IF amplifier provides 55 dB gain and is sensitive to signals on the order of a couple of mV. If any ripple is present on V_{DD} the IF amplifier detects it and starts operating. This unwanted behavior was not tested for in Chapter 3. Even though the Power pin (connected to V_{DD}) on the GP4L probe has a capacitor on the order of 50 nF, there is still a cable connecting the GP4L probe to the chip. As a rule of thumb, 1 mm line length adds 1 nH. Fig. 5.10 shows the addition of inductance of the GP4L probe to the chip. The probe can add an inductance of around 100 nH, which, coupled with parasitic capacitance, would cause the oscillation to start. The oscillation has been recreated in simulations by placing a 45 pF capacitor between V_{DD} and the input of the IF amplifier along with an inductance of 100 nH on the V_{DD} line.

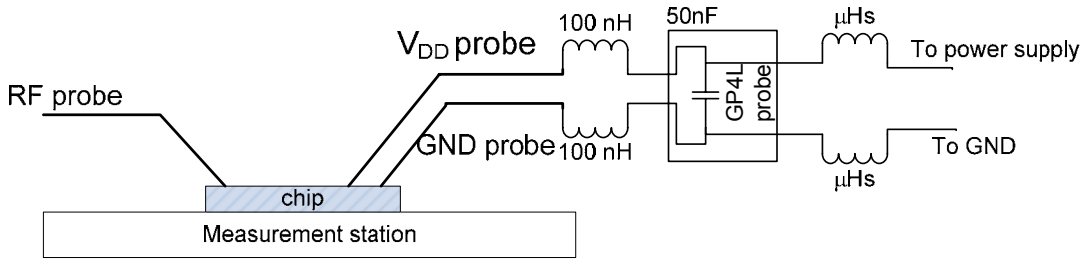


Fig.5. 10 Equivalent circuit of measurement setup

Another possibility for the oscillation occurrence is due to improper V_{DD1} decoupling. Unlike the power supply pin from the GP4L probe, V_{DD1} is neither decoupled on chip nor on the probe itself. Again, due to the inductance added by the long cable connecting the pin to the chip and parasitic capacitance, the low frequency oscillation would occur.

A last possibility is that the IF amplifier is unstable. Even though the phase margin was simulated to be 70º, added phase from the folded cascode could make the amplifier unstable or from feedback from parasitic capacitive coupling in layout.

Each of these possibilities was investigated. For examining V_{DD} decoupling, a 22nF SMD capacitor was mounted on chip through bond-wiring, as shown in Fig.5.11. Measurements with this capacitor revealed that the oscillation was not suppressed.
For further investigations to sustain this assumption, the RF input of the LNA-detector chip is connected to the Agilent E4407B ESA-E Series Spectrum Analyzer. As a first test-case, DC voltages and currents are supplied. The spectrum analyzer shows that the oscillation is fed back to the input of the front-end and detected with the Spectrum Analyzer, at 4.96 MHz, at -61dBm power level. By decreasing V_{DD1}, the oscillation is diminished until the point it vanishes when this power supply is 550mV. This is a critical point in the buffers since the threshold to where they start operating is close to 600mV, as given by V_{BIAS}. A second test-case is when V_{DD1} is completely switched off and other DC bias currents and voltages are on. There is no oscillation detected on the Spectrum Analyzer. This point is an indication that the IF amplifier and V_{DD} decoupling are not the cause of the oscillation. Had the IF amplifier been the cause, the oscillation would have been detected in the spectrum analyzer. These conclusions lead to the belief that the output buffers cause the oscillation.

A third test-case is performed by switching off the current only for the mixer and only for the LNA, while letting all other blocks functioning including the power supply of the output buffers. By switching off the mixer current, the oscillation was suppressed. When the mixer current is switched off, but V_{DD} is on, the voltage at the IF amplifier input is equal to $V_{DD.}$ By supplying a DC voltage different than ground or V_{DD} at the IF amplifier input, which in turn sets a voltage at the gates of the output buffers, these pass their DC threshold. This starts the oscillation. The reason for the oscillation can be linked to either V_{DD1} or ground connection.

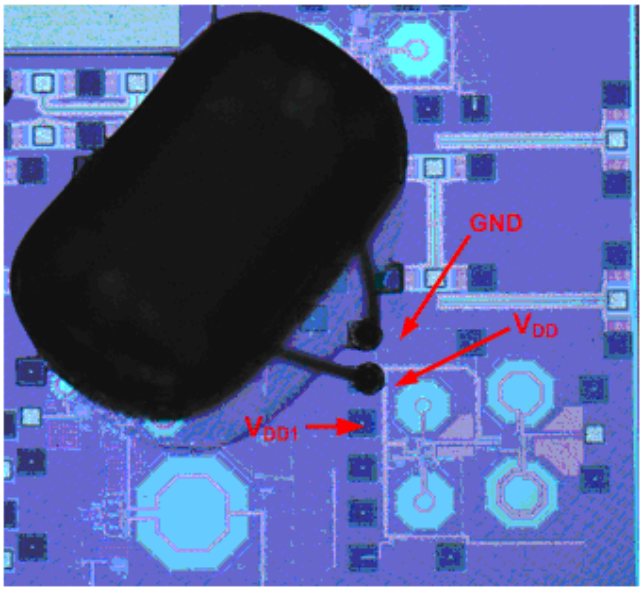


Fig.5. 11 SMD capacitor wire-bonded on chip

To test whether the oscillation is caused by V_{DD1} or the ground connection, another 22nF SMD capacitor was mounted on chip through bond-wiring, for V_{DD1} decoupling. The experiment shows that the oscillation is still not suppressed. This indicates that the ground connection is the cause. The output buffers can consume 10 times more current than the RF circuit. The load represented by the oscilloscope and the cable connecting to it may be more than 100 pF which, when charged in 10 ns, would result in a peak current as high as 10 mA. If any of the wires (either outside cables or on chip wires) conducts current, the voltage drop over ground or the power supply is quite high. For a resistance of 30 Ω and 10 mA, the voltage is 300 mV. The oscillation could be started by switching on the power supply or any interference. The high gain of the IF amplifier also contributes to amplifying any interferences.

The ground is common to all chip blocks as all of them are connected to the same ground mesh, as shown in Fig. 5.12 (a). Once there is a voltage drop on the ground, all circuit blocks sense it. Therefore, circuit blocks see different reference voltages. A solution to this would be to employ the so called ground “star connection”, as shown in Fig. 5.12 (b).

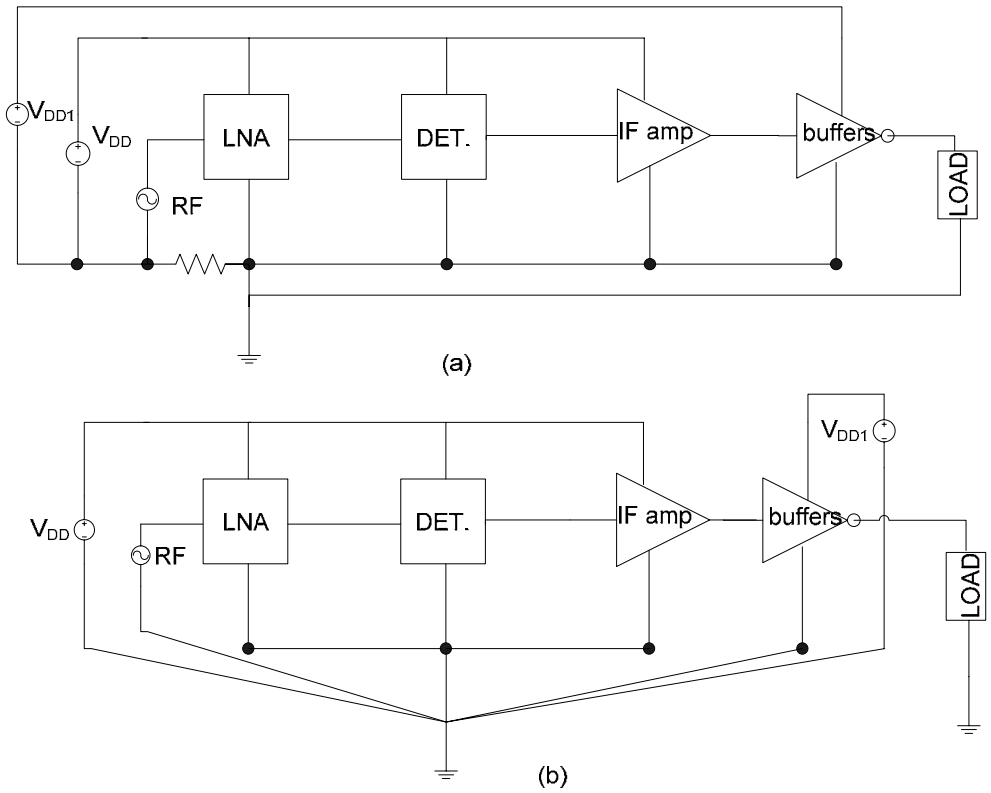


Fig.5. 12 (a) Distributed ground connection (b) star-ground connection

This section concludes the discussion about the measurement results of the fabricated ICs. Both ICs detect the RF signal and produce a pulse at the output. When the DC biasing point is set, there is an unwanted oscillation occurring at the output. Due to this oscillation, higher input power is required to test chip functionality. The possible reasons for the oscillation have been investigated and a systematic ruling out of causes has been performed. The circuit block causing the oscillation was found to be the output buffers. The next chapter presents the summary and conclusions of this thesis and provides recommendations for future work.

Chapter 6. Summary and Recommendations

The front-end designed in this thesis is intended for low power, low cost applications such as WSN. The receiver is designed in CMOS 65 technology functioning at a frequency of 24 GHz, employing the OFSK modulation scheme and attaining a data rate of 5 Mbps. The main design goal in this thesis was to simplify the receiver architecture in order to obtain a current consumption of maximum 1 mA.

For the reduction of power consumption, a simplification of frequency translation architectures has been employed. Among the architectures considered, the direct conversion architecture is selected since it fits the requirement of low power and simplicity. For downconversion, the classical quadrature downconversion RF blocks are not used, since they consume too much power. Instead, FM detectors are reviewed and the quadrature detector is selected for implementation. It has the advantage of simplicity, and consuming a DC current of 400 μA.

The design and implementation of the front-end are treated in Chapter 3. The detection principle is derived first, followed by the presentation of the receiver architecture. The double-stage front-end achieves in simulation the required performance of detecting a 24 GHz signal at -50 dBm input power with 1 mA DC current. By multiplexing 2 signals with a 400 MHz frequency deviation, the receiver can correctly demodulate the information into a stream of digital bits.

The layout of the receiver is performed in the CMOS 65 technology. Two versions of the receiver are sent for tape-out: the LNA-detector which is the complete receiver, and the detector with a common gate input. The second version is designed to provide a way to measure the functioning of the FM detector alone.

The measurement results of the 2 chips are considered in chapter 5. The receiver detects the RF signal and operates around 22.5 GHz best. Since the high frequency multiplexer was not delivered at the time measurements were performed, the input is provided by internally modulated OOK and FM signals of the signal generator. The generator has several

limitations among which a limited 64 MHz frequency deviation and a limited 1 MHz data rate, which hinders the correct evaluation of the receiver's performance. Furthermore, upon setting the DC biasing points, an unwanted oscillation occurs, which demands more RF input power in order to demodulate the RF signal. Several attempts to stop the oscillation have been made: an SMD capacitor has been wire-bonded between the power supply and ground, and, in a further step, between the output buffers' power supply and ground. The ruling out of possible causes lead to the conclusion that the output buffers ground connection is the cause of oscillation.

There are several recommendations for future work regarding the 24 GHz front-end design. The goal of this thesis was to investigate whether the presented FM detector performs as required when implemented in the CMOS 65 technology. The answer is "yes", but with several limitations. Receiver sensitivity and stability seem to be more serious limitations of this implementation. As underlined in chapter 2, the calculated receiver sensitivity should be -60 dBm. With -50 dBm input power, the receiver produces a minimum amplitude of around 2 mV, which is the least required for the functioning of the IF amplifier. To reach the -60 dBm calculated sensitivity, the gain of the previous stage, the LNA, needs to be increased. This can be implemented either by increasing the LNA DC current or by providing a pre-LNA amplifier stage. The last option is more viable, since then the first stage could provide 15 dB gain and a small noise figure, while the next stage could be a high gain amplifier increasing the signal level to -20 to -25 dBm as required by the mixer. Therefore, even though the current consumption has been limited to 1 mA, the receiver actually does need more current. In the present case, there are 600 μA flowing through the LNA. If this is doubled, the gain increases from 22 to 26.5 dB and the signal amplitude to the mixer increases from 24.1 to 40.8 mVpk-pk and from 16.6 to 27 mVpk-pk.

Another point of concern is the dual gate mixer itself. In order to reduce current consumption, the simplest form of mixer has been chosen. Nevertheless, the doubly balanced form of this mixer has better specifications, in terms of linearity and conversion gain [1]. As in the case of the single-balanced mixer from Chapter 3, Section 3.3, the doubly balanced mixer topology requires a differential output from the phase shifter. If a

differential output can be supplied, then also the compact receiver designed in this thesis could be an alternative for a redesign of the front-end.

One of the more immediate changes is the redesign of the IF amplifier. The amplifier performs the function of detecting changes on the order of mV at the output of the mixer. But its sensitivity to these changes is too high by attaining a very high gain, and may be the cause of oscillation when coupled with the output buffers needed to drive the load represented by the oscilloscope. An alternative to the IF amplifier could be an operational transimpedance amplifier, which can provide the same amount of gain, 50dB, at the expense of more power consumption and a differential input and/or output. A balanced output would solve many

From the layout point of view, the 180 μm lines used to connect the input to the LNA and the cascode transistor to the LNA LC tank should be shortened. On the other hand, due to the size of the inductors, it is hardly possible to limit long connections. Therefore, a transmission line implementation of the lines should be employed. Furthermore, the parasitic behavior should be more seriously investigated. In the layout of the phase shifter, parasitic capacitance can be taken as an advantage. Since the coupling capacitance, C_K, from Fig. 3.24 needs to be as small as a couple fF, lines having more parasitic capacitance can be employed to provide this capacitance. From what parasitic extraction simulations show, there is extra phase shift incurred by the parasitic capacitance in the phase shifter. By eliminating the 3 series capacitors that provide the value of C_K, extra space and less capacitance can be achieved.

While measuring the two chips, the oscillation detected upon providing DC biasing indicates that the output buffers need some further attention. The layout of the IF amplifier and output buffers would need to be better implemented, taking care to decouple the power supply of the buffers at low frequencies and to provide them a separate ground connection as outlined in Chapter 5, Section 5.4. Also, to lower the current that needs to charge the capacitive load of the cable and oscilloscope, a different probe should be used that does not equate to 50-100 pF. It has been noticed within measurements that a lower load probe decreases the oscillation. If the output could be measured with a 50 Ω probe, there would be less interference and less cause for oscillation but also the output would not be rail to rail rather in the order of mV.

The 24 GHz front-end for WSN applications has been designed and manufactured. According to circuit simulations, the front-end meets the requirements of the application at a power consumption of 1.2 mW. Some problems have been recognized and solutions addressing them are proposed. Possibly in a next phase of design, these solutions can be implemented and would provide better specifications to the front-end.

Reference

[1] J. Cui, Y. Lian and M. F. Li, "A low voltage dual gate integrated CMOS mixer for 2.4 GHz band applications" in *Proc. of the 2004 International Symposium on Circuits and Systems (ISCAS)*, vol. 1, pp. 964-967, 2004

Appendix. Compact Receiver Design

Using the concept underlined in Chapter 3 Section 3.2, a circuit implementation is created. The compact receiver combines the LNA and the mixer action into one system.

There are two classes of mixers employed in IC design: passive and active mixers. At the expense of more power consumption, active mixers are preferred since they provide gain and thereby reduce noise present in the system [1]. Even though passive mixers have the advantage of speed and higher linearity, more gain and less noise is favored for this receiver.

A further categorization of active mixers leads to single-balanced and double-balanced mixers, as shown in Fig. App.1 (a), (b). Besides higher gain and lower noise, double-balanced mixers are commonly used since they provide less even-order harmonic distortion and high LO-IF isolation [2, 3]. Nevertheless, single-balanced mixers consume less power, since they employ one set of differential switching core transistors and provide less input-referred noise for a certain power dissipation [1]. This type of mixer receives the RF signal in a single-ended way, while the LO is applied differentially. For the current application, this type of mixer is used since it reduces the number of components on chip and provides a simple architecture.

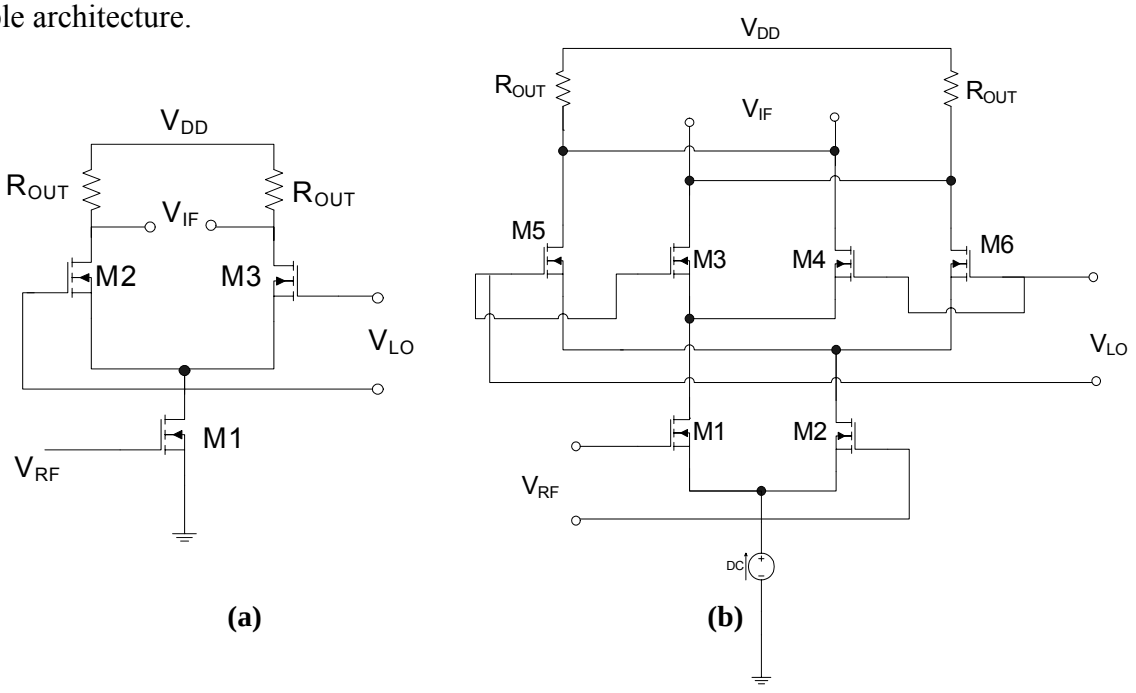


Fig. App. 1 Single balanced mixer topology (a) and Double balanced mixer topology (b).

The choice of the LNA topology is again subject to many options. Most common topologies are the inductive degenerated common source LNA, which assures both noise and input impedance matching, and the common gate stage which features high reverse isolation. Inductive degenerated LNAs lend themselves to narrowband applications and have lower reverse isolation. To improve gain and reduce voltage headroom, an LC resonant tank provides high resistance at the operation frequency.

For this receiver, an LNA with 50 Ω input impedance matching and high gain is required. The reverse isolation consideration has not been taken into account since a cascode would seriously impair the voltage headroom.

Fig. App.2 shows a schematic of the compact receiver. The signal enters from the RF port and is impedance matched to 50 Ω by the use of capacitor-resistor, C_1-R_1 combination. Further on, it passes through transistor M1, operating in saturation, that functions like a low noise amplifier. Gain is obtained at 24 GHz by the resonant tank formed by L_1-C_2. The amplified signal is taken at the drain of M1 and fed to the 90º phase shifter. Thereafter, a voltage controlled voltage source (VCVS) is used to feed the mixer transistors, M2 and M3, with a phase shifted version of the RF signal. The mixer core is biased by a 1 V voltage source- V_G. After signal multiplication, the downconverted signal is collected differentially by resistors R_{out}. The transconductor transistor, M4, takes the amplified signal from the output of the LNA. All mixer transistors operate in the saturation region. From M4, the DC signal is fed back to the initial LNA transistor, M1. This path rejects the RF signal through an inductor, L_2. In the initial design phase, the RF signal was also fed back to the LNA transistor. It was noticed that the voltage gain decreased due to more impedance seen at the source of M1. Therefore, the RF signal was AC grounded at the base of the LNA, through capacitor C_{decpl}.

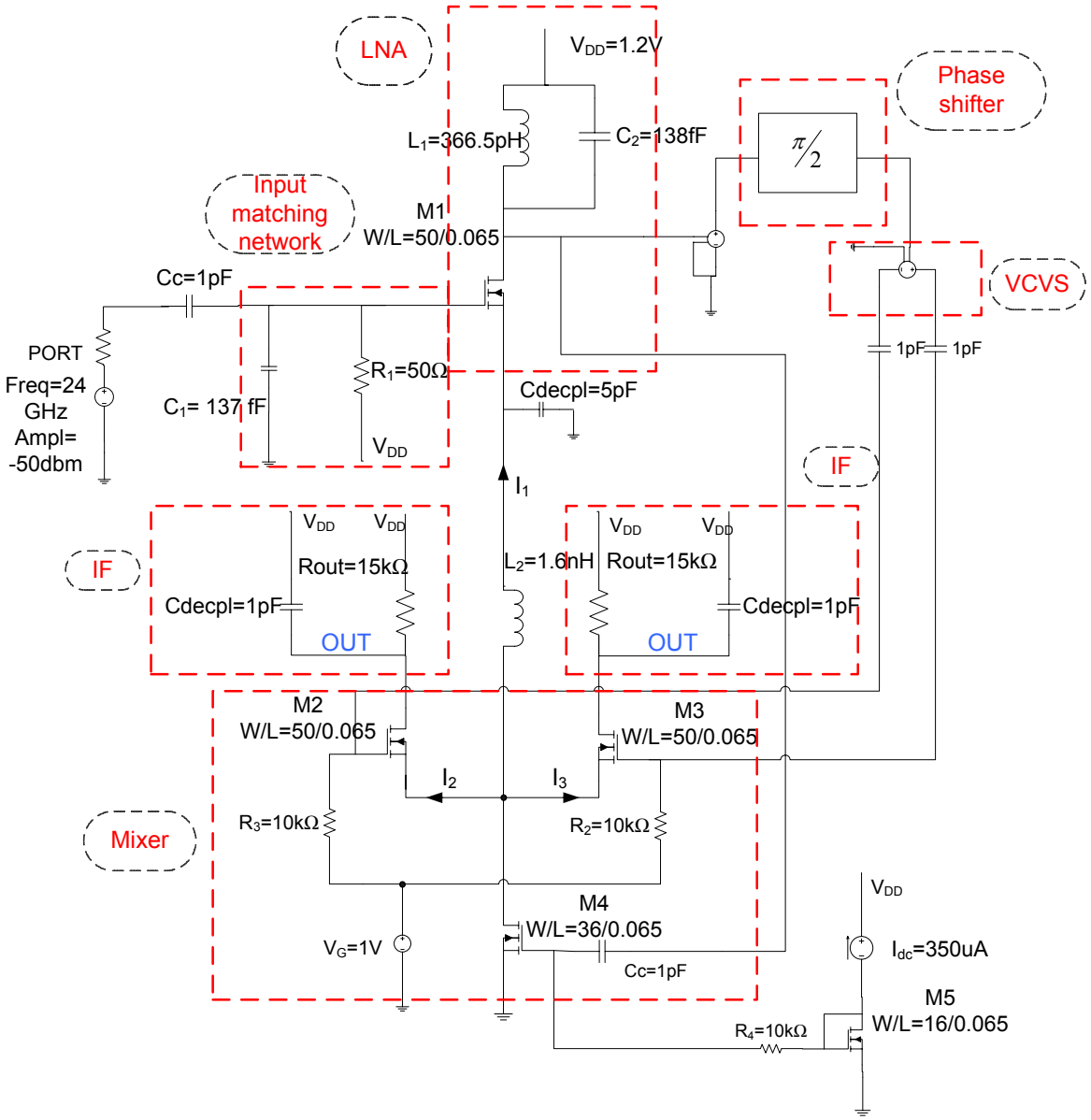


Fig. App. 2 Schematic of compact receiver

1.1 Front-end Design

The main goal of the receiver is to provide a high downconverted output voltage. A high conversion gain and a high LO signal make this goal possible.

The mixer's conversion gain is [1]:

$$A_v = \left|\frac{v_{IF}}{v_{RF}}\right| = \frac{4}{\pi} \cdot g_m \cdot R_{out} \qquad \text{(app-1)}$$

where g_m is the transconductance of the transconductor transistor, M4, and R_{out} is the load resistance. Thus, by maintaining a high transconductance and a high load resistance, a high output voltage is attained.

The maximum 1 mA current consumption is also required. Biasing of the transconductor transistor, M4, is performed with a current mirror and a current source, I_{dc}, providing 350 μA. The entire receiver consumes a total of 900 uA. Most of the current, I_1, passes through the feedback path leaving only I_2=I_3=60 μA through the core transistors, M2-M3. They are dimensioned with an aspect ratio of 50/0.065. The idea is to make the transistors switch faster, by increasing their width and decreasing the drain current. Enlarging the width increases the gate to source capacitance seen at their source and shunts the RF current. Whereas decreasing the drain current increases the impedance seen looking into the source terminals of the core transistors and allows more RF current to flow through the capacitance at the source terminals [1].

Using (app-1), with load resistors (Rout) of 15 kΩ and g_m of 400 μS, the conversion gain should theoretically be 26 dB. This value is not attained in simulations since the RF signal will leak through parasitic capacitances and resistances. After passing through the mixer core, the downconverted signal is low pass filtered by capacitor, C_{decpl} and resistor, R_{out}.

The LNA is designed for maximum gain to ensure a high voltage swing. The LNA transistor, M1, has an aspect ratio of 50/0.065 as well. It is biased from a 1.2V voltage source (V_{DD}), and is impedance matched to 50Ω by a parallel combination of a 50 Ω resistor (R_1) and a 137 fF capacitor (C_1). However, the input resistor adds noise to the LNA, degrading its performance. The LC tank resonates at 24 GHz, by employing a standard 445 pH inductor and a capacitance of 137 fF.

The phase shifter is the most difficult block of the compact receiver to design. Presented in Chapter 3 Section 3.2, the original phase shifter provides a single ended output, whereas the single balanced mixer requires a differential input. A filter is needed to be able to split the signals in two 90 degrees shifted signals. Several phase shifters are investigated, among which a polyphase filter and the original phase shifter. For each implementation, the same problem was encountered, such as how to provide two phase shifted signals without using a

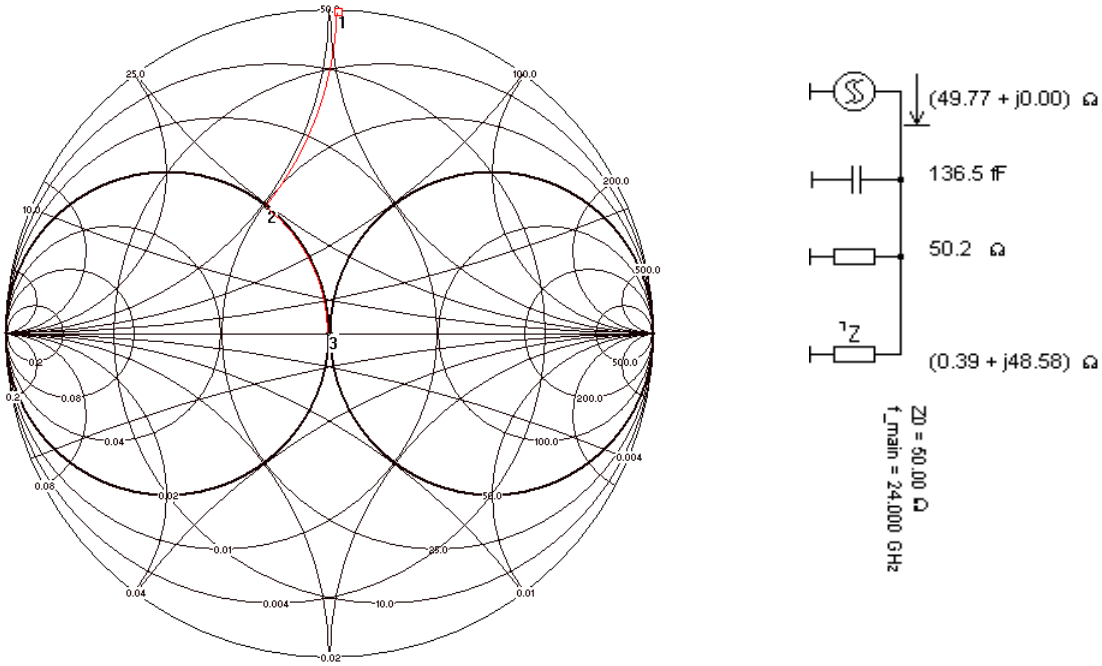
VCVS and how to reduce the impedance loading between the LC tank and the phase shifter, without using an ideal VCVS.

These problems have been the real bottlenecks in the compact receiver design. Several other problems will be also addressed in Section 1.3.

1.2 Simulation results

A number of simulations using both types of phase shifters are performed . Simulations are carried out with a 1.2 V power supply (V_{DD}) and at a temperature of 27º. A 50 Ω impedance port provides the 24 GHz RF input with a sensitivity level of -50 dBm. Several ideal components are kept in the design, since this receiver is used in order to verify the theoretical concept.

An input impedance matching network composed of a capacitor and a resistor transforms the nearly inductive impedance seen at the input of the LNA. At 24 GHz, the normalized impedance looking into the input of the LNA is Z_{11}=-0.0286+j0.9916. A matching network consisting of a 50 Ω resistor and 137 fF capacitor is presented in Fig.App.3.



(a) **(b)**

Fig. App. 3 Smith Chart of impedance matching (a); network circuit (b)

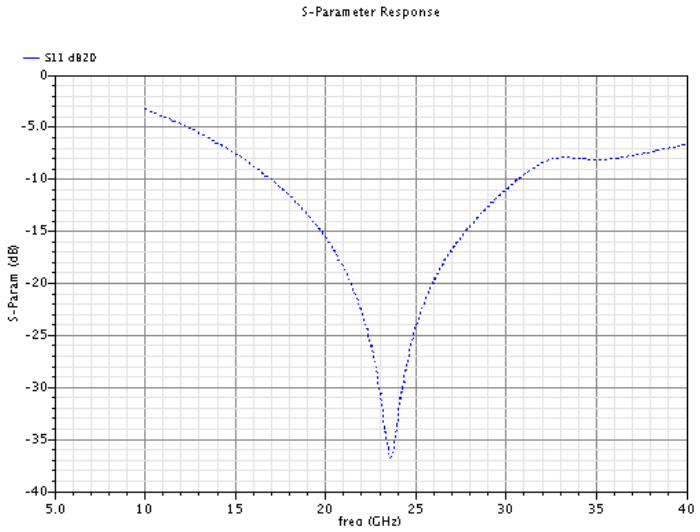


Fig. App. 4 Input reflection coefficient, S_{11}

The result of matching can be quantified as the input reflection coefficient in the compact receiver shown in Fig.App.4. Around 24 GHz, there is more than -35dB rejection. Also the matching is quite wideband, as S_{11} is below -10dB in a frequency range of 14 GHz.

The voltage gain has also been simulated. A standard inductor of 444.5 pH with a Q of 19.3 is chosen. Based on (app-2), the capacitance should be 99 fF for a resonance at 24 GHz.

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \qquad \text{(app-2)}$$

In reality, the resonance is achieved with C=138 fF. According to (app-2), the resonant frequency based on this capacitance is 20.3 GHz. This does not take into account the resonant tank losses and additional parasitic capacitance from the components and from the transconductor stage. The losses decrease the resonant frequency or introduce other resonances.

To avoid impedance loading effects, the ideal VCVS is still kept between the resonator and the phase shifter. With this ideal component, the gain has been simulated to reach 14.45 dB, as shown in Fig.App.5.

Because the simulated gain at this point has an acceptable value, the attention is presently directed to the design of the phase shifter.

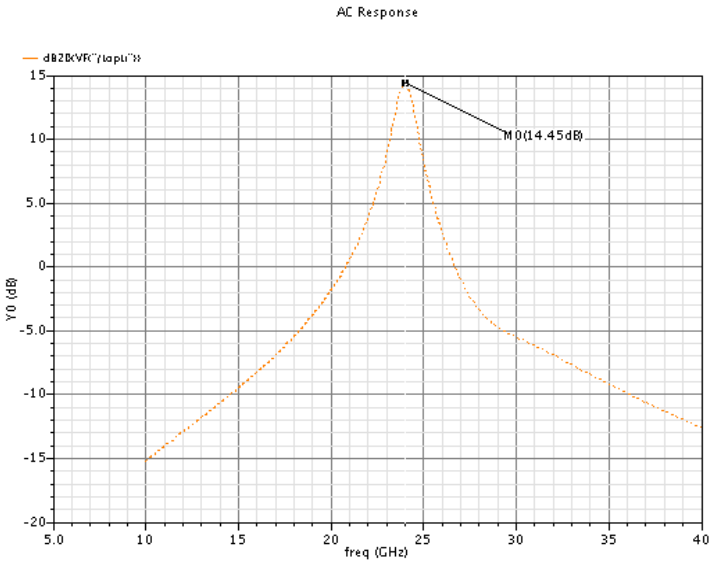


Fig. App. 5 Simulated gain of compact receiver

For this purpose, two types of phase shifters were investigated: the original phase shifter presented in Chapter 3 Section 3.2 and a polyphase filter.

To dimension the phase shifter, a first task is to choose an inductor that provides a right inductance value with a high Q factor. This is found in the standard inductor with a value of 300 pH and a Q of 26.8. Furthermore, for a frequency of 24 GHz, the value of C_0 and C from Fig.3.2, are determined from Eq. (3-9): $w = \frac{1}{\sqrt{L \cdot (C_0 + C)}}$

Therefore, (C+ C_0) should be 146 fF. Eventually, the phase shifter has been dimensioned to have C_0=256 fF and C=29 fF. Following the ideal VCVS, the signals are made to be 90 degrees phase shifted, and found to be 26 mVpk-pk and 20 mVpk-pk before entering the mixer core. The RF current passing through the transconductor transistor M4 is 220 µA pk-pk.

The second phase shifter that was investigated is a one stage polyphase filter, shown in Fig. App.6. This filter provides the generation of quadrature signals from a single phase input. It only allows to pass a signal at a frequency equal to $\frac{1}{2 \cdot \pi \cdot R \cdot C}$. [3]. Due to the two in-phase and quadrature generated signals, this filter lends itself well to the current application. The

polyphase filter uses a 305 Ω resistor and a 33 fF capacitor. Together with the C_{GS} of M4 which adds 60 fF to the capacitance, it provides a phase shift of 90 degrees at 24GHz. Prior to entering the mixer core, the signals are as low as 4 mVpk-pk. The problem for this small signal is the 3dB signal loss. Moreover, the LC tank has been re-dimensioned to account for the different LO signal fed to the mixer. For this phase shifter implementation, the gain achieved by the LNA is 9 dB at 24 GHz. For an input signal of 2 mVpk-pk, 9dB gain provides almost 6mVpp, which with the 3dB insertion loss accounts for the 2-2.5mVpp at the mixer core transistors.

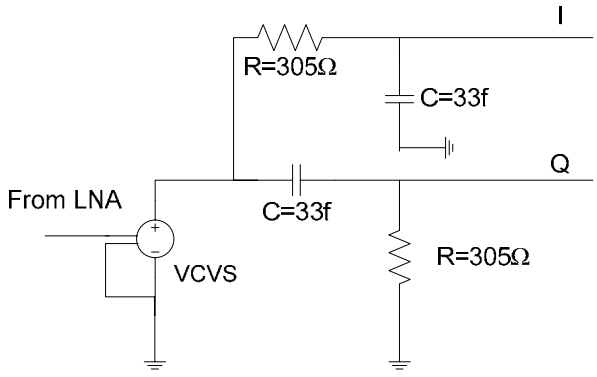


Fig. App. 6 Schematic of polyphase filter

The conversion gain and the output voltage of the mixer can at this point be simulated. By running a transient simulation for 100ns or 200ns, it is ensured that the mixer output has converged to a stable downconverted value. Furthermore, a DFT transform is performed on the downconverted signal, from which an exact value of the output voltage can be obtained. Fig.App.7 shows the downconverted output voltage and the DFT transform performed on the transient signal for each phase shifter implementation.

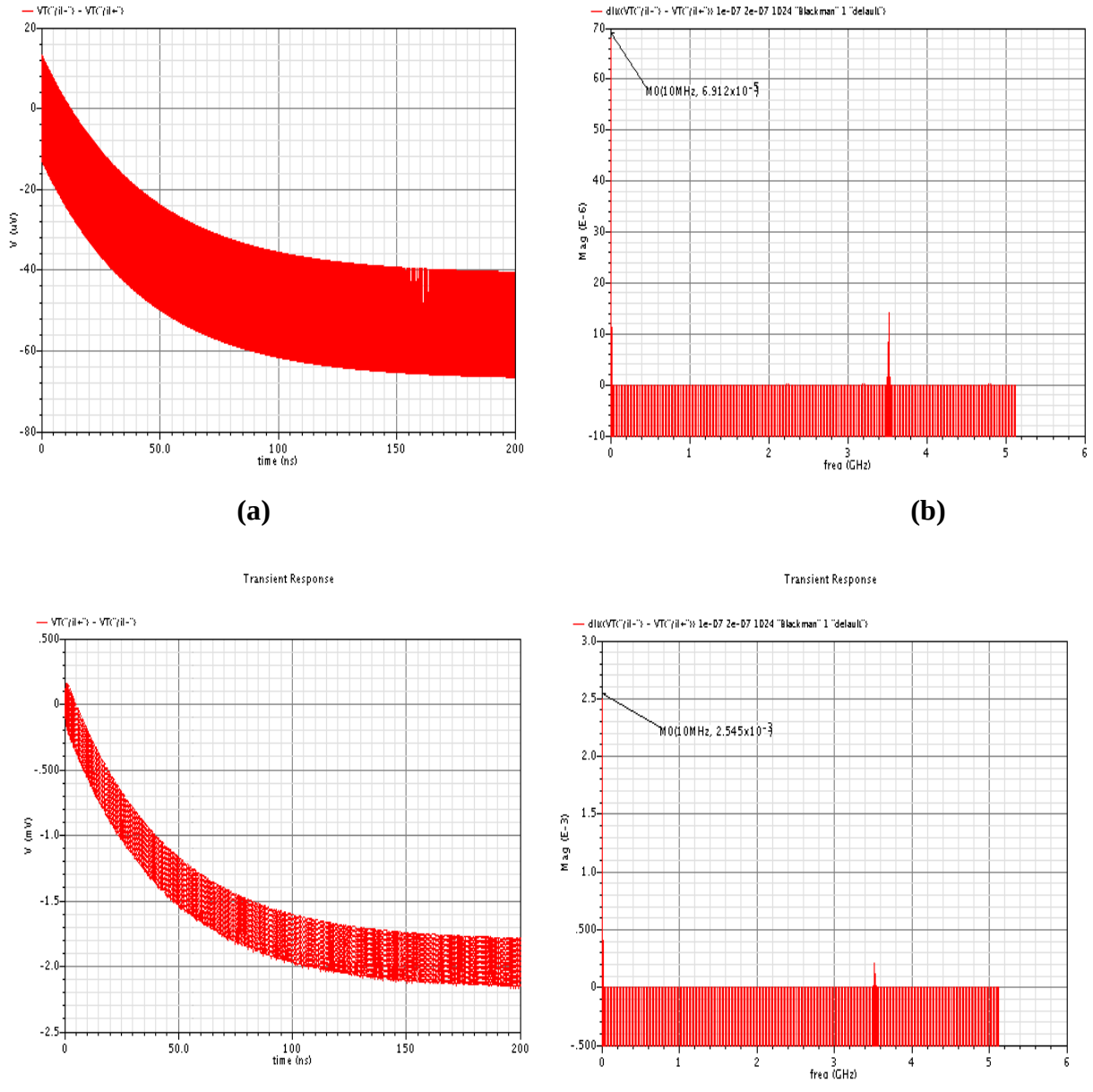


Fig. App. 7 a) Simulated mixer output with polyphase filter phase shifter; b) DFT transform on output with polyphase filter phase shifter; c) Simulated mixer output with original phase shifter; d) DFT transform on the output with original phase shifter.

Fig.App.7 (a) shows the output signal with the polyphase filter. It reaches a value of only 69 uV, which is far from fulfilling the design goal of 5 to 10 mV.

Fig App.7 (c) shows the output signal which reaches a DC average of about 2mV. In accordance to what has been stated in Section 3.2, this value is still quite small, but closer to the design goal. At the output of the mixer, an IF amplifier with large gain can be designed which can raise the downconverted signal to 1.2 V, which can then further be passed to digital signal processing.

Based on these results, a discussion will be held in the next section as to why the output does not meet the goal and what improvement can be made.

1.3 Downconverted Output Level Discussion

A conclusion to the simulation results section is that the compact receiver might not be best for implementing the detection concept.

Several problems have been identified within the course of the receiver design. Making use of ideal components, such as voltage controlled voltage sources (VCVS) during simulation is just an intermediate step towards a final design. The signal gain drops when more realistic models are used in the simulations. Loading effects also intervene once the VCVS is removed. The LC tank has high output impedance, while the phase shifter (both the original one and the polyphase filter) has low impedance. An impedance transformation such as capacitor tapping to lower the impedance can be used to solve the loading, although this decreases the gain, whereas a high gain is needed to keep the LO amplitude high. The original phase shifter implementation requires the additional ideal component to split the signal into two quadrature versions. This is also not a solution since a real implementation of the VCVS (such as a voltage follower) leads to more current consumption.

The second phase shifter implementation is also problematic. The polyphase filter is known to attenuate signals by a 3 dB insertion loss, if loaded with a network of the same input impedance [3]. This leads to a weak LO amplitude which barely allows the switching of the mixer core transistors. A solution to this problem would be to add a buffer following the quadrature outputs. Unfortunately, this would add more current consumption, surpassing the power consumption goal of this receiver. All of these problems lead to a decrease in the output downconverted signal level.

Another identified problem is the DC feedback. Most of the DC current flows through the feedback path, which leaves very little current to the mixer core transistors. They are biased in the saturation region, but have little current flowing through them. Thus, their transconductance is small (400uS) and resistance is high. Increasing the DC current would decrease the current flowing through the LNA which would, in turn, increase the mixer gain. This trade-off would be easier if the LNA would not need to provide a high gain or if

an additional stage could be used. A cascoded transistor for the LNA might be a solution to this problem, but this would increase the voltage headroom. Increasing the power supply is also not an option since this has been fixed by the technology.

For all these reasons, the compact receiver has not been chosen for implementation.

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