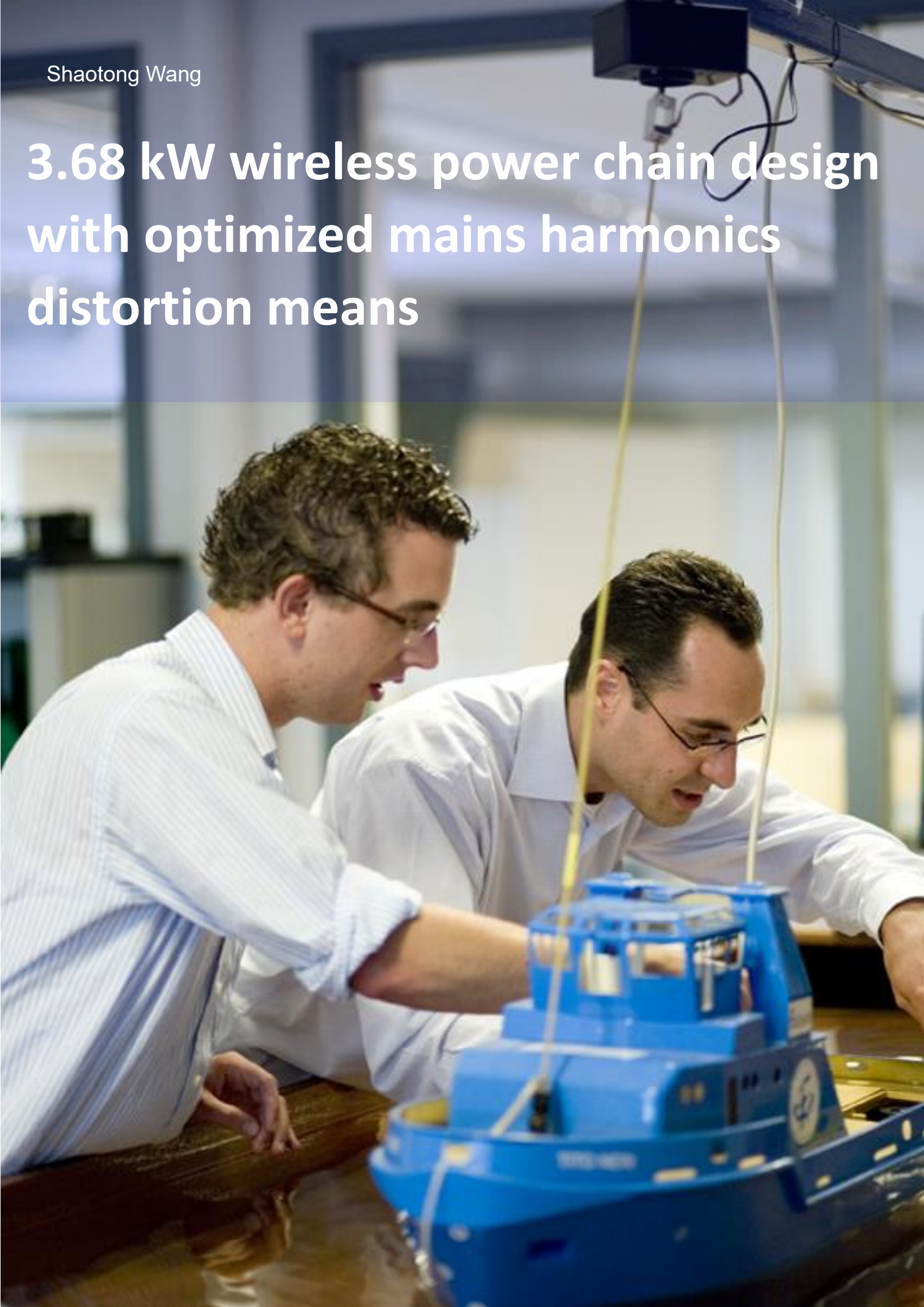
Shaotong Wang

3.68 kW wireless power chain design with optimized mains harmonics distortion means



3.68 kW wireless power chain design with optimized mains harmonics distortion means

By

Shaotong Wang

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Supervisor:	Prof. P. Bauer	
Thesis committee:	Dr. T. B. Soeiro	TU Delft
	Dr. S. H. Tindemans	TU Delft
	Ing. W. Ettes	Philips

TU Delft

Abstract

This Thesis project is executed at Philips in the Netherland for the cordless kitchen system group.

In order to enable the current cordless kitchen system to the 3.68 kW power level, measures needs to be taken to reduce the mains harmonics. The problem is that with the increase of the power level from 2.40 kW to 3.68 kW, the amplitude of the undesired harmonics in mains current will exceed the limit according the mains harmonics standard (IEC). Hence, this project aims to investigate means and measures to reduce the undesired mains harmonics.

In the cordless kitchen system, the mains harmonics are generated due to the existence of the communication time slot around the zero crossing of the mains voltage. The background of having a communication time slot in this system is introduced in detail in section 2. To remove the negative effect of communication time slot on the mains harmonics, a compensator is built which is connected in parallel with the DC input terminals of the existing transmitter stage. The compensator can fix the mains current, such that the amplitude of undesired harmonics are reduced.

The compensator consist of a Boost converter and a Buck converter. The duty cycles of the two converters depend on the compensation current needed. Therefore a current sensor, a zero crossing detector and a control circuit were developed and described in this report.

Finally, the simulation result and practical result are provided and evaluated. As a result of this work, the amplitudes of the mains harmonics are significantly reduced, such that the cordless kitchen system meets the standards for mains harmonics.

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1. Introduction

In people's daily life, a lot of electrical appliances are used in the kitchen, for example the kettle, the food processor and the rice cooker. When using these appliances at the same time, the large number of mains cords causes a mess on the kitchen countertop. To solve this problem, a cordless kitchen system is under development, based on the wireless power transfer (WPT) technology.

The aim of this project is to improve the Power Factor (PF) of the wireless power chain which is applied in the cordless kitchen system. Generally speaking, the cordless kitchen system consists of two channels, the power channel and the communication channel. The power channel transfers power from the mains source to the appliance. The communication channel is used to communicate from the transmitter to the receiver and vice versa.

The block diagram of the power channel is shown in figure 1.1 and consists of a low frequency rectifier (LF rectifier), a high frequency inverter (HF inverter), a transmitter coil (Tx) and a receiver coil (Rx).

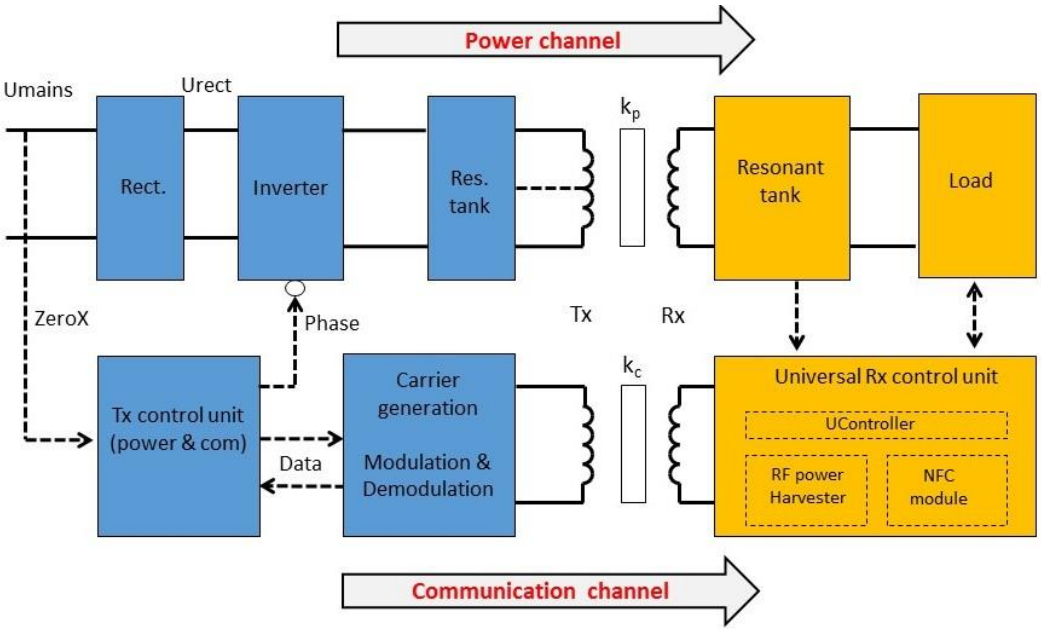


Figure 1.1: Block diagram of the cordless kitchen system

The low frequency power drawn from the 50/60Hz mains source is converted to high frequency power by a cascade of a LF rectifier and a HF inverter. Next, the power is transferred via a magnetic field from the transmitter coil to the receiver coil. The transmitter coil is located under the kitchen countertop. This magnetic field is captured by the receiver coil which is usually located at the bottom of the appliance. Because there is no mains cord used in that process, this power chain is called a wireless power chain. Typical target appliances for this system are heating appliances (kettles), motor driven appliances (food processors) and the combination of those two (rice cookers) [1].
Besides the power channel, a communication channel exist between the transmitter and receiver, see figure 1.1. This communication channel is based on Time Division Multiplexing, which is performed during a communication time slot around every zero crossing point of mains voltage.

Be aware that both the power transfer as well as the communication are using the magnetic field. Therefore, to avoid the interference, these processes need to be executed in different time slots. Therefore the choice is made to switch off the power channel for approximately 1.0 - 1.5 mSec around the zero crossing of the mains voltage, to create a communication time slot [2]. Consequently, the mains input current of the cordless kitchen system becomes

discontinuous which induces mains harmonics. Because of this, the practical limit for the power transfer is limited to 2.40 kW. Above this power level, the amplitude of some of the mains harmonics between 50Hz and 2000Hz will not satisfy the standards of the International Electro technical Commission (IEC) [3]. The maximum power which can be drawn from a single phase equals 3.68 kW. To increase the power transfer of the cordless kitchen system to this level, the IEC standards for mains harmonics cannot be met, unless measures are taken. In this report, measures are described how to increase the power transfer level up to 3.68 kW, while satisfying the IEC standards. To realize this goal, the effect of the communication time slot on the harmonic content of the mains current of the cordless kitchen system is investigated.

During earlier work on this topic [4], several alternative power chain diagrams were investigated to reduce the harmonic content of the cordless kitchen system at power levels above 2.40 kW. During this project, control schemes for these power chain diagrams are investigated, by means of simulations (LTSpice) and calculations (Matlab).

This report can be divided into seven chapters. Chapter 1 is introduction. In chapter 2, the main problem to be solved is described in detail. The load characteristic of the power channel is described in chapter 3. In chapter 4, different solutions are described on system level to reduce the amplitude of the harmonics of the mains current. In chapter 5, the design of the new power channel is introduced. In chapter 6, the simulation results under different control methods are provided, and the practical results are provided as well and evaluated. In chapter 7, the conclusion is presented and future work on this topic is suggested.

2. Problem statement

As it was mentioned in the introduction part, during the communication time slot, the power transfer is switch off to avoid interference between the two channels. The communication channel operates in sync with the power channel and communication is performed around the zero crossing of mains voltage. Therefore the current through the transmitter coil (Tx) is zero during the communication time slot [5]. In the figure 2.1, the blue curve shows the current through the transmitter coil. It can be observed that the transmitter coil current shows a gap near the zero crossing of the mains voltage with a duration of proximally 1.0 - 1.5 mSec during every half mains period. During this time slot the communication is performed without interference from power transfer magnetic field [1].

Due to this current gap the mains current becomes discontinuous as well. The lower plot in figure 2.1 shows the shape of the mains current. The plot shows that the current remains zero for 1.0 - 1.5 mSec around the zero crossing point and will be called “mains current gap” in the sequel of this report.

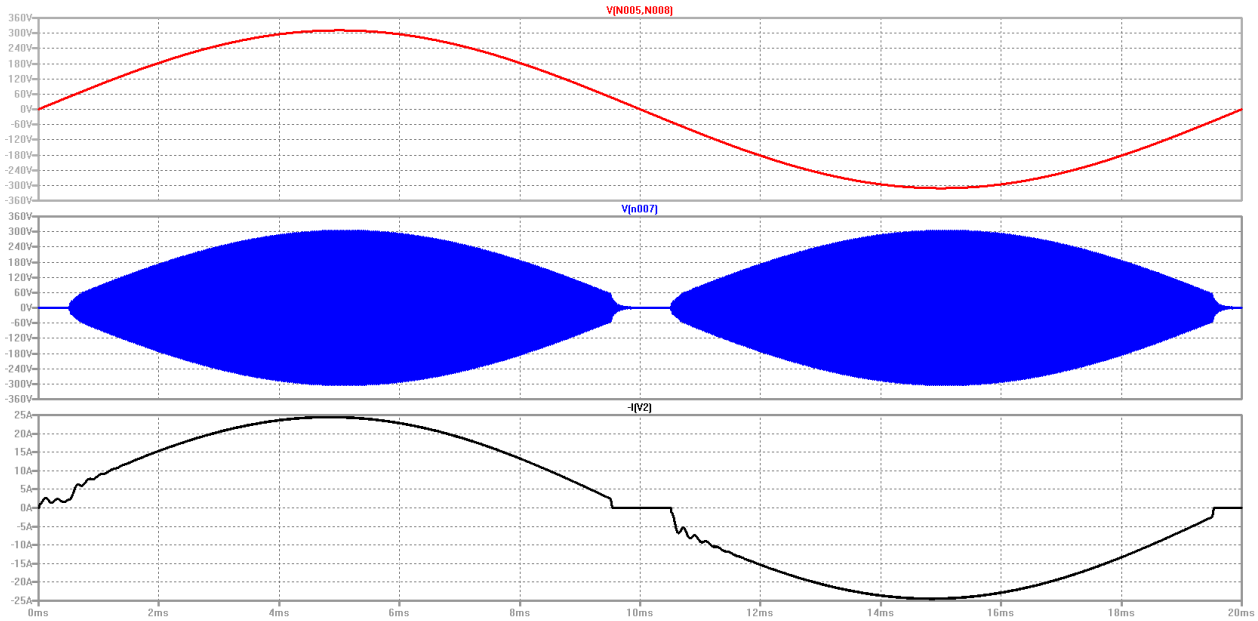


Figure 2.1: The mains voltage (red curve), the transmitter coil current (blue curve) and the mains current (black curve).

Due to the mains current gap, undesired harmonics are induced to the power grid. Currently, the cordless kitchen system is rated at 2.40 kW. According to the IEC61000-3-3 standard proposed by international Electro Technical Commission (IEC), the measured mains harmonics meet the standard at this power level. However, when the power level of this system is increased to 3.68 kW, the mains harmonics exceed the maximum tolerance limits.
In the figure 2.2, the harmonic content of the mains current is shown for the 3.68 kW power level. The red curve indicates the IEC harmonic current limits, the blue curve indicates the harmonics of the mains current. As figure 2.2 shows, the amplitude of the 9^{th}, 11^{th}, 13^{th}, 15^{th}, 17^{th}, 21^{st}, 23^{rd}, 25^{th}, 27^{th}, 29^{th}, 35^{th}, 37^{th} and 39^{th} harmonics exceed the acceptable harmonic limit. Therefore, removing or partially removing the current gap in the mains current is necessary. Therefore, the aim of this project is to design a new power channel which can provide a discontinuous transmitter current as well as a continuous mains current. Furthermore, the cost and size increase of the new power chain should be limited. A reduction of the efficiency must be avoided. To achieve low cost, the new power channel must be realized by adding a sub system on the top of the existing cordless kitchen system. Because a passive solution will cause the new power chain to become bulky and heavy, an active solution is preferable.

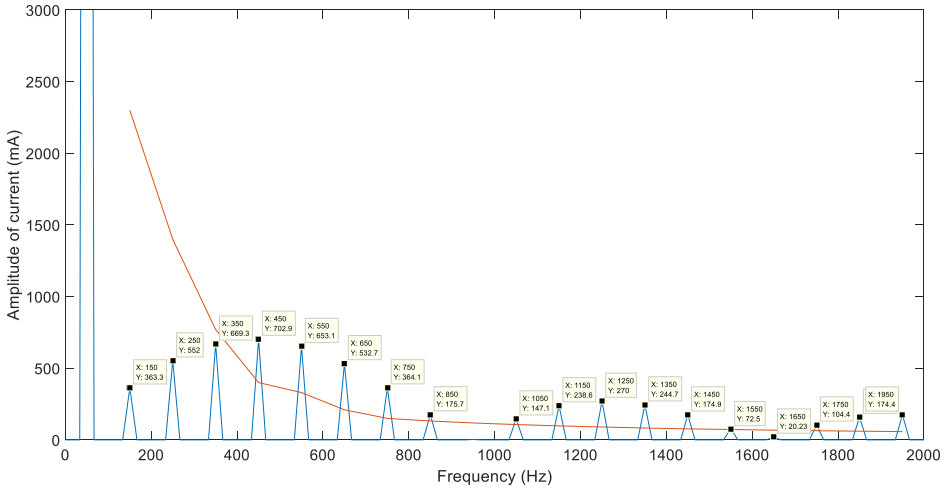


Figure 2.2: The mains harmonic content of the mains current at 3.68 kW power level.

3. Load characteristic of the power channel

3.1 Introduction

In this chapter, the load characteristic of the power channel of the cordless kitchen system is described, as perceived by the mains source. Firstly, the load characteristic of the power channel without the communication time slot is discussed (linear load). Secondly, the effect of the communication time slot on the load characteristic will be discussed (non-linear load). Next the origin of the mains harmonics will be investigated.

3.2 Power channel as a linear load

In the case without the communication time slot, the current gap in the mains current does not exist, so the mains current is completely a sinusoidal wave, like figure 3.1 shows.

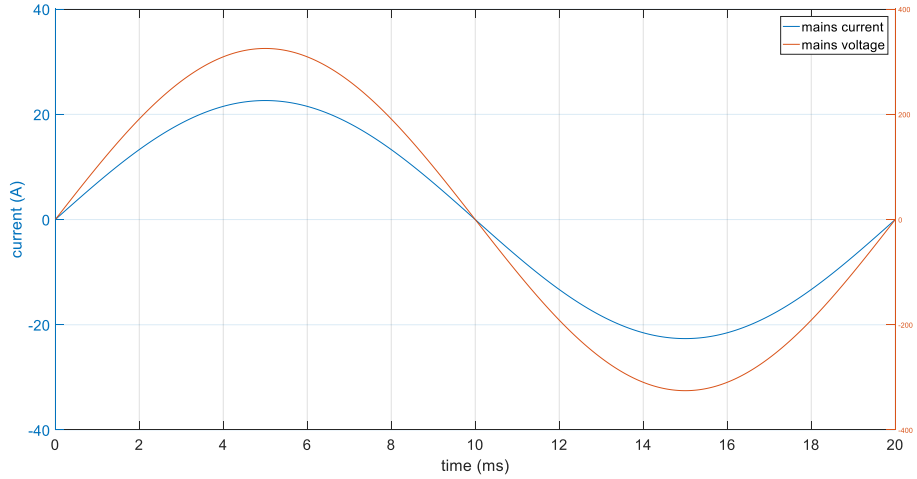


Figure 3.1: The mains voltage and the mains current without the current gap.

The red curve represents the mains voltage. The blue curve is the current through the transmitter coil (Tx). The maximum current which can be drawn from a single phase equals 16A. Therefore, the maximum power that can be drawn can be calculated by equation (1).

$$P_{max} = U_{mains\_rms} \cdot I_{mains\_rms} = 230 \cdot 16 = 3680 \ \ W \tag{1}$$

The equivalent load resistance can be calculated by the equation (2).

$$R_{load\_eq} = \frac{U_{mains\_rms}}{I_{mains\_rms}} = 14.375\Omega \tag{2}$$

In this ideal case, the mains current is in phase with the mains voltage and does not show higher harmonics. All the power is transferred via the first harmonic (50 Hz).

3.3 Power channel as a non-linear load

Now the mains current gap is introduced to the mains current, see figure 3.2.

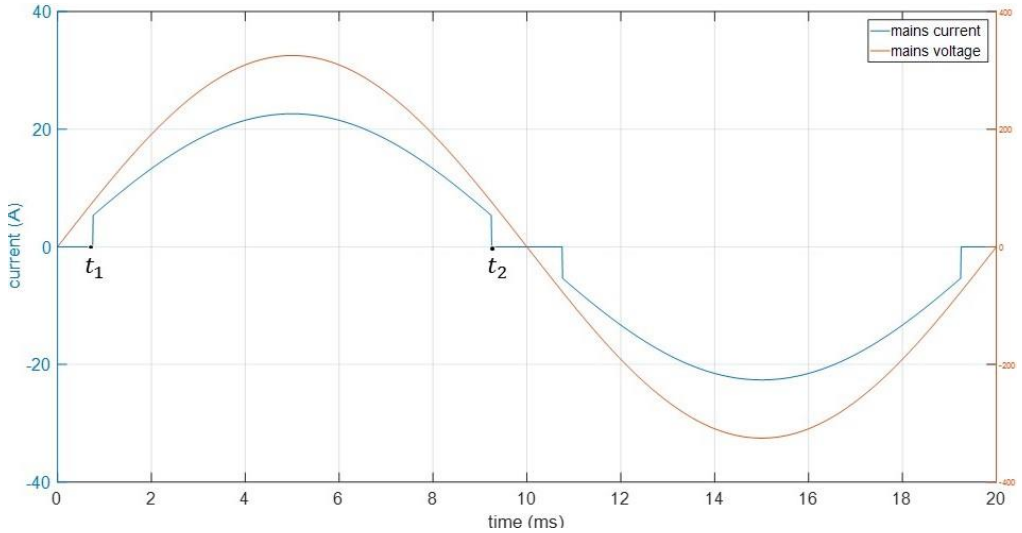


Figure 3.2: The mains voltage and the mains current with current gap.

The red curve represents the mains voltage. The blue curve is the mains current where t_1 and t_2 are 0.75 mSec and 9.25 mSec respectively. Figure 2.2 shows the Fourier analysis of the mains current with the mains current gap. As can be seen, the undesired mains harmonics exceed the IEC harmonics standard.

$$U_{mains}(t) = \hat{U}_{mains}\sin(\omega t) \quad (3)$$

$$U_{mains\_rms} = \frac{\hat{U}_{mains}}{\sqrt{2}} \quad (4)$$

$$I_{mains}(t) = \frac{2}{T_{mains}}\int_{t1}^{t2} \hat{I}_{mains}\sin(\omega t)dt \quad (5)$$

$$I_{rms} = \sqrt{\frac{2}{T_{mains}}\int_{t1}^{t2}(\hat{I}_{mains}\sin(\omega t))^2 dt} = 15.956A \quad (6)$$

The rms value of the first harmonic of the mains current becomes:

$$I_{rms\_1st} = \left(1 - \frac{4\cdot t_1}{T_{mains}} + \frac{2\sin(2\omega t_1)}{\omega T_{mains}}\right)\cdot\frac{\hat{I}}{\sqrt{2}} = 15.912A \quad (7)$$

Based on equation (6) and (7), we can calculate the real power and apparent power.

$$P_{real} = U_{rms}\cdot I_{rms_{1st}} = 3659.76W \quad (8)$$

$$P_{ap} = U_{rms}\cdot I_{rms} = 3669.88W \quad (9a)$$

The power transferred due to the higher mains harmonics can be calculated by equation (9b)

$$P_{nth} = \frac{2}{T_{mains}}\int_0^{\frac{T_{mains}}{2}} 311\sin(\omega t)\cdot\hat{I}_{nth}\sin(n\omega t)\cdot dt = 0 \quad (9b)$$

where n can be any integer number. According to the equation (9b), only mains harmonics (50 Hz) can transfer power. The harmonics which has different frequency from the frequency of mains voltage (50 Hz) contribute nothing to the power transmission.

3.4 Mains harmonics and Power factor

Because the communication time slot is symmetrical around the zero crossing of the mains voltage, the first harmonic of the mains current is in phase with the mains voltage and the mains current shows only odd harmonics. When any odd integer is substituted into equation (9b), the outcome of P_{nth} is always zero. Therefore, it can be concluded that only the first harmonics of the mains current transfers' power to the cordless kitchen system.

Hence, the power factor PF and power reduction due to the communication slot can be calculated:

$$PF = \frac{P_{real}}{P_{ap}} = \frac{3659.76}{3669.88} = 0.9972 \quad (10)$$

$$Power\ \ reduction = P_{nom} - P_{real} = 3680 - 3659.76 = 20.24W \quad (11)$$

The power reduction is the power which is not transferred to the appliance during the communication time slot and equals 20.24 W. However, because of the ramping duty cycle applied, the power reduction is more than 20.24 W, and it is equal to 83 W. The ramping duty cycle will be discussed in detail in chapter 5.4.

4. Alternative power channel

There are two different solution directions to make the cordless kitchen system meet the mains harmonic standard at 3.68 kW, and these are:

1. A passive solution
2. An active solution

For the active solution two directions are possible, the series structure and the parallel structure.
With the series structure a so called active Power Factor Corrector (PFC) is put in between the LF rectifier and the terminals of the inverter. In this way, the mains power flows through the active PFC component. The advantage of this is that the mains current meets the mains harmonic standard for every power level. The disadvantage of this solution is that the power is processed twice, both by the PFC and the inverter, which has a negative impact on the efficiency. Furthermore, this solution is voluminous and might cause thermal issues as well.
With the parallel structure the mains current gap is filled by putting a so called compensator in parallel with the LF rectifier. Compared to the series structure, the power dissipated by the active component is expected to be smaller, and the cost of the active components is lower. However, during the communication time slot, the mains current needs to be controlled such that the compensation current fits inside the current gap.

4.1 Passive solution

To make the cordless kitchen system meet the mains harmonic standard, first a passive solution is considered. In order to (partly) fill the mains current gap during the communication time slot, a passive second order filter is put in between the mains source and the LF rectifier, see figure 4.1.

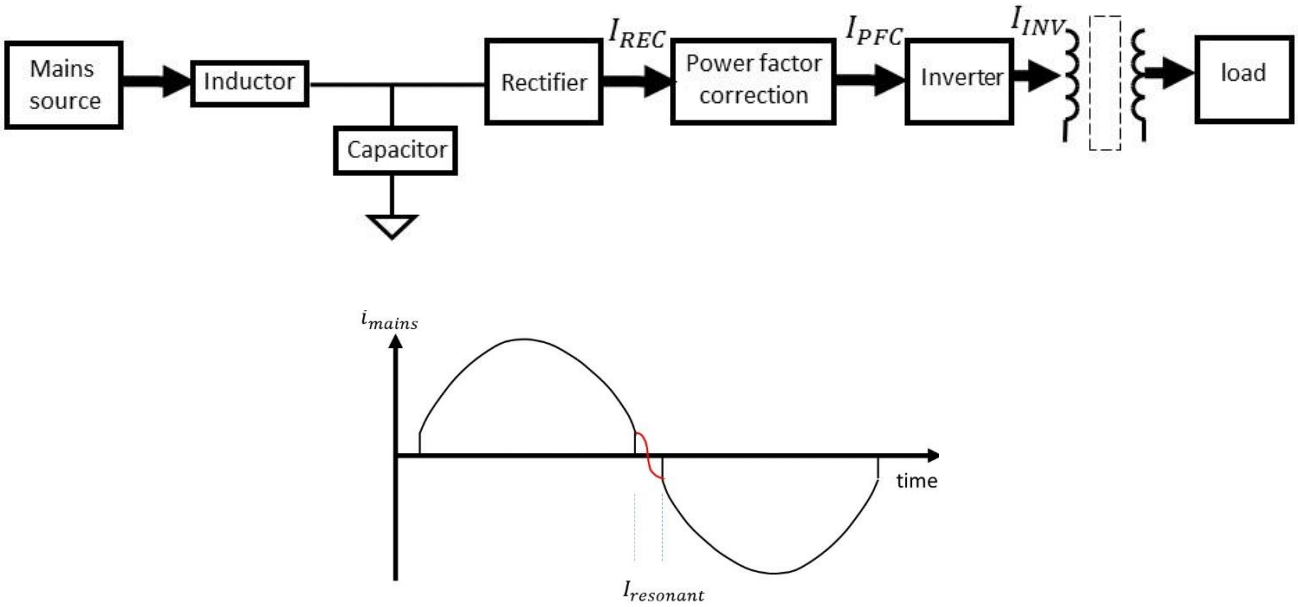


Figure 4.1: Filling the mains current gap with a second order filter.

During the communication time slot, the inverter stops operating. The LC filter starts to oscillate, and the current through the inductor swings from positive to negative. If half of the resonance period of the LC filter equals the communication time slot duration, the mains current gap is filled by this resonant current. The lower plot in figure 4.1 illustrates how the mains current gap is compensated by the resonant current. The circuit is simulated with LTspice, and the results are illustrated in figure 4.2.

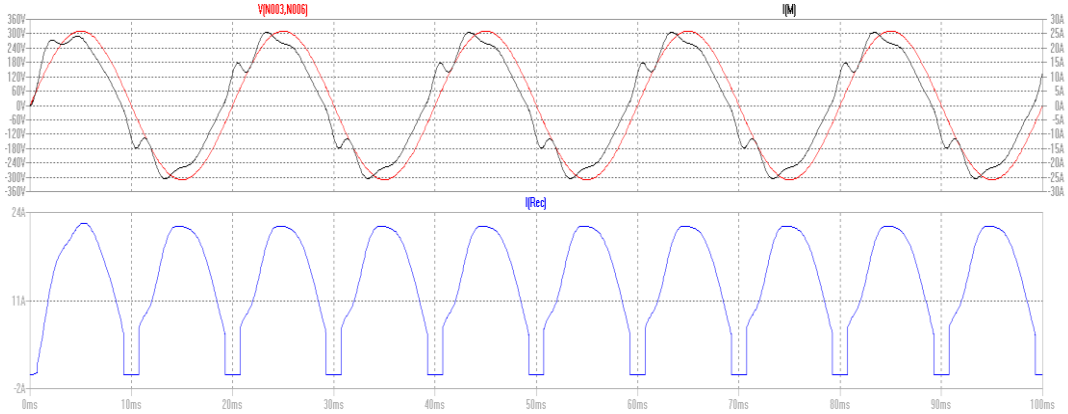


Figure 4.2: Mains voltage (red), Mains current (black) and Rectifier current (blue).

In figure 4.2 the black curve represents the mains current, the red curve represents the mains voltage and the blue curve represents the rectified current (Irec). As figure 4.2 indicates, the current gap of the mains current is filled during the existence of the communication time slot. However, it can be observed that there is a considerable phase difference between the mains current and mains voltage, which causes the decrease of the power factor. Additionally, a considerable distortion of the mains current is introduced, which cause an increase of the amplitudes of the undesired harmonics.

To conclude, the passive solution can fill the current gap in the mains current, however, it has considerable of drawbacks. The LC filter not only operates during the communication time slot, but also during the inverter operation interval. During the full mains period oscillations are super positioned on top of the mains current with period of 2×1.5 mSec, which increases the magnitude of undesired harmonics. Besides, the LC filter increases the phase difference between mains voltage and mains current. Consequently, the power factor will be significantly reduced. Therefore this solution is omitted.

4.2 Active solution: The series structure

In the series structure, the Active PFC is cascaded with the main power channel. Figure 4.3 shows the configuration of the series structure. This cascaded PFC component can provides almost unity power factor and minimizes the THD which shows the negative influence of the undesired harmonics [6].

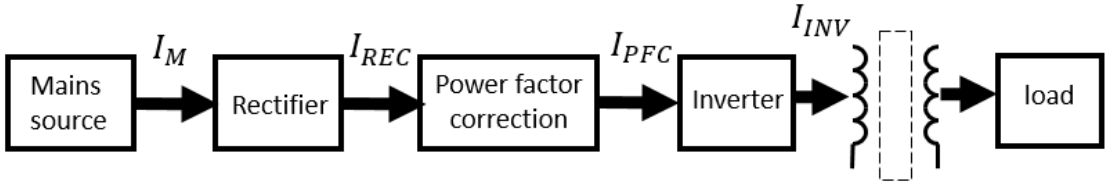


Figure 4.3 Configuration of the series structure

In the series structure, the power processed by the active PFC is approximately equal to the power processed by the inverter [7]. Therefore, a relative large amount of power will be dissipated inside the active PFC and can be considered as loss. At a power level of 3.68 kW, the mains current is equal to 16 A. Such a large current (16A) causes a power loss of $R_{PFC}{I_{REC}}^2$ which lead to thermal problems, where R_{PFC} is the equivalent series resistance of the added component. Because of that, the series structure is not worked out in more detail.

4.3 Active solution: The shunt structure

For the shunt structure, an additional power channel is applied, connected in parallel with the main channel. This additional power channel only operates during communication slot, in order to fill the current gap in the mains current. When the communication time slot is finished, the energy transmitted should be released to the inverter, in order to maximize the efficiency. In [8] a shunt structure is proposed and indicated in figure 4.4(a).

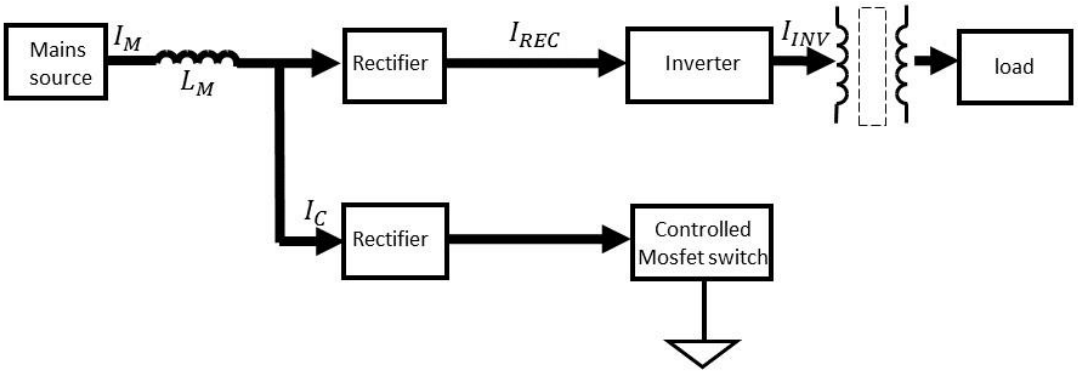


Figure 4.4 (a) Configuration of the original shunt structure

In this structure the Mosfet is switched on during the communication time slot. During this event, the mains current increase, because the mains voltage are applied on the input inductor L_M. When the event is over, the Mosfet switch is switched off simultaneously, so the increased mains current flows through the mains power channel [8]. Be aware that, as figure 4.4 (b) is showing, the two rectifiers might be identical or even combined, because the parasitic diode of the Mosfet result in always conduction for the reversing direction current.

This structure has considerable drawbacks: Firstly, an input inductor L_M should be installed, which can cause a phase shift between mains voltage and mains current. Secondly, the modulation of the compensation current, during communication time slot, cannot be precisely controlled. Thirdly, when the increased mains current through L_M flow to the main power channel, the inverter voltage will be distorted. Therefore, in this case, this type of shunt configuration is modified.

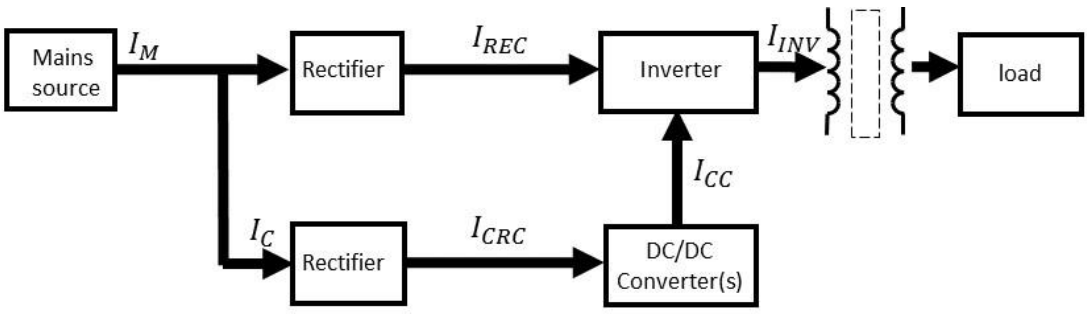


Figure 4.4 (b): Configuration of the modified shunt structure

The additional rectifier act's as an input source for the DC/DC converter. The output of the DC/DC converter is injected into the inverter such that the compensated power will not be lost. For the configuration in figure 4.4 (b), there is no input inductor L_M, and the compensation current I_{CRC} and the releasing current I_{CC} are both under control by the DC/DC converters.

Based on this configuration, the compensation current *Ic* flowing in the additional power channel is indicated by figure 4.5.

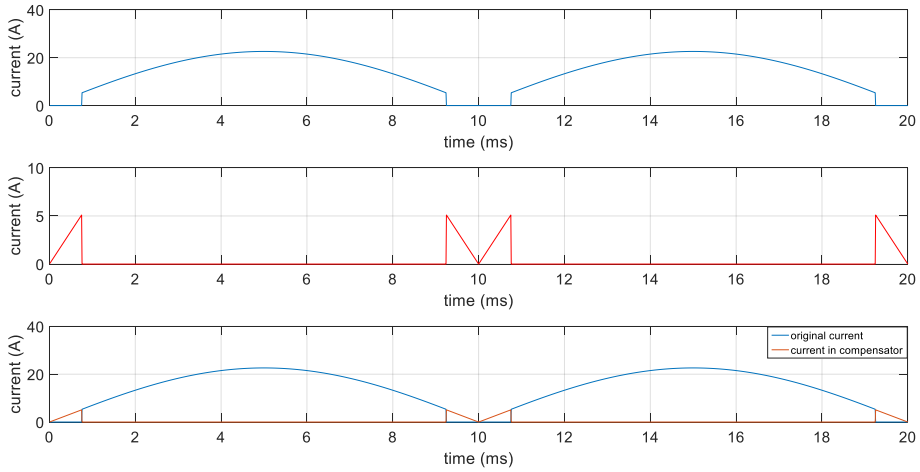


Figure 4.5: The compensation of mains current.

The top curve shows the mains current wave form without compensation. The middle curve shows the wave form of the compensator current in 100% compensation mode. The bottom curve indicates mains current wave form with 100% compensation.
In figure 4.5, it can be observe that the current represented by the red curve completely fills the current gap. That is so called full compensation. The duration of the communication time slot around zero crossing point is 1.5 mSec wide which is indicated by Tw in the next equations. For Tw yields:

$$T_w = t1 - t2 \quad = 1.5 \ \ mSec \tag{12a}$$

According to figure 4.5, the average and rms current which is needed to be compensate can be calculated by the following equations:

$$I_{ave\_com} = \frac{2}{0.5T_m} \cdot \int_0^{\frac{T_w}{2}} \hat{I}_{mains} \sin(\omega \cdot t) \cdot dt = 0.78A \tag{12b}$$

$$I_{rms\_com} = \sqrt{\frac{4}{T_m} \cdot \int_0^{0.75ms} (\hat{I}_{mains} \sin(\omega t))^2 dt} \quad = 1.18A \tag{13}$$

And the maximum peak value of the compensation current equals:

$$I_{peak\_com} = \hat{I}_{mains} \sin\left(\omega \cdot \frac{T_w}{2}\right) = 5.1667A \tag{14a}$$

At the end of the communication time slot, the maximum operation voltage of the compensator becomes:

$$U_{peak\_com} = \hat{U}_{mains} \sin\left(\omega \cdot \frac{T_w}{2}\right) = 75.93 \ \ V \tag{14b}$$

4.4 Choice between series structure and shunt structure

Compared with the series structure, the shunt structure with the additional power channel operates independent from the main channel. This means that this added sub system will not influence the current or voltage of the original main

channel.

Besides, the rms current through the additional shunt structure is calculated at 1.18A, see equation (12b). This rms current is much smaller than the current through the PFC in series structure.

Therefore, the dissipated power in the additional components inside the shunt structure is much smaller than it is in series structure. Furthermore, the smaller the current rating of the additional components means that the additional cost is smaller as well. Therefore, the shunt structure is preferred above the series structure.

Now the shunt structure is chosen as a means to reduce the mains harmonics, the next step is to consider how to realize the additional power channel for the shunt structure. Figure 4.5 indicates that the desired current shape is what the red curve represents. Because the additional power channel is situated at the DC side of the rectifier, the negative part of the red curve should be mirrored to positive axis. Figure 4.5 shows the calculated result from Matlab which represents the desired current flowing through additional power channel for 100% compensation

The current represented by the red curve in figure 4.5 fills the current gap in the mains current completely. A Fourier analysis is performed to investigate the harmonics for 100% compensation. Figure 4.6 shows the harmonics before and after adding the compensation current channel.

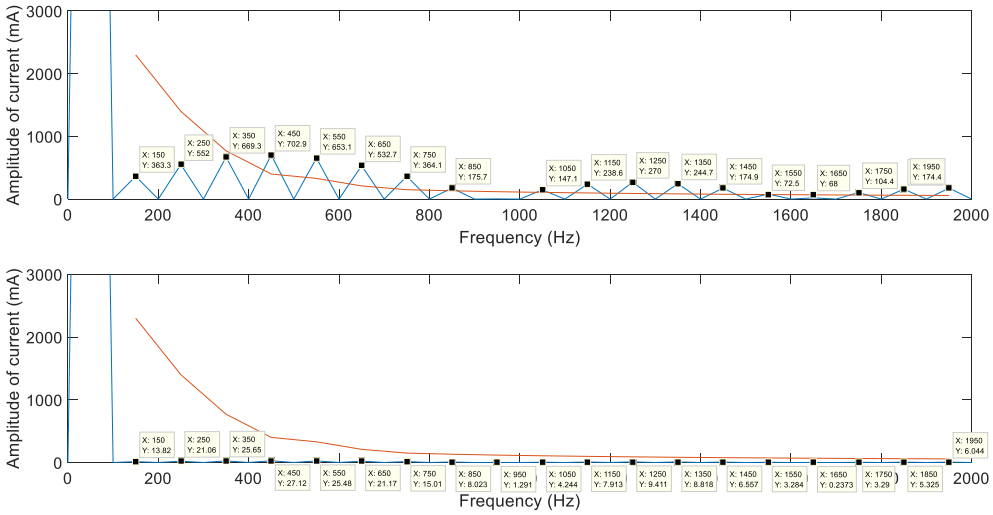


Figure 4.6: The mains harmonic content of the mains current at 3.68 kW power level

In the upper plot of figure 4.6, the red curve represents the highest tolerated value of the harmonics according the IEC standard. The blue curve represents the mains current harmonics without compensation. It can be seen that the harmonics of mains current without Compensation channel is the same as what figure 2.2 shows.

In the lower plot the blue curve shows the mains current harmonic content with 100% compensation. No higher harmonics can be seen, which means that the mains current is completely compensated to a perfect sinusoidal wave shape. It has to be noted that this is only valid for the ideal mathematical model. In reality, some distortion might be taken into account.

In the most practical cases, it is not necessary to compensate the mains current to a perfect sinusoidal wave, so reducing the amplitude of compensation current, as shown in figure 4.5,could be considered. The higher the compensation current through the additional power channel, the more expensive the components become. In order to reduce the cost of the additional power channel to a minimum, the smallest amplitude of compensation current should be

calculated. In figure 4.7, the reduced amplitude of compensation current and the relative harmonics analysis are shown.

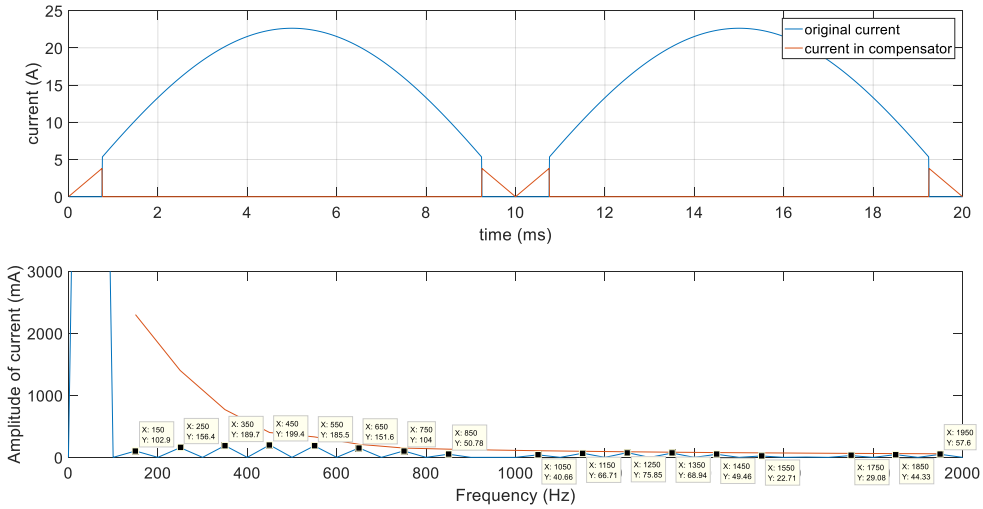


Figure 4.7: The mains harmonic content at 3.68 kW power level

The upper plot shows the mains current wave form where the peak current is 75% of the value of the complete compensation condition. This value is derived by means of simulation. The lower plot shows the mains current harmonic content with 75% compensation. As figure 4.7 shows, the IEC harmonics standard will also be met, even without compensation for the full 100%. To calculate how much current is reduced from 100% compensation to 75% compensation, the rms value of mains current in these two conditions are calculated.

$$\Delta I_{rms} = (100\% - 75\%) \cdot \sqrt{\frac{4}{T_m} \cdot \int_0^{0.75ms} (\hat{I}_{mains} \sin(\omega t))^2 dt} \text{ = 0.296 A}$$

Compared with the 100% compensation case, the rms value of the compensation current in this case is 0.296 A smaller.

5. Implementation of the shunt structure

5.1 Introduction

Before setting up the simulation model of the shunt structure, the operating principle must be made clear, which includes the operating event and the current levels in each building block. In figure 5.1a, the operating principle is illustrated in more detail.

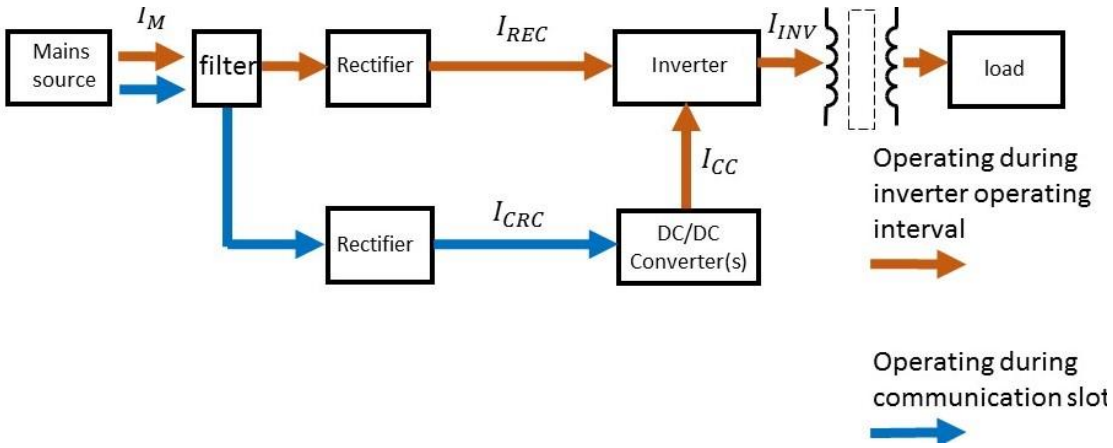


Figure 5.1 (a): Illustration of the operating principle

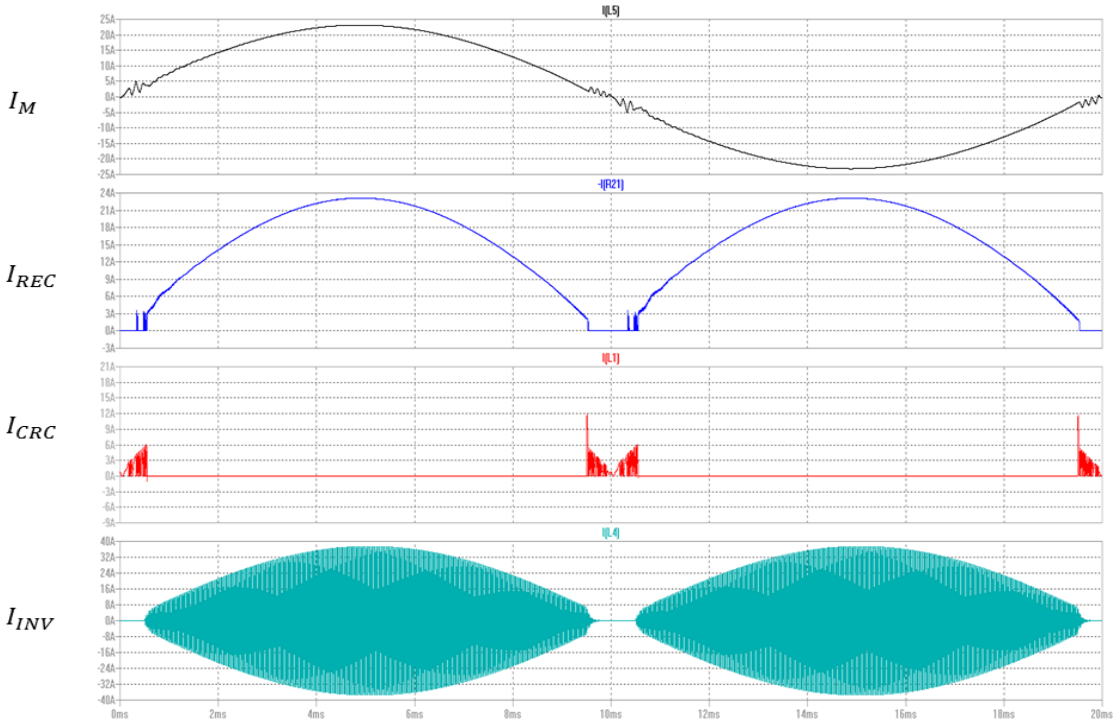


Figure 5.1 (b): The currents through the relevant building blocks of the shunt structure

As can be seen in figure 5.1b, there is no power transfer from the main inverter to the load during the communication time slot. However, the mains current seems not to be effected by the 'no power transferred time slot'. That is because the compensation power channel is active during the communication time slot. It can be observed that the mains current exists of the superposition of the compensation current I_{CRC} and the rectifier current I_{REC}.

Furthermore, the compensation current I_{CRC} is used to store the energy in a capacitor located in DC/DC converter. When the inverter starts to operate, the DC/DC converter releases this energy to the inverter.

As a next step, the configuration of the DC/DC converter will be addressed. The DC/DC converter is supposed to provide the following functions:

1. To shape the compensation current I_{CRC} according figure 4.6
2. To gradually release the stored energy in an intermediate storage capacitor, such that the functionality of the mains inverter is not influenced

5.2 The configuration of the compensator

In order to realize these two functions, a cascade of two converters is considered. This is a common approach to improving the power factor. The two cascaded converters results in high power factor and fast response output voltage by using two independent controllers [9]. In between the two converters, a storage capacitor is located. Basically, during the communication time slot, the Converter 1 shapes the input current and stores energy into that storage capacitor. After this event, the energy stored in the storage capacitor will be released to the inverter, in order to maximize the efficiency. If that process is not under control, the energy will be released in a very short time, which will cause a current ripple and audible noise, see figure f in appendix I. Especially in the case that a receiver coil is connected to the inverter, the receiver coil acts as a speaker which can enhance the audible noise. Because of that, converter 2 is needed to modulate and slow down the energy releasing process.

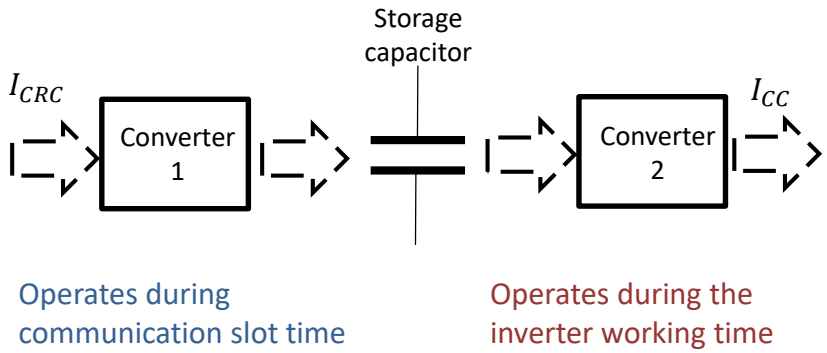


Figure 5.2: Configuration of Compensation channel.

From figure 5.2, it can be observed that during the communication time slot, the Converter 1 draws the compensation current from grid, and during inverter operation, the Converter 2 transfers the stored energy to the load.

5.2.1 Option for converter 1: Flyback converter

As in implantation for Converter 1, first the flyback converter is considered. The scheme of the converter is provided in appendix I figure a. The advantage of using the flyback converter in this case is that the primary side is isolated from the secondary side. That is, if the switch M1 is switched off, there is no input current to the flyback converter. The disadvantage of using the Flyback converter is that the switch must handle both a relatively high rms current and higher drain-source voltage (> 650 V).

5.2.2 Option for converter 1: Boost converter

As a second option for an implementation for Converter 1 the boost converter is considered. The scheme of the Boost converter is provided in appendix I figure b. Compared with the flyback converter, the active switch must handle a lower rms current. This is because during the operation period, the input current I_{CRC} of the converter exists of both the switch current during the On time interval and the diode current during the Off time interval.

Be aware that for proper operation, output voltage of the Boost converter must always be higher than the input voltage. As the input voltage of the boost converter becomes higher than the output voltage, the boost diode will keep conducting until the voltage of the storage capacitor is equal or higher than the input voltage (mains voltage). Therefore, when the mains voltage reaches the peak value of 325 V, the voltage across the storage capacitor will become 325 V as well. Because initially a lower voltage is considered across the storage capacitor (see chapter 5), an enable switch will be applied between the rectifier and the Boost converter. The Boost converter will only be enabled during communication time slot.

5.2.3 Option for converter 2: Buck converter

According to the analysis in chapter 5.2, converter 2 is used during the energy releasing process of the energy from the storage capacitor towards the main inverter. To clarify the requirements of converter 2, a compensator without converter 2 is test, and the test result is provided in appendix I figure f.

From that figure, it should be noticed that after the communication time slot, an obvious current ripple appears both in mains current and transmitted current. That is because the energy releasing process is too fast. Slowing down that process can remove the ripple. Therefore, the converter 2 is need to slow down this process.

To slow down that process, the voltage across the load should be reduced, so the buck converter is taken into account. The scheme of the buck converter is provided in appendix I figure c.

5.3 Operating modes for the Boost and Buck converter

In general, DC/DC converters can operate in Continuous Conduction Mode (CCM), Boundary Conduction Mode (BCM) and Discontinuous Conduction Mode (DCM).

5.3.1 Boost converter operating mode

In the Compensation channel a Boost converter is cascaded with a Buck converter. The schematic can be found in appendix I. With the Boost converter, the average current through the Compensation channel is controlled, based on the calculation performed in methodology section. Keeping the average current equal, the advantages and disadvantages of the three operating mode will be discussed. In all the three modes, the average current through the inductor equals:

$$I_{ave} = \frac{A}{T_s}$$

where A is the area surrounded by the blue curve (inductor current of the converter) and x-axis in figure 5.3 (a). With the same average current, the area A should be the same for the other two operating modes.

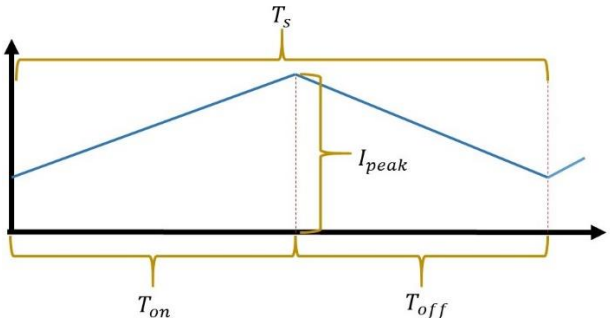


Figure 5.3 (a): Continuous Conduction Mode analysis

From the figure 5.3 (a), it can be derived that:

$I_{peak} < \frac{2 \times A}{T_s}$.

This is because the area of trapezoid is larger than the relative triangle area.

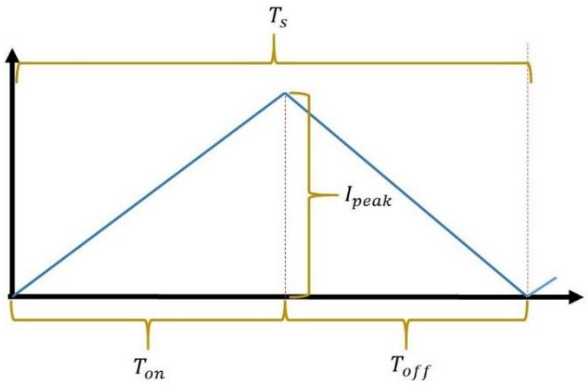


Figure 5.3 (b): Boundary Conduction Mode analysis

The same yields for BCM; for I_{peak} can be written:

$I_{peak} = \frac{2 \times A}{T_s}$

It can be concluded that the peak current in BCM is larger than the peak current in CCM.

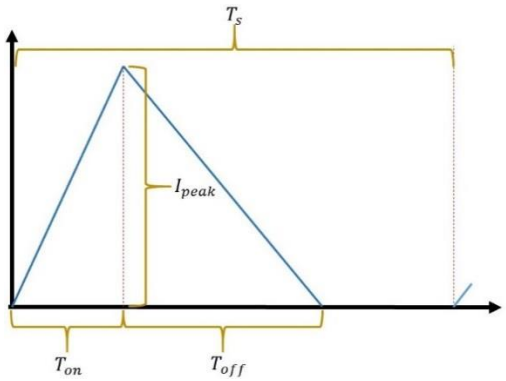


Figure 5.3 (c): Discontinuous Conduction Mode analysis

In DCM, for I_{peak} can be written:

$I_{peak} > \frac{2 \times A}{T_s}$.

The peak current in this mode is highest among the three operation modes.

For the price of components, for example the active switch (Mosfet) and diode, the higher rms current capability means higher price. Therefore, in order to reduce cost, the CCM is the first choice. The average compensator current I_{CRC} need to be shaped into sinusoidal wave to compensate the current gap. In BCM mode, I_{CRC} is proportional to it's I_{peak}. In CCM and DCM, I_{CRC} depends on not only I_{peak} but also another parameter. Therefore, controlling I_{CRC} in BCM is easier than that in the other two modes. Eventually, the BCM mode is applied in this case.

In order to maintain BCD operation, a Self-Oscillating (SO) Boost converter circuit is used to drive the active switch of converter. The SO circuit can assist the control circuit to realize the current peak control [10].

For the current peak control, the switch of converter is turned on, at the moment the current through the inductor returns back to zero. The switch of converter is turned off, at the moment the current through the inductor reaches the reference current [10]. Hence, the converter always works in BCM, and the peak current never exceeds the reference level. The principle of SO control circuit is shown by figure 5.3(d), and the schematic of SO control circuit is shown in appendix I figure d.

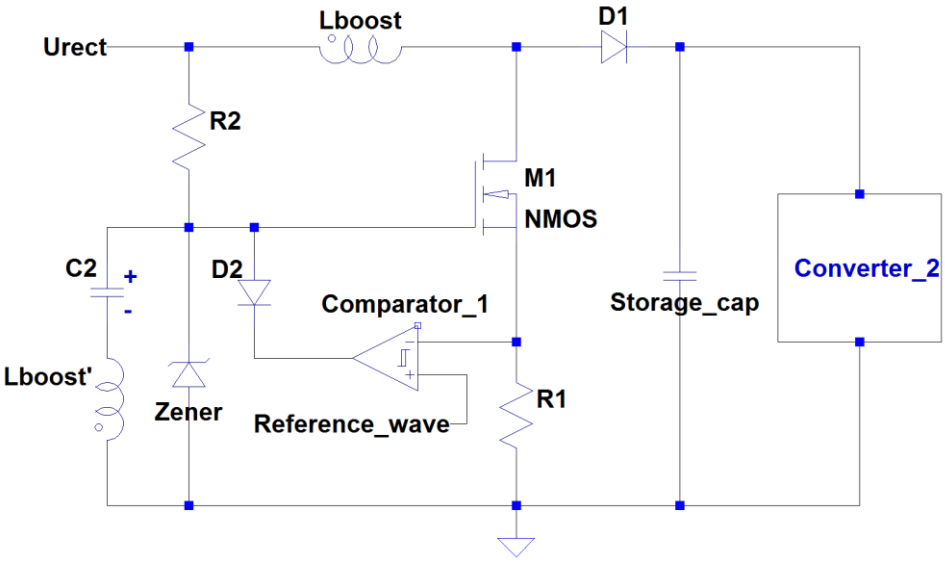


Figure 5.3 (d): The principle of SO Boost control circuit.

The inductor L_{boost} is coupled with inductor L_{boost}'. The breakdown voltage of the Zener diode is 10V, so the drive voltage for M1 is 10V at most. M1 is switched on until the current through L_{boost} reaches the reference peak. At that moment, the comparator_1 output 0 V to the gate of M1, M1 will be switched off, at the same time capacitor C2 is discharged. Then the current through L_{boost} start to decrease, and C2 start to charge. When the current through L_{boost} decreases to 0 A, the voltage across L_{boost}' disappears, so the voltage across C2 will switch on M1 again [11].

5.3.2 Buck converter operating mode

Because the power processed by the two converters is equal, and the operating time of Buck converter is about 6 times longer than the Boost converter, the current flowing through the Buck converter is much lower than the current through the Boost converter. Therefore the operating mode of the Buck converter is not very critical, all three operating modes can be applied. However, to simplify the control circuit of the Buck converter, also DCM is considered for the Buck converter as well.

5.3 Design of the Boost and Buck converter

5.3.1 Boost converter design

To design the Boost converter, the following conditions should be clarified. The schematic of the Boost converter can be found in Appendix I. According to the equations (1) (2) (4) (5) (6), the parameters of the Boost converter can be specified:

1. The maximum voltage applied to the boost inductor is 75.9 V, see equation (14b)

2. When the voltage applied on the boost inductor reaches its maximum value (75.9 V), the average current input should be equal to 5.1 A.

3. Because 500V is the breakdown voltage of the Mosfet's in the main inverter, the maximum output voltage of the Boost converter might become 450 V. The breakdown voltage of the Mosfet in compensator is chosen at 500 V as well.

Based on the above conditions, the value of Boost inductor and the storage capacitor can be calculated.

The charge Q_{stored} , stored in the storage capacitor, can be calculated by equation (15):

$$Q_{stored} = 2 \cdot \int_0^{\frac{T_w}{2}} \sqrt{2}\ I_{rms} \sin(\omega \cdot t) \cdot dt = 4 \cdot 10^{-3} J \qquad (15)$$

To make sure the voltage across the storage capacitor is always smaller than 450V, the value of the storage capacitor should be:

$$V_{storage\_capacitor\_max} = \frac{Q_{stored}}{C_{storage}} + V_s < 450\ \ V \qquad (16)$$

where V_s is the voltage across the intermediate storage capacitor in steady state. The value of V_s depends on the input and output voltage ratio of the buck converter. It will be discussed in next section, here V_s is assumed to be 145V.

$$C_{storage\_capacitor} > 13\ \ uF$$

Because 500V is the breakdown voltage of the Boost Mosfet, the maximum voltage across the intermediate storage capacitor V_s must be chosen far away from this value, for example 300 V. Therefore, a value of 15uF is chosen for the storage capacitor.

In terms of determining the value of inductor in Boost converter, the control circuit should be mentioned briefly. With the SO Boost converter circuit, the switch will be turned Off when the Boost inductor current reaches a certain upper limit. Then the inductor current reduces and when the current becomes zero, the switch will be turned On again by the SO Boost control circuit.

Hence, the value of Boost inductor influence on the frequency of the Boost converter. According to figure 2.2, the low frequency harmonics which are smaller than 2000 Hz are need to be improved. Therefore, we have to use an inductor which can guarantee the Boost converter to operate at a frequency larger than 2000 Hz. Additionally, to avoid audible

noise the lowest value of Boost converter frequency should be larger than 20 kHz.
Based on equation (1) to (6), we can derive the time function of the input voltage and output voltage of the Boost converter, in between the begin and end event of the communication time slot: $½\cdot(T_m - T_w)$ < t < $½\cdot(T_m + T_w)$

$$V_{Boost\ in}(t) = |\widehat{U}_{mains}\sin(\omega t)| \tag{17}$$

$$V_{Boost\ out}(t) = \begin{cases} V_s + \frac{\hat{I}_{boost\ out}}{\omega \cdot C_{storage}}\cos(\omega t) & for\ \ \frac{n*T_m - T_w}{2} < t < 0 \\ V_s - \frac{\hat{I}_{boost\ out}}{\omega \cdot C_{storage}}\cos(\omega t) & for\ \ 0 < t < \frac{n*T_m + T_w}{2} \end{cases} \tag{18a}$$

$$\frac{1}{1-D_{boost}} = \frac{V_{Boost\ in}(t)}{V_{Boost\ out}(t)} \tag{18b}$$

$$\frac{V_{out}(t)}{V_{in}(t)} = \frac{\hat{I}_{mains}\cdot\sin(\omega t)}{\hat{I}_{boost\ out}\cdot\sin(\omega t)} = \frac{\hat{I}_{mains}}{\hat{I}_{boost\ out}} \tag{18c}$$

where D_{boost} is the duty cycle of the Boost converter, $\hat{I}_{boost\ out}$ is the amplitude of the output current of the Boost converter which is considered as also a sin wave.

For the Boost converter, the inductor current rise and fall time can be calculated by the following equations:

$$t_{rise}(t) = \frac{I_{Boost\ lim}}{L\cdot V_{Boost\ in}(t)} \tag{19}$$

$$t_{fall}(t) = \frac{I_{Boost\ lim}}{L\cdot(V_{Boost\ out}(t) - V_{Boost\ in}(t))} \tag{20}$$

where $I_{Boost\ lim}$ is the upper Boost inductor current limit. It can be calculated by:

$$I_{Boost\ lim} = 2 \cdot I_{peak\_com} = \ 2 \cdot |\hat{I}_{mains}\sin(\omega \cdot \frac{T_w}{2})| \tag{21}$$

The reason why it is multiplied 2 is that the Boost converter operates in BCM and therefore current curve of Boost converter has a triangle shape [12]. The average inductor current value should be a half of the peak current value. For the operating frequency of the Boost converter yields:

$$f_{boost}(t) = \frac{1}{t_{rise}(t) + t_{fall}(t)} \tag{22}$$

To avoid the audible noise, the boost operating frequency $f_{boost}(t)$ should be always larger than 20 kHz, during the communication time slot which is from $½\cdot(n * T_m\ - T_w)$ to $½\cdot(n * T_m + T_w)$.
To make sure that the lowest value of $f_{boost}(t)$ becomes larger than 20 kHz, the Boost inductor *L* has to be smaller than 143 uH. In this project, the inductance is chosen to be 100 uH. When substituting the storage capacitance of 15uF into equation (16), the storage voltage $V_{storage\_capacitor\_max}$ can be calculated at 411.7 V. The schematic of the Boost converter can be found in appendix.

5.3.2 Buck converter design

For the Buck converter, the input terminals are connected across the storage capacitor, and the output terminals are connected to the input terminals of the mains inverter, like what figure 5.2 shows. The input voltage and the output voltage of the Buck converter is calculated by the following equations:

$$V_{Buck\ in} = V_{storage\_capacitor\_max} - \frac{1}{\omega\ C_{storage}} \int_{\frac{n*T_m+T_w}{2}}^{t} .I_{Buck\ in}(\tau)d\tau \quad (23a)$$

$$V_{Buck\ out} = \widehat{U}_{mains}\ \sin(\omega t) \quad (23b)$$

where I_{buck_in} is the average input current of the Buck converter during its operating period, which depends on the input and output voltage during that period. Based on the analysis of Buck converter in DCM [13]:

$$\frac{V_{Buck\ out}}{V_{Buck\ in}} = \frac{D_{Buck}}{D_{Buck}+\Delta} \quad (24)$$

where Δ is the time interval when the current through the buck inductor decreasing, in an operating period.

$$I_{buck\ in} = \frac{D_{Buck}(V_{Buck\ in}-V_{Buck\ out})}{2\ L_{Buck}} \quad (25)$$

where D_{Buck} is duty cycle, and T_s is the period of Buck converter which is a constant specified of 10 us. For the buck converter yields:

$$\frac{V_{Buck\ out}}{V_{Buck\ in}} = \frac{D_{Buck}}{D_{Buck}+\Delta}$$

$$V_{Buck\ in} \cdot I_{buck\ in} = \frac{{V_{Buck\ out}}^2}{R_{load\_eq}} \quad (26)$$

Based on equation (23b), the average output voltage during the communication time slot is:

$$V_{out\_ave} = \frac{2}{T_w} \int_0^{0.75ms} \widehat{U}_{mains} \sin(\omega t)\, dt = 38.11\ V$$

Because in the section 5.3.1 is assumed that the voltage across the storage capacitor V_s equals 145 V, the duty cycle D_{Buck} can be calculated at 0.3. Under those conditions, the operation time of releasing Q_{stored} should be as long as possible. However, to be aware that after the output voltage $V_{Buck\ out}$ becomes larger than its input voltage $V_{Buck\ in}$, the Buck converter will not operate anymore. Therefore, the releasing process should be ended before that. Based on the equations (23a) (23b) (24) (25), the inductance of the Buck converter is specified of 100 uH.
When the output voltage of the Buck converter becomes larger than its input voltage, the power flow might inverse. Therefore a diode is placed series with the output Buck converter. The schematic can be found in appendix.

5.4 Ramping duty cycle

Because of the existence of the communication time slot, the AC output current of the main inverter is reduced to zero during this event. The sharp edge on the envelope of the AC output current induces audible noise, because the complete Tx coil assembly acts as a loud speaker. In order to reduce this audible noise, the duty cycle of the main inverter is ramped down gradually to zero before entering the commutation time slot.

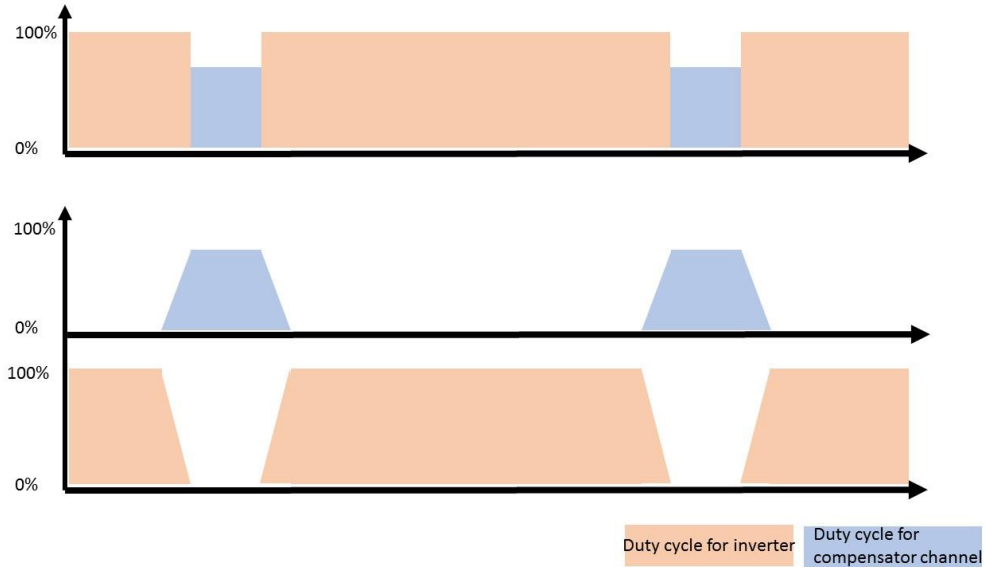


Figure 5.4: Duty cycle pattern of the mains inverter and compensator channel

The same yields for the ramp up of the duty cycle of the main inverter, after the commutation time slot is finished, see Figure 5.4. The upper figure of figure 5.4 shows the original duty cycle; the lower figure shows the up and down ramping of the Duty cycle of the main inverter. Because the duty cycle of the main inverter changes gradually, and the envelope of the AC output current of the mains inverter shows no sharp corners. Therefore the current in the compensator channel has to change gradually as well, instead of changing instantly.

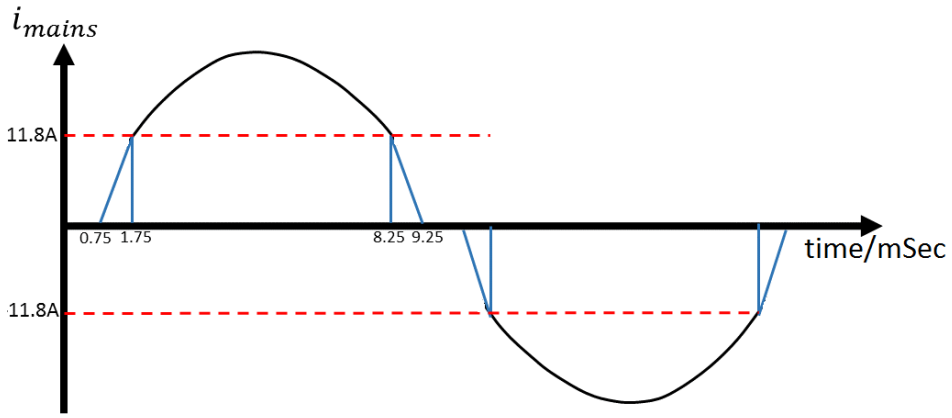


Figure 5.5: The mains current with the applied Duty cycle pattern in time domain.

Because the applied duty cycle pattern, the power reduction due to the existence of the communication timeslot must be re-calculated. The mains input power P_{real} without compensator can be divided into two parts, the ramping up part and the sinusoidal wave part. As figure 5.5 shows, the four triangle areas encapsulated by the blue curves and x-axis are the ramping parts, and the two areas encapsulated by the black curves and x-axis are the sinusoidal wave parts.

To calculate the power reduction under these conditions, the mains input power P_{real} with ramping duty cycle should be determined. For the ramping part, the mains current roughly behaves linearly. If the ramping up and down time equals 1 mSec the energy can be calculated by:

$$E_{ramp} = 4 \times \int_{0.75\ ms}^{1.75\ ms} U_{mains} \cdot I_{mains} = 3.29\ J \tag{27}$$

For the sinusoidal wave part yields:

$$E_{sin} = 2 \times \int_{1.75\ ms}^{8.25\ ms} U_{mains} \cdot I_{mains} = 68.65\ J \quad (28)$$

Based on E_{ramp} and E_{sin}, the mains input power P_{real} can be calculated by:

$$P_{real} = \frac{E_{ramp}+E_{sin}}{T_m} = 3597\ W \quad (29)$$

So the power reduction becomes:

$$Power\ \ reduction = \ \ P_{nom} - P_{real} = 3680 - 3597 = 83\ W \quad (30)$$

5.5 Control circuit design

The control circuit is designed for controlling the Compensation channel. Referring to the SO circuit, the average current through Compensation channel during communication slot can be adjusted by means of changing the upper limit of Compensation channel current. There are two control methods introduced in this section:

1. Charge controlled circuit
2. Proportional compensation circuit

Before introducing these two control methods, the approach used to drive the duty cycle should be illustrated first. To modulate a duty cycle to realise a ramping duty cycle pattern like Figure 5.4, a trapezoid wave and a saw tooth generator are required. These two waves are connected to the input terminals of a comparator [14]. In this project the trapezoid waveform acts as the reference signal. That is, if the value of the trapezoid wave is larger than the value of saw tooth generator, the comparator output becomes 'HIGH', otherwise the comparator output becomes 'LOW'. This is shown by figure 5.6.

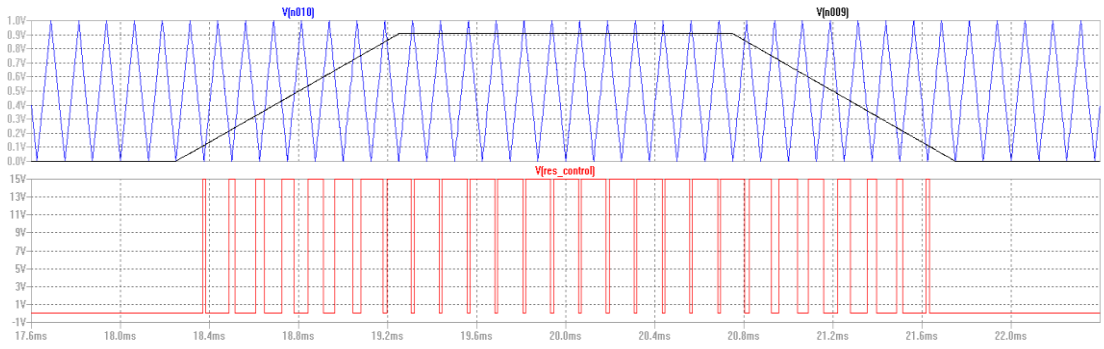


Figure 5.6: the working principle of duty cycle drive.

The upper plot shows the trapezoid wave and saw tooth generator; the lower plot shows the duty cycle pattern as a function of time. In this project, an Arduino is utilized, so the duty cycle can be programed directly.

5.5.1 Charge controlled circuit

This method is relative complicated but this control circuit behave is precise and robust. To explain this control method, two basic equations should be illustrated first. In figure 4.5, the area surrounded by red curve and x-axis is regarded as

the compensation current integral area (which is basically charge). During each period, the desired compensation current integral area is proportional to the peak of rectified mains current. This can be shown by following equation:

$$A_{int\_reference} = \hat{I}_{mains} \int_{\frac{n*T_m-T_w}{2}}^{\frac{n*T_m+T_w}{2}} \sin(\omega t)dt = 9.3812 \times 10^{-4} \times \hat{I}_{mains} \quad (31)$$

where n can be any integer number, and $A_{int\_reference}$ is the desired compensation current integral area, and $\hat{I}_{mains}$ is the peak of rectified mains current. Equation (31) indicates that the desired compensation current integral (area reference) can be calculated using the peak of rectified mains current measured. Therefore the parameter $A_{int\_reference}$ is used as reference in a PI control loop.

Based on sensing the rectified mains current I_{sense}, the compensation current integral area can be sensed with an integrator.

$$A_{int\_sensed} = \int_{\frac{n*T_m-T_w}{2}}^{\frac{n*T_m+T_w}{2}} I_{sense} \quad (32)$$

where I_{sensed} is the current measured by current sensor.

When comparing $A_{int\_reference}$ with A_{int_sensed}, the current (charge) through the SO Boost circuit is determined by a PI control circuit. Figure 5.7 shows the block diagram of the complete PI control circuit. For more detail, please refer to Appendix II

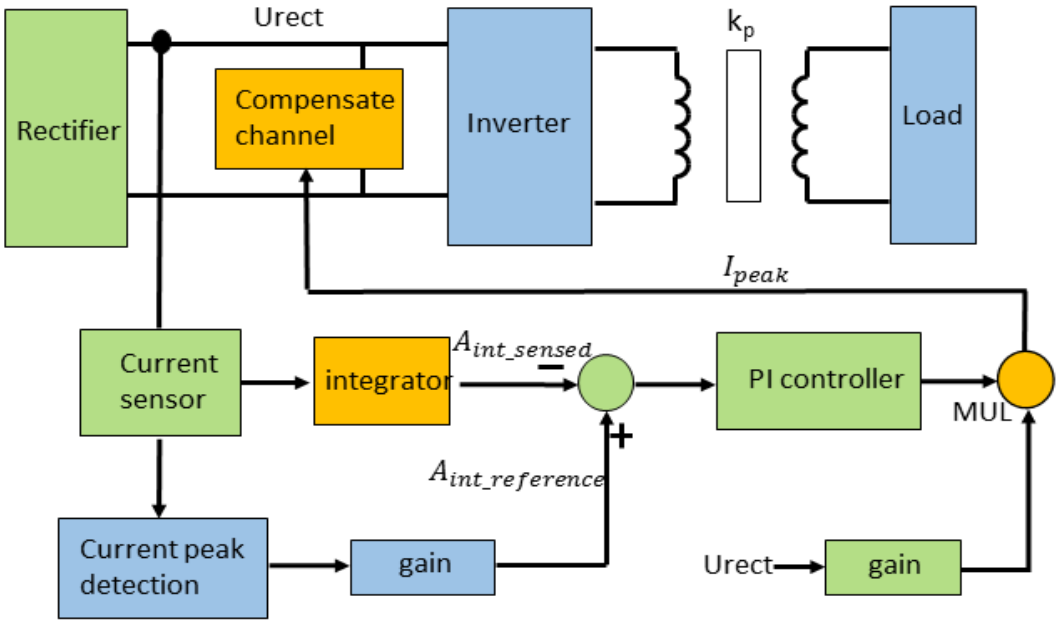


Figure 5.7: block diagram of Charge controlled circuit.

The green blocks operate during the entire period of the mains voltage; the blue blocks operate during inverter operating time; the yellow blocks operate during the communication slot.

5.5.2 Proportional compensation circuit:

As already illustrated in the previous control method part, the required compensation current is proportional to the peak of rectified mains current. Base on that, we can use saw tooth wave generator and trapezoid wave generator to generate duty cycle to directly control compensation current, instead of using SO circuit. The height of the trapezoid wave is also proportional to the duty cycle. Therefore, the duty cycle can be adjusted by changing the height of trapezoid wave, as a linear function of the peak of rectified mains current.

On 3.68 kW power level, the peak of rectified mains current is 22.6 A, and the scaled height of the trapezoid wave equals 1V. At 2.5 kW power level, the peak of rectified mains equals 10.9A and the height of trapezoid wave becomes 0.438V. Therefore, the duty cycle can be adjusted by means of changing the height of trapezoid wave as a function of peak value of rectified mains current.

$$(H_{tra} - 1) = 0.11 \times (I_{peak} - 16) \tag{33}$$

$$H_{tra} = 0.11 \times I_{peak} - 0.76 \tag{34}$$

where H_{tra} is the height of trapezoid wave, and I_{peak} is the measured peak of rectified mains current. The height of trapezoid wave can be calculated using the measured value of the peak mains current. According to the figure 5.6, the duty cycle changes with the height of trapezoid. The block diagram is shown by figure 5.8. For more detail, please refer to Appendix II

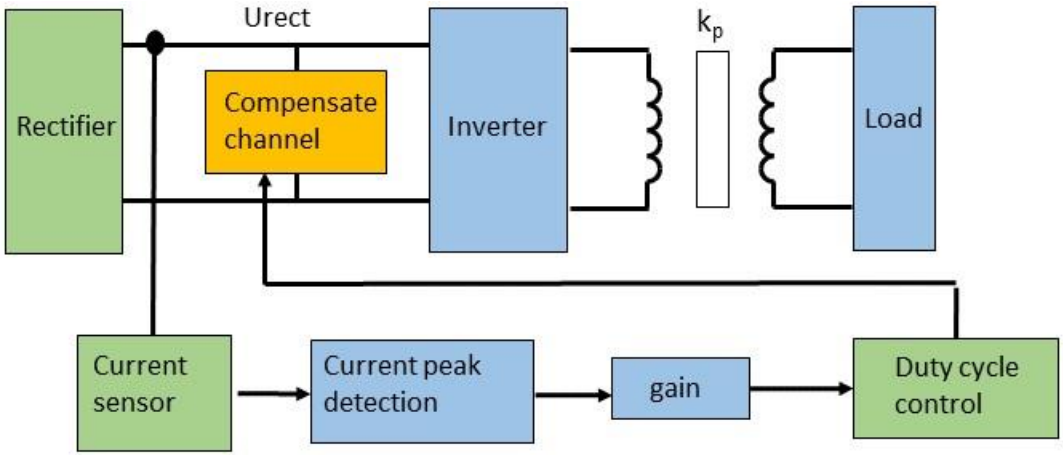


Figure 5.8: block diagram of Proportional compensation circuit.

The schematic model both of these two circuits can be found in appendix II.

6. Simulation results

6.1 Simulation of the power channel without compensation

In this chapter the simulation results will be illustrated. In order to show the improvement obviously, the mains current in the original power channel is presented here. In figure 6.1, the “mains current gap” to be filled can be found near the zero crossing points.

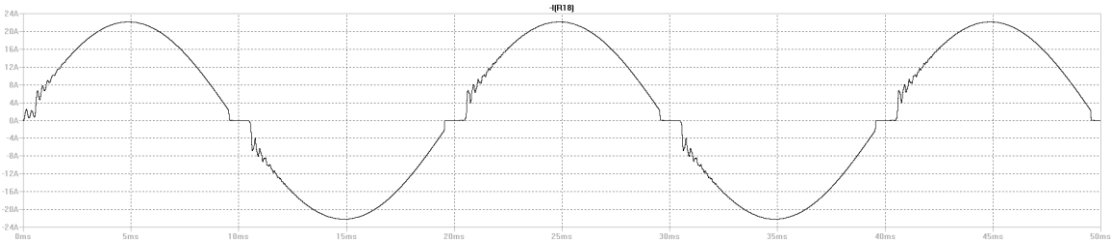


Figure 6.1: The mains current wave form without compensation of the “mains current gap”

6.2 Simulation of the power channel with compensation

6.2.1 Behaviour of the compensator channel

The compensator channel consist of a Boost converter and a Buck converter, like what is shown in the figure 4.7. In this part, the mains current and inverter output current will be displayed first. Secondly, the input current of the Boost converter, the voltage across the storage capacitor and the output current of the Buck converter are observed.

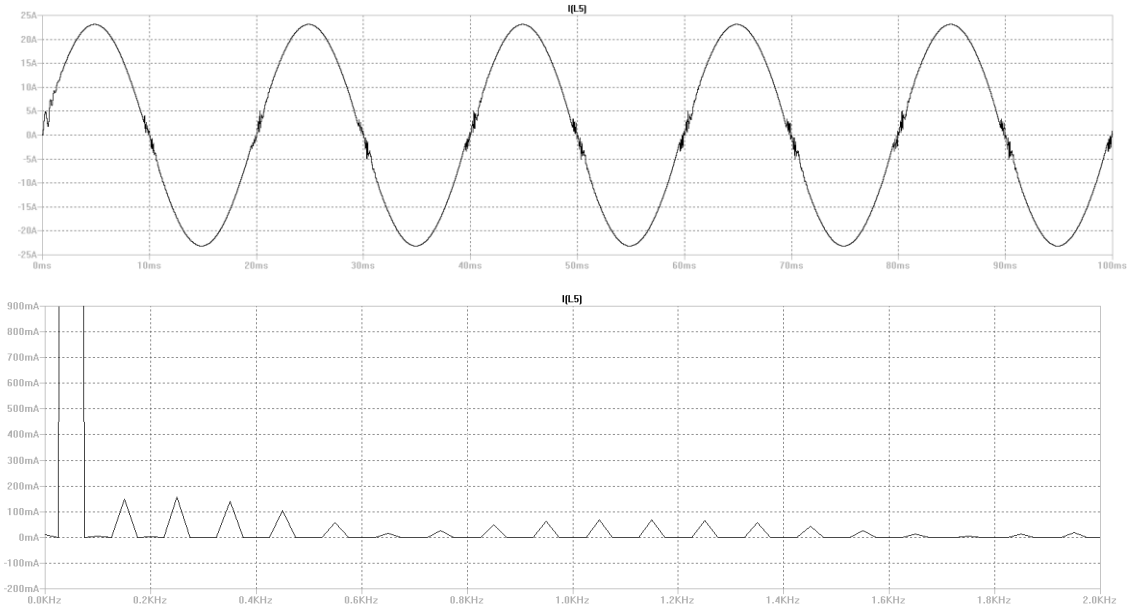


Figure 6.2: The mains current wave form with compensation of the “mains current gap”

The upper figure of figure 6.2 shows the mains current curve over 5 mains periods. The lower figure shows the Fourier analysis of the mains current. It indicates that the “mains current gap” of the mains current is compensated by the Compensation channel. Comparing with figure 6.1, the steep edges of the mains current near the zero crossing point are removed. The result of the Fourier analysis tells that the undesired harmonics are significantly reduced, so that the mains current at 3.68 kW power level meets the IEC standard.

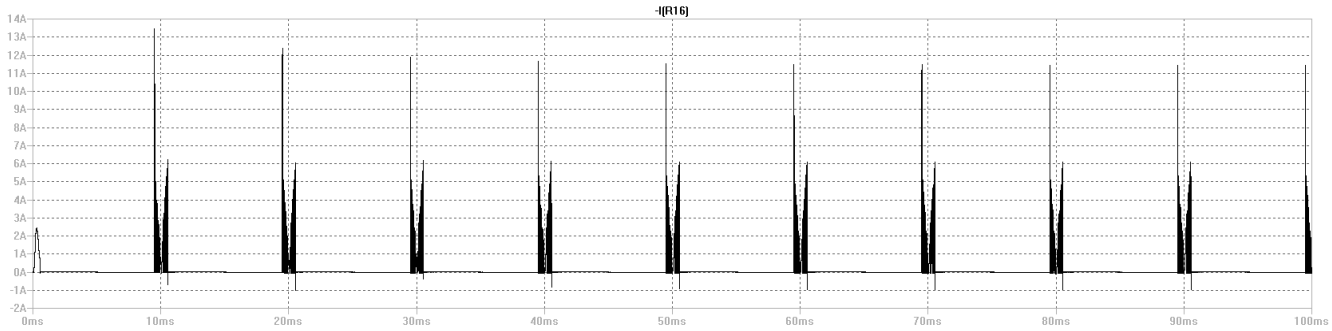


Figure 6.3: The input current of the Boost converter (I_{CRC})

The input current of the Boost converter is in fact the compensation current to fill the "mains current gap" near the zero crossing points. From figure 6.3, it can be seen that there is a relatively large current peak up to 13.4A during every half mains cycle. Using a larger inductance in Boost converter lowers the peak current here. However, in this case because the average current is low, the overshot current is acceptable.

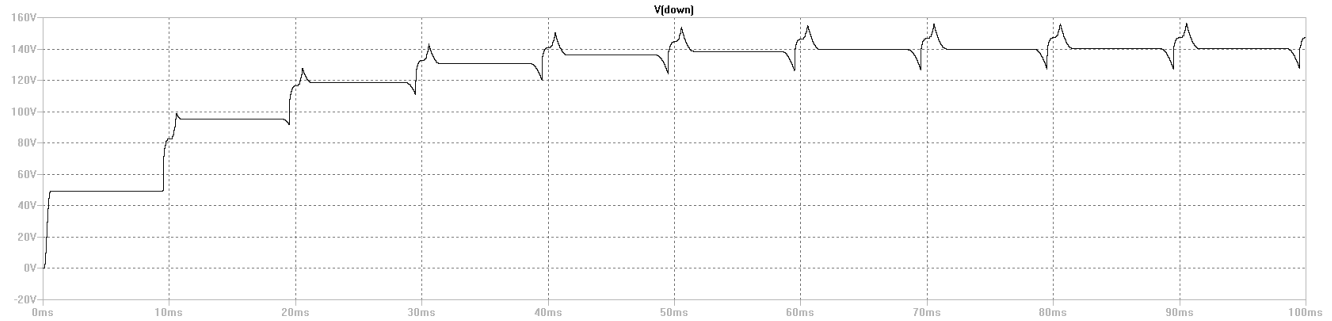


Figure 6.4: Voltage across storage capacitor.

The storage capacitor is charged every half mains period, until the voltage reaches a certain steady state. In the steady state condition the average voltage across storage capacitor is 140V, and the peak voltage equals 155V which is lower than components' maximum limit voltage.

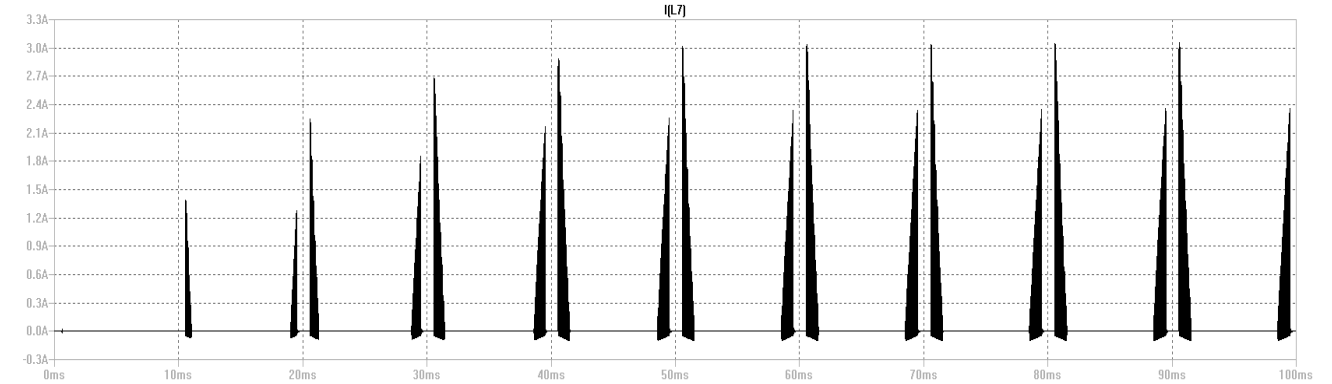


Figure 6.5: The output current of Buck converter (I_{CC}).

Figure 6.5 shows the output current of the Buck converter. The peak current has a value of 3A which is much lower than the peak current through the Boost converter. That is because the operating period of the Buck converter is larger than the operating period of the Boost converter.

6.2.2 Results of Charge controlled circuit

Figure 6.6 shows the behaviour of the mains current, directly after switching On the power chain. The response time of the Compensation channel under Charge control is clearly visible.

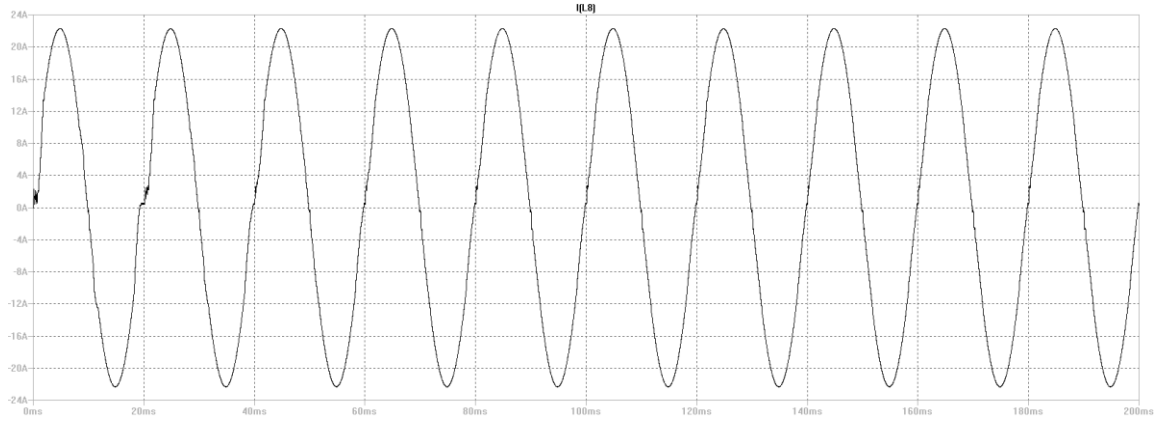


Figure 6.6: The mains current from t = 0 under Charge control

Based on the observation of figure 6.6, the power chain will reach its steady state after 80ms which is as long as 4 mains periods.

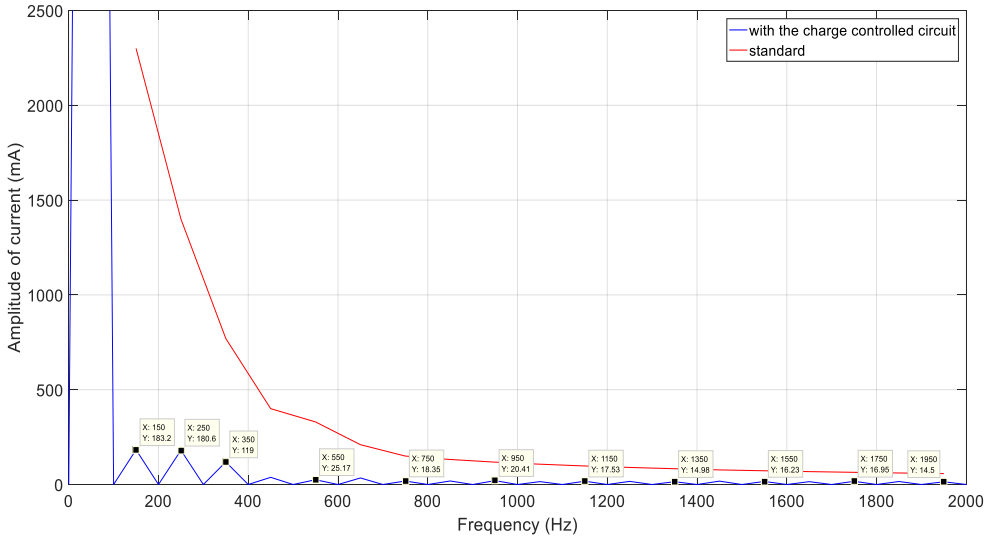


Figure 6.7: Harmonics of mains current under Charge control

6.2.3 Results of Proportional compensation circuit

Figure 6.8 shows the behaviour of the mains current, directly after switching On the power chain. The Compensation channel operates under the Proportional compensation control.

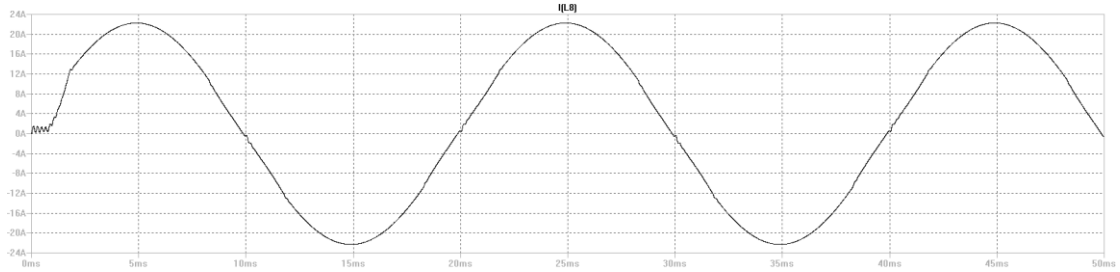


Figure 6.8: The mains current from t = 0 under Proportional compensation control

Based on the observation of the figure 6.8, it takes only one mains period to reach the steady state. This is significantly shorter than the response time of the Charge controlled circuit.

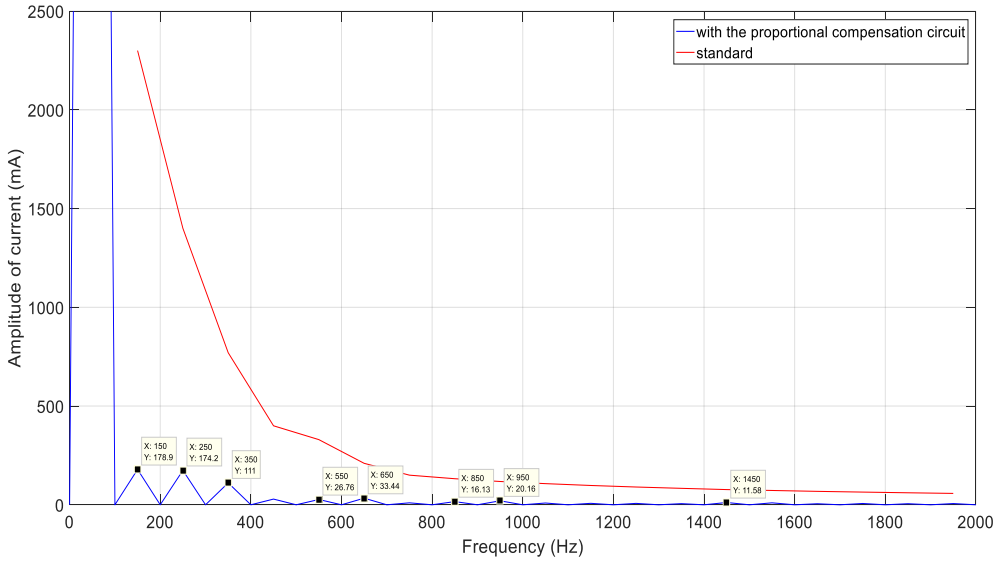


Figure 6.9 (a): harmonics of mains current under the proportional compensation control.

From figure 6.9 (b), it can be concluded that both control methods help the cordless kitchen system to meet the IEC harmonics standard at power level of 3.68 kW. Furthermore, based on the Fourier analysis, the Charge controlled method shows smaller amplitudes of undesired harmonics than the Proportional compensation control method, especially in frequency range from 1000 Hz to 2000 Hz. However, the implementation of the Proportional compensation circuit is easier than that of Charge controlled circuit, because the number of components needed for the former is less than the later. Hence, after the evaluation of these two control methods, the Proportional compensation method will be applied in the experimental setup.

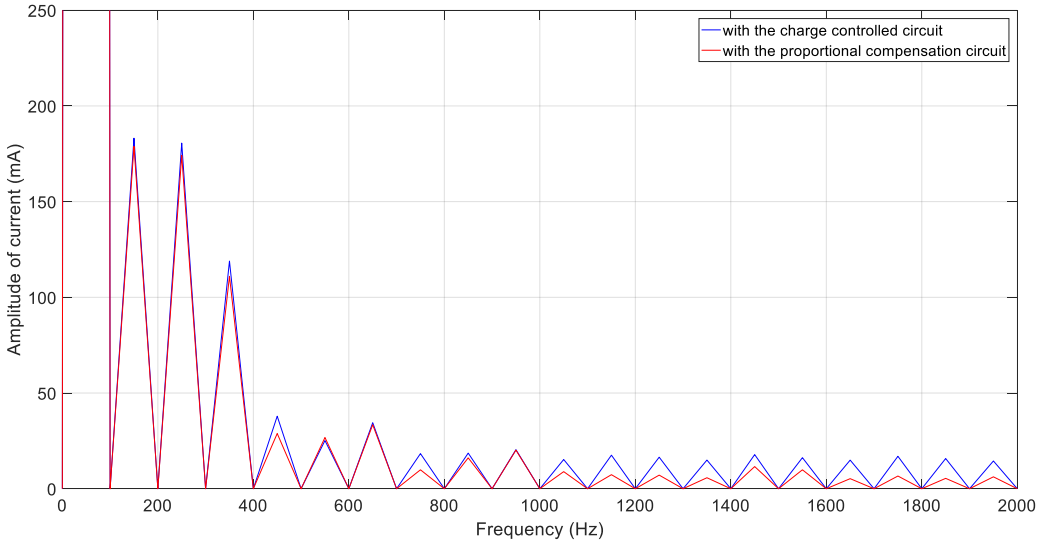


Figure 6.9 (b): Comparison of mains harmonics reduction under Charge control and Proportional compensation control.

6.3 Simulation of the current in the appliance

To evaluate the power received by the appliance, the output current of the high frequency inverter is observed, see figure 6.10.

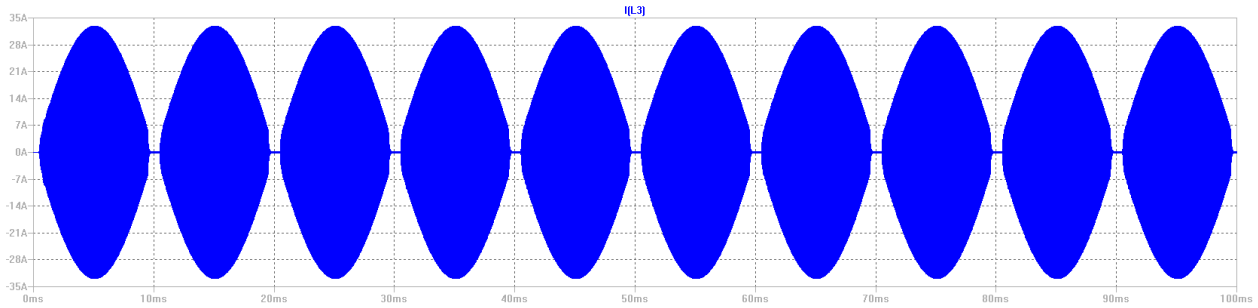


Figure 6.10: The output current of the high frequency inverter.

Because the load is resistive the envelope of the Tx and Rx current is sinusoidal, except during the communication time slots near the zero crossing of the mains voltage.

7 Experimental setup and results

To investigate the operation of the new power channel in combination with the Compensation channel, the following building blocks should be built. (The overall experimental setup is available in appendix III):

- a simplified power channel
- a Zero X detector
- a current sensor
- a control circuit, including software

7.1 The Simplified power channel

Because of time constraints, a simplified power channel is used to test the experimental Compensation channel and its control. The simplified power channel is used to create a mains current with the well known “mains current gap”, similar as with the high frequency inverter stage.

Because most high power appliances are in fact heating appliances they can be considered as ohmic loads. Therefore, to test the behaviour of the experimental Compensation channel, it is not necessary to build the high frequency inverter, Tx transmission coil and resonant tank. Therefore, the main inverter can be simulated as a simple resistance load, connected to the rectified mains by means of a controlled power switch.

Regarding the Compensation channel, the current through the compensator can be described by equation (35).

$$I_C = C \cdot f(t) \cdot \sqrt{2}\ I_{rms}\sin(\omega t) \tag{35}$$

For $f(t)$ can be written:

$$f(t) = \begin{cases} 1 \ \ when \ \ \frac{n \cdot T_{mains} - T_w}{2} < t < \frac{n \cdot T_{mains} + T_w}{2} \\ 0 \qquad\qquad when \ \ other \ \ value \ \ of \ \ t \end{cases} \tag{36}$$

where C is a constant between 0 to 1, and n represents any positive integer. The equations (35) and (36) indicate that during communication time slot, the compensator current is proportional to the voltage across the compensator. The ratio of the compensator voltage and the compensator current equals:

$$R_{eq} = \frac{V_{mains}}{i_C} = C \cdot \frac{311}{\sqrt{2}\ I_{rms}} \tag{37}$$

where the R_{eq} is the modulated equivalent resistance value of the compensator, as perceived by the mains voltage source. Therefore, the compensator can be simplified to a modulated resistor which consists of a duty cycle controlled Mosfet and a fixed-value resistor (R_f). For the compensator current can now be written:

$$i_C = D \cdot \frac{V_{mains}}{R_f} \tag{38}$$

where D is the modulated duty cycle. Therefore, for the equivalent resistor yields:

$$R_{eq} = \frac{V_{mains}}{i_C} = \frac{R_f}{D} \tag{39}$$

The compensator resistor can be modulated by adjusting the duty cycle. The schematic of the modulated resistor can be found in appendix II.

7.2 The Zero crossing detector

Both the simplified power channel and Compensation channel are connected directly to the mains source. Therefore the driving circuit of the simplified power channel as well as the control circuit of the Compensation channel needs to be in sync with the mains voltage. With a Zero crossing detector, the synchronisation with the mains voltage is realised. When the zero crossing point is detected, a new drive cycle and a new control cycle are activated. The schematic of zero crossing sensor can be found in appendix III.

7.3 The Current sensor

According figure 5.7, the value of the rectified mains current need to be measured as a feedback signal for the control circuit. For this purpose a current sensor is applied which consist of a current transformer, an integrator and an amplifier. The figure 7.1a the block diagram of the current sensor is shown. The schematic of the current sensor is available in appendix III, including the integrator and amplifier circuit.

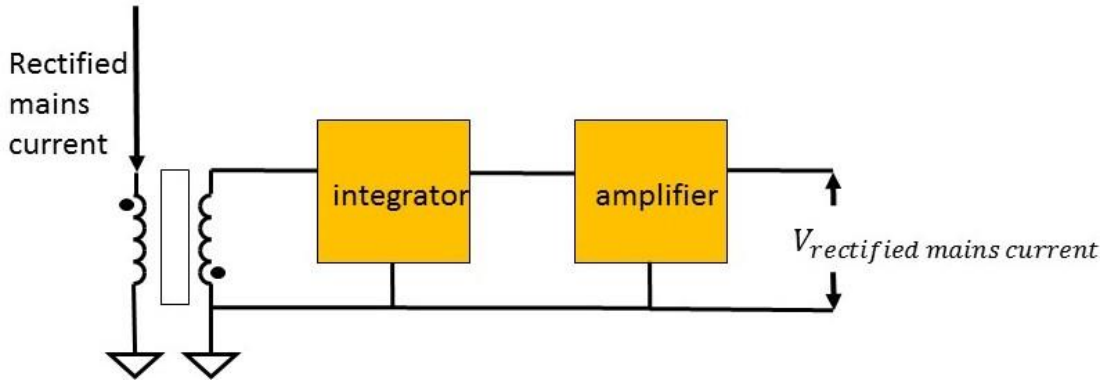


Figure 7.1a: Block diagram of the current sensor.

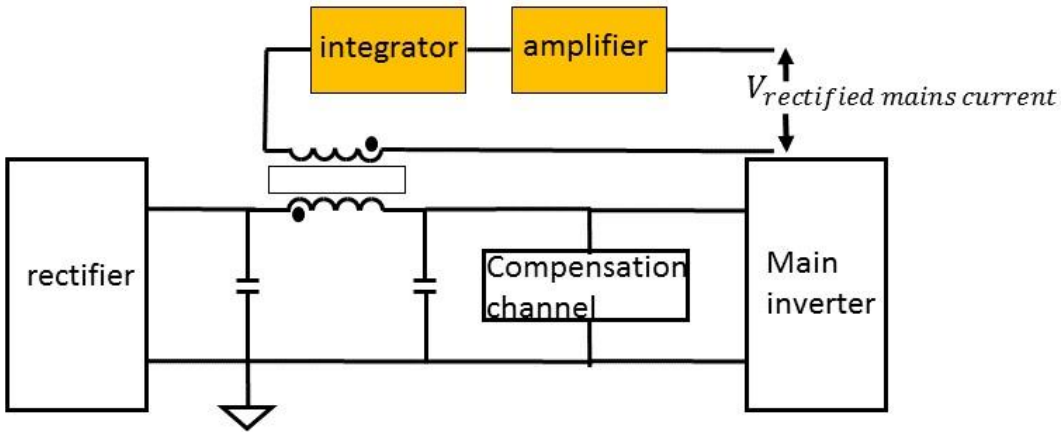


Figure 7.1b: Differential mode choke inductor applied as current sensor

The configuration of Figure 7.1a requires a separate current transformer. In figure 7.1b the existing differential mode choke inside the pi filter is used to sense the rectified mains current. The advantage of applying this configuration is that no extra circuit component is required. Instead, a few windings are added to the differential mode choke to make it a current transformer. It is available in the overall circuit illustration figure in appendix III.

7.4 Control circuit

The schematics of the two proposed block diagrams according figure 5.7 and 5.8, can be found in appendix II. During the evaluation of the two control methods by means of LT Spice simulations, it appears that the compensator channel with Proportional compensation method reaches the steady state faster and has lower undesired harmonics than the other one. Hence, the Proportional compensation control circuit will be implemented in the experimental test setup, see appendix II.

7.5 Arduino program

Two Arduino systems are utilized for this project. The Arduino 1 is used to drive the Mosfet inside the simplified power channel and provides the ZeroX signal. Furthermore, Arduino 1 is used to reset the output of the integrator capacitor of the current sensor.
Arduino 2 is used to drive the Mosfet inside the Compensation channel. The code is provide in appendix IV.

7.6 Experimental results

In order to observe whether the compensator can reduce the amplitude of the low frequency harmonics, the prototype is built and operating at 0.65 kW power level. The reason why it operating at 0.65 kW instead of 3.68 kW is that finding a load which can sustain 3.6 kW heat is difficult. Therefore, from the measured result, we will pay attention to the mains current changing before and after applying the compensator.
In this section, the currents through main load, through compensator are presented. Then the mains currents without and with compensator are provided.

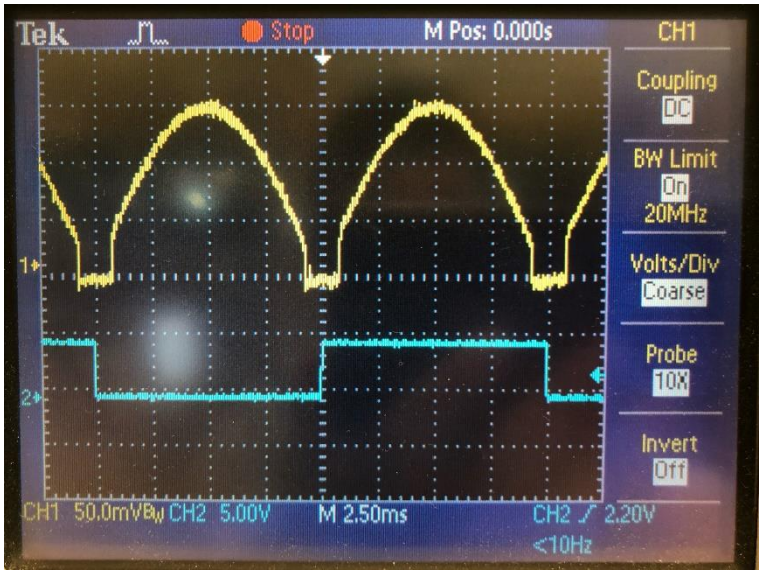


Figure 7.2: The wave form of current I_{REC} without compensation of the “mains current gap”

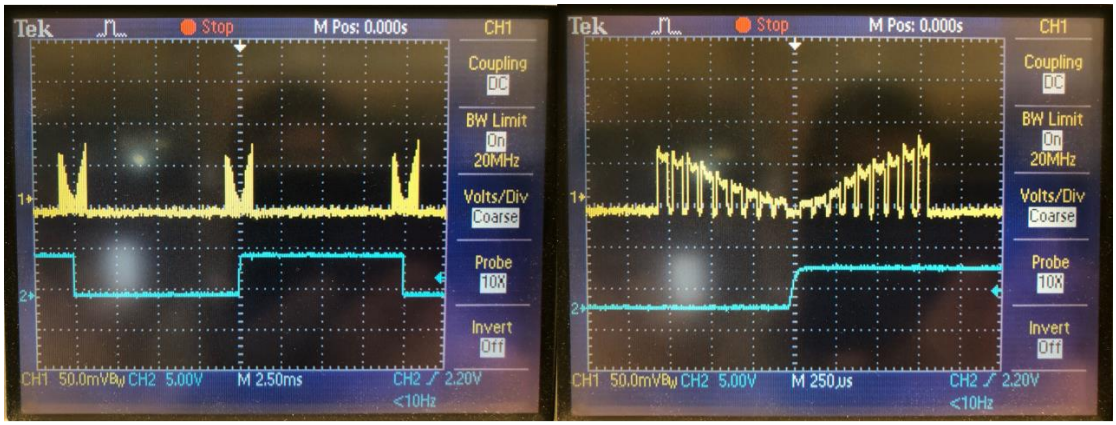
In figure 7.2 the yellow curve is the current I_{REC} through the main load. The blue curve is the zero cross signal which is a square wave with the same frequency with mains voltage. The rising and falling edges of the blue curve represent the zero crossing of the mains voltage. It can be observed that the 1.5 mSec communication time slots exist near the zero crossing of the mains voltage.

To quantify the current, the parameters in the current probe should be mentioned. The ratio of the output voltage and the sensed current is 1V/2A. Besides, the oscilloscope is setting to Probe 10x, so the amplitude of sensed current can be calculated as follows:

$$\frac{150\times10}{1000}\times 2 \quad = 3 \ A.$$

Similarly the peak value of the needed compensation current can be calculated as well:

$$\frac{40\times10}{1000}\times 2 = 0.8 \ A.$$



a) b)

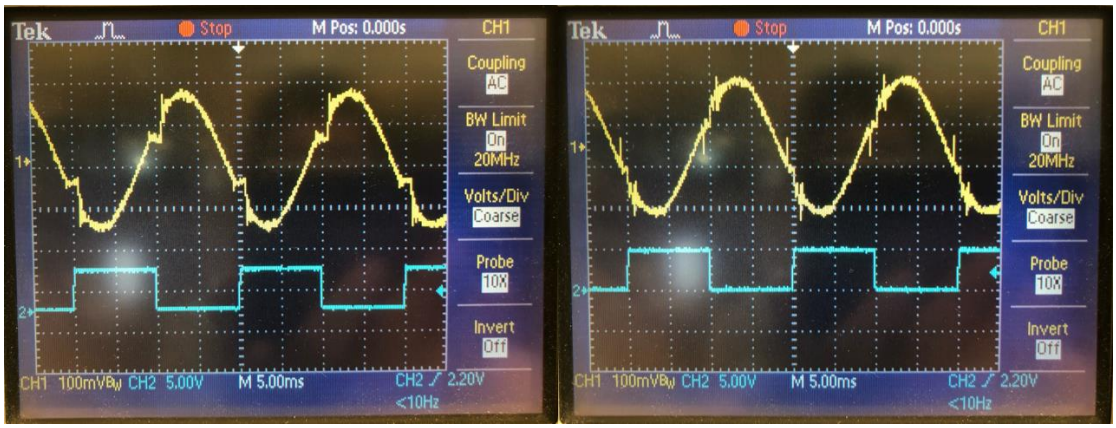
Figure 7.3: The current through the compensator

The left scope according Figure 7.3a is shows the zoomed out current through the compensator. The right scope shows the current through the compensator zoomed in.

As it was illustrated in the section 5.5, the duty cycle is determined automatically by the control circuit. Based on the measurement result indicated by figure 7.3, the duty cycle of the compensator circuit is about 80%. In terms of the compensator peak current and because of the phase shift between mains current and mains voltage, the peak in the right half part is slightly higher than the left half part. Therefore, we use an average value of the peaks in the left and right parts, which is:

$$\frac{60\times10}{1000}\times 2\times 70\% = 0.84 \ A.$$

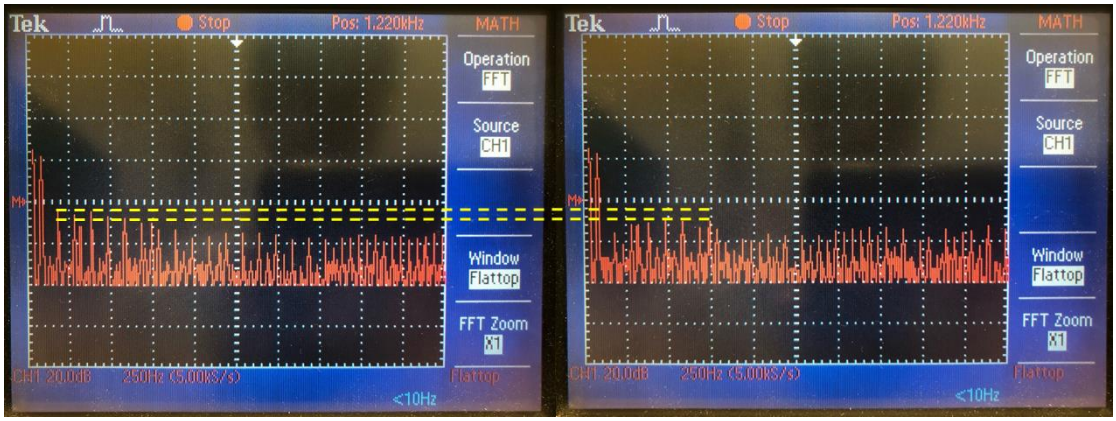
Comparing the required peak Compensation current (0.8A), the measured peak Compensation current equals 0.84A which is close to that value.



a) b)

Figure 7.4: The mains current without and with compensator

The left scope (Figure 7.4a) shows the measured mains current without the compensator, and the right scope shows the measured mains current with the compensator in use.
From the figure 7.4, it can be observed that the current gap is filled by the compensator current. The Fourier analysis result is provided by the figure 7.5.



a) b)

Figure 7.5: The Fourier analysis of the mains current in dB coordinate

The left scope of Figure 7.5 shows the Fourier analysis without the compensator, and the right scope shows the Fourier analysis with compensator in use. In this project, the low frequency (<2 kHz) mains harmonics needs to be considered, so the first horizontal division is important. The yellow dash lines highlight the reduction of the low frequency mains harmonics. In figure 7.5, the mains harmonics in the frequency range of 100 Hz to 1000 Hz are reduced by 6 dB in average. Based on figure 7.5, the amplitudes of every harmonics within 2000 Hz is translated in decade coordinate, see figure 7.6.

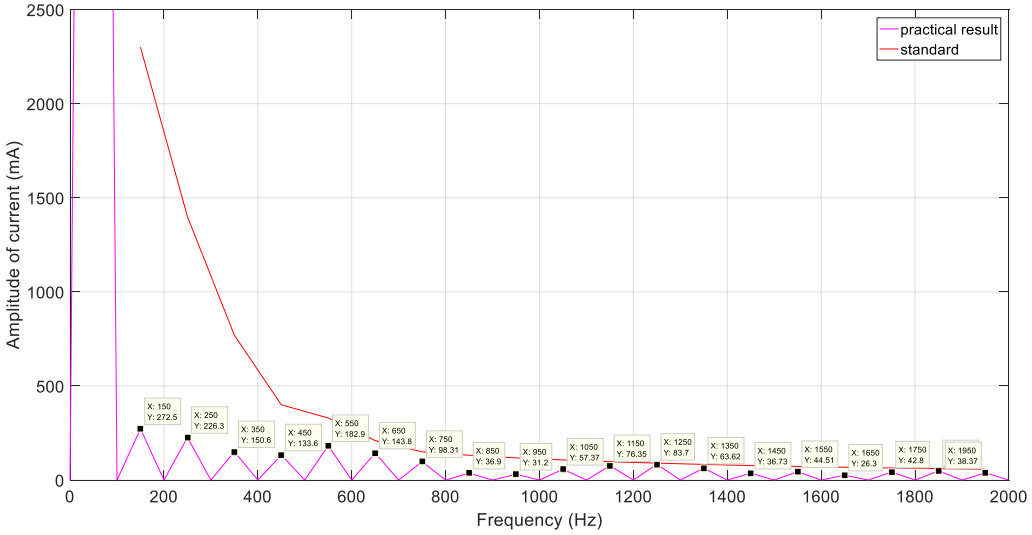


Figure 7.6: The Fourier analysis of the mains current in decade coordinate

From figure 7.6, the THD factor can be calculated by:

$$THD = \frac{\sqrt{V_2{}^2+V_3{}^2+V_4{}^2+V_5{}^2+\cdots+V_{40}{}^2}}{\sqrt{V_1{}^2+V_2{}^2+V_3{}^2+V_4{}^2+\cdots+V_{40}{}^2}} \quad (40)$$

The THD factor without compensation is:

$$THD_{original} = 0.158 \quad (41)$$

The THD factor with compensation is:

$$THD_{compensated} = 0.039 \quad (42)$$

Form the THD factor result it can be concluded that the overall amplitude of the harmonics are significantly reduced. However, there is still an issue with the compensated mains current. From figure 7.4, it can be observed that a phase difference exist between mains voltage and mains current. Figure 7.2 and figure 7.3 indicate that the inverter and compensator current are in phase with the mains voltage. The phase difference between mains voltage and current is causes by the passive filter located between rectifier and inverter.

8. Conclusion

8.1 Achievements

To upgrade the power level of the cordless kitchen system from 1.5 kW to 3.68 kW it is necessary to fill the mains current gap caused by communication time slot, so that the mains harmonics meet the IEC harmonics standard IEC 61000-3-2:2018. In order to realize this, a shunt compensator circuit is proposed which operates during communication time slot and is connected in parallel with existing inverter stage.
The shunt compensator circuit exists of a cascade of an enable switch, a Boost converter, a storage capacitor and a Buck converter and a control circuit. The control method of a shunt compensator circuit can be based on Charge control and Proportional compensation control. All building blocks are illustrated in section 5.

A simulation model is created by using LTspice. The simulation results indicates that with the compensator circuit the mains current gap can be compensated, and that the mains harmonics will be reduced below the IEC harmonics standard 61000-3-2:2018.

A simplified experimental setup is built to verify the operating principle of the shunt compensator circuit and includes a current sensor, the Proportional compensation control method and a micro controller (Arduino). The measured results indicate that the amplitudes of the mains harmonics are significantly reduced by applying the compensator circuit. With the shunt compensator circuit the THD of the mains current is reduced by 75%. However, because a simplified model is applied in the experimental setup, the result might differ from an implementation in the “real” cordless kitchen system.

With the shunt compensator circuit a low cost & simple solution is achieved which reduces the mains harmonics and provides the highest efficiency at the same time; only a small part of the input power needs to be processed.

8.2 Future work

For future work on this project, there are some details that needs to be improved. Firstly, the passive filter located between rectifier and inverter need to be improved such that the phase difference between mains voltage and mains current needs to be reduced, as is illustrated in section 6.2. Secondly, building a PCB for the complete cordless kitchen system is desired instead of using a simplified model to test the principle. Finally, use a suitable equivalent load which can operate at 3.68 kW power level.

Appendix

Appendix I: Detail of Compensation current channel

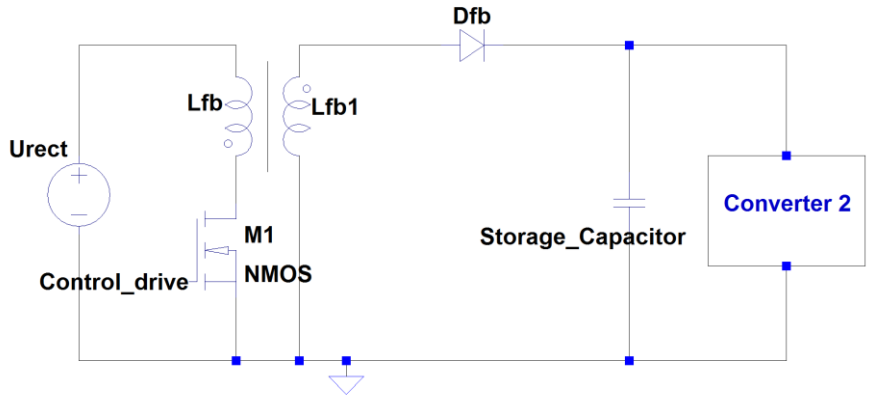


Figure a: The flyback converter

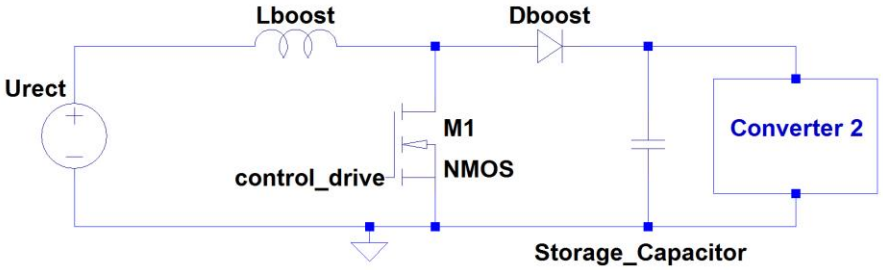


Figure b: The Boost converter

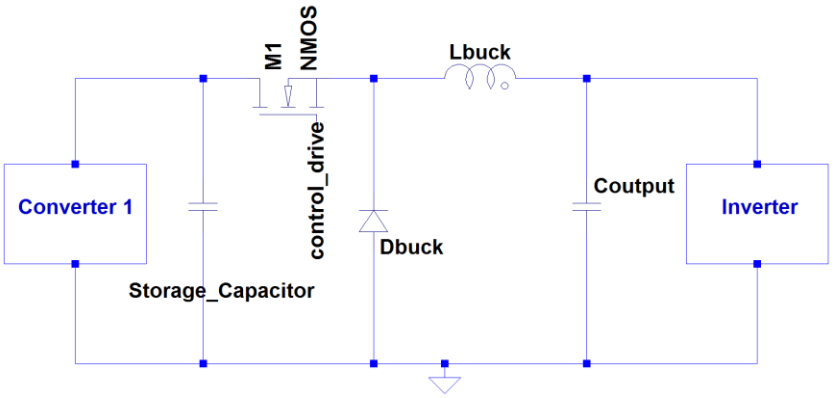


Figure c: The Buck converter

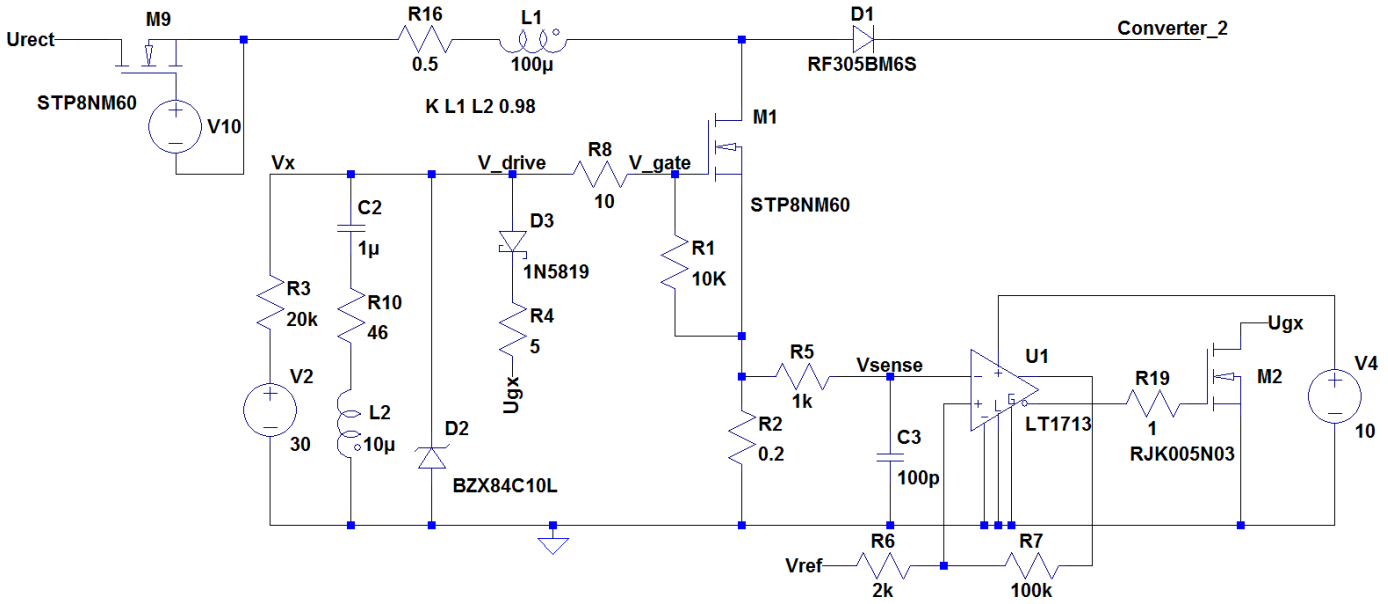


Figure d: Self-Oscillating (SO) drive of the Boost converter

To illustrate the operating principle of the SO circuit, two time intervals and two events are discussed. The two time intervals are the switch-on interval and the switch-off interval, and two events are switch-on moment and switch-off moment. The voltage polarity of every component is listed by table 1.

	Voltage of L_1	Voltage of L_2	C_2 voltage	M_2	V_{gate}
Switch on interval	'+'	'+'	discharging	off	+10V
Switch off moment	'+ => -'	'+ => -'	5V, Start to charge	off => on	+10V => 0V
Switch off interval	'-'	'-'	charging	off	0
Switch on moment	'- =>0'	'- =>0'	10V, start to discharge	off	0V =>10V

Table 1: The state of core components in SOPS circuit

The voltage source of 30V is used to charge C_2 to a steady state voltage, to start operation of the Boost converter. A high ohmic resistor R3 connected in series with the 30V voltage source to startup the Boost converter but also to restrict it's influence to the SO circuit. At the switch off moment, i_{R2} reaches the reference current, and then the comparator output becomes positive and turns on switch M_2. At the event of i_{L1} get to zero, D_1 opens the circuit, and there is no voltage applied on L_1 as well as L_2. Consequently, $V_{drive} = 0 + V_{sops} = 10V$, and then switch M_1 is switched on. With this SO circuit operation, the Boost converter operates always in BCM.

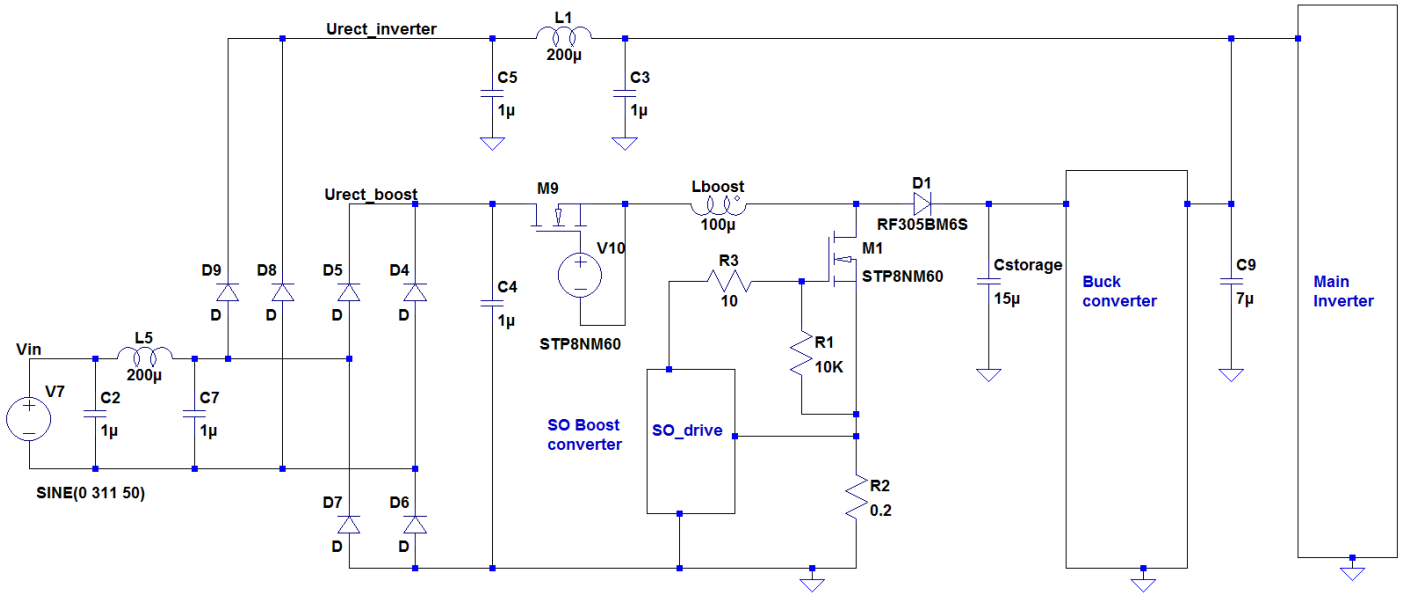


Figure e: Overall overview of the compensation channel

The two power channels indicated in this figure are original power channel and added power channel. The two channels connected with mains source with separate rectifiers. The original power channel consist of the rectifier, the pi filter and the inverter. The added channel consist of the rectifier, Boost converter with SO drive circuit and buck converter. The output terminal of the added channel is current with the pi filter, so that the power drawn by the added circuit can be injected to the inverter.

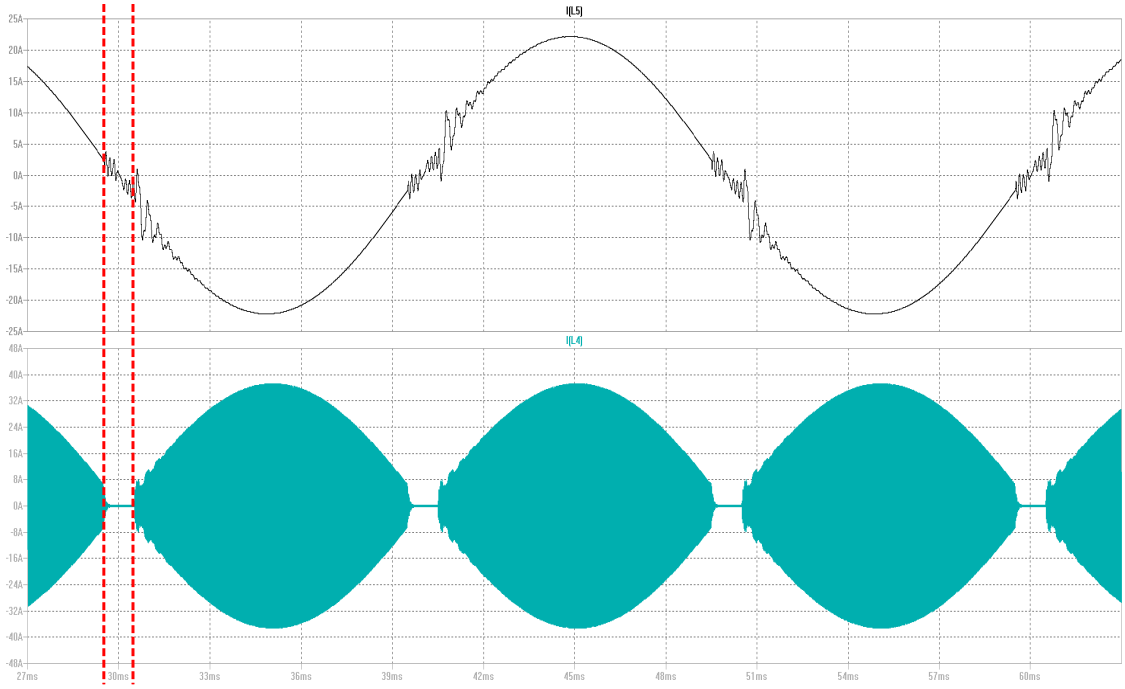


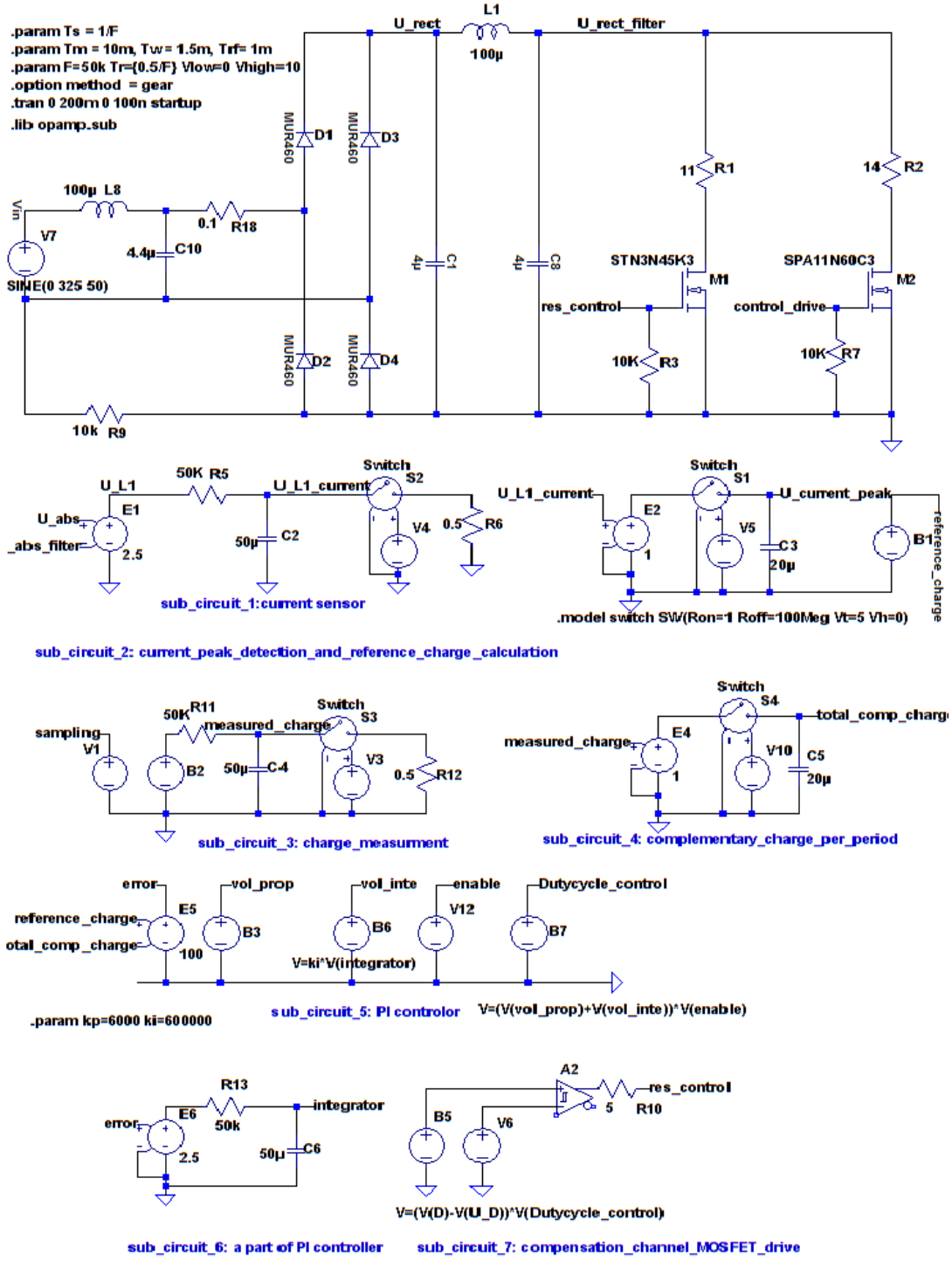
Figure f: Simulation result for the compensator without converter 2:

In this figure, the upper plot is mains current, and the lower plot is transmitted current. The two red dash lines indicate the communication time slot. From this figure, it should be noticed that after the communication time slot, an obvious current ripple appears both in mains current and transmitted current. That is because the energy releasing process is too fast. Slowing down that process can remove the ripple. Therefore, the converter 2 is need to slow down this process.

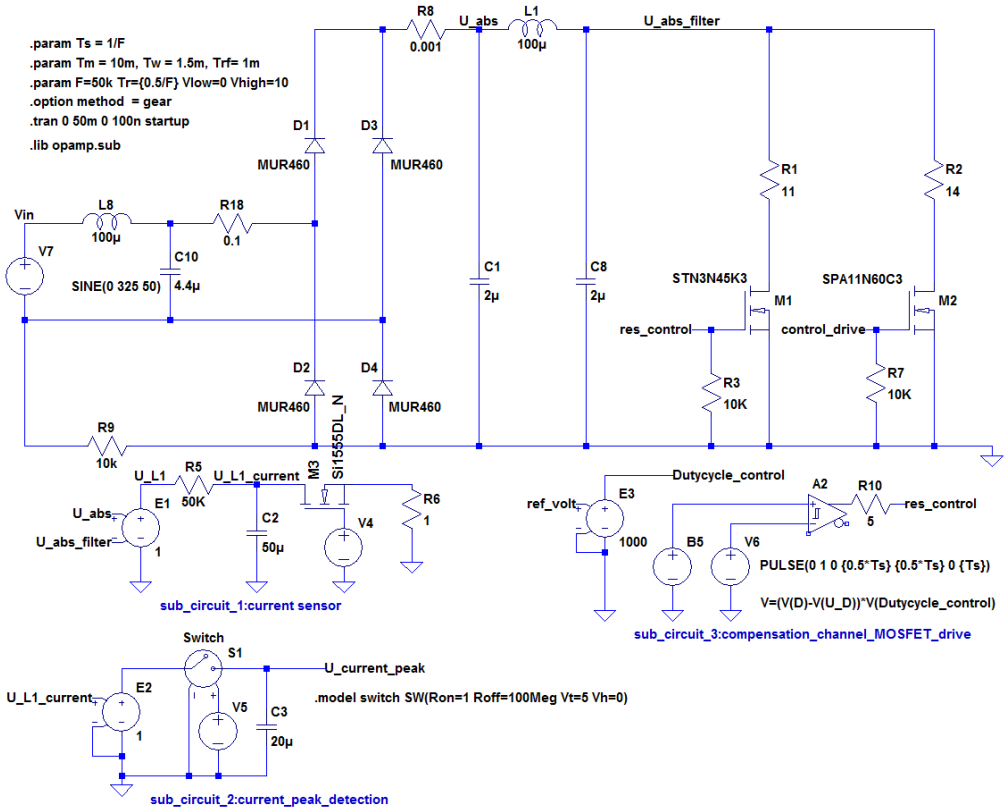
Appendix II: Control circuit with simplified Compensation current channel.

Schematic model Charge control Circuit

The signal process order is from sub_circuit_1 to sub_circuit_7. As in chapter 5.5 illustrated, first the rectified mains current is detected by the current sensor, and then based on the measured current, the amount of compensating charge and the charge needed to be compensated are compared as a feedback signal and a reference signal respectively. The error calculated is executed by a PI controller. Finally, the signal is delivered to the PWM generator and fed to the compensation Mosfet M1.



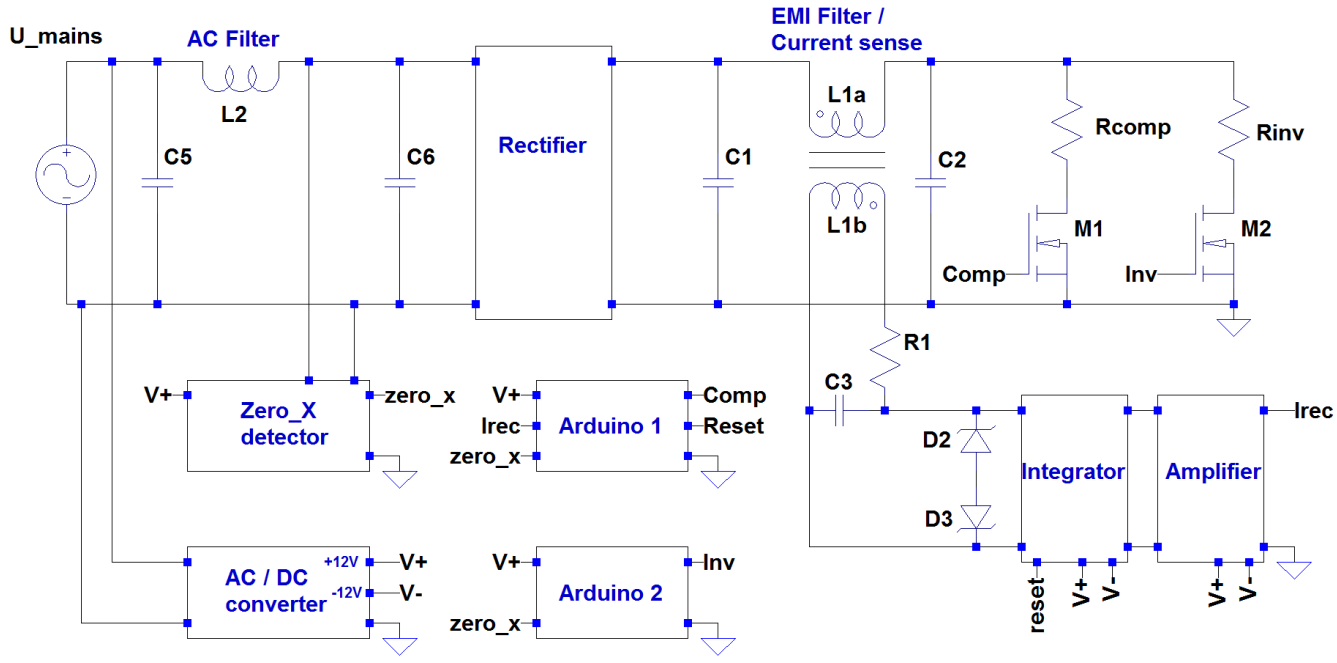
Schematic model Proportional compensation circuit



The signal process order is from sub_circuit_1 to sub_circuit_3. As chapter 5.5 illustrated, first the rectified mains current is detected by the current sensor. Then the peak value of rectified mains current is sampled and measured. H_{tra} is therefore proportional to the measured peak value of rectified mains current (H_{tra} is illustrated in chapter 5.5.2). Finally, the signal H_{tra} further adjusted and then delivered to the PWM generator which drives the compensation Mosfet M1.

Appendix III: Experimental set up

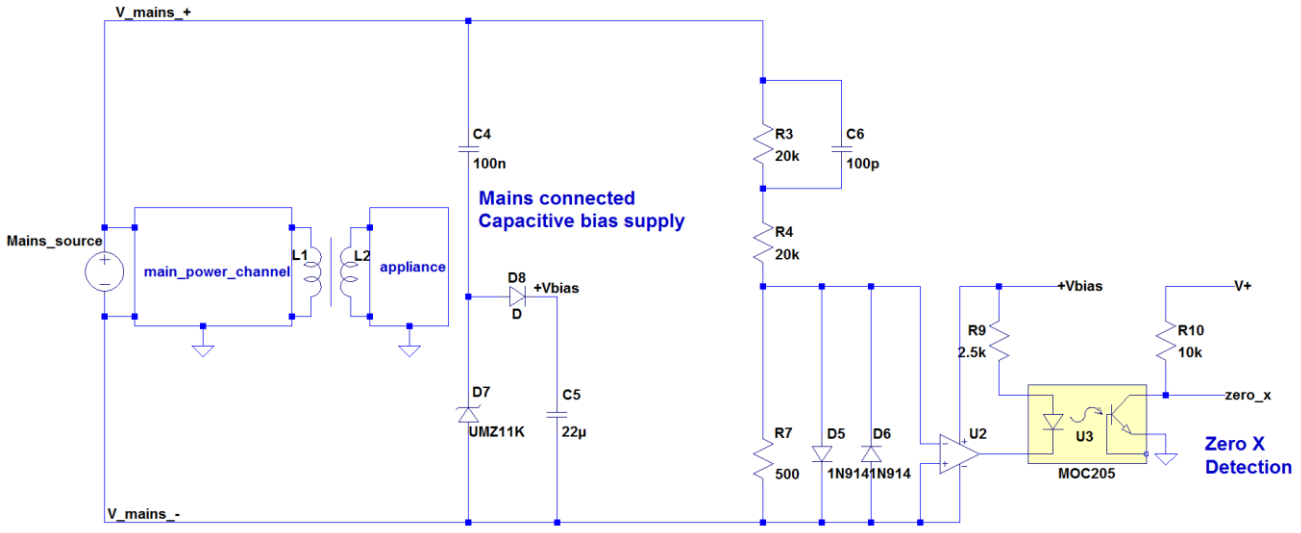
The overall circuit overview:



From this figure, the following details can be noticed:

1) The inverter is simplified to a modulated resistor which consists of a Mosfet and resistor.
2) The compensator is simplified to a modulated resistor, because of the linear character illustrated in chapter 7.1.
3) As it is discussed in chapter 7.6, the AC filter might cause the phase difference between mains voltage and mains current.
4) Zero crossing signal sent to Arduino to sync it with mains voltage.
5) An AC/DC converter is applied to power the two Arduino's and Opamp's.

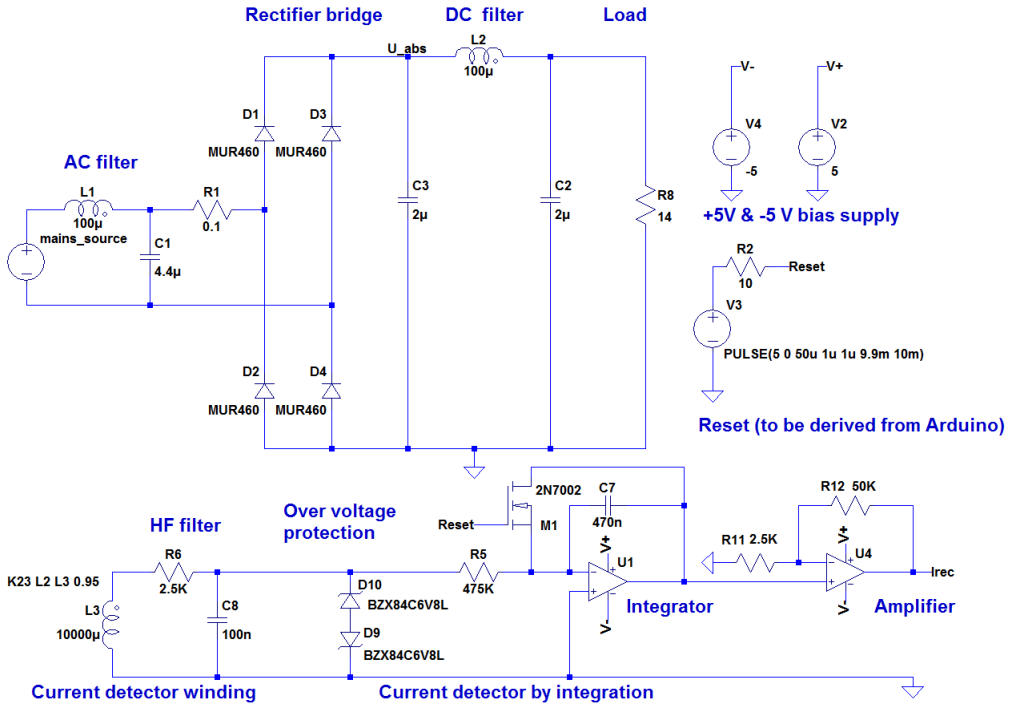
Zero cross circuit:



From this figure, the following details can be noticed:

1) The Mains source is floating, so the power supply for the Opamp U2 and the diode side of the photo coupler MOC205 should be also floating.
2) The components C4, D7 and C5 are utilized to provide a floating power source for some components.
3) R3 and R4 act as voltage divider for the photo coupler.
4) The diode D5 and D6 is used to make the input voltage to the Opamp U2 with in the range of -0.7V to 0.7V.

Amplifier and integrator circuit:



The reset pulse signal for the integrator is provided by Arduino. The inductor L2 and L3 are coupled, so that the voltage across L2 can be detected by the sub circuit. The formulas' for the integrator and amplifier are respectively:

$$V_{out} = -\frac{1}{C_7 R_5}\int_0^t V_{in}\,dt \qquad\qquad V_{out} = (1+\frac{R_{12}}{R_{11}})V_{in}$$

Appendix IV: Arduino code

Arduino used to drive the main inverter:

This code is used to control the switch of the simplified inverter and the reset switch in integrator. The operation of this Arduino sync the mains voltage, by using zero cross detection circuit. When the zero crossing signal (zero_x) changes from 1 to 0 or vice versa, the Arduino will start a new operation period.

```
int discharge = 3;
int mainInv = 5;
int zero_x = A5;
bool edge = LOW;
bool lastEdge = LOW;
bool timerworking = LOW;

#define delayTime                34              //Extra delay to set the pulses
#define maxTimerTime             60000           //Needs to be higher than the highest delay time
#define portDischargeOn          PORTD | 0x08    // PIN 3 ON
#define portDischargeOff         PORTD & 0xF7    // PIN 3 OFF
#define portMainInvOn            PORTD | 0x20    // PIN 5 ON
#define portMainInvOff           PORTD & 0xDF    // PIN 5 OFF

int flag = 0;
unsigned int counter = 0;
//int stopp = 0;
int changingCycle = 23;
float period = 16000/changingCycle;
int increamental = period/changingCycle;
//int i = 1;
int Ton = 0;

void setup() {
  // put your setup code here, to run once:
  pinMode (discharge, OUTPUT);
  pinMode (mainInv, OUTPUT);
  pinMode (zero_x, INPUT_PULLUP);

  DDRD |= B01111000;

  noInterrupts();   //Disable global interrupts
  TCCR1A = 0;       //Set entire TCCR1A register to 0
  TCCR1B = 0;       //Set entire TCCR1B register to 0

  OCR1A = maxTimerTime;       //set compare match register to desired timer count
  TCCR1B |= (1 << WGM12);     //Turn on CTC mode:
  //TCCR1B |= (1 << CS11);
  TCCR1B |= (1 << CS10);      //1* prescaler
  TIMSK1 |= (1 << OCIE1A);    //Enable timer compare interrupt:
```

```
    attachInterrupt(digitalPinToInterrupt(2), ActivatePulse ,CHANGE );
    interrupts();                       //Enable global interrupts:
}

void ActivatePulse(){
    //digitalWrite (9, HIGH);
    timerworking = HIGH;
    TCCR1B |= 0x01;    //start counting
    TCNT1 = maxTimerTime - 1;
}

void loop() {
    // put your main code here, to run repeatedly:
    }

ISR(TIMER1_COMPA_vect) {

    if (timerworking == HIGH){
        TCCR1B &= 0xF8;    // stop counting
        switch (flag){
            case 0:
              // digitalWrite (discharge, HIGH);
                PORTD = portDischargeOn;
                flag = 1;
                TCNT1 = maxTimerTime - 800 + TCNT1 + delayTime;    // 62.5ns * 800=0.05ms
                break;

            case 1:
                //digitalWrite (discharge, LOW);
                PORTD = portDischargeOff;
                flag = 2;
                TCNT1 = maxTimerTime - 11200 + TCNT1 + delayTime; // 62.5ns * 11200=0.7ms
                //counter++;
                //timerworking = LOW;
                //stopp = 0;
                break;

            case 2:
                //digitalWrite (mainInv, HIGH);
                PORTD = portMainInvOn;
                flag = 3;
                TCNT1 = maxTimerTime - 45333 + TCNT1 + delayTime; // 62.5ns * 45333=2.83ms
                break;

          case 3:
                //digitalWrite (mainInv, HIGH);
                flag = 4;
```

```
            TCNT1 = maxTimerTime - 45333 + TCNT1 + delayTime;    // 62.5ns * 45333=2.83ms
            break;

        case 4:
            //digitalWrite (mainInv, HIGH);
            flag = 5;
            TCNT1 = maxTimerTime - 45334 + TCNT1 + delayTime;    // 62.5ns * 45334=2.83ms
            break;

        case 5:
            PORTD = portMainInvOff;
            flag = 0;
            timerworking = LOW;
            break;
      }
      TCCR1B |= 0x01;    //start counting
   }
   else{
      TCCR1B &= 0xF8;    // stop counting
   }
}
```

Arduino used to drive the compensator

This code is used to control the switch of the simplified compensator. The operation of this Arduino sync the mains voltage, by using zero cross detection circuit. When the zero crossing signal (zero_x) changes from 1 to 0 or vice versa, the Arduino will start a new operation period.

```
// int discharge = 3;
//int mainInv = 5;
int current_sensor = A5;
//bool edge = LOW;
//bool lastEdge = LOW;


#define delayTime                34                //Extra delay toset the pulses
#define maxTimerTime             60000             //Needs to be higher than the highest delay time
#define portDischargeOn          PORTD | 0x08      // PIN 3 ON
#define portDischargeOff         PORTD & 0xF7      // PIN 3 OFF
#define portAssisOn              PORTD | 0x20      // PIN 5 ON
#define portAssisOff             PORTD & 0xDF      // PIN 5 OFF

bool timerworking = LOW;
int flag = 0;
unsigned int counter = 0;
//int stopp = 0;
int changingCycle = 23;
```

```
int period = 1200;
//int increamental = period/changingCycle;
int i = 1;

int height = 0;
int Ton = 0;
int Toff = 0;
float coef = 0.002;


//int periodSlope = 3200;
//int STon = 0.85 * 3200;
//int decre = STon/5;

void setup() {
   // put your setup code here, to run once:
   //pinMode (discharge, OUTPUT);
   //pinMode (mainInv, OUTPUT);
   //pinMode (zero_x, INPUT_PULLUP);
   pinMode (current_sensor, INPUT);

   DDRD |= B01111000;

   noInterrupts();    //Disable global interrupts
   TCCR1A = 0;           //Set entire TCCR1A register to 0
   TCCR1B = 0;           //Set entire TCCR1B register to 0

   OCR1A = maxTimerTime;         //set compare match register to desired timer count
   TCCR1B |= (1 << WGM12);      //Turn on CTC mode
   //TCCR1B |= (1 << CS11);
   TCCR1B |= (1 << CS10);      //1* prescaler
   TIMSK1 |= (1 << OCIE1A);    //Enable timer compare interrupt:
   attachInterrupt(digitalPinToInterrupt(2), ActivatePulse ,CHANGE );
   interrupts();                        //Enable global interrupts:
}

void ActivatePulse(){
   //digitalWrite (9, HIGH);
   timerworking = HIGH;
   Ton = coef * height * period + 1;
   if (Ton > 1080){
      Ton = 1080;
   }
   Toff = period - Ton + 1;
   TCCR1B |= 0x01;    //start counting
   TCNT1 = maxTimerTime - 1;
}
```

```
void loop() {
   // put your main code here, to run repeatedly:
   }

ISR(TIMER1_COMPA_vect) {

   if (timerworking == HIGH){
      TCCR1B &= 0xF8;    // stop counting
      switch (flag){

         case 0:
            PORTD = portAssisOn;
            flag = 1;
            i++;
            TCNT1 = maxTimerTime - Ton;
            break;

         case 1:
            PORTD = portAssisOff;
            if (i>=10){
              flag = 2;
              i=1;
            }
            else{
            flag = 0;
            }
            TCNT1 = maxTimerTime - Toff;
            break;

         case 2:
            PORTD = portAssisOff;
            flag = 3;
            TCNT1 = maxTimerTime - 45333 + TCNT1 + delayTime; // 62.5ns * 45333=2.83ms
            break;

         case 3:
            flag = 4;
            TCNT1 = maxTimerTime - 22667 + TCNT1 + delayTime;    // 62.5ns * =1.416ms
            break;

         case 4:
            height = analogRead (current_sensor);
            flag = 5;
            TCNT1 = maxTimerTime - 43134 + TCNT1 + delayTime;    // 62.5ns * 45334=2.83ms
            break;
```

```
        case 5:
            flag = 6;
            TCNT1 = maxTimerTime - 21000 + TCNT1 + delayTime; // 62.5ns * 21000=1.31ms
            break;

        case 6:
            PORTD = portAssisOn;
            flag = 7;
            i++;
            TCNT1 = maxTimerTime - Ton;
            break;

        case 7:
            PORTD = portAssisOff;
            if (i>=10){
              flag = 0;
              i=1;
              timerworking = LOW;
              break;
            }
            else{
            flag = 6;
            }
            TCNT1 = maxTimerTime - Toff;
            break;
            }


      TCCR1B |= 0x01;    //start counting
   }
   else{
      TCCR1B &= 0xF8;    // stop counting
   }
}
```

Bibliography

[1] P.D.Vries, "Reduction of mains harmonic distortion for wireless kitchen appliances," PHILIPS, Drachten, 2014.

[2] M. Mohammad and F. A. Ali, "A low-Distortion Selft-Oscillating Power Factor Correction Circuit for Low-Cost Applications," IEEE, Sharif, 2014.

[3] IEC, "IEC 61000-3-2:2018," International Electrotechnical Commission, 2018.

[4] S. Wang and W. Ettes, "Optimization of the Power Factor of an inductive power transmitter," PHILIPS, Drachten, 2017.

[5] W. Eettes and B. Andries, "Single phase Hyrid Power Factor Correction," EPE2001, 2001.

[6] R. M. Pratap, K. P. Anup and D. Das, "An Active PFC Boost Converter Topology for," IEEE, Rourkela, India, 2015.

[7] U. Suma, V. L and A. Usha, "Active Power Factor Correction Technique for Single," IEEE, Bangalore, 2014.

[8] L. C. Tzuen and M. H. Tsung, "Shunt semi-active power factor correction circuit for," IET Power Electronics, Kaohsiung, 2014.

[9] S. A. Hussain and D.-C. L. Dylan, "A High-Efficiency AC/DC Converter With Quasi-Active," *IEEE transations on power electronics,* vol. 25, no. 5, pp. 1103-1109, 2010.

[10] C. Yi, N. Yurong and Z. Siheng, “An Input-Adaptive Self-Oscillating Synchronous Boost Converter for LED Driving with Ultra-Low Wide-Range Voltage Input,” IEEE, Zhejiang,China.

[11] O. L. Michael, "UCC38050 100-W Critical Conduction," TEXAS INSTRUMENTS, 2004.

[12] S. Borekci and I. M. Luleci, "Low-Cost IC less Self Oscillating Boost PFC," IEEE, 2013.

[13] Mohan, Undeland and Robbins, Power Electronics Converters, Applications, and Design, Media Enhanced, 2003.

[14] K. G. Rahul, K. N. Jitendra, G. Nitin and G. Vikas, "Novel Closed Loop Control for Power Factor," in *International Conference on Innovations in Power and Advanced Computing Technologies*, Jaipur, India, 2017.