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Photovoltaic to Virtual Bus Series–Parallel Differential Power Processing for Photovoltaic Systems

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ABSTRACT Photovoltaic (PV) systems are frequently subject to voltage and current mismatches caused by various factors, such as partial shading, differing panel tilt angles, dust accumulation, and cell degradation among PV elements. These mismatches can significantly reduce the overall efficiency of PV systems by preventing individual modules or strings from operating at their maximum power point (MPP). This article introduces a novel architecture termed PV to virtual bus series–parallel differential power processing, which effectively mitigates mismatches in both series-connected PV modules (i.e., current mismatches) and parallel-connected PV strings (i.e., voltage mismatches). The proposed architecture employs a combination of string-level converters (SLCs) and module-integrated converters (MICs) that process only a fraction of the total power. Notably, the architecture leverages virtual buses on the primary side of both SLCs and MICs, leading to reduced voltage rating requirements for SLCs and lower power rating demands for MICs. This design reduces the stress on individual components, making the system more cost-effective and reliable. The article provides a comprehensive analysis of the requirements for SLCs and MICs, along with a detailed explanation of how the proposed architecture ensures that PV modules consistently operate at their respective MPPs. In addition, it explains how the virtual bus voltage is balanced through mathematical power flow equations, ensuring stable and efficient operation. Finally, the architecture's effectiveness is validated through real-time simulation results with two PLECS real-time (RT) boxes, which demonstrate its capability to address mismatch issues and optimize the performance of PV systems.

INDEX TERMS Distributed maximum power point tracking (DMPPT), module-integrated converters (MICs), photovoltaic (PV) systems, photovoltatronics, PV to virtual bus (PV2VB) differential power processing (DPP), series–parallel differential power processing (SPDPP), string-level converters (SLCs).

NOMENCLATURE

BF	Bidirectional flyback.
DAB	Dual active bridge.
DMPPT	Distributed maximum power point tracking.
DPP	Differential power processing.
FPP	Full power processing.
LCOE	Levelized cost of energy.
MIC	Module-integrated converters.
MPP	Maximum power point.
PDPP	Parallel differential power processing.
PV2B	PV to bus.
PV2PV	PV to PV.
PV2VB	PV to virtual bus.
SDPP	Series differential power processing.
SLC	String-level converters.
SPDPP	Series–parallel differential power processing.

I. INTRODUCTION

Photovoltaic (PV) systems are often affected by mismatch conditions, leading to a reduction of energy yield and consequently worsening LCOE [1], [2], [3], [4]. One promising approach to mitigate these issues is DMPPT, which can be classified into FPP and DPP architectures.

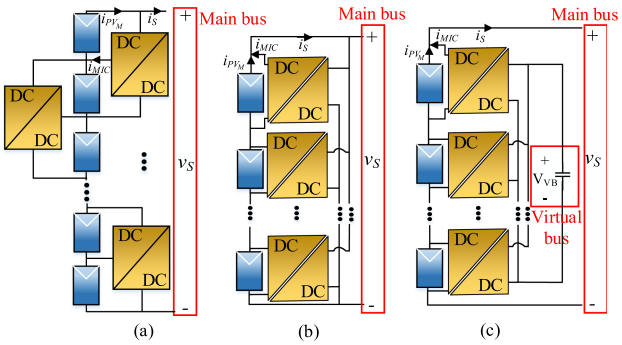

FIGURE 1. PV systems using (a) PV2PV, (b) PV2B, and (c) PV2VB SDPP architectures.

FPP architectures, such as microinverters [5], [6], modular multilevel cascade inverters [7], parallel dc optimizers, and series dc optimizers [8], are well-established, proven technologies and available on the market. These architectures eliminate mismatch-related losses by using a wide range of power converters. However, they process all the power generated by the PV modules, even under uniform conditions, leading to increased power conversion losses, as well as larger and more costly converters. To overcome these drawbacks, the concept of DPP was introduced for PV applications. DPP architectures are further categorized into SDPP, PDPP, and SPDPP.

In SDPP architectures, categorized into PV2PV [9], [10] [see Fig. 1(a)], PV2B [11], [12] [see Fig. 1(b)], and PV2VB [13], [14] [see Fig. 1(c)], MICs specifically manage the differential current between individual PV modules (i_{PV_M}) and the overall PV string current (i_S). The MICs do not process any power when the PV modules are subject to uniform conditions. During mismatch conditions, MICs process only a fraction of the total power, while most of the power generated by the PV modules flows directly to the output without local processing. This provides two key advantages: first, it reduces the operating time of MICs and improves system efficiency, even if the efficiency of SDPP MICs is lower than that of FPP MICs. Second, it reduces component stress, leading to enhanced reliability and a longer lifespan.

In [15] and [16], it is shown that even with 98% conversion efficiency for FPP MICs and 90% efficiency for SDPP MICs, the PV2PV, PV2B, and PV2VB architectures improve system conversion efficiency by 0.3%, 1.6%, and 1.3%, respectively, over their FPP counterparts. Furthermore, these efficiency gains are achieved while the power ratings of SDPP converters in PV2PV, PV2B, and PV2VB are only 33%, 16%, and 33% of those of the dc-FPP converters.

On the other hand, in PDPP architectures, categorized into PV2B [17], [18], [19], [20] [see Fig. 2(a)] and PV2VB [21] [see Fig. 2(b)], SLCs provide the required differential voltage between PV groups and a common bus to eliminate mismatch losses among parallel-connected PV groups. High system conversion efficiency up to 99.58% [20] along with reduced component rating highlights the significant potential to reduce the LCOE in PV systems. However, for applications

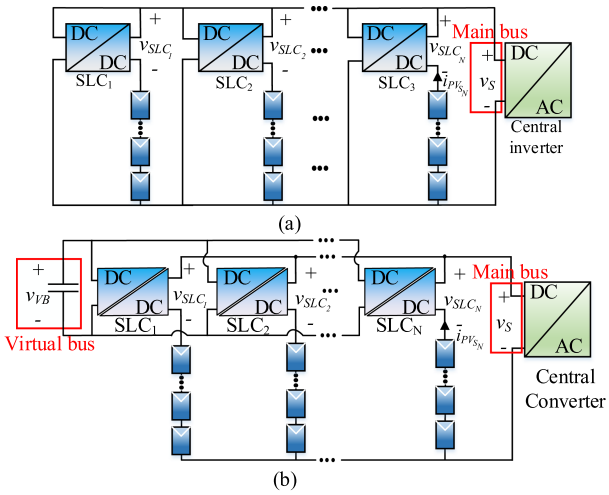

FIGURE 2. PV systems using (a) PV2B and (b) PV2VB PDPP architectures.

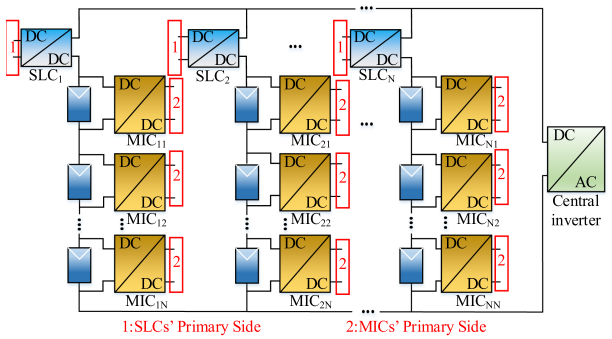

FIGURE 3. General SPDPP architecture.

in which module-level DMPPT is required, PDPP configurations are unable to remove mismatch losses among the series-connected PV modules.

To solve this problem, SPDPP architectures (see Fig. 3) can be employed that are able to mitigate mismatch losses among both PV strings and PV modules with high conversion efficiency [22], [23], [24]. These results highlight the potential for reducing initial costs and improving the LCOE of PV systems through SPDPP architectures. By combining different SDPP and PDPP architectures and varying the connection methods for the primary sides of MICs and SLCs, various SPDPP architectures can be implemented, each with its own advantages and challenges.

A distinct SPDPP topology, based on the PV2PV SDPP concept, was introduced in [22] and [23]. This architecture improves modularity and scalability by utilizing switched inductors in all SPDPP MICs and SLCs. As shown in Table I, the SDPP PV2PV architecture offers several advantages, including low voltage rating and the use of nonisolated MICs, which enhance efficiency, simplify the design, and reduce the cost and size of MICs. In addition, since both the input and output of SDPP PV2PV converters are connected to PV groups (e.g., strings of cells or PV modules), they can be implemented at a very high granularity level [21]. However,

TABLE 1. Comparison of DPP Architectures

Feature \ Architecture	SDPP			PDPP	
	PV2PV [9], [10]	PV2B [11], [12]	PV2VB [13], [14], [15], [25], [26]	PV2B [17], [18]	PV2VB [27], [28], [21]
Cross-coupling effect	Sig	Minimal	Minimal	Minimal	Minimal
Availability against failure	Minimal	Minimal	Minimal	Minimal	Minimal
Processed power	Minimal–Significant[1]	Minimal	Minimal	Moderate	Moderate
Accumulation effect	Yes	No	No	No	No
System efficiency	Fair–Excellent[1]	Good	Good	Good	Good
Scalability	Good	Poor	Excellent	Fair	Excellent
Converters voltage gain	Low	High	Low–Average[2]	High	Low–Average[2]
Converters voltage rating	Low	High	Low–Average[2]	High	Low–Average[2]
Converter Simplicity	Excellent	Fair	Fair	Fair	Fair
Converter Cost	Excellent	Good	Good	Fair–Good	Fair–Good
Isolated Converter	NR	RQD	RQD	OP	RQD
Bidirectional Converter	RQD	RQD	RQD	OP	RQD
Recommended MPPT granularity level	C/SM/M	M	SM/M	S	S

OP: Optional (it adds extra features and options), RQD: Required, NR: Not Recommended, C/SM/M/S: Cell/Submodule/Module/String.
1) It depends on the length of the PV string.
2) It depends on the voltage defined for the virtual bus.

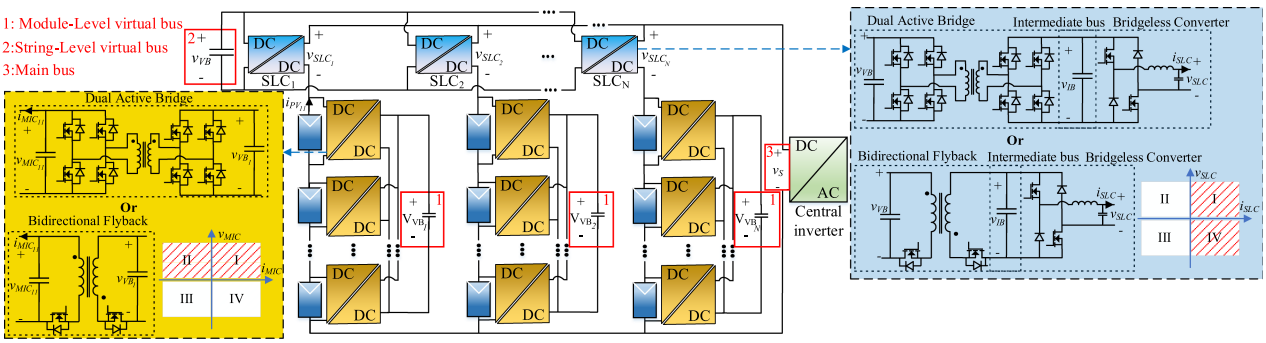

FIGURE 4. Schematic of the proposed PV2VB SPDPP architecture with possible associated SLCs and MICs topologies. In this configuration, the primary side of the MICs is connected directly to the PV modules, so $v_{\mathrm{MIC}_{ji}} = v_{\mathrm{PV}_{ji}}$.

the effectiveness of this architecture in longer PV strings is limited by the accumulation effect [29], [30].

To address this issue, PV2B SDPP architecture can be employed. While they avoid the accumulation effect, they also ensure that the maximum power ratings of MICs remain below the PV module's MPP, even in worst-case scenarios. However, the main challenges in PV2B SDPP/PDPP architectures lie in the following points.

1) The high-voltage step-up ratios required for MICs/SLCs, which create difficulties in designing efficient and cost-effective MICs/SLCs.
2) Components on the main bus side of MICs/SLCs need to tolerate high voltage stress.
3) Scalability is limited, as expanding the system with additional PV modules increases the main bus voltage, which requires a redesign of the MICs/SLCs.

The PV2VB architecture eliminates the drawbacks associated with PV2PV and PV2B architectures. This article introduces a fully PV2VB SPDPP architecture (see Fig. 4). The proposed PV2VB SPDPP architecture builds upon two foundations: the PV2VB PDPP architecture [21], [27], [28] and the PV2VB SDPP architecture introduced in [15]. The PV2VB SPDPP architecture eliminates mismatch-related losses among both series-connected PV modules and parallel-connected PV strings. In addition, it processes only a portion of the PV power without suffering from the accumulation effect, thereby enabling high system conversion efficiency. On top of that, the voltage rating of the MICs and SLCs according to the virtual bus voltage rather than the voltage of the main dc bus. By selecting a lower voltage for the virtual bus, the component voltage ratings of both the MICs and SLCs can be reduced. Furthermore, since the voltage of MICs and SLCs is tied to the virtual bus voltage, expanding the system with additional PV modules does not require upgrading the old MICs and SLCs to higher voltage ratings, improving scalability. However, it is crucial to keep the virtual bus voltage constant and maintain power balance within the virtual buses. This article also provides the necessary equations and control methods to achieve virtual bus balancing.

The rest of this article is organized as follows. Section II outlines the overall structure of the SPDPP architecture, including the associated MICs, SLCs, and central converter, and explains the role of each within the system. Section III details the control loops of the SLCs and central converter, providing

an in-depth analysis of the system's steady-state operation. Section IV discusses the considerations required to design PV2VB SPDPP architecture. Section V presents the real-time simulation with two PLECS real-time (RT) boxes, validating the architecture's performance and highlighting its inherent advantages. Finally, Section VI concludes this article.

II. OVERVIEW OF THE PV2VB SPDPP ARCHITECTURE

In the PV2VB SPDPP architecture, the primary sides of the SLCs and MICs are connected to the virtual buses, as shown in Fig. 4. When the architecture has N_S PV strings each consisting of N_M PV modules, there will be $N_{SM} = N_S \times N_M$ PV modules, N_S module-level virtual buses, and one string-level virtual bus. This means that the total number of objectives, i.e., variables that need to be controlled is

$$N_T = N_{SM} + N_S + 1. \tag{1}$$

Therefore, N_T actuators are required to control all the objectives. To achieve this, the architecture includes N_{SM} MICs, N_S SLCs, and one central converter. The roles of each component within the architecture, their requirements, and potential topologies will be discussed in detail in the following sections.

A. MODULE-INTEGRATED CONVERTER

In this architecture, the primary sides of the MICs are connected to the module-level virtual buses, while the secondary sides are directly connected to the terminals of the PV modules. The primary ports of MICs are connected in parallel. In turn, the distribution of the module-level virtual bus capacitor at the inputs of MICs is possible.

The MICs are responsible for tracking MPP of their respective PV modules. To achieve this, they must inject/or withdraw differential current (i_{MIC}) between the PV string (i_{SLC}) and the MPP current of their respective PV modules (i_{PV}) into/from their corresponding module-level virtual bus. MICs connected to PV modules with higher current generation inject current into their virtual bus, while those connected to lower generating modules draw power. Therefore, MICs must also establish a path for the efficient transfer of power to and from the module-level virtual buses. As a result, MICs must be bidirectional, capable of operating in both the first and second quadrants of the voltage–current (V–I) curve.

Another critical requirement for the MICs is isolation to prevent any short circuiting between PV modules. Although various topologies, such as DAB, push–pull, and forward converters, can be used, BF topologies are often preferred due to their high voltage gain, simplicity, and inherent galvanic isolation, which provide significant advantages [13], [14], [15], [25], [26].

B. STRING-LEVEL CONVERTER

In the PV2VB SPDPP architecture, the SLCs primary side connects to the string-level virtual bus, while its secondary side is located between the PV string and the main bus. The primary goal of SLCs is to ensure that the string-level virtual bus is balanced. To achieve this, SLCs control the string-level virtual bus by manipulating the string currents. SLCs must add or subtract differential voltage between the main bus and the MPP voltage of their respective PV strings. Notably, due to the presence of MICs, each PV module is operating at its MPP even under partial shading. Therefore, the MPP voltage of a PV string is equal to the sum of the MPP voltages of its PV modules. It means SLCs connected to the PV strings with high voltage must generate a negative voltage, while the other must generate a positive one. Since the current of PV strings is always positive (upward in Fig. 4), SLCs connected to the PV strings with high voltage inject the power to the string-level virtual bus, while the others extract the power from the string-level virtual bus. In other words, SLCs must also establish a path for the efficient transfer of power to and from the string-level virtual bus.

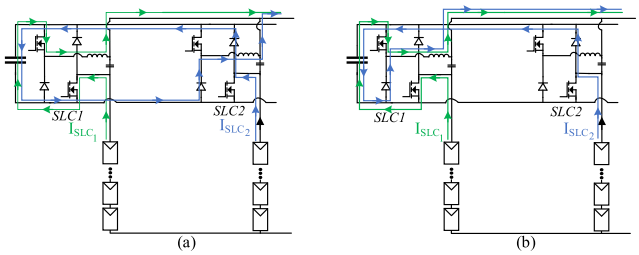

FIGURE 5. Direction of the currents generated by the PV strings in a PV2VB PDPP architecture with nonisolated SLCs. (a) Ideal current path. (b) Nonideal practical current path.

A variety of topologies can be utilized for SLCs, as long as they incorporate three key features. First, they must be capable of operating efficiently in both the first and fourth quadrants of the V–I curve, as previously discussed. In addition, they must be voltage-source converters, enabling connection to the capacitive virtual bus. Finally, isolation is also crucial to allow independent voltage control of each PV string and to ensure that the current from the ith PV string is confined to flow through its respective ith SLC [21], [27]. To explain more, let us consider the case that the SLC is not isolated. For instance, it is realized with only a bridgeless (BL) converter. Furthermore, let us consider a scenario where PV string 1 and PV string 2 generate currents with magnitudes I_{SLC_1} and I_{SLC_2}, respectively. Ideally, I_{SLC_1} must flow through SLC1, and I_{SLC_2} must flow through SLC2, as depicted in Fig. 5(a). However, due to, e.g., minor differences in the SLC parameters, which can be attributed to factors, such as parasitic elements, the current from PV string 2 might instead flow through SLC1 [see Fig. 5(b)]. This situation is undesirable as it leads to increased losses, thermal stress, and power rating of the SLCs. It should be noted that this imbalance can occur with changing switching sequences, not just in the example provided above. Therefore, employing isolated topologies ensures that the current from the ith PV string exclusively flows through the ith SLC, maintaining system balance and efficiency.

In [21], a BF converter followed by a BL converter is used as SLC. BF converters are well suited for this application due to their simplicity and ability to provide galvanic isolation.

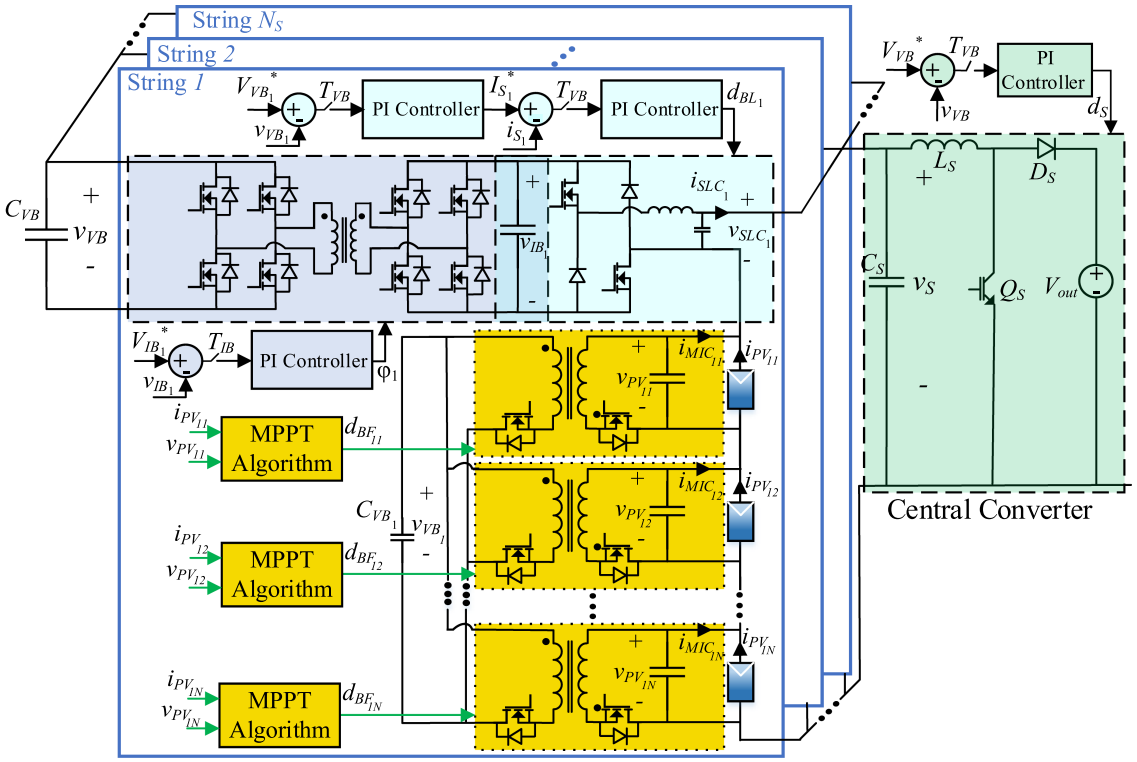

FIGURE 6. PV2VB SPDPP architecture with the associated central converter, SLCs, and MICs topologies considered in this study and the required control loops and MPPT blocks.

However, their use is typically restricted to power levels of a few hundred watts. For higher power levels, it becomes necessary to explore alternative topologies better suited for such applications [32]. As a result, in other studies [27], [28], the BF is replaced with a DAB converter as the first stage of the SLCs, which is more appropriate for high-power applications, while keeping the second-stage BL converters unchanged. The full explanation of the performance of the BF and BL as the SLC, as well as the DAB and BL as the SLC, has been discussed in [21], [27], and [28], respectively. Future research could explore new single-stage topologies that may reduce initial costs while maintaining the same functionality.

C. CENTRAL CONVERTER

In a PV2VB SPDPP architecture, the central converter plays a crucial role in regulating the string-level virtual bus voltage by adjusting the main bus voltage. Specifically, the string-level virtual bus voltage (v_{VB}) is controlled through manipulation of the main bus voltage.

The central converter can be either a dc–dc or dc–ac converter, depending on whether it is connected to a dc or ac grid. Unlike the SLCs and MICs, the central converter does not need to adhere to any architecture-specific requirements.

III. CONTROL STRATEGY FOR THE PV2VB SPDPP ARCHITECTURE

In the PV2VB SPDPP architecture, capacitors are placed at both the module-level and string-level virtual buses, with no direct source or load connected to them. Therefore, it is essential to control the power injected into or withdrawn from the virtual buses to prevent voltage fluctuations, ensuring effective operation of the MICs/SLCs.

For smooth and effective performance, the PV2VB SPDPP architecture must fulfill two main control objectives: tracking the MPP of all PV modules and controlling and stabilizing the voltage of both module-level and string-level virtual buses. Achieving these objectives requires implementing various control loops, as illustrated in Fig. 6. The following sections provide a detailed explanation of the control strategy, the operating principle of the various controllers, and the supporting mathematical equations.

A. MODULE-INTEGRATED CONVERTER

In the PV2VB SPDPP architecture, the primary function of the MICs is to ensure that each PV module operates at its MPP. To achieve this, the ith MIC of the jth PV string continuously monitors the voltage ($v_{\mathrm{PV}_{ji}}$) and current ($i_{\mathrm{PV}_{ji}}$) of its corresponding PV module, as depicted in Fig. 6. The chosen MPPT algorithm then adjusts the control variables of MICs to track the PV module's MPP. Therefore, the first objective of the PV2VB SPDPP architecture, which is tracking the MPP of all PV modules, is achieved by independently applying an MPPT algorithm to each MIC. However, the output voltage of the MICs, which corresponds to the PV module's operating voltage, is closely linked to the module-level virtual bus voltage. Thus, it is critical to regulate and stabilize the virtual bus

voltage to prevent interference with the MPPT algorithm and ensure consistently optimal performance.

B. STRING-LEVEL CONVERTER

In PV2VB SPDPP architecture, a jth SLC controls its output current (i_{SLC_j}) to stabilize the jth module-level virtual bus voltages. This section explores the relation between the jth SLCs output current (i_{SLC_j}) and jth module-level virtual bus voltage (v_{VB_j}). For simplicity, it is assumed that the converters are lossless. Based on these assumptions, power relationship within the architecture can be derived as follows:

$$p_{\mathrm{VB}_j} = p_{\mathrm{out}_j} - p_{\mathrm{in}_j}. \tag{2}$$

In the context of the proposed architecture, p_{VB_j}, p_{out_j}, and p_{in_j}represent the instantaneous jth module-level virtual bus power, the power delivered by the jth string, and the power generated by the PV modules of the jth string, respectively; these values can be computed as follows:

$$p_{\mathrm{VB}_j} = C_{\mathrm{VB}_j} \cdot v_{\mathrm{VB}_j} \cdot \frac{dv_{\mathrm{VB}_j}}{dt} \tag{3}$$

$$p_{\mathrm{out}_j} = v_{\mathrm{PV}_{S_j}} \cdot i_{\mathrm{SLC}_j} = \sum_{i=1}^{N_M} v_{\mathrm{PV}_{ji}} \cdot i_{\mathrm{SLC}_j} \tag{4}$$

$$p_{\mathrm{in}_j} = \sum_{i=1}^{N_M} v_{\mathrm{PV}_{ji}} \cdot i_{\mathrm{PV}_{ji}} \tag{5}$$

where C_{VB_j} and $v_{\mathrm{PV}_{S_j}}$ represent the module-level virtual bus capacitance and summation of PV modules voltage of the jth string, respectively. It should be mentioned that the capacitance is likely to be the same for all the module-level virtual buses ($C_{\mathrm{VB}_1} = C_{\mathrm{VB}_2} = \ldots = C_{\mathrm{VB}_{N_S}}$). The following equation can be obtained by substituting (3)–(5) in (2)

$$\begin{aligned} p_{\mathrm{VB}_j} &= \frac{dv_{\mathrm{VB}}}{dt} \cdot C_{\mathrm{VB}_j} \cdot v_{\mathrm{VB}_j} \\ &= \sum_{i=1}^{N_M} v_{\mathrm{PV}_{ji}} \cdot i_{\mathrm{PV}_{ji}} - v_{\mathrm{PV}_{S_j}} . i_{\mathrm{SLC}_j}. \end{aligned} \tag{6}$$

It is crucial to recognize that the current and voltage of PV modules are governed by MICs to ensure that they operate at their MPPs. In addition, $v_{\mathrm{PV}_{S_j}}$naturally corresponds to the sum of the individual PV module voltages in the jth string. Therefore, the only controllable variable for managing the module-level virtual bus power—and by extension, the module-level virtual bus voltage—is the SLC current. When the average power of the virtual bus at the module level is kept at zero, the following equation is obtained:

$$P_{\mathrm{VB}_j} = 0 \rightarrow I^*_{\mathrm{SLC}_j} = \frac{\sum_{i=1}^{N_M} V_{\mathrm{MPP}_{ji}} \cdot I_{\mathrm{MPP}_{ji}}}{\sum_{i=1}^{N_M} V_{\mathrm{MPP}_{ji}}}, \quad \frac{dv_{\mathrm{VB}_j}}{dt} = 0 \tag{7}$$

where $I^*_{\mathrm{SLC}_j}$ is the equilibrium SLC current at which the module-level virtual bus voltage is constant. It is important to note that capital letters represent the steady-state values of the variables. By combining (6) and (7), the following equation can be derived, which describes the instantaneous rate of change of the virtual bus voltage as a function of the SLC output current:

$$\frac{dv_{\mathrm{VB}_j}}{dt} = \frac{\sum_{i=1}^{N_M} V_{\mathrm{MPP}_{ji}} \cdot I_{\mathrm{MPP}_{ji}}}{C_{\mathrm{VB}_j} \cdot v_{\mathrm{VB}}} \cdot \left(1 - \frac{i_{\mathrm{SLC}_j}}{I^*_{\mathrm{SLC}_j}}\right). \tag{8}$$

Equation (8) shows that the virtual bus voltage rises when the SLC output current drops below the equilibrium level, and vice-versa.

Similar to the PDPP PV2VB architecture in [27] and [28], topologies proposed for the SLCs consist of two stages, with their performance decoupled by an intermediate bus capacitor, referred to as the decoupling capacitor. When DAB converters are employed as the first stage, the voltage of this intermediate bus is regulated by controlling the phase shift (φ) between the two ac voltage waveforms across the windings of the isolation transformer, using a closed-loop controller. Power is transferred from the leading bridge to the lagging bridge based on this phase shift. The BL converters then generate both positive and negative voltages by adjusting the duty cycle accordingly. A detailed explanation of the operation of the proposed SLCs has been provided in [27] and [28].

C. CENTRAL CONVERTER

In the PV2VB SPDPP architecture, the central converter regulates the main bus voltage (v_S) through its duty cycle. However, this regulation primarily aims to stabilize the string-level virtual bus voltage (v_{VB}), as shown in Fig. 6. Using a procedure similar to Section III-B, the following equation is derived:

$$P_{\mathrm{VB}} = 0 \rightarrow V^*_S = \frac{\sum_{j=1}^{N_S} V_{\mathrm{PV}_{S_j}} \cdot I^*_{\mathrm{SLC}_j}}{\sum_{j=1}^{N_S} I^*_{\mathrm{SLC}_j}}, \frac{dv_{\mathrm{VB}}}{dt} = 0 \tag{9}$$

where V^*_S represents the equilibrium main bus voltage, at which the string-level virtual bus voltage remains constant. In addition, the instantaneous rate of change of the string-level virtual bus voltage as a function of the main bus voltage can be derived as follows:

$$\frac{dv_{\mathrm{VB}}}{dt} = \frac{\sum_{j=1}^{N_S} V_{\mathrm{PV}_{S_j}} \cdot I_{\mathrm{SLC}_j}}{C_{\mathrm{VB}} \cdot v_{\mathrm{VB}}} \cdot \left(1 - \frac{v_S}{V^*_S}\right) \tag{10}$$

where C_{VB}represents the string-level virtual bus capacitance. Equation (10) indicates that the string-level virtual bus voltage increases when the main bus voltage drops below the equilibrium level and decreases when the main bus voltage exceeds the equilibrium level.

Therefore, the second objective of the PV2VB SPDPP architecture, which is controlling and stabilizing the module-level and string-level virtual buses' voltages, is achieved by regulating the SLCs output current to control the module-level virtual bus, and the main bus voltage to control the string-level virtual bus.

IV. DESIGN CONSIDERATIONS FOR THE PV2VB SPDPP ARCHITECTURE

For the PV2VB PDPP architecture, a physical setup has been implemented, and its performance has been validated through experimental testing. The experimental results demonstrate system efficiency ranging from 96% to 99%, as presented in [27]. In addition, Olalla et al. [15] investigated various shading scenarios and reported an efficiency of up to 97.1% for the PV2VB SDPP architecture. These findings indicate a promising efficiency for the fully PV2VB SPDPP architecture, which integrates both PV2VB PDPP and PV2VB SDPP. In the following sections, the considerations necessary for ensuring the desirable operation of the SPDPP architecture are discussed.

A. MODULE-LEVEL VIRTUAL BUSES AND MICS RATING

Since the primary side of the MICs is connected to the module-level virtual bus, the voltage rating of the primary-side components is dependent on the module-level virtual bus voltage. Selecting a very low voltage for the module-level virtual bus increases the required capacitance, as the maximum allowable voltage ripple decreases [33]. In addition, low virtual bus voltage results in higher conduction losses for the DPP converters due to increased current. Conversely, selecting a very high module-level virtual bus voltage requires components with higher voltage ratings, leading to increased component costs and switching losses. To achieve a 1:1 conversion ratio and allow for symmetrical implementation on both the primary and secondary sides of the MICs, it is recommended that the module-level virtual bus voltage be set close to the nominal MPP voltage of the PV modules, denoted as (V_{MPP_n}).

MICs in a string are activated when a current mismatch occurs among the PV modules within that string. In the worst-case scenario, the power rating P_{MIC} of the MICs is equal to [15]

$$\frac{P_{\mathrm{MIC}}}{I_{\mathrm{MPP}_n} \cdot V_{\mathrm{MPP}_n}} = \frac{(N_M - 1)}{N_M} \tag{11}$$

where I_{MPP_n} and V_{MPP_n}represent the nominal MPP current and voltage of the PV modules, respectively. However, such extreme mismatch conditions are rare. The impact of reduced MIC ratings in the SDPP architecture has been studied in detail over long-term scenarios in [15].

B. STRING-LEVEL VIRTUAL BUS AND SLCS RATING

In the proposed architecture, the primary sides and secondary sides of SLCs first-stage DAB converter in Fig. 6 are connected to the string-level virtual bus and to the intermediate bus voltage, respectively. Consequently, the voltage rating of the first stage (DAB or BF converters) is determined by the voltage at the intermediate bus. Similar to MICs, to maintain a 1:1 conversion ratio and facilitate symmetrical implementation on both the primary and secondary sides of the first stage, it is advisable to select the string-level virtual bus voltage to be close to the intermediate bus voltage (V_{IB_j}). In contrast to MICs, SLCs begin processing power when voltage mismatches occur among PV strings. A comprehensive power rating analysis of SLCs can be found in [27]. Although Nazer et al. [27] focus on PV2V PDPP architecture, the same power rating analysis can be applied to the proposed SPDPP architecture.

In the SPDPP architecture, unlike the PV2VB PDPP architecture, the voltage differences between PV strings are generally not significant, particularly when DMPPT is implemented at the submodule level. In this scenario, there are no bypass diodes to circumvent a PV submodule, and the effects of irradiance mismatch or temperature variation on submodule-level MPP tracking are relatively minor. As a result, the voltage discrepancies between strings will not be as pronounced as in the PV2VB PDPP architecture when all PV modules are functioning. This allows for the selection of a string-level virtual bus voltage that is lower than that in the PV2VB PDPP architecture.

However, if short-circuited PV modules occur within a PV string, resulting in a drop in the string voltage, it is crucial for the SLCs to generate sufficient voltage to compensate for the differential voltage between the main bus voltage and the PV string voltage to ensure operation at the MPP. Therefore, selecting a very low voltage for the string-level virtual bus is not advisable in such cases. Ultimately, the selection of the appropriate string-level virtual bus voltage primarily depends on fault conditions rather than shading.

While BF converters are preferred for MICs, the situation differs for SLCs, which may require higher power ratings. BF converters are typically limited to power outputs of a few hundred watts, making them less suitable for SLCs. As a result, DAB converters are favored for this application. In this study, BF converters are employed for the MICs, while DAB converters are utilized for the first stage of the SLCs. BL converters as the second stage of SLCs are responsible to generate the required negative and positive voltage so that the SLCs can work in the first and fourth quadrant of the *I–V* curve, as shown in Fig. 4 [27].

C. CONTROLLERS

Assuming a search-based MPPT algorithm, such as perturb and observe, the architecture incorporates three distinct control loops:

1) a central controller that regulates the string-level virtual bus voltage;
2) SLC controllers that adjust the module-level virtual bus voltages;
3) controllers that manage the intermediate bus voltage within an SLC, as illustrated in Fig. 6.

In this study, proportional–integral controllers are employed for system control.

In contrast to the third controller, the first two controllers, which regulate the main bus voltage and string current, may inadvertently disrupt the operation of the MPPT algorithm. Therefore, achieving a harmonious control mechanism that effectively integrates with the MPPT algorithms requires

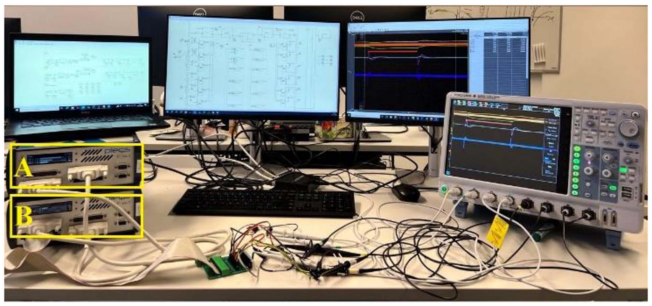

FIGURE 7. Real-time simulation setup with two PLECS RT-Box-2. (a) Plant and (b) controller for real-time simulations.

attention. To mitigate interference between the SLC controllers and the MPPT algorithm, it is advisable to extend the sampling times of these controllers. This can be expressed mathematically as follows:

$$T_{\mathrm{VB}} = T_{\mathrm{VB}_M} = 4 \cdot m \cdot T_{\mathrm{MPPT}}|_{m=1,2,\ldots} \tag{12}$$

where T_{VB}, T_{VB_M}, and T_{MPPT} represent the sampling time of the string-level virtual bus controller, the sampling time of the module-level virtual bus controller, and the perturbation period of the MPPT algorithm, respectively. By designing the controllers with these increased sampling times, the MPPT algorithms can operate independently, without being hindered by premature or conflicting control actions from the controllers. This careful coordination is for maintaining accurate MPP tracking and optimizing the overall performance of the PV system.

V. REAL-TIME SIMULATION RESULTS

This section demonstrates the ability of the proposed fully PV2VB SPDPP architecture to perform MPPT at the module level while maintaining constant module-level and string-level virtual bus voltages. Fig. 7 illustrates the real-time simulation setup, consisting of two PLECS RT-Box-2 for the real-time simulation model. One RT box emulates the converters and PV modules, measures the corresponding voltages and currents, and transfers these signals to the second RT box. The other RT box executes the control algorithms, generates the pulsewidth modulation (PWM) signals, and sends them back to the first RT box for implementation to complete the closed loop. The electrical specifications and component values of the architecture are summarized in Table II and control parameters in Table III. The evaluated architecture connects two PV strings to two SLCs, with each string comprising six series-connected PV modules, each equipped with an associated MIC (see Fig. 8). There is no limitation on using alternative modulation methods for the converters; however, PWM modulation has been implemented in this study.

To assess the architecture's overall performance, three distinct tests were conducted:

1) current mismatch among PV modules, with an emphasis on evaluating the performance of the MICs;
2) voltage mismatch between PV strings, highlighting the functionality and effectiveness of the SLCs;
3) scenarios I and II occur simultaneously to evaluate the performance of the MICs and SLCs in mitigating mismatches at the same time.

In all scenarios, sudden and fast changes have been introduced—conditions that are more extreme than those typically found in real environments, where variations occur more gradually. This ensures that the control strategy is tested under harsher conditions.

TABLE 2. Electrical Specifications and Component Parameters of the System

	Parameter	Symbol	Value
Electrical specifications	PV system rated power	P_{sys}	4 kW
	String-level virtual bus voltage	V_{VB}	200 V
	Module-level virtual bus voltage	$V_{\mathrm{VB_j}}$	70 V
	MPP voltage of the PV module	V_{MPP}	64 V
	MPP current of the PV module	I_{MPP}	5.3 A
	Switching frequency	f_{SW}	10 kHz
	Discretization time step of real-time simulation	T_{disc}	6.25 μs
	MPPT algorithm perturbation period	T_{MPPT}	5 ms
Components' parameters	String-level virtual bus capacitance	C_{VB}	10 mF
	Module-level virtual bus capacitance	$C_{\mathrm{VB_1}}, C_{\mathrm{VB_2}}$	40 mF

TABLE 3. Controllers' Parameters

	Parameter	Symbol	Value
Central Controller	Sampling Time	T_{VB}	20 ms
	Proportional Coefficient*	$K_{P_{\mathrm{VB}}}$	0.005
	Integral Coefficient	$K_{I_{\mathrm{VB}}}$	0.005
DAB Controller	Sampling Time	T_{IB}	100 μs
	Proportional Coefficient	$K_{P_{\mathrm{IB}}}$	0.0025
	Integral Coefficient	$K_{I_{\mathrm{IB}}}$	0.015
BL Controller (inner loop)	Sampling Time	T_{BL1}	20 ms
	Proportional Coefficient	$K_{P_{\mathrm{BL1}}}$	0.06
	Integral Coefficient	$K_{I_{\mathrm{BL1}}}$	0.2
BL Controller (outer loop)	Sampling Time	T_{BL2}	20 ms
	Proportional Coefficient	$K_{P_{\mathrm{BL2}}}$	0.07
	Integral Coefficient	$K_{I_{\mathrm{BL2}}}$	0.14

A. CURRENT MISMATCHES AMONG PV MODULES

In Scenario I, all PV modules initially operate under uniform conditions. A partial shading scenario occurs at 1.4 s, as illustrated in Fig. 8. In Scenario I, it is assumed that no bypass diodes are activated in the shaded PV modules. Therefore, they operate at a lower MPP current with respect to the unshaded PV modules, but at a similar MPP voltage. At 10.4 s (9 s after the first disruption), the system is restored to uniform conditions to evaluate the architecture's overall performance, particularly focusing on the performance of the MICs. During this assessment, there is no voltage mismatch between string 1 and string 2.

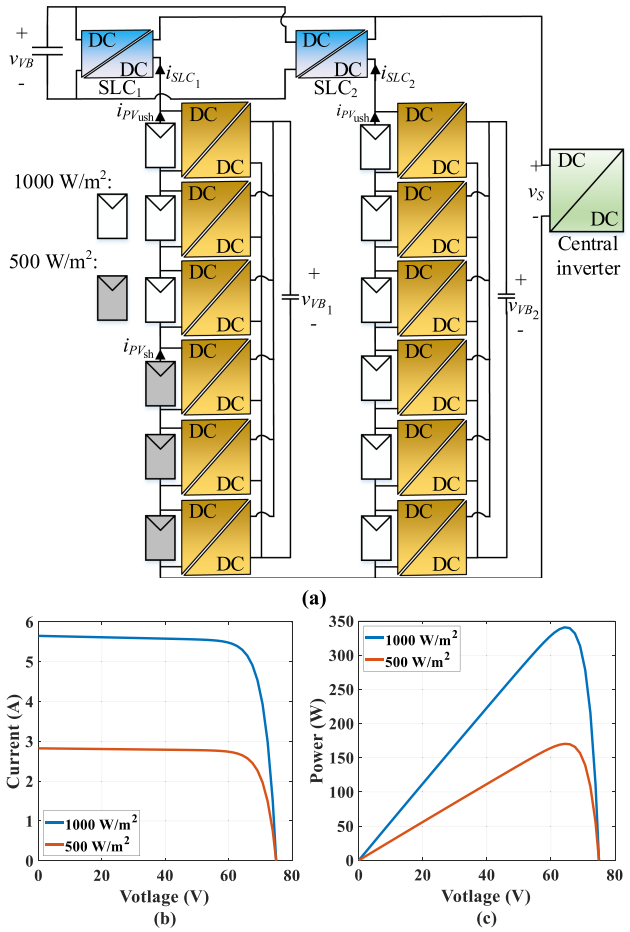

FIGURE 8. (a) Evaluated PV2VB SPDPP architecture using two PLECS RT boxes. (b) *I–V* curves and (c) *P–V* curves used in the real-time simulation.

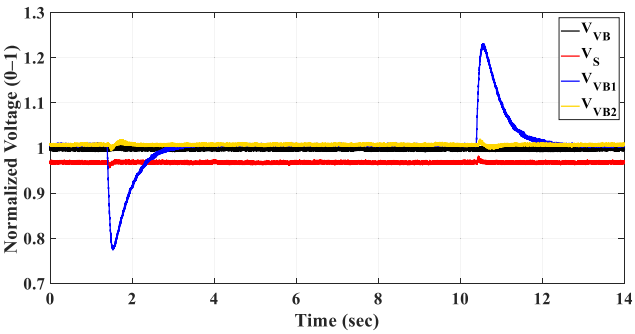

FIGURE 9. Normalized voltage waveform (V_{VB1} and V_{VB2}, V_{VB}, and V_S are normalized by 70 V, 200 V, and 400 V, respectively). Scenario I: three PV modules in string 1 transition from uniform condition to mismatch conditions, as shown in Fig. 8, and then return to the uniform condition.

Fig. 9 illustrates the voltage waveforms of the module-level virtual buses, the string-level virtual bus, and the main bus during Scenario I. The results demonstrate that the controllers effectively maintain the virtual bus voltages at both the module and string levels. After each disturbance, the voltages successfully return to their desired values. Furthermore, the following observations are noted.

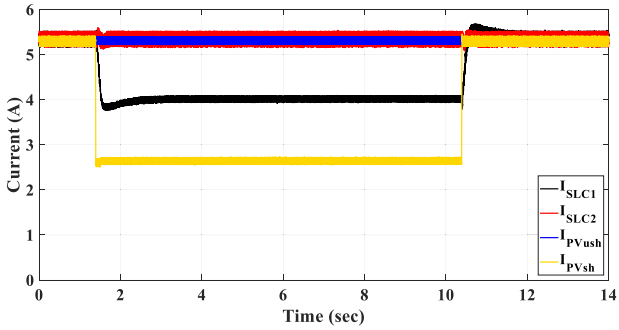

FIGURE 10. Current waveform. Scenario I: three PV modules in string 1 transition from uniform condition to mismatch conditions, as shown in Fig. 8, and then return to the uniform condition.

Module-Level Virtual Buses: In String 1, current mismatches among the PV modules result in voltage variations on the associated module-level virtual buses. In contrast, as no mismatches occur in String 2, its module-level virtual bus remains largely unaffected.

String-Level Virtual Bus: Since there are no mismatches among the PV string voltages, the string-level virtual bus voltage remains stable and unaffected by disturbances.

Main Bus Voltage: The main bus voltage closely follows the value predicted by (9), thereby validating the mathematical model presented.

These findings confirm the system's capability to manage voltage dynamics effectively under the given conditions.

Fig. 10 presents the current of a shaded PV module (I_{PVsh}) and an unshaded PV module (I_{PVush}). The figure demonstrates the architecture's capability to effectively track MPP of PV modules during transitions. Key observations include the following.

Tracking MPP: The MPP currents of both shaded and unshaded PV modules adjust appropriately during transitions, highlighting the architecture's ability to adapt to varying shading conditions and maintain optimal power extraction.

Impact of Mismatches in String 1: Mismatches only occur in string 1, leading to changes in its current (I_{SLC1}), as determined by (7). This adjustment ensures that the module-level virtual bus voltage remains constant at 70 V. In contrast, the current of string 2 (I_{SLC2}) remains unaffected, as no mismatches are present in string 2.

Together, Figs. 9 and 10 confirm the effective performance of the PV2VB SPDPP architecture in handling current mismatches among PV modules while maintaining system stability and efficient operation.

B. VOLTAGE MISMATCHES AMONG PV STRINGS

There are various factors that can cause mismatches among PV string MPP voltages, including PV module short circuits, bypass diode activation, temperature differences, and more. In Scenario II, the case where the bypass diode is activated is considered; however, this does not compromise the generality of the system's ability to compensate for voltage mismatches caused by other factors.

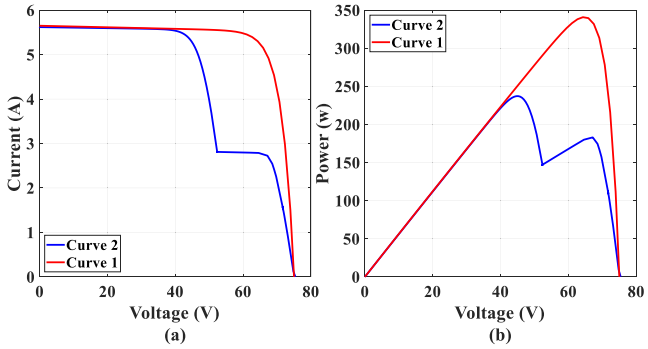

FIGURE 11. PV module's (a) *I–V* curves and (b) *P–V* curves used in the real-time simulation.

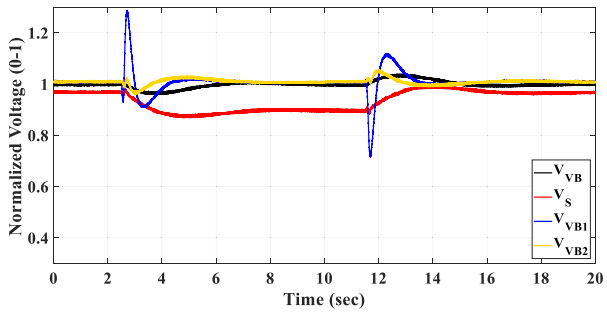

FIGURE 12. Normalized voltage waveform (V_{VB1} and V_{VB2}, V_{VB}, and V_S are normalized by 70 V, 200 V, and 400 V, respectively). Scenario II: three PV modules in string 1 transition from uniform condition to voltage mismatch conditions, as shown in Fig. 11, and then return to the uniform condition.

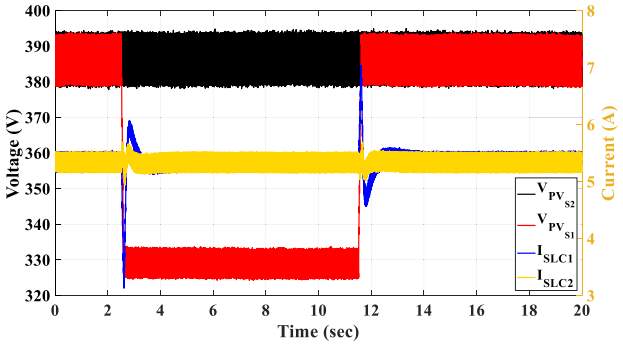

FIGURE 13. Strings' voltage and current waveform. Scenario II: three PV modules in string 1 transition from uniform condition to voltage mismatch conditions, as shown in Fig. 11, and then return to the uniform condition.

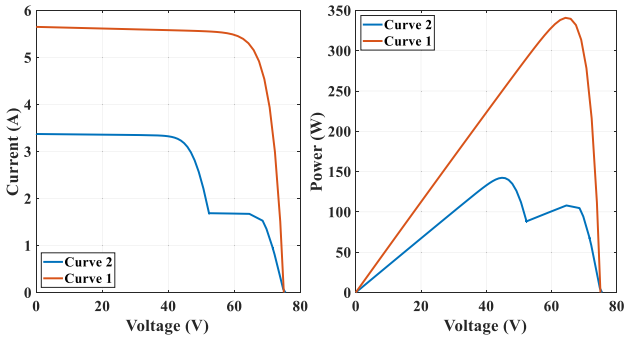

FIGURE 14. PV module's (a) *I–V* curves and (b) *P–V* curves used in the real-time simulation.

In Scenario II, mismatches among PV string voltages are introduced to assess the system's response and performance. In this scenario, initially, all PV modules operate under uniform conditions, ensuring no mismatches in the system. In this condition, all PV modules generate an *I–V* curve equal to "Curve 1" in Fig. 11. At approximately 2.3 s, three out of six PV modules in string 1 transition to generate an *I–V* curve equal to "Curve 2" (see Fig. 11), while the remaining PV modules keep generating "Curve 1." This results in a voltage mismatch between String 1 and String 2. Finally, at approximately 11.3 s (9 s after the first distribution), all PV modules return to their uniform conditions, eliminating the voltage mismatch. This scenario is designed to evaluate the ability of the PV2VB SPDPP architecture to manage voltage mismatches among PV strings dynamically and maintain stable system performance during transitions.

Fig. 12 illustrates the voltage waveforms of the module-level virtual buses, string-level virtual bus, and main bus during Scenario II. The voltage mismatches among the PV modules of string 1 lead to observable variations in all virtual buses' voltage. This is expected, as the mismatch creates voltage imbalances between the two strings. Moreover, the module-level virtual bus associated with string 1 experiences more pronounced voltage variation due to the localized nature of the mismatches within this string. Besides, Fig. 12 shows that, despite the disturbances, the system effectively restores the string-level virtual bus voltages to the desired value of 200 V by manipulating the main bus voltage according to (9).

Fig. 12, thus, validates the ability of the PV2VB SPDPP architecture to manage and mitigate the effects of voltage mismatches effectively.

Fig. 13 illustrates that both strings operate at 385 V under uniform conditions. However, when a mismatch occurs, string 1 and string 2 operate at 385 V and 330 V, respectively, which correspond to the summation of the MPP voltages of their associated PV modules. This demonstrates that the proposed architecture effectively handles voltage mismatches between strings. Furthermore, according to (7), since the global MPP current of the PV modules remains unchanged before and after introducing the mismatch, the equilibrium currents in the strings also remain constant. This observation is validated through real-time simulation.

C. MISMATCHES AMONG PV STRINGS' VOLTAGES AND MODULES' CURRENTS

In Scenario III, both PV string voltage and PV module current mismatches are introduced to evaluate system performance. Initially, all PV modules operate uniformly, generating an identical *I–V* curve ("Curve 1" in Fig. 14). At around 0.8 s, three out of six PV modules in String 1 transition to a different *I–V* curve ("Curve 2" in Fig. 14), while the rest maintain "Curve 1." This leads to both voltage mismatches between Strings 1 and 2 and current imbalances within String 1. At

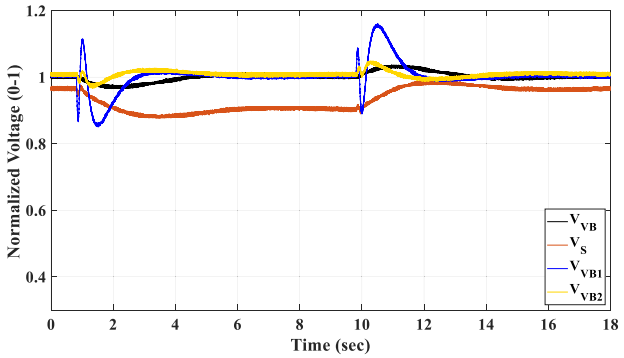

FIGURE 15. Normalized voltage waveform (V_{VB1} and V_{VB2}, V_{VB}, and V_S are normalized by 70 V, 200 V, and 400 V, respectively). Scenario III: three PV modules in string 1 transition from uniform condition to voltage mismatch conditions, as shown in Fig. 14, and then return to the uniform condition.

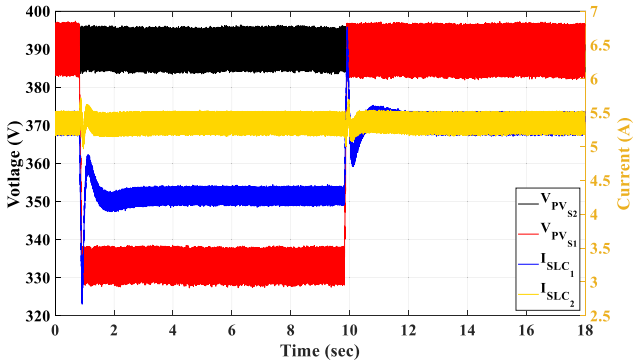

FIGURE 16. Strings' voltage and current waveform. Scenario III: three PV modules in string 1 transition from uniform condition to voltage mismatch conditions, as shown in Fig. 14, and then return to the uniform condition.

approximately 9.8 s, all PV modules return to uniform conditions, resolving these mismatches.

This scenario tests the PV2VB SPDPP architecture's capability to manage simultaneous voltage and current mismatches effectively. Fig. 15 illustrates the resulting voltage fluctuations across module-level, string-level, and main virtual buses, highlighting the expected voltage imbalances due to mismatches in String 1. Despite these disturbances, the system successfully restores the module-level and string-level virtual bus voltages to the target values of 70 and 200 V by adjusting the main bus voltage.

Fig. 16 further demonstrates that, under uniform conditions, both strings operate at 385 V. However, when mismatches occur, String 1 remains at 385 V, while String 2 drops to 330 V, reflecting the sum of the MPP voltages of their respective PV modules. In addition, due to current mismatches within String 1, the string current (I_{SLC1}) fluctuates as predicted by (7), a behaviour confirmed through real-time simulation.

Overall, Figs. 15 and 16 demonstrate that the architecture maintains efficient MPP tracking while gradually adjusting virtual bus voltages when the system is subject to significant variations in both voltage and current. This controlled response ensures that the slower reaction of the central controller does not compromise MPPT efficiency.

The PV2VB SPDPP architecture requires multiple PV emulators—12 for the system studied—but limited availability led to reliance on real-time simulation-based validation. A complete evaluation of the efficiency of the proposed architecture was not possible, owing to the constraints of the RT boxes. Nonetheless, as mentioned in Section IV, experiments from previous work have shown that PV2VB PDPP architectures achieve efficiency between 96% and 99%, while efficiencies up to 97.1% are reported for PV2VB SDPP architectures, suggesting promising efficiency for the fully PV2VB SPDPP architecture. On the other hand, outdoor validation of such a large system is complicated by the need for numerous PV modules, large installation spaces, stringent safety regulations, equipment relocation logistics, variable weather conditions, and typical low sunlight in The Netherlands. Future work should consider implementing a physical setup to further validate the system's performance.

Eventually, one important aspect of this architecture is the wiring and connector design. Since each module is also connected to a shared virtual bus, it is necessary to carefully arrange the PV strings to minimize wiring complexity and mitigate related issues.

VI. CONCLUSION

This article proposes a novel fully PV2VB SPDPP architecture for PV systems, designed to effectively mitigate both current and voltage mismatches among PV modules and strings. The study thoroughly elaborates on the system's mathematical framework, control methods, SLCs, and MICs duties, and details the requirements for SLCs, MICs, controllers, and the overall architecture. Real-time simulations validate the architecture's performance, demonstrating its ability to maintain stable module-level and string-level virtual bus voltages while efficiently tracking the MPP of PV modules.

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