Dual-Loop Passive-Input Sigma–Delta Modulator

By

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Abstract

This thesis presents a passive-input dual-loop continuous-time sigma-delta modulator that suppresses first-stage quantization noise in the analog domain. The proposed dual-loop architecture requires only a fixed digital attenuation, avoiding a complex digital cancellation filter and dedicated calibration loop. Implemented in TSMC 65 nm CMOS, the modulator operates from a 1.2 V supply with a 100 MHz sampling frequency and around 200 kHz signal bandwidth. Schematic-level simulations achieve 100.61 dB peak SNDR, 103.66 dB dynamic range, and 183.1 dB FoM_{SNDR} while consuming 1.094 mW. RCC-extracted simulations achieve 100 dB SNR and 99.53 dB SNDR, demonstrating that the architecture retains high resolution and competitive energy efficiency.

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Chapter 1. Introduction

High-resolution ADCs are essential in automotive, medical imaging, and battery-powered Internet of Things (IoT) systems, where dynamic ranges above 90 dB may be required, along with high linearity and low power [1]–[3]. These requirements are difficult to satisfy simultaneously because reducing noise and increasing bandwidth or linearity generally raises the power consumption.

The energy efficiency of high-resolution ADCs is commonly evaluated using the Schreier figure of merit FoM_{SNDR} [4], which combines the peak signal-to-noise-and-distortion ratio (SNDR), signal bandwidth, and power consumption. Among the surveyed state-of-the-art noise-shaping ADCs with signal bandwidths of 150–250 kHz and FoM_{SNDR} >170 dB, none has demonstrated an SNDR above 94 dB for input frequencies spanning the full signal band [1], [5], [6], [7]–[9]. Therefore, achieving an SNDR above 100 dB over a 200 kHz bandwidth while maintaining competitive energy efficiency remains challenging.

Successive-approximation-register (SAR) ADCs offer good energy efficiency, but their switched-capacitor inputs require a power-hungry driver and a front-end anti-aliasing filter [1], [3]. In contrast, CTSDMs provide inherent anti-alias filtering and often have a resistive input that is easier to drive [1], [10], [11]. Replacing the conventional active input integrator with a passive RC network can further reduce front-end power and improve linearity [6]. However, optimizing this network to meet thermal-noise, capacitor area and noise-shaping requirements can be challenging [12]. A multi-stage noise-shaping (MASH) architecture can alleviate this trade-off by using a second stage to suppress the residual first-stage quantization noise. Still, these typically require accurate matching between analog transfer functions and digital cancellation filters [13]. To address these limitations, this thesis investigates the design of a passive-input MASH CTSDM targeting a signal bandwidth of about 200 kHz, an SNDR above 100 dB, a dynamic range above 100 dB, and an FoM_{SNDR} above 181 dB.

1.1. Active versus Passive Continuous-Time Sigma-Delta Modulators

Figure 1.1 shows the basic structure of a CTSDM. It consists of a continuous-time loop filter, a clocked quantizer, and a digital-to-analog converter (DAC) in a negative-feedback path. The loop can be linearized by replacing the quantizer with an equivalent gain κ and an additive quantization error E_Q. The input signal V_{IN} and the feedback signal V_{DAC} are processed by the transfer functions $L_0(s)$ and $L_1(s)$, respectively, producing the quantizer-input voltage V_Y. The quantizer quantizes V_Y at the sampling frequency $f_s = 1/T_s$, and produces the output bitstream D_{OUT}.

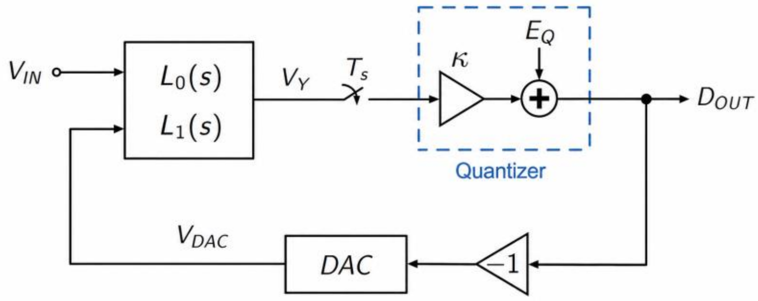


Figure 1.1 Basic block diagram of a continuous-time sigma-delta modulator.

Because $L_0(s)$ and $L_1(s)$ describe continuous-time paths, they cannot be inserted directly into a z-domain loop equation. Assuming negligible input aliasing and an NRZ feedback DAC, the corresponding sampled-data transfer functions are [11]:

$$L_0(z) = \mathcal{Z}_{T_s}\{\mathcal{L}^{-1}[L_0(s)]\}$$
$$L_1(z) = (1 - z^{-1})\mathcal{Z}_{T_s}\left\{\mathcal{L}^{-1}\left[\frac{L_1(s)}{s}\right]\right\}$$

Here, $\mathcal{Z}_{T_s}\{\cdot\}$ denotes sampling the corresponding time-domain response at $t = nT_s$ followed by the z-transform, and $L_1(z)$ includes the NRZ DAC pulse response. Using these discrete-time equivalents, the output bitstream can be written as:

$$D_{OUT} = V_{\mathrm{IN}}(z)\frac{\kappa L_0(z)}{1+\kappa L_1(z)} + E_Q(z)\frac{1}{1+\kappa L_1(z)} \tag{1.1}$$

The signal transfer function (STF) and noise transfer function (NTF) are therefore given by:

$$STF(z) = \frac{\kappa L_0(z)}{1+\kappa L_1(z)} \tag{1.2}$$

and

$$NTF(z) = \frac{1}{1+\kappa L_1(z)} \tag{1.3}$$

The main difference between active and passive CTSDMs is the distribution of gain around the loop. In an active CTSDM, the DC gain is provided by active integrators. In a fully passive CTSDM, the loop filter consists only of passive filters, which significantly reduce the input swing of the quantizer. Therefore, a high quantizer gain is required to recover the total loop gain and maintain the SDM stability. Therefore, a single-bit quantizer (comparator) is commonly used in passive modulators because its gain is high and adjusted automatically based on the loop filter gain [6].

The difference between active and passive integrators can be illustrated using first-order passive and active RC networks shown in Figure 1.2. Their transfer functions are:

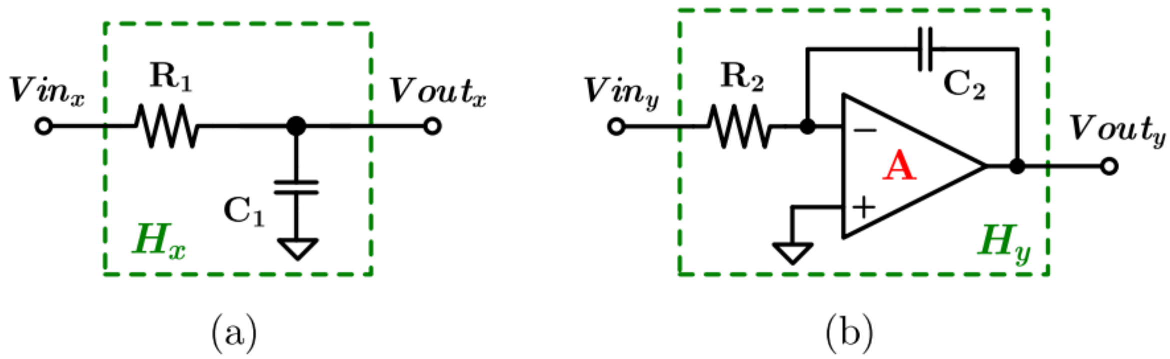


Figure 1.2 RC integrators: (a) Passive and (b) Active [14].

$$H_x(s) = \frac{1}{1+sR_1C_1} \tag{1.4}$$

and

$$H_y(s) \approx \frac{-A}{1+sR_2C_2(A+1)} \tag{1.5}$$

Both transfer functions describe lossy low-pass networks. Their pole frequencies can be made approximately equal when $R_1C_1 = R_2C_2(A+1)$. The difference between their frequency responses in this case will be only the DC gain (A). Therefore, the voltage at the comparator input is approximately A times smaller in the passive implementation. Furthermore, the required time constant in the active integrator is (A+1) less than that in the passive integrator. Therefore, using passive integrators increases the area, especially for low bandwidths. However, at bandwidths greater than a few hundred kilohertz, the required time constants are smaller, making the passive implementation more suitable for higher-bandwidth applications.

Traditional SDMs consist of a number of active integrators equal to the loop filter order [11]. In contrast, hybrid active–passive architectures use fewer amplifiers than the loop-filter order [15]–[17], while fully passive implementations eliminate amplifiers [18]–[20]. This reduces power consumption and improves energy efficiency [21]. Furthermore, passive integrators can simplify the design process by eliminating the need for moderate- or high-gain amplifiers and the associated stability concerns associated with their multiple poles and zeros [14]. These advantages are important in scaled CMOS technologies, in which high-gain amplifier design is challenging due to reduced supply voltage and intrinsic gain [14].

The effective gain of a two-level quantizer can be determined by evaluating the root-mean-square (rms) values of its output and input signals:

$$\kappa = \frac{D_{OUT,\mathrm{rms}}}{V_{Y,\mathrm{rms}}} \tag{1.6}$$

For a normalized single-bit output with values $+1$ and -1, $D_{OUT,\mathrm{rms}} = 1$, and hence

$$\kappa = \frac{1}{V_{Y,\mathrm{rms}}} \tag{1.7}$$

Equation (1.7) shows why a passive loop filter can still provide a large total loop gain. The passive filter attenuates the signal applied to the quantizer, while its output remains at a full digital level. Therefore, the smaller $V_{Y,\mathrm{rms}}$ produces a larger equivalent quantizer gain. For a two-level quantizer, this gain automatically adjusts itself as the loop-filter attenuation changes. A reduction in loop-filter DC gain can therefore be partly compensated by an increase in κ, although this also increases the input-referred noise of the quantizer.

The comparator gain is nonlinear and decreases with increasing input signal amplitude [14]. This reduction in κ at larger input amplitudes results from changes in the quantizer bitstream. As the input approaches full scale, the bitstream contains longer sequences of identical decisions, thereby increasing its low-frequency content. This content is emphasized by the low-pass loop filter, resulting in a larger rms voltage at the quantizer input. Since the amplitude of the two-level quantizer output remains fixed, the equivalent gain consequently decreases.

1.2. Passive-Input Loop Filter Topologies

This section examines passive-input and hybrid loop-filter architectures for CTSDMs. First, it introduces a fully passive loop filter. A passive RC–OTA topology is then introduced to increase the comparator input swing, reduce loading between filter stages, and provide more clearly defined pole and zero locations. For both topologies, the corresponding transfer functions, dominant noise sources, and associated noise–area–performance trade-offs are discussed. Finally, previous single-loop passive-input and hybrid CTSDM implementations are reviewed to trace the development of these architectures and identify the remaining limitations that motivate the adoption of the MASH approach discussed in the following section.

1.2.1. Fully Passive Loop Filter

Figure 1.3 shows a CTSDM whose loop filter is implemented entirely using resistors and capacitors. The first low-pass filter is formed by R_{IN}, R_{DAC}, and C_1, while R_2, R_3, and C_2 form the second low-pass filter and introduce a high-frequency zero. Since the loop filter contains no active gain stage, its voltage gain does not exceed unity, and the effective loop gain is supplied by the equivalent gain of the single-bit quantizer, as discussed in Section 1.1. With appropriate pole and zero locations, this structure can provide second-order quantization-noise shaping.

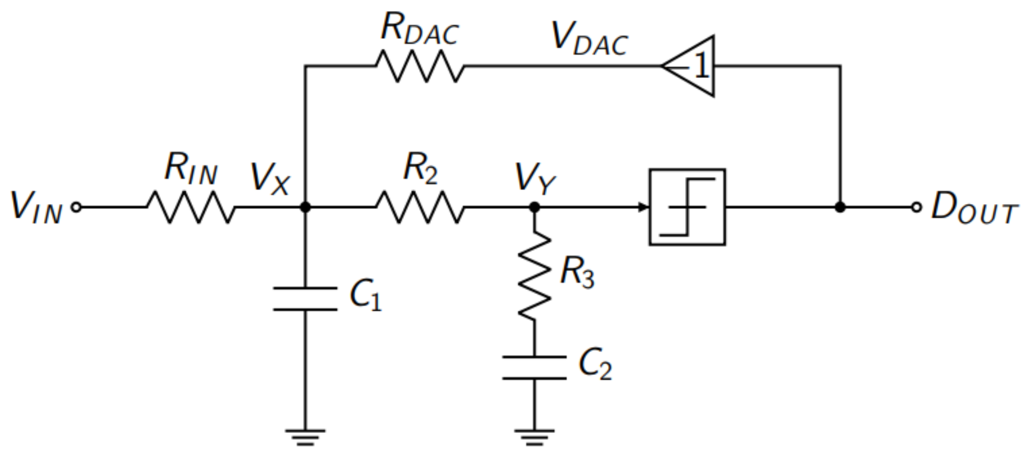


Figure 1.3 CTSDM with a fully passive loop filter [12].

The transfer function from the DAC output to the quantizer input is:

$$L_1(s) = \frac{V_Y(s)}{V_{DAC}(s)} = \left(\frac{R_{IN}}{R_{IN}+R_{DAC}}\right) \frac{1+sC_2R_3}{1+s[C_2(R_S+R_P)+C_1R_P]+s^2C_1C_2R_SR_P} \tag{1.8}$$

The two resistance terms used in the transfer function are ($R_P = R_{IN} \parallel R_{DAC}$) and ($R_S = R_2 + R_3$). The low-frequency gain is determined by the resistive divider formed by R_{IN} and R_{DAC}. The numerator introduces a zero at $\omega_z = \frac{1}{R_3C_2}$, while the denominator produces two real poles. When $R_S \gg R_P$, their frequencies can be approximated as $\omega_{p1} \approx \frac{1}{R_PC_1}$ and $\omega_{p2} \approx \frac{1}{R_SC_2}$. These expressions are only approximations because the passive sections are mutually loaded. The zero changes the asymptotic response above ω_z from a second-order roll-off of approximately -40 dB/dec to approximately -20 dB/dec.

The dominant thermal-noise sources are the comparator noise, R_{IN}, R_{DAC}, and R_2. The noise contributions from R_{IN} and R_{DAC} are directly referred to the modulator input. The low-frequency contribution of R_3 is reduced by the series capacitor C_2, whereas the input-referred contribution of R_2 increases above the corner frequency associated with $(R_PC_1)^{-1}$. Its power spectral density can be written as:

$$\overline{v_{n,R_2,\text{in}}^2}(\omega) = 4kTR_2\left(1+\frac{R_{IN}}{R_{DAC}}\right)^2(1+\omega^2R_P^2C_1^2), \tag{1.9}$$

where k is Boltzmann's constant, and T is the absolute temperature.

The fully passive topology has no static bias current and uses highly linear passive elements. However, its loading effects make it difficult to control the pole locations independently. Placing both poles close to DC requires large RC time constants. Since the thermal-noise specification limits the resistor values, the required time constants generally lead to large capacitances. Moving the first pole above the signal bandwidth reduces the required C_1 and keeps the rising contribution of R_2 out of band, but it also weakens the in-band noise shaping. A larger oversampling ratio may then be required to obtain the target SQNR.

The absence of loop-filter gain also means that V_Y is small. Consequently, the comparator must have low input-referred noise and offset, together with a sufficiently short regeneration time to avoid metastability. Increasing the sampling frequency can strengthen the quantization-noise suppression, but further reduces the signal processed by the comparator and increases the clocking requirements. Therefore, the lack of gain and isolation limits the scalability of the fully passive topology for high-resolution operation and motivates the addition of an OTA to realize a passive RC-OTA loop filter.

1.2.2. Passive RC-OTA Loop Filter

Figure 1.4 shows a passive RC-OTA topology. The first stage is a passive low-pass network formed by R_P and C_1, but it is followed by an OTA with transconductance G_m. The OTA output is loaded by R_2, R_3, and C_2. This topology preserves the passive input node while adding gain and reducing the loading between the two filter sections [12].

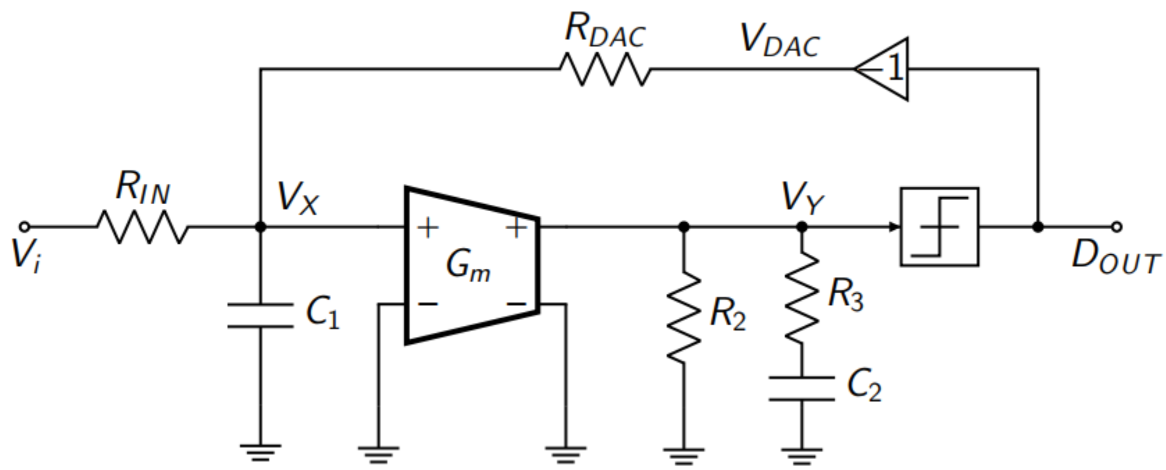


Figure 1.4 CTSDM with a passive RC-OTA loop filter [12].

The corresponding DAC-path transfer function is:

$$H_{DAC}(s) = \frac{V_Y(s)}{V_{DAC}(s)} = \left(\frac{R_{IN}}{R_{IN}+R_{DAC}}\right)\frac{G_m R_2(1+sC_2R_3)}{(1+sR_PC_1)(1+sR_SC_2)} \tag{1.10}$$

The two poles and the zero are therefore $\omega_{p1} = \frac{1}{R_PC_1}$, $\omega_{p2} = \frac{1}{R_SC_2}$, and $\omega_z = \frac{1}{R_3C_2}$.

Unlike the fully passive case, these poles are more clearly defined because the OTA isolates the first RC integrator from the output network. The low-frequency gain is the product of the resistive-divider attenuation and G_mR_2. For $R_{IN} = R_{DAC}$, it is approximately $G_mR_2/2$.

The additional gain increases the comparator-input swing and suppresses the input-referred contribution of comparator noise. It also reduces the probability of metastability. A large effective R_2 allows the required second pole to be obtained with a smaller C_2. The passive input network attenuates the high-frequency shaped quantization error before it reaches V_X. As a result, the OTA has a relatively small input swing, relaxing its linearity requirements and allowing its power consumption to be selected primarily based on its noise requirement [12].

The main thermal-noise sources remain R_{IN}, R_{DAC}, and the OTA. The OTA noise referred to the modulator input is:

$$\overline{v_{n,\mathrm{OTA,in}}^2}(\omega) = \frac{4kT\Gamma_{\mathrm{OTA}}}{G_m}\left(1+\frac{R_{IN}}{R_{DAC}}\right)^2(1+\omega^2 R_P^2 C_1^2), \tag{1.11}$$

where Γ_{OTA} is the OTA excess-noise factor. The input-referred OTA noise begins to increase above approximately $\omega_{n,\mathrm{OTA}} \approx \frac{1}{R_P C_1}$. This frequency is equal to the first loop-filter pole. Therefore, the first noise-shaping pole and the OTA-noise amplification corner cannot be optimized independently. Moving ω_{p1} toward DC improves the in-band suppression of quantization noise, but it also causes the input-referred OTA noise to rise at a lower frequency. If the pole is lowered by increasing C_1, the loop-filter area also increases. On the other hand, placing ω_{p1} above the signal bandwidth keeps the OTA-noise spectrum relatively flat in band and reduces the required C_1, but produces a less effective NTF and may require a larger OSR. This thermal-and-quantization noise trade-off has motivated several approaches, including higher-order passive-active filters [16], resonator loop-filter structures [12], FIR feedback [22], and multi-stage noise-shaping architectures [6].

1.2.3. Previous Passive-Input and Hybrid Sigma-Delta Designs

Fiedler and Hoefflinger reported a second-order fully passive CTSDM for audio applications in 1984 [23]. This work demonstrated that a passive loop filter could realize noise shaping without static amplifier power. However, its attenuation resulted in a small comparator input swing, while comparator noise was not suppressed by any preceding gain. Benabes and Kielbasa subsequently analyzed a fully passive CTSDM using the impulse-invariant transformation [24]. Instead of assuming ideal integrators, the sampled-domain model was derived from the Laplace-domain response of the actual continuous-time loop filter.

A major development was the use of passive RC input stages followed by active gain. A 2010 design used a passive input network to attenuate high-frequency quantization noise before it reached the active stage [25]. This architecture is representative of the passive RC-OTA topology analyzed in Section 1.2.2. Later designs used this concept to increase the loop-filter order by combining passive RC integrators with simple interstage low-gain amplifiers. Figure 1.5 shows a third-order CTSDM, which uses low-gain open-loop amplifiers between passive integrators, thereby reducing both the number of amplifiers and the required amplifier gain [14]. The interstage amplifiers improved the isolation between passive sections and reduced the input-referred comparator noise.

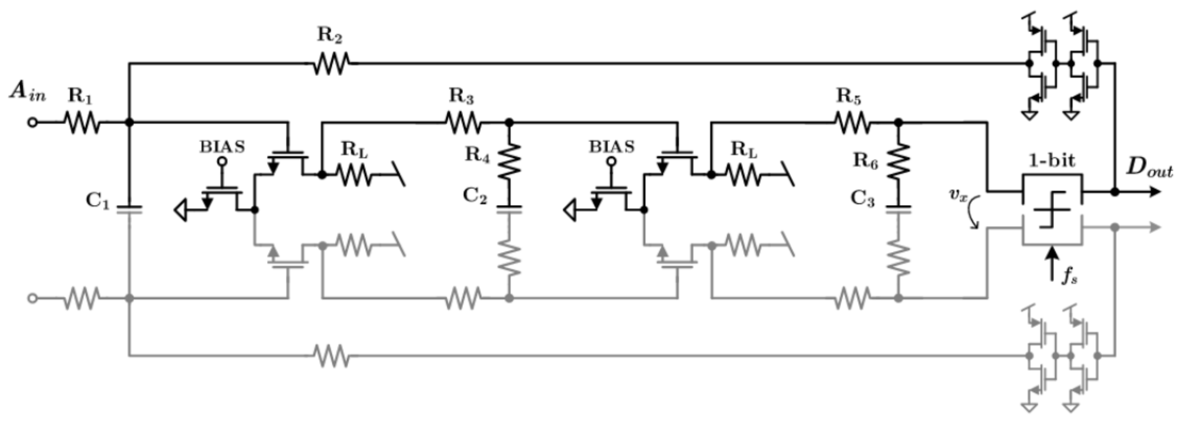


Figure 1.5 3rd order RC-OTA CTSDM [14].

The single-OTA resonator [12] represents another development of the passive RC-OTA concept. A positive-feedback capacitor is connected between the passive input node and the OTA output, as shown in Figure 1.6. This feedback can create complex-conjugate loop-filter poles, so that a resonant peak in the loop-filter response produces a corresponding notch in the NTF. In addition, the resonant pole frequency can be separated from the frequency at which the input-referred OTA noise begins to increase. However, the positive-feedback damping is sensitive to G_m and component spread, and thus tuning may be needed to maintain the intended pole locations across process, supply, and temperature variation [12].

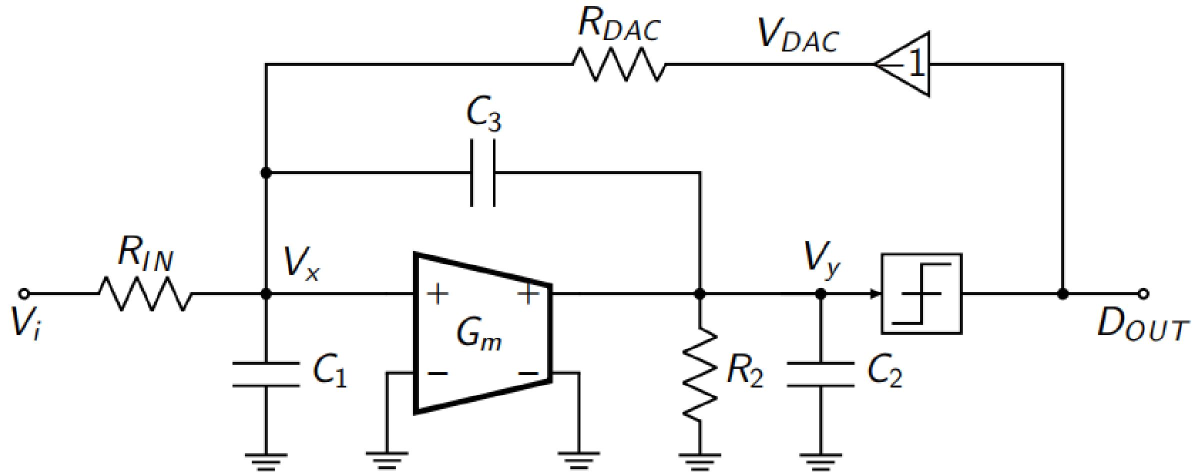


Figure 1.6 Block diagram of the Single-OTA Resonator [12].

Multi-stage noise shaping (MASH) has also been applied to passive-input modulators. Nowacki *et al.* reported a continuous-time 2-1 MASH in which a second-order first stage was cascaded with a first-order second stage [6]. A signal related to the first-stage quantization error was amplified and applied to the second stage, while digital cancellation combined the two outputs. Low-gain stages were used to reduce loading and increase the internal signal swing. The architecture, therefore, obtained third-order noise shaping from two lower-order loops. Still, its cancellation response depended on the analog stage responses, the interstage gain, the quantizer gain, and the digital filter coefficients [6].

Previous work has followed two broad approaches to resolve the thermal-and-quantization noise trade-off introduced in Section 1.2. The first modifies the single-loop transfer function using higher-order, resonant, or FIR techniques. The second adds another SDM stage to suppress or cancel the residual quantization noise. The latter approach leads to the MASH architectures discussed in the following section.

1.3. MASH Architectures for Sigma-Delta Modulators

1.3.1. Operating Principle and Quantization-Noise Cancellation

Increasing the order of a single-loop SDM strengthens the in-band suppression of quantization noise. However, the closed-loop stability, internal voltage swings, coefficient sensitivity, and maximum stable input amplitude become more difficult to control as the loop order increases [11]. A MASH architecture obtains a high overall noise-shaping order by cascading lower-order SDMs. Each feedback loop can therefore be designed with a relatively low order, while the outputs of the stages are combined to cancel the quantization errors introduced by the earlier stages.

Figure 1.7 shows a generic two-stage MASH. The first stage processes the input $U(z)$ and produces the digital output $D_1(z)$. Its quantization error $E_1(z)$ is then applied to the second stage, which produces

$D_2(z)$. The digital filters $H_1(z)$ and $H_2(z)$ combine the two outputs to cancel $E_1(z)$. In this subsection, $H_1(z)$ and $H_2(z)$ denote the digital cancellation filters.

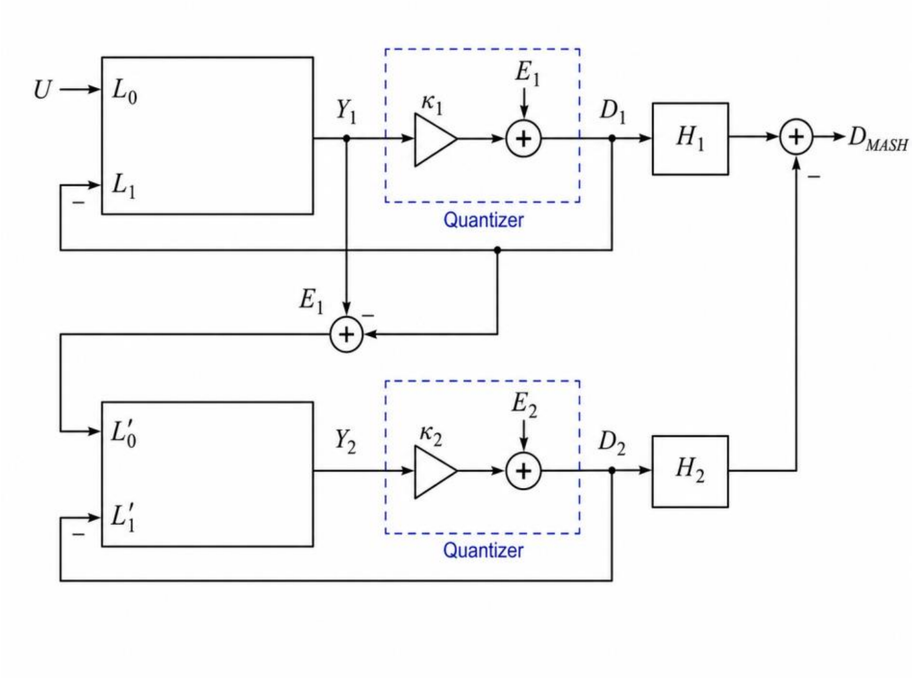


Figure 1.7 Block diagram of two-stage MASH architecture.

$$D_1(z) = \mathrm{STF}_1(z)U(z) + \mathrm{NTF}_1(z)E_1(z). \tag{1.12}$$

The second stage processes the first-stage quantization error, giving:

$$D_2(z) = \mathrm{STF}_2(z)E_1(z) + \mathrm{NTF}_2(z)E_2(z). \tag{1.13}$$

For the output summer convention shown in Figure 1.7, the combined output is

$$D_{\mathrm{MASH}}(z) = H_1(z)D_1(z) - H_2(z)D_2(z). \tag{1.14}$$

Substituting the two stages' outputs gives

$$\begin{gathered} D_{\mathrm{MASH}}(z) = H_1(z)\mathrm{STF}_1(z)U(z) \\ +[H_1(z)\mathrm{NTF}_1(z) - H_2(z)\mathrm{STF}_2(z)]E_1(z) \\ -H_2(z)\mathrm{NTF}_2(z)E_2(z). \end{gathered} \tag{1.15}$$

Equation (1.15) shows that the first-stage quantization error is removed when:

$$H_1(z)\mathrm{NTF}_1(z) = H_2(z)\mathrm{STF}_2(z). \tag{1.16}$$

A simple and commonly used selection that satisfies this condition is:

$$H_1(z) = \mathrm{STF}_2(z), H_2(z) = \mathrm{NTF}_1(z). \tag{1.17}$$

Under ideal cancellation, the output becomes

$$D_{\mathrm{MASH}}(z) = \mathrm{STF}_1(z)\mathrm{STF}_2(z)U(z) - \mathrm{NTF}_1(z)\mathrm{NTF}_2(z)E_2(z). \tag{1.18}$$

The sign of the final quantization-error term depends on the output-summer convention and does not affect its power spectral density. Equation (1.18) shows that E_1 is cancelled, while the remaining error E_2 is shaped by the product of the two NTFs. For example, consider a 2-2 MASH whose two stages have

$$\mathrm{STF}_1(z) = \mathrm{STF}_2(z) = z^{-2}, \mathrm{NTF}_1(z) = \mathrm{NTF}_2(z) = (1 - z^{-1})^2. \tag{1.19}$$

The resulting output is

$$D_{\text{MASH}}(z) = z^{-4}U(z) - (1 - z^{-1})^4 E_2(z). \tag{1.20}$$

Thus, the combined output has fourth-order quantization-noise shaping, even though each internal feedback loop is only second order. System stability is consequently closer to that of two second-order loops than to that of one fourth-order loop. Nevertheless, each constituent SDM must remain stable over its intended input range, and the interstage scaling must prevent the second stage from overloading.

A further advantage is that the first stage continues to define the input range and dominate the input-referred noise, while the later stages process quantization-error-related signals rather than the input signal. With appropriate scaling, the internal ranges of the later stages can therefore be selected independently, while preserving the maximum stable input amplitude of the first stage [11]. The input of the second stage is also noise-like. Consequently, its quantization error is generally less correlated with the original input, thereby reducing tonal behaviour.

1.3.2. Noise Leakage and Passive-Input Implementation Challenges

The high SQNR of a MASH requires perfect matching between $H_2(z)$ and $\text{NTF}_1(z)$. By contrast, moderate coefficient errors in a high-order single-loop SDM will change the realized STF and NTF, but sufficient in-band loop gain will still ensure strong suppression of quantization error. In a MASH, the first-stage error is shaped only by the relatively low-order first-stage NTF and must then be cancelled by a separate path. Small differences between the analog stage responses and the digital cancellation filters can therefore produce a significant residual component [11].

Let the subscript a denote the actual analog transfer functions. The transfer function from the first-stage quantization error to the combined output is

$$T_{E_1}(z) = H_1(z)\text{NTF}_{1,a}(z) - H_2(z)\text{STF}_{2,a}(z). \tag{1.21}$$

Under ideal conditions, $T_{E_1}(z) = 0$. Component mismatch, finite amplifier gain, delay error, or inaccurate digital coefficients make the two terms unequal, allowing E_1 to leak to the output. This leakage can dominate the final spectrum because E_1 is normally larger than E_2 and has only the first-stage noise shaping. An unfiltered or weakly shaped residual can therefore set the practical SQNR, and the required cancellation accuracy becomes increasingly demanding as the target resolution increases [11]. In a CTSDM, the realized NTF and STF also depend on the feedback-DAC pulse shape. These errors are particularly important when the digital coefficients are fixed while the analog RC values and active-stage gains vary across process, supply, and temperature [6].

To illustrate this sensitivity, Figure 1.8 presents a behavioural Monte Carlo simulation of a conventional 2–1 MASH with a nominal SQNR of 115 dB. The model includes a second-order first stage and a first-order second stage and uses an OSR of 256, a normalized sinusoidal input peak amplitude of 0.5, and fixed nominal digital cancellation filters. The standalone first-stage nominal SQNR is 74.1 dB. Independent variations bounded by ±5% were applied to the analog transfer-function coefficients in 1000 cases, while the digital cancellation filters retained their nominal coefficients. The resulting SQNR has a mean of 103.99 dB and a standard deviation of 6.06 dB, corresponding to an average degradation of 11 dB relative to the ideal case. This wide distribution shows that the residual first-stage quantization noise depends strongly on the relative mismatch between the analog and digital cancellation paths. These results support the need for either accurate coefficient matching, calibration, or a MASH architecture with reduced sensitivity to analog–digital transfer-function mismatch.

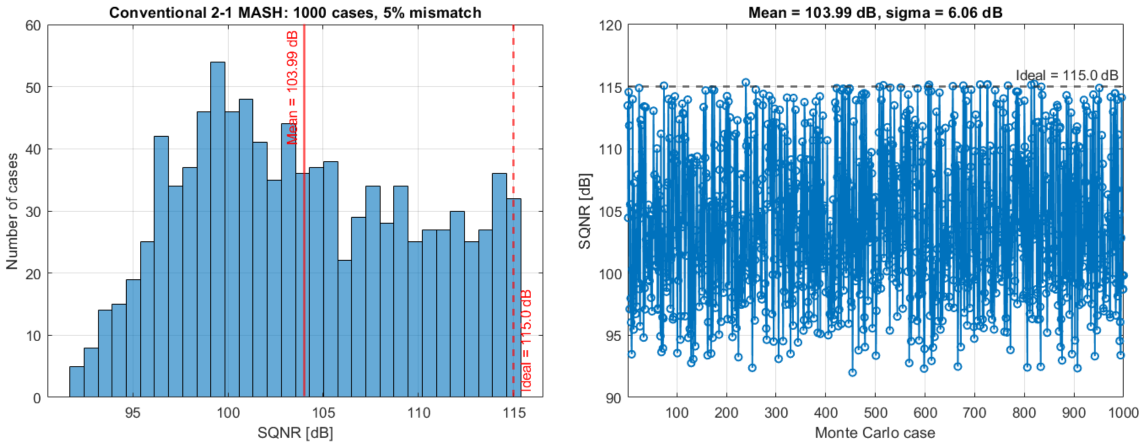


Figure 1.8 Monte Carlo SQNR of a conventional 2–1 MASH under ±5% analog-coefficient mismatch.

Using MASH stages based on passive-input topologies introduces additional difficulties because the equivalent gain of a single-bit quantizer is large and signal-dependent. A passive loop filter produces a small quantizer-input swing, while the quantizer output remains at a full digital level. As discussed in Section 1.1, changes in the input amplitude alter the quantizer-input rms voltage and therefore change the equivalent quantizer gain. Since this gain affects the NTF poles, the analog NTF is not perfectly fixed. A digital cancellation filter derived from a single nominal gain estimate cannot exactly reproduce the analog response across all input amplitudes and operating conditions.

Direct extraction of E_1 is also less straightforward. In an active loop whose equivalent quantizer gain is close to unity, the quantization error can be obtained by subtracting the quantizer input from its output. In a passive loop, however, the comparator input may only be a small fraction of the full digital output. Nowacki showed that this large gain complicates SMASH-like direct-error coupling, as a simple subtraction no longer yields the required first-stage error [6]. A conventional passive-input MASH can instead sense the first comparator-input signal, amplify it, and use digital cancellation to reconstruct the required relationship [6].

Figure 1.9 shows the conventional passive-input continuous-time 2-1 MASH reported by Nowacki. The second-order first stage is followed by the analog interstage gain G_{mid} and the first-order second stage. G_{C1} denotes the equivalent linearized gain of the first-stage comparator. The digital cancellation path compensates for the filtering introduced by the first-stage NTF, the second-stage STF, and the relevant gain and delay terms [6]. In particular, the $\frac{1}{G_{mid}}$ and $\frac{1}{G_{C1}}$ factors compensate for the interstage gain and the first-stage comparator gain, respectively.

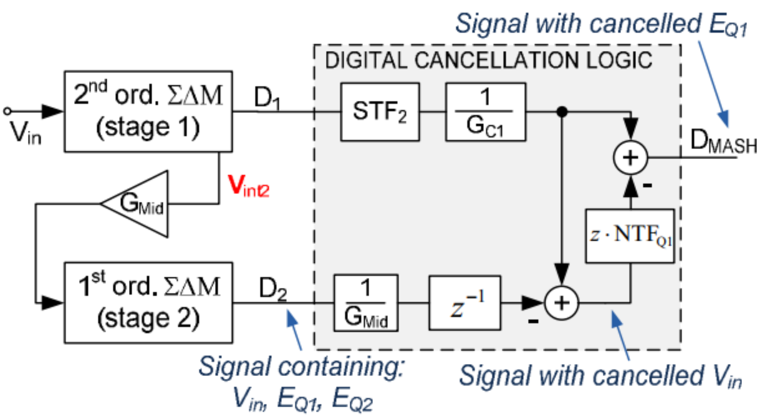


Figure 1.9 Block diagram of Nowacki's passive-input 2-1 MASH architecture [6].

The cancellation path requires several digital coefficients that together define its gain and delay compensation. Depending on the architecture and target resolution, these coefficients may be obtained through analytical estimation, calibration, or mismatch-aware offline optimization. In Nowacki's design, the cancellation logic is simplified by approximating the relevant transfer functions over the signal band and then mapping the resulting coefficients to a compact digital implementation. A genetic-algorithm-based design procedure was then used to obtain an operating point that remained sufficiently insensitive to analog component variation without runtime calibration [6].

1.3.3. Sturdy-MASH (SMASH) Architecture

The sensitivity to cancellation mismatch described in Section 1.3.2 can be reduced by adopting the Sturdy-MASH (SMASH) architecture shown in Figure 1.10. The SMASH architecture differs from the conventional MASH shown in Figure 1.7 in two main ways: the output of the second stage is coupled back into the first-stage loop, and the separate digital noise-cancellation filters are removed [11].

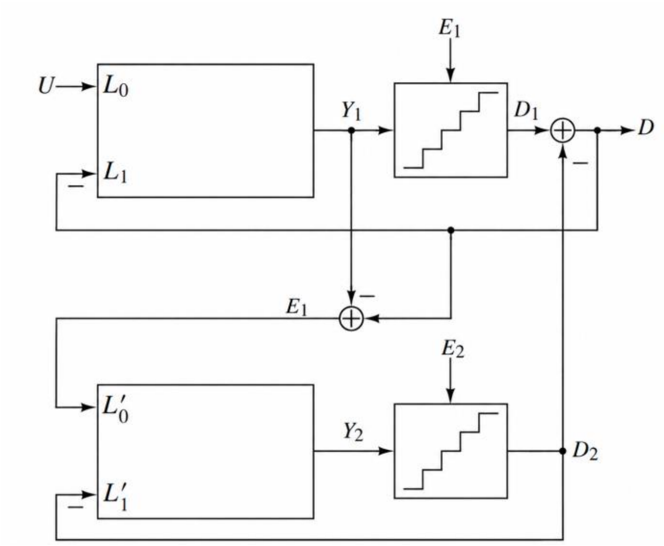


Figure 1.10 Block diagram of a two-stage Sturdy-MASH architecture, adapted from [11].

The output of the modulator is now given by:

$$D = \mathrm{STF}_1 \cdot U - \mathrm{NTF}_1 \cdot \mathrm{NTF}_2 \cdot E_2 + \mathrm{NTF}_1 \cdot (1 - \mathrm{STF}_2) \cdot E_1 \quad (1.22)$$

where E_1 and E_2 denote the first- and second-stage quantization errors. The residual E_1 contribution is proportional to $1 - \mathrm{STF}_2$. Exact cancellation would require $\mathrm{STF}_2 = 1$, corresponding to an unrealizable delay-free second-stage STF, even with ideal circuitry. Instead, [11] proposes $\mathrm{STF}_2 = 1 - \mathrm{NTF}_2$, which gives

$$D = \mathrm{STF}_1 \cdot U - \mathrm{NTF}_1 \cdot \mathrm{NTF}_2 \cdot (E_1 + E_2) \quad (1.23)$$

Thus, the main advantage of the SMASH architecture is that it replaces the highly mismatch-sensitive analog–digital noise cancellation of a conventional MASH with lower-sensitivity noise shaping, while still maintaining the improved stability properties of the MASH scheme [11]. On the other hand, the first-stage quantization error is shaped rather than eliminated, so both E_1 and E_2 contribute to the final output. Furthermore, the required relationship $\mathrm{STF}_2 = 1 - \mathrm{NTF}_2$ must still be realized sufficiently accurately over the signal band, so the architecture is less sensitive, but not insensitive, to circuit nonidealities. In passive-input implementations, the large and signal-dependent comparator gain complicates the direct extraction and coupling of E_1 [6]. These advantages and limitations motivate investigating whether the related dual-loop passive architectures in [13] can achieve high resolution with simpler digital processing and manageable analog complexity.

1.3.4. Thesis Motivation and Research Questions

Section 1.2.3 reviews passive-input and hybrid CTSDM designs that collectively span signal bandwidths from approximately 0.02 to 60 MHz. However, they all achieve less than 80 dB SNDR and less than 180 dB FoM_{SNDR}. The exception is the single-OTA resonator, which achieves 99.2 dB SNDR and 184 dB FoM_{SNDR} over the audio bandwidth. Existing passive-input designs have therefore not yet combined high resolution, dynamic range and efficiency with bandwidths of several hundred kilohertz.

The starting point of this work is the family of dual-loop passive sigma–delta architectures disclosed by van Veldhoven [13]. The patent presents several embodiments with different noise-cancellation approaches, interstage coupling points, and gain implementations. These alternatives were studied to identify the architectural concept offering the most promising basis for a high-resolution implementation in 65 nm CMOS.

An analog-domain noise-cancellation concept was selected because it implements the noise-cancellation filter mainly in the analog path, leaving only a fixed attenuation in the digital path. However, the corresponding circuit implementation disclosed in the patent was not adopted directly. Its fully passive first loop, separate analog cancellation network, and loading between passive sections result in a small comparator-input swing, increased input-referred noise, and considerable implementation complexity. Chapter 2 discusses the operating principle and cancellation conditions in detail and develops two modified circuit-level implementations derived from the initial concept to overcome these limitations.

The resulting implementations are evaluated in terms of first-stage quantization-noise suppression, preservation of the maximum stable input amplitude, power efficiency, and sensitivity to variations in resistors, capacitors, and transconductance. Accordingly, the central research question is:

To what extent can the selected dual-loop passive-input concept disclosed in [13], together with the circuit-level modifications developed in this work, meet the target resolution and energy-efficiency specifications when realised in 65 nm CMOS?

1.4. System-Level Specifications

The proposed modulator is implemented in 65 nm CMOS and operates from a 1.2 V supply. It targets a signal bandwidth of about 200 kHz at a sampling frequency of 100 MHz, corresponding to an OSR of 256. The peak SNDR target exceeds 100 dB. To ensure that the in-band performance is primarily limited by circuit noise rather than quantization noise, the SNR and SQNR targets are set to 103 dB and 115 dB, respectively. A dynamic range above 100 dB and a maximum stable input amplitude of approximately 0.9 V_{ref}, corresponding to 1.08 V_{peak} for a 1.2 V reference, are also targeted. To ensure competitive energy efficiency, a target Schreier figure of merit, FoM_{SNDR}, greater than 181 dB is specified, corresponding to a power-consumption target below 1.55 mW. Table 1.1 compares the target specifications of this work with the reported performance of selected state-of-the-art ADCs operating over similar signal bandwidths [1], [7], [8] and with that of the previously reported passive-input MASH SDM discussed in Section 1.3.2 [6].

Table 1.1 Comparison with selected state-of-the-art noise-shaping ADCs

	Nowacki [6] ISSCC'16	Gao [7] ISSCC'25	Lozada [8] VLSI'24	Yoon [1] VLSI'25	Xing [9] ISSCC'26	Target of this work
Architecture	DT	DT	CT	CT	CT	CT
Tech (nm)	65	55	28	28	28	65
Supply (V)	1	1.2	1.1	1	1	1.2
Power (μW)	1570	307	380	392	400	<1550
F_S (MHz)	1000	20	12.8	80 (coarse), 20 (fine)	50	100
BW (kHz)	10000	156.25	200	250	250	195.3
OSR	50	64	32	160	100	256
SNDR (dB)	72.2	93.3	89	91.2	98.5[a] / 93.9[b]	>100
DR (dB)	77	95	92.1	92.7	99.7	>100
FoM_{SNDR} (dB)	170.2	180.4	176.2	179.2	186.5[a] / 181.9[b]	>181

[a] Measured at f_{in} = 12.3 kHz. [b] Measured at f_{in} = 202.3 kHz.

1.5. Thesis Organization

The remainder of this thesis is organized as follows:

Chapter 2 presents the system-level design of the proposed passive-input MASH architecture. It derives the quantization-noise cancellation equations and evaluates comparator-input and amplifier-output sensing implementations.

Chapter 3 optimizes the noise–power trade-off and maps the required loop-filter transfer functions to circuit-level component values.

Chapter 4 describes the transistor-level implementation in 65 nm CMOS. It presents the two OTAs, the biasing circuits, the comparators, the feedback DACs, the custom TSPC D flip-flop, the clock-generation circuit, and the layout, together with the design considerations and block-level verification of each circuit.

Chapter 5 evaluates the complete modulator through schematic-level and RCC-extracted simulations. It presents the nominal performance, amplitude and frequency sweeps, PVT-corner behavior, Monte Carlo robustness, post-layout results, power breakdown, and idle-tone behavior.

Chapter 6 summarizes the main findings, discusses the limitations of the implemented architecture, and identifies possible directions for future work.

Chapter 2. System-Level Design

This chapter introduces the architecture of the proposed passive-input MASH sigma-delta modulator. The system-level block diagram is presented first, followed by the derivation of the main equations describing the signal path and quantization-noise cancellation. Next, two possible implementations of the proposed architecture are explored. Based on this comparison, the final topology is selected.

2.1. Proposed Architecture

The proposed architecture is shown in Figure 2.1 [13]. It consists of two sigma-delta modulators (SDMs), whose summing nodes and integrators are implemented with passive components. The first SDM consists of a first summing node, the loop filter H_1 and a feedback loop. The second loop digitizes the unshaped quantization noise of the first loop and the scaled input, and subtracts the corresponding quantization-noise contribution from the first loop's output. The C_1 and C_2 blocks shown can be configured as amplifiers, attenuators, and filters to ensure that the shaped noise of the first loop appears at the output of the second loop. Furthermore, C_2 and the second loop's noise transfer function suppress the quantization noise introduced by the second loop. It is important to note that C_1 is implemented in the analog domain, whereas C2 is implemented in the digital domain. This proposed architecture can be seen as a SMASH architecture with a simple digital noise-cancellation filter.

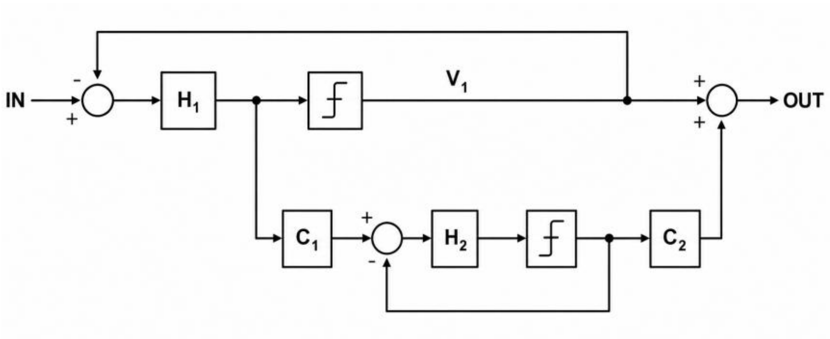


Figure 2.1 The proposed MASH architecture.

Since H_1 and H_2 are implemented using passive low-pass filters, the quantizers must provide the gain required to suppress the quantization error. For analysis, they are linearized by replacing the quantizers with gains (g_1 and g_2) and quantization errors (E_1 and E_2), as shown in Figure 2.2.

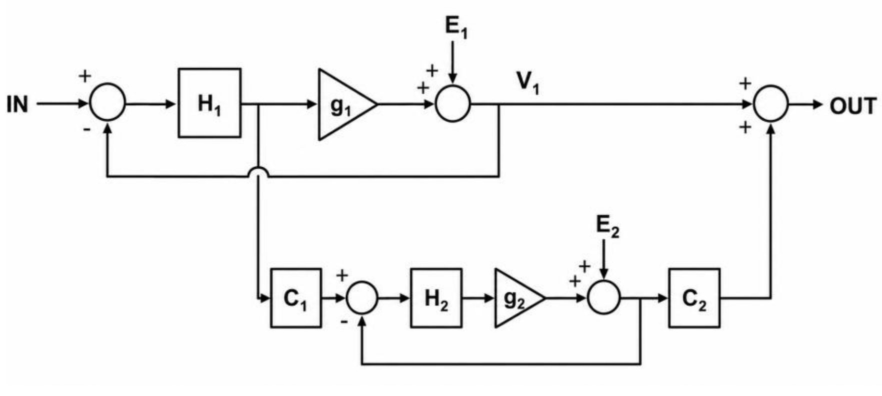


Figure 2.2 The linearized model of the proposed MASH architecture.

From Figure 2.2, the following transfer function can be determined:

$$OUT = IN\left(\frac{H_1g_1}{1+H_1g_1} + \frac{H_2g_2}{1+H_2g_2}\frac{C_1C_2H_1}{1+H_1g_1}\right) + E_1\left(\frac{1}{1+H_1g_1} - \frac{H_2g_2}{1+H_2g_2}\frac{C_1C_2H_1}{1+H_1g_1}\right) + E_2\left(\frac{C_2}{1+H_2g_2}\right) \quad (2.1)$$

Equation (2.1) shows that appropriate values of C_1 and C_2 can attenuate E_2 and cancel E_1, thereby reducing the in-band quantization noise relative to that of the single-loop SDM. To relax digital noise cancellation, C_2 is deliberately chosen as an attenuator with attenuation factor 1/A. Therefore, the cancellation condition becomes:

$$C_1 = \frac{1+H_2g_2}{H_2g_2}\frac{1}{H_1}A \qquad \& \quad C_2 = \frac{1}{A} \quad (2.2)$$

Substituting (2.2) into (2.1) yields (2.3):

$$OUT = IN + E_2\left(\frac{1}{A(1+H_2g_2)}\right) \quad (2.3)$$

Equation (2.3) shows that adding the second stage improves the overall modulator performance relative to the single-loop SDM. The output signal is a relatively unfiltered version of the input, E_1 is cancelled, and E_2 is shaped by the loop filter of the second stage and attenuated by $C_2 = \frac{1}{A}$. Assuming that the 2nd modulator's STF is unity, the cancellation condition in (2.2) simplifies to $C_1 \approx \frac{A}{H_1}$. Therefore, the cancellation requirement changes from analog–digital matching to analog–analog matching between C_1 and $1/H_1$. Since both responses are implemented on the same chip, they can track more closely, although mismatches and loading still limit cancellation accuracy [13].

Figure 2.3 shows the circuit-level implementation of the architecture proposed in [13]. Both SDMs are implemented with fully passive loop filters. The block C_1 is realized by amplifier A, resistors R_5, R_9, R_{10}, and R_{11}, and capacitors C_5, C_6, and C_7 [13]. The R_5–C_5 branch realizes one of the zeros of $C_1(s)$, while C_7 realizes the second. Resistor R_{11} limits the high-frequency increase in the STF, thereby preventing excessive input swing and overload in the second SDM [13].

As discussed in Chapter 1, the fully passive first-loop filter is a second-order low-pass network with two real poles and one high-frequency zero; its exact transfer function is given by Equation (1.8). In pole–zero form, $H_1(s)$ can be written as

$$H_1(s) = H_1(0)\frac{1+s/\omega_z}{(1+s/\omega_{p1})(1+s/\omega_{p2})}.$$

Where $H_1(0)$ is the DC gain, ω_{p1} and ω_{p2} are the two pole frequencies, and ω_z is the high-frequency zero frequency.

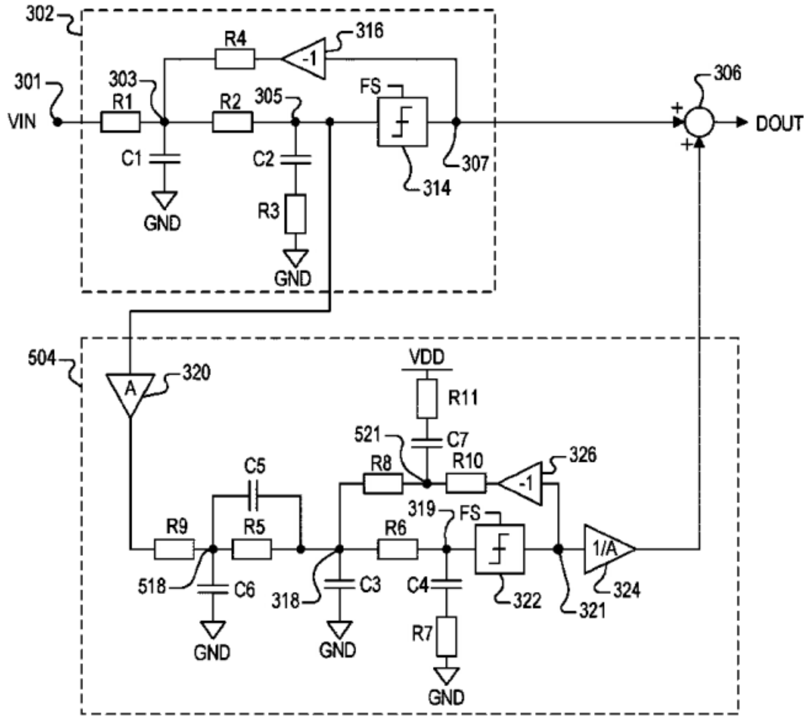


Figure 2.3 Block diagram of the MASH architecture proposed in [13].

For good quantization noise suppression, the two pole frequencies should be placed sufficiently below the upper edge of the signal band so that the first-loop response exhibits an approximately second-order roll-off of −40 dB/dec outside the signal band. Together with the feedback loop and the equivalent quantizer gain, this two-pole response provides the desired second-order quantization-noise shaping in the first SDM.

Since $C_2 = 1/A$, the cancellation condition in Equation (2.2) requires the combined response $C_1(s)C_2(s)$ to approximate the inverse of $H_1(s)$:

$$C_1(s)C_2(s) = \frac{C_1(s)}{A} \approx \frac{1}{H_1(s)} = \frac{1}{H_1(0)}\frac{\left(1 + s/\omega_{p1}\right)\left(1 + s/\omega_{p2}\right)}{1 + s/\omega_z}.$$

Consequently, the cancellation response must contain two zeros at the two first-loop pole frequencies. It should also contain a high-frequency pole at the zero frequency of $H_1(s)$. To illustrate the required cancellation response, Figure 2.4 assumes a signal bandwidth of 200 kHz, pole frequencies of 10 kHz and 20 kHz, and a high-frequency zero at $f_s/1.5$ = 66.7 MHz. These values are illustrative; the important point is that both poles lie within the signal band, whereas the zero lies far above it. The high-frequency zero of $H_1(s)$ at $f_s/1.5$ lies outside the plotted frequency range. For clarity, the magnitude responses in Figure 2.4 are normalized to $H_1(0) = 1$.

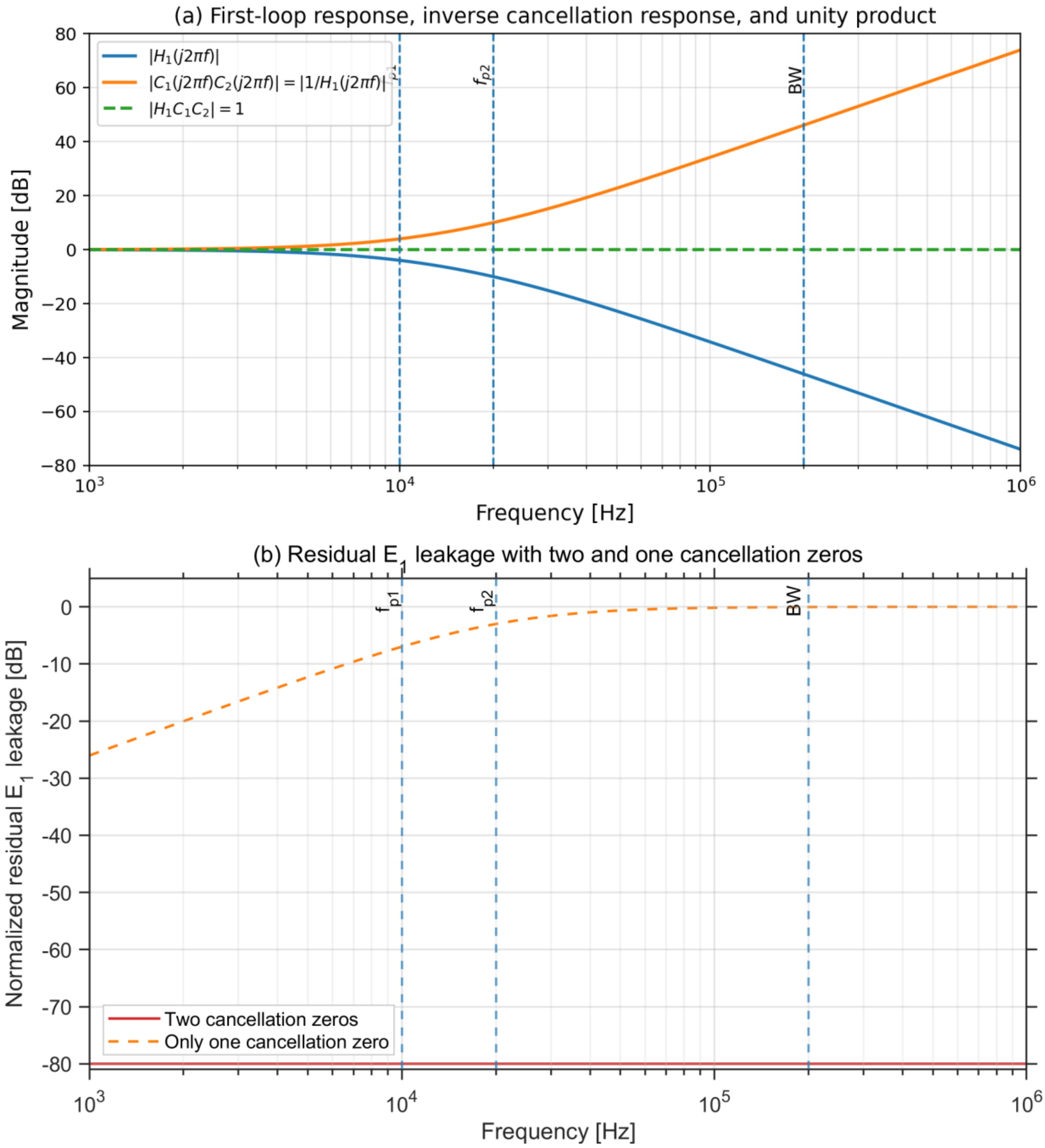


Figure 2.4 Cancellation of a second-order first-loop response: (a) $H_1(s)$, its inverse response $C_1(s)C_2(s)$, and their ideal unity product; (b) normalized residual E1 leakage for two-zero and one-zero cancellation responses.

Over the signal band, ideal matching causes the second path to generate an E_1 contribution equal in magnitude and opposite in sign to the corresponding contribution in the first path, resulting in complete cancellation of the first-stage quantization noise at the MASH output. Figure 2.4(b) shows the magnitude of the normalized residual cancellation error relative to the uncanceled E_1 contribution in the first path. With two correctly placed cancellation zeros, the residual leakage is ideally zero; therefore, the corresponding curve is displayed at the selected −80 dB plotting floor. When only one cancellation zero is present, one pole of $H_1(s)$ remains uncompensated. Consequently, the residual E_1 leakage increases with frequency and approaches 0 dB at frequencies well above the remaining pole. Similarly, a mismatch between the pole frequencies of $H_1(s)$ and the zero frequencies of $C_1(s)$ results in incomplete cancellation and residual E_1 leakage.

As discussed in Chapter 1, conventional MASH SDMs implement the noise-cancellation filtering in the digital domain and suffer from a mismatch between the analog and digital NTFs. Because the quantizer gain, and therefore the NTF, is signal-dependent, the required digital cancellation filter is complex and can only be approximated. Therefore, the noise-cancellation logic for a passive MASH typically requires a complex and power-hungry calibration circuit. In contrast, this architecture implements most of the noise-cancellation filtering in the analog domain and requires only a digital attenuator, which can be implemented using a simple shift register.

However, the implementation shown in Figure 2.3 has two main limitations. First, the first loop uses a fully passive loop filter. As discussed in Chapter 1, passive loop filters increase the input-referred noise contributions from the quantizer and resistor R_2. Furthermore, the voltage swing at the quantizer input is reduced, which complicates the quantizer's circuit-level implementation. In addition, the loading effects between passive components introduce complex design trade-offs. Second, loading between the C_1 and H_2 networks forms a coupled fifth-order second loop, making it difficult to satisfy the cancellation condition in Equation (2.2) while maintaining sufficient suppression of E_2. Therefore, a modified version of this architecture is presented in the next section.

2.2. Possible Implementations of the Proposed Architecture

The limitations discussed in the previous section motivate two circuit-level modifications that simplify the architecture described in [13], while preserving the MASH input–output relationship. First, the main gain associated with C_1 is moved into the first-loop filter H_1, yielding an RC–OTA first loop that addresses the limitations of the fully passive loop filter, as discussed in Section 1.2. Second, the required cancellation response is realized through STF_2, avoiding a separate passive C_1 network between the two loops. The resulting comparator-input and amplifier-output sensing architectures are examined in Sections 2.2.1 and 2.2.2, respectively.

2.2.1. First Implementation: Comparator-Input Sensing Architecture

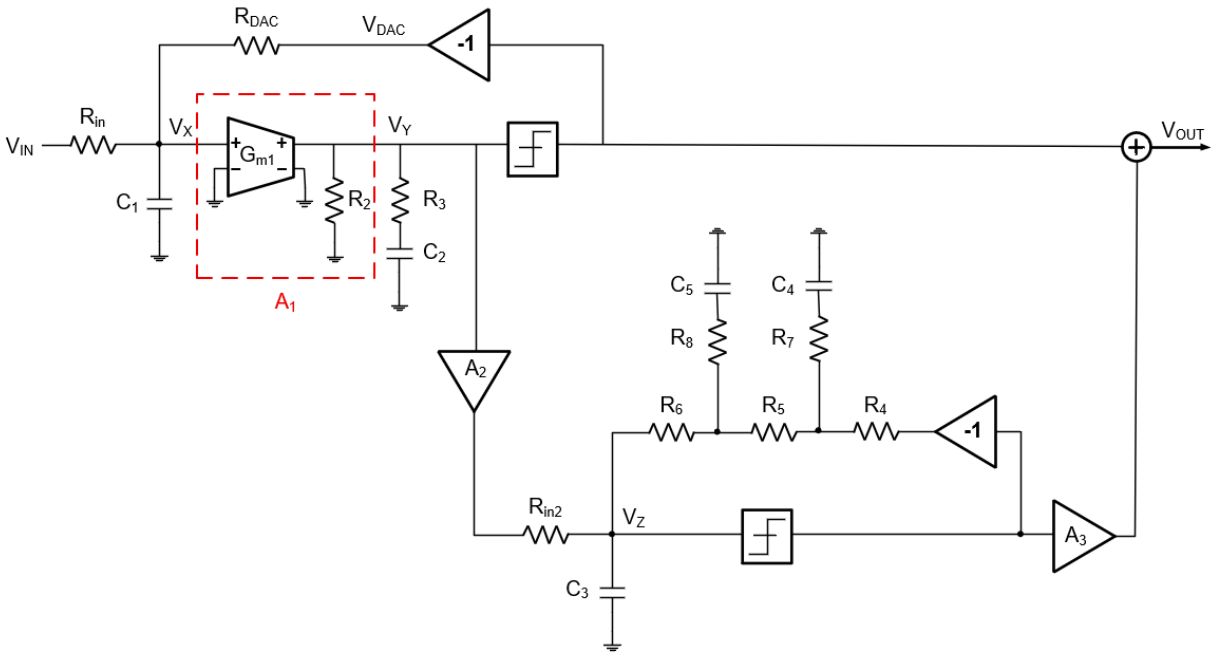


Figure 2.5 Block diagram of comparator-input sensing architecture.

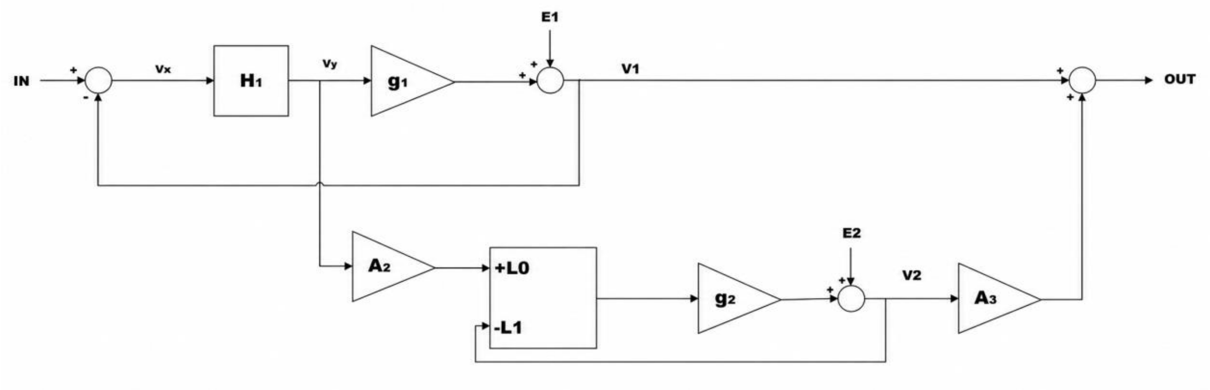


Figure 2.6 System-level model of comparator-input sensing architecture.

Figure 2.5 shows the block diagram of the modified architecture, in which the amplifier A1 is moved into the first SDM loop, and the C_1 filter is combined with the second SDM loop. Figure 2.6 shows the linearized model of the second SDM loop. In this model, the input and DAC transfer functions are denoted by L_0 and L_1, respectively. H_1 denotes the transfer function of the first RC-OTA SDM and includes the gain A_1 of the first OTA, highlighted in Figure 2.5. An additional amplifier A_2 is inserted to relax the second-loop comparator's noise requirement and reduce the probability of metastability in the second-loop comparator (Q_2). Furthermore, A_3 is implemented in the digital domain, and it corresponds to C_2 shown in Figure 2.1.

The topology can first be understood intuitively before proceeding with the mathematical derivation. To cancel the first-loop quantization noise at the final output, its shaped component must propagate through the two paths with equal magnitudes and opposite signs. At the input of the first-loop comparator (Q_1), the shaped quantization noise E_1 is further attenuated by H_1, which has two low-frequency poles. Accordingly, STF_2 must introduce two zeros at the same frequencies. The shaped noise is also amplified by A_1A_2 before reaching the input of the second SDM. Digital attenuation is therefore required so that its contribution at the output of the second path matches the corresponding first-path contribution in magnitude. Furthermore, a digital delay is required at the output of SDM_1 to match the delay of SDM_2.

From Figure 2.6, the following transfer functions can be determined:

$$STF_1 = \frac{H_1 g_1}{1+H_1 g_1} \quad \& \quad NTF_1 = \frac{1}{1+H_1 g_1}$$

$$STF_2 = \frac{g_2 L_0}{1+g_2 L_1} \approx \frac{L_0}{L_1} \quad \& \quad NTF_2 = \frac{1}{1+g_2 L_1}$$

$$OUT = IN(STF_1 + A_2 A_3 H_1\, NTF_1\, STF_2) + E_1(NTF_1 - A_2 A_3 H_1\, NTF_1\, STF_2) + E_2(A_3\, NTF_2) \tag{2.4}$$

Equation (2.4) shows that STF_2 and the amplifier gains (A_1, A_2, and A_3) must be selected to attenuate the E_2 contribution and suppress E_1, thereby reducing the in-band quantization noise relative to that of the single-loop SDM. The required condition is obtained with the following choice:

$$STF_2 = \frac{1}{A_2 A_3 H_1(s)} \tag{2.5}$$

Substituting (2.5) into (2.4) yields (2.6):

$$OUT = IN + E_2\left(\frac{A_3}{1+g_2 L_1}\right) \tag{2.6}$$

This condition is satisfied by the following choices:

$$\frac{L_1(s)}{L_0(s)} = H_1(s) \qquad \& \quad A_3 = \frac{1}{A_2 H_1(0)} \frac{L_1(0)}{L_0(0)} = \frac{2}{A_1 A_2} \tag{2.7}$$

Equation (2.6) shows that the input signal appears unfiltered at the output. At the same time, the quantization noise of the first loop is cancelled, and the quantization noise of the second loop is shaped by the second loop filter and attenuated by a factor of $\frac{A_1 A_2}{2}$.

It should be noted that $L_0(s)$ and $L_1(s)$ have the same poles, so these common poles cancel in the ratio $\frac{L_1(s)}{L_0(s)}$ and do not affect the cancellation condition given in Equation (2.7). To cancel the first-loop quantization noise, the zeros of $L_1(s)$ should be shifted to higher frequencies, while the zeros of $L_0(s)$, the input transfer function, should be placed at the frequencies of the first-loop poles. Furthermore, a digital attenuation factor $A_3 = \frac{2}{A_1 A_2}$ is required. To simplify the digital logic, A_3 can be implemented using a shift register that realizes an attenuation factor of $\frac{1}{2^n}$.

The next step is to select an SDM_2 topology that satisfies these cancellation requirements. Figure 2.7 shows the chosen architecture. It places a low-pass filter in the feedback path, thereby producing a high-pass response in the SDM's STF. R_7 and R_8 are added to introduce two zeros, supporting the stability of the second SDM. The circuit is designed to provide three low-frequency poles for good noise shaping, two low-frequency zeros in $L_0(s) = \frac{V_z(s)}{V_{in}(s)}$, and two well-defined zeros in $L_1(s) = \frac{V_z(s)}{V_{DAC}(s)}$ that can be shifted to higher frequencies. On the other hand, the loading effects complicate the analysis of this simple circuit. Therefore, Section 2.2.2 introduces a simpler architecture.

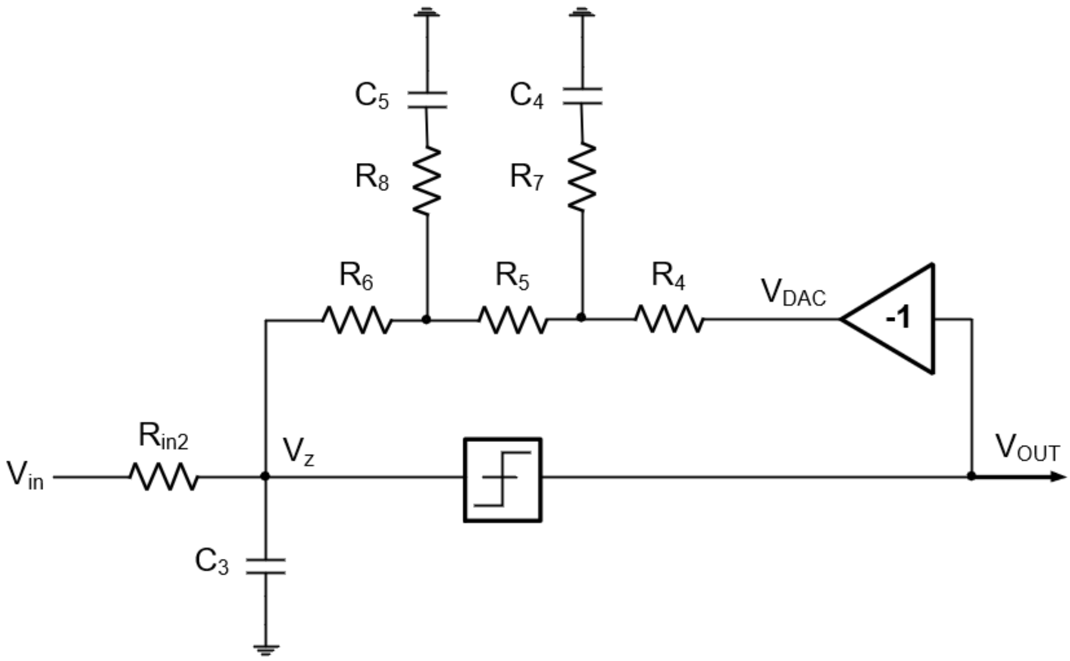


Figure 2.7 Circuit-level model of the second SDM loop.

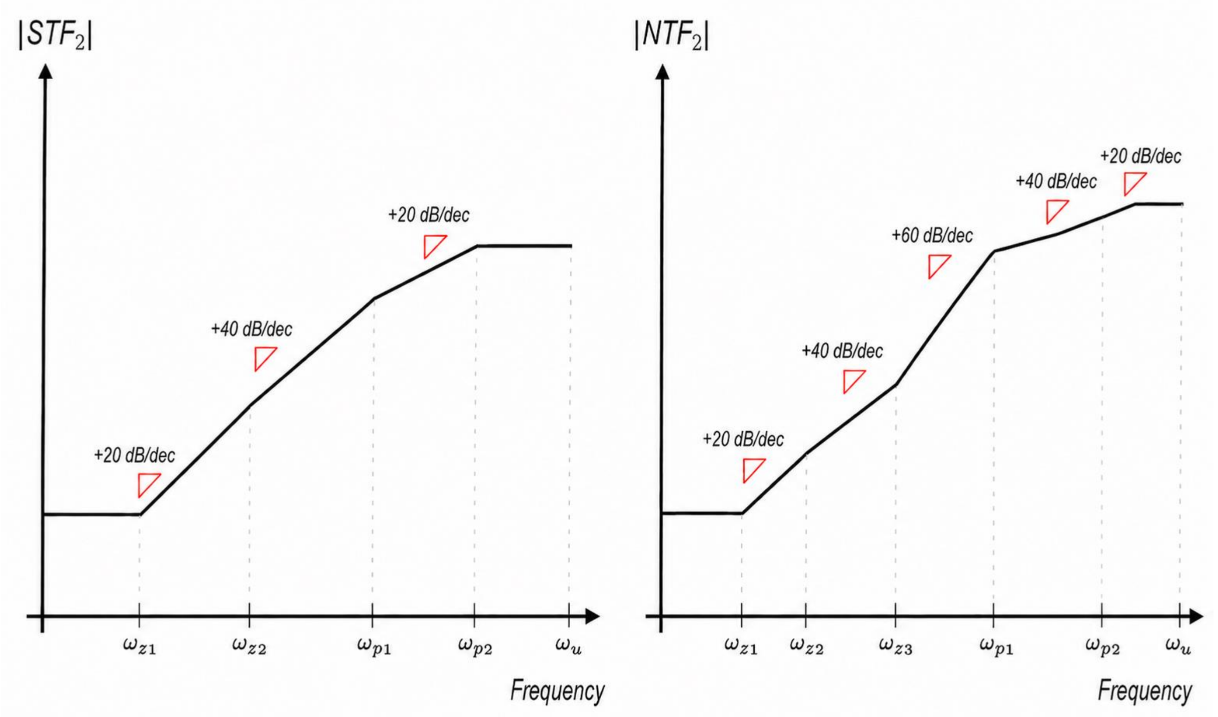
As mentioned above, the exact analysis of this circuit is complex. However, simplified equations can be derived by assuming $R_4 = R_5 = R_6 = R$ and $R_{in2} = 3R$, thereby making the input and DAC resistances equal. The additional assumptions $R \gg R_7$ and $R \gg R_8$ are adopted to place the poles of $L_1(s)$ at low frequencies and the zeros at high frequencies. Under these assumptions, the following transfer functions can be derived:

$$L_0(s) = \frac{V_z(s)}{V_{in}(s)} = \frac{0.5[\left(\frac{1}{3}C_4C_5R^2\right)s^2 + (\frac{2}{3}(C_4 + C_5)R)s + 1]}{(0.5C_3C_4C_5R^3)s^3 + \left(C_3C_4 + C_3C_5 + \frac{2}{3}C_4C_5\right)R^2s^2 + \left(\frac{3}{2}C_3 + \frac{2.5}{3}C_4 + \frac{4}{3_4}C_5\right)Rs + 1} \tag{2.8}$$

$$L_1(s) = \frac{V_z(s)}{V_{DAC}(s)} = \frac{0.5\ [(C_4C_5R_7R_8)s^2 + (C_4R_7 + C_5R_8)s + 1]}{(0.5C_3C_4C_5R^3)s^3 + \left(C_3C_4 + C_3C_5 + \frac{2}{3}C_4C_5\right)R^2s^2 + \left(\frac{3}{2}C_3 + \frac{2.5}{3}C_4 + \frac{4}{3_4}C_5\right)Rs + 1} \tag{2.9}$$

$$\frac{L_1(s)}{L_0(s)} = \frac{(C_4C_5R_7R_8)s^2 + (C_4R_7 + C_5R_8)s + 1}{\left(\frac{1}{3}C_4C_5R^2\right)s^2 + (\frac{2}{3}(C_4 + C_5)R)s + 1} \tag{2.10}$$

Figure 2.8 shows the representative asymptotic magnitude responses of STF_2 and NTF_2 for the comparator-input sensing architecture. Because the second-loop input is taken from the Q_1 input, the sensed E_1 component includes the two in-band poles of $H_1(s)$. The cancellation condition, therefore, requires STF_2 to introduce two in-band zeros at the corresponding pole frequencies. The three poles of $L_1(s)$ appear as the three zeros of NTF_2, whereas the two zeros of $L_1(s)$ appear as the poles of NTF_2. Consequently, the NTF_2 slope increases successively across its three zeros and is then reduced by the two higher-frequency poles.



(a) Representative bode plot of **STF**$_2$ (b) Representative bode plot of **NTF**$_2$

Figure 2.8 Representative asymptotic Bode plots of STF_2 and NTF_2 for the comparator-input sensing architecture.

Equations (2.8) and (2.9) show that increasing R, C_3, or C_4 shifts the poles and zeros of $L_0(s)$ to lower frequencies. On the other hand, the zeros of $L_1(s)$ can be shifted to higher frequencies by decreasing R_7 and R_8. To approximate $H_1(s) = \frac{L_1(s)}{L_0(s)}$ over the desired bandwidth, R, C_3, and C_4 must be optimized so that the zeros of $L_0(s)$ align with the corresponding pole frequencies of $H_1(s)$. This adjustment also shifts the poles of the second-loop NTF to lower frequencies, thereby increasing suppression of the second-loop quantization noise. R_7 and R_8 can then be optimized independently to shift the zeros of $L_1(s)$ to higher frequencies; this adjustment also improves the second-loop noise-shaping response.

As shown in Equation (2.5), $H_1(s)$ should equal $\frac{1}{A_2A_3}\frac{L_1(s)}{L_0(s)}$ within the desired bandwidth to cancel the quantization noise of the first loop (E_1) at the MASH output. If $H_1(s)$ and $\frac{1}{A_2A_3}\frac{L_1(s)}{L_0(s)}$ do not match, part of E_1 leaks to the MASH output. This leaked component then combines with the quantization noise of the second loop (E_2), which is suppressed by the NTF of the second SDM. Exact cancellation is difficult because $H_1(s)$ has one zero, whereas $\frac{L_1(s)}{L_0(s)}$ has two, and loading effects complicate the alignment of the poles of $\frac{L_1(s)}{L_0(s)}$ with those of $H_1(s)$. Even without exact cancellation, the first-loop quantization noise can be suppressed sufficiently to increase the MASH SQNR by more than 25 dB relative to that of the first SDM. The remainder of this section evaluates the robustness of the cancellation to component mismatches and presents a design example that explains this behaviour.

Table 2.1 Component Values of comparator-input sensing architecture shown in Figure 2.5

Component name	Numerical value
R_{IN} & R_{DAC}	3.5 kΩ
R_2	58 kΩ
R_3	350 Ω
R_4&R_5&R_6	108 kΩ
R_{in2}	324 kΩ
A_1	116
A_2	8.83
A_3	1/512
C_1	250 pF
C_2	50 pF
C_3	5 pF
C_4	27 pF
C_5	43 pF

Figure 2.9 shows the Bode plots of the two terms in Equation (2.5) that must be equal to cancel the E_1 leakage completely within the desired bandwidth, for the design whose component values are listed in Table 2.1. Furthermore, Figure 2.10 shows the first-SDM NTF (blue), the second-loop E_2-to-output NTF (black), and the E_1-leakage transfer function at the MASH output (red) within the desired bandwidth.

As shown in Figure 2.9, the two terms are not exactly matched. The difference between the two responses decreases to zero at their crossing frequency and then increases towards the upper edge of the bandwidth. Figure 2.10 shows that the E_1-leakage transfer magnitude is approximately −97 dB at the lower band edge, decreases to a notch where the two terms in Figure 2.9 match, and then increases towards the upper band edge. This produces a notch in the E_1-leakage transfer function. If PVT variation or component mismatch alters either transfer-function term shown in Figure 2.9, the notch frequency is expected to shift. However, the overall suppression over the desired bandwidth remains robust. The simulations in Section 2.2.2 further verify this behaviour.

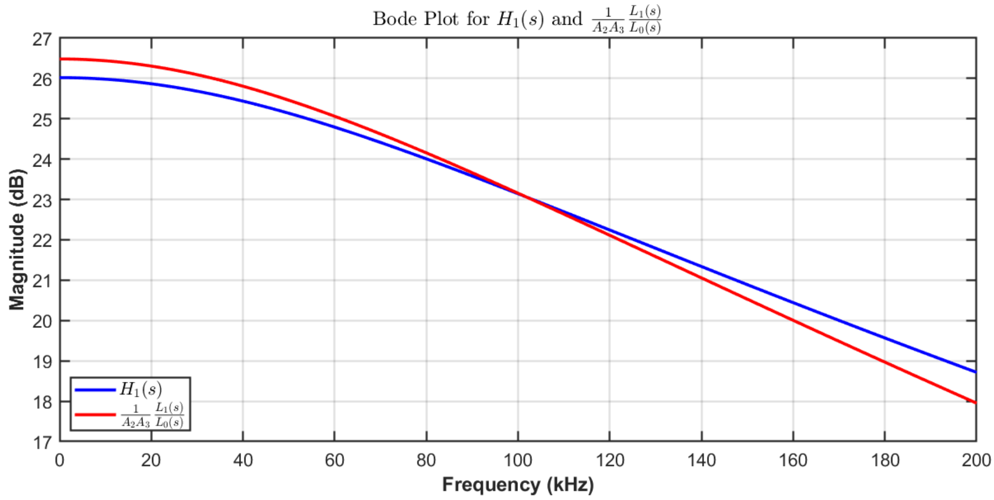


Figure 2.9 Bode plot for $H_1(s)$ and $\frac{1}{A_2A_3}\frac{L_1(s)}{L_0(s)}$ of the realized design.

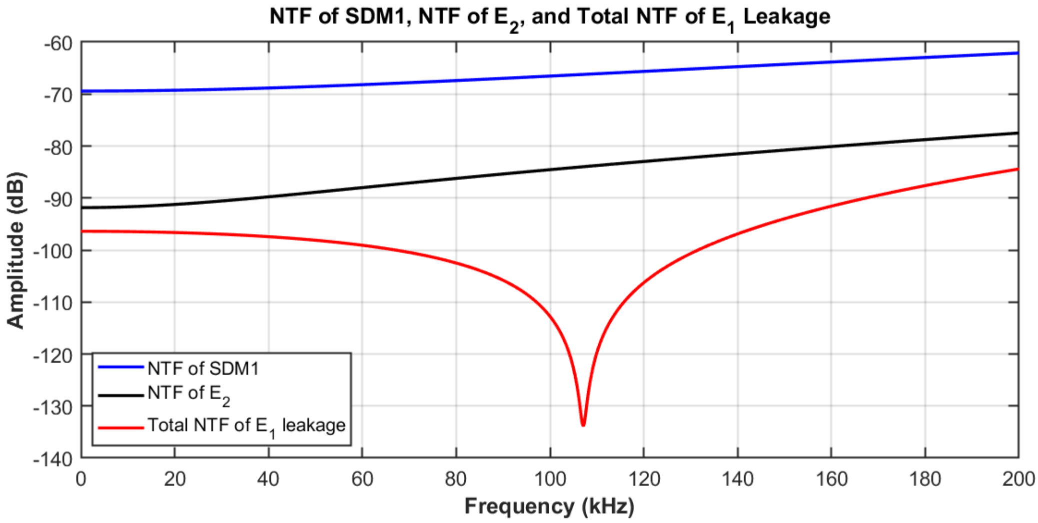


Figure 2.10 Bode plots of the SDM1-output NTF, the E_1-to-MASH-output NTF, and the E_2-to-MASH-output NTF.

However, this architecture has two major disadvantages. First, analysis of the second-SDM loop filter remains complex even under the assumptions introduced earlier. The loop-filter design requires iterative optimization in Simulink to determine the values of R, C_3, and C_4 that maximize SQNR. Furthermore, the architecture requires an additional amplifier A_2 before the second SDM. Therefore, maintaining a simple digital circuit requires accurate matching to the analog gain A_1A_2. Section 2.2.2 presents an alternative architecture that addresses these two limitations.

2.2.2. Second Implementation: Amplifier-Output Sensing Architecture

The two limitations of the previous implementation can be addressed by adding an additional resistor R_3 between the amplifier output and the Q_1 input, as shown in Figure 2.11. R_3 provides resistive isolation, allowing the amplifier output V_{x2} to be sensed before the signal encounters the additional in-band pole at V_y. Accordingly, the input to the second SDM is an amplified 1st-order noise-shaped quantization error. The second-loop STF therefore requires only one zero at the same frequency as this pole. A low-pass network in the second-loop feedback path provides this zero while simplifying the feedback network. The additional amplifier A_2 shown in Figure 2.5 can then be moved inside the second-SDM loop. This placement reduces passive loading and creates a well-defined pole–zero pair at the comparator input. The shaped E_1 component is then amplified by A_1 before reaching the second SDM, so the required digital attenuation only needs to match A_1.

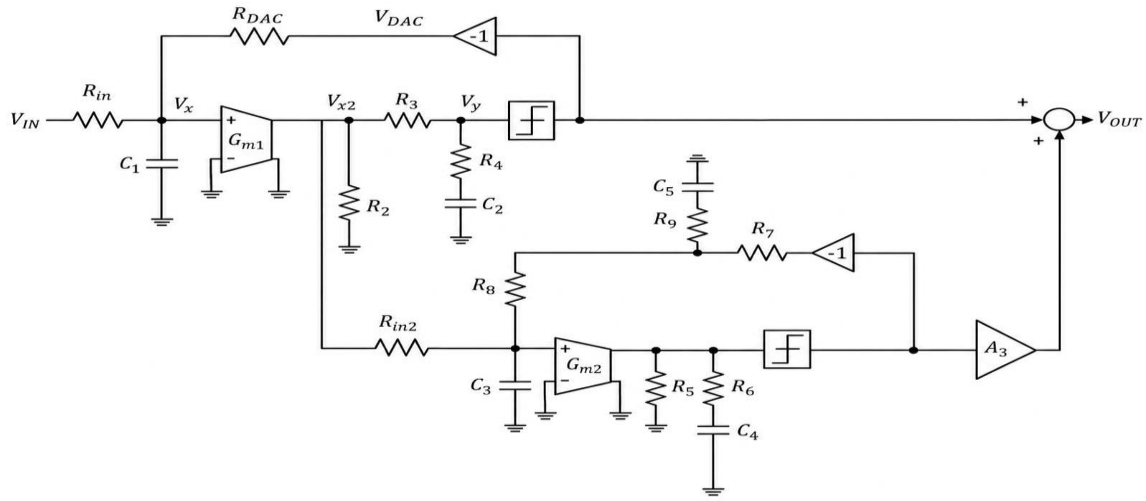


Figure 2.11 Block diagram of amplifier-output sensing architecture.

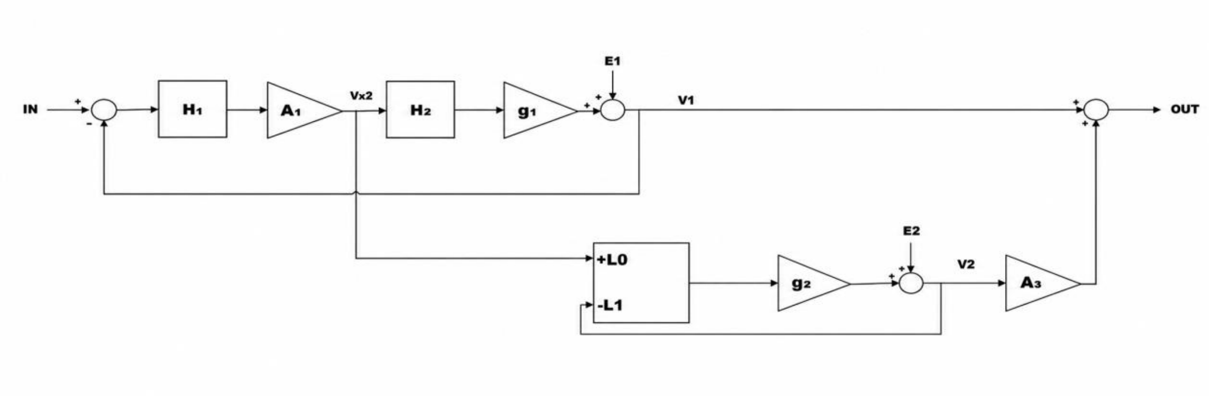


Figure 2.12 System-level model of amplifier-output sensing architecture.

Figure 2.12 shows the system-level model of the architecture, including H1 and H2, while the corresponding circuit-level implementation is shown in Figure 2.11. H_1 is the transfer function $\frac{V_x}{V_{in}}$, which has one pole at $\omega_{p1} = \frac{1}{(R_{in} \parallel R_{DAC})C_1}$. H_2 is the transfer function $\frac{V_y}{V_{x2}}$, which has the extra pole and zero associated with the first SDM. It should be noted that the input to the second loop is now derived from the amplifier's output, which has a high voltage swing. Although increasing A_1 would provide stronger attenuation of the second-loop quantization noise, as discussed below, it would also increase the swing at V_{x2} and, consequently, impose a more stringent linearity requirement on the G_{m1} stage.

From Figure 2.12, the following transfer function can be derived:

$$STF_1 = \frac{H_1 H_2 A_1 g_1}{1 + H_1 H_2 A_1 g_1} \quad \& \quad NTF_1 = \frac{1}{1 + H_1 H_2 A_1 g_1}$$

$$STF_2 = \frac{g_2 L_0}{1 + g_2 L_1} \approx \frac{L_0}{L_1} \quad \& \quad NTF_2 = \frac{1}{1 + g_2 L_1}$$

$$OUT = IN(STF_1 + A_1A_3H_1\ NTF_1\ STF_2) + E_1(NTF_1 - A_1A_3H_1\ NTF_1\ STF_2) + E_2(A_3\ NTF_2) \quad (2.11)$$

Equation (2.11) shows that E_2 is further attenuated by A_3. Furthermore, if STF_2 and the gains A_1 and A_3 are selected properly, E_1 can be cancelled, thereby reducing the in-band quantization noise relative to that of the single-loop SDM. The E_1-cancellation condition is obtained by choosing:

$$STF_2 = \frac{1}{A_1A_3H_1(s)} \quad (2.12)$$

Substituting (2.12) into (2.11) yields (2.13):

$$OUT = IN + E_2(\frac{A_3}{1+g_2L_1}) \quad (2.13)$$

This can be achieved easily if we choose:

$$\frac{L_1(s)}{L_0(s)} = H_1(s) \qquad \& \quad A_3 = \frac{1}{A_1H_1(0)}\frac{L_1(0)}{L_0(0)} = \frac{2}{A_1} \quad (2.14)$$

Equation (2.13) shows that the input signal appears unfiltered at the output. At the same time, the quantization noise of the first loop is cancelled, and the quantization noise of the second loop is shaped by the second loop filter and attenuated by a factor of $\frac{A_1}{2}$. Because A_1 is constrained by the allowable output swing of the G_{m1} stage, the E_2 contribution receives less digital attenuation than in the comparator-input sensing architecture. However, as discussed later in this section, the second SDM loop in the amplifier-output sensing architecture has a well-defined 3rd pole that can be placed at a low frequency, resulting in better NTF than the comparator-input sensing architecture.

The remaining design step is to select a second-SDM loop that satisfies the cancellation condition in Equation (2.14). Figure 2.13 shows the chosen architecture for the second SDM loop. The feedback low-pass filter produces a high-pass response in the SDM STF. The transfer function $\frac{V_y(s)}{V_x(s)}$ introduces the same pole–zero pair into $L_0(s)$ and $L_1(s)$, allowing their locations to be optimized to increase suppression of the E_2 contribution.

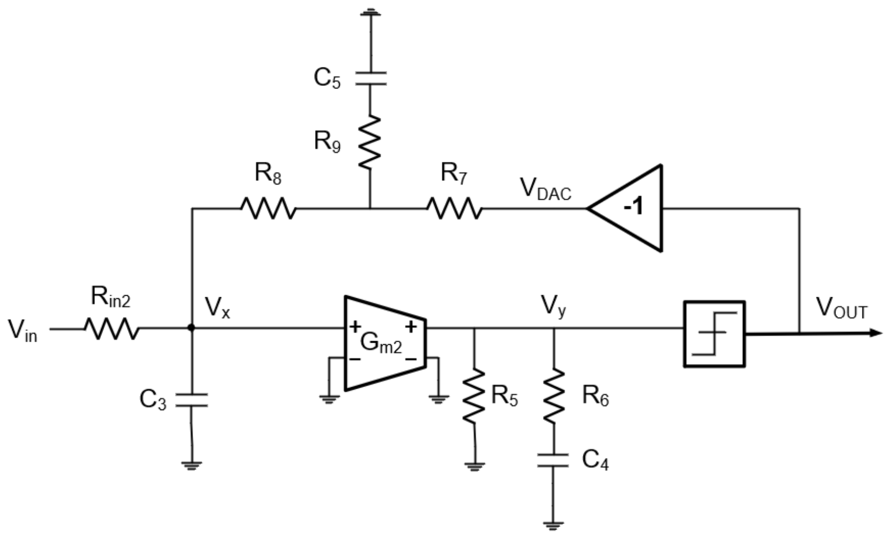


Figure 2.13 Circuit-level model of the second SDM loop.

For simplicity, assume that $R_7 = R_8 = R$ and $R_{in2} = 2R$, so that the input and DAC resistances are equal. The additional assumption $R \gg R_9$ places the pole of $L_1(s)$ at a low frequency and its zero at a high frequency. Under these assumptions, the following transfer functions can be derived:

$$L_0(s) = \frac{V_y(s)}{V_{in}(s)} = \frac{0.5[\,(0.5C_5R)\,s + 1]}{(0.5C_3C_5R^2)s^2 + (C_3 + 0.75C_5)R\,s + 1} * \frac{C_4R_6\,s + 1}{C_4(R_5 + R_6)\,s + 1} \tag{2.15}$$

$$L_1(s) = \frac{V_y(s)}{V_{DAC}(s)} = \frac{0.5(C_5R_9\,s + 1)}{(0.5C_3C_5R^2)s^2 + (C_3 + 0.75C_5)R\,s + 1} * \frac{C_4R_6\,s + 1}{C_4(R_5 + R_6)\,s + 1} \tag{2.16}$$

$$\frac{L_1(s)}{L_0(s)} = \frac{C_5R_9\,s + 1}{(0.5C_5R)\,s + 1} \tag{2.17}$$

As shown by Equations (2.15) and (2.16), there is a well-defined pole at $\omega_{p3} = \frac{1}{(R_5+R_6)C_4}$ and a zero at $\omega_{z2} = \frac{1}{R_6C_4}$, which can be chosen to achieve optimal NTF for the second SDM loop. Furthermore, increasing R shifts the remaining two poles to lower frequencies, thereby strengthening the second-loop noise-shaping response. Equation (2.17) shows that suppression of E_1 at the MASH output requires the pole at $\omega_p = \frac{1}{0.5C_5R}$ to coincide with the pole of $H_1(s)$, while the zero at $\omega_z = \frac{1}{C_5R_9}$ is shifted to a higher frequency. This can be done for a given R by selecting R_9 << R and choosing C_5 that ensures $(0.5R_{in}C_1)^{-1} = (0.5R_{in2}C_5)^{-1}$. As shown, the design procedure for this architecture is much simpler than that of the comparator-input sensing architecture. Chapter 3 presents the detailed design procedure for the amplifier-output sensing architecture.

Figure 2.14 shows the corresponding representative responses for the amplifier-output sensing architecture. In this topology, the signal applied to the second loop is sensed at the output of A_1. Therefore, the sensed E_1 component is only first-order noise shaped. Consequently, STF_2 requires only one in-band zero, located at the corresponding pole frequency of $H_1(s)$, rather than the two in-band zeros required by the comparator-input sensing architecture. Compared with the comparator-input architecture in Figure 2.8, the amplifier-output architecture places the poles of L1(s), and hence the zeros of NTF2, at lower and more closely spaced frequencies. Meanwhile, the NTF2 poles remain at higher frequencies, extending the third-order noise-shaping region and improving the suppression of second-loop quantization noise.

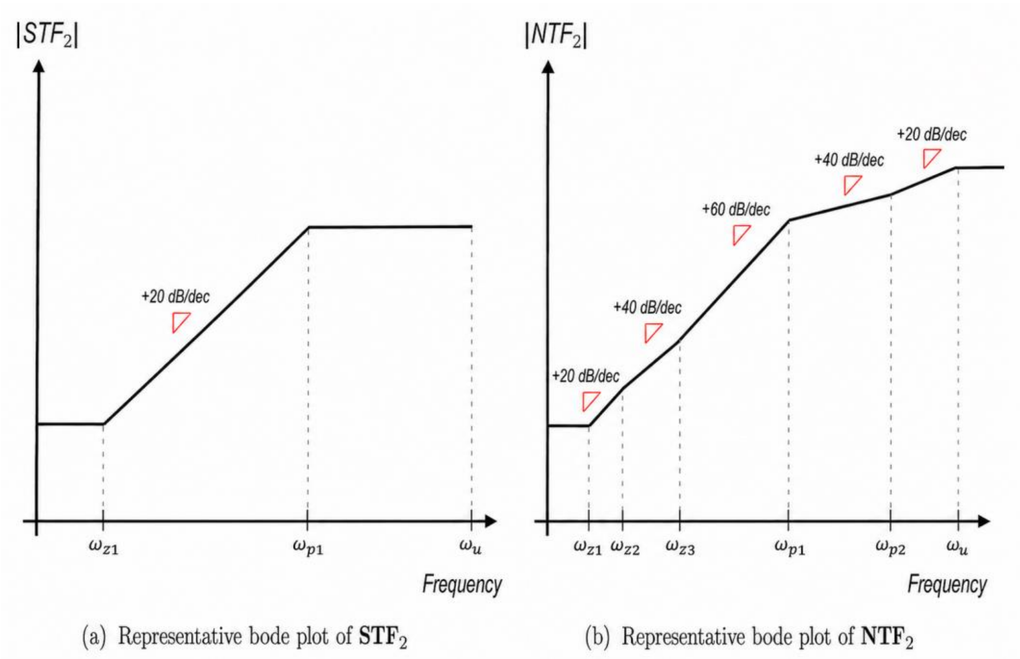


Figure 2.14 Representative asymptotic Bode plots of STF_2 and NTF_2 for the amplifier-output sensing architecture.

Table 2.2 Component Values of amplifier-output sensing architecture shown in Figure 2.11

Component name	Numerical value
R_{IN} & R_{DAC}	3.5 kΩ
R_2 & R_3	6.725 kΩ
R_4	180 Ω
R_{IN2}	56 kΩ
R_5	360 kΩ
R_6	19.6 kΩ
R_7 & R_8	76.2 kΩ
R_9	8 kΩ
G_{m1}	2 mS
G_{m2}	222 µS
C_1	246.5 pF
C_2	100 pF
C_3	34 pF
C_4	3 pF
C_5	27.2 pF

Figure 2.15 displays the output spectrum of a system-level simulation of the topology illustrated in Figure 2.11 using the component values listed in Table 2.2. The simulation uses a 40.4358 kHz sinusoidal input with a peak amplitude of 1.02 V. The modulator achieves 119 dB SQNR and −121.25 dB THD over a bandwidth of around 200 kHz at a 100 MHz sampling frequency. The first SDM achieves 92.87 dB SQNR and −72.63 dB THD. This means that the second SDM improves the SDM1 SQNR by 26.1 dB and the THD by 48.6 dB, showing its effectiveness.

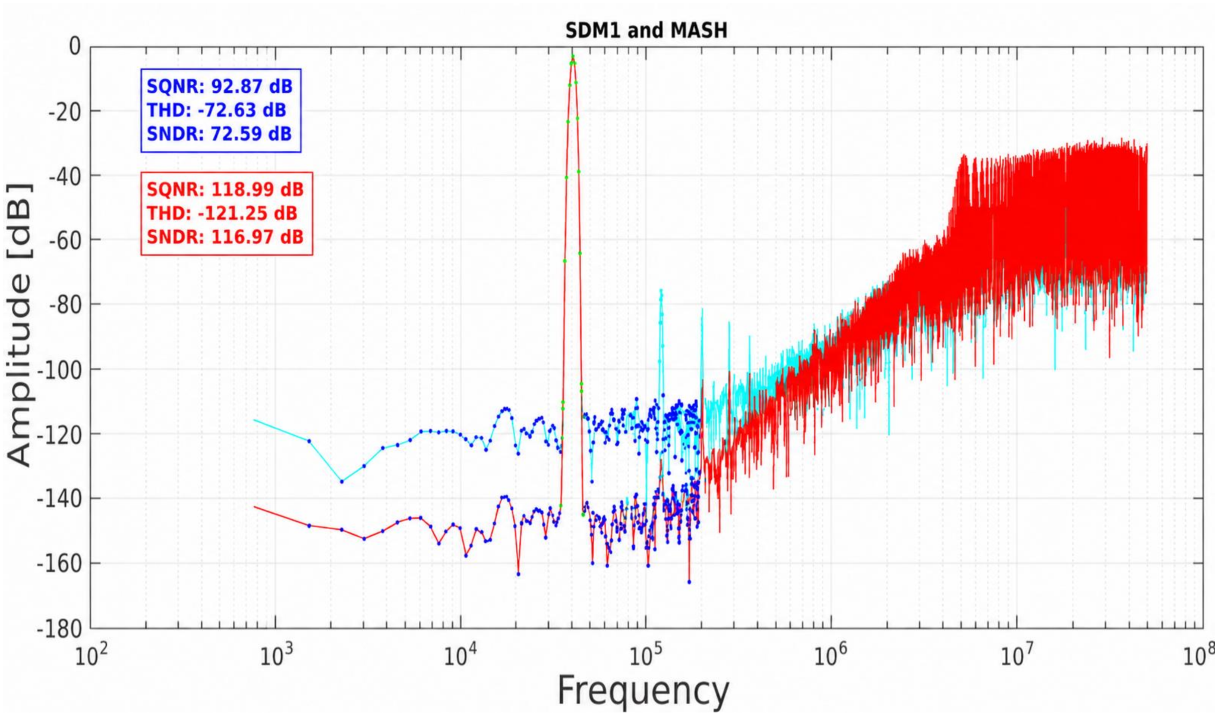


Figure 2.15 Spectrum of the SDM1 (blue) and MASH (red) output bitstreams of the amplifier-output sensing architecture.

Similar to the comparator-input sensing architecture, the proposed architecture suppresses E_1 leakage at the MASH output. The same analysis indicates that this architecture is robust to component mismatch because such a mismatch primarily shifts the notch frequency while preserving the overall in-band suppression. To verify this robustness, the design was modelled in Simulink and evaluated in 50 simulation runs with random ±5% variations applied to the R, C, and G_m component values. The histogram of the resulting $SQNR_{mash}$ values is shown in Figure 2.16. The mean $SQNR_{MASH}$ is 117.5 dB, with a standard deviation of 1.24 dB.

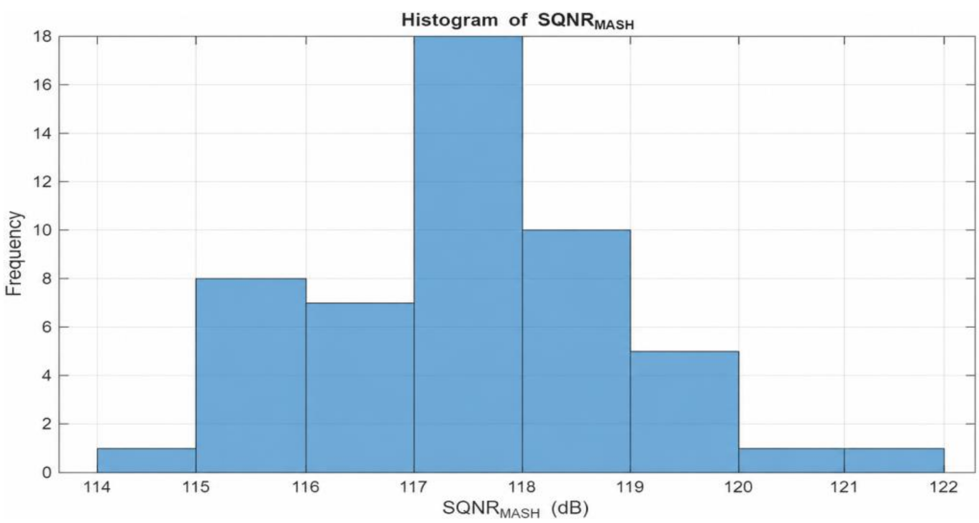


Figure 2.16 Histogram of $SQNR_{MASH}$ under ±5% component mismatch.

Chapter 3. Loop-Filter Design

This chapter presents a systematic design procedure for the amplifier-output sensing architecture shown in Figure 2.11, subject to given bandwidth and SNR requirements. Furthermore, it justifies the component values listed in Table 2.2 and explain the associated trade-offs. As discussed in Chapter 1, this design targets an SNR of 103 dB and an SQNR of 115 dB over a bandwidth of around 200 kHz. The second loop can increase the first-stage SQNR by approximately 25 dB; therefore, the first-SDM design target is an SQNR of 90 dB over a bandwidth of around 200 kHz.

3.1. Input Stage and 1st OTA Power Optimization

In the first SDM in our MASH architecture (RC-OTA SDM), the input-stage noise contribution is determined by the OTA, along with the input and DAC resistors, as shown in Figure 3.1. The optimization procedure described in [26] is applied here.

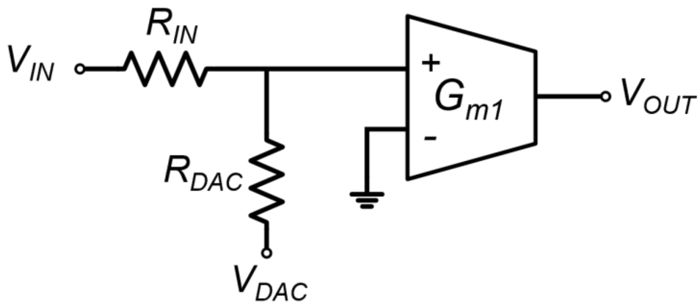


Figure 3.1 Dominant noise sources.

Neglecting the OTA's 1/f noise, the total input-referred noise in a bandwidth f_{bw} can be estimated as:

$$V_{n,in}^2 = 4kTR_{IN}f_{bw} + \frac{4kTf_{bw}}{R_{DAC}}R_{IN}^2 + \frac{4kTf_{bw}}{G_{m1}}\left(1 + \frac{R_{IN}}{R_{DAC}}\right)^2 \tag{3.1}$$

Assuming that $R_{IN} = R_{DAC}$ gives:

$$V_{n,in}^2 = 8kTf_{bw}\left(R_{IN} + \frac{2}{G_{m1}}\right) \tag{3.2}$$

Similarly, the ADC's power consumption is dominated by the first OTA and the DAC. The power consumption of these blocks can be estimated as follows:

$$P_{OTA,DAC} = \frac{V_{ref}^2}{R_{IN}} + V_{DD} * \frac{2G_{m1}}{\beta} \tag{3.3}$$

where $\beta = G_{m1}/I_d \approx 20V^{-1}$.

As shown in the equations above, there is a trade-off between input-referred noise and power consumption. Increasing G_{m1} decreases its noise but increases its power consumption. Similarly, decreasing R_{DAC} decreases its noise but increases its power consumption. Given these trade-offs, R_{DAC}

and G_{m1} can be optimized to minimize power consumption for a given target SNR within a certain bandwidth.

By fixing the SNR target, the ADC's input-referred noise power must satisfy:

$$V_{n,in}^2 = \left(\frac{V_{in,rms}}{10^{\frac{SNR}{20}}}\right)^2 \tag{3.4}$$

From Equation (3.2), the input resistor can then be expressed as:

$$R_{IN} = \frac{V_{n,in}^2}{8kTf_{bw}} - \frac{2}{G_{m1}} \tag{3.5}$$

For a second-order SDM with a 1-bit quantizer, the maximum stable amplitude (MSA) is about 0.9*V_{ref} [11]. As a result, $V_{in} = 1.08V$, resulting in $V_{n,in} = 5.4\ \mu V_{rms}$ for the target 103 dB SNR. The power consumption of the DAC and first OTA as a function of G_m is shown in Figure 3.2. As shown, the minimum power consumption at 103 dB SNR over a bandwidth of around 200 kHz is 529 µW. The optimized G_{m1}, R_{IN}, and R_{DAC} values are 2 mS, 3.5 kΩ, and 3.5 kΩ, respectively.

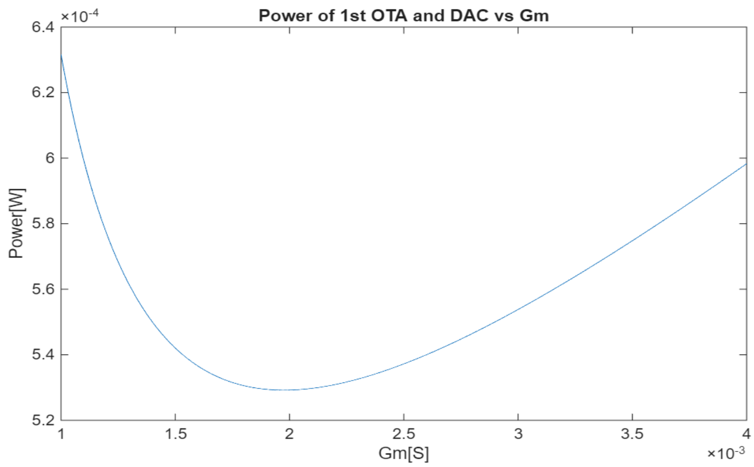


Figure 3.2 Power and noise optimization.

3.2. Loop Filter Design

The design begins with the first-SDM loop shown in Figure 3.3. Section 3.1 gives the optimal values of G_{m1}, R_{in}, and R_{DAC} as 2 mS, 3.5 kΩ, and 3.5 kΩ, respectively. The next step is to select C_1. As discussed in Chapter 1, the first pole should be placed at or just beyond the upper edge of the signal bandwidth to optimize thermal-noise efficiency and quantization-noise suppression. Accordingly, C_1 = $(2\pi \frac{R_{in}}{2} f_{BW})^{-1}$= 465.7 pF; however, this value would occupy a large area. To improve area efficiency, C_1 is reduced to 246.5 pF, while the SQNR specification is maintained by optimizing the second-pole frequency. C_1 can be further reduced only by increasing the allowable noise budget, which permits a larger R_{in} for the same bandwidth. For a fixed SNR target, increasing the bandwidth requires a smaller R_{in} to satisfy the noise budget; consequently, C_1 remains approximately constant.

To satisfy the linearity requirement of the G_{m1} stage, the voltage swing at the node V_{x2} should be limited to less than 200 mV. The voltage swing at V_{x2} is directly proportional to G_{m1} and R_2. The simulation results show that R_2 = R_3 = 6.725 kΩ produces an 185 mV voltage swing at V_{x2}. Given that the zero and second-pole frequencies are given by $\omega_z = (R_4C_2)^{-1}$ and $\omega_{p2} = ((2R_2 + R_4)C_2)^{-1}$

respectively, R_4 and C_2 can be selected to maximize the SQNR of SDM1. A larger R_2 is desirable because it can reduce the required C_2 area and increase A_1; however, increasing A_1 will increase the linearity requirement of the G_{m1} stage. A_1 can be increased either by improving the linearity of the G_{m1} stage to tolerate a larger output swing or by reducing the voltage swing at V_x. The latter can easily be done by moving $\omega_p = (0.5R_{in}C_1)^{-1}$ to a lower frequency, but this will require lowering the SNR target as mentioned earlier. Furthermore, reducing the SNR target will enable decreasing G_{m1}, increasing R_2, and decreasing C_2, given the same amplifier gain.

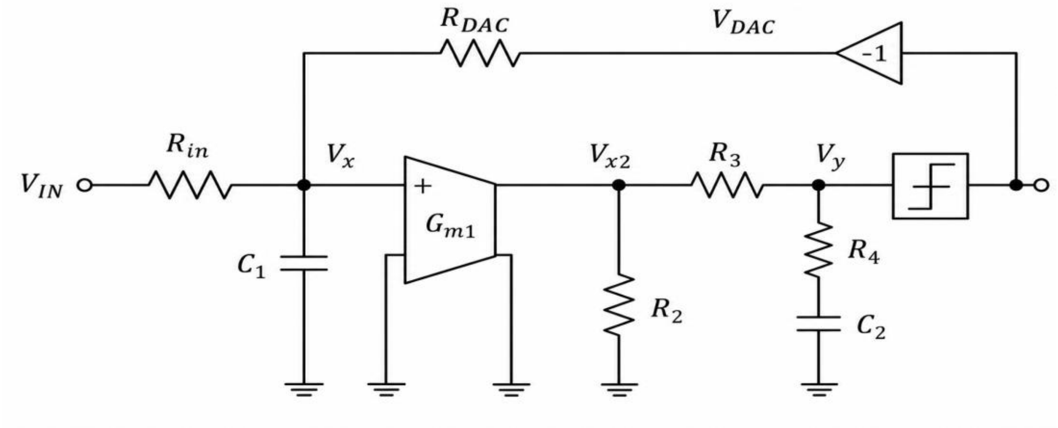


Figure 3.3 Circuit-level model of the first SDM loop.

Regarding the second SDM shown in Figure 2.13, Equations (2.15) and (2.16) define a pole at $\omega_{p3} = \frac{1}{(R_5+R_6)C_4}$ and a zero at $\omega_{z2} = \frac{1}{R_6C_4}$; these frequencies can be selected to optimize the second-loop NTF. To reduce loading between the two SDM loops, R_{in2} should satisfy $R_{in2} \gg R_2$. The initial design sets $R_{in2} = 10 * R_2$ as a practical approximation to this condition. For the initial analytical approximation, $R_7 = R_8 = R$ and $R_{in2} = 2R$, so that the input and DAC resistances are equal. C_5 can then be selected such that $(0.5R_{in}C_1)^{-1} = (0.5R_{in2}C_5)^{-1}$ to equate the pole of $\frac{L_1(s)}{L_0(s)}$ and $H_1(s)$ as shown in Equation (2.17). R_9 is then set to $\frac{R_{in2}}{10}$ to ensure that the zero of $\frac{L_1(s)}{L_0(s)}$ is placed at a higher frequency than its pole. The only remaining component is C_3, which should be chosen to shift the two zeros of the second-loop NTF to lower frequencies. Equation (2.15) shows that the two zeros of the second loop NTF are given by:

$$\omega_{z1,2} = \frac{C_3 + 0.75C_5}{C_3C_5R} \pm \frac{\sqrt{(C_3 + 0.75C_5)^2 - 2C_3C_5}}{C_3C_5R} \quad (3.6)$$

Equation (3.6) shows that increasing C_3 shifts the NTF zeros to lower frequencies. Thus, C_3 presents a trade-off between capacitor area and second-loop noise-shaping performance. With $A_1 = 6.725$, the required digital attenuation factor is $\frac{2}{A_1}$. To implement the digital scaling as $\frac{1}{2^n}$, A_3 is set to 1/16, and an additional analog amplifier should provide the remaining scaling with a gain of 4.76. Alternatively, the required gain can be realized by increasing the second-loop DAC resistance because the second-loop gain is $\frac{R_{DAC}}{R_{in}} = \frac{R_7+R_8}{R_{in2}}$. Table 2.2 lists the final values obtained after Simulink optimization. It should be noted that the SDM2 gain is slightly increased, and the pole of $\frac{L_1(s)}{L_0(s)}$ is pushed slightly to a lower frequency to obtain a transfer function similar to the one shown in Figure 2.9. This adjustment is intended to preserve robustness to component mismatch, as discussed above.

Chapter 4. Circuit Implementation

To demonstrate the feasibility of the newly proposed MASH architecture, the amplifier-output sensing architecture has been implemented in TSMC 65 nm technology. This chapter describes the detailed implementation of the blocks shown in Figure 2.11.

4.1. OTA_1

As established in Section 3.2, OTA_1 requires a DC gain of 22.35 dB. To satisfy the overall noise target, its input-referred noise density should not exceed $2.88\, nV/\sqrt{Hz}$. To improve the noise and power efficiency of OTA_1, the current-reuse architecture is chosen because it doubles G_m for the same bias current compared with the telescopic architecture. To improve the linearity of the OTA, a pseudo-differential OTA is preferred over a differential pair with a tail current source, as proposed in recent designs [27]. In addition, stacking four transistors between V_{DD} and ground allows a higher V_{DS} for each device, keeping them well within the saturation region compared to stacking 6 transistors. The pseudo-differential OTA linearity can be further improved by adding tail resistors [28]. Based on these considerations, the current-reuse tail-resistor linearized OTA shown in Figure 4.1 [28] is selected for this design.

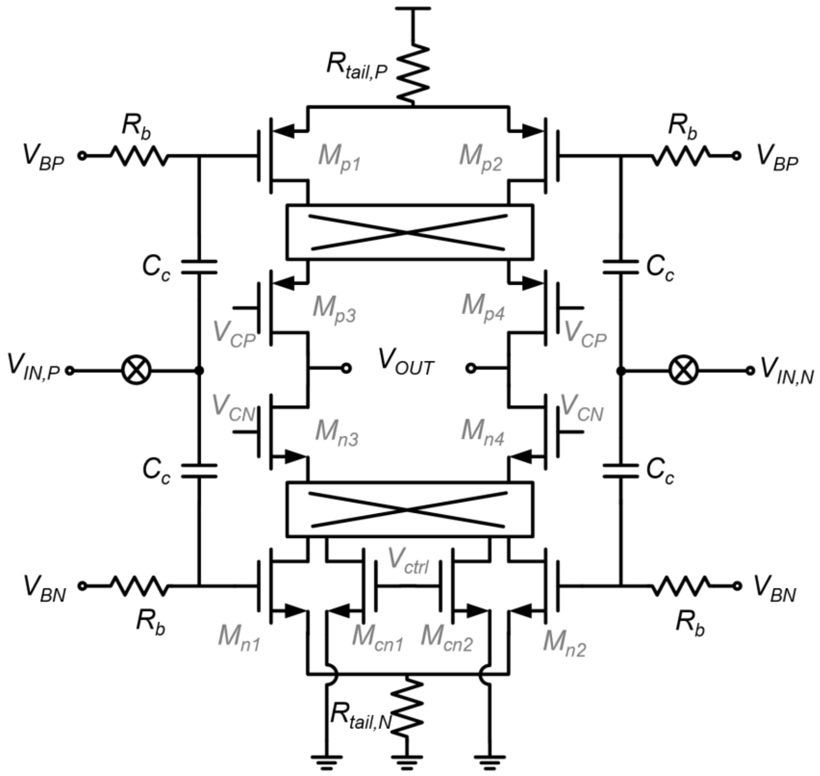


Figure 4.1 The current-reuse tail-resistor linearized OTA_1 [26].

The rationale for using a tail resistor can be explained with a simplified OTA model with different source loading, as shown in Figure 4.2. If we use a tail current source, the large-signal model of the output current has compressive nonlinearity because the tail current source limits the maximum output current. On the other hand, if we use a pseudo-differential input with no source loading, the output current has an expansive nonlinearity that follows the square law. Therefore, if we use a tail resistor with a value between these two extremes, a 'sweet point' can be achieved to linearize the V-I characteristic. The values of $R_{tail,N}$ and $R_{tail,P}$ are chosen to cancel the 3^{rd}-order distortion of each differential pair using Equations (4.1) and (4.2) [28].

$$R_{tail,N} = \frac{nV_T}{2 \times I_{tail,N}} = \frac{26\ mV}{2 \times 0.7 \times 240\ \mu A} = 77.4\ \Omega \tag{4.1}$$

$$R_{tail,P} = \frac{nV_T}{2 \times I_{tail,P}} = \frac{26\ mV}{2 \times 240\ \mu A} = 54.2\ \Omega \tag{4.2}$$

Where n is the process-dependent factor, V_T is the thermal voltage, and $I_{tail,N}$ and $I_{tail,P}$ are the negative and positive tail currents, respectively. The current values are derived assuming $g_m/I_d \sim 20V^{-1}$ for both the NMOS and PMOS input pairs. It should be noted that 30% of the NMOS input-pair current is shunted to ground through $M_{cn1,2}$ to stabilize the OTA common-mode voltage.

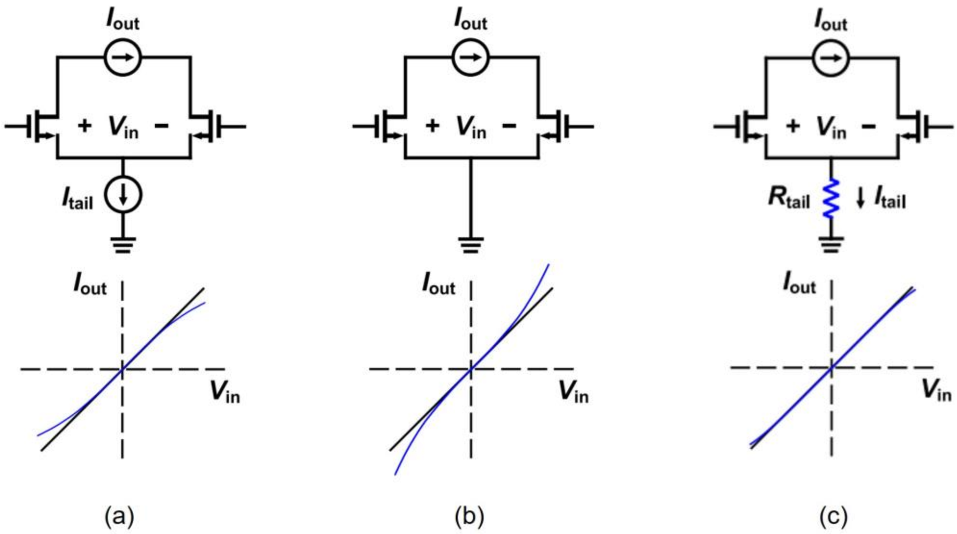


Figure 4.2 Simplified version of OTA with different source loading: (a) tail current source, (b) pseudo-differential, (c) tail resistor [28].

To improve power efficiency, the input pairs $M_{n1,2}$ and $M_{p1,2}$ are biased in weak inversion. OTA_1 employs input chopping at $f_s/2$ to suppress the flicker noise of the NMOS and PMOS input pairs; the chopping network and frequency selection are discussed below. The required single-ended equivalent transconductance is increased from 2 mS to 2.4 mS in order to meet the target noise specification of $2.88nV/\sqrt{Hz}$ because 30% of the NMOS input-pair current is used in the CMFB loop. Furthermore, the flicker noise of the cascode transistors $M_{P3,4}$ and $M_{N3,4}$ is not modulated and remains as a residual input-referred contribution because only the input pairs are chopped. The input-referred noise density across corners (TT, SS, FF) and temperature (-40 °C – 100 °C) of OTA_1 is shown in Figure 4.3. The corresponding Periodic AC (PAC) response of OTA1 under the same corner and temperature conditions is shown in Figure 4.4. At the signal-band edge of around 200 kHz, the simulated gain ranges from approximately 21.48 dB to 24.18 dB, with a nominal TT/27°C gain of 22.89 dB.

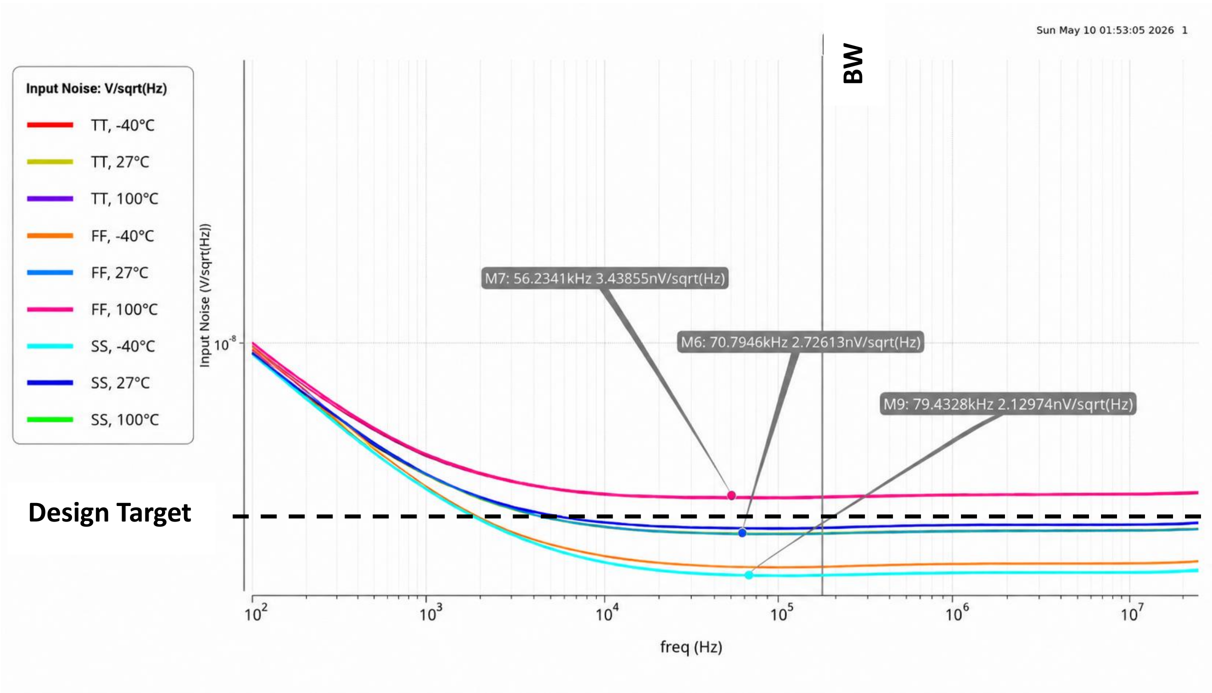


Figure 4.3 Input referred noise of OTA_1 across process corners and temperature.

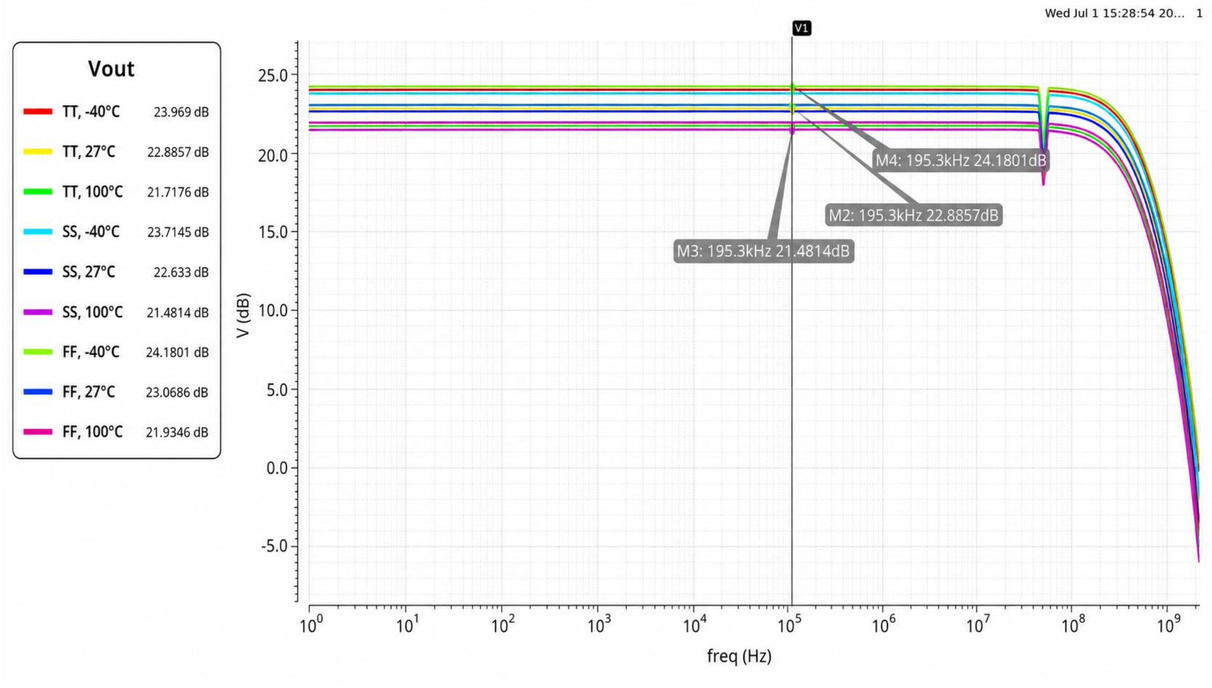


Figure 4.4 PAC response of OTA_1 across process corners and temperature.

Chopping is used to reject the flicker noise of the input pairs. To avoid increasing the noise floor due to intermodulation with the quantization noise, the chopping frequency should be f_s or $f_s/2$ [27]. The input chopper periodically commutates the OTA input capacitance and therefore presents a finite switched-capacitor resistance R_{ch} inversely proportional to chopping frequency f_{ch} [29]. Consequently, choosing $f_{\mathrm{ch}} = f_s/2$ instead of f_s doubles R_{ch}. Since the input node sees $R_{\mathrm{in}} \parallel R_{\mathrm{DAC}} \parallel R_{\mathrm{ch}}$, the larger chopper resistance reduces the additional loading and preserves the intended input-network resistance. The up-modulated input signal passes through the high-pass filter formed by the biasing resistor (R_b) and the coupling capacitor (C_c). The DC bias voltages of the input transistors are set through biasing resistors, enabling the PMOS and NMOS input transistors to be biased independently. However, the biasing resistors introduce thermal noise, which is low-pass filtered when referred to the OTA input. Therefore, we need to push the cutoff frequency to a low value. The high-pass coupling network is formed by R_b = 300 kΩ and C_c = 2 pF, giving a cutoff frequency of 265.3 kHz. The biasing resistor value is selected based on simulation results to ensure that its contribution is less than 2% of the total input-referred noise of OTA_1.

To generate the biasing voltages V_{BP} and V_{BN} for the input pairs and V_{CP} and V_{CN} for the cascode stage, a replica biasing scheme is used, as shown in Figure 4.5. Each branch of the replica-bias network draws approximately 6 μA, while the corresponding branch in the main OTA is biased at 20 times this current to achieve the target transconductance. The 1:20 current ratio is selected to reduce the power overhead of the bias network. This 1:20 scaling factor is also preserved for the tail resistors to maintain the intended voltage drops and operating points.

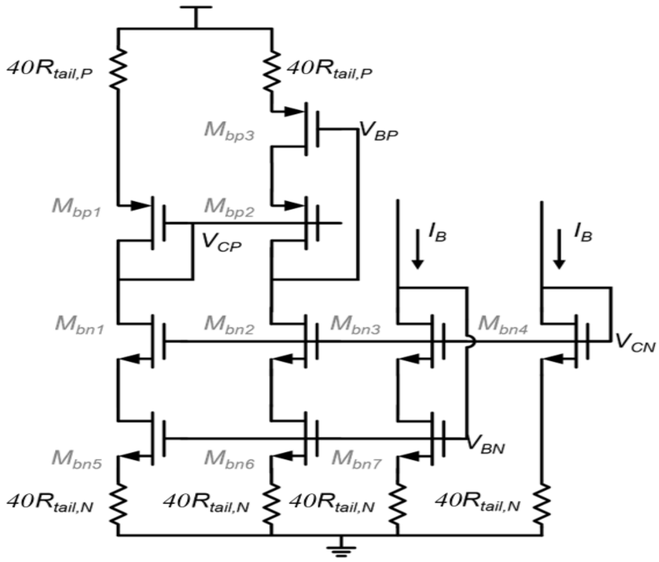


Figure 4.5 Biasing circuit of OTA_1.

The common-mode feedback (CMFB) [27] shown in Figure 4.6 ensures that the OTA differential outputs are maintained around $V_{DD}/2$. The two differential pairs, M_{cp3}-M_{cp6}, compare the OTA outputs to a reference voltage $V_{cm}= V_{DD}/2$. The input pairs produce two differential currents proportional to ($V_{outn} - V_{cm}$) and ($V_{outp} - V_{cm}$). These currents are added at the V_{ctrl} node, ensuring that the control voltage is proportional to $(V_{outp} + V_{outn})/2 - V_{CM}$. Therefore, this negative feedback loop ensures that $(V_{outp} + V_{outn})/2 = V_{CM}$, so that the OTA CM output equals the reference voltage. A compensation capacitor (C_{comp} = 100 fF) ensures loop stability, with a simulated phase margin = 85.4°, as shown in Figure 4.7.

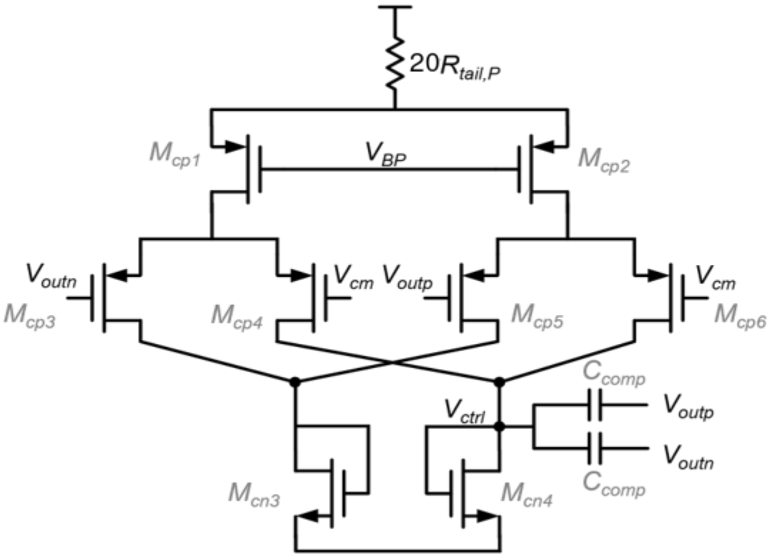


Figure 4.6 CMFB of OTA_1.

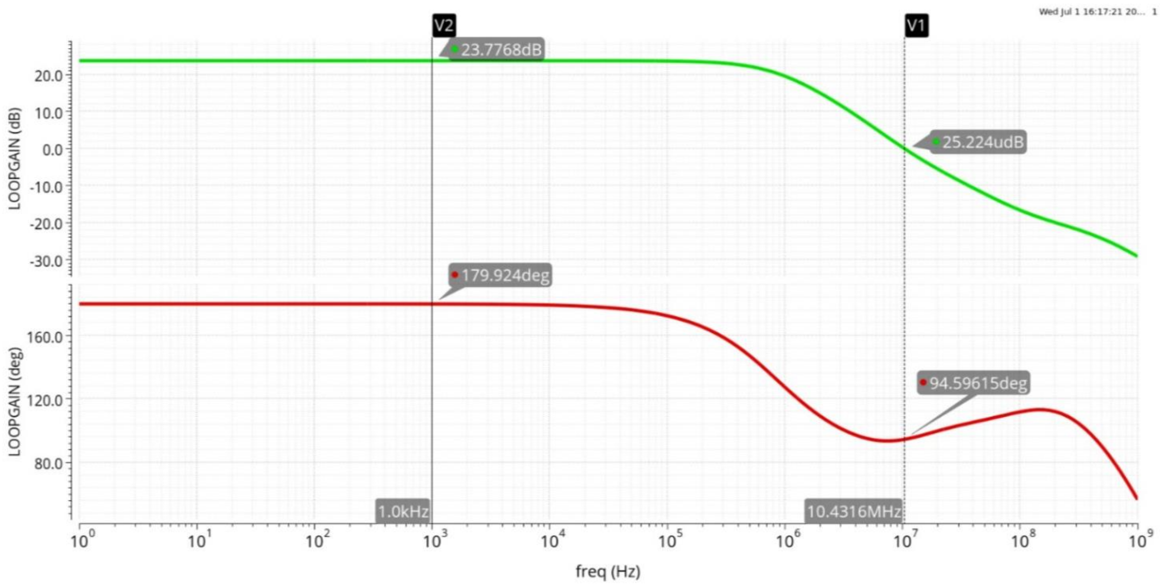


Figure 4.7 CMFB loop stability analysis.

Table 4.1 OTA_1's transistor sizing

Name	W/L(um/um)	Multipliers	Fingers	I_d(uA)
$M_{p1,2}$	2.5/0.11	1	40	149
$M_{p3,4}$	2.5/0.36	2	20	149
$M_{n1,2}$	3.3/0.11	16	1	101.4
$M_{n3,4}$	1.35/0.41	2	20	144
$M_{cn1,2}$	3.3/0.11	4	1	42.6
$M_{bn1,2,3}$	1.15/0.41	2	1	5.9
M_{bn4}	1.15/4.29	1	1	5.8
$M_{bn5,6,7}$	2.8/0.11	1	1	5.9
M_{bp1}	2.15/2.965	1	1	5.9
M_{bp2}	2.15/0.36	2	1	5.97

M_{bp3}	3.8/0.11	1	1	5.97
$M_{cp1,2}$	1.3/0.4	1	1	9.3
$M_{cp3,4,5,6}$	10/0.3	1	3	4.65
$M_{cn4,5}$	8/0.35	1	1	9.3

4.2. OTA_2

The noise and linearity requirements of OTA_2 are relaxed because the first amplifier gain suppresses them. The required single-ended equivalent transconductance of OTA_2 is 222 µS, which makes its power consumption around 10 times lower than that of OTA_1. The nominal input-referred noise density target is $8.65\ nV/\sqrt{Hz}$. OTA_2 should have a high DC gain (38dB) to relax the noise requirement of the second stage comparator. However, the gain inaccuracy of OTA_2 is not a critical issue because OTA_2 is placed within the second-stage loop. Still, the noise requirement of OTA_2 is important because the gain of the first amplifier is low. Therefore, a current-reuse differential OTA topology, shown in Figure 4.8, is chosen for OTA_2 because of its noise and power efficiency. The linearity requirement of OTA_2 is greatly less stringent than that of OTA_1. Therefore, the tail-resistor linearization employed in OTA_1 is not required. Although the six-transistor stack reduces the available voltage headroom and complicates maintaining adequate saturation margin across PVT variations, reliable operation can still be achieved through careful device sizing and bias design.

The input pairs $M_{n1,2}$ and $M_{p1,2}$ are biased in weak inversion to improve energy efficiency. On the other hand, the current sources M_{n6} and M_{p5} are biased in strong inversion to improve their matching. The cascode transistor pairs $M_{n3,4}$ and $M_{p3,4}$ are biased in weak inversion to decrease their overdrive voltage, ensuring that we can stack 6 transistors within a 1.2V power supply across PVT variations. Long-length diode-connected transistors, M_{bp6} and M_{bn5}, are used to generate the cascode biasing voltages. The biasing current is generated by a constant g_m biasing circuit and mirrored to OTA_2 via M_{bp4}.

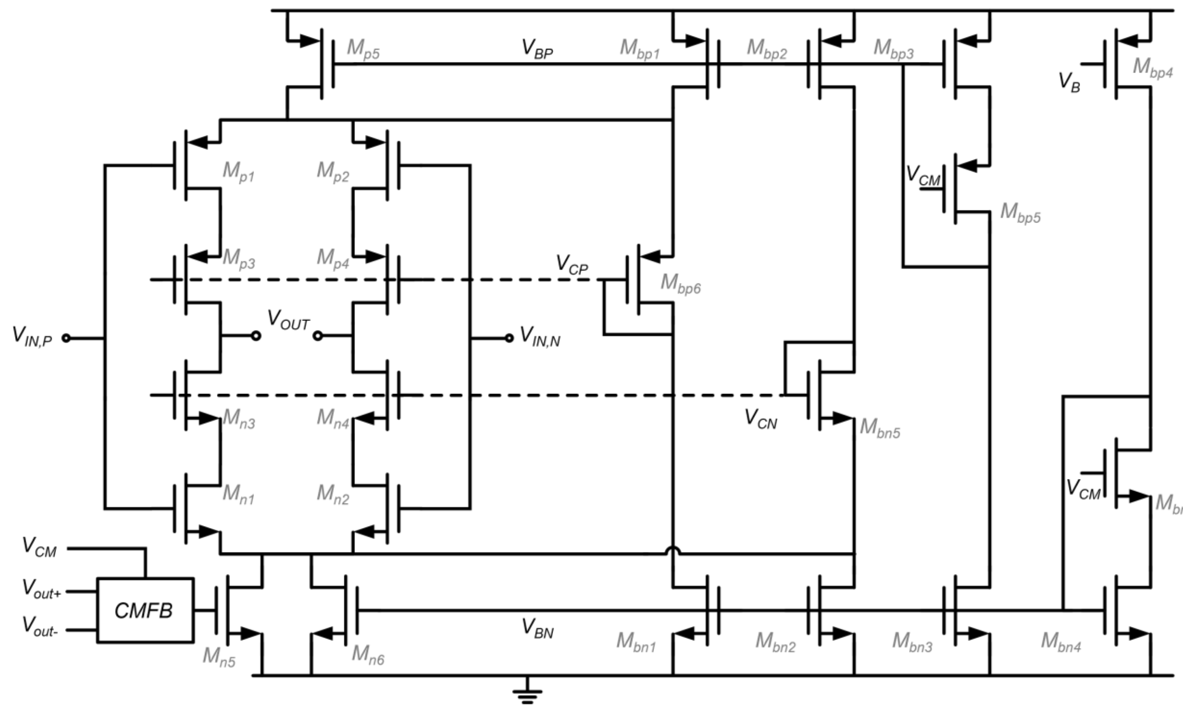


Figure 4.8 Schematic of OTA_2 including the biasing circuit [26].

Figure 4.9 shows the input-referred noise density across corners (TT, SS, FF) and temperature (-40 °C – 100 °C) of OTA$_2$. The OTA$_2$ noise performance is verified across process corners and temperature, meeting the target noise specification of $8.65\ nV/\sqrt{Hz}$.

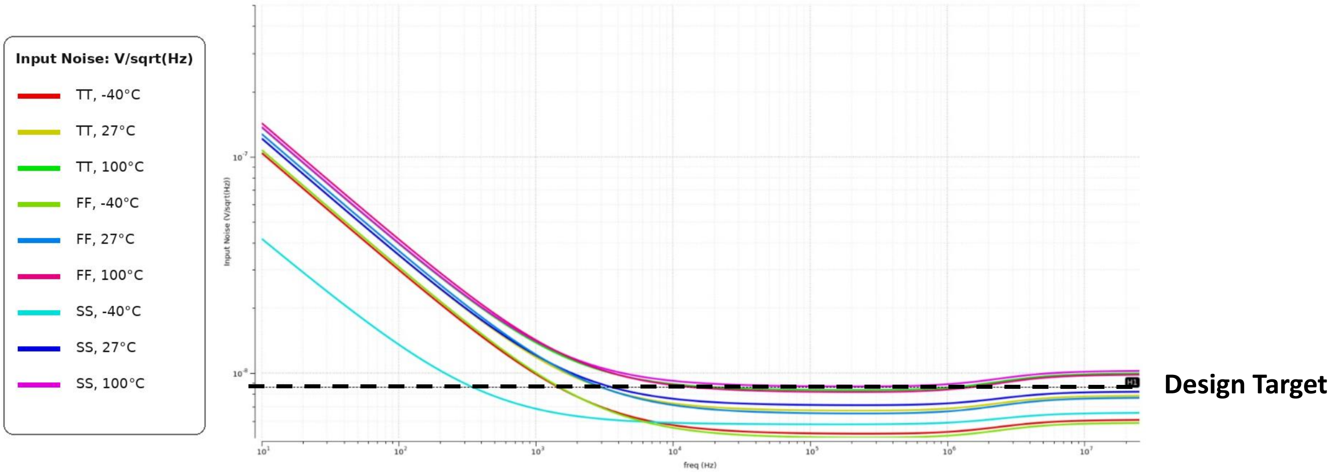


Figure 4.9 Input referred noise of OTA$_2$ across process corners and temperature.

4.3. Constant g_m biasing

To generate the bias voltages of OTA$_1$ and OTA$_2$, the constant-g_m biasing circuit is designed similarly to the one proposed in [28]. As shown in Figure 4.10, the current mirrors M_5 and M_6 ensure that the currents through M_1 and M_2 are equal when M=1. Transistors M_1 and M_2 are biased in weak inversion. The negative feedback loop formed by transistors M_3 and M_4 establishes a PTAT current through R_{bias} given by:

$$I_B = \frac{nV_T}{R_{bias}} \ln(K) \tag{4.3}$$

where n is the process-dependent slope factor, and V_T is the thermal voltage. With R_{bias} = 37 kΩ and K=4, the bias current is 1 µA. The remaining transistors form the start-up circuit. When the circuit turns on, the drain voltages of M_1 and M_2 are 0. This state is passed through the inverter formed by M_{10} and M_{11}, which turns on M_9. Then, M_9 introduces a current through M_4, which is mirrored through M_5 and M_6, charging the internal nodes. When the drain voltages of M_1 and M_2 increase, M_9 is turned off, and the circuit operates around its operating point. The capacitors C_1 and C_2 are used to ensure loop stability.

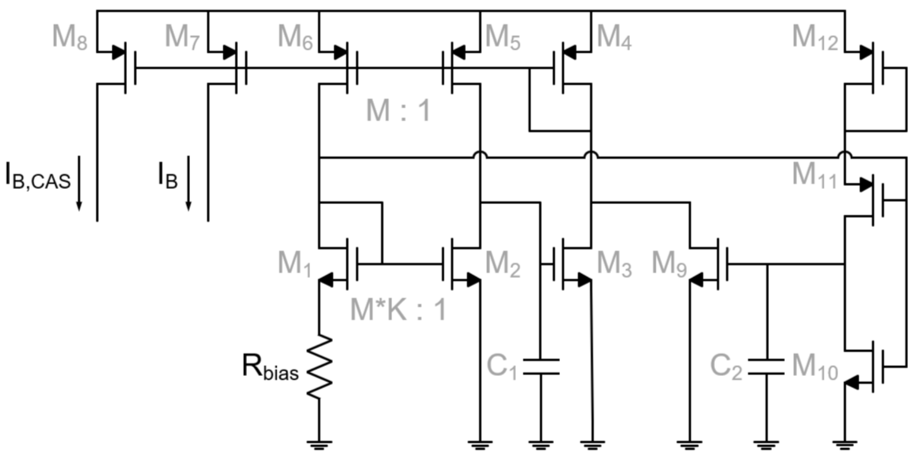


Figure 4.10 Schematic of constant g_m biasing.

As discussed in Chapter 2, this design requires reasonable matching between the digital attenuation and the analog gain. Therefore, variation in the first amplifier gain should be minimized across PVT corners. The constant-gm biasing circuit helps reduce this variation. Residual gain variations due to process and resistor tolerances can be controlled by trimming R_{bias} since the transconductance of M_2 is inversely proportional to R_{bias}.

4.4. Comparator

As discussed in Chapter 1, passive or hybrid SDMs have loop filters with low DC gain; therefore, they require high quantizer gain to recover the total loop gain. The gain of the single-bit quantizer is adjusted automatically because it has only two levels; therefore, the total loop gain is less sensitive to the DC gain of the loop filter. In addition, a single-bit quantizer is selected because of its simplicity and the inherent linearity of the 1-bit DAC.

For its simplicity, speed, and low power consumption, a modified version of the StrongARM comparator [30], described in [31] and shown in Figure 4.11, has been implemented for this design. To ensure loop stability, the design maintains a 1/8-clock-period delay between the comparator and DAC clock edges. The comparator input voltage swing in this design is limited to 7.4 mV because of the limited loop filter DC gain. The maximum tolerable input-referred noise of the comparator that does not degrade the SDM performance is 400 μV_{rms}, as verified using Simulink simulations.

The input pair $M_{n1,2}$ is sized to provide high transconductance during the amplification phase, thereby increasing the amplification gain and reducing the input-referred noise. Fortunately, the larger $M_{n1,2}$ area required to achieve high transconductance reduces the comparator's mismatch-induced offset, since $M_{n1,2}$ are the dominant offset contributors. The sizing of $M_{p1,2}$ is reduced to maintain comparator speed. The input-referred noise is reduced by decreasing the overdrive voltage of the $M_{n1,2}$ pair and increasing the capacitance at the Q and P nodes.

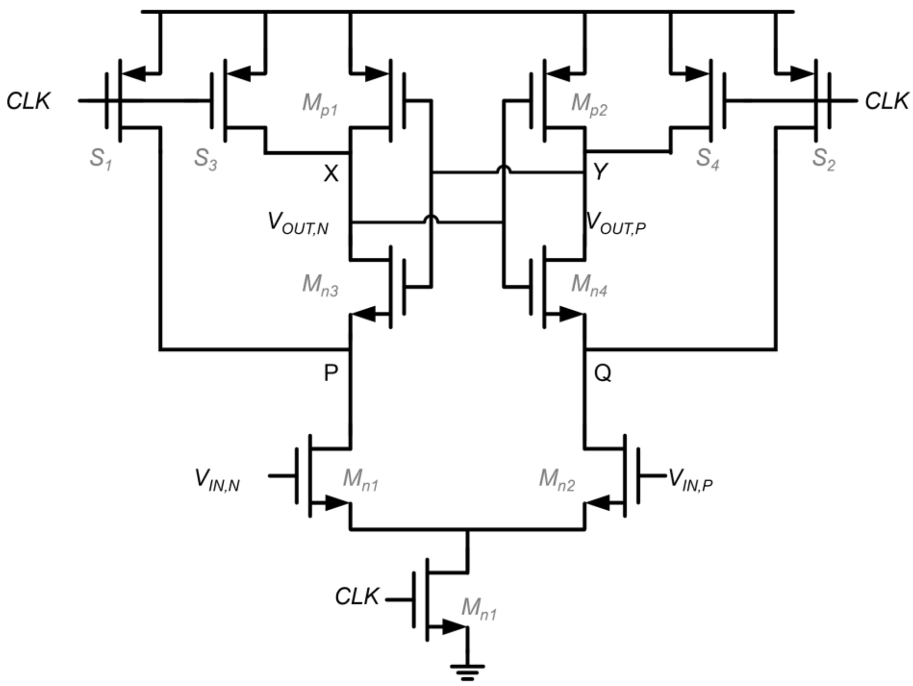


Figure 4.11 Schematic of the modified StrongARM comparator [26].

The input-referred noise of the comparator is simulated using the method described in [5]. For a comparator with negligible offset and ($V_{IN,P}$ - $V_{IN,N}$) = 0, transient noise produces ONEs and ZEROs with equal probabilities. Applying a small positive differential DC voltage V_S biases the comparator output toward ONE, such that a ZERO occurs only when the equivalent input-referred noise is less than $-V_S$ [5]. Assuming zero-mean Gaussian noise, the area under a Gaussian distribution from $-\sigma_n$ to $+\sigma_n$ is 68.26%, and hence that from $-\infty$ to $-\sigma_n$ is 15.87% [5]. Thus, adjusting V_S until approximately 16% of a sufficiently large number of decisions are ZEROs gives $V_S \approx \sigma_n$, where σ_n is the rms input-referred noise of the comparator [5].

The simulated input-referred noise is 100 μV_{rms}, as shown in Figure 4.12, corresponding to a factor-of-four margin relative to the maximum tolerable value of 400 μV_{rms}. Since the comparator consumes only 19.5 µW, corresponding to approximately 1.8% of the total system power, relaxing its noise performance toward the maximum allowable value would provide negligible improvement in the overall power efficiency. This additional margin is therefore retained to improve robustness against noise and performance variations across PVT corners. The comparator operates from $V_{\mathrm{DD}} = 1.2$ V at $f_s = 100$ MHz.

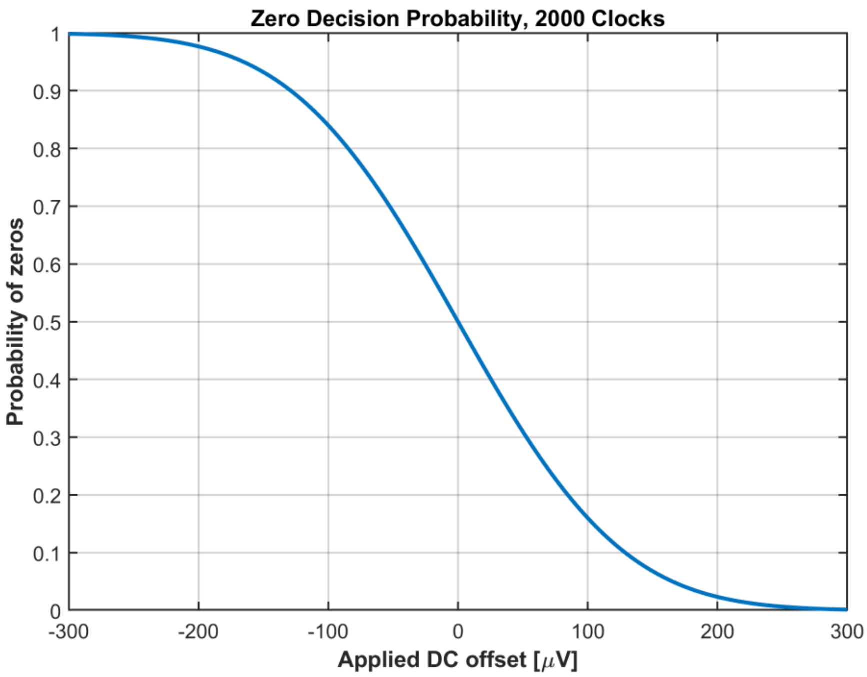


Figure 4.12 Output ZEROs probability versus the applied DC input over 2000 clock cycles.

4.5. Feedback DAC

DAC performance is critical for high-resolution CTSDMs because its non-idealities are directly referred to the input without being shaped, thereby degrading the overall ADC performance. The main concerns in DAC implementation, especially at high sampling frequencies, are clock jitter and Inter-Symbol Interference (ISI). The Switched-Resistor (SR) DAC is chosen for this design due to its simplicity. A Non-Return-to-Zero (NRZ) DAC is chosen over the Return-to-Zero (RZ) DAC because it offers better jitter robustness. However, the main issue with the NRZ DAC is ISI caused by unequal rise and fall times during DAC switching. The ISI problem can be resolved by separately matching the rise and fall times of the two D flip-flops (DFFs) shown in Figure 4.13 through careful sizing and layout [32].

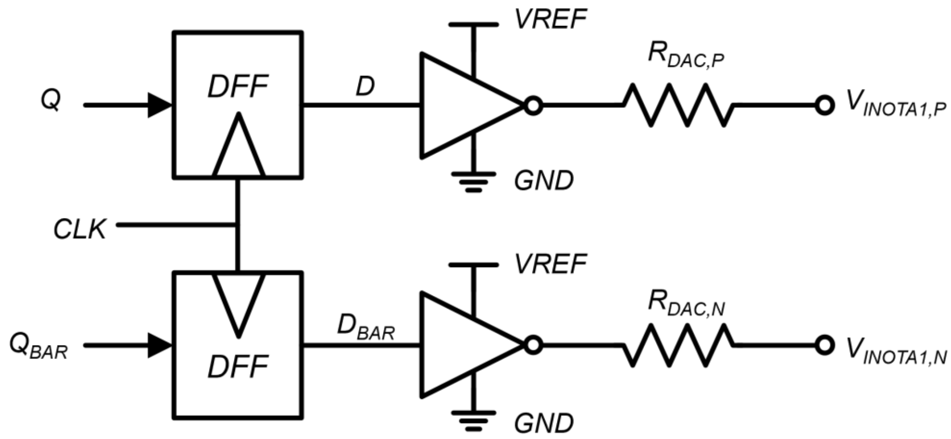


Figure 4.13 Representative diagram of the DAC [26].

The on-resistance of the DAC switches should be minimized to decrease the rise and fall times and reduce their input-referred noise. Therefore, the DFFs in the two DAC paths should have sufficient driving capability to produce fast and well-matched transitions at the D and D_{bar} nodes shown in Figure 4.13. This is important because the DAC clock jitter is directly referred to the SDM input, while unequal switching transitions increase ISI. A custom True Single-Phase Clock (TSPC) DFF is therefore used in this design. Its topology, operating principle, and performance are discussed in Section 4.6.

4.6. TSPC DFF

The driving capability of the DFF is important in this design because of its jitter sensitivity. Furthermore, the driving capability of the DFF determines the rise and fall times at the D and D_{bar} nodes shown in Figure 4.13. Slow or unequal transitions increase Inter-Symbol Interference (ISI) and make the DAC output more sensitive to clock jitter. As mentioned in Chapter 1, this design targets an SNDR of 100 dB over a bandwidth of around 200 kHz. Therefore, the signal-to-jitter-noise ratio (SJNR) must exceed 112 dB to preserve SDM performance. Simulation results show that the DFF with the highest driving capability in the TSMC library in 65 nm technology results in 104 dB SJNR, limiting the SDM performance to 98.8 dB SNDR. Therefore, a custom True Single-Phase Clock (TSPC) DFF is implemented.

Figure 4.14 shows the split-output TSPC DFF topology described in [33]. The circuit implements master-slave operation using only one clock phase. The input D is evaluated by the master stage and represented at the internal nodes A1 and A2. During the opposite clock phase, this state is transferred through the slave nodes B1 and B2 to the output Q. The split paths prevent input changes from overwriting the stored output during the active phase. Furthermore, only two transistors are directly controlled by CK, reducing the capacitive loading of the clock network. This topology is suitable for the DAC driver because TSPC logic provides high-speed operation, low power consumption, and reduced clocking complexity [33]. With the custom TSPC DFF, the simulated SJNR increases from 104 dB to 119 dB, exceeding the required 112 dB specification and supporting the target system performance. The simulated power consumption of the TSPC DFF is 3.5 µW at 100 MHz.

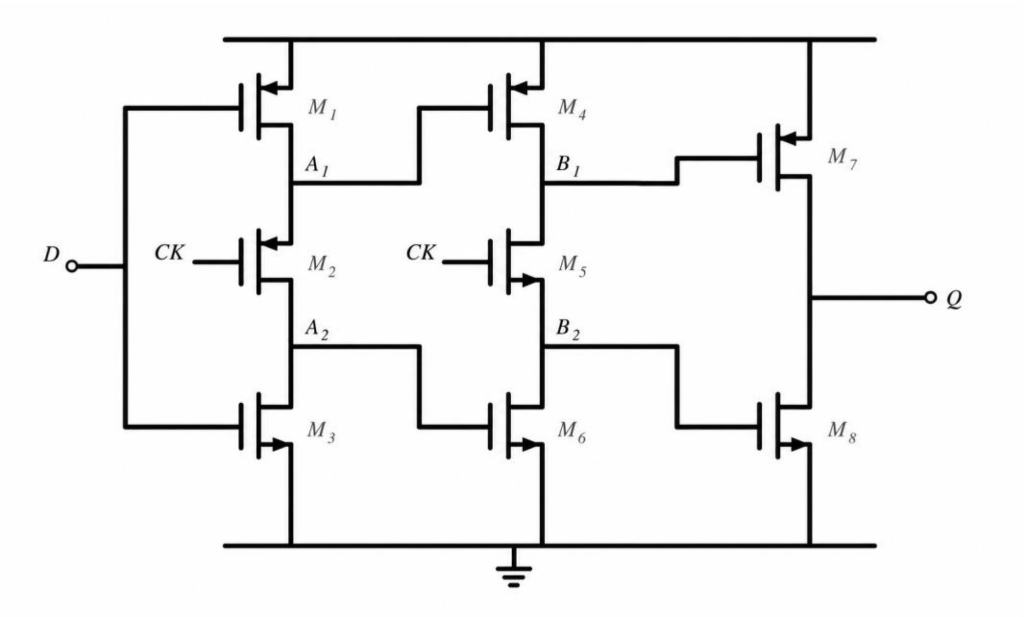


Figure 4.14 Schematic of the split-output TSPC DFF topology.

4.7. Clock Generator

As discussed in Section 4.4, a $T_s/8$ excess loop delay is kept between the comparator and DAC clock edges to give the comparator enough time to generate the output logic, ensuring stability. The DAC and comparator clocks operate at f_s = 100 MHz, whereas the chopper clocks ($\emptyset_1$ and $\emptyset_2$) operate at $f_s/2$. The resulting timing scheme is shown in Figure 4.15. An external 400 MHz clock can be supplied to the chip. This external clock can be divided internally by a Johnson counter using flip-flops from the 65nm standard cell library, producing two clock signals separated by $T_s/8$. However, receiving a clean 400 MHz CMOS clock signal is challenging in 65nm technology. Alternatively, an external 100 MHz clock can be supplied to the chip and delayed internally using an inverter chain to produce the required phase difference.

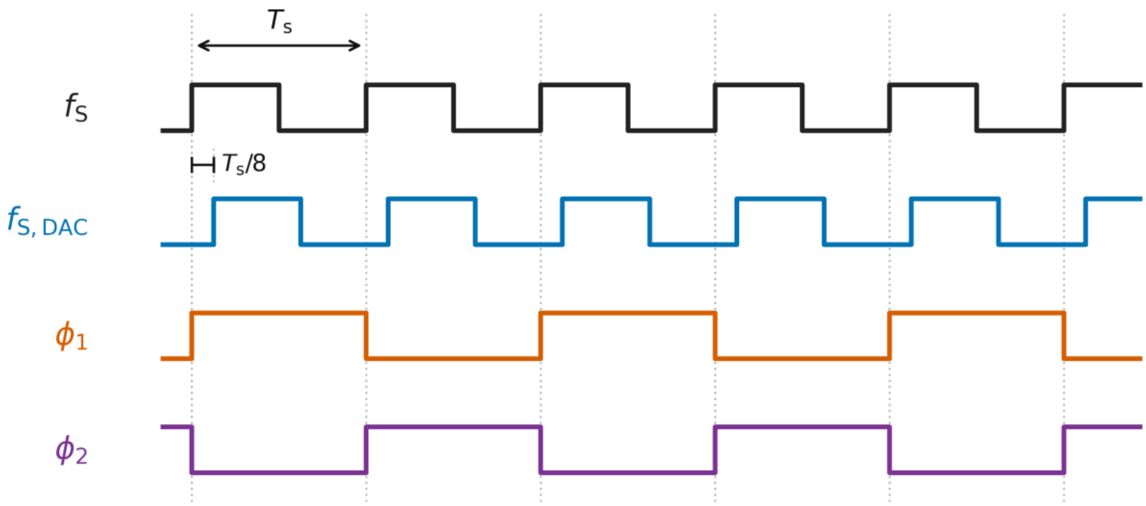


Figure 4.15 The timing scheme generated by the clock generation circuit.

The inverter delay chain will add extra jitter noise to the external clock. As mentioned earlier, the jitter noise in the quantizer clock (f_s) is suppressed by the NTF when referred back to the SDM input, similar to the quantization noise. On the other hand, the jitter in the DAC clock ($f_{s,DAC}$) is directly referred to the SDM input, degrading its performance. Therefore, the clean external clock must control the DAC, whereas the comparator is controlled by the delayed clock version, as shown in Figure 4.16. The DAC clock is then used as the input of the inverter chain, which is further delayed by 3/8 T_s and inverted to generate the comparator clock. The delay of the inverter has been increased by increasing its output resistance instead of its capacitance to reduce dynamic power consumption. Since the delay of the inverter chain varies across PVT corners, a 3-bit-controlled multiplexer is used to select the comparator clock from different taps along the delay chain, as shown in Figure 4.16. The multiplexer can therefore be digitally trimmed to compensate for delay variations.

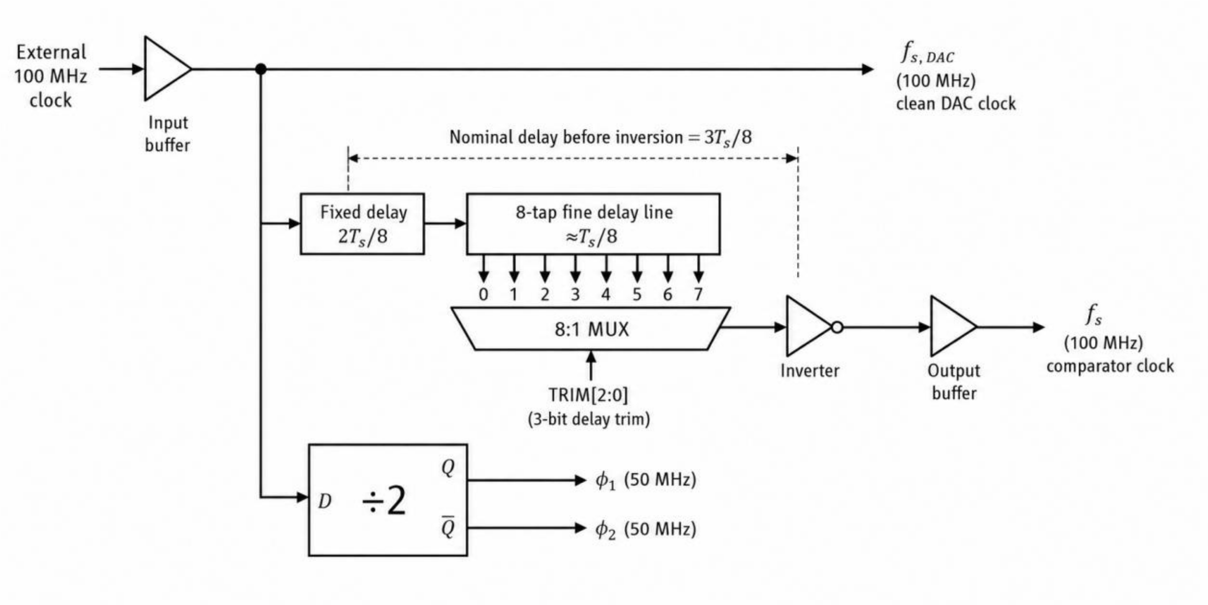


Figure 4.16 The block diagram of the clock generation circuit.

4.8. Layout

The design has been implemented in an area of 600 µm × 680 µm, as shown in Figure 4.17, with the main circuit blocks highlighted. The area is mainly dominated by the first SDM loop filter capacitors C_1 and C_2. These capacitors are implemented using MIM structures, allowing the input and DAC resistors to be placed underneath and improving the area utilization. The clock-generation circuit is placed close to the DAC D flip-flops to shorten the critical clock routing and reduce the additional delay and jitter introduced by routing parasitics.

Special attention was given to the layout of OTA1 because its matching and noise performance directly affect the overall modulator performance. The tail resistors are placed close to each other, and the bias transistors are positioned near the input-pair devices to improve their matching. The tail resistors and AC-coupling capacitors are surrounded by an N-well guard ring to reduce coupling from nearby circuitry. In addition, the chopping-clock routes are kept short and shielded to limit clock feedthrough and interference with sensitive analog nodes. Since the nominal value of the OTA tail resistor is relatively small, the routing resistance between the resistor and the OTA devices is minimized to prevent changes to the biasing of the input pair.

Unsilicided p + polysilicon resistors are used for both R_{in} and R_{DAC} because of their relatively high sheet resistance and low temperature coefficient. The voltage-dependent nonlinearity associated with the polysilicon-to-metal contact interfaces is discussed in [34]–[36]. To mitigate this effect, both resistors are implemented with the maximum permitted width of 10 µm and a multiplicity of two. The effectiveness of this approach in increasing the contact area and reducing contact-related nonlinearity while preserving the required resistance values was demonstrated in [26].

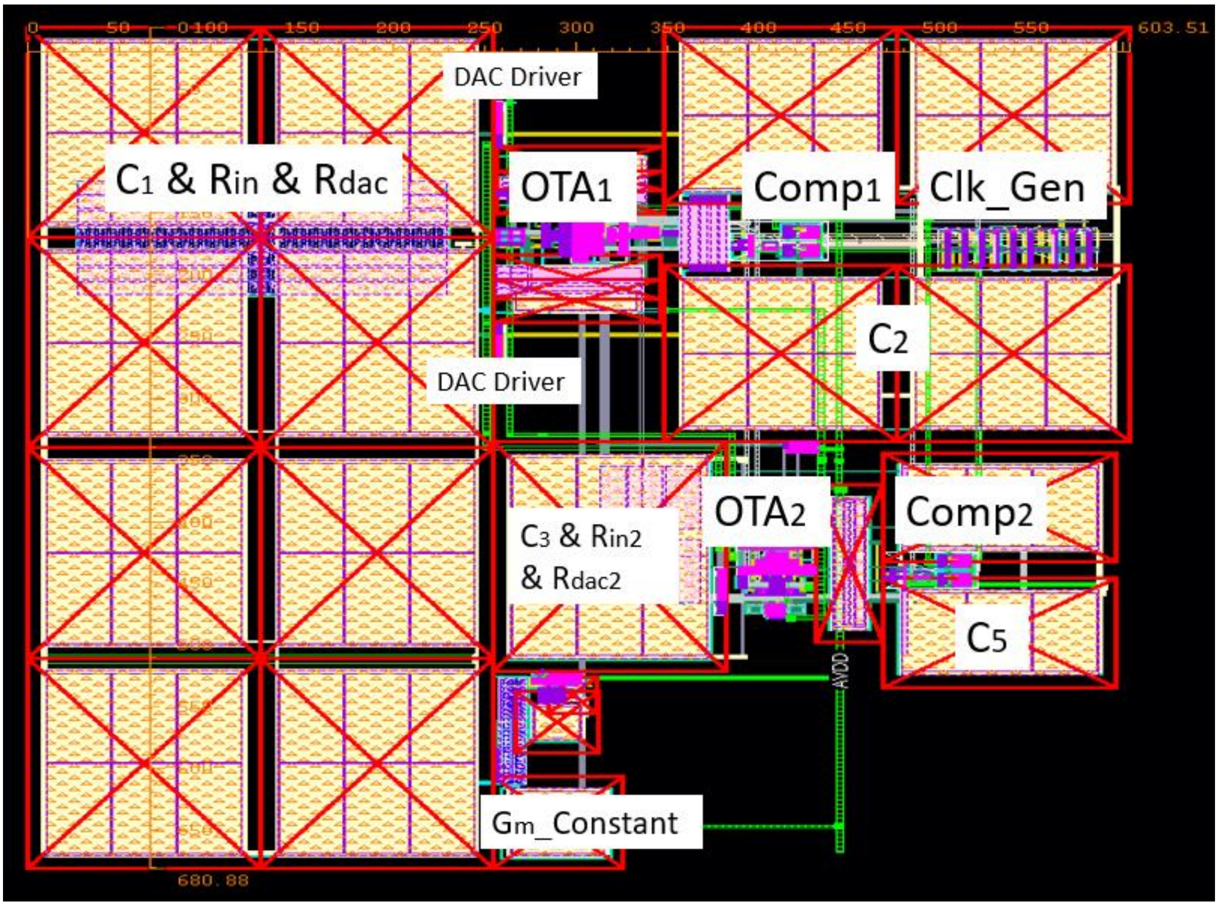


Figure 4.17 Layout of the SDM.

Chapter 5. Simulation Results

This chapter presents the simulation results for the complete design at the schematic level and after post-layout extraction. It includes the nominal performance, input-amplitude and frequency sweeps, PVT-corner behaviour, Monte Carlo results, post-layout performance, power consumption, and idle-tone behaviour.

5.1. Peak Schematic-Level Performance

The top-level schematic combines OTA1, OTA2, the two comparators, the NRZ DACs, the clock-generation circuit, and the passive components shown in Figure 2.11. The design is implemented in TSMC 65 nm CMOS and operates from a nominal 1.2 V supply. The DAC and comparator clock signals operate at fs = 100 MHz. The chopping signals $\emptyset_1$ and $\emptyset_2$ operate at fs/2. The signal bandwidth used for all top-level evaluations is f_{BW} = 195.3 kHz, corresponding to an OSR of 256. The SQNR values are taken from quantization-limited simulations that exclude circuit noise, while the SNR and SNDR values are taken from transient-noise simulations that include the stated circuit-noise sources.

Figures 5.1 and 5.2 display the schematic-level output spectra of SDM1 and the complete MASH output without and with thermal noise simulations, respectively. These simulations use a 40.4358 kHz sinusoidal input with a peak amplitude of 1.08 V. SDM1 achieves 88.99 dB SQNR, while the complete MASH achieves 110.7 dB SQNR. The second loop, therefore, improves the SQNR by 21.71 dB. When circuit noise and distortion are included, the MASH output achieves 101.31 dB SNR, −108.9 dB THD, and 100.61 dB SNDR, while the corresponding SDM1 values are 88.09 dB SNR, −70.43 dB THD, and 70.36 dB SNDR. The MASH SDM improves SNDR by 30.25 dB over SDM1 alone. The all-noise SNR of 101.31 dB and SNDR of 100.61 dB achieve the 100 dB system target used during the circuit design.

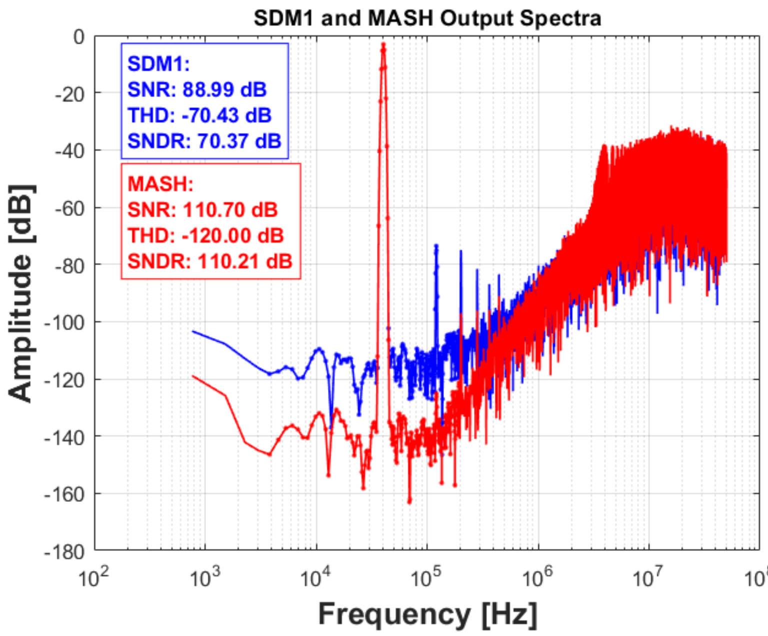


Figure 5.1 Spectrum of the SDM1(blue) and MASH(red) output bitstreams for quantization-limited simulations

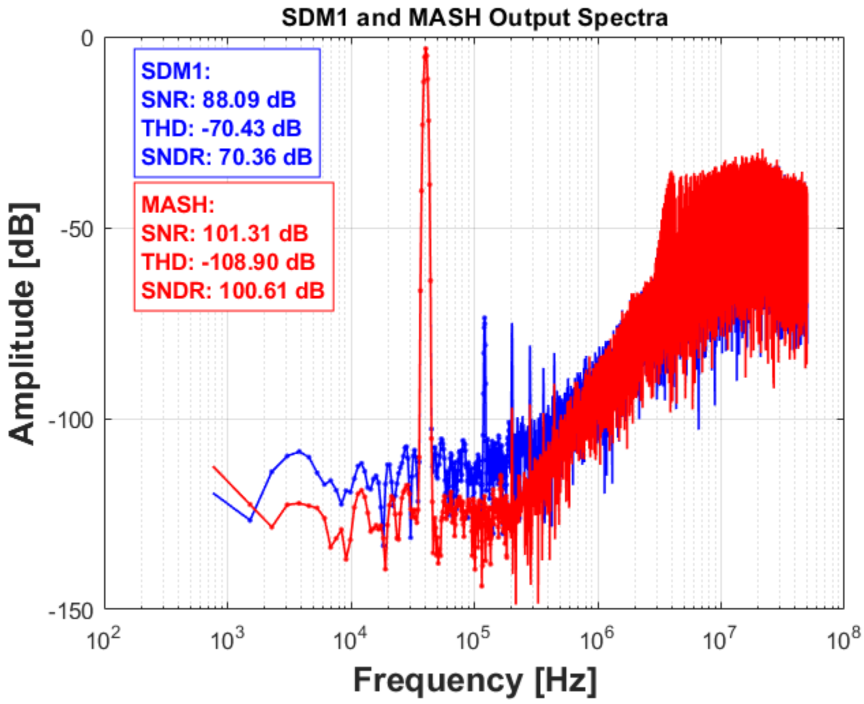


Figure 5.2 Spectrum of the SDM1(blue) and MASH(red) output bitstreams for simulations including circuit noise

5.2. Amplitude-Sweep Results and Dynamic Range

The peak SNR, peak SNDR, maximum stable amplitude (MSA), and dynamic range (DR) are determined from a sweep of the input amplitude. The amplitude of the input sinusoidal signal is swept from 1.2 µV to 1.2 V to measure the dynamic range of the SDM. The input frequency is fixed at 40.4358 kHz to include the third-order harmonic in the bandwidth. Figure 5.3 shows the simulated SNR and SNDR versus input amplitude. The amplitude sweep extends to 0 dBFS, corresponding to a peak input amplitude of 1.2 V, at which the simulated SNR is 78.83 dB. The lower limit of the DR is when the SNR equals 0 dB. With this definition, the simulated DR is 103.66 dB. The peak SNR and SNDR are 101.31 dB and 100.61 dB, respectively, at the maximum stable amplitude (MSA) of −0.92 dBFS (1.08 Vpk).

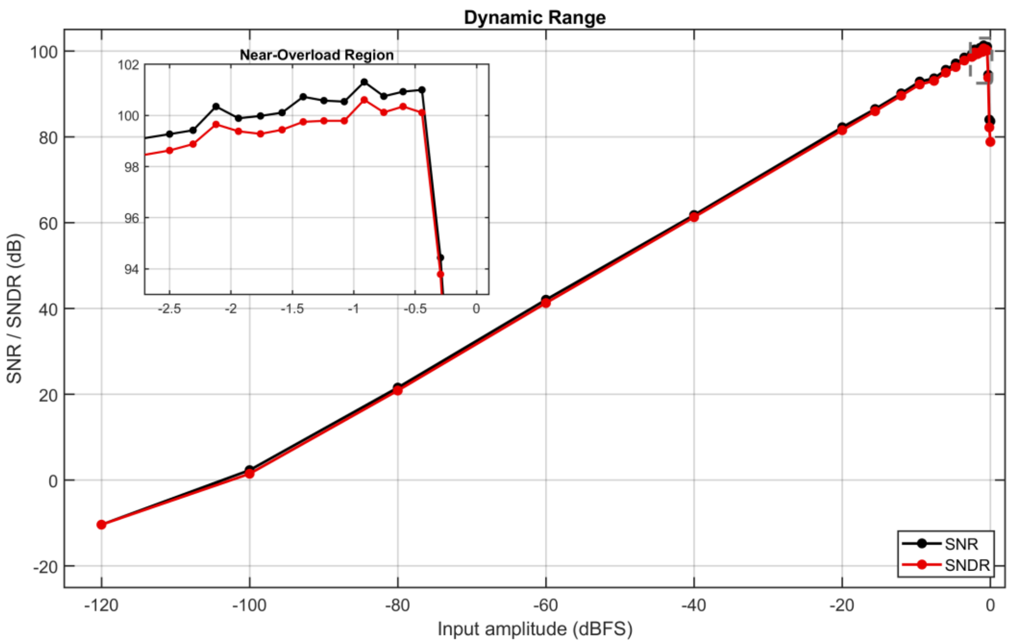


Figure 5.3 The simulated SN(D)R versus input amplitude.

5.3. Frequency-Sweep Results

The schematic frequency sweep was performed with the input amplitude fixed at 85% FS and all noise sources enabled. The sweep covers input frequencies from 8.392 kHz to 191.5 kHz. Figure 5.4 shows the SNR and SNDR of the MASH output as a function of input frequency over this range. The change in SNR is limited across the input-frequency range, changing by only 1.17 dB between the highest and lowest points of the sweep. The variation in SNDR is larger than that in SNR because the cancellation of the first-loop harmonic distortion is imperfect and frequency-dependent. As the input frequency changes, its harmonics move through regions with different cancellation accuracy, causing the residual THD at the MASH output to vary. Therefore, the lowest SNDR is expected near 65.1 kHz, where the third harmonic lies close to the upper edge of the signal band and experiences weaker cancellation. The highest SNDR in the sweep is 100.35 dB, observed at 119.78 kHz, where the SNR is 101.39 dB. The lowest SNDR is 98.4 dB at 63.32 kHz, where the SNR is 100.33 dB.

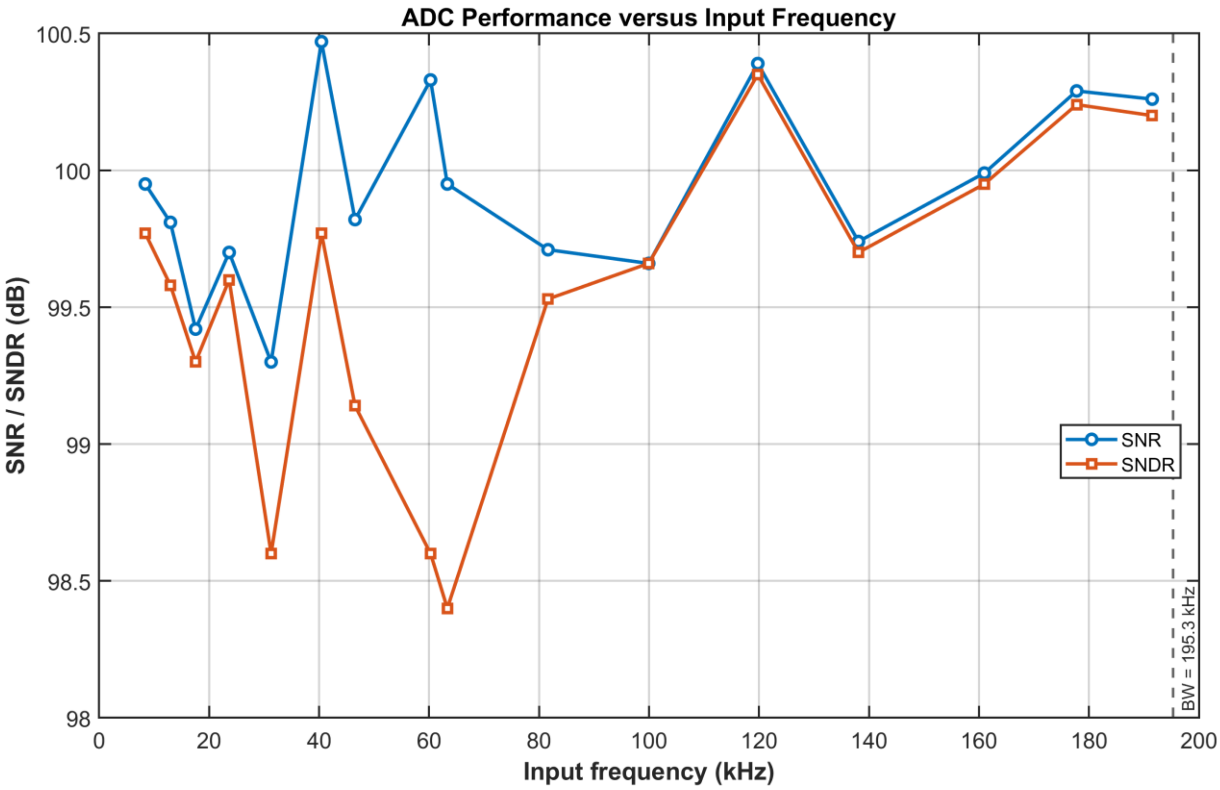


Figure 5.4 SNR and SNDR VS input frequency

5.4. PVT-Corner Simulation

The top-level design is evaluated across process, supply voltage, and temperature corners to assess its functionality and performance relative to the target. The simulated process corners are TT (typical–typical), SS (slow–slow), and FF (fast–fast). The temperature is swept across −40 °C, 27 °C, and 100 °C. An additional TT case is simulated at a supply voltage reduced by 5% from the nominal 1.2 V to 1.14 V, representing a lower supply condition. These simulations use a 1.02 Vp, 40.4358 kHz sinusoidal input signal. Figure 5.5 shows the output-bitstream spectra of the complete design with thermal noise and without trimming at nominal temperature. Table 5.1 lists the SNDR values for each simulated condition. The SNDR changes only slightly across the temperature range, indicating that the thermal-noise performance is relatively stable. The supply-voltage reduction from 1.2 V to 1.14 V reduces the SNDR by approximately 0.20 dB at room temperature and by 0.98 dB at 100 °C, which is likely related to the reduced headroom available to OTA1 at the lower supply. The performance is slightly degraded at high temperature because of the increased thermal noise, since the input-stage noise was optimized at room temperature, as mentioned in Section 3.1.

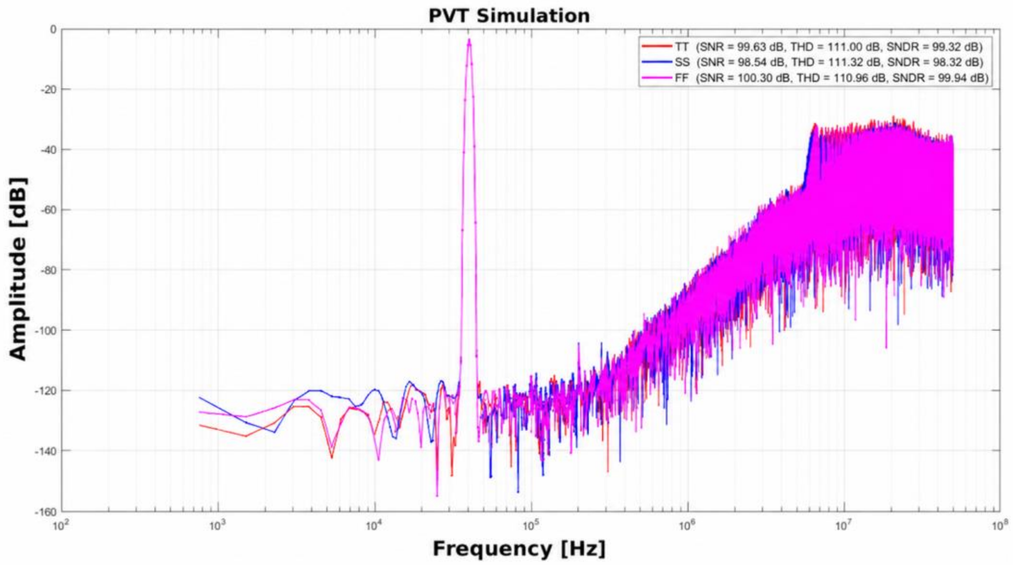


Figure 5.5 Spectrum of output bitstreams across TT, FF and SS corners at 27°C.

Table 5.1 SNDR Performance table under different PVT Corners

Corner (Supply)	$-40°C$	$27°C$	$100°C$
TT (1.2V)	100.31	99.32	98.3
TT(1.14V)	100.13	99.12	97.32
SS(1.2V)	99.08	98.32	97.9
FF(1.2V)	101.41	99.94	98.22

5.5. Monte-Carlo Analysis

Monte Carlo simulations are performed to assess the design's sensitivity to component mismatch. Figure 5.6 shows the spectrum of 20 Monte Carlo iterations. This plot shows a limited spread around the nominal value and no visibly isolated low-performing case. Figures 5.7 and 5.8, respectively, show the spread in SQNR, THD, and SNDR and the corresponding histogram. The SQNR remains around 114 dB, indicating good immunity to mismatch, consistent with the architecture discussed in Chapter 2. The data are consistent with the system-level mismatch analysis in Chapter 2, where a 50-iteration Simulink sweep with ±5% random variation yielded a mean SQNR of 117.5 dB with a standard deviation of 1.24 dB.

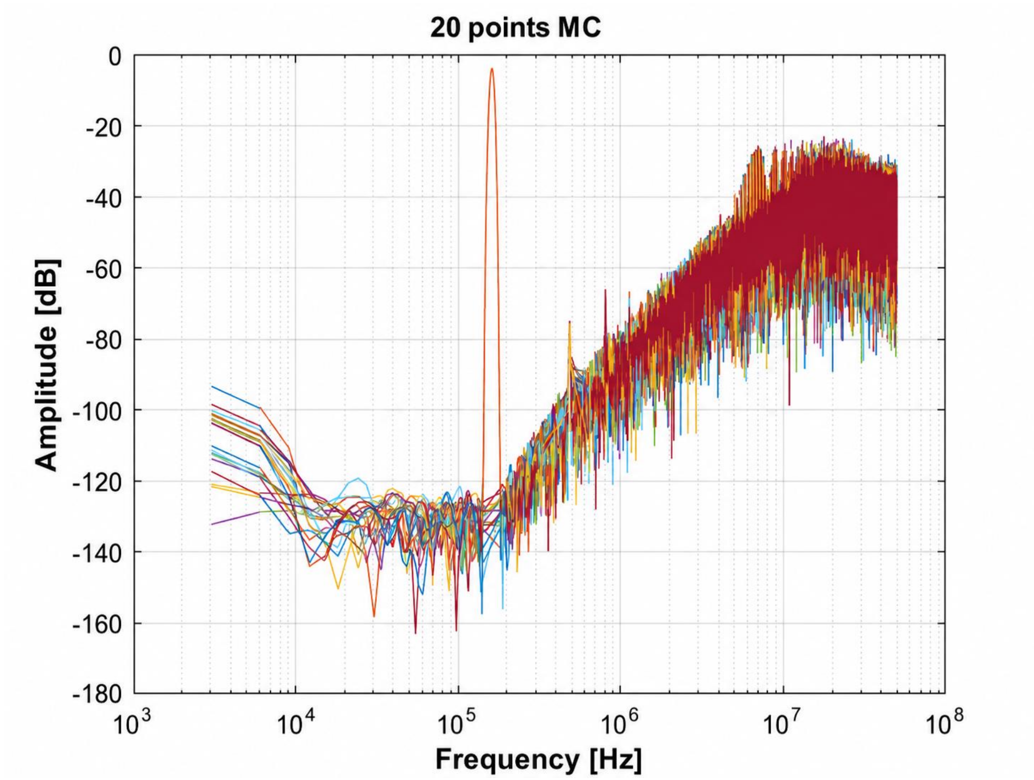


Figure 5.6 Spectrum of output bitstreams with Monte Carlo simulation.

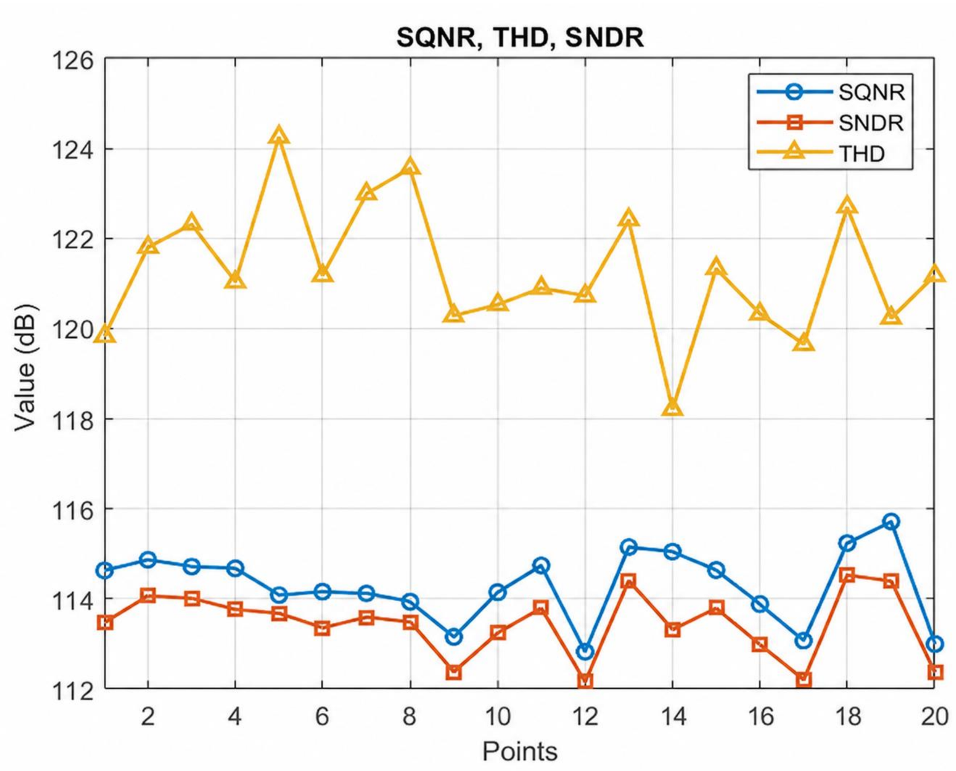


Figure 5.7 SQNR, THD and SNDR across 20 cases.

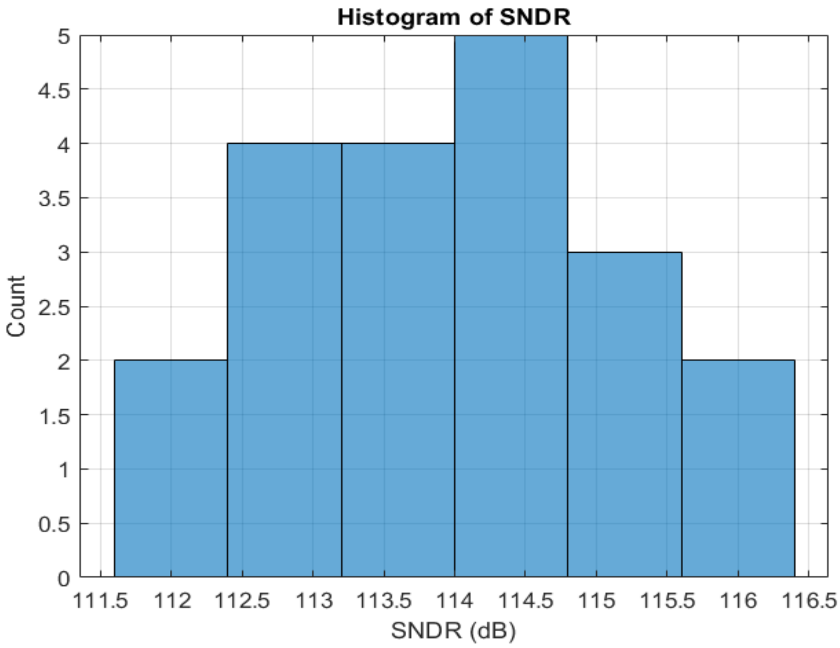


Figure 5.8 Histogram of SNDR across 20 cases.

5.6. Post-Layout Performance

Post-layout simulations are performed using an RCC parasitic-extracted netlist, which includes the parasitic resistances, capacitances, and coupling capacitances of the layout. Figures 5.9 and 5.10 show the RCC-extracted output spectra of the MASH output without and with thermal noise simulations, respectively. The complete MASH SQNR increases slightly from 110.7 dB to 110.93 dB after extraction. The quantization noise remains low compared to the thermal noise after post-layout extraction. Therefore, the complete MASH SNDR changes from 100.61 dB to 99.53 dB after extraction, with a reduction of 1.08 dB. The post-layout SNR of 100 dB achieves the system target used during the circuit design, while the SNDR of 99.53 dB is very close to the target.

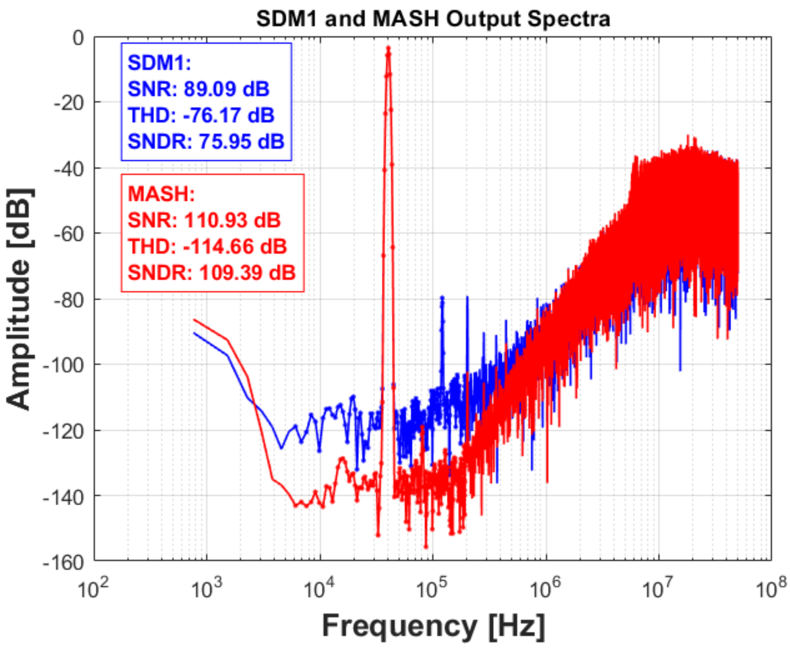


Figure 5.9 Spectrum of Output bitstreams of post-layout extraction for quantization-limited simulations

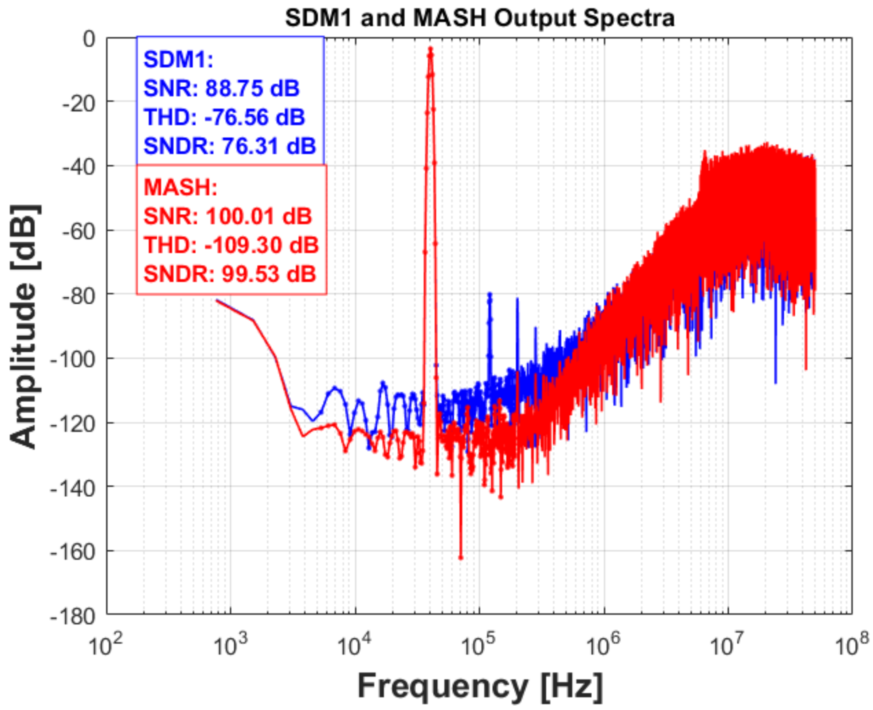


Figure 5.10 Spectrum of Output bitstreams of post-layout extraction for simulations including circuit noise

5.7. Power Consumption

The total simulated schematic-level power consumption of the complete ADC is 1093.5 µW. Figure 5.11 shows the breakdown across the main circuit blocks. OTA1 is the dominant consumer, with 37.8% of the total power. DAC1 consumes 35.1% of the total power, and OTA1 and DAC1 together account for 72.9% of the total power. This is consistent with the design strategy established in Chapter 3, where OTA1 and the first-stage DAC were identified as the blocks that must carry the largest share of the power budget in order to meet the noise and linearity specifications. The clock-generation circuit contributes 17% of the total because of its high dynamic power consumption. The remaining blocks, OTA2, DAC2, and the comparators, each contribute less than 4%. This shows that the power overhead of the second SDM loop is relatively small.

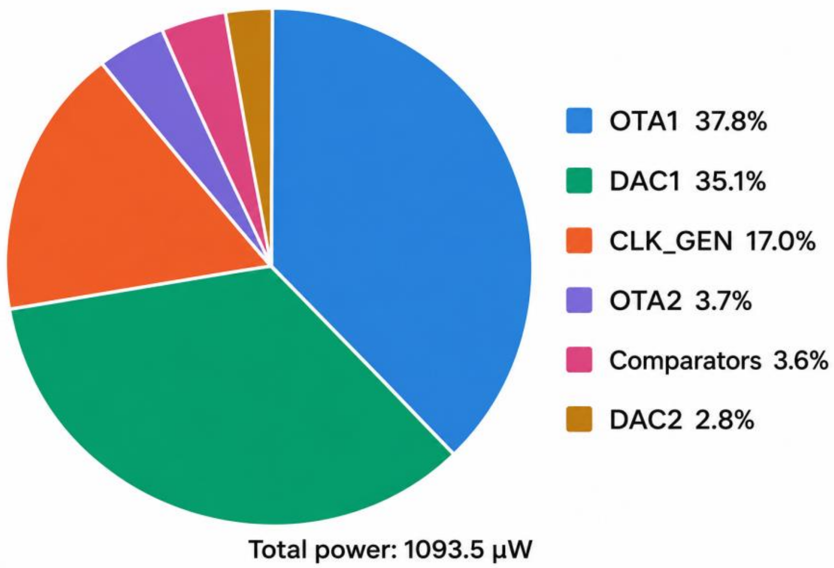


Figure 5.11 Power breakdown of the SDM.

5.8. Idle Tones

Idle tones are observed in the SDM1 output spectrum when the input of the ADC is shorted because a 1-bit quantizer is used in the loop. These idle tones are cancelled at the MASH output, as illustrated in Figure 5.12. As illustrated earlier, the MASH architecture cancels the quantization noise and harmonic distortion of the first loop, so the MASH output is mainly determined by the noise and distortion generated in the second stage. Idle tones are less pronounced in SDM2 because its input is the first-stage residue, which behaves like a dithered signal and reduces the periodic quantizer sequences.

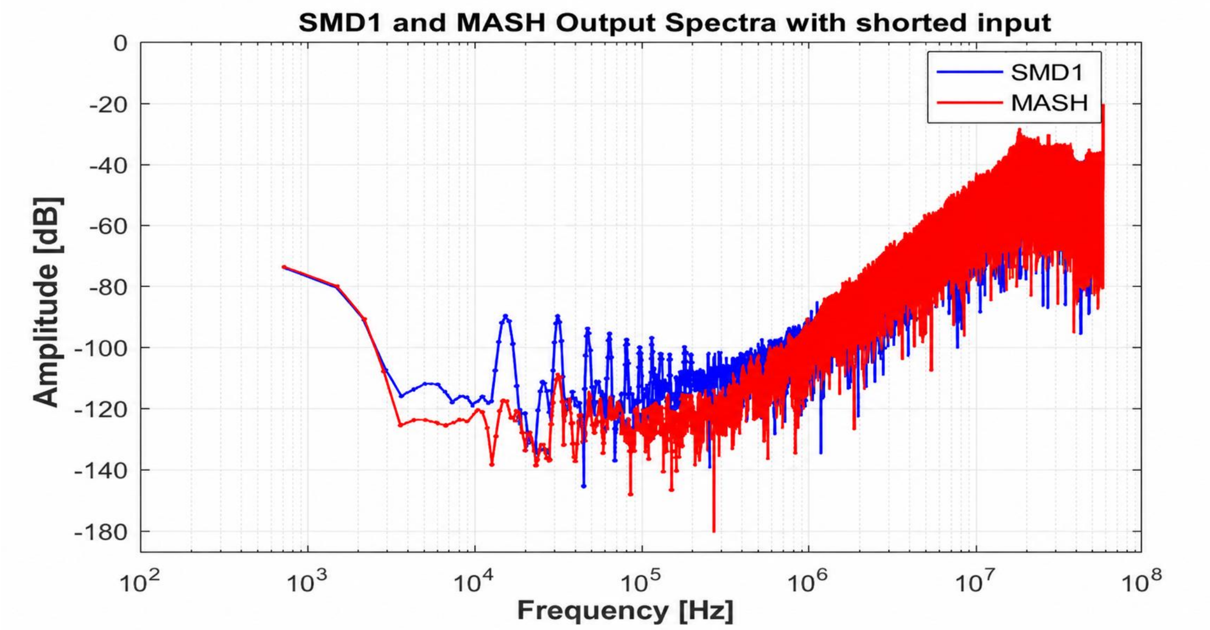


Figure 5.12 Behaviour of idle tones with shorted input for SDM1 and MASH outputs.

Chapter 6. Conclusion and Future Work

6.1. Conclusion

This thesis presents a high-resolution passive-input MASH CTSDM for a signal bandwidth around 200 kHz. The design was implemented in a 65 nm TSMC CMOS process, operates from a 1.2 V supply, and consumes 1.094 mW at the schematic level. Schematic-level simulations achieve a peak SNDR of 100.61 dB and a dynamic range of 103.66 dB, corresponding to FoM_{SNDR} and FoM_{DR} values of 183.1 dB and 186.3 dB, respectively. RCC-extracted simulations achieve an SNR of 100 dB and an SNDR of 99.53 dB, indicating that the target performance is largely retained after parasitic extraction. PVT-corner and Monte Carlo simulations also indicate robust operation under the evaluated process, supply, temperature, and component variations without a dedicated calibration loop.

Overall, the results indicate that the selected dual-loop passive-input concept, together with the circuit-level modifications developed in this work, can meet the target resolution and energy-efficiency specifications at the schematic level and after parasitic extraction. The main findings supporting this conclusion are as follows:

1. **Suppression of the first-stage quantization noise without complex digital cancellation:** Most of the quantization-noise cancellation is implemented in the analog path, while the digital path requires only a fixed attenuation factor that can be realized using a shift register. The SQNR increases from 88.99 dB for SDM1 to 110.7 dB for the complete MASH, corresponding to an improvement of 21.71 dB. This result demonstrates that the first-stage quantization noise can be strongly suppressed without a complex digital cancellation filter or a dedicated calibration loop.
2. **Preservation of input range and robustness with limited second-stage overhead:** The design preserves a maximum stable input amplitude of 1.08 V, corresponding to approximately $0.9V_{ref}$, and achieves a simulated dynamic range of 103.66 dB. A 50-run system-level analysis with random ±5% variations in R, C, and G_m gives a mean MASH SQNR of 117.5 dB with a standard deviation of 1.24 dB. Circuit-level Monte Carlo simulations also show a limited spread, with the SQNR remaining around 114 dB. In addition, the second-stage circuitry accounts for only 8.3% of the total simulated power, indicating that it provides good quantization-noise suppression with limited power overhead.
3. **Energy efficiency and dynamic range relative to active-integrator-based designs:** The achieved FoM_{SNDR} of 183.1 dB exceeds the original target of 181 dB, while the simulated dynamic range reaches 103.66 dB. These results show that a passive-input MASH architecture can achieve energy-efficiency and dynamic-range performance comparable to or exceeding that of active-integrator-based designs. This supports the feasibility of combining passive-input operation with high resolution and competitive energy efficiency.

Table 6.1 compares the simulated performance of this work with the measured performance of selected state-of-the-art ADCs.

Table 6.1 Simulated performance of this work compared with selected state-of-the-art ADCs.

	This work	Nowacki [6] ISSCC'16	Gao [7] ISSCC'25	Lozada [8] VLSI'24	Yoon [1] VLSI'25	Xing [9] ISSCC'26
Architecture	CT	DT	DT	CT	CT	CT
Tech (nm)	65	65	55	28	28	28

Supply (V)	1.2	1	1.2	1.1	1	1
Power (uW)	1094	1570	307	380	392	400
Fs (MHz)	100	1000	20	12.8	80 (coarse), 20 (fine)	50
BW (kHz)	195.3	10000	156.25	200	250	250
OSR	256	50	64	32	160	100
SNDR (dB)	100.6	72.2	93.3	89	91.2	98.5[a]/ 93.9[b]
DR (dB)	103.7	77	95	92.1	92.7	99.7
FoM_{SNDR} (dB)	183.1	170.2	180.4	176.2	179.2	186.5[a]/181.9[b]
FoM_{DR} (dB)	186.3	175	182.1	179.3	180.7	187.8

[a] Measured at f_{in} = 12.3 kHz. [b] Measured at f_{in} = 202.3 kHz.

6.2. Future Work

6.2.1. Silicon Measurement and Experimental Validation

Silicon measurements should verify the SNR, SNDR, SQNR, dynamic range, maximum stable input amplitude, power consumption, and analog-cancellation accuracy across samples and operating conditions. They should also assess PVT robustness, clock-jitter sensitivity, and idle-tone behavior.

6.2.2. PVT-Robust First-Stage Amplifier

Cancellation accuracy depends on matching the digital attenuation to the first-stage gain A_1. Although R_{bias} trimming can compensate for gain variations, a first-stage amplifier with gain variation limited to approximately 1% across PVT corners could eliminate the need for trimming and enable calibration-free design.

6.2.3. Switched-Capacitor DAC for Improved Clock-Jitter Robustness

Due to the high sampling frequency and high SNR specification, our design is sensitive to clock jitter. Therefore, the switched-capacitor (SC) DAC is attractive due to its excellent jitter robustness. The SC DAC is robust to jitter because it has an exponentially decaying pulse shape, which has a low amplitude at the end of the clock cycle. Therefore, the induced charge difference due to clock jitter is minimized. However, the SR DAC was selected for this design because of time constraints. Future work should compare an SC DAC with the implemented SR DAC to determine how the DAC architecture affects the required slew rate, settling performance, linearity, and power consumption of OTA_1.

6.2.4. Higher-Bandwidth and Lower-Resolution Operation

A relaxed SNR target would increase the allowable input-referred noise budget, permitting a larger R_{in} and therefore a smaller C_1 for the same bandwidth. This is important because increasing the bandwidth while maintaining the same SNR requires a smaller R_{in}. Relaxing the SNR target would therefore reduce the first-stage capacitor area. It would also allow a lower G_{m1} and a larger R_2. The larger R_2 could reduce the required C_2 area and increase A_1. Together, these changes would improve power and area efficiency, relax the circuit-noise and clock-jitter requirements, and make the architecture more suitable for higher-bandwidth applications.

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