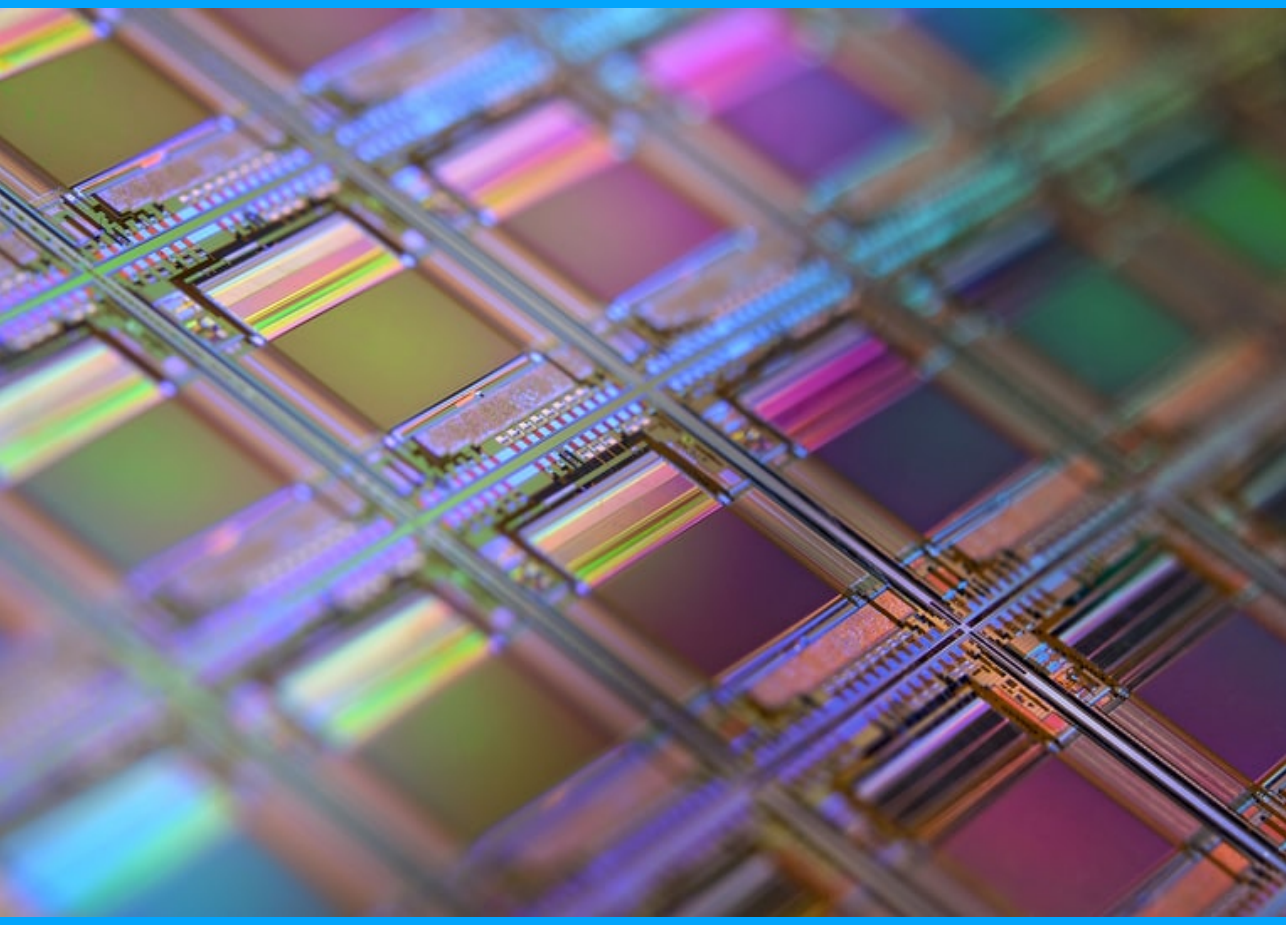
THERMAL ANALYSIS OF CU PILLARS IN FLIP-CHIP PACKAGES

Denver Xavier Desouza



TU Delft

THERMAL ANALYSIS OF CU PILLARS IN FLIP-CHIP PACKAGES

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Science is a wonderful thing
if one does not have to earn one's living at it.

Albert Einstein

ABSTRACT

THERMAL management is a very crucial step to ensure the reliability of Integrated Circuits (IC)s. The increase in power density has resulted in the formation of multiple, high-intensity, and non-uniform hotspots. This has not only affected the lifetime but also the performance of several devices. Optimization of the package design and layout are the methods investigated to solve this problem. In flip-chip packaging, each IC product varies with respect to power densities, die area, pin-count, laminate and PCB layers, etc. It is therefore important in understanding how the arrangement and geometry of each layer (in particular the interconnect layer) impacts the overall thermal management.

In this study, the different parameters that make a Cu pillar interconnect are analyzed. The variation of these parameters is also carried out using Finite Element Model (FEM) simulations and their influence on junction temperatures.

The second part of the thesis looks at new designs/dimensions for Cu pillar interconnect and addresses the thermal as well as mechanical comparisons with verified geometries. For this Ansys mechanical and homogeneous modeling are utilized for stress and warpage comparisons.

The third part of the thesis discusses a literature gap. Research papers have only spoken about the effect of Cu pillars under a uniform power source. In reality, there are non-uniform power densities that cause hotspots of different sizes and intensities. A set of experiments analyzes the placement of pillars with respect to hotspot location and their impact on junction temperature. These experiments provide a better understanding to the designer for pillar placements during the layout stage.

Finally a small study on the thermal benefits of Cu to Cu interconnect is demonstrated as the future for flip-chip packages. A study on the thermal benefits of filler materials affecting underfill's thermal performances is also carried out.

ACKNOWLEDGEMENTS

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I would like to also thank my family and parents in particular for the sacrifices made in funding my Msc. studies. This thesis is dedicated to them.

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ACRONYMS

CFD Computational Fluid Dynamics

CTE Coefficient of Thermal Expansion

EM Electromigration

FEM Finite Element Model

IC Integrated Circuits

IMC Inter Metallic Compounds

PCB Printed Circuit Board

PR Photo Resist

SiP System in Package

TO Topological Optimization

UBM Under Bump Metallization

WLP Wafer Level Packages

1

INTRODUCTION

In the book of life, the answers aren't in the back

Charlie Brown

IN this chapter the focus is on introducing the history of Cu pillars and the role they play in flip-chip packages. The next section highlights the advantages that Cu pillar interconnect technology has over its predecessor. The third section deals with the motivation behind the thesis and the reasons for going into a thermal analysis. The last section looks through the outline of the experiments and the questions that the thesis will answer.

1.1. IC PACKAGES OVERVIEW

The cost, form factor, and the performance have become the key factors in selecting the right package for a particular IC [1]. This also depends on the application where these ICs are used, for example portable electronics, space electronics, medical appliances, automotive chips, etc. The two commonly talked about packages in the Wafer Level Packages (WLP) are the wire-bond and flip-chip WLPs.

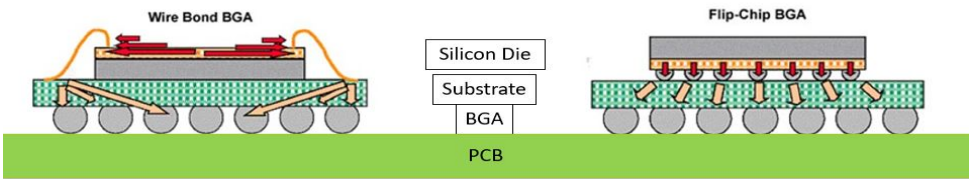


Figure 1.1: Wire Bond and Flip-Chip Package [2]

Figure 1.1 shows the wire-bond and flip-chip packages. From this figure, it can be seen that wire-bonds have active components (orange) facing away from the die. They use wire-bonds for connection to the substrate. On the contrary, flip chips have the active components of the die facing the substrate. Hence the name "Flip-chip". The two packages have very different processing steps. In the case of the wire-bond packages, there is a need for a wire bonder to attach the wire-bonds. Flip chips which were invented by IBM in the 1960s requires flux for the interconnect attachments as well as underfill encapsulation for the protection [1]. Table 1.1 shows the different steps for wire-bond and flip-chip packages.

	Wire-Bond Package	Flip-Chip Package
Step 1	Wafer	Wafer
Step 2	Dice	Wafer Bumping
Step 3	Die Attach	Dice
Step 4	Curing	Flux
Step 5	Wire Bonding	Reflow
Step 6	Encapsulate	Underfill Encapsulation
Step 7	BGA Attach	BGA Attach
Step 8	Marking	Marking
Step 9	Testing	Testing

Table 1.1: Wire-bond and Flip-Chip processing steps [1]

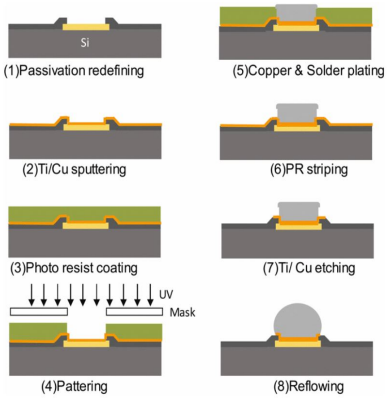
Advantages of flip-chip technology:

- **Higher Package Density**: Flip-chip technology makes use of the entire surface area of the die for pin placement and routing. This allows the designer plenty of room for routing of high-density I/O products. This is a limiting factor for the wire-bond packages as they only use the periphery sides of the die for interconnects.
- **Reduced Substrate Area**: The area of the substrate in flip-chip technology is reduced as compared to the wire-bond packages. This is because the interconnections are directly attached on top of the substrate/laminate and require no wire-bonds.
- **Speed**: The flip-chip technology boasts of better electrical performances due to the shorter interconnects and much wider pins. This helps in reducing the inductance and thereby increasing the speed of currents flowing through. Thus the signal integrity is better for higher frequency applications.
- **Reliable**: In terms of interconnects, flip chips are more reliable and less susceptible to fatigue and mechanical failures like fractures as compared to the wire-bonds.
- **Low Signal disturbances**: The benefit of flip chips is for instance interference of signals to/from the chip. There are no bond wires (which can pick up disturbances/noise) and less IR drop due to the short distance from the substrate to the chip.

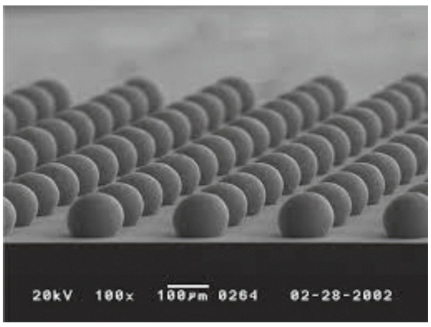
- **Cost**: The flip-chip technology today is matured and manufactured on a large scale. It is therefore becoming cost-effective. Comparing the costs of the two WLPs varies with respect to the application.

Flip-Chip Interconnects

- **C4 Bumps**: The first interconnections in conventional flip-chip packages is the controlled collapse chip connection (C4) bumps. These are bumps made of Pb/Sn or Pb-free solder. They are called controlled collapsible because the stand-off height is maintained by the solder volume [3]. The processing steps include passivation layer formation, Under Bump Metallization (UBM) sputtering, Photo Resist (PR) coating, PR strip, etching, and solder re-flow. Figure 1.2a shows the fabrication processes of C4 fabrication and Figure 1.2b shows SEM view of C4 bumps [3].



(a) C4 process steps [3]



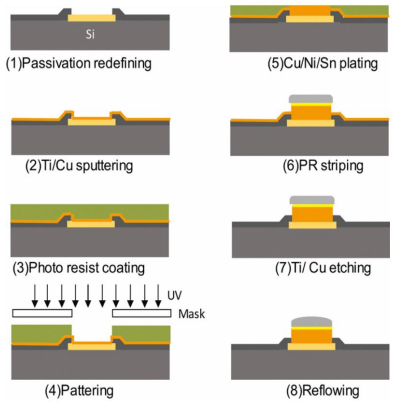
(b) SEM image of C4 bumps with 250µm pitch [3]

Figure 1.2: C4 process and bumps [3]

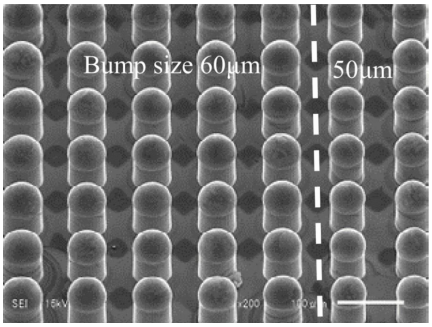
- **C2 Pillars**: With the technology node going down and the need for higher density I/O pins, reducing bump pitch becomes a constraint for C4 [3]. A solution to this was the use of Cu pillars discovered by IBM in 2001. These copper pillars consisted of a thin Cu post and a tiny volume of solder cap. This allows the fabrication of interconnects with pitches as low as 100 µm [4]. The processes of C2 are similar to that of its predecessor. Figure 1.3 shows the processes and pillar designs of C2 interconnect [3].

Advantages of C2 (Cu Pillars) over C4 bumps:

- **Ultrafine pitch**: C2 and micro copper pillars have been documented to have pitches down to 50 µm. This is useful for high-density pin counts.
- **Lower Bump geometries**: This is because there is only a tiny volume of solder being used as a cap. This enables C2 interconnects to have narrow pitches and avoid the problem of solder bridging which is dominant in narrow C4 pitches.



(a) C2 process steps [3]



(b) SEM image of C2 pillars (50/60µm diameter) with 100µm pitch [3]

Figure 1.3: C2 process and bumps [3]

- **Cost reduction**: This technology has been fabricated on a large scale basis by many semiconductor industries like TSMC, Global Foundries, Samsung, etc.
- **Reduced signal impedance**: Copper has lower impedance than solder and therefore improved electrical performances.
- **Better thermal conductivity**: Cu has a thermal conductivity of ≈ 385 W/mK and this is roughly 7 times higher than solder's conductivity (≈ 60 W/mK)
- **Yield strength**: Cu pillars have a higher Young's modulus as compared to solder. Therefore it possesses a higher yield strength [5].

1.2. MOTIVATION

The semiconductor industry has benefited from the progress made under Moore's Law. Moore's law states that the number of transistors doubles every 2 years. While this trend has resulted in high performance and more accurate circuits with faster speeds, it has its own pitfalls. By increasing the number of transistors on a given die area it leads to increasing the power density [6]. Figure 1.4 shows the increase in the power density of the Intel microprocessors. From Pentium IV onwards the power density expressed in Watts/cm^2 can be compared to power densities produced by a hot plate, a nuclear reactor, and even comparable to that of a nozzle of a rocket [7]. This power density trend has an impact on the thermal management of the IC. There is also a reduction of the feature size, area, transistor size, and power consumed by these transistors. But since there is a drastic increase in the number of transistors, the total power density has also increased. The amount of heat generated from such complex circuits leads to reliability issues, poor life-time, and performance issues. It is estimated that almost half of the failures in ICs are down to temperature related issues [6].

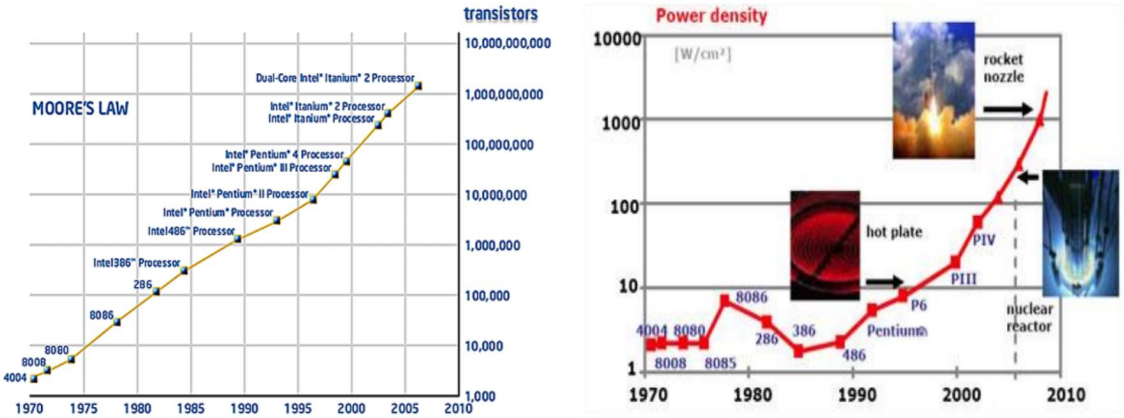


Figure 1.4: Power and density trend-lines [7]

By increasing the number of transistors, the number of electrons in the ultra-thin silicon has also rapidly increased. This causes the scattering of photons away by these electrons. Ultimately leading to a reduction of heat removal by the photons [8, 9]. The junction temperature has been affected by this thermal mismanagement. High junction temperatures cause overheating and damage to the silicon die. This temperature increase also leads to electro-migration failure, which is the transport of metal atoms because of electron flow in the package. This results in the formation of voids and an increase in thermal resistance leading to circuit failure. Another problem faced is the non-uniformity of the temperature [10]. This can lead to performance degradation (due to temperature drift) of circuitry and reliability issues. For example, the temperature runaway can become a problem (more heat will make the design faster, and will cause more leakage currents, which causes again more power, etc. until the device breaks due to over-temperature). In IC packages different materials are used and this means different Coefficient of Thermal Expansion (CTE) [11]. This mismatch can cause unwanted stresses to the packages like delamination when subjected to thermal stress. Harsh environmental conditions and fluctuating weather conditions can lead to the breakdown of electronic components [8]. The repeated heating and cooling of ICs possess a danger of repeated fatigue cycles thus leading to the failure of the package. The International Technology Roadmap for Semiconductors (ITRS) Council, therefore, projects the junction temperature for every technology node to avoid reliability issues [12].

There have been advancements made in both materials and package-level design to address the thermal issues. In terms of materials, there has been an investigation into materials that possess high thermal conductivity, low thermal resistance, matching CTE, etc., and combined to the package design. The shift to flip-chip IC fabrication, replacing the traditional solder bumps with Copper Pillar thermal bumps, etc. have had a positive impact on the regulation of heat flow in the ICs. There is also a need to model these designs as accurately as possible on simulation software like Ansys RedHawk, FloTherm, etc. This can provide a better understanding of how the actual model behaves and noting

any design problems beforehand. This would not only save time and money but also become the basis for redesigning the thermal management solution.

1.3. THESIS OUTLINE

The thesis focuses on the benefits of having Cu pillars as interconnects for flip-chip packages in order to have better thermal management. This work relies heavily on the use of Computational Fluid Dynamics (CFD) FEM simulation tools such as Siemens Flotherm. By this thesis work, we look at answering the following questions:

- ***How to characterize and quantify heat removal by Cu pillars?***
- ***What does the effect of pillar geometry and pillar density add to the overall thermal analysis?***
- ***How does the addition of novel designs compare to existing designs thermally and mechanically?***
- ***What is the thermal effect of pillar placement with respect to the hot spot power and area?***
- ***What is the future for Cu pillars and the neighboring underfill?***

1.4. REPORT LAYOUT

Chapter 2 discusses the literature survey of Cu pillars. The first section explains the process of heat flow in IC packages. The different patents of Cu pillars are then addressed in the following section. The different layers that are involved in the pillar design are also elaborated on. Literature on topics such as the characterization of heat removal via pillars/bumps, the thermal benefit of having pillars/bumps are also summarized. Finally, a conclusion on the reliability issues and various failure mechanisms caused by the addition of Cu pillars.

Chapter 3 describes the simulation environment and the different simulation experiments. The software tool which is used and its features. It also explains the test vehicle setup and the different components used. Tests on the stability of the model are also carried out and finally, the various boundary conditions are addressed. It also answers the scientific questions raised through missing literature work.

Finally, Chapter 4 concludes with a summary of the results obtained. This chapter also talks about the future scope and projects that will be carried out beyond the thesis.

2

LITERATURE STUDY

2.1. HEAT FLOW IN IC PACKAGES

2.1.1. CONDUCTION

This is the most common and fastest mode of heat transfer from on-chip. The basic principles of conduction can be expressed as the equivalent in the electrical domain. This is an easier approach to understanding the thermal domain. Both domains have a "through" and an "across" variable as shown in figure 2.1 also a tabular comparison is shown below in Figure 2.1.

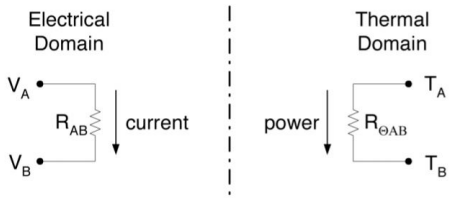


Figure 2.1: Fundamental Relationships in the Electrical and Thermal Domains [6]

Domains	Electrical Domain			Thermal Domain		
	Variable	Symbol	Units	Variable	Symbol	Units
Through Variable	Current	I	Amperes	Power or Heat Flux	P_D	Watts
Across Variable	Voltage	V	Volts	Temperature	T	°C
Resistance	Electrical Resistance	R	Ohms	Thermal Resistance	$R_{\theta AB}$	°C/W
Capacitance	Electrical Capacitance	C	Farads	Thermal Capacitance	C_θ	J/°C
Ohm's law	$\Delta V_{AB} = V_A - V_B = I.R_{AB}$ (2.1)			$\Delta T_{AB} = T_A - T_B = P_D.R_{\theta AB}$ (2.2) (derived from Fourier's Law)		

Table 2.1: Electrical and Thermal Domain Variables [13]

For instance, the current is the through variable in the electrical domain, and in the thermal domain, the power is the through variable. Similarly for the voltage and temperatures in the across variables. For both domains, resistance can be defined as the parameter which obstructs the flow in the through variable. Thus both domains have the same foundation and possess their own "Ohm's Law" [13].

2.1.2. CONVECTION AND RADIATION

In the above sections, heat flow was done mainly through conduction. The other two mechanisms that are responsible for heat flow are convection and radiation. These are dominant heat flows at the package to air/fluid interface [13].

Radiation and convection are more complicated than the conduction mechanism of heat transfer. For example in convection occurs when there is solid to liquid contact at different temperatures. The heat transfer rate is then dependent on the fluids buoyancy, specific heat capacity, density, viscosity, and fluid-fluid interface. Other factors include its surface area and the orientation, and shape. A simplistic model for the convective behavior can be written as:

$$q = k.A.\Delta T \tag{2.3}$$

where:

q=	heat transfer per second [J/s]
k=	convective heat transfer coefficient [$Wm^{-2}°C$]
A=	heat transfer area [m^2]
ΔT=	temperature difference [°C]

Radiation is a heat transfer process by emission of electromagnetic waves. The heat transfer via radiation is governed by "Gray Body" radiation which is:

$$q = \epsilon.\sigma.A.(T_h^4 - T_c^4) \tag{2.4}$$

where:

q=	heat transfer per second [J/s]
ϵ=	emissivity of object
σ=	Stefan-Boltzman constant =$6.67.10^{-8}$ [$Wm^{-2}K^{-4}$]
A=	heat transfer area [m^2]
T_h=	hot body temperature [K or °C]
T_c=	cold body temperature [K or °C]

2.2. CU PILLAR BUMP PATENTS

The first Cu pillar design was done by IBM in 2001. The design consisted of two parts: the metal post and a Tin solder [14, 15]. The melting temperature of the solder was 20 ° C lower than that of the Cu to ensure the stand-off height [14]. IBM named this pillar design as metal post solder chip connection (MPS-C2) (See Figure 2.2).

Francessca Tung from Advanced Materials Packaging (APS) had quantified the design in terms of pillar height. She had the minimum height for the post to be 55 µm and the overall design to have a height of 120 µm [15, 16].

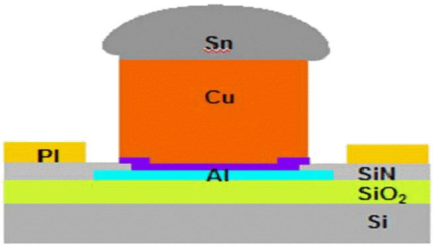
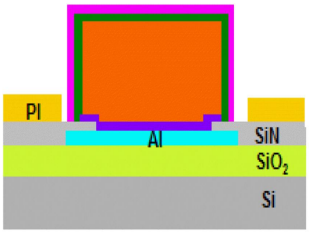
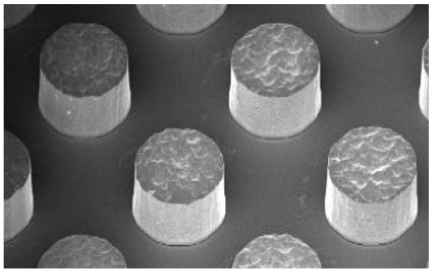


Figure 2.2: IBM's MPS-C2 [14, 15]

In 2007, Intel added a diffusion layer and an external wetting layer to the metal post [15, 17]. The solder would then be placed on top of this structure. In 2006, Intel published the integration of Cu on top of the die, and this was the first step of flip-chip interconnects with Cu post (See Figure 2.3). This design had a pitch of 175 µm [18].



(a) Intel's Cu post patent [15, 17]



(b) SEM image of Intel's design [18]

Figure 2.3: Intel Pillar Design [17, 18]

TSMC's design is similar to that of IBM's but uses an elongated Cu pillar structure as the base [4] (See Figure 2.4). For the Cu pillar height to solder height, it is done in the ratio of 2:1*.

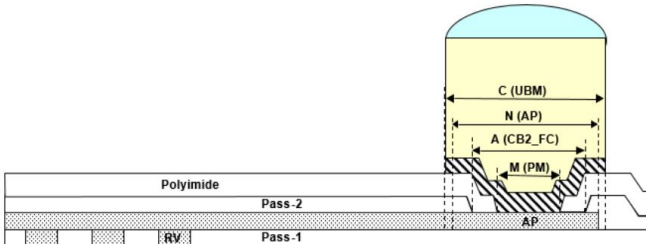


Figure 2.4: TSMC elongated pillar design [4]

* For NXP employees-refer TSMC Cu pillar design rules for the sizing numbers [4]

2.3. CU PILLAR LAYERS

Cu pillars come in different sizes depending on the process capabilities of the manufacturer. But the layer stack-up remains the same. As mentioned in the previous section, most pillar designs are in line with IBM's MPS-C2. Figure 2.5 shows each layer and Table 2.2 states their purpose in the Cu pillar design.

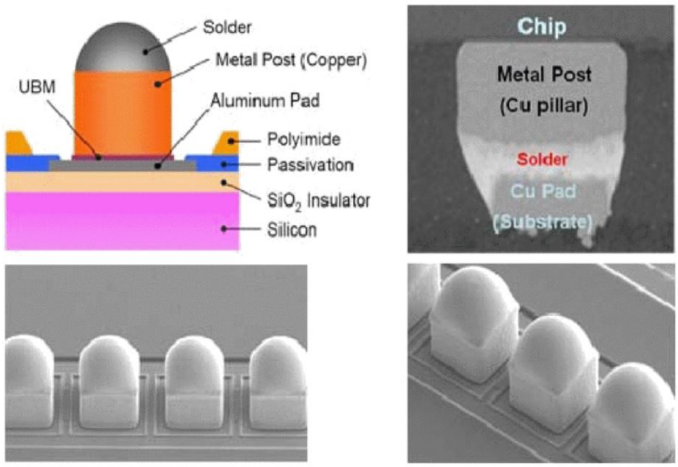


Figure 2.5: Layers in Cu pillar design [15]

Layer	Purpose
Passivation	To provide protection to the active components on the die.
Polyimide	This layer is used as a buffer for mechanical stresses. It possesses good adhesive properties and also acts as an insulator.
Aluminum pad	To route the pillar to the respective signals.
UBM	The electrical connection between die and pillar.
Metal Post	Cu pillar for the signals to flow from the substrate to die and vice/versa.
Solder	To connect the pillar to the substrate/laminate when soldered. Usually, eutectic lead-free solder is used.

Table 2.2: Layers and their purpose [19]

2.4. CHARACTERIZATION OF HEAT REMOVAL

R_{th} (Thermal Resistance) is the principal index that represents the heat removal capability of pillars and bumps [20]. Xianging Lu et al. [20] created a FEM schematic of die and substrate and used solder balls (C4) as the interconnect (See Figure 2.6).

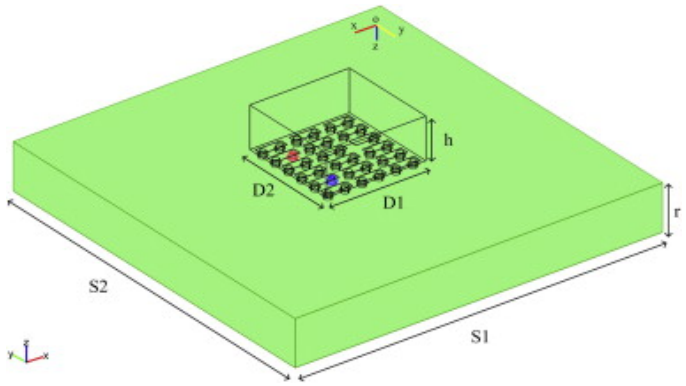


Figure 2.6: Model of flip-chip [20]

Since these bumps are embedded in the structure, heat flow in bumps is by conduction. We can use the Fourier Diffusion equation for heat through conduction as follows:

$$\frac{\partial T}{\partial t} = \frac{k}{\rho c_p}\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \frac{Q}{\rho c_p} \tag{2.5}$$

where:

T= Temperature as a function in the x,y,z and t (time) [K]
k= Thermal conductivity [W/m.K]
ρ= Density [Kg/m ^{3}]
c $_p$= Specific heat capacity[J.kg^{-1}.K^{-1}]
Q= Power density [W/m^3]

Let P_i be the power removal of the *ith* bump and the bump is at the area S_i [20]. The boundary conditions for the upper and lower sides of the die can be written as:

$$\left.\frac{\partial T}{\partial z}\right|_{z=h} = \begin{cases} \frac{P_i(t)}{k_d S_i} & \text{if } (x,y) \in S_i \\ 0 & \text{else} \end{cases} \tag{2.6}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0} = -\frac{\alpha}{k_d}\left(T_{\text{top}} - T_{\text{amb}}\right) \tag{2.7}$$

where:

T_{top}= Ambient Temperature [K]
T_{amb}= Temperature on the top boundary [K]
α= Heat transfer co-efficient to the environment [W.m^{-2}.°K]
k_d = Thermal conductivity of the die [W/m.K]

This calculation assumes that heat propagation along the z-direction. The lateral heat flow is ignored. The same set of boundary conditions can be applied to each layer. Another way of representing Fourier's diffusion in the z-direction is by Ohm's law:

$$R_{\text{th}} = \frac{T_1 - T_2}{q} = \frac{\Delta z}{kA} \tag{2.8}$$

where:

T_1= Temperature at surface 1 [K]
T_2= Temperature at surface 2 [K]
q= Power [W]
R_{th} = Thermal resistance [K/W]
Δz= Height of the bump [m]

Yang Liu et al. [21] also used the same method for thermal analysis of Cu pillars in flexible LEDs (See Figure 2.7).

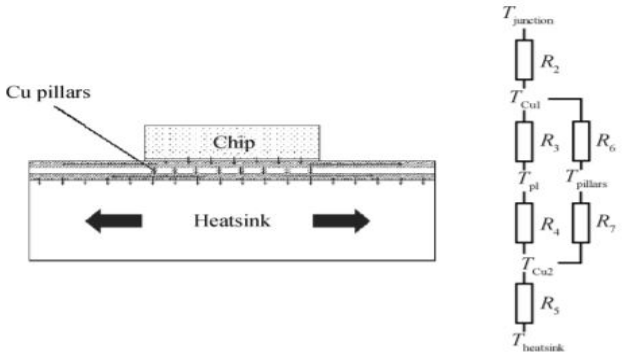


Figure 2.7: Cu pillar model in LED [21]

It can be seen that the Cu pillars are in parallel with the polyimide layer in their model. So the thermal resistance is a parallel combination pillars and polyimide.

$$\frac{1}{R_{\text{parallel}}} = \frac{1}{R_{\text{PI}}} + \frac{1}{R_{\text{Cu}}} \tag{2.9}$$

The calculation can be simplified by ratioing the areas of Cu and polyimide:

$$R_{\text{PI}} = \frac{\Delta n}{K_{\text{PI}} A(1-X)} \tag{2.10}$$

$$R_{\text{Cu}} = \frac{\Delta n}{K_{\text{Cu}} AX} \tag{2.11}$$

where:

A= Surface area of entire interconnect layer [m^2]
X = Area ratio
Δn= Thickness [m]

Thus the parallel resistance can be equated as:

$$\frac{1}{R_{\text{parallel}}} = \frac{K_{\text{Cu}} AX}{\Delta n} + \frac{K_{\text{PI}} A(1-X)}{\Delta n} \tag{2.12}$$

This method of characterization is therefore applicable for Cu pillars in flip-chip. The equivalent thermal resistance would be the parallel resistances of the pillars and underfill.

2.5. EFFECT OF PILLAR GEOMETRY

As mentioned in the Cu pillar patents, pillars come in different sizes. Depending on the processing capabilities of the manufacturer, pillars of different widths and heights can be designed. R_{th} can again be used to evaluate the thermal performances.
According to Fourier's 1-D diffusion equation, R_{th} can be expressed as:

$$R_{\text{th}} = \frac{t}{k.A} \tag{2.13}$$

where:

t= thickness or height of the pillar [µm]
A= Cross-sectional area of the pillar [μm^2]
k_d = Thermal conductivity of the die [W/m.K]

- **Width:** Increasing the width of the pillar would result in increasing the cross-sectional area. Therefore the R_{th} would also decrease.
- **Height:** R_{th} is directly proportional to the thickness or height (See equation 2.13). A lower height would result in a decrease in R_{th}.
- **Cu:solder ratio:** The thermal conductivity of Cu is 385 W/mK and is higher than solder ≈ 60 W/mK at room temperature. Using the series resistance rule, the equivalent (thermal) resistance of the pillar is given as:

$$R_{\text{th-eq}} = R_{\text{th-Cu}} + R_{\text{th-solder}} \tag{2.14}$$

$$R_{\text{th-eq}} = \frac{t_{\text{Cu}}}{k_{\text{Cu}}.A} + \frac{t_{\text{solder}}}{k_{\text{solder}}.A} \tag{2.15}$$

Another constraint is the fixed stand-off height, which can be expressed as:

$$t_{\text{total}} = t_{\text{Cu}} + t_{\text{solder}} \tag{2.16}$$

$$t_{\text{solder}} = t_{\text{total}} - t_{\text{Cu}} \tag{2.17}$$

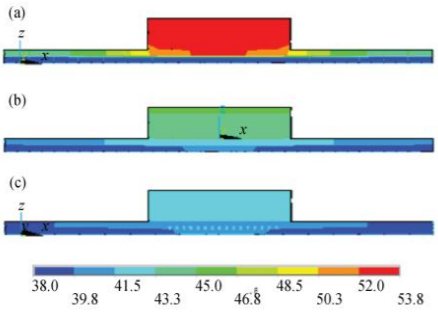
Using the above relation, equation 2.15 can be re-written as:

$$R_{\text{th-eq}} = \frac{t_{\text{Cu}}}{385.A} + \frac{t_{\text{total}} - t_{\text{Cu}}}{60.A} \tag{2.18}$$

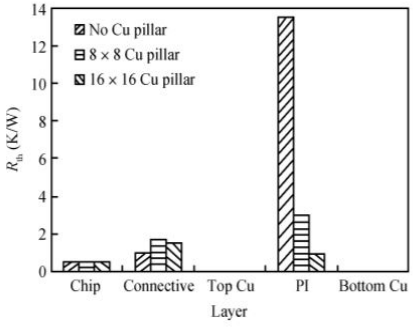
Therefore equation 2.18 shows that decreasing the Cu post thickness would result in a higher thermal resistance and vice-versa.

2.6. EFFECT OF PILLAR DENSITY

Yang Liu et al. [21] in the same paper on pillars in LEDs have also addressed the impact of pillar density on thermal management. Three use-cases were conducted namely, (a) no pillars, (b) 8x8 pillars, and (c) 16x16 pillars. The other boundary conditions was a 1 Watt source on the die and a fixed heat sink of 37 °C at the bottom of the package (Refer Figure 2.7).
Figure 2.8 shows the temperature distribution and the decrease in the thermal resistance by the addition of pillars to the model.



(a) Temperature distribution (a) no pillars, (b) 8x8 pillars (c) 16x16 pillars [21]



(b) Thermal resistance of each layer[21]

Figure 2.8: Temperature distribution and thermal resistance[21]

Figure 2.9 also shows the effect of power to the chip temperature based on the three use cases.

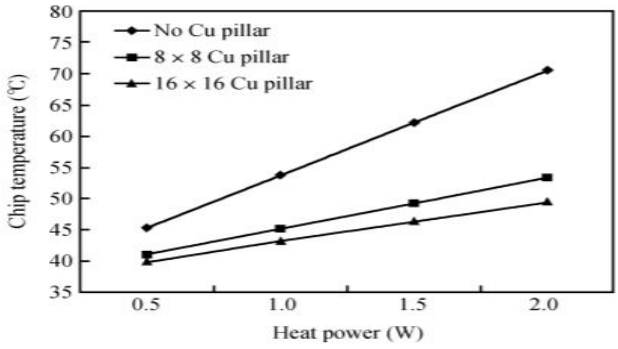


Figure 2.9: Chip temperature against power [21]

This set of simulations prove that thermal resistance decreases as the number of Cu pillars increases. This is because the area of Cu increases and thereby thermal conductivity increases.

2.7. EFFECT OF PILLAR PLACEMENTS

With respect to the placements of pillars, there wasn't any research paper on missing pillars. The only source of reference was a paper written on solder (C4) bumps by Xianging Lu et al. [20]. The paper discusses the impact of having a void, a cracked, and a missing bump to temperature distribution in the chip.
The set-up of the model can be referred to Figure 2.6. Figure 2.10 is the meshed model with a cracked, void, and missing bump.

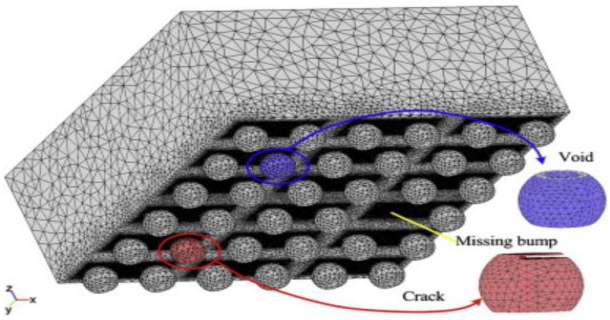
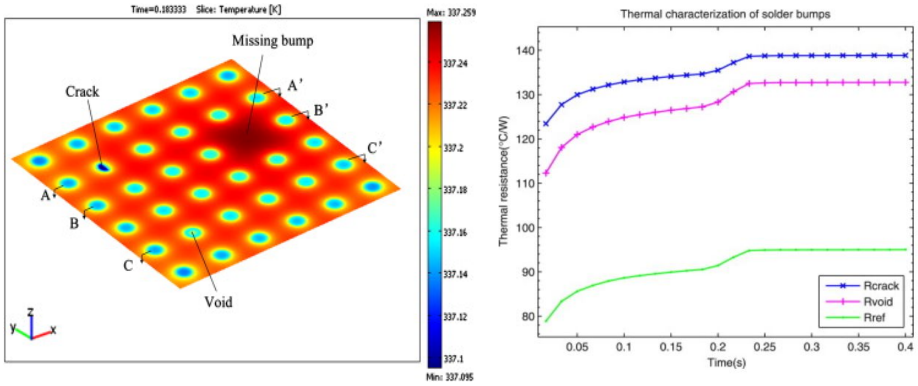


Figure 2.10: Meshed model [20]

A pulsating heat source of 0.45 W was applied to the chip. Figure 2.11 shows the thermographical results of the hotspots created by the defective bumps and the R_{th}.



(a) Temperature distribution with defective bumps [20]

(b) Thermal resistance of defective bumps[20]

Figure 2.11: Temperature distribution and thermal resistance[20]

These results show that pillar/bump placement is important to thermal management. The main focus was on the effects caused by the missing bump but also to acknowledge the effect of having cracked/void bumps would also be detrimental to heat flow in ICs.

2.8. FAILURE MECHANISMS OF CU PILLARS

There are a number of failure types that can be associated with Cu pillars. These failures usually appear at the interface between die and pillar or pillar and laminate. Although there are other failure mechanisms appearing away from this interface because of the loading stresses, and strain caused by the Cu distribution. Analyzing the root cause of these failures is complex and requires experimental data and testing. The following are some of the documented failures as a first-order effect of Cu pillars:

2.8.1. ELECTROMIGRATION

Electromigration (EM) is a phenomenon leading to a failure that is caused by the electrons flowing in an interconnect. The momentum of electron flow collides with the atoms that make the interconnect layer. This leads to the scattering of atoms on the opposite side of the current flow [22]. Therefore voids are formed which leads to an open circuit and increase in the R_{th}.

K. Frank et al. [23] investigated the effect of current density and temperature to the EM failure. The test vehicle consisted of a 19x19 mm^2 die, and 6 pillars (1 input and 5 output) of sizes 35µm Cu, 2µm Ni (barrier layer), and 15µm solder. The pillars are elongated with UBM of 30x40µm. They are connected in a parallel configuration [23]. Figure 2.12 shows the schematic of the setup:

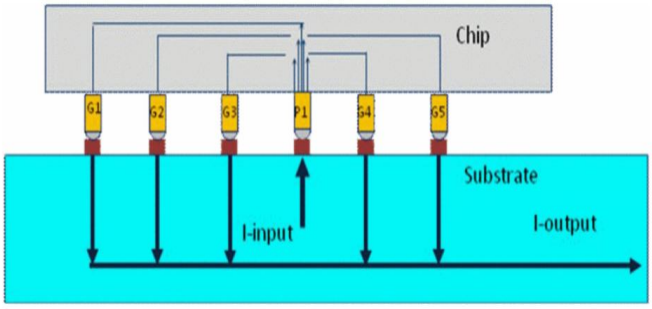


Figure 2.12: EM test schematic [23]

The experiments were conducted for 3 different currents (0.5, 0.7, and 0.9 A), and 3 different temperatures (140,150, and 160 ° C. Table 2.3 shows the results of the test done. Increasing the current density contributed to the increase in failed samples. A similar trend was observed with the increase in the temperature for 0.9 A current. The time taken for 5% failures (t50(hrs) @5%) decreases by 18 times from 0.5 A to 0.9 A at 160 C [23]. This is because of the increase in current density in the pillars resulting in Joule's heating. Figure 2.13 shows the EM failure for 0.9 A current at different temperatures.

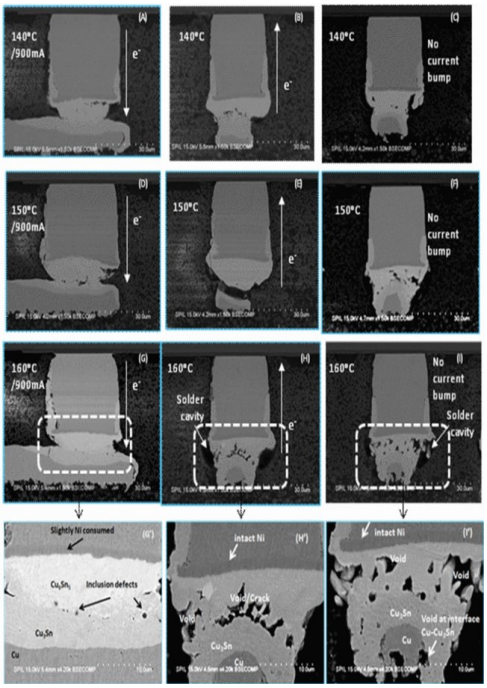


Figure 2.13: EM failure of pillar at 900 mA at different temperatures [23]

Leg	Current (A)	Current density (KA/cm^2)	Oven Temp(C)	Bump Temp(C)	Fail/ Tested	Duration (hrs)	t50(hrs) @5%
1	0.9	90	140	162	17/20	850	80.73
2	0.9	90	150	172	14/20	850	47.45
3	0.9	90	160	182	11/14	850	16.30
4	0.7	70	160	173	7/14	850	83.46
5	0.5	50	160	167	3/11	850	304.61

Table 2.3: EM performance with different currents and temperatures [23]

The EM failure can be predicted using Black's equation:

$$MTTF = AJ^{-n} \exp(E_a/kT) \tag{2.19}$$

where:

MTTF=Mean time to failure [hrs]
J= Current density [A/cm^2]
A= Experimentally determined constant
n= Exponent for current density
E_a= Activation energy [J]
k= Boltzman's constant [J/K]
T= Temperature [K]

The parameters such as E_a and n can be calculated with the help of experimental data. For the same MTTF the amount of current that can flow through pillars of different widths can be estimated. Frank et al. [23] had conducted an experiment for an MTTF of 10 years with 0.1% cumulative failures (criteria bases increase in resistance by 5%). Figure 2.14 shows the effect of pillar width (UBM sizing) to the maximum allowed current.

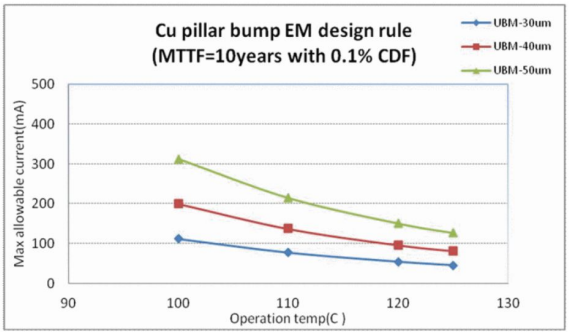


Figure 2.14: Maximum current for MTTF of 10 years [23]

The conclusion that can be drawn for pillar designs with respect to the EM failures is that higher current densities and high temperatures increase the failure rate. The other observation made was the increase in pillar widths makes it less susceptible to EM failures at high currents.

2.8.2. STRESS DUE TO PILLAR GEOMETRY

Tsung Lin et al. [24] have analyzed to understand the failure mechanism caused by the width of copper pillars, opening of passivation layer (PL), and its thickness. The test vehicle for their measurement experiment consisted of a die with dimensions 10.2 mm x 10.2 mm. There were 3042 bumps with the pitch fixed at 162 µm. The substrate was 31 mm x 31 mm x 1.16 mm. The base case (BL) has copper pillar bump dimensions as follows, Cu height as 45 µm, pillar diameter 90 µm , Passivation Layer (PL) of thickness 5 µm with 50 µm (See Figure 2.15).

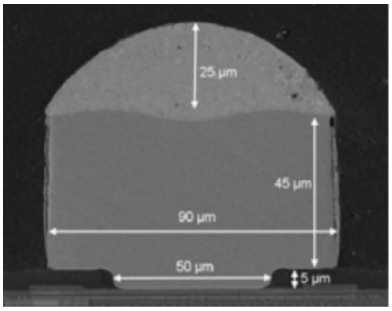


Figure 2.15: Base case dimension of Cu pillar [24]

Figure 2.16 the cross-section of the bumps was examined after Thermal Cycling Test (TCT) of 500 cycles. Delamination between the Al pad and the UBM was observed, which results in peeling.

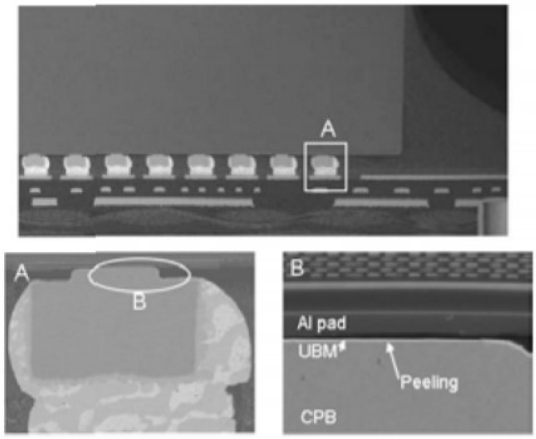


Figure 2.16: SEM investigation of peeling/delamination in Cu pillars [24]

With these results, Tsung Lin et al. [24] then conducted a mechanical analysis using FEM to investigate failures caused by variation of pillar width (60 µm & 105 µm), PL opening (30 µm & 60 µm), and PL thickness (5 µm & 10 µm). Out of all the possible combinations, the use cases with Cu diameter of 60 µm and re-passivation opening of 60 µm would give rise to irregular bump geometry (PL must be smaller than pillar diameter) and thus only 6 use cases were possible. Figure 2.17 shows the meshed model.

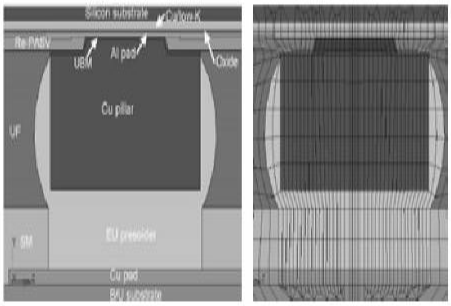


Figure 2.17: FEM mesh of Cu pillar for delamination failure [24]

Table 2.4 shows the results obtained for geometry variations in Cu pillar width, PL sizing. The most optimum case is Case 1 which is a large pillar diameter and small re-passivation opening.

Case	BL	1	2	3	4	5	6
Pillar diam. (μm)	90	105	105	60	105	105	60
Re-PASV opening size (μm)	50	30	60	30	30	60	30
Re-PASV Thickness (μm)	5	5	5	5	10	10	10
Pillar σ_1 at 90°C (MPA)	703	631	617	1010	658	643	978
Pillar σ_1 at −55°C(MPA)	492	526	642	393	637	696	492

Table 2.4: Effect on pillar geometry to stress [24]

2.8.3. STRESS DUE TO UNDERFILL

UNDERFILL'S MODULUS

Tsung Lin et al.[24] also studied the effect of Young's modulus on the first principal stress (σ1). The temperature cycling test (TCT) is divided into two cycles, i.e. low and high temperature. The model setup is the same as in Figure 2.17. The stress was simulated from the outermost copper pillar.

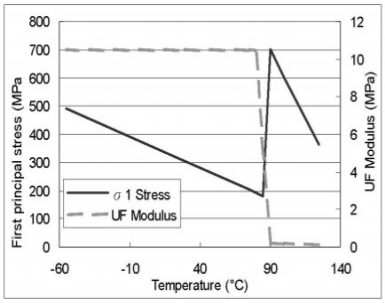


Figure 2.18: Underfill modulus and first principal stress relation at different temperatures [24]

In Figure 2.18 it can be seen that the stress in the high temperature cycle rises faster than in the low cycle. It is also seen that at 90 °C is most susceptible inter-facial delamination because of the high tensile stress and low Young's modulus of underfill. It is therefore important for the underfill to be hard (higher modulus) in the high temperature regions as well.

UNDERFILL'S T_G

An additional parameter of the Underfill that was investigated is the temperature at which the underfill transits from a hard glassy material to a rubbery, soft material, also known as glass transition temperature.

	UF1	S1	S2
Modulus	10.5/0.015	10.5/0.015	10.5/0.015
CTE	26/103	26/103	26/103
Tg	85	95	115
Pillar design	Case 1	Case 1	Case 3
Pillar σ_1 at Tg +5° C (MPA)	631	543	596
Pillar σ_1 at −55°C(MPA)	526	523	421
Warpage (mm)	0.089	0.091	0.096

Table 2.5: Effect of underfill Tg to principal stress [24]

Tsung Lin et al.[24] recorded the data shown in Table 2.5. It can be concluded that for a more reliable Underfill (at 90° C) a high Tg would be required. But this would be at the expense of higher warpage.

3

Cu Pillar Thermo-Mechanical Simulations

3.1. Simulation Model Setup

3.1.1. Simulation Tool

To model the heat flow in IC packages, a CFD simulation tool was required. For this, a CFD tool called Flotherm is used. Flotherm is an industry-wide simulation tool for analyzing thermal designs of electronic components [25]. The tool enables engineers to create digital twins and features to allow modification of the design before production. Flotherm uses the physics of CFD techniques to predict airflow, temperature, and heat transfer co-efficient in various components [25]. Flotherm solves Navier-Stoke's 3D partial differential equations along with a heat balance equation.

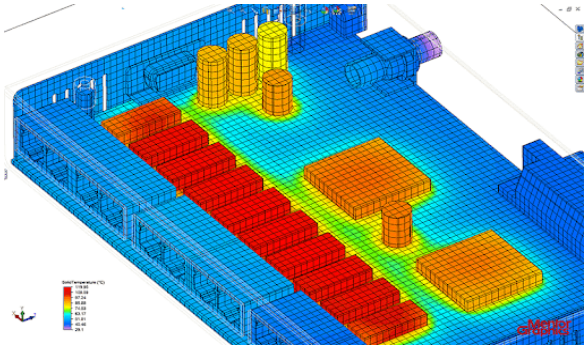


Figure 3.1: 3D- Model of a board in Flotherm [26]

Features of Flotherm:

- Converged solutions for convective, conductive, and radiative heat transfer

- Multi-fluids capability
- Able to model turbulent, laminar and transitional flows
- Radiation exchange factor calculation
- Use of SmartPart for PCB, Die modelling
- Monitor points to check for temperatures at different points
- Able to solve for Joule heating in 3D electronics [25]

3.1.2. TEST VEHICLE SETUP

For the thesis experiment, a test vehicle called "IPTVx" was selected. The dimensions of the package were extracted from System in Package (SiP) using Cadence Innovus. The test vehicle was a bare silicon in a flip-chip package attached to a Printed Circuit Board (PCB) board. The dimensions of the assembly are shown in Table 3.1.

Component	Dimensions (mm)
Die	5 × 4.2 × 0.2
Underfill	5 × 4.2 × 0.06
Laminate	10 × 10 × 0.574
BGA	8.6 × 7.3 × 0.3
PCB	138.5 × 121.5 × 1.694

Table 3.1: Dimensions of IPTVx assembly

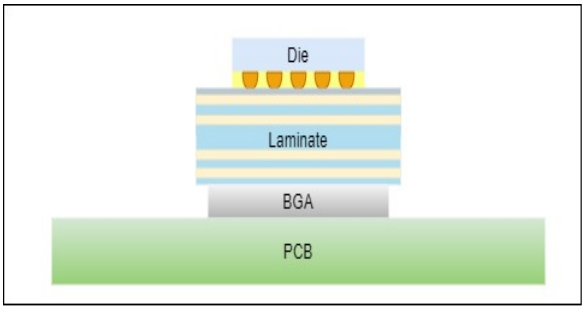


Figure 3.2: IPTVx layers

LAMINATE AND PCB LAYERS

The laminate has layers that are split up as Cu and Fr4. The first layer is the solder resist with metal vias (same dimensions of the respective pillars). The laminate is a 4 layer metal design. The thermal conductive numbers were made from educated assumptions. The theory was based on Kafadarova et al. [27] paper on thermal calculation for metal and dielectric layers in PCB. According to the paper, the percentage (m) of metal vias in a given layer is given as:

$$m = \frac{nA_{via}}{wh} \tag{3.1}$$

where:

n= number of vias
A_{via}= Area of via [mm^2]
w= width of via [mm]
h= height of via [mm]

With this percentage, the thermal conductivity in the z-direction can be modeled as:

$$K^z_{eff} = mK_{via} + (1-m)K^z_{\text{layer}} \tag{3.2}$$

For the lateral thermal conductivity's, the paper proposed the following equations:

$$K^x_{eff} = K^y_{eff} = (1-\sqrt{m})K^{\text{lateral}}_{\text{layer}} + \frac{\sqrt{m}}{\frac{1-\sqrt{m}}{K^{\text{lateral}}_{\text{layer}} + \frac{\sqrt{m}}{K_{\text{via}}}}} \tag{3.3}$$

where:

K_{via}= thermal z-direction conductivity of vias [W/mK]
K^z_{layer} = thermal z-direction conductivity of material [W/mK]
$K^{\text{lateral}}_{\text{layer}}$ =thermal x,y direction conductivity of material [W/mK]

It was found that the lateral thermal conductivities were negligible and the major heat transport was through the z-direction. With this consideration, the assumption made was the metal layers to have 90% Cu and for the Fr4 the calculation was based on an average on other test vehicles. Table 3.2 shows the dimensions of the laminate layers along with the respective orthotropic thermal conductivity.

Layer	Name	thickness [mm]	kx [W/mK]	ky [W/mK]	kz [W/mK]
1	Solder Resist	0.021	0.3	0.3	0.3
2	Metal-1	0.015	347	347	347
3	Dielectric-1	0.03	0.5	0.5	5
4	Metal-2	0.021	347	347	347
5	Dielectric-2	0.4	0.5	0.5	5
6	Metal-3	0.021	347	347	347
7	Dielectric-3	0.03	0.5	0.5	5
8	Metal-4	0.015	347	347	347
9	Solder Resist	0.021	0.3	0.3	0.3

Table 3.2: IPTVx laminate layer and conductivity's

For modeling the PCB layers, the "PCB" smart part was used. This SmartPart in Flotherm models each of the metal and dielectric layers as metal composition percentages. The layer details were calculated using the .odb file. Table 3.3 shows the 8 layer PCB board with its dimensions and compositions.

Layer	Name	Metal %	thickness [mm]
1	Metal	84.5	0.04
2	Via	3.2	0.071
3	Metal	76.2	0.018
4	Via	3.2	0.107
5	Metal	62.9	0.018
6	Via	3.2	0.27
7	Metal	93.9	0.018
8	Via	3.2	0.61
9	Metal	92.2	0.018
10	Via	3.2	0.27
11	Metal	93.9	0.018
12	Via	3.2	0.107
13	Metal	91.6	0.018
14	Via	3.2	0.071
15	Metal	93.1	0.04

Table 3.3: IPTVx PCB dimensions

The thermal conductivity of the other components in the assembly is taken from the standard Flotherm library.

- Silicon: 117.5 [W/mK]
- Solder(SnAgCu): 58 [W/mK]
- Copper: 385 [W/mK]
- Underfill: 0.9 [W/mK]

DIE SMART PART

Another component used in the model was the "Die SmartPart" in Flotherm. This smart part did not have much information documented. To understand the smart part, a set of experiments were performed. The smart part was compared to a cuboid of Silicon with uniform power [1 Watt], a cuboid of Silicon with a collapsed source [1 Watt]. The results are shown in Table 3.4.

	Die_top [C]	Die_middle [C]	Junction [C]
Die smart part	46.46	46.91	46.87
Si	46.51	46.96	46.89
Si collapsed source	46.47	46.91	46.87

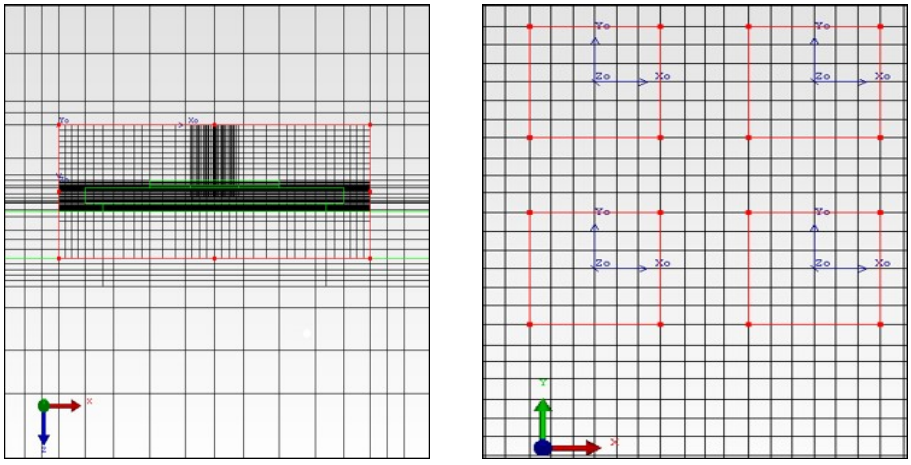
Table 3.4: Die smart part comparison

The numbers from the above table show that the Die SmartPart behaves identically to a cuboid of Si with a collapsed source in the z-direction. This is ideally what a flip-chip die would be, with the active components (transistors) at the bottom of the die assembly.

GRIDDING

The meshing involves the use of FEM. The total number of cells was 1074552 and the maximum aspect ratio was 149 (above the PCB-air interface). A volume region mesh was also added to localize the mesh. This reduces the number of cells considerably and saves computational time. Figure 3.3a shows the meshed structure.

In addition to this, mesh inflation was also applied to certain assemblies. For the package, the mesh was inflated by 3.5 mm on top, 1 mm on the bottom, and 0.5 mm on either side. This is done in order to capture the solid-air heat propagation. Similarly, the spacing between the Cu pillars was also inflated to model the behavior of the lateral heat flow (see Figure 3.3b To prevent unnecessary, long simulation times but maintaining an



(a) Volume region mesh of IPTVx

(b) Mesh inflation in Cu pillars

Figure 3.3: Meshing layout of IPTVx

accurate grid, the model was checked for grid (in-)dependency. Several simulations with different grid coarseness were performed, both for gridding of air around the package as well as the space between the Cu pillars in the underfill. Monitor points for the temperature were used to determine grid independence.

Cells	Mesh Type	Die [C]	1 [C]	2 [C]	3 [C]	4 [C]	5 [C]	6 [C]
1418848	Coarse	44.35	44.31	44.31	44.30	44.30	44.29	44.11
2327916	Med	44.08	44.04	44.04	44.03	44.03	44.02	43.85
2520818	Fine+Cupillars mesh	44.09	44.05	44.05	44.04	44.04	44.03	43.86
4679496	Fine+Cupillars mesh	44.07	44.04	44.04	44.03	44.03	44.02	43.85
8856766	Fine+Cupillars mesh	44.07	44.04	44.04	44.03	44.02	44.02	43.85

Table 3.5: Mesh in-dependency check

From Table 3.5 it can be seen that once the meshing type moves to medium and fine the numbers do no vary. Even further increase in the number of cells in Cu pillars also showed no variation. Hence the model can be assumed as mesh/grid independent.

The model was also checked for de-keypointing, which can occur if geometry edges do not line up with grid lines. Consequently, the solver calculates with different dimensions differently as those defined by the geometries themselves.

BOUNDARY CONDITIONS

The boundary conditions applied to the model are as follows:

- Power: 2 Watts uniform power or 2 Watts of power varying over a surface area (depending on the scope of the simulations).
- Solver: Conduction Only. Since the focus is on the pillars which are embedded inside the package. The major mode of heat transport is via conduction.
- Ambient Temperature: 35 ° C as the ambient temperature.
- Heat Sink: 37 ° C at the bottom the package was placed. This ensures that a fixed source will provide a fixed reference for one-on-one comparison.

3.2. CHARACTERIZATION

For the characterization, the thermal resistance method was used. First, the different pillars are listed below:

3.2.1. TSMC PILLARS

Chip manufacturer TSMC provides design rule manuals for the technology nodes they offer. These manuals have rules for pillar geometries with oblong shapes [4]. Ying-Chih Lee et al. [28] studied the shape and pattern of Cu pillars. The experiments resulted that Cu pillars with oblong-shaped and aligned radially inwards have 2%-10% less tensile stresses as compared to circular designs. This type of design is adopted by TSMC.

To simplify the model approximate dimensions of TSMC pillars are shown in Table 3.6.

	Type 1	Type 2	Type 3	Type 4
Pitch (µm)	$110 \leq P < 130$	$130 \leq P < 150$	$150 \leq P < 180$	$180 \leq P < 210$
Radius (µm)	34.15	38.5	45	53.65
Height (µm)	60	60	60	60

Table 3.6: TSMC Cu pillar rules [4]

From the above table, it can be seen that Type 1 to Type 4 pillar has its own respective pitch and radius. The pitches range from 110 µm to 200 µm. The radius scales up through each pillar design. From this table, it can be established that as pillar width (i.e. radius) increases the pitch also increases. Therefore, for a given area Type 1 would have more number pillars due to the low pitch and narrow width as compared to a Type 4 pillar. The other parameter is the height or stand-off height. From the TSMC document [4], the rule stated that the stand-off height had to be maintained at 60 µm.

3.2.2. NOVEL DESIGNS

To broaden the characterization, 2 novel designs were added. The pillar designs were aimed at going "Beyond TSMC" rules. Table 3.7 shows the two new designs with their dimensions.

	Type a	Type b
Pitch (um)	$80 \leq P < 110$	$80 \leq P < 110$
Radius (um)	28.7	34.15
Height (um)	60	60

Table 3.7: Novel pillar design dimensions

The novel pillar designs are labeled as Type a and Type b. Type b has the same pillar geometry as that of Type 1 (See Table 3.6), but has its pitch narrowed down to 80 - 100 µm. Similarly, the same pitch of Type b was used for Type a but the radius was scaled down. The motivation for having pillars with narrow pitches and slender widths are as follows:

- X.R. Zhang el al. [29] studied the structure optimization for Cu pillars. In their research, they had several pillar sizes of different pitches, height, ratio, etc. Table 3.8 shows the different dimensions used. On comparing the last 2 rows of the table, an approximation can be used to justify Type a's pitch, height, and also the radius.

Pad Pitch (µm)	Diameter (µm)	Cu Post (µm)	Cap (µm)
200	100	65	35
150	80	50	35
100	65	45	30
50	25	17	15

Table 3.8: Dimensions used by Global Foundry Cu pillars [29]

Gerber et al. [30] also proposed pillar designs with pitches as narrow as 50 µm and similar stand-off heights.

- As the technology node continues to become smaller and smaller, the emphasis is on the interconnects to have finer pitches. This was the outline for International Technology Roadmap for Semiconductors (ITRS) conference in 2003 [31].
- The reason for slender pillar geometries is not only for meeting the narrow pitch condition. Copper is known to affect the transistor's characteristics and add unwanted stresses as well. The layout designer would therefore like to have as little copper as possible.

3.2.3. THERMAL RESISTANCE

Chapter 2.4 explained how 3-D Fourier's heat diffusion equation can be expressed in a simple 1-D form. It also defined the thermal resistance or R_{th} (See equation 2.8) as a function of material parameters:

$$R_{\text{th}} = \frac{t}{kA} \tag{3.4}$$

where:

t= thickness or height of the pillar [µm]
A= Cross-sectional area of the pillar [µm^2]
k = Thermal conductivity of the Cu&solder [W/m.K]

With this equation in hand, the thermal resistances of the different pillar designs is show below:

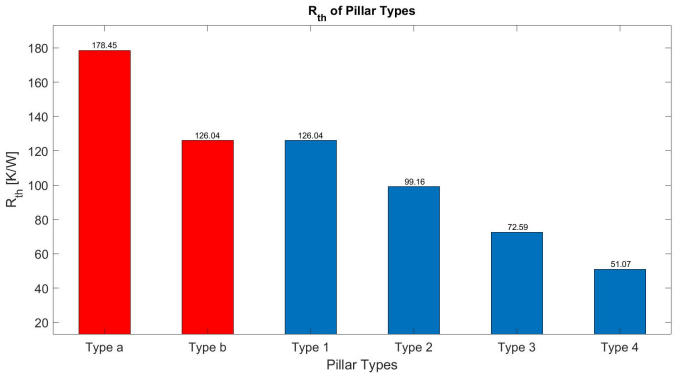


Figure 3.4: R_{th} per pillar of the different pillar designs

The above plot shows the R_{th} TSMC pillars in blue and the novel designs in red. It can be seen that the novel designs have a high R_{th} as compared to Type 4 of TSMC designs. The radius of Type a is roughly 1.9 times smaller than Type 4, therefore the area of Type a is 3.5 times smaller than Type 4. Since R_{th} is inversely proportional to area, Type a has a 3.5 times higher R_{th} than Type 4. A similar inference can be made for the R_{th} of the other

pillar designs. On the other hand smaller width pillars with lower pitches enable more pillars under a given area. This compensates for the high R_{th} by having a higher density of thin pillars.

3.3. VARIATION IN GEOMETRY, PITCH, AND DENSITY

In this section, the pillar geometry, pitch as well as density are varied. The outline is to see how these variations affect the overall thermal management. Table 3.6 and Table 3.7 shows the 6 pillar types with different combinations of pitch and radius. The test vehicle has a uniform power of 2 Watts applied.

To understand the effect of these variations, a simple regression equation was used. This equation expressed the T_J (Junction temperature) at the center of the die as a function of weightages for pitch and density. This was done for each pillar design. The T_J equation is shown below:

$$T_J[C] = a_0 + a_1.\,\text{Pitch}\,[\mu\text{m}] + a_2.\,\text{Density} \tag{3.5}$$

where:

T_J= Junction temperature at center [C]
a_{1-2}= Weight's for each parameter

The densities were 7×7, 13×13, and 21×21. Along with a regression equation each pillar design had its respective surface plot. The surface plot was a 3-D graph showing the T_J dependency on pitch and density.

Pitch [µm]	Density	$T_J[C]$
80	49	54.63
80	169	53.38
80	441	52.11
90	49	54.51
90	169	53.14
90	441	51.73
100	49	54.42
100	169	52.90
100	441	51.34

Table 3.9: T_J of Type a pillar

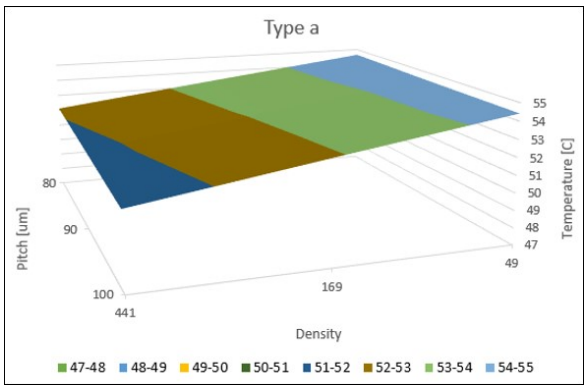


Figure 3.5: Type a surface plot

The regression equation for Type a pillar is shown below:

$$T_J = 56.812 - 0.024.\,\text{Pitch}\,[\mu\text{m}] - 0.007.\,\text{Density} \tag{3.6}$$

Table 3.9 and Figure 3.5 shows the T_J as a function of pitch and density. The regression equation 3.6 shows the weightage of the pitch and density as well. The weightage for pitch is bigger but the variation caused a slight reduction in T_J. This is because the pitch has a very small increment of a maximum of 20 µm increase. The surface plot shows a

linear slope for the density variation. 49 pillars result in higher T_J whereas 441 pillars resulted in the lowest T_J. This is because more number of pillars means more amount of copper and thus a better thermal performance.

The surface plot of the other pillar designs were all similar in terms of their slopes with the reduction in T_J as dimensions become larger. The rest of the plots and tabulation of data is in Appendix A.

Since the variation in pitch offered little to the T_J, the data were averaged for the respective pitches and plotted in Figure 3.6.

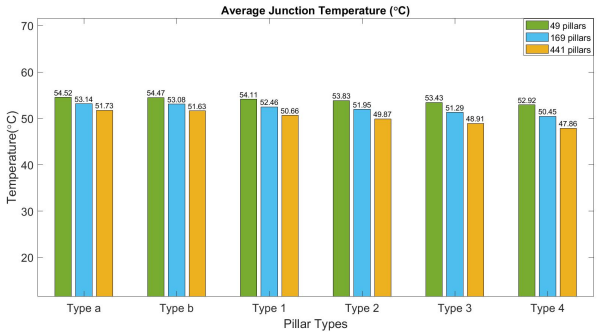


Figure 3.6: T_j of the different pillar designs for different densities

The above table shows the effect of density on the T_J. Type a and Type b were expected to records the highest temperatures. Similarly Type 4 was expected to be the lowest because the pillar has the largest radius.

For each pillar design, it can be seen that for 49, 169, and 441 show a small reduction (from Type a to Type b, and from Type b to Type 1, so on). The reason behind this is because the ratio of Cu to underfill is not significantly being changed by the increase in pillar width (radius). Recalling equation 2.12 and expressing R_{th} as Cu and underfill:

$$\frac{1}{R_{\text{parallel}}} = \frac{K_{\text{Cu}} AX}{\Delta n} + \frac{K_{\text{uf}} A(1-X)}{\Delta n} \tag{3.7}$$

where:

A= Surface area of entire interconnect layer [m^2]
X = Area ratio
Δn= Thickness [m]

Thus for a decrease in T_J, the R_{th} should also reduce. This means in equation 3.7, the area ratio (X) of Cu:underfill must be significantly higher. Table 3.10 shows the area ratio (X) for the different densities and pillar types. It can be seen for each density the ratio isn't increasing by a large amount from the novel designs to the TSMC pillars and therefore the T_J does not have a significant decrease. The dimension of the vias connecting the pillars to M1 of the laminate also impacts the T_J. Hence small reductions for larger pillars even though the area ratios are the same.

	Density		
	49	169	441
Type-a	0.006	0.02	0.06
Type-b	0.008	0.03	0.08
Type-1	0.008	0.03	0.08
Type-2	0.01	0.03	0.11
Type-3	0.02	0.05	0.15
Type-4	0.02	0.07	0.23

Table 3.10: Area ratio (X) of Cu:underfill for different pillar densities

Within each pillar design, the reduction can be seen by the different color bar graphs. From 49 pillars to 169, a reduction of around 2 °C can be seen. Similarly from 169 pillars to 441, the same reduction is noted. Thus for a 4 times increase in density, only a couple of degrees is noted. The reason for the small reduction is due to the heat being obstructed in the preceding layers. The dielectric layers in the laminate offer a high thermal resistance to the model. The equivalent thermal resistance is a set series of R_{th}'s from junction to PCB (See Figure 3.7). So even though there is a decrease in the thermal resistance in the interconnect layer, the overall thermal resistance is dictated by the substrate's thermal resistance.

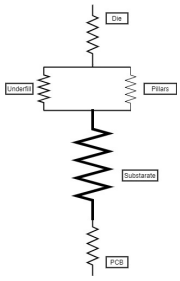


Figure 3.7: Series R_{th} of IC package

Another reason for the small reduction is the point of measurement is at the junction center, adding more pillars away from the center has less of an effect on the $T_{J\text{-center}}$. The effect of pillar placements are explained in Section 3.5.

The regression equations of each pillar is summarized in Table 3.11. A "general" equation with the radius as a parameter is also shown.

	Regression Equations
Type-a	$T_J = 56.812 - 0.024.\ \text{Pitch}\ [\mu\text{m}] - 0.007.\ \text{Density}$ (3.8)
Type-b	$T_J = 57.466 - 0.032.\ \text{Pitch}\ [\mu\text{m}] - 0.007.\ \text{Density}$ (3.9)
Type-1	$T_J = 57.055 - 0.024.\ \text{Pitch}\ [\mu\text{m}] - 0.008.\ \text{Density}$ (3.10)
Type-2	$T_J = 57.424 - 0.025.\ \text{Pitch}\ [\mu\text{m}] - 0.01.\ \text{Density}$ (3.11)
Type-3	$T_J = 56.972 - 0.021.\ \text{Pitch}\ [\mu\text{m}] - 0.011.\ \text{Density}$ (3.12)
Type-4	$T_J = 57.613 - 0.024.\ \text{Pitch}\ [\mu\text{m}] - 0.012.\ \text{Density}$ (3.13)
"General" Equation	$T_J = 57.41 - 0.036.\ \text{Pitch}\ [\mu\text{m}] - 0.009.\ \text{Density} + 0.034\ \text{Radius}\ [\mu\text{m}]$(3.14)

Table 3.11: Regression equation of each pillar design and the "General" equation*

*Only applicable for same boundary conditions

3.4. MECHANICAL RELIABILITY OF NOVEL DESIGNS

The novel designs were introduced in the previous section. From Table 3.6 it can be seen that Type a, Type b and Type 1 (TSMC) are very comparable and vary by only a degree. This raises the question: *How reliable are these designs as compared to TSMC?* For this, a mechanical simulation showing warpage and stress comparisons is conducted.

3.4.1. MECHANICAL SETUP

Ansys Mechanical and Work Bench are the tools used for the mechanical comparison. Afripin et al. [32] proposed the use of homogenized modeling of the Cu pillar along with its underfill. The setup is shown in Figure 3.8.

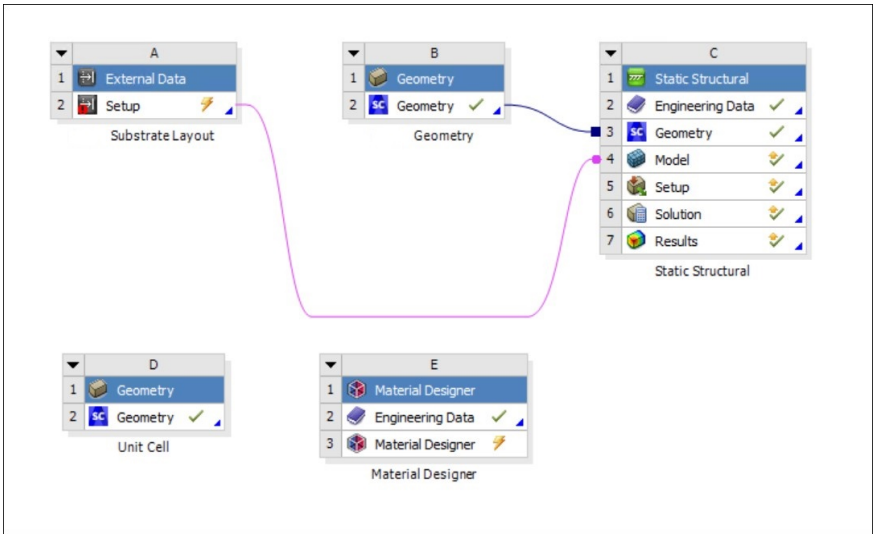


Figure 3.8: Mechanical setup

The procedure for pillar modeling for each pitch is as follows:

- **System A**: This consists of importing and reading external data. For the IPTVx, the substrate layers are modeled in Cadence. So the SiP files containing the description of metal, dielectric, and Cu vias are imported and converted in System A.
- **System B**: This system describes the geometry of the model. For the mechanical comparisons, modeling the die, underfill (with pillars) and substrate is sufficient for the stress and warpage comparisons.
- **System C**: This is the system consisting of Steady-State Thermal physics. For the geometry and the model, a link is created from System B and System A respectively. This is considered as the "Global Model".
- **System D**: This system utilizes Spaceclaim, a tool acquired by Ansys for modeling geometries of different shapes. Figure 3.9 shows a unit cell (quarter model) of the

pillar along with the underfill created in Spaceclaim. The x and y dimensions of the unit cell are 0.5 times pitch and extruded with the height of the pillar. Similarly, the x and y dimensions of the pillar is the radius.

- **System E**: Once a unit cell is created, it can then be linked or copied to the Material Designer. This is another tool acquired by Ansys. In Figure 3.9 the unit cell is conformally meshed using the Material designer. It then performs a homogeneous mixing of material properties. The result is a unit cell with homogeneous properties of all three materials. This step is repeated for different temperatures to obtain orthotropic properties of Young's, and Bulk's modulus, Poison's ratio along with CTE. Finally, this is entered as material properties for the "Underfill with pillar" block in System C.

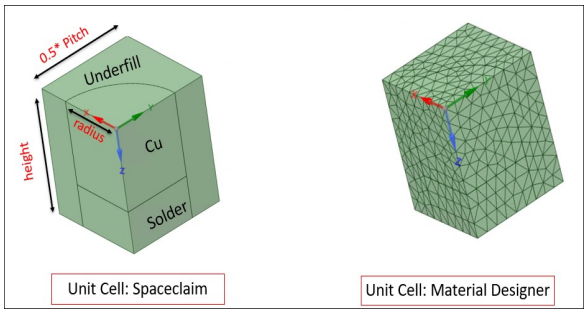


Figure 3.9: Unit Cell: Spaceclaim and Material Designer

CONSTRAINTS

In System C, the geometry model has a set of fixed supports. On each of the four corners of the laminate, a certain set of degrees of freedom are applied. They are: Fixed in all directions, Free in only the - direction, Free in the x and y direction, and Free in all directions (See Figure 3.10).

The other constraint is the thermal conditioning added. For this, the model is allowed to cool from a stress-free state of 150 °C at the rate of 5 °C/min.

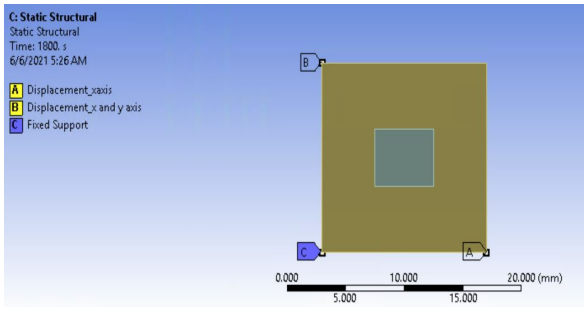


Figure 3.10: Static structure constraints

MATERIAL PROPERTIES

Figure 3.11 and Figure 3.12 show the Young's Modulus and CTE in the x-direction for Cu and underfill. Cu has Young's modulus of 15 times higher than the underfill. For the CTE the underfill is 4.5 times higher than Cu.

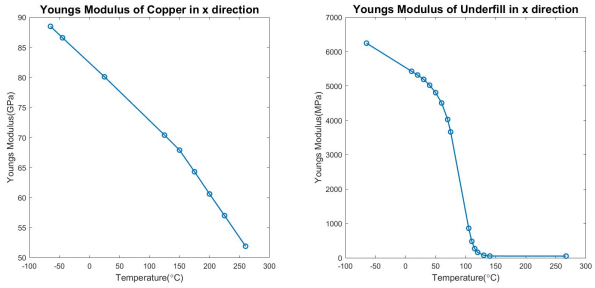


Figure 3.11: Young's Modulus of Cu and Underfill

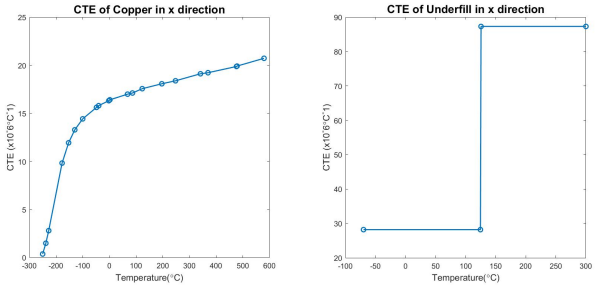


Figure 3.12: CTE of Cu and Underfill

UNIT CELL PROPERTIES

Figure 3.13 shows the Young's modulus and CTE. Analyzing the two plots it can be seen that Type b's unit cell has a higher Young's Modulus and lower CTE for lower pitches. This is because for the unit cell of Type b only the pitch has been reduced. This means that the percentage of Cu is higher for that particular unit cell. And from looking at individual material properties, higher Cu results in higher Young's Modulus. The converse can be inferred for the CTE.

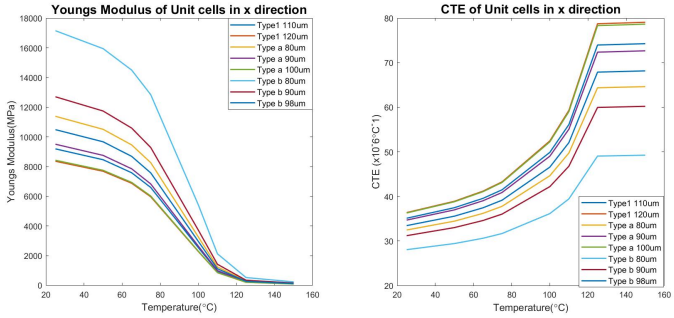


Figure 3.13: Unit cell's Young's Modulus and CTE

3.4.2. WARPAGE

The warpage simulation is the direct deformation in the z-direction. The warpage is dependent on the Young's Modulus and CTE. Figure 3.14 shows the warpage profile at 25°C for Type 1 pillar with 110 µm. It can be seen that the maximum deformation is the highest at the die center. This was the same plots for the other pillar types at different pitches.

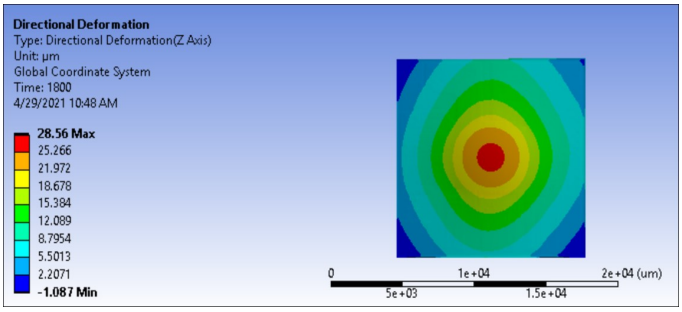


Figure 3.14: Warpage at 25°C for Type 1 pillar with 110 µm pitch

Figure 3.15 shows the maximum deformation for each of the pillar types for their respective pitches. The results were documented for 125°C, 100°C, and 25°C. To have a better understanding Figure 3.16 shows the average for different pitches as a percentage increase in the deformation of the novel designs as compared to TSMC's Type 1.

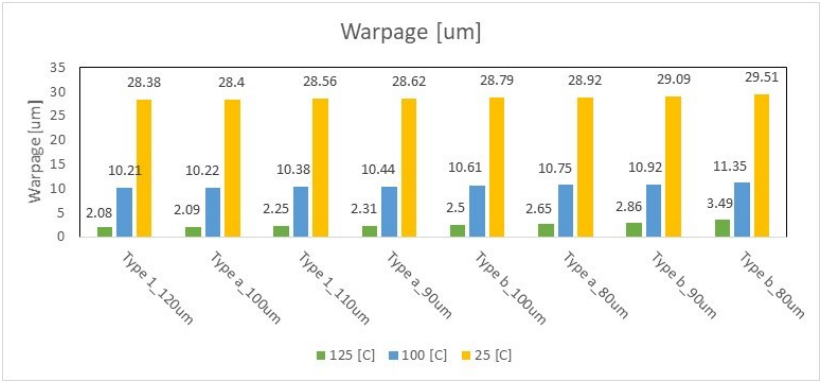


Figure 3.15: Maximum Warpage of the pillars

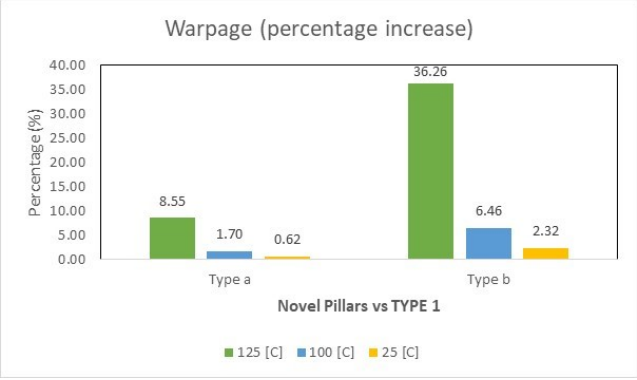


Figure 3.16: Percentage increase in maximum warpage from Type 1

Hao et al. [33] studied the effect of Young's Modulus and CTE on warpage. It was concluded that the dominant mechanical property of the two dictates the warpage, which is seen in Figure 3.16.

3.4.3. NORMAL STRESS

The next type of comparison performed was the normal stress or σ_z stress in the z-direction. This stress analysis is useful in understanding stresses which would lead to failures such as delamination, peeling in the z-direction. Figure 3.17 shows the warpage profile at 25°C for Type 1 pillar with 110 µm. It can be seen that the maximum stresses are on the corner of the underfill layer. This was the same plots for the other pillar types at different pitches.

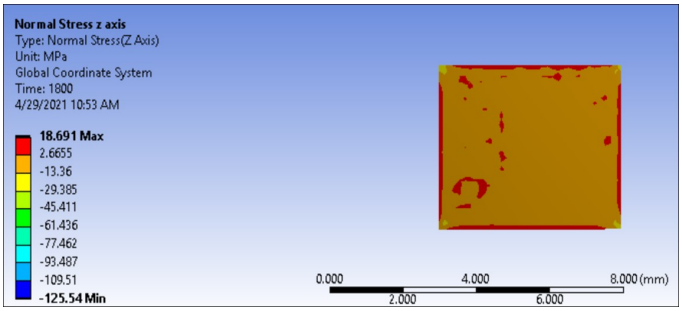


Figure 3.17: Normal Stress at 25°C for Type 1 pillar with 110 µm pitch

Figure 3.18 shows the maximum σ_z stress for each of the pillar types for their respective pitches. The results were documented for 125°C, 100°C and 25°C. Figure 3.19 shows the average for different pitches as a percentage increase in the normal stress of the novel designs as compared to TSMC's Type 1.

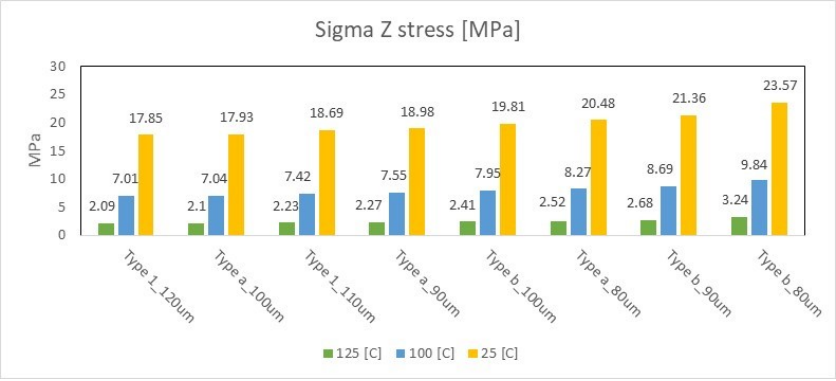


Figure 3.18: Maximum Sigma-z stress of the pillars

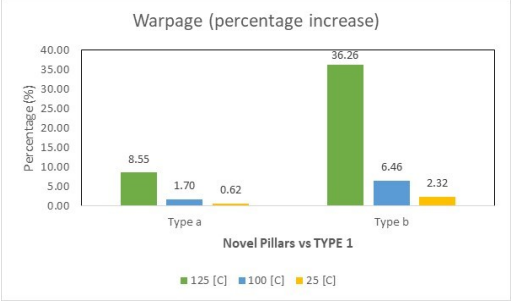


Figure 3.19: Percentage increase in maximum Sigma-z stress from Type 1

3.4.4. TENSOR STRESS

In the previous subsection, the normal stress talks about the stress only on z face (σ_{zz}). The stresses on each face in the z-direction can also be included. The two other stresses are denoted by (σ_{xz}) and (σ_{yz}). These stresses are referred to Shear or Stress Tensor. To calculate the stress tensor, the magnitude of the two remaining stresses is added. Figure 3.20 shows the warpage profile at 25°C for the Type 1 pillar with 110 µm. It can be seen that the maximum stresses are on the corner of the underfill layer. This was the same plots for the other pillar types at different pitches.

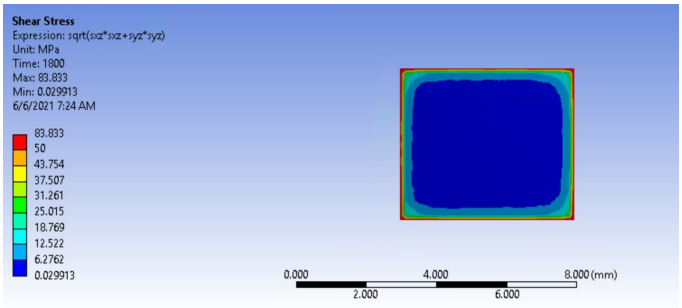


Figure 3.20: Shear Stress at 25°C for Type 1 pillar with 110 µm pitch

Figure 3.21 shows the maximum shear stresses for each of the pillar types for their respective pitches. The results were documented for 125°C, 100°C and 25°C. Figure 3.22 shows the average for different pitches as a percentage increase in the stresses of the novel designs as compared to TSMC's Type 1.

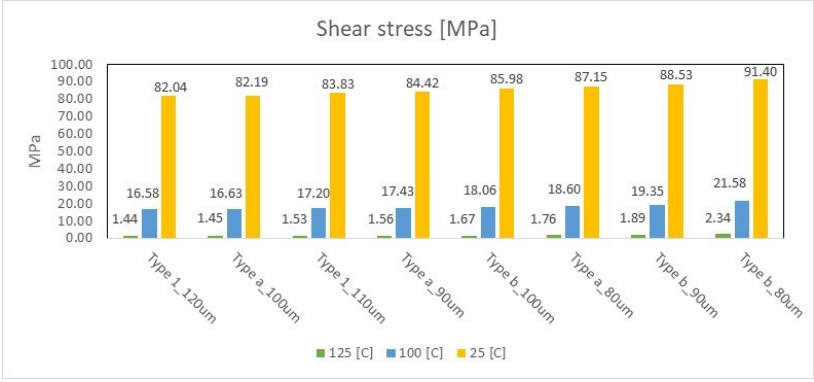


Figure 3.21: Maximum Shear stress of the pillars

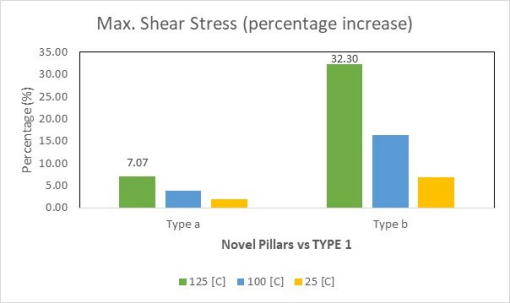


Figure 3.22: Percentage increase in maximum Shear stress from Type 1

3.4.5. MAXIMUM PRINCIPLE STRESS

The maximum principle stress is the normal stress calculated at the angle θ when the shear stress is zero [34]. This stress indicates the failure caused by the growth of a crack perpendicular to the stress [35].

Figure 3.23 shows the maximum principle stresses for each of the pillar types for their respective pitches. The results were documented for 125°C, 100°C and 25°C. Figure 3.24 shows the average for different pitches as a percentage increase in the maximum principle stress of the novel designs as compared to TSMC's Type 1.

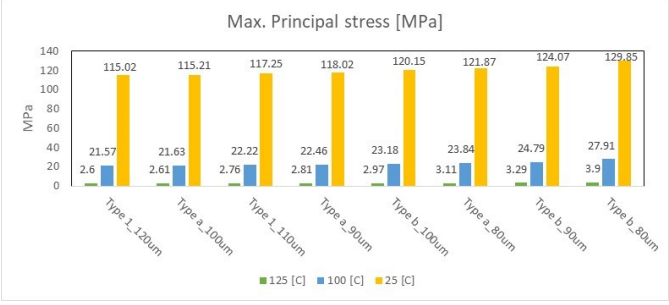


Figure 3.23: Maximum of Max. Principle stress of the pillars

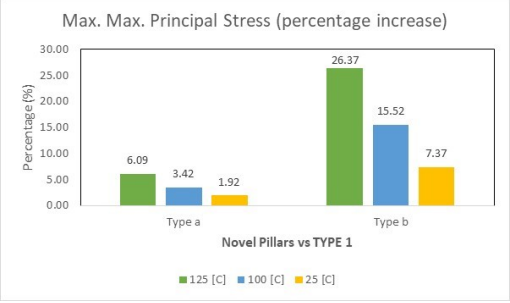


Figure 3.24: Percentage increase in Maximum of Max. Principle stress from Type 1

3.4.6. EQUIVALENT STRESS

The equivalent stress or the von Mises yield. This stress indicates the yielding of the material subjected to loading (thermal). According to this, yielding occurs if the stresses applied are greater than the materials criterion [36]. This is useful for understanding the fatigue failure in materials.

Figure 3.25 shows the maximum equivalent stresses for each of the pillar types for their respective pitches. The results were documented for 125°C, 100°C and 25°C. Figure 3.26 shows the average for different pitches as a percentage increase in the von Mises stress of the novel designs as compared to TSMC's Type 1.

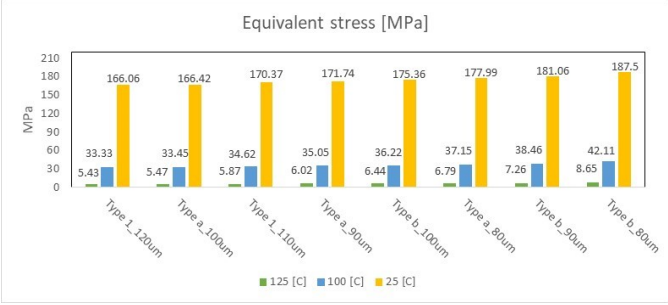


Figure 3.25: Maximum Equivalent stress of the pillars

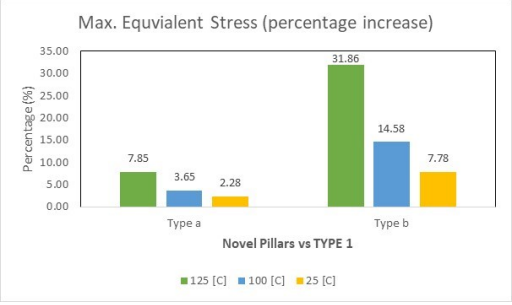


Figure 3.26: Percentage increase in maximum Equivalent stress from Type 1

3.4.7. CONCLUSION

The conclusions drawn from the above mechanical tests point to Type a being relatively good and Type b faring the worst. This is due to the fact Type b has only its pitch scaled-down but Cu radius intact. Thus this leads to higher warpage and stress numbers. In order to completely rule Type b further tests with experimental data is required.

3.5. PILLAR PLACEMENT WITH RESPECT TO HOTSPOT

The literature from previous papers speaking about Cu pillars use a uniform power source across the silicon. However, in a given IC there are a number of instances with high power densities causing hotspots. Thus it is crucial in understanding the effect of pillar placements with respect to hotspot.

The setup is the same as mentioned in Section 3.1.2. The power is now a 2 Watt source with an area 0.2×0.2 mm_2 at the center of the die. This will act as the hospot for the simulations. TSMC's Type 1 pillars are used in these simulations.

USE CASES

Figure 3.27 shows the different use cases for pillar placements.

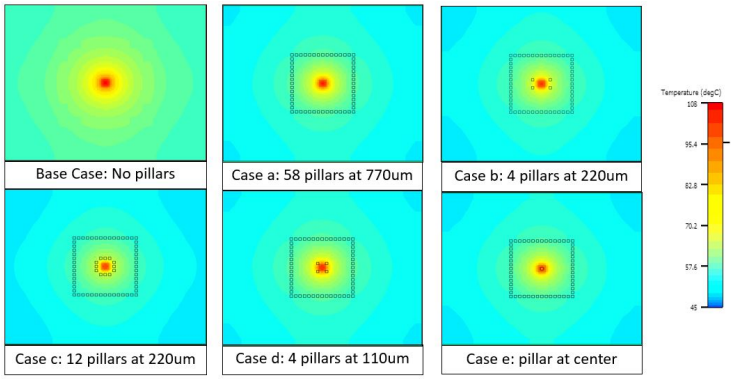


Figure 3.27: Use cases for pillar placements

- Base Case: This is the case when no pillars are placed. The concentric rings of heat produced by the hotpot are seen due to no pillar placements. The heat has to only travel upwards in the silicon. This is the case where other results will be based upon.
- Case a: This consists of 58 pillars placed at 770µm from the hotspot center. This is typically what an IC layout looks like with pillars far away from the instance.
- Case b: In addition to the 58 pillars, 4 more pillars are added at 220µm from the center.
- Case c: This case has the addition of 12 pillars at 220µm from the center. These pillars form a circle identical to the conductive circles produced by the hotspot.
- Case d: In this case, 4 pillars are added at 110µm from the center. These pillars are now touching the corner es of the power source.
- Case e: This is the last case with the addition of a single pillar at the center of the hotspot.

Monitor points are placed on the junction center as well as on the sides of the junction between die and underfill.

RESULTS

Figure 3.28 shows the bar plot for the different cases. It can be seen that the highest temperatures are recorded at the junction center. This is because of the location of the hotspot. The base case shows the highest temperatures, as expected. Moving to case (a), see's a reduction of 2°C when 58 pillars are added. Case (b), see's a further reduction of 2°C as 4 more pillars are added at 220 µm. Case (c), and case (d) follows this trend as well. Case (e), which is the last case, has a significant reduction of 21°C from the base case. This was the addition of a single pillar at the center.

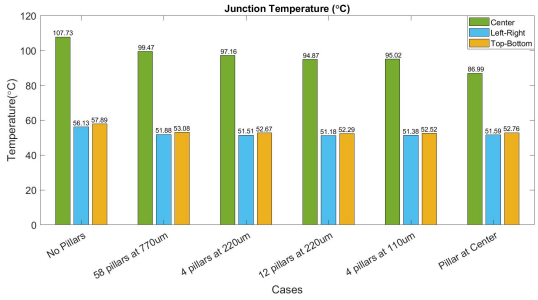


Figure 3.28: Junction Temperature of pillar placements

This simulation was repeated for instances of different areas with the same 2 Watt source. This is done because hotspots come in different sizes and power densities. The areas of the hotspot are 0.04 mm^2, 0.01 mm^2 and 0.0025 mm^2. Figure 3.29 shows the ΔT reduction plots of the junction center from the respective base cases. For cases (a)-(d) it can be seen that the reduction in temperature is not very significant for the different areas. But case (e) which has an addition of a single pillar shows a massive reduction of 21°C, 31°C and 52°C for the respective areas.

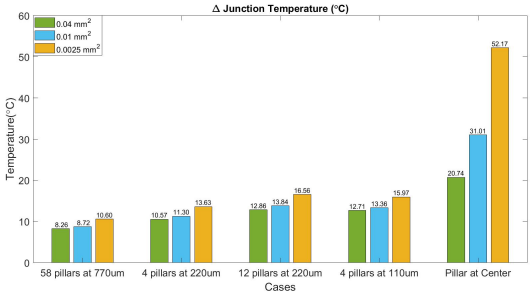


Figure 3.29: ΔJunction Temperature of pillar placements with different areas

The conclusion from these simulations is that placing pillars at arbitrary locations

from the hotspot is not going to have a significant impact as placing a pillar closest to the hotspot source. The thermal effect is therefore more pronounced at the center of hotspots.

3.6. FUTURE PILLAR DESIGN AND UNDERFILL

Currently, there is active research on topics relating to interconnects. This section addresses thermal improvements in the pillar material section and the underfill's thermal conductivity.

3.6.1. CU-CU INTERCONNECT

There is a need to go even further down in pitch and the discussion has been on the removal of solder cap to achieve this [37]. This leads to the interconnect technology called "All Cu" or Cu-Cu" interconnects. Figure 3.30 shows the progress from solder bumps to all Cu interconnects. The problems faced with such a shift are the processing temperatures of Cu. Cu has a melting temperature of 1085 °C [38], and this possesses a challenge to subject the package to such high temperatures. Zürcher et al. [39] documented using low sintering processes for an all Cu interconnect.

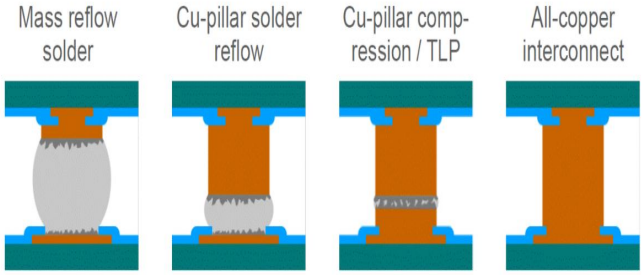


Figure 3.30: flip-chip interconnect trend [38]

Through the thesis work, the thermal conductivity of the Cu-Solder pillars was analyzed against Cu-Cu interconnects. The current TSMC pillars have 40 µm of Cu and 20 µm of solder (See Figure 3.31).

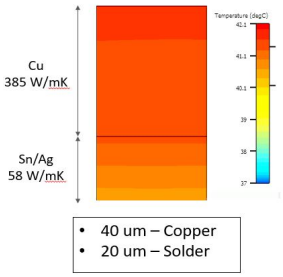


Figure 3.31: Cu-Solder dimensions and conductivity

The thermal conductivity of the 2 materials in series can be calculated via the series resistance formula.

$$\frac{L_{eq}}{K_{eq}} = \frac{L_{Cu}}{K_{Cu}} + \frac{L_{Sol}}{K_{Sol}} \tag{3.15}$$

The resulting thermal conductivity was 133 W/mK. This is roughly 66% less than the thermal conductivity of Cu. Therefore, an "All-Cu" interconnect would be a more thermally beneficial interconnect.

A simulation was performed with a single Type 1 pillar at the center of a hotspot source of 2 Watts. The area of the hotspot was reduced for each trial. Figure 3.32 shows the temperature reduction (from having no pillars) for Type 1 pillar with "All Cu" and Cu-solder materials.

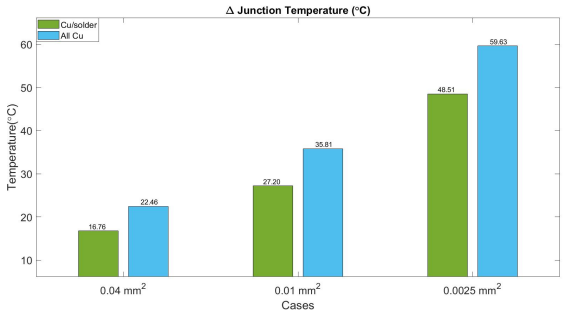


Figure 3.32: ΔJunction Temperature of Cu/Solder and All Cu with different areas

From the above figure, it is obvious that "All Cu" has a higher reduction in temperature due to its higher thermal conductivity. The results are also proportional to the increase in thermal conductivity. The temperature reduction in "All Cu" is 1.33 times greater than Cu-solder, which is to proves that the former has a 33% increase in thermal conductivity.

3.6.2. UNDERFILL THERMAL CONDUCTIVITY

The pillars are surrounded by a thermoplastic material which is called the underfill. The underfill is used to provide the mechanical bond from die to substrate, to provide protection to the pillars from mechanical stresses and also to correct the CTE mismatch from die to substrate [40].

Sun Lee et al. [41] studied the use of filler materials like silica and carbon in the underfill. The studies showed that the use of filler materials improved the thermal conductivity of the underfill by 1-2 W/mK.

The current underfill used is from Namics manufacturer. It is a capillary underfill (CUF) and the properties are shown in Table 3.12.

Thermal Conductivity [W/mK]	Viscosity [Pa·s]	Tg [°C]	Modulus of elasticity [GPa]	C.T.E $\leqq$ Tg [ppm]
0.9	55	95	12	22

Table 3.12: Underfill properties [42]

To understand the effect of this improvement to the whole thermal management of the IC, a set of simulations were performed. The simulation was for a uniform power of 2 Watts and 58 Cu pillars. Figure 3.33 shows the results for increasing the thermal conductivity of the underfill from 0.9 W/mK. The reduction in T_J is very minimal despite the conductivity increases by 2 times and 4 times. It is only when the thermal conductivity is increased to 10-20 W/mK that the reduction is pronounced. However, an underfill with such high thermal conductivity is extremely unlikely to exist. So the conclusion is that the emphasis is on the Cu pillars to act as the pathway for heat to flow from die to substrate.

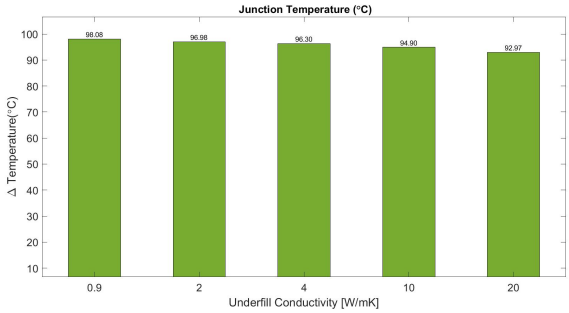


Figure 3.33: Junction Temperature of underfill with different thermal conductivity

3.7. MODEL CONSTRAINTS

The above experiments were completely modeled in a simulation platform. Therefore there are some limitations with each simulation which are discussed in this sub-section.

In Section 3.2 the characterization was done using the R_{th} method. The R_{th} is a simplified 1-D representation of heat flow in the model. This formula does not take into

account the heat flow in the lateral x and y directions. It therefore is not a very accurate representation for heat removal capabilities for pillars with different geometries. Another limitation is the pitch factor, the pitch has an effect on the heat flow but this cannot be interpreted from the R_{th} equation.

In Section 3.3 and in particular Table 3.11 shows the use of regression analysis to predict T_J as a function of pitch and density. These equations are based not only on the save test vehicle model but also on the boundary conditions that have been set. The numbers and weightages would therefore vary for different test vehicle setups and also different boundary conditions like ambient temperature, air-speed, power, etc.

In Section 3.4 the modeling in Ansys used a homogenized global model. This was done to save computational time and tedious steps in meshing individual pillars. This is an accurate comparison of stresses and warpage from the global level (viewed from silicon). To understand the stresses within the pillar design, local modeling is required. Thus an accurate representation of each layer involved in the pillar design should be taken into consideration to evaluate stresses at all levels. There is also a need for experimental data to validate at what stresses a particular failure type occurs. Another assumption made was the modeling utilized linear elastic structures. In reality materials such as underfill which are thermosets are viscoelastic in nature. In other words, time or rate dependent modeling is not being considered.

In Section 3.5 the placement of pillars is discussed. The conclusion was that pillars further away from the hotspot are thermally ineffective and its potential is canceled out due to the lateral heat spread in silicon. In the silicon there are metal connections from pillar to source (Alu cap layer, Alu plugs, etc.). This would mean that heat would be channeled through this layer which was not modeled in the simulations. Some of the manufacturer rules were also not met during the placement of pillars. Rules such as minimum copper percentage should be greater than 13% and minimum pitch/overlapping were not considered.

In Section 3.6 the "All Cu" pillars were modeled with the same dimensions as that of TSMC's pillars. There were no papers to justify "All Cu" having dimensions as TSMC.

All the above simulations modeled the pillar as Cu and solder cylinders. The shape is a topic of research as soldered pillars lose a bit of the stand-off height and also the shape. Another assumption made was that pillars compromised of Cu and solder only. In reality there are formations of Inter Metallic Compounds (IMC) between Cu and solder. Chen et al. [43] studied the failure caused by IMC progression and lifetime. To incorporate this into the thesis simulations, experimental data are needed for validation. Another assumption made was Joule heating through package material was also ignored.

4

CONCLUSION

Sigh! There goes another summer, Snoopy

Charlie Brown

The increase in power density will continuously lead to overheating of chips and decreases their reliability. Flip-chip packaging will therefore play a crucial role in improving the thermal management and increase the lifetime of such IC's. Through the thesis simulations the thermal importance of Cu pillars has been demonstrated. Moving forward with these results the following conclusions are drawn:

- Different pillar geometries can be ranked for the heat removal capabilities using the R_{th} equations. The novel designs showed the highest R_{th} as compared to TSMC's designs. Among TSMC's pillars, Type 4 was the best owing to the largest radius. This characterization will be useful for layout designers to pick pillars based on thermal benefits.
- The next set of simulations was on the variation in pillar geometry (i.e. width), pitch, and density. For different pillar geometries, the results were quite comparable with one another. The substantial increase in pillar density resulted in a T_J reduction of 1-2 °C. The reasons were the ratio of Cu:underfill did not increase significantly to improve overall thermal heat flow, the thermal resistance offered by the laminate, and the pillars placed away from the point of measurement. The small variations in pitch resulted in a small reduction in temperature. Finally, the results were summarized in a regression equation which can be used for different combinations of pitch and density*.
- The addition of novel designs was based on moving to finer pitches and tiny volume of Cu interconnects. The thermal performances were relatively comparable

*Only applicable for same boundary conditions

with TSMC's Type 1 pillar. However, the mechanical comparison showed that Type b faring the worst among the three. The conclusion drawn from this is in order to have comparable mechanical stresses, not only the pitch but also the radius needs to be scaled down together.

- The effect of pillar placements addresses a literature gap of non-uniform power density. Through the simulations, it can be concluded that pillar placements closer to the hotspot have a more pronounced effect.
- The last set of simulations discusses the future of the interconnect layer. It can be concluded that "All Cu" is proving to be thermally better than Cu-solder. The same cannot be said for the underfill, which needs its conductivity to be increased by 10 times and above for overall thermal improvements.

4.1. FUTURE SCOPE

The work done in this thesis has highlighted the thermal benefits of pillars in the IC layout. It also addresses the importance of mechanical simulations for the pillar's reliability. The following are some of the future works that can be carried on as a continuation of this thesis:

- **Topological Optimization (TO)**:In Section 3.5 the pillar placements are with respect to a single hotspot. In reality, IC products have multiple hotspots of varying intensities and sizes. It is a tedious process for the layout engineers to manually creates SiP files to address this issue. TO is one such automated process that optimizes layout and structure in a given 3D geometrical design like a package [44]. The TO will have the instructions and rules set by the manufacturer, the DRC checks used in layout tools, etc. and solve for optimum pillar placements. Multiple solutions can be generated and can then be evaluated.
- **Layout Optimization**: In Section 3.5, placing pillars at the center of the hotspot is seen as the optimal thermal solution. However, there are some restrictions with respect to the amount of Cu under a sensitive instance. This brings up a couple of new research topics. One of them is placing pillars with its positive thermal as well as negative effects on the mechanical and electrical domains and evaluating the trade-off. The other topic up for discussion is if high power density instances can be restructured in such a way that there is room created to accommodate a Cu pillar.
- **Laminate Optimization**: Section 3.5 shows that optimum pillar placements can have a significant impact on the thermal management of ICs. The laminate offers an obstruction to the flow of heat coming from the junction. Since the laminate is built up of metal layers of varying thickness and vias connecting them, an optimization of the entire laminate design would further help the heat flow. This would mean thicker metal layers near the junction to remove heat and vias directly under the pillars to transfer heat to the PCB in the shortest path possible.
- **Pillar Mechanical Tests**: Through the thesis work in Section 3.4, the preliminary comparison on a global level showed that there can be pillars going beyond TSMC's

rules. The next step is to evaluate the stresses and other mechanical tests on a local modeling scheme. This would involve a direct look into pillar stresses and also experimental data would be required to co-relate at what stresses a failure type occurs.

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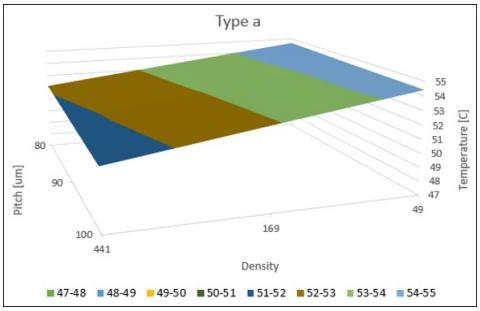
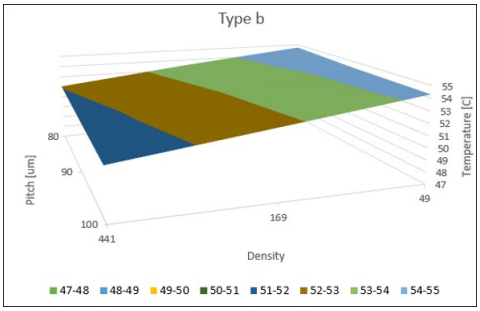
Appendices

A

SURFACE PLOTS OF PILLARS



(a) Type a surface plot



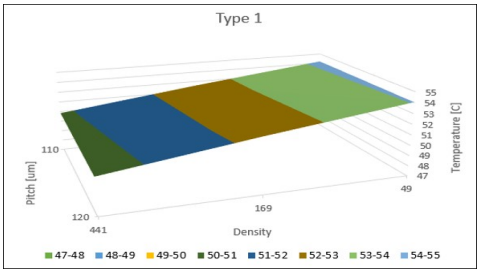
(b) Type b surface plot

Pitch [µm]	Density	$T_J[C]$
80	49	54.63
80	169	53.38
80	441	52.11
90	49	54.51
90	169	53.14
90	441	51.73
100	49	54.42
100	169	52.90
100	441	51.34

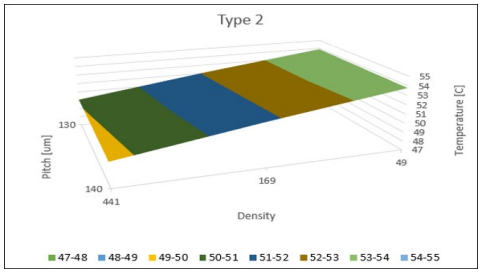
Table A.1: T_J of Type a pillar

Pitch [µm]	Density	$T_J[C]$
80	49	54.70
80	169	53.46
80	441	52.04
90	49	54.43
90	169	53.04
90	441	51.63
100	49	54.30
100	169	52.75
100	441	51.23

Table A.2: T_J of Type b pillar



(a) Type 1 surface plot



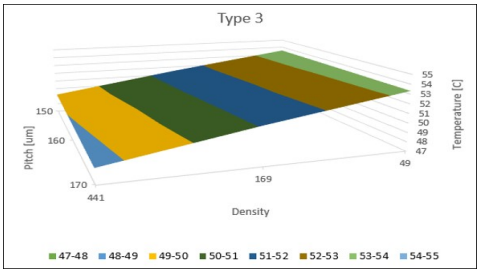
(b) Type 2 surface plot

Pitch [µm]	Density	$T_J[C]$
110	49	54.17
110	169	52.57
110	441	50.84
120	49	54.04
120	169	52.34
120	441	50.47

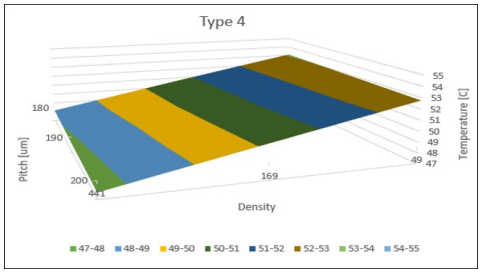
Table A.3: T_J of Type 1 pillar

Pitch [µm]	Density	$T_J[C]$
130	49	53.88
130	169	52.07
130	441	50.07
140	49	53.77
140	169	51.82
140	441	49.67

Table A.4: T_J of Type 2 pillar



(a) Type 3 surface plot



(b) Type 4 surface plot

Pitch [µm]	Density	$T_J[C]$
150	49	53.53
150	169	51.49
150	441	49.22
160	49	53.43
160	169	51.31
160	441	48.91
170	49	53.32
170	169	51.08
170	441	48.59

Table A.5: T_J of Type 3 pillar

Pitch [µm]	Density	$T_J[C]$
180	49	53.08
180	169	50.67
180	441	48.17
190	49	52.92
190	169	50.50
190	441	47.83
200	49	52.75
200	169	50.18
200	441	47.57

Table A.6: T_J of Type 4 pillar

B

Mechanical Data

B.1. UNIT CELL DATA

Pitch = 110um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	9199.6	8468.6	7589.6	6598.1	2539.9	958.09	232.91	104.12
E2 [MPa]	9199.7	8468.6	7589.6	6598.1	2539.9	958.09	232.91	104.12
E3 [MPa]	23940	23133	22345	21646	19312	18443	17771	17038
G12 [MPa]	2968.9	2722.5	2426.3	2094.1	778.82	289.39	69.847	31.185
G23 [MPa]	3417.2	3142.6	2812	2439.5	928.93	348.6	84.525	37.769
G31 [MPa]	3417.2	3142.6	2812	2439.5	928.93	348.6	84.525	37.769
nu12	0.32965	0.33088	0.33268	0.33509	0.34792	0.35418	0.35731	0.35788
nu13	0.12463	0.11874	0.11018	0.0989	0.042705	0.016874	0.004258	0.001986
nu23	0.12463	0.11874	0.11018	0.0989	0.042705	0.016874	0.004258	0.001986
aX [C^{-1}]	3.51E-05	3.75E-05	3.96E-05	4.15E-05	4.99E-05	5.61E-05	7.40E-05	7.43E-05
aY [C^{-1}]	3.51E-05	3.75E-05	3.96E-05	4.15E-05	4.99E-05	5.61E-05	7.40E-05	7.43E-05
aZ [C^{-1}]	2.26E-05	2.30E-05	2.32E-05	2.31E-05	2.18E-05	2.09E-05	2.05E-05	2.05E-05
Pitch = 120um								
Temp [C]	25	50	65.00	75	100	110	125	150
E1 [MPa]	8364.5	7691.6	6882.6	5971.9	2279.4	856.97	208.01	92.966
E2 [MPa]	8364.5	7691.6	6882.6	5971.9	2279.4	856.97	208.01	92.966
E3 [MPa]	20950	20200	19452	18769	16439	15575	14952	14325
G12 [MPa]	2790.3	2557.5	2277.6	1964	727.62	269.96	65.111	29.067
G23 [MPa]	3131.5	2876.9	2570.4	2225.7	840.31	314.24	76.071	33.982
G31 [MPa]	3131.5	2876.9	2570.4	2225.7	840.31	314.24	76.071	33.982
nu12	0.33911	0.34071	0.34305	0.3462	0.36288	0.37103	0.3751	0.37584
nu13	0.12807	0.12215	0.11352	0.1021	0.044527	0.017674	0.004469	0.002085
nu23	0.12808	0.12215	0.11352	0.1021	0.044527	0.017674	0.004469	0.002085
aX [C^{-1}]	3.64E-05	3.89E-05	4.12E-05	4.33E-05	5.25E-05	5.93E-05	7.87E-05	7.91E-05
aY [C^{-1}]	3.64E-05	3.89E-05	4.12E-05	4.33E-05	5.25E-05	5.93E-05	7.87E-05	7.91E-05
aZ [C^{-1}]	2.33E-05	2.37E-05	2.39E-05	2.39E-05	2.23E-05	2.12E-05	2.06E-05	2.06E-05

Table B.1: Type 1

Pitch = 80um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	11395	10519	9465.6	8271.7	3260.3	1242.1	303.35	135.72
E2 [MPa]	11395	10519	9465.6	8271.7	3260.3	1242.1	303.35	135.72
E3 [MPa]	30214	29283	28408	27674	25318	24429	23654	22695
G12 [MPa]	3415.5	3136	2799.9	2422	909.77	339.39	82.063	36.651
G23 [MPa]	4142.5	3819.5	3430	2989.4	1162.6	440.16	107.17	47.923
G31 [MPa]	4142.5	3819.5	3430	2989.4	1162.6	440.16	107.17	47.923
nu12	0.30404	0.30432	0.3047	0.30526	0.30874	0.31065	0.31165	0.31183
nu13	0.12502	0.11908	0.11048	0.09913	0.042756	0.016889	0.004261	0.001987
nu23	0.12502	0.11908	0.11047	0.099129	0.042756	0.016889	0.004261	0.001987
aX [C^{-1}]	3.25E-05	3.45E-05	3.62E-05	3.78E-05	4.46E-05	4.97E-05	6.44E-05	6.46E-05
aY [C^{-1}]	3.25E-05	3.45E-05	3.62E-05	3.78E-05	4.46E-05	4.97E-05	6.44E-05	6.46E-05
aZ [C^{-1}]	2.16E-05	2.19E-05	2.20E-05	2.20E-05	2.12E-05	2.06E-05	2.04E-05	2.04E-05
Pitch = 90um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	8433.1	7755.5	6940.8	6023.4	2300.9	865.32	210.07	93.888
E2 [MPa]	8433.1	7755.5	6940.8	6023.4	2300.9	865.32	210.07	93.888
E3 [MPa]	21202	20448	19695	19010	16675	15808	15180	14544
G12 [MPa]	2805.3	2571.4	2290.2	1975	731.98	271.62	65.516	29.248
G23 [MPa]	3156	2899.6	2591	2243.9	847.8	317.14	76.783	34.301
G31 [MPa]	3156	2899.6	2591	2243.9	847.8	317.14	76.783	34.301
nu12	0.3384	0.33996	0.34225	0.34533	0.36164	0.36961	0.3736	0.37433
nu13	0.12774	0.12181	0.1132	0.1018	0.044365	0.017605	0.004452	0.002077
nu23	0.12774	0.12181	0.1132	0.1018	0.044365	0.017605	0.004452	0.002077
aX [C^{-1}]	3.63E-05	3.88E-05	4.11E-05	4.31E-05	5.22E-05	5.90E-05	7.83E-05	7.86E-05
aY [C^{-1}]	3.63E-05	3.88E-05	4.11E-05	4.31E-05	5.22E-05	5.90E-05	7.83E-05	7.86E-05
aZ [C^{-1}]	2.32E-05	2.36E-05	2.38E-05	2.37E-05	2.22E-05	2.11E-05	2.06E-05	2.05E-05
Pitch = 100um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	10496	9677.7	8693.9	7581.1	2958.6	1122.3	273.55	122.35
E2 [MPa]	10496	9677.7	8693.9	7581.1	2958.6	1122.3	273.55	122.35
E3 [MPa]	27878	26994	26153	25433	23093	22214	21479	20605
G12 [MPa]	3234.7	2968.5	2648.4	2288.8	856.17	318.87	77.041	34.403
G23 [MPa]	3848	3544.3	3178.2	2764.9	1066.2	402.2	97.76	43.702
G31 [MPa]	3848	3544.3	3178.3	2764.9	1066.2	402.19	97.76	43.702
nu12	0.31425	0.31492	0.31588	0.3172	0.32448	0.32816	0.33001	0.33035
nu13	0.1238	0.11789	0.10933	0.09806	0.042186	0.016643	0.004196	0.001957
nu23	0.1238	0.11789	0.10934	0.098059	0.042186	0.016642	0.004196	0.001957
aX [C^{-1}]	3.34E-05	3.56E-05	3.75E-05	3.92E-05	4.66E-05	5.21E-05	6.79E-05	6.82E-05
aY [C^{-1}]	3.34E-05	3.56E-05	3.75E-05	3.92E-05	4.66E-05	5.21E-05	6.79E-05	6.82E-05
aZ [C^{-1}]	2.19E-05	2.23E-05	2.24E-05	2.24E-05	2.14E-05	2.07E-05	2.05E-05	2.05E-05

Table B.2: Type a

Pitch = 80um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	17163	15955	14509	12854	5420.2	2129.8	528.11	236.93
E2 [MPa]	17163	15956	14509	12854	5420.3	2129.8	528.12	236.94
E3 [MPa]	40718	39576	38559	37765	35372	34450	33499	32167
G12 [MPa]	4604	4242.2	3807	3314.8	1282.4	484.26	117.76	52.647
G23 [MPa]	6003.3	5570.8	5048.7	4453	1833.6	711.91	175.45	78.627
G31 [MPa]	6003.2	5570.8	5048.7	4453	1833.6	711.91	175.45	78.627
nu12	0.25649	0.2546	0.25166	0.24777	0.22753	0.21761	0.2126	0.21168
nu13	0.1443	0.13804	0.12888	0.11662	0.0526	0.021239	0.005418	0.002532
nu23	0.1443	0.13804	0.12888	0.11662	0.0526	0.021239	0.005418	0.002532
aX [C^{-1}]	2.81E-05	2.94E-05	3.06E-05	3.17E-05	3.61E-05	3.95E-05	4.90E-05	4.93E-05
aY [C^{-1}]	2.81E-05	2.94E-05	3.06E-05	3.17E-05	3.61E-05	3.95E-05	4.90E-05	4.93E-05
aZ [C^{-1}]	2.07E-05	2.09E-05	2.10E-05	2.11E-05	2.07E-05	2.04E-05	2.03E-05	2.04E-05
Pitch = 90um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	12711	11752	10600	9291.6	3715.4	1424.3	348.9	156.19
E2 [MPa]	12711	11752	10600	9291.6	3715.4	1424.3	348.9	156.19
E3 [MPa]	33214	32225	31311	30562	28207	27314	26491	25426
G12 [MPa]	3678.6	3380.1	3021	2616.8	988.82	369.77	89.507	39.983
G23 [MPa]	4565.6	4215.7	3793.6	3315.2	1305.4	496.85	121.27	54.254
G31 [MPa]	4565.6	4215.7	3793.6	3315.2	1305.4	496.84	121.27	54.254
nu12	0.2901	0.28986	0.28945	0.28895	0.2871	0.28652	0.28629	0.28625
nu13	0.12806	0.12205	0.11332	0.10179	0.044154	0.017489	0.004418	0.002061
nu23	0.12806	0.12205	0.11332	0.10179	0.044154	0.017489	0.004418	0.002061
aX [C^{-1}]	3.12E-05	3.30E-05	3.46E-05	3.60E-05	4.22E-05	4.68E-05	6.00E-05	6.02E-05
aY [C^{-1}]	3.12E-05	3.30E-05	3.46E-05	3.60E-05	4.22E-05	4.68E-05	6.00E-05	6.02E-05
aZ [C^{-1}]	2.13E-05	2.16E-05	2.17E-05	2.17E-05	2.10E-05	2.06E-05	2.04E-05	2.05E-05
Pitch = 100um								
Temp [C]	25	50	65	75	100	110	125	150
E1 [MPa]	10496	9677.7	8693.9	7581.1	2958.6	1122.3	273.55	122.35
E2 [MPa]	10496	9677.7	8693.9	7581.1	2958.6	1122.3	273.55	122.35
E3 [MPa]	27878	26994	26153	25433	23093	22214	21479	20605
G12 [MPa]	3234.7	2968.5	2648.4	2288.8	856.17	318.87	77.041	34.403
G23 [MPa]	3848	3544.3	3178.2	2764.9	1066.2	402.2	97.76	43.702
G31 [MPa]	3848	3544.3	3178.3	2764.9	1066.2	402.19	97.76	43.702
nu12	0.31425	0.31492	0.31588	0.3172	0.32448	0.32816	0.33001	0.33035
nu13	0.1238	0.11789	0.10933	0.09806	0.042186	0.016643	0.004196	0.001957
nu23	0.1238	0.11789	0.10934	0.098059	0.042186	0.016642	0.004196	0.001957
aX [C^{-1}]	3.34E-05	3.56E-05	3.75E-05	3.92E-05	4.66E-05	5.21E-05	6.79E-05	6.82E-05
aY [C^{-1}]	3.34E-05	3.56E-05	3.75E-05	3.92E-05	4.66E-05	5.21E-05	6.79E-05	6.82E-05
aZ [C^{-1}]	2.19E-05	2.23E-05	2.24E-05	2.24E-05	2.14E-05	2.07E-05	2.05E-05	2.05E-05

Table B.3: Type b

B.2. WARPAGE AND STRESS COMPARISON

	Warpage [um]		
	125 [C]	100 [C]	25 [C]
Type 1_110um	2.25	10.38	28.56
Type 1_120um	2.08	10.21	28.38
Type a_80um	2.65	10.75	28.92
Type a_90um	2.31	10.44	28.62
Type a_100um	2.09	10.22	28.4
Type b_80um	3.49	11.35	29.51
Type b_90um	2.86	10.92	29.09
Type b_100um	2.5	10.61	28.79

Table B.4: Warpage data

	Max Sigma Z Stress [MPa]			Min Sigma Z Stress [MPa]		
	125 [C]	100 [C]	25 [C]	125 [C]	100 [C]	25 [C]
Type 1_110um	2.23	7.42	18.69	-5.4	-29.32	-125.54
Type 1_120um	2.09	7.01	17.85	-4.98	-27.73	-120.76
Type a_80um	2.52	8.27	20.48	-6.28	-32.32	-134.41
Type a_90um	2.27	7.55	18.98	-5.54	-29.83	-127.08
Type a_100um	2.1	7.04	17.93	-5.01	-27.88	-121.19
Type b_80um	3.24	9.84	23.57	-8.02	-37.22	-147.33
Type b_90um	2.68	8.69	21.36	-6.72	-33.69	-138.24
Type b_100um	2.41	7.95	19.81	-5.94	-31.23	-131.25

Table B.5: Sigma-z stress data

	Max Max. Principal Stress [MPa]			Min Max. Principal Stress [MPa]		
	125 [C]	100 [C]	25 [C]	125 [C]	100 [C]	25 [C]
Type 1_110um	2.76	22.22	117.25	0.41	2.48	-10.44
Type 1_120um	2.6	21.57	115.02	0.41	2.76	-8.46
Type a_80um	3.11	23.84	121.87	0.42	1.69	-15.45
Type a_90um	2.81	22.46	118.02	0.41	2.37	-11.18
Type a_100um	2.61	21.63	115.21	0.41	2.74	-8.63
Type b_80um	3.9	27.91	129.85	0.46	-0.56	-26.96
Type b_90um	3.29	24.79	124.07	0.43	1.2	-18.25
Type b_100um	2.97	23.18	120.15	0.42	2.02	-13.44

Table B.6: Max. Principle stress data

	Max Equivalent Stress [MPa]			Min Equivalent Stress [MPa]		
	125 [C]	100 [C]	25 [C]	125 [C]	100 [C]	25 [C]
Type 1_110um	5.87	34.62	170.37	0.13	7.28	50.44
Type 1_120um	5.43	33.33	166.06	0.13	7.22	49.66
Type a_80um	6.79	37.15	177.99	0.13	7.36	52.3
Type a_90um	6.02	35.05	171.74	0.13	7.27	50.73
Type a_100um	5.47	33.45	166.42	0.14	7.22	49.72
Type b_80um	8.65	42.11	187.5	0.17	8.46	56.83
Type b_90um	7.26	38.46	181.06	0.14	7.57	53.35
Type b_100um	6.44	36.22	175.36	0.13	7.29	51.56

Table B.7: Equivalent stress data

	Shear Stress [MPa]		
	125 [C]	100 [C]	25 [C]
Type 1_110um	1.53	17.20	83.83
Type 1_120um	1.44	16.58	82.04
Type a_80um	1.76	18.60	87.15
Type a_90um	1.56	17.43	84.42
Type a_100um	1.45	16.63	82.19
Type b_80um	2.34	21.58	91.40
Type b_90um	1.89	19.35	88.53
Type b_100um	1.67	18.06	85.98

Table B.8: Shear stress data

C

Pillar Placements Data

	Area [mm^2]	$T_{J\text{-center}}$ [C]	$T_{J\text{-left/right}}$ [C]	$T_{J\text{-top/bottom}}$ [C]
No Pillars	0.04	107.73	56.13	57.89
58 pillars at 770um	0.04	99.47	51.88	53.08
4 pillars at 220um	0.04	97.16	51.51	52.67
12 pillars at 220um	0.04	94.87	51.18	52.29
4 pillars at 110um	0.04	95.02	51.38	52.52
Pillar at Center	0.04	86.99	51.59	52.76
No Pillars	0.01	136.76	56.18	57.94
58 pillars at 770um	0.01	128.04	51.88	53.08
4 pillars at 220um center	0.01	125.46	51.51	52.67
12 pillars at 220um from corners	0.01	122.92	51.18	52.29
4 pillars at corner	0.01	123.40	51.40	52.55
Pillar at Center	0.01	105.75	51.42	52.56
No Pillars	0.0025	173.86	56.06	57.81
58 pillars at 770um	0.0025	163.25	51.79	52.99
4 pillars at 220um center	0.0025	160.23	51.51	52.67
12 pillars at 220um from corners	0.0025	157.30	51.18	52.29
4 pillars at corner	0.0025	157.89	51.41	52.55
Pillar at Center	0.0025	121.68	51.28	52.41

Table C.1: Pillar placements with respect to hotspot area

	Power [W]	$T_{J\text{-center}}$ [C]	$T_{J\text{-left/right}}$ [C]	$T_{J\text{-top/bottom}}$ [C]
No Pillars	2	107.73	56.13	57.89
58 pillars at 770um	2	99.47	51.88	53.08
4 pillars at 220um	2	97.16	51.51	52.67
12 pillars at 220um	2	94.87	51.18	52.29
4 pillars at 110um	2	95.02	51.38	52.52
Pillar at Center	2	86.99	51.59	52.76
No Pillars	1	70.45	46.54	47.40
58 pillars at 770um	1	66.79	44.46	45.05
4 pillars at 220um center	1	65.77	44.28	44.85
12 pillars at 220um from corners	1	64.76	44.11	44.66
4 pillars at corner	1	64.84	44.22	44.78
Pillar at Center	1	61.38	44.32	44.90
No Pillars	0.5	53.38	41.81	42.24
58 pillars at 770um	0.5	51.59	40.74	41.03
4 pillars at 220um center	0.5	51.10	40.64	40.93
12 pillars at 220um from corners	0.5	50.62	40.56	40.84
4 pillars at corner	0.5	50.67	40.61	40.89
Pillar at Center	0.5	49.05	40.67	40.95

Table C.2: Pillar placements with respect to hotspot power source

D

All Cu and Underfill Analysis

	Area [mm^{2}]	Cu/Solder	All Cu
		$T_{J\text{-center}}$	$T_{J\text{-center}}$
Base case	0.04	107.73	107.73
Single pillar	0.04	90.97	85.27
Base case	0.01	70.52	70.52
Single pillar	0.01	109.56	100.954
Base case	0.0025	53.33	53.33
Single pillar	0.0025	125.35	114.226

Table D.1: All Cu vs Cu/Solder with varying hotspot area

	Power [W]	Cu/Solder	All Cu
		$T_{J\text{-center}}$	$T_{J\text{-center}}$
Base case	2	107.73	107.73
Single pillar	2	90.97	85.27
Base case	1	70.52	70.52
Single pillar	1	63.30	60.69
Base case	0.5	53.33	53.33
Single pillar	0.5	50.00	48.74

Table D.2: All Cu vs Cu/Solder with varying hotspot power

	58 Pillars at 770 um				
Underfill's k [W/mK]	0.9	2	4	10	20
$T_{J\text{-center}}$	98.08	96.98	96.30	94.90	92.97

Table D.3: Effect of Underfill's thermal conductivity