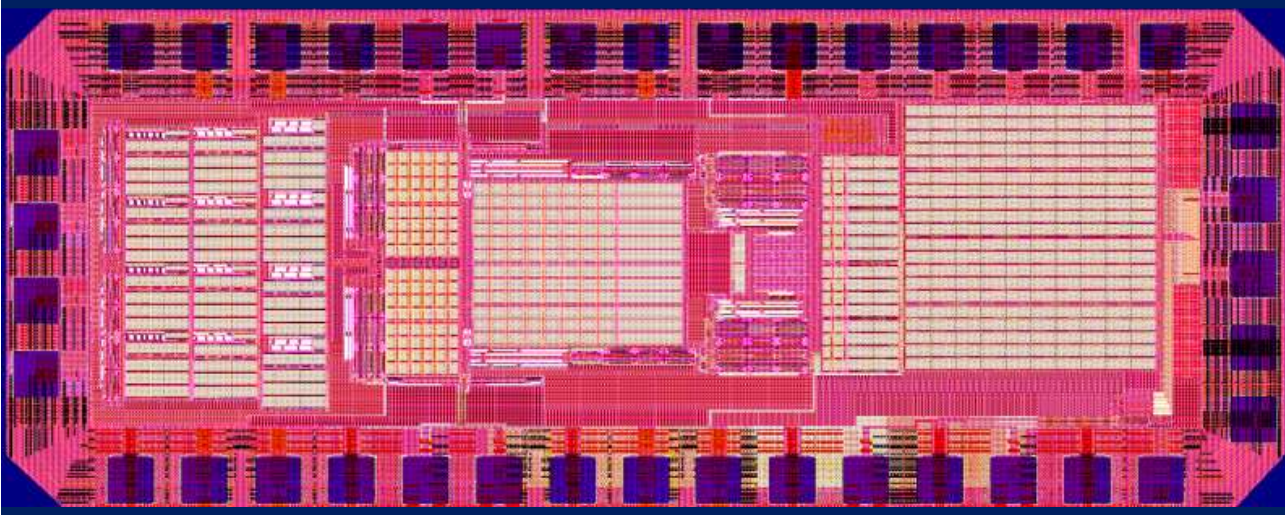
DESIGN AND IMPLEMENTATION OF A LOW POWER MIXER-FIRST RECEIVER FOR IEEE 802.11 ah STANDARD

Madhumitha Jayavel



TU Delft

Design and implementation of a Low Power Mixer-first Receiver for IEEE 802.11ah standard

Thesis

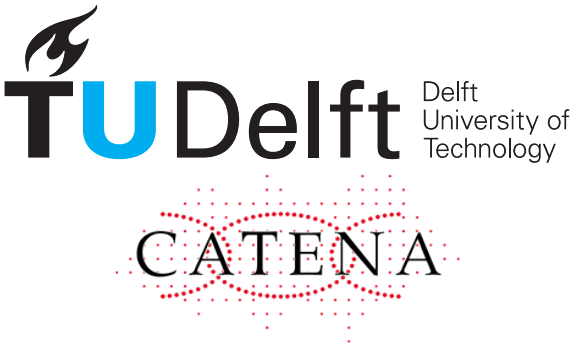
to obtain the degree of Master
at Delft University of Technology,
publicly defended on

by

Madhumitha Jayavel

Master Committee members:

Dr. M. Spirito,	Technische Universiteit Delft
Dr. M. Babaie,	Technische Universiteit Delft
Dr. F. Sebastiano,	Technische Universiteit Delft
Mr. J. Olink,	Catena Microelectronics B.V.
Mr. M.A. Montazerolghaem ,	Technische Universiteit Delft.



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Madhumitha Jayavel
Delft, October 2020

Contents

Summary

Can machines talk?, is the cornerstone question that has led to the development of today's communication field. Internet of things (IoT) is one such technology developed that allows different machines to communicate with each other, for the benefit of humankind. IoT has emerged as a standard technology welcomed by people into their homes, now more than ever. IoT has its applications varying from normal house gate opening system to monitoring gas leakages in a big nuclear power plant. They primarily need to support wideband operations with low power. With the growing demand towards low power applications, the thesis focuses on implementing a low power receiver design for IoT application. To support the specified frequency range and power consumption requirements, a mixer First receiver architecture is proposed. In the proposed architecture, the main power-consuming block of the RX chain, LNA, is removed. This serves as the first stage, providing input impedance matching and reducing the noise factor for the rest of the receiver chain. For the proposed mixer first architecture, different design strategies are used to provide input impedance matching, and also to maintain a low noise operation. The receiver design is aimed for IEEE 802.11ah standard. Thus, the receiver configuration is based on the standard requirement. A reconfigurable ZIF/LIF architecture is designed. The baseband of the receiver supports a 3^{rd} order filtering with power consumption of 4 mW. The designed receiver is implemented in a TSMC 40 nm and is in fabrication process.

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Introduction

IoT refers to a network of connected devices that exchange data for different applications using different wireless standards such as Cellular, ZigBee, Bluetooth, Mesh Networks, and the widely used Wireless Fidelity (WiFi). Most WiFi standards, such as a, b, g, n, and ac, operate at 2.4/5 GHz frequency bands. However, with this relatively high operating frequency, WiFi transceivers are power-hungry and have a low coverage range. To increase the relatively short range of WiFi, explicitly for IoT applications that do not require high data rates but require long-range data transmission and low power operation, a sub 1GHz WiFi standard - 802.11ah - was introduced. The 802.11ah standard performs better than the high-frequency networks in terms of penetration through obstacles, short and busty data transfer over long distances. Every wireless communication system consists of a transmitter at the source which modulates the information into a medium, and a receiver which reproduces the information at the destination. The thesis focuses on the **receiver design for the WiFi 802.11ah standard**.

This chapter explains why and how, among these different communication standards, the WiFi 802.11ah is more appropriate for the IoT application. This is followed by an overview of the 802.11ah standard along with the specifications. Using these requirements later in the chapter, system-level receiver design specifications are derived using MATLAB toolbox and theoretical equations. Further, the state-of-the-art designs for the 802.11ah standard are summarized. Finally, the structure of the entire thesis report is outlined.

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1.1. Background

WiFi 802.11ah, also called as HaLow, operates in frequency bands below 1 GHz, allowing wider coverage area. Theoretically, for an electromagnetic wave $\lambda = c/f$ (c is the speed of light), the lower the frequency (f) of operation, the larger is its wavelength (λ). During signal propagation, different loss mechanisms, such as attenuation, diffraction, and multipath affect the signal strength and properties. The free-space path loss is inversely proportional to the square of the wavelength. Thus, low-frequency signals can travel farther covering up to a kilometer in the case of 802.11ah. The long wavelength signals provide good penetration through obstacles, but the low-frequency band of operation implies a slower speed of data transmission. For 802.11ah, the data rate is improved from 150 Kbps to 78 Mbps for a single transmit antenna, by increasing the bandwidth from 1 MHz to 16 MHz [1]. Energy efficiency is also an important criterion for IoT networks. The large number of sensor modules in the network needs to serve for a long lifespan, without the constant need for battery replacement. 802.11ah achieves communication among a larger number of devices with low power consumption because of improvements to its PHYsical (PHY) and Medium Access Control (MAC) layers. WiFi 802.11ah is not the sole available standard, other technologies like LoRa and sigFox aim for IoT application as well. Table 1.1 lists down the key specification for different standards [2],[3]. From the comparison, it can be seen that WiFi 802.11ah satisfies most of the requirements for long-range IoT applications.

Technology	Frequency	Max. Data rate	Max. Range	Power consumption	Cost
WiFi HaLow	Sub-1GHz	346 Mbps	1 km	Low	Low
ZigBee	2.4 GHz, Sub-1GHz	250 kbps	100 m	Low	Low
Bluetooth Low Energy	2.4 GHz	1 Mbps	50 m	Low	Low
Bluetooth Low Energy	2.4 GHz	1 Mbps	50 m	Low	Low
LoRa	867-928 MHz	50 kbps	25 km	Low	Low
sigFox	868-902 MHz	1 kbps	40 m	Low	Medium

Table 1.1: Different technologies used for IoT applications.

1.2. Overview: IEEE 802.11ah standard

WiFi 802.11ah standard was developed in 2016 to support long-range data transmissions in the sub-1GHz frequency band by the IEEE computer society. It operates in different frequency bands in different countries (Appendix A). A frequency range between 863-930 MHz can license operation in significant countries, such as Europe, the USA, and Japan. It provides flexible bandwidths (1/2/4/8/16 MHz), different modulation schemes (BPSK/QPSK/16,64,256QAM), and 11 modulation coding schemes (MCS). The standard's key points, required for the design of the receiver chain are stated in Table 1.2 [1]. With these requirements, the receiver design specifications are derived in further sections.

Frequency Band	Sub 1 GHz (400 MHz - 1000 MHz)
Bandwidth	1/2/4/8/16 MHz
Modulation	BPSK,QPSK, 16/64/256 QAM
Application	IoT
Minimum Sensitivity	-98dBm(1 MHz,BPSK)/-58dBm(16 MHz,256-QAM)
Adjacent Channel Rejection (ACR)	19dB(1 MHz,BPSK)/-9dB(16 MHz,256-QAM)
Non-Adjacent Channel Rejection (NACR)	35dB(1 MHz,BPSK)/7dB(16 MHz,256-QAM)
Maximum Input Power	-30dBm (all modulation schemes)
Maximum packet error rate (PER)	10% (256 octects)

Table 1.2: IEEE 802.11ah specifications.

1.3. System Design and Requirements

In general, for a radio frequency (RF) receiver system, the incoming signal from the antenna is first filtered by the band-select filter. It selects the desired frequency band and rejects the interference. For most of the RF applications, a surface acoustic wave (SAW) filter is used for the band selection. The filter requires very high selectivity at RF (high quality-factor (Q) value) along with tunable center frequencies, a property very difficult to implement in CMOS chips. The Q is defined as the ratio of the center frequency to the bandwidth. The RF signal is then amplified by the LNA, and to suppress the noise contribution of the following stages. Subsequently, the signal is downconverted to baseband (BB) frequency by mixers. It can be converted to zero intermediate frequency (ZIF) or low intermediate frequency (LIF) depending on the local oscillator (LO) frequency. The BB signal is further amplified and filtered for the desired channel, before converting the analog signal to the digital domain using an analog-to-digital converter (ADC).
Exploring the blocks of the receiver, different parameters such as gain, noise, filtering order, and linearity are required to decide the design parameters for the system. These requirements are calculated from the IEEE 802.11ah specifications using MATLAB models and theoretical equations. The thesis was done in collaboration with CATENA MICROELECTRONICS B.V. Hence, the receiver was designed to be compatible with their existing ADC design.

1.3.1. Gain specifications

The gain required for the receiver chain depends on the receiver sensitivity (802.11ah standard) and the utilized ADC. The gain control is required to meet the receiver sensitivity and blocker requirements, since the dynamic range for the ADC is limited. The input signal of a wireless system has unpredictable signal power variation over a wide dynamic range because of multi-path propagation, interference, and many other factors. For 802.11ah, the lowest receiver sensitivity value is -98 dBm for MCS-10 and the maximum input signal power is -30 dBm, resulting in a dynamic range of 68 dB. Thus, a gain control is required to narrow the input signal variation to avoid saturation at the ADC. For large signal input, the gain of the receiver chain has to be lowered using the programmable architecture

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and vice-versa for smaller signals. A 10 bit 40 nm sigma-delta ADC is considered for the calculations. The key parameters for the ADC are specified in Table.1.3.

Input frequency [IF]	[1.88,1.91,1.94] MHz
Signal to Noise ratio	[58.3, 61.3, -] dB
Input Peak Voltage	[550,770,-] mVpk

Table 1.3: ADC Specification.

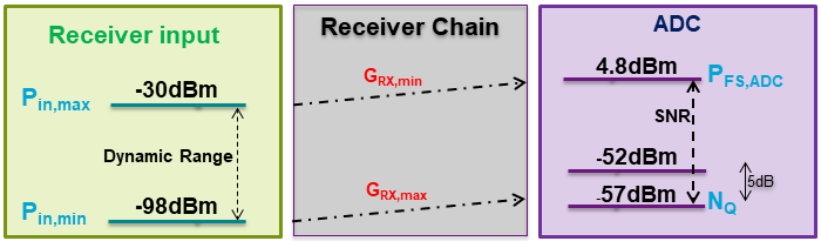

Figure 1.1: Signal levels along the system.

Minimum Gain: The maximum input signal power (-30 dBm) has to be amplified to map the full-scale input level of ADC. The full-scale input is the largest signal amplitude of the ADC, that can be delivered at the converter input, without saturation. This mapping gives the minimum required gain of the system. The input peak voltage from the specification is given as 550 mVpk, which corresponds to 4.8 dBm (P_{ADC}) for a 50 Ω reference impedance.

Input peak voltage P_{ADC} = 500 mVpk = 4.8 dBm; $\left[P_{dBm} = 10*\log\left(\frac{\left(\frac{(Vpk}{\sqrt{2}}\right)^2}{\frac{R}{1mW}}\right)\right]$

Maximum input signal P_{in} = -30 dBm;

A 10dB PAPR is assumed for OFDM. Thus, the necessary gain is 24.8 dB (P_{ADC}-P_{in}-PAPR).

Maximum Gain: It maps the amplification required for the minimum input signal (-98 dBm for MCS-10) to the minimum input level of the ADC. For small input power signals, the thermal and quantization noise dominates the noise floor of the ADC. This is considered as the minimum input level, and can be calculated from the full-scale input and signal-to-noise ratio (SNR). The theoretical equation for an ADC is given as, SNR = 6.02N + 1.76dB (over the Nyquist bandwidth). Thus, for a 10bit ADC, an SNR of 61 dB is considered. In the logarithmic scale, the quantization noise floor (N_Q) can be calculated by subtracting the full-scale signal power and the SNR value (P_{ADC} - SNR = -57 dBm). The minimum signal power of the ADC is considered as -52 dBm (5 dB higher than the calculated N_Q). Thus for -98

dBm receiver sensitivity and -52 dBm minimum input signal power, a gain of 46 dB is required.

Thus, the receiver architecture is required to have a programmable gain of 24 dB for the strongest signal to 46 dB for the weakest input signal(Figure.1.1).

1.3.2. SNR estimation for different MCS

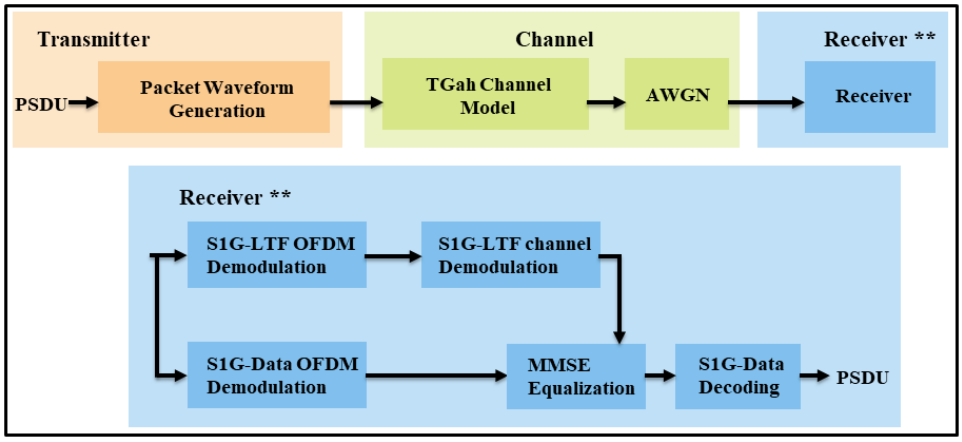

Figure 1.2: MATLAB transceiver and channel model for 802.11ah [4].

In the standard, a PER less than 10% for a packet length of 256 octets is considered to specify the receiver sensitivity, ACR, and NACR values [1]. When data is transmitted as a packet through a channel, the ratio of incorrectly received packets (one or more bit errors) to the total number of packets received is called packet error rate. A MATLAB model for 802.11ah transceiver, satisfying all specifications, along with indoor and outdoor channel loss parameters, is used for the analysis of PER against a varying SNR ratio for different bandwidths [4]. Along these lines, according to 802.11ah standard for a 10% PER, the required SNR for individual modulation scheme can be calculated. Fig.1.2 depicts the blocks used in the transceiver and the channel model.

At first, 256 octet packets of data are randomly generated in the transmitter block. These packets are aligned according to the specified data structure using the waveform generator (2.1.1), and time-synchronized with a known delay. The SNR values are swept and for each value, 10000 packets of short preamble data are transmitted. The packets are added with path loss (TGah non-line of sight indoor channel model) and additive white Gaussian noise in the channel section for practicality. In the receiver, the input data is initially time-synchronized. Using the LTF1 field, channel estimation is performed, and from ”data field”, the receiver data

is demodulated. Using delay synchronization, equalizer, noise estimator, and the channel state information, the transmitted data is recovered. This data is compared against the input, and the corresponding PER for the respective SNR is plotted in Fig.1.3 for different bandwidths.

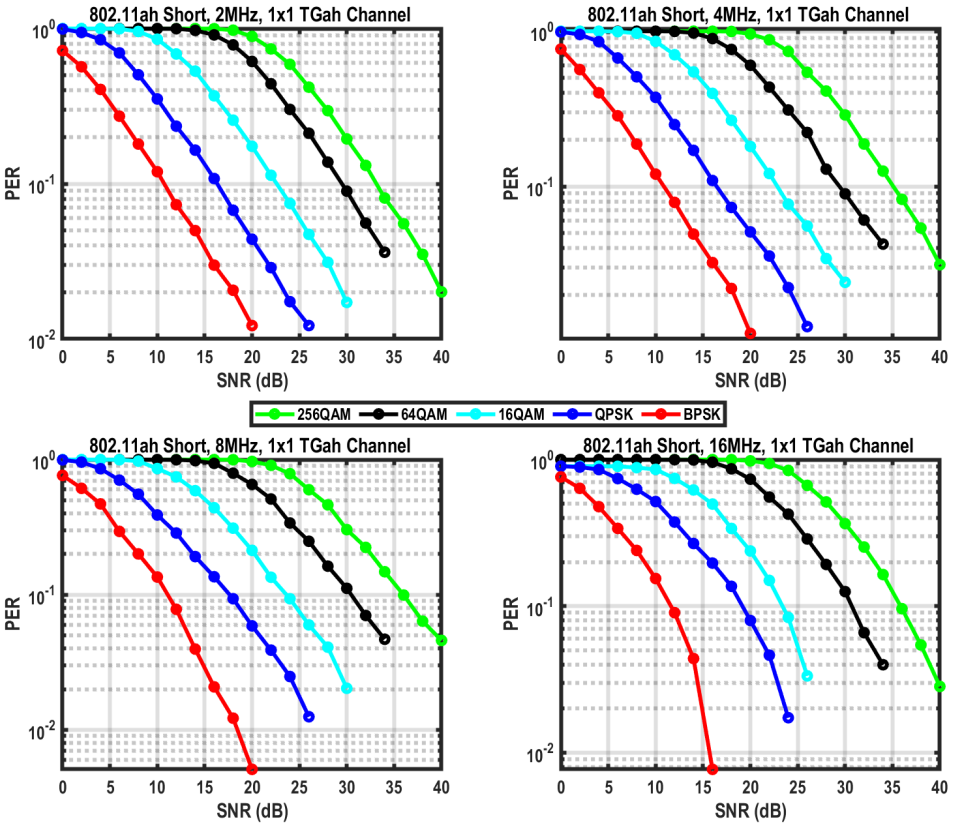

Figure 1.3: PER vs. SNR plots for different MCS.

The different modulation scheme from BPSK to 256 QAM denotes the increase in the number of information per symbol transmission within the given bandwidth. The higher-order modulation comes at the expense of decreased robustness to interference and noise. Hence, higher modulation schemes require a higher SNR ratio for a particular PER. The same trade-off is visible in the output plots. For 4 MHz bandwidth, BPSK modulation (one bit) requires an SNR of 11 dB, whereas for 256-QAM (8 bits) requires 35 dB SNR to achieve 10% PER for the same specifications.

1.3.3. Noise Figure

The ratio of the total output noise power (from amplifiers, mixers) of the RF system to the noise contributed by the input source (antenna) is defined as noise figure

(NF). It gives the quality of the system. Since the components in the system themselves introduce noise, the SNR at the output is lower than the SNR at the input of the system. Thus, the overall SNR (output SNR/input SNR) of the receiver decreases. The lower the value of the NF, the better is the performance of the receiver chain. Generally, if the input signal power is less than or equal to the noise power, it will not be detectable. Thus, it is necessary to have a maximum allowable NF for the receiver chain. The maximum noise degradation allowed for a receiver chain can be calculated with the receiver sensitivity value and the required SNR (calculated from 1.3.2). The detectable input signal power at the receiver input is given by the receiver sensitivity. The minimum power of the input signal is calculated from the desired output SNR across the operational bandwidth, with noise power added. Theoretically, $P_{sen} = -174dBm/Hz + NF + 10\log BW + SNR_{\min}$, where P_{sen} is the sensitivity, NF is the receiver total noise figure, BW is the signal bandwidth, SNR_{min} is the minimum required SNR, and the term −174dBm/Hz is the equivalent of 300K thermal noise of the 50 Ω input impedance. For 802.11ah standard, the receiver sensitivity for different modulation schemes and bandwidths is specified [1]. Thus, the calculated SNR values, and the standard values of the receiver sensitivity together can be used for the calculation of the maximum possible NF value. From Table.4.1, it can be seen that an NF < 7.46 dB is required from the receiver chain, calculated across the minimum SNR mode (BPSK) and maximum SNR mode (256 QAM).

Bandwidth	MCS mode	Modulation Type	SNR(dB)	10log(BW)	Min. RX Sens.(dBm)	NF(dB)
2MHz	0	BPSK - 1/2	11	63.01	-92	7.98
4MHz	0	BPSK - 1/2	11	66.02	-89	7.97
8MHz	0	BPSK - 1/2	11	69.03	-86	7.96
16MHz	0	BPSK - 1/2	11.5	72.04	-83	7.46
2MHz	8	256 QAM - 3/4	32.5	63.01	-69	9.48
4MHz	9	256 QAM - 5/6	35	66.02	-64	8.97
8MHz	9	256 QAM - 5/6	36	69.03	-61	7.97
16MHz	9	256 QAM - 5/6	36	72.04	-58	7.95

Table 1.4: Calculation of NF for different modes.

1.3.4. Baseband filtering order

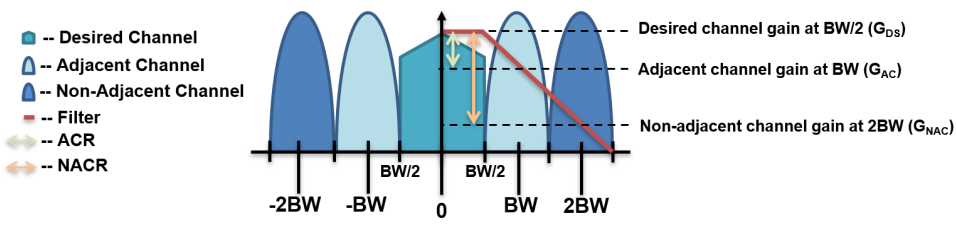

Figure 1.4: Channel distribution ZIF architecture.

The adjacent channel (neighbouring the desired channel) and non-adjacent channel (the alternate channel to the desired one) need to be rejected according to the

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802.11ah standard to properly receive the transmitted signal. The ACR and NACR values specify the required filtering order to be generated from the receiver chain. Consider a channel depiction of a ZIF architecture as in Fig.1.4. Each channel is considered to be bandwidth (BW) apart. The ACR is the ratio of gain from the desired channel 3dB bandwidth (BW/2) to the adjacent channel central frequency (BW). Similarly, for NACR, it is the ratio of 3dB bandwidth (BW/2) of the desired channel and the non-adjacent channel central frequency (2BW). The filtering slope can be calculated using the slope formulae as,

$$Filter_{roll-off} = \left(\frac{G_{DS} - G_{AC}}{\frac{BW}{2} - BW}\right) = \left(\frac{G_{DS} - G_{NAC}}{\frac{BW}{2} - 2BW}\right) \tag{1.1}$$

$$ACR = \frac{G_{DS}}{G_{AC}} \qquad NACR = \frac{G_{DS}}{G_{NAC}} \tag{1.2}$$

Using, the equations above, the filtering order can be expressed in terms of ACR and NACR.

$$Filtering/decade_{ACR} = \frac{ACR}{\log\left(\frac{BW}{\frac{BW}{2}}\right)} = \frac{ACR}{\log(2)} = 3.32 * ACR \tag{1.3}$$

$$Filtering/decade_{NACR} = \frac{NACR}{\log\left(\frac{2BW}{\frac{BW}{2}}\right)} = \frac{NACR}{\log(4)} = 1.66 * NACR \tag{1.4}$$

Modulation Type	Code Rate	ACR (dB)			NACR (dB)		
		1MHz	2MHz	Filtering	1MHz	2MHz	Filtering
BPSK	1/2 ×1/2	19	-	63.12	35	-	58.13
BPSK	1/2	16	16	53.15	32	32	53.15
QPSK	1/2	13	13	43.19	29	29	48.16
256 QAM	1/2	8	8	26.58	24	24	39.86

Table 1.5: Calculation of Filtering Order for different modes.

Table.1.5 gives the roll-off specifications, calculated using equations 1.3 and 1.4 across different modulation schemes. The maximum roll-off required is 63.12 dB, which leads us to the requirement of a 3rd order filter at BB of the receiver. The LIF architecture also results in similar specifications and requires a 3rd order BPF at BB.

1.3.5. Image Rejection Ratio

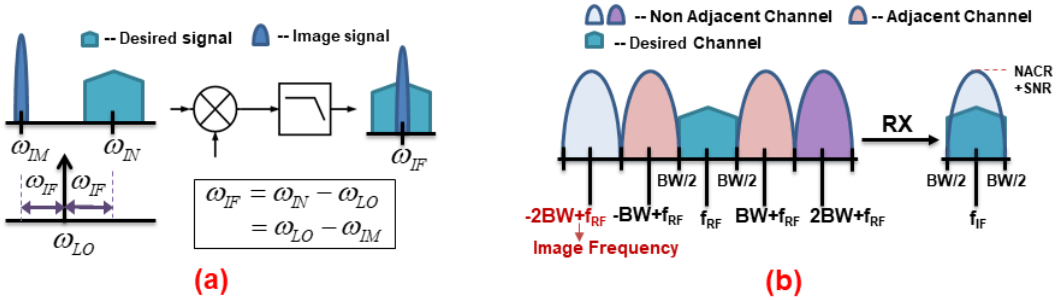

Figure 1.5: (a) Effects of image signal in LIF architecture (b) 802.11ah Waveform indicating Image frequency.

One of the major problems in a LIF architecture is the image signal. Consider a signal $cos(\omega_{IN}t)$ at the RF input. This is downconverted by LO signal $cos(\omega_{LO}t)$. The downconversion can be termed as a simple multiplication of the RF and LO signal ($cos(\omega_{IN}t) * cos(\omega_{LO}t)$). Thus, the BB signal after LPF equals $1/2 * cos(\omega_{IN} - \omega_{LO})t$ (Fig.1.5(a)). Since, $cos(\omega_{IN} - \omega_{LO})t = cos(-\omega_{IN} + \omega_{LO})t$, the desired signal at ω_{IN} above the ω_{LO} and the unwanted signal ω_{IM} at ω_{IN} below the ω_{LO} are both downconverted to the same BB frequency. This unwanted signal and its frequency are called the image signal and image frequency, respectively. This overlapping of desired and image signal, corrupts the information transmitted, and affects the NF of the receiver chain (Fig.1.5(a)). Thus, the image signal also needs to be filtered with a proper rejection ratio. Smaller the IF frequency, the closer, the image signal to the desired signal. Thus, a comparatively smaller IF frequency requires a higher rejection ratio (high-Q filter). The common solution to avoid this effect, is to use an image rejection filter in the analog or digital domain.

For 802.11ah, 1MHz bandwidth operation (smaller IF frequency), consider f_{RF} as *1.001GHz* and f_{LO} as *1GHz*. Thus, the desired signal at baseband after mixing lies at *1MHz (=1.001GHz-1GHz)*. In addition to the desired outputs, the image signal at f_{RF}*=999MHz* also falls in the same *1MHz (=1GHz-999MHz)* band (Fig.1.5(b)). The input image is located at the non-adjacent channel band (-2BW+f_{RF}) . Thus, a sharp filtering is not required. The amount of image rejection for different modulation schemes and bandwidths can be calculated as the sum of corresponding SNR and the NACR value. Table.1.6 calculates the required IRR value to be around 43 dB.

1.3.6. Linearity: IIP_n

Linearity is a critical parameter for both transmitter and receiver. In a receiver system, components such as LNA, mixer, and amplifiers contribute to non-linearity. In the case of an amplifier, the output power and input power should follow a linear line with a gain equivalent slope. However, CMOS based devices are inherently non-

Mode	Rate	NACR	SNR (dB)		IRR
			2MHz	4MHz	
BPSK	1/2	32	11	1	43
QPSK	3/4	27	16	16.5	43.5
16 QAM	3/4	20	23	23.5	43.5
256 QAM	5/6	7	34	36	43

Table 1.6: Calculation for the IRR for different modes.

linear, and saturation can result in unwanted signals at non-harmonic frequencies causing inter-modulation distortion (IMD). The standard performance parameter for linearity includes 1-dB compression (P1dB) point, second-order intercept (IP2), and third-order intercept point (IP3). For large blocker signals, the receiver experiences a gain compression because of the supply voltage limitation. The 1dB gain drop between the input and output signal power on a logarithmic plot is called P1dB. The IP2 and IP3 are signal levels of second and third-order products of IMD.

For 802.11ah, the maximum input signal of -30 dBm should be satisfied. Hence, the P1dB should be greater than -30 dBm. The specification for allowed IP2 and IP3 products (in-band) are calculated theoretically using power series expansion.

$$IIP_n = \frac{\Delta}{n-1} + P_{in} \tag{1.5}$$

Where IIP_n is the signal level of the n-th order IMD product, P_{in} is the power of the signal and ΔP is the difference between the signal strength and the noise floor. Thus, using the input signal power level and noise floor level, the intercept point specification can be derived. Theoretically, the noise floor can be calculated from the receiver sensitivity equation (*-174 + NF + 10log(BW)*). For a 1MHz bandwidth and 6 dB NF, the *noise floor = -108 dBm*. Consider the maximum signal power -30 dBm. The receiver amplifies the signal by gain (G_{RX}) and provides a 35 dB rejection (NACR). The signal level at the output is termed as OIP_n, and is equal to *-30 - 35 +* G_{RX}. Mapping it to the input by subtracting the gain, the input signal power (P_{in}) is -65 dBm. Substituting the values in Equation.1.5, Input second-order intercept (IIP2) is -22 dBm and Input third-order intercept point (IIP3) is -43 dBm.

1.4. State-of-the-art

802.11ah standard was launched in 2016 and with 5 years of launch, it is still not as popular as the other standards in its category. It faces tough challenges for adaptation because of the difference in frequency range compared to the widely used WiFi/Bluetooth applications. Few of the existing designs were studied and analysed for finding the challenges in the receiver design, and to understand the scope of the thesis (Table.5.10).

The receiver design from IMEC group is based on a current-mode RF front-end. Its analog baseband operates over the wide frequency band for 1,2 MHz MCS

0-4, and achieves the required filtering (ACR, NACR) by digitally assistance [5]. The work portrays excellent competitive results in terms of NF(6dB) and power consumption (4.4mW). However, the receiver is designed with off-chip elements such as inductors for current mode LNA, and FPGA for DC-offset calibration and automatic gain control. A ZIF receiver is implemented for narrow bandwidth 1,2 MHz 802.11ah application. However, the paper lacks information about flicker noise effect on NF .

Researchers from Tsinghua University have implemented a reconfigurable ZIF/LIF architecture for 1,2, and 8MHz bandwidth [6]. It uses an inductor-less active balun LNA and active double-balanced Gilbert mixer in the front end. In their work, a 4th order filter is implemented by a cascading the reversed Thomas-Tow Biquad filter and multi-feedback filter. It provides a programmable gain with required filtering, 4 dB NF and 12 mW power consumption. However, the paper lacks much information about the linearity performance of the receiver.

Another design from Navitas solution Korea demonstrates a LIF receiver for 2/4 MHz [7]. It consists of a passive I/Q mixer, similar to the idea proposed, but with input LNA block. It supports a 4th order filtering from the baseband for 65 dB gain and 8dB NF, costing 30mW power consumption.

The transceiver design from Palma ceia semidesign operates for the entire frequency range of 700MHz to 928MHz, supporting operation in all countries [8]. It also supports 4 MHz bandwidth along with the mandatory 1,2 MHz across all modulation schemes. The receiver provides a very low NF of 3dB, trading off with larger power consumption equaling to 22mW. However, the authors have not discussed circuit details of the receiver to understand the design trade-off.

	IMEC [5]	Tsinghua University [6]	Navitas Solutions [7]	Palma Ceia [8]	**Targeted Specification**
Frequency Band	755-928 MHz	750-930 MHz	868/915 MHz	755-928 MHz	**863-930 MHz**
Gain	23-83 dB	100 dB(max)	65 dB	-	**24-44 dB**
Bandwidth	1,2 MHz MSC 0-4	1,2,8 MHz	1,2,4 MHz	1,2,4 MHz	**1,2,4 MHz**
Filter Order	3rd Order	4th Order	4th Order	-	**3rd Order**
NF	6 dB	4 dB	8 dB	3 dB	**6 dB**
Power	4.4mW	12mW	30mw	22mW	**4 mW**
1dB	-18 dBm (min gain)	-	-	-10 dBm	**-30 dBm**
IIP3	-14 dBm	-	-	-17 dBm	**-48 dBm**
Architecture	Low IF	Zero IF/Low IF	Low IF	-	**Zero IF/Low IF**

Table 1.7: Overview of prior art and targeted specifications.

In the upcoming chapters, the receiver chain with the requirements will be implemented and simulated in the Cadence platform. Further, different design strategies are formulated to satisfy the strict NF, ACR, input impedance and gain specifications along with the intended low power consumption criterion. The designed system should also support a programmable gain (24 dB-46 dB) and programmable

bandwidth (1/2/4 MHz) architecture.

1.5. Thesis Outline

The report is divided into 6 chapters explaining the receiver design step by step. The following chapter-2, explains in detail about the overall receiver architecture including the mixer structure. Chapter-3 discusses the block level design of the ZIF and LIF architecture. It also explains the blocks added for the bandwidth and gain programmability. Chapter-4 shows the amplifier schematics used and the simulation results for the receiver design. Chapter-5 presents the layout details and the post-layout simulation results. Finally, chapter 6 concludes the report along with the future scope of the project.

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2

Reconfigurable (ZIF/LIF) Receiver design

The chapter explains the receiver architecture designed. The different types of receivers are discussed briefly and then a choice is made, compatible with the 802.11ah standard. The data structure of the standard is also discussed to analyse the waveform configuration across different bandwidths, for choosing the receiver architecture.

2.1. Receiver Architecture

The commonly used architectures for wireless communication are the Homodyne/ZIF and the LIF receivers. The first block of the conventional RX is an off-chip SAW filter (band-select filter). It offers rejection to out-of-band (OOB) interference with limited tunability. The proposed passive mixer-first receiver design based on N-path filter structure can provide good linearity and tunability (using the LO frequency) [1],[2]. The receiver's BB impedance provides the necessary filtering for the interference, and programmability of bandwidth and gain. A general description of the ZIF and the LIF structure is given below.

ZIF architecture downconverts the RF signal directly to zero frequency, removing the issue caused by the image signal (Fig.2.1(a)). The input signal at RF (point A) is band selected first to remove the OOB blockers. The LNA amplifies the signal, and the LO downconverts it to DC (point B and point c respectively). It requires only a simple lowpass filter (LPF) (point D) for channel selection (Fig.2.1(b)). The main disadvantage of ZIF receivers is flicker noise and DC offsets. Flicker noise is a low-frequency noise with 1/f power spectral density. It occurs in all electronic devices, especially in CMOS. Its value increases inversely to the frequency, thus it dominates all other noises in the low-frequency region.

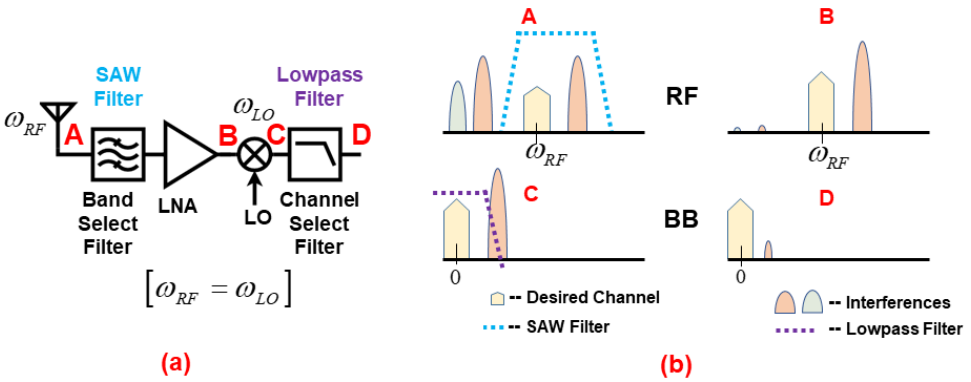

Figure 2.1: (a) ZIF Receiver. (b) Spectra at each stage of the ZIF receiver.

The frequency at which white noise dominates the flicker noise is called the flicker noise corner frequency (f_c). Since ZIF architecture operates around DC, it is sensitive to the flicker noise, corrupting the incoming weak signal. The LO signal can also leak to the mixer input, and cause self-mixing during the downconversion, resulting in a large DC term (Fig.2.2).

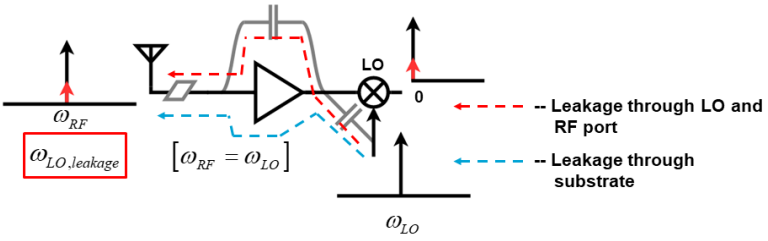

Figure 2.2: LO leakage in ZIF architecture.

The LO signals can leak to the antenna since both, the RF and the LO operate at the same frequency (Fig.2.2). The signal can leak to the antenna via two paths, denoted in Fig.2.2. The First path is through the parasitic capacitance of mixer to LNA output. It is then leaked to the antenna by the capacitance of between input and output of LNA. The Second path is through the substrate of the chip to the antenna. The leaked signal can be radiated and get reflected back to the same system. This causes self-mixing and a huge DC term at the output of the mixer. This DC offset can saturate the baseband amplifiers, affecting its functionality.

LIF architecture shown in Fig.2.3(a), first removes the OOB blockers, at point A, using the band-select filter. It then amplifies the signal and suppresses the noise through LNA, as shown at point B. It rejects the image in RF (point C), down-converts to IF (point D) and finally the channel select filter is applied to remove in-band blockers (point E) (Fig.2.3(b)). It downconverts the RF to low IF frequency. Downconversion to a non-zero frequency decreases the corruption caused by the flicker noise and DC offset to the signal.

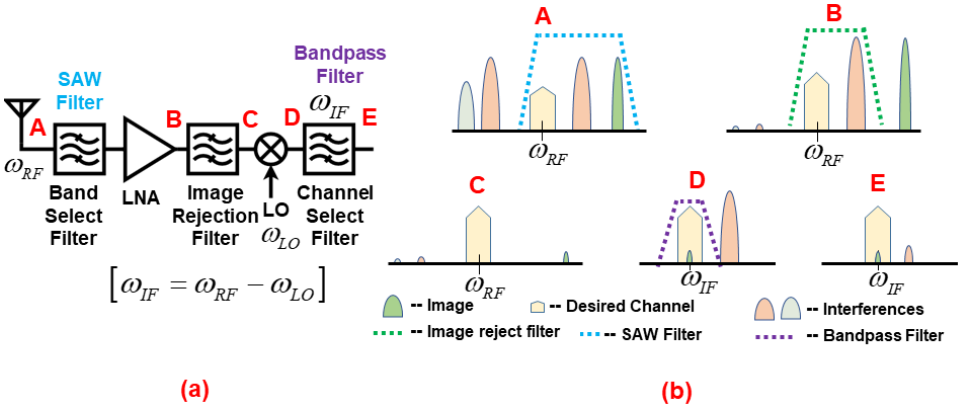

Figure 2.3: (a) LIF Architecture. (b) Spectra at each stage of the LIF receiver.

From this, we can choose the architecture, which causes less distortion to the signal (less noise). The 802.11ah data structure is analysed to understand the channel locations for different bandwidths.

2.1.1. 802.11ah Data Structure

With sub-1GHz spectrum operation, the standard enables a very narrow bandwidth and continuously spread channel. There are 9(10 for 1MHz) modes available under each modulation scheme for different coding rates. The information is transmitted as data through the PHY/MAC layers by orthogonal sub-carriers. The number and position of subcarriers vary with channel bandwidth. To understand in detail, the waveform configuration for different bandwidths is generated with the help of WLAN toolbox in MATLAB [3]. The important input parameters for the generator includes the bandwidth, modulation coding scheme, and also the physical layer conformance procedure (PLCP) protocol data unit (PPDU) format. The PPDU format can be broadly classified into three categories: S1G Long Format, S1G Short Format and S1G 1MHz Format, represented in Fig.2.4 (numbers written below the format structure denotes the symbol size of each field).

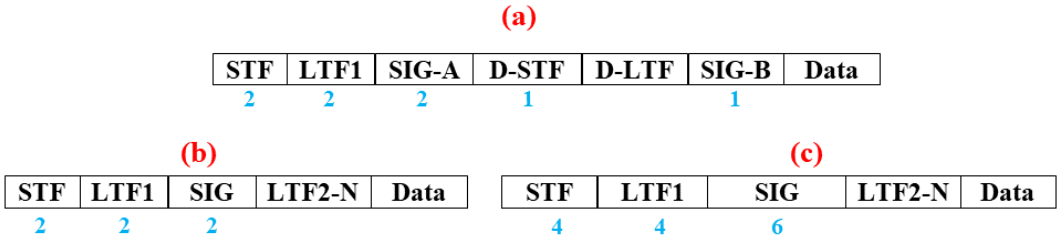

Figure 2.4: PPDU Field Structure : (a) S1G Long Format, (b) S1G Short Format, and (c) S1G 1MHz Format.

- **Long preamble higher bandwidth mode** - This mode can be used as

both single and multi-user transmission. From Fig.2.4, it consists of different fields, such as, STF for coarse synchronization, LTF1 for fine synchronization and initial channel estimate, SIG-A contains the transmission parameters, D-STF for gain control, D-LTF for MIMO channel estimation, SIG-B contains MCS information in multi-user mode, and the variable-length data field contains the data payload carriers,

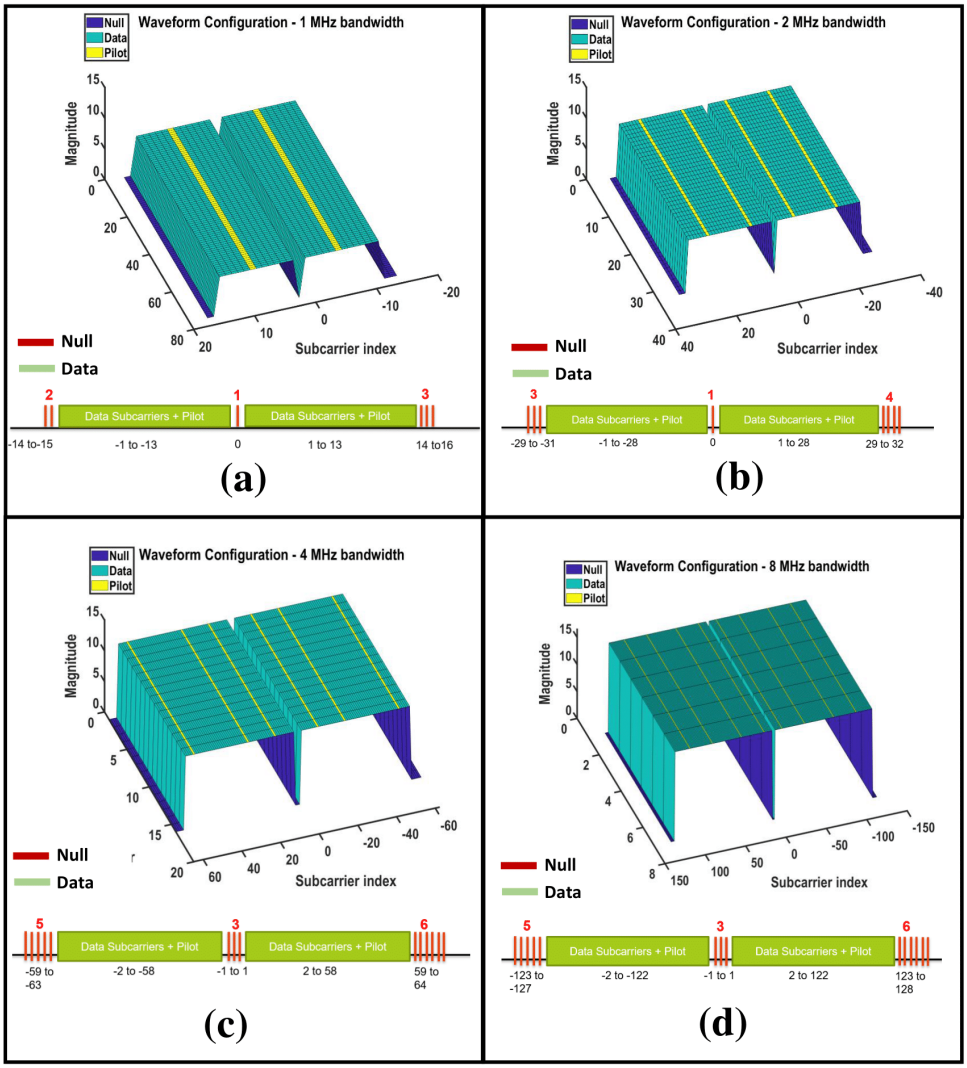

Figure 2.5: 802.11ah waveform representation (a) 1 MHz Bandwidth, (b) 2 MHz Bandwidth, (c) 4 MHz Bandwidth, and (d) 8 MHz Bandwidth.

- **Short preamble higher bandwidth (expect 1MHz) mode** - This mode is

a single-user transmission with fields and beamforming similar to long PPDU mode. Also, the PPDU consists of LTF2-N field, for subsequent MIMO estimations, shown in Fig.2.4 (b).

- **1MHz bandwidth mode for all modulation schemes** - They are targeted for low data rate applications. Fig.2.4 (c) shows the field structure for S1G 1MHz mode. It consists of an extended preamble to accommodate new modulation and code rates. Although it consists of similar fields, the number of symbols per field is higher, so it can achieve higher sensitivity.

A random value is created in MATLAB for 256 data length. It is aligned for S1G short PPDU mode for single transmission profile (1 transmitting antenna and 1 receiver antenna modelling) for BPSK modulation MCS 0 (code rate = 1/2) [3]. The created data set (PSDU) is fed to WlanWaveformGenerator available in MATLAB toolbox. The toolbox supports only short preamble data format. The generator modulates the data and adds an OFDM window. The output data is extracted from the time domain with the knowledge of the preamble sizes. It consists of information about the location, and number of data, pilot and null subcarriers for individual bandwidths. The output plot for the 1 MHz bandwidth, can be visualized from Fig. 2.5(a). Similarly, for other bandwidths, the outputs are shown in Fig.2.5(b),(c),(d).

The application for WiFi HaLow lies in both outside and inside environment. For outdoor conditions, the vehicular motion is compensated for doppler spread, using travelling pilots. The previous standards used, the constant pilot locations at the same subcarriers for the transmission time. Whereas, travelling pilots were introduced in 802.11ah. These could change subcarrier locations across time and can be very effective in tracking the varying channel conditions. Fig.2.6 depicts the plots for traveling pilot locations. It can be noticed that even with travelling positions, the null location of subcarriers does not change.

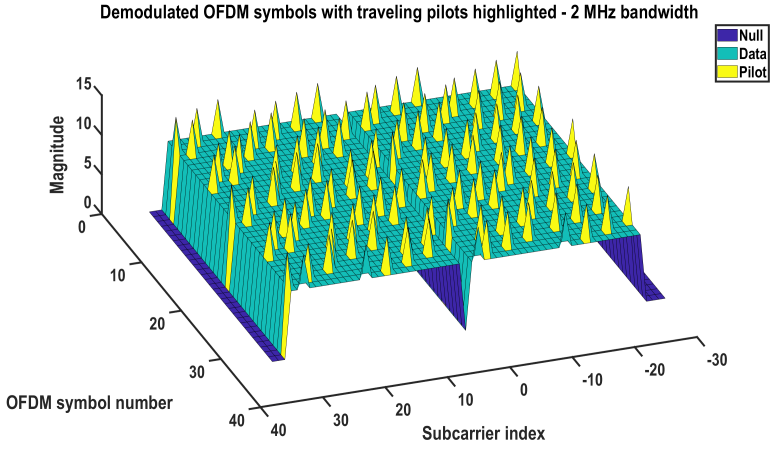

Figure 2.6: Travelling pilot per OFDM symbol.

2.1.2. Design choice : Reconfigurable architecture

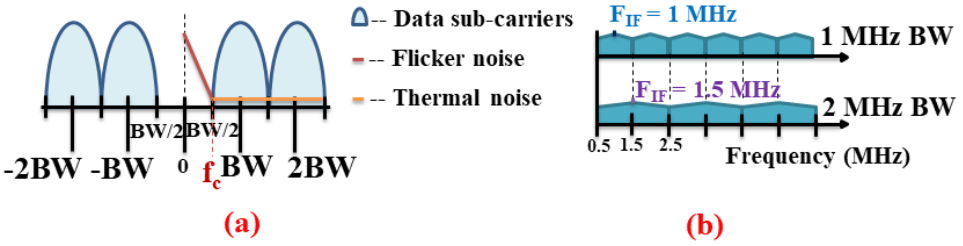

Figure 2.7: (a) Flicker noise depiction (1 MHz BW). (b) 802.11ah channel arrangement (1/2 MHz BW).

With knowledge about the location of null data and data carriers, calculations are performed to analyse the waveform in the time domain. For sub-1GHz 802.11ah, the guard intervals (GI) between the subcarriers are 8 μs or 4 μs. For all bandwidth modes, the tone spacing between adjacent sub-carriers is 31.25 kHz [4]. The DFT/IDFT period for a subcarrier frequency spacing of 31.25 kHz is 32 μs. Depending upon the guard interval, each OFDM symbol duration is 40 μs or 36 μs (GI+DFT/IDFT). All modulation schemes for bandwidth 1MHz and 2MHz configuration have only one null at zero frequency. Thus only 15.6 kHz (31.25/2 kHz) is the margin available from zero. This can be considered as the f_c required from the design to have a similar SNR ration for all data subcarriers (Fig.2.7(a)). This low f_c is very challenging to achieve in CMOS technology. Thus, a LIF architecture is proposed for low data bandwidth (1 MHz and 2 MHz) to improve the NF of the circuit. BW/2 (1 MHz/2) is considered as the feasible f_c, for 1 MHz bandwidth. Thus, the desired signal is spread between 500 kHz and 1.5 MHz. A IF frequency (f_{IF}) = 1 MHz is considered as the baseband configuration. Considering the same starting point, for 2 MHz bandwidth, the desired signal is between 500 kHz to 2.5 MHz with f_{IF} = 1.5 MHz (Fig.2.7(b)). For 1 MHz bandwidth, only 26 subcarriers (data and pilot) per OFDM symbol, carry information. However, for higher bandwidths, the number of data and pilot tones increases (114 for 4 MHz, and 242 for 8 MHz bandwidth). The number of nulls at DC is also higher (3 for 4 MHz), so a simple ZIF architecture can be used. The thesis focuses on the design of a **reconfigurable ZIF/LIF architecture for 1/2/4 MHz bandwidth**. For the programmable architectural design, the circuit designs are inextricably linked.

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3

Block level Receiver design

The chapter introduces the implemented receiver architecture design, by explaining about each of its blocks. A SAW-less receiver with a mixer-first design is proposed for this thesis. Starting with the theory of the proposed mixer-first receiver along with its properties and the equations governing, are described. The downconverted signal is to be filtered, and amplified in the BB domain. The ZIF design, comprising of the active 2^{nd} order filter, followed by the single-pole active LPF, is explained (Figure.3.1(a)). For the LIF architecture, the first block is the BPF, followed by the image rejection filter (polyphase filter (PPF)) and notch filter (Figure.3.1(b)). All these blocks are discussed, along with the equations governing it.

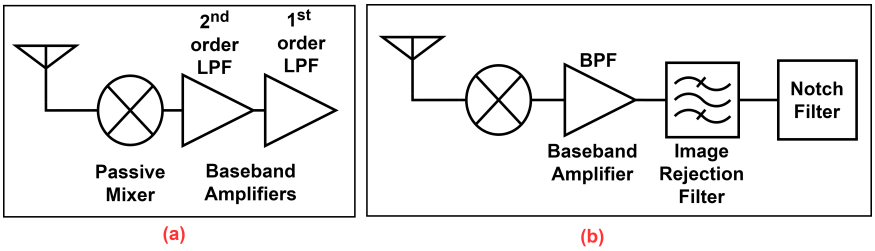


Figure 3.1: (a) ZIF architecture (b) LIF architecture.

3.1. N-path filter

A N-path filter offers channel selection at RF. It should provide good selectivity (high-Q) and wideband operation. The N-path filter provides a high-Q BPF, similar to SAW/BAW filters, along with programmable center frequency [1]. It is also CMOS friendly, as it consists of only switches and capacitors.
A narrow bandpass shaped filtering can be realized by downconverting the RF current to BB, then lowpass filtering the BB current, creating BB voltage and finally

upconverting the current (Fig.3.2(a)). Thus, the switch provides the necessary up and down-conversion of BB voltage to RF. The switches are considered ideal, except for the on-resistance (r_{on}). The r_{on} is cumulated for all the paths and added as a single entity, since only one switch is active at a time. The r_{on}, antenna source resistance R_S, and the capacitance (C) form the BB LPF. The time constant for the r_{on}, R_S and C is designed larger than the switching period (T_{LO}). For an input signal frequency equal to the LO frequency, the capacitors after many settling periods, track the average DC value of the input. Whereas, for other input frequencies, the output is zero. In this way, the BPF functionality can be observed. The switches are controlled using the LO signals. With non-overlapping LO waveforms, as shown in Fig.3.2(b), only one path is conducting at a time. By varying the LO frequency, the BPF frequency of operation can be changed.

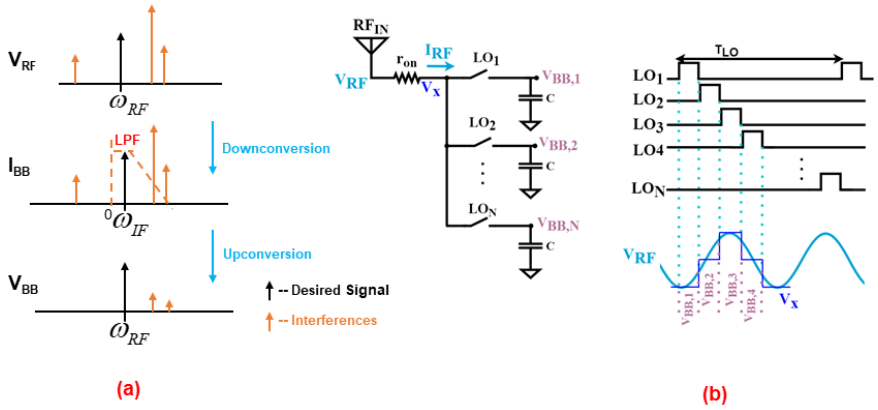


Figure 3.2: (a) Narrow BPF. (b) N-path passive mixer and LO waveform.

Thus at RF input a narrow BPF with center frequency $f_{c,N-path} = 1/2.\pi.N.R_S.r_{on}.C$ and Q nearly 1000 (fc = 1GHz / BW = 1MHz) can be realized. The linearity of the N-path filter is also good. Since the switches do not provide any gain and the OOB signals are also attenuated.

The major disadvantages are the harmonic responses and NF. The N-path structure bandpasses all the integer multiples of the clock frequency as well. Thus, creating bandpass responses at harmonics of the fundamental frequency. One solution is to make a differential structure, which rejects the even harmonics (explained in section.4.3). The passive mixer lacks the gain parameter, so the effects of BB noise can be seen directly at RF. Proper design strategies are to be used to reduce the NF within the specifications.

3.2. Mixer First Architecture

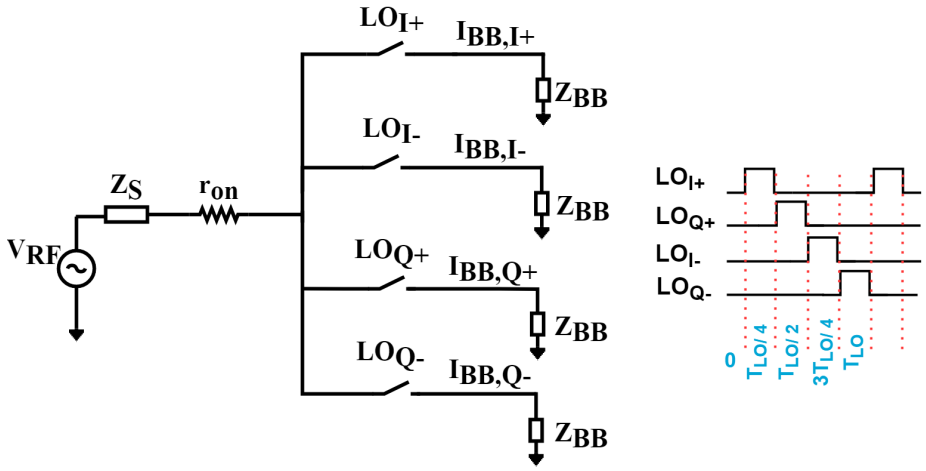


Figure 3.3: RX with 4-phase LO passive-mixer first design with LO waveform.

In the proposed design, the input RF signal is directly downconverted by mixing operation to BB frequencies by passive mixers (Fig.3.3). The mixers are used to select the desired frequency band and to transform the high-frequency input RF signal (≈1 GHz) to low frequency BB signals (≈1 MHz). The current mode passive mixer consists of switches driven by quadrature LO signals followed by BB stages. With current mode operation, the voltage swing is small at the input and output of the mixer, thus maintaining good linearity. The output from the LO block is a periodic signal turning the switches ON and OFF. Using the LO frequency for downconversion, wideband tuning can be easily achieved by changing the time period of the local oscillator (T_{LO}). The passive mixers provide good linearity, low flicker noise and are used in current mode with low load resistance resulting in lower swing at input and output. Since the structure does not provide any isolation between RF and BB stages, there exists a transparent path across them. The passive mixer used, provides a bidirectional path between RF and BB, thus the impedance is transparent along the receiver chain. This transparent property can be used as an advantage for providing input matching with only BB components.

3.2.1. Impedance Transparency

Consider a passive mixer as shown in Fig.3.3, for analyzing the impedance equations. The four-phase LO produces differential quadrature BB signals ($I_{BB,I+}$ from 0°, $I_{BB,I-}$ from 180°, $I_{BB,Q+}$ from 90°, and $I_{BB,Q-}$ from 270°). The non-overlapping 25% dutcy-cyle LO prevents the I-Q crosstalk [2]. Consider an ideal M phase LO clock system, with only resistive components for source impedance, as shown in Fig.3.4. The input impedance (Z_{in}) for the M-phase system is derived as (Appendix B)

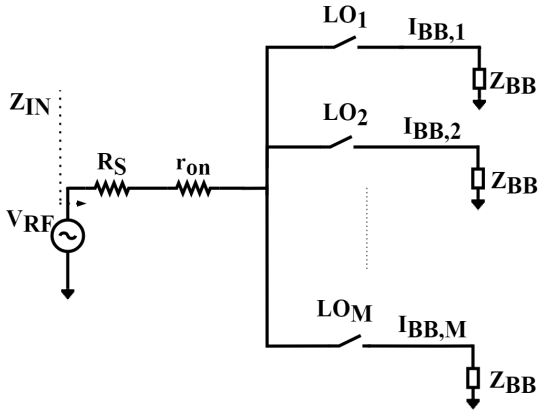


Figure 3.4: RX with M-phase LO passive-mixer first design.

$$Z_{in} = \frac{R_s}{r_{on} + R_s}\left[r_{on} + \frac{R_s \frac{M^2}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) Z_{BB}\,(\omega - \omega_{LO})}{M\,(r_{on} + R_s) + Z_{BB}\,(\omega - \omega_{LO})}\right] \tag{3.1}$$

From the equation.3.1, the input impedance (Z_{in}) after mixing, equals to the frequency-shifted baseband impedance $Z_{BB}(\omega - n\omega_{LO})$. Thus a low-Q BB impedance can be transferred to a high-Q RF impedance. A non-overlapped four-phase 25% duty-cycle LO driving four switches, along with their BB load impedance (Z_{BB}), holds a property named as, *impedance transformation*. This proves the transparent/bidirectional path between the RF and BB.

The Input impedance Z_{in} can be tuned directly using Z_{BB} giving a transparent path and a bidirectional conversion, because of lack of isolation. The Z_{in} at BB is a LPF, but it is frequency shifted to a high-Q BPF filter, at every integer multiple of LO. Thus, allowing to implement an on-chip high-Q BPF filtering at RF.

From the linear model depicted in Fig.3.5(b), the Z_{in} is directly proportional to Z_{BB}. Considering the BB impedance, as a parallel circuit consisting of resistance (R_{BB}) and capacitance (C_{BB}), the values of passive components can be determined from the input impedance matching equation. Rewriting the impedance equation for M phase passive mixer structure with assumption $\frac{M^2}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) = \gamma$

$$Z_{RF} = (r_{on} + R_s)\left[\frac{\gamma Z_{BB}\,(\omega - \omega_{LO})}{M\,(r_{on} + R_s) + [1 - \gamma] Z_{BB}\,(\omega - \omega_{LO})}\right] \tag{3.2}$$

The Impedance Z_{BB} consisting of both capacitive and resistive components and can be represented as,

$$Z_{BB}\,(\omega - \omega_{LO}) = \frac{R_{BB}}{1 + j\omega R_{BB} C_{BB}\,(\omega - \omega_{LO})} \tag{3.3}$$

$$Z_{RF} = \frac{\gamma}{\frac{M}{R_{BB}} + j\omega C_{BB}(\omega - \omega_{LO})M + [1-\gamma]\frac{1}{(r_{on}+R_S)}} \tag{3.4}$$

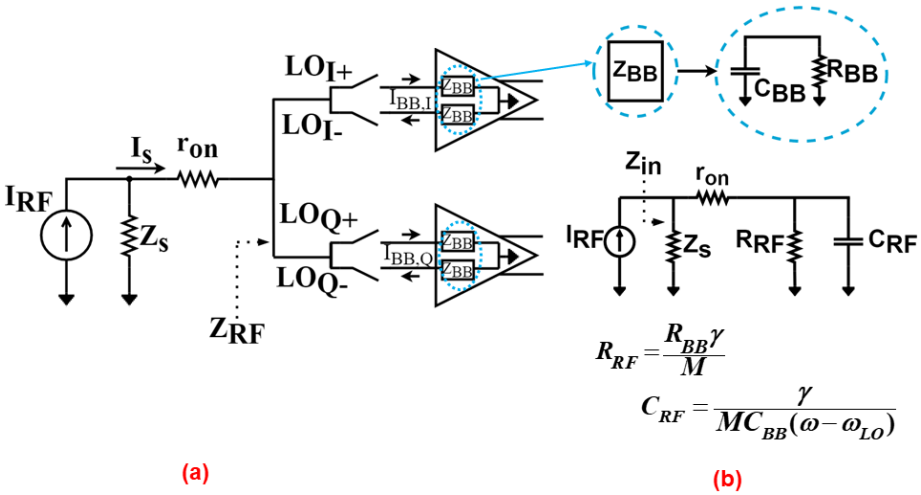


Figure 3.5: (a) Passive mixer schematics. (b) Equivalent LTI model of the design in (a).

The equation $Z_{\text{in}} = Z_s \| (r_{on} + Z_{RF})$ is considered for the input matching condition. Substituting back the equations, the passive components - resistance and capacitance values can be derived as,

$$R_{RF} = R_{BB}\frac{\gamma}{M+[1-\gamma]\frac{R_{BB}}{(r_{on}+R_S)}} \simeq \frac{R_{BB}\gamma}{M} \tag{3.5}$$

$$X_{RF} = \frac{C_{BB}(\omega-\omega_{LO})M}{\gamma} \simeq \frac{C_{BB}(\omega-\omega_{LO})M}{\gamma} \tag{3.6}$$

Thus for input impedance matching, a simple transparent equation $Z_S = r_{on} + \frac{R_{BB}\gamma}{M}$ is used. Thus, the passive mixer structure provides methods to have an input impedance matching through BB components, on-chip high-Q RF filtering and wide tunable frequency band, based on LO.

3.3. Zero IF Design

The ZIF architecture is used for higher bandwidth operation i.e. 4 MHz. The first stage in BB is crucial for the input impedance matching and NF, due to the transparent property of passive mixers. Since the input RF signal is downconverted directly to zero frequency, the flicker noise of the TIA is also critical. The 3rd-order filter requirement is difficult to achieve with a single stage. Thus, a two-stage design with a second-order complex conjugate poles as the first stage, followed by a single-pole

active filter is proposed (Figure.3.6). A higher order filter as, the first stage rejects the blockers with a higher slope, improving the linearity.

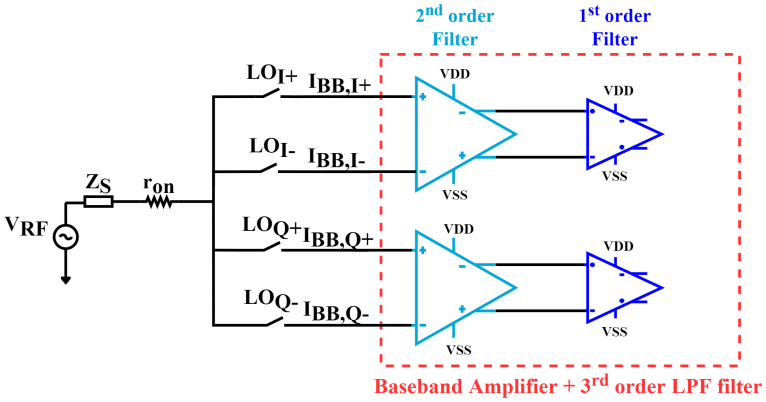


Figure 3.6: Basic structure of a ZIF receiver architecture.

3.3.1. TIA structure

The filtering is to reject the interference and to satisfy the ACR/ NACR requirements. The variable gain of the BB stage is to reduce the input variation at ADC input. A current-mode operation is carried out in the mixer stage. Thus, reducing the voltage swing, and improving the linearity of RX chain. The BB design should provide a low input impedance to support current mode operation at its input. After filtering, most of the operation occurs in the voltage domain, so a current (I) to voltage (V) conversion is also an important criterion for BB design.

A passive network can also be used for this purpose. However, the low input impedance and gain requirements are difficult to achieve. Thus, an active amplifier is required to provide an I-V conversion and a programmable gain. The amplifier is termed as transimpedance amplifier (TIA) (Fig.3.7). The $R_F \| C_F$ feedback path, provides a low-input impedance and also filters out interferences. The C_{IN} at the input of TIA to ground, filters the blocker current, when the the TIA's loop gain decreases [3]. If the open-loop gain of the amplifier is $-A_v$, the input impedance seen from the BB is $R_F/1+A_v \| C_F(1+A_v)$. Increasing the gain of the amplifier reduces the input impedance, and size of passive components required for a specific gain and bandwidth. The C_{IN} value required for large blocker signal is very high. Also, for narrow bandwidth operations, similar to 802.11ah standard's 1/2 MHz operation, the required sizes of R_F and C_F is also high. Limited by the input impedance, gain and noise, the R_F is fixed. Thus, for bandwidth the only tunable parameter is C_F. Thus, C_F requires a very large value for 1,2 MHz operation. Also, the basic structure provides only a 1^{st} order filter, thus motivating for more complex design structure.

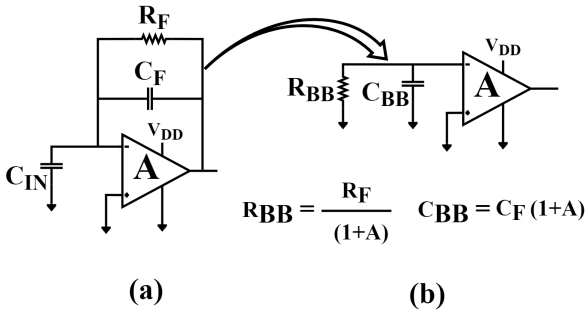


Figure 3.7: (a) Basic structure of a TIA (b) BB impedance in terms of feedback components.

With 2^{nd} order design and separate positive feedback capacitance, the TIA in [4] offers more blocker rejection. The complex poles provide a flat gain curve. However, the TIA burns very high power (50 mW). The baseband TIA requires a very high gm of 0.36 S, to move the unwanted zero created from the positive feedback and to make the system stable. A current-mode filter with complex conjugate poles, is given by [5]. This filter, can also be used for RX design [6]. It reduces the in-band noise by producing a high-pass noise shape. However, the noise shaping for 802.11ah standard around 1/2 MHz at BB requires high power consumption and larger area. The highpass shaping of noise depends on the active inductance value (proportional to $1/gm^2$), which affects the pole location. For a narrow channel, either the inductor value needs to be high, sacrificing the power or requires very high capacitance area. Other single-opamp filter structures, such as multiple feedback design or sallen-key, also suffer from a heavy tradeoff between NF and filter roll-off ([7]). The single-opamp 3^{rd} order design requires large passive elements at its input, increasing the NF directly. Also, very high gm is required to keep such system stable [8]. Also, all the above mentioned design, requires a big C_{IN}. Thus, the challenge is to, reduce the required BB capacitance C_{IN}, and to maintain a low power operation over a NF <7.46 dB (802.11ah standard). The filter should also provide the necessary 3^{rd} order slope. Also for a flat response, a complex conjugate pole pair is required from the design.

Adding an active feedback to the basic TIA structure improves the linearity and balances the trade-off between NF and power [9],[8] (Fig.3.8).

3.3.2. 2^{nd} Order Complex filtering with feedback network

The design of the first stage, 2^{nd} order low pass filter is given in Fig.3.8.

Filtering :

The feedforward path consists of the TIA along with the feedback resistance, R_F. Thus, with low input impedance, the input current from BB, i_{BB} is converted to first stage output voltage, V_{out1}. The feedforward stage provides the input matching and gain. The entire filtering is done in the feedback network. It consists of

RC circuitry and an operational transconductance stage (OTA) stage. It is designed to provide two real zeros, which are converted as complex conjugate poles in the closed-loop transfer function. The capacitors C_1 and C_3 behave as an open circuit for the signal passband and the feedforward path amplifies the signal. During the stop band, the feedback network provides the required filtering.

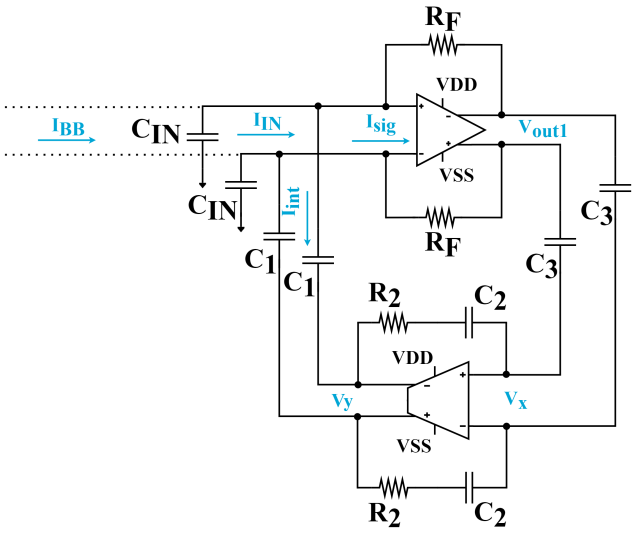


Figure 3.8: Filtering TIA with active feedback network.

Noise Shaping - gm :

The NF of the first stage is minimised because of the in-band noise shaping of the feedback path. Since the feedback network works as a 2^{nd} order highpass, the noise of gm stage is injected only in the stopband, with respect to the overall LPF.

Decrease in Capacitance value :

The large input capacitance, required for filtering the OOB and reducing the voltage swing at the TIA input, can be reduced by using the feedback structure. The feedback capacitance C_1 is boosted by the feedback network during the stop-band, thereby increasing its swing, to absorb OOB blockers. However, a grounded capacitance C_{IN} is still required to absorb most of the blocker. As, the feedback network requires large power consumption to completely absorb the blocker current by themselves. There exists a trade-off between area and power, however the capacitance required is lesser than the capacitance required for other designs discussed in the introduction.

The gain and impedance equations governing the first stage with ideal TIA and OTA are derived. The input current I_{IN}, gets divided as signal current (I_{sig}) to the TIA and as interference current (I_{int}) to the OTA.

$$I_{IN} = I_{sig} + I_{int} \tag{3.7}$$

The current through the TIA flows directly through the feedback resistance, and can be given by Equation.3.8.

$$I_{sig} = -\frac{V_{out,1}}{R_F} \tag{3.8}$$

The current equation of OTA can be calculated by using KCL equations at the node V_y.

$$I_{int} = -V_{out,1}\frac{C_2}{C_3}(R_2SC_2 + 1)SC_1 \tag{3.9}$$

The zeros formed in the feedback network are, one at DC due to C_1 and the other at $1/R_2C_2$ (Equation.3.9). Substituting the Equations.3.8 and 3.9 in Equation.3.7, the transimpedance gain of the first-stage is derived as,

$$G_{FS} = \frac{V_{out,1}}{i_{BB}} = \frac{-R_F}{S^2C_2^2\frac{C_1}{C_3}R_2R_F + SC_1\frac{C_2}{C_3}R_F + 1} \tag{3.10}$$

Equating this to a standard 2^{nd} order low pass filter equation, the cut-off frequency and Q, can be calculated as,

$$\omega = \sqrt{\frac{C_3}{R_1R_FC_1C_2^2}} \tag{3.11}$$

$$Q = \sqrt{\frac{R_2C_3}{R_FC_1}} \tag{3.12}$$

The input impedance equation for matching is directly equal to R_F, since the feedback network is open circuited for DC at BB. From the calculations, it is clear that both gain and $S11$ depends heavily on R_F, creating a bottleneck for the tunability. Thus, with a two-stage design, the tunability for R_F can also be relaxed. The gain of the first-stage, however has to be high enough to suppress the subsequent stage noise.

3.3.3. 2^{nd} BB stage: Active Single pole filter

The second stage is cascaded to the input stage. An only-passive second stage can also provide the required 3^{rd} order filtering. However, the gain programmability would be very difficult. Thus, an active single-pole basic structure shown in Fig.3.9 is considered. It is a voltage gain amplifier, providing real pole, from the feedback components, $R_{F,SP}$ and $C_{F,sp}$. The other advantage of implementing active second stage is explained while designing the LIF stage. The NF of the second stage is suppressed by the gain of first chain, thus allowing room for decreasing power consumption. Also, since the first stage R_F value is mostly limited by the input

impedance matching, the second stage feedback resistor $R_{F,SF}$ can also be used for tuning the gain. The input impedance for this stage, ideally is R_1, since the opamp provides a virtual ground at its input.

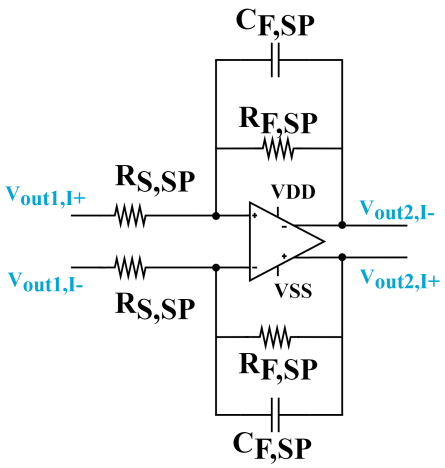


Figure 3.9: Second stage LPF structure.

The voltage gain of the inverting active LPF is,

$$\frac{V_{out,2}}{V_{out,1}} = \frac{\frac{-R_{F,SP}}{R_{S,SP}}}{1 + SC_{F,SP}R_{F,SP}} \tag{3.13}$$

The cut-off frequency is given as,

$$f_{SP} = \frac{1}{2\pi R_{F,SP}C_{F,SP}} \tag{3.14}$$

3.3.4. Gain and Bandwidth of cascaded stages

The cascaded design of the first stage (TIA with active feedback network) and the second stage (single-pole filter), provides the total gain of the BB. Considering both the equations.4.56 & 3.13, the overall gain with ideal components is,

$$\frac{V_{out,2}}{I_{IN}} = \frac{-R_F}{S^2C_2^2\frac{C_1}{C_3}R_2R_F + SC_1\frac{C_2}{C_3}R_F + 1} \times \frac{\frac{-R_{F,SP}}{R_{S,SP}}}{1 + SC_{F,SP}R_{F,SP}} \tag{3.15}$$

From the equation, it can be seen that, the gain of the receiver can be increased or decreased by using the resistors. Similarly, the bandwidth of the receiver can also be modified by using the passive components, easily. The cascaded design provides a 3^{rd} order LPF. The input impedance of the single-pole stage, R_1 acts as

a load for the first stage. Thus, the total input impedance equation for the 3^{rd} order design is, $R_F \| R_1$. Thus, to decrease the load of the first stage TIA, the R_1 value should be very high. However, the value of R_1 directly affects the NF, resulting in a trade-off.

3.4. Low IF Design

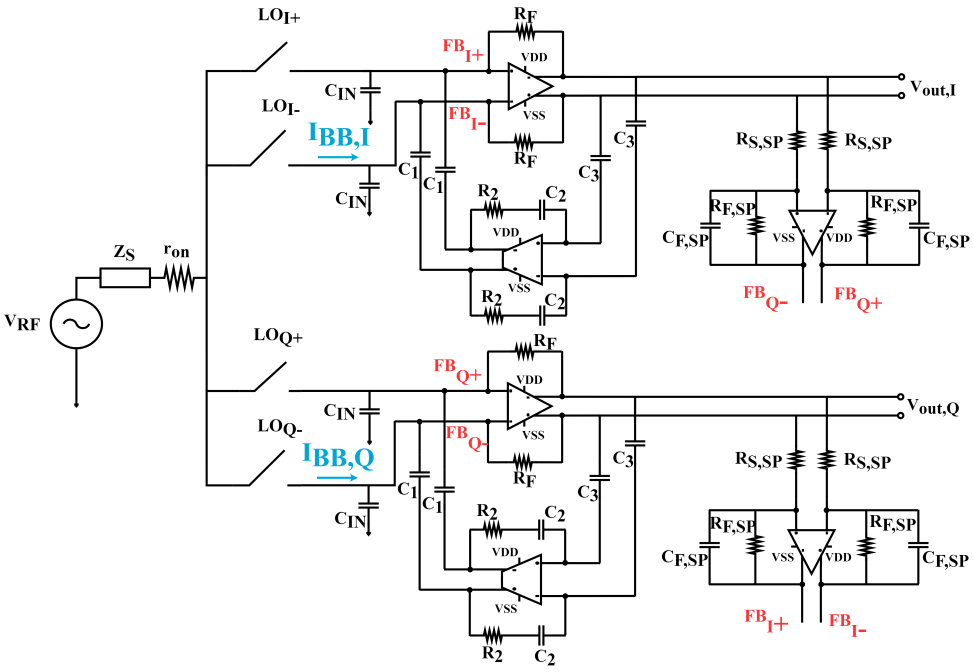


Figure 3.10: LIF architecture with 2^{nd} order LPF filter and 1^{st} order filter as complex feedback filter.

The LIF architecture, needs to implement a BPF shape in BB (Fig.**??**). Implementing a 3^{rd} order BPF with low power consumption for a narrow-bandwidth (1/2 MHz) is very challenging. Thus, an LPF-to-BPF transformation technique is used to achieve the required filtering. A method to modify the center frequency through an additional feedback structure without affecting the bandwidth is suggested in [10],[11]. The center frequency of the LPF is shifted to get a BPF response. The design idea is to apply additional feedback between the I and Q path. The 2^{nd} order LPF used for LIF design can still be used as the first stage for LIF architecture. The I and Q channel feedback through resistors are used in the design [10] (Figure.3.11). The complex BB input impedance value for the feedback structure is given in Equation.3.16 [10]

$$Z_{BB} = \left[\left(\frac{1+A}{R_F} + \frac{1}{R_{FC}}\right) \pm j\frac{A}{R_{FC}}\right]^{-1} \tag{3.16}$$

The feedback from I to Q (and vice-versa) results in the imaginary term in the above equation. Thus, varying the resistor value, the input matching frequency is shifted (shift in center frequency), resulting in a BPF.

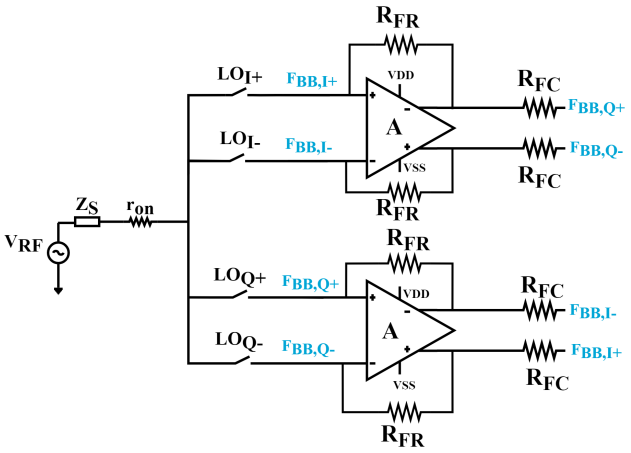


Figure 3.11: Receiver schematic with complex feedback.[10]

3.4.1. Complex Feedback: IQ channel

The resistor added in feedback, directly contributes to the noise of the system. Also, adapting the feedback structure for a second-order system requires more complex equations. The resistor also affects the symmetricity of the transfer function. Thus, an active stage is used instead of the resistor to create a balanced cross-connection. To achieve a BPF structure, the already existing ZIF design is modified and IQ feedback is applied (Fig.3.12). The gm denotes the transconductance of the feedback amplifier. The equations governing the feedback architecture are discussed below,

Impedance Analysis :

The idea proposed in [10], is for providing a complex wide matching, to account for antenna variations. Thus, the input impedance equations are analysed to provide a complex impedance matching, and shift the center frequency of operation. Analysing the input impedance equation for the active feedback design (Figure.3.12)

$$I_+ = V_{I+}\frac{1+Z_{21}}{R_F} + gmV_{Q+} \tag{3.17}$$

where, the Z_{21} of the first stage can be assumed to be A. The R_F denote the feedback resistor of the first stage (Section.3.3). Considering, $V_{Q+} = -jV_{I+}$

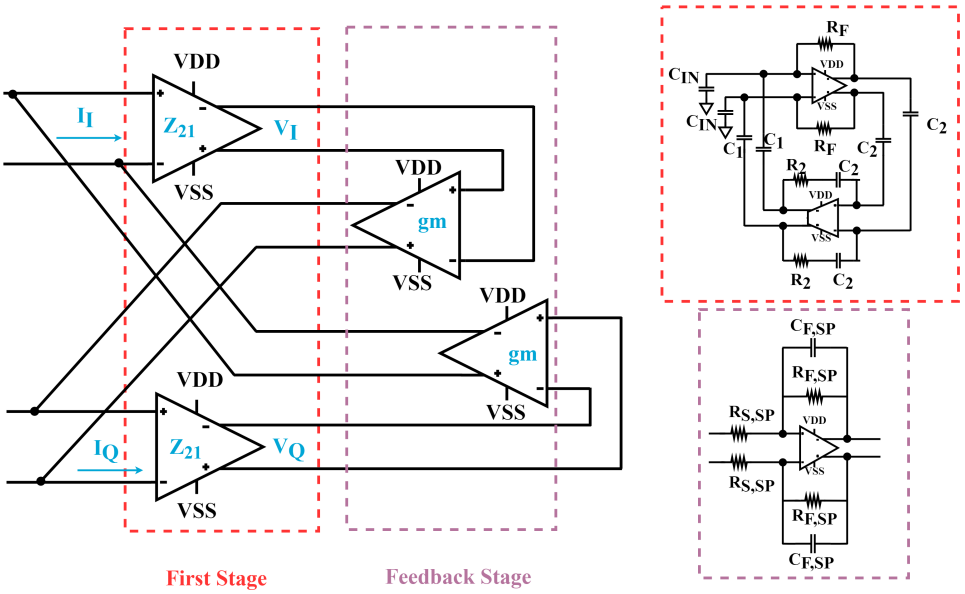


Figure 3.12: IQ feedback structure for LPF to BPF transformation.

$$I_+ = V_{I+}\left(\frac{1+A}{R_F} - jgm\right) \tag{3.18}$$

$$Z_{BB} = \left(\frac{R_F}{1+A} - jgm\right) \tag{3.19}$$

Thus, from the Z_{BB} impedance equation, the gm value can be varied to get a shift in center frequency. However, from MATLAB simulation, the bandpass transformed filter was unstable ((Fig.3.13(b)). So the analysis was carried out with gain equations to understand the stability issue and possibly achieve the BPF. The gain equation for a 1^{st} order system is derived to verify the idea.

Gain Analysis :

$$I_Q = jI_I \tag{3.20}$$

$$V_I = \left(I_I + gmV_Q\right)Z_{21} \tag{3.21}$$

$$V_Q = \left(jI_I - gmV_I\right)Z_{21} \tag{3.22}$$

Using cramer's rule,

$$V_I = I_I Z_{21} \frac{1 + jgmZ_{21}}{1 + gm^2 Z_{21}^2} \tag{3.23}$$

$$V_Q = jI_I Z_{21} \frac{1 + jgmZ_{21}}{1 + gm^2 Z_{21}^2} \tag{3.24}$$

From the above equations, the modified transimpedance gain is given as, $Z_{21,new} = Z_{21} \frac{1+jgmZ_{21}}{1+gm^2 Z_{21}^2}$.

For a simple 1st-order LPF filter, as shown in Fig.3.7, the R || C is applied as feedback to the opamp. The new transformed equation for the feedback structure is calculated as

$$Z_{21,new} = \left(\frac{R}{1 + j\omega RC}\right) \frac{1 + jgm\left(\frac{R}{1+j\omega RC}\right)}{1 + gm^2 \left(\frac{R}{1+j\omega RC}\right)^2} \tag{3.25}$$

$$Z_{21,new} = \left(\frac{R}{1 + jRC(\omega - \omega_o)}\right) \tag{3.26}$$

Where $\omega_o = gm/C$ is the resonant frequency. The transformed $Z_{21,new}$ consists of frequency-shifted impedance, which helps to change the center frequency to achieve the BPF directly (Fig.3.13(a)).

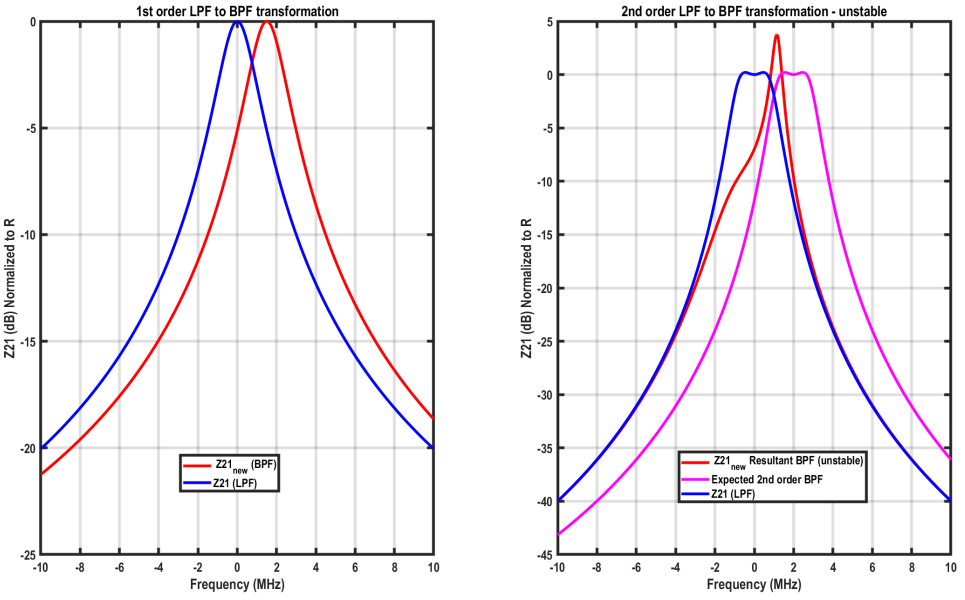


Figure 3.13: (a) 1^{st} order LPF to BPF transformation plot. (b) 2^{nd} order LPF to BPF transformation without any design modification.

Now considering the 2^{nd} LPF, as shown in Fig.3.8, the new gain equation at ω is calculated as

$$Z_{21} = \frac{R_F}{1 - \frac{\omega^2}{\omega_n^2} + j\frac{\omega}{\omega_n Q}} \tag{3.27}$$

$$Z_{21,new} = \frac{R_F}{1 - \frac{\omega^2}{\omega_n^2} + j\left(\frac{\omega}{\omega_n Q} - gmR_F\right)} \tag{3.28}$$

Without any design conditions, the output equation of the transformed structure results in peaking and is unstable (Fig.3.13(b)).

The Equation.3.28 should not have any imaginary part at the resonance. Hence

$$\left(\frac{\omega}{\omega_n Q} - gmR_F\right) = 0 \iff \omega = \omega_n Q gmR_F \tag{3.29}$$

Substituting back ω value, to get the $Z_{21,max}$ equation as

$$Z_{21,new} = \frac{R_F}{1 - gm^2 R_F^2 Q^2} \tag{3.30}$$

To guarantee the stability, the denominator must be positive,

$$gmR_F Q << 1 \tag{3.31}$$

The Q value has to be decreased, to maintain the gain equation positive at resonance. Also, the second term of the denominator (equation.3.28) should be positive, $\omega_n > \omega$. Thus, the cut-off frequency of the BB (ω_n) should be greater than the center frequency of the filter (ω) (Fig.3.14). From the MATLAB simulations, for ω_n = 4 × ω, stable output is obtained. The Q value for the filter is calculated as, 0.25 (ω/ω_n). Considering R_F value as 1 $K\Omega$, gm has to be less than 4 mS (from equations.3.31). With these design modifications, the required center frequency shift is observed for $gm = 1.75mS$, however with a reduced filter order (Fig.3.14). Thus a reconfigurable architecture using the same stages for LIF and ZIF is proposed. The structure requires a few more switches to alter the paths for the output ports. The output of the second stage (single pole) is fed to the input of the first stage (TIA with active feedback) to realize the complex IQ sharing structure to transform the LPF to BPF for LIF architecture (Figure.3.10).

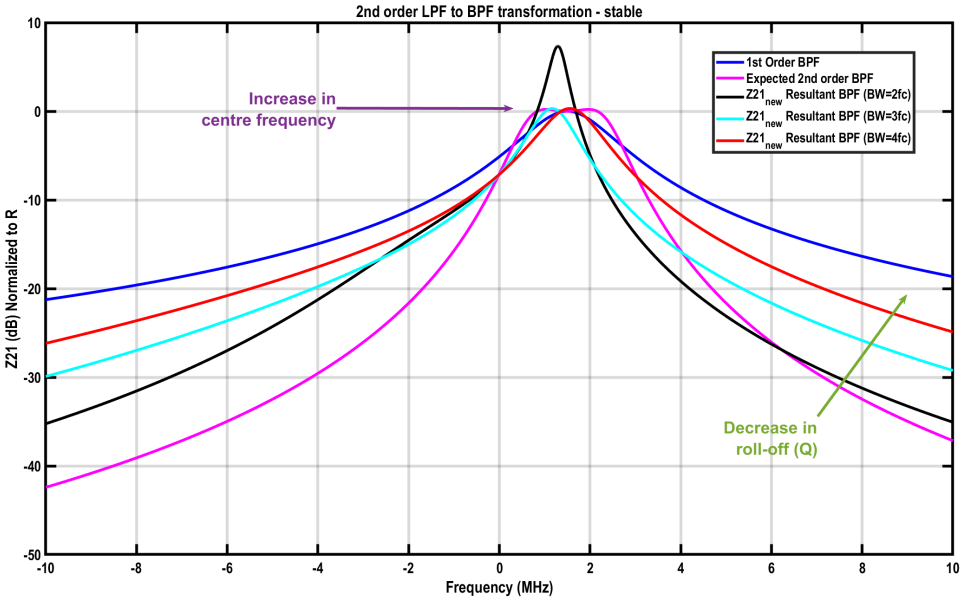


Figure 3.14: Stable 2^{nd} order LPF to BPF transformation.

3.4.2. Polyphase Image rejection filter

The next important block in a LIF architecture is the image rejection filter. In general, an image rejection filter can also be placed at RF, prior to downconversion. However, a filter with sufficient selectivity (requires very high-Q) at high frequency is very difficult to implement. Therefore, the image rejection filter is placed in BB after the filter block. The cascaded PPF, based on Hilbert transformation, is used for the image rejection [12]. After downconversion, both the signal and the image lie at the same frequency, but with conjugate complex representations [13]. Thus, if the quadrature signals (I and Q path) are summed together, it is possible to reject the image in BB. In Hilbert transformation, the positive and negative frequency signals are filtered differently (shift-by-90°). Consider an RC circuit branch, as shown in Fig.3.15(a). The input to the RC circuit are considered, $V_{in} + V_{im}, -V_{in} - V_{im}, jV_{in} - jV_{im}$, and $-jV_{in} + jV_{im}$. These inputs are resultant of downconversion process, with V_{in} denoting the signal and V_{im}, the image.

Consider the signal at a single branch (top), with V_{in}, as the input fed to an RC circuit at one side, and $-jV_{in}$ at the other side. The V_{out1} is taken at the RC node. Solving KCL at that node, the output equation is calculated as,

$$V_{out1} = V_{in}\frac{R_{PPF}C_{PPF}\omega + 1}{jR_{PPF}C_{PPF}\omega + 1} \tag{3.32}$$

For $\omega = 1/R_{PPF}C_{PPF}$, the $V_{out1} = V_{in} \pm jV_{in}$. Thus, circuit performs a simple vector summation for the provided signal inputs. Similarly, for the image V_{im}, the output can be denoted as,

$$V_{out1} = V_{in} \frac{-R_{PPF}C_{PPF}\omega + 1}{jR_{PPF}C_{PPF}\omega + 1} \tag{3.33}$$

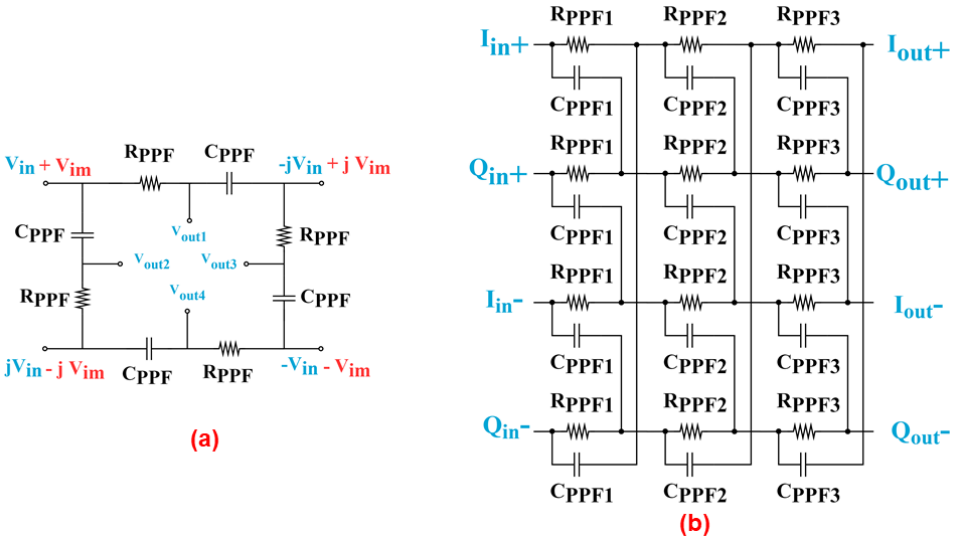


Figure 3.15: (a) A RC network working as PPF (b) The cascaded PPF structure.

At resonance $\omega = 1/R_{PPF}C_{PPF}$, the output voltage is zero. In this way the image can be rejected from the signal, using quadrature paths. Extending the theory, the inputs can be mapped to $V_{out,I+}$, $V_{out,Q-}(-jV_{out,I+})$, $V_{out,I-}$, and $V_{out,Q+}(jV_{out,I+})$. For a single stage PPF, the rejection is only at $R_{PPF}C_{PPF}$. To provide rejection across a bandwidth, a cascaded structure can be used. From simulation results of [12], it can be calculated that, for a 43 dB image rejection. it requires three-cascaded structures (Fig.3.15(b)). The load of each stage affects the gain of the signal. However, the image rejection value is unaltered, since the zero from the numerator does not change because of load. Consider a load Z_{L1} at the output of the first stage. For multi stage PPF, the load impedance can be calculated from [14] as

$$Z_{L1} = \frac{R_{PPF2} + Z_{L2} + sC_{PPF2}R_{PPF2}Z_{L2}}{1 + sC_{PPF2}\left(R_{PPF2} + 2Z_{L2}\right)} \tag{3.34}$$

Thus, the frequency dependent input impedance of the PPF is $R_{PPF1}\|C_{PPF1}$ in series with Z_{L1}. The input impedance is very high at DC, and falls to $R_{PPF1}\|C_{PPF1}$ at resonant frequency. The low input resistance of the first stage of the PPF can heavily load the circuit that drives it. Thus, a low output impedance stage, such as a buffer is required. The output stage of the PPF should also be a balanced termination. Any mismatches at the load can directly, degrade the image rejection [12].

3.4.3. Buffer stages

A gm stage is used as a buffer for isolating the PPF and the input stages (Fig.3.16). The buffers placed in front of both the PPF are used for impedance isolation. The resistor added in feedback provides a current path reducing the voltage swing and improving the linearity. The resistors can also be used for gain programmability, since the first stage passive components are limited by the input impedance matching and center frequency tuning for LIF design.

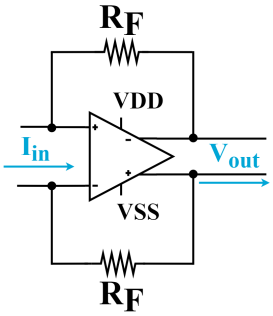


Figure 3.16: Buffer stage design with feedback resistance.

3.4.4. Polyphase Notch Filter

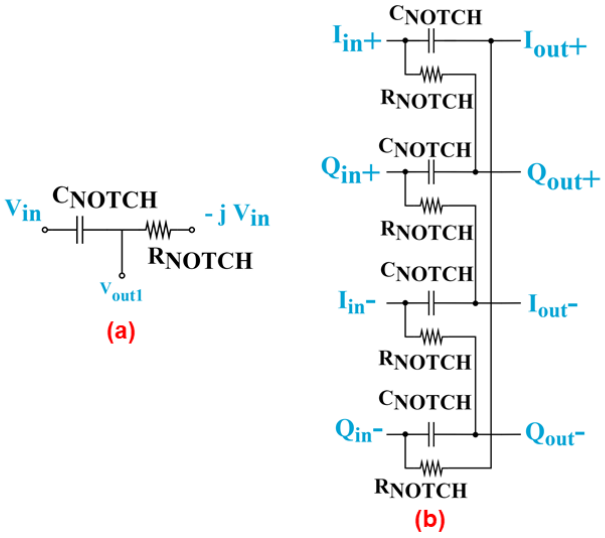
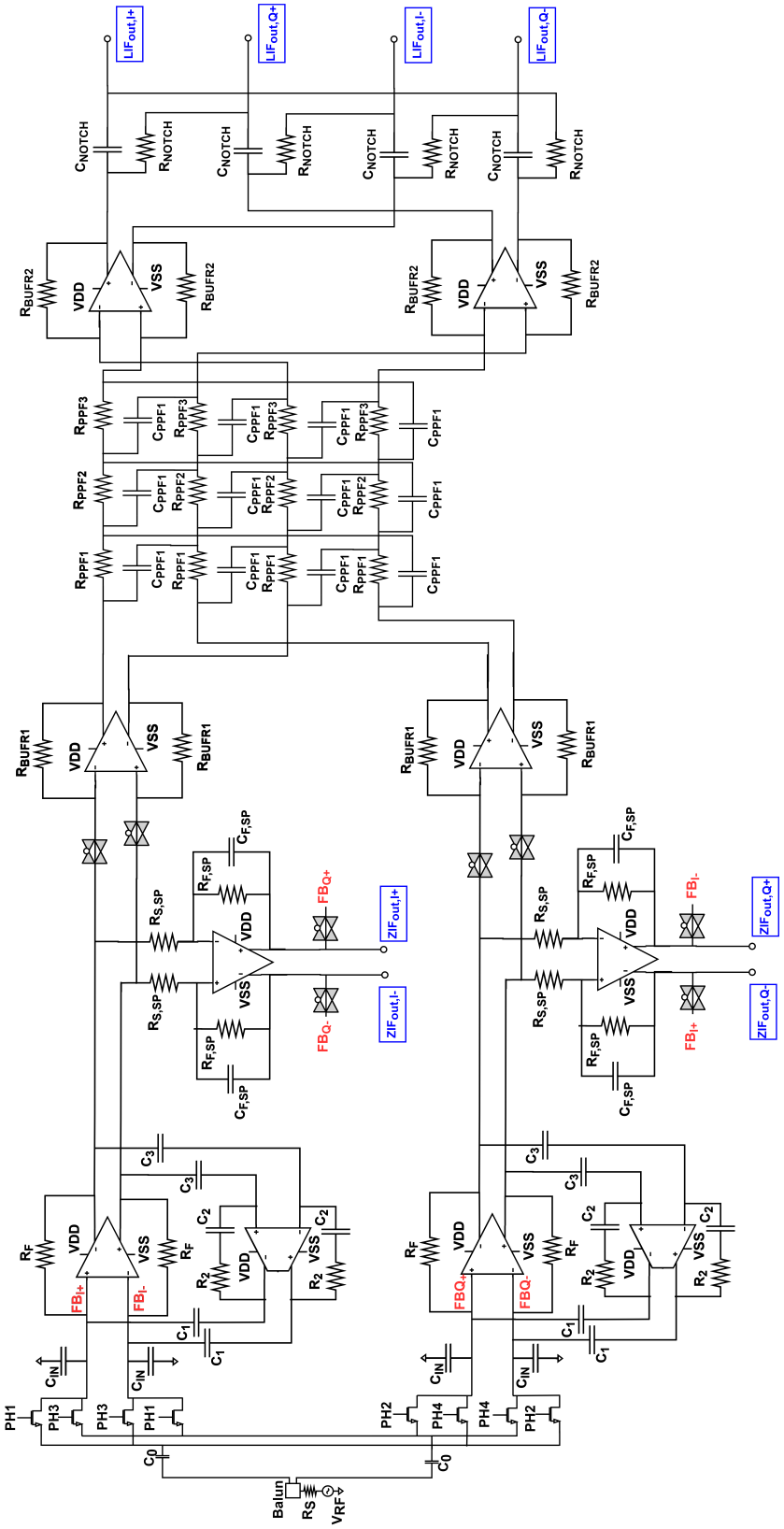


Figure 3.17: (a) A CR network working as notch filter (b) The notch filter structure.

The LIF design should also provide a 3^{rd} filtering to satisfy the ACR and NACR requirements. Ideally, the first stage provides ACR of only 8 dB. Thus, it requires another 2^{nd} order filter to achieve the standard specification. In order to decrease the power consumption, a notch filter, based on PPF is designed. The losses and NF degradation caused by the passive components are maintained low by properly optimizing its values. A notch filter is designed, by simply inverting the image rejection filter characteristics. The LPF and HPF structure in PPF is reversed providing a narrow band-stop filter. Consider a single branch with CR components, as shown in Fig.3.17(a). The output voltage $V_{out} = \frac{j(\omega R_{NOTCH} C_{NOTCH} - 1)}{1 + j\omega R_{NOTCH} C_{NOTCH}}$.

For pole frequency, $\omega = 1/R_{NOTCH} C_{NOTCH}$, the output is zero. Thus, creating a perfect notch at the required frequency. The notch is placed in the first non-adjacent channel, to satisfy both the ACR and NACR values. A single stage notch filter designed, for quadrature paths is given in Fig.3.17(b). The R_{NOTCH} and C_{NOTCH} values, are designed satisfying the trade-off between the NF and pole location. Increasing the R_{NOTCH} value and decreasing the C_{NOTCH} value both increase the NF of the RX chain.

The entire block level representation of the design is presented in Figure.3.18


LIFout,I+
LIFout,Q+
LIFout,I-
LIFout,Q-
CNOTCH
RNOTCH
RBUFR2
RBUFR1
VDD
VSS
RPPF3
RPPF2
RPPF1
CPPF1
ZIFout,I+
ZIFout,I-
ZIFout,Q+
ZIFout,Q-
RS,SP
RF,SP
CF,SP
FBQ+
FBQ-
FBI+
FBI-
RF
R2
C3
C2
C1
CIN
C0
PH1
PH2
PH3
PH4
Balun
RS
VRF

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4

Receiver schematics and Design parameters

The chapter presents a circuit-level view of all the blocks of the RX chain. A simple inverter design is used as an amplifier. The gain and noise equations are derived, for individual blocks by considering practical gm values. The design parameters of the receiver chain are calculated from the standard and the equations are derived. Finally, the full view of the entire RX chain, with circuit-level representation, is presented.

4.1. Inverter as an amplifier design

Moore's law dominance has pushed most of the research into scaling the CMOS technology. Thus analog devices have become more difficult to design and integrate. Thus, many analog circuits have been modified or replaced by digital implementations. Following the path, a simple CMOS inverter circuit can be implemented as an analog amplifier [1].

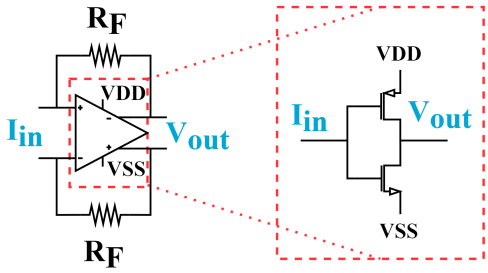

Figure 4.1: TIA design with inverter (as amplifier).

For CMOS inverter to act as an analog circuit, the operating point where both input and output have the same voltage level. This optimum bias point is achieved by using a feedback resistor, thus making it a self-biasing amplifier. The output node is settled to half of the supply voltage and the gm from PMOS and NMOS is summed up (high gm value).
A differential amplifier, based on the inverter is designed in this work. The PMOS P1 and P2 are operated in saturation to decrease the common mode gain. For common-mode input V_{CM}, the output node is diode connected to P1 & P2 gate. This provides a low common mode gain of gm_n/gm_{CM}, since the PMOS is also biased in saturation. However, to operate all the transistors in saturation with VDD (1.1 V) is difficult. Since it requires enough voltage headroom to satisfy two gate-source voltage for the inverter pair and the overdrive voltage of the PMOS (P1 & P2). So, a higher threshold device (hvt-PMOS) is used for P1 and P2. Also, designing a lower overdrive voltage for inverter's PMOS can ensure all the transistors to be biased in saturation, improving both the differential and common-mode gain.

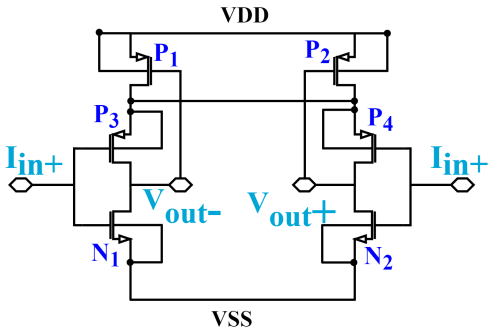

Figure 4.2: Differential TIA design in BB.

4.2. 2^{nd} order TIA with active feedback network design with finite gm

The first stage of the receiver is the 2^{nd} order LPF. It consists of two amplifier paths, one for feedforward and one in feedback. The differential inverter design is used for the TIA, and a simple inverter design is used for the feedback gm design (Fig.4.3(a),(b)). The block-level gain equations were presented in section.3.3.2, assuming ideal amplifiers. Now the inverter circuit is used as an amplifier, and the design equations are calculated. Consider the small signal model shown in Fig.4.3(c). In the small signal model, the output resistance r_o is considered parallel to the gm current. The impedance Z_2 in the feedback gm stage, denotes the series impedance between R_2 and C_2.

4.2.1. Gain and Bandwidth derivation

For the feedforward TIA stage, the input current in terms of output voltage is represented as

$$I_{sig} = \frac{V_{sig} - V_{out,1}}{R_F} \tag{4.1}$$

$$I_{sig} = gm_{TIA}(R_F I_{sig} + V_{out,1}) + \frac{V_{out,1}}{r_o} \tag{4.2}$$

Considering $gm_{TIA}ro >> 1$, and $gm_{TIA}R_F >> 1$, the current equation is simplified as

$$I_{sig} = \frac{gm_{TIA}}{1 - gm_{TIA}R_F} V_{out,1} \tag{4.3}$$

Considering $R_F >> 1/gm_{TIA}$, the DC gain of the filter is given from the feedforward path, since the feedback path is open circuited. Thus, $\frac{V_{out,1}}{I_{sig}} = -R_F$

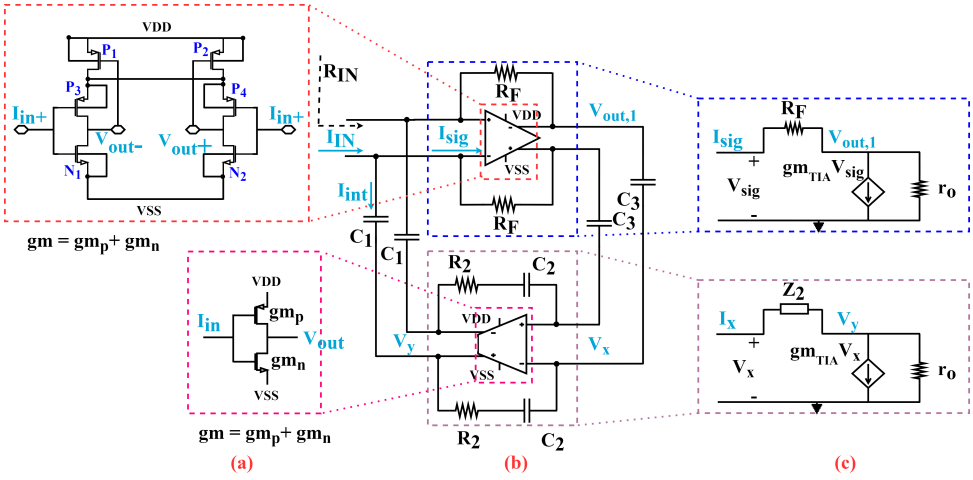

Figure 4.3: (a) Amplifier design (b) Placement of inverter on the filter block diagram (c) small signal models for the feedfoward and feedback paths.

To analyze the limitations of the finite-gm stage alone, an ideal opamp is considered in feedforward path. The nodal equations for V_x and V_y, are derived from the small signal model Fig.4.3(c).

$$(V_{out,1} - V_x)SC_3 = \frac{V_x - V_y}{Z} \tag{4.4}$$

$$\frac{V_x - V_y}{Z} = gm_{OTA}V_x + \frac{V_y}{r_o} \tag{4.5}$$

Thus, the new transformation equation for the gain of first stage is

$$\frac{V_{out,1}}{I_{sig}} = \frac{\left(s^2 \frac{C_1 C_2^2 R_2}{C_3 gm_{OTA}} + s\frac{\left(2C_1 + \frac{C_2}{C_3}\right)}{gm_{OTA}} + 1\right) R_F}{s^2\left(R_F R_2 C_1 \frac{C_2^2}{C_3} + \frac{C_1 \frac{C_2^2}{C_3}(R_2 - R_F)}{gm_{OTA}}\right) + s\frac{\left(2C_1 + \frac{C_2}{C_3} + C_1 R_F\right)}{gm_{OTA}} + 1} \tag{4.6}$$

The equation shows the existence of complex conjugate zero due to the limitation of the gm value in the feedback path. Proper design choices should be made to place the zeros away from the required band to avoid stability issues. The complex conjugate pole location (ω_n), Q factor, and zero location (ω_Z) equations are derived after comparing it against a standard LPF equation.

$$\omega_n = \sqrt{\frac{1}{R_F R_2 C_1 \frac{C_2}{C_3} + \frac{C_1 \frac{C_2^2}{C_3}(R_2 - R_F)}{gm_{OTA}}}} \tag{4.7}$$

$$Q = \sqrt{\frac{C_1 C_3 gm_{OTA}\left(R_2 + R_1\left(gm_{OTA} R_2 - 1\right)\right)}{C_2 + C_1 C_2\left(2 + gm_{OTA} R_1\right)}} \tag{4.8}$$

$$\omega_Z = \sqrt{\frac{C_3 gm_{OTA}}{R_2 C_1 C_2^2}} \tag{4.9}$$

The ω_Z location has to be one decade apart from the ω_n location, to have a flat band in the desired signal band and to attenuate the non-adjacent channels sufficiently.

$$\frac{\omega_Z}{\omega_n} \approx \sqrt{gm_{OTA} R_F} \tag{4.10}$$

4.2.2. Input impedance matching and Receiver gain equation

The other important specifications are the input impedance matching $S11$, and receiver gain. The input impedance can be derived, using the small-signal model for the receiver chain at DC. The first stage of the BB is connected to the mixers. Figure.4.4(a), depicts the receiver chain with the first stage block. The resistor seen from the BB is termed as $\frac{R_{BB}\gamma}{M}$, according to Equation.3.5. First, the input impedance of the first stage R_{BB} is derived, and then substituted in the receiver equation. Calculating the KCL equations from Figure.4.4)(b),

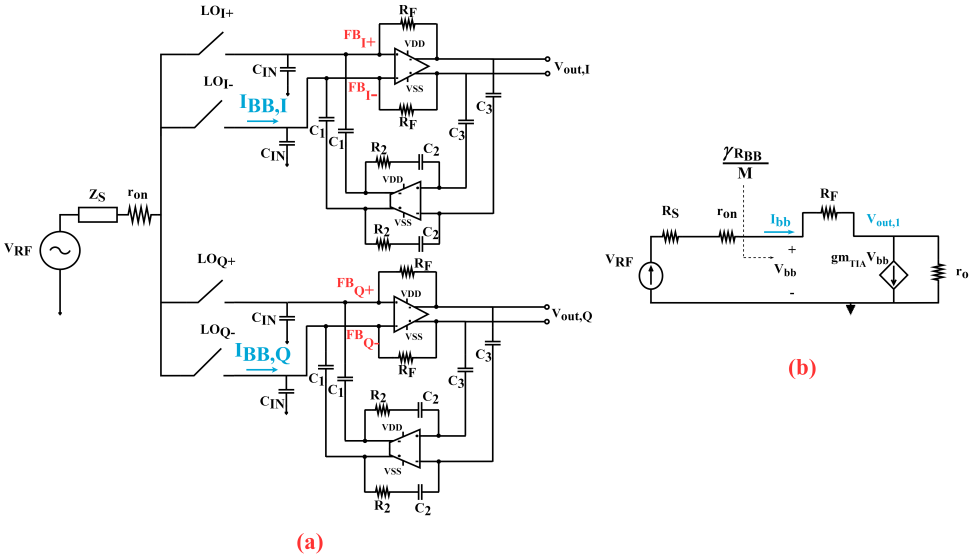

Figure 4.4: (a) Receiver chain with first stage design (b)Small signal model of receiver chain to calculate input impedance equation.

$$I_{BB} = \frac{V_{BB} - V_{out,1}}{R_F} \tag{4.11}$$

$$\frac{V_{out,1} - V_{BB}}{R_F} + gm_{TIA}V_{BB} + \frac{V_{out,1}}{r_o} = 0 \tag{4.12}$$

$$R_{BB} = \frac{R_F}{gm_{TIA}r_o} + \frac{1}{gm_{TIA}} \tag{4.13}$$

$$R_S = r_{on} + \frac{R_{BB}\gamma}{M} \tag{4.14}$$

$$R_S = r_{on} + \frac{R_F\gamma}{Mgm_{TIA}r_o} + \frac{\gamma}{Mgm_{TIA}} \tag{4.15}$$

The receiver DC gain equation can also be calculated with the same small signal model (Fig.4.4(b)),

$$I_{BB} = gm_{TIA}\left(R_F I_{BB} + V_{out,1}\right) + \frac{V_{out,1}}{r_o} \tag{4.16}$$

Considering, $gm_{TIA}r_o >> 1$ and $1/gm_{TIA} << R_F$

$$V_{out,1} = I_{BB}\left(-R_F\right) \tag{4.17}$$

The BB current in terms of input RF current for M-phase mixer is [2],

$$I_{BB} = -\frac{1}{M} sinc\left(\frac{\pi}{M}\right) I_{RF} \tag{4.18}$$

where the $\frac{1}{M} sinc\left(\frac{\pi}{M}\right)$ denotes the conversion loss. The RF input current can be written as, $V_S/(R_S + r_{on})$. Substituting the value of I_{RF} and Equation.4.18 in Equation.4.17,

$$V_{out,1} = \frac{1}{M} sinc\left(\frac{\pi}{M}\right) \frac{1}{R_S + r_{on}} R_F \tag{4.19}$$

The gain equation of a 4-phase Mixer with the designed first stage in BB is given as,

$$A_{V,RX} = \frac{\sqrt{2}}{\pi} \frac{1}{R_S + r_{on}} R_F \tag{4.20}$$

The input impedance matching equation (4.15) has heavy dependence on the intrinsic gain $gm_{TIA}.r_o$. Since, gm_{TIA} is a temperature variant parameter, the matching can vary with temperature differences.

4.2.3. Temperature effects on the receiver input matching and gain

The input impedance of the receiver chain shows direct dependency on the transconductance (gm_{TIA}). This motivates us to analyze the side effects of the temperature variations on the receiver. The parameters from the design equation subjected to dependencies are the gm_{TIA} and Intrinsic gain $(gm_{TIA}.r_o)$. The equations relating to the parameters to temperature and process corner variation are given below

$$\begin{aligned} gm &= u_n \cos x_n \frac{w}{l}(v_{gs} - v_{th}) \quad r_o = \left[\lambda \frac{u \cos x}{2} \frac{w}{L} (V_{gs} - V_{th})^2\right]^{-1} \\ V_{th} &= V_{to} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{2\phi_F}); \phi_F = \frac{KT}{q} \ln\left(\frac{N_A}{N_i}\right) \end{aligned} \tag{4.21}$$

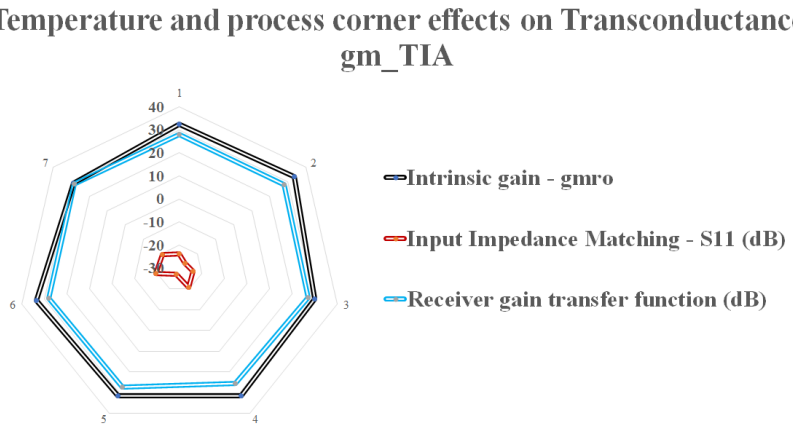

Figure 4.5: Simulation results for model and temperature variations.

Multiple simulations varying the temperature (-40°C to 80°C) and process corners (SS, TT, FF) were carried out (Appendix B). From the equations and simulation output (Fig.4.5), it is seen that intrinsic gain is fairly a constant value since gm_{TIA} and r_o have opposite dependency in-accordance to temperature variations, thus equalizing (cancelling) the variations. The input impedance equation (4.13) is also a constant because the first term (R_F and $gm_{TIA}r_o$) in the equation contributes around 70% of the value and the second term (gm_{TIA}) contributes the rest 30%. Thus a variation of gm_{TIA} for -20 to 15% within 30% contribution does not affect the net result. Thus, both the $S11$ equations are not heavily dependent on temperature and process variations.

4.2.4. Noise Analysis

The noise gain equations are derived for the first stage. Since the first stage of a system always need to be optimized for noise contribution. The subsequent stages noise will get suppressed by the first stage gain and hence its contribution is minimal. The major noise sources, the resistors ($V_{n,RF}^2$ and $V_{n,R2}^2$), feedforward TIA ($V_{n,tia}^2$), and feedback OTA ($V_{n,gm}^2$), are considered (Fig.4.6).

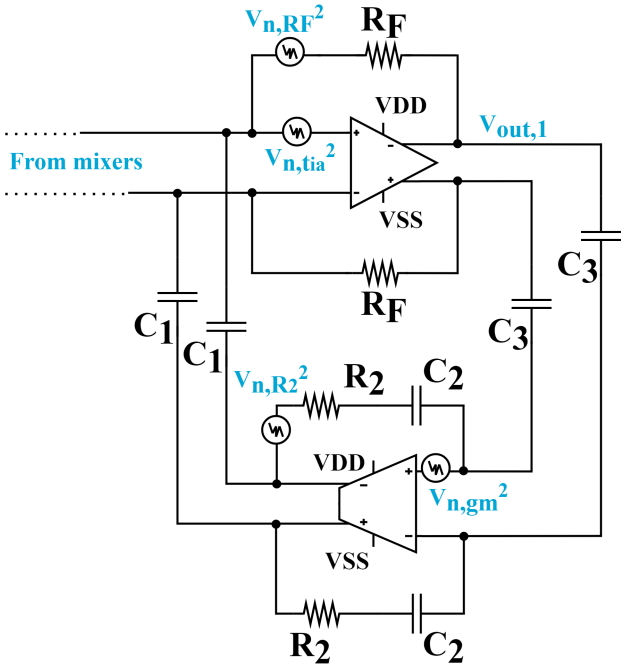

Figure 4.6: First filter stage with noise sources.

The noise gain equations for individual sources are given from [3].

$$\frac{V_{out,1}}{Vn_{R_F}} = \frac{1}{S^2\left(R_F R_2 C_1 \frac{C_2^2}{C_3} + R_F C_1\right) + SR_1 C_1 + 1} \tag{4.22}$$

$$\frac{V_{out,1}}{Vn_{tia}} = \frac{S^2 R_F R_2 C_1 \frac{C_2^2}{C_3} + SR_F C_1}{S^2\left(R_F R_2 C_1 \frac{C_2^2}{C_3} + R_F C_1\right) + SR_1 C_1 + 1} \tag{4.23}$$

$$\frac{V_{out,1}}{Vn_{gm}} = \frac{SR_F C_1 + 1}{S^2\left(R_F R_2 C_1 \frac{C_2^2}{C_3} + R_F C_1\right) + SR_1 C_1 + 1} \tag{4.24}$$

$$\frac{V_{out,1}}{Vn_{R_2}} = \frac{SR_F C_1}{S^2\left(R_F R_2 C_1 \frac{C_2^2}{C_3} + R_F C_1\right) + SR_1 C_1 + 1} \tag{4.25}$$

From the above equations given, it can be seen that the elements in the feedback path contribute to a highpass shaped noise. Whereas, the feedforward path contributes to the inband low pass noise profile. Thus, for noise analysis, only the feedforward path is considered. Also, the feedback resistor is transformed as R_{BB}

for easier calculations (Fig.4.7(a)). The time invariant model, shown in Fig.4.7(b) can be used to analyse the system noise. Various sources of noise are added as real resistances (instead of impedance). There are three fundamental sources of noise: R_s thermal noise modelled for the source resistance, similarly baseband resistance R_{BB} and passive mixer ON resistance r_{on}. The power loss due to conversion is also denoted using a virtual resistance R_{SH}, parallel to the baseband resistance R_{BB}. The amplifier noise is modeled in the conventional way as a pair of correlated voltage ($V^2_{n,gm_{TIA}}$) and current source ($I^2_{n,gm_{TIA}}$). They both depend on input voltage referred noise sources. The voltage source is connected in series and the current in shunt. The current source is multiplied with the shunt resistance and is given as $R^2_{BB}I^2_{n,gm_{TIA}}$ [4].

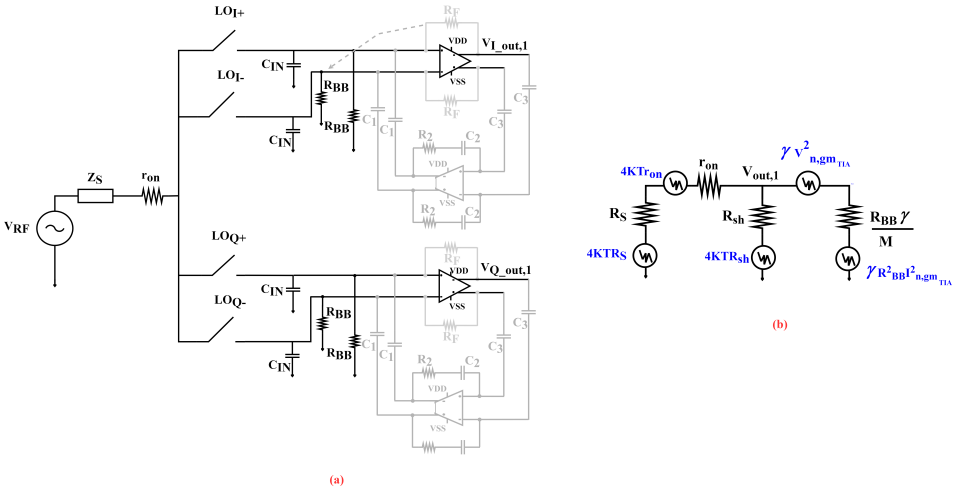

Figure 4.7: (a) Simplified circuit for noise analysis (b) Noise model for receiver circuit.

The noise gain transfer function of individual noise sources are

$$\overline{V^2_{n,out,1,R_S}} = \left(\frac{\gamma R_{BB}R_{sh}}{\gamma R_{BB}R_{sh} + \gamma R_{BB}R_S + \gamma R_{BB}r_{on} + r_{on}R_{sh} + R_SR_{sh}}\right)^2 \cdot 4KTR_S \quad (4.26)$$

$$\overline{V^2_{n,out,1,r_{on}}} = \left(\frac{\gamma R_{BB}R_{sh}}{\gamma R_{BB}R_{sh} + \gamma R_{BB}R_S + \gamma R_{BB}r_{on} + r_{on}R_{sh} + R_SR_{sh}}\right)^2 \cdot 4KTr_{on} \quad (4.27)$$

$$\overline{V^2_{n,out,1,R_{sh}}} = \left(\frac{\gamma R_{BB}R_S + \gamma R_{BB}r_{on}}{\gamma R_{BB}R_{sh} + \gamma R_{BB}R_S + \gamma R_{BB}r_{on} + r_{on}R_{sh} + R_SR_{sh}}\right)^2 \cdot 4KTR_{sh} \quad (4.28)$$

$$\overline{V_{n,out,1,R_{BB}}^2} = \left(\frac{r_{on}R_{sh} + R_S R_{sh}}{\gamma R_{BB}R_{sh} + \gamma R_{BB}R_S + \gamma R_{BB}r_{on} + r_{on}R_{sh} + R_S R_{sh}}\right)^2 \cdot \gamma R_{BB}^2 \overline{I_{n,gm_{TIA}}^2} \tag{4.29}$$

$$\overline{V_{n,out,1,TIA}^2} = \overline{V_{n,gm_{TIA}}^2} \tag{4.30}$$

The noise factor is the ratio of total output noise to the input source noise, and for the proposed circuit design is given as [4],

$$F = \frac{\overline{V_{n,out,1,R_S}^2} + \overline{V_{n,out,1,r_{on}}^2} + \overline{V_{n,out,1,R_{sh}}^2} + \overline{V_{n,out,1,R_{BB}}^2} + \overline{V_{n,out,1,TIA}^2}}{\overline{V_{n,out,1,R_S}^2}} \tag{4.31}$$

$$\begin{aligned} F = 1 + \frac{r_{on}}{R_S} + \frac{R_{sh}}{R_S}\left(\frac{R_S + r_{on}}{R_{sh}}\right)^2 + \gamma\frac{R_F}{R_S}\left(\frac{R_S + r_{on}}{\gamma R_F}\right)^2 \\ + \gamma\frac{\overline{V_{n,gm_{TIA}}^2}}{4KTR_S}\left(\frac{R_S + r_{on}}{\gamma R_F} + \frac{R_{sh} + R_S + r_{on}}{R_{sh}}\right)^2 \end{aligned} \tag{4.32}$$

The $\overline{V_{n,gm_{TIA}}^2}$ for an opamp is given as, $4KT\gamma_{amp}/gm_{TIA}$, where γ_{amp} is 2/3. Substituting, the expression to the Equation.4.32.

$$\begin{aligned} F = 1 + \frac{r_{on}}{R_S} + \frac{R_{sh}}{R_S}\left(\frac{R_S + r_{on}}{R_{sh}}\right)^2 + \gamma\frac{R_F}{R_S}\left(\frac{R_S + r_{on}}{\gamma R_F}\right)^2 \\ + \gamma\frac{2\gamma_{amp}}{3gm_{TIA}}\left(\frac{R_S + r_{on}}{\gamma R_F} + \frac{R_{sh} + R_S + r_{on}}{R_{sh}}\right)^2 \end{aligned} \tag{4.33}$$

The Noise margin can be met by sufficient gm_{TIA} which reduces the last term value or by using smaller switches (r_{on}) that changes the initial term. However, both contribute to an increase in power consumption of BB and clock driving buffers, respectively. A larger feedback resistor (R_F), improves the last term. However, the impedance matching and gain specification limits the possible NF value. Also from existing design literature reports, it can be noted that the amplifier noise is the dominating noise source [4], [5]. Also the contribution from R_{sh} should be noted, since it has direct effects on baseband amplifier noise and the second term in NF equation. R_{sh} has its effect both on the NF and input impedance and should not be neglected in calculations.

Thus, it can be seen that the design parameter R_F is limited by the S11 (Equation.4.15) and gain (Equation.4.20). Thus, optimizing the noise is limited. Mixer's on-resistance can be decreased, however, the effect in NF is trivial and also consumes more power. Also, another requirement for programmable bandwidth requires more capacitance because of R_F limited tuning range. Thus, to increase the

R_F, the input impedance (Z_{in}) of the RX chain (with RF and BB stages) is increased using a balun (Figure.4.8). Since the value required to provide input impedance matching is increased, R_F value can be easily increased. Careful designing is done to make sure the increased R_F value does not overboard the minimum gain specification, as an increase in R_F, enhances the gain as well.

4.3. Differential 4-path passive mixer

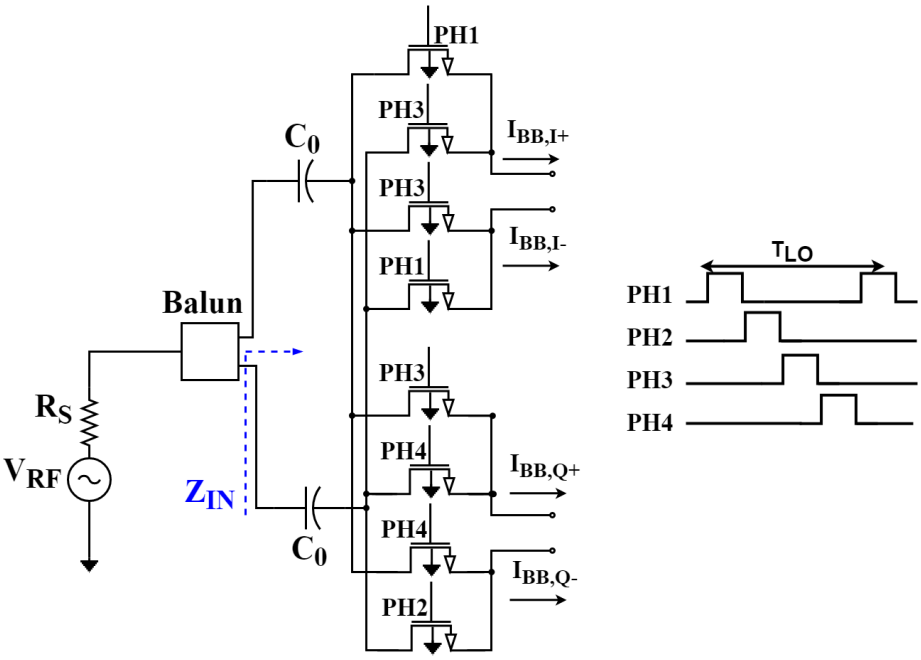

Figure 4.8: The proposed 4-path passive mixer-first design schematics.

The antenna is modelled as an input voltage source V_{RF} and R_S (50Ω). The differential form of the proposed n-path passive mixer is used in this thesis (Fig.4.8). The single-ended input is converted to differential pair by off-chip balun [6]. The balun selected provides a 1:4 impedance ratio with insertion loss around 1 dB for the specified frequency band (Appendix B). The insertion loss is also added as a part of the receiver chain during the simulation. An off-chip input capacitance C_0 of value, 400 pF is used to block the low frequency signals (below 400 MHz). The architecture increases the range of BB resistance possible. Since, the value of BB impedances is constrained by the input impedance matching (S11 dB). From the section.3.2.1, it is seen that $Z_S = r_{on} + \frac{R_{BB}\gamma}{M}$. With the balun design, the resistance seen at mixer input is four-times. For the differential design, the r_{on} is twice its value (seen as series resistance at differential input). Altogether the BB resistance can be doubled. The bandwidth of the receiver chain depends on the

BB impedance. For the 802.11ah 1/2 MHz bandwidths, this increase relaxes the capacitor value, which otherwise would require theoretically, 3.18 nF (Appendix B). Now, each path operates differential, but the anti-phase NMOS switches (say, 0 ° and 180 °) are together connected to a single capacitance [7]. Thus, for even harmonics, the average DC value is summed to be zero (Fig.4.8). The BB voltages ($V_{I/Q,+/-}$) are considered as the output connecting to the rest of the RX chain. The switches down-convert the RF signal to BB and also up-convert, thus producing an N-path based filter at RF input. Thus, differential quadrature outputs are generated at the mixer outputs.

4.3.1. Design parameters : r_{on}, W/L

The value of r_{on} is used for calculating the size of NMOS switches. From the design equation in section.3.2.1, the input impedance matching and the analyses of the advantage in using a higher BB resistance support smaller value for r_{on}. Even in terms of NF, a smaller r_{on} value is beneficial. For an NMOS switch, the r_{on} is proportional to *L/W* [8]. The length of the NMOS switch is considered to be 40 nm, the lowest for the technology used. The smaller channel length increases the speed of the devices and lowers the power consumption. Thus, for a lower r_{on}, a larger device (W) is required.

The limiting factor for the lowest possible value of r_{on} is power consumption. For the aim to design the receiver within 4 mw power consumption, the clock generation is estimated to have a 1 mW power consumption, considering 2.5 mW for the BB, 0.25 mW power consumption for the buffers driving the switches. For 0.25 mW power consumption, the capacitance value (c_{mix}) that can be driven is given by, power consumed = $c_{mix} \times VDD^2 \times f_{LO}$. For a $VDD = 1.1V$ (standard for 40 nm technology), f_{LO} = 1 GHz, the capacitance value is 200fF. Each micrometer in a mixer can be considered as capacitor of value 1fF. Thus, a 200fF can be mapped to 200 μ m. For each of 8 switches, W = 24 μ m, L = 40 nm, and V_{th} = 700m, the r_{on} = 17 Ω.

4.3.2. First stage: Passive Design parameters

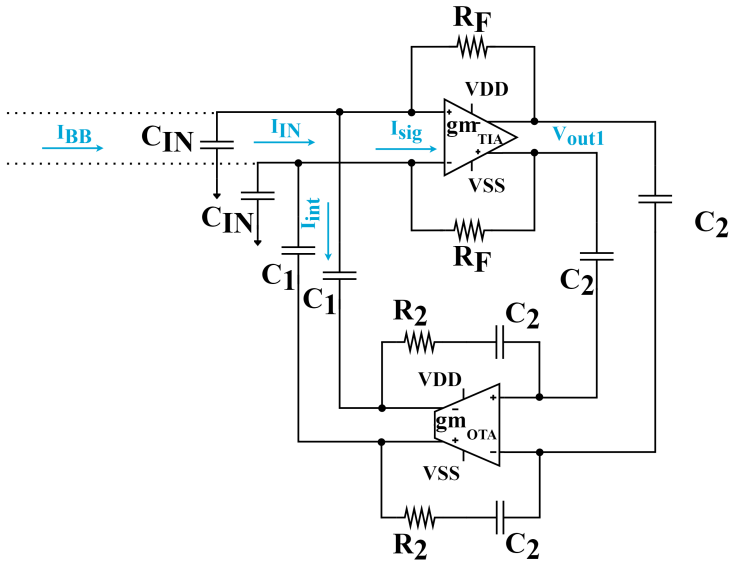

Figure 4.9: 2^{nd} order filter design for deriving the design parameters.

The value for R_F can be calculated by using the gain equation (Equation.4.20). Consider the minimum gain requirement from section.1.3.1, $A_{V,RX}$=24 dB. Substituting the values r_{on} = 17 Ω, the up-converted source impedance R_S = 200 (Section.4.3.1), we get R_F = 7 KΩ. Analyzing the stability equation (4.10), for $\omega_Z > 10\omega_n$ and R_F = 7 KΩ, the gm_{OTA} required is 14 mS. The location of the zero increases with gm, but also increases the power consumption of the receiver, so the minimum stable condition is chosen.

Considering the R_F value to be 7 KΩ, the other passive components value are derived using the bandwidth and Q-factor equations. For calculations, the variable C_3 is assumed to be equal to C_2, there by reducing the number of unknown variables for designing (Figure.4.9). The bandwidth (Equation.3.11) is equated to 4 MHz for ZIF design. The Q-factor (Equation.3.12) value is considered to be > 0.7 for complex conjugate poles.

$$\omega_n = \sqrt{\frac{1}{R_F R_2 C_1 C_2}} \iff \pi 2MHz \tag{4.34}$$

$$R_2 C_2 = \frac{1}{4\pi^2 10^{12} R_F C_1} \tag{4.35}$$

$$Q = \sqrt{\frac{R_2 C_2}{R_F C_1}} \tag{4.36}$$

$$R_2 C_2 = C_1 0.49 R_F \tag{4.37}$$

Substituting, the value of R_2C_2 from Equation.4.37 to Equation.4.35, a single value for the term C_1 = 17 pF is derived. Since, R_2C_2 as individual values does not alter any of the above equations, only their product value should remain a constant. Assuming R_2 = 10 KΩ, the C_2 is calculated close to 3pF. The other important parameter is the gm_{TIA} of the feedforward stage. From the noise specification, a standard NF < 6 dB is aimed. Substituting all the resistor values in the equation.4.33 (Table.4.1), a gm_{TIA} of 3 mS is calculated for an optimized NF of 6 dB.

Antenna Source	Mixer r_{on}	Power loss R_{sh}	R_F	First stage - opamp
1	0.34	0.314	0.02238	0.0101/gm

Table 4.1: Noise contribution of individual sources.

4.4. 1st order low pass filter

Following the first stage, the first order low pass filter consists of the differential inverter as its amplifier, to satisfy its input dc bias (Figure.4.10(a),(b)). The input resistance $R_{S,SP}$ converts the voltage to current. The feedback resistor along with the inverter provides a low impedance path, amplifies and converts it back to voltage. The gain and input impedance equations with finite value gm are derived using small signal (Figure.4.10(c)).

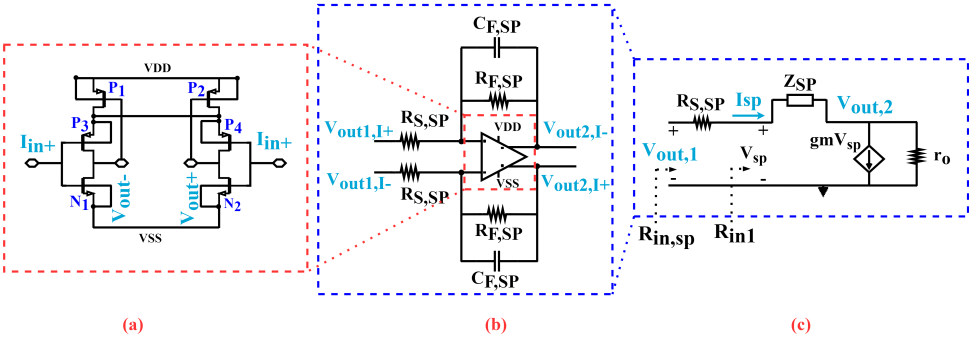

Figure 4.10: (a) Basic differential TIA structure (b) Single pole design with inverter as amplifier (c) Small signal model of design in (b).

4.4.1. Gain and input impedance equation

The voltage gain across the amplifier is derived from the small signal model (Figure.4.10(c)). The impedance Z_{SP} is $R_{F,SP} \| C_{F,SP}$. Analysing the KCL equation at input and output node, the gain is calculated as,

$$\frac{V_{out,1} - V_{sp}}{R_{S,SP}} = \frac{V_{SP} - V_{out,2}}{Z_{SP}} \tag{4.38}$$

$$\frac{V_{SP} - V_{out,2}}{Z_{SP}} = gmV_{SP} + \frac{V_{out,2}}{r_o} \tag{4.39}$$

$$A_{V,SP} = \frac{\frac{sC_{F,SP}R_{F,SP}r_o - gmR_{F,SP}r_o}{R_{S,SP}}}{S^2R_{F,SP}^2C_{F,SP}^2 + S\left(2C_{F,SP}R_{F,SP} - c_{F,SP}R_{F,SP}\right) + 1 + \frac{R_{F,SP}^2}{r_o} - (gm+1)R_{F,SP}} \tag{4.40}$$

From the equation, it can be seen that, even for a single pole system, there exist a zero under finite gm condition. However, this zero is placed far away from the desired pole ($\omega_{Z,sp} \approx \frac{gmr_oR_{F,SP}}{R_{F,SP}C_{F,SP}}$). It consists of two real poles, one at the $\omega_n = \frac{1}{C_{F,SP}R_{F,SP}}$ location and other pole far way from the desired frequency band. The DC gain of the amplifier, considering the impedance $Z_{SP} = R_{F,SP}$, is calculated as

$$A_{v,SP_{DC}} = \frac{R_{F,SP}r_o(gmR_{F,SP} - 1)}{R_{S,SP}(r_o - R_{F,SP}^2 - R_{F,SP}r_o(gm+1)} \approx \frac{R_{F,SP}}{R_{S,SP}} \tag{4.41}$$

For the input impedance derivation, the circuit is split into two halves. The R_{in1}, shown in (Figure.4.10(c)), can be calculated similar to the feedforward TIA expression. The impedance, R_{in1} (Equation.4.13), in series with $R_{S,SP}$ is given as the input impedance of the second stage.

$$R_{in} = \frac{R_{F,SP}}{gmr_o} + \frac{1}{gm} \tag{4.42}$$

$$R_{in,sp} = R_{S,SP} + \frac{R_{F,SP}}{gmr_o} + \frac{1}{gm} \tag{4.43}$$

The input impedance $R_{in,sp}$ of the second stage should be higher than the output impedance of the first stage to avoid loading. Since in the ZIF architecture, the $R_{in,sp}$ can be mapped as a parallel resistor to the first stage output impedance.

$$R_{IN,TIA} = \frac{R_F}{gm(r_{o,TIA} \| R_{in,sp})} + \frac{1}{gm} \tag{4.44}$$

Hence, a smaller value decreases the input impedance of the first stage and hence the input impedance matching (S11).

4.4.2. Noise Analysis

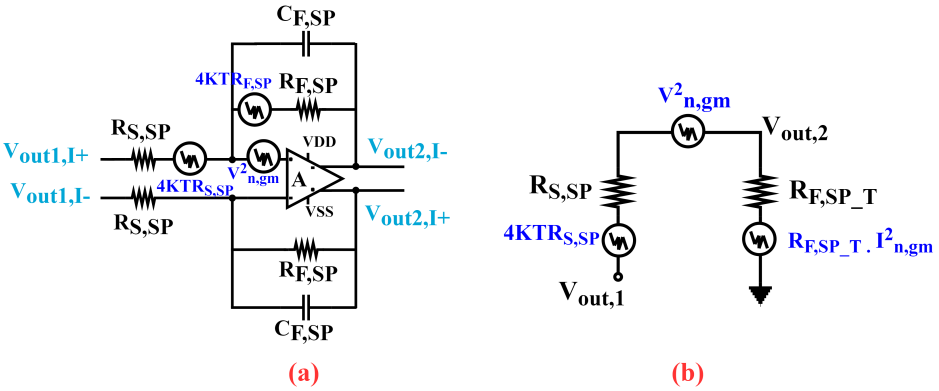

Figure 4.11: (a) Second stage filter with noise sources (b) Noise source model.

Similar to the first stage noise analysis, there are three dominant noise sources (Figure.4.11)(a). The thermal noise from $R_{S,SP}$,R_{F,SP_T} and the opamp voltage noise and the current noise with nodal impedance. For calculation purpose, the feedback resistor $R_{F,SP}$ is transferred to input as R_{F,SP_T} $(= R_{F,SP}/(1+A))$ (Figure.4.11)(b). The second stage noise are referred to the input of baseband (Figure.4.12). The noise sources are divided by the first stage gain. The factor of γ is introduced for baseband transformation. The noise gain functions of individual sources are,

$$\overline{V_{n,out,2,R_S}^2} = \left(\frac{R_{F,SP\_T}}{R_{F,SP\_T} + R_{S,SP} + R_S}\right)^2 4KTR_S \tag{4.45}$$

$$\overline{V_{n,out,2,R_{S,SP}}^2} = \left(\frac{R_{F,SP\_T}}{R_{F,SP\_T} + R_{S,SP} + R_S}\right)^2 \frac{\gamma 4KTR_{S,SP}}{A_{First\_stage}^2} \tag{4.46}$$

$$\overline{V_{n,out,2,R_{F,SP\_T}}^2} = \left(\frac{R_{S,SP} + R_S}{R_{F,SP\_T}^2 + R_{S,SP} + R_S}\right)^2 R_{F,SP\_T}.I_{n,gm}^2 \tag{4.47}$$

$$\overline{V_{n,out,2,gm}^2} = \overline{V_{n,gm}^2} \tag{4.48}$$

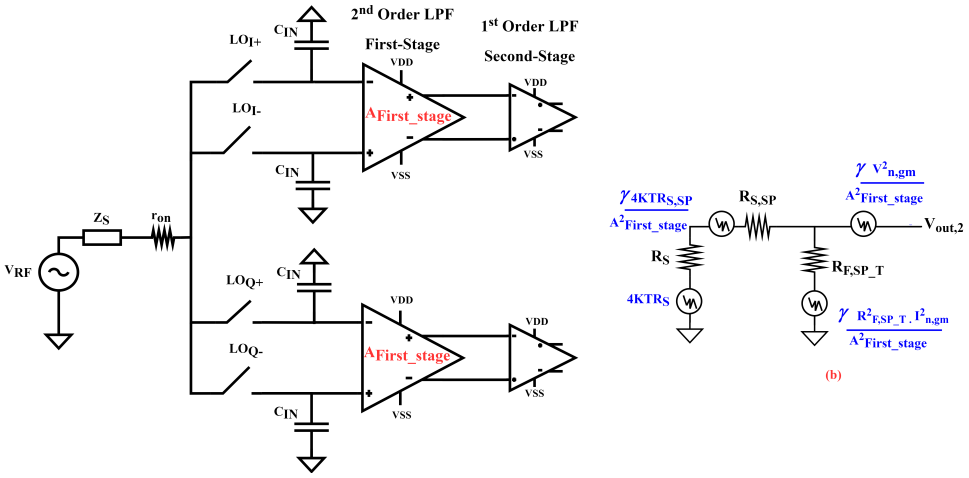

Figure 4.12: Input referred Noise of Second stage (1^{st} order filter).

$$F_{SP} = 1 + \frac{\gamma R_{S,SP}}{R_S A^2_{First\_stage}} + \frac{\gamma R_{F,SP}}{R_S A^2_{First\_stage}} \left(\frac{R_{S,SP} + R_S}{R_{F,SP}} \right)^2 + \frac{\gamma V^2_{n,gm_{sp}}}{4KTR_S A^2_{First\_stage}} \left(\frac{R_S + R_{F,SP} + R_{S,SP}}{R_{F,SP}} \right)^2 \tag{4.49}$$

Similar to the first stage, noise can be optimized by increasing R_{F,SP_T} and gm_{SP}. There is also another design parameter $R_{S,SP}$. From the noise equation, it can be seen that the input resistor $R_{S,SP}$ affects the second term in the above equation. Thus a higher value will directly increase the NF. Though, suppressed by the gain, a larger value can contribute to noise. However, to avoid the first stage loading, the input impedance of the second stage should be greater than output impedance of the first stage ($r_{o,TIA}$). This limits the value of $R_{S,SP}$, and indirectly the $S11$. So, proper designing is required to look into the trade-off and assign values.

4.5. ZIF architecture: Design parameters

The entire ZIF architecture with 2^{nd} order LPF filter as the first stage and 1^{st} order LPF filter as the second stage is shown in Figure.4.13. The design parameter considering only first stage was given in Section.4.3.2. Separate analysis cannot be done for the second stage alone. For the receiver design structure, the second stage design parameter depends on the first stage values also, like the input impedance trade-off discussed it Section.4.4.1 and the noise analysis.

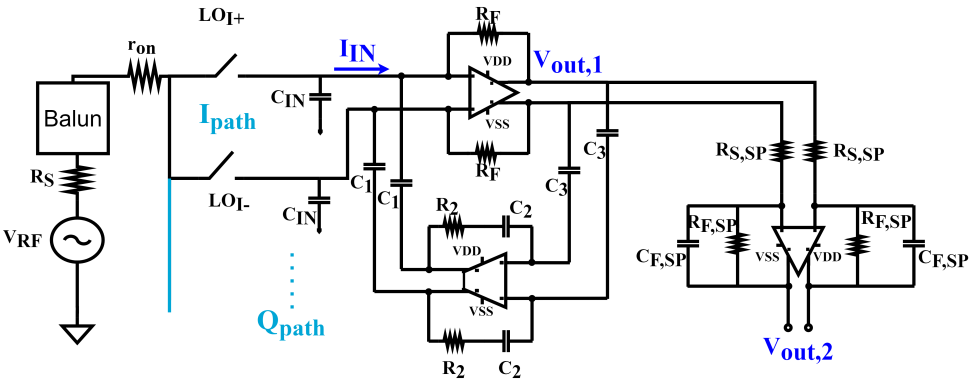

Figure 4.13: ZIF architecture (Ipath alone).

The input resistor of the second stage has to be carefully designed because it affects directly the first stage gain, receiver's noise and input impedance. From Equation.4.43,

$$R_{in,sp} = R_{S,SP} + \frac{R_{F,SP}}{gm_{SP}r_{o_{SP}}} + \frac{1}{gm_{SP}} \iff R_{in,sp} \approx R_{S,SP} \tag{4.50}$$

The above approximation is valid because for the intended low power operation $1/gm_{SP}$ should be negligible. The intrinsic gain ($gm_{SP}r_{o_{SP}}$) is of the order 30-50 for CMOS 40 nm technology (L = 1μm), Hence, the second term contribution can be approximated to a small value. Modifying the Equation.4.44 with the approximation,

$$R_{IN,TIA} = \frac{R_F}{gm_{TIA}(r_{o,TIA} \| R_{S,SP})} + \frac{1}{gm_{TIA}} \tag{4.51}$$

From Section.4.2.2, the input impedance of the feedfoward TIA is directly related to the the matching equation,

$$R_S = r_{on} + \frac{\gamma R_{IN,TIA}}{4} \tag{4.52}$$

The standard S11 dB value, -20 dB is considered for matching. Substituting all values from Section.4.3.2 (R_F = 7 $K\Omega$, gm_{TIA} = 5 mS, $gm_{TIA}r_{o_{TIA}}$=50), the $R_{S,SP}$ = 5.5 $K\Omega$. Similarly, the receiver gain equation can also be modified for the loading effect as (Equation.4.16 and from Section.4.2.2),

$$A_{v,RX} = \frac{\sqrt{2}}{\pi} \frac{1}{r_{on} + R_S} \frac{R_{S,SP}.r_{o,TIA}(1 - gm_{TIA}R_F)}{gm_{TIA}r_{o,TIA}R_{S,SP} + (R_{S,SP} + r_{o,TIA})} \tag{4.53}$$

Theoretically a gain drop of 3 dB is calculated, results from $R_{S,SP}$ = 5.5 $K\Omega$. The design so far has been for minimum gain specification (24 dB). So, to satisfy the specification, the gain from second stage should be at least 3 dB from Equation.4.41

($A_{V,SP} = R_{F,SP}/R_{S,SP}$), the value for $R_{F,SP}$ = 7.7 $K\Omega$. For the second stage LPF filter, the capacitance value $C_{F,SP}$ is calculated from the bandwidth Equation.4.40 ($\omega_{SP} = 1/R_{F,SP}C_{F,SP}$) as $C_{F,SP}$ = 10pF.

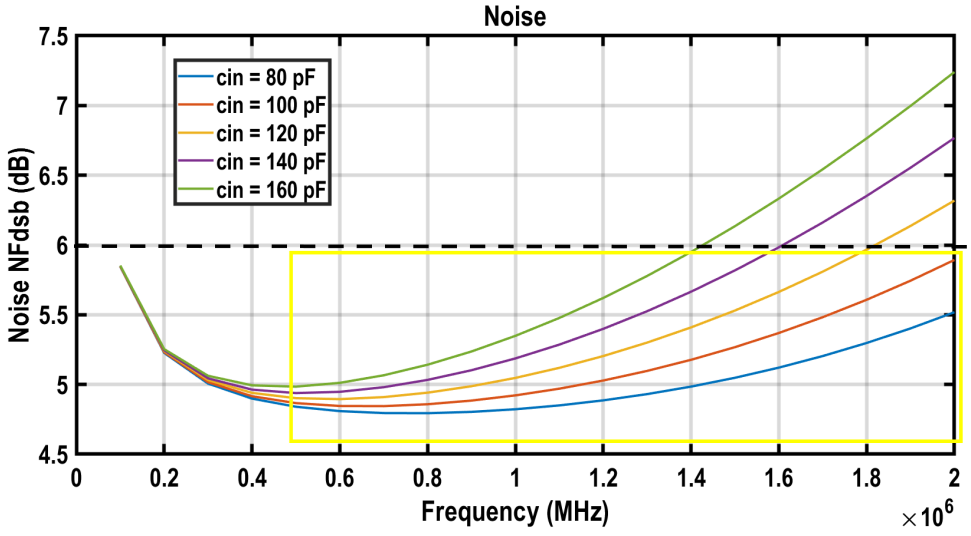

Figure 4.14: NF value for different C_{IN}.

The input capacitance C_{IN} value, for a simple TIA with feedback resistance alone can go upto 700pF (Appendix B). However, here some quality amount of current is also drawn with the help of C_1 in the feedback structure. The value of C_{IN} is limited by the linearity analysis, to absorb the blocker current. The blocker specification for 802,11ah is not explicitly given in the standard. The other dependence of C_{in} is NF and bandwidth. From the simulation results, shown in Figure.4.15, it can be seen that for the required band of operation, then noise curve is below 6dB for $C_{IN} = 100pF$. Also, the C_{IN} with finite gm causes the complex poles and moves the zero location far then what was calculated. Thus, from simulation results, a gm_{OTA} of 6 mS is enough to place the zero at 20 MHz (10 times the pole location). Also, from the simulation, it is clear that, the variation in gm does not affect the bandwidth or the gain. So all other design parameters can be unaltered.

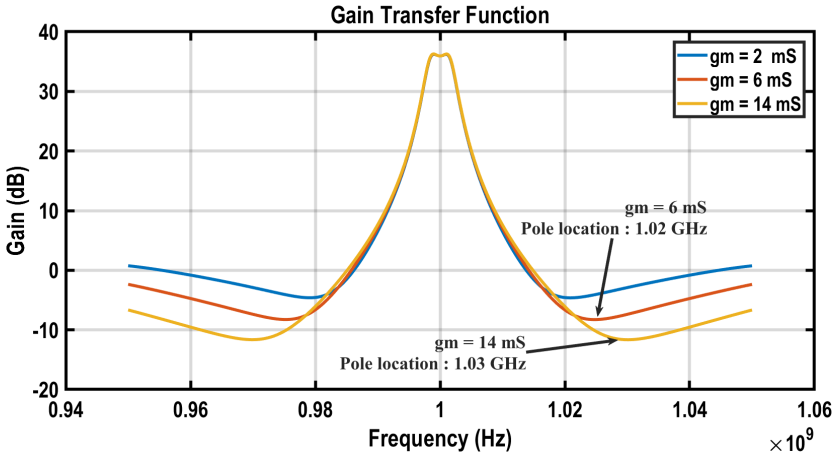

Figure 4.15: Gain transfer function for different gm_{OTA} values.

4.5.1. Programmable Gain: design parameters

The receiver should support a programmable gain of 24 to 44 dB. The visible tuning parameters for gain are resistors. The overall gain for both stages cascaded can be derived from Equation.4.41 and Equation.4.20 as,

$$A_{V,RX} = \frac{\sqrt{2}}{\pi} \frac{1}{r_{on} + R_S} \frac{R_F R_{F,SP}}{R_{S,SP}} \tag{4.54}$$

The resistor values R_F are fixed with respect to input impedance matching value. Compromising on matching, the R_F can be increased till 15 $K\Omega$, until S11 < -10 dB. However, the gain can be only increased till 30 dB (4.54). The $R_{S,SP}$ has to be decreased to increase the gain of the receiver system. However, decreasing the $R_{S,SP}$, again degrades the S11 further (>-10 dB). So it is maintained constant throughout the programmability mode. The other parameter is $R_{F,SP}$. Increasing in $R_{F,SP}$ can be helpful in increasing the gain as well as decreasing the NF. Although, it can still affect the S11 from Equation.4.50. However, its contribution is only 5% and S11 can be maintained around -10dB. The capacitance values are adjusted according to the bandwidth equations.

The last parameter left to design is the gm_sp. The transconductance of second stage can be calculated using the noise equations. The NF of first stage is designed for 5.6 dB (Section.4.3.2). The aim is to design the ZIF architecture within NF of 6 dB. Thus, the margin for gm can be calculated by equating the noise Equation.4.61 to 0.4 dB (Table.4.2). For a NF of 0.36 dB, the gm_{SP} is designed as 3 mS.

Antenna Source	$R_{S,SP}$	$R_{F,SP}$	Second stage - opamp
1	0.00506	0.0355	$4.68^{-6}/gm_{SP}$

Table 4.2: Noise contribution of individual sources

From simulations, the Q-factor value is not enough. Since, the values were calculated with ideal equations, the effect from finite gm is not accounted. As with finite gm, the unknown variables equations were complex and were not converging easily to solutions. The only assumption made for designing, $C_3 = C_2$, is analyzed. Re-assuming, $C_3 = C_2/\alpha$, the frequency and gain transfer functions are calculated as (From Section.3.3.2),

$$G_{FS} = \frac{V_{out,1}}{i_{BB}} = \frac{-R_F}{S^2 C_2^2 \frac{C_1}{C_3} R_2 R_F + S C_1 \frac{C_2}{C_3} R_F + 1} \tag{4.55}$$

$$G_{FS,new} = \frac{-R_F}{\alpha S^2 C_2 C_1 R_2 R_F + \alpha S C_1 C_2 R_F + 1} \tag{4.56}$$

$$\omega_n = \sqrt{\frac{1}{\alpha R_F R_2 C_1 C_2}} \tag{4.57}$$

$$Q = \sqrt{\frac{R_2 C_2}{\alpha R_F C_1}} \tag{4.58}$$

$$\omega_Z = \sqrt{\frac{gm_{OTA}}{\alpha R_2 C_1 C_2}} \tag{4.59}$$

Comparing it with the ideal equations, It is a common multiplication term and doesn't change any relation. This term can be included as the term to denote the effect of finite gm. The simulation results show that, decreasing the α value, improves the Q-factor (Figure.4.16). However, increases the required C_3 value. From simulation, the value of α is 0.2 (for the required bandwidth and ACR). The same factor is used for other configurations and the theoretical values was seen to be matching the simulation outputs. Thus, the required value of C_3 is 15 pF.

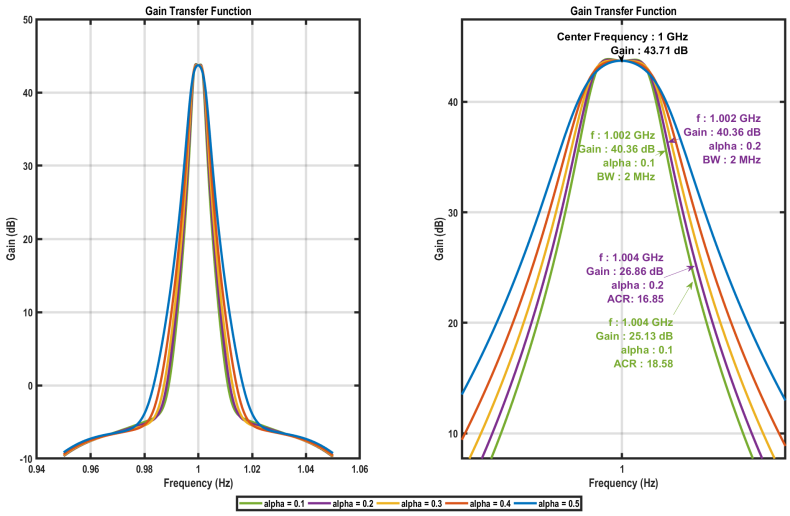

Figure 4.16: Effect of α on the bandwidth and Q-factor.

Parameter	Value
Length of the NMOS Switch L_{mixer}	40 nm
Width of the NMOS Switch W_{mixer}	24 μm
Input baseband capacitor C_{IN}	100 pF
Feedback capacitance OTA C_1	17 pF
Feedback capacitance OTA C_2	3 pF
Feedback capacitance OTA C_3	15 pF
Feedback Resistor OTA R_2	10 $K\Omega$
Feedback Resistor TIA R_F	5 $K\Omega$
Input resistor Second-stage $R_{S,SP}$	5.5 $K\Omega$
Feedback resistor Second-stage $R_{F,SP}$	7.7 $K\Omega$
Feedback capacitance Second-stage $C_{F,SP}$	10 pF
Transconductance of TIA gm_{TIA}	3 mS
Transconductance of OTA gm_{OTA}	6 mS
Transconductance of Second-stage gm_{SP}	3 mS

Table 4.3: ZIF architecture Design parameters for minimum gain configuration.

4.5.2. Inverter design

The gm of the amplifiers, were derived using the design equation. The inverters has to be designed accordingly. The differential inverter used for the amplifiers in feedforward first stage design and the second stage. The simple pseudo differential inverter is used for feedback OTA. The input stage requires proper feedback cancellation to maintain the negative feedback loop. So, a fully differential circuit is

required. However, for the inverter in OTA is a pseduo differential circuit maintaining good linearity. Since, the output swing of pseudo differential circuit ($VDD/2$) is higher then the fully differential circuit ($(VDD - VOV_{P1})/2$). The second stage following the first stage is also designed as fully differential circuit to support common DC bias.
For the self-biased amplifiers implemented, the important parameter to be designed is the W/L ratio depending on the gm. For any MOSFET device working as an amplifier, the intrinsic gain gmr_o should be maximum. From [8], the gm is $(2I_{Drain\_current})/Vov$, where Vov denotes the overdrive voltage and is given as $V_{gs} - V_{th}$. The output resistance is $1/\lambda I_{Drain\_current}$. Simplifying, the equation, the intrinsic gain is proportional to $2L/(V_{gs} - V_{th}\lambda)$. The channel length modulation factor λ can't be designed, and the over drive voltage is mainly dependent on the biasing point. The only parameter to improve gain is L, because of large channel length, the device can slow down and increase area. However, large L also reduces the flicker noise. The L value is considered to be layout friendly as well, since the area is a big constrain (with huge capacitance required for narrow bandwidth). The L value is chosen after noise analysis, to improve the flicker noise level. The length of the MOSFET is increased and the flicker noise level is observed for L = 240 nm and L = 1 um. It gives a noise drop of 5 dB, suppressing the flicker noise to be around the desired specification, 6 dB (Appendix B). The inverter PMOS is sized 4X times the NMOS to support the mobility ratio.

Pseudo Differential inverter design parameters

The inverter is used for the OTA design and need to be designed for a gm of 6 mS (Figure.4.17(a)). For the MOSFET designed, $|V_{gs}|$ = $|V_{ds}|$, since the output and the input are connected together through the resistor. In the inverter $|V_{gs}|_{PMOS}$ = $|V_{ds}|_{PMOS}$ = $|V_{gs}|_{NMOS}$ = $|V_{ds}|_{NMOS}$. So from the supply to ground, $VDD - V_{dsPMOS} - V_{dsNMOS}$ = 0. Hence the $V_{dsoutput}$ is $VDD/2$. For a standard 1.1V VDD, the output is 550 mV. For a 40 nm, L = 1 m, V_{thPMOS} = 423.3 mV and V_{thNMOS} = 422.6 mV, thus for the inverter all devices work in saturation, $V_{gs} > V_{th}, V_{ds} > V_{gs} - V(th)$. Now the required W is calculated from the equation [8]

$$gm = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) \tag{4.60}$$

The length of the channel is fixed by the flicker noise analysis and the $(V_{gs} - V_{th})$ is fixed for the biasing. The value of W is calculated for gm = 6 mS (Table.5.7)

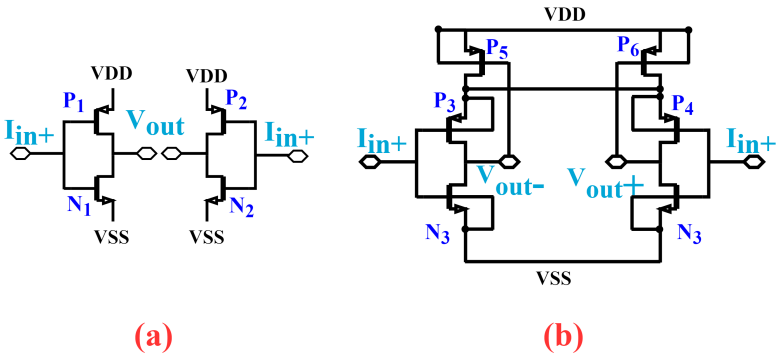

Figure 4.17: (a) Pseudo Differential inverter schematics (b) Differential inverter schematics.

PMOS	NMOS
W : 256 μm; L : 1 μm	W : 64 μm ; L : 1 μm

Table 4.4: OTA inverter design parameter (gm = 6 mS).

Fully differential inverter design parameters

Considering the schematics given in the (Figure.4.17(b)). Following a similar analysis as in previous section, from supply to ground, VDD - V_{dsP5} - V_{dsP3} - V_{dsN3} = 0. With the resistor feedback, V_{dsP3} = V_{gsP3} = V_{dsN3} = V_{gsN3}. Hence to keep the transistors in saturation, V_{gs} > 500 mV and V_{dsP3} should be > $V_{gsP3} - V_{th}$ (> 200 mW). This exceeds the value of input supply voltage, so either the VDD has to be increased or to operate in saturation, the V_{th} of P5/P6 can be increased. Also, the overdrive voltage of the inverter devices is decreased. This allows to operate all devices in saturation, however, because of lower overdrive, for the same OTA specification, the differential inverter would require more W than the inverter design. Thus at saturation, the output voltage is $(VDD - Vov)/2$. Using similar Equation.4.60, the value of gm for individual amplifiers are calculated.

P5/P6	P3/P4	N3/N4
W : 48 μm; L : 1 μm	W : 384 μm ; L : 1 μm	W : 96 μm; L : 1 μm

Table 4.5: TIA inverter design parameter (gm = 3 mS).

P5/P6	P3/P4	N3/N4
W : 32 μm; L : 1 μm	W : 256 μm ; L : 1 μm	W : 64 μm; L : 1 μm

Table 4.6: Second stage inverter design parameter (gm = 3 mS).

4.6. LIF Architecture

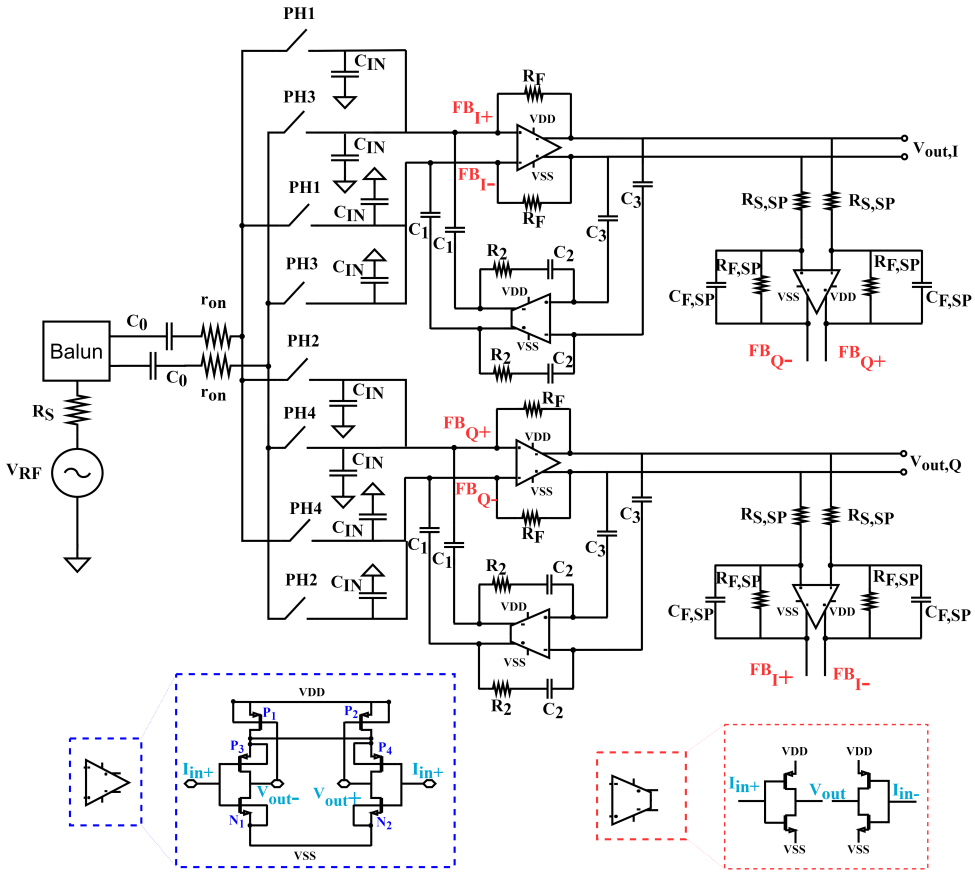

Figure 4.18: LIF architecture BPF with inverter as amplifier.

The 2^{nd} order first stage filter and complex feedback second stage, are designed with inverter as amplifiers (Figure.4.18). The input impedance and gain equations of first stage are similar to the one defined in ZIF design architecture. Initially, a low pas filter with bandwidth equal to four times the center frequency.is designed (from Section.3.4.1). The required gm to satisfy the input impedance equation results in unstable behaviour for 2^{nd} Order system. The gm constrain for the second stage is calculated based on the stability of the transformed BPF to the desired center frequency with reduced roll-off (Section.3.4.1). The first stage parameters are used to provide the bandwidth, and gain. The bandwidth should be modified for the required bandwidth for the LIF design. For frequency shifting, only a small gm value is required, contributing to more NF degradation. From, the noise model equations, the NF of the second stage is derived as (Section.4.4.2)

$$F_{SP} = 1 + \frac{\gamma R_{S,SP}}{R_S A^2_{First\_stage}} + \frac{\gamma R_{F,SP}}{R_S A^2_{First\_stage}} \left(\frac{R_{S,SP} + R_S}{R_{F,SP}} \right)^2 + \frac{\gamma V^2_{n,gm_{sp}}}{4KTR_S A^2_{First\_stage}} \left(\frac{R_S + R_{F,SP} + R_{S,SP}}{R_{F,SP}} \right)^2 \quad (4.61)$$

4.6.1. BPF filter design parameters

The design parameters used for ZIF architecture can be used for the LIF design as well. Since it provides a design producer for the low pass filter (Section.4.3.2). The first stage values are derived for the minimum gain and cut-off frequency four times the center frequency (for 1.5 MHz, BW = 3 MHz). The value of $gm_{SP}QR_F$ should be less than 1. For the low gain mode, R_F is 5 $K\Omega$, and considering the Q as 0.25, the required gm_{SP} is 800 μS. However, this gm_{SP} is modified for stable operation and is not perfectly matched at the input. The maximum input matching is obtained for gm_{SP} calculated using the Equation.4.62

$$Z_{BB} = \left(\frac{R_F}{1 + A} - jgm \right) \quad (4.62)$$

The gm is equated to the imaginary part of the impedance value at the required frequency, thereby moving the center frequency. From simulation, the required gm is 1.1 mS. However, the modified stable operation gm value is lesser than the value calculated from Equation.4.62. Observing from simulation results, a reduced S11, around -10 dB is achieved. The gm_{SP} is very low, and could cause significant increase in NF. From simulations, this reduced gm_{SP} value for second stage increases the NF by 2 dB (from 6.1 dB to 8 dB). The input resistor $R_{S,SP}$ and $R_{F,SP}$ are both designed for 5 $K\Omega$. It reduces the gain of the second stage by improving the NF. The gm_{tia} of the 2^{nd} order LPF is increased to compensate for the loss. There is a trade-off with power. However, the power consumption from second stage is reduced (4 X lower compared to ZIF), because of small gm. The gm of first stage can be increased up to the balancing point. From simulation, increasing the gm of the first stage from 3 mS to 6 mS, the noise is 7.25 dB for low gain mode (24 dB). The power consumption is still maintained below 2.8 mW in BB (desired specification). The Changing R_F for gain progarammability, affects the gm, since $gm_{sp}R_FQ$ should be less then 1, and for increase in R_F, the gm_{sp} should be changed for every mode. And both the resistor $R_{S,SP}$ and $R_{F,SP}$ are designed for minimum noise. Thus, the other buffer stages used for impedance isolation is used for gain programmability. The parallel capacitance $C_{F,SP}$ is placed for improving the attenuation for the zero produced from the first stage feedback network. In ideal virtual ground condition, $C_{F,SP}$ is a parallel capacitance to C_{IN}. From simulation it was observed that, the S11 gets deteriorated if $C_{F,SP}$ increasing, since it adds to the imaginary impedance value. Hence, the minimum $C_{F,SP}$ required for for S11 around -10 dB is used. From simulation, it is 1 pF (Figure.4.19).

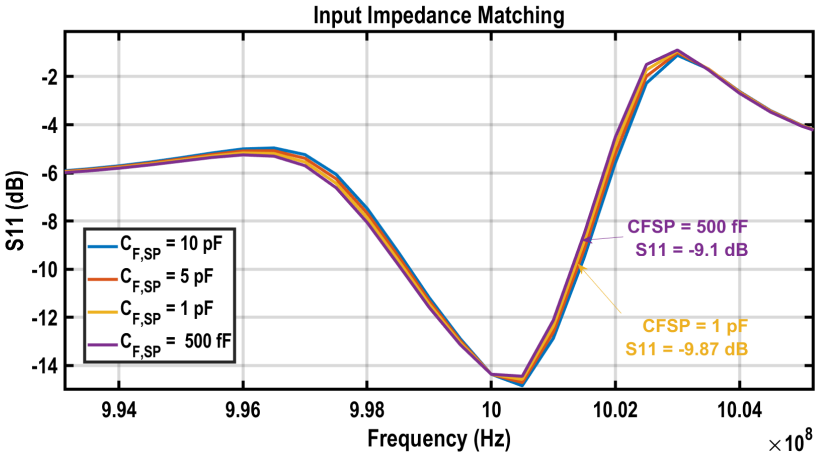

Figure 4.19: Optimized $C_{F,SP}$ from S11 simulation results.

The inverter's for the new gm (800 uS) is designed in the same procedure specified in Section.4.5.2

P5/P6	P3/P4	N3/N4
W : 8 μm; L : 1 μm	W : 64 μm ; L : 1 μm	W : 16 μm; L : 1 μm

Table 4.7: OTA inverter design parameter (gm = 6 mS).

4.6.2. Buffers: Gain programmability

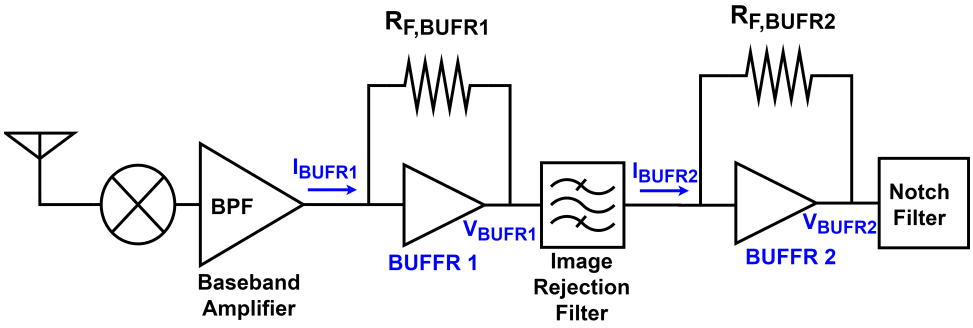

Figure 4.20: Buffers placement in the receiver chain.

The buffers are placed in front of the image rejection and notch filter (Figure.4.20). The very low input impedance of the polyphase filter can affect the driving stage. Hence, the buffer is placed to provide impedance isolation. The buffer also has a

feedback resistor $R_{F,BUFR}$ used for gain programmability. As seen, from previous section, an extra variable is required to provide the necessary gain programmability in LIF mode. The gain of the buffer is given as,

$$\frac{V_{out,bufr}}{i_{in,bufr}} = -R_{F,BUFR1} - \frac{1}{gm} \tag{4.63}$$

The gain is equal to - $R_{F,BUFR}$, since $1/gm >> R_{F,BUFR}$. The polyphase filter can be considered as a bandstop filter for the image and passes all other signals ideally. The cascaded gain for both the buffers, $R_{F,BUFR1} \times R_{F,BUFR2}$ can be used for gain programmability. The BPF is designed for gain of 24 dB, however the image rejection and notch filter accounts for signal loss because of RC or CR series combination (Figure.4.23). The 3 stage image rejection accounts for a gain drop of 7 dB, and the notch also can account for 3 dB signal loss (from simulation). This gain drop also needs to be compensated. Analysing the noise for both the amplifiers using small signal models given in Figure.4.21

$$F_{bufr1} = 1 + \frac{\gamma R_{F,BUFR1}}{R_S A A_{BPF}^2} + + \frac{\gamma V_{n,gm_{bufr1}}^2}{4KTR_S A_{BPF}^2}\left(\frac{R_S + \gamma R_{F,BUFR1}}{\gamma R_{F,BUFR1}}\right)^2 \tag{4.64}$$

$$F_{bufr2} = 1 + \frac{\gamma R_{F,BUFR2} A_{PPF_L OSS}^2}{R_S A A_{BPF}^2 A_{BUFR1}^2} + + \frac{\gamma V_{n,gm_{bufr2}}^2 A_{PPF_L OSS}^2}{4KTR_S A_{BPF}^2 A_{BUFR1}^2}\left(\frac{R_S + \gamma R_{F,BUFR2}}{\gamma R_{F,BUFR2}}\right)^2 \tag{4.65}$$

Assuming, both the resistors are equal, from simulation it was observed that 5 $K\Omega$ each is enough for the minimum gain configuration. The BPF filter stage is designed for a NF of 7.25 dB. The aim of the design is to end up with a NF of 7.3 dB for the low gain mode. The individual blocks noise contribution can be mathematically calculated using the simulation results. 0.025dB for buffer1, 0.02 dB for buffer2, 0.011 dB for image rejection filter and 0.0001 dB for notch filter. The low values for notch and image rejection filter is because of noise suppression due to the previous stage gain. The buffers contribution is mainly because of the gm. A substantial gm is required to suppress the noise and leads to increase in power consumption. The gain of BPF is considered 23 dB, and for the buffer 19 dB. $(\frac{\sqrt{2}}{\pi}\frac{R_F}{R_S + r_{on}})$

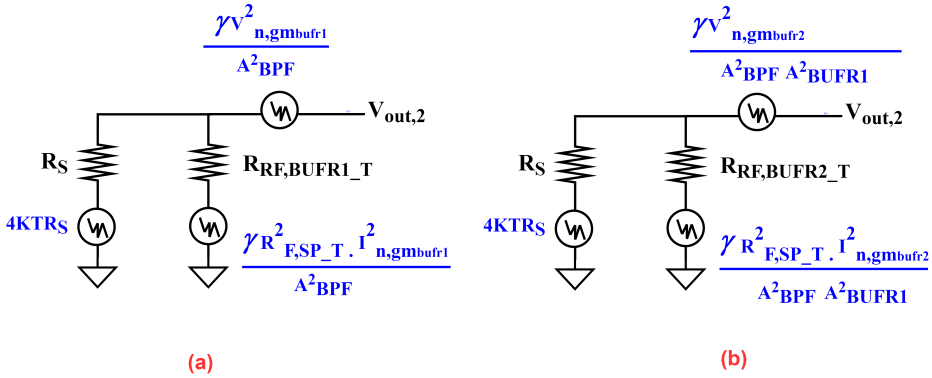

Figure 4.21: (a) Small signal model for Buffer1 (b) Small signal model for Buffer2.

source	$R_{F,BUFR1}$	amplifier	gm	NF
1	0.0018	$1.32*10^{-}5/gm$	3 mS	0.0268 dB

Table 4.8: Noise contribution for Buffer 1

source	$R_{F,BUFR2}$	amplifier	gm	NF
1	$2.44*10^{-}4$	$1.782*10^{-}6/gm$	600 uS	0.016 dB

Table 4.9: Noise contribution for Buffer 2

Equating to the desired NF, the gm of buffer1 is 3 mS and buffer2 is 600 uS (4.8,4.9).

4.6.3. Image rejection filter: passive components values

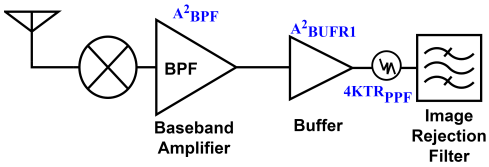

Figure 4.22: The image rejection filter noise source.

The Image rejects filter comprises of R and C value. The image rejection for 2 MHz, has to be from 997.5 MHz (f_{low}) to 998.5 MHz (f_{high}), with centre frequency at 999.5 MHz (f_{mid}). In general, the first stage of the polyphase filter is designed

for f_{high}, the second stage for f_{mid}, and the last stage for f_{low} [9]. With this design procedure, the impedance of each stage is higher than the previous stage. Considering, the second stage impedance is higher than the first stage, the load impedance value seen by the first stage is large. Thus, reducing the signal loss. From Section.3.4.2, the input impedance is considered as $R_{PPF}||C_{PPF}$. For calculation purpose, assuming there is only one stage with ideal load impedance. The dominant noise source is R_{PPF}. For four paths, the resistance can be considered as $R_{PPF}/4$. The PPF filter noise sources are input refereed with equation (Figure.4.22),

$$F = 1 + \frac{\gamma R_{PPF1}}{4R_S A^2_{First\_stage} A^2_{Buffr1}} \tag{4.66}$$

From, which the desired R_{PPF1} value is derived as 20 $K\Omega$ with NF 0.097 dB. With the resistance value known, the capacitance value for the first stage can be calculated from the pole frequency values f_{high} (Section.3.4.2). The C_{PPF} is calculated as 16 pF. The same capacitance value is used for other stages and their respective resistor values are derived concerning their pole frequencies. A 3 stage filter is proposed since for a fixed bandwidth, multiple stages are required to spread out the pole frequencies and reject the signal with the desired ratio. Figure.3.4.2 shows, the gain transfer function of a single stage filter vs. three stage filter. For the single stage, a rejection of 33 dB is created only at one frequency (f_{low} = 997.5 MHz), whereas the 3 stage can reject 37 dB of image signal over the desired bandwidth. From simulation results, for the calculated RC value, the attenuation for the image was only 35 dB. This is because of the placement of the pole frequencies. There exists a bulge between the pole frequencies. Rather than placing three poles at 999.5 MHz, 998.5 MHz, and 997.5 MHz, if the distance between the two pole frequency is decreased (999.5, 998.7, 997.8), this bulge value drops and increasing the attenuation level, without compromising on bandwidth. Since the filtering at each pole is like a notch filter, the attenuation will still be visible at 997.5 MHz. To increase the attenuation, the value of capacitance is increased to be 18 pF, The corresponding resistor values are also modified. Since there is a decrease in resistor values, the NF also improves.

	$1^{st} stage$	$2^{nd} stage$	$3^{5d} stage$
R_{PPF}	3.5 $K\Omega$	6 $K\Omega$	12 $K\Omega$
C_{PPF}	18 pF	18 pF	18pF

Table 4.10: Image rejection filter passive components values.

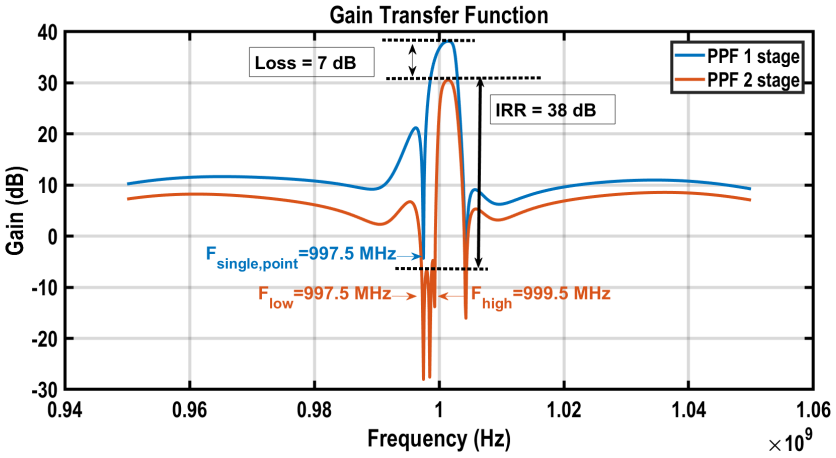

Figure 4.23: One stage vs. three stage polyphase filter design.

4.6.4. Notch filter: passive components values

The notch filter also comprises of CR components in a similar arrangement as the image rejection filter. The purpose of the filter is to improve the ACR and NACR ratios. The notch filter is placed at the 1^{st} non-adjacent channel frequency (f_{notch}). For a 2 MHz bandwidth, the center frequency is 1.5 MHz. So the notch location is 3.5 MHz. The notch filter also needs to compromise NF for the signal loss in the previous stage image reject filter. For easy layout, the same value of capacitance can be used for both the image rejection and notch filters. The contribution of the notch filter to NF is well suppressed by the input gain stages. Hence, a capacitance value similar to the image rejection filter, 18 pF is chosen. The corresponding resistor for the pole location $\omega = 1/R_{NOTCH}P_{NOTCH}$, is 1.7 $K\Omega$. However, placing the notch filter $\delta\omega$ away from the f_{notch} improves the NF. The pole frequency increases with a decrease of R_{NOTCH} values, which decreases the losses in the filter. Also placing the notch filter exactly at f_{notch}, provides a higher ACR than the required value. Hence, it is placed at $\delta\omega$ giving a margin to improve the NF. The value of $\delta\omega$ is optimized using the simulation results.

Since both image rejection and notch filters are based on passive components, the performance of the circuit varies with component mismatches. Hence, to understand how accurate is the design, all the passive components values are increased or decreased by 20%, 10%, and 5%. From the simulation outputs, the accuracy of the system can be estimated (Appendix B). The circuit design could handle 5% of the variation, meaning when the passive components undergo a process variation of $\pm$ 5%, the outputs are within the specifications still (center frequency, ACR, and IRR). Capacitor and resistor banks are used to provide more accuracy. Each value in the bank is 5% higher or lower, thus with enough branches, a 20% accurate RC circuit can be designed.

4.7. ZIF/LIF re-configurable schematics: design parameters

The ZIF/LIF reconfigurable architecture is designed. The reconfigurability needs a few more design blocks. Analyzing the design parameters, both passive and active components need to be tuned. The passive components are made programmable to satisfy the bandwidth and filter-roll off. The passive components can be configurable by using programmable bank structures. The active components are also made programmable using parallel amplifiers structure. Each of the paths is turned on/off using control signals

4.8. Programmable gain and bandwidth

The programmable gain and bandwidth are achieved by tuning the passive components. A simple bank of the resistors and capacitors can be used to increase or decrease, its value. A parallel structure with switches and components is used (Figure.4.24).

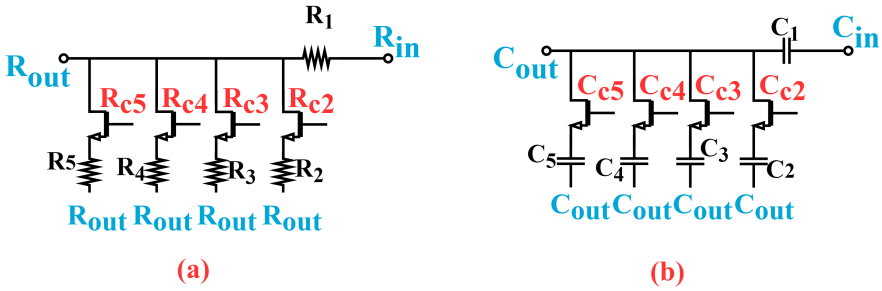

Figure 4.24: Resistor and Capacitor banks for tuning the gain and bandwidth.

The highest resistor value (R_1) is placed inline with input and output pins. The rest of required resistor values ($R_{req,n}$) are obtained through the parallel circuits ($R_{req,n} = R_1 \| R_2 .... R_n$). From the equations, the programmable resistors are used for gain variations. A similar structure is used for capacitance as well, however with the required capacitance addition for a nth configuration is, $C_{req,n} = C_1 + C_2 + ... C_n$. Capacitors are used for tuning the bandwidth of the receiver chain. NMOS-based switches are used in the RC banks. To reduce the voltage drop across the switch, a lower threshold devices (lvt-NMOS). Thus, it increases the output voltage ($VDD - V_{th}$) and the on-resistance of the switch. The control signals are given at the gate of the switch, thus switches the V_{gs} of the NMOS from the cut-off and linear region. The gain and bandwidth specification provide the range of resistor and capacitor value to be tuned. The step size of tuning is based on the analysis of process variation.

4.8.1. Passive Components : Process variation

Most of the resistors and capacitors in the design are programmable. Simulations are performed, varying the passive components value by ±20%, ±10%, and ±5% (Appendix B). The resistor and capacitor values are increased and decreased together for one set of simulations. For the other simulations, it is increasing and decreasing in opposite directions. To analyze the individual effects of R and C, and its combined effects on the gain, S11, and NF outputs. From the simulation results, it can be seen that the noise varies the least for increasing the resistor by 20% and decreasing the capacitor by 20%. Since, feedback resistors are used in most of the stages, increasing in R_F, decreases the NF (Equation.4.32). On similar grounds, a decrease in capacitor value decreases the noise bandwidth. The highest increase in NF is from decreasing the resistor and increasing the capacitor. For the input impedance matching, the increase in resistor decreases the S11 value. Since, it is already designed for optimum resistor values, to lower power consumption. In terms of gain transfer function outputs, the increase in resistor increases the gain curve, and the capacitor alters the bandwidth. However, the changes are within the specifications. Thus, the design passive components can handle 20% process variations. Thus, for programmability, the step size is 20% higher or lower.

4.8.2. Programmable gm stage

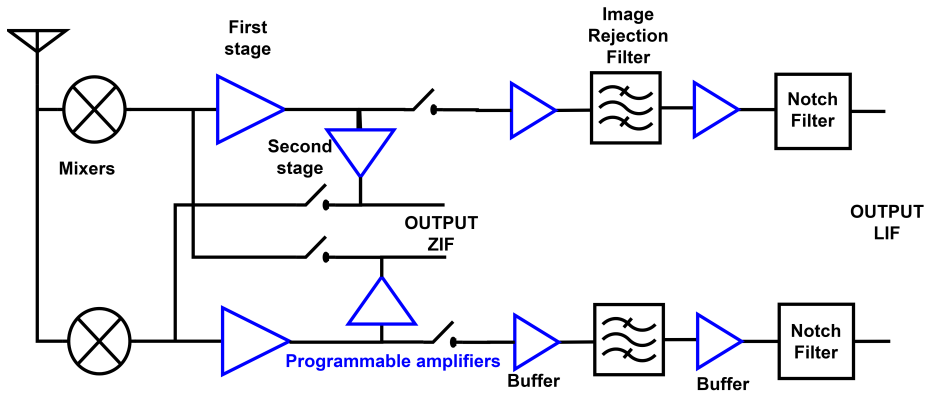

Figure 4.25: Programmable amplifiers in the receiver chain.

All the amplifiers used in the receiver chain are made programmable (Figure.4.25). The is also made programmable since it's an important block for the stability of the receiver (complex conjugate zero location). The existing amplifiers are added with PMOS and NMOS for controlling the amplifiers. The P_{SW} and N_{SW} are biased in linear region for switching purpose for both circuits (Figure.4.26(a),(b)). The control lines drive the gate of the device (PSW & NSW), turning the circuit ON/OFF. This way, a programmable gm stage is obtained. All the devices, except switches, are biased in saturation for higher gains. The P1,P3 are designed as hvt deceives, and body connected P3, P4 to help in biasing all the transistors in saturation.

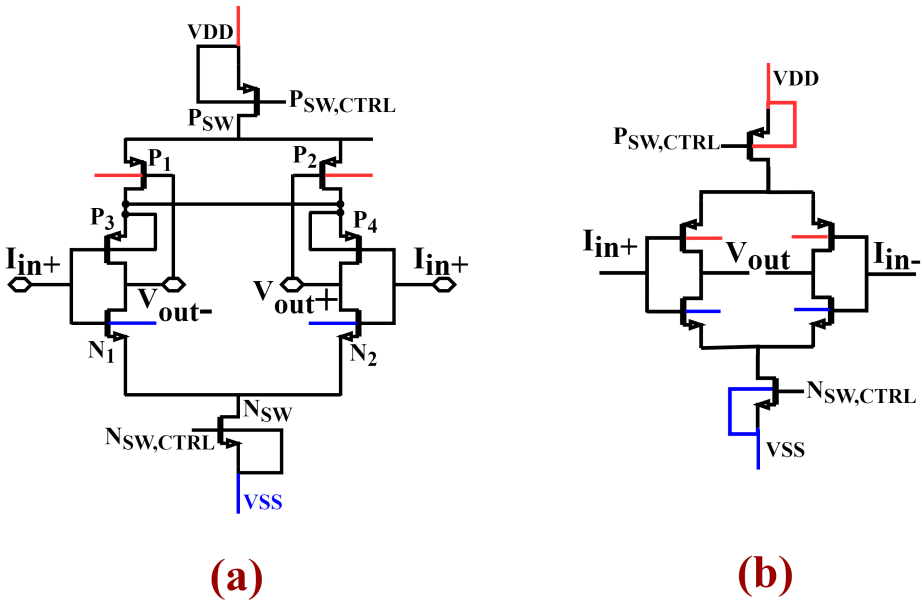

Figure 4.26: Programmable inverter design (a) Fully differential (b) Pseudo differential.

The buffers are only used for turn on/off programmability. However, the other feedforward TIA and feedback OTA employ multiple turn on/off amplifiers, to increase and decrease the gm. The individual inverter specification along with current consumption is tabulated below :s(Table.4.11,4.12,4.13).

	OTA - BB	**OTA - AA**	**OTA - CC**
gm_{tia}	800 μS	800 μS	2.4 μS
I_D	75 μA	75 μA	230 μA
$Power_{DC}$	0.36 mW	0.36 mW	1.1 mW
$pmos_{inv} W/L$	64 $\mu m/1\mu m$	64 $\mu m/1\mu m$	192 $\mu m/1\mu m$
$nmos_{inv} W/L$	16 $\mu m/1\mu m$	16 $\mu m/1\mu m$	48 $\mu m/1\mu m$
$nmos_{switch} W/L$	128 $\mu m/40nm$	128 $\mu m/40nm$	
$pmos_{switch} W/L$	128 $\mu m/40nm$	128 $\mu m/40nm$	
gm_{switch}	240 μS	240 μS	

Table 4.11: Programmable amplifiers for the feedback OTA.

4.8.3. Switches design: Transmission gate

Transmission gates are used for the reconfigurable architecture. During the ZIF operation, the first two stages are used as a 3^{rd} order filter and the output needs to

	TIA - AA	TIA - CC
gm_{cm}	640 μS	770 μS
gm_{inv}	1.52 mS	1.85 mS
I_D	88 μA	107 μA
$Power_{DC}$	0.42 mW	0.517 mW
$pmos_{cm} W/L$	40 $\mu m/1\mu m$	48 $\mu m/1\mu m$
$pmos_{inv} W/L$	320 $\mu m/1\mu m$	384 $\mu m/1\mu m$
$nmos_{inv} W/L$	80 $\mu m/1\mu m$	96 $\mu m/1\mu m$
$nmos_{switch} W/L$	128 $\mu m/40nm$	
$pmos_{switch} W/L$	128 $\mu m/40nm$	
gm_{switch}	270 μS	

Table 4.12: Programmable amplifiers for the feedforward TIA OTA.

be taken out of the chip. In LIF the output of the second stage has to be cross-feed to the first stage input. The output of the first stage is considered as the LIF output port. Thus there are two sets of switches required to support both the architecture. One at ZIF output switching and another at LIF output switching. The turn-on and turn-off of the switches are controlled by the input signals. A transmission gate switch with both PMOS and NMOS is used for the design to transfer the signals without any voltage drop. Also, using the transmission gate improves the linearity. since it can provide full swing output voltage, unlike NMOS or PMOS only switches. The r_{on} of the transmission gates are lower compared to individual devices. For switching activities, L = 40 nm is chosen for high-speed operation. The simulation output values (gain, S11, and noise), have a drop because of the r_{on} of the switch. The r_{on} is optimized, from simulation, to have 0.1% variation in the values. The width of the device is designed from these simulation results.

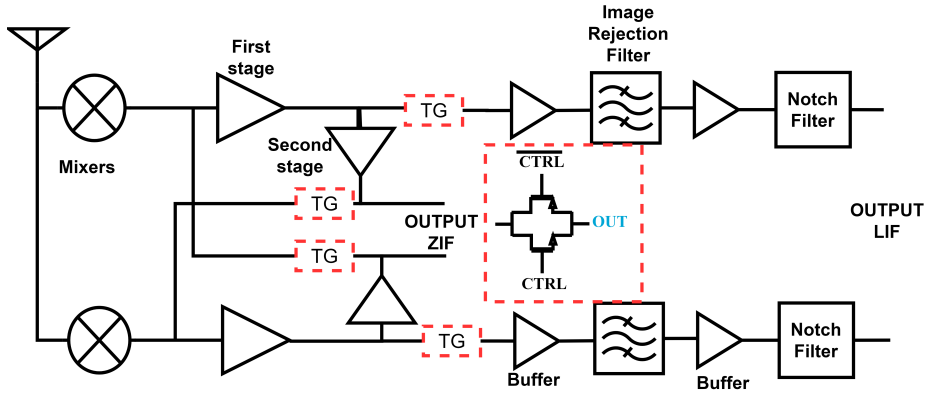

Figure 4.27: Transmission gate for ZIF/LIF Reconfigurability.

	SP - AA	SP - CC
gm_{cm}	384 μS	128 μS
gm_{tia}	900 μS	308.3 μS
I_D	53 μA	17 μA
$Power_{DC}$	0.25 mW	0.08 mW
$pmos_{cm} w/l$	24 $\mu m/1\mu m$	8 $\mu m/1\mu m$
$pmos_{inv} w/l$	192 $\mu m/1\mu m$	64 $\mu m/1\mu m$
$nmos_{inv} w/l$	48 $\mu m/1\mu m$	16 $\mu m/1\mu m$
$nmos_{switch} w/l$	128 $\mu m/40nm$	
$pmos_{switch} w/l$	128 $\mu m/40nm$	
gm_{switch}	167 $\mu m/40nm$	

Table 4.13: Programmable amplifiers for the Second stage OTA.

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5

Simulation result and Post Layout simulation result

The chapter shows the results of simulations for both the ZIF and LIF architecture for all gain configuration and wideband operation. It shows the performance of the receiver in terms of S11, noise, gain, linearity and power consumption. After the result plot and analyses the layout of the receiver chain is explained. It explains the layout of all the blocks of the RX chain. Next, the post layout simulation results are depicted. The design was implemented in TSMC 40 nm technology and is sent for fabrication.

5.1. Simulation: Design parameters

The design parameters for both the configuration was derived with theoretical equations in the previous chapter. The receiver circuit is implemented as schematics in the cadence platform. Spectre RF simulations are performed to calculate the gain transfer function, input impedance and noise of the receiver chain. The jist of design parameters used in the simulations for each individual block are presented below

Passive Mixers - The 8 NMOS switches are designed to provide the mixing operation. The parameters used for the switch is tabulated below. The power consumption denotes the power required to drive a capacitance of the same size of the mixer.

First Stage - It provides the necessary 2^{nd} order filtering for both the architectures. The passive components are programmable for different bandwidths 1,2,4 MHz. The gm stages are also made programmable for suppressing the noise in LIF mode. After constructing an entirely reconfigurable structure for LIF and ZIF mode, the bandwidth and Q-factor in ZIF mode were reduced. So, to compensate it, the values of the capacitors were increased and decreased depending on the equations given in Section.4.2.1. The C_1 in increased from 17 pF to 20 pF, C_2 is decreased from 3

Passive Mixers	
$W_{mx,nmos}$	24 μm
$L_{mx,nmos}$	1 μ m
r_{on}	17 Ω
$Power_{dc}$	0.25 mW

Table 5.1: Passive Mixer design parameters.

pF to 1 pF. With these modifications, the desired bandwidth and ACR was obtained. The DC power consumption of LIF mode is 0.5 mW higher, however this is balanced in the second stage configurations.

First stage - 2nd Order TIA with active filtering		
	ZIF - 4 MHz	**LIF - 2 MHz**
C_3	15 pF	40 pF
C_1	20 pF	16 pF
R_F	5 $K\Omega$	5 $K\Omega$
gm_{TIA}	3.04 mS	6 mS
$Power_{dc}$	1.88 mW	2.4 mW
C_{IN}	100 pF	
R_2	10 $K\Omega$	
gm_{OTA}	6.4 mS	
C_2	1 pF	

Table 5.2: The first stage design parameters.

Second stage/Complex feedback stage : It operates as a simple LPF in ZIF mode, but is used as complex feedback in LIF mode. The value of $C_{F,SP}$ was also increased to compensate the same effect, from 10 to 12 pF. The power loss between ZIF and LIF is almost balanced from the second stage value.

Second stage - 1st Order single pole filter		
	ZIF - 4 MHz	**LIF - 2 MHz**
$C_{F,SP}$	12 pF	1 pF
$R_{F,SP}$	7.7 $K\Omega$	5 $K\Omega$
$R_{S,SP}$	5 $K\Omega$	2 $K\Omega$
gm_{SP}	3.6 mS	616 μ S
$Power_{dc}$	0.33 mW	0.08 mW

Table 5.3: The second stage design parameters.

Buffer stage : They are added to provide the impedance isolation and support LIF gain programmability. From the noise summary results, the noise from the low gm of buffer2 degrades the NF value more than estimated. This might be due to neglecting the loading effect and finite gm effect of buffers. Thus to lower the NF value, the gm of buffer2 is increased to 2.4 mS.

The image rejection and notch filter The image rejection and notch are pro-

Buffer design parameters		
	ZIF - 4 MHz	**LIF - 2 MHz**
$R_{F,BUFR1}$	5 $K\Omega$	5 $K\Omega$
$R_{F,BUFR2}$	5 $K\Omega$	5 $K\Omega$
gm_{BUFR1}	4 mS	
gm_{BUFR2}	2.4 mS	
$Power_{dc}$	0.81 mW	

Table 5.4: The first and second buffer design parameters.

grammable bank of RC and CR combinations. It provides the required image rejection and the ACR/NACR ratio. Though causes signal attenuation, the losses are compensated by the buffers gain.

Image rejection and notch filter		
	ZIF - 4 MHz	**LIF - 2 MHz**
C_{PPF}	18 pF	
C_{NOTCH}	18 pF	
R_{NOTCH}	1.7 $K\Omega$	
R_{PPF1}	3.5 $K\Omega$	
R_{PPF2}	6 $K\Omega$	
R_{PPF2}	12 $K\Omega$	

Table 5.5: The polyphase image rejection design parameters.

5.2. ZIF mode: 4 MHz BW

The ZIF mode is made to operate over a gain programmability of 24 to 44 dB gain. The gain and bandwidth programmability for different values are given in the Table.5.9

5.2.1. Input impedance matching

The input impedance improves as the gain drops, since the matching is mainly from the BB resistors. For higher gain, the resistors value increases, and the input matching decreases. The matching varies from *-20.47* dB for the minimum gain mode to *-11.61* dB for maximum gain. Plot.5.1, depicts the matching for different gain configurations.

Zero IF - 4 MHz									
Mode	1	2	3	4	5	6	7	8	9
C_{in}	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF
R_F	5 $K\Omega$	7.5 $K\Omega$	5 $K\Omega$	7.5 $K\Omega$	10 $K\Omega$	10 $K\Omega$	15 $K\Omega$	15 $K\Omega$	15 $K\Omega$
C_1	20 pF	20 pF	20 pF	20 pF	20 pF	20 pF	20 pF	20 pF	20 pF
C_2	1 pF	1 pF	1 pF	1 pF	1 pF	1 pF	1 pF	1 pF	1 pF
C_3	30 pF	24 pF	27 pF	21 pF	21 pF	18 pF	18 pF	15 pF	15 pF
R_2	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$
$C_{F,SP}$	12 pF	12 pF	8 pF	8 pF	6 pF	4 pF	4 pF	4 pF	2 pF
$R_{F,SP}$	5 $K\Omega$	5 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	15 $K\Omega$	15 $K\Omega$	20 $K\Omega$	25 $K\Omega$
$R_{S,SP}$	5 $K\Omega$	5 $K\Omega$	5 $K\Omega$	5 $K\Omega$	5 $K\Omega$	5 $K\Omega$	5 $K\Omega$	5$K\Omega$	5$K\Omega$
NF (at 1 MHz) (dB)	7.5	6.4	6.8	5.8	5.4	5.3	4.9	4.9	4.8
S11 (dB)	-20.4	-16.28	-20.16	-16.3	-14	-14	-11.4	-11.5	-11.6
Gain (dB)	23.8	26.2	30.8	32	34	37.5	39	41	44
ACR (dB)	18.1	18.3	18.9	18	18	17	18	15	16

Table 5.6: ZIF architecture - Different gain configuration.

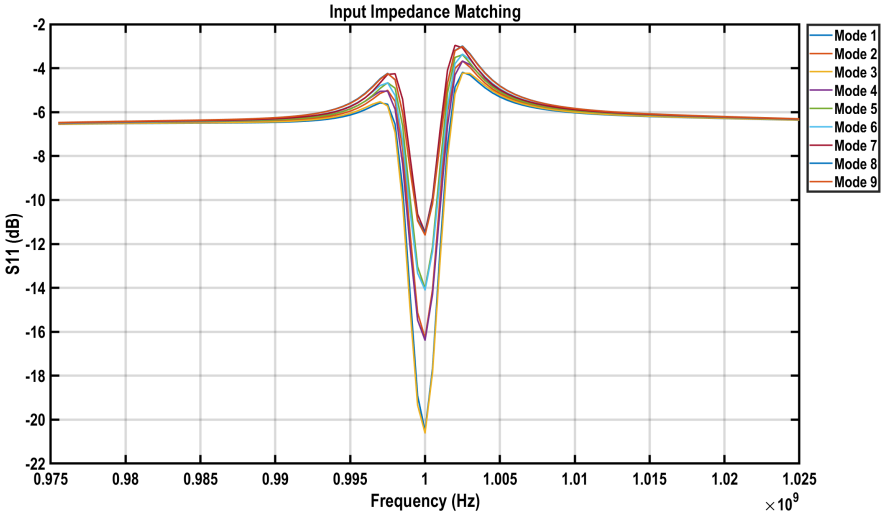

Figure 5.1: Input impedance matching - ZIF architecture.

The wideband operation is possible by tuning the center frequency of the passive mixer. For 802.11ah standard, the frequency of operation is from 863-930 MHz. The output plot for wideband matching is given in Figure.5.2.

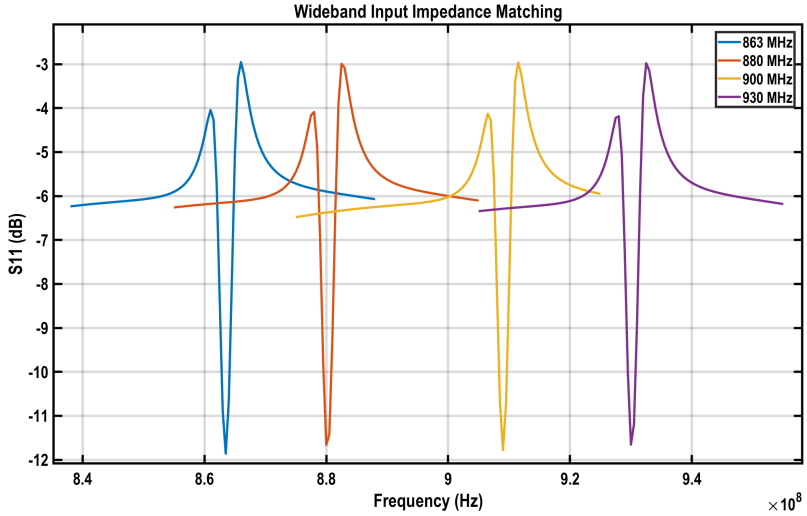

Figure 5.2: wideband (930 MHz - 863 MHz) Input impedance matching - ZIF architecture.

5.2.2. Gain transfer function

The required gain specification is implemented by tuning the resistors and the capacitors to maintain the bandwidth and ACR/NACR ratios. As the R_F value increases, the zero location also improves. The output plot.5.3 depicts the different gain configuration. The similar wideband gain transfer function output is depicted in plot.5.4.

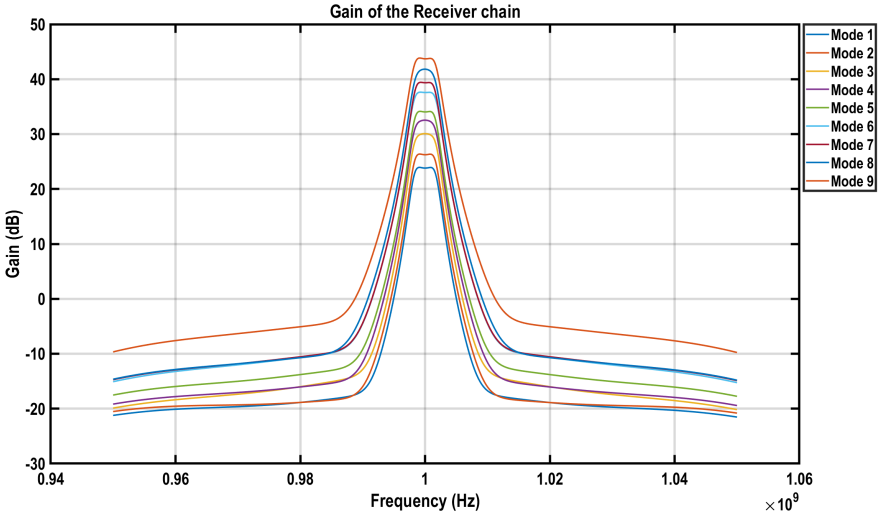

Figure 5.3: Gain transfer function - ZIF architecture.

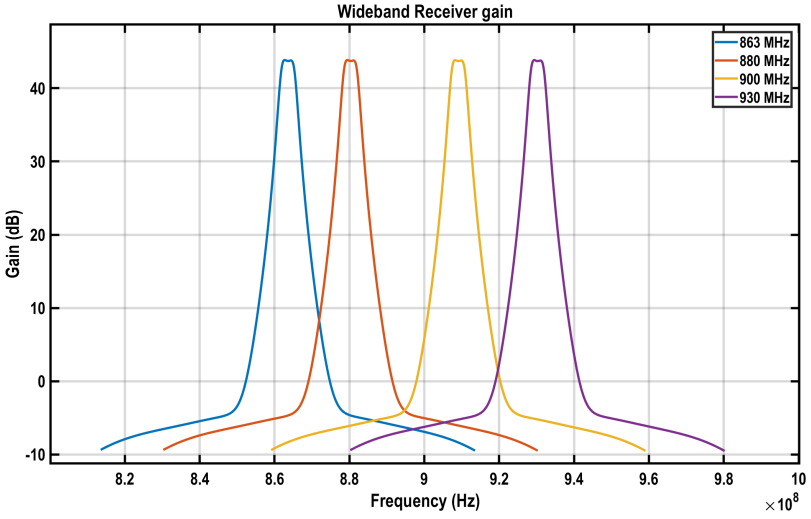

Figure 5.4: wideband (930 MHz - 863 MHz) Gain transfer function - ZIF architecture.

5.2.3. Noise performance

The NF value is affected by many parameters. First, from the low frequency noise or the flicker noise. Clearly from the output plot.5.5, the steep increase below 500 kHz is from flicker noise effect. The other effect towards high frequencies is from the in-band noise shaping provided by the feedback OTA gm. At the center frequency,

the noise varies from *4.9* dB for higher gain configuration to *7.6* dB for minimum gain configuration. The noise remains fairly consent over the wideband operation of ZIF (plot.5.6).

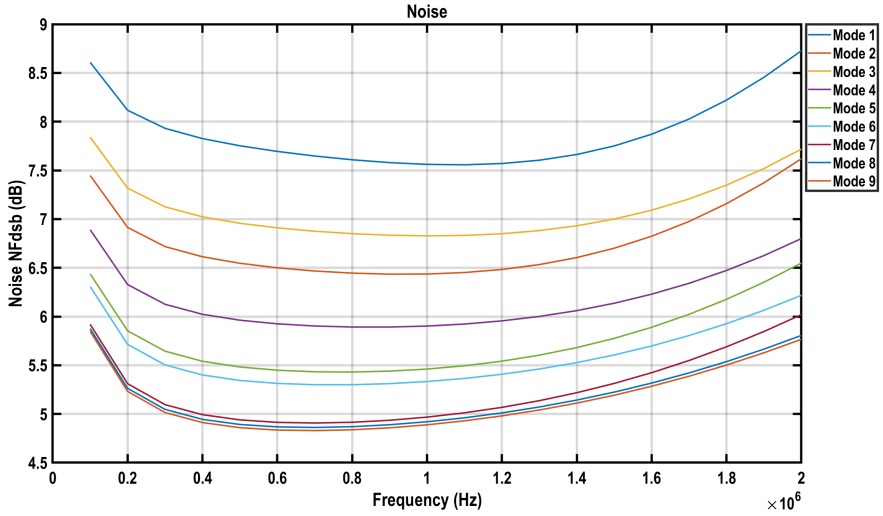

Figure 5.5: Noise transfer function - ZIF architecture.

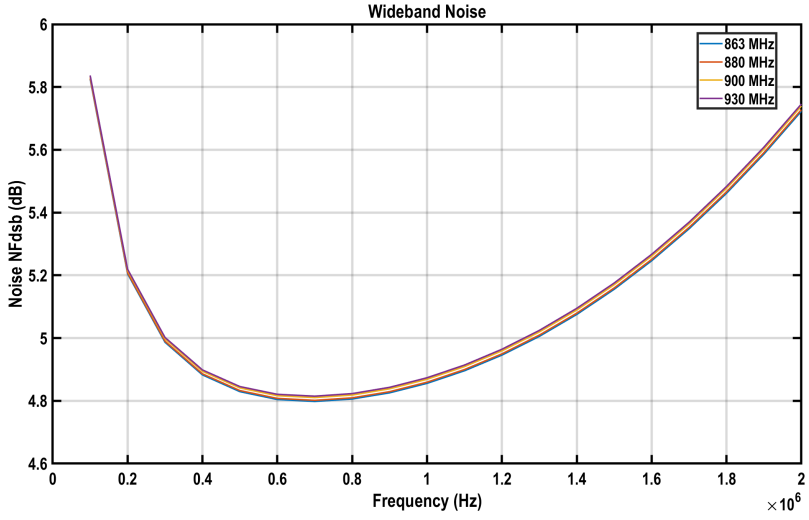

Figure 5.6: wideband (930 MHz - 863 MHz) Noise transfer function - ZIF architecture.

5.2.4. Linearity: Single tone and Two tone test results

The linearity parameters discussed in Section.1.3.6 are calculated from single and two tone test.

In a **single tone test**, a single input with amplitude *A* at a particular frequency is fed as input. A periodic steady state analysis (pss) simulation is performed to calculate the output signal level at the output. The difference is given as the gain or receiver. Now, the *A* is increased until the gain of the receiver drops by 1 dB. This is termed as the P1dB compression point.

For two tone a similar set-up is repeated, however, the frequencies are chosen such that the intermodulation products fall inside the desired band. Thus the drop in the signal level can be mapped to the Equation.1.5, to find the IIP3.

The simulation result of such a point is presented in the plot.5.11. From the graphs, the 1 dB drop between the signal power and slope 1 gives the P1dB to be -18 dBm. The intersection point for slope 3 and slope 1 gives the IIP3 point as -9 dBm.

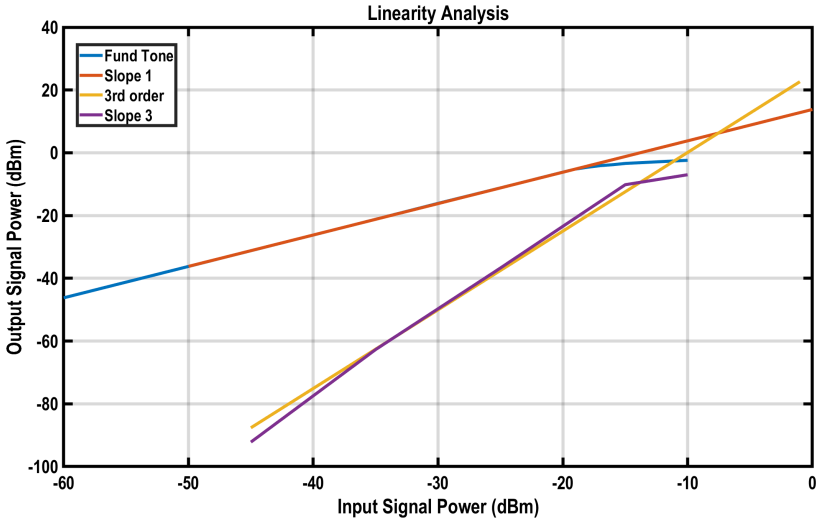

Figure 5.7: P1dB and IIP3 slope form representation.

5.2.5. Overall power consumption

The thesis was designed with an aim for lowering the power consumption. The total power consumption for ZIF mode from the two stages sum to 2.3 mW.

The power consumption from the mixer is 0.25mW (Section.4.3.1). Estimating, 1 mW power consumption for the clock. The total power consumption of the ZIF architecture is **3.5 mW**.

Component	Power Consumption
gm_{OTA}	1.46 mW
gm_{TIA}	0.517 mW
gm_{SP}	0.33 mW

Table 5.7: Individual power consumption for the amplifiers implemented.

5.3. LIF mode: 1,2 MHz BW

The LIF uses feedback buffer resistors for gain programmability. The different configurations for the gain programmability for 2 MHz is given in the Table.

Low IF - 2 MHz					
Mode	1	2	3	4	5
C_{in}	100 pF	100 pF	100 pF	100 pF	100 pF
R_F	5 $K\Omega$	7.5 $K\Omega$	5 $K\Omega$	7.5 $K\Omega$	10 $K\Omega$
C_1	16 pF	16 pF	16 pF	16 pF	16 pF
C_2	1 pF	1 pF	1 pF	1 pF	1 pF
C_3	40 pF	40 pF	40 pF	40 pF	40 pF
R_2	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$
$C_{F,SP}$	1 pF	1 pF	1 pF	1 pF	1 pF
$R_{F,SP}$	5 $K\Omega$	5 $K\Omega$	10 $K\Omega$	10 $K\Omega$	10 $K\Omega$
$R_{F,BUFR1}$	5 $K\Omega$	6 $K\Omega$	6 $K\Omega$	7 $K\Omega$	7 $K\Omega$
$R_{F,BUFR2}$	5 $K\Omega$	5 $K\Omega$	6.5 $K\Omega$	8 $K\Omega$	9.5 $K\Omega$
$R_{S,SP}$	2 $K\Omega$	2 $K\Omega$	2 $K\Omega$	2 $K\Omega$	2 $K\Omega$
NF (at 1 MHz) (dB)	7.5	7.1	6.9	6.7	6.6
S11 (dB)	-11.03	-10.7	-10.32	-10.1	-9.7
Gain (dB)	30.41	32.5	34	37.2	41.9 44
IRR (dB)	38	38	38	38	38

Table 5.8: LIF architecture - Different gain configuration.

5.3.1. Input impedance matching

The input impedance matching for LIF is limited because of the complex feedback. The s11 is maintained around -10 dB throughout different gain configurations (Plot.5.8).

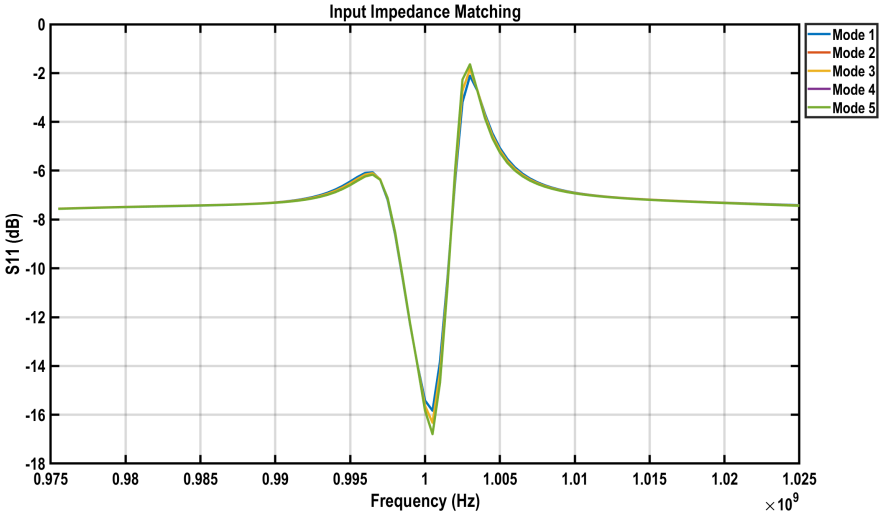

Figure 5.8: Input impedance matching - LIF architecture.

5.3.2. Noise performance

The NF for LIF architecture suffers from similar flicker and bandpass noise shaping. Another critical block to contribute is the complex feedback amplifier (gm $\approx$ 600 μ S). The noise is maintained within the desired specification by properly designing the blocks concerning noise contributions. The effect of small gm is still visible from the noise summary, but overall the NF is less then *7 dB* for higher gain mode (Plot.5.9).

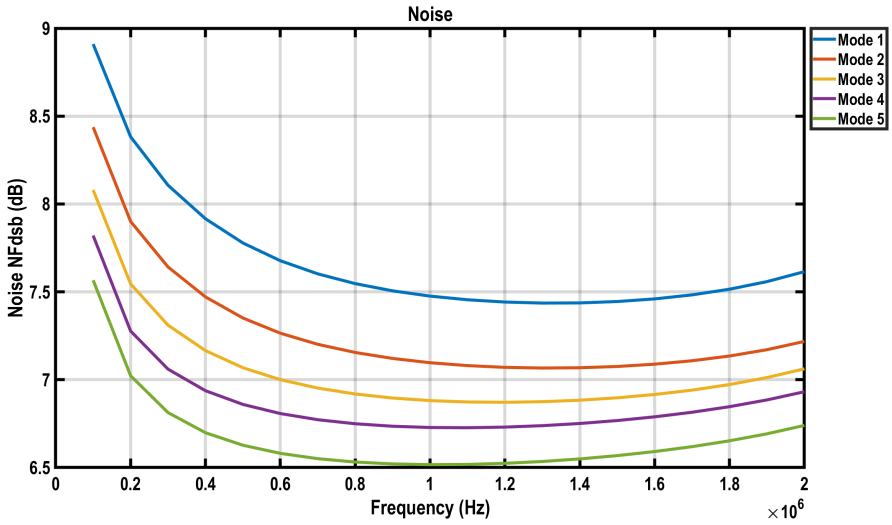

Figure 5.9: Noise analysis - LIF architecture.

5.3.3. Gain transfer function

The increase in gain is possible by tuning the buffer resistors. These act like a cascaded structure and improve the gain. The gain configuration for different modes are given below (Plot.5.10).

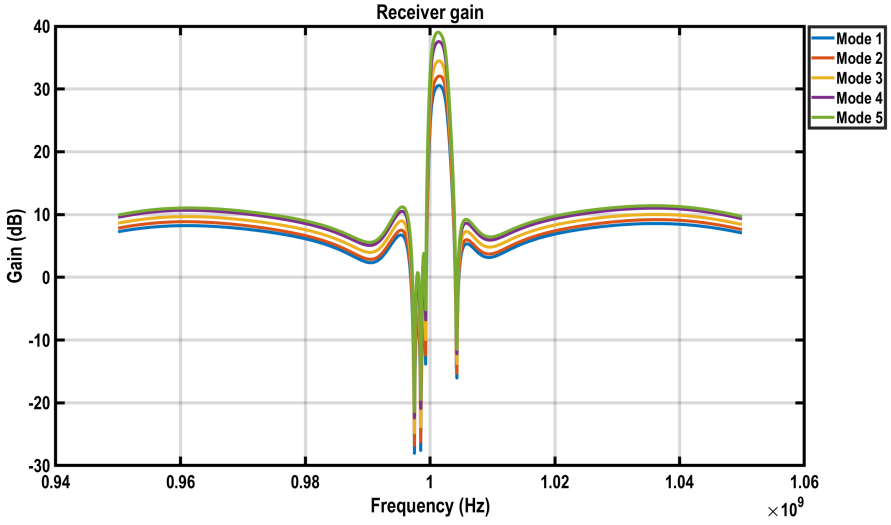

Figure 5.10: Gain transfer function - LIF architecture.

5.3.4. Linearity: Single tone and Two tone test results

The similar simulations are carried out for LIF architecture 5.11. From the graphs, the 1 dB drop between the signal power and slope 1 gives the P1dB to be -26 dBm. The intersection point for the slope 3 and slope 1 gives the IIP3 point as -17 dBm.

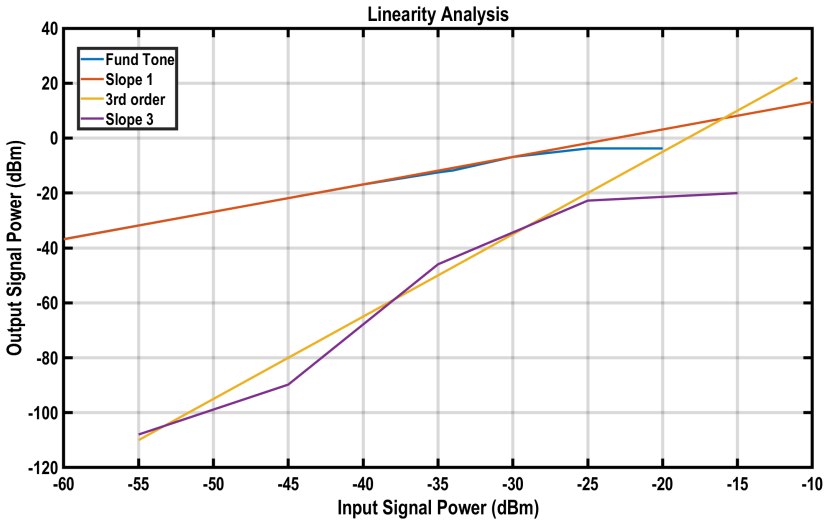

Figure 5.11: P1dB and IIP3 slope form representation.

5.3.5. Overall power consumption

The overall power consumption is higher than the ZIF architecture, since two additional buffers are designed for impedance isolation and gain programmability. The power consumption from BB sums to 2.867 mW.

Accounting for the buffer for mixer and the clock, the total power consumption is **4.1 mW**.

5.3.6. 1 MHz Bandwidth mode

Following similar design procedures, the 1 MHz bandwidth was also designed (Appendix B).

Low IF - 2 MHz			
C_{in}	100 pF	R_F	5 $K\Omega$
C_1	50 pF	R_2	10 $K\Omega$
C_2	1 pF	$R_{F,SP}$	5 $K\Omega$
C_3	80 pF	$R_{F,BUFR1}$	5 $K\Omega$
$C_{F,SP}$	1 pF	$R_{F,BUFR2}$	5 $K\Omega$
C_{PPF1}	40 pF	$R_{S,SP}$	2 $K\Omega$
C_{PPF2}	80 pF	R_{PPF}	6 $K\Omega$
C_{PPF3}	100 pF		
C_{NOTCH}	40 pF		

Table 5.9: LIF architecture - Different gain configuration.

However, it requires huge capacitors to satisfy the narrow bandwidth filtering and image rejection. The total capacitance required is around 2 nF (1.96 nF). So the 1 MHz was only designed and verified using simulations. The passive components required more area, thus the layout was done only for 2 MHz, which required comparatively smaller capacitance (516 pF).

5.4. Layout

The layout for the designed architecture was implemented on 40 nm technology with six thin and two thick metal layers. The layout of individual blocks like mixers, OTA, and TIA, are discussed. Further, an extra test-buffer is implemented at the output port to provide an impedance match at the output, for not affecting the performance of the chip.

5.4.1. Mixers

The mixers are in the input RF block of the chip. They are NMOS switches with clock lines at the gate terminal. The clock lines for input also needs to run through a symmetric path, to avoid delays. The dimension of NMOS is L = 40 nm, W = 24 μm. Two types of structures were implemented to understand the design trade-off between nr (number of fingers) and finger width. Type 1: nr = 24 and finger width is 1 μm, Type 2: nr = 12 and width is 2 μm. Increasing the number of fingers adds to series resistance and can cause poor noise. Increasing the per finger width increases the parasitics. From the noise simulation output from the pex file, the strutted with more number of fingers is preferred. The individual NMOS are bulk combined to form the two sets of mixer units. These are placed 110 μm apart, for mapping the RF input to the source of the NMOS. The clocks of individual sets are combined to form the BB input.

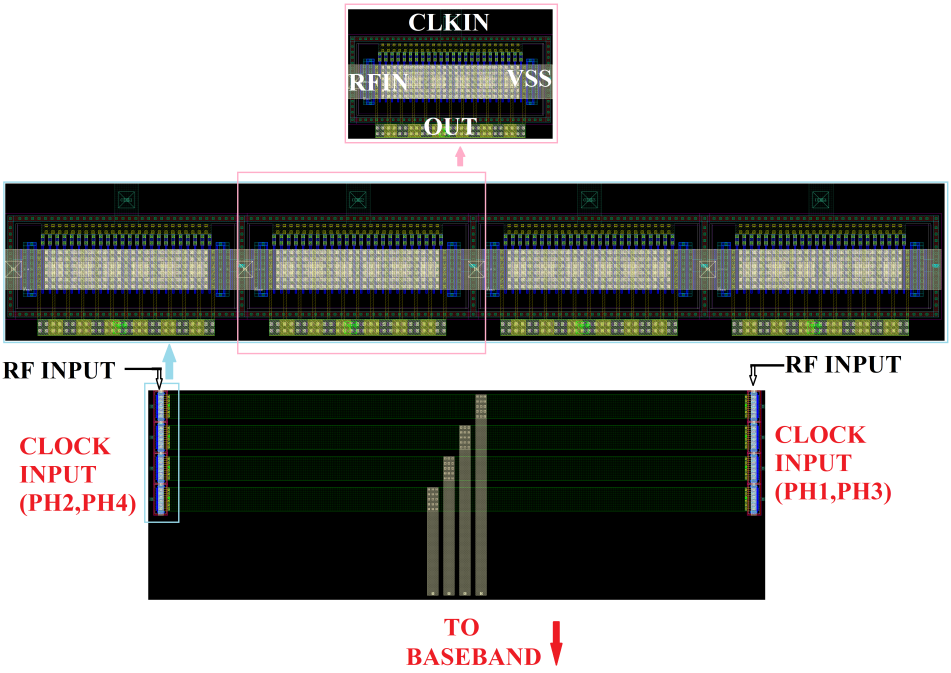

Figure 5.12: Mixer layout - The differential version to the nmos cell inside.

5.4.2. Programmable inverter design

For the amplifiers, a single unit cell is implemented. This unit cell is repeated to the required number of W/L ratios. Analysing the amplifiers sizes from simulation ((Table.4.11,4.12,4.13)), the minimum cell of dimension, number of fingers as 8 and the finger width as 1 μm, is considered. The schematics and layout comparison of the individual amplifier is depicted in the Figure.5.13,5.14 The deceives are implemented with the shared drain and source concept. This unit cell is used for other amplifiers in the receiver chain.

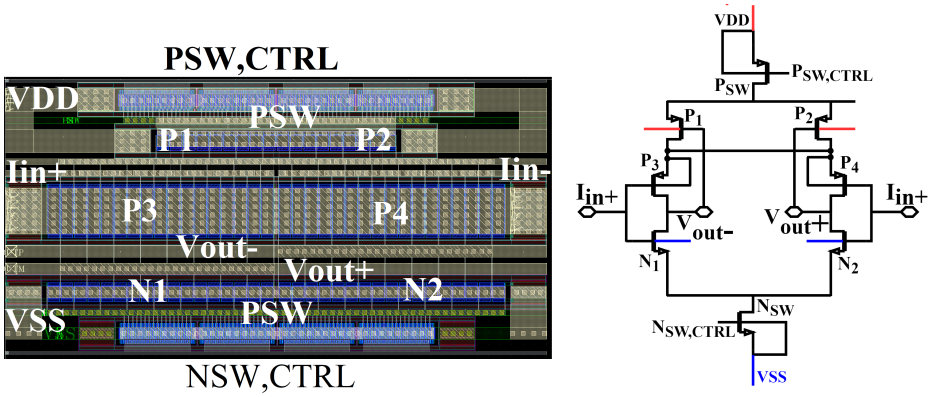

Figure 5.13: Layout and schematics for differential inverter design.

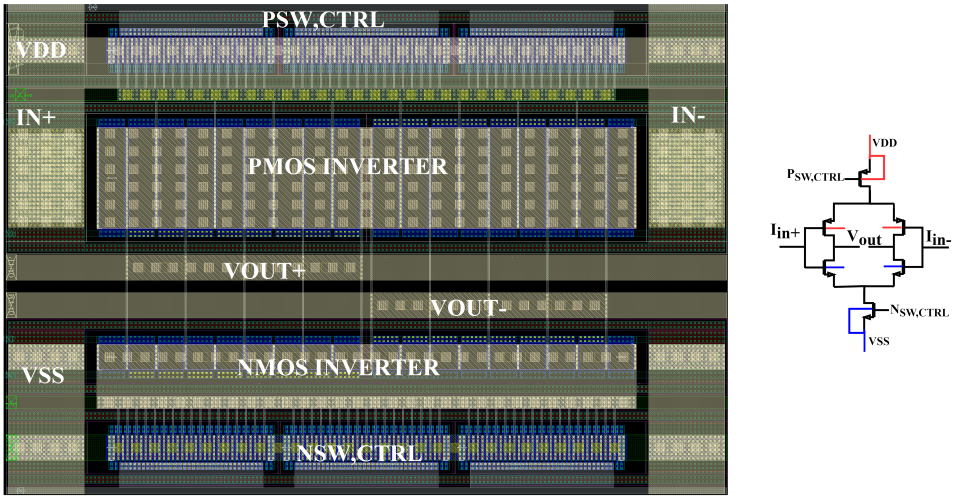

Figure 5.14: Layout and schematics for pseudo inverter design.

5.4.3. First stage layout

The input lines from mixer pass through the C_{IN} and C_1 to the feedfoward TIA and feedback OTA. The connection lines are made sure to be the thick metal layers, to reduce series resistance. The first stage is used as the filter. The layout of the design is depicted in the Figure.5.15.

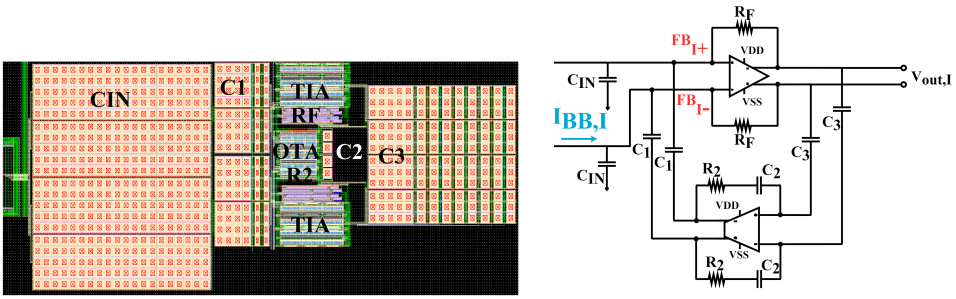

Figure 5.15: The implementation of the 2^{nd} order low pass filter.

5.4.4. Second stage layout

The second stage performs as the low pass filter and also need to provide the complex feedback. Thus the placement of the design is important. Since, it has to provide a cross-connection path, the I and Q signals should be properly guarded to reduce the cross-talk effect. The second stage design and the implementation is shown in the figure

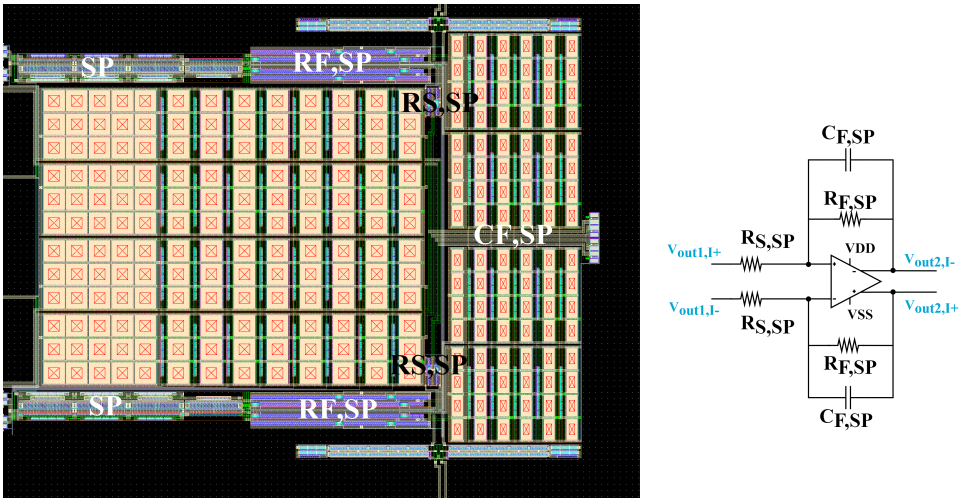

Figure 5.16: The second stage design and schematics.

5.4.5. Polyphase image reject filter

The buffers along with the filter design is shown in the figure.5.18. The notch filter had to be removed and transformed to PCB design due to area constrain.

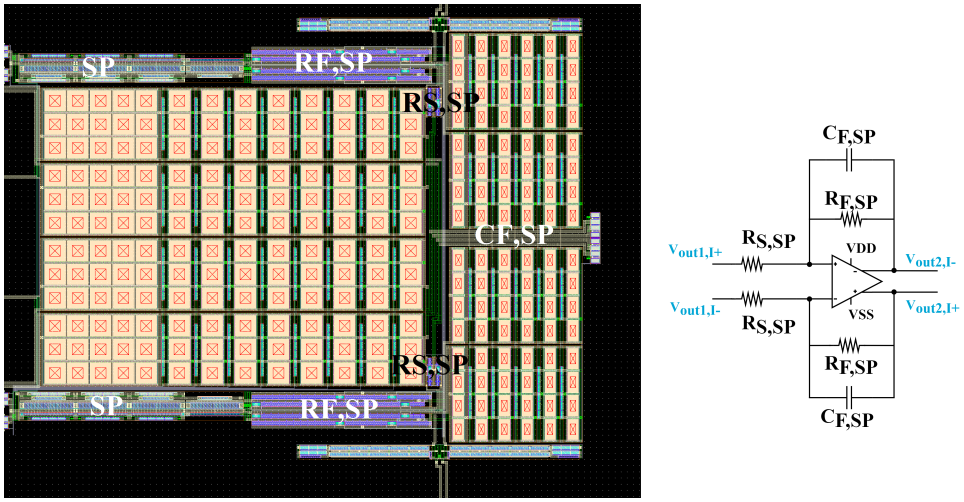

Figure 5.17: Buffers and Image rejection filter implementation.

Finally, the layout of the entire chip is shown in Figure.5.18.

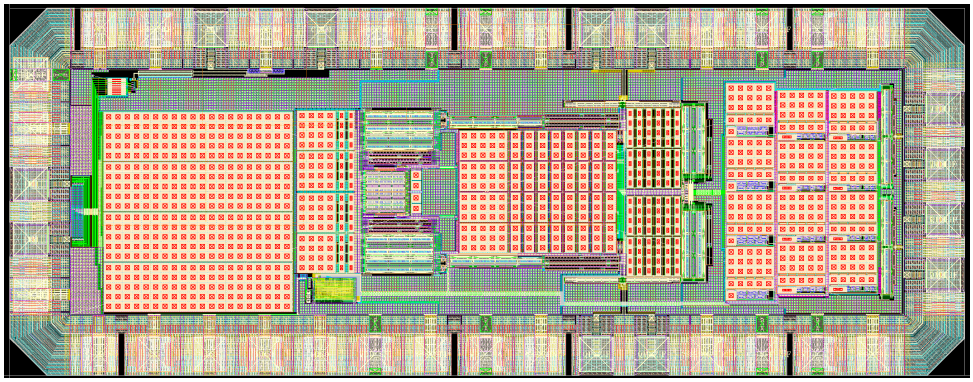

Figure 5.18: Full Chip.

5.5. Post-layout simulation results

After the layout has been completed. A design check rule (DRC) is applied to check for design constrains. These ensure safe performance of the chip. Then a layout vs. schematics is performed to check for any discrepancies. Further after clearance, a pex simulation to extract all relevant design along with their RC parasitics are generated. A spectre RF simulation is run with the calibre view to generate the post-layout simulations. Running a spectre RF for such narrow bandwidth usually takes days to complete. Thus, the high gain mode for both architecture are evaluated.

5.6. ZIF mode: 4 MHz BW

The results for the post layout simulation compared against the schematics are shown below,

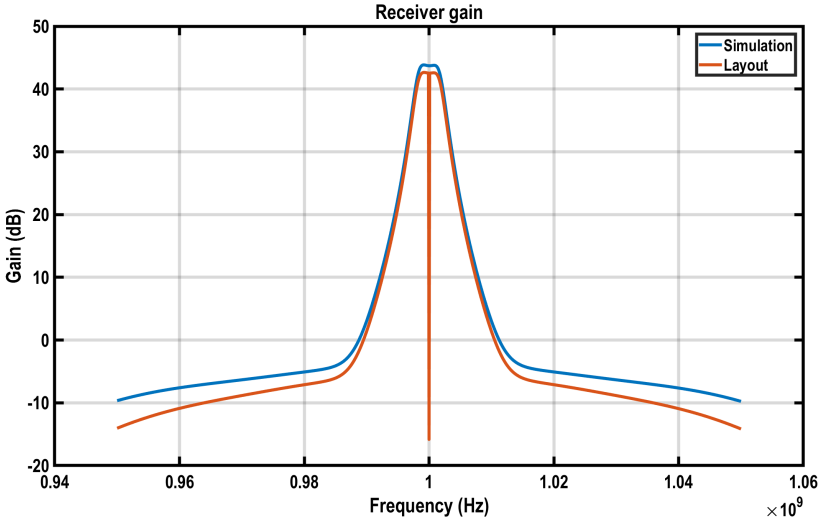

Figure 5.19: Layout vs schematics - Gain transfer function.

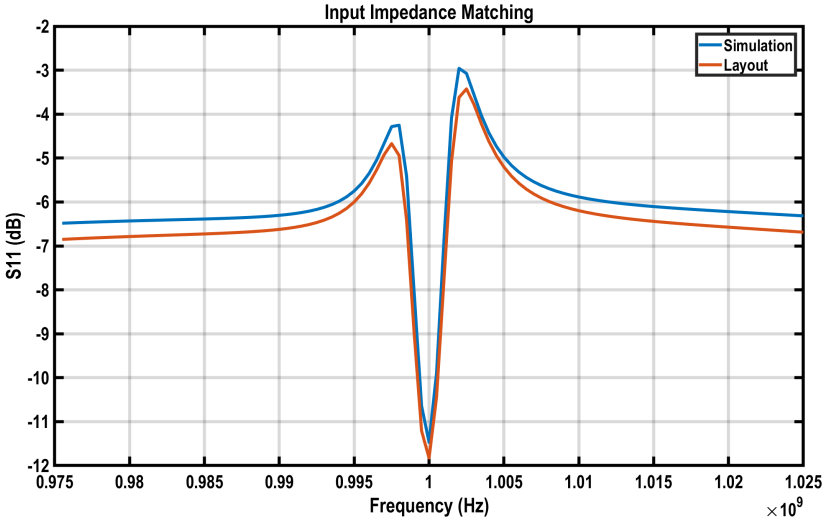

Figure 5.20: Layout vs schematics - Input impedance.

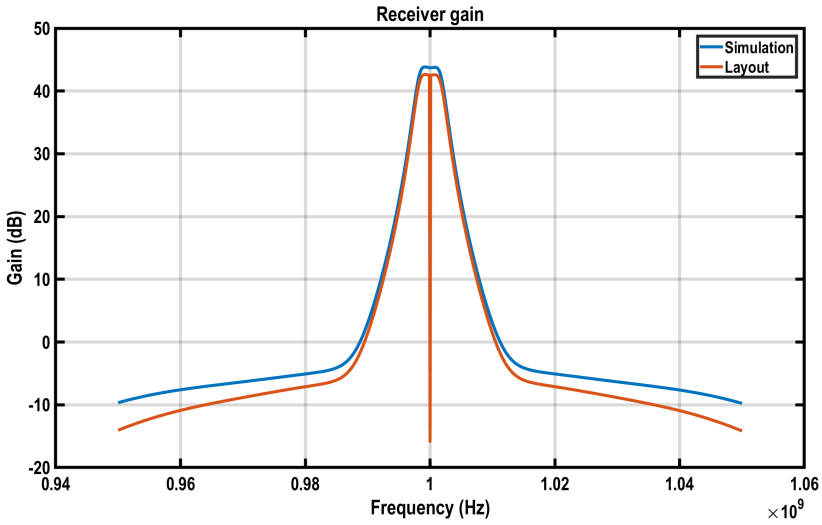

Figure 5.21: Layout vs schematics - noise transfer function.

5.7. LIF mode: 2 MHz BW

The results for the post layout simulation compared against the schematics are shown below,

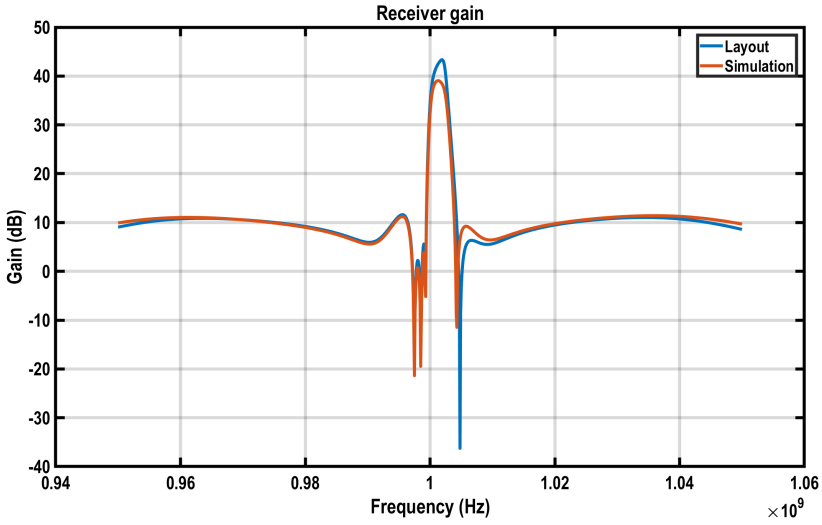

Figure 5.22: Layout vs schematics - Gain transfer function.

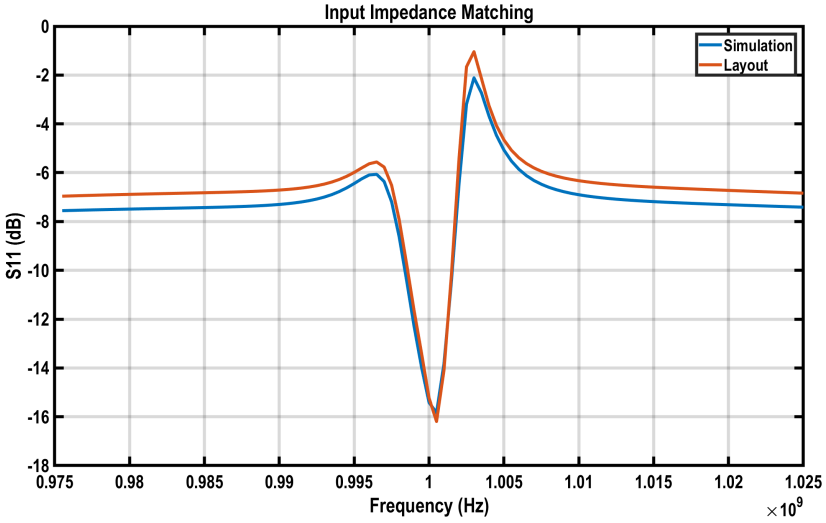

Figure 5.23: Layout vs schematics - Input impedance.

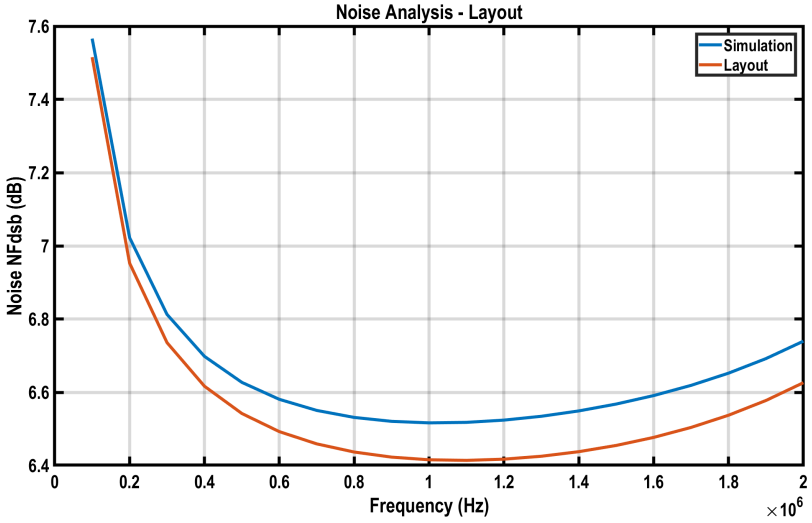

Figure 5.24: Layout vs schematics - noise transfer function.

The results show that the receiver implemented works within the desired specifications. The receiver provides the NF between 4.8 dB for low gain ZIF to 7.5 dB high gain ZIF configuration with an overall power consumption less then 4 mW. It also provides the necessary gain and bandwidth programmability with resistors and capacitors. The image rejection filter provides an IRR of 38 dB and the notch filter

provides a ACR/NACR of 17dB/32dB with 20% accuracy.

Targeted Specification	Implemented design output	
Frequency Band	863-903 MHz	863-930 MHz
Gain	24-44 dB	24-44 dB for ZIF mode, 28-40 dB for LIF
Bandwidth	1,2,4 MHz	2,4 MHz
Filter	3rd Order	3rd order filter for ZIF mode; reduced order of LIF improved using notch filter.
NF	6 dB	4.8 - 7.6 dB in the center frequency
Power	4 mW	4.1 mW for LIF mode (ZIF operates at lower power)
1dB	-30 dBm	-18 dBm for ZIF and -26 dBm for ZIF ,
IIP3	-48 dBm	-9 dBm for ZIF and -17 dBm for LIF

Table 5.10: The targeted vs. obtained results from the implementation.

6

Conclusion

The work presents a low power mixer-first receiver design for 802.11ah standard. The work uses a reconfigurable ZIF/LIF architecture. The receiver provides a ACR/NACR of 18 dB/30 dB for both ZIF and LIF architecture by 3^{rd} order filter roll-off and notch filter respectively. The receiver works below 4 mW for ZIF configuration and about 4.1 mW for LIF mode. It also provides a 24 - 44dB gain programmability. The receiver provides a -20 dB input impedance match for the minimum ZIF gain mode. It provides less than 5 dB NF for the high gain ZIF mode. The work also explains a system level design of the receiver through MATLAB models and theoretical equations (chapter 1). It provides the receiver requirements - gain, noise, linearity, filtering order and IRR. In order to satisfy the standard data structure, a reconfigurable, LIF for narrow-bandwidths (1/2 MHz) and ZIF for 4 MHz bandwidth is implemented. The receiver design uses a differential mixer-first receiver design architecture explained in chapter 3. The baseband of the receiver is a 3^{rd} order LPF with two stages in case of ZIF mode or a low pass to bandpass transformed filter for LIF mode. The LIF mode also consists of image rejection filter and notch filter to improve the ACR/NACR requirements. The receiver uses transmission gates for providing the necessary reconfigurability. It also consists of buffers placed in series with the passive filters in LIF mode. These provide the necessary impedance isolation and gain programmability for the LIF mode.
A simple inverter based differential amplifier is used for providing the necessary transimpedance gain in the BB. The inverter is self-biased, by placing a resistor between the input and output path. chapter 4 explains, the effect of finite transconductance value and the necessary equations for designing the receiver. Both the LIF and ZIF receiver design is presented based on the derived equations ans simulation results from the cadence platform. The simulation results and layout figures are depicted in chapter 5.

A

802.11ah/HaLow standard

A.1. Frequency of operation across different countries

Country	Frequency (MHz)
Australia	915-928
China	775-779, 779-787
Europe	863-868.6
Japan	915.9-929.7, 920.5-923.5
New Zealand	915-928
Singapore	866-869, 920-925
South Korea	917-923.5
United States	902-928

B

RX Design

B.1. The Input Impedance Z_{IN}

The ideal LO clock is represented as a period function with respect to its turn-on and turn-off period,

$$S_{I+}(t) = \begin{cases} 1, & kT_{\mathrm{LO}} \le t \le \left(k+\frac{1}{4}\right)T_{\mathrm{LO}}, \quad k\epsilon\mathcal{Z} \\ 0, & \left(k+\frac{1}{4}\right)T_{\mathrm{LO}} < t < (k+1)T_{\mathrm{LO}}, \quad k\epsilon\mathcal{Z} \end{cases} \tag{B.1}$$

Where, k denotes the number of LO clock period for a single path. Simplifying the equation.B.1 with Fourier series [1],

$$\begin{aligned} S_{I+}(t) &= \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_{LO}t} \\ a_k &= \frac{1}{4}\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4} \\ S_{I+}(t) &= \sum_{k=-\infty}^{\infty} \frac{1}{4}\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4}e^{jk\omega_{LO}t} \end{aligned} \tag{B.2}$$

Where, n denotes the number of paths in the passive mixer. Similarly for other paths,

$$\begin{aligned} S_{I-}(t) &= S_{I+}\left(t-\frac{T_{LO}}{2}\right) = \textstyle\sum_{k=-\infty}^{\infty}(-1)^k\frac{1}{4}\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4}e^{jk\omega_{LO}t} \\ S_{Q+}(t) &= S_{I+}\left(t-\frac{T_{LO}}{4}\right) = \textstyle\sum_{k=-\infty}^{\infty}\frac{1}{4}\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4}e^{jk\omega_{LO}t}e^{-jn\frac{\pi}{2}} \\ S_{Q-}(t) &= S_{I+}\left(t-\frac{3T_{LO}}{4}\right) = \textstyle\sum_{k=-\infty}^{\infty}\frac{1}{4}\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4}e^{jk\omega_{LO}t}e^{jn\frac{\pi}{2}} \end{aligned} \tag{B.3}$$

Considering a single path, I_+, the baseband current is written as, $i_{BB,I+}(t) = S_{I+}(t)\times i_{RF}(t)$. The i_{RF} is considered as the input RF current. The baseband current

B

($i_{BB,I+}$) flows through the load impedance ($Z_{BB,I+}$), creating a voltage $v_{BB,I+}(t) = [S_{I+}(t) \times i_{RF}(t)] * z_{BB,I+}(t)$, where * denotes convolution [2]. It can be seen from the Fig.3.3 that, all the load impedance are same value, so a single variable z_{BB} is used in the derivation. Looking at the RF side, the voltage drop can be calculated by summing, the V_{BB} for all paths and the voltage drop across the switch due to r_{on}. The voltage drop at RF, substituting all equations, is written as:

$$\begin{aligned} v_{RF}(t) = r_{on} i_{RF}(t) &+ S_{I+}(t) \times \{[S_{I+}(t) i_{RF}(t)] * z_{BB}(t)\} \\ &+ S_{I-}(t) \times \{[S_{I-}(t) i_{RF}(t)] * z_{BB}(t)\} \\ &+ S_{Q+}(t) \times \{[S_{Q+}(t) i_{RF}(t)] * z_{BB}(t)\} \\ &+ S_{Q-}(t) \times \{[S_{Q-}(t) i_{RF}(t)] * z_{BB}(t)\} \end{aligned} \tag{B.4}$$

Taking the Fourier transform to simplify the terms [1],

$$[S_{I+}(t) i_{RF}(t)] = \sum_{n=-\infty}^{\infty} \frac{1}{4} e^{-jn\frac{\pi}{4}} \sin c\left(\frac{n}{4}\right) e^{jn\omega_{LO}t}$$

$$[S_{I+}(\omega) \times I_{RF}(\omega)] * Z_{BB}(\omega) = \sum_{n=-\infty}^{\infty} \frac{1}{4} e^{-jn\frac{\pi}{4}} \sin c\left(\frac{n}{4}\right) 2\pi I_{RF}(\omega - n\omega_{LO}) Z_{BB}(\omega) \tag{B.5}$$

$$S_{I+}(\omega) \times [S_{I+}(\omega) \times I_{RF}(\omega)] * Z_{BB}(\omega) =$$

$$= \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} a_m a_n I_{RF}(\omega - (n+m)\omega_{LO}) Z_{BB}(\omega - m\omega_{LO}) \tag{B.6}$$

Combining the like terms and performing the summation,

$$V_{RF}(\omega) = r_{on} I_{RF}(\omega) + \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} a_m a_n I_{RF}(\omega - (n+m)\omega_{LO}) Z_{BB}(\omega - m\omega_{LO}) \left[1 + (-1)^{n+m} + e^{j(n+m)\frac{\pi}{2}} + e^{-j(n+m)\frac{\pi}{2}}\right] \tag{B.7}$$

The last part equals to M if n+m=4k,

$$V_{RF}(\omega) = r_{on} I_{RF}(\omega) + M \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} a_m a_n I_{RF}(\omega - (n+m)\omega_{LO}) Z_{BB}(\omega - m\omega_{LO}) \tag{B.8}$$

Calculating input impedance (Z_{in}) from the previous equations for 4 phase system (substituting n=m=2k),

$$\begin{aligned} Z_{in}(\omega) &= r_{on} + 4 \sum_{n=-\infty}^{\infty} |a_n|^2 Z_{BB}(\omega - n\omega_{LO}) \\ |a_n|^2 &= \left[\frac{1}{4} \frac{\sin(n\pi/4)}{n\pi/4} e^{-jn\pi/4}\right]^2 \end{aligned} \tag{B.9}$$

Expanding the summation and ignoring the higher order terms,

$$Z_{in}(\omega) = r_{on} + \frac{2}{\pi^2}\left[Z_{BB}\left(\omega - \omega_{LO}\right) + Z_{BB}\left(\omega + \omega_{LO}\right)\right] \tag{B.10}$$

B.2. Baseband Impedance calculation

Considering a 4-phase mixer (Fig.B.1(a)), the voltage drop at RF is given in terms of Z_{RF},

$$V_{RF}(\omega) = \left[I_{RF}(\omega) - I_S(\omega)\right] Z_{in}(\omega) \tag{B.11}$$

Equating both equations (B.10 and B.11), the input impedance for a 4 phase passive mixer is derived as in [3],

$$Z_{in} = r_{on} \| Z_s(\omega) + \frac{\left(\frac{Z_S(\omega)}{Z_S(\omega)+r_{on}}\right)^2 \frac{2}{\pi^2} Z_{BB}\left(\omega - \omega_{LO}\right)}{1 + \frac{2}{\pi^2} Z_{BB}\left(\omega - \omega_{LO}\right) \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2 + [Z_S(\omega + 4K\omega_{LO}) + r_{on}]}} \tag{B.12}$$

Considering only resistive components for source impedance and for M-path mixer, as in Fig.B.1(a) , the input impedance can be rewritten as,

$$Z_{\text{in}} = r_{on} \| Z_s(\omega) + \frac{\left(\frac{Z_S(\omega)}{Z_S(\omega)+r_{on}}\right)^2 \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) Z_{BB}(\omega - \omega_{LO})}{1 + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) Z_{BB}(\omega - \omega_{LO}) \sum_{k=-\infty}^{\infty} \frac{1}{(Mk+1)^2 + [Z_S(\omega + MK\omega_{LO}) + r_{on}]}} \tag{B.13}$$

$$Z_{\text{in}} = \frac{r_{on} R_s}{r_{on} + R_s} + \frac{\left(\frac{R_S}{R_S+r_{on}}\right)^2 \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) Z_{BB}(\omega - \omega_{LO})}{1 + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) Z_{BB}(\omega - \omega_{LO}) \sum_{k=-\infty}^{\infty} \frac{1}{(Mk+1)^2 + [R_S + r_{on}]}} \tag{B.14}$$

Using the identity, $\sum_{K=-\infty}^{\infty} \frac{1}{(KM+1)^2} = \frac{\pi^2}{M^2 \sin^2\left(\frac{\pi}{M}\right)}$,

$$Z_{in} = \frac{R_s}{r_{on} + R_s}\left[r_{on} + \frac{R_s \frac{M^2}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) Z_{BB}\left(\omega - \omega_{LO}\right)}{M\left(r_{on} + R_s\right) + Z_{BB}\left(\omega - \omega_{LO}\right)}\right] \tag{B.15}$$

Expressing the equation in terms of Z_{RF},

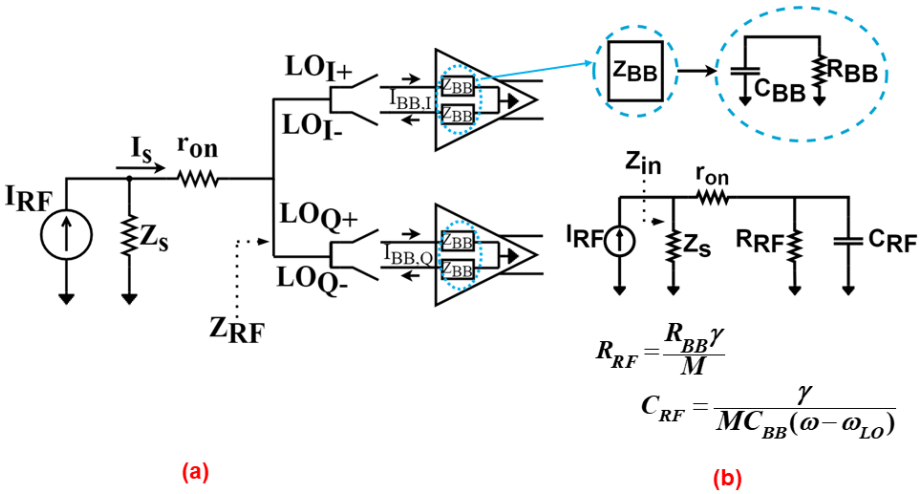

Figure B.1: (a) Passive mixer schematics. (b) Equivalent LTI model of the design in (a).

$$Z_{RF} = (r_{on} + R_s)\left[\frac{\frac{M^2}{\pi^2}\sin^2\left(\frac{\pi}{M}\right)Z_{BB}(\omega - \omega_{LO})}{M(r_{on} + R_s) + \left[1 - \frac{M^2}{\pi^2}\sin^2\left(\frac{\pi}{M}\right)\right]Z_{BB}(\omega - \omega_{LO})}\right] \quad \text{(B.16)}$$

B.3. Transform Balun specification

A off-chip, low cost balun such as ADTL2-18+, TCM4-14+, or TCM4-14 can be used. The insertion loss across the operation frequency is depicted in the Fig.B.2. The power consumption of the chosen balun is around 0.25 W.

FREQUENCY (MHz)	INSERTION LOSS (dB)	INPUT R. LOSS (dB)
200.00	1.22	11.75
300.00	1.11	13.94
500.00	0.85	17.09
700.00	0.86	18.47
800.00	0.76	16.98
1000.00	0.67	12.08
1200.00	0.69	8.13
1300.00	0.90	6.67
1350.00	1.06	6.06
1400.00	1.35	5.52

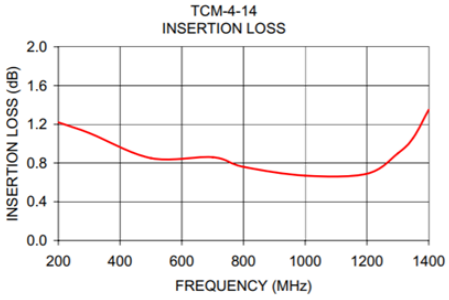

Figure B.2: PER vs. SNR plots for different MCS.

B.4. Large capacitor value calculation for general 1st order receiver design

The BB impedance can be calculated from the design equation.3.5. Asumming r_{on} to be a lest value 5Ω, in-order to increase the possible range of BB resistance value. For 4-phase passive mixer, BB resistance value is,

$$\begin{aligned} Z_S &= r_{on} + R_{BB}\frac{\gamma}{M} \\ \gamma &= \frac{M^2}{\pi^2}\sin 2\left(\frac{\pi}{M}\right) = \frac{8}{\pi^2} = 0.81 \\ 50 &= 5 + \frac{R_{BB}(0.81)}{4} \\ R_{BB} &= 222\Omega \\ R_{RF} &= \frac{R_{BB}\gamma}{M} \\ R_{RF} &= 45\Omega \end{aligned} \tag{B.17}$$

The frequency equation for $R_{BB} \parallel C_{BB}$ (BB impedance) is $f_{3dB} = 1/2\pi R_{eq} C_{BB,max}$. The $R_{eq} = (R_S + r_{on}) \| R_{RF}$, which is 25 Ω. For 802.11ah 1 MHz bandwidth, the maximum required BB capacitance value is calculated as,

$$C_{BB,max} = \frac{2}{2.\pi.M.R_{eq}.10^6} = 3.18nF \tag{B.18}$$

Now for a differential structure,

$$\begin{aligned} 4 * Z_S &= 2 * r_{on} + R_{BB}\frac{\gamma}{M} \\ \gamma &= \frac{M^2}{\pi^2}\sin 2\left(\frac{\pi}{M}\right) = \frac{8}{\pi^2} = 0.81 \\ 200 &= 10 + \frac{R_{BB}(0.81)}{4} \\ R_{BB} &= 938\Omega \\ R_{RF} &= \frac{R_{BB}\gamma}{M} \\ R_{RF} &= 190\Omega \end{aligned} \tag{B.19}$$

$R_{eq} = 100\Omega$, and the $C_{BB,max} = 797pF$ (4X times lower than equation.B.18).

B.5. Temperature and Process analysis

	Temp	$gm_{tia}mS$	$gm_{tia}r_o$	Expected S11 (dB)	Simulated S11 (dB)
TT	27	15.1	32.5	-25.2	-23.8
TT	-20	12.3	33.5	-27.3	-26.8
TT	80	17.3	30	-24.2	-24.1
SS	10	10.1	31.6	-18.4	-20.9
SS	80	13.7	31.3	-23.8	-26.9
FF	-40	16.2	33.7	-21.7	-19.5
FF	80	21	28.9	-22.5	-20.7

Table B.1: Process and temperature variation effect on S11

	Temp	$gm_{tia}mS$	$gm_{tia}r_o$	Expected Gain (dB)	Simulated Gain (dB)
TT	27	15.1	32.5	26	27.9
TT	-20	12.3	33.5	26	27.8
TT	80	17.3	30	26	27.1
SS	10	10.1	31.6	25.9	25.6
SS	80	13.7	31.3	26	27.1
FF	-40	16.2	33.7	26	28.2
FF	80	21	28.9	26.1	28.3

Table B.2: Process and temperature variation effect on Gain

	Temp	$gm_{tia}mS$	$gm_{tia}r_o$	Expected Noise (dB)	Simulated Noise (dB)
TT	27	15.1	32.5	5.96	6.18
TT	-20	12.3	33.5	5.93	5.71
TT	80	17.3	30	6.15	6.40
SS	10	10.1	31.6	5.85	5.95
SS	80	13.7	31.3	6.75	6.72
FF	-40	16.2	33.7	5	5.50
FF	80	21	28.9	5.69	6.02

Table B.3: Process and temperature variation effect on Noise

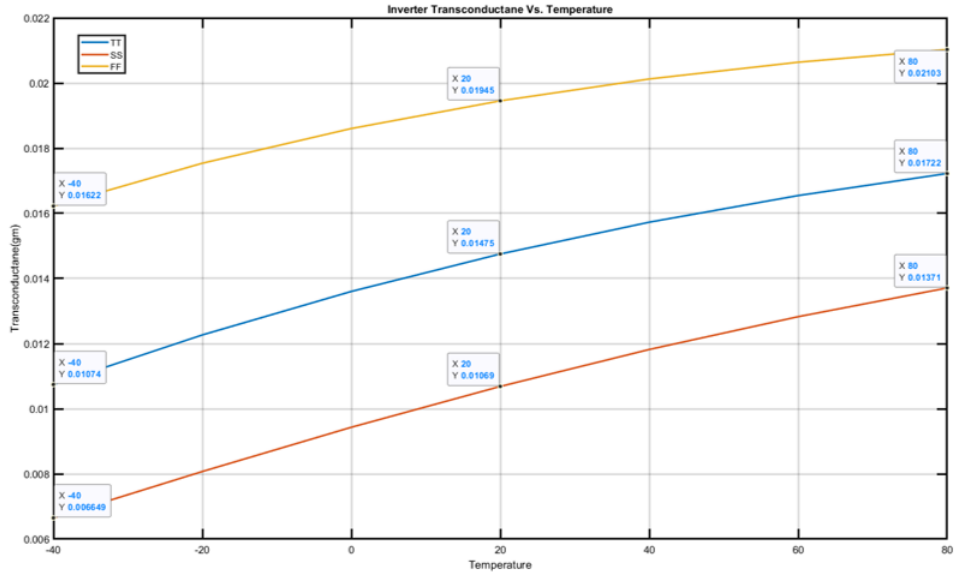

Figure B.3: Temperature and model variation effect on inverter transconductance gm_{tia}

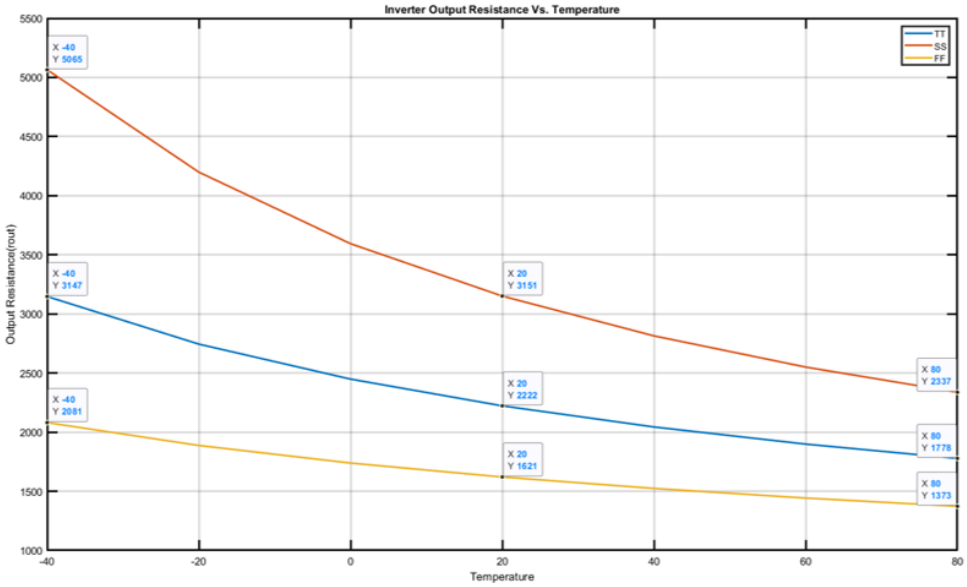

Figure B.4: Temperature and model variation effect on output resistor r_o

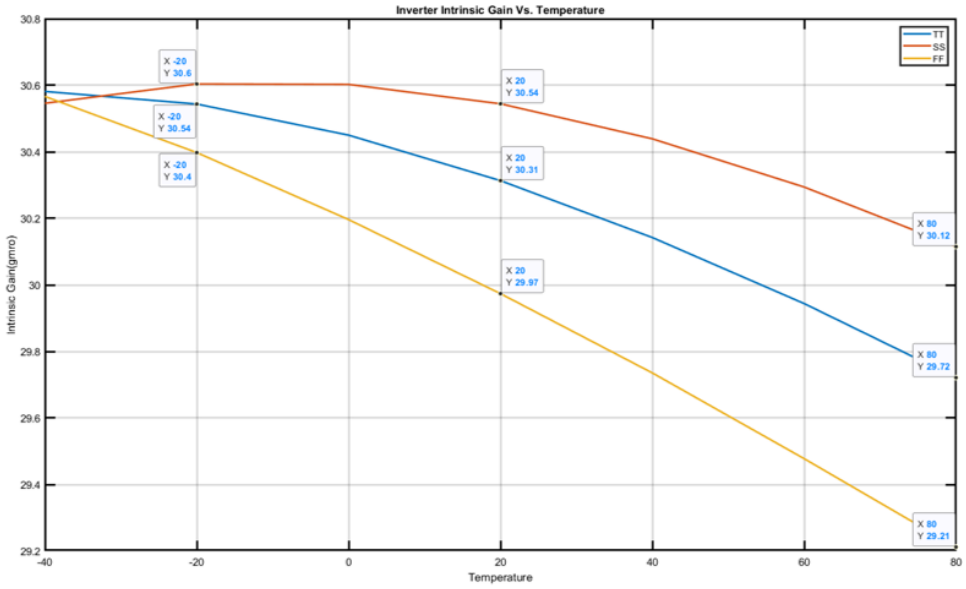

Figure B.5: Temperature and model variation effect on intrinsic gain of inverter $gm_{tia}r_o$

B.6. Length of the MOSFET estimation

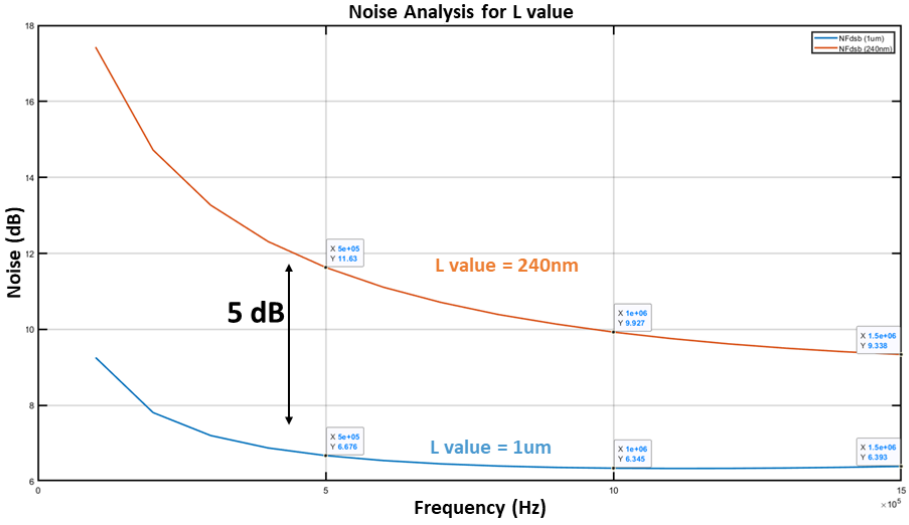

Figure B.6: Noise analysis for L = 240 nm and L = 1 um.

B.7. Process variation for image rejection and notch filter

	20%		IRR	
	min	**max**	**min**	**max**
5000 Ω	4000 Ω	6000 Ω	18dB/34dB	20dB/33dB
1700 Ω	1360 Ω	2040 Ω		
800 Ω	640 Ω	960 Ω	**Center frequency**	
55pF	44pF	66pF	**min**	**max**
80pF	64pF	96pF	1.2M	0.8/700kHz
100pF	80pF	120pF	**ACR/NACR**	
22 pF	17.6pF	26.4pF	**min**	**max**
1600 Ω	1280 Ω	1920 Ω	11dB/20dB	19dB/30dB

Table B.4: 20% variation analysis - IRR, center frequency, and ACR/NACR

	5%		IRR	
	min	**max**	**min**	**max**
5000 Ω	4750 Ω	5250 Ω	28dB/37dB	33dB/37dB
1700 Ω	1615 Ω	1785 Ω		
800 Ω	760 Ω	840 Ω	**Center frequency**	
55pF	52.2pF	57.7pF	**min**	**max**
80pF	76pF	84pF	1M	0.9M
100pF	95pF	105pF	**ACR/NACR**	
22 pF	20.9pF	23.1pF	**min**	**max**
1600 Ω	1520 Ω	1680 Ω	16dB/32dB	15dB/35dB

Table B.5: 5% variation analysis - IRR, center frequency, and ACR/NACR

B.8. 1 MHz LIF operation : simulation outputs

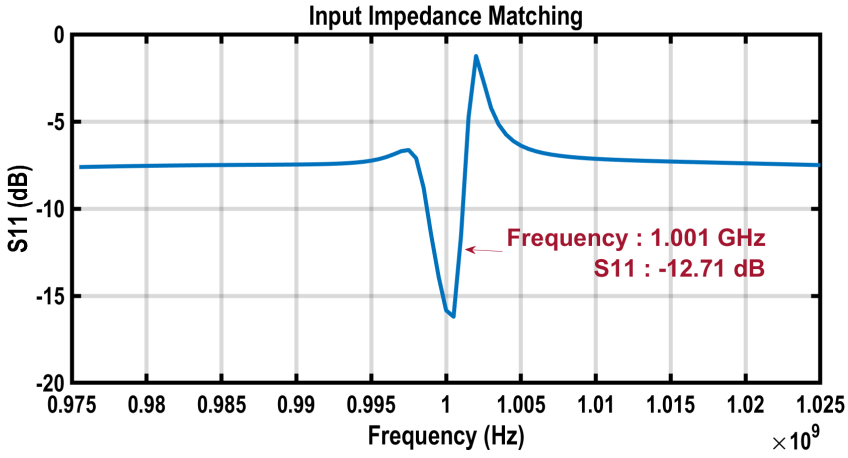

Figure B.7: Input impedance - LIF architecture

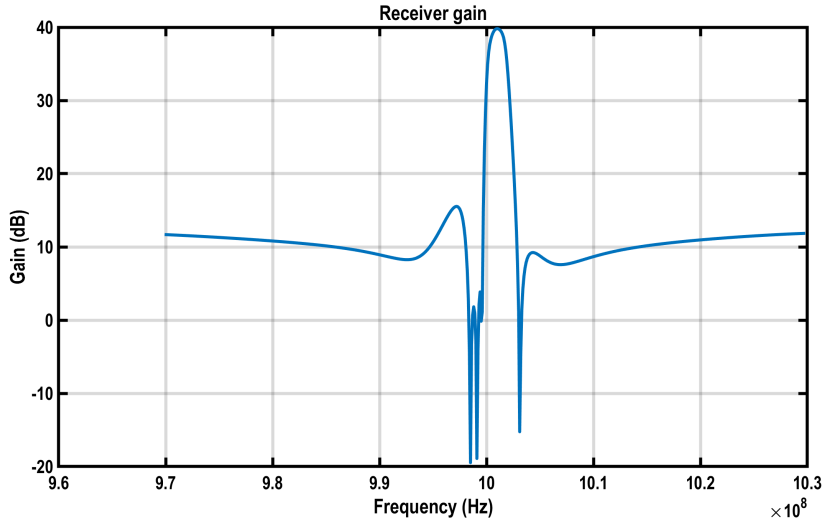

Figure B.8: Gain transfer function - LIF architecture

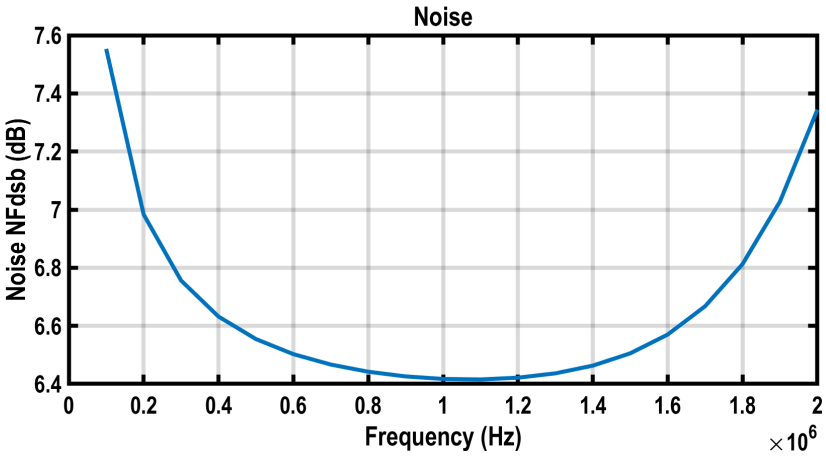

Figure B.9: Noise transfer function - LIF architecture

References

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[2] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, *Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers,* IEEE Transactions on Circuits and Systems I: Regular Papers **57**, 2353 (2010).

[3] A. Mirzaei and H. Darabi, *Analysis of imperfections on performance of 4-phase passive-mixer-based high-q bandpass filters in saw-less receivers,* IEEE Transactions on Circuits and Systems I: Regular Papers **58**, 879 (2011).

List of Figures

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Abbreviations & Acronyms

ACR Adjacent Channel Rejection. 3, 5, 8, 11, 26, 39, 73, 82, 83, 85, 101, 103

ADC analog-to-digital converter. 3, 4, 26

BAW bulk acoustic Waves. 21

BB baseband. 3, 8, 9, 13, 21–27, 29–31, 35, 36, 46, 48, 52–54, 68, 83, 92, 93, 103, 111, 119

BPF bandpass Filter. 8, 21, 22, 24, 31–36, 67, 70, 119, 120

BPSK Binary phase-shift keying. 2, 3, 6–8, 10

CMOS Complementary Metal–Oxide Semiconductor. 3, 9, 13, 18, 21, 43, 44, 60

D-LTF beamformed long training field. 16

D-STF beamformed short training field. 16

DFT discrete Fourier transform. 18

f frequency. 2, 13

flicker noise corner frequency. 14, 18

GI guard intervals. 18

gm transconductance. 27, 33, 38, 43, 44, 56, 57, 64, 65

HPF highpass Filter. 39

IDFT inverse discrete Fourier transform. 18

IF intermediate frequency. 9, 14, 18

IIP2 Input second-order intercept. 10

IIP3 Input third-order intercept point. 10, 88, 92

IMD inter-modulation distortion. 10

IoT Internet of things. ix, 1–3

IP2 second-order intercept. 10

IP3 third-order intercept point. 10

IRR image rejection ratio. 9, 10, 100, 103, 123

LIF low intermediate frequency. ix, 3, 8, 9, 11–13, 18, 21, 29, 31, 35, 36, 38–40, 67, 68, 70, 77, 81, 82, 89, 90, 92, 101, 103, 119, 120

LNA low noise amplifier. ix, 3, 9, 11, 13, 14

LO local oscillator. 3, 9, 13, 14, 22–25, 107, 119

LoRa Long range. 2

LPF lowpass filter. 9, 13, 21, 22, 24, 28, 30, 31, 33–36, 39, 44, 46, 59, 61, 68, 82, 103, 119

LTF1 initial long training field. 16

LTF2-N long training field. 17

MAC Medium Access Control. 2, 15

MCS modulation coding schemes. v, 2–7, 10, 16, 110, 119, 121

MIMO multiple-input and multiple-output. 16, 17

NACR Non-Adjacent Channel Rejection. 3, 5, 8–11, 26, 39, 73, 83, 85, 101, 103

NF noise figure. 6, 7, 9, 11, 18, 22, 25, 27–29, 31, 39, 52, 54, 56, 59, 61, 62, 67, 68, 70–73, 75, 82, 86, 90, 100, 103, 123

NMOS Negative channel metal oxide semiconductor. 44, 54, 64, 74, 75, 77, 81, 93

OFDM orthogonal frequency-division multiplexing. 4, 17, 18

Output intercept point. 10

OOB out-of-band. 13, 14, 22, 28

opamp Operational amplifier. 27, 30, 34, 45, 52, 58

OTA operational transconductance stage. 28, 29, 49, 64–66, 76–78, 86, 93, 95, 123

PAPR peak to average power ratio. 4

PER packet error rate. 3, 5, 6, 110, 119, 121

PHY PHYsical. 2, 15

PLCP physical layer conformance procedure. 15

PMOS Positive channel metal oxide semiconductor. 44, 75, 77

PPDU PLCP protocol data unit format. 15, 17, 119

PPF polyphase filter. 21, 36–39, 72, 119

PSDU Presentation Layer Service Data Unit.. 17

Q quality-factor. 3, 9, 21, 22, 24, 25, 29, 35, 36, 46, 55, 63, 64, 68, 120

QAM Quadrature amplitude modulation. 2, 3, 6–8, 10

QPSK Quadrature Phase Shift Keying. 2, 3, 8, 10

on-resistance. 22, 24, 25, 53, 54, 108–111

RF radio frequency. 3, 6, 9, 13, 14, 21–25, 36, 48, 53, 54, 93, 107–109

RX receiver. ix, 13, 23, 24, 26, 27, 39, 43, 53, 54, 81, 119

SAW surface acoustic wave. 3, 13, 21

SIG signalling field. 16

SNR signal-to-noise ratio. v, 4–7, 9, 10, 18, 110, 119, 121

STF short training field. 16

time period of the local oscillator. 22, 23

TIA transimpedance amplifier. 25–31, 35, 44, 45, 49, 57, 60, 61, 64, 76, 93, 95, 119

WiFi Wireless Fidelity. 1, 2, 10

ZIF zero intermediate frequency. ix, 3, 7, 8, 11–14, 18, 21, 25, 32, 35, 40, 55, 57, 59, 62, 67, 68, 76, 77, 81–83, 87, 88, 92, 100, 101, 103, 119, 120

Nomenclature