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32.2 A Pitch-Matched ASIC with Integrated 65V TX and Shared Hybrid Beamforming ADC for Catheter-Based High-Frame-Rate 3D Ultrasound Probes

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Intra-cardiac echography (ICE) probes (Fig. 32.2.1) are widely used in electrophysiology for their good procedure guidance and relatively safe application. ASICs are increasingly employed in these miniature probes to enhance signal quality and reduce the number of connections needed in mm-diameter catheters [1-5]. 3D visualization in real-time is additionally enabled by 2D transducer arrays with, for each transducer element, a high-voltage (HV) transmit (TX) part, to generate acoustic pulses of sufficient pressure, and a receive (RX) path, to process the resulting echoes. To achieve the required reduction in RX channels, micro-beamforming (μBF), which merges the signals from a subarray using a delay-and-sum operation, has been shown to be an effective solution [3,4]. However, due to the frame-rate reduction that is associated with μBF, these designs cannot serve emerging high-frame-rate imaging modes (~1000 volumes/s) like 3D blood-flow and elastography imaging. In-probe digitization has recently been investigated to provide further channel-count reduction, make data transmission more robust, and enable pre-processing in the probe [1-3]. However, these earlier designs have either no TX functionality [2,3] or only low-voltage (LV) TX [1] integrated. Combining μBF and digitization with area-hungry HV transmitters in a pitch-matched scalable fashion while supporting high-frame-rate imaging remains an unmet challenge. The work presented in this paper meets this target, enabled by a hybrid ADC, the small die size of which allows for co-integration with 65V element-level pulsers.

Figure 32.2.2 gives an overview of the architecture. The elements of a 2D transducer array are connected to unipolar HV pulsers, implemented as an area-efficient pull-up, pull-down structure. An isolation switch (T/R) is merged with the TX structure to protect the LV RX circuitry during pulsing with only one additional LV transistor. The RX path features an analog front-end (AFE) comprising a low-noise amplifier (LNA) and a programmable-gain amplifier (PGA) that, together, realize a voltage gain ranging from –6 to 48dB. This enables time-gain compensation (TGC), a reduction of the dynamic range (DR) by increasing the AFE gain over time to compensate for the propagation attenuation of the acoustic signal. The second-stage amplifier further converts the single-ended signal to a differential output to provide common-mode interference rejection for the following stages. Both amplifier stages include a low-frequency regulation path to maintain the operating points while switching gains during one pulse-echo (PE) cycle.
The outputs of three AFEs are merged by μBF, implemented using analog sample-and-hold (S/H) cells. The choice of the μBF subarray size presents a trade-off: larger groups help to reduce the channel count [3,4] but in turn suffer from reduced image quality due to the finite delay quantization as well as frame-rate loss, since the narrower μBF beamwidth covers a smaller part of the volume of interest and hence more pulse-echo cycles need to be combined to construct a full image. In this design, a 3×1 subarray achieves a 3-fold channel reduction while only requiring RX beams steered to seven elevation angles on the chip, enabling >1000 volumes/s for a target imaging depth of 10cm.
Following the μBF, an ADC is shared by two subarrays, forming a subgroup of 3×2 elements. The ADC outputs are transmitted to the periphery of the chip, where a clock data recovery (CDR) and datalink circuit realign and combine the data. Two subgroup outputs are merged, 8b/10b-encoded and fed to cable drivers, realizing a 12-fold total channel count reduction. As such, a full 3D ICE probe with about 1000 elements requires only <100 data channels in the catheter.

The ADC is strongly integrated with the architecture of the ultrasound ASIC (Fig. 32.2.3). A charge-sharing successive-approximation (SAR) first stage directly employs the S/H cells of the μBF as sampled inputs [3], avoiding the need for a power-hungry, high-bandwidth ADC driver as in [1,2]. To minimize the area and power impact of the converter, a hybrid structure between the energy-efficient, fast but area-wise inefficiently scaling SAR first stage and an area-efficient, linear but slow single-slope (SS) second stage is chosen. In contrast to [2], the SS ramp is generated using compact current sources rather than a capacitive digital to analog converter (CDAC). For the 10b 24MS/s ADC, a trade-off between the stages is found in a 6b SAR and 5b SS distribution with 1b of redundancy to correct for non-idealities in the conversion. To deal with variability, the SAR reference charge, SS current, and comparator offset are locally calibrated in a short interval between the TX and RX phases with a reference provided through the PGA. Adjusting to the arrayed nature of the application, one ADC is shared by two RX subarrays, both performing SAR and SS conversion alternatingly, thus dividing the area. A major benefit of this is that the CDAC of the ADC can be pre-charged for the next SAR conversion during SS operation, removing the need for a high bandwidth reference generator as required in other SAR ADCs [1,2]. Performing the conversion entirely in the charge domain additionally enables the use of metal-oxide-semiconductor capacitors (MOSCAPs) in the CDAC. While their voltage-dependent capacitance excludes them from use in many other ADC architectures, in charge-sharing topologies they reduce area through high integration density, improve comparator offset as well as noise tolerance [6] and can be sized to have negligible impact on the system linearity, which is limited by the AFE. A comparison to the prior art in miniature ultrasound probe ADCs is given in Fig. 32.2.5. Being fully integrated with an efficient reference generator, local variation calibration and working with a low-bandwidth driver as well as being more than 4× smaller and consuming more than 1.5× less power than comparable designs per subarray [3], the shared hybrid ADC is a suitable solution for application in large ultrasound arrays.

An 8×9 element prototype was fabricated in a 0.18μm BCD process and its performance was verified electrically by wirebonding out several transducer bondpads and evaluating the ADC outputs. As the TX operation has a small duty cycle, the total power consumption is dominated by the RX part, with 0.65mW/element in the core and 1.23mW/element including the datalink and LVDS drivers. The subgroup power and area distribution as well as its pitch-matched floorplan are shown in Fig. 32.2.5. Figure 32.2.4 shows the AFE gain and signal to noise ratio (SNR) characterized by applying a sinusoidal test input from a waveform generator at 5.95MHz. An 8.1MHz -3dB cut-off frequency is seen in the highest 48dB gain setting with -6dB steps to the lowest total gain of -6dB. The peak SNR is 52.3dB with a folded -35dB third and -62dB fifth harmonic from the PGA output stage in an 80% bandwidth around the transducer center frequency. Finally, the time domain plots in Fig. 32.2.4 show 65V pulsing and a demonstration of the TGC in one PE cycle, confirming the availability of the full DR for high frame-rate imaging.

As shown in Fig. 32.2.5, a transducer array is directly mounted on top of the ASIC. To enable manufacturing on the small prototype, the chip is enlarged and two dummy element rings are included. For acoustic measurements, the assembly is immersed in a water tank and connected to an FPGA through a 1m cable. By sweeping the transducer surface pressure at all AFE gain settings and recording the ADC outputs, the characterized DR is found to be 91dB (Fig. 32.2.4). The input-referred noise at the highest gain with the transducer elements loaded by water is 12.7nV/√Hz at 6MHz, around 5nV/√Hz higher than what the electronics are designed for with the difference being attributed to the thermal noise of the transducer. Two tones appear due to mismatch in the μBF S/H cells but by recording and subtracting the pattern, they are readily removed. A pulse-echo imaging experiment with a phantom of 3 needles placed in front of the ASIC is described in Fig. 32.2.6. While the aperture is too small to provide the resolution of a full array, the needle heads can clearly be distinguished in 3D space, demonstrating the imaging capability of the system at the intended frame-rate.

Figure 32.2.7 summarizes the performance and compares the system with previously presented catheter-based ultrasound systems. In this work, element-level HV TX and AFEs as well as RX μBF and in-probe digitization are integrated in a scalable fashion for 3D imaging. An area-efficient ADC and architecture enable the circuitry to fit in an element area small enough for sufficient spatial sampling while also enabling high frame-rate imaging at a feasible channel count. Combined with competitive power consumption and large dynamic range, this makes the design a promising solution for next-generation imaging catheters.

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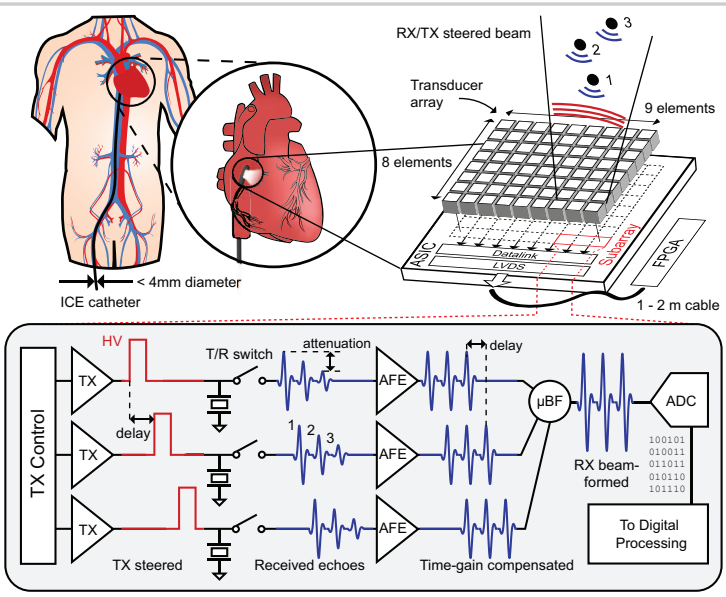


Figure 32.2.1: Overview of the application and applied techniques.

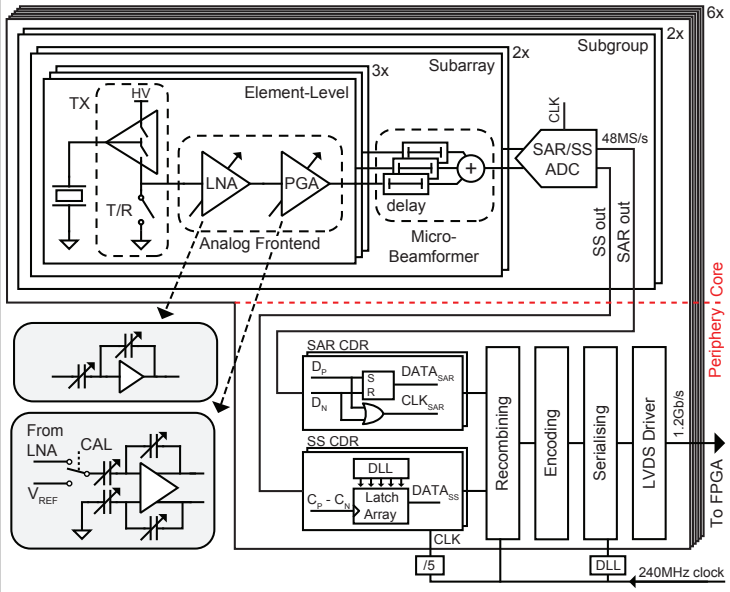


Figure 32.2.2: System block diagram with analog front-end details.

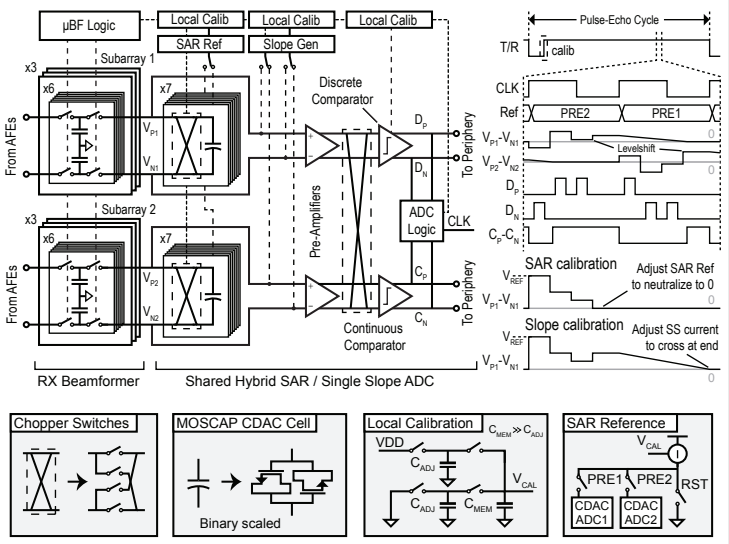


Figure 32.2.3: Circuit diagram of the shared hybrid ADC with timing diagram (showing 3b SAR conversion for simplicity).

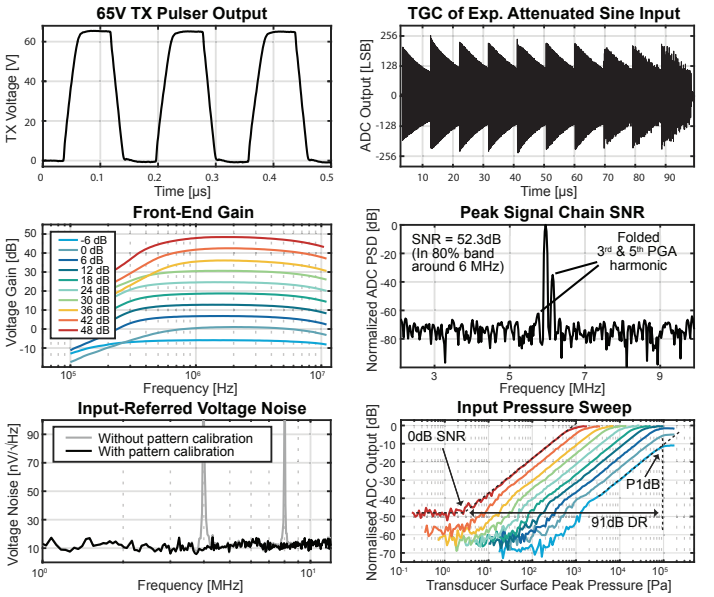
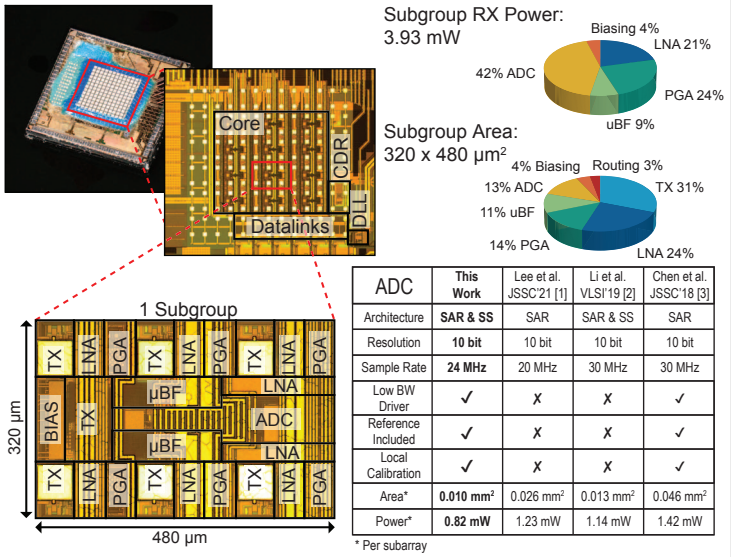


Figure 32.2.4: Electrical and acoustic measurement results.



ADC	This Work	Lee et al. JSSC'21 [1]	Li et al. VLSI'19 [2]	Chen et al. JSSC'18 [3]
Architecture	**SAR & SS**	SAR	SAR & SS	SAR
Resolution	**10 bit**	10 bit	10 bit	10 bit
Sample Rate	**24 MHz**	20 MHz	30 MHz	30 MHz
Low BW Driver	✓	✗	✗	✓
Reference Included	✓	✗	✗	✓
Local Calibration	✓	✗	✗	✓
Area*	**0.010 mm²**	0.026 mm²	0.013 mm²	0.046 mm²
Power*	**0.82 mW**	1.23 mW	1.14 mW	1.42 mW

* Per subarray

Figure 32.2.5: Die micrograph with subarray floorplan, distribution of area/power and state-of-the-art comparison of miniature ultrasound probe ADCs.

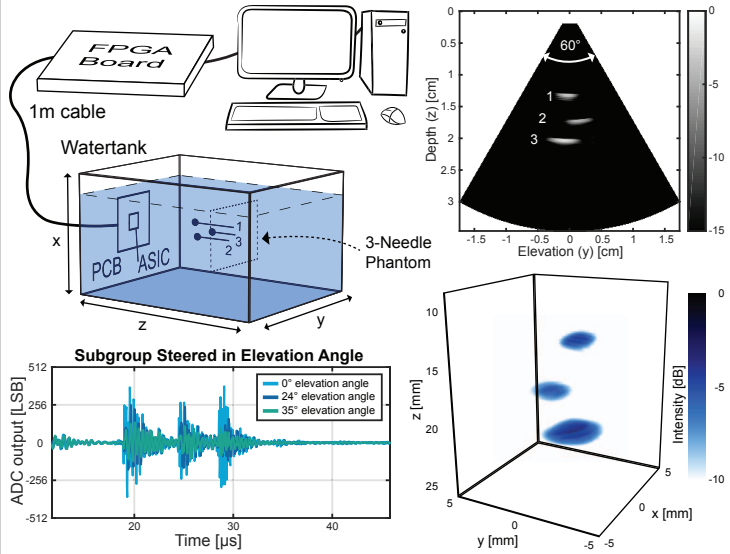


Figure 32.2.6: Imaging of a 3-needle phantom in a watertank: experimental setup, example subgroup output, B-mode image, and 3D rendering.

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	This Work	Lee et al. JSSC'21 [1]	Kang et al. JSSCC'20 [5]	Li et al. VLSI'19 [2]	Chen et al. JSSC'18 [3]	Wildes et al. TUFFC'16 [4]
Process	**180 nm BCD**	180 nm	180 nm BCD	180 nm	180 nm	N/A
Transducer	**2D PZT**	2D PMUT	1D CMUT	2D PZT	2D PZT	2D PZT
Array Size	**8 x 9**	6 x 6	64	4 x 4	6 x 24	60 x 14
Integrated Transducer	✓	✗ *	✓	✓	✓	✓
Center Freq.	**6 MHz**	5 MHz	7 MHz	5 MHz	5 MHz	5.6 MHz
Pitch-Matched	✓	✗ †	✓	✓	✓	✓
Element Pitch	**160 µm x 160 µm**	250 µm x 250 µm	205 µm x 1800 µm	150 µm x 150 µm	150 µm x 150 µm	110 µm x 180 µm
Integrated TX	✓	✓	✓	✗	✗	✓
Max. TX Voltage	**65 V**	13.2 V	60 V	N/A	N/A	40 V
Digitization	✓	✓	✗	✓	✓	✗
RX Architecture	**AFE + µBF + ADC + Datalink**	AFE + ADC	AFE	AFE + ADC	AFE + µBF + ADC + Datalink	AFE + µBF
Channel Reduction	**12−fold**	N/A	N/A	N/A	36−fold	15−to 20−fold
Supported Frame-Rate	**1000 vol/s**	N/A	N/A	N/A	200 vol/s	50 vol/s
Active Area / El.	**0.032 mm² §**	0.063 mm²	0.464 mm²	0.023 mm²	0.026 mm² §	N/A
RX Power / El.	**1.23 mW §**	1.14 mW	5.2 mW	1.54 mW	0.91 mW §	< 0.12 mW
Input DR	**91 dB**	N/A	82 dB	N/A	85 dB	N/A
Peak SNR	**52.3 dB**	57.8 dB ‡	N/A	49.8 dB	51.8 dB	N/A

* Transducers on separate board connected with wires
† Scalability limited by transducer connection out of pitch
‡ ADC only, excluding AFE
§ Including the datalink and LVDS drivers

Figure 32.2.7: Performance summary and comparison with the state of the art in ultrasound catheter imaging systems.

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