A Combined Time-Gain Compensation Low-Noise Amplifier For Ultrasound Imaging Applications

MSc Thesis

by

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Abstract

This work presents a type of low noise amplifiers (LNA) that are used for ultrasound imaging systems. To account for the attenuating nature of ultrasound echo signals, a so-called time gain compensation (TGC) circuit is required. By increasing the gain over time, the output dynamic range is decreased, while the switching artifacts are suppressed by the continuous gain control.

The proposed work combines the LNA structure with TGC functionality. This is done, such that the first component in the ultrasound receive chain does not need to be able to handle the full dynamic range of the input signal. The goal is to reduce die area and power consumption costs compared to systems that utilize separate LNAs and TGCs.

The combined TGC-LNA consists of a transimpedance amplifier (TIA) with an exponentially-varying feedback resistance. As the feedback network and feed-forward path are separately designed, the design of the TGC functionality and low noise functionality can for a large part be independently designed.

The TGC functionality is implemented by an exponentially-varying feedback resistance. This is achieved by means of implementing triode transistors as voltage-controlled resistors. Three branches with differently sized triode devices are required to obtain the full gain range of 40 dB.
A two-stage telescopic amplifier realizes the loop amplifier. The bias current of the first stage is a linear function of the total feedback resistance to create a constant unity-gain bandwidth in a power efficient method.

Realized in 0.180 μm BCDMOS technology, the combined TGC-LNA amplifies the signals from a Capacitive Micromachined Ultrasound Transducer (CMUT) with a center frequency of 7.5 MHz. The total achieved gain range is 40 dB where the gain varies during a receive period of 100 μs. During the receive period the total harmonic distortion remains below -44 dB and the noise floor is 1.12 pA/$\sqrt{Hz}$ at the highest gain setting. Drawing 5.5 mW from a 1.8 V supply and requiring approximately 0.01 mm^2 die area, the proposed TGC-LNA provides a new method for reducing power consumption and area costs for miniature ultrasound applications.

Keywords: Ultrasound imaging, transimpedance amplifier, time-gain compensation, triode transistors, continuous gain control.

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Contents

List of acronyms

AGC Automatic Gain Control

AFE Analog Front End

ASIC Application Specific Integrated Circuit

CDN Current Division Network

CMFB Common Mode Feedback

CMUT Capacitive Micromachined Ultrasound Transducer

DR Dynamic Range

LNA Low Noise Amplifier

MIM Metal Insulator Metal capacitor

OTA Operational Transconductance Amplifier

PVT Process/Voltage/Temperature

SNR Signal to Noise Ratio

TGC Time Gain Compensation

THD Total Harmonic Distortion

TIA Transimpedance Amplifier

TR-switch Transmit/Receive Switch

UGBW Unity Gain Bandwidth

VGA Variable Gain Amplifier

1 Introduction

Over the past century the life expectancy of human beings has greatly increased. This is especially the case in the western world, where the economy is thriving. One of the consequences of a higher life expectancy is that diseases that are connected to ageing are becoming more prevalent [1]. One group of diseases that became more prevalent for ageing populations are cardiovascular diseases. For example, the World Health Organization (WHO) published that the most common cause of death in the year 2016 was ischaemic heart disease [2].
To accurately diagnose and treat patients with cardiovascular diseases, nowadays ultrasound imaging is often utilized. Ultrasound echography allows for accurate and safe scanning of the patient, while being widespread available, due to its affordability.

Traditional ultrasound systems are quite bulky with large probes connected via cable to large imaging systems. Often these probes are placed outside the body as there is no room for these probes inside the body. In recent years, however, there is a shift to smaller, more accurate and even more affordable ultrasound devices. One focus for designing smaller devices is to create ultrasound probes that are able to be applied inside the patient's body. These smaller devices are enhancing the efficacy, affordability and general use of ultrasound applications.
Apart from the trend for smaller devices, imaging systems are also moving from 2D imaging to 3D imaging. This trend is greatly increasing the number of transducer elements in a probe. To cope with both the smaller probes and the larger number of transducer elements, Application Specific Integrated Circuits (ASICs) are used to interface with the transducers. ASICs are required to minimize power and area requirements while also trying to minimize the number of necessary external cables.

A critical module of the ASIC is the Analog Front End (AFE). The AFE receives and partly processes incoming echo signals before data is sent to an external imaging system. Current in-probe AFEs, due to limitations in die size and power consumption, make trade-offs that causes their performance to lag behind that of AFEs in imaging system. By improving on the AFE's power and area efficiency the imaging performance of the AFE can be improved.

This thesis focuses on the design of a certain type of Low Noise Amplifier (LNA), which is one of the first components in the receive chain. The LNA in ultrasound applications is commonly followed by a Time Gain Compensation (TGC) amplifier. The TGC is used to take care of the signal attenuation present in echo signals. The goal of this thesis is to combine the LNA and TGC amplifier in a single structure aiming at an area- and power-efficient design.

1.1. Background

Ultrasound imaging has become mainstream in the diagnosis and treatment of cardiovascular diseases, as it is safe to use while also being affordable. It decreases the need for conventional surgeries, as minimally invasive operations are possible. These minimally invasive operations reduce stress for the patient while increasing the recovery speed. Ultrasound imaging allows for treatment even at advanced age without large health risks.
An example of an ultrasound application in which this thesis work can be applied is transesophageal echocardiography, where a relative small probe is placed inside the esophagus of the patient to obtain a clear image of

the heart. The advantage with respect to conventional echography is that reflections due to the ribs and lungs are eliminated and have no impact on the image quality [3].

1.2. Ultrasound Imaging System

In an ultrasound imaging system, high frequency acoustic waves in the order of several MHz are used to image tissue. As acoustic waves travel through the body, the waves scatter and echo back to the imaging system. Measured reflections are used to reconstruct an image of the scanned tissue. This requires a system that is able to both transmit and receive ultrasound pulses.

Ultrasound imaging systems are widespread and Figure 1.1 shows a typical block diagram of such a system [4]. It contains mainly three different blocks. The first block represents the transducer elements. The transducer elements are responsible for both the transmission and reception of acoustic waves and the transduction between the electrical and acoustical domain. Ultrasound transducers are often implemented using either piezo electric or capacitive micromachined transducers.
For miniature catheter-based echo probes the transducers are placed on top of an ASIC [5]. The ASIC represents the second block and is required to decrease the number of cables required to read out and control the large number of separate transducer elements. The ASIC contains the front-end electronics responsible for both the transmission (TX) and reception (RX) of acoustic signals. The ASIC also has driving capabilities to send data to the third block, which is the back-end imaging system. This third block receives and processes the data of the ASIC to form images to reconstruct the scanned tissue.

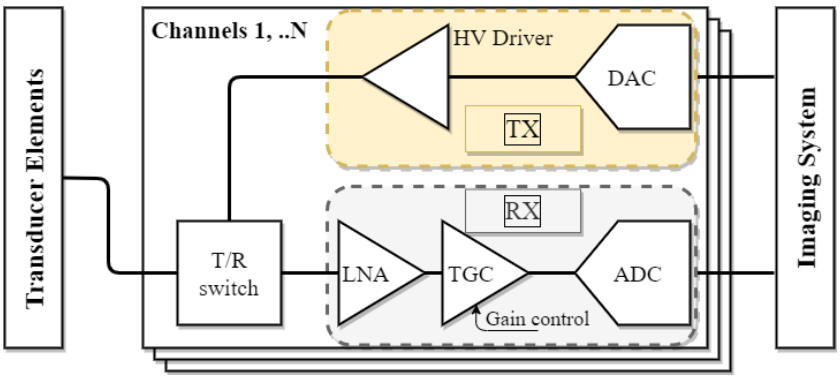


Figure 1.1: Block diagram of a typical ultrasound system [4]

This work focuses on the receive path, aiming at improving area and power efficiency. As can be seen in Figure 1.1 the receive path contains both a low noise amplifier and a time gain compensation amplifier. In this work these components are combined in a single amplifier. The next section deals with the time gain compensation functionality.

1.3. Introduction to Time-Gain Compensation

The ultrasound pulses are traveling through the body for a certain distance before they are back-scattered to the imaging probe. Signal energy is lost over traveling distance and the received echo signal will be attenuated. In [6] it becomes clear that the attenuation of ultrasound signals is exponential or linear in dB and proportional to both the signal frequency and to the signal travel distance. The general attenuation of ultrasound signals can be expressed as follows:

$$\text{Attenuation} = \alpha * \left[\frac{\text{dB}}{\text{MHz} * \text{cm}}\right] * l[\text{cm}] * f[\text{MHz}] \tag{1.1}$$

This poses an immediate limitation to the possible frequencies that can be used for a certain imaging depth. Even though higher frequencies can improve the image resolution, the depth of view is reduced with increased frequency due to the attenuation.

Longer distance travelling signals will return at a later time moment to the transducer. This means that there is a direct connection between the signal attenuation and the receive time. The later signals arrive the more

attenuated they are. To obtain a constant amplitude envelope time-gain compensation (TGC) amplifiers are introduced. A TGC amplifier increases its gain over time to mitigate the effect of signal attenuation to achieve a constant output amplitude envelope.

Figure 1.2 shows the signal attenuation over time and applies an ideal gain compensation to achieve a constant output amplitude envelope [7]. Another viewpoint looks into the dynamic range (DR) of the system. Figure 1.2 shows that the instantaneous dynamic range, i.e., the ratio of the largest and the smallest echo-signal amplitudes, is constant. However, due to signal attenuation, the overall dynamic range is much larger than the instantaneous dynamic range. A typical reflected ultrasound signal has an instantaneous DR of up to 60 dB. Adding an attenuation of 40-50 dB results in an overall dynamic range of more than 100 dB[8]. An overall DR of more than 100 dB is beyond the range of many regular ADCs or requires very power expensive ADCs[9]. TGCs are therefore necessary to reduce the overall dynamic range of the output signal. Ideally the TGC follows the signal attenuation and the end result is that the overall DR is equal to the instantaneous DR.

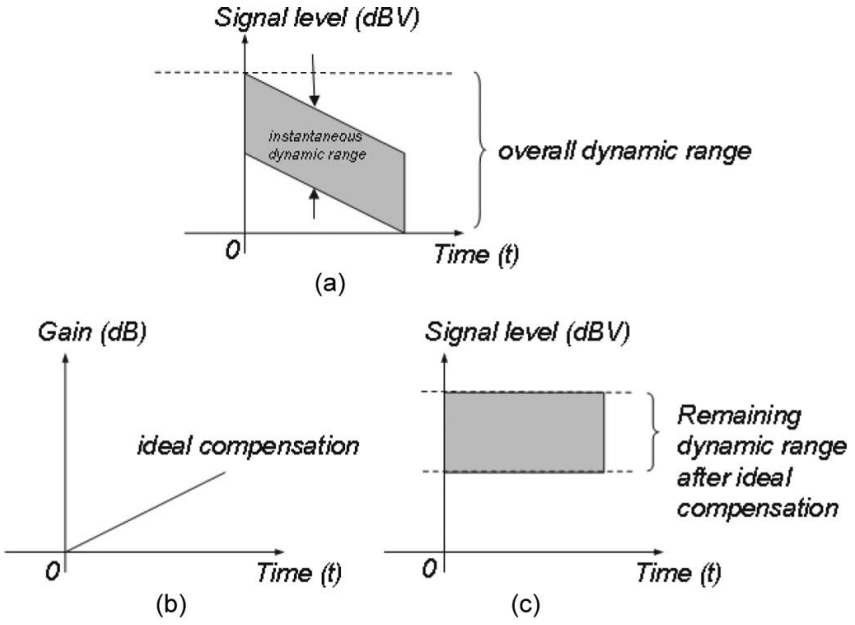


Figure 1.2: Dynamic range echo signal over time: (a) Dynamic range incoming echo signal, (b) Ideal Time Gain Compensation gain, (c) Ideal remaining dynamic range after compensation. [7]

1.4. Motivation

Figure 1.1 shows a typical ultrasound system as is used in literature. It shows that the TGC is placed after the LNA. This is non-desirable for multiple reasons. The first is that the LNA needs to tackle both the noise performance as well as be able to handle the full dynamic range of the attenuating signal. This means that the LNA needs to deal with an input dynamic range larger than 100 dB while maintaining a low noise performance at the cost of high power consumption.

The other reason is that designing a separate TGC amplifier is not cost efficient as it costs both power as well as die area. To reduce both power consumption as well as die area this work aims at combining both the TGC and LNA together in a single amplifier. This changes the receive path in the block diagram of Figure 1.1, which can be simplified to the block diagram of Figure 1.3.

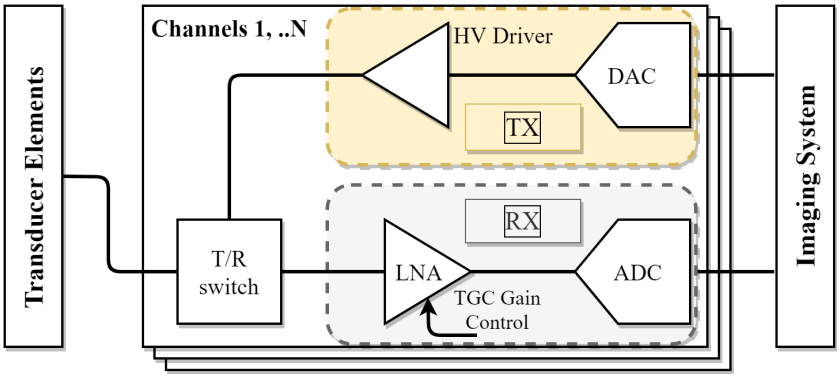


Figure 1.3: Block diagram ultrasound system with combined TGC-LNA amplifier

There are hardly any combined TGC-LNA amplifiers described in literature. [10] shows one such amplifier, although the architecture presented in [10] is too large for miniature 3D imaging probes that have smaller pitch sizes.
There are multiple reasons why TGCs and LNAs have not been combined thus far in literature. It is difficult to combine both the variable gain functionality while maintaining low noise performance. Low noise amplifiers typically have large gains to suppress input referred noise of subsequent components in the receive chain. However, the TGC functionality not only requires high gain for the lowest input amplitudes, but requires smaller gains for the larger input currents. These smaller required gains can lead to noise performance issues. Also while varying the gain a decent bandwidth must be maintained to minimize distortion [8]. Maintaining relatively large bandwidths can cause stability issues. Varying the gain is often implemented by varying impedance values. This can cause certain poles to move several decades in the frequency domain and must be taken care of to maintain stability.

In short, a combined TGC-LNA requires many trade-offs between noise performance, bandwidth, stability and linearity, while the power and area should be kept as small as possible. If these difficulties are overcome, the power and area savings will improve future ultrasound imaging systems.

1.5. Design Requirements

The presented TGC-LNA is designed in TSMC 180nm BCD-Gen2 technology with a 1.8 V supply. To be able to compare the designed TGC-LNA with other works the same capacitive micromachined input transducer as in [10] is used. The target specifications for the combined TGC-LNA are given in Table 1.1 and are based on the characteristics of the input transducer.

The transducer behaves as a resonator with a certain resonance frequency and bandwidth. For the transducer used, this means that the bandwidth of interest is 5-10 MHz with a center frequency of 7.5 MHz. The noise of the input transducer is limited by the impedance of the transducer. The noise specification is given as a spot current noise density at a lower density than that of the transducer to minimize signal to noise degradation. In other words the noise of the transducer should dominate the total noise performance.
Apart from specifications based on the transducer, special care is given to the Total Harmonic Distortion (THD) as linearity issues for TGCs are hardly covered in literature.

Table 1.1: Target performance specifications

Input center frequency	7.5MHz
Bandwidth	5-10MHz
Gain range	40dB
THD	<-40dB
Peak input signal amplitude	$0.5\mu A$ - $50\mu A$
Receive time period	100μs
Input referred noise density	$1\text{pA}/\sqrt{\text{Hz}}$ at 7.5MHz

While designing the combined TGC-LNA die area and power consumption are taken into account. In [10] the die area and power consumption costs are 0.12 mm^2 and 5.2 mW respectively. The aim is to design a TGC-LNA with comparable performance. Therefore choices are made with respect to minimizing both die area as well as power consumption.

1.6. Document Structure

The remainder of this thesis presents the design steps taken for a combined TGC-LNA amplifier for ultrasound imaging applications and is structured as follows. Chapter 2 covers the prior art on existing TGC structures, after which chapter 3 shows the steps taken to converge to a viable architecture for a combined TGC-LNA amplifier. Chapter 4 goes in depth into the different circuit implementations, while chapter 5 shows the obtained performance of this work. Finally, as this work is a proof of concept and does not contain a finished product, chapter 6 outlines the steps that need to be taken to be able to finalize a complete product.

2

Prior Art

The time gain compensation amplifier is a certain type of Variable Gain Amplifier (VGA). The TGC varies its gain as a function of time. Equation (1.1) suggests that incoming signals undergo a dB-linear attenuation over distance. Assuming a constant speed of sound the attenuation is also dB-linear over time, which results in exponentially decreasing input signals over time. As the incoming signals are attenuated exponentially over time, the gain variation over time should ideally also be exponential. A circuit of which the gain varies purely exponentially as a function of time, however, can be difficult to design. In the literature multiple methods have been used for designing amplifiers with TGC functionality.

This chapter aims to categorize the prior art on TGCs, looking into the different existing architectures. For each architecture the advantages and disadvantages are covered and the gap with respect to this work is made clear. There are various ways to categorize the literature on TGCs. There are two main methods to categorize the prior art:

1. Categorization based on architecture type.
2. Categorization based on function implementation.

When categorizing the prior art based on the architecture type, the same architecture type may include different functionalities. The different functionalities are the different methods used for approaching the ideal exponential gain variation. For example a traditional amplifier with multiple feedback paths could have exponentially increasing discrete gain steps or a continuous interpolation between gain steps. A categorization based on architecture type, such as is done in [11],[12],[13], is useful to verify what the capabilities are of different architectures to be able to design a new architecture type.
Categorizing the prior art based on function implementation has the benefit that categorization is done at a higher level. It starts at what the purpose is of the designed circuitry. As multiple architectures can implement the same functionality, a categorization based on functionality allows for a good comparison between the performance of both different functionalities as well as the performance of different architectures for a given functionality.

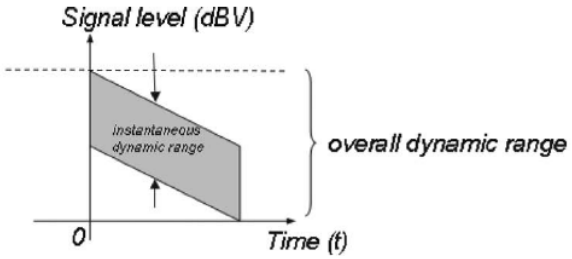
In this chapter the categorization of the prior art on TGCs is done based on the implemented function, in the same manner as is done in [10].
There are two main approaches for designing an amplifier with built-in TGC functionality:

1. TGCs with discrete gain steps
2. TGCs with continuous gain variation

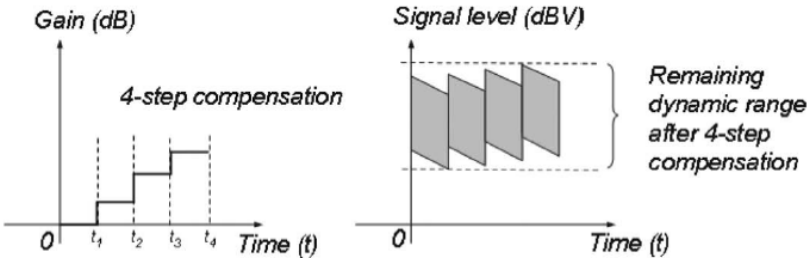
The next few sections cover these two main categories.

2.1. Discrete Time Gain Compensation

Varying the gain with exponentially increasing gain steps is a viable method to approach an exponential function via multiple discrete gain steps. The biggest advantage of using discrete gain steps is that the gain can be



(a) Instantaneous dynamic range input signal.



(b) Discrete gain variations and instantaneous dynamic range after discrete gain steps.

Figure 2.1: Instantaneous dynamic range input signal and output signal of a TGC with discrete gain variation [7].

accurately set by means of relatively simple digital logic. TGCs with discrete gain steps are relatively simple to configure and the gain is accurate.

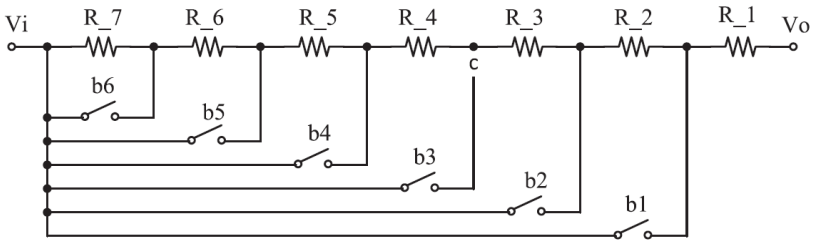
There are, however, a few drawbacks to using discrete gain steps with respect to continuous gain variation. The first drawback becomes apparent in Figure 2.1b. Because the gain is not constantly varying, the instantaneous dynamic range is not completely constant over time. This results in an overall dynamic range that is larger than the instantaneous required dynamic range. The dynamic range requirement for the circuitry is therefore larger than the instantaneous dynamic range of the signal. The difference between the overall required dynamic range and the instantaneous dynamic range reduces with increasing number of gain steps. Increasing the number of gain steps will inevitably result in larger die area and increasing circuit complexity.

Transient artifacts associated with switching are another drawback of using discrete gain steps. These switching artifacts can have adverse effects on the ultrasound image. As the switching is time based and time is proportional to the image depth, switching will produce adverse effects at certain image depths related to gain-switching moments. Larger settling artifacts are expected with larger gain steps. To minimize the negative effects switching artifacts impose it is necessary to create small gain steps.[14][10] Decreasing the gain step size requires an increase in the total number of gain steps, leading to larger die area and increased circuit complexity.

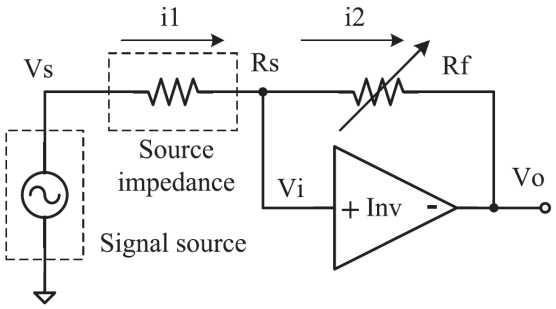
Even though there are some drawbacks to the use of discrete gain steps, it is still useful to view the different existing architectures as discrete variable gain amplifiers are well established in literature. In some cases existing discrete architectures can be converted to continuous gain variation by using analog control signals instead of digital signals.
The next subsection covers the most common architectures for implementing a TGC functionality with discrete gain steps.

2.1.1. Discrete Gain Set By Impedances

Using digitally-programmable impedance networks the gain of discrete TGCs can be accurately defined. The most common impedance networks used are resistive ([7, 8, 15–17]) and capacitive networks ([18–20]). However, networks based on the ratio of transconductances are also used ([11, 21, 22]). To minimize the effects of PVT (Process/Voltage/Temperature) variations on the absolute value of impedance, often impedance ratios are used.



(a) Digitally programmable resistive feedback array



(b) Overall closed loop amplifier with resistive feedback

Figure 2.2: Amplifier with closed loop resistive feedback using a programmable resistive feedback array [17]

In TGC designs both open-loop as well as closed-loop configurations are documented. Figures 2.2 and 2.3 show a closed loop and an open loop respectively for the implementation of discrete gain steps based on resistances. It should, however, be noted that Figure 2.3 does contain local feedback. Both figures have a gain that is based on a resistive impedance ratio. In case of Figure 2.2 the gain is approached by R_f/R_s when the feedforward amplifier gain is large. In case of Figure 2.3 the gain is set by the ratio of the digitally programmable degeneration resistor R_s and the load resistance R_L.

As stated in [7] an open loop amplifier can be beneficial for achieving high bandwidths while maintaining low power requirements. On the other hand, open loop amplifiers may perform lower in accuracy as the gain is often highly influenced by active components.
When using an amplifier in closed loop configuration the added benefit is that both the feedforward and feedback path can be separately designed. This, however, can come at the expense of extra required power.

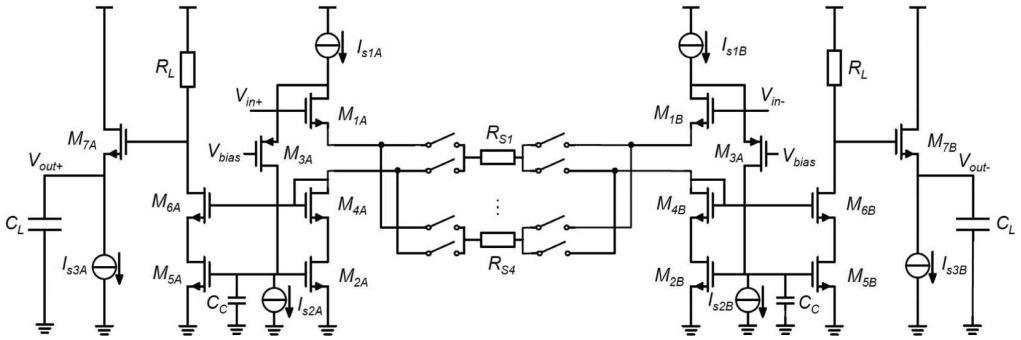
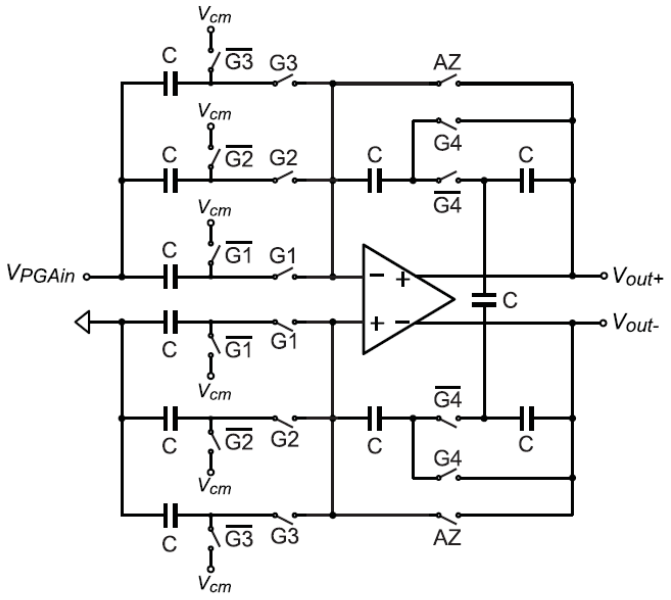


Figure 2.3: Open loop amplifier with digitally programmable degeneration resistors [16][7]

As resistors are inherently noisy, capacitors are also commonly used to set the gain in TGC amplifiers [18–20]. Figure 2.4 shows a fully differential amplifier with a digitally programmable capacitive feedback [19]. Even though capacitors have the added benefit that they are noise free, there is still a trade-off to be made. As on-chip capacitance is quite area expensive, adding multiple gain steps will increase the total required capacitance and die area considerably. Certainly in miniature ultrasound probes this can become an issue.



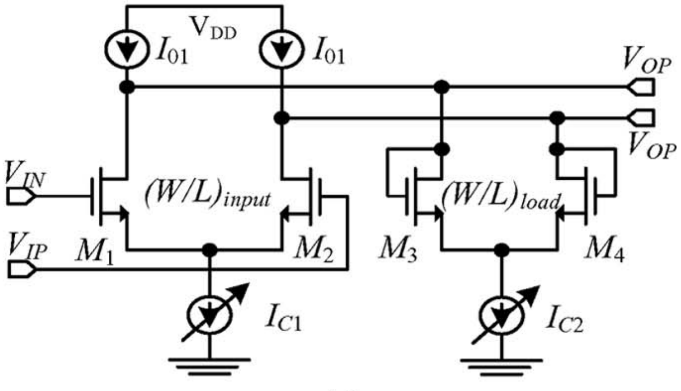
	G1	G2	G3	G4
6 dB	0	1	1	1
12 dB	0	1	0	0
18 dB	0	1	1	0
24 dB	1	1	1	0

Figure 2.4: Fully differential programmable gain amplifier with capacitive feedback, including gain control code map [19]

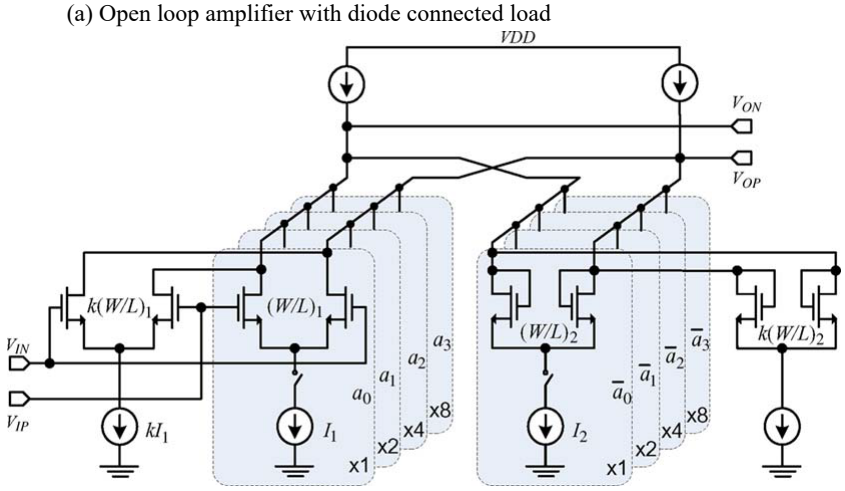
When the operating frequencies are very high and die area becomes an issue, an open loop amplifier with a gain set by the ratio of different transconductances can be utilized [11]. Figure 2.5a shows an open loop amplifier in which the gain is set by a ratio of transconductances as follows:

$$Gain = \frac{gm_{in}}{gm_{out}} = \sqrt{\frac{\frac{W}{L}_{in}}{\frac{W}{L}_{out}} \frac{I_{C1}}{I_{C2}}} \tag{2.1}$$

Again, because the gain is set by a ratio of impedances adverse effects due to process and temperature variations are minimized [11]. As equation 2.1 suggests, the gain can be set by varying the bias current of the transistors. Changing the bias currents by large amounts to increase the total gain range of the amplifier can result in poor linearity performance [11]. For this reason it is useful to not only vary the bias current, but also the W/L ratio of the transistors. Figure 2.5b shows a method for discretely changing both the W over L ratio as well as the bias currents. This leads to a TGC functionality with large possible gain variation while not compromising linearity performance.



(a) Open loop amplifier with diode connected load

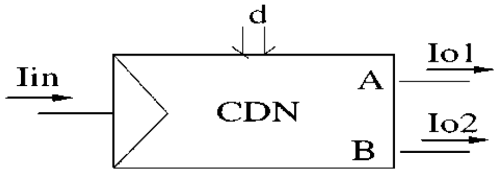


(b) Open loop amplifier with multiple options for different transconductance ratios

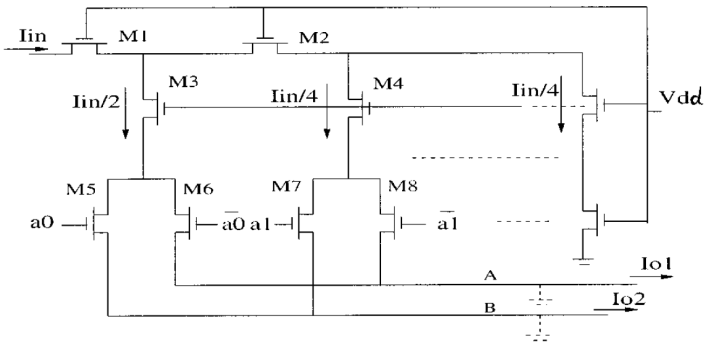
Figure 2.5: Open loop amplifier structures with a gain set by transconductance ratios. [11]

2.1.2. Current Steering

Until now TGCs have been covered that change impedances or impedance ratios to vary the gain in discrete steps. Another approach is not changing the impedances, but changing the current ratio that flows into different impedances [23]. This can easily be done by means of a current steering method as is done in a current division network (CDN), see Figure 2.6. A current division network splits the input current into two different output currents. The ratio in which the input current is divided can be digitally programmed, see Figure 2.6b. Since the ratio between the feedback current and the current flowing into the next stage, I_{o1} and I_{o2} respectively in Figure 2.7, can be changed, the overall gain from input to output can be digitally programmed.



(a) Symbol used for a current division network (CDN)



(b) Schematic of the current division network

Figure 2.6: Discrete closed loop amplifier in which the gain is set by the current division network [23].

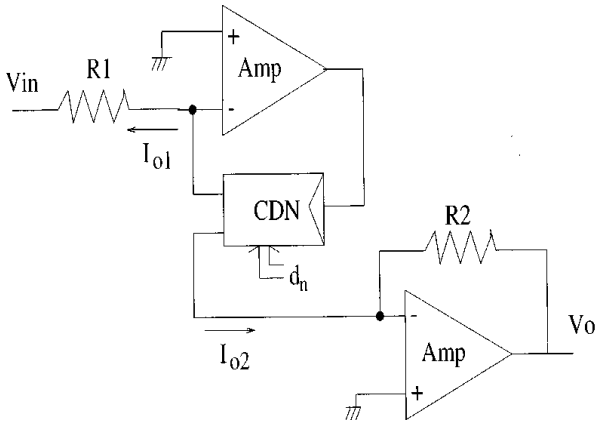


Figure 2.7: TGC with a current division network determining the overall gain [23]

2.2. Continuous Time Gain Compensation

To mitigate the drawbacks of discrete gain steps as mentioned in section 2.1, continuous time gain compensation is required. The aim for continuous TGCs is to use an analog control signal to set an exponential gain curve. Typically the analog control signal is a linearly varying control voltage [10]. As the required gain variation is exponential, using a linear control voltage ideally a linear-in-dB control is created.
This so-called dB-linearity is often used as a performance metric as it shows the gain sensitivity to the control voltage.

There are three main methods used in literature to design continuous time gain compensation amplifiers:

1. Pure exponential functionality: Often relies on inherent exponential properties of components, such as bipolar transistors.

2. Pseudo exponential functionality: An equation that approximates a pure exponential function is implemented.

3. Interpolation functionality: Discrete exponential gain steps are implemented. However, switching is done continuously to create a smooth exponential gain variation over time.

The next subsections cover each of the three different methods.

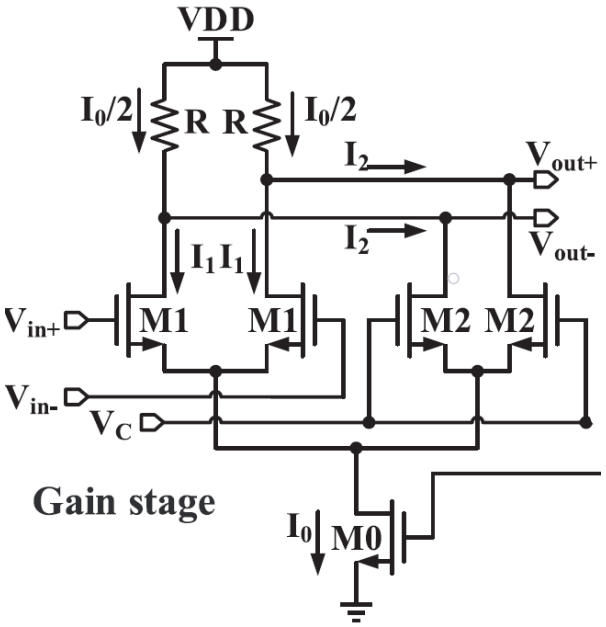
2.2.1. Exponential Functionality

Variable gain amplifiers are not only used for TGC functionality. Often they are also used in Automatic Gain Control (AGC) amplifiers. By breaking the feedback loop of such AGC amplifier topologies and by exchanging the feedback control signal with an independent time varying control signal, the AGC amplifier can be transformed into a TGC amplifier.

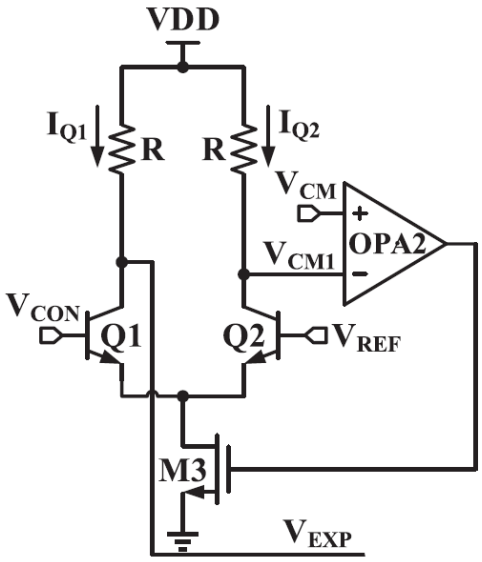
Pure exponential gain control can be achieved by using bipolar transistors [24, 25]. Figure 2.8 shows part of the circuitry that is responsible for a VGA with exponential gain control as described in [25]. The total gain of the gain stage can be written as follows:

$$A = \frac{V_{out}}{V_{in}} = -g_{m1}R = -\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_1}R \tag{2.2}$$

This shows that the total gain is proportional to the square root of the bias current. To create an exponentially varying gain the bias current I_1 has to become an exponentially varying current. One method to create an exponentially varying current based on a linearly varying control voltage is shown in Figure 2.8b. The basic operation is to create an exponential current with the use of bipolar transistors and copy this current as the bias current for the gain stage. The other parts of the circuit shown are used to not only set the bias current, but also to maintain the correct common mode output voltage.



(a) Gain stage with gain controlled by bias current.



(b) Part of bias network responsible for creating an exponential bias current.

Figure 2.8: Gain stage and corresponding bias network responsible for a continuous variable gain amplifier with exponential gain control [25].

If the technology to be used does not have the option to use bipolar transistors, also MOSFET transistors can be used [13]. Using MOS transistors in the subthreshold operating region will result in exponential behaviour. However, if the transistors move out of the subthreshold operating region the exponential gain control is lost. This poses limitations on the total gain range that can be achieved as the currents through the subthreshold devices need to remain limited.

TGCs with purely exponential gain curves are optimal for dynamic range reduction. It comes at the price of having to rely on the inherent exponential properties of certain devices. In some technologies bipolar transistors are not feasible, posing limitations for using those devices. The main drawback that comes from depending on inherent device properties is that those properties are often sensitive to PVT variations. Either these variations are tolerable or PVT variation cancellation circuits need to be designed.

2.2.2. Pseudo Exponential Functionality

The second method of obtaining continuous gain control utilizes pseudo exponential functions. Instead of depending on the inherent properties of for example bipolar transistors a function is implemented that approaches an exponential function in a certain gain range.

Table 2.1 shows a few possible pseudo exponential approximations. The first choice in designing a TGC based on pseudo exponential approximations is choosing the right approximation for the application. To obtain larger gain ranges tradeoffs need to be made. Approximations tend to only be accurate for small ranges. To create larger gain ranges the approximation has to be made more accurate. This solution has the drawback that the approximation becomes more complex and more difficult to implement. Another option is to choose for a simpler approximation to implement and to cascade multiple gain stages. Each gain stage will reduce the overall dynamic range by their respective gain range. This, however, also means that each gain stage with the exception of the last stage has to deal with an overall larger dynamic range than the output signal. The circuits need to be designed in such a way to accommodate for this larger dynamic range.

Table 2.1: A few exponential approximations and their usable gain ranges [26].

Type of approximation	Approximated exponential equation	Obtainable dB-linear range with $\pm$ 0.5 dB error
Taylor series approximation	$f(x) = 1 + x + \frac{1}{2}x^2$	12 dB
Pseudo-exponential approximation	$f(x) = \frac{1+\frac{x}{2}}{1-\frac{x}{2}}$	15 dB
Duong's approximation [27]	$f(x) = \frac{k+(1+ax)^2}{k+(1-ax)^2}$	56 dB
Duong's second approximation [26]	$f(x) = \frac{\sqrt{((b-ax)-c)^2+d}}{\sqrt{((b+ax)-c)^2+d}}$	84 dB

From Table 2.1 it can be observed that most of the approximation equations are based on divisions. One method to create divisions is by making use of an open loop amplifier in which the gain is set by a ratio of input and output transconductances. Figure 2.9 shows such an amplifier. As the input and output devices can be matched, the effect of process variations is minimized.

To control the gain of the amplifier the input and output gm need to be controlled. The gm is highly dependent on the bias current, I_A and I_B in Figure 2.9. Therefore the gain is often controlled by changing the bias currents [26–30]. Depending on the equation to be implemented different strategies can be used. A frequently used component is the differential pair to create both a $1 + x$ and a $1 - x$ current component.

One example of creating the square root function of Duong's second approximation is by applying the control voltage to the body of the differential pair to utilize the body effect. As the body effect, see equation 2.3, is an inherent square root function, the bias currents can be made proportional to a square root function.

$$V_{TN} = V_{T0} + \gamma \left(\sqrt{|V_{sb} + 2\phi_f|} - \sqrt{|\phi_f|} \right) \tag{2.3}$$

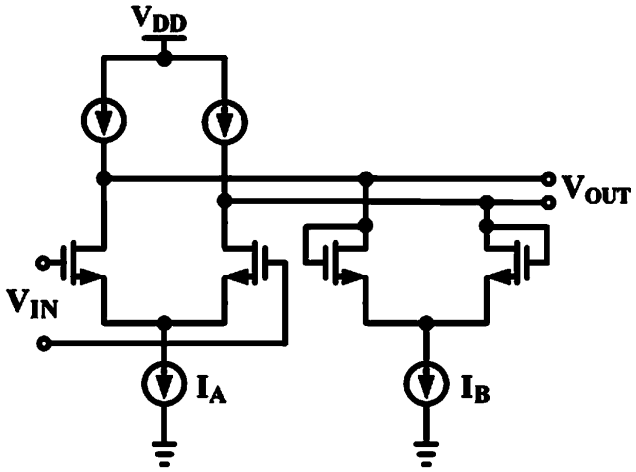


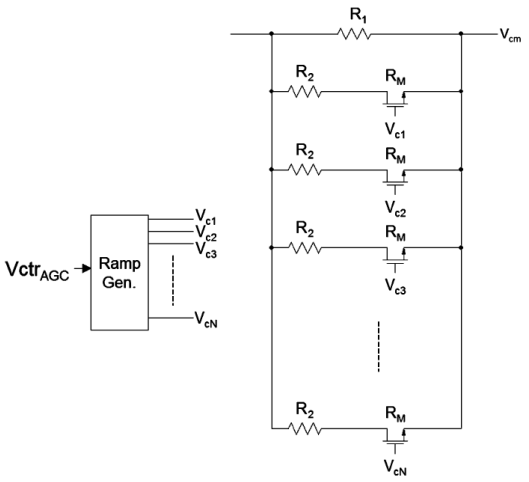
Figure 2.9: General VGA structure often used for pseudo exponential implementations [31].

Not all pseudo exponential amplifiers utilize the open-loop configuration of Figure 2.9. In [4] a closed-loop amplifier configuration is used to design a combined TGC-LNA. It uses a current amplifier with a gain that is proportional to $(1+x)/(1-x)$. However, dynamic range and distortion performance are an issue.

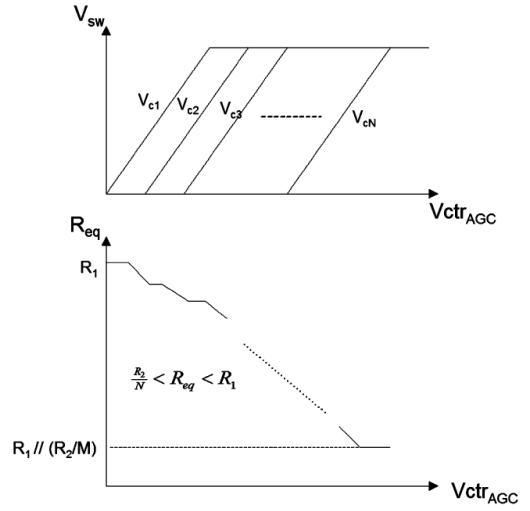
The main advantage of pseudo exponential TGCs is that by means of using divisions the adverse effects of PVT variations are minimized due to matched devices. It is not required to use inherent exponential properties of different components to approximately obtain an exponential gain curve. The main drawback is that the gain range, in which approximations hold, is quite limited.

2.2.3. Continuous Interpolation

The third approach for obtaining an approximated exponential gain curve is by means of interpolating between different discrete gain steps [10, 12, 32, 33]. An amplifier with an extended feedback network is created. For example Figure 2.10 shows an array of resistors. The different switches together with ramping control voltages allow for the equivalent resistance to change continuously. Even though Figure 2.10 does not show a very smooth resistance variation, in [12] it is shown that a smooth curve can be obtained by utilizing sufficient resistances and effectively utilizing multiple switches simultaneously. However, this comes at the price of quite an extensive feedback network. Miniature ultrasound probes may not have enough die area required for such extensive networks.



(a) Array of resistors with multiple switches used for continuously changing the equivalent resistance



(b) Control voltages for different switches and resulting equivalent resistance

Figure 2.10: Array of resistors with corresponding control signals and equivalent resistance [12].

When using a method as used in Figure 2.10, by means of interpolation the effective impedance is changed. Although this is an effective method to alter the gain of an amplifier, another method can also be used to obtain the same results. By means of current steering the point at which feedback is applied is continuously altered [10]. Continuously changing the point at which feedback is applied will also lead to a continuously varying gain. Figure 2.11 shows the proposed combined TGC-LNA of [10]. It shows a capacitive ladder network with multiple nodes at which feedback can be applied. Using the control voltages $V_{GP/N0} - V_{GP/N5}$ the feedback current $G * I_{in}$ can be steered to the different feedback nodes. Allowing for continuous control voltages results in a continuous gain control.

The design proposed in [10] utilizes the same input transducer as this work and also combines both the LNA with the TGC functionality. Therefore the performance requirements of [10] are comparable to the requirements of this work and is used as comparison for this work.

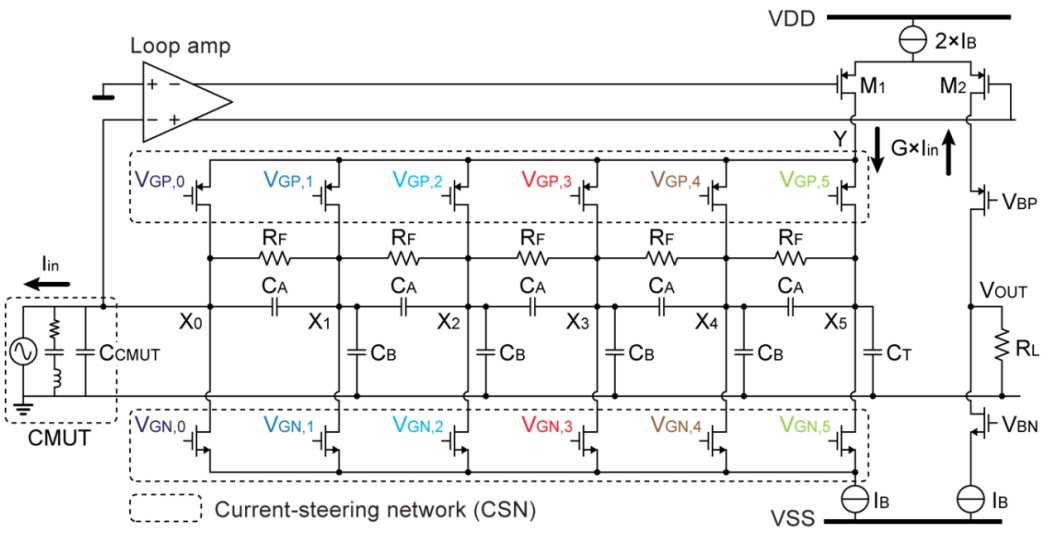


Figure 2.11: Continuous interpolation by means of current steering [10]

2.3. GAP

In the literature the TGC is often placed after the low noise amplifier. This has implications on both the TGC as the LNA. First of all it means that the LNA has to deal with the full dynamic range of the input signal. Extra power is required to handle the large dynamic range.
Regarding the TGC amplifier, the noise specifications are quite relaxed as the input-referred noise of the TGC is reduced by the gain of the low noise amplifier. This means that in the literature the different TGCs are designed without taking noise in consideration.

Designing a separate LNA and a separate TGC amplifier has the advantage that both functionalities can be independently designed from each other. However, there are multiple disadvantages. First the power consumption will be quite high as considerable power is required for the LNA to handle the full dynamic range and for the separate TGC. The second disadvantage deals with die area. As both the LNA and TGC are independently designed it is reasonable to assume that the required die area for designing both amplifiers separately will be larger than to combine both functionalities in a single amplifier. Especially in miniature ultrasound probes die area is a precious resource.

There is hardly literature on combined TGC-LNA designs. In [10] a combined TGC-LNA design is presented. However, due to the interpolation control scheme, combined with a capacitive feedback array the die area is quite large. This work aims at designing a combined TGC-LNA with minimal die area requirements. The covered prior art in this chapter is used as an inspiration for this work.

3

Architecture

The goal of this chapter is to find a suitable architecture for implementing an amplifier with both low noise performance as well as TGC functionality. Starting with the input signal source, the signal is analysed to be able to make the correct decisions regarding the overall amplifier structure.

3.1. Modeling of Input Transducer

The designed TGC-LNA will be the first component after the transducer in the receive path of acoustic echo signals with the exception of the often implemented Transmit/Receive switch (TR switch). It is therefore necessary to carefully look into the properties of the transducer and the effective electric loading it poses to the input of the amplifier to be designed.

The transducer used in this work is a Capacitive Micromachined Ultrasound Transducer (CMUT). To model the electrical impedance of the CMUT the generalized van Dyke model is used [34] as is shown in Figure 3.1. The model shows a capacitive branch and a resonator branch. The natural operating frequency range of the transducer is around the resonance frequency.

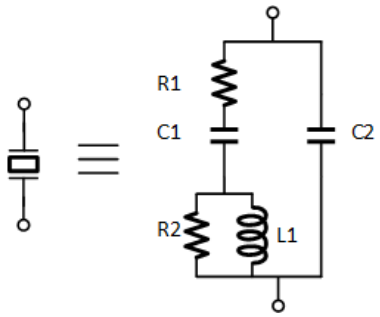


Figure 3.1: Generalized Van Dyke model used to model the input CMUT transducer

Table 3.1 shows the electronic parameters used for the van Dyke model. The intended operating frequency range is centered around the 7.5 MHz. In appendix A.1.1 the transducer impedance around the center frequency is computed to be approximately 1.2 kΩ. This is a relatively large impedance for regarding the input signal source as a voltage source. Therefore the input signal is modelled as an input current.

In this work often only the large capacitor named C_{in} is shown together with a current source as the model for the CMUT. This is done for two reasons. The first is to make circuit diagrams simpler and clearer to the reader. The second is that the total impedance of the input transducer is dominated by the large capacitor.

Table 3.1: Model parameters of used CMUT

Component	Value
R_1	1.1 mΩ
R_2	16.9 kΩ
C_1	2.38 pF
C_2	17.62 pF
L_1	3.1 mH

3.2. Transimpedance Amplifier

As explained in the previous section the input signal source is modelled as a current source. However, most of the components after the TGC-LNA will handle voltage inputs. That means that there needs to be a current to voltage conversion somewhere in or before the amplifier to be designed.

Open loop amplifiers are often used in literature for pseudo exponential TGC amplifiers, see section 2.2.2. Still they pose a few drawbacks with respect to amplifiers with feedback. First of all most open loop amplifiers are voltage amplifiers, requiring a current to voltage conversion before the TGC. When instead of using a voltage amplifier the input current is injected into the open loop amplifier in the same path as the bias current, it may be difficult to create a bias current that achieves both the required noise performance as well as handle the dynamic range of input currents, due to the very large input dynamic range.

The second drawback is that in open loop amplifiers both the noise performance as well as the gain must be handled by the same devices. Regarding amplifiers in feedback configurations the different performance metrics can be separately designed for. When designing the feedback path the gain can be accurately determined and while designing the feed forward path both noise, bandwidth and distortion can be taken into account, which simplifies the TGC-LNA design.

Compared to open loop amplifiers, amplifiers in feedback configuration tend to use more power as more power is required for a high feed forward gain to accurately set the overall gain. The big advantage, however, is that using a feedback topology both the TGC and LNA function can almost separately be designed. For this reason a closed-loop TIA is designed in this work.

The general topology that is designed in this work looks like the shown TIA in Figure 3.2. When the feed-forward gain A is large enough the total transimpedance gain will be dominated by the feedback impedance Z_{gain}. If the feedback impedance value varies exponentially as a function of time the TGC functionality is implemented.
For this reason the design process is divided into three steps. First the feedback impedance is designed. Secondly the feed-forward amplifier is designed, after which the two are combined for the final step.

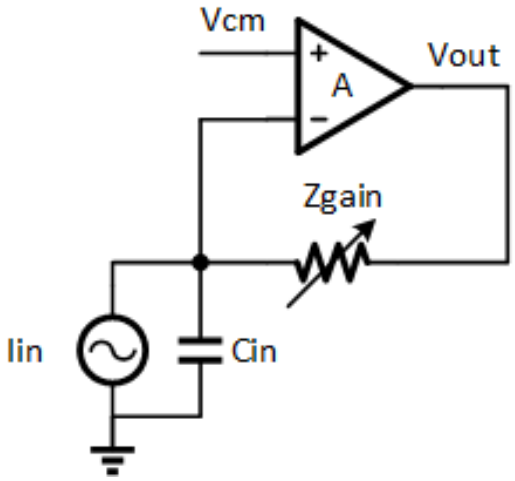


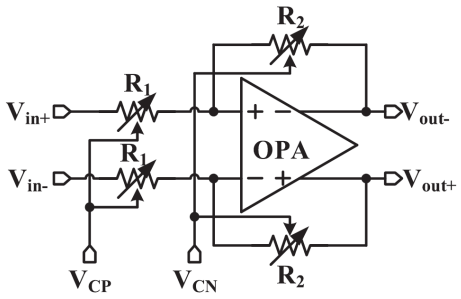
Figure 3.2: General idea of low noise transimpedance amplifier with included TGC functionality

3.3. Feedback Impedance

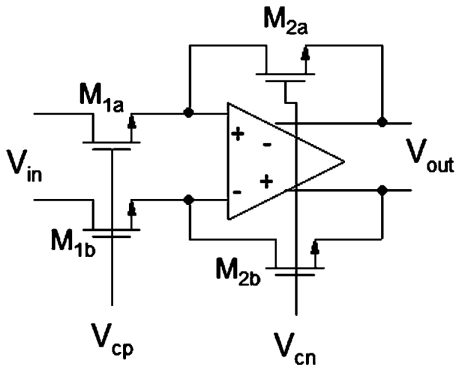
As stated in chapter 2 the ideal gain should be an exponential function of time. Given the TIA topology the ideal gain would be set by a feedback impedance with an exponential dependence on time. This section aims at finding an impedance that can change its value exponentially over time.

Small size TGC amplifiers are crucial for being able to produce pitch-matched receive circuitry. Pitch-matched means that the circuitry required for reading out a single transducer fits underneath the area that the same transducer occupies on the custom ASIC. It is, however, difficult to obtain both small readout circuitry and reasonable power consumption for 2-D transducer arrays [19]. The small usable area has a direct impact on what devices can be utilized and what devices should be avoided as much as possible.

Capacitors are components that occupy quite a large area. For example the TGC as proposed in [10] occupies 0.12 mm^2 using a capacitive feedback array. This is much larger than the pitch sizes for 2D-arrays as posed in [19], where the size of an individual transducer element is about 0.0225 mm^2. It is generally known that capacitors occupy quite a bit of area on an ASIC and are therefore avoided as much as possible in this work.



(a) Pseudo exponential voltage amplifier using varying impedances



(b) Mos transistors used as controllable pseudo resistors

$$R_M = \frac{1}{K(V_{GS} - V_T)}$$

$$A_v = \frac{R_{m1}}{R_{m2}} = \frac{R + \Delta R}{R - \Delta R} = \frac{1 + \frac{\Delta R}{R}}{1 - \frac{\Delta R}{R}}$$

$$\frac{1+x}{1-x} \cong e^{2x} \quad \text{for} \quad x \leq 0.6$$

(c) Corresponding equations for individual resistances and overall pseudo exponential gain

Figure 3.3: Pseudo exponential gain control using MOS transistors as pseudo resistors [12]

Fundamentally a controllable impedance is required. In Figure 3.3 MOS transistors operating in the triode region are used as controllable resistors. The impedance of the triode devices is inversely proportional to the overdrive voltage and can be expressed as:

$$R = \frac{1}{K\left(V_{GS} - V_T\right)} \tag{3.1}$$

Suppose that the overdrive voltage is an exponentially decaying voltage, the impedance of the triode device will increase exponentially. Figure 3.4 shows the general idea of a MOS triode device with exponential control as the feedback impedance in a TIA.

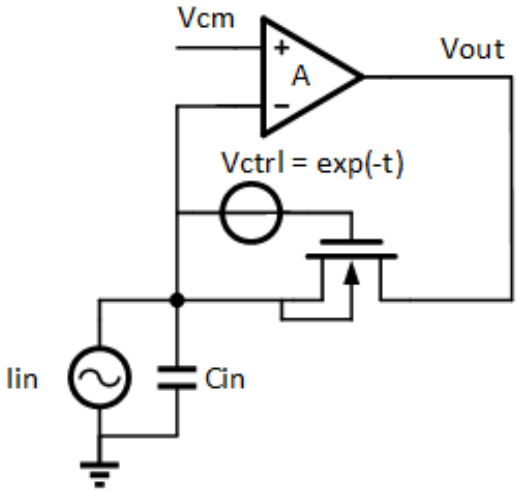


Figure 3.4: Using a MOS transistor with exponentially decaying overdrive voltage in the triode operating region to create an exponentially increasing impedance

This TIA topology poses some issues that need to be solved:

- First of all the linearity and gain range for a triode device must be looked into.
- Next a convenient method for creating a floating overdrive voltage needs to be created.

The following sections deal with these two issues.

3.3.1. MOS Resistance

The MOS transistor has multiple operating regions. It is important that the transistor operates in the right operating region to obtain the required results. For transistors to operate as controllable resistors they should operate in the triode region, where the drain current can be expressed as in [35]:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \tag{3.2}$$

In this equation I_D represents the drain current, μ_n the electron mobility in a N-channel MOSFET, C_{ox} the gate oxide capacitance, $\frac{W}{L}$ the transistor aspect ratio, $V_{GS} - V_T$ the overdrive voltage applied to the transistor and V_{DS} the drain-source voltage of the MOS device. If the conditions are met for the triode operating region and if second order effects are neglected the drain current has a quadratic dependency on the drain-source voltage. Unless the quadratic term becomes insignificant the quadratic term will introduce a significant second order distortion.
If the drain-source voltage is kept small in comparison to the overdrive voltage, suppose in (3.2) $V_{DS} < 2 (V_{GS} - V_T)$ [35], then we have:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} \tag{3.3}$$

In this case the transistor can be seen as a resistor with a value that is expressed as:

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} \tag{3.4}$$

By controlling the overdrive voltage the on-resistance of the MOSFET can be controlled.

It is important to note that a linear resistance can only be achieved in deep triode region, meaning that the condition $V_{DS} < 2 (V_{GS} - V_T)$ should be maintained at each time instant. If not, as stated, the quadratic term will introduce second order distortion. Or worse, when the drain-source voltage becomes larger than the overdrive voltage the MOS device enters the saturation region and there is no longer a direct dependency between the drain-source voltage and the drain current. This becomes clear from the saturation current:

$$I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \tag{3.5}$$

When the operating region goes into saturation the link between output voltage and input current is lost and therefore the data will be lost.

The deep triode condition is expressed as:

$$\text{Deep triode condition:} \qquad V_{DS} < 2\left(V_{GS} - V_T\right) \tag{3.6}$$

and poses limitations on both the minimal possible overdrive voltage and the maximum output swing. A trade-off presents itself between extending the possible resistance range of a transistor and its linearity performance.

3.3.2. Improved Linearity MOS Resistance

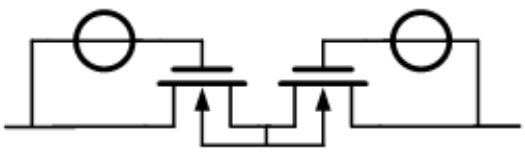
Before any decisions can be made about the minimal possible overdrive voltage and the maximum output swing, the optimal configuration for creating MOS transistors needs to be looked into. The on-resistance, see (3.4), only is a constant value if the independent parameters are constant. However, the threshold voltage can become a non-constant function of the drain-source voltage due to the body effect.

Consider the transistor configuration of figure 3.4. The input current is a pure AC current and no DC bias current is added to keep the drain-source voltage at a minimum. The body effect can be expressed as follows:

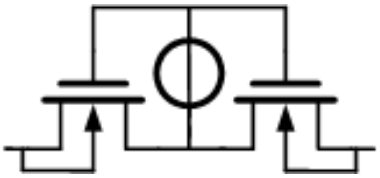
$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{3.7}$$

Considering only first-order effects the only parameter that can change as a function of the drain-source voltage is the source-bulk voltage V_{SB}. If V_{SB} is constant the threshold voltage will remain constant and therefore the MOS resistance will be very linear. As only AC current flows into the triode device the side with the lowest potential will change over time. Effectively this results in the drain and the source switching positions each half period. Even when the bulk in Fig 3.4 is connected to either side of the MOS device, the bulk only tracks the source for half a period each cycle. Using this configuration the on-resistance will be constant for a half period and will change during the other half of the period. The overall output will suffer from non-linearity.

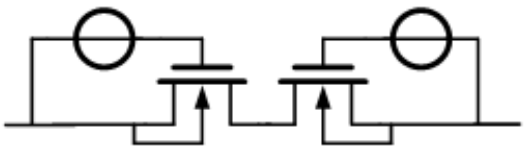
To improve the linearity of the MOS device for the duration of a complete period the configuration of MOS devices must be altered. One method of reducing the non-linearity is to make the resistance change for both positive as well as negative input currents equal. This can be done by using two MOS devices in series and connecting the bulk on opposite sites, as is shown in Figure 3.5. There are four different possibilities for connecting the bulks on opposite sides and choosing which node the floating source/sources will track. On the other hand, there are only 2 different configurations with respect to the linearity performance. Either the bulks and floating sources are connected on the same sides, or they are connected on opposite sides. The configurations in Figures 3.5a and 3.5b are essentially the same as the two MOS devices have simply shifted position. The same goes for 3.5c and 3.5d.



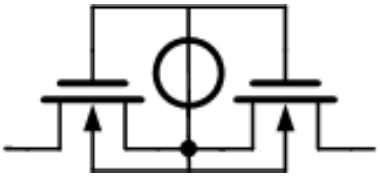
(a) Triode devices with bulks connected to the middle node, floating sources connected to the outer nodes



(b) Triode devices with bulks connected to the outer nodes, floating source connected to the middle node



(c) Triode devices with both bulks and floating sources connected to the outer nodes



(d) Triode devices with both bulks and floating source connected to the middle node

Figure 3.5: Triode MOS devices configuration for increased linearity, variation of resistance used in [5]

Looking into possible die area required for designing the different configurations a choice can be made for which two configurations have the most potential for implementation. Floating sources are often implemented using capacitors and the amount of capacitors are to be minimized. It is expected that the area required for implementing a separate well for changing the bulk connection is smaller than the area required for implementing the floating source. This assumption is based on the relative small sizes of the triode devices for implementing high resistances. These small transistors will therefore also require relatively small separate wells.

Minimizing the amount of floating voltage sources leaves the configurations 3.5b and 3.5d. In this work configuration 3.5b is implemented, because it proved to have less distortion issues, due to the well balanced architecture.

3.4. Obtaining 40 dB Gain Range

3.4.1. Determining Output Voltage Swing

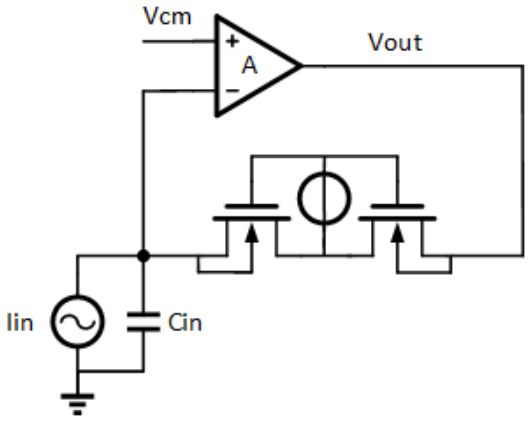


Figure 3.6: Transimpedance amplifier with pseudo resistor configuration

With Figure 3.6 chosen as the configuration for the controllable resistor the trade-off between determining the minimal overdrive voltage and maximum output swing can be made. The main goal is to maximize the possible gain range, while minimizing non-linearity.

The TGC-LNA is designed in a 0.18 μm BCD CMOS process with a 1.8V supply. The transistors used are 2V devices limiting the maximum possible control voltages. Considering the TIA of Figure 3.6 not only the maximal output swing and minimal overdrive voltage, but also a common mode voltage V_{cm} needs to be determined. This V_{cm} acts as both the DC input and output voltage of the amplifier and must be chosen with care, such that all transistors in the loop amplifier will operate in saturation region. V_{cm} should be chosen as low as possible to allow for the largest possible control voltage range leading into the largest possible gain range. In this work the common mode voltage is set to $V_{cm} = 0.5$ V to allow enough headroom for a single cascoded loop amplifier.

For determining the maximum allowable voltage swing multiple things are taken into account. First of all the minimal allowable resistance regarding current noise must be computed. Secondly the maximal swing for allowing the loop amplifier to work correctly needs to be determined. Finally the trade-off between maximizing both output swing and gain-range must be made.

The noise specification for the TGC-LNA is such that the total output noise is dominated by the input transducer and not by the TGC-LNA. The noise specification, as set in section 1.5 and elaborated in 3.1, is set as an input referred current noise density of 1 pA/$\sqrt{\text{Hz}}$ for the smallest input current. The total pseudo MOS resistor will be noisy in the same way as a normal resistor, resulting in a current noise density of:

$$i_n = \sqrt{\frac{4kT}{R}} \quad \left[\frac{\text{A}}{\sqrt{\text{Hz}}}\right] \tag{3.8}$$

Where i_n is the current noise density, k the Boltzman constant, T the temperature in Kelvin and R the effective resistance. If the complete noise density is originating from the resistance the minimal resistance is computed to

be $R_{min} = 17.1$ kΩ. As the intended environment for the transducer is inside a human body, the temperature in (3.8) is set to body temperature (37 °C, or 310.15 K).

The minimal resistance should be multiple times larger than the computed 17.1 kΩ to leave room for noise originating from the loop amplifier. Also the maximum output amplitude will be quite small using a 17.1 kΩ resistor. With the smallest input current amplitude being 0.5 μA, the output amplitude will be $0.5\mu\text{A} * 17.1\text{k}\Omega = 8.6$ mV. It is reasonable to expect the noise coming from the loop amplifier to be much larger than the noise coming from the pseudo resistor. Therefore, to leave approximately 90% of the noise budget for the loop amplifier the maximum resistance should be about 100 kΩ. This would result in an output amplitude of 50 mV, the same amplitude used in the TGC-LNA as proposed in [10].

With a 50 mV swing there is still enough headroom at the output to keep a possible cascoded output stage in saturation. Regarding the trade-off between obtainable output swing and gain range, the output swing can be increased with subsequent amplifier blocks, however the total gain range should be settled within the TGC-LNA. Therefore it is desirable to attribute a higher importance to obtainable gain range than obtainable output swing. It is therefore decided that, based on the noise analysis and maximizing the gain range, the output swing is maximally 50 mV.

3.4.2. Achievable Gain Range Single Branch

The total gain range should be 40 dB with an output voltage amplitude of 50 mV. Using the given input current specifications, see section 1.5, the required resistance range can be computed. The input current amplitude decreases exponentially over time from 50 μA to 0.5 μA, resulting in a required exponential resistance increase from 1 kΩ to 100 kΩ.

To obtain the potential gain range of a single pseudo resistor as in configuration 3.5b, the range in overdrive voltages need to be computed. Given the output voltage amplitude of 50 V the maximum drain-source voltage should be 50 mV. Using the deep triode operating region condition, see 3.6, the minimal overdrive voltage $(V_{GS} - V_T)$ is 100 mV. The maximum gate voltage determines the maximum overdrive voltage possible. The maximum gate voltage is either the 1.8V supply voltage or 2V higher than the lowest possible transistor terminal potential, since they are 2V devices. Gate voltages higher than the supply voltage can be achieved by using charge pumps or connecting a pre-charged capacitor between two different nodes.

The maximum gate voltage is between 1.8 V (supply voltage) and 2.45 V (0.5 V common mode voltage minus the output amplitude). Assuming a threshold voltage of about 550 mV and setting the maximum output voltage to $0.5V_{cm} + 0.05V_{signal} = 550$ mV the maximum possible overdrive voltage is computed as follows:

$$(V_{GS} - V_T) = 1.8\text{ V} - 0.55\text{ V} - 0.55\text{ V} = 0.7\text{ V} \qquad \text{(using 1.8 V supply voltage)}$$
$$(V_{GS} - V_T) = 2.45\text{ V} - 0.55\text{ V} - 0.55\text{ V} = 1.35\text{ V} \qquad \text{(using 2.45 V as maximum gate voltage)}$$

Since the MOS resistance is inversely proportional to the overdrive voltage, the range in overdrive voltage equals the resistance range for the pseudo resistor. With the maximum and minimum overdrive voltages known the resistance can change by:

$$\frac{V_{GT_{max}}}{V_{GT_{min}}} = \frac{0.7\text{ V}}{0.1\text{ V}} = 7 = 16.9\text{ dB} \qquad \text{(using 1.8 V supply voltage)}$$
$$\frac{V_{GT_{max}}}{V_{GT_{min}}} = \frac{1.35\text{ V}}{0.1\text{ V}} = 13.5 = 22.6\text{ dB} \qquad \text{(using 2.45 V as maximum gate voltage)}$$

Even though the gain range can be extended by almost a factor 2 when using charge pumps, both the gain range using the 1.8 V supply voltage as well as the gain range using the 2.45 V gate voltage do not suffice the specified 40 dB gain range. A method for increasing the gain range needs to be designed.

3.4.3. Extending the Gain Range: T-Network

Before extending the gain range a method can be designed for extending the overall gain or increasing the output voltage swing without increasing the drain-source voltage of the triode devices.
A T-network is often implemented for increasing the voltage gain in an amplifier in exchange for higher power

consumption. Figure 3.7a shows what a typical T-network would look like when used in combination with a variable pseudo resistor. The overall gain from input current to output voltage is written as follows:

$$\frac{V_{out}}{I_{in}} = R_1 + \frac{R_1 R_3}{R_2} + R_3 \tag{3.9}$$

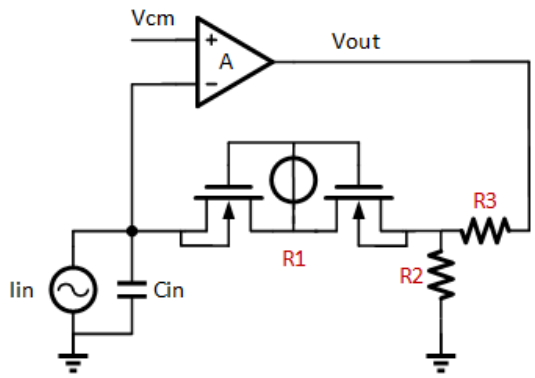
Using this T-network requires R_2 and R_3 to be small in comparison to R_1 so that the overall gain is dominated by the varying pseudo resistor. If this is not the case, a 10X variation in R_1 will no longer result in a 10X variation in gain, leading to a smaller gain range. Suppose $(R_2 \ll R_1)$ & $(R_3 \ll R_1)$ the gain can be expressed as:

$$\frac{V_{out}}{I_{in}} \approx R_1 + \frac{R_1 R_3}{R_2} \tag{3.10}$$

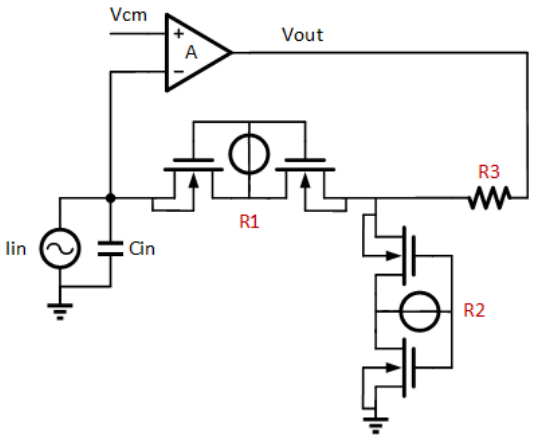
In this case the effective feedback resistance R_1 is increased with a factor of $\left(1 + \frac{R_3}{R_2}\right)$. With a fixed R_3/R_2 ratio the overall gain range is not increased. Only the output voltage swing is increased. Having said that, if the ratio of R_3/R_2 is also changed over time together with R_1 the gain range can be extended.

The ratio of R_3/R_2 can be changed if for example R_2 is also a varying pseudo resistor, as is shown in Figure 3.7b. To obtain a higher gain range over time R_2 should decrease. It is less effective to increase R_3 over time as the condition that both R_2 and R_3 need to be small in comparison to R_1 has to hold.

Even though Figure 3.7b shows a method of increasing the gain range there are some significant drawbacks to using this configuration. First the control voltage of both R_1 and R_2 need to be different from each other. In addition the control voltages can no longer be pure exponential functions as the overall gain will no longer be an exponential function.
Secondly the resistance change in R_1 is not altered. This means that the total resistance range of R_1 is in the order of 17-22 dB. Still R_1 needs to be able to handle the full 40 dB input current change, which will lead to linearity issues.
It is for this reason concluded that a T-network is only optional to increase the output voltage swing, but not for extending the gain range of the TGC-LNA. Another method for increasing the gain range must be used.



(a) T-network for increasing the gain with a fixed output swing increase



(b) T-network for increasing the gain range

Figure 3.7: Different implementations of a T-network to either increase the output voltage swing or extend the gain range

3.4.4. Extending the Gain Range: Multiple Branches

The total gain range of a feedback network with a single pseudo resistor is limited to about 17-23 dB. Using multiple branches where each branch operates on a different part of the gain range can increase the total gain range. The minimal number of branches required for a gain range of 40dB is three when the supply voltage is used as the maximum gate voltage. When gate voltages above the supply voltage are allowed the theoretical minimal amount of branches for achieving a 40 dB gain range is reduced to two. Still, it is better to use three branches. This is because sufficient gain overlap is required between different branches to account for a smooth

transitioning between different branches.

Figure 3.8 shows a TGC-LNA which utilizes three different branches. Each branch has differently sized pseudo resistors in such a way that the total 40 dB gain range is obtainable with the correct switching mechanism.
The next section deals with the mechanism to change between different branches.

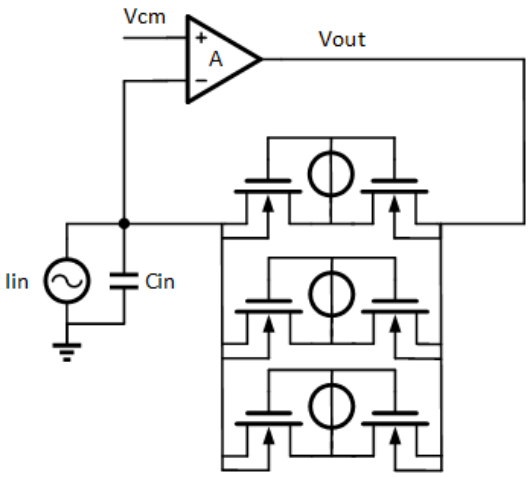


Figure 3.8: Using multiple branches with pseudo resistors to extend the gain range

3.5. Branch Switching

Ideally each of the three different branches of Figure 3.8 operates on a separate interval of the total gain range. For the correct functioning of the transimpedance amplifier a switching method between different branches is required. This section deals with two separate methods for switching between the different branches: An explicit switching method and an implicit one.

3.5.1. Explicit Switching

By means of explicit switching the different branches are connected between the input and output during active operation and disconnected when the branch should be inactive. This can be done by using switches for each branch. This method will require multiple control signals as each switch needs its own control.

A way of implementing explicit switching is by means of utilizing voltage followers, as shown in Figure 3.9. The voltage follower only operates as a voltage follower if the active devices get enough bias current. If the bias current for the voltage follower becomes very small it no longer functions properly and can be seen as a very high impedance, effectively disconnecting the corresponding branch from the output.

Steering the bias current from one voltage follower to another can be smoothly done by means of a current steering principle, as is demonstrated in [10]. When current steering is applied, there is a smooth transition from one branch to the other branches and after a transition only one branch is connected.

There are multiple advantages of using voltage followers and a current steering method. First of all the total gain range can be evenly split between different branches and each branch can individually be optimized. This is the case as for most of the time only a single branch is connected to the output. During transition, however, multiple branches are connected to the output and the overall gain is set by the parallel connection of resistances. This does not need to form a problem as each branch can handle a larger gain range than required for the total specified 40dB.
The second advantage is that the DC output voltage is increased by a single gate source voltage. This will give the loop amplifier more headroom and simplifies its design.

There are also a few significant drawbacks for using voltage followers and the current steering method. First adding a bias current for the voltage follower means adding a current source with direct connection to the input,

which can significantly increase the input-referred current noise. Secondly the added bias sources result in higher power consumption, which is undesirable. Also multiple different control signals need to be created. Not only for the pseudo resistors of each branch, but also for the current steering between the different voltage followers. Finally the added voltage followers will add circuit complexity and also distortion.

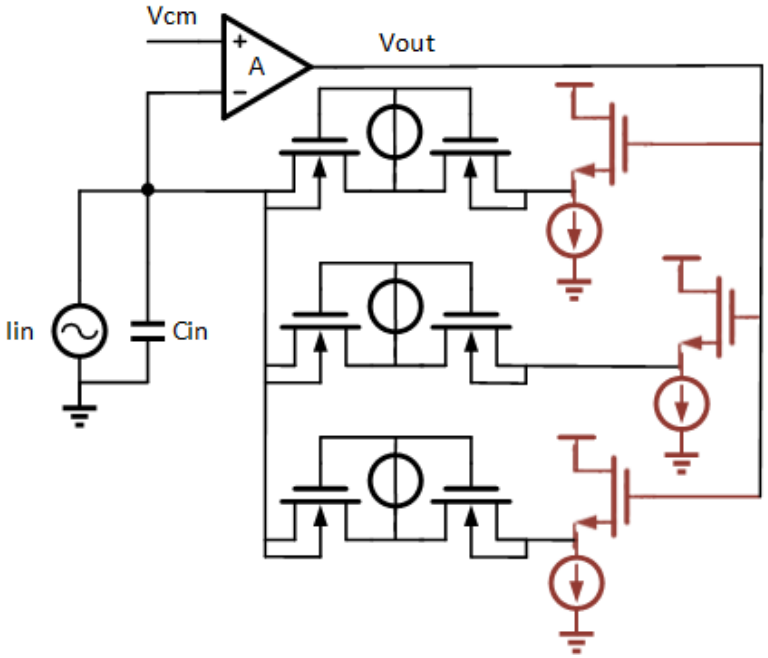


Figure 3.9: Explicit switching method by means of utilizing voltage followers

3.5.2. Gain Control (Impedance Steering)

As there are multiple significant drawbacks to using an explicit switching method for switching between branches, an implicit switching method is introduced. By implicit switching it is meant that no switches are being implemented, but the resistance from each branch will determine which branch is the dominating/active branch.

Going back to the configuration of Figure 3.8, the multiple branches can be seen as a parallel connection of resistances. The total resistance and thus the gain is set by the overall parallel resistance. This overall resistance is dominated by the smallest individual parallel branch. If the resistance of a certain branch is the smallest resistance for the intended resistance range of said branch, than the other branches do not have to be disconnected.

Implicit branch switching can be achieved by continuing the increase in resistance for a certain branch, even when its intended gain range is already achieved. This can be done by continuing the decrease of the gate-source voltage. Eventually this turns the triode devices off, which greatly increases the resistance of that particular branch.
If the control voltages for the different branches decrease at different rates slowly the smallest-resistance/dominating branch is smoothly switched.

3.6. Control voltage generation

This section covers the design of the control signal generation circuitry. There are multiple methods for generating the control voltage. First the nature of the control signal must be determined. As covered in section 3.3 the control signal should be an exponential decaying gate voltage in case of a single branch of pseudo resistors. Even with multiple branches, each control signal will still have to resemble an exponential decaying gate voltage. This is because of the implicit switching that is utilized, causing the overall impedance to be dominated by just a single branch for most of the receiving period.

There are mainly two ideas for setting the control voltage to obtain the desired gain curve. The first is to utilize a type of automatic gain control circuit to set the gain exactly to the required gain by means of a feedback network.

The second is to use a fixed control voltage function that does not require the gain to be measured and compared to the required gain in a feedback configuration. This would ideally make this type of control voltage design less complex and less prone to stability issues, since there are less control loops to be taken care of.

The gain control should be designed in such a way that the gain curve will have the following performance attributes:

- The gain range should span 40 dB
- The gain range/impedance range should span from 1 kΩ-100 kΩ
- The 40 dB gain variation should happen within the receive period of 100 μs

3.6.1. Feedback Loop

To set the gain to a desired gain curve a type of automatic gain control can be utilized. By comparing the obtained gain with the desired gain a feedback topology is possible to minimize the difference between the desired and obtained gain. There are three main ingredients required for creating the control feedback.

1. A method for measuring the gain
2. A method for designing the desired gain curve
3. A method for combining the information of the obtained gain and the desired gain in a feedback topology

Equation (3.4) shows that the on-resistance of the triode devices is inverse proportional to the overdrive voltage. As the gate-source voltage of the triode devices is the overdrive voltage shifted with a DC threshold voltage the gate-source voltage can be used as a measurement for the obtained gain.

A topology that can be used to obtain the desired gain curve is shown in Figure 3.10. Here the MOS device is a copy of the MOS devices in the main TIA. To keep the MOS device in the same triode operating region a small drain-source voltage is required. The loop amplifier will set the drain-source voltage to a DC reference voltage V_{ref}. This reference voltage is chosen to be very small, comparable to the output voltage swing of the TIA.
The gain curve can be set by changing the drain current of the triode device. Suppose the current source in Figure 3.10 is an exponentially decreasing current, then the on-resistance should increase exponentially to keep the drain-source voltage at a constant V_{ref} level. The control voltage V_{ctrl} is the gate-source voltage that provides the desired gain. This means that this control signal should be compared to the measured gate-source voltage of the TIA in a feedback topology.

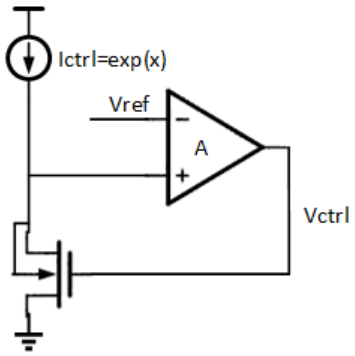


Figure 3.10: Topology for obtaining the desired exponential gain curve

With the topology of Figure 3.10 there are two issues that need to be tackled. First the current source needs to be an accurate exponential current source. This is because the accuracy of the current source is directly related to the accuracy of the gain control. Second the topology shown works nicely with a single branch, however multiple branches are required to achieve the total 40 dB gain range. To control the different branches multiple different control signals are required, which cannot be done using a single loop amplifier in the setting as used in Figure

3.10.

To solve these two issues the topology of Figure 3.11 is introduced. The exponential current source is implemented using a bipolar transistor, which inherently will have an exponential current behaviour. This also enables the control signal of the bipolar transistor to be a linear ramp signal that can be easily generated by means of an integrator.
To tackle the issue of a single loop amplifier while using multiple branches the idea of utilizing offset voltages is introduced. First a copy of all different triode devices of the multiple branches is placed in the control generation circuit. The idea is to not control each branch individually, but to control all the branches simultaneously with the same control circuit. This is necessary to obtain the correct gain curve even during the transition between branches. The offset voltages are used to obtain three different control voltages. To this end two floating voltages are required that can be implemented for example by pre-charged capacitors.

The reason constant offsets are introduced has to do with the impedance switching. Each control voltage is an exponential decaying function of time. The offset voltages can be chosen in such a way that the impedance switching happens each time around the deep triode condition of an overdrive voltage of around 100mV.

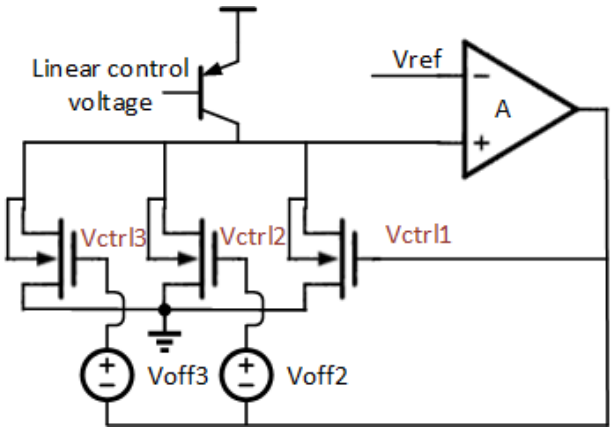


Figure 3.11: Method of creating multiple control signals with a single loop amplifier.

With both a method for measuring the obtained gain and for generating the control signals a feedback topology is required for setting the correct gate-source voltages. Figure 3.12 shows a possible topology for a feedback circuit that combines the gate-source measurement together with the desired gain control signals. Using a buffer and a loop amplifier the gate control signal is compared to the gate-source voltage generated by the control circuit, see Figure 3.11. The error is fed back to the loop amplifier, which drives the gates of the triode devices.

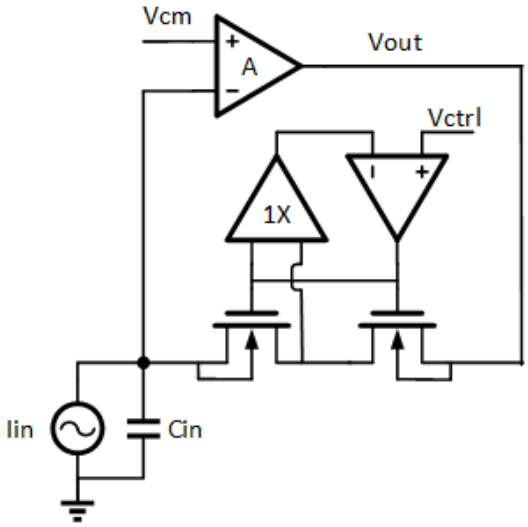


Figure 3.12: Feedback topology for automatic gain control

Using this topology the TGC will have an accurate exponential gain curve. However, there may be practical limitations of using this method. Adding buffers and loop amplifiers for each branch will result in increased circuit complexity and power consumption. Moreover, it is reasonable to believe that the multiple loops that are created in both Figures 3.11 and 3.12, will cause stability issues. Either these stability issues will have to be taken care off, or another method for generation control voltages must be designed. As the circuit complexity is already quite high with possibly large power consumption, it may be worthwhile to design a different type of control signal.

3.6.2. RC Network (Exponential Discharge)

Instead of using feedback loops to create a type of automatic gain control, a control voltage can be created that will be exponential by nature. By discharging a pre-charged capacitor with a resistor an exponential voltage drop is to be expected. In Figure 3.13 a simple schematic is shown in which a capacitor is pre-charged before the receiving period and released during the receive period. When released the resistor will exponentially discharge the gate-source voltage and thus the impedance of the triode device will increase exponentially.

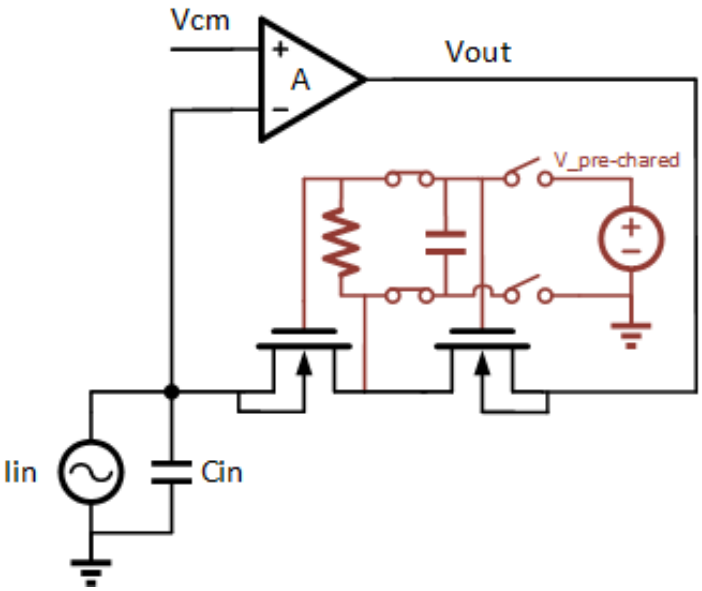


Figure 3.13: Exponential RC discharge as control signal

This implementation has the drawback that capacitors are required, meaning a die area increase is inevitable. On the other hand, the main advantage is the simplicity of the control signal generation. It does not require external control signals, nor is the same control signal used for each capacitor, meaning that correlated noise for different transducer elements will be minimized.

Even though each branch will behave as an exponentially increasing resistance, the overall parallel resistance does not automatically follow the desired gain curve. To this end the exponential control voltage should be optimized for each branch. There are three variables that can be freely chosen, the discharge resistance, the initial pre-charged voltage for the discharge capacitor and the moment the pre-charged capacitor is released. It is assumed that the different triode devices for each branch are already optimized for the respectable gain ranges at which each branch has to operate.
To reduce control complexity and to maximize the possible gain range for each branch all discharge capacitors are pre-charged to the same potential, either being the supply voltage or a different high potential. Often in ultrasound systems transducers are used for both transmitting and receiving. As the receive circuitry should be shielded from the transmit circuitry, due to the presence of high voltage pulses, often a TR switch is used. It is possible to utilize the same digital signals for the TR switch as for the release moments of the different pre-charged capacitors. This, however, means that all the capacitors will be released simultaneously. Even though using multiple release moments can utilize the possible gain range better than a single release moment, it is chosen to use a single moment. This is done as to be able to reuse existing control signals for the TR switch. Moreover, digitally releasing capacitors during the receiving period will cause sudden resistance changes, possibly leading to transient effects each time a new branch is released.

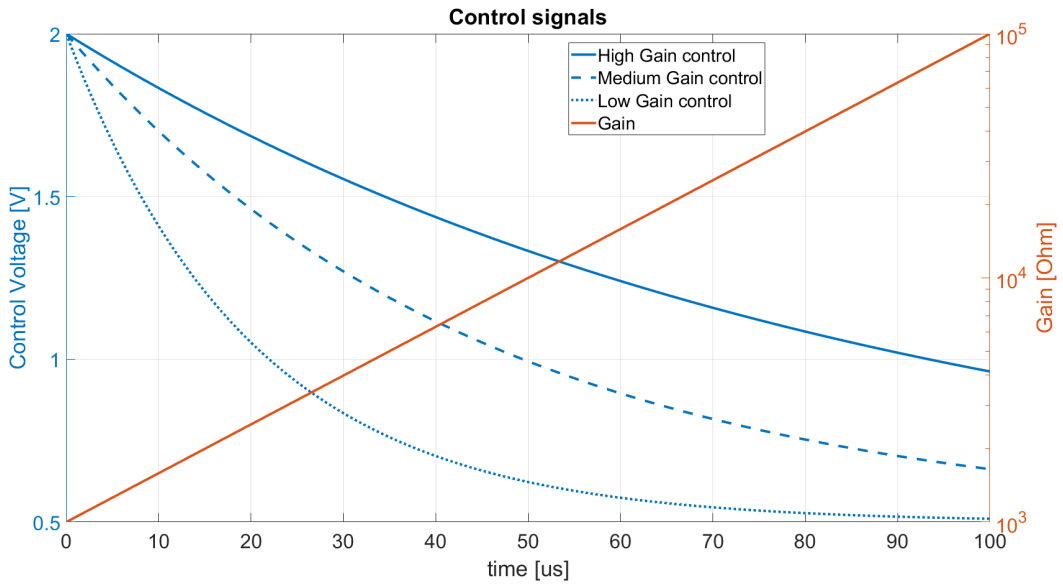


Figure 3.14: Example of possible exponential control signals

Each branch requires its own exponential control voltage, see Figure 3.14. They can not be the same for all the branches as each branch is supposed to dominate the resistance at different time intervals. To obtain different control voltages the resistance values for the different branches are changed. Each branch will have its own RC time constant to let each branch be the dominating resistance at its supposed time interval.
Because there is no automatic gain control to set the gain to the desired gain curve another method should be used to be able to change the gain curve. This can be done by using resistance trimming. By trimming the resistance the RC time constants can be tuned, tuning the overall gain curve until the desired gain curve is reached.

3.6.3. MOS-FET-C Network (Linear Discharge)

The total receive period is 100 μs in this work. This would require the RC time constants for each branch to be in the order of $\mathcal{O}(10\ \mu\text{s})$. With a capacitance of a few pF the discharge resistance is required to be quite large in the order of $\mathcal{O}(1\ \text{M}\Omega)$. These large resistances will require quite a big die area. Even when the die area can be shared if the capacitors are Metal Insulator Metal (MIM) capacitors and the resistances are high resistance poly-resistors

it is possible that the total area is quite large. To reduce area costs the discharge resistance in Figure 3.13 can be exchanged for a transistor operating in the saturation region.

Figure 3.15 shows a linear discharge method where the resistance has been changed for a transistor operating in the saturation region. In the saturation region the drain current is set by the overdrive voltage. The drain-source voltage hardly has an effect on the drain current. This means that a constant current can be drawn from the pre-charged capacitor if the gate-source voltage of the transistor can be set to a constant value.

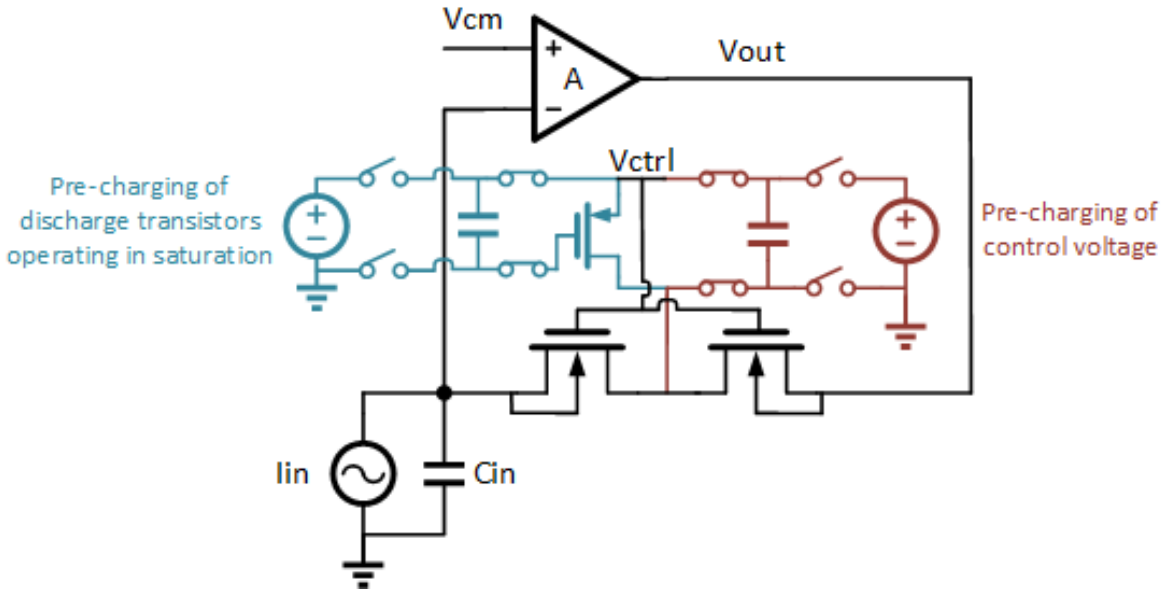


Figure 3.15: Linear discharge of capacitor as control signal

Using a linear discharge technique will mean that the overall resistance will no longer increase as a pure exponential function. However, because the gain error will be a systematic recurring gain error, during digital post processing the less ideal gain curve can be taken care off. This is only the case if the non-ideal gain is close to the ideal exponential gain so no resolution is lost before the post processing.

3.7. Overall Feedback network

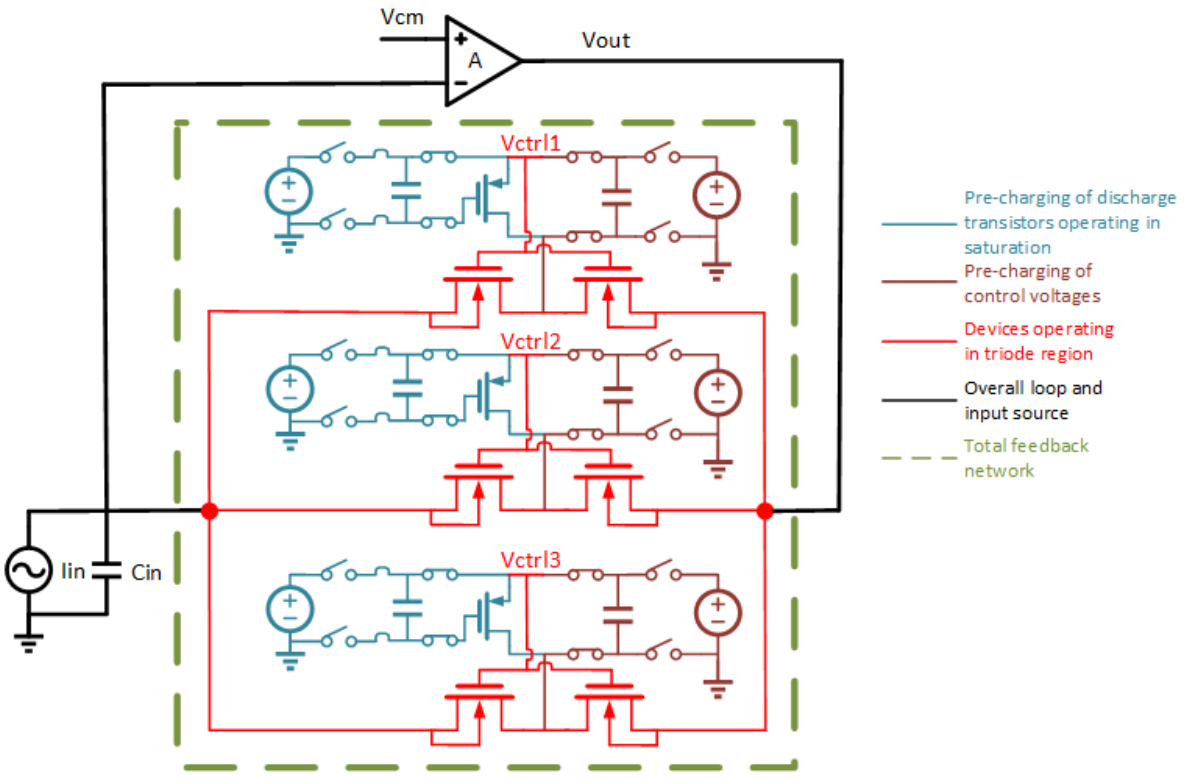


Figure 3.16: Complete feedback network including connections to the input transducer and loop amplifier.

The complete feedback network is shown in Figure 3.16. It shows three separate branches, each containing the discussed dual transistor configuration. The aspect ratio of the transistors is exponentially varied between the three feedback branches.

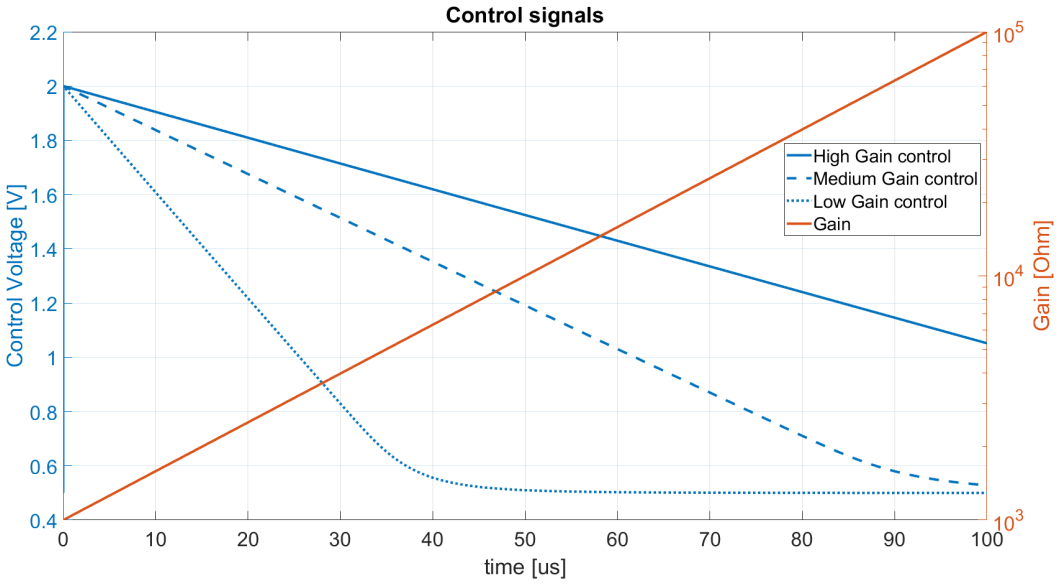


Figure 3.17: The control signals for the different branches

Figure 3.17 shows the three control signals as a function of time. To control each control voltage two different capacitors are required. The capacitor required for setting the control signal is chosen to be 5 pF as a trade-off between minimizing the area cost and obtaining an accurate discharge current. The capacitor required for controlling the discharge transistor is chosen to be 2 pF. A smaller capacitor can be used as this capacitor is not actively discharged. Smaller capacitors are desired as it means lower area costs and 2 pF is enough such that the leaking current has a negligible effect on the control voltage. For the entire feedback network of three branches 6 different capacitors are required with a total combined capacitance of 21 pF.

4

Design

The previous chapter has covered the overall architecture of the TGC-LNA. A transimpedance amplifier architecture has been chosen and the feedback network has been designed. That leaves the focus in this chapter on the feed forward path of the TIA.

This chapter covers the circuit design for the loop amplifier and its bias current. The simulated circuit can be observed in Figure 4.7, where Figure 3.16 represents the feedback network and Figure 4.12 represents the varying bias of the first stage. The input transducer is modeled as an input current source with an input capacitor of 18 pF.

4.1. Loop Amplifier

As stated in chapter 3 the TIA architecture is chosen, such that the low noise functionality and the TGC functionality can be as much as possible separately designed. Using this method the main design focus of the loop amplifier is the noise performance while maintaining a low power consumption.

Even though the TGC functionality is largely dominated by the feedback network, the gain variation will have large influence on the performance of the loop amplifier and must be taken into account. The following sections cover the different aspects of the low noise loop amplifier and how to deal with the different trade-offs that are present.

4.1.1. Architecture

The starting position for designing the loop amplifier is to select the right amplifier structure. To select an amplifier architecture the performance metrics of different architecture types must be compared. While comparing different architectures the low noise and low power performance metrics are given priority as the loop amplifier will be the main power consumer and noise producer for the combined TGC-LNA.

Apart from the noise and power performance, gain control will also prove to be an important aspect. Given a large input capacitor and a large feedback resistance, the dominant pole in the loop will be determined by the transducer capacitor and the feedback resistance. Because the feedback resistance changes over time, the input pole also changes over time. Given a fixed loop amplifier, a time varying unity gain bandwidth (UGBW) will occur. With a decreasing feedback resistance the UGBW increases, which means that excessive power is used to maintain an unnecessary large UGBW. Fixing the UGBW at a certain frequency will result in an overall lower power consumption as the power can be turned down for smaller feedback impedances.
To fix the UGBW the gain of the loop amplifier must be changed together with the feedback impedance. This requires the loop amplifier's gain to be controllable.

There are multiple architecture types for LNAs mentioned in literature for ultrasound applications. Those range from noise cancellation amplifiers [36] to current re-use amplifiers [10] or even the combination of both [37].

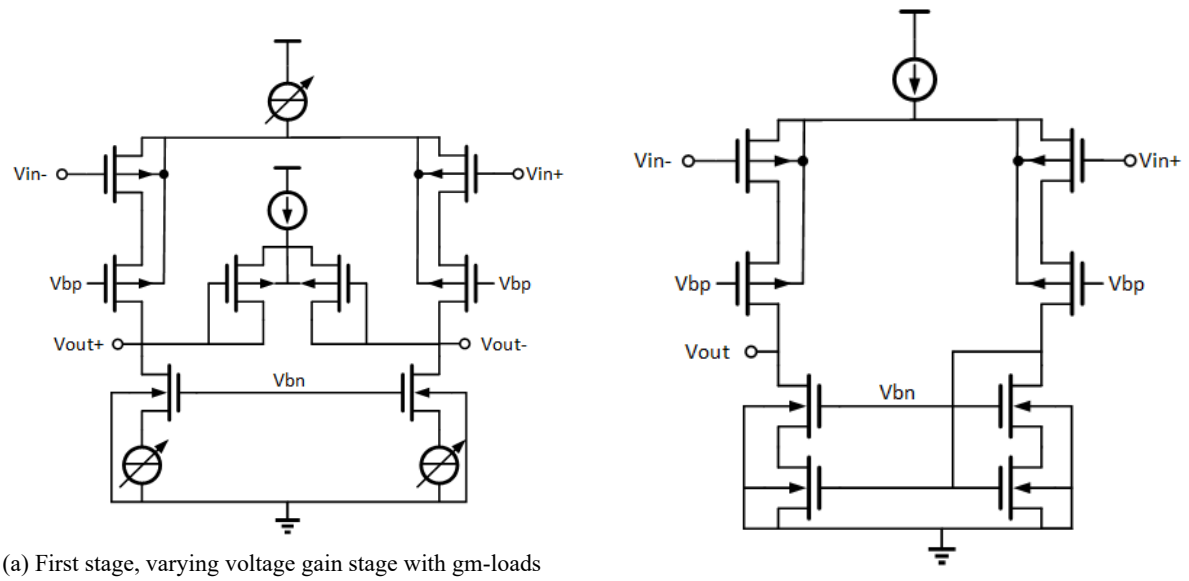
In this work the loop amplifier consists of a telescopic two stage amplifier as is shown in figure 4.1. Two stages

proved to be enough to obtain the required bandwidth and loopgain requirements. The first stage is used to optimize noise performance and to control the gain, while the second stage is used to obtain the required loopgain and output impedance for loop stability. Eventually a single ended amplifier is required for the TIA as ultrasound transducers are inherently single ended. For this reason the second stage is a differential to single ended amplifier stage. It should be noted that the first stage uses diode connected transistors as gm-loads to reduce the gain of the first stage. This is done to increase the bandwidth of the first stage. As the input transducer together with the feedback resistance form the dominant pole, the gm-loads are used to make sure that the output pole of the first stage is non-dominant and does not compromise loop stability.

Low power usage is very important for the LNA and for this reason high current efficiency is required. Therefore current re-use amplifiers are often utilized [10]. In current re-use amplifiers both NMOS and PMOS devices are used simultaneously for the input devices, see Figure 4.2. This makes the effective input gm the addition of the individual transconductances. The noise power scales inverse proportional to the input transconductance and thus current re-use amplifiers are an efficient way of designing LNAs.

Even though current re-use LNAs have better current efficiencies, the telescopic structure as shown in Figure 4.1 is chosen in this work. Current re-use amplifiers require the input voltage to be around mid supply as both NMOS and PMOS devices are to be used and enough headroom is required for the cascodes. The input voltage, however, is relatively low at 0.5 V to allow for large overdrive voltage ranges for the triode feedback transistors. This low input voltage does not leave enough headroom for other cascodes and thus PMOS devices are used as the input devices.
It would be possible to use a current re-use amplifier and increase the power efficiency of the LNA if the input voltage level would be increased. This can be achieved by inserting a capacitor at the input that is pre-charged at a certain voltage level to obtain a DC voltage shift. As area is very expensive in 2D transducer arrays the choice is made to not utilize a DC voltage shift capacitor as capacitors require a lot of die area.

Regarding noise cancellation amplifiers, such as presented in [36, 37], its control schemes are more complex than that of the telescopic or current re-use amplifiers. Given that gain control is important for stability and the added complexity of the varying feedback network, a telescopic amplifier is the safer option for a first prototype. Therefore the noise cancellation architectures are not used in this work.



(a) First stage, varying voltage gain stage with gm-loads

(b) Second stage, differential to single amplifier

Figure 4.1: The different stages of the loop amplifier

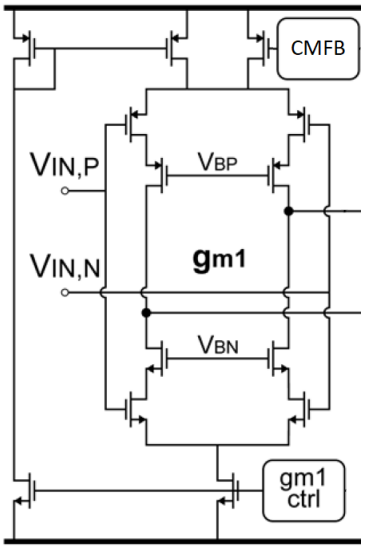


Figure 4.2: First stage of a current re-use amplifier [10]

4.1.2. Noise Optimization

The noise specification for the TGC-LNA is defined as 1 pA/$\sqrt{\text{Hz}}$ spot noise density at the center frequency. Given that the feedback resistance is about 100 kΩ this leaves about 0.9 pA/$\sqrt{\text{Hz}}$ current noise density for the loop amplifier. The input-referred noise of the loop amplifier is often expressed as a noise voltage. As the loop amplifier senses an input voltage its noise can be modeled as an input voltage noise, present at the virtual ground of the TIA. The input-referred noise is converted into input-referred current noise by the impedance connected to the virtual ground, which is dominated by the transducer impedance.
At the center frequency of 7.5 MHz the input impedance is approximately 1.2 kΩ, which gives the loop amplifier room for 1.2 kΩ*0.9 pA/$\sqrt{\text{Hz}}$ = 1.1 nV/$\sqrt{\text{Hz}}$ input referred voltage noise density. The amplifier can be optimized to obtain this noise density at minimum power consumption.

Before noise optimizations can be made the noise sources must be made clear. Looking at transistors there are mainly two types of noise worth looking into. The first is the thermal channel noise, which is represented as [35]:

$$v_{n-Thermal} = \sqrt{\frac{4kT\gamma}{g_m}} \qquad [\frac{V}{\sqrt{Hz}}] \tag{4.1}$$

In this equation $v_{n-Thermal}$ is the input referred thermal voltage noise density, k the Boltzman constant, T the temperature in Kelvin, γ a coefficient determined to be approximately 2/3 for long channel devices and gm the transistor transconductance. The transconductance is a determining factor for the thermal noise density and its value can be designed for and optimized.

The second noise source is the flicker or 1/f noise [35]:

$$v_{n-flicker} = \sqrt{\frac{1}{f}\frac{K}{C_{ox}WL}} \qquad [\frac{V}{\sqrt{Hz}}] \tag{4.2}$$

Here $v_{n-flicker}$ is the flicker voltage noise density, f the frequency, C_{ox} the oxide capacitance, W and L the width and length of the transistor respectively. The frequency is determined by the application and thus by the transducer, which can not be altered. The same goes for the oxide capacitance, which can not be altered as it is mostly process dependent. This leaves the dimensions of the transistor, which can be changed to lower the flicker noise density. Larger transistor area will reduce the 1/f noise of transistors, however the stability of the system must be taken into account. Increasing the transistor area increases the gate capacitance, which leads to non-dominant poles moving into lower frequencies. The area must not be increased such that non-dominant poles will cause stability issues.

In multi-stage amplifiers the first stage will often dominate the noise as the noise of the subsequent stages have lower gain towards the output than the first stage. In other words the input referred noise of a certain stage is reduced by the gain of all the preceding stages.

The first stage of the amplifier is shown in Figure 4.1a. In this diagram not all of the transistors contribute the same amount towards the input referred noise. Generally speaking the cascodes contribute less to the input referred noise than the input transistors. This is due to the fact that the gain from the gate of a cascode transistor to the output is smaller than the gain from the input device to the output. This effectively means that the input referred noise is reduced by the gain of the input device.

The devices that act as current sources do have an equal transfer function towards the output of the amplifier stage as the input devices. They form the same cascoded structure towards the output, meaning that if all the devices would have equal characteristics the input referred noise of the current sources is equal to those of the input devices, which is undesirable. For this reason the current sources will be designed differently than the input devices. If the gain from the current source towards the output is lower than the gain from input to output the input referred noise will be less than that of the input devices. For this reason the current sources are designed to have a relative small transconductance. This is achieved by reducing the W/L ratio of the current source transistors.

4.1.3. Distortion

Distortion or non-linearity can have multiple origins. Distortion can originate from non-linear transfer functions, but can also come from imbalance in the circuitry. Imbalance, for example, is the main form of distortion in the feedback network. A single feedback transistor showed an imbalance in the threshold voltage for positive and negative input signals and therefore a dual transistor configuration is required.
The second stage of the amplifier is susceptible to both distortion due to imbalance as well as due to non-linear transfer functions. First of all the second stage shows the largest output voltage swing. As transistors show non-linear behaviour for larger voltage swings this usually must be taken into account. However, as the output voltage swing is fairly small at 50 mV amplitude it is to be expected that with careful biasing the inherent non-linear behaviour of the transistors will have a minimal effect on the overall distortion behaviour of the amplifier. Therefore no extra precautions are taken to minimize the inherent non-linearity of the transistors.

With regard to the imbalance of the second stage, its differential to single-ended structure is imbalanced by nature. Figure 4.1b shows that the signal path for positive and negative input signals is different. To minimize the distortion the imbalance must be kept at a minimum. It is to be expected that the voltage swing at the right side of the amplifier is very small compared to the swing of the left side. This is due to the fact that the left side sees the voltage swing as a result of the input signal, while the right side needs to be able to deal with a relative constant bias current.

Thus, minimization of the distortion as a result of circuit imbalance can be achieved by minimizing the effect of the drain-source voltage on the behaviour of the transistors. To this end two measures are taken. First the second stage is a cascoded stage. The increased gain by the cascodes reduces the voltage swing present at the drain sides of the current mirror devices. As the drain-source voltage is less sensitive to the input signal distortion is reduced.
The second measure biases the bottom current mirror in strong saturation, because in the saturation operating region the drain current is the least sensitive to the drain-source voltage. To further optimize the current mirror long channel devices are used, because long channel devices minimize the channel length modulation effect. This is beneficial as the channel length modulation makes the drain current again sensitive to the drain-source voltage and is to be avoided.

The end result of the second stage does not look balanced as the DC voltage at the right side is no longer equal to the left side DC voltage. However, due to the current mirror operating in strong saturation the gain from Vin- to Vout roughly equals the gain from Vin+ to Vout and distortion due to imbalance is minimized.

Another point of view looks at the current mirror efficiency. If the current mirror gain is not equal to 1 there will be a gain imbalance for positive and negative input signals. It is therefore important that the current mirror is as accurate as possible. The only thing that varies between the two devices of the current mirror is the drain-

source voltage. Thus the sensitivity of the drain current to the drain-source voltage should be minimized. This, again, results in biasing the current mirror devices in strong saturation.

4.1.4. Stability

With a varying feedback network, a closer look into the loop stability is required. Given the Operational Transconductance Amplifier (OTA) structure, a simplified model can be drawn to compute the dominant input pole. To this end the model of Figure 4.3 is used. The two stage amplifier is modeled with a certain net transconductance value gm and an output resistance R_o. The loopgain can be computed by breaking the loop and is expressed as the amplifier gain followed by the gain from the output back to the input. This is expressed as follows:

$$\text{Loopgain} = \frac{V_i}{V_x} \tag{4.3}$$

$$0 = gmV_x + V_o\left(\frac{1}{R_o} + \frac{sC_{in}}{1+sR_{fb}C_{in}}\right) \tag{4.4}$$

$$V_o = V_i\left(1+sR_{fb}C_{in}\right) \tag{4.5}$$

$$gmV_x = -V_i\left(1+sR_{fb}C_{in}\right)\left(\frac{1}{R_o} + \frac{sC_{in}}{1+sR_{fb}C_{in}}\right) \tag{4.6}$$

$$\frac{V_i}{V_x} = \frac{-gmR_o}{1+s\left(R_{fb}+R_o\right)C_{in}} \tag{4.7}$$

From this simplified model it becomes clear that the dominant pole is determined not only by the input capacitor and the feedback resistance, but also the output impedance. As the feedback resistance changes, so does the frequency location of the dominant pole. The first simulation of Figure 4.4 shows that, while neglecting higher order poles, both the bandwidth and unity gain bandwidth change with the feedback resistance.

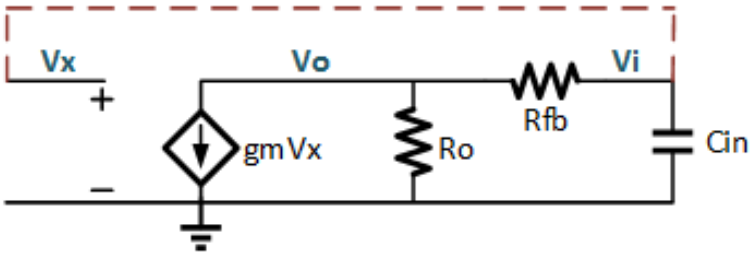


Figure 4.3: Simplified model used to locate the dominant pole frequency. The dashed line suggests how the amplifier structure operates in closed loop configuration.

A moving unity gain bandwidth (UGBW) gives rise to multiple issues that need to be dealt with. Given a certain required UGBW, increasing the UGBW means that power is unnecessarily spent on increasing the bandwidth, even if it does not contribute to the performance of the amplifier. This means that a fixed UGBW is desired to minimize power consumption.

Another issue originates from secondary poles that have been ignored until now. Apart from the input capacitor there will also be an output capacitor comprised of the load capacitor and multiple drain-gate capacitors coming from the output devices of the second stage. With relative large output resistances it is expected that higher order poles will cause stability issues. To keep the amplifier stable the phase margin should be kept as large as possible. Again this can be achieved by keeping the UGBW at a fixed frequency.

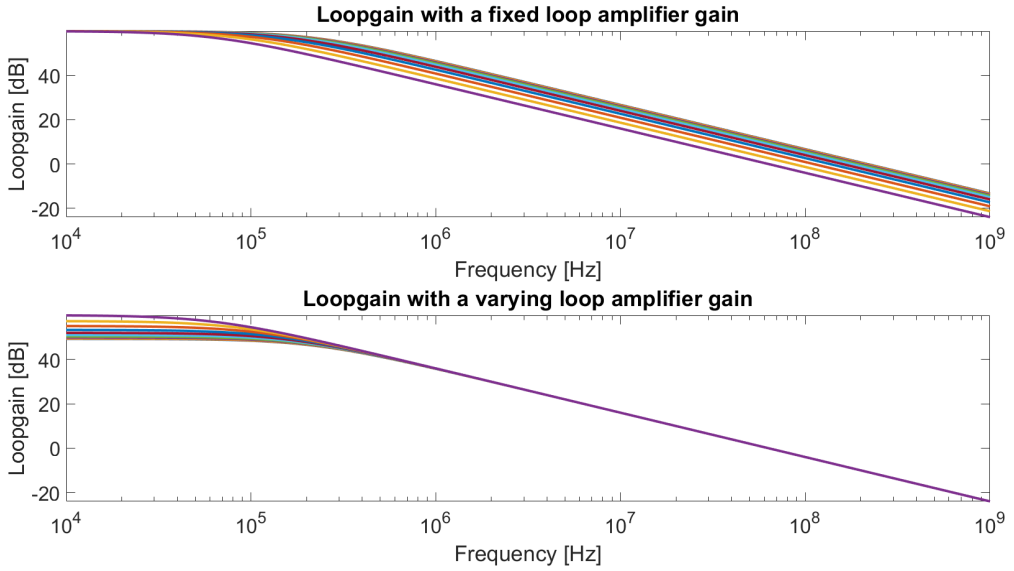


Figure 4.4: Loopgain for different feedback resistances, simulated both with a constant and a varying loop amplifier gain.

To keep the UGBW fixed while the dominant pole changes, the DC gain of the loop amplifier should be altered. This is shown in the second subfigure of Figure 4.4. If the pole frequency increases, while the DC gain decreases the UGBW can be maintained constant. To change the DC gain of the OTA while having the largest impact on the power consumption the gain of the first stage is made variable.

The gain of the first stage, see Figure 4.1a, is defined by the ratio of input and load transconductances ($\frac{gm_{in}}{gm_{load}}$). Changing either the input or load transconductance will alter the gain. Using the gm over id biasing methodology as proposed in [38], the transconductance can be expressed as follows:

$$gm = \frac{I_D}{nU_T} \tag{4.8}$$

The transconductance can be seen as linearly dependent on the drain current. Here I_D is the drain current, n the subthreshold slope factor and U_T the thermal voltage. For (4.8) to hold the transistors are biased in weak inversion. This, because of the exponential current behaviour of the transistor in weak inversion. The result of decreasing the drain current of the input devices would end in the decrease of the input gm and thus the gain of the first stage.

Decreasing the gain by decreasing the input drain current has multiple effects on the performance of the amplifier. Turning down the power consumption not only decreases the DC gain, but also increases the input referred noise, as is shown by equation (4.1). This means that to achieve a constant UGBW a higher noise density is to be expected.

A varying noise floor does not need to pose significant issues. As presented in [8] a varying noise floor does not compromise performance as long as it does not degrade the signal to noise ratio (SNR). In [8] the noise floor is changed deliberately together with the gain of the TGC amplifier to achieve a lower power consumption. This means that if the required gain difference is smaller than the difference in the noise floor the expected increase in noise density does not degrade the overall performance of the TGC amplifier.

In this design the gain range is set to be 40dB. This means that for a constant SNR the noise density may also differ by 40dB. It is reasonable to assume, given the output resistance of the second stage and equation (4.7) that the DC loopgain varies less than 40dB. As the DC loopgain variation is directly proportional to the input gm of the first amplifier stage it is reasonable to believe that the noise density increase will be smaller than the signal gain difference. This means that there will be no expected SNR performance reduction due to changing the gain

of the first stage to achieve a constant UGBW.

With a constant UGBW the stability issues are not yet solved. The higher order poles located at the output of the second stage must be placed at sufficiently high frequencies, such that they do not compromise the phase margin and pose stability issues. There are two different capacitors that need to be looked into. The first is the output load capacitance. The second is the output capacitance of the second stage comprising the drain-gate capacitances of the output devices.

The output load capacitance is set to be 250 fF as this is a reasonable input capacitance for a subsequent output buffer. With a relative large output resistance, the pole presented due to the output capacitance with the output impedance will be at relatively low frequencies. As the pole at the output is a non-dominant pole in the loop the phase margin of the loop decreases, decreasing the stability margins of the amplifier. To increase the frequency at which the load capacitor will affect the loop a series resistance is used as is shown in Figure 4.5. The 25 $k\Omega$ series resistance gives a -3 dB frequency at 25 MHz. This frequency such that the output voltage swing that the load capacitor experiences at the band of interest is not compromised, while increasing the pole in the loop to higher frequencies, increasing loop stability.

Apart from the added resistance shown in series with the load capacitor in Figure 4.5, also a shunt resistance is used. This shunt resistance is used to provide what is called resistive broadbanding. Decreasing the output impedance of the amplifier increases the pole frequency of the pole caused by the output impedance and the output capacitance of the second stage. A small DC current flows through the shunt resistor, creating a DC unbalance in the second stage and increasing distortion. However, the shunt resistor is chosen to be large enough, such that the DC current is only 1% of the total bias current for each branch, resulting in a minimal distortion increase.

In summary three different methods are used to increase the stability of the amplifier. First the gain of the first stage is made variable to decrease the power consumption and create a constant unity gain bandwidth. Secondly a series resistance is used to decrease the effect of the load capacitor on the loop stability. Lastly a shunt resistance is used to push the output pole frequency of the second stage to a sufficiently high frequency, such that that it does not degrade the loop stability.

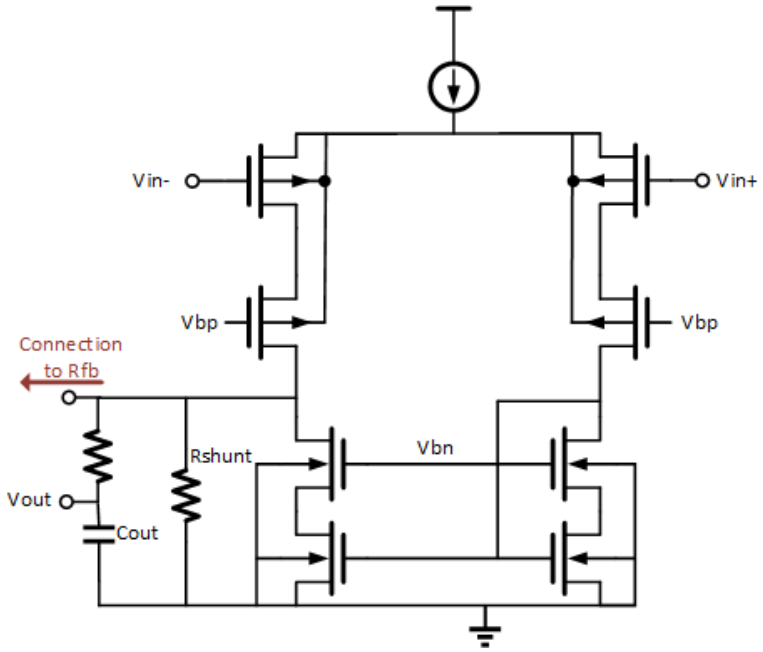


Figure 4.5: Stability measures taken in the form of broadbanding resistors.

4.1.5. Common Mode Feedback

The first stage is a fully differential stage and thus the common mode output level needs to be defined. This is done using a common mode feedback (CMFB) network. Usually such a network is implemented by sensing the

average of the two output voltage levels and comparing it to a desired voltage level and feeding back the amplified difference signal to a node that is able to affect the common mode output level.

CMFB amplifiers often have low gain and wide bandwidth requirements for loop stability. The loopgain will be quite large as the internal gain of the main amplifier is utilized as it forms a part of the feedback loop.

The CMFB in this work is slightly different than usual as it does not utilize a separate CMFB loop amplifier. Figure 4.6 shows the used CMFB network. Instead of sensing the average between the different output terminals the source side of the load transistors is used as a measure for the common-mode output level. Given that the load current is a constant DC current the source side of the load transistors will have a voltage level that is a voltage shift from the common-mode output and can therefore be used to sense the common-mode output level.

From the common-mode sensing node a voltage drop of one gate-source voltage is created with the use of a diode connected transistor. The resulting voltage (Vcm-Control) controls the two CMFB control transistors. It should be noted that the bottom current sources of Figure 4.1a are implemented by two different transistors. This is done for the following two reasons.
First of all the overall bias current is a largely varying current over time. As it is difficult with the applied CMFB scheme to control both the common mode output voltage as well as to take care of the varying bias current a separate transistor is used to accommodate for the varying bias current.
Secondly, splitting the current source into two differently sized transistors decreases the transconductance at the the common mode control node, reducing the loopgain of the CMFB loop. This will increase the loop stability.

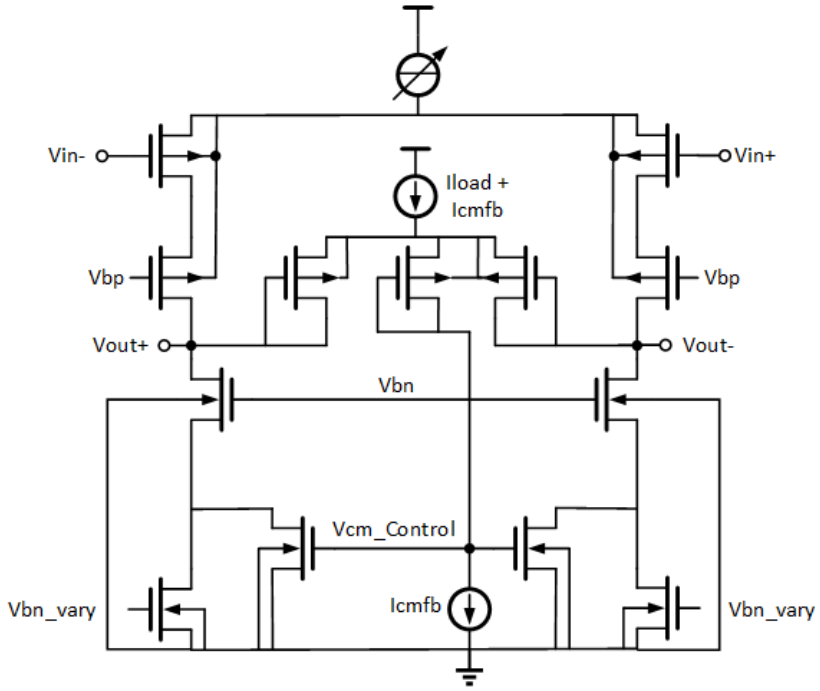


Figure 4.6: First stage with implemented common mode feedback

The CMFB scheme used has some drawbacks. As the common mode output voltage is not compared to a reference voltage the common mode output voltage will not be fixed to a certain voltage level. This is not a problem as the second stage contains a fully differential input, meaning that the output sensitivity to the common mode output voltage of the first stage is small. Off course the common mode output voltage needs to be confined within a certain range to allow for enough headroom for all the transistors in the amplifier to operate in the saturation region.

The current required for the CMFB, I_{CMFB} in Figure 4.6, can be quite small in comparison to the load current. To obtain a constant voltage drop the current source powering the diode connected transistor with I_{CMFB} needs to be quite accurate, which should be taken into account when designing the DC current sources.

4.1.6. Overall Loop Amplifier

The overall design of the loop amplifier is shown in Figure 4.7. Apart from the two stage amplifier, also the connections to the input transducer, output capacitor and feedback network are shown. The transistor aspect ratios are given in Table 4.1. The transistors are sized in a way to minimize both area costs and noise, while maximizing loop stability.
The bias current varying as a function of the gain is covered in the next section.

Table 4.1: Transistor aspect ratios of the loop amplifier

Transistor	Aspect Ratio Single Transistor $\left[\frac{\text{Width}}{\text{Length}}\right]$	Number of fingers	Total aspect ratio $\left[\frac{\text{Width}}{\text{Length}}\right]$
M1-M2	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	895	$\frac{1.61\ \text{mm}}{0.18\ \mu\text{m}}$
M3-M4	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	410	$\frac{738\ \mu\text{m}}{0.18\ \mu\text{m}}$
M5-M6	$\frac{4.5\ \mu\text{m}}{0.45\ \mu\text{m}}$	50	$\frac{225\ \mu\text{m}}{0.45\ \mu\text{m}}$
M7-M8	$\frac{15\ \mu\text{m}}{1.8\ \mu\text{m}}$	7	$\frac{105\ \mu\text{m}}{1.8\ \mu\text{m}}$
M9-M10	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	60	$\frac{108\ \mu\text{m}}{0.18\ \mu\text{m}}$
M11	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	300	$\frac{540\ \mu\text{m}}{0.18\ \mu\text{m}}$
M12-M13	$\frac{15\ \mu\text{m}}{1.8\ \mu\text{m}}$	3	$\frac{45\ \mu\text{m}}{1.8\ \mu\text{m}}$
M14-M15	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	30	$\frac{54\ \mu\text{m}}{0.18\ \mu\text{m}}$
M16-M17	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	15	$\frac{27\ \mu\text{m}}{0.18\ \mu\text{m}}$
M18-M19	$\frac{1.8\ \mu\text{m}}{0.18\ \mu\text{m}}$	10	$\frac{18\ \mu\text{m}}{0.18\ \mu\text{m}}$
M20-M21	$\frac{4.5\ \mu\text{m}}{0.45\ \mu\text{m}}$	10	$\frac{45\ \mu\text{m}}{0.45\ \mu\text{m}}$

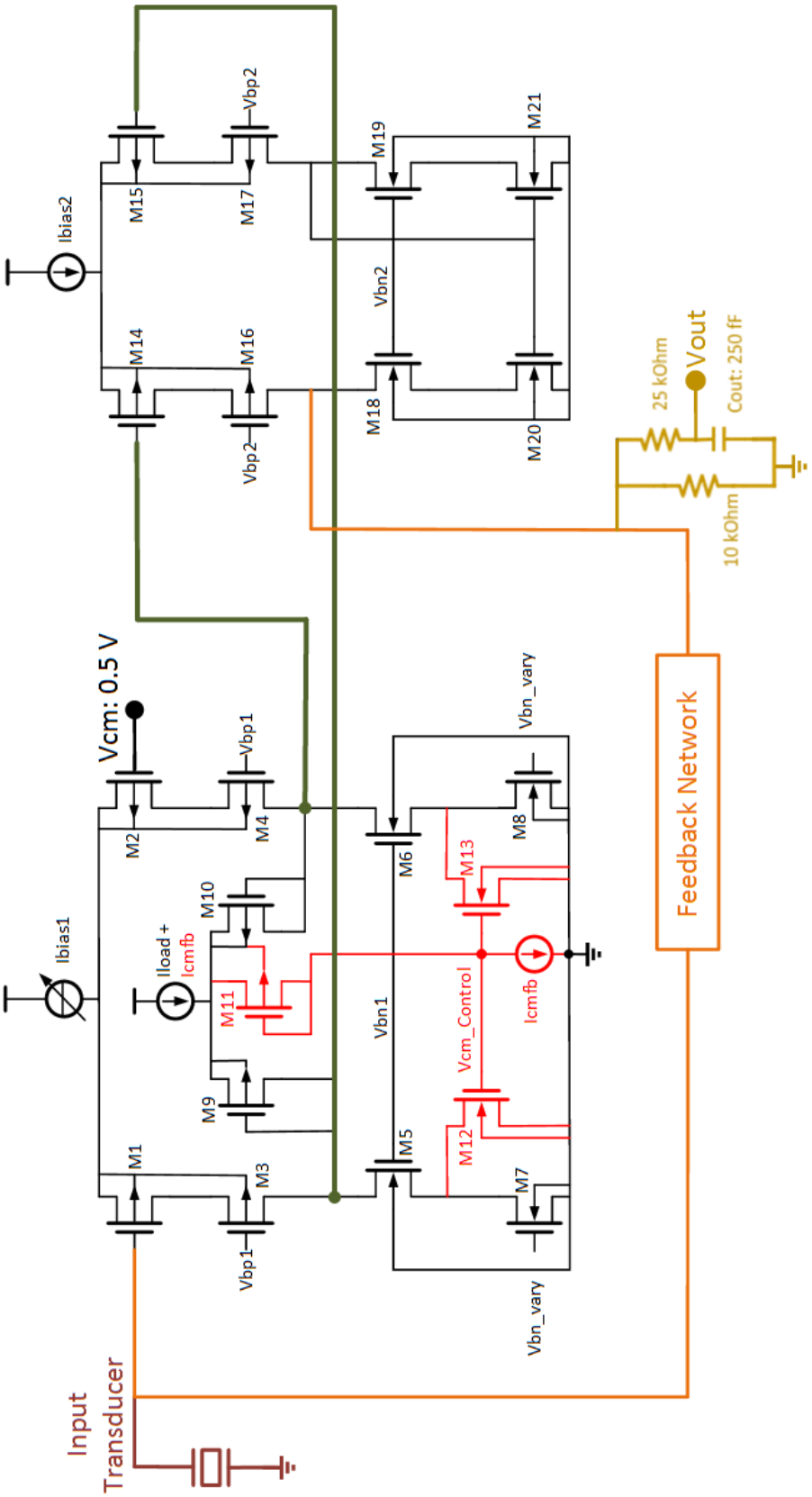


Figure 4.7: Overall loop amplifier, including connections with the input transducer, the feedback network and the output capacitor.

4.2. Variable Bias Current

As stated in section 4.1.4 to achieve a constant unity-gain bandwidth the gain of the first stage is made variable. This is done by changing the bias current of the first stage. Before a variable bias current source can be created it is important to know how this current source should behave. The current source behaviour can be deducted from the loopgain equation, see equation (4.7). The input transconductance should change in the same manner as the dominant pole. The dominant pole frequency as a function of time can be expressed as follows:

$$\text{Dominant Pole} = \frac{1}{2\pi \left(R_{fb} + R_o\right) C_{in}} \quad [\text{Hz}] \tag{4.9}$$

R_{fb} Changes from 1 kΩ to 100 kΩ in 100 μs

$$R_{fb} = 100^{\left(\frac{t}{100\mu s}\right)} \quad [\text{k}\Omega] \tag{4.10}$$

$$\text{Dominant Pole} = \frac{1}{2\pi \left(100\text{k}\Omega^{\left(\frac{t}{100\mu s}\right)} + R_o\right) C_{in}} \quad [\text{Hz}] \tag{4.11}$$

$$\tag{4.12}$$

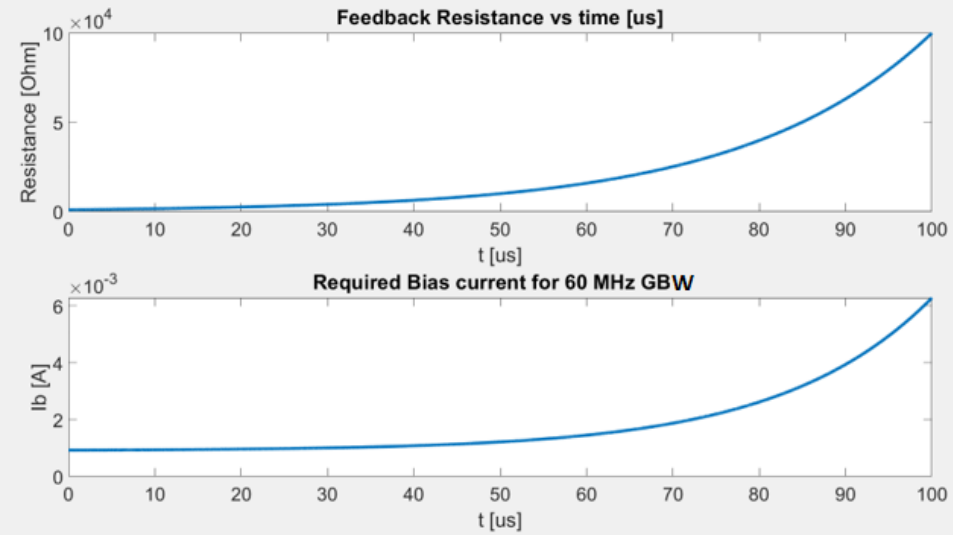
Given (4.11) it is noticeable that the dominant pole changes exponentially and thus the input transconductance also needs to change exponentially. Knowing how the input gm changes, the bias current can be computed to accommodate for this change. The required bias current can be computed in two different methods. The first is to utilize (4.11) and compute the bias current as an exponential function of time. The second method makes use of the strong connection between the bandwidth and the feedback resistance and writes the bias current as a function of the feedback resistance. The following equation shows how the transconductance of the first stage can be expressed as a function of the feedback resistance:

$$gm(t) = gm(100\mu s) * \frac{R_{fb}(t) + R_o}{R_{fb}(100\mu s) + R_o} \tag{4.13}$$

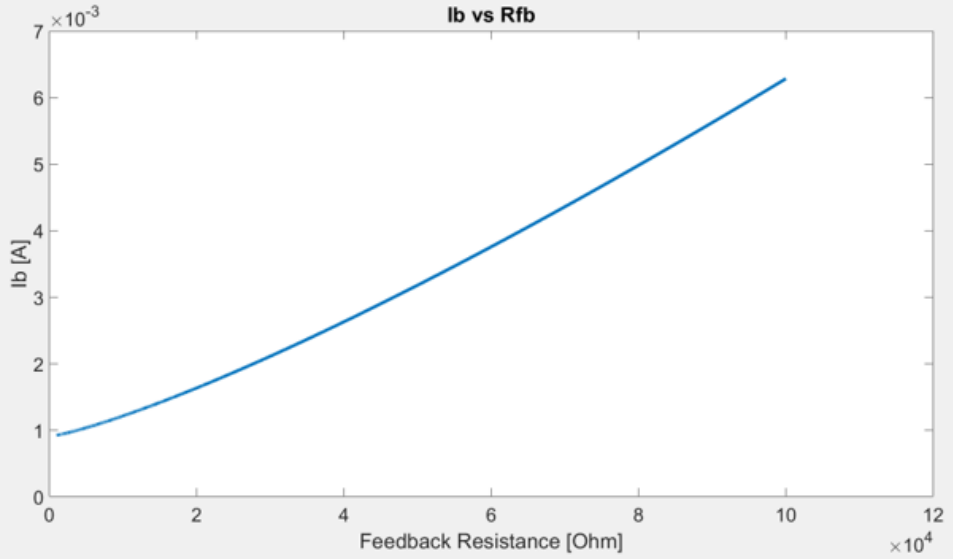
The input gm is designed to suffice the required noise performance at the highest gain setting. Therefore the gm at t=100 μs is taken as the base value of the transconductance. Equation (4.13) shows that the strong dependency between the feedback resistance and the bandwidth results in a linear dependency between the input gm and the feedback resistance. The required bias current can now be computed using equation (4.8) and is verified by simulations.

Figure 4.8 shows the relation between the feedback resistance, the bias current and the time to keep the unity gain bandwidth at a constant 40 MHz. From 4.8a it can be observed that indeed both the feedback resistance and the bias current follow exponential curves. When the bias current is expressed as a function of the feedback resistance an approximately linear curve follows, as shown in Figure 4.8b. This result is in line with the expectations as computed in (4.13). In (4.8) the inherent assumption is made that the ratio between transconductance and bias current remains constant. This assumption no longer holds as the bias current variation is so large that the operating points of the transistors change over time. The result is that Figure 4.8b does not show an exact linear relation between the bias current and the feedback resistance.

Using the two curves from 4.8 there are two different methods for creating the varying bias current source. The first is to create a separate controllable exponentially variable current source and the second is to design a current source based on a linear function depending on the feedback resistance.



(a) Both bias current and feedback resistance as function of the time



(b) Required bias current as function of the feedback resistance

Figure 4.8: Relationship bias current and feedback resistance for a UGBW of 60 MHz

4.2.1. Exponentially Varying Current Source

There are multiple methods to create an exponentially varying current source. Using for example bipolar transistors an exponentially varying current source can be created. However, using bipolar transistors, controlling the output current with minimal effects of process variations can be difficult. Therefore, in [10], a piece-wise exponential approximation current source is designed.

Figure 4.9 shows the varying bias current source as proposed in [10]. It uses multiple exponentially scaled constant current sources and multiple differential pairs to vary the output current by means of current steering.

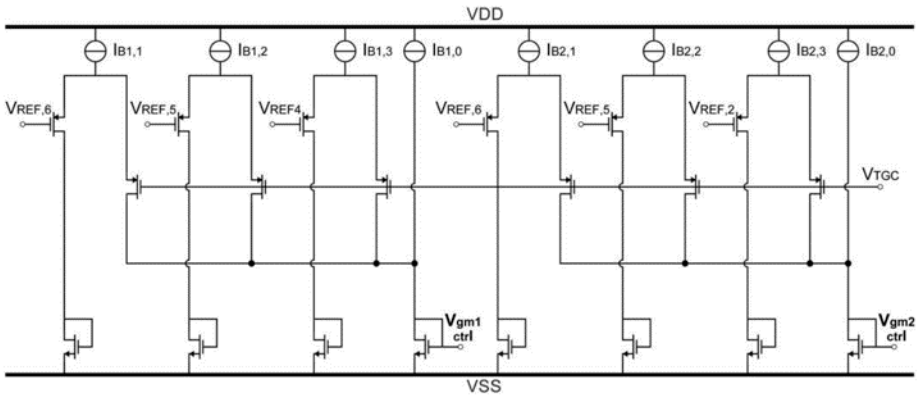


Figure 4.9: Piece-wise exponential approximation for a current source [10]

To control the output current both the control voltage as well as the reference voltages can be altered. Optimizing the reference voltages will lead to an optimized bias current variation as needed, while an external ramp voltage, such as V_{TGC} in Figure 4.9, is required to control the time period at which the bias current variation occurs.

Even though the bias current variation curve can be optimized it may not form the best solution for designing the varying bias current source. There are some issues with this configuration. First of all an external control signal needs to be created, together with the different reference voltages. Secondly the constant current sources, as shown in Figure 4.9, are not very power efficient as at each moment in time a fraction of the current is just sinked into ground without being utilized for the main amplifier. The third issue deals with the strong relation between the required bias current and the feedback resistance, as shown in Figure 4.8b. Even though the bias current curve can be optimized, using the configuration as presented in [10] the relation between the feedback resistance and the bias current is lost. This means that even though the bias current curve is as required, but the feedback resistance behaves differently than expected, the constant UGBW can no longer be guaranteed.

4.2.2. Bias Current Linearly Dependent on the Feedback Resistance

As the relation between the required bias current and the feedback resistance is approximately linear it is desirable to design the bias current as a function of the feedback resistance. From Figure 4.8b it is observed that the feedback resistance and the bias current are directly proportional to each other. This means that an active method is required to create the varying bias current source.

Figure 4.10 shows the method used in this work for creating the bias current source. It uses an active loop with a loop amplifier to obtain the following relation between the feedback resistance and the bias current:

$$I_b = I_{cnst}\frac{(R_1 + R_{fb})}{R_2} \tag{4.14}$$

$$R_1 \propto R_o \tag{4.15}$$

$$R_2 \propto \frac{1}{R_{fb}(100\mu s) + R_o} \tag{4.16}$$

In these equations I_{cnst} is a constant current that scales the total bias current, R_1 a resistance used for setting the DC bias current component, R_o the output impedance of the second stage, R_{fb} is a scaled version of the feedback resistance, R_3 is a resistance used for setting the linear coefficient. The current consumption of the bias current generation circuit can be quite small as only a scaled version of the required bias current source is needed. By means of current mirrors the required bias current can be injected into the first stage.

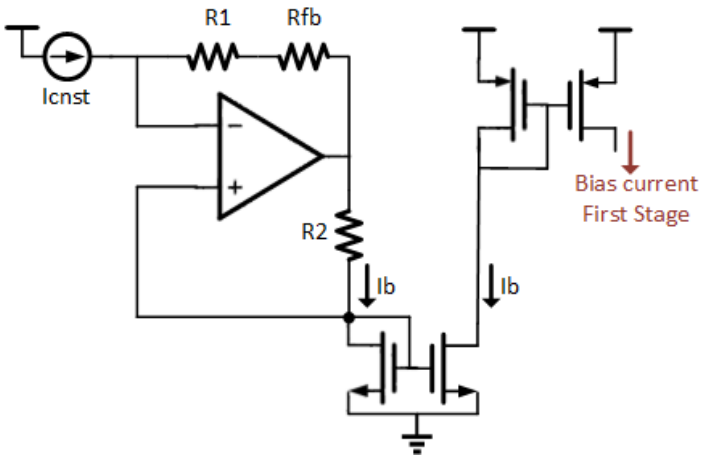


Figure 4.10: Linearly varying current source based on the feedback resistance

4.2.3. Bias current issues

Given the bias generation as shown in Figure 4.10 there are two concerns for the overall amplifier performance. First of all the feedback configuration consists of two different feedback loops. This means that there is a positive feedback loop and stability can become an issue.

Noise is another concern for the bias current source generation circuit. The current noise from the bias generation circuit is directly copied and scaled to the main amplifier. This means that even when the current noise of the generation circuit is quite small, the input referred noise can be quite extensive, due to the current gain to the main amplifier.
To decrease the input-referred noise due to the bias circuitry two measures are taken. First, the current gain is minimized as much as possible by increasing I_{cnst} while decreasing the scaled version of the feedback resistance. This is required to keep the voltage swing at the output of the loop amplifier limited within operational bounds. Another measure taken is an additional low-pass filter, see Figure 4.11. The bias current varies much slower than the signal, meaning that a low-pass filter can be introduced to minimize in-band noise.

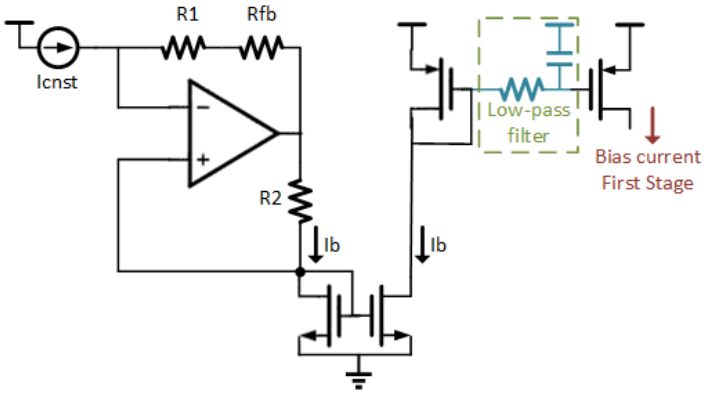


Figure 4.11: Linearly varying current source based on the feedback resistance with additional low pass filter

4.2.4. Complete first stage with varying bias

The variable biasing of the first stage is shown in Figure 4.12. It uses the bias current generation circuit of Figure 4.11 and current mirrors to inject the bias current into the first stage.

It can be observed that the bottom NMOS transistors M7 and M8 are biased, such that half of the varying bias current and half of the load current flows through each of these transistors. This is done so transistors M12 and M13 do not have to deal with the varying bias current.

The DC current sources (I-CMFB and I-Load) are not yet implemented and are to be designed in future work. This means that the interconnections regarding the DC bias sources are expected to be different in a complete implementation. The ideal DC current sources are also the reason that the biasing of the second stage is not shown, as the bias current of the second stage is also a DC current.

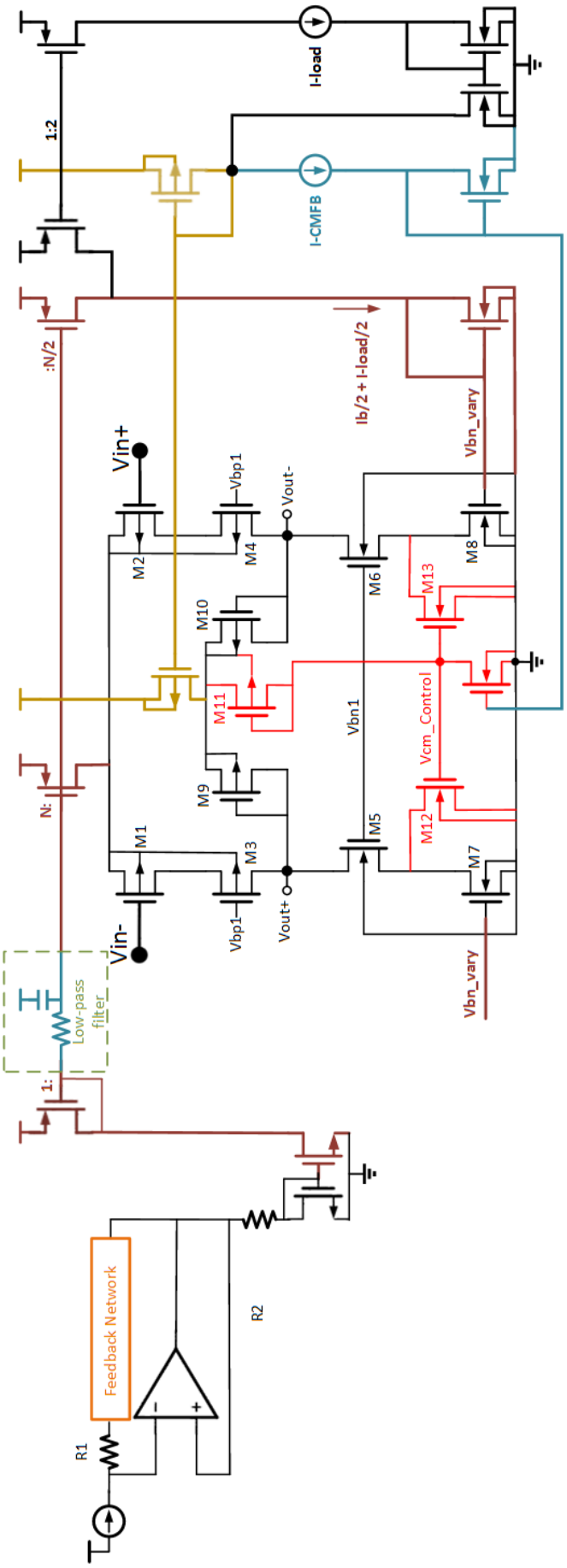


Figure 4.12: First stage complemented with its varying bias current source

5 Results

In the previous chapters the design of a combined TGC-LNA has been presented. The goal of this chapter is to verify whether the amplifier operates as intended. To this end all separate components have been simulated and the results are presented in this chapter.

The schematic of Figure 4.7 shows the total TGC-LNA simulated in this chapter, where Figure 3.16 shows the implemented feedback network and Figure 4.12 the varying bias current generation for the first stage biasing. To simulate the input transducer the electrical equivalent, shown in Figure 3.1, is used, where the total impedance is dominated by the large capacitor.

5.1. Feedback configuration

From section 3.3 it is clear that to improve the linearity of the feedback impedance a dual transistor configuration as shown in Figure 3.5b is used. This is done to minimize the effect of a varying threshold voltage as a function of the input signal.

Figure 5.1 shows the difference in distortion behaviour between the single transistor configuration and the dual transistor configuration for the feedback network. The great improvement in linearity is due to the elimination of even order harmonics by implementing the dual transistor configuration.

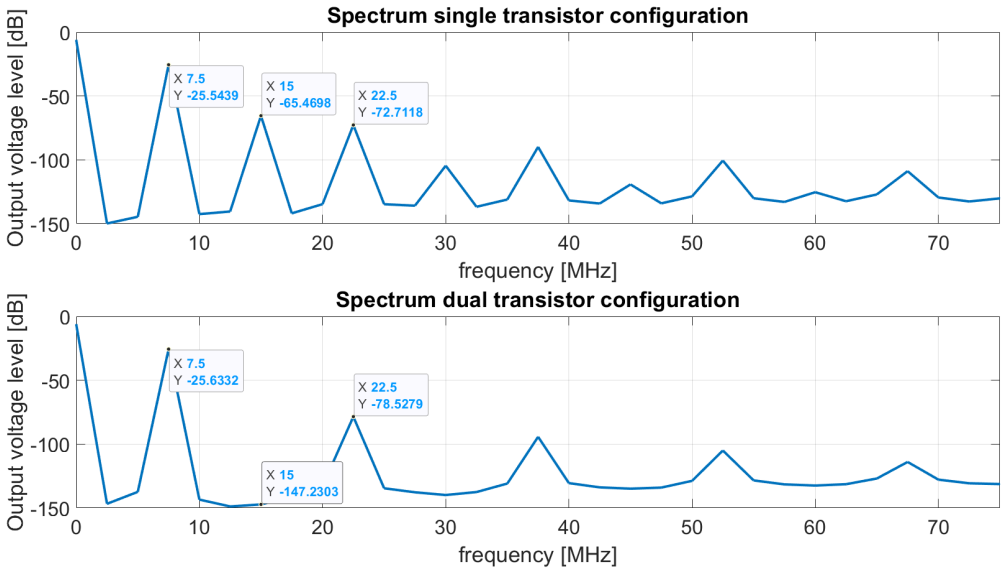


Figure 5.1: Spectrum of both single and dual feedback transistor configurations

5.2. AC response

To simulate both the gain and bandwidth of the combined TGC-LNA amplifier first an AC analysis is carried out. Figure 5.2 shows the closed loop AC response of the designed TGC-LNA. As the receive period is 100 us the closed loop gain is simulated for different time instants corresponding to different gain settings. The AC response shows that the DC gain varies from 60 to 100 dBΩ. This means that during the receive period the gain changes the required 40 dB.

For the TGC-LNA to operate in the required gain range the bandwidth of the closed loop gain should be larger than the band of interest. For the designed amplifier the band of interest is between 5 MHz and 10 MHz. This means that the closed loop should be larger than 10MHz to obtain the desired gain curve. From Figure 5.2 it can be observed that the bandwidth for each time instant is larger than the band of interest.

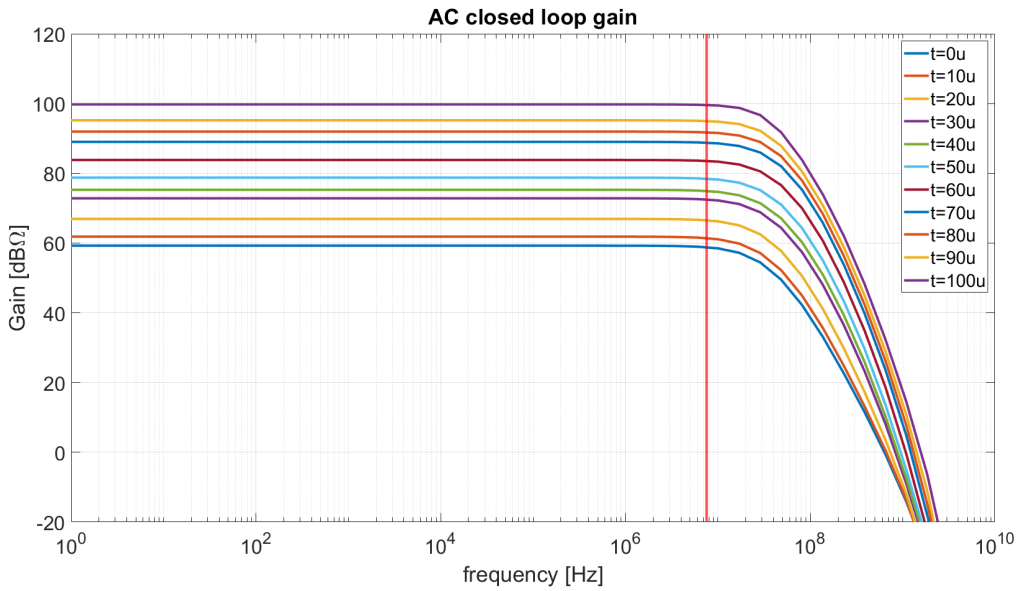


Figure 5.2: Closed loop bandwidth for different time instants

Figure 5.3 shows that the bandwidth does change over time. This is expected as the bias current variation is non ideal because of mismatches and non-perfect current mirroring. Even though the bandwidth changes over time it remains at least a factor two larger than the band of interest. This means that both the closed loop gain and bandwidth meet the requirements.

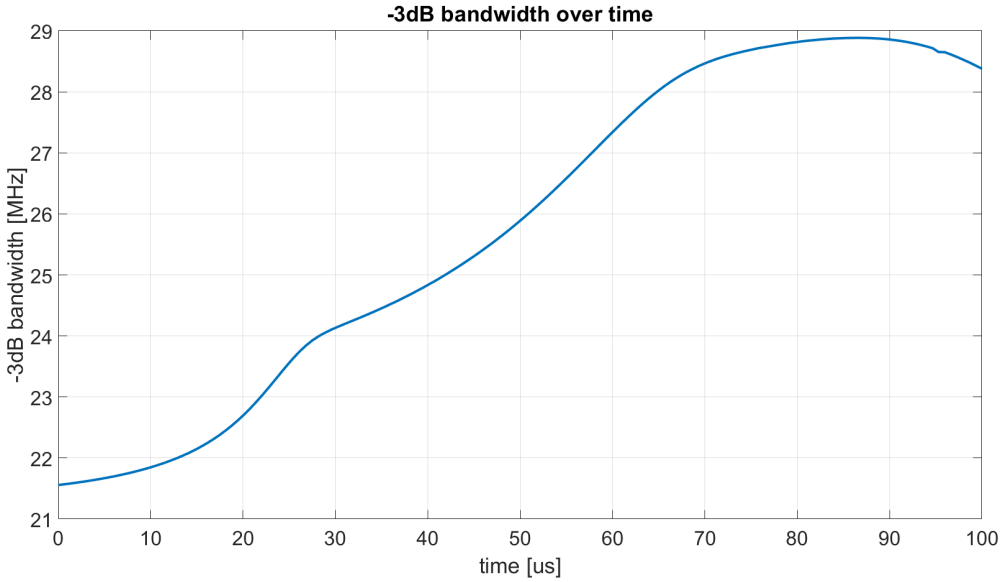


Figure 5.3: -3dB bandwidth variation over time

5.3. Stability

5.3.1. Overall Loop

The goal of the varying bias current of the first stage is to create a constant unity gain bandwidth. Figure 5.4 shows the bode plots main amplifier feedback loop. As expected, the main pole changes with quite some margin, but the unity gain bandwidth varies much less. It should be observed that the higher order poles do change over time, resulting in a varying phase margin over time. Figure 5.5 shows that the phase margin does indeed vary over time, but never falls below 60 degrees. This suggests that the main amplifier is quite stable.

Apart from the phase margin, Figure 5.5 also shows that the unity gain bandwidth is not entirely constant but varies between 32-47 MHz. This variation is to be expected given the linearization between the required bias current of the first stage and the feedback resistance.
Another error is introduced when the current mirror structure that copies the current from the bias generation circuit into the first stage is not exactly one. Due to mismatches and secondary effects, such as channel length modulation, the bias current is not exactly copied to the first stage.

Even though the unity gain bandwidth is not completely constant over time, its variation is minimized by the varying bias current. Given that the phase margin exceeds the 60 degrees at each time instant, the variation in UGBW does not degrade the TGC-LNA performance.

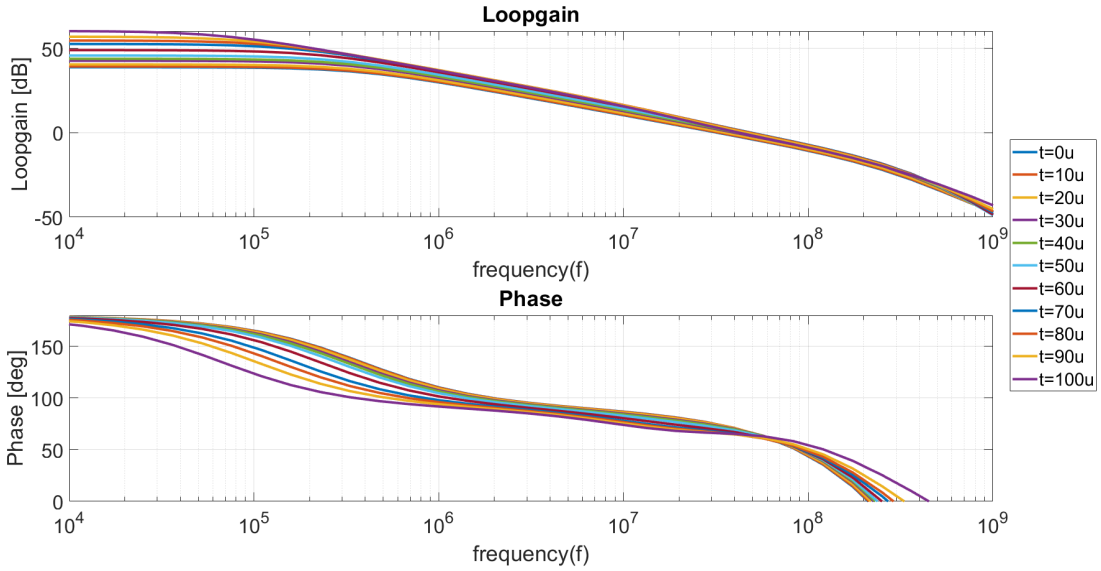


Figure 5.4: Loopgain and phase of the main loop

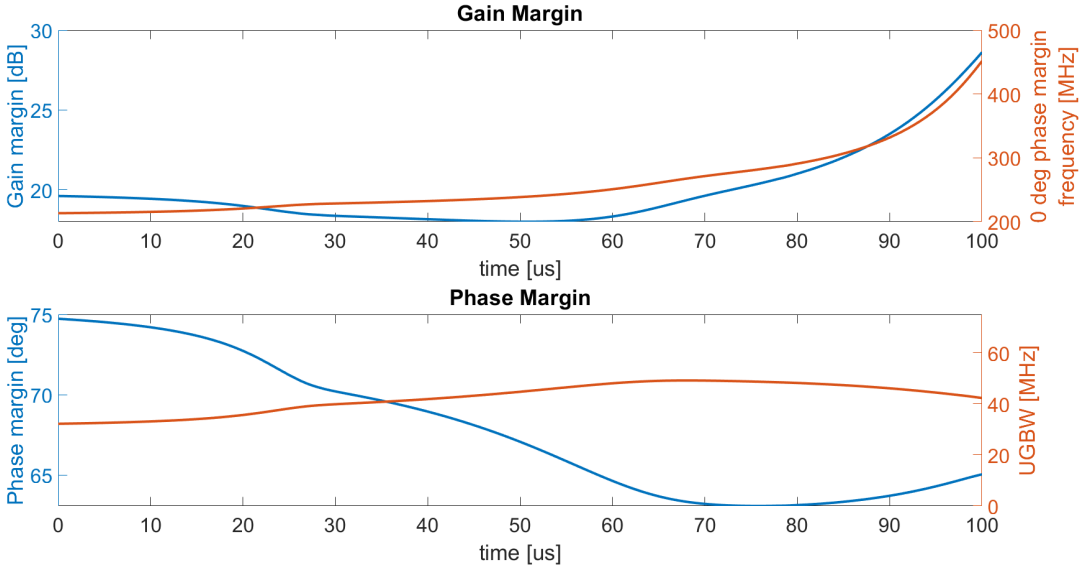


Figure 5.5: Gain margin and phase margin of the main loop

5.3.2. CMFB

Figure 5.6 shows the bode plots for the common mode feedback loop. The varying bias current of the first stage alters the output impedance of the first stage, which results in a varying DC gain over time. As can be observed, the result of the varying DC gain is an almost constant unity gain bandwidth, as is confirmed by Figure 5.7. The phase margin of the CMFB stays well above 60 degrees, resulting in a stable CMFB loop.

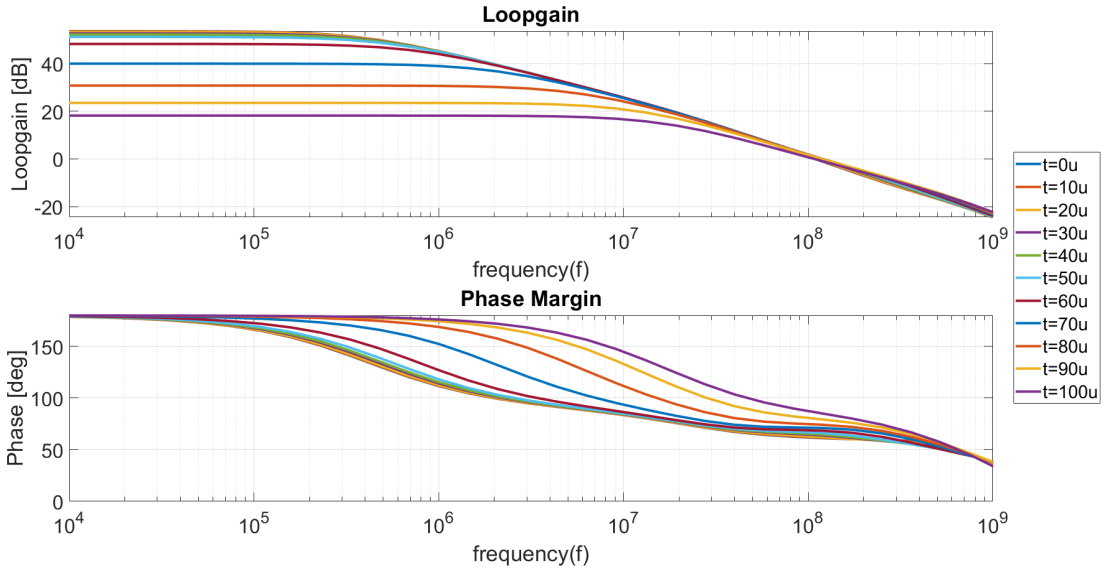


Figure 5.6: Loopgain and phase of the common mode feedback loop

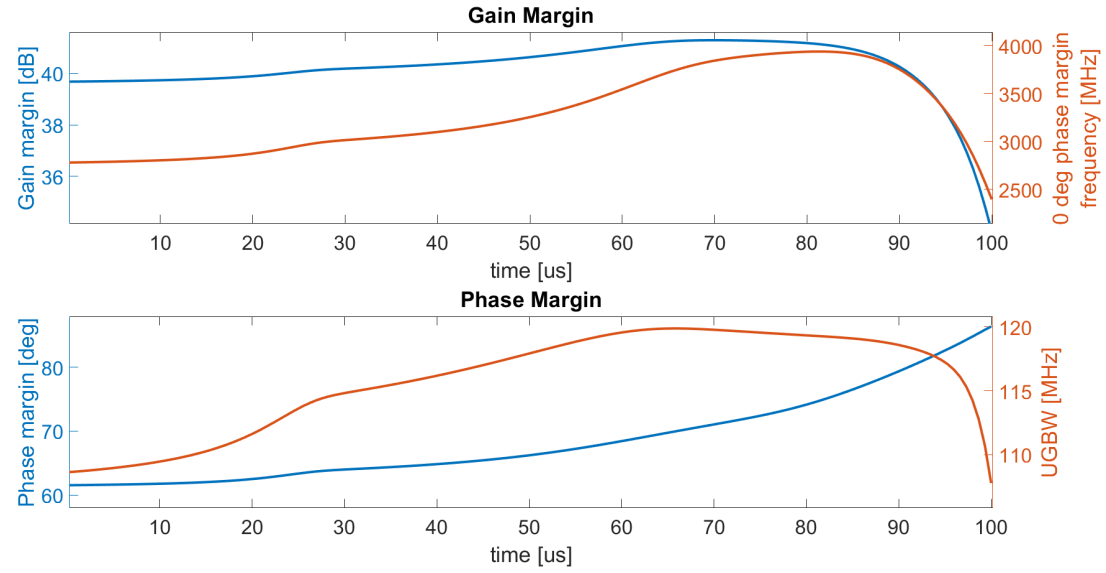


Figure 5.7: Gain margin and phase margin of the common mode feedback loop

5.4. Transient response

Figures 5.8 to 5.10 show the different transient responses of the combined TGC-LNA.

To vary the gain the feedback network is controlled by a pre-charged capacitor. This capacitor is linearly discharged by a transistor operating in the triode region. Figure 5.8 shows the control voltages necessary for the different branches as a function of time. As there are three different branches in the feedback network, three different control voltages are required. The initial control voltage is set to be two volt for each feedback branch. With only a 1.8 V supply voltage the 2 V control voltage is achieved by pre-charging a floating capacitor.
From Figure 5.8 it can be observed that each control signal shows a linear discharge at a different rate. This is required such that each feedback branch is dominating the total feedback impedance during its intended gain range.

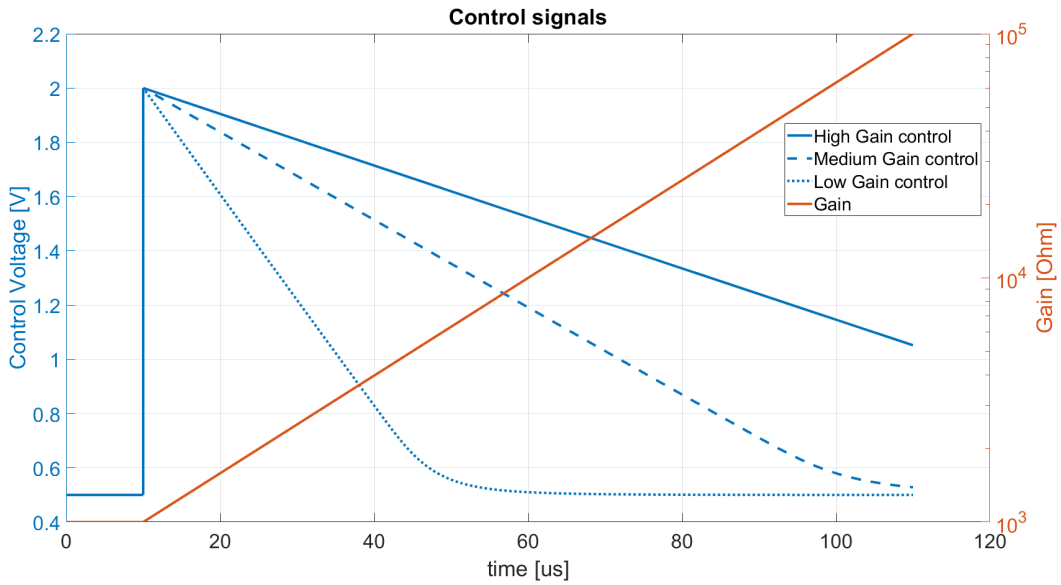


Figure 5.8: Feedback network control signals

Two different simulations are conducted to be able to assess the transient behaviour of the combined TGC-LNA amplifier. The first simulation tests the transient response on a fixed sinusoidal signal with a frequency equal to the center frequency of 7.5 MHz. This simulation is performed to assess the instantaneous performance of the amplifier at certain gain settings. The second simulation tests the overall transient performance for the entire duration of the receive period.

Figure 5.9 shows the instantaneous transient behaviour of the amplifier. To test the instantaneous transient performance the control signals of Figure 5.8 are fixed at certain time instants, after which a single 7.5 MHz sinusoidal input current is amplified. The magnitude of the input current changes proportional to the exponentially decreasing input signal of the ultrasound transducer. Figure 5.9 shows that over time the input current signal changes from a 50 μA amplitude to 0.5 μA, but the output voltage amplitude stays roughly constant. This means that a time gain compensation amplification is successfully performed. Section 5.5 covers the distortion behaviour of this simulation.

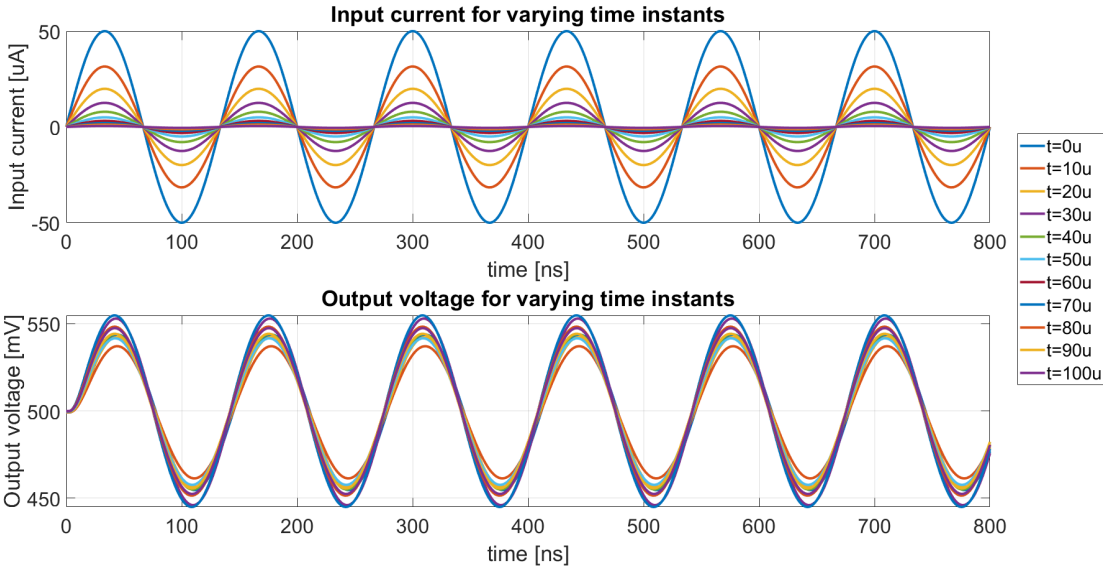


Figure 5.9: Input current and Output voltage simulated at certain time instants of the gain range

Figure 5.10 shows the transient behaviour for an exponentially decaying sinusoidal signal. In this simulation not only the varying feedback network is changed, but also the bias current of the first stage is altered over time. It shows that for a 40 dB variation of the input current amplitude the output voltage amplitude varies much less, with an amplitude variation between 43-56 mV.

There are three observations that are important for the assessment of the TGC performance. First of all, with a 40 dB varying input current the output voltage dynamic range is much smaller than the input signal as is expected of the time gain compensation functionality. Even though a TGC functionality is implemented ideally a constant output voltage amplitude is desired, which is clearly not the case. This can be attributed to the fact that the control voltages are linearly declining over time instead of the ideal exponential decay. Using resistors instead of triode transistors the gain curve can be optimized at the cost of larger die area requirements.

The transient output voltage shows a recurring gain variation profile. This is to be expected as there are three different feedback branches that are all dominant at different time intervals. As long as the signal to noise ratio is not degraded by the output variation the output variation can be dealt with in post processing.

Lastly it can be noticed that the gain of the amplifier is lacking at the start of the receive period. This is the case as the bias current of the first stage is very low, meaning that the loopgain is quite small. This means that the virtual AC ground at the input of the amplifier is no longer functioning as a real AC ground, but has a voltage swing on it. This could be prevented by increasing the bias current at the starting point of the receive period. An increased bias current would, however, cause the UGBW to vary more.

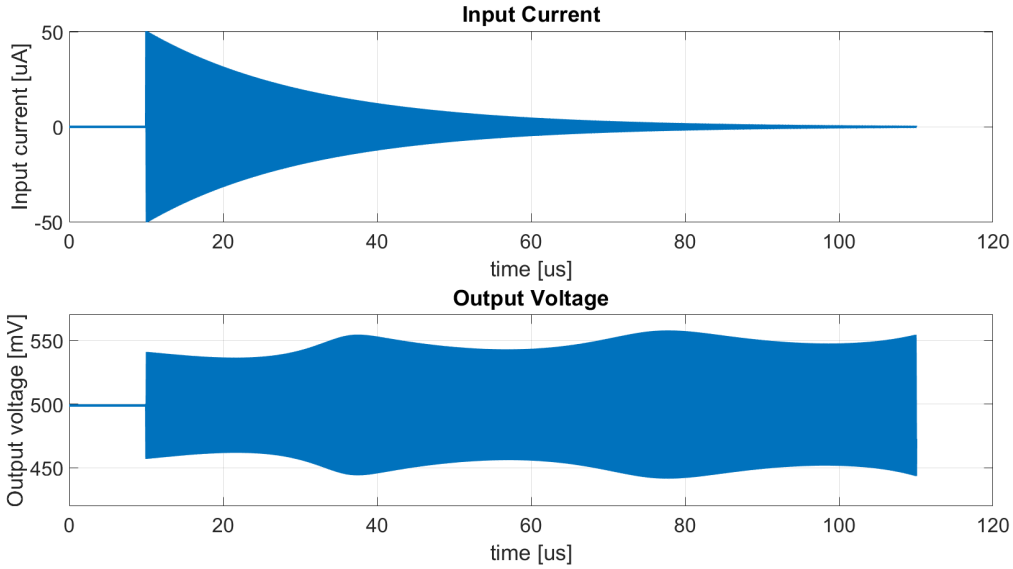


Figure 5.10: Transient response TGC-LNA

5.5. Gain accuracy and Distortion

Looking at the transient response of Figure 5.10 it looks like the amplitude of the output voltage swings by quite some margin. However, the gain error, computed in dB is actually quite small. Figure 5.11 shows the simulated gain results compared to the ideal exponential gain curve. The gain error is computed to be between -1.8 dB +1 dB. The gain error is a systematic error that can be accounted for in the external post processing. This, however, is only the case when the total dynamic range reduction is large enough, such that the SNR will not be degraded by subsequent ADCs. The goal of the TGC amplifier is to decrease the overall dynamic range by 40 dB. Given the gain variation shown in Figure 5.11, the total dynamic reduction is approximately 4 dB less than ideal. Still 36 dB is good enough, such that the subsequent ADCs are capable of handling the signals dynamic range.

When optimizing the gain curve in future work, again changing the control signals of Figure 5.8 into exponentially decaying signals minimizes the gain error. This would require the in saturating operating discharge

transistors to be substituted for resistors, such that the control signals will decrease exponentially over time at the cost of extra die area.

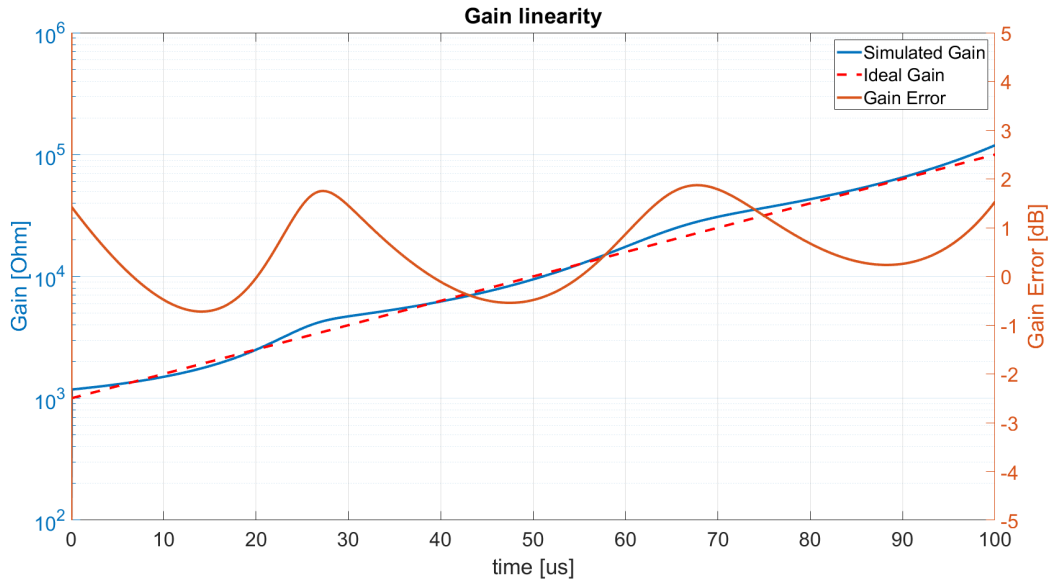


Figure 5.11: Gain accuracy

Even though Figure 5.11 suggests that the TGC amplifier functions properly, a dynamic range reduction would be meaningless if the signal was distorted, such that the all information is lost. To keep the information loss to a minimal the total harmonic distortion allowed is set to be -40 dB. Figure 5.12 shows both the output spectrum for different time instants as well as the THD as a function of time. It can be observed that the THD stays below -45 dB for the entire duration of the receive period. The distortion behaviour of the combined TGC-LNA thus meets the specifications.

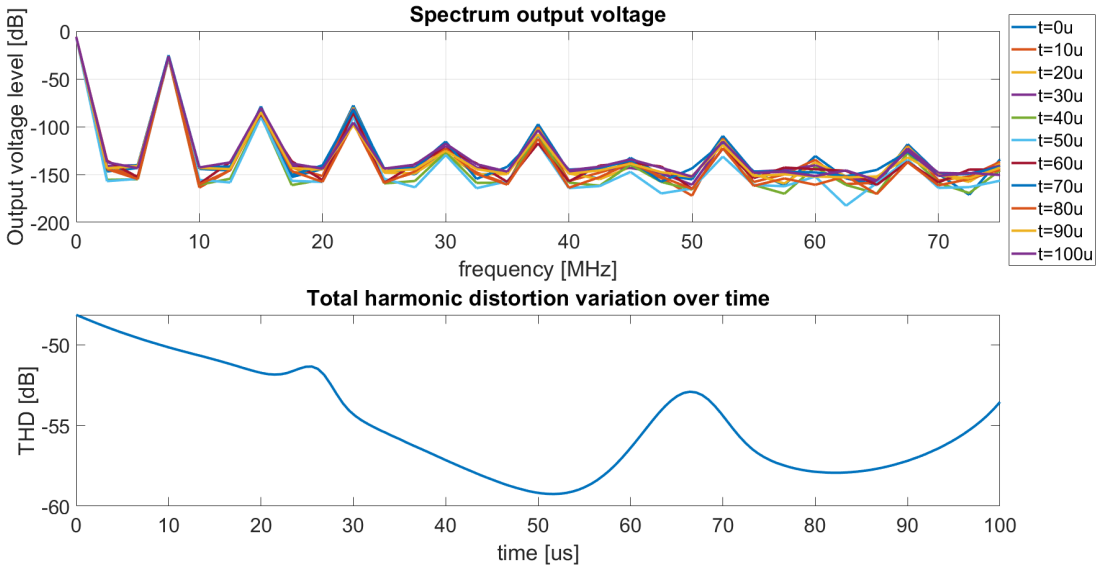


Figure 5.12: Output spectrum and total harmonic distortion

5.6. Noise Performance

The previous sections show that the combined TGC-LNA amplifier meets the specifications for the time gain compensation functionality. This section covers the low noise performance of the design.

5.6.1. Feedback network

Equation 3.8 suggests that the total noise of the feedback network can be modelled as the current noise of an equivalent resistor. The noise budget for the loop amplifier is based on this model and it is therefore important to simulate the validity of the model. Figure 5.13 compares the noise of the feedback network to the noise of the equivalent resistor as a function of time. It shows that equation 3.8 is indeed an appropriate model for the noise of the feedback network.

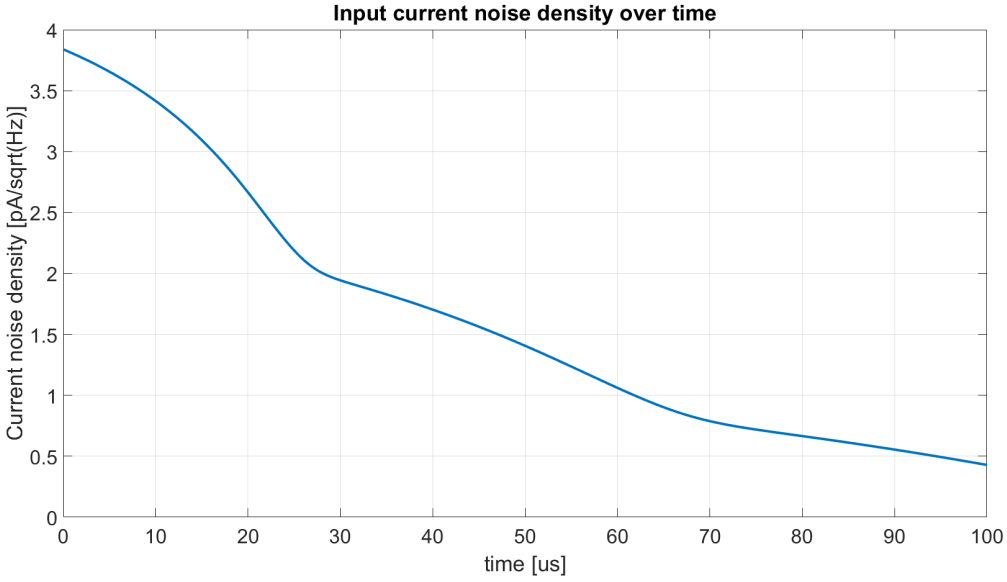


Figure 5.13: Input referred current noise density generated by the feedback network

5.6.2. SNR

The noise of the feedback network leaves the designed noise budget for the main loop amplifier. Figure 5.14 shows the total input- and output-referred noise density of the combined TGC-LNA amplifier. The noise specification is set, such that the noise of the amplifier should be less than the noise coming from the input transducer. The spot noise of the input transducer at the center frequency is 1 pA/$\sqrt{\text{Hz}}$. At the highest gain setting the noise density simulated is 1.12 pA/$\sqrt{\text{Hz}}$, which means that the spot noise specification is almost met at this gain setting. For lower gain settings the noise performance is met as the input signal amplitude increases proportionally with the feedback resistance, while the noise increases with the square root of the feedback resistance. This means that for lower gain settings the signal amplitudes rise faster than the noise, increasing the SNR.

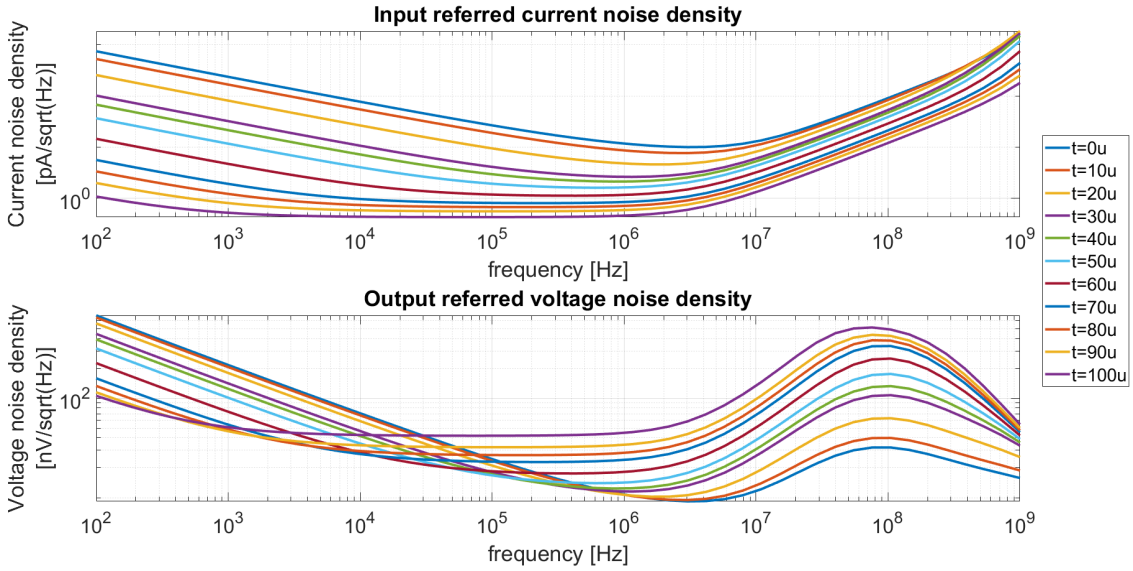


Figure 5.14: Input and output referred noise densities

Even though the spot noise density performance is not entirely met, the total noise power of the TGC-LNA amplifier is less than that of the input transducer. Integrating the simulated noise density over the bandwidth of interest and comparing it to the input signal the SNR can be computed. Figure 5.15 shows the signal to noise ratio of the amplifier as a function of time. As expected, the worst SNR of 43 dB is at the highest gain setting at the end of the receive period. Integrating the 1 pA/$\sqrt{Hz}$ over the same bandwidth of interest gives a SNR of 35 dB. This means that even though the spot noise at the center frequency is larger for the TGC-LNA amplifier, the total in-band noise power is less than that of the input transducer.

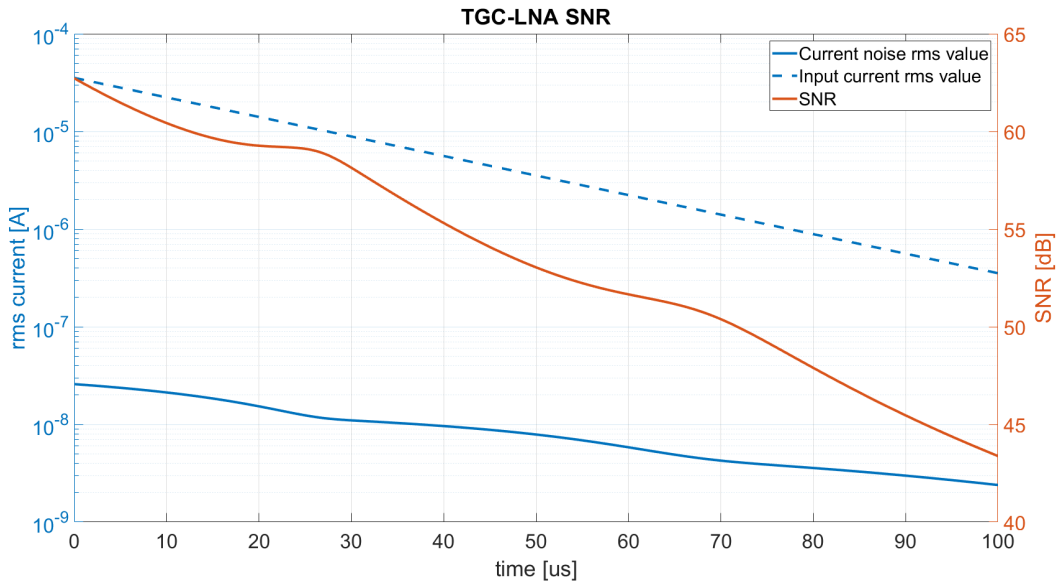


Figure 5.15: Input referred SNR, excluding noise coming from the input transducer

To improve on the noise performance of the combined TGC-LNA amplifier, mainly two options are available. The first is to increase the power consumption by increasing the bias current of the first stage. Increasing the bias current increases the input transconductance which lowers the input referred noise of the loop amplifier.

The second option is to change the architecture of the first stage to fit that of a current re-use amplifier. This

would require not only a PMOS differential input pair, but also a NMOS differential pair. As the input voltage is quite low at 500 mV a DC voltage shift is needed. As this is often implemented using a floating capacitor, an increased noise performance comes at the price of a larger die area.

5.7. Power

The combined TGC-LNA amplifier meets most of the performance specifications. However, the power consumption should not outweigh the performance achieved. Figure 5.16 shows the instantaneous and average power consumption during the receive period. As expected the instantaneous power shows an approximately exponential behaviour as the first stage bias current changes exponentially over time.
The average power consumption is simulated to be 5.5 mW. This is a comparable power consumption when compared to the 5.2 mW as presented in [10], which uses the same input transducer.

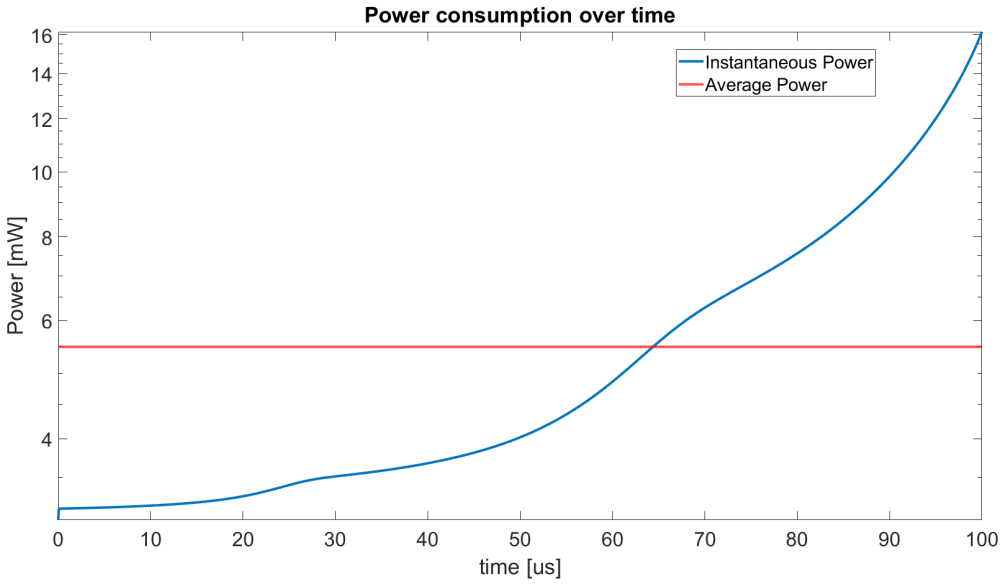


Figure 5.16: TGC-LNA total power consumption during receive phase

5.8. Estimated Area

The estimation of the total required die area is based on the transistor dimensions of Table 4.1 and the total capacitance required for the feedback network. The estimated area represents the die area required for a single TGC-LNA unit. In this estimation the area required for the bias network is left out. This is done as a single bias network can bias multiple TGC-LNA units and therefore does not need to be placed together with every TGC-LNA.

Using Table 4.1 the total area requirements for the transistor channel area is about 1800 μm^2. Given that this only includes the channel area, thus excluding the area required for the drain and the source connections and excluding the interconnect, it can be assumed that the total required area for the TGC-LNA is much larger than the 1800 μm^2. Assuming that the channel area is about 40% of the total required transistor and interconnect area, the TGC-LNA requires about 4500 μm^2.

As stated in section 3.7 the total required capacitance for the feedback network is 21 pF. Using MIM capacitors the capacitance per unit area is about 5 fF/μm^2. Given the 21 pF of the feedback network, the total required area for the MIM capacitors is 4200 μm^2. There should be room available for shielding the capacitors from each other and interconnect. Assuming a 20% overhead, the total area required is about 5250 μm^2 for the MIM capacitors.

The total area requirements can be computed in two ways. One method puts the MIM capacitors and the TGC-LNA next to each other, requiring $5250 + 4500 \approx 10000$ $\mu m^2 = 0.01$ mm^2 for the total chip.

The other method makes use of the fact that the MIM capacitors can be stacked on top of the amplifier in higher metal layers. This reduces the total area requirements by approximately half to 0.005mm^2. When the MIM capacitors are placed on top of the transistors sufficiently shielding is required, such that the MIM capacitors do not load the amplifier.

6

Conclusion and Discussion

6.1. Conclusion

This work has presented a new method of combining a TGC amplifier together with a LNA for ultrasound imaging applications. A transimpedance amplifier with an exponentially varying feedback resistance has been designed to obtain a 40 dB gain range. The TGC-LNA achieves a 1.12 pA/$\sqrt{\text{Hz}}$ input-referred noise density at the cost of 5.5 mW power consumption and an estimated 0.01 mm^2 die area. The non-linearity is limited to a THD of -44 dB.

The design of the combined TGC-LNA amplifier is simplified by using a negative feedback amplifier architecture. Using this architecture both the low noise functionality and the TGC functionality can be separately designed for.

The feedback network is responsible for the TGC functionality of the TGC-LNA. To this end the feedback network consists of three branches, each responsible for a part of the total 40 dB gain range. Each branch consists of two transistors operating in the triode region that are configured such that distortion and die area requirements are minimized. An internal capacitive discharge circuit takes care of the voltage signals capable of setting the time-varying gain. This means that there is no external ramp voltage required as a control signal.

The feed forward path, consisting of a two-stage loop amplifier, takes care of the low noise functionality of the TGC-LNA. This is the case as the feedback network has such a high resistance that noise from the feedback network is small in comparison to the loop amplifier. Even though the first stage is designed with the design focus on its noise performance it also plays an important role in both the power consumption as well as the stability performance. With a varying bias current, based on the total feedback resistance, the unity gain bandwidth variation is limited to a minimum, while power is being saved.

Overall the combined TGC-LNA achieves a 40 dB total gain range, while the dynamic range reduction of the input signal is approximately 36 dB. Table 6.1 shows a comparison of the work presented in this thesis to a similar work in literature. It should be noted that the estimated die area of this work is based on the transistor sizes of the loop amplifier and total capacitance requirements of the feedback network for a single TGC-LNA. It is often difficult to compare the performance of one amplifier with others in literature as the required performance is highly dependent on the type of ultrasound transducer used in said work. However, in [10], the same transducer is used and it can be concluded that this work competes in achieved performance with that of the literature. At the cost of a bit higher power consumption a lower simulated noise performance is achieved while reducing the area requirements by a factor of about 10. The linearity performance is not covered in [10] and can therefore not be compared.

Table 6.1: Performance comparison

	This Work*	[10]
Process	**0.18 μm HV BCDMOS**	0.18 μm HV BCDMOS
Bandwidth	**5 MHz**	7 MHz
Max gain	**105 dBΩ**	107 dBΩ
Full gain range	**41 dB**	37 dB
Gain error	**-1.8 to +1 dB**	$\pm$1 dB
Gain control	**Continuous**	Continuous
Input capacitance	**18 pF**	18 pF
Noise density at center frequency	**1.12 pA/$\sqrt{\text{Hz}}$ @7.5 MHz**	1.7 pA/$\sqrt{\text{Hz}}$ @5 MHz
Power	**5.5 mW**	5.2 mW
Worst THD	**-44 dB**	—
Die Area	**0.01 mm^2 ****	0.12 mm^2

*** Simulation Results**
**** Estimated Die Area**

6.2. Discussion and Future Work

Most of the performance requirements for the TGC-LNA are met in simulations. Still, there are some performance aspects that require further attention. The next sections cover the necessary steps remaining for a successful prototype and possible future work on improving the TGC-LNA performance.

6.2.1. Remaining Prototype Implementation steps

This work is still in its experimental phase. The road to a successful prototype needs to cover at least the following steps.
First of all the bias circuitry for constant bias circuits has been ideal and remains to be designed for any tape-out. In addition to the constant current bias circuitry, the varying bias current generation circuit is still in need of an optimized loop amplifier that allows for a stable loop control.

The stability of the main amplifier loop remains a concern worth looking into. Due to the large transimpedance gain and the large input pole variations over time, the system is quite susceptible to stability issues. In this work the stability issues are taken care of by means of resistive broadbanding. Before any prototype can be manufactured, corner simulations are necessary to show if the loop remains stable over PVT variations. The same goes for capacitive parasitics. Given the large feedback resistances the complete system can be quite susceptible for parasitic capacitances. When designing the layout of the ASIC these parasitics must be taken into account. This can be done either by shielding the signal path from parasitics or simulations show that the resistive broadbanding is sufficient for keeping the loop stable.

6.2.2. Future Work

After this work has been prototyped, there is still room for optimization and improvement on the design. In future work the following changes can be applied to improve on the design.
First the gain control can be varied to obtain a better approximation of the ideal exponential gain curve. Due to the linear variation of the control voltages the gain curve shows some variation over time, resulting in a smaller dynamic range reduction as designed for. Using resistors instead of transistors operating in saturation, the gain variation would show a better approximation of an exponential curve. However, the cost of it would be a larger die area. With MIM (Metal insulator Metal) capacitors the same die area can be used for both the resistors and capacitors. This means that using resistors the die area does not necessarily have to increase significantly. If the extra area costs are acceptable for the application, then using resistors instead of transistors operating in saturation might outperform the current implementation.

The second improvement that can be made deals with the noise performance. As shown in chapter 5 the SNR is not degraded by the noise of the amplifier. However, the spot noise density at the centre frequency is a fraction larger than the requirements state. To improve on the noise performance the first stage of the amplifier can be

altered to become a current re-use amplifier or the power consumption should rise. This results in either a higher power consumption or larger die area requirements as a current re-use amplifier requires a DC voltage shift, which is implemented using a floating capacitor.

A

Appendix

A.1. Architecture Design

A.1.1. Transducer Model

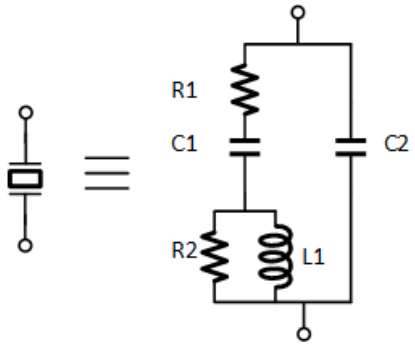


Figure A.1: Generalized Van Dyke model used to model the input CMUT transducer

Figure A.1 shows the model used for the ultrasound transducer, which is loading the input of the TGC-LNA. The impedance can expressed as follows:

$$Z = \left(R_1 + \frac{1}{sC_1} + R_2 \parallel sL_1 \right) \parallel \frac{1}{sC_2} \tag{A.1}$$

$$Z = \left(\frac{R_2 + s\left(L_1 + R_2C_1 + R_1R_2C_1\right) + s^2L_1C_1\left(1 + R_1\right)}{sR_2C_1 + s^2L_1C_1} \right) \parallel \frac{1}{sC_2} \tag{A.2}$$

$$Z = \frac{R_2\left(C_1 + C_2\right) + s\left(L_1\left(C_1 + C_2\right) + R_2C_1C_2 + R_1R_2C_1C_2\right) + s^2L_1C_1\left(C_2 + R_1C_2\right)}{sR_2C_1C_2 + s^2L_1C_1C_2} \tag{A.3}$$

Using equation (A.3) together with the parameter values of the CMUT as shown in Table A.1 the impedance characteristics of the transducer can be plotted as a function of frequency. Figure A.2 shows that the capacitive branch containg C_2 dominates the total impedance within the operating frequency range. At the center frequency of 7.5 MHz the transducer impedance is about 1.2k Ω.

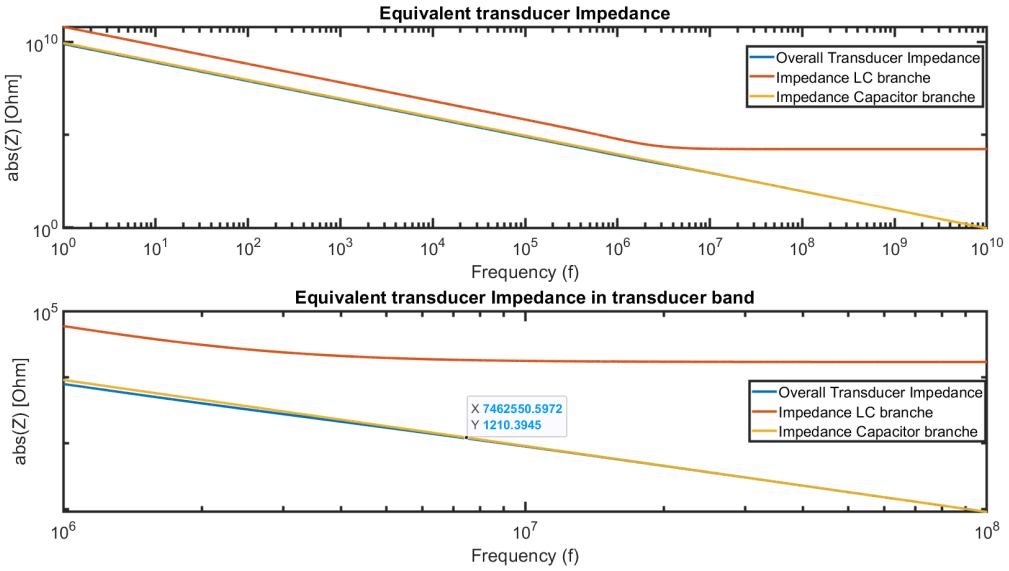


Figure A.2: Electric impedance characteristics CMUT

Table A.1: Van Dyke model parameters

Component	Value
R_1	1.1mΩ
R_2	16.9kΩ
C_1	2.38pF
C_2	17.62pF
L_1	3.1mH

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