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A 19.8 mW Eddy-Current Displacement Sensor Interface with Sub-Nanometer Resolution

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***Abstract*—This paper presents an eddy-current sensor (ECS) interface intended for sub-nanometer displacement sensing in hi-tech applications. The interface employs a 126 MHz excitation frequency to mitigate the skin-effect, and achieve high resolution and stability. An efficient on-chip sensor-offset compensation scheme is introduced which removes sensor-offset proportional to the standoff distance. To assist in the ratiometric suppression of noise and drift of the excitation-oscillator, the ECS interface consists of a highly linear amplitude-demodulation scheme that employs passive capacitors for voltage-to-current conversion. Using a PCB-based pseudo-differential ECS, stability tests were performed which demonstrated a thermal drift of < 7.3 nm/$^\circ C$ and long-term drift of only 29.5 nm over a period of 60 hours. The interface achieves an effective noise floor of 13.4 $pm/\sqrt{Hz}$ which corresponds to a displacement resolution of 0.6 nm in a 2 kHz noise-bandwidth. The ECS interface is fabricated in TSMC 0.18 μm *CMOS* technology and dissipates only 19.8 mW from a 1.8 V supply.**

***Index Terms*—inductive, eddy-current, sensor, displacement, amplitude demodulation, oscillation, chopping.**

I. Introduction

Sub-nanometer (sub-nm) displacement sensing is one of the most important requirements in advanced metrology and high-tech industries e.g. wafer scanners and relay mirror experiment (RME) [1]. Incremental sensors, such as linear encoders and interferometers, possess high resolution and therefore are frequently used in these applications. However they are bulky and costly. Absolute sensors, such as capacitive and inductive sensors, can compete with incremental sensors in these applications because the typical measurement range (Δx_{max}) is small: in the order of few micrometers.

Capacitive sensors [2], [3], though compact with high resolution, require electrical access to the target, which is often an issue. They are also sensitive to environmental conditions such as humidity, dirt etc. Eddy-current sensors (ECSs), on the other hand, are immune to these disadvantages, but their stability is limited by the skin-effect [4], [5]. Since eddy-current is induced deep with in the target, the effective displacement sensed by an ECS is dependent on the skin-depth δ $(= 1/\sqrt{\pi\mu\sigma f_{exc}})$, where μ is the magnetic permeability, σ is the electrical conductivity and f_{exc} is the excitation frequency of the ECS. Hence a change in skin-depth can be taken as an apparent displacement. For instance, a temperature change of 1 $^\circ C$ in a copper target can cause displacement errors of $\approx$ 100 nm when f_{exc} is 1 MHz. To attain sub-nm measurements, the temperature has to be controlled with an accuracy of 1 mK which is often not possible. A practical way to obviate this instability issue is to use a higher excitation frequency ($f_{exc} > 100$ MHz) in the ECS interface [5]–[7].

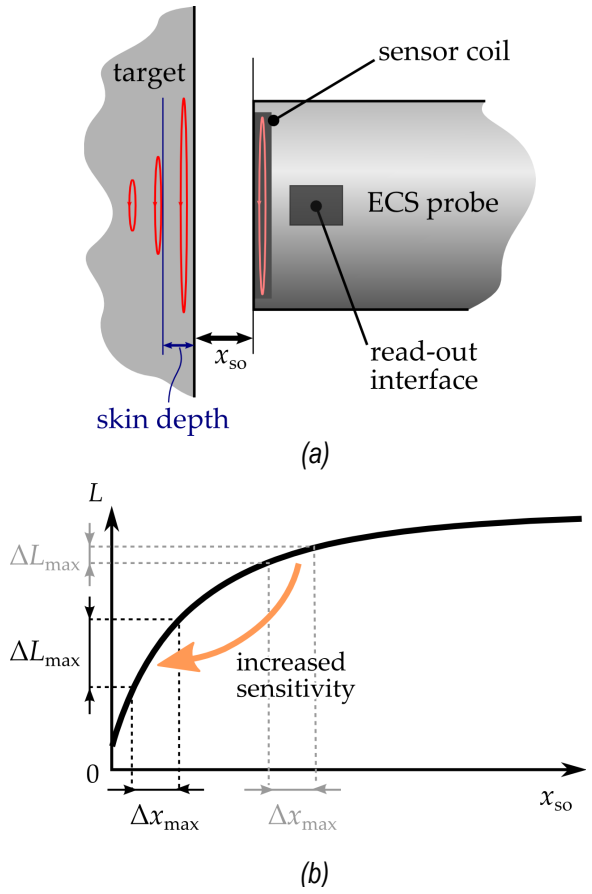

Fig. 1. Sub-nm ECS interface (a) Readout chip integrated in the sensor probe. (b) Small x_{so} improves sensitivity and sensor-to-offset ratio.

However, it is not trivial to increase the excitation frequency in present ECS interfaces. This is largely due to the: (a) use of large ECS coils ($L > few\ \mu H$); (b) large parasitic inductance (L_{par}) of the cable between the ECS coil and readout circuitry; and (c) high power dissipation in the readout circuitry [8], [9]. Large ECS coils typically have low stability and a low self-resonance frequency (*SRF*). The parasitic inductance L_{par} of

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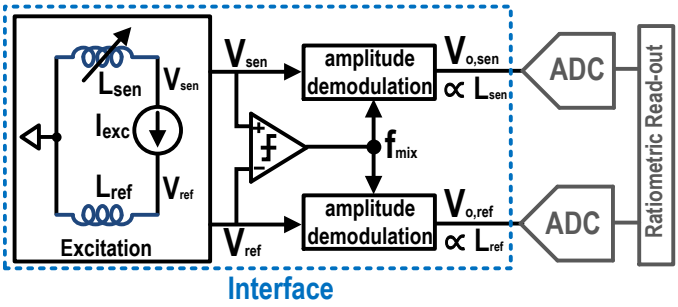

Fig. 2. Conceptual block diagram of the ECS interface.

the cable, between the ECS coil and the readout circuitry, degrades the sensitivity and exacerbates the dynamic range by adding offset inductance. Parasitic inductance also degrades the stability of the ECS interface. The readout circuitry is typically not monolithic and dissipates a large amount of power ($>$ 500 mW). This makes it difficult to remove the cable between the ECS coil and the readout circuitry because self-heating can cause large displacement errors due to thermal expansion [10]–[12].

A sub-nm ECS must use a stable flat sensing coil (with high SRF) in close proximity to the ECS interface, the power dissipation of which must then be low enough ($<$ 20 mW) to avoid self-heating and displacement errors due to thermal expansion. A monolithic solution for the readout circuitry is attractive for a compact ECS interface with low power dissipation. The conceptual diagram of such an ECS interface is shown in Fig. 1(a), where a power-efficient monolithic readout interface is integrated into the sensor probe to obviate a large L_{par}.

Mechanical assembly poses another challenge for ECSs [5]. Although sub-nm resolution must be achieved over a displacement range (Δx_{max}) of only a few micrometers, the nominal stand-off distance (x_{so}) to the target is often a few hundreds of micrometers due to mechanical assembly tolerances. There are two issues with a large standoff distance: (a) low sensitivity due to non-linear characteristics of the sensor (Fig. 1(b)) which necessitates lower noise from the readout circuitry; (b) large sensor-offset ($\propto x_{so}$) which exacerbates both the dynamic range (DR) and non-linearity of the ECS interface. Thus, a smaller x_{so} is attractive as it improves sensitivity and the signal-to-offset ratio of the system.

A conceptual block diagram of a pseudo-differential ECS interface is shown in Fig. 2 which performs three important functions: excitation, demodulation and ratiometric readout. ECS coils, a sensor coil L_{sen} and a reference coil L_{ref}, are excited by a high frequency excitation current I_{exc}. This produces two voltages V_{sen} and V_{ref}, the amplitudes of which are directly proportional to L_{sen} and L_{ref} respectively. Oscillator outputs are amplitude-demodulated to generate baseband voltages $V_{o,sen}$ and $V_{o,ref}$, using a synchronous clock ($f_{mix} = f_{exc}$). These voltages are digitized and their ratio is calculated to compute $D_{out} = L_{sen}/L_{ref}$, which gives the measure of the displacement. The amplitude is chosen as the carrier of the displacement information due to higher sensitivity when compared to the frequency or losses in the LC resonator [13]–[15].

Self-oscillation is found to be a power-efficient way to generate I_{exc} and to excite ECS coils at a high f_{exc} [16]. However, noise and drift of the front-end excitation-oscillator are important concerns. Ratiometric measurement helps in suppressing these because of their correlated-multiplicative (CM) nature. However, the efficacy of this suppression is limited by the presence of any non-linearity, e.g. due to g_m stages, in the demodulator [4], [17]. It is also more difficult to attain high linearity ($>$ 70 dB THD) at a high f_{exc}. The non-linearity of the demodulator is further exacerbated due to the presence of large input offsets caused by a large x_{so} and L_{par}. To maintain the efficiency of ratiometric measurements in suppressing the noise and drift of the excitation-oscillator, linear amplitude-demodulation and on-chip sensor-offset compensation are indispensable.

In this work, we present an ECS interface with displacement resolution of 0.6 nm in a 2 kHz noise-bandwidth, with a power consumption of only 19.8 mW [18]. This is achieved by: (a) exciting ECS coils with a high f_{exc} (= 126 MHz) to alleviate the performance degradation caused by the skin-effect; (b) utilizing capacitors for voltage-to-current (V2I) conversion to obviate the use of non-linear g_m blocks in the demodulator and perform linear amplitude-demodulation; (c) introducing an on-chip sensor-offset-compensation scheme to remove the sensor-offset ($\propto x_{so}$), without degrading the efficacy of the ratiometric suppression of the excitation-oscillator's noise and drift.

The paper is organized as follows. Section II discusses the architecture of the ECS interface, along with the proposed sensor-offset compensation scheme. Section III shows the circuit implementation of important blocks of the interface. Section IV discusses experimental results achieved from the ECS interface prototype. Section V summarizes the performance and concludes the paper.

II. ECS Interface

A. Architecture Overview

Figure 3 depicts the detailed system architecture of the ECS interface. The interface consists of two channels: a sensor-channel and a reference channel. These process voltage amplitudes directly proportional to the sensor coil L_{sen} ($= L_{so} \pm \Delta L(x)$) and the reference coil L_{ref} ($= L_{so}$) respectively, where L_{so} is the value of L_{ref} (and L_{sen}) at the nominal standoff x_{so}. The excitation of ECS coils is achieved with a PMOS-based self-oscillating front-end [16] which comprises of L_{ref}, L_{sen} and a tank capacitance C. The excitation frequency generated by them is given by $f_{exc} = 1/2\pi\sqrt{(L_{sen} + L_{ref}) * C}$. The voltage swings of the excitation-oscillator outputs V_{sen} and V_{ref} are controlled by a digitally programmable tail-current source $I_{ss,osc}$.

The excitation-oscillator outputs V_{sen} and V_{ref} are converted into currents I_{sen} and I_{ref} using capacitors C_{in} and C_{ref}. The low input-impedance of the transimpedance amplifier (TIA) is exploited for this. A clock f_{mix} synchronous to I_{sen} and I_{ref} (but in quadrature to V_{sen} and V_{ref}) is generated using a fast continuous-time comparator. Currents I_{sen} and I_{ref} are demodulated to zero intermediate-frequency

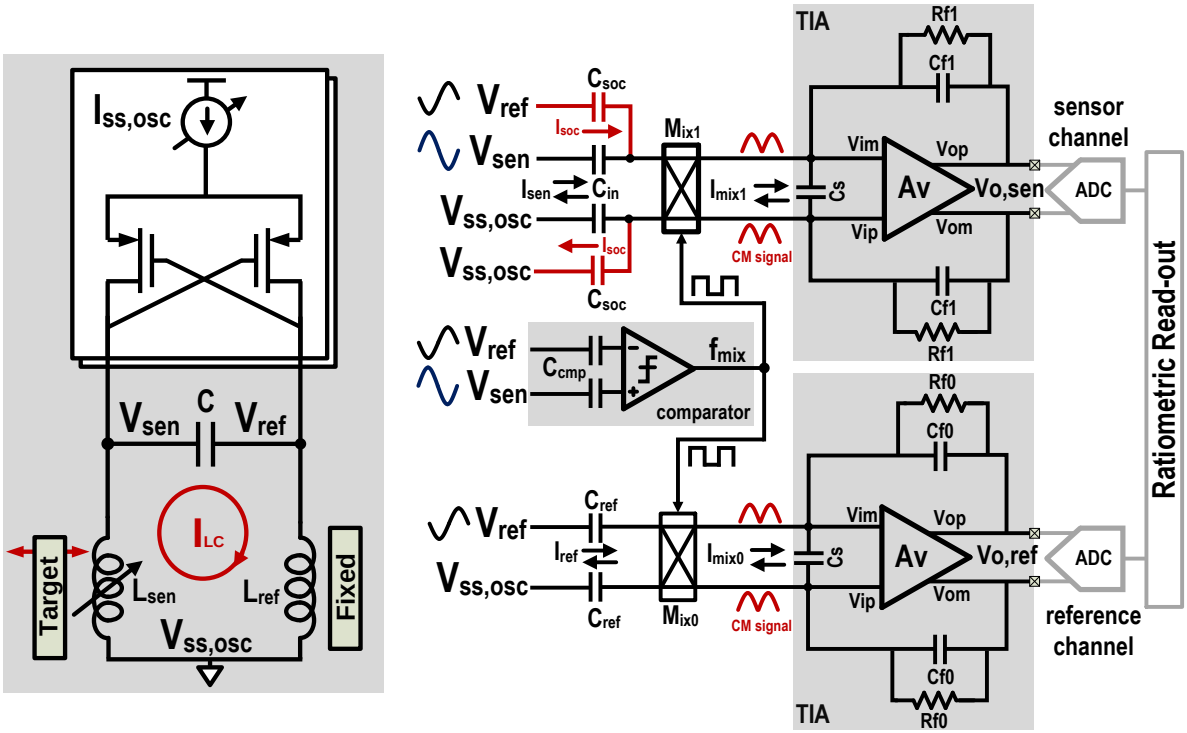

Fig. 3. Architecture of the ratiometric ECS interface with (a) excitation oscillator and (b) two channel amplitude-demodulation.

(IF) using passive current-mixers M_{ix1} and M_{ix0} [19]. TIAs amplify and filter demodulated currents I_{mix1} and I_{mix0} to generate baseband voltages $V_{o,sen}$ and $V_{o,ref}$. These voltages are digitized and a ratiometric readout $D_{out} = V_{o,sen}/V_{o,ref}$ is performed to suppress the drift and noise of the excitation-oscillator.

B. Sensor-offset compensation

As shown in Fig. 1(b), the maximum sensor-inductance change ΔL_{max} is usually a small fraction of the standoff inductance L_{so} ($\propto$ x_{so}). Hence I_{sen} consists of a large signal proportional to L_{so} (and x_{so}), along with the useful displacement information in $\Delta L(x)$. This offset signal degrades the linearity of the demodulator and therefore must be compensated for before being amplified.

The proposed ECS interface leverages the anti-phase relationship between the sensor and reference coil voltages for sensor-offset-compensation. To mitigate sensor-offset, V_{ref} is used to generate a compensation current I_{soc} through capacitor C_{soc} (= C_{in}). This current is added to I_{sen} at the input of M_{ix1}. The TIA output $V_{o,sen}$ then depends only on $\Delta L(x)$. The signal gain in the reference channel is scaled down by a factor β (= $\Delta x_{max}/x_{so}$) with C_{ref} = $\beta * C_{in}$ so that the reference channel output $V_{o,ref}$ corresponds to only the maximum inductance change ΔL_{max} and not L_{so}. The modified ratiometric readout D^*_{out} is given by,

$$D^*_{out} = \frac{V_{o,sen}}{V_{o,ref}} = \frac{|V_{sen}| - |V_{ref}|}{\beta \cdot |V_{ref}|} = \frac{\Delta L(x)}{\beta \cdot L_{so}} = \frac{\Delta x}{\Delta x_{max}} \quad (1)$$

where $V_{o,sen}$ and $V_{o,ref}$ are the output of the sensor and the reference channel respectively, $|V_{sen}|$ and $|V_{ref}|$ are the amplitudes of the two outputs of the oscillator. Due to the proposed sensor-offset-compensation technique, the sensor channel output $V_{o,sen}$ is proportional to $|V_{sen}| - |V_{ref}|$ i.e. $\Delta L(x)$ and does not depend on the standoff inductance L_{so}.

The choice of using V_{ref} for the sensor-offset compensation is important. Current I_{soc}, generated from V_{ref} using capacitor C_{soc}, contains all CM terms of the excitation oscillator and hence preserves the functionality of the ratiometric readout in suppressing them after sensor-offset compensation. This would not be possible if the compensation current is not generated from the excitation-oscillator itself. Figure 4 depicts the working principle of the sensor channel, with sensor-offset-compensation, for the case L_{sen} > L_{ref} i.e when the target is farther from the nominal standoff position.

III. Circuit Implementation

A. Front-end Excitation Oscillator

This section discusses the implementation of the excitation-oscillator of the ECS interface. As shown in Fig. 5, a PMOS-based cross-coupled LC oscillator structure is employed. Off-chip ECS coils L_{sen} and L_{ref} form a resonator along with the on-chip capacitor C. The voltage swing can be calculated as:

$$|V_i| = j \cdot 2\pi \cdot f_{exc} \cdot L_i \cdot I_{LC} \quad (2)$$

where V_i is the excitation-oscillator output voltage corresponding to the ECS coil L_i, f_{exc} is the excitation frequency

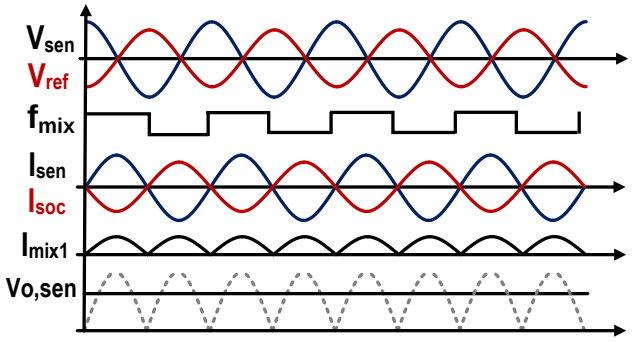

Fig. 4. Working principle of the sensor-channel in the ECS interface.

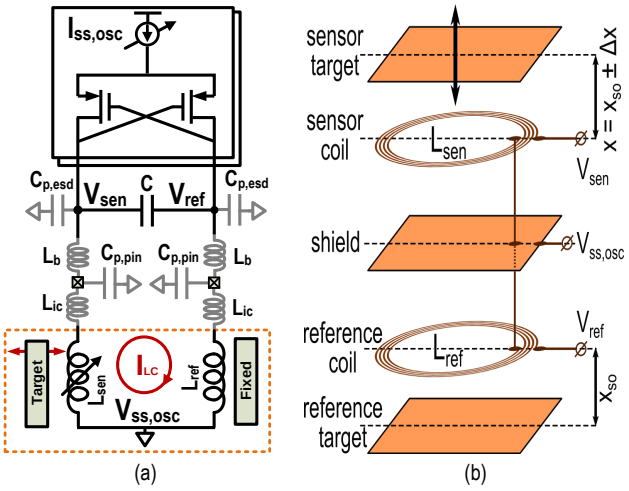

Fig. 5. Self-oscillating front-end to excite ECS coils.

generated by the LC resonator and I_{LC} is the resonance current flowing in the LC tank. I_{LC} can be derived from the excitation-oscillator bias current $I_{ss,osc}$, tank quality factor Q and switching efficiency η [20], [21]. The oscillator bias current $I_{ss,osc}$ is digitally programmable to provide currents from 520 μA to 2.16 mA. The tail current source is cascoded to prevent modulation due to oscillator output swing. One important point to note is that the effective oscillator amplitude-noise also flows through both ECS coils (like I_{LC}) and is suppressed with ratiometric measurement [4].

Since ECS coils are off-chip, care must be taken to minimize various parasitic elements between coils and interface circuitry. Figure 5(a) shows important parasitic components namely: electrostatic discharge (ESD), cell parasitic capacitance $C_{p,esd}$, package-pin parasitic capacitance $C_{p,pin}$, bond-wire inductance L_b, and coil-to-pin interconnect parasitic inductance L_{ic}. ESD cells with 1 KV HBM ESD protection and a small parasitic capacitance ($\approx$ 100 fF) are chosen so that $C_{p,esd}$ is much smaller than the tank capacitance C ($\approx$ 8 pF). A QFN package with a small L_b ($\approx$ 1.5 nH) and $C_{p,pin}$ ($\approx$ 0.3 pF) is used. The matching between two L_bs is attempted by connecting nodes V_{sen} and V_{ref} to pins of the package which are at same angles. One important concern is that L_b can make a high-frequency parasitic resonance loop along with

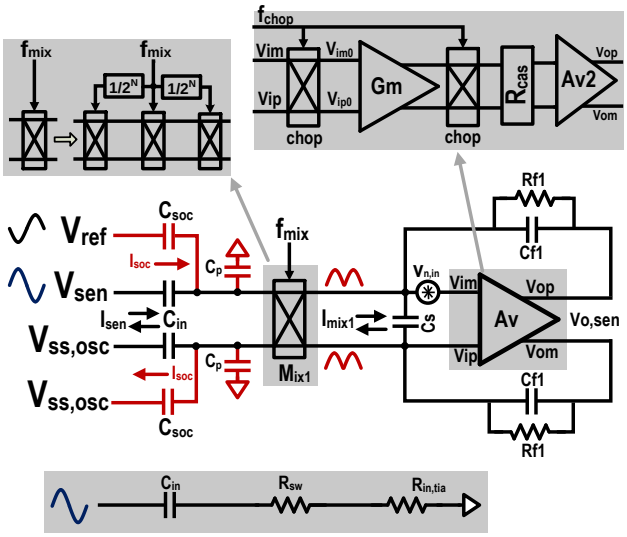

Fig. 6. Architecture of the sensor-channel demodulator.

$C_{p,pin}$ and C. Then, the front-end can start to oscillate at a frequency which is independent of sensor and reference coils. This is obviated by ensuring that the primary LC resonator has a higher Q than parasitic resonators. This also limits the lower bound of the excitation frequency [4].

Figure 5(b) illustrates the conceptual structure of the sensor head. It consists of two coils L_{sen} and L_{ref} of identical geometry. The matching between the sensor and the reference coils is important for the efficacy of the sensor-offset-compensation technique. The coils are shielded from each other using a grounded middle layer to obviate mutual inductance. The thickness of the shield should be at least 6 times higher than the skin-depth at the excitation frequency, to prevent interaction between the two coils. The nominal value of L_{ref} is achieved by positioning a fixed reference target at a nominal standoff x_{so} from reference coil. The nominal standoff for the sensor coil is chosen to be same as x_{so}. This approach has three important advantages: (a) the nominal inductance of both ECS coils is very close at $x = x_{so}$ which helps in accurate sensor-offset compensation, (b) drift in ECS coils, e.g. due to thermal expansion, is suppressed by the ratiometric readout, and (c) the real reference quantity used in the system is the distance between the reference target and L_{ref}. This is attractive because we are sensing displacement and using the reference same as the measurand makes the system inherently more stable [22].

B. Amplitude Demodulation

This section discusses the implementation of the amplitude-demodulation block in the ECS interface. Figure 6 depicts the details of demodulator in the sensor channel. The demodulation in the reference channel is identical to that of the sensor-channel, the only difference being $C_{ref} = \beta * C_{in}$. As explained in Section II, capacitor C_{in} (= 500 fF) is used to generate current I_{sen}. Capacitor C_{soc} ($= C_{in}$) generates I_{soc} from V_{ref} to compensate for the sensor-offset. For this

reason, I_{sen} and I_{soc} are added at the input of M_{ix1} where the impedance is low around f_{exc} [19].

A synchronous clock f_{mix} ($=$ f_{exc}) is used for the amplitude-demodulation. Direct down-conversion to zero IF is chosen to reduce the complexity of the demodulator. However this puts additional constraints on the offset and flicker noise, which are dealt with in this work by employing chopping at various levels [23]. Downconversion mixers and amplifiers in both TIAs are chopped to mitigate their low frequency errors. Unbalanced inputs to the demodulator causes common-mode signals at $2*f_{exc}$ at the virtual ground of the TIA. Capacitor C_s provides low impedance and assists the TIA in suppressing this and higher harmonics of f_{exc}.

1) Capacitors for V2I: As shown in Fig. 6, the demodulation scheme uses passive capacitors (C_{in} and C_{soc}) as V2I blocks. The effective transconductance gain can be calculated as the product of transfer gain of the V2I block and the downconversion mixer, and is given by,

$$G_{m,eff} = 2\pi \cdot f_{exc} \cdot C_{in} \cdot \frac{2}{\pi} = 4 \cdot f_{exc} \cdot C_{in} \tag{3}$$

With f_{exc} = 126 MHz and C_{in} = 500 fF, $G_{m,eff}$ evaluates to 252 $\mu A/V$. This is equivalent to a switched-capacitance-resistor value of $\approx$ 4 $k\Omega$. As an example, for $|V_{sen}|$ = 400 mV and β = 0.1, the maximum current ($\propto \Delta x_{max}$) input to the TIA is calculated as 10 μA. Hence, for $\Delta x_{max} = 10\ \mu m$ and $\Delta x_{min} = 1\ nm$, the minimum current to be detected by the TIA is 1 nA.

Employing capacitors as V2I has a number of advantages. Firstly, it improves the linearity and reduces power consumption of the demodulator. Passive resistors [24] can also be employed for this purpose however they degrade the quality factor of the LC resonator. Another issue with using resistors is that the common-mode voltage of the excitation-oscillator outputs is too low for the TIAs to function properly. Using capacitors as V2I also relaxes the mixer size due to the quadrature relationship between the switch resistance R_{sw} and capacitive reactance (Fig. 6). This helps in reducing the parasitic capacitance (C_p in Fig. 6) and improves noise performance of the demodulator. Capacitors also assist in increasing the excitation-frequency as they present higher transconductance-gain with frequency whereas more current and area has to be spent to improve the transconductance-gain of g_m cells and resistors, respectively.

2) Downconversion Mixer: Current-driven passive mixers are attractive due their low flicker noise, and hence they are often employed for demodulation to zero IF [19], [25], [26]. The proposed sensor-offset compensation scheme further reduces the mixer's noise contribution by removing the excess offset-current flowing through them [27]. Due to the high frequency operation of downconversion mixers, the charge injection of mixers Mix_1 and Mix_0 can cause significant residual offset. This is mitigated by a nested-chopping scheme operating at $f_{mix}/4096$ [28], [29].

However for mixers to work in current-mode, the mixer switch resistance R_{sw} and TIA input impedance ($R_{in,tia}$) should be much smaller than the capacitive impedance at f_{exc} ($R_{sw} + R_{in,tia} << \frac{1}{j \cdot 2\pi \cdot f_{exc} \cdot C_{in}}$). A small R_{sw} can be achieved by increasing the size of switching transistors. However this causes an increase in the parasitic capacitance C_p which deteriorates the noise performance of the demodulator. Assuming the noise of the amplifier A_v is the dominant source, the noise-figure NF of the demodulator can be evaluated as:

$$NF = \frac{C_{in} + C_P}{C_{in}} \tag{4}$$

In this work, mixers are sized to add total parasitic capacitance C_p of only 50 fF which degrades noise of TIA by only 10 %. Sensor-offset compensation capacitor C_{soc} does affect the noise of the sensor-channel TIA adversely, hence NF has a minimum value of 3 dB. As per simulations, the effective R_{sw} is 150 Ω (increased 3 times due to nested-chopping) and the capacitive reactance at 126 MHz is $\approx$ 2.5 $k\Omega$. The quadrature relationship between these two impedances further helps in defining currents predominantly by the capacitance.

3) Transimpedance amplifier: The TIA is one of the most important block in the proposed demodulation scheme. For capacitors to perform efficiently as V2I blocks, the TIA must present a low input impedance $R_{in,tia}$ within the bandwidth of the input. The impedance transformation property of current-driven mixers shifts this low impedance to the input of mixers around f_{exc} [19]. The amplifier A_v must possess high gain at low frequency to achieve this. Also, the negative feedback in the TIA should still be present at $2 * f_{exc}$ because the input to the TIA consists predominantly of a baseband signal around DC and $2 * f_{exc}$ (I_{mix1} in Fig. 4). To ensure the proper functioning of capacitors as V2I, A_v is designed for a $>$ 110 dB DC gain and a $>$ 1 GHz unity-gain-frequency f_u ($\approx$ $8 * f_{mix}$).

The schematic of the amplifier A_v is shown in Fig. 7. The amplifier consists of a two-stage Miller-compensated amplifier. The first stage is a telescopic amplifier and the second stage A_{v2} is a common-source (CS) stage. To achieve high DC gain without deteriorating high-frequency behavior of the amplifier, gain-boosting is employed in the telescopic amplifier [30]–[32]. Auxiliary (gain-boosting) amplifiers, for both PMOS and NMOS cascodes, are also realized as two-stage amplifiers to achieve sufficient gain. Auxiliary amplifiers consist of a folded-cascode amplifier followed by a CS amplifier, and they are Miller-compensated. Although the use of a differential signal path reduces charge-injection errors, unbalanced inputs to the TIA lead to common-mode signals at $2*f_{mix}$. These are suppressed by common-mode feedback (CMFB) circuitry and capacitor C_s. Two auxiliary amplifiers and the main amplifier have their own CMFB control.

The noise of the amplifier A_v is the dominant source in the demodulator. The input-referred noise $v_{n,in}$ required from the amplifier in the TIA can be evaluated as,

$$v_{n,in} \leq \Delta v_{sen,min} \cdot NF \tag{5}$$

where $\Delta v_{sen,min}$ is the minimum detectable change in the amplitude of V_{sen}. For $|V_{sen}| = 400\ mV$, $x_{so} = 100\ \mu m$ and $\Delta x_{min} = 1\ nm$, $\Delta v_{sen,min}$ is 4 μV. Hence $v_{n,in} < 2\ \mu V$ is required from the amplifier in the TIA,

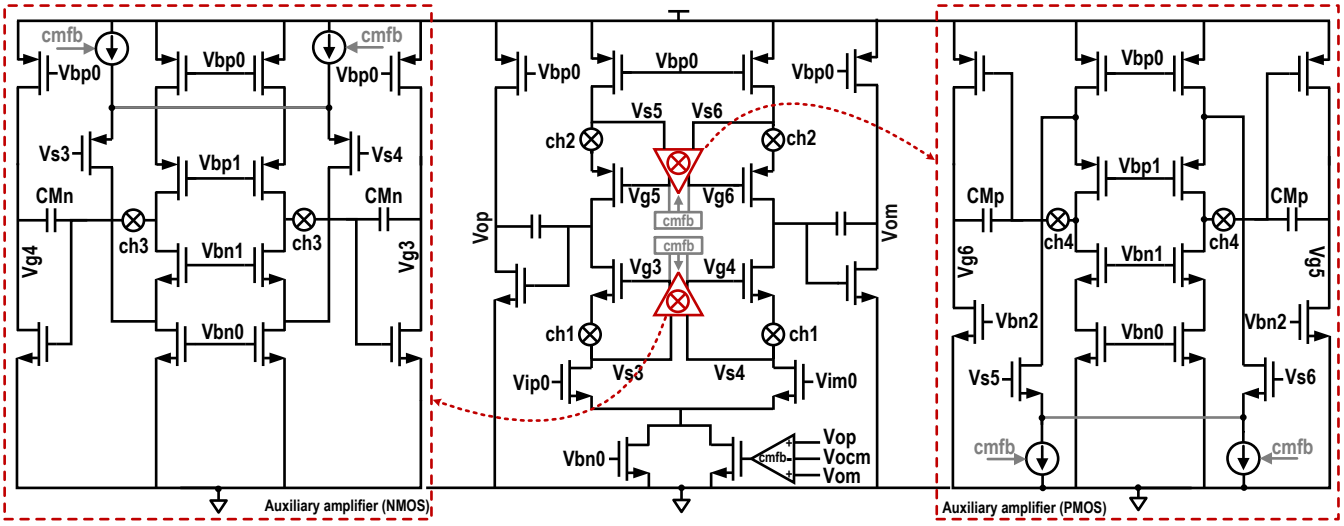

Fig. 7. Schematic of the amplifier A_v used to realize TIAs. Two-stage chopped auxiliary amplifiers are used for gain-boosting.

for NF = 3 dB. For a bandwidth of 2 kHz, the amplifier A_v should possess an effective input thermal noise floor smaller than 45 $nV/\sqrt{Hz}$.

Low-frequency errors of the amplifier are very important for the zero IF demodulation scheme. We have mitigated them using chopping technique in this work. As shown in Fig. 7, both the amplifier A_v and auxiliary amplifiers are chopped to mitigate their offset and low-frequency noise. Choppers are always placed at low impedance nodes to reduce their residual offsets, caused by self-mixing. PSS simulations show that the amplifier achieves a 113 dB DC gain over a 3-dB bandwidth $\approx$ 4 kHz. The amplifier is not unity-gain compensated.

C. Quadrature Clock Generation

This section illustrates the implementation of the quadrature clock comparator needed for the generation of the clock which has a $\pi/2$ radian phase lead compared to the excitation-oscillator outputs. The design of a comparator, that is fast enough, is very important because any excess phase difference over $\pi/2$ radians attenuates the effective input signal to the TIA and degrades the input SNR to the TIA. This attenuation is proportional to cos($\Delta\phi$) where $\Delta\phi$ is the phase difference between the ideal quadrature-clock phase and the phase of the comparator output. As an example, at f_{exc} = 200 MHz, a 500 ps excess delay translates to $\Delta\phi$ = 36 °C causing the signal to be attenuated by 20 %. For this reason, a fast continuous-time comparator has been designed.

Figure 8 shows the schematic of the continuous-time comparator designed for the interface. The comparator consists of 3 stages: (1) quadrature generation stage, (2) self-biased preamplifier, and (3) regenerative latch. The quadrature generation stage provides a low input impedance so that capacitors C_{comp} (= 200 fF) generate currents proportional to input voltages V_{sen} and V_{ref}. These currents, in quadrature to the excitation-oscillator voltages, are converted into voltages V_{op1} and V_{om1} at low impedance nodes, resulting in smaller delay at the

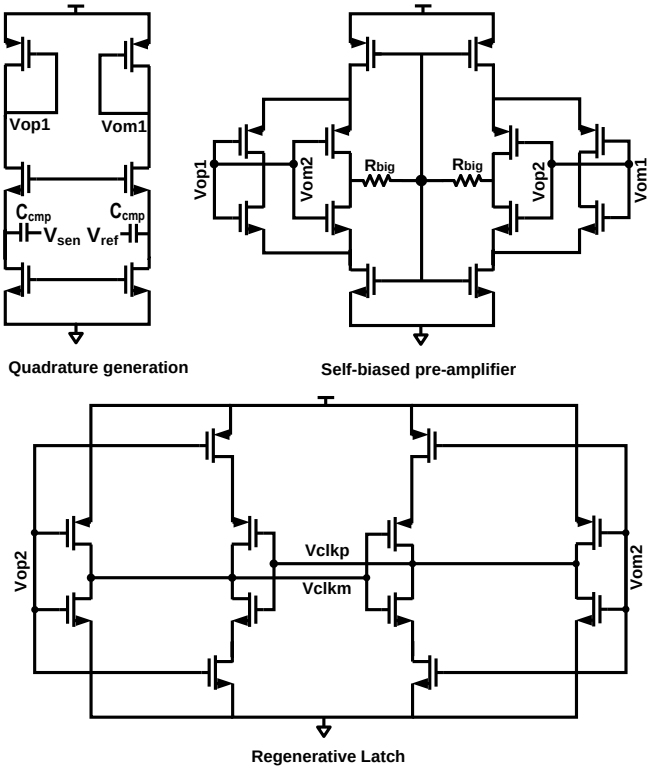

Fig. 8. Continuous-time comparator to generate clock in quadrature to excitation-oscillator's outputs.

expense of a low voltage gain. The self-biased preamplifier stage [33] amplifies the output of the 1^{st} stage and also sets the optimum amplifier-to-latch transfer point which desensitizes the effect of PVT variations on the comparator delay [34]. This is important for minimizing the delay due to the regeneration stage. At f_{exc} = 126 MHz, $\approx$ 0.4 ns delay of the comparator causes $\approx$ 5 % signal attenuation.

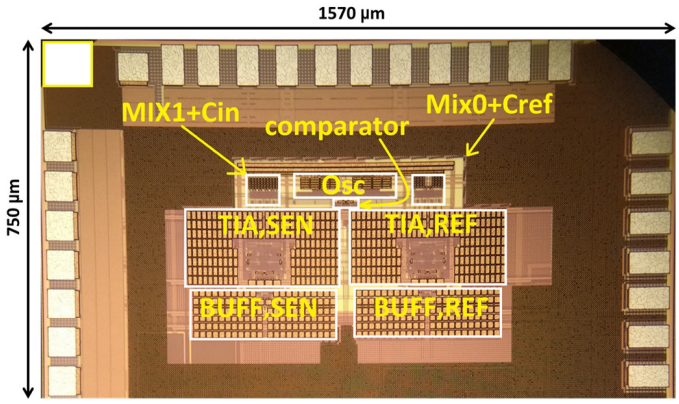

Fig. 9. Chip micrograph of the ECS interface.

IV. Experimental Results

To evaluate the usefulness of proposed concepts in precision displacement sensing, a microchip was fabricated. As shown in Fig. 9, the ECS interface occupies only 1.18 mm^2 in TSMC 0.18 μm *CMOS* technology. The interface consumes 11 mA from a 1.8 V supply, which includes 2.2 mA consumed by two on-chip unity-gain output buffers used to drive an off-chip ADC. The analog output of the chip is digitized using an evaluation board of the 24-bit ΣΔADC AD7779.

A. PCB-based ECS

A PCB-based sensor was used to evaluate the performance of the microchip and its usefulness in sensing displacement. Figure 10(a) depicts the structure of the PCB-based sensor. It consists of two flat coils, of identical geometry, implemented in the top and bottom layer of a custom four-layer PCB. Each coil consists of four, 35 μm thick, turns with a 200 μm pitch and an 8 mm outer diameter. The coils are shielded from each other by two ground planes to prevent mutual inductance. Their distance to the moving sensor target and fixed reference target is established by a number of precision 10 μm stainless-steel spacers. Spacers are positioned 3 mm away from the coils so as not to affect the sensitivity of coils.

Figure 10(b) illustrates the custom PCB designed for the characterization of the ECS interface. Nylon nuts and bolts are used to position sensor and reference targets with the help of stainless steel spacers with high stiffness. With a copper target and nominal standoff x_{so} = 105 μm (14 spacers minus coil thickness of 35 μm), the effective standoff inductance L_{so} is found to be ≈ 100 nH (including $L_{ic} \approx$ 20 nH) using an impedance analyzer. The coil used for the characterization of the ECS interface is similar to coil 3, annotated in Figure 10(b) (but underneath the copper target in the figure).

B. Transfer characteristic

Figure 11 shows the measured transfer characteristic obtained using the ECS interface and the PCB-based sensor, where $D_{out} = V_{o,sen}/V_{o,ref} = \Delta x/\Delta x_{max} \approx \Delta L(x)/(\beta * L_{ref})$ (Eqn. 1). To introduce a displacement Δx, the number of spacers between the sensor target and the sensor coil is varied. This introduces an effective displacement of 10 μm

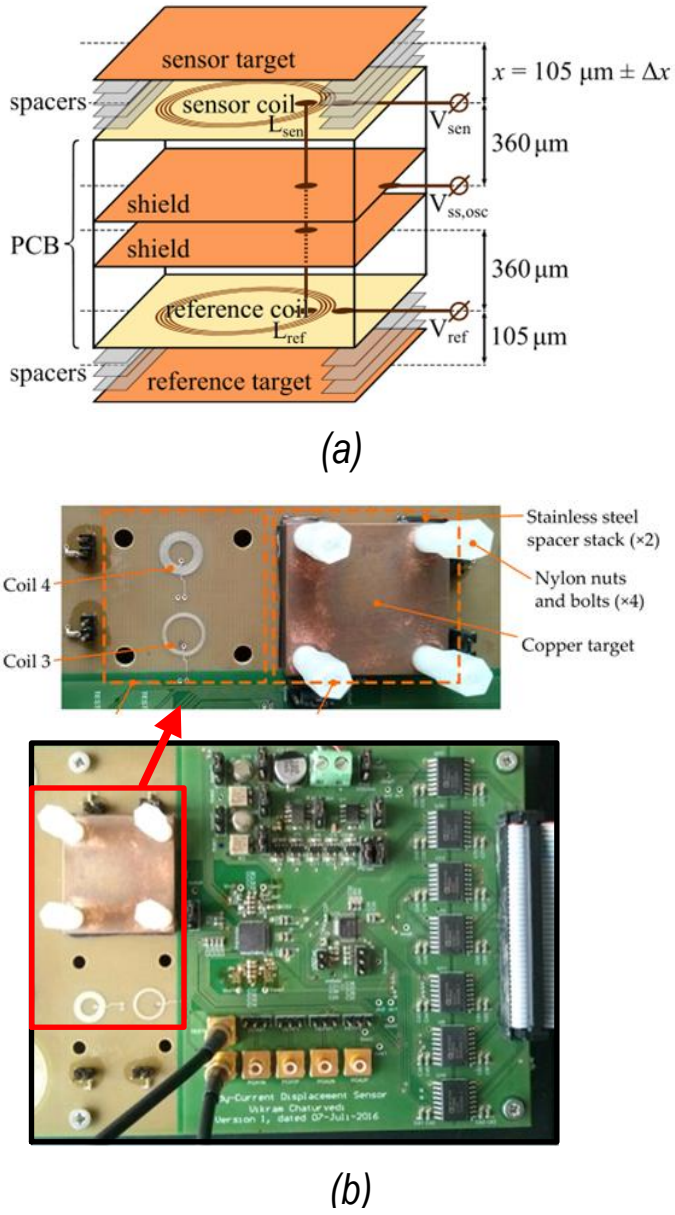

Fig. 10. PCB-based ECS. (a) conceptual sensor structure. (b) customized PCB with copper target.

with each spacer, around nominal standoff x_{so} = 105 μm (Fig. 5 and Fig. 10). The distance between the reference coil and reference target is kept fixed at 105 μm.

The transfer characteristics is evaluated at three different values of $I_{ss,osc}$, 1.2 mA, 1.52 mA and 1.84 mA, to evaluate the effectiveness of the ratiometric principle in suppressing the effect of the oscillator bias current ($I_{ss,osc}$). Output $V_{o,sen}$ has a higher slope at higher $I_{ss,osc}$ due to higher gain. Three $V_{o,sen}$ curves meet at a single point where $L_{sen} = L_{ref}$. The variation in $V_{o,ref}$ is dominated by the improvement in the quality factor of the sensor-coil, in spite of a decrease in f_{exc}, with higher x_{so}. The ratiometric readout D_{out} (Eqn. 1) is well matched for three values of $I_{ss,osc}$.

The presence of the null in D_{out} around the nominal x_{so} = 105 μm shows that the sensor-offset is indeed compensated by the ECS interface. The deviation of zero-crossing

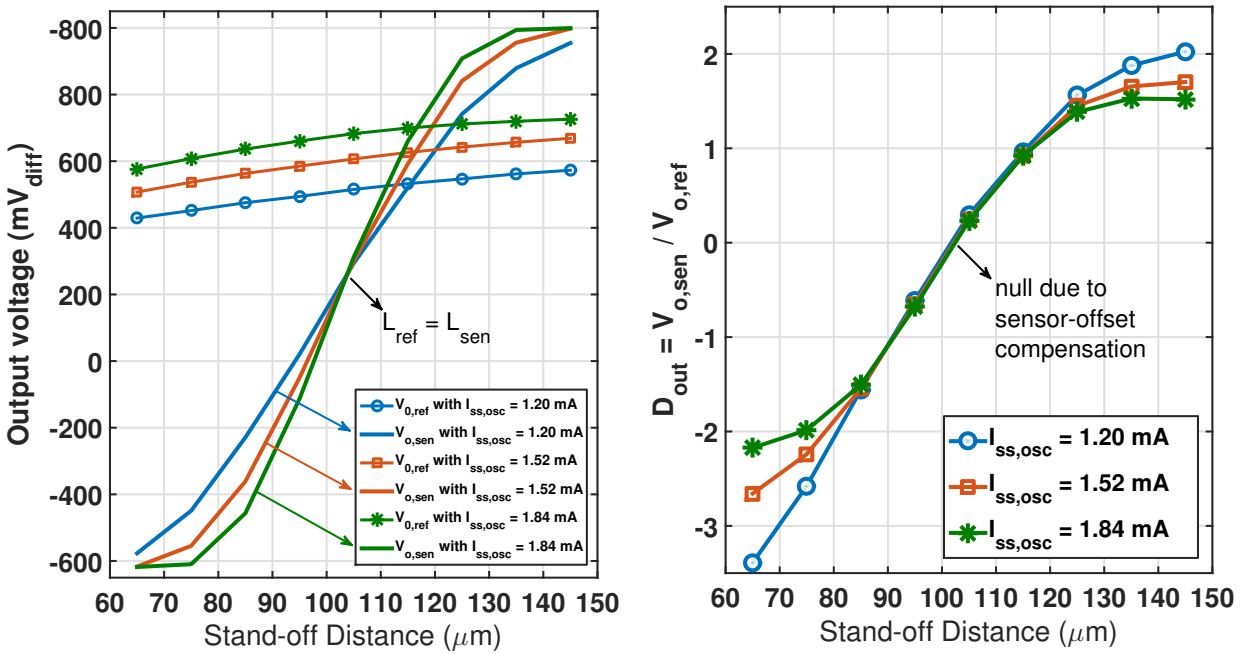

Fig. 11. Measured transfer characteristics at different values of $I_{ss,osc}$. The effective displacement is standoff distance minus nominal standoff (= 105 μm)

from x_{so} = 105 μm is due to a small mismatch ($\approx$ 3 nH) between L_{sen} and L_{ref}, caused primarily by the difference in parasitic inductances. The maximum displacement range Δx_{max} was found to be 10 μm which matches closely to $\beta * x_{so}$, with β = 0.1 and x_{so} = 105 μm. The limited output voltage range of the TIA manifests itself as the saturation of D_{out} at larger displacements. The ratiometric readout D_{out} for higher ($I_{ss,osc}$) saturates at smaller standoffs due to larger signal swing from the excitation-oscillator.

Due to pseudo-differential structure of the sensor, the excitation frequency f_{exc} also undergoes change with the displacement. An excitation frequency deviation of Δf_{exc} = 1.3 MHz, around f_{exc} = 126 MHz, for a displacement change of Δx_{max} = 10 μm was noticed. This confirms that the frequency output in the ECS is indeed less sensitive when compared to the output amplitude ($\Delta f_{exc}/f_{exc} \approx$ 1 %).

C. Noise characterization

To evaluate the noise performance of the ECS interface, fast Fourier transform (FFT) was used. Measured 2^{17} point FFTs of two output voltages and D_{out} are shown in Fig. 12, with Δx_{max} = 10 μm (standoff distance = 115 μm). The noise spectrum in two output voltages was found to be dominated by the oscillator amplitude-noise. The suppression of the low-frequency amplitude-noise of the excitation oscillator, due to ratiometric readout D_{out}, is clearly noticeable. The spectral shaping is primarily due to the decimation filter of the off-chip $\Sigma\Delta$ ADC. Low-frequency noise was found be dominated by residual flicker noise from the tail-current source of the excitation-oscillator. In a 2 kHz noise-bandwidth, the calculated SNR was found to be 86.6 dB, which corresponds to a resolution of 14.1 bits over Δx_{max} (= 10 μm). This corresponds to a displacement resolution of 0.6 nm and

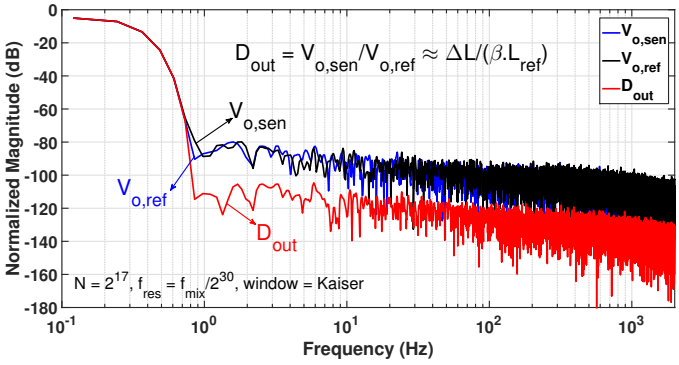

Fig. 12. Measured spectrum of the output voltages and D_{out}.

effective noise floor of 13.4 $pm/\sqrt{Hz}$. For coil inductance = 100 nH, this corresponds to an inductance resolution of 0.58 pH. The signal bandwidth could not be directly measured because of practical difficulty of introducing μm range single-tone vibration into the sensor target. However, the signal bandwidth in the ECS interface is limited by the bandwidth of the amplifier A_v used in the TIA. Parasitic extracted PSS simulations reveal that the amplifier A_v has 3-dB bandwidth of $\approx$ 4 kHz.

Another experiment was also performed to evaluate the suppression efficacy of the ratiometric measurement. A 2 kHz frequency component was introduced in the oscillator bias current by switching on and off 80 μA in parallel to a fixed current of 1.12 mA. The output spectrum of output voltages and D_{out} is shown in Fig. 13. It can be noted that the signal tone at 2 kHz is suppressed by 34 dB by the ratiometric measurement. This shows that ratiometric measurement suppresses variation in $I_{ss,osc}$, which is instrumental in improving the noise and drift performance of the ECS interface. A 34 dB suppression also endorses the high linearity of the

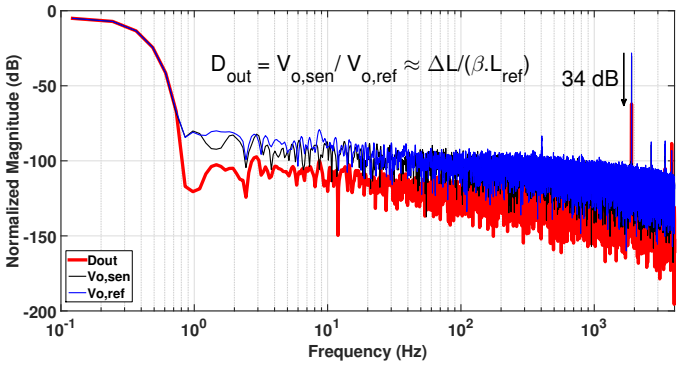

Fig. 13. Suppression of a 2 kHz tone in oscillator bias-current by ratiometric measurement.

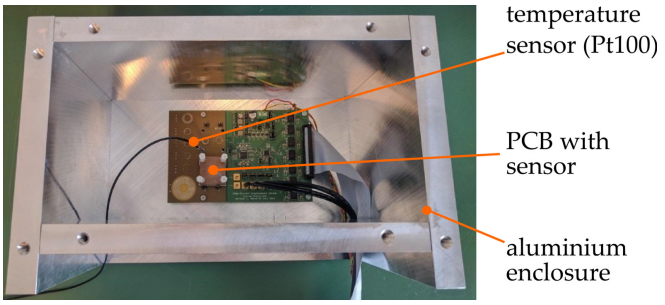

Fig. 14. Test setup for stability characterization of the ECS interface.

demodulators, when compared to [4] which achieved ≈ 24 dB of ratiometric suppression. A higher noise floor is also noticed in the spectrum which we feel is due to the inter-modulation effect of the switched-current source.

Using an LNA (SR560) and a low-noise spectrum analyzer (HP4395A), the output noise floor of the reference channel is found to be 136 nV/Hz. This would translate into a 92.9 dB SNR, if all of oscillators amplitude-noise was suppressed by the ratiometric readout. In practice, it is slightly less because of the finite input impedance of the demodulator which allows some of oscillator's amplitude-noise to escape from the LC tank. This illustrates an important trade-off when using capacitors as V2I instead of a g_m block.

D. Stability characterization

Stability tests were performed on the ECS interface using the climate chamber ACS DY110C. The temperature and humidity were controlled using the software LabVIEW®. As shown in Fig. 14, the PCB-based ECS and the readout interface were placed inside a thick Aluminium box to ensure a highly stable environment. During the experiment, a high precision temperature sensor Pt100 was used to find the exact temperature of the PCB-based ECS inside the Aluminium box (Fig. 10). The Aluminium box, with the ECS and interface inside, was placed in the climate chamber, and precautions were taken to isolate mechanical vibrations of the climate chamber from coupling to the sensor.

For thermal stability characterization, humidity was kept fixed at 40 % and temperature was stepped from 20 $^{\circ}C$ to 40 $^{\circ}C$, in steps of 5 $^{\circ}C$, and then back to understand the hysteresis effects. Figure 15 shows the drift in D_{out}

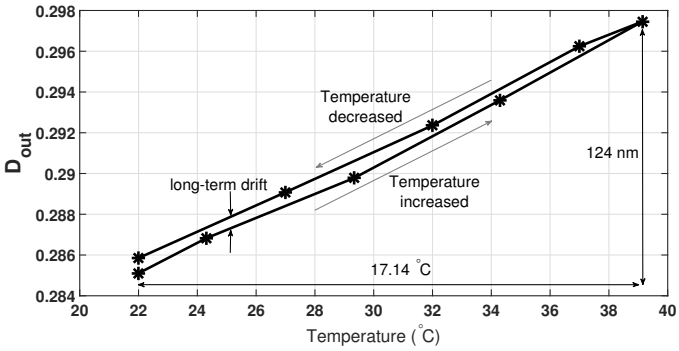

Fig. 15. Thermal stability characterization of the ECS interface.

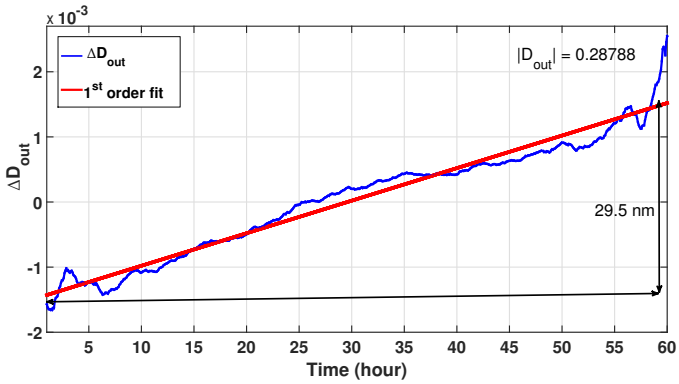

Fig. 16. Long-term stability characterization of the ECS interface.

caused by the change in temperature. A temperature change of 17.14 $^{\circ}C$ caused an effective displacement error of 124 nm ($\Delta x = \Delta D_{out} * \Delta x_{max}$), which corresponds to a thermal drift of 7.24 nm/$^{\circ}C$. This amount of thermal drift is very low because various applications requiring such a high displacement resolution have very well-controlled environments ($\Delta T < 10 - 20\ mK$). The difference in plots for the two directions of the temperature change is attributed to the long-term drift (the experiment took ≈ 22 hours to complete).

For long-term stability, temperature and humidity of the climate chamber were kept fixed at 25 $^{\circ}C$ and 40 % respectively. The experiment was carried out for 60 hours, during which data was captured once every 5 minutes for a duration of 1 second. Figure 16 shows the effect of long-term drift on D_{out}. After the 1^{st} order fit, the effective drift was calculated as ≈ 29.5 nm over 60 hours. The deviation from the linear behavior is attributed to mechanical vibrations of the climate chamber which were not attenuated enough by the vibration isolator. High precision applications such as wafer scanners are frequently calibrated between each run (< 2 minutes). Hence a long-term drift of 29.5 nm over 60 hours is quite benevolent.

E. Performance comparison

Table I summarizes the performance of the ECS interface and compares it to the state-of-the-art from both academia and industry. The presented ECS interface achieves 0.6 nm in a 2 kHz noise-bandwidth. This is at least 30 x better than [9]. Despite a higher f_{exc}, better resolution and implementation in a sub-micron CMOS process, the interface dissipates similar power [4], [7]. Thermal drift is found to at least one order

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

	This work	[4]	[8]#	[7]	[9]#	[35]
Standoff Distance	105 μm	3 mm	1 mm	3 mm	2.286 mm	3 mm
Excitation Frequency (MHz)	126	20	-	15	-	0.3125
Resolution (nm)	0.6	65	60	135	21	2930
Noise Bandwidth (kHz)	2	1	0.52	1	1	10
Inductance Resolution (pH)	0.58	1.5	-	3.8	-	-
Thermal Stability (nm/$^\circ C$)	8	90	few 1000s	-	few 1000s	-
Power Consumption (mW)$^\$$	19.8	18	$\approx$ 750	18*	$\approx$ 700*	7.3
Technology	0.18 μm CMOS	0.35 μm BICMOS	-	0.35 μm BICMOS	-	0.6 μm CMOS
FoM_{ECS} (aJ/Hz)	4.73	19.4	-	55.5	-	220

* digital output from the ECS interface.
$ power consumption of an output ADC ($<<$ 1 mW) is negligible compared to that of ECS interfaces.
# high precision ECS products available in the market.

better than the previous state-of-the-art [4]. Furthermore, it achieves an inductance resolution of 0.58 pH which outperforms that of precision LCR meters.

To compare the power-efficiency of ECS interfaces, a figure-of-merit (FoM_{ECS}) was introduced in [4],

$$FoM_{ECS} = \frac{P}{BW \cdot 2^{ENOB}} \cdot \frac{1}{f_{exc}} \tag{6}$$

where P is the power consumption, BW is the measurement bandwidth, $ENOB$ is effective-resolution of the interface (in bits) and f_{exc} is the excitation frequency of the ECS interface. The presented ECS interface is at least four times better than the state-of-the-art, when it comes to power-efficiency.

V. CONCLUSION

An ECS interface for sub-nanometer displacement sensing is presented. The degradation of the stability due to the skin-effect is mitigated using a high excitation frequency ($>$ 100 MHz). A small standoff distance, along with integrated read-out circuitry in close proximity to the ECS coils, is employed to improve the sensitivity of the system. Ratiometric measurement is found to be instrumental in suppressing the noise and drift of the excitation-oscillator. To assist this ratiometric suppression, a highly linear amplitude demodulation scheme is realized using a passive (capacitive) voltage-to-current conversion approach. Sensor-offset-compensation is found to be helpful in obviating the detrimental effect of sensor-offset on the linearity of the interface, particularly demodulator blocks.

At a nominal standoff of 105 μm, the ECS interface achieved a displacement resolution of 0.6 nm (in 2 kHz noise-bandwidth) within a 10 μm displacement range. The thermal drift was found to be $<$ 7.3 nm/$^\circ C$, in the range of 20 $^\circ C$ to 40 $^\circ C$. A 60-hour long-term stability experiment showed a drift of only 29.5 nm. What is more, all of this is achieved by consuming only 11 mA from a 1.8 V supply. By increasing f_{exc}, reducing the standoff distance and compensating sensor-offset, this is the only ECS interface to achieve sub-nanometer displacement resolution.

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