

Document Version

Final published version

Licence

Dutch Copyright Act (Article 25fa)

Citation (APA)

Pashaeifar, M., de Vreede, L. C. N., & Alavi, M. S. (2025). A Millimeter-Wave Power Amplifier With an Integrated CMOS Isolator/Circulator/Receiver. *IEEE Journal of Solid-State Circuits*, 61(2), 525-537.
<https://doi.org/10.1109/JSSC.2025.3570656>

Important note

To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright

In case the licence states "Dutch Copyright Act (Article 25fa)", this publication was made available Green Open Access via the TU Delft Institutional Repository pursuant to Dutch Copyright Act (Article 25fa, the Taverne amendment). This provision does not affect copyright ownership.
Unless copyright is transferred by contract or statute, it remains with the copyright holder.

Sharing and reuse

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

A Millimeter-Wave Power Amplifier With an Integrated CMOS Isolator/Circulator/Receiver

Masoud Pashaeifar^{1b}, Member, IEEE, Leo C. N. de Vreede^{1b}, Senior Member, IEEE,
and Morteza S. Alavi^{1b}, Senior Member, IEEE

Abstract—This article presents a reconfigurable millimeter-wave (mm-wave) fully integrated transceiver (TRX) front end that comprises a power amplifier (PA) and an integrated nonreciprocal ultra-compact isolator/circulator/receiver (RX). The circulator is based on a ring quarter-wave transmission line (QTL) topology with adjusted characteristic impedances, which improves transmitter (TX)-to-antenna insertion loss and TX-to-RX isolation. The circulator’s nonreciprocal gyrator features an AND-gate switching-based N -path filter while also acting as a mixer-first RX. By activating the embedded cross-coupled negative resistors, the circulator can be reconfigured as an isolator. This compact N -path filter-based circulator/isolator occupies only 0.38 mm². Over a 27.1–31.1-GHz band, the realized front end offers >20-dB TX-to-RX isolation, with a measured TX-to-antenna insertion loss of 1.7~2.2 dB. The RX path tolerates the PA’s blocker signal, achieving 5-dBm in-band and 13-dBm out-of-band (OOB) B_{1dB} . The PA delivers 15.15-dBm peak output power with 33% drain efficiency. The functionality of the proposed frequency division duplex (FDD) front end is evaluated by simultaneous TX/RX operation with a 400-MHz TX/RX modulation bandwidth and 400-MHz channel spacing. The measured AM–PM of the realized PA with the integrated isolator shows relatively high voltage standing wave ratio (VSWR) resilience at the lower power level and less robustness against VSWR around its peak output power. The front-end prototype occupies only 0.7 mm², including circulator, PA, quadrature hybrid coupler LO generators, and baseband circuits.

Index Terms—Blocker-tolerant receiver (RX), circulator, CMOS, duplex, fifth-generation (5G), frequency division duplex (FDD), full-duplex, gyrator, in-band full-duplex, isolator, millimeter-wave (mm-wave), mutual coupling, N -path filter, power amplifiers (PAs), voltage standing wave ratio (VSWR) resilience.

I. INTRODUCTION

MILLIMETER-wave (mm-wave) bands accommodate various high-throughput communication and high-resolution sensing systems, such as 60-GHz Wi-Fi (IEEE 802.11ad and IEEE 802.11ay standards) [1], [2], [3] and automotive radar [4], [5], [6]. Owing to silicon technology

scaling, mm-wave phased-array systems enable the development of satellite communication and fifth-generation (5G) cellular wireless networks to address the demand for high data throughput and low latency. In addition to allocating wide channel bandwidth at mm-wave frequencies, dual orthogonal polarization further increases channel capacity and enhances spectral efficiency. Nevertheless, their shorter wavelength leads to lower penetrability and higher free-space path loss, thus limiting coverage [7].

Beamforming architectures address the required link budget (LB) while reducing interference and increasing link security [8]. However, the directional and line-of-sight connections make the link even more susceptible to small obstacles, degrading the distance and mobility support. Moreover, mm-wave dual-polarized phased-array systems pose stringent requirements on the transceiver’s (TRX) performance specifications, power consumption, and, most importantly, the occupied silicon area.

The ongoing 5G new radio (NR) frequency range two (FR2) standard has utilized mm-wave bands (e.g., 24.25–29.5 GHz, 37–43.5 GHz, and 47.2–48 GHz), while the time division duplex (TDD) ensures channel reciprocity. Although industry and research groups have vastly developed the 5G NR system and shown promising performance in supporting multi-Gbit/s data rate [9], [10], [11], [12], its coverage range must be improved. However, TDD introduces additional delay due to duplex switching, which becomes more pronounced when using repeaters and relays for coverage extension. In addition to TDD, full-duplex systems such as frequency division duplex (FDD) and in-band full-duplex recently gained momentum, envisioning more innovative and revolutionary link protocol design [13], [14], [15]. Considering the stringent area restriction of the phased array structures, implementing the front end with appropriate duplexing and bandpass filtering to support the FDD and in-band full-duplex systems at mm-wave frequencies is very challenging.

Employing separate antennas for the transmitter (TX) and the receiver (RX) provides sufficient isolation in full-duplex systems at the cost of a larger form factor [16]. Electrical balance duplexer (EBD) and its counterparts, such as the hybrid coupler and the Wilkinson combiner, offer a high TX-to-RX isolation for a single-antenna system and occupy a reasonably low area [17], [18], [19], [20]. However, they still suffer from 3-dB loss at the TX and RX paths. Magnetic-free CMOS circulators have recently been presented at RF

Received 10 June 2024; revised 16 February 2025 and 28 April 2025; accepted 6 May 2025. Date of publication 2 June 2025; date of current version 30 January 2026. This article was approved by Associate Editor Bodhisatwa Sadhu. This work was supported by NWO/NXP 5G Partnership Project 15593. (Corresponding author: Masoud Pashaeifar.)

The authors are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: m.pashaeifar@ieee.org).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/JSSC.2025.3570656>.

Digital Object Identifier 10.1109/JSSC.2025.3570656

0018-9200 © 2025 IEEE. All rights reserved, including rights for text and data mining, and training of artificial intelligence and similar technologies. Personal use is permitted, but republication/redistribution requires IEEE permission.

See <https://www.ieee.org/publications/rights/index.html> for more information.

Authorized licensed use limited to: TU Delft Library. Downloaded on February 16, 2026 at 08:28:21 UTC from IEEE Xplore. Restrictions apply.

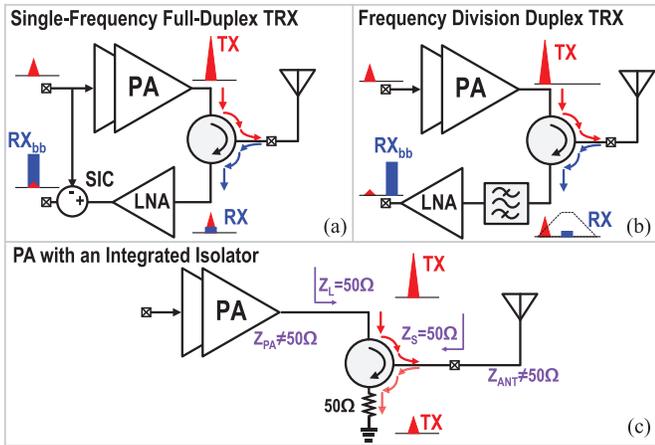


Fig. 1. Simplified form of the possible applications employing the mm-wave integrated circulator/isolator. (a) In-band full-duplex TRX front end. (b) FDD TRX front end. (c) PA with an integrated isolator.

and mm-wave bands for in-band full-duplex links [21], [22], [23], [24], [25], [26]. As illustrated in Fig. 1(a), apart from the circulator's isolation, which is crucial to prevent the RX from saturation, further self-interference cancellation (SIC) is required. Nonetheless, achieving high SIC in a practical phased array system considering process, voltage, and temperature (PVT) variations and mutual coupling issues of the closely spaced antenna arrays is a daunting task. Moreover, state-of-the-art mm-wave CMOS circulators are still relatively large for phased-array systems and introduce a high loss comparable to EBDs and hybrid couplers.

Fig. 1(b) depicts an FDD TRX front end utilizing a circulator as the duplexer. In contrast to in-band full-duplex, the TX signal acts as an out-of-band (OOB) blocker and, hence, demands a sharp bandpass filter (BPF). Because implementing integrated compact BPF is not easily feasible at mm-wave, standalone mixer-first RX architectures and active BPFs have gained significant research attention [27], [28], [29], [30]. Recent advancements in LiNbO₃ filters [31], [32] have demonstrated reasonably acceptable performance within a compact form factor, showing promise for future integration in mm-wave systems. Moreover, in [13], an E-band Backhaul-on-glass FDD module comprising TRX, power amplifiers (PAs), and diplexer is introduced. However, due to its significant form factor, the FDD module is not scalable in a phased array system to enhance the link budget (LB).

In addition to the full-duplex TRX operation, the integrated circulator can be reconfigured to an isolator. As depicted in Fig. 1(c), despite the impedance of the PA and the antenna, the isolator simultaneously provides matched sourcing impedance for the antenna and optimum loading conditions for the PA. This is opposed to the balanced amplifiers [33], [34] and the reconfigurable matching networks [35], [36], [37], which only provide matched loading conditions to the antenna or the PA.

This article demonstrates the feasibility and implementation of two separate solutions for mm-wave phased array systems. First, we elaborate on our recently published compact single-antenna mm-wave full-duplex front end [38] capable of operating as an FDD front end, supporting simultaneous

transmit and receive (STAR) FDD communication with up to 400-MHz modulation bandwidth. Second, we reconfigure the chip to a voltage standing wave ratio (VSWR)-resilient PA with an integrated isolator. The proposed reconfigurable architecture features: 1) an mm-wave N -path filter as a non-reciprocal gyrator that simultaneously functions as a blocker tolerant RX; 2) a compact differential ring quadrature transmission lines topology with adjusted characteristic impedances to improve the TX-to-antenna insertion loss (IL_{TX}), RX gain (G_{RX}), and TX-to-RX isolation; 3) an integrated push-pull PA directly connected to the proposed circulator/isolator; and 4) embedded negative resistors to reconfigure the front end to an integrated isolator.

This article is organized as follows. Section II presents the system requirements and analysis. The proposed circulator/isolator architecture is given in Section III, where we proposed a pass-transistor-based AND-gate switching to realize an N -path filter at mm-wave frequencies. Section IV elaborates on the circuit implementation details of the 40-nm bulk CMOS technology prototype. Section V presents the experimental results of the FDD front end, and Section VI reports the measurement results of the integrated isolator. Finally, this article is concluded in Section VII.

II. MM-WAVE FULL-DUPLEX FRONT-END SYSTEM LEVEL DESIGN AND TRADE-OFFS

This section discusses system design specifications and trade-offs for an mm-wave phased-array full-duplex link.

A. LB Calculations

In a conventional single-input single-output (SISO) link, the LB can be calculated as

$$LB_{SISO} + LM = P_{TX} + 2 \times G_A - P_{S-RX} \quad (1)$$

where P_{TX} and P_{S-RX} are TX signal power and RX sensitivity of a TRX element, respectively. G_A is the antenna gain and LM is the link margin. As mentioned, modern communication systems aim to support multi-Gb/s data throughput by allocating wider bandwidth, which means a higher RX noise floor. They also employ high-order complex modulation schemes, requiring a higher signal-to-noise ratio (SNR). As a result, the RX sensitivity ($P_{S-RX} = -174 \text{ dBm} + 10 \log BW + NF_{dB} + SNR_{dB}$) increases, thus, the LB decreases. As such, mm-wave bands are inevitable in accommodating signals with large modulation bandwidths. This attribute raises two more issues: 1) higher free-space path loss and 2) lower TX output power due to technology limitations at such frequency bands. In summary, modern communications systems demand a higher LB to address higher free-space path loss, while their LBs suffer from high RX sensitivity and limited TX output power. To address these challenges, as exhibited in Fig. 2, an N -element phased array link offers $30 \log N$ LB improvement.

As an example of a short-range link, for example, $d = 100\text{-m}$ line-of-sight, we assume two 64-element TRXs employing a 400-MHz 64-QAM OFDM scheme (requiring SNR = 25 dB) at the 28-GHz carrier frequency. Considering 4-dB antenna gain (G_A) and 10-dB LM, $P_{TX} - NF > -13.79 \text{ dBm}$ is required to address path loss of a 100-m long link.

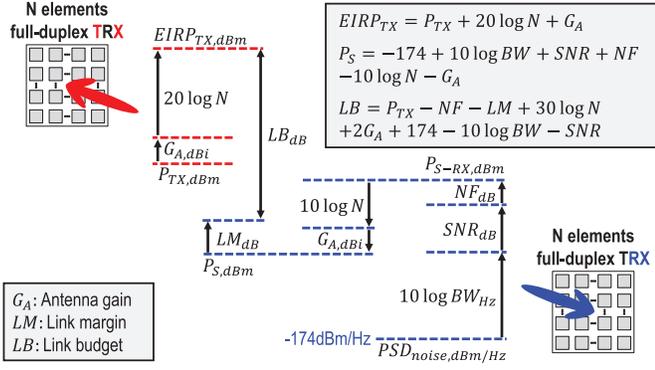


Fig. 2. LB calculation of a full-duplex link employing two N -elements phased-array TRXs.

B. Isolation and Linearity Requirements

As depicted in Fig. 1(a) and (b), the TX signal interferes with the RX as they operate simultaneously in a single antenna full-duplex radio. Mitigating RX sensitivity degradation caused by TX signal enforces stringent specifications for duplexer (e.g., a circulator) isolation and RX linearity. Moreover, an in-band full-duplex system employs SIC along with the circulator's TX-to-RX isolation (ISO) to ensure that the TX signal and its distortions are well below the RX noise floor. Therefore, as discussed in [21], ISO + SIC must be less than $P_{TX} - NF + 174 \text{ dBm} - 10 \log BW$. However, in a phased array system with the same RX and TX beam direction, since the TX interferers are combined coherently alongside the RX signals, the required ISO + SIC can be calculated as

$$\text{ISO} + \text{SIC} > P_{TX} - NF + 174 \text{ dBm} - 10 \log BW_{RX} + 10 \log N \quad (2)$$

where BW_{RX} is the RX signal modulation bandwidth and P_{TX} is the average TX output power per element. Here, we assume equal TX and RX bandwidths. However, the TX and RX bandwidths can be configured independently, allowing asymmetric data links where uplink and downlink rates differ. In this regard, if $BW_{TX} > BW_{RX}$, the required ISO + SIC is relaxed. In this case, (2) should be modified by $-10 \log(BW_{TX}/BW_{RX})$ to account for the lower interfering TX power density within BW_{RX} . Conversely, if $BW_{TX} < BW_{RX}$, the required ISO + SIC may be more stringent depending on the modulation scheme and carrier-aggregation structure, and a detailed per-carrier component (CC) analysis is necessary.

Now, assuming ISO = 20 dB and 400 MHz RX/TX modulation bandwidth, SIC > 72.21 dB is required for the design, as previously mentioned. Nevertheless, extending in-band full-duplex phased array systems requires a higher SIC, which is practically difficult considering PVT variations and mutual coupling.

Moreover, the dual-polarization feature introduces another interferer due to the antenna's limited horizontal-vertical (H-V) isolation (e.g., 20 dB). Therefore, canceling perpendicular polarization's TX signal leakage is inevitable, making the system even more complex. Therefore, even though in-band full-duplex link architecture offers the highest

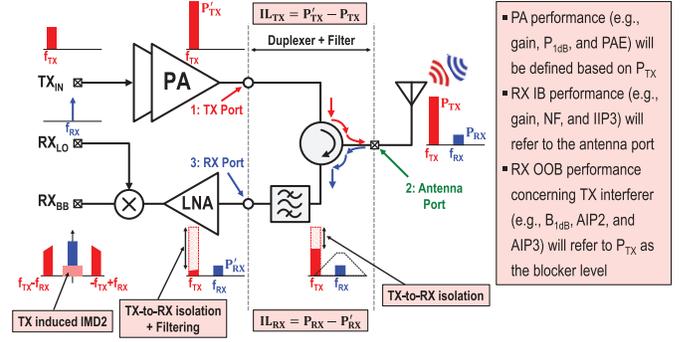


Fig. 3. TX-induced second-order distortion mechanism in the fully integrated FDD TRX.

spectrum efficiency, it is not readily extendable to dual-polarization massive-MIMO systems.

Similarly, a conventional single-antenna FDD system demands high duplexer isolation. For instance, third-generation (3G) wireless systems require >50-dB duplexer isolation, where the duplexer handles 15-V signal swing to support $P_{TX} = 24 \text{ dBm}$ [18]. Such a duplexer adds high loss ($\sim 2 - 3 \text{ dB}$) at both RX and TX paths [39], degrading TX efficiency and RX sensitivity. In contrast, in modern phased array systems, a portion of the required LB is provided by the overall beamforming gain ($30 \log N$), which results in a lower P_{TX} per element while the RX sensitivity of each element is higher. This relaxes the requirements on the duplexer isolation and linearity for each TRX element, enabling fully integrated mm-wave wideband full-duplex links.

As depicted in Fig. 1(b), in the RX path of an FDD system, the channel selects filters to suppress the TX signal as well as any other interferers, for example, mutual coupling and orthogonal-polarization signals, to prevent RX amplifiers from saturation. Therefore, unlike in-band full-duplex systems, a dual-polarization phased array FDD system does not entail another interferer cancellation loop but compels more stringent OOB interferer rejection.

Even though the TX signal occupies another frequency band, its noise and distortion levels must stay well below the RX noise floor. This imposes a stringent requirement on RX linearity and its OOB interferer tolerance specifications, such as input 1-dB compression point (IP_{1dB}), input third-order intercept point (IIP_3), and, for a direct conversion RX architecture, input second order intercept point (IIP_2).

A conventional FDD system considers TX, RX, and duplexer as separate components with their own specifications. On the contrary, this work aims to study the design of a fully integrated front end, including the duplexer. Therefore, we redefine the TRX specifications based on the antenna port's signal levels, as shown in Fig. 3. We defined antenna-port referred IIP_3 (AIP_3) and antenna-port referred IIP_2 (AIP_2) to address TX-induced distortions. Thus, the AIP_2 specification can be calculated as

$$\text{AIP}_2 > 2P_{TX} - NF + 174 \text{ dBm} - 10 \log BW_{RX} + 10 \log N - 6 \text{ dB} \quad (3)$$

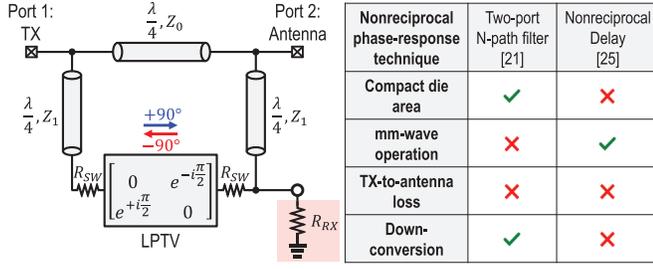


Fig. 4. Magnetic-free CMOS circulators [21], [25].

As with the ISO + SIC calculation, we assume equal TX and RX bandwidths; therefore, a detailed analysis is required when the TX and RX bandwidths are configured independently. Note that, in practice, specifying the required distortion and noise levels needs complex system-level calculations. Nevertheless, these simplified equations help determine the trade-offs and right design choices.

Recalling the design example introduced in Section II-A, and considering that $P_{TX} - NF = -13.8$ dBm while both the TX and RX bandwidths are 400 MHz, the AIP₂ can be calculated as

$$AIP_2 > 54.4 \text{ dBm} - NF + 10 \log N. \quad (4)$$

Note that the TX impairments are assumed to combine coherently, which is a somewhat pessimistic assumption.

III. PROPOSED MM-WAVE CIRCULATOR/ISOLATOR ARCHITECTURE

As depicted in Fig. 4, the magnetic-free CMOS circulators comprise a circle of three quarter-wave transmission lines (QTLs) and a nonreciprocal linear periodic time-variant (LPTV) circuit. LPTV provides a $+90^\circ$ phase shift in one direction and a -90° phase shift in the opposite direction, leading to wave propagation only in one direction. The LPTV component can be implemented either by a two-port N -path filter or a nonreciprocal delay. N -path filters occupy a small die area and contain an embedded down-conversion path [22]. However, they are impractical at the mm-wave frequencies as generating and amplifying the nonoverlapping clocks of the N -path filter is challenging. Therefore, a nonreciprocal delay technique has been exploited to extend the operational frequency of the CMOS circulators to mm-wave at the cost of occupying a relatively large area [25]. Nevertheless, both LPTV solutions introduce a high IL_{TX} , basically caused by the switches' impedance (R_{SW}), and heavily depend on the employed technology node.

To mitigate this undesired loss, we proposed a non-continuous QTL characteristic impedance to have a degree of freedom for optimizing IL_{TX} . As depicted in Fig. 4, the QTL impedance of the direct path is Z_0 , which defines the impedance of the circulator, while the impedance of the two other QTLs (Z_1) is chosen to be greater than Z_0 . As discussed in [21], the IL_{TX} is mainly determined by R_{SW} , independent of the employed LPTV structure and its configuration. The IL_{TX} can be calculated as follows:

$$IL_{TX} = \frac{1}{S_{21}} = 1 + \frac{Z_0 R_{SW}}{Z_1^2}. \quad (5)$$

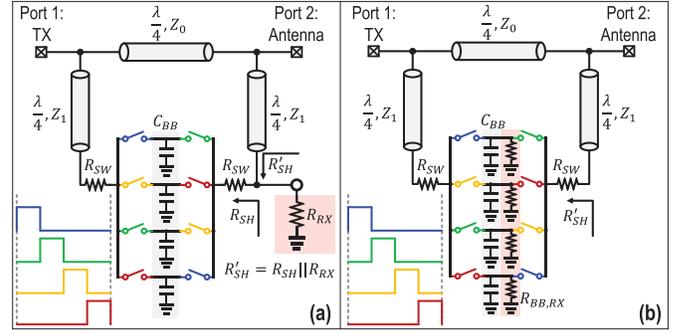


Fig. 5. Magnetic-free CMOS circulators utilizing an N -path filter as LPTV and termination resistor placed at the (a) RX port and (b) baseband.

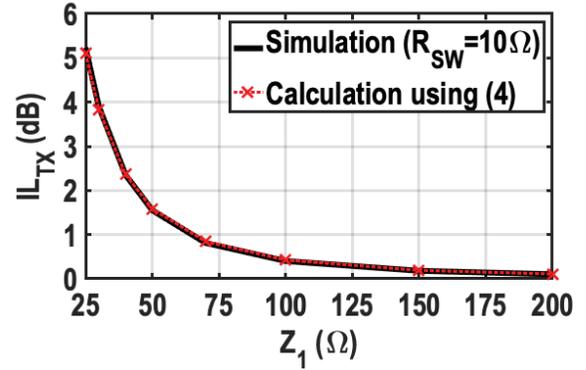


Fig. 6. Simulated and calculated IL_{TX} versus Z_1 while $Z_0 = 50 \Omega$.

As can be inferred from the above equation, selecting a larger Z_1 decreases the IL_{TX} . Note that the TX bandwidth in the TX path is largely determined by the PA and its matching network and is not significantly affected by the value of Z_1 .

As exhibited in Fig. 5(a), the two-port N -path filter is chosen in this work to benefit from its embedded down-converter and compact die area. Considering $Z_0 = 50 \Omega$ and $R_{SW} = 10 \Omega$, Fig. 6 shows the simulation results with ideal switches reasonably match the calculated IL_{TX} using (5).

Since the N -path filter down-converts the RX signal, in the full-duplex front-end mode of operation, the actual RX port of the circulator is left open [$R_{RX} = \infty$; see Fig. 5(a)] [22]. Therefore, assuming an infinite number of paths ($N \rightarrow \infty$) and using a relatively higher impedance value for Z_1 compared to Z_0 , the desired RX signal arrives with a higher voltage amplitude at the baseband, benefiting the conversion gain (G_{RX}) and NF. However, due to the finite number of paths ($N = 4$), the impedance presented by the N -path filter (R_{SH}) is limited. Thus, the G_{RX} and NF improvements are not persistent and slightly degrade at greater Z_1 values. Utilizing $R_{SW} = 10 \Omega$ and $C_{BB} = 500$ fF, the simulation results with ideal switches are demonstrated in Fig. 7, which confirms the substantial improvement of G_{RX} , NF, and TX-to-RX isolation. As shown, $Z_1 = 150 \Omega$ is chosen in this design to maximize G_{RX} and TX-to-RX isolation and minimize IL_{TX} and NF. Nevertheless, to achieve the mentioned benefit, the giveaway is bandwidth. Fig. 8 depicts G_{RX} versus baseband frequency for various Z_1 , where utilizing greater Z_1 narrows the bandwidth. This

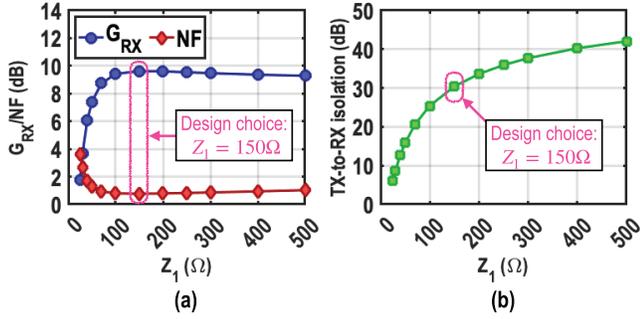


Fig. 7. Simulated (a) G_{RX} , NF and (b) TX-to-RX isolation versus Z_1 while $Z_0 = 50 \Omega$ and $C_{BB} = 500$ fF.

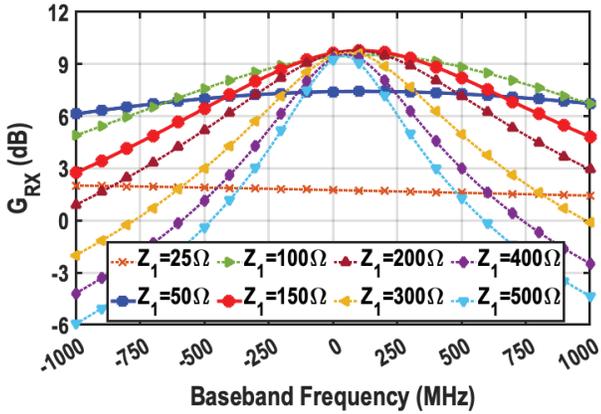


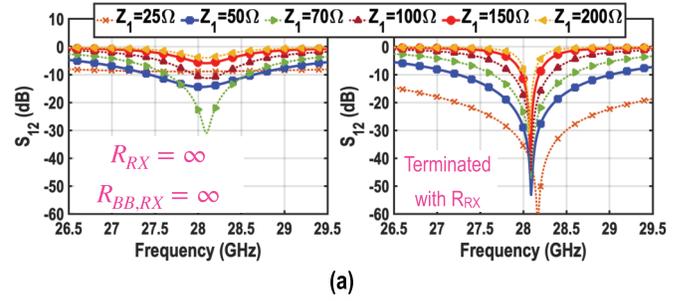
Fig. 8. Simulated G_{RX} versus baseband frequency for various Z_1 values while $Z_0 = 50 \Omega$ and $C_{BB} = 500$ fF.

simulation results indicate an inverse relationship between Z_1 and the 1-dB bandwidth ($BW_{1\text{dB}} \propto (1/Z_1)$); for example, at $Z_1 = 100 \Omega$, the bandwidth is approximately 320 MHz, whereas at $Z_1 = 200 \Omega$, the bandwidth decreases to roughly 155 MHz. Additionally, in an ideal scenario, assuming linear passive components and that overall linearity is predominantly determined by the mixers and the baseband amplifiers, this increased voltage gain directly translates into a degradation of the IIP_2/IIP_3 by roughly the same amount as the gain improvement.

Moreover, as $R_{RX} = \infty$ in the full-duplex configuration, the RX signal passes through the nonreciprocal N -path filter in this structure and is eventually absorbed in the TX port termination [22]. Therefore, a termination resistor R_{RX} must be employed at the RX port to reconfigure the proposed circulator to an isolator. Incorporating with R_{SH} , the termination resistor must provide a matching condition for the clockwise propagating waves, thus establishing reverse isolation from the antenna port to the TX port. Assuming matching conditions at TX and antenna ports, the following condition must be satisfied for the termination resistor:

$$R_{SH} \parallel R_{RX} = \frac{R_{SH} \times |R_{RX}|}{R_{SH} + R_{RX}} = \frac{Z_1^2}{Z_0}. \quad (6)$$

Fig. 9(a) demonstrates the simulated S_{12} (Port 1: TX and Port 2: antenna) without (left) and with (right) R_{RX} termination resistor and reveals three observations: 1) even without a



Values of R_{RX} OR R_{BB} required to terminate the clockwise propagating waves						
Z_1	25Ω	50Ω	70Ω	100Ω	150Ω	200Ω
R_{RX}	19Ω	162Ω	$-1.6k\Omega$	-290Ω	-248Ω	-267Ω
$R_{BB,RX}$	54Ω	590Ω	$-7.2k\Omega$	$-1.15k\Omega$	-980Ω	$-1.06k\Omega$

Fig. 9. (a) Simulated S_{12} without (left) and with (right) R_{RX} termination for various Z_1 values while $Z_0 = 50 \Omega$, $C_{BB} = 500$ fF, and $R_{BB,RX} = \infty$. (b) Resistor values required for R_{RX} or $R_{BB,RX}$ for terminating the reflected wave from the antenna port when the PA port is excited (clockwise propagating waves).

termination resistor, reverse isolation is achieved when $Z_1 = 70 \Omega$; 2) the bandwidth of the reverse isolation, achieved by termination, decreases when it becomes greater than Z_1 ; and 3) as shown in Fig. 9(b), a positive termination resistor is utilized for $Z_1 < 70 \Omega$, while a negative resistor is required to satisfy the termination condition when $Z_1 \geq 70 \Omega$.

Moreover, Fig. 5(b) shows that the clockwise wave can be terminated with the baseband resistors ($R_{BB,RX}$). As reported in Fig. 9(b), the required baseband resistors are larger than RF termination, and their parasitics can be absorbed in the baseband capacitors (C_{BB}).

A. N -Path Filter Design

As mentioned, the nonreciprocal LPTV circuit is implemented as two back-to-back N -path filters to benefit from their compact area, which is crucial for phased array systems. In a conventional N -path filter, for example, a four-path filter, nonoverlapping 25% LO clocks are required to diminish the charge sharing of switches, providing high- Q filtering. Obviously, generating and amplifying 25% LO clocks requires very broadband circuits, which are not feasible at the mm-wave frequencies. In [40] and [41], a quadrature mixer topology is introduced to avoid generating 25% LO clocks for SAW-less GPS applications. Although it simplified the LO generation circuitry, its overall performance does not advance the conventional 25% LO quadrature mixer at GPS operational frequency. We proposed an N -path filter structure with pass-transistor-based AND-gate switches driven by quadrature 50% LO clocks to achieve the nonoverlapping operation at the mm-wave frequencies. In this context, as exhibited in Fig. 10, each path's capacitor is connected to the shared RF node when both switches are ON, replicating bitwise AND-gate operation and resembling 25% nonoverlap switching. Introducing an AND gate series switch doubles the effective ON-resistance in the signal path. To mitigate this, we compensate by doubling the

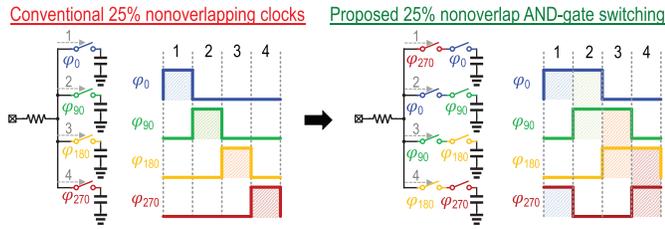


Fig. 10. AND-gate switching N -path filter's principles.

size of the switches to maintain a comparable effective resistance. However, this solution comes at the cost of doubling the switch size, thus increasing the parasitic capacitance by roughly $4\times$. The switches can be driven by sinusoidal LO signals, which enables utilizing inductors to resonate out the parasitic capacitors of the switches.

Unlike conventional subharmonic mixers, which use cascaded double-balanced mixers to operate at $2\times$ LO frequency with 50% switching [42], [43], the proposed structure creates 25% nonoverlap switching at LO frequency. A key advantage of this design is its compact layout, where the series switches are implemented as a single block without intermediate metal connections. This minimizes parasitic capacitance at the middle node, crucial for maintaining high-frequency performance.

B. Design Choices

As mentioned, this article intends to study the feasibility of implementing two separate structures. Therefore, the design choices are made to address the requirements of both architectures instead of optimizing one's performance. For the nonreciprocal delay, the N -path filter can be implemented single-ended or differential [21], [44]. We chose differential to place the circulator between the PA and the balun. Hence, Z_0 is smaller ($22\ \Omega$ instead of $50\ \Omega$), thus, the inductors are smaller. Moreover, the power handling of the circulator/isolator is higher in the differential mode, and it can be scaled further by reducing Z_0 . To increase output power, we need to decrease the PA's required optimum load (R_{opt}), which scales power handling accordingly. Nonetheless, the differential structure offers less conversion gain and NF in the FDD front-end configuration. Its performance also suffers from step-down impedance and balun loss. The required $P_{\text{TX}} - \text{NF} > -13.79\ \text{dBm}$ can be achieved since the power handling is higher. Additionally, the differential structure possibly offers a higher AIP₂.

IV. CIRCUIT IMPLEMENTATION

Fig. 11 demonstrates a detailed schematic of the proposed mm-wave circulator/isolator featuring two back-to-back AND-gate switching N -path filters. A two-step lumped-element CLC π -network is employed to realize the circulator's PA-to-antenna QTL. Its equivalent impedance Z_0 is set to $22\ \Omega$ to match R_{opt} as integrated into a PA's matching network. Two $70\text{-}\Omega$ LCL π -networks are utilized to form the circulator's remaining QTLs. They connect the TX and antenna ports to the LPTV circuit and perform dc blocking. Here, the LCL 's top side inductors are absorbed in C_1 . Accordingly,

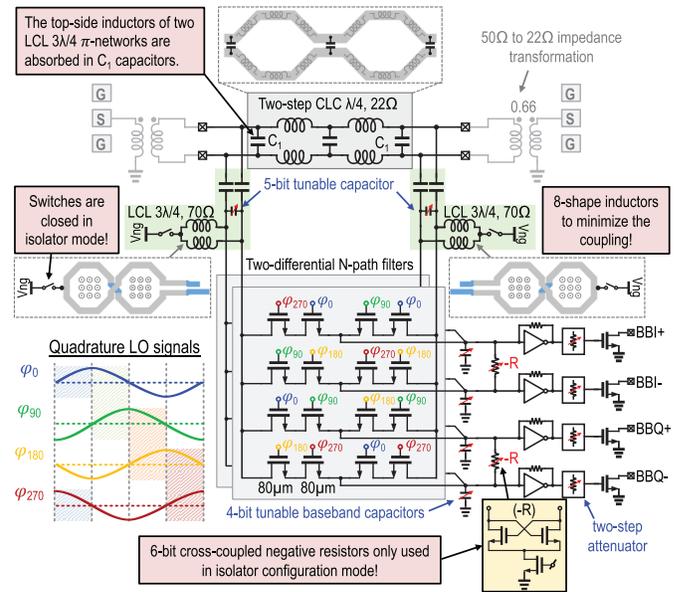


Fig. 11. Schematic of the proposed circulator/isolator.

the proposed LPTV circuit is implemented by two-differential N -path filters (see Fig. 10), whose switches are realized by NMOS transistors with relatively large channel width ($80\ \mu\text{m}$) to minimize their ON-resistance (R_{sw}). In 40-nm bulk CMOS technology, the NMOS devices exhibit an ON-resistance of approximately $1\ \text{k}\Omega/\mu\text{m}$. The parasitic capacitors of the switches are resonated out by two differential inductors, which are combined with the LCL 's bottom-side inductors. Additionally, two 5-bit tunable capacitors are employed to adjust the resonance frequency. As depicted, the inductors are implemented with an 8-shape to minimize the unwanted couplings, thus enabling a compact layout.

The down-converted baseband signals are amplified by self-bias inverter-based transconductance amplifiers and their subsequent open-drain NMOS transistors. A two-step attenuator is implemented in each baseband path, providing possible attenuations of 8 and 16 dB. Besides, 4-bit tunable capacitors are utilized in the baseband to control the RX bandwidth slightly.

As discussed, negative resistors are utilized in the baseband to provide matching conditions for the clockwise propagating waves in the isolator configuration. The negative resistors are implemented using 6-bit switchable cross-coupled NMOS transistors. Their supply voltage (V_{ng}) is provided from the center tap of the 8-shaped inductors. Note that the center tap is open when the circulator configuration is employed.

Regarding stability, using negative resistors in the isolator configuration could potentially create a loading condition that might destabilize the PA or affect return loss. Although we ensure that the PA is unconditionally stable under the tested conditions; however, in a practical implementation, temperature-based reconfiguration of the negative resistors may be required to ensure consistent stability over varying environmental conditions.

Fig. 12 exhibits the implemented quadrature LO generator. Two differential transformer-based quadrature hybrid couplers

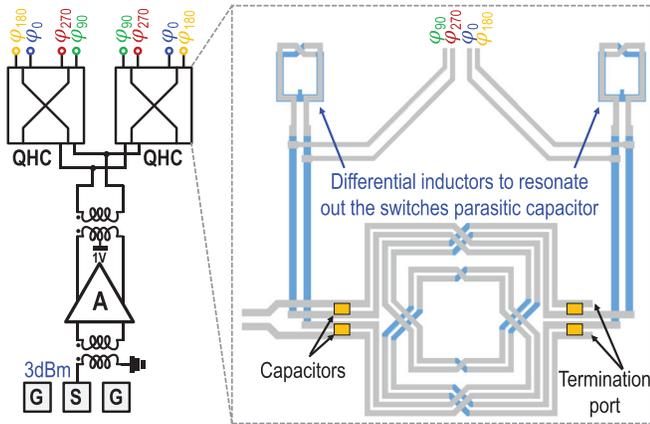


Fig. 12. Schematic of the quadrature LO generator and the 2-D layout view of the implemented QHC.

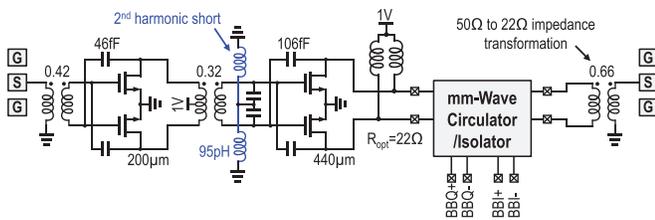


Fig. 13. Schematic of the proposed PA with an integrated circulator/isolator.

(QHCs) generate the mm-wave sinusoidal quadrature LO clocks. Two differential inductors are used to resonate out the parasitic capacitors of the N -path filter’s switches. Moreover, a neutralized common-source input amplifier provides the required LO power level of QHCs.

Fig. 13 demonstrates the schematic of the proposed PA with an integrated circulator/isolator. The circulator/isolator is located between the PA and the output balun. A neutralized common-source push-pull PA is designed with an input second harmonic short condition to boost its linearity. Besides, an 8-shaped symmetrical inductor resonates out the parasitic capacitors of the PA and provides its dc feed. Finally, a neutralized common-source pre-driver is implemented to drive its following PA.

V. MEASUREMENT RESULTS PART—I: “AN FDD FRONT END”

Fig. 14 exhibits the die micrograph of the mm-wave PA with an integrated circulator/isolator and the standalone mm-wave circulator/isolator. The chip is fabricated in 40-nm bulk CMOS technology. The core area occupied by the proposed circulator/isolator, its LO generators, and baluns is 0.38 mm^2 , while the PA with an integrated circulator/isolator occupies 0.7 mm^2 . All measurements are performed using a high-frequency probe station. The dc supplies, bias voltages, digital control signals, and RX baseband signals are wire-bonded directly to an FR4 printed circuit board (PCB). This work uses a 1-V supply voltage for the pre-driver, PA, and LO amplifier, while 1.4-V is used for baseband self-biased transconductances. This section presents the measurement

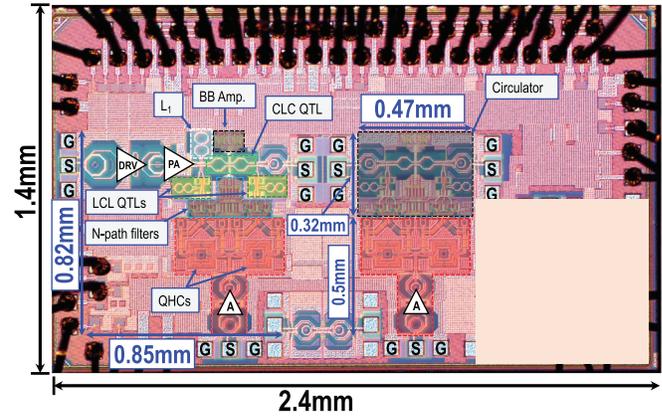


Fig. 14. Die micrograph of the proposed PA with an integrated circulator/isolator.

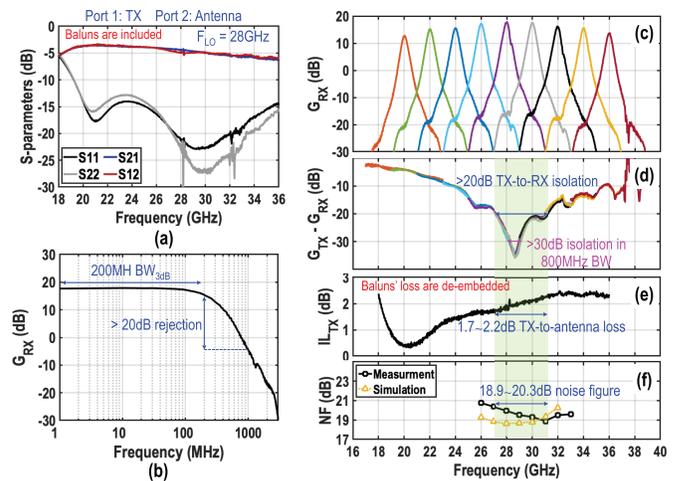


Fig. 15. Measured (a) small-signal S -parameter, (b) RX gain versus baseband frequency, (c) RX-gain at various LO frequencies, (d) TX-to-RX isolation, (e) TX-to-antenna insertion loss over the 20-to-36 GHz band, and (f) noise figure.

results for the circulator/RX configuration to support the mm-wave FDD front end. Note that the cross-coupled negative resistors are off in this configuration, and the switches at the circulator’s 8-shaped inductors’ center tap are open. In all measurements presented in this section, the baseband amplifiers remain active.

A. Circulator Performance

Fig. 15 exhibits the S -parameter measurement results of the circulator, including its baluns’ loss. The RX achieves 400-MHz 3-dB bandwidth (B_{3dB}) with 18-dB gain, and 20-dB rejection at 1-GHz spacing away from the carrier frequency. Moreover, the circulator is widely tunable over a 22-to-36-GHz band trade off, which exists in a 30-dB TX-to-RX isolation in an 800-MHz bandwidth. It also offers >20 -dB isolation within the 27.1–31.1-GHz band. The measured IL_{TX} is 1.7–2.2 dB, and the noise figure (NF) is 18.9–20.3 dB in the same band. Note that the measured NF includes the insertion-loss/NF of the circulator and the mixer-first down conversion path. Simulations indicate that the balun’s

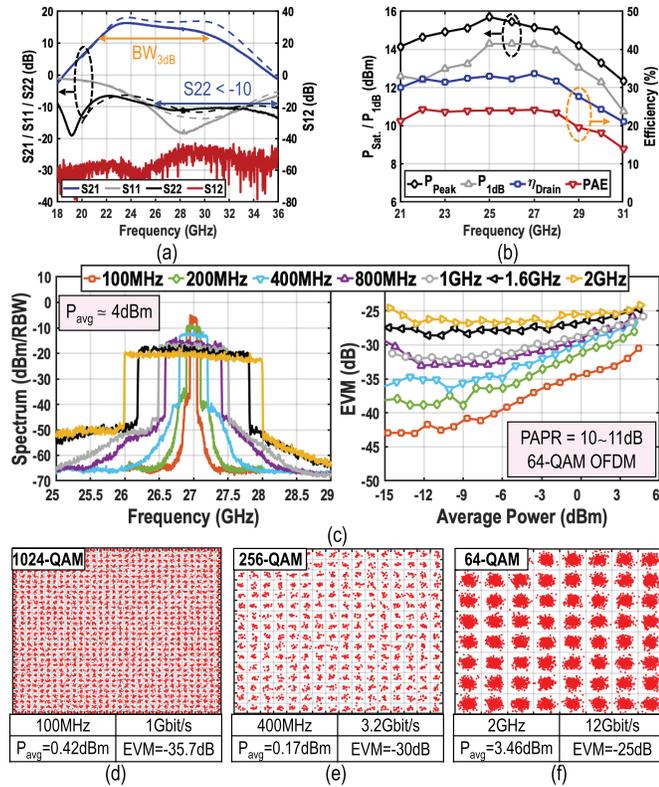


Fig. 16. (a) Measured (solid lines) and simulated (dashed lines) small-signal S -parameters, (b) measured large-signal CW, and (c) measured 64-QAM OFDM signals spectrum and EVM versus output power of the TX path for various modulation bandwidths. The measured constellations of (d) 1024-QAM, (e) 256-QAM, and (f) 64-QAM OFDM signals.

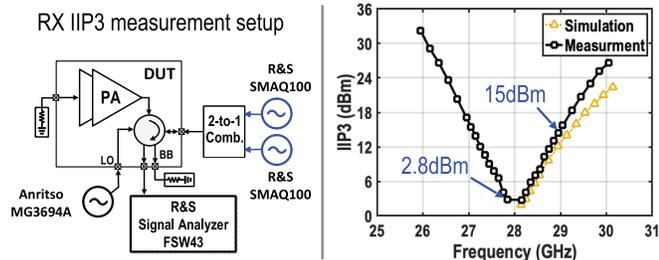


Fig. 17. Measurement setup and the measured IIP3.

impedance transformation ($50 \rightarrow 22 \Omega$) incurs about 5.6 dB of loss, the circulator stage adds roughly -3.3 dB—primarily due to the high effective switch resistance (25Ω), even though a gain was expected—and the mixer contributes about 1.2-dB conversion loss. Additional degradation from parasitic capacitances further impacts performance. Therefore, there is a trade-off between PA power handling and RX's NF. Here, we prioritized the PA power handling for the benefit of the isolator configuration. Nevertheless, employing more advanced technology nodes that offer lower switching impedance with much lower parasitic capacitors can improve RX performance and IL_{TX} , thus increasing TRX's LB.

B. Tx Performance

Fig. 16 demonstrates the small-signal and large-signal performance of the TX path. The S -parameter measurement results show that the integrated PA offers almost 10-GHz B_{3dB}

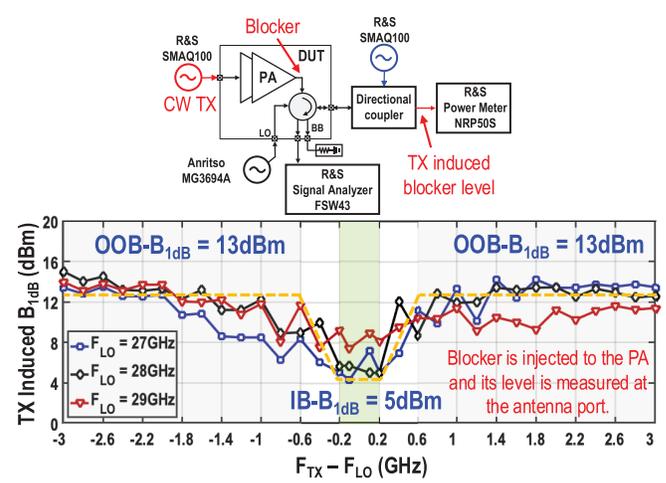


Fig. 18. Measurement setup and the measured TX induced B_{1dB} at various carrier frequencies.

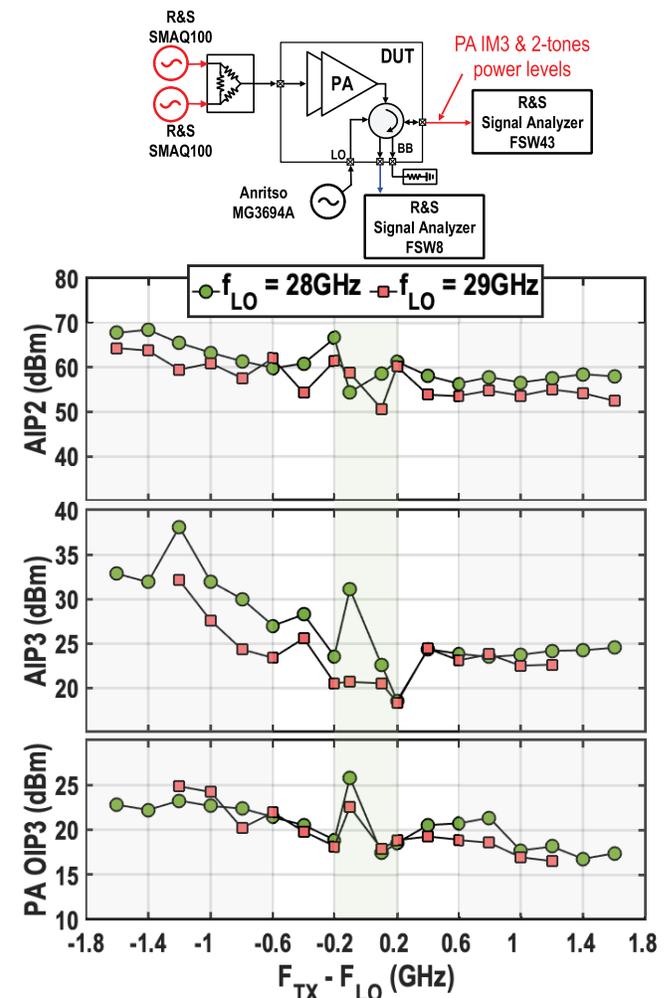


Fig. 19. Measurement setup and the measured PA OIP3, FDD front-end AIP3, and AIP2.

with 15.4-dB small-signal gain. Owing to the relatively low measured IL_{TX} , the PA achieves 15.15-dBm peak power at the antenna port with 33%/24.2% drain-efficiency/PAE. Its

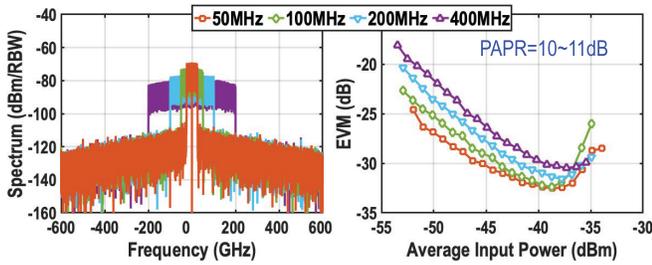


Fig. 20. OFDM signal measurement results of the RX path.

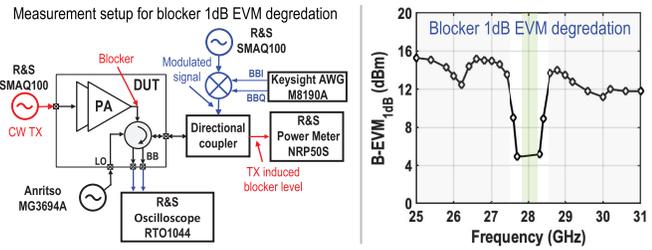


Fig. 21. RX EVM degradation under the OOB CW TX blocker measurement setup and results.

$P_{1\text{ dB}}$ also exceeds 14 dBm. The spectrum and EVM of the modulated 64-QAM OFDM signals with various modulation bandwidths, up to 2 GHz, are depicted in Fig. 16. Additionally, the measured constellations of 1024-QAM, 256-QAM, and 64-QAM OFDM signals are shown, achieving up to 12 Gbit/s data rate, which is limited by measurement instruments.

C. RX Performance

First, the IIP3 is measured using the measurement setups shown in Fig. 17, where the measured IB IIP3 is 2.8 dBm while the related OOB IIP3 at 600 MHz offset is 15 dBm. As illustrated in Fig. 18, RX gain compression under a large blocker is measured when the CW blocker signal is applied to the PA, and its power is measured and reported at the antenna port. The measured TX induced $B_{1\text{ dB}}$ at various carrier frequencies are demonstrated in Fig. 18, where the front end achieves better than 5-dBm IB TX induced $B_{1\text{ dB}}$ while its OOB TX induced $B_{1\text{ dB}}$ is 13 dBm, confirming its capability to support FD and FDD TRX operations. Additionally, OIP3 of the PA and AIP2/AIP3 of the fully integrated FDD front end are measured using the measurement setups shown in Fig. 19. Fig. 19 presents the measured PA OIP3, FDD front end AIP3, and AIP2. A class-AB biasing condition is employed to diminish PA’s OIP3 contribution to AIP2, while the second harmonic is shorted at the PA input. As determined by (4), the FDD front end may require a higher OOB AIP2, depending on the modulation bandwidth and number of antennas. Hence, a better layout practice, an improved ground and supply isolation, and an IIP2 calibration can potentially improve AIP2.

Moreover, Fig. 20 exhibits a 64-QAM OFDM spectrum and EVM with modulation bandwidths up to 400 MHz. The RX EVM degradation under an OOB CW TX blocker is also measured; as shown in Fig. 21, a CW TX blocker level that causes a 1-dB degradation in the EVM of a 400-MHz OFDM

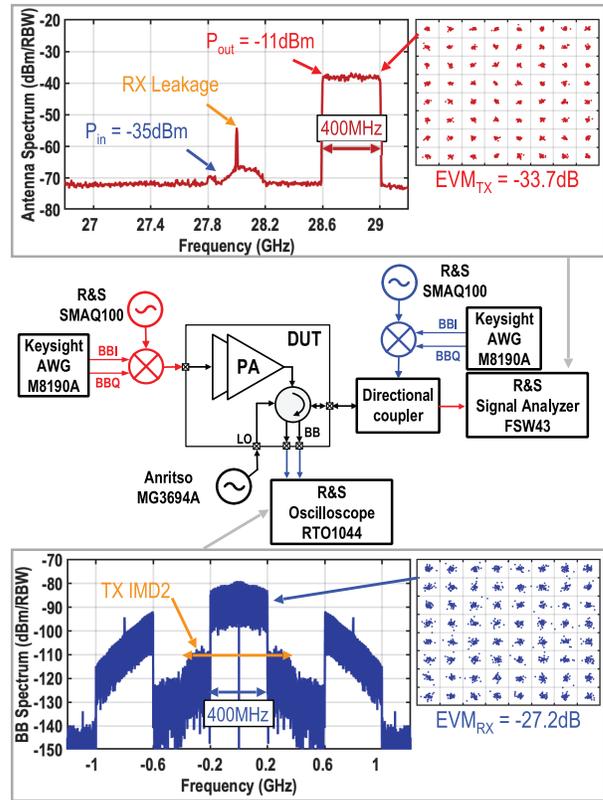


Fig. 22. Full simultaneously transmit and receive FDD measurement results. A -35-dBm 400-MHz 64-QAM OFDM RX signal at the 28-GHz carrier frequency is injected into the antenna port through a directional coupler. Simultaneously, a -11-dBm 400-MHz 64-QAM OFDM TX signal at the 28.8-GHz carrier frequency is delivered to the antenna port by the PA.

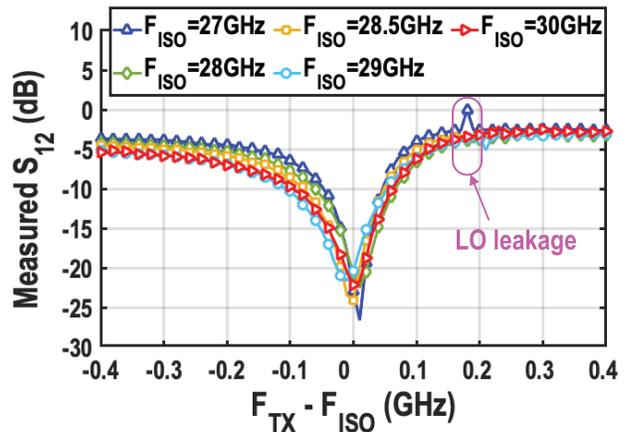


Fig. 23. Measured S_{12} of the standalone isolator while cross-coupled negative resistors are ON.

signal is observed. This measurement not only reflects linearity degradation but also captures the TX-induced degradation in the RX NF. Owing to the circulator’s effective suppression of TX leakage, the TX-induced NF and linearity degradation remain within acceptable limits, as evidenced by the modest overall EVM degradation. Consequently, the proposed front end can support FDD, although an additional SIC is required for IBFD applications.

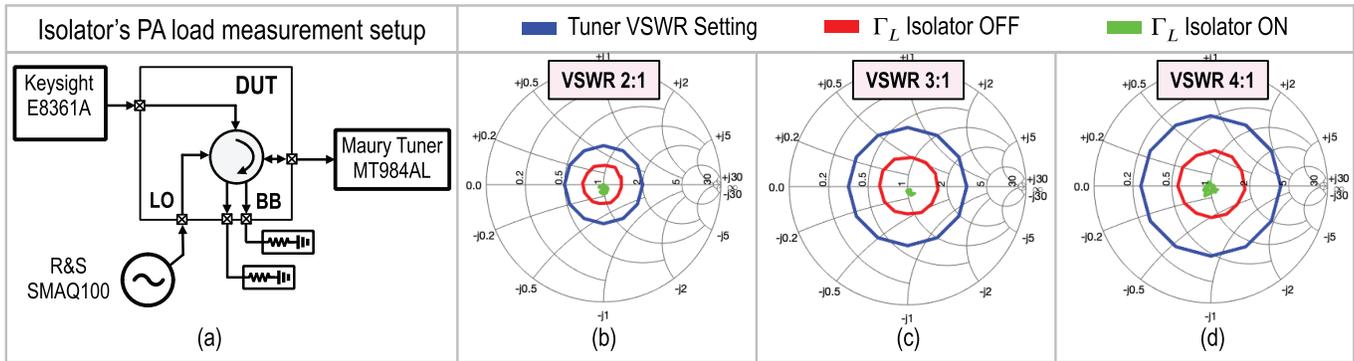


Fig. 24. (a) Simplified measurement setup. The measured load provided by the isolator for (b) VSWR 2:1, (c) VSWR 3:1, and (d) VSWR 4:1.

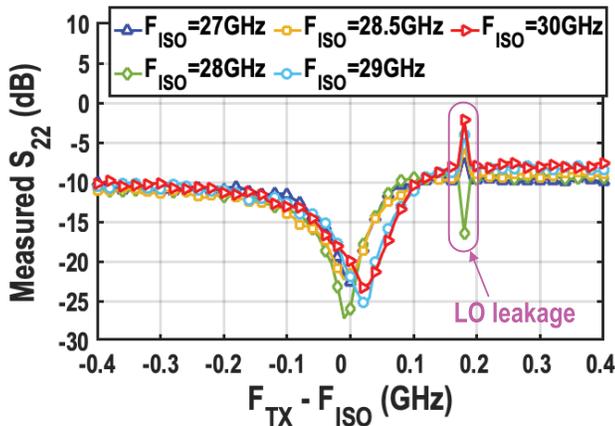


Fig. 25. Measured S_{22} of the PA with the integrated isolator while cross-coupled negative resistors are ON.

Lastly, Fig. 22 demonstrates full FDD measurement results, where a -35 -dBm 400-MHz 64-QAM OFDM RX signal at 28-GHz carrier frequency is injected to the antenna port, while a -11 -dBm 400-MHz 64-QAM OFDM TX signal at 28.8-GHz carrier frequency is delivered to the antenna port. Note that TX IMD2 limits the PA's output power and requires further IIP_2 calibration. The baseband spectrum shows >40 -dB TX suppression owing to TX-to-RX isolation of the circulator and suppression of the N -path filter down-converter.

VI. MEASUREMENT RESULTS PART—II: “A VSWR RESILIENT PA”

This section presents the measurement results of the isolator configuration, where the switches at the circulator's 8-shape inductors' center tap are connected to a 0.7-V supply. Using 6-bit control settings, a fraction of cross-coupled negative resistors turn on to achieve reverse isolation in the isolator. As we expected, Fig. 15(a) shows that in the standalone circulator configuration, S_{12} is almost equal to S_{21} , achieving no reverse isolation. On the contrary, Fig. 23 reports the measured S_{12} of the stand-alone isolator configuration, showing >15 -dB reverse isolation. This reverse isolation is necessary to provide optimum loading conditions for the PA independent of the actual antenna load. Since the integrated isolator is part of the

PA, its power consumption must be taken into account; hence, the revised peak PAE is 15.1%.

The unexpected behavior in Fig. 23 at $F_{TX} - F_{ISO} \approx 0.2$ GHz is due to LO leakage from the N -path filter, which interferes with small-signal CW measurements. This effect is exacerbated by the lack of phase synchronization between the VNA and LO signal source, as well as low measurement power. To mitigate this, the isolator's operating frequency (F_{ISO}) was tuned 200 MHz away from the LO frequency, using the 5-bit tunable capacitors (see Fig. 11), though some residual LO leakage remains, explaining the observed artifact.

Fig. 24(a) presents the simplified setup used to measure the load provided by the isolator for the PA. Fig. 24(b)–(d) exhibits the measured load at 28.5 GHz, where the blue line is the VSWR of the antenna provided by the load tuner, the red line is the load seen by the PA when the isolator is off, and the green line is the load seen by the PA when the isolator is ON. The measurement results confirm that the isolator can always provide a perfect optimum load for the PA even for VSWRs 4:1. Note that the radius of the red circle is smaller than the antenna VSWR circle owing to the loss of the balun and the circulator/isolator.

Furthermore, the PA with the integrated isolator is evaluated. As shown in Fig. 16(a), S_{22} of the PA in the FDD front-end configuration is around 10 dB. However, since the signal injected from the antenna port is absorbed in the isolation configuration, S_{22} is expected to be improved. Fig. 25 exhibits the measured S_{22} of the PA when a fraction of the cross-coupled negative resistors is ON. As shown in Fig. 9, a narrow band S_{12} and consequently a narrow band S_{22} were expected as we chose a larger Z_1 value compared to Z_0 . Nonetheless, the bandwidth can be improved by selecting a smaller Z_1 at the cost of higher IL_{TX} .

Lastly, we measured the amplitude-to-phase (AM-PM) distortions at the input compression point (IP_{1dB}) of the PA versus load VSWR. Fig. 26 compares the measured AM-PM distortions and IP_{1dB} (circles) of the PA with and without the isolator's contribution. Note that we reported 12 measurement results for VSWR 1:1 to show the repeatability of the measurements. As demonstrated, the isolator provides a relatively high VSWR resiliency at the lower powers. However, moving toward peak power, the AM-PM improvement degraded due to the saturation of the switches. As such, the voltage swing

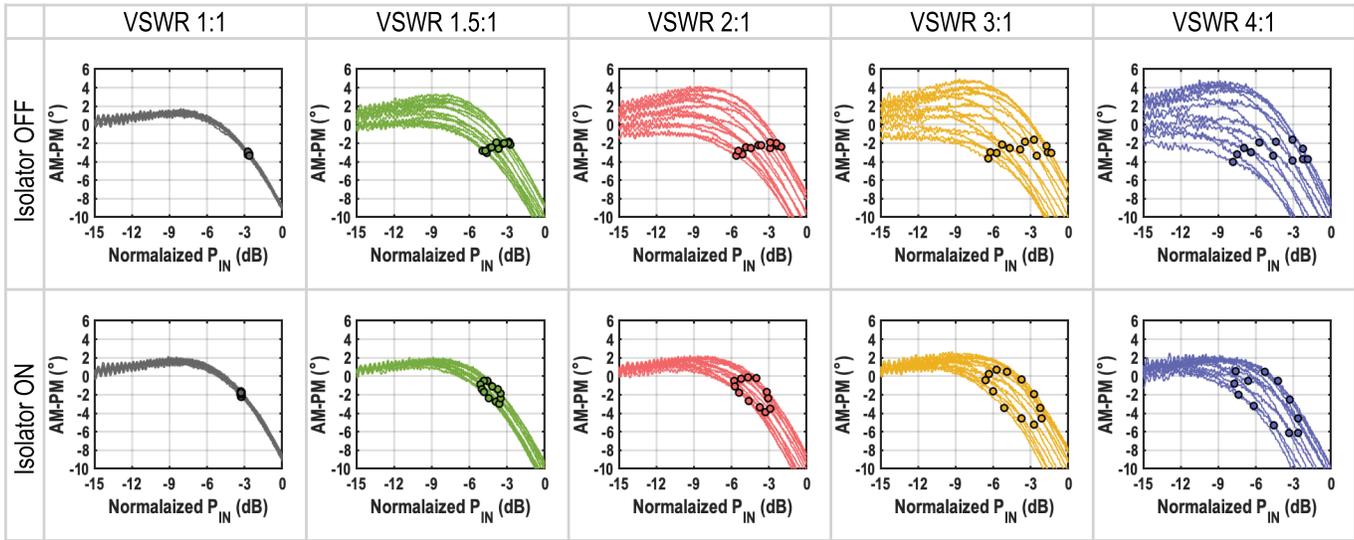


Fig. 26. Measured AM-PM distortions and IP_{1dB} of the PA with and without isolator's contribution.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR WORKS

Parameter	This Work	Nonreciprocal Circulators / RXs			Active Quasi-Circulator		Blocker Tolerant RX / Filter			FD / FDD TRX	
		Reiskarimian ISSCC 2017	Dinc ISSCC 2017	Garg ISSCC 2021	Hwang JSSC 2024		Boynton RFIC 2020	Song RFIC 2020	Hari RFIC 2021	Mondal ISSCC 2019	Shahramian RFIC 2022
Architecture	PA with an integrated N-path filter based isolator/circulator/RX	N-path filter based circulator RX	Circulator with nonreciprocal delay	FD circulator RX with SIC	Distributed active quasi-circulator		Series mixer-first RX	Mixer-first RX with passive Elliptic LPF	Reflection-mode N-path filter	Separate antenna TRX	FDD Module-on-glass TRX
Technology	40nm CMOS	65nm CMOS	45nm SOI	45nm SOI	28nm CMOS		65nm CMOS	65nm CMOS	45nm SOI	65nm CMOS	130nm SiGe
Core Area (mm ²)	0.7 (FD/FDD front-end), 0.38 (Circulator RX)	0.94	2.16	4.54	0.25		NR	0.63	2.25 (Die)	0.48 (Single channel)	12.4 (Die) 1040 (Module)
Supply (V)	1 (PA + LO), 1.4 (BB)	2.4	NR	NR	2		NR	1.2	1→1.3	1	3.3
Frequency (GHz)	TX: 21-31, RX: 22-36	0.61-0.975	22.7-27.3	25.5-27.75	25.7-27.4	20.5-35.5	9-31	21-29	6-31	28 & 37	71-76 & 81-86
G_{RX} (dB)	18	28	-3.2 (Ant. to RX)	16.1	-3.1 (Ant. to RX)	-7.3 (Ant. to RX)	40	3-6	-6 @28GHz*	16.1 & 10.9	72
RX BW_{3dB} (MHz)	400	20	NA	800	NA	NA	NR	500	1-1.22GHz	500	4000
NF (dB)	18.9-20.4	6.3	3.3-4.4 (without RX)	5.8	8.9-11.1	16.1-16.7	12.5-17	12-14.5	18.5 @28GHz*	6.2 & 7.0	6.6-7.9 & 7.2-8.4
IB IIP3 (dBm)	2.8	-18.4	NA	NR	NA	NA	NR	NR	6.3	NR	>0 (?)
OOB IIP3 (dBm)	15 ($\Delta F/BW=1.5$)	15.4 ($\Delta F=500MHz$)	NA	NR	NA	NA	21*	NR	20 ($\Delta F/BW=1$)	NR	NR
IB B_{1dB} (dBm)	5†	NR	NA	11.5 (with SIC)	NA	NA	-45*	-6	-8*	NR	NR
OOB B_{1dB} (dBm)	13* ($\Delta F/BW=1.5$)	NR	NA	NR	NA	NA	-6→-4	3.4 ($\Delta F/BW=2$)	4.4 ($\Delta F/BW=1$)	NR	NR
TX-to-antenna insertion loss (dB)	1.8 @ 28GHz	1.8	3.3	3.1	2.4-3.1	1.9-4.5	NA	NA	NA	NA	2.5-3*
TX-to-RX isolation (dB)	>30 (28.3-29.1GHz) >20 (27.1-31.1GHz)	26* / 40 (with Bal. Network)	>18.5	53 (with SIC)	>20	>21	NA	NA	NA	NA	>40
P_{DC} (mW)	LO buffer: 89 Baseband: 19.9	108	78.4	RX: 88 SIC: 23.5	28.6	107	72→162	22.8	146-384	37.6 (Single channel)	RX*: 2000 TX*: 3200

*Graphically estimated †Blocker signal is applied to the PA, and its level is measured at the antenna port *Single supply including LDOs, configuration and calibration functions.

at the N -path filter nodes can be reduced by choosing a smaller Z_1 in the cost of higher IL_{TX} . IP_{1dB} follows a similar trend, indicating limited improvement at higher output power levels.

Table I summarizes the measured results of the proposed mm-wave front end and compares them with those of the state-of-the-art in three different modes of operation, namely, non-reciprocal circulators/RXs, blocker-tolerant RX/filters, and FD/FDD front end. To the best of the author's knowledge, the realized prototype is the first reconfigurable fully integrated mm-wave FDD front end featuring integrated PA, isolator, circulator, and RX.

VII. CONCLUSION

This article features a fully integrated mm-wave FDD front end, comprising a two-stage PA, an integrated circulator as the duplexer, and a mixer-first RX implemented as a part of the circulator. The proposed circulator/isolator is realized by utilizing an advanced ring QTL topology with adjusted characteristic impedances to improve TX-to-antenna insertion loss and TX-to-RX isolation at the cost of a narrower bandwidth. The implemented circulator's LPTV circuit consists of an AND-gate switching-based N -path filter, enabling a mixer-first RX operation. As a proof of concept, a configurable prototype chip is realized in 40-nm bulk CMOS whose circulator occupies

only 0.38 mm² core area, thanks to the ultra-compact N -path filter structure. Including its isolator's loss, the PA delivers 15.15 dBm peak output power with 33% drain efficiency. The realized front-end prototype occupies only 0.7 mm², including circulator, PA, quadrature hybrid coupler LO generators, and baseband circuits. The functionality of the proposed FDD front end is evaluated by a STAR measurement with 400 MHz TX/RX modulation bandwidth and channel spacing. Moreover, the PA with the integrated isolator showed a significant VSWR resiliency at the lower power level. However, its robustness against VSWR was degraded around its peak output power.

REFERENCES

- [1] M. Boers et al., "A 16TX/16RX 60 GHz 802.11ad chipset with single coaxial interface and polarization diversity," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3031–3045, Dec. 2014.
- [2] A. Tomkins et al., "A 60 GHz, 802.11ad/WiGig-compliant transceiver for infrastructure and mobile applications in 130 nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2239–2255, Oct. 2015.
- [3] B. Sadhu et al., "A 250-mW 60-GHz CMOS transceiver SoC integrated with a four-element AiP providing broad angular link coverage," *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1516–1529, Jun. 2020.
- [4] D. Guermandi et al., "A 79-GHz 2 × 2 MIMO PMCW radar SoC in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2613–2626, Oct. 2017.
- [5] M. Kalantari, W. Li, H. Shirinabadi, A. Fotowat-Ahmady, and C. P. Yue, "A W-band single-antenna FMCW radar transceiver with adaptive leakage cancellation," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1655–1667, Jun. 2021.
- [6] T. Dinc, S. Kalia, S. Akhtar, B. Haroun, B. Cook, and S. Sankaran, "High-efficiency class-E power amplifiers for mmWave radar sensors: Design and implementation," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1291–1299, May 2022.
- [7] S. A. Busari, K. M. S. Huq, S. Mumtaz, L. Dai, and J. Rodriguez, "Millimeter-wave massive MIMO communication for future wireless systems: A survey," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 2, pp. 836–869, 2nd Quart., 2018.
- [8] B. Sadhu et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.
- [9] A. Verma et al., "A 16-channel, 28/39GHz dual-polarized 5G FR2 phased-array transceiver IC with a quad-stream IF transceiver supporting non-contiguous carrier aggregation up to 1.6GHz BW," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 1–3.
- [10] B. Sadhu et al., "A 24–30-GHz 256-element dual-polarized 5G phased array using fast on-chip beam calculators and magnetoelectric dipole antennas," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3599–3616, Dec. 2022.
- [11] H.-C. Park et al., "4.1 a 39GHz-band CMOS 16-channel phased-array transceiver IC with a companion dual-stream IF transceiver IC for 5G NR base-station applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 76–78.
- [12] J. D. Dunworth et al., "A 28GHz bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 70–72.
- [13] S. Shahramian et al., "An all-silicon E-band backhaul-on-glass frequency division duplex module with <24dBm PSAT & 8dB NF," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2022, pp. 59–62.
- [14] S. Mondal, R. Singh, and J. Paramesh, "21.3 a reconfigurable bidirectional 28/37/39GHz front-end supporting MIMO-TDD, carrier aggregation TDD and FDD/full-duplex with self-interference cancellation in digital and fully connected hybrid beamformers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 348–350.
- [15] R. Garg, S. Jain, P. Dania, and A. Natarajan, "14.3 a 26GHz full-duplex circulator receiver with 53dB/400MHz(40dB/800MHz) self-interference cancellation for mm-wave repeaters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 222–224.
- [16] S. Mondal and J. Paramesh, "Power-efficient design techniques for mm-wave hybrid/digital FDD/full-duplex MIMO transceivers," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2011–2026, Aug. 2020.
- [17] B. van Liempd, J. Craninckx, R. Singh, P. Reynaert, S. Malotau, and J. R. Long, "A dual-notch +27dBm tx-power electrical-balance duplexer," in *Proc. ESSCIRC 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 463–466.
- [18] G. Qi, B. van Liempd, P. Mak, R. P. Martins, and J. Craninckx, "A SAW-less tunable RF front end for FDD and IBFD combining an electrical-balance Duplexer and a switched-LC N -path LNA," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1431–1442, May 2018.
- [19] K. Shi, H. Darabi, and A. A. Abidi, "Design and analysis of an electrical balance duplexer with independent and concurrent dual-band TX-RX isolation," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1385–1396, May 2022.
- [20] J. Hwang, D. Yoo, and B.-W. Min, "Compact mm-wave ultra-wideband and low-noise phase alternately distributed quasi-circulators," *IEEE J. Solid-State Circuits*, vol. 59, no. 5, pp. 1351–1360, May 2024.
- [21] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, "A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, May 2017.
- [22] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, "Analysis and design of commutation-based circulator-receivers for integrated full-duplex wireless," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2190–2201, Aug. 2018.
- [23] M. B. Dastjerdi, S. Jain, N. Reiskarimian, A. Natarajan, and H. Krishnaswamy, "Analysis and design of a full-duplex two-element MIMO circulator-receiver with high TX power handling exploiting MIMO RF and shared-delay baseband self-interference cancellation," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3525–3540, Dec. 2019.
- [24] N. Reiskarimian, M. Khorshidian, and H. Krishnaswamy, "Inductorless, widely tunable N -path shekel circulators based on harmonic engineering," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1425–1437, May 2021.
- [25] T. Dinc, A. Nagulu, and H. Krishnaswamy, "A millimeter-wave non-magnetic passive SOI CMOS circulator based on spatio-temporal conductivity modulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3276–3292, Dec. 2017.
- [26] A. Nagulu and H. Krishnaswamy, "28.5 non-magnetic 60GHz SOI CMOS circulator based on loss/dispersion-engineered switched bandpass filters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 446–448.
- [27] P. Song and H. Hashemi, "Mm-wave mixer-first receiver with passive elliptic low-pass filter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 271–274.
- [28] S. Hari, C. J. Ellington, and B. A. Floyd, "A 6–31 GHz tunable reflection-mode N -path filter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 143–146.
- [29] Z. G. Boynton and A. Molnar, "RTu1B-3 a 9–31GHz 65nm CMOS down-converter with >4dBm OOB B1dB," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 279–282.
- [30] C. Yang, S. Su, and M. S. Chen, "Millimeter-wave receiver with non-uniform time-approximation filter," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1201–1211, May 2023.
- [31] O. Barrera, S. Cho, J. Kramer, V. Chulukhadze, J. Campbell, and R. Lu, "38.7 GHz thin film lithium niobate acoustic filter," in *Proc. IEEE Int. Microw. Filter Workshop (IMFW)*, Feb. 2024, pp. 87–90.
- [32] S. Cho et al., "23.8-GHz acoustic filter in periodically poled piezoelectric film lithium niobate with 1.52-dB IL and 19.4% FBW," *IEEE Microw. Wireless Technol. Lett.*, vol. 34, no. 4, pp. 391–394, Mar. 2024.
- [33] M. Pashaefar, L. C. N. de Vreede, and M. S. Alavi, "A millimeter-wave mutual-coupling-resilient double-quadrature transmitter for 5G applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3784–3798, Dec. 2021.
- [34] M. Pashaefar, A. Kumar Kumaran, L. C. N. De Vreede, and M. S. Alavi, "A chain-weaver balanced power amplifier with an embedded impedance/power sensor," *IEEE J. Solid-State Circuits*, vol. 59, no. 12, pp. 3938–3951, Dec. 2024.
- [35] N. S. Mannem, M. Huang, T. Huang, and H. Wang, "A reconfigurable hybrid series/parallel Doherty power amplifier with antenna VSWR resilient performance for MIMO arrays," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3335–3348, Dec. 2020.
- [36] C. R. Chappidi, X. Wu, and K. Sengupta, "Simultaneously broadband and back-off efficient mm-Wave PAs: A multi-port network synthesis approach," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2543–2559, Sep. 2018.

- [37] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri, "Integrated self-healing for mm-wave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1301–1315, Mar. 2013.
- [38] M. Pashaeifar, L. C. N. De Vreede, and M. S. Alavi, "A millimeter-wave front-end for FD/FDD transceivers featuring an embedded PA and an N-path filter based circulator receiver," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2022, pp. 11–14.
- [39] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1348–1360, May 2018.
- [40] O. Ikeuchi, N. Saito, and B. Nauta, "Quadrature sampling mixer topology for SAW-less GPS receivers in 0.18 μ m CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2010, pp. 177–178.
- [41] J. Kim and J. Silva-Martinez, "Low-power, low-cost CMOS direct-conversion receiver front-end for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2090–2103, Sep. 2013.
- [42] L. Sheng, J. C. Jensen, and L. E. Larson, "A wide-bandwidth Si/SiGe HBT direct conversion sub-harmonic mixer/downconverter," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1329–1337, Sep. 2000.
- [43] A. Mazzanti, E. Sacchi, P. Andreani, and F. Svelto, "Analysis and design of a double-quadrature CMOS VCO for subharmonic mixing at Ka-band," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 2, pp. 355–363, Feb. 2008.
- [44] A. Nagulu et al., "Nonreciprocal components based on switched transmission lines," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4706–4725, Nov. 2018.



Masoud Pashaeifar (Member, IEEE) received the M.Sc. degree in circuits and systems from the University of Tehran, Tehran, Iran, in 2013, and the Ph.D. degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2024.

He led the Hardware Research Group, Bakhtar Communication Company, Tehran, from 2014 to 2018, focusing on wireless communication system design. From September 2022 to December 2024, he was with Apple Inc., Munich, Germany, as a

Senior mm-Wave IC Design Engineer. He is currently a Principal Wireless Connectivity Architect and Designer with NXP Semiconductors, Eindhoven, The Netherlands, where he develops next-generation communication systems. His research interests include millimeter-wave (mm-wave) and sub-THz integrated circuit and system design for wireless communication and radar applications.

Dr. Pashaeifar received the IEEE Solid-State Circuits Society Predoctoral Achievement Award from 2021 to 2022.



Leo C. N. de Vreede (Senior Member, IEEE) received the Ph.D. degree (cum laude) from Delft University of Technology, Delft, The Netherlands, in 1996.

In 1996, he was appointed as an Assistant Professor with Delft University of Technology, working on the nonlinear distortion behavior of active devices. In 1999 and 2015, he was appointed as an Associate Professor and a Full Professor at Delft University of Technology, where he became responsible for the Electronic Research Laboratory (ERL/ELCA).

During that period, he worked on solutions for improved linearity and RF performance at the device, circuit, and system levels. He is currently a Co-Founder/Advisor of Anteverta-mw, Eindhoven, The Netherlands, a company that specializes in RF device characterization. He has co-authored more than 130 IEEE-refereed conference papers and journal articles. He holds several patents. His current research interests include RF measurement systems, RF technology optimization, and (digital-intensive) energy-efficient/wideband circuit/system concepts for wireless applications.

Dr. de Vreede was a co-recipient of the IEEE Microwave Prize in 2008 and a Mentor of the Else Kooi Prize Awarded Ph.D. Work in 2010 and the Dow Energy Dissertation Prize Awarded Ph.D. Work in 2011. He was a recipient of the TUD Entrepreneurial Scientist Award in 2015. He co-guided several students who won (Best) Paper Awards at the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), the Program for Research on Integrated Systems and Circuits (PRORISC), the European Solid-state Circuits and Devices Conference (ESSDERC), the International Microwave Symposium (IMS), the Radiofrequency Integration Technology (RFIT), and the Radio Frequency Integrated Circuits Symposium (RFIC).



Morteza S. Alavi (Senior Member, IEEE) was born in Tehran, Iran. He received the B.S.E.E. degree from Iran University of Science and Technology, Tehran, in 2003, the M.S.E.E. degree from the University of Tehran, Tehran, in 2006, and the Ph.D. degree in electrical engineering from Delft University of Technology (TU-Delft), Delft, The Netherlands, in 2014.

He was the Co-Founder and CEO of DitIQ B.V., Delft, a local company developing energy-efficient, wideband wireless transmitters for the next

generation of the cellular network. Since September 2016, he has been with the Electronic Circuits and Architectures (ELCA) Research Group, TU-Delft, where he is currently an Associate Professor. He has co-authored the book *Radio-Frequency Digital-to-Analog Converter* (Elsevier, 2016). His primary research interests are designing high-frequency and high-speed wireless/cellular communication and in the field of wireline transceivers.

Dr. Alavi and his students received many awards, including the Best Student Paper Award (First Place) of the 2017 RFIC Symposium held in Honolulu, HI, USA, the 2021 Institute of Semiconductor Engineers (ISE) President Best Paper Award of the International SoC Design Conference (ISOCC), and the 2022 Best Paper Award of the honorable mentioned IEEE Brain and SSCS Joint Communities paper.