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Analysis and Design of Connected Slot Arrays with Artificial Dielectrics

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Abstract—Connected arrays of slots loaded with artificial dielectric layers have been proposed to realize wideband phased arrays with large scan capability. The role of the artificial dielectric superstrate is to provide a wide angle impedance matching transformation from the impedance at the feeding port of the unit cell to the free space impedance. This wideband transformer also reduces the negative effects of the ground plane on the impedance matching. Unlike dielectric superstrates, artificial dielectrics can avoid the propagation of surface waves and the occurrence of scan blindness over very wide scan volumes and large frequency ranges. The analytical method used for the modeling of the unit cell is described. The analysis is based on closed-form expressions for both the connected array and the artificial dielectric, thus it can be used to simulate the main array parameters with minimal computation resources. The method is then used to design a 5:1 connected array with scanning capability up to 60 degrees in all azimuthal directions.

Index Terms—artificial dielectrics, connected slot array, phased arrays, wideband arrays, wide scanning

I. INTRODUCTION

Antenna arrays that can operate over wide bandwidths and wide scan ranges have become increasingly attractive for multifunction radar and communication systems, in order to reduce the number of antennas on platforms where space is at a premium. Among others, some of the solutions that have been proposed for wideband, wide scanning arrays include tapered slot antennas [1]–[3], metal flared-notch elements [4], [5], long-slot arrays [6], [7] and tightly-coupled dipole arrays [8]–[11].

Most of the mentioned designs are based on array configurations where the radiating elements and the feed structure are printed on vertical printed circuit boards (PCBs) [12]. Such an arrangement can lead to costly assembly, and its complexity increases when dual-polarization is required and when the array period is reduced to target operation at higher frequency. This issue motivated research efforts to enable implementation of the arrays based on a single multilayer planar PCB [13]–[15].

One of the proposed concepts that allows for a planar array configuration was demonstrated in [16] and consists of an array of connected slots with artificial dielectric layers (ADLs) as a superstrate. The ADLs provides a broadband impedance transformer, as proposed in [17]. Moreover, thanks to their equivalent anisotropic properties, the ADLs do not excite surface waves over large frequency and scan ranges.

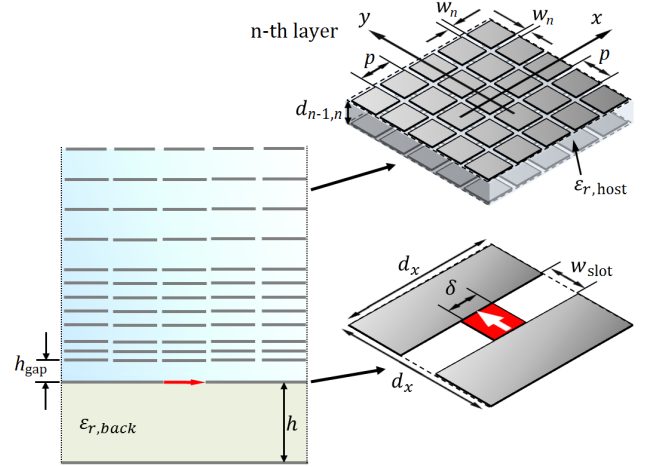


Fig. 1. Unit cell of the connected slot array loaded with ADLs.

The design in [16] targeted the frequency band from 6 to 15 GHz and scanning of at least 60 degrees for all azimuth planes.

In this work, strategies are proposed to enhance the bandwidth performance of the connected slot array with ADLs. To enlarge the frequency band without increasing significantly the number of metal layers, ADLs where each individual layer can differ from the others in terms of geometrical parameters are employed. By dropping the assumption of identical layers, the analytical formulas in [18], [19] are no longer applicable. Thus, more general closed-form expressions are given here, for flexible designs of artificial dielectric slabs that are not uniform along the stratification. Based on the described analysis method, an example of a design with 5:1 bandwidth is presented.

II. ANALYSIS METHOD

The array unit cell, shown in Fig. 1, includes a connected slot element in the presence of a backing reflector. Above the slot, a number of artificial dielectric layers are placed, which consist of a periodic arrangement of sub-wavelength patches embedded in a host medium. To analyze the unit cell, analytical spectral solutions of connected arrays [20] and ADLs [18], [19] can be combined in a single tool that can provide

the active input impedance with minimal computational effort and can be used for optimization during the design phase.

A. Active Input Impedance

The active input impedance of the connected array of slots can be expressed as a Floquet expansion as follows [20]:

$$z_{\text{act}} = -\frac{1}{d_x} \sum_{m_x=-\infty}^{\infty} \frac{\text{sinc}^2(k_{xm} \frac{\delta}{2})}{D(k_{xm})} \quad (1)$$

where m_x are the indexes of the Floquet waves, characterized by the wave numbers $k_{xm} = k_{x0} - 2\pi m_x/d_x$. Here, $k_{x0} = k_0 \sin\theta \cos\phi$, where k_0 is the propagation constant in the free space and θ, ϕ are the angles towards which the array is pointing. The function $D(k_x)$ represents the transverse connected array Green's function [20] and accounts for the periodicity along the y -axis and for the stratification along z . It is expressed as a summation of Floquet modes with wave numbers $k_{ym} = k_{y0} - 2\pi m_y/d_y$ and $k_{y0} = k_0 \sin\theta \sin\phi$:

$$D(k_x) = \frac{1}{d_y} \sum_{m_y=-\infty}^{\infty} G_{xx}(k_x, k_{ym}) J_0\left(k_{ym} \frac{w_s}{2}\right). \quad (2)$$

where J_0 is the zeroth order Bessel function and G_{xx} is the xx -component of the magnetic spectral dyadic Green's function from a magnetic source. This Green's function accounts for the stratification along the z -axis and it can be defined in terms of the current solutions of equivalent transmission lines that represent the layered media above and below the plane of the slots:

$$G_{xx}(k_x, k_y) = G_{xx,\text{up}}(k_x, k_y) + G_{xx,\text{down}}(k_x, k_y) = -\frac{I_{\text{up,TE}} k_x^2 + I_{\text{up,TM}} k_y^2}{k_\rho^2} - \frac{I_{\text{down,TE}} k_x^2 + I_{\text{down,TM}} k_y^2}{k_\rho^2} \quad (3)$$

where $k_\rho^2 = k_x^2 + k_y^2$. The currents at the plane $z = 0$ are given by

$$I_{\text{up},Ti} = \frac{1}{Z_{\text{up},Ti}}; \quad I_{\text{down},Ti} = \frac{1}{Z_{\text{down},Ti}} \quad (4)$$

where Ti can refer to either the transverse electric (TE) or the transverse magnetic (TM) mode. The impedances representing the upper and lower stratifications are calculated using the equivalent circuit models in Fig. 2. In these models, the transmission lines for the TE and the TM incidence have characteristic impedances $Z_{0\text{TE}} = \zeta k/k_z$ and $Z_{0\text{TM}} = \zeta k_z/k$, respectively, with ζ and k being the impedance and the wavenumber of the pertaining dielectric slab and with $k_z = (k^2 - k_{x0}^2 - k_{y0}^2)^{1/2}$. Each layer of the ADL is represented as an equivalent susceptance (B_n). A transformer with turn ratio $1 - k_{\rho m}^2/(2k_{\text{layer}}^2)$ is included in the TE equivalent circuit [18], [19], where $k_{\rho m}^2 = k_{xm}^2 + k_{ym}^2$ and k_{layer} represents the propagation constant of the medium in which the layer (array of patches) is embedded or it is an average propagation constant if the layer is located at the interface between two different media.

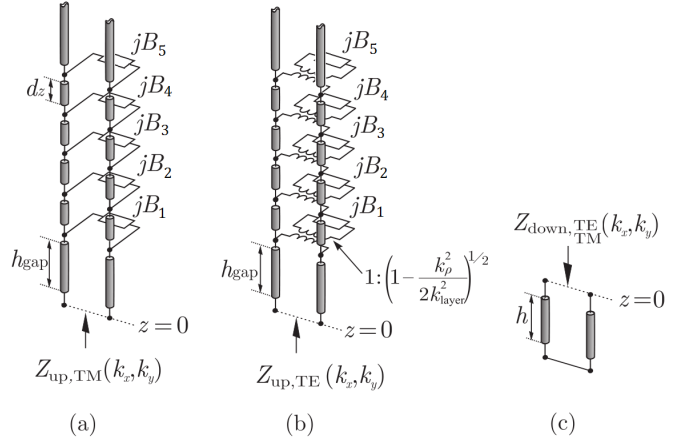


Fig. 2. Equivalent transmission-line model of a five-layer ADL for a generic (a) TM and (b) TE plane wave; (c) equivalent shorted line representing the backing reflector.

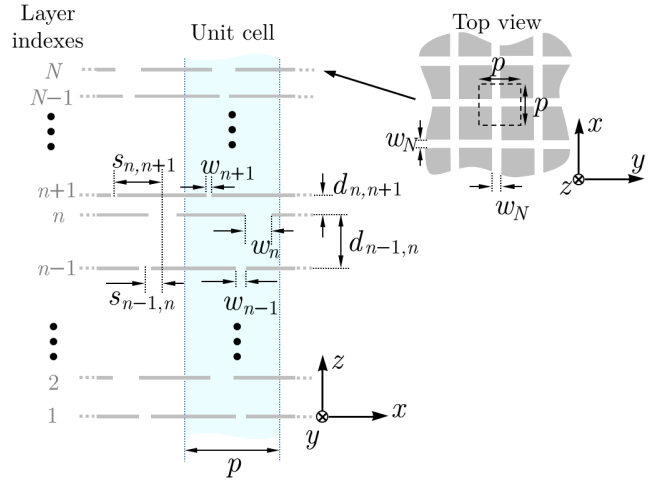


Fig. 3. Cross section view of the unit cell of z -aperiodic ADLs, with definition of the geometrical parameters.

B. Equivalent Susceptance of Artificial Dielectric Layers

The analytical expressions of the susceptance of artificial dielectric layers were derived in [18], [19], for layers that are periodic along the stratification, aligned or shifted. Here more general formulas are provided, for ADLs in which each metal layer can have different geometrical parameters. The geometry under consideration is shown in Fig. 3 and consists of N layers with indexes $n \in [1, 2, \dots, N]$. Each layer is an array of perfectly conducting square patches, infinitely thin along z and doubly periodic in the transverse dimensions. The periods are equal along x and y and given by p . Although the transverse periods are assumed to be the same for all the layers, all other geometrical parameters can vary in each layer and they are function of the index n . The gaps between the patches in the n -th layer are characterized by width w_n both along x and y . The distance between any pair of contiguous layers, with indexes n and $n + 1$, is denoted by $d_{n,n+1}$ and

can change arbitrarily along the stratification. Also the mutual shift between adjacent layers $s_{n,n+1}$ can vary with n and can be an arbitrary portion of the unit cell.

For $n \in [2, 3, \dots, N-1]$, the layer susceptance can be written as a Floquet expansion with indexes m :

$$B_n = \frac{jp}{\zeta_0 \lambda_0} \sum_{m \neq 0} \{S_m(w_n)[f_m(d_{n,n+1}) + f_m(d_{n-1,n})] + S_m(w_{n+1})g_m(s_{n,n+1}, d_{n,n+1}) + S_m(w_{n-1})g_m(s_{n-1,n}, d_{n-1,n})\} \quad (5)$$

where

$$S_m(w) = \frac{\left| \text{sinc} \left(\frac{\pi m w}{p} \right) \right|^2}{|m|} \quad (6)$$

$$f_m(d) = -\cot \left(\frac{-2j\pi|m|d}{p} \right) \quad (7)$$

$$g_m(s, d) = e^{j2\pi m s/p} \csc \left(\frac{-2j\pi|m|d}{p} \right). \quad (8)$$

In the function definition, the dependence on the period p is omitted, since it is assumed to be fixed and equal for all the layers. For the first and last layers ($n = 1$ and $n = N$) the susceptance changes as

$$B_1 = \frac{jp}{\zeta_0 \lambda_0} \sum_{m \neq 0} \{S_m(w_1)[-j + f_m(d_{1,2})] + S_m(w_2)g_m(s_{1,2}, d_{1,2})\} \quad (9)$$

$$B_N = \frac{jp}{\zeta_0 \lambda_0} \sum_{m \neq 0} \{S_m(w_N)[-j + f_m(d_{N-1,N})] + S_m(w_{N-1})g_m(s_{N-1,N}, d_{N-1,N})\}. \quad (10)$$

By implementing the equations (1) to (10) in a Matlab code, an analytical tool is obtained to estimate the matching performance of the array unit cell.

III. DESIGN STRATEGY

As an example, a design of an array unit cell with 5:1 bandwidth is described in this section.

A. Artificial Dielectric Design

The first step of the ADL design is to define a tapered transmission line transformer from 377 to 80 Ohm, with a continuous impedance variation (Fig. 4(a)). A line with exponentially tapered characteristic impedance is considered. The length of the transmission line determines the lower bound of the frequency band and must be selected to be around 0.5λ at the lowest frequency. The transformer is then discretized in a number of small transmission line sections, each with constant characteristic impedance, as shown in Fig. 4(b). The discrete transformer exhibits an upper bound to the frequency range, which corresponds to the frequency at which each section becomes 0.5λ . This bound determines the minimum number of sections that is needed. The transmission

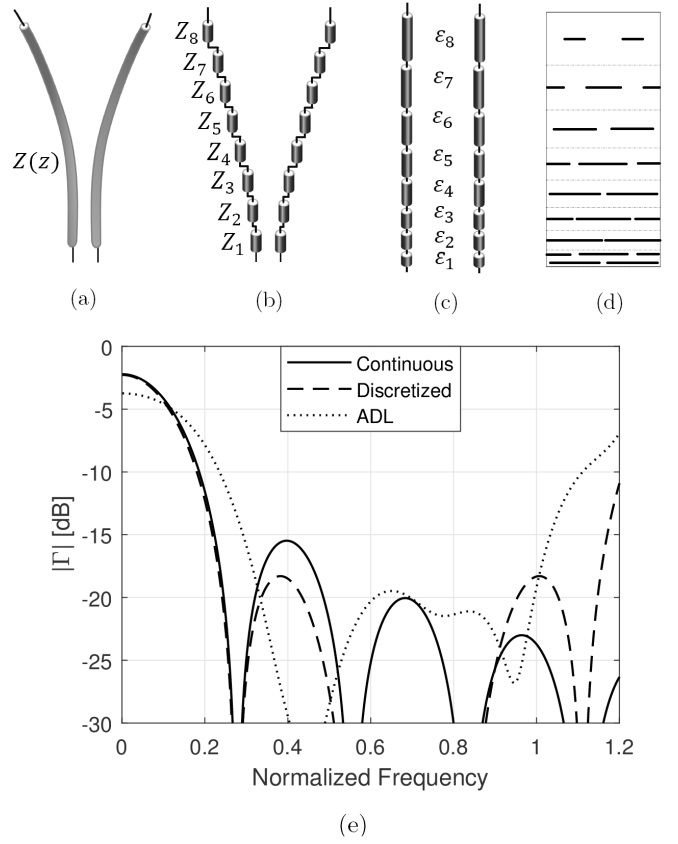


Fig. 4. Steps of the ADL design: (a) ideal tapered transmission line transformer; (b) stepped transmission line; (c) equivalent multilayer slab; (d) artificial dielectric

line sections are then replaced with lines with varying relative permittivities to obtain the required characteristic impedances (Fig. 4(c)). The length of the lines scales accordingly so that their electrical length is constant. Finally, the sections are imagined to describe the propagation of a plane wave through an artificial dielectric structure. Each relative permittivity is converted into a capacitive layer by a synthesis procedure obtained using the closed-form expressions in eqs. (5)-(10). The resulting artificial dielectric structure includes 9 layers and is shown in Fig. 4(d).

The reflection coefficient of the tapered and the discretized transmission lines is shown in Fig. 4(e). Also the reflection coefficient of a plane wave impinging on the synthesized artificial dielectric layers is shown. To limit the number of layers, some of the dielectric slabs only contain one artificial dielectric layer, providing a frequency dispersive equivalent permittivity. For this reason the bandwidth of the final ADLs is slightly reduced, but still covering the target 5:1 bandwidth.

B. Infinite Array Simulation of Matching Performance

The designed ADL slab is then simulated in combination with the connected slot element and the backing reflector using the equations (1)-(4). The geometrical parameters of the slot are summarized in Table I. The resulting active voltage

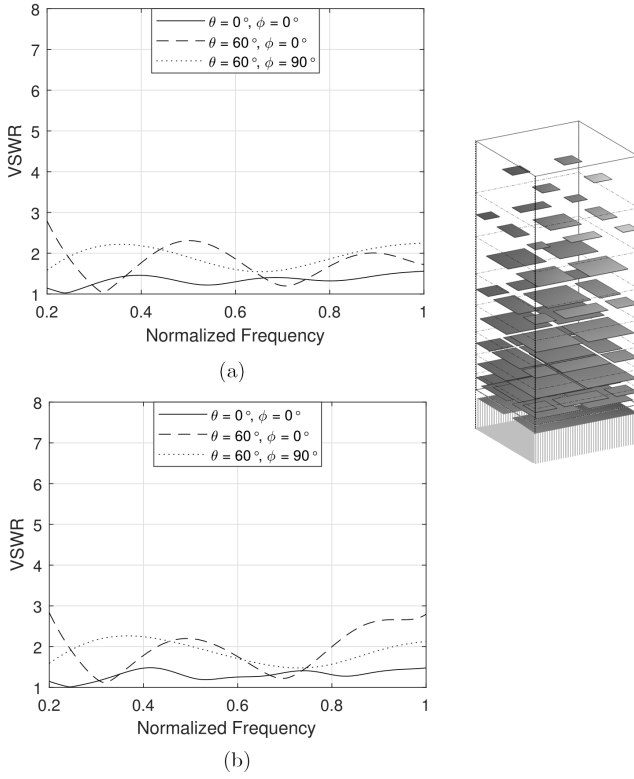


Fig. 5. Active voltage standing wave ratio for broadside, and scanning to 60 degrees on the E -plane and the H -plane: (a) calculated with the described analysis method and (b) simulated with CST.

TABLE I
DIMENSIONS OF THE SLOT ELEMENT; λ_0 IS THE FREE-SPACE WAVELENGTH AT THE MAXIMUM FREQUENCY OF INVESTIGATION f_0

$d_x = d_y$	w_{slot}	δ	h	h_{gap}	p
$0.43\lambda_0$	$0.1\lambda_0$	$0.25\lambda_0$	$0.2\lambda_0$	$0.03\lambda_0$	$d_x/2$

standing wave ratio (VSWR) is shown in Fig. 5, calculated with both the proposed analytical method and simulated with CST, for validation. The impedance at the feeding port is equal to 80 Ohm. The VSWR is lower than 3 for scanning up to 60 degrees in the main planes, over a 5:1 bandwidth. The overall height is 0.24λ at the lowest frequency of operation.

C. Feed structure

The results in Fig. 5 have been calculated by considering a delta-gap feed in the slot and by adding an ideal series capacitance $Z_c = (j\omega C)^{-1}$ to the active input impedance of the unit cell. The capacitor allows to improve the matching performance at lower frequencies by counteracting the inductance of the ground plane, similarly to the inter-element capacitance in tightly coupled dipole arrays [8]. A possible practical implementation of the feed is depicted in Fig. 6: a microstrip line is employed to feed the slot and it is terminated with a capacitive plate, acting as the series capacitance. The other end of the microstrip is connected to an integrated

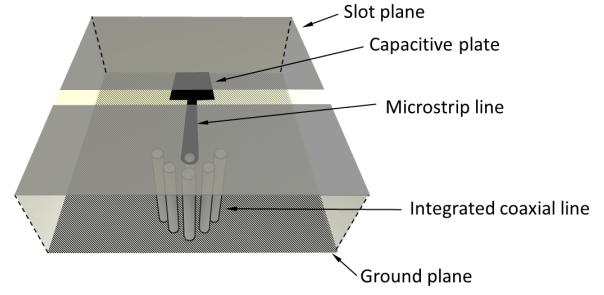


Fig. 6. Sketch of a typical implementation of the feeding structure for a connected slot unit cell.

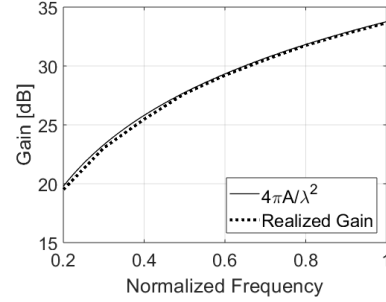


Fig. 7. Broadside realized gain versus frequency of an array with 32×32 elements, based on the infinite array simulation of the unit cell in Fig. 5. The maximum theoretical directivity is also shown for comparison.

coaxial line that reaches the ground plane where the connector can be located.

D. Infinite Array Simulation of Realized Gain

The broadside realized gain, based on infinite array simulations of the unit cell, is plotted as a function of the frequency in Fig. 7. A windowing techniques is used to estimate the patterns of a finite array with 32×32 elements. In the same figure, the maximum directivity from the array aperture is also shown, to quantify the efficiency. The scan performance is evaluated in Fig. 8, which shows the realized gain patterns for broadside and scanning to 30 and 60 degrees in the H - and E -planes. It can be observed that the scan loss remains less than 1.1 dB below the ideal $\cos \theta$ profile, also reported in the figure.

IV. CONCLUSIONS

Connected arrays of slots loaded with artificial dielectric have a number of advantages to realized wideband wide-scanning array apertures. Their are low-profile, simple to manufacture with a single multi-layer PCB and can be designed with analytical formulas. The procedure to simulate the active input impedance of the unit cell was summarized, taking into account artificial dielectric layers that can be non-periodic along the vertical direction. This assumption allows the design of tapered impedance transformers to realize wideband matching slabs, with a reduced number of metal layers. An example of design covering 5:1 bandwidth and scanning up to 60 degrees was presented and validated with CST simulations.

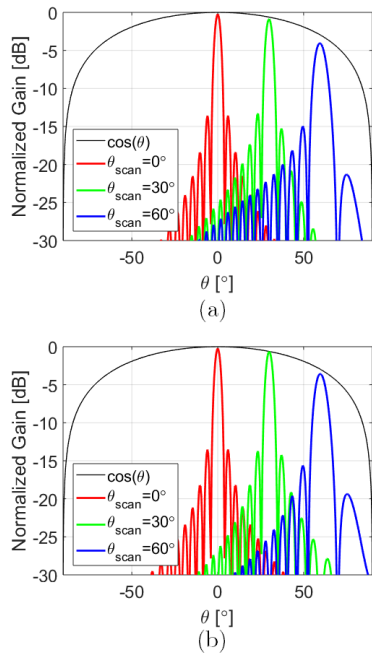


Fig. 8. Realized gain patterns for an array with 32×32 elements, for scanning in the (a) H - and (b) E -plane, based on the infinite array simulation of the unit cell in Fig. 5. The theoretical $\cos \theta$ dependence of the projected aperture is also shown for comparison.

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