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DOI
10.1109/OJIES.2024.3417939

Publication date
2024

Document Version
Final published version

Published in
IEEE Open Journal of the Industrial Electronics Society

IEEE Open Journal of the
Industrial Electronics Society

Received 22 May 2024; accepted 17 June 2024. Date of publication 24 June 2024;
date of current version 3 July 2024. The review of this paper was arranged by Associate Editor H. Abu-Rub.

Digital Object Identifier 10.1109/OJIES.2024.3417939

Pole-to-Pole Short-Circuit Categorization for Protection Strategies in Primary Shipboard DC Systems

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This work was supported by the Netherlands Enterprise Agency through the MENENS project under Grant MOB21012.

ABSTRACT The protection of dc systems in mobility applications, such as land transport, aircraft, and shipping, presents significant challenges due to the need for high-power-density equipment in confined spaces. This article focuses on dc systems onboard ships, for which diverse applications require different power levels, architectures, and protection strategies. Existing protection frameworks and regulations are often inadequate or outdated for the field, leading to certification issues and insufficient fault analysis. This research proposes a use-case-based categorization of short-circuit currents for primary systems. A reference scenario is created using a simulation model of a 5-MW system in a superyacht to provide a short-circuit inventory. The study proposes three contributions: a comprehensive fault inventory, a qualitative categorization, and relevant recommendations for power converter design. The research highlights the importance of fault categorization in understanding the impact of various short circuits on shipboard dc systems. The study emphasizes the importance of the evolution of materials and power converters in developing efficient protection technologies for ships. This work addresses some fundamental gaps in shipboard dc systems, providing a foundation for improved protection strategies and regulations, ultimately contributing to the advancement of protection of shipboard dc systems.

INDEX TERMS DC power systems, dc protections, shipboard dc systems, short-circuit analysis.

NOMENCLATURE

BTS	Bus-tie switch.
C_{out}	Output capacitor.
R_{th}	Thevenin resistor.
L_p	Parasitic inductance.
ESR	Equivalent series resistance.
V_g	Generator voltage.
DP	Dynamic positioning.
ECO	Economic cruising.
CRU	Full-speed cruising.
R_{SC}	Short-circuit resistor.

I. INTRODUCTION

The protection of dc systems has proven to be a challenging enterprise when considering mobility applications. Several sectors, such as land transportation, aircraft electrification, and shipping, require a relatively large amount of power in a compact volume [1], [2], [3]. For example, a Scania heavy-duty full-electric truck has a traction power ranging from 270 to 450 kW. Meanwhile, inland cargo ships, which have electric propulsion, require 2–5 MW [3], [4]. These electric systems may feature a dc microgrid, which inherently have a relatively low impedance characteristic between

power sources and loads. The multiple power converters utilized in transportation systems are integrated through different components, such as passive filters and protection devices for safety and electromagnetic compatibility compliance, and several meters of cable for the actual interconnection.

Energy storage systems, such as batteries, supercapacitors, and filtering capacitors, could amplify the effect of a potential malfunction that could lead to a catastrophic failure, e.g., fault conditions such as short circuits. Unfortunately, state-of-the-art dc ships lack effective fault analysis and protection technologies that accelerate their implementation. This has been reported in the literature as a hurdle in other fields that demand a high power density in a low-voltage class and medium-voltage dc systems [5], [6].

The installation of protection solutions in shipboard power systems is limited by application-specific constraints. Several parameters, such as power level, architecture, reliability, redundancy, and cost effectiveness, are assessed differently. Hence, the adoption of shipboard dc technology is not uniform across applications, affecting the relevance of different protection technologies.

Furthermore, existing protection frameworks for residential buildings, such as [7], and regulations, namely NPR-9090 [8], are not entirely suitable for shipboard dc systems. Current dc systems require a goal-based approval from classification societies (e.g., DNV-GL) [9], and arising challenges suggest that they should switch to rule-based regulations. Paradoxically, provisions intended for quality assurance on dc ships, such as IEEE 1709 [10] and IEEE 45 [11], need to be revised to consider new and advanced technologies concerning protection. Furthermore, a comprehensive categorization of faults in general onboard primary dc systems is missing.

This article presents a use-case-driven categorization of short-circuit currents (or fault currents) in primary shipboard dc systems, potentially valuable in multiple ship types. Such a categorization can simplify the assessment of faults onboard, which could become time critical for dc ships. A simulation model of the primary dc system for a 5-MW superyacht similar to that shown in Fig. 1 allows the analysis and characterization of different fault currents. The system features a distributed architecture with converters close to loads and generators and dc distribution lines. A representative categorization is possible by considering several test cases in various fault locations, initial conditions, and protection schemes. Therefore, the selectivity scheme aligns with the three-zone time-coordinated scheme in [12]. Ultimately, the overall fault current analysis feeds the categorization proposed in this article.

This work has four main takeouts that could enhance the design of safe and fault-tolerant dc systems onboard: 1) a fault inventory that allows for a better understanding of the behavior of pole-to-pole fault currents, which can become a worst case scenario onboard (especially relevant for industry focusing on similar use cases); 2) the categorization based on the fault inventory and its potential consequences can facilitate risk assessment in the early stages of ship design; 3) it could be possible to enhance the significance of dc ship regulations by generalizing the categorization; and 4) fault analysis and categorization could also boost the design of power converters by increasing awareness of possible threats and their quantification.

FIGURE 1. Referential case study for shipboard dc systems. Moonrise superyacht manufactured by Feadship in 2022. Credit to Feadship.

This research covers pole-to-pole (type-A) short circuits in shipboard dc systems, as these events potentially have the most destructive consequences [13]. Since generic dc systems are dependent on power electronics, severe overcurrent can become catastrophic for their power switches [13], [14]. Other types of faults, such as open circuit, pole-to-ground (type-B), and pole-to-pole-to-ground (type-C) short circuits, are beyond the scope of this document. The terms type-A fault, event, short-circuit current, and pole-to-pole short circuit are used interchangeably throughout the text. Open-circuit faults generally occur in generator feeders and have a limited overcurrent due to power drives [13]. Type-B and type-C faults depend on the grounding of the system [15], [16], which makes it difficult to conduct a representative study. However, the literature suggests that type-B faults are less problematic than type-A, as primary shipboard dc systems frequently feature a floating ground [17]. Depending on the grounding scheme, type-C events can become similar to type-A, which highlights the relevance of the latter.

Energy storage devices (e.g., batteries) in large vessels are typically connected to dc bus bars through a dc–dc converter. Therefore, filter capacitors govern the fault current in pole-to-pole short circuits. The low impedance of dc systems and the capacitor energy facilitate a high-current build-up with minimum time constants [5], [18]. The fault current from ac sources and freewheeling diodes could represent a relatively lower threat to the system. The diodes have conducting resistance that could dampen the fault despite their potential permanent damage [17]. Furthermore, the fault current coming from batteries is beyond the scope of this article because, since they require dc–dc converters operating in the current control mode to impose the charging profiles, a

current limiting feature would be naturally imposed that restricts the influence of the battery energy capacity to a bus fault. Furthermore, faults between the battery and the dc–dc converter are typically resolved within a few microseconds resulting in only a small dynamic influence of the dc bus of the ship. The fault current from capacitors, batteries, and ac sources and their current characteristics are further discussed in [15].

The analysis and waveform estimation of the fault current in shipboard dc systems is challenging. Standard recommendations, such as [19], describe the current from different sources, proposing independent solutions for the calculations of rise and decay. However, they cannot accurately predict fault currents for several feeders in parallel and are focused only on ac systems. The voltage drops in a converter-controlled low-voltage dc grid with fuse protection are investigated in [20]. The work shows several tests with various fuses and assesses the protection performance in a bipolar system, which is uncommon in shipping. The study also covers two-location fault testing using *RL* transmission lines. However, the purpose of their research diverges from maritime applications, especially in relation to primary distribution. Consequently, the potential energy of the capacitors and the characteristics of the power (300 W) and voltage (380 V) do not allow an appropriate comparison.

The lack of a cost-effective solution for dc protection in maritime applications hinders their adoption in general. Mechanical dc circuit breakers have slow response times and minimal losses. Solid-state counterparts exhibit acceptable response times but high losses, whereas hybrid circuit breakers do not have significant differences from the other cases [15], [18], [21]. Therefore, solid-state circuit breakers in shipboard dc systems serve regularly as BTSs, especially for highly demanding applications, such as offshore supply vessels and cable layers. Until now, fuses have still been preferred for the protection and galvanic isolation of faulty feeders on dc ships, despite their limitations in response time and extensive replacement period [9].

State-of-the-art protection technologies are not sufficiently developed to satisfy the high demands of the shipping industry. Consequently, the evolution of materials and power converters should lead to improved and efficient protection technologies. This article aims to provide insight into the characteristics of different short-circuit currents, giving an integrated perspective on design, regulation, and diagnosis. Therefore, the numerical model incorporates fuse-based protection strategies to assess their performance. For this purpose, a simple method that facilitates the process and its repeatability is necessary. This research employs a six-step approach, susceptible to iteration in all steps as follows.

1) *System information collection:* Baseline definition of the primary shipboard dc system under study is provided. The main parameters come as input from an existing vessel, so a relatively realistic scenario is taken into account. However, significant modifications are necessary to adapt the specifications to the numerical model.
2) *System modeling:* A model in alignment with the purpose of the simulation considering distribution architecture, cabling, loads, and protection components is developed. The sampling period, the discretization method, the solver, the simulation time, the initial conditions, and the type of model per component are defined.
3) *Test case definition:* The definition of scenarios implies decisions about the operation modes that affect the initial conditions and loads. The location of the short circuits and the protection mechanisms complement the decision-making process.
4) *Simulation and results analysis:* Simulations and individual confirmation of success for all relevant scenarios are executed. Characterization and analysis of key parameters, such as peak current, specific energy, and absorbed energy, for relevant test cases are performed.
5) *Performance analysis:* The performance of state-of-the-art protection approaches based on peak current, average current-rate variation, absorbed energy, and peak power estimation for critical test cases is compared.
6) *Fault categorization:* Fault categorization is defined based on qualitative criteria. The fault severity indicates the category, which also considers detection speed, localization complexity, and potential consequences.

The rest of this article is organized as follows. Section II shows a detailed description of the simulation model. Section III summarizes the test cases in the study. Section IV presents the fault inventory, comparing three relevant protection strategies, fault characteristics, and a sensitivity analysis of the cabling inductance. Section V focuses on the protection performance benchmark studying critical test cases and potential consequences. Section VI includes the fault categorization. Finally, Section VII concludes this article and summarizes prospects for future research.

II. SYSTEM DESCRIPTION

This section aims to describe the different components of the model and detail the main assumptions and limitations. Fig. 2 illustrates the primary distribution system of a referential superyacht using a dc system. The system has a dual bus radial configuration integrated via a single BTS. There are six power supply feeders, four of which are generators, and two include energy storage. Furthermore, two load zones *(blue dots)* or load feeders integrate propulsion and hotel loads into the dc system. The green shade in Fig. 2 represents the switchboard and indicates that all components within are located close together. The remaining drives are located close to the generators and loads and at a certain distance from the switchboard in a distributed architecture, as discussed in [4] and [22]. Weight and volume reductions and flexible component positioning are possible with distributed architectures [5]. The feasibility of

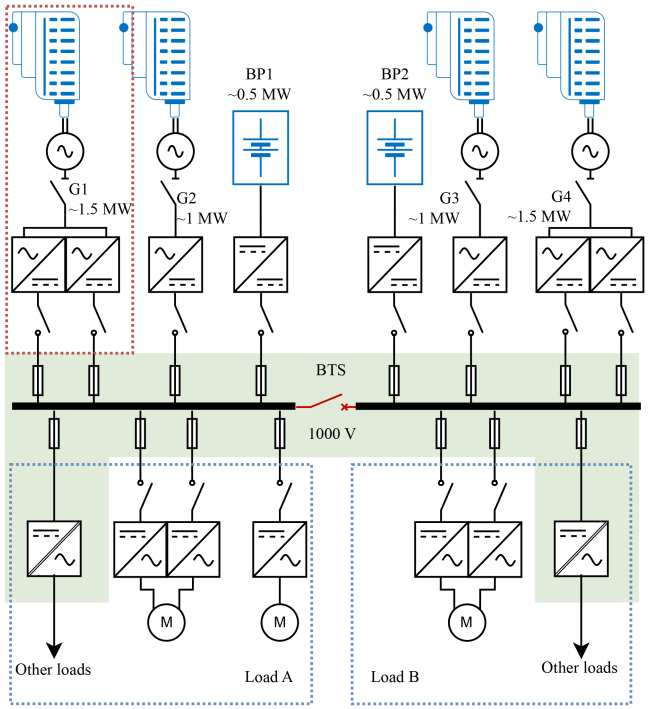

FIGURE 2. Referential case study for shipboard dc systems. Primary shipboard dc system, suitable for the superyacht. Red dots: components placed close together. Blue dots: load zones. Green shade: switchboard components placed close together.

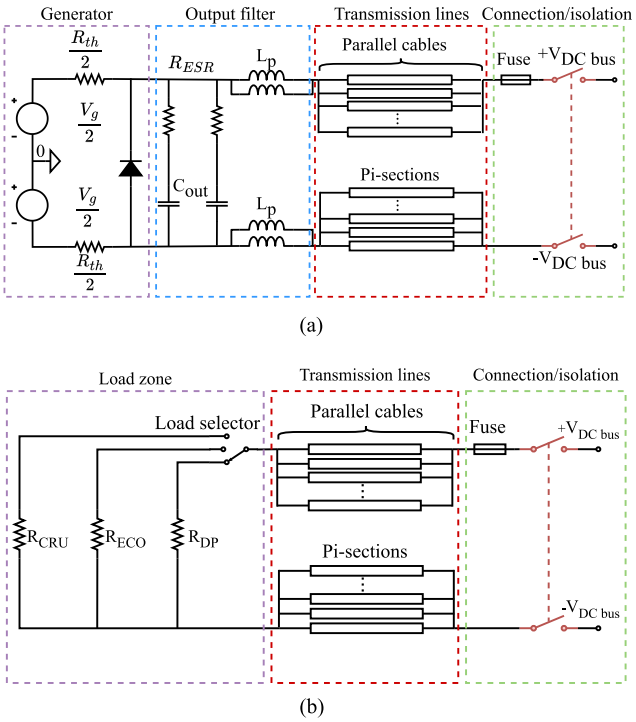

FIGURE 3. Schematic diagram of the modeled power supply feeders and load zones. (a) Feeder circuit for the main generator. (b) Equivalent circuit of a load zone. Purple dash: generator, load. Blue dash: output filter. Red dash: parallel transmission lines. Green dash: bus coupling point, disconnector, and fuse.

distributed dc ships onboard could be improved by analyzing their protection demands.

Transient and steady-state analyses are necessary for fault current characterization in a dc circuit. The following sections present the model segments intended for the simulation of the dc system as follows: 1) load and supply feeders; 2) fuses; 3) BTS; 4) short-circuit branch; and 5) summary of parameters.

A. LOAD AND SUPPLY FEEDERS

Since the dc system (see Fig. 2) has six supply feeders and two load zones, two general types of circuit are used in the modeling. The power supply feeder is shown in Fig. 3(a) and the load zone feeder is depicted in Fig. 3(b). The supply feeders in this work are of three types: 1) primary generators (G1 and G4); 2) secondary generators (G2 and G3); and 3) battery packs (BP1 and BP2). The main difference among the types is the number of output filters and the cable count, which also depends on the number of circuits.

For example, generators G1 and G4 utilize two converter drives as in Fig. 3(a), generators G2 and G3 require one converter drive, and battery packs BP1 and BP2 have three output filters for a single drive. Table 1 summarizes the cable count per component and the number of circuits.

The following components in Fig. 3 describe the circuits in the model: 1) sources; 2) output filters; 3) transmission lines; and 4) load.

TABLE 1. Cabling Arrangement per Main Component in the DC System Based on 1-kV Class DC Cables According to [9]

Component	Cables per line	Circuits
Generators G1and G4	8	2
Generators G2 and G3	9	1
Battery packs BP1 and BP2	9	1
Load zones A and B	9	2

1) SOURCES

The model of the power supplies consists of ideal dc sources and equivalent Thevenin resistors (R_{th}) to limit the output power of the source, accounting for the steady-state initial conditions of the fault. The voltage source V_g and the equivalent resistor are divided into two, creating the middle point grounding while keeping the rest of the circuit floating.

2) OUTPUT FILTERS

The original manufacturer of the drive provides data for the output filter capacitors (C_{out}), their ESR, and the parasitic inductances (L_p), which ultimately guide the transient characteristics of the circuit. Such parameters are assumed to be constant for the operation frequency and temperature for this work. The ESR absorbs part of the potential energy, limiting the amount of energy supplied to the fault. The energy absorbed by the ESR depends on the location of the fault within the dc system, and Section IV provides further discussion.

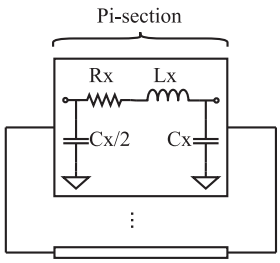

FIGURE 4. Schematic diagram of the pi transmission line segment employed in the model.

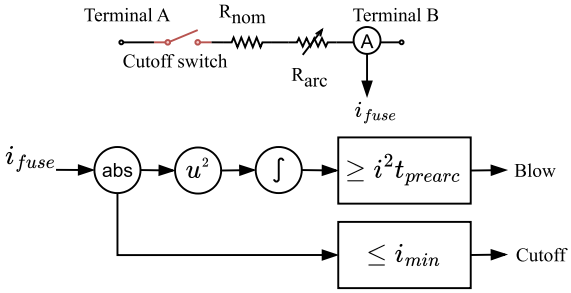

FIGURE 5. Schematic and control diagrams of the modeled fuse.

In addition, parasitic inductance affects the maximum current and the di/dt of the fault. However, the effect of these inductances is negligible compared with those of the transmission lines.

3) TRANSMISSION LINES

The transmission line model incorporates the effects of the cabling impedance in the system model. The pi model depicted in Fig. 4 corresponds to that of the simulation. Cable manufacturers provide parameters R_x, L_x, and C_x, which are mainly dependent on intrinsic characteristics and geometry [23]. For simulation, the parameters extracted come from marine-certified cable catalogs in the range of 1000 V [24].

4) LOAD

The load is modeled as a fixed resistor that represents an equivalent power consumption. The initial conditions are assumed constant since load variations in shipboard systems occur in hundreds of milliseconds, whereas short-circuit overcurrents happen within several microseconds. Furthermore, the power flow is considered unidirectional, and the load does not have an input filter. The effect of additional filter capacitors is discussed in different test cases in Section IV and discussed further in [17], where the input filter can increase the short-circuit current in a generator–motor feeder. The influence of load inductance is examined through a sensitivity analysis in Section IV. For this research, three operation modes define the values of the load resistors that ultimately impose the initial conditions.

1) *DP mode:* The DP mode requires the propulsion systems to maintain the vessel in a relatively static position ($\approx$ 17% of installed power).
2) *ECO mode:* It indicates a reduced speed or economic cruising that maintains optimal fuel consumption ($\approx$ 25% of installed power).
3) *CRU mode:* It refers to the maximum cruising speed for the propulsion system ($\approx$ 84% of installed power).

B. FUSE

Fuses are essential in shipboard dc systems to provide the first layer of protection and galvanic isolation [9], [10]. However, the literature rarely reports their behavior in dc cases, and there are no standard methodologies for their modeling. Ravyts et al. [20] study voltage dips in a fuse-protected bipolar dc system caused by short circuits. The study includes tests with various fuses in the system without focusing on the behavior of the fuse itself. The work in [25] shows an *RC* circuit and a variable resistor to model the arcing of a fuse for a dc power supply. The fuse model in [26] uses an algorithm to calculate the *RC* values while removing the variable resistor. However, the variety of feeders, transmission lines, and parasitic components complicate the tuning of the *RC* constant in a shipboard dc system. Furthermore, the large capacitors in the output filters dominate the dynamic response of the circuit, allowing the assumption that the fuse capacitors are negligible in the model. Consequently, the fuse model consists of a variable resistor (arcing resistor) in series with the nominal resistor and a cutoff switch, as depicted in Fig. 5.

The reference control structure of the fuse in Fig. 5 incorporates a *specific energy* threshold that represents the prearcing. *Specific energy* refers to i^2t and is hereinafter used as the specific energy of the current impulse in $\mathrm{J}\cdot\Omega^{-1}$. The fuse blows when the threshold is exceeded (in the datasheet), activating a linearly increasing variable resistor that simulates the arcing of the fuse. The fuse cutoff triggers when the minimum current $i_{\min}$ is reached. Despite the limitations of the fuse models, their behavior gives sufficient insight for complete system simulation.

C. BUS-TIE SWITCH

The BTS or bus coupler exists in various architectures and technologies and was extensively discussed in [6] and [18], providing several components that differ significantly in dynamic response, efficiency, and protection effectiveness. For the simplified model, the component response time is sufficient to provide insight into how low- and high-speed components could affect the fault. Fig. 6 includes the simple BTS utilized in the model and the simplified control strategy. The overcurrent threshold $i_{\max}$ and the duration of the transport delay define the switch time response that controls the ideal switches.

The time response of the BTS follows the typical time response of a mechanical switch with a series fuse, which is around 8 ms [27], and the maximum opening time in a certified solid-state BTS, which is close to 21 μs [28].

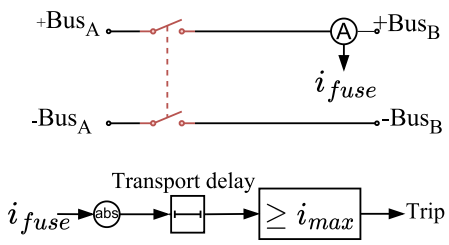

FIGURE 6. Schematic and control diagrams of the BTS.

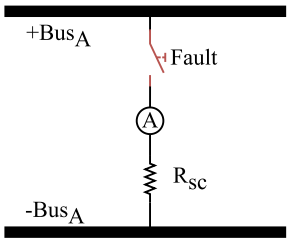

FIGURE 7. Schematic diagram of the pole-to-pole short-circuit branch utilized in the model.

TABLE 2. Summary of Parameters Utilized in the Simulation Model

Component	Value [Unit]
C_{out}	14.4 mF
ESR	5.5 mΩ
L_p	4 nH
V_{BUS}	1000 V
R_{nom}	0.229 mΩ
R_{SC}	100 μΩ
Load line	≈ 60 m
Source line	≈ 50 m

D. SHORT-CIRCUIT BRANCH

The generation of faults in the simulation environment requires a short-circuit (fault) resistor R_{SC}. The fault resistor is 100 $\mu\Omega$ to represent a solid short circuit. The magnitude differs in more than one order of magnitude from the ESR and load resistors and is about half of the nominal resistance of the fuse. The load resistors R_{DP}, R_{ECO}, and R_{CRU}, and the equivalent source resistors, are on the order of hundreds of milliohms, and the nominal resistance of the fuse is in the hundreds of microohms range. The diagram section in Fig. 7 shows how the branch is integrated into the model.

E. SUMMARY OF PARAMETERS

The simulation model tools, adjustments, and parameters can significantly affect the outcome. The parameters in Table 2 facilitate a reasonable analysis and replication, together with the following configurations.

1) The system integration utilizes Simulink, and the circuit models the PLECS blockset.
2) The Simulink and PLECS configurations use the fixed-step discrete solver at a sampling rate of 10 ns.
3) The discretization of the system is based on the fifth-order Runge–Kutta method, as the accuracy for high-speed events is considered better than the second-order Tustin method [29].
4) The sampling time of 10 ns satisfies the Nyquist criterion and accounts for most of the aliasing effects.
5) The sampling rate is more than 100 times faster than the increase time of a short-circuit current of ≈ 170 kHz for proper transient visualization.
6) Algebraic loops and divisions by zero are minimized to facilitate computation and improve accuracy.
7) The pi transmission line model accounts for the effect of *RLC* parameters in each cable and includes the effects of wave propagation.

III. TEST CASES

A selection of test cases with different variables is necessary to provide a comprehensive testing framework. The variables are operation mode (3), fault location (5), and protection approach (3) for 45 possible test cases. The operation modes DP, ECO, and CRU and the fuse model were introduced earlier in Section II. Fault locations and the associated protection approaches are introduced in the following sections.

A. LOCATION

The physical location of the fault can significantly affect the outcome of the event, given the relative complexity of the use case studied. The distributed approach with dc cabling modifies the impedance of the circuit compared to the centralized switchboard. For instance, in a pole-to-pole fault close to the output filter of generator G1, the adjacent output filter dominates the time response τ of the first current overshoot (1).

Moreover, the remaining current flowing into the fault comes from various places with different time responses. The characteristics of the output filters together with the impedance of the dc cables could justify such variations

$$\tau \approx \frac{L_p}{R_{ESR} + R_{SC}}. \tag{1}$$

Therefore, the variable location tests include five places, indicated with a red flash in Fig. 8. Generators G1 and G2 and battery pack BP1 have different cable counts per feeder and output filters, giving several options to study.

Bus A short circuits are particular cases that can simultaneously accumulate energy from all the filters at the fault point. These cases do not have adjacent filters and are affected by the impedance of the entire circuit. Furthermore, load zone A has an extra set of cables that can modify the characteristic impedance even further, affecting the fault current to a greater extent. The faults are located on Bus A, so it is assumed that the behavior of instances on Bus B will mirror the other cases.

B. PROTECTION APPROACH

The protection strategies are selected considering two objectives. First, analyze the natural response of the dc system

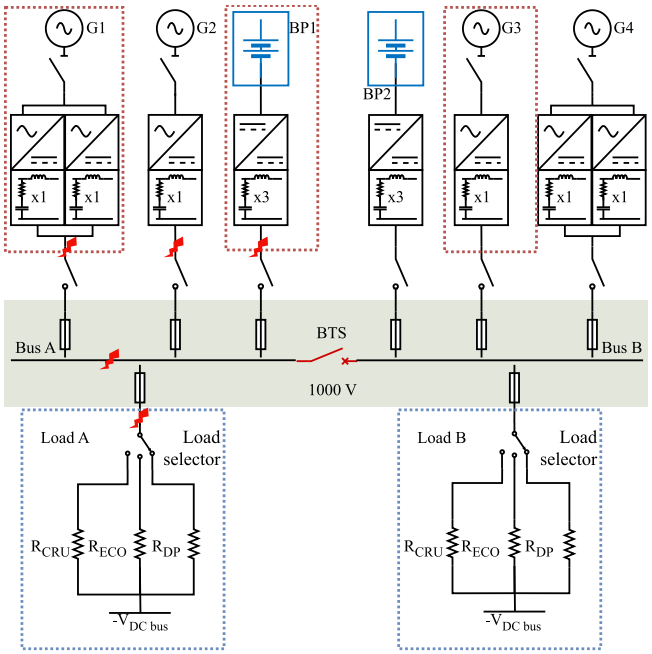

FIGURE 8. Simplified diagram of the system including the short-circuit locations. Red dots: components placed close together. Blue dots: load zones. Green shade: switchboard components placed close together.

in the event of a fault and provide insight into the worst case scenario, and second, benchmark two popular protection strategies based on fundamental protection components (fuses and BTS), as specified in [9] and [11]. The unrecoverable blackout is the worst case considered for the system. A blackout is considered unrecoverable if the downtime exceeds a predefined limit, which depends on the type of vessel, e.g., 60 s from blackout detection to thrust restoration in DP types.

The protection approaches are divided into three possibilities:

1) system without feeder protection and low-speed BTS (8 ms);
2) system with feeder fuses and low-speed BTS (8 ms);
3) system with feeder fuses and high-speed BTS (21 μs).

The framework of this research facilitates the creation of an inventory of short-circuit currents from the simulation, which is compared, in principle, with analytical methods.

IV. FAULT CURRENT CHARACTERIZATION

This section aims to present significant findings from the simulation model under different conditions. The benchmark of several test cases based on extracted and calculated parameters, such as peak current, dissipated energy, and specific energy, allows a comprehensive distinction among fault types and locations, which is the core of the categorization in Section VI.

The inventory follows a logical structure, in principle, providing a complete overview of the selected cases. In Section IV-A, the potential energy stored in the capacitors and the energy dissipated by the ESR are discussed. In Section IV-B, the analytical model based on circuit analysis and the potential limitations of the method are introduced. Sections IV-C–IV-E cover the results and calculations of the test case. Section IV-C shows the system without protection, Section IV-D shows the system with feeder fuses, and Section IV-E shows the upgrade to feeder fuses and a high-speed BTS. The section ends with a dc cabling sensitivity analysis, given that their length affects the fault current waveform. The cable length ranges from centralized to distributed primary systems in a single-feeder test.

TABLE 3. Potential Energy Stored in Capacitors Per Feeder

Generators G1 and G4 (kJ)	Generators G2 and G3 (kJ)	Battery packs BP1 and BP2 (kJ)	Total (kJ)
14.4	7.2	21.6	86.4

A. POTENTIAL ENERGY

Most of the transient-state energy in a dc short circuit gets transferred from the output filter capacity. Table 3 summarizes the potential energy of the capacitors for the superyacht case in Fig. 2, including the equivalent total energy.

The energy dissipated during the short circuit reflects a fraction of the potential stored in the filtering capacitors. The ESR dissipates the remaining energy, which varies depending on the location of the fault. Therefore, the architecture and parameters of the dc system affect the proportion in which they split apart. The reason is that the ESR is approximately one and a half orders of magnitude larger than R_{SC}, and the location affects the equivalent ESR influencing the fault. The energy dissipation ratio from R_{SC} to ESR in the superyacht based on the fault location is as follows.

1) *generators G1 and G4:* 27.5 times;
2) *generators G2 and G3:* 55 times;
3) *battery packs BP1 and BP2:* 18.3 times;
4) *buses A and B:* 4.58 times;
5) *loads A and B:* 4.58 times.

In short, the component storing the energy can dissipate most of it during the transient. The energy dissipation ratio facilitates the health estimation of the output filters by providing insight about the absorbed energy during the fault.

B. ANALYTICAL MODEL

Mathematical models are essential for simulation tools and can be used to analyze fault currents in shipboard dc systems to a certain extent. For example, the power grid in Fig. 2 has multiple sources connected to the two buses via dc power lines. For faults adjacent to any of the output filters, it is possible to estimate the behavior of the fault current by working with simple assumptions. Fig. 9 shows a simplified circuit of the feeder that connects generator G1. As the fault resistor is adjacent to the filter, the current through the transmission lines is initially neglected.

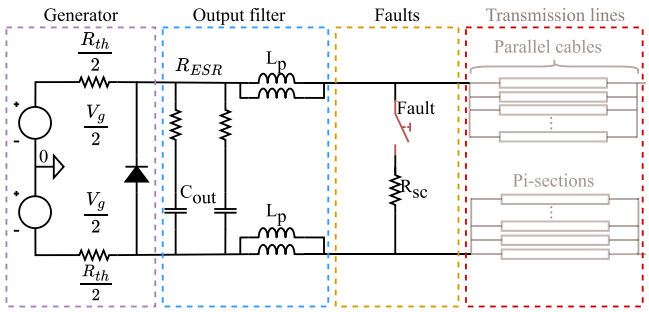

FIGURE 9. Schematic of the simplified generator G1 circuit for short-circuit current analysis. Purple dash: generator. Blue dash: output filter. Yellow dash: short-circuit resistor. Red dash: parallel transmission lines.

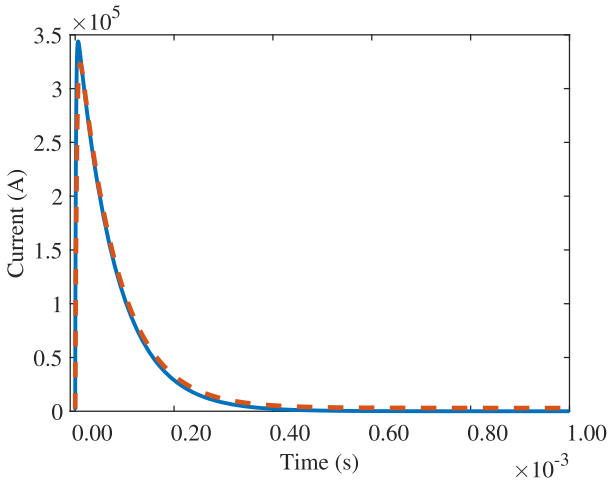

FIGURE 10. Comparison of fault currents during a pole-to-pole short circuit in a single-feeder system based on generator G1 and maximum nominal load. Blue: analytical model. Dash red: simulation model.

In the case of an event such as a type-A fault, the mathematical representation gives

$$2L_p\frac{di_{SC}}{dt} + i_{SC}R_{SC} = v_{cap} - C_{out}R_{ESR}\frac{dv_{cap}}{dt} \tag{2}$$

$$i_{SC} = C_{out}\frac{dv_{cap}}{dt} + \frac{V_g - V_{BUS}}{R_{TH}} \tag{3}$$

where i_{SC} is the fault current and v_{cap} is the capacitor voltage.

The current response can be overdamped or underdamped depending on the parameters, which gives two families of solutions in (4) and (5), respectively, for the differential equations system. More details on solution and analysis methods are available in [15], [17], [30], and [31]

$$i_{SC}(t) = \frac{e^{-\alpha t}}{2\beta}\left[\frac{V_{cap}}{L_p}\left(e^{\beta t} - e^{-\beta t}\right) + \beta I_g(0)\left(e^{\beta t} + e^{-\beta t}\right)\right] \tag{4}$$

$$i_{SC}(t) = e^{-\alpha t}\left[\frac{V_{cap}}{\omega_d L_p}\sin\omega_d t + I_g(0)\cos\omega_d t\right] \tag{5}$$

where $I_g(0)$ is the initial condition of the generator current, which is given by the operating mode, $\alpha = \frac{R_{ESR}}{2L_p}$, $\beta = \sqrt{\left(\frac{R_{ESR}}{2L_p}\right)^2 - \frac{1}{L_pC_{out}}}$, and $\omega_d = \sqrt{\frac{1}{L_pC_{out}} - \left(\frac{R_{ESR}}{2L_p}\right)^2}$.

The fault current from the circuit in Fig. 9 is overdamped, and Fig. 10 shows in blue the current response obtained by using the parameters from Table 2 in (5). The peak current is $\approx$ 343 kA with a peak time of $\approx$ 6 μs.

A simulation of the feeder in Fig. 9, attached to the load, is shown in dashed red in Fig. 10. This result suggests that it is possible to estimate the first current overshoot in a pole-to-pole short circuit, as long as the fault occurs close to a filter. The single feeder simulation reaches $\approx$ 323 kA in about 10 μs despite including parallel cables in the analysis.

However, the results of the analytical method are overly complex when studying the entire circuit. The augmented system introduces numerous state variables, and thus, numerical methods are preferred. The fault current computation results are less intensive and potentially more accurate. The information aids in mitigating possible threats, conceivably enhancing design procedures and streamlining the analysis.

C. NONPROTECTED SYSTEM

This section includes the main takeaways of the numerical model that utilizes a nonprotected approach under type-A faults. The related test cases show the natural response without feeder protection. The low-speed BTS is the only protection component in this configuration, and its influence is limited. It is worth mentioning that this case is not practical in reality, but it gives insight into the phenomenon. The section covers the following topics: 1) the fault current at different locations for a single operation mode is shown; 2) the fault current sources and their contribution to a single event are analyzed; 3) the voltage disturbances present during a short circuit are outlined; and 4) several short-circuit characteristics in different operation modes are discussed.

1) FAULT CURRENT AT VARIOUS LOCATIONS

The event location significantly affects its waveform because cabling modifies the impedance of each feeder. Fig. 11 shows the natural response of several faults in the system under study, which facilitates their comparison.

The output capacitors dominate the behavior of the phenomenon. An initial overshoot is visible when the fault occurs adjacent to generator G1 or G2 and battery pack BP1. The earliest response in these signals is rather aggressive, and they appear to overlap completely. The time scale of the figure allows for a comparison among the five fault locations and other figures, but creates an overlapping perception. However, their di/dt is different, shifting the current peak and the time to peak. The inset in Fig. 11 shows the fault in generator G2 reaching about 173 and 339 kA for generator G1 and 495 kA for the battery pack BP1. After the initial overshoot,

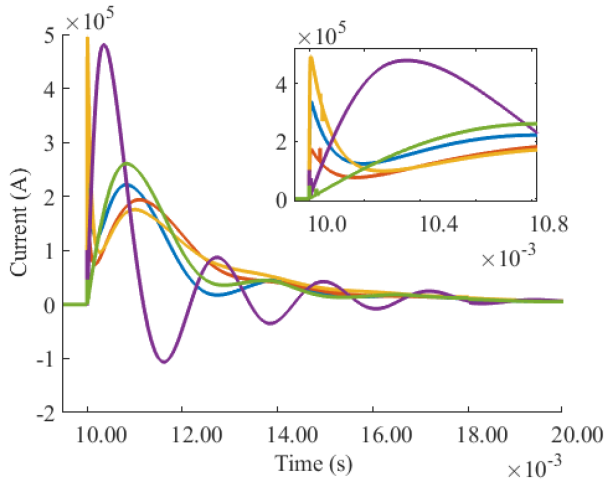

FIGURE 11. Pole-to-pole short-circuit current response at various locations with the dc system operating in the DP mode. Blue: generator G1. Red: generator G2. Yellow: battery pack BP1. Purple: bus A. Green: load zone A. Inset: Detail of the initial current overshoot after the short circuit.

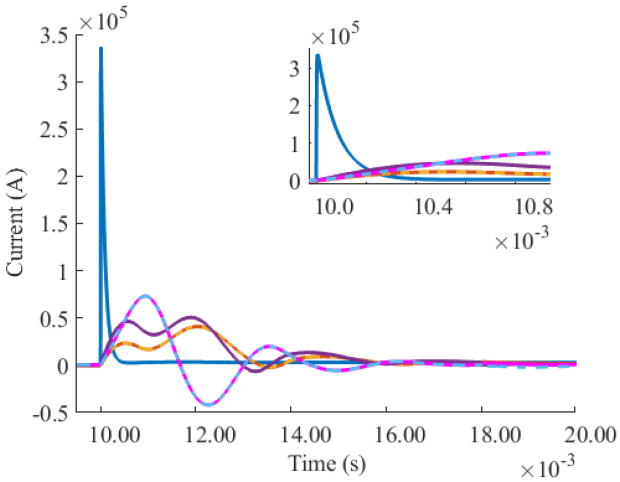

FIGURE 12. Fault current fed by different sources into a pole-to-pole short circuit at generator G1 in the dc system operating in the DP mode. Blue: generator G1. Red: generator G2. Dash yellow: generator G3. Purple: generator G4. Magenta: battery pack BP1. Dash light blue: battery pack BP2. Inset: Detail of the initial current variation after the short circuit.

the inductance and capacity of the complete system must be considered. The current exhibits subsequent amplitude decaying oscillations that supply the utmost energy to the fault. An overview of the waveform shows that the first overshoot has a limited area, implying that its energy is lower than that of the first subsequent peak despite the lower maximum. Faults at bus A or load zone A behave differently from the other cases. The initial overshoots are comparable to the subsequent overshoots obtained at the other points. In addition, the impedance of the feeders shifts the initial peaks, which also implies higher energy.

Furthermore, the resonance among the components in the dc system governs the oscillations in the fault currents. The current from the sources varies with different decay factors and frequencies, making the period irregular. The zero crossing visible in bus A (purple) is also a consequence of the oscillations and does not work in fault clearing.

2) FAULT CURRENT SOURCES

In practice, direct measurement of the short-circuit current is not feasible. However, at least partial waveform reconstruction is possible from measurements present in real applications. For instance, adding together the output current of the converters in the dc system can be derived in any of the fault current waveforms in Fig. 11. This section intends to analyze the contribution of the different sources in a particular fault and some of the implications.

The current measured in the output filters when the short circuit occurs by generator G1 is visible in Fig. 12. Most of the energy stored in the adjacent capacitors is dissipated by the ESR, and the remaining energy is transferred to the fault. Notice the initial di/dt among the signals compared to generator G1 (blue).

In Fig. 12, the average di/dt in generator G1 is approximately 51.3 kA $\cdot\mu$ s^{-1}, whereas the same variable at generator G4 is close to 81.4 A $\cdot\mu$ s^{-1}. The current rise at the sources away from the fault has a comparable behavior, and they overlap in the simulation. This result suggests that it would be possible to detect a type-A event when it occurs adjacent to an output filter.

The fault current oscillations are challenging to anticipate in real-time usage, and the lack of consistent behavior impedes their utilization in protections. Despite the existence of zero-crossing in some signals in Fig. 12, these events depend on the damping factor of the grid for the specific transient, and the operation of a circuit breaker should not rely on them. For example, zero crossing of battery packs (magenta and dash light blue) occurs approximately 2 ms after the short circuit. Meanwhile, the current in generator G4 (purple) oscillates without a zero crossing until after 3 ms. In contrast, the current of the adjacent filter does not have zero crossings, which aligns with well-known dc protection obstacles.

3) VOLTAGE DISTURBANCES

Significant voltage variations are logical consequences of a fault in a low-impedance dc system such as shipboard grids. This section discusses the sequence of events that depict voltage disturbances that arise from a pole-to-pole fault on generator G1.

1) Short circuit occurs.
2) The voltage in generator G1 drops to zero as the output capacitors are discharged.
3) The subsequent current oscillations force the voltage decay at the remaining locations.
4) The voltage in all nodes stabilizes at 0 V after a few milliseconds.
5) All the potential energy in the capacitors gets dissipated.

6) The BTS trips 8 ms after the fault, creating voltage oscillations.
7) The voltage restoration starts at the healthy side of the system.

The numerical model shows the voltage oscillations caused by the abrupt load change. Such variations can cause sympathetic tripping in a shipboard dc system, potentially compromising the correct protection selectivity. The amplitude, characteristics, and mitigation of voltage variations require a detailed study, which is beyond the scope of this article.

4) FAULT CURRENT CHARACTERISTICS

The characterization of the fault current requires the analysis of the peak amplitude together with the specific and dissipated energy. Including parameter and initial condition variations facilitates a more complete understanding of the phenomena. The study of test cases considers the following parameters: 1) peak current; 2) specific energy during the initial overcurrent and the complete fault; 3) absorbed energy also for the first overshoot and the rest of the event; 4) specific and absorbed energy from the filter adjacent to the fault point (when applicable); and 5) peak power.

The analysis is applicable to the entire set of tests. However, battery feeders feature the highest capacitance of the system, and only such cases are discussed. Type-A faults at bus A are studied in Sections IV-D and IV-E, investigating more realistic scenarios.

1) *Peak current:* The events placed adjacent to output filters (generators G1–G4 and battery packs BP1 and BP2) show consistent similarities. The total fault current exhibits a first high-frequency overshoot followed by a composite of subsequent oscillations. Therefore, the peak current analysis includes the first overshoot, supplied mainly by the adjacent filter, and the first succeeding peak. The cases without adjacent filters (bus bars and load zones) behave differently. The first overshoot shows a lower frequency, whereas the second peak is significantly lower than in the other instances (see Fig. 11).
2) *Specific energy:* The specific energy of the fault current allows the calculation of the absorbed energy for any component of the circuit path. The specific energy calculation uses (6), where t_1 coincides with the start of the fault in all cases. The end of the interval t_2 has two instances for calculation: 1) the initial discharge is accounted until the local minimum via the first derivative, which is the starting point for the subsequent discharges; and 2) it covers the fault current until it reaches the (approximate) steady state.

$$\frac{W}{R} = \int_{t_1}^{t_2} i^2(t)\,dt. \tag{6}$$

3) *Absorbed energy:* The absorbed energy considers the specific energy transferred to the short-circuit resistor. The calculation is carried out in the same intervals as in the previous case, according to

$$E = R_{\mathrm{SC}} \int_{t_1}^{t_2} i^2(t)\,dt. \tag{7}$$

4) *Energy from adjacent filters:* Replicating the analyses in items 2) and 3) for the output energy from the contiguous filter allows the evaluation of their contribution in the first overshoot.
5) *Peak power:* The instantaneous peak power allows the visualization of the power reached at the maximum fault current.

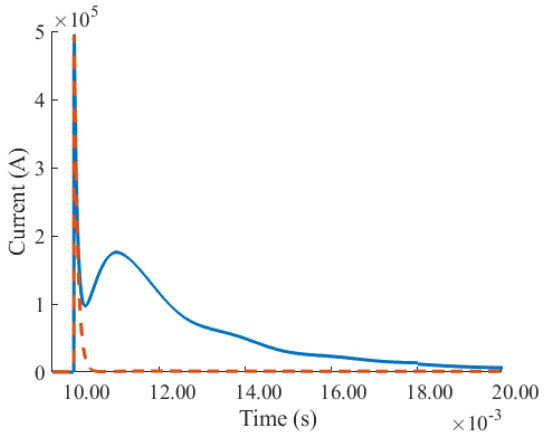

FIGURE 13. Current supplied by the filter adjacent to a pole-to-pole short circuit at the battery pack BP1 with the dc system operating in the DP mode. Blue: short-circuit current at battery pack BP1. Dash red: current supplied by the filter adjacent to the fault location.

Table 4 summarizes the analysis of pole-to-pole short circuits at battery pack BP1 in the dc system for the DP, ECO, and CRU operating modes. The main characteristics of the events are the following.

1) The subsequent current peak is about 35%, on average, of the initial overshoot.
2) The specific and absorbed energy of the initial discharge are close to 20% of the total.
3) The energy supplied by the adjacent filter during the initial peak is about 17% of the total and about 83% of that during the first overshoot (see Fig. 13).
4) The energy stored in the output filter is about 21.6 kJ (see Table 3), and from (7), the ESR dissipates approximately 20.78 kJ during the first overshoot.

In addition, initial conditions appear to have little influence on fault characteristics, and energy seems to decrease when the initial load is the highest (CRU mode). For instance, the peak current in the DP mode is approximately 1.3% larger than in the CRU mode, absorbing the maximum energy. Furthermore, the difference in specific and absorbed energy is close to 2.1% in favor of the DP case. Therefore, the initial conditions of type-A faults adjacent to an output filter have a negligible influence on the phenomenon.

The analysis in Table 4 provides insight into the natural response of pole-to-pole short circuits in shipboard dc systems. This information could facilitate the development

TABLE 4. Characteristics Analysis of Pole-to-Pole Fault Currents With Different Initial Conditions at the Battery Pack BP1

Operation mode	Peak current (kA)		Specific Energy ($kJ \cdot \Omega^{-1}$)		Energy (kJ)		Energy from adjacent filter		Peak power (MW)
	First	Subsequent	First	Total	First	Total	Specific ($kJ \cdot \Omega^{-1}$)	Energy (kJ)	
DP	495.56	175.79	13576	66405	1.36	6.64	11337	1.13	24.55
ECO	495.32	175.52	13554	66227	1.35	6.62	11325	1.13	24.53
CRU	493.58	173.53	13474	65023	1.35	6.5	11245	1.12	24.36

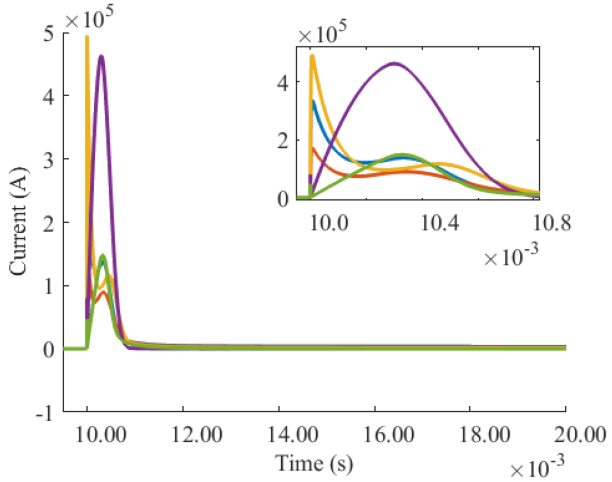

FIGURE 14. Pole-to-pole short-circuit current at various locations with fuse protection, and the dc system operating in the ECO mode. Blue: generator G1; Red: generator G2; Yellow: battery pack BP1; Purple: bus A; Green: load zone A. Inset: Detail of the initial current overshoot after the short circuit.

of future protection systems and the proper design of well-known technologies. However, the rest of the short-circuit inventory studies more realistic scenarios based on currently approved solutions.

D. FUSE PROTECTION

After the analysis of natural response, a system configuration closer to an actual implementation is studied. The protection system of certified dc ships is mainly based on fuses for selectivity and galvanic isolation [9], [26]. This section investigates several type-A faults in a shipboard dc system similar to Fig. 8, where each feeder has fuses, as described in Section II. The fuse selection is based on marine-certified fuses [32] and the nominal drive current plus minimum 10% as a security margin.

The procedure is equivalent to the nonprotected case, and, therefore, the section includes, in principle, the same subsections. Nevertheless, the behavior of bus bar and load zone faults is significantly different from the other cases, requiring a dedicated analysis. Hence, the section outline is the following: 1) fault current at different locations; 2) fault current sources; 3) voltage disturbances; 4) characteristics of short-circuit current; and 5) bus bar faults.

TABLE 5. Fuse Activation and Degradation Derived From the Faults at Various Locations With a Low-Speed BTS in Fig. 14

Location	Blown	Degraded
Generator G1	FG1	FG2 and FG3
Generator G2	FG2	FG3
Battery pack BP1	FB1	FG2 and FG3
Bus A	All	N/A
Load A	FLA	ALL

1) FAULT CURRENT AT VARIOUS LOCATIONS

Fig. 14 shows the simulations of pole-to-pole short circuits located in various sections of the dc system. From the nonprotected system case, it is clear that the location of the faults can affect their waveform, which is mainly due to the nonhomogeneous characteristics of the feeders in the dc system. Including fuses does not have a significant apparent influence on the initial waveform of the fault current. At least initially, the overcurrent peak varies only slightly in magnitude compared to Fig. 11, attributed to the nominal resistance of the fuse.

Faults adjacent to a filter exhibit a first overshoot followed by a subsequent overshoot, which decreases significantly as the effect of the arcing resistor grows. The remaining phenomenon shows only a slow magnitude decay until it reaches the nominal current of the source. The fuse cutoff does not completely clear the fault, since the short-circuit resistor is in parallel with the output filter, whereas the fuse is in series with the cable at the bus connection point.

The faults at bus bars and load zones exhibit a behavior comparable to that in the nonprotected case, and the effect of the fuse is visible only after the initial overcurrent. Eventually, the fuse cuts off, and the fault current drops to zero, clearing the fault from the power supplies in the system.

The output of the simulations suggests that it is possible to isolate a faulty generation feeder with the fuse and remain operating with the rest of the system. However, sympathetic tripping and accelerated fuses degradation are plausible consequences of a fault. Table 5 summarizes the blown and degraded fuses during short circuits in Fig. 14 according to the numerical model. The fuse is considered to be degraded when the current increase during the fault is significant, but not high enough to activate the prearcing for the duration of the simulation. On average, fuse prearcing starts about 1 ms after fault, which is consistent with catalog data [32]. The nomenclature identifies the fuse by its location in the system as follows:

1) *generator feeders (G1–G4):* FG1, FG2, FG3, and FG4;

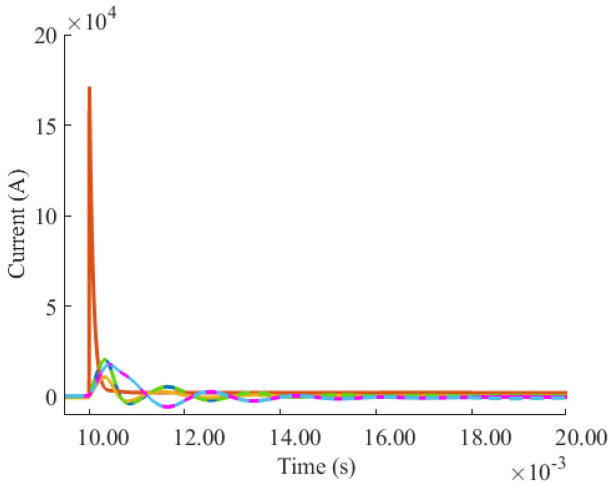

FIGURE 15. Fault current fed by different sources into a pole-to-pole short circuit at generator G2 with fuse protection, and the dc system operating in the ECO mode. Blue: generator G1. Red: generator G2. Yellow: generator G3. Dash green: generator G4. Magenta: battery pack BP1. Dash light blue: battery pack BP2.

2) *battery pack feeders BP1 and BP2:* FB1 and FB2;
3) *bus bars A and B:* FBusA and FBusB;
4) *load feeders A and B:* FLA and FLB.

2) FAULT CURRENT SOURCES

This section completes the fault analysis by focusing on the current from the supplies. The type-A short-circuit current in generator G2 shown (in red) in Fig. 14 is equivalent to the source currents in Fig. 15.

In general, the fuse attenuates the current oscillations after the initial overcurrent. The time response of the fuses may not be sufficient to avoid the discharge of adjacent capacitors. Thus, the initial overshoot lacks attenuation, and the total energy in the contiguous capacitor is transferred into the fault and the ESR.

3) VOLTAGE DISTURBANCES

Pole-to-pole faults located close to an output filter can create a severe voltage drop when using feeder fuses. This section describes the voltage fluctuations caused by the feeder fuses. The voltage disturbances in the presence of a pole-to-pole short circuit at generator G2 exhibit the following sequence of events.

1) Short circuit occurs.
2) The capacitor voltage in generator G2 drops to zero after about 0.96 μs.
3) Voltage at the bus bars initially decays as in the case without protection.
4) The feeder fuse blows, showing the protective effect after around 0.28 ms.
5) Voltage in the healthy nodes start to recover.
6) The BTS trips 8 ms after the fault, creating voltage oscillations.
7) The voltage restoration in the healthy side ends after a few milliseconds.

This result could become representative, assuming that the voltage drop protection, featured in most certified drives, triggers after the BTS (8 ms). This scenario is consistent with the recommended three-zone protection scheme for shipboard dc systems [12].

4) FAULT CURRENT CHARACTERISTICS

This section examines further the parameters of the pole-to-pole faults located close to an output filter in the referential shipboard dc system. Table 6 summarizes the parameters, already introduced in Section IV-C, at battery pack BP1 for different initial conditions.

The main takeouts from the analysis are the following.

1) The subsequent current peak is about 23.8% of the initial overshoot.
2) The specific and absorbed energy of the initial discharge are close to 76% of the total.
3) The energy supplied by the adjacent filter during the initial peak is about 64% of the total and around 84% of that during the first overshoot.
4) The energy stored in the output filter is approximately 21.6 kJ, and the ESR dissipates approximately 20.72 kJ.

In general, including the feeder fuses could prevent the largest share of potential energy from being transferred to the fault. Such a scenario is only applicable if the fault occurs close to an output filter in a similar use case. The phenomenon is attributed to the sharp increase in current, which is possible when the inductance between the fault and the output filter is low. Section IV-F covers the effect of the inductance in the waveform of the short circuit. As a complement, Section V summarizes the comparison of protection performance for the different test cases. The analysis benchmarks the nonprotected, fuse feeder protected, and fuse feeder protected with high-speed but-tie switch cases.

5) FAULT AT THE BUS BARS

Bus bar faults require dedicated analysis and classification, and this section studies type-A events at the bus bars with a worst case perspective. Despite having similar behavior to the bus fault, the load zone event has an additional set of dc cabling that increases the impedance. Therefore, the short-circuit current is damped and isolated by the fuses, while the overcurrent-driven thermal stress in the other feeders can be reduced, possibly allowing the generation feeders to continue operating.

Hence, the bus bar fault results are important for understanding the protection mechanisms for future shipboard dc systems. The purple signal in Fig. 14 is the total fault current in bus A. The peak value is the second largest among the test cases in the plot. However, the rise and fall times are comparable, which implies that the transferred energy becomes significantly higher than in other instances. In addition, the event occurs approximately in parallel with all the filters,

TABLE 6. Characteristics Analysis of Pole-to-Pole Fault Currents With Different Initial Conditions at the Battery Pack BP1, Considering Fuse Feeder Protection

Operation mode	Peak current (kA)		Specific Energy ($kJ \cdot \Omega^{-1}$)		Energy (kJ)		Energy from adjacent filter		Peak power (MW)
	First	Subsequent	First	Total	First	Total	Specific ($kJ \cdot \Omega^{-1}$)	Energy (kJ)	
DP	487.8	116.71	13423	17660	1.34	1.76	11342	1.13	23.8
ECO	491.56	116.62	13497	17728	1.35	1.77	11330	1.13	24.16
CRU	489.76	115.94	13376	17583	1.33	1.75	11245	1.12	23.99

TABLE 7. Characteristics Analysis of Different Short-Circuit Currents at Bus a Considering Fuse Protection

Operation mode	Peak current (kA)	Specific Energy ($kJ \cdot \Omega^{-1}$)	Energy (kJ)	Peak power (MW)
DP	463.79	65591	6.56	21.51
ECO	463.52	65544	6.55	21.48
CRU	461.14	65090	6.51	21.29

which decreases the resulting ESR and facilitates the energy transfer to the fault.

The numerical model indicates that the fault can create an unrecoverable blackout (worst case scenario) by blowing all the fuses in the generation feeders. The energy transferred from the capacitors surpasses the fuse limits in all generation feeders. Considering that the acceptable worst case involves losing one bus, a blackout is inherently a catastrophic fault that demands prolonged downtime for a partial recovery. The parameters in Table 7 describe the main characteristics of the pole-to-pole event on bus A with different initial conditions.

The absence of initial overshoot is not necessarily positive, as the peak current rises close to the maximum in the battery pack BP1 (see Table 6). The total energy in the capacitors is 86.4 kJ (see Table 3), and the amount transferred to the fault is, on average, 6.54 kJ, while the amount dissipated in the ESR is approximately 29.98 kJ. The outcome suggests that the fuses limit the transfer and dissipation of 57% of the potential energy in the output filters. However, the specific and absorbed energy are approximately 4.87 times larger than that of the battery pack BP1 case. Such a result could indicate that, despite the benefits of feeder fuses, short circuits in shipboard dc systems remain potentially dangerous, and the development of proper technology is necessary.

E. HIGH-SPEED BTS

Shipboard power grids utilized in sensitive applications, such as offshore platforms and cable layers, demand stricter design requirements than a superyacht [5], [9]. Therefore, it is recommended to employ solid-state BTSs in dc system protections to enhance the performance of the three-zone scheme [33]. The braking time of solid-state protection components (several microseconds) against their mechanical counterparts (a few milliseconds) can justify the recommendation [18]. Nevertheless, their cost, availability, and efficiency can hinder their deployment in shipboard dc systems.

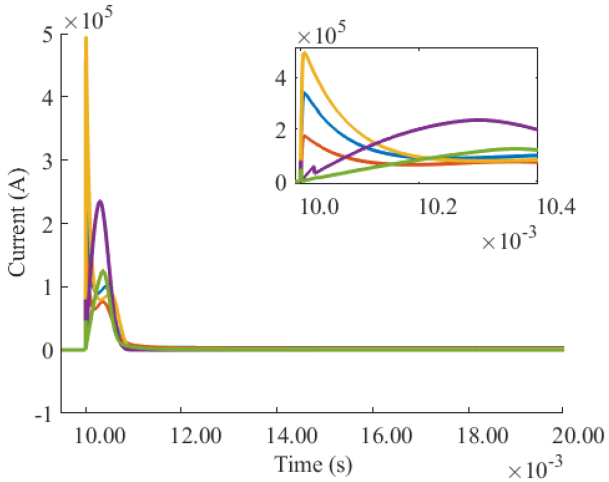

FIGURE 16. Pole-to-pole short-circuit current response at various locations with fuse protection and high-speed BTS, and the dc system operating in DP mode. Blue: generator G1. Red: generator G2. Yellow: battery pack BP1. Purple: bus A. Green: load zone A. Inset: Detail of the initial current overshoot after the short circuit, and the effect of the BTS.

The numerical model in this section includes a high-speed BTS, assuming negligible losses, to evaluate the protection performance gain of the system under several type-A faults. The response time of the BTS is 21 μs, according to the marine-certified solid-state component in [28]. The procedure is similar to previous cases, and the section covers the following topics: 1) fault current at different locations; 2) fault current sources for one of the locations; 3) voltage disturbances for the same case; and 4) the fault characteristics of two representative test cases.

1) FAULT CURRENT AT VARIOUS LOCATIONS

This section shows the effect of the high-speed BTS on the total fault current at different locations within the shipboard dc system. The analyses in Sections IV-C and IV-D conclude that faults occurring close to a filter get most of the initial overshoot energy from the capacitors, which implies that the high-speed BTS should not modify the fault current waveform of such cases during the first overcurrent.

Fig. 16 shows the fault current at various locations in the dc system. The corresponding signals in generators G1 and G2 and the battery pack BP1 exhibit no apparent differences against the previous case (see Fig. 14). On the contrary, short

TABLE 8. Fuse Activation and Degradation Derived From the Faults at Various Locations With a High-Speed BTS in Fig. 16

Location	Blown	Degraded
Generator G1	FG1 and FG2	None
Generator G2	FG2	None
Battery pack BP1	FB1 and FG2	None
Bus A	FG1, FG2, FB1	None
Load A	FLA	FG1, FG2, FB1

circuits located on bus A and load zone A display interesting differences to consider.

The action of the BTS interrupts the current build-up in bus A and load A by curtailing the energy transfer. Moreover, sympathetic fuse tripping, mentioned in Section IV-D, can become more apparent when having a high-speed BTS. Table 8 summarizes the activation and degradation of fuses during faults in Fig. 16, since the model can determine whether a fuse blows and the event instant.

The indicators in Table 8 depend mainly on the sizing of the fuse. For example, the fuse in generator G2 can experience sympathetic tripping when a short circuit occurs in generator G1, since the sizing corresponds to the lowest current. On the contrary, the cases condensed in Table 5 show the degradation of the fuse in generator G2 for the same fault location. Consequently, the action of the high-speed BTS can create oscillations sufficiently large to force the sympathetic tripping of the fuse, which could prolong the downtime of the faulty bus.

2) FAULT CURRENT SOURCES

Given that the added value of the high-speed BTS is most noticeable during pole-to-pole short circuits at the bus bars, this section studies the fault current sources for the bus A fault case and highlights the contribution of the component.

The fault current on the bus bars lacks the initial current overshoot since the use case does not include a dc bus capacitor (see Fig. 16). Instead, the current waveform is relatively similar for all contributing sources, as shown in Fig. 17.

The BTS action, detailed in Fig. 17, explains the current drop at approximately 21 μs after the fault in Fig. 16. The BTS trips during the build-up, interrupting the current flow from bus B and allowing continuous operation with one bus. In this case, determining the availability of the bus after a fault could be simplified to measuring the bus and load voltages to a certain extent. In addition, the fuses on the faulty bus eventually blow, clearing the fault and protecting the sources from a long-lasting overcurrent.

3) VOLTAGE DISTURBANCES

This section provides insights into the voltage disturbances when a bus A short circuit occurs, and the system has a high-speed BTS.

Section IV-D shows that buses A and B might fail simultaneously after a type-A fault on bus A when using a low-speed

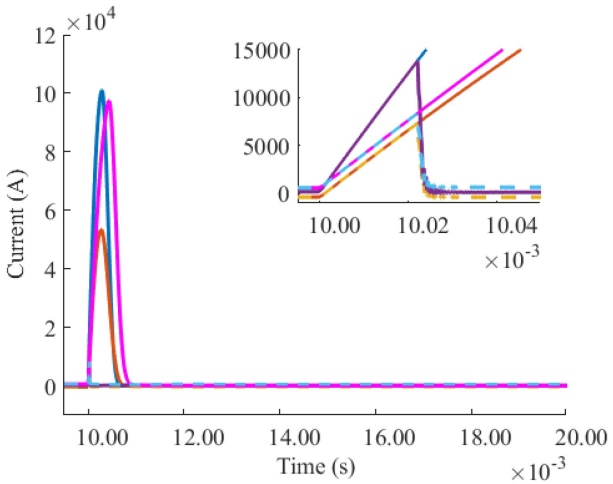

FIGURE 17. Fault current fed by different sources into a pole-to-pole short circuit at bus A with fuse protection and high-speed BTS, and the dc system operating in the DP mode. Blue: generator G1. Red: generator G2. Yellow: generator G3. Dash green: generator G4. Magenta: battery pack BP1. Dash light blue: battery pack BP2.

BTS. By deploying the high-speed component, the system can recover the voltage from the healthy side relatively quickly.

The BTS acts in a time frame comparable with the fault time, generating voltage oscillations, after which bus B and load zone B remain active. Thereafter, fuses on the faulty side operate, allowing the voltage recovery on the healthy bus, providing adequate time for diagnosis and reconfiguration actions. Finally, some control actions, such as load shedding and load management, can limit the effect of the contingency, allowing a better operation scenario during defect corrections.

4) FAULT CURRENT CHARACTERISTICS

This section aims to quantify the fault characteristics in the presence of a high-speed BTS. The fault characteristics of the battery pack are condensed in Table 9, considering the parameters explained in Section IV-C.

As anticipated, the parameters describing the fault adjacent to a filter are similar to those of the low-speed BTS case, and Section V presents a more in-depth comparison. Nevertheless, the main characteristics of short-circuit currents are the following.

1) The subsequent current peak is about 18.3% of the initial overshoot.
2) The specific and absorbed energy of the initial discharge are close to 83% of the total.
3) The adjacent filter provides 71% of the total energy and about 85.5% of it during the first overshoot.
4) The energy stored in the output filter is approximately 21.6 kJ, and the ESR dissipates about 20.76 kJ.

In addition, the fault on bus A exhibits different characteristics that highlight the benefit of the high-speed BTS. Table 10 summarizes the indicators describing pole-to-pole faults at the bus bars for various initial conditions.

TABLE 9. Characteristics Analysis of Pole-to-Pole Fault Currents With Different Initial Conditions at the Battery Pack BP1, Considering Fuse Protection and a High-Speed BTS

Operation mode	Peak current (kA)		Specific Energy ($kJ\cdot\Omega^{-1}$)		Energy (kJ)		Energy from adjacent filter (kJ)		Peak power (MW)
	First	Total	First	Total	First	Total	Specific	Energy	
DP	487.8	89.74	13219	15932	1.32	1.59	11361	1.14	23.79
ECO	491.56	89.66	13294	16003	1.33	1.6	11350	1.13	24.16
CRU	489.76	89.06	13204	15883	1.32	1.59	11265	1.13	23.99

TABLE 10. Characteristics Analysis of Pole-to-Pole Short-Circuit Currents With Different Initial Conditions at Bus A, Considering Fuse Protection and a High-Speed BTS

Operation mode	Peak current (kA)	Specific Energy ($kJ\cdot\Omega^{-1}$)		Energy (kJ)		Peak power (MW)
		First	Total	First	Total	
DP	235 56		16849	1.68	5.55	
ECO	235.43		16837	1.68	5.54	
CRU	234.38		16729	1.67	5.49	

BTS protection significantly reduces the peak current, allowing the specific energy to drop close to the case of battery pack BP1. Consequently, the short-circuit resistor absorbs about 1.68 kJ, and the ESR dissipates approximately 7.7 kJ, which comprises roughly 10.8% of the total potential energy.

The results suggest that increasing the performance of the BTS can improve the protection of the dc system in the event of a bus bar or load zone fault. However, it has a significantly limited effect on events close to output capacitors because of their disposition into the grid.

F. INDUCTANCE SENSITIVITY

Since the cable inductance is a function of the line length, the previous characterization can become somewhat susceptible to that parameter. A sensitivity analysis of the transmission line length in a single-feeder test could facilitate the visualization of such a tendency. The simplified model includes the feeder of G1, which requires a double circuit (18 cables per pole) attached to a load that demands the nominal power and is in parallel with a type-A fault branch. The iterative simulation varies the length of the transmission line from 0 to 120 m, taking steps of 4 m, increasing the distance from the output filters to the load and the short circuit.

The procedure advances using different computation tools and transmission line models to determine whether the model is agnostic to the software. The tools used are PLECS, LTSpice, OrCAD, and PSim, showing negligible differences across the tests. However, the tools based on SPICE models are considered more accurate, given the possibility of including more behavioral details.

In addition, the sensitivity analysis considers the variations in the transmission line model to enhance simulation performance. The variations include the pi section based on the telegrapher's equation, the *RL* model as lumped components, and an equivalent *L* model.

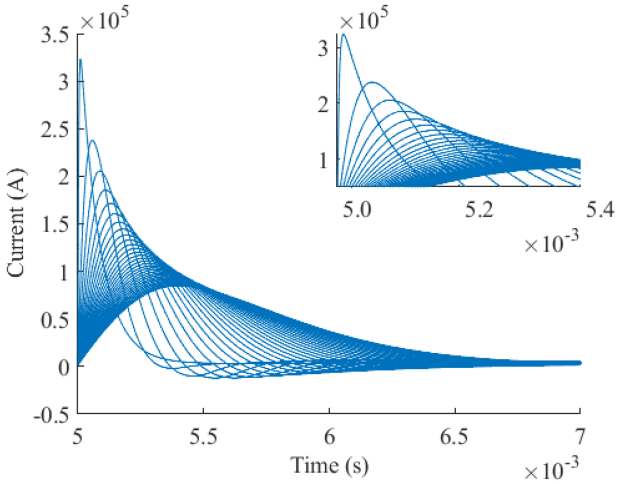

FIGURE 18. Simulation of the line length sensitivity analysis in generator G1 during a pole-to-pole short circuit using pi section models in a single-feeder model.

The pi-section-based model gives the only relevant result, since the error between pi sections and equivalent *L* models is close to 3.4% for the maximum peak and about 1.4% for the minimum. Furthermore, pi-section-based simulations and *RL*-based models have comparable results, in which the *RL* case demands a fraction of the computational burden of the pi. Nevertheless, the *RL* model standardized in [30] and utilized in [21] seems appropriate for complex shipboard dc systems.

The simulation in Fig. 18 shows the effect of the line length on the short-circuit current for the single-feeder test. The peak current, the average di/dt, and the time-to-peak current change significantly. The power line could delay the current overshoot to curtail the peak utilizing a high-speed BTS depending on the architecture and design constraints.

The influence of the resistive parameters on the limitation of the maximum current is considered negligible. Hence, the energy absorbed by the sort circuit resistor is similar to some extent for all cases. For the same type of fault, the maximum values for the extreme cases (0 and 120 m) are summarized in Table 11.

The sensitivity analysis indicates that it could be possible to modify the waveform of a short circuit by changing the inductance in the terminals by a few microhenries. However, it may be necessary to assess the effect of the inductance regarding stability and impedance while achieving appropriate

TABLE 11. Summary of Extreme Parameters in the Line Length Sensitivity Analysis in Generator G1 During a Pole-to-Pole Short Circuit

Peak current	$\Delta i/\Delta t$	Cabling inductance
334767 A	312.73 kA $\cdot \mu s^{-1}$	0 H
85012 A	2.09 kA $\cdot \mu s^{-1}$	2.64 µH

TABLE 12. Performance Indicators' Summary for the Battery Pack BP1 Considering Pole-to-Pole Fault Currents and Low-Speed and High-Speed BTSs

Bus-tie switch type	Peak current	$\Delta i/\Delta t$	Total energy	Peak power
Low-speed	491.56 kA	54136 A $\cdot \mu s^{-1}$	1.77 kJ	24.16 MW
High-speed	491.56 kA	54136 A $\cdot \mu s^{-1}$	1.6 kJ	24.16 MW

damping. Furthermore, the development of improved shipboard dc protections should not entirely rely on the damping effect of the inductance, given the variety and applications of power grids onboard.

V. PERFORMANCE ANALYSIS

This section aims to benchmark the performance of the protection approaches studied in Section IV; the shipboard dc system with feeder fuses and low- and high-speed BTSs. The severity of a short circuit in a dc system can be quantified by analyzing the peak current, the average di/dt (8), and the energy absorbed. By determining the performance indicators for battery pack BP1 and bus A, it is possible to assess the protection countermeasures in state-of-the-art shipboard dc systems

$$\frac{\Delta i}{\Delta t} = \frac{I_{\max}}{t_{I_{\max}} - t_{\text{fault}}}. \tag{8}$$

A. BATTERY PACK BP1

The high-speed BTS has little effect on the total short-circuit current for filter-adjacent faults compared to the low-speed case. In addition, fuses partially mitigate the propagation of the fault, which enables continuous operation in these cases. Table 12 summarizes the performance indicators for the fault in battery pack BP1.

A peak current fed by a relatively large capacity appears aggressive. The average maximum of 491 kA in a 1000-V dc system is a possible threat indication for the vessel. The average di/dt suggests that fault mitigation could become challenging, while the (thermal) stress of several components can become unendurable. Meanwhile, the total energy dissipated in the fault decreases by approximately 9.6%, which, in principle, reduces the stress in the output capacitors. However, the dissipated energy in the filter, estimated in 20.8 kJ from Table 9, may remain excessive. Hence, a high-speed BTS could reduce the propagation of faults near the output capacitors, with limited stress reduction in the ESR.

Subsequently, estimating capacitor damage is fundamental to diagnose the extent of a possible defect. The temperature

TABLE 13. Performance Indicators Summary for the Bus a Considering Pole-to-Pole Fault Currents and Low-Speed and High-Speed BTSs

Bus-tie switch type	Peak current	$\Delta i/\Delta t$	Total energy	Peak power
Low-speed	463.79 kA	1527.4 A $\cdot \mu s^{-1}$	6.56 kJ	21.51 MW
High-speed	235.56 kA	777.26 A $\cdot \mu s^{-1}$	1.68 kJ	5.55 MW

rise estimation in the capacitor core is a well-known damage indicator, and the temperature limits are available in most datasheets. The following equation yields the approximate core temperature in the capacitor based on power losses and thermal properties:

$$T_{\text{core}} = T_{\text{air}} + P_{\text{loss}} R_{\text{th}_{c-a}} \left(1 - e^{-t/\tau}\right) \tag{9}$$

with T_{core} and T_{air} being the temperature at the core of the capacitor and the ambient temperature, respectively, P_{loss} the power losses in the ESR, $R_{\text{th}_{c-a}}$ the core-to-air thermal resistance, and τ the thermal time constant of the capacitor [34], [35].

The following example illustrates the temperature rise estimation in a referential output capacitor in battery pack BP1. The analysis is based on an array of seven parallel legs of two series capacitors of reference 520C562T500DG2B [36] from CDM Cornell Dubilier. The equivalent capacitance obtained is 19.6 mF and the ESR is 5.6 mΩ, since the modules indicate 5.6 mF and 19.7 mΩ in the datasheet. The equivalent ESR is close to the value in Table 2, allowing a fair estimate. The battery pack utilizes three output capacitors, which leads to a peak power loss of approximately 1.03 MW per leg. The thermal resistance of the base capacitor is 0.84 °C $\cdot$ W^{-1} if it has a metal heatsink and an air circulation of 5 m $\cdot$ s^{-1} [36]. Since the losses in ESR are significant, the short circuit leads to an uncontrollable temperature rise that exceeds the damage threshold (around 105 °C) within tens of microseconds. Overheating increases the ESR, leading to a wear-out fault when the nominal value doubles [37], [38]. The calculation assumes impedance balance among capacitor modules and submodules, splitting the fault current evenly.

B. BUS A

The performance protection gain from the high-speed BTS becomes appealing when analyzing short circuits at the bus bars. Table 13 summarizes the calculations based on (6)–(8) for high- and low-speed BTS and faults at bus A. The peak current decreases at about 49.2% of the expected value with a low-speed component. The current variation rate drops to half (50.9%) of the average indicator. The specific and absorbed energy of the short-circuit current are only around 25.6% of the reference value. In addition, the peak power is close to one-fourth (25.8%) of the maximum power expected with a low-speed BTS.

Furthermore, the maximum power dissipated by the output capacitors on the recovered side decreases significantly. For instance, when taking the same reference capacitor as in

TABLE 14. Categorization of Short Circuits in a Double-Bus Shipboard DC System Considering Low-Speed and High-Speed BTS Based on Section IV

Location	Potential consequence		Detection	Localization	Severity
	Protection SB+F	Protection FB+F			
Bus A or B	• Blackout • Multiple capacitor wear-out	• Bus failure • Selective capacitor wear-out	Slow	Complex	1
Battery Packs BP1 or BP2	• Feeder failure	• Feeder failure	Fast	Simple	2
Largest filter	• Double bus instability • Long-lasting overcurrent • Selective capacitor wear-out	• Sympathetic failure • Single bus instability • Long-lasting overcurrent • Selective capacitor wear-out			
Generators G1 or G4	• Feeder failure	• Feeder failure	Fast	Simple	3
Smaller filter	• Double bus instability • Long-lasting overcurrent • Selective capacitor wear-out	• Sympathetic failure • Single bus instability • Long-lasting overcurrent • Selective capacitor wear-out			
Generators G2 or G3	• Feeder failure	• Feeder failure	Fast	Simple	4
Smallest filter	• Double bus instability • Long-lasting overcurrent • Selective capacitor wear-out	• Single bus instability • Long-lasting overcurrent • Selective capacitor wear-out			
Load A or B	• Load feeder failure • Double bus instability • Selective capacitor wear-out	• Load feeder failure • Single bus instability • Selective capacitor wear-out	Slow	Complex	5

battery pack BP1, the ESR losses at generator G4 jump from approximately 1.98 MW to 38.28 kW per leg. As of (9), the core temperature drops from a thermal damage of roughly 268 °C to a reasonable level of about 49 °C. On the other hand, the output filters on the faulty side are exposed to potential wear-out. Generator G2 seems especially vulnerable, since the ESR losses yield an approximate 2.2 MW peak per leg, which from (9) gives a core temperature close to 295 °C, damaging the component.

Therefore, the protection performance gained from the implementation of high-speed BTS is remarkable. The fault in bus A is effectively contained into a less threatening state while restraining the possible capacitor wear-out, which is essential in the operation of the dc system. The high-speed BTS could prevent the blackout discussed in Section IV-D, limiting a multicapacitor wear-out, affecting most of the primary system, into a selective wear-out, degrading only a section of the grid. Nevertheless, the inventory shows that the absence of efficacious feeder protection represents a substantial hurdle, which compels further investigation and improvement.

VI. FAULT CATEGORIZATION

The quantitative analysis in the fault inventory comprehensively describes the possible threats in the superyacht. The purpose of this section is to harness the results in Section IV to create a generic framework suitable for multiple types of vessels. Such a framework relies upon a fault categorization using qualitative indicators, such as potential consequences, detection speed, localization complexity, and fault severity.

The fault categorization is summarized in Table 14, followed by the categorization indicators and the interpretation of severity.

A. INDICATORS

The categorization utilizes several indicators to provide a comprehensive overview of the faults and determine their severity. The short-circuit categorization indicators are the following:

1) location;
2) potential consequences:
   a) protection with slow BTS and fuses ($SB{+}F$);
   b) protection with fast BTS and fuses ($FB{+}F$);
3) detection;
4) localization.

The location and potential consequences depending on the protection scheme are discussed in depth in Section IV. Detection and localization participate in the categorization by jointly analyzing di/dt differences and locations as follows.

Faults close to an output filter exhibit a high di/dt that is relatively straightforward to separate (e.g., Fig. 12). Assuming that the protection systems fit within a three-zone selectivity scheme, the alert signal generated by the drive can swiftly provide the most likely location of the fault.

In contrast, faults occurring far from the drives are more complex to identify (e.g., Fig. 17). The fault alerts could show a similar time stamp, suggesting that the most likely fault location is the bus bars or the load zones. However, it is necessary to compare the detection alerts and combine them with detection algorithms to accurately determine the location. Consequently, detecting such faults is complex and slow. Notice that previous definitions are possible by assuming the existence of appropriate di/dt and average current detection as in [7] and [39].

B. SEVERITY INTERPRETATION

The severity indicator in Table 14 provides the fault category for each scenario. The lowest severity indicator implies the most severe type of short circuit. Although the categorization seems initially counterintuitive, the arrangement allows the worst case visualization always as number one. In addition, the proposed numeration is consistent with the task prioritization schemes existent in most industrial controllers.

The categorization begins from the bus bars as the worst case, followed by generation feeders to finalize in the load zones. The categorization order from the highest to the lowest output capacitance is governed by the equivalent capacity that feeds the initial fault overcurrent. For example, the adjacent capacitor dominates the initial overshoot in a fault at generator G2. In the case of bus A, the measured overcurrent is supplied simultaneously by all parallel capacitors with their respective time constant.

VII. OUTLOOK AND CONCLUSION

A fault categorization considering potential threats in shipboard dc systems has been proposed in this article. The general methodology can be extrapolated to several types of vessels to enhance protection and control systems in modern sustainable vessels. A better understanding of faults was introduced, which is essential for the proper design and protection of power converters. In addition, the outcome of this work could help the evolution of the regulatory requirements of maritime power systems. To the best of the authors' knowledge, the conducted studies have no precedent.

The fault characterization provides a framework for analyzing possible short circuits at different locations onboard, utilizing comprehensive parameters to describe and differentiate events. Faults located in generation feeders produce similar fault waveforms, whereas events at the bus bars require different analyses. In the same way, fluctuating characteristics lead to variable consequences that escalate from a single-feeder failure to a blackout.

The added value of the work lies in combining different techniques to give essential insight about the events. The techniques used involve analytical methods, simplified numerical models, and complete simulation models covering 45 test cases.

From the analytic model, it is possible to determine the approximate waveform of the initial overcurrents in the events adjacent to the filter because most of the energy comes from the capacitor. However, bus bar and load zone faults require additional complex calculations to incorporate all feeders, compromising the practical benefit of the method.

Complimentarily, the complete numerical model allows a comprehensive analysis of the fault current and the sources involved. The studies compare the effect of three system configurations during pole-to-pole short circuits in various scenarios: 1) the nonprotected approach; 2) the protection with feeder fuses; and 3) their combination with a high-speed BTS were compared.

Ultimately, fuses can interrupt the propagation of specific faults after the initial overshoot, blocking about 70% of the potential energy. However, the rest of the phenomena could be sufficient to cause permanent damage in some components and temporary malfunctions. The system becomes more fault-tolerant by incorporating the high-speed BTS since the healthy bus is effectively protected. Faults on the bus bars and load zones seem to be attenuated by current limitation. However, initial overshoots are not significantly affected by the performance of the BTS, which can still lead to permanent damage.

The simulation model based on realistic state-of-the-art shipboard dc systems mainly considers a distributed switchboard. Thus, parallel cabling creates electric distances among the components that could dampen the peak current. The purpose of the simplified simulation model was to include the inductive effect of the cabling to expand the applicability of the results. Correspondingly, the sensitivity analysis shows that the inductance dominates the damping effect of the short circuit in the case study.

The scale of the dc system is an obstacle for the experimental validation of the simulation results considering the entire system. However, the detailed study of the simplified feeder shown in this document is the basis for future work that involves systematic testing of novel protection devices. A combination of low-power mock-up shipboard dc systems and high-power single-feeder tests could provide sufficient evidence in validating the results. The following subjects are considered relevant for future work in the development of dc protection systems.

1) The BTS model requires an independent study, mainly focusing on certified topologies and assessing their limitations.
2) Experimental validation is necessary to assess the dependence of ESR and other parasitic elements on temperature and frequency during a fault.
3) Fuse models are widely considered oversimplified, as their behavior is challenging to model. Validation with scaled-down setups could reduce the uncertainty of the study, but only for specific fuses and distribution architectures.
4) Faults to ground and pole-to-pole-to-ground require further investigation, since they depend on the grounding scheme.
5) Simulations based on ideal sources may not be suitable for long-lasting fault assessments and their potential effect on drive controllers.
6) The adaptation of the model to a real-time environment could help reduce uncertainty while potentially increasing accuracy.

The development of hardware protection requires significant improvement. The current situation shows that blocking of the fault current sources may be necessary to reduce the possibility of severe defects. However, solid-state circuit breakers are not considered cost-effective or efficient enough to be suitable for widespread use in maritime applications.

Advancements in protection technologies enable safe primary dc systems, crucial for the integration of alternative energy sources. Such technologies are fundamental for global emission reduction and a sustainable future.

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