Briefs

Single-Grain Si TFTs With ECR-PECVD Gate SiO_2

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***Abstract*—High-performance Si thin-film transistors (TFTs) are fabricated inside a single, location-controlled grain with gate SiO_2 deposited by electron cyclotron resonance plasma enhanced chemical vapor deposition (ECR-PECVD). The position of the large grains is controlled by μ-Czochralski (grain-filter) process with excimer-laser crystallization. Owing to the low interface trap density of ECR-PECVD SiO_2 the single-grain Si TFTs showed a smaller subthreshold swing of 0.45 V/decade, in addition to a higher field-effect mobility for electrons of 460 cm^2/Vs than that with low-pressure chemical-vapor deposited (LPCVD) SiO_2.**

***Index Terms*—Crystal growth, dielectric materials, excimer lasers, location-control, poly-Si, thin-film transistors (TFTs).**

I. Introduction

Excimer-laser crystallization of amorphous-Si (a-Si) film has facilitated the realization of driver circuit integrated liquid crystal displays (LCDs), since polycrystalline-Si (poly-Si) thin-film transistors (TFTs) can be formed on glass substrates without thermal damage [1]. Although the poly-Si TFTs have higher field-effect mobility compared to that of a-Si TFTs, it is still lower than that of MOS transistors formed on bulk Si wafers, and not sufficient for other system applications, such as digital/analog converter, power controller, or processor. The lower carrier mobility is predominantly caused by carrier scattering at potential barriers formed at grain boundaries. This can be solved by forming TFTs inside a grain [2], i.e., single-grain Si TFTs, which do not have any grain boundary in the active region.

For producing the single-grain Si TFTs on glass, it is essential to control the position of large grains at a desired position on the substrate. The positions of the grains can be controlled by local melting/unmelting of the Si film. We have carried out local structural and/or material variations of the underlying materials by a conventional photolithography step [3], [4], rather than spatially modifying the intensity of the incident laser light [5]. The method has an advantage that one can accurately control the position of the grains with respect to the substrate. The μ-Czochralski (grain-filter) process [4], basically uses locally increased thickness of the a-Si film and geometric selection of grains through a vertical narrow constriction. TFTs fabricated inside such location-controlled Si grains showed a field-effect mobility $\mu_{\rm FEe}$ for electrons of as high as 430 cm^2/Vs and very low off-current of around 0.1 pA [6]. Subthreshold swing S, however, was as high as 1.2 V/decade [2], [6].This would be predominantly caused by an inferior Si/SiO_2 interface resulted by the gate SiO_2 formed by low-pressure chemical vapor deposition (LPCVD) with nonoptimized deposition conditions.

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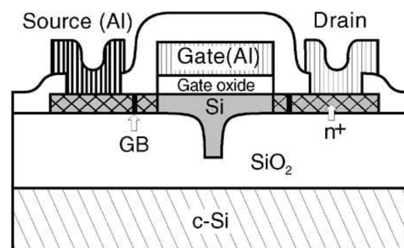

Fig. 1. Schematic view of the single-grain Si TFTs.

On the other hand, electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) allows one to form a dense SiO_2 layer and good Si/SiO_2 interface, owing to the remote plasma process and high electron density in the plasma [7]. It has been reported that SiO_2 deposited by the ECR-PECVD at room temperature with successive annealing at 333 °C has an interface trap density $D_{\rm it}$ in the order of 10^{10} $cm^{-2}eV^{-1}$ [8]. Poly-Si TFTs fabricated with the SiO_2 as a gate insulator is reported to have S of as low as 0.21 V/decade [9].

In this study, ECR-PECVD SiO_2 was used as a gate insulator of the single-grain Si TFTs fabricated inside a location controlled grain. The properties of the single-grain Si TFTs will be presented and discussed.

II. Experimental

The single-grain Si TFTs were fabricated inside location-controlled grains by the μ-Czochralski (grain-filter) process. The structure of the TFTs is schematically shown in Fig. 1.

First, holes were formed in a 750-nm-thick SiO_2 layer by photolithography and anisotropic dry etching. By varying the exposure energy to photoresist, the diameter of the original holes was varied from 900 to 1250 nm. Successively, a 875-nm-thick TEOS PECVD SiO_2 layer was deposited over the structure, reducing the diameter of the final holes varying from 70 to 200 nm. Then a-Si films with a thickness of 250 nm were deposited by LPCVD at a temperature of 545 °C. One shot of XeCl excimer-laser (308 nm, 56 ns) irradiated the structure with an energy density of 1.02 J/cm^2 at a substrate temperature of 450 °C.

A SEM image of a grid of location controlled grains, after defect delineation etching, is shown in Fig. 2. Grains were grown from the seeds near the bottom of the grain filters, located beneath the center of each grain. Since the spacing between the holes is 3 μm in this particular example, which is smaller than the obtainable grain diameter of 6 μm with an enough distance, grains collide and form a grid of square shaped grains. Electron backscatter diffraction (EBSD) analysis of such grains showed that the planer defects in the grains are mainly Σ 3 grain boundaries [10]. It was also found that there are no clear preferred surface crystallographic orientations of these grains.

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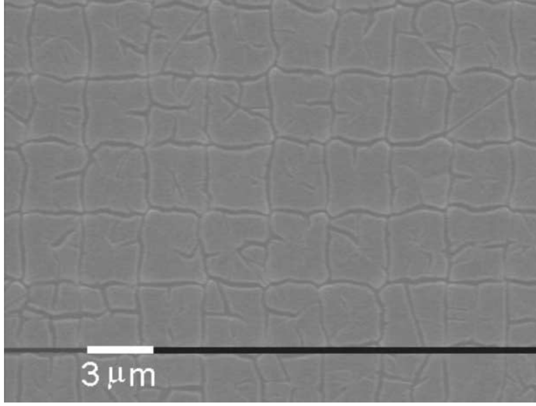

Fig. 2. SEM image of the grid of location controlled grains formed by μ-Czochralski (grain-filter) process.

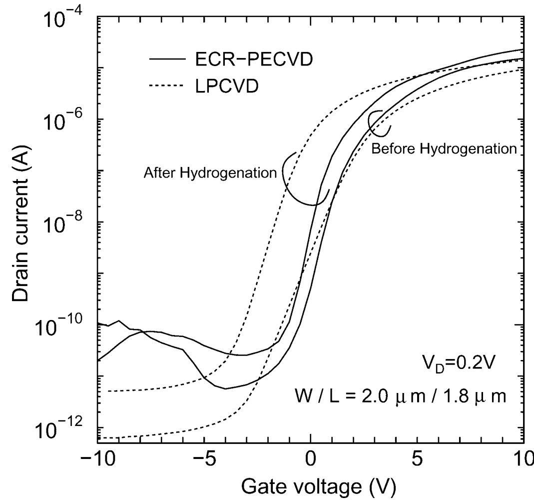

Fig. 3. (Thick line) I_D–V_G characteristics of single-grain Si TFTs fabricated with ECR-PECVD SiO_2 and (dotted line) LPCVD SiO_2 as a gate insulator. The characteristics before and after plasma-hydrogenation are shown.

After formation of the location controlled grains, the Si film was patterned into islands by dry etching. The TFT channel region was designed so that a single grain covers the entire channel area.

Then, a 137-nm-thick SiO_2 film was deposited by ECR-PECVD [8] at room temperature. Microwaves of 2.45 GHz parallel to the magnetic field lines were introduced to the chamber via a quartz window. SiH_4 and O_2 were used as source gasses and pressure was kept at 1 mtorr. The sample was successively annealed at 333 °C in H_2O and N_2 ambient. As a reference, SiO_2 film with a thickness of 165 nm was deposited by LPCVD at a temperature of 424 °C.

The gate electrode was then formed with sputtered Al and, successively, phosphorous ion (1×10^{16} cm^{-2}) were implanted into the source and drain regions with a self-alignment manner. After activation of the implanted atoms by excimer-laser irradiation (300 mJ/cm^2), passivation oxide and the drain and source electrodes were formed. The channel length and width were measured by SEM to be 2.30 μm and 1.83 μm, respectively. For reference purpose, TFTs were fabricated also with $\{100\}$ oriented, silicon-on-insulator (SOI) bonded wafers with identical process steps as the single-grain Si TFTs. The samples were annealed in hydrogen plasma ambient with a substrate temperature of 350°C and a duration of 30 min.

TABLE I
CHARACTERISTICS OF SINGLE-GRAIN SI TFTS BEFORE AND AFTER HYDROGEN-PLASMA ANNEALING

	Before hydrogen-plasma		After hydrogen-plasma	
	ECR-PECVD	LPCVD	ECR-PECVD	LPCVD
μ_{FEe} (cm^2/Vs)	450±50	290±50	460±80	420±70
S (V/dec.)	0.55±0.08	0.97±0.15	0.45±0.05	0.70±0.25
V_{TH}	2.7±1.0	3.0±0.5	4.2±1.0	0.2±0.4
I_{off} (A)	(4±2)×10^{-12}	(7±1)×10^{-13}	(1±1)×10^{-11}	(5±0.5)×10^{-12}

III. RESULTS AND DISCUSSION

Fig. 3 shows typical I_D–V_G characteristics of the single-grain Si TFTs before plasma-hydrogen annealing. The extracted average characteristic values with the standard deviation are tabulated in Table I. Here the threshold slope and off-current was defined by linear extrapolation of the I_D–V_G curves and by the minimum drain current, respectively. The average μ_{FEe} value which was evaluated by the maximum in a linear regime with a low V_D, of the single-grain Si TFTs with ECR-PECVD SiO_2 (450 cm^2/Vs) was higher than that of the TFTs with LPCVD SiO_2 (290 cm^2/Vs). The μ_{FEe} value for the TFTs fabricated with the SOI wafer was 700 cm^2/Vs. The leakage current of the TFTs with ECR-PECVD SiO_2, however, is higher than that with LPCVD SiO_2, especially in the strong negative V_G bias. The S value, calculated at the maximum slope, of the TFTs with ECR-PECVD SiO_2 was 0.55 V/decade, much lower than that with LPCVD SiO_2 (0.97 V/decade). The low S value of the TFTs with ECR-PECVD SiO_2 was a result of the low D_{it} value. The D_{it} value of the SiO_2 deposited by ECR-PECVD and LPCVD, estimated from high frequency and quasistatic C–V characteristics of MOS capacitors, was 9.7×10^{10} cm^{-2}eV^{-1} and 8.2×10^{11} cm^{-2}eV^{-1}, respectively. It should be mentioned that these MOS capacitors were not annealed in the plasma hydrogen ambient, but in nitrogen at 350 °C for 30 min, which is similar to conditions of the rest of the TFT process steps after the gate SiO_2 deposition. S can be described as

$$S \cong \frac{\kappa T}{q} \ln 10 \left(1 + \frac{qN_{bt}t_{Si} + qD_{it}}{C_{ox}}\right) \tag{1}$$

where N_{bt} is the bulk trap state density per unit volume, t_{Si} the thickness of Si and C_{ox} the gate oxide capacitance per unit area. By using the equation and the D_{it} values for each oxide, N_{bt} was estimated to be 3.6×10^{16} cm^{-3}eV^{-1} and 4.2×10^{16} cm^{-3}eV^{-1} for TFTs with LPCVD SiO_2 and ECR-PECVD SiO_2, respectively. The slightly higher N_{bt} value for TFTs with ECR-PECVD SiO_2 would be the cause of the higher leakage current. The N_{bt} values are smaller than that of conventional poly-Si TFTs (2×10^{17} cm^{-3}eV^{-1} [11]) but apparently larger than that of single-crystalline Si MOSFETs (5×10^{15} cm^{-3}eV^{-1} [12]). While the relatively large N_{bt} value might be caused by the planar defects in the grain, it could be caused by the defects in the grain filter which the TFT channel region possesses. Shifting the active channel region from the grain filter to the outside and/or decreasing the thickness of the Si will thus be effective to reduce total amount of defects $(N_{bt}t_{Si})$ and hence improve the S value. It should be noted that the spread in the S value of the single-grain Si TFTs with ECR-PECVD SiO_2 is much less than that of the LPCVD. This could be associated with the random surface crystallographic orientation of the grains. For the TFTs with LPCVD SiO_2, the surface crystallographic orientation dependent D_{it} gives a large influence on S, whereas S of the TFTs with ECR-PECVD SiO_2 is predominantly determined by N_{bt} as the D_{it} is much less.

The transfer characteristics and characteristic values after the hydrogen-plasma annealing is also shown in Fig. 3 and in Table I, respectively. For the single-grain Si TFTs with LPCVD SiO_2, both μ_{FEe} and

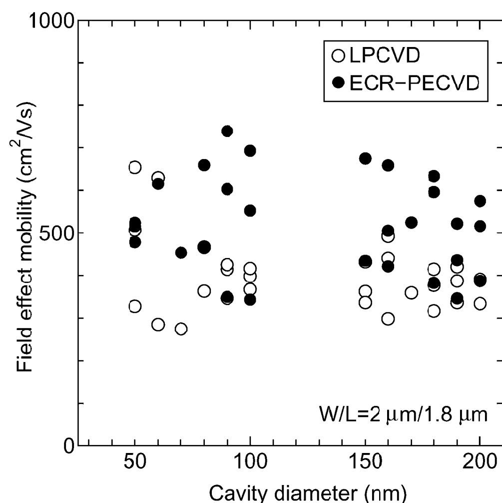

Fig. 4. (Open circles) Field effect mobility of single-grain Si TFTs with ECR-PECVD and (closed circles) LPCVD SiO_2 as a function of diameter of grain filter.

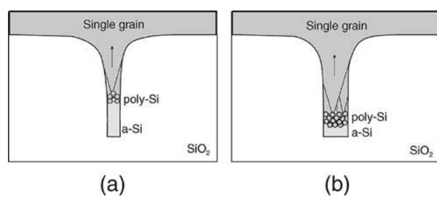

Fig. 5. Schematic view of μ-Czochralski process with (a) smaller and (b) larger grain-filter diamter.

S value were improved by the hydrogen-plasma annealing, whereas the TFTs with ECR-PECVD SiO_2 do not show such clear improvement. The improved characteristics of the TFTs with LPCVD SiO_2 are, however, still inferior to that with the ECR-PECVD SiO_2. This suggests that the hydrogen-plasma passivates the bulk or interface traps more effectively in the single-grain Si TFTs with LPCVD SiO_2 than that with the ECR-PECVD. The threshold voltage V_{th} of TFT with ECR-PECVD SiO_2 is relatively high. This was caused by possible negative charges trapped in the bulk SiO_2 during the deposition as the V_{th} value before hydrogen plasma annealing is already high (3.2 V).

For both single-grain Si TFTs, the spread of μ_{FEe} is a few times higher than that for the SOI-TFTs (10 $\mathrm{cm}^2/\mathrm{Vs}$). This could be associated with the random surface crystallographic orientation and spread in the amount and directions of planar defects being mainly Σ 3 grain boundaries, in the channel [10].

Fig. 4 shows μ_{FEe} of the single-grain Si TFTs as a function of the final hole diameter of the grain filter. The μ_{FEe} shows very gentle decrease with the diameter of the cavity. The decrease is predominantly caused by the increase in the amount of random planar defects in the grain. In the μ-Czochralski process, if the grain-filter is narrow and deep enough, one grain of poly-Si is occluded in the grain-filter, as shown in Fig. 5(a). When the diameter of the grain-filter is large, the effect of the grain occlusion becomes less, resulting in the increased number of random planar defects, such as high angle grain boundaries. The decrease of μ_{FEe} is, however, rather gentle with the grain-filter diameter. This is because, the melt depth increases with the cavity diameter, as heat conduction in the Si column increases. When the melt depth increases, the occlusion is more effective owing to the longer grain-filter path, as shown in Fig. 5(b). It is possible that the improved grain occlusion in the vertical growth phase made the mobility dependence on the cavity diameter gentle.

IV. Conclusion

High-performance Si TFT is fabricated inside a single, location-controlled grain with gate SiO_2 deposited by ECR-PECVD. The position of the large grains is controlled by μ-Czochralski (grain-filter) process with excimer-laser crystallization. Owing to the low interface trap density of ECR-PECVD SiO_2, the single-grain Si TFTs showed both a smaller subthreshold swing of 0.45 V/decade and a higher field-effect mobility for electron of 460 $\mathrm{cm}^2/\mathrm{Vs}$. The characteristic values are superior to the single-grain Si TFTs with conventional LPCVD SiO_2. Plasma-hydrogenation annealing improved the TFTs with LPCVD SiO_2 effectively, however, the characteristic values do not exceed those of the TFTs with ECR-PECVD SiO_2. These superior performance suggest that the combination of the single-grain Si TFT by μ-Czochralski (grain-filter) with ECR-PECVD gate SiO_2 is attractive for future system circuits integration in active-matrix LCDs.

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