Universal Digital Class D Current Driver for Inductive Motors

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Master of Science Thesis

TU Delft Delft University of Technology

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Universal Digital Class D Current Driver for Inductive Motors

By

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September 2021

To obtain the degree of Master of Science in Microelectronics

At the Delft University of Technology

Master of Science

in Electrical Engineering

at the Delft University of Technology,

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Abstract

This thesis discusses the basic architecture, design details, circuit implementation, and measurements of a digital class D current driver.

The driver contains two main parts: a digital control loop and analog circuits.

Parts of the important part in the digital control loop contain noise shaper, plant compensator, and cable capacitance compensator. The noise shaper has two core functions: 1. It seeks to minimize the difference between the process variable and the set point. 2. It shapes the noise that is generated in the forward loop. The plant compensator is used to compensate for the output filter, the load, and the cable. The cable capacitance compensation is a measure-based technique to generate a negative output capacitance to compensate for the cable capacitance. The analog circuits consist of a full bridge, data acquisition circuits, and floating supplies.

Multiple simulation models have been made in Matlab. According to the simulation results, the amplifier shows its flexibility and performance to handle a large range of inductive loads.

A prototype has been implemented. The measurement results show that most of the hardware performance is as intended. Due to the time limitation, the whole amplifier is not tested.

Keywords: Noise shaping, current driver, pole-zero compensation, cable capacitance compensation.

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Acknowledgments

I am deeply grateful to all the people who have helped me during my master thesis project in one way or another. The two years' study ad work, being the hardest and the most personal task I have ever faced so far, could not be complete without the help of my family and friends.

I would like to thank my supervisor, Dr. Chris Verhoeven, for his invaluable support and suggestions to complete this project.

I am grateful to my supervisor Anton Montagne, who has been my most important mentor during these three years in Delft. I think it is an honor to become one of his students. During the first year of the master program, I learned a lot from Chris and his course of Structural Electronic design and its master class. I remember he always quoted the sentence from Einstein that everything should be made as simple as possible, but no simpler. It helps me to solve different kinds of scientific problems in my graduation project. In this wide-range project, his invaluable support helped me connect many courses that I studied in TU Delft. At the end of the project, I have the confidence to handle multi-discipline projects and become an independent researcher in the future.

I would like to thank my daily in-company supervisor Mr. Nekeman, for his continuous support and encouragement throughout my master thesis project. He kept a close relationship with me to the project through weekly meetings, and he was always willing to share his knowledge with me. When I met some tough problems during the graduation project, he was always patient and helped me.

I am grateful to Jurre Kalf, who is the first student partner with me in this project. During the first half of the internship, we had plenty of meetings to discuss analog circuits and lots of enjoyable chats during the internship time. He is the key member to realize the final prototype.

I would like to thank Sjoerd Burm, the second student partner with me in this project. We had many conversations on implementing the firmware and lots of enjoyable chats during the internship time. He is the key member to realize the final prototype.

I would also like to thank Prof. Wouter Sedrijn and Dr. Fabio Sebastiano for allowing me to be part of the thesis committee to judge my work.

I want to thank my friends from TU Delft who made my time in the Netherlands a happy experience.

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I want to express my gratitude to two special friends in the Microelectronics department: Chenyan Zhang and Yu Huang. During this special year, we had many connections in terms of study, life, and entertainment. We helped and learned a lot from each other.

Lastly, I would like to thank my family for all that they have done for me. I could not take the courage to study 10000 km away from home without their support. Thanks for their continuous love, care, and encouragement throughout my life.

Haoyuan Li

Delft, September 20th 2021

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1. Introduction

1.1. Scope of the project

The scope of the thesis is to design a digital input current output power amplifier with a flexible digital control loop. In general, the motor is usually driven by a high-efficiency power amplifier. If the amplifier's efficiency is high, the losses in the amplifier are low such that cooling is not necessary for it. To achieve a high power efficiency, the switching amplifier or class D amplifier is a common option.

In this specific assignment, the motor is the power amplifier's load, and it can be driven by the current or the voltage. It is favorable to be driven by the current. According to the Torque equation and Lorentz force law, the motor's torque is proportional to the motor's current. Therefore, the torque of the motor can be accurately controlled by controlling the current through it.

If the voltage driver drives the motor, its torque will be influenced by its impedance based on Ohm's law. The impedance of the motor varies with frequency, temperature, and position.

Figure 1.1 shows an example of a fixed frequency current output power amplifier with an analog control loop. The reference signal determines the frequency of the switching amplifier, which frequency is f_{ref}.

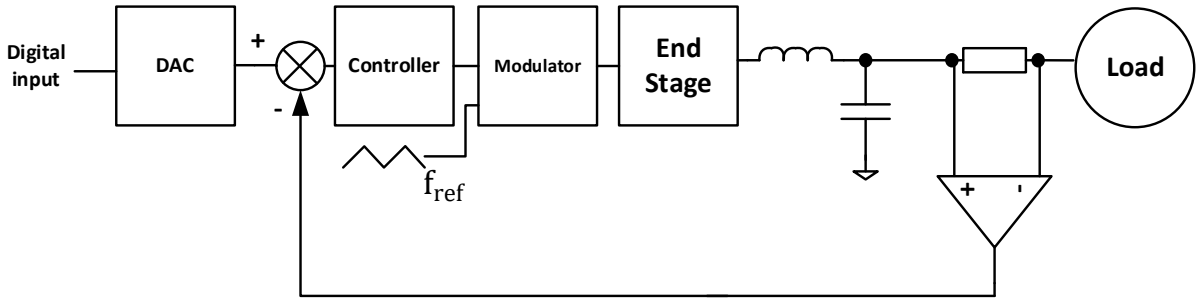


Figure 1.1 Example of Analog current output power amplifier

As mentioned before, the analog control loop has two main limitations. First of all, the amplifier always needs a DAC to transfer the digital input to the analog input, which will cause more delay and more significant inaccuracy. Secondly, the analog controller and modulator limit the flexibility of the amplifier.

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The main control loop of the digital-in power amplifier can be designed in the digital domain to obtain higher flexibility. With highly tunable parameters in the digital domain, the amplifier can quickly meet the demand of various projects. As a result, the power amplifier with a mixed-signal control loop will be a more impressive candidate than the power amplifier with an analog control loop.

This project will focus on the design of the power amplifier with the mix signal control loop, which is the title of the thesis project.

1.2. Prior art

This thesis deals with designing a current driver with a flexible digital control loop. In literature, most of the power amplifiers with the digital control loop are voltage drivers. The techniques which are applied for the voltage drivers can solve similar problems in the current drivers. Several typical digital class D voltage drivers have been reported to [2]–[6]. There are two topologies of these closed-loop voltage drivers: 1. With feedback before the output filter. 2. With feedback after the output filter.

The topology with feedback before the power stage has been widely applied in mobile applications [2]-[4]. However, it does not mitigate the influence of the output filter components on the signal transfer.

Constructing the feedback after the power stage can be the issue above. But the output filter components will influence the control loop. In 2009, the structure reported by T. Mouton et al. [5] had emerged as an interesting candidate, which employed a digital compensation filter to cancel the effect of the output filter. The research in [6] optimized the controller in [5] to further improve the system's stability.

The topologies above only apply to resistive loads. The amplifiers must apply for inductive loads, which means the order of the plant will be larger than the situation for the resistive load. This configuration will increase the requirement of the digital compensation filter. Fortunately, there are some techniques to decrease the order of the plant:

1. Apply current mode control techniques. It can convert the power stage of the driver from a voltage source to a current source. With the current mode control, the output filter inductor will not influence the control loop. Section 2.2.3 illustrates the details of the current mode control. This technique is widely applied in the Switch Mode Power Converter (SMPC) applications [7]–[8] and switching amplifier applications [9].

2. Employ fixed-ripple current self-oscillating techniques. With the fixed-ripple current module, the effect of the output filter on the control loop can be effectively eliminated.

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This technique has been discussed in [10]-[11]. Section 2.2.3 presents the details of the fixed-ripple current self-oscillating configurations.

However, the works of literature above [7]–[11] do not apply with a digital control loop. Therefore, digital current drivers driving inductive loads and their control loop is an area of research with little to no publication.

Besides, the required current driver needs to drive a large cable capacitance, which is referred to in Section 1.3. The effect of the cable capacitance will dramatically influence the control loop, which has not yet been discussed in the literature.

In conclusion, this project aims to design an amplifier which is in a new research area. It needs to combine the old configurations to design a new concept.

1.3. Objectives

Table 1.1 lists the required specification of the digital power amplifier. The information of the source impedance is confidential.

Table 1.1 Required specificatiosn form of the power amplifier

Group	Symbol	Parameter	Condition	Min	Typ	Max	Unit
Source and load	$f_{\mathrm{I,in}}$	Input frequency	Sample rate = 20kHz	-	-	10	kHz
	I_d	Continuous output current	RMS	-	1.25	-	A
	I_d	Peak output current	Duration < 5s	-	-	3	A
Supply	V_{sup}	Power stage supply voltage	-	-	32	-	V
Dynamic behavior	f_b	Amplifier bandwidth	-	20	-	-	kHz
	τ	Source to load delay	-	-	-	12.5	us
	δ	Step response overshoot	-	-	-	20	%
Inaccuracy and nonlinear behavior	σ_1	Static gain error	-	-	-	0.5	%
	σ_2	Gain flatness	0 – 100 Hz	-	-	0.1	%
	σ_3	Gain inaccuracy	-	-	-	0.5	%
Efficiency	η	Power efficiency	*	80	-	-	%
Noise performance	i_e	The equivalent output referred current noise	0 – 1000 Hz	-	-	$6.76 * 10^{-16}$	A^2Hz^{-1}

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Operating conditions	T	Ambient temperature	-	-	45	-	°C

Cost factors:

The designed amplifier should have a tunable digital control loop to satisfy the requirements of different projects.

* Load and output condition: R_m = 5.5 Ω and I_{load} = 3 A

1.4. Report Organization

This thesis presents the design of a mixed-signal current output power amplifier, including basic architecture, prototype implementation, and experimental results. Apart from the introductory chapter, the rest of the report is divided into seven chapters.

Chapter 2 contains the concept design of the power amplifier, including the design considerations and the design of the top-level architecture. This chapter presents four concepts and compares them in different aspects. In the end, a fixed frequency current output power amplifier is proposed.

Chapter 3 illustrates the detailed design of the proposed concept. The design process of the digital control loop and the analog acquisition board is demonstrated in this chapter.

Chapter 4 evaluates the performance of the detailed design, the simulation model, and the simulation results are shown in this chapter.

Chapter 5 shows the implementation of the prototype, including the digital control loop implementation and analog board implementation.

Chapter 6 describes the test procedure of the complete amplifier.

Chapter 7 demonstrates the overall performance of the digital power amplifier.

Finally, Chapter 8 summarizes the conclusions of this thesis and gives suggestions for future work.

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2. Conceptual design

2.1. Design approach

In this application, a step-by-step structured design methodology is followed [12], and the outlines of the design progress are as follows:

1. Consider the required specifications of the power amplifier to find a more orthogonal design method. A linear simulator SLiCAP is used to facilitate design considerations.

2. Generate four concepts based on the design considerations.

3. Model and evaluate the performance of the concepts.

4. Compare the concepts and select the best concept.

5. Develop and evaluate the best concept (Detailed design).

6. Implement the developed proposed concept

7. Do the integration test for the amplifier block and analyze the measurement results.

2.2. Design considerations

According to the required specifications, the performance is expressed in terms of power efficiency, large-signal behavior, small-signal behavior, sampling, and noise. At the end of Section 2.3, four concepts are designed and compared. After ranking the concepts, the best concept is selected and further developed in Chapter 3.

2.2.1. Power efficiency

Calculating the losses equations for the class D current driver can directly estimate the efficiency of the power amplifier. The details of the equations are presented in Section 3.2. In this assignment, the design of the power efficiency can be designed independently with the design of the noise, small-signal behavior.

There are the following reasons: 1. During the efficiency design, the switching frequency of the amplifier can be designed for the highest value. In this case, the corner frequency of the output filter can also be designed for the highest frequency, which has the minimum effect on the control loop. 2. The current sense resistor can be designed to the largest value, contributing to the lowest current noise.

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2.2.2. Large signal behavior

The plant is modeled and presented in Figure 2.1. The current through the load I_{load} mainly contains two components, including signal current which compromises the input set point signal, and ripple current which contains the information of switching signal.

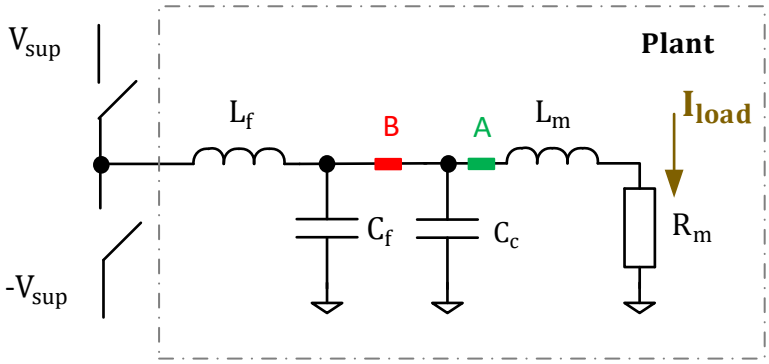


Figure 2.1 Equivalent circuit model of the load with two current sensing branches

The feedback signal of the current amplifier is the output current. The output current is defined as the current through the current sense branch. Figure 2.1 presents two current sense branches to sense the output current. Compared with sensing the current through branch B, sensing the current through branch A has two advantages: 1. It has a higher accuracy since this configuration directly controls the current through the motor. 2. The effect of the cable capacitance on the control loop can be nearly ignored, as $C_f \gg C_c$ in the practical situation.

However, the distance between the load and the amplifier is too long (>40m), requiring a long cable to construct the feedback path. It will increase the area and cost, which is unacceptable for the current assignment. Therefore, this configuration will become a recommendation in future assignments. Sensing the current through branch B does not need to construct a long feedback loop. However, the cable capacitance will have a more considerable impact on the control loop. It will need to be taken into account during the small-signal behavior design.

In this case, assuming the switching scheme of the current driver is fixed frequency, the ripple current through the filter inductor can be expressed as:

$$I_{Ripple,Lf} = \frac{V_{sup}}{2L_f f_{pwm}}(1 - (2D - 1)^2) \tag{2.1}$$

Where D is the duty cycle of the PWM signal.

With Eq 2.1, the ripple current through the load can be expressed as:

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$$I_{Ripple,load} = \frac{\frac{1}{sC_f}}{\frac{1}{sC_f} + R_{sense} + \frac{1}{sC_C} // (R_m + sL_m)} I_{Ripple,Lf} \quad (2.2)$$

Where $s = 2\pi f_{pwm}$.

In the mix signal application, the ripple current may have an effect on the nonlinearity at the output of the ADC. Figure 2.2 illustrates the plant of the current driver. The amplifier's output current I_{out} is sensed by a current sense resistor R_s and amplified by the differential amplifier with a gain of A_d.

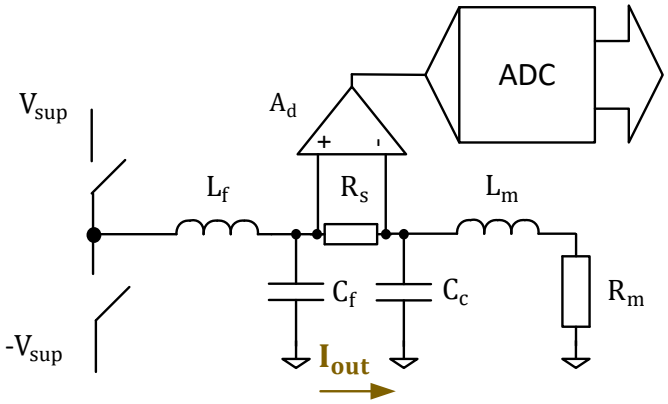


Figure 2.2 Equivalent circuit model of the load with the current sense circuit and the ADC

The ripple current comprises the high-frequency content, which requires a high-speed ADC to prevent the aliasing. However, the maximum sample rate of the FGPA will limit the ADC's sampling frequency. An alternative is synchronizing the sampling frequency with the switching frequency. The ripple components can be effectively attenuated by the Sinx/x filter, introduced by holding operation in the ADC. But the ripple current varies with its duty cycle. This results in a signal-dependent error which will degrade the accuracy of the feedback signal. Figure 2.3 shows the error for two given duty cycles.

The maximum value of the nonlinearity equals the peak value of the ripple current. There are several possible solutions to minimize the effect:

a. Decrease the value of the ripple current.

The peak value of the ripple current is inverse proportional to the switching frequency and the output filter inductance. Therefore, increase the switching frequency and the output filter inductance can effectively decrease the ripple current. Nevertheless, this solution will lead to more power consumption and a larger area.

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b. Apply an anti-aliasing filter at the input of the ADC to remove the ripple current signal before sampling.

The anti-aliasing filter limits the bandwidth of the ADC input signal. However, this anti-aliasing will introduce latency to the control loop, which degrades the stability. It can be effectively compensated in the digital domain, which is discussed in Section 3.5.1.

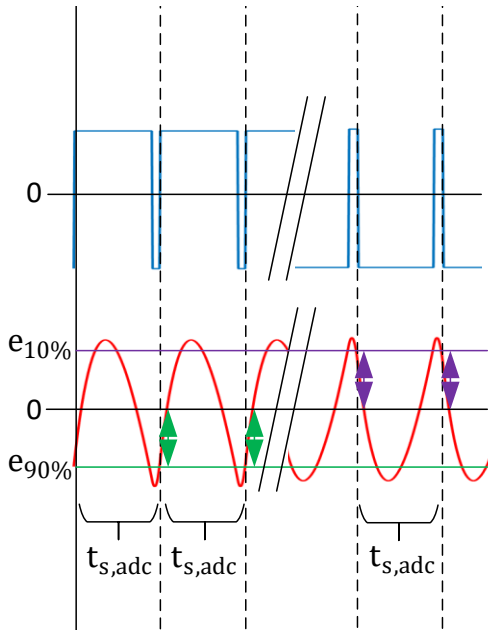


Figure 2.3 Ripple current and its sampled signal for a given duty cycle (Green: Error when the duty cycle is 90%, Purple: Error when the duty cycle is 10%. Red: Ripple current. Blue: PWM signal) (Sampling time $t_{s,adc}$)

2.2.3. Small-signal behavior

The design of the small-signal stability is one of the core works in this project. The power amplifier should be stable under the variation of load and output filter components. In this project, the plant contains the output filter C_f and L_f, the load L_m and R_m, the current sense resistor R_s, and the cable capacitance C_c. Ideally, the output current I_{out} is the current through the load. But the cable capacitance will affect the accuracy. It can be compensated by the techniques which are mentioned in Section 3.4.6. An equivalent model of the plant is demonstrated in Figure 2.4.

The transfer function of the plant $P(s) = \frac{I_{out}}{V_{in}}$ models the current through the current sense resistor I_{out} for each possible switching stage output voltage V_{in}. There are four poles and two zeros introduced by the plant P(s). The approximated symbolic equation of the poles and zeros are summarized in Table 2.1, and SLiCAP calculates the detailed symbolic transfer function.

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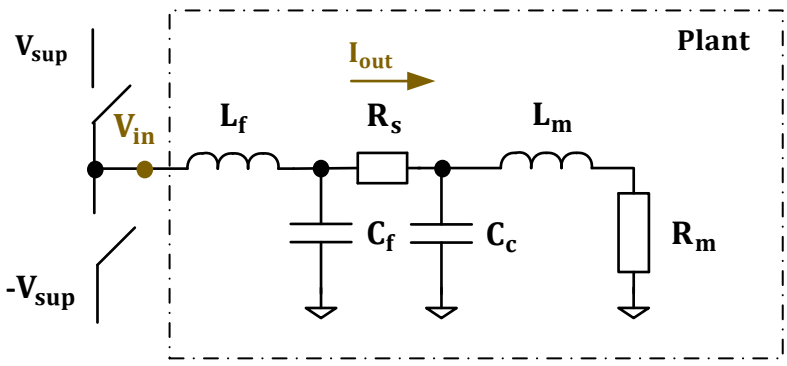


Figure 2.4 Equivalent circuit model of the plant

The pole and zeros of the plant P(s) will influence the small-signal behavior of the control loop. A digital plant compensator will be introduced to compensate them. Such a technique has been applied in [5], [6], and [13].

This topology is a model-based approach to the compensation of the poles and zeroes in P(s). As a result, the performance of the compensation is limited by the model of the plant.

Table 2.1 Estimation of poles and zeros in the transfer function of the plant

Pole(s)/ Zero(es)	**Real/Complex conjugate**	**Estimation frequency (Hz)**	**Condition**
Pole	Real	$p_1 = \frac{R_m + R_s}{L_m + L_f}\frac{1}{2\pi}$	$L_f + L_m >> C_c R_m R_s$
Poles	Conjugate pairs	$p_{2,3} = \frac{1}{2\pi\sqrt{L_f C_f}}$	$L_m >> L_f$
Pole	Real	$p_4 = \frac{1}{2\pi C_c R_s}$	$C_c << C_f$
Zeroes	Conjugate pairs	$z_{1,2} = \frac{1}{2\pi\sqrt{L_m C_c}}$	$L_m >> \frac{C_c R_m{}^2}{4}$

A block diagram of the digital plant compensator is shown in Figure 2.5. This system is assumed to be a discrete-time system. Therefore, the transfer functions are in the z domain.

Ideally, the transfer of the plant compensator $H_c(s)$ and the plant P(s) equals to 1. But in practice, due to the high complexity of P(s), $H_c(s)$ and P(s) can never have perfect cancellation. To relief the requirement of the plant compensator, it is preferable to investigate the possibility of decreasing the complexity of the plant.

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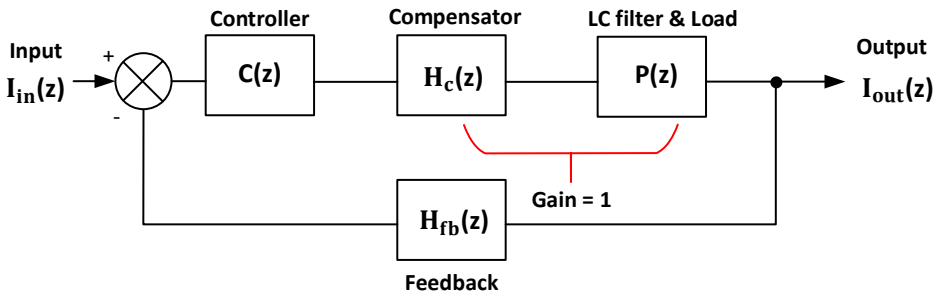


Figure 2.5 Equivalent model of the plant compensator and the plant

The complexity of the plant is related to the order of the plant. Various current sense techniques have been discussed in [7]-[11]. The following discussion will give a brief introduction to these techniques.

1. Current mode control

The nature of the switching stage is operating against the supply, which is equivalent to a voltage source. The current mode control converts the power amplifier into a voltage-controlled current source, as shown in Figure 2.6. It has been applied to many Switch Mode Power Converter (SMPC) applications. After applying the current mode control technique, the filter inductance ideally does not affect the control loop.

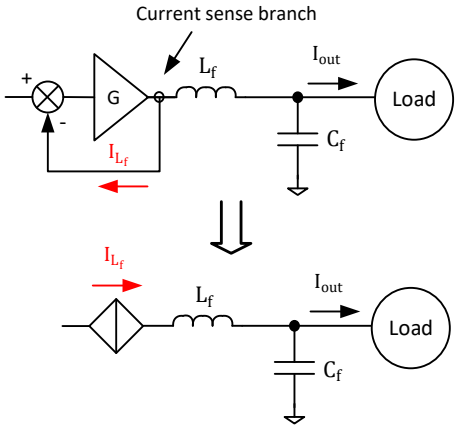


Figure 2.6 Equivalent model of the current mode control

However, the current mode scheme has some limitations:

a. The peak inductor current is not controlled. It will clip the circuit if the peak current is too large.

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b. Due to the poor regulation and sub-harmonics oscillation, the inductor current cannot be accurately controlled.

c. The common-mode voltage input of the current sense circuit is high, which requires high CMRR active components in the current sense circuit. Without a high CMRR current sense circuit, the nonlinearity at the output of the current sense circuit will be large.

Several methods exist for the first and second limitations to protect the circuit and compensate for the poor regulation and sub-harmonics oscillation. For example, a peak current mode control SMPC with slope compensation is proposed, and it does not have those two limitations [7]. For the third limitation, the large common-mode voltage can be avoided by sensing the current at the power supplies. However, the power supply current contains the shoot-through current signal, influencing the power amplifier's accuracy. A blanking circuit can be employed in many integrated circuits applications to reject the shoot-through [14]. The application for board-level circuits requires the power stage has a blanking circuit that currently does not exist.

2. Fixed ripple current self-oscillating control

In addition, self-oscillating fixed ripple current topology can effectively decrease the complexity of control loop design. Different from the fixed frequency amplifier with the current mode control, it has three advantages:

a. Its switching frequency decreases with output voltage excursion. Hence, switching loss will be less compared with the fixed frequency amplifier.

b. Because of the spread spectrum, the Electromagnetic Interference (EMI) spectrum of the self-oscillating amplifier is wider and will probably lower energy levels.

The self-oscillating amplifier whose operation is based on PWM modulation of a first-order oscillator, which have an oscillating frequency that drops with the output voltage excursion. The analog memory element in this topology is an inductor. The inductor is driven from a power stage with rail-to-rail drive capabilities, such as a half-bridge switching stage. Figure 2.7 shows the concept of a first-order hysteresis-based oscillator.

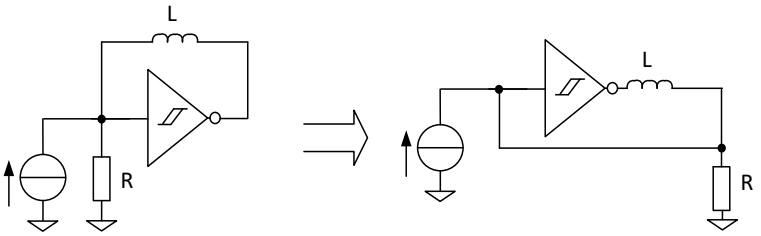


Figure 2.7 Top-level model of the first-order oscillator

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With a combination of the trans-impedance amplifier indicated in Figure 2.8, filter inductance and filter capacitance to the loop transfer is eliminated.

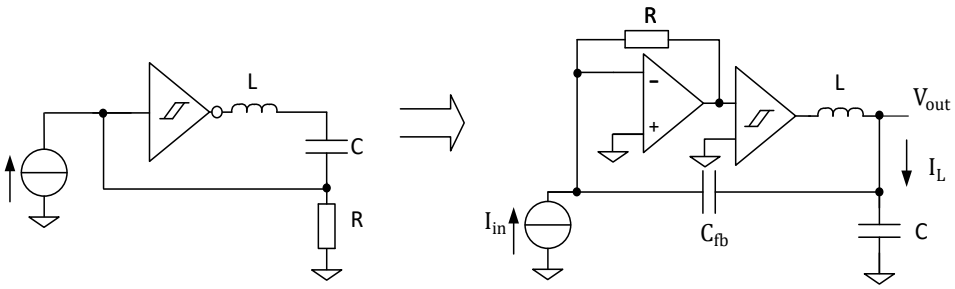


Figure 2.8 Top-level model of fixed ripple current module

Figure 2.8 shows the top level of the self-oscillating fixed ripple current trans-impedance amplifier. The trans-impedance gain from the input current I_{in} to V_{out} can be written as:

$$\frac{V_{out}}{I_{in}} = -\frac{1}{sC_{fb}} \tag{2.3}$$

In conclusion, the current mode control and the fixed ripple current self-oscillating control can effectively decrease the complexity of the control system design. Based on these topologies, four concepts are generated, and they will be further discussed and compared in Section 2.3 and Section 2.4.

2.2.4. Sampling

In this application, the effect of the sampling and quantization of the PWM signal must be considered. Pulse width modulation sampling is a term representing the type of modulation sampled that occurs in a pulse width modulator in the presence of a sampled input signal. The input signal must be sampled up to the PWM carrier frequency to match the sampling rate of the PWM signal with the input signal. This process can be modeled by adding a zero-order-hold block in series with the input signal that takes one sample for each PWM cycle, illustrated in Figure 2.9. It shows the equivalent model of uniform sampling. The PWM signal's frequency spectrum will fill up with harmonics of the modulating signal in this case. In other words, the sampling process will cause distortion.

The distortion caused by sampling can be dealt with in different ways. It can be corrected by approximating NPWM using a high or linear order interpolation filter [15]. In this application, the sample rate of the input signal is 20kHz, which requires an interpolation filter with a delay of $T_{filter} = \frac{2}{20000Hz} = 100\mu s$. The delay of the interpolation filter exceeds the source to load delay (12.5us) requirement, which can be found in Section 1.3. Therefore, it is unpractical to apply the linear order interpolation filter. An alternative is employing a Butterworth filter as

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an interpolation filter, which attenuates the distortion signal and contributes to the closed-loop response.

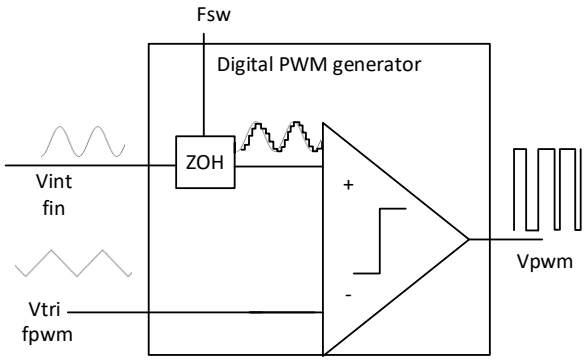


Figure 2.9 Equivalent model of the sampling effect

2.2.5. Quantization – Limited duty cycle

The quantization process of the digital PWM generator will lead to quantization error. For a digital PWM generator, the edges of the PWM signal can not be at random times but have to be synchronized to a high-frequency master clock. Consequently, the resolution of the duty cycle is limited by the master clock. Figure 2.10 elucidate the quantization effect in the time domain.

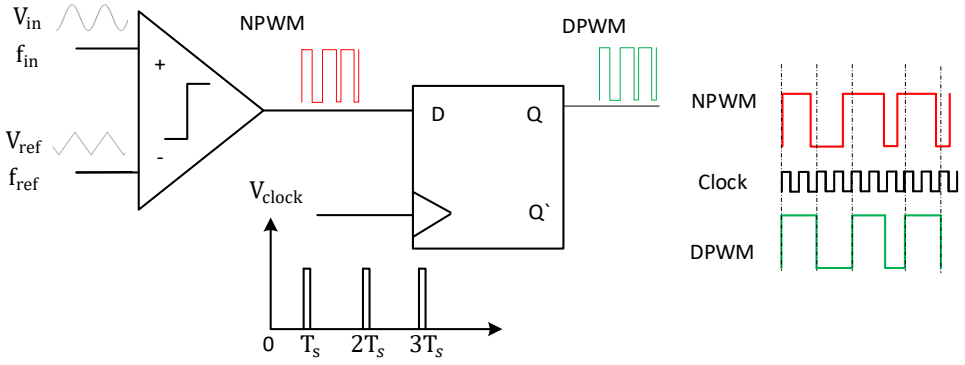


Figure 2.10 Elucidation of quantization of the duty cycle in the time domain

The quantization error manifests as noise in the PWM signal. Since quantization is a highly nonlinear process, the exact effect of quantization on the signal content and the quantization noise is hard to be measured. Several assumptions need to be made before introducing quantization noise and the quantizer into the linearization model: 1. The error sequence of the quantization noise N(z) is a stationary and random process. 2. The error sequence is

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uncorrelated with itself and with the input sequence X(z). 3. The probability density function of the quantization error is uniform over the range of quantization error. [16]

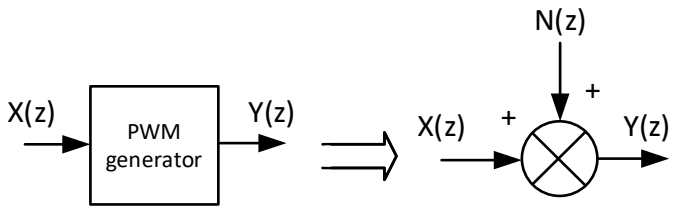


Figure 2.11 Small signal equivalent model of digital PWM generator (X(z): input signal. Y(z): output signal. N(z): noise signal

These assumptions allow the quantization process to be modeled as an additive white noise source depicted in Figure 2.11.

The conversion gain from the sample time T_s to an equivalent output noise voltage $V_{out.time}$ can be written as:

$$V_{out.time} = \frac{T_s}{T_{sw}} 2V_{sup} \tag{2.4}$$

The conversion gain from the sample time T_s to an equivalent input noise voltage $V_{in.time}$ can be found as:

$$V_{in.time} = \frac{T_s}{T_{sw}} \frac{2V_{sup}}{G} = \frac{T_s}{T_{sw}} \frac{V_{ref}}{V_{sup}} 2V_{sup} = T_s \frac{2V_{ref}}{T_{sw}} \tag{2.5}$$

where G is the gain of the power stage.

From this, the contribution of the time error to the spectrum of the total equivalent input noise voltage as:

$$S_{in,v} = S_{in,t} \left(\frac{2V_{ref}}{T_{sw}}\right)^2 \tag{2.6}$$

If the time error is equally distributed in the range of 0 to $\pm$Ts, its mean square error is $\frac{{T_s}^2}{3}$. Assuming a uniform spectrum of the quantization error up to $\frac{f_s}{2}$, the power spectral density of the quantization error can be obtained as:

$$S_{in,t} = \frac{{T_s}^2}{3} \frac{2}{f_s} \tag{2.7}$$

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Therefore, based on Eq 2.6 and Eq 2.7, the output referred current noise can be estimated due to this quantization process. Figure 2.12 illustrates the small-signal equivalent model of the PWM generator, power stage, and plant.

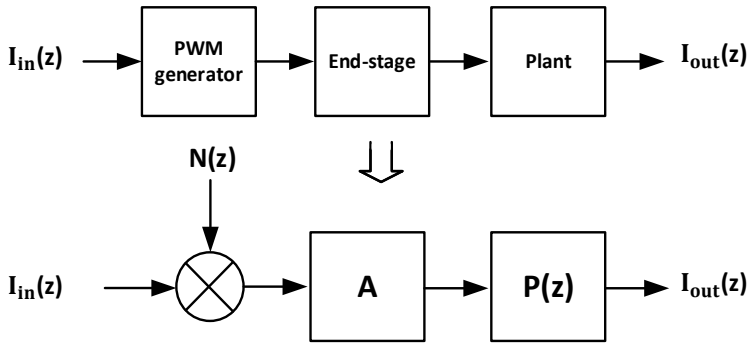


Figure 2.12 Small signal equivalent model of the digital PWM generator (only with quantization effect), power stage, and plant

Therefore, the output referred current noise due to this quantization process can be calculated by the noise transfer function (NTF):

$$\mathrm{NTF}\,(z) = \frac{I_{out}(n)}{N(n)} = AP(z) \tag{2.8}$$

Where A is the gain of the power stage, which equals to V_{sup} in the half-bridge concept.

The output referred current noise:

$$S_{out,i} = S_{in,v}\big(AP(z)\big)^2 = \frac{2}{3f_s^3}\left(\frac{2V_{tri}}{T_{sw}}V_{sup}P(z)\right)^2 \tag{2.9}$$

Where $A=V_{sup}$ is the gain of the power stage. When the frequency is equal to or less than 1 kHz, P(z) can be approximated as $\frac{1}{R_m+R_s}$. In the case of R_m = 50 Ω, R_s = 0.2 Ω, T_{sw}= 1 µs, V_{tri}=1 V, V_{sup}=32 V and maximum spectral density $\sqrt{S_{out,i}}$ = 26 $\mathrm{nA\sqrt{Hz}^{-1}}$. To meet the requirement of noise performance, the master clock rate needs to be increased to a larger frequency span. This technique is referred to as oversampling. The minimal oversample clock rate is calculated as:

$$f_s = \sqrt[3]{\frac{2\big(2V_{sup}V_{tri}\big)^2}{3S_{out,i}\big(T_{sw}(R_m+R_s)\big)^2}} = 1.17\ \mathrm{GHz} \tag{2.10}$$

According to Eq 2.10, a master clock of more than 1.17 GHz would be needed. This frequency is not achievable for the current FPGA master clock.

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There are several ways to increase the duty cycle resolution without applying extremely high frequency:

1. Dither

Applying a dithering converter at the digital PWM generator's output will help increase the resolution of the duty cycle, but it will introduce noise. There are some techniques to solve this problem [17], but it will require more design requirements.

2. Noise shaping.

The noise shaping technique can shape the noise spectrum. The Sigma-delta PWM topology effectively implements noise shaping ideas and has been widely used in many mix-signal audio amplifier applications [2]-[6].

The outline of the Sigma-delta PWM topology reduces the in-band quantization is as follows: 1. Measure the quantization error 2. Correct the error using negative feedback.

The effectiveness of the Sigma-delta PWM is dependent on the loop of the feedback network. Hence, modifying the loop is the core work to shape the noise. The small-signal equivalent model of the loop can be modeled as Figure 2.13. The loop consists of the controller C(z), the gain of the power stage A, the plant P(z), the feedback path $H_{fb}(z)$. The controller C(z) contains 1. The filter function in the forward loop shapes the noise, called a loop filter or noise shaper. 2. The plant compensator.

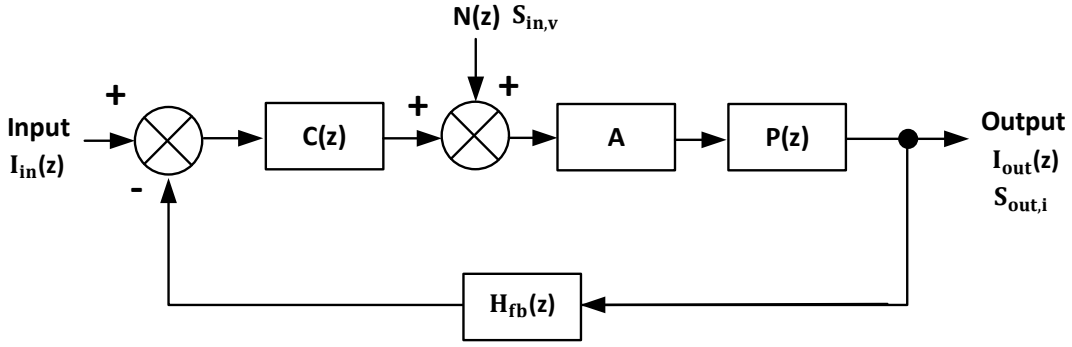


Figure 2.13 Block diagram of the digital power amplifier (Discrete-time system)

Figure 2.13 shows the small-signal equivalent model of the amplifier, where $H_c(z)$ is the transfer function of the controller, A is the gain of the power stage, P(z) is the transfer function of the plant and $H_{fb}(z)$ is the transfer function of the feedback network. In this case, the noise transfer function NTF (z) can be expressed as:

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$$\mathrm{NTF}\,(z) = \frac{I_{out}(z)}{N(z)} = \frac{AP(z)}{1 + AH_{fb}(z)C(z)P(z)} \tag{2.11}$$

Where $H_{fb} \approx 1$ at low frequency. It can be noticed that the transfer function of the controller will dominate the NTF, which will be referred to as noise shaper in the following sections.

With the feedback loop, the output referred current noise can be expressed as:

$$S_{out,i} = S_{in,v}\big(\mathrm{NTF}\,(z)\big)^2 \tag{2.12}$$

The noise shaper contributes to the noise performance and small-signal bandwidth since it is the controller. During the design phase, it is impossible to design the amplifier's noise performance and small-signal behavior. They will be considered and designed together.

2.2.6. Design consideration result

Based on Sections 2.2.1 to 2.2.5, the structure of the amplifier should fulfill the requirements as follows:

1. The controller of the amplifier must consist of the noise shaper and the plant compensator.
2. When the switching frequency is fixed, the sampling frequency of the ADC should be synchronized with the switching frequency.
3. A reconstruction filter should be applied to the input stage of the amplifier
4. An anti-aliasing filter needs to be applied in series with the input of the ADC.

As discussed in Section 2.2.3, the current mode control technique and the fixed ripple current self-oscillating technique are helpful to decrease the complexity of the controller. However, they will dramatically change the architecture of the amplifier. Therefore, they are classified as four different concepts. After modeling the concepts and verifying their feasibility, four concepts are discussed and compared in detail in Section 2.3 and Section 2.4.

Based on a comparison table (Table 2.6), the best concept is selected, which will become the top-level architecture of the digital amplifier. After determining the best concept, the noise budgets are discussed in Section 2.5. According to the noise budgets, several applicable ADCs are compared. In the end, the ADC for this application is selected and pre-ordered.

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2.3. Concepts

This section will compare their performance parallelly regarding noise, flexibility, accuracy, complexity, EMI, area, and cost. In the end, the best concept is selected based on Table 2.6. Chapter 3 will further develop it.

2.3.1. Fixed frequency voltage-mode control topology – Concept 1

Concept 1 is a fixed frequency current driver. Figure 2.14 shows its top-level block diagram.

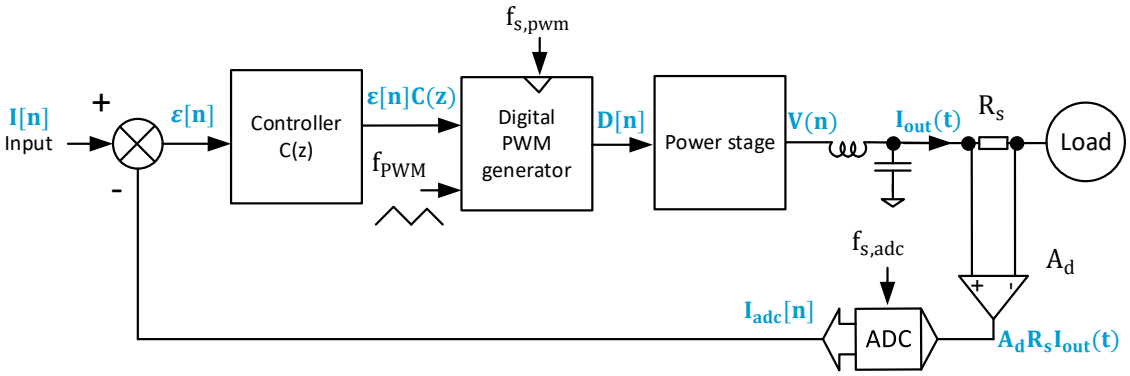


Figure 2.14 Fixed frequency digital power amplifier with voltage-mode control (Controller includes noise shaper and plant compensator)

In Figure 2.14, the ADC has a sampling frequency of $f_{s,adc}$, while the clock frequency of the PWM generator is $f_{s,PWM}$. The switching rate of the power stage equals f_{PWM}. The gain of the differential voltage amplifier is A_d.

The relation of the digital signal I[n] and its full-scale value $I_{fs}(t)$ can be expressed as:

$$I[n] = \frac{I_i(t)}{I_{fs}(t)} 2^N \tag{2.13}$$

Where $I_i(t)$ is the current input signal, $I_{fs}(t)$ is the full-scale value. N is the resolution of the signal.

This concept contains one current feedback loop. The current sense resistor Rs sense the output current signal. Then it is transferred to the voltage signal by a differential voltage amplifier with a gain of Ad. With an ADC in the feedback path, the voltage signal will be converted to the digital count signal I[n]. The digital compensation filter compensates the poles and zeroes in the plant in the controller. As discussed in Section 2.2.3, the model-based compensation will limit the performance of the amplifier. Concepts 2, 3, and 4 are the possible solutions for it. The discussion of Concept 1 is as the table below:

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Table 2.2 Discussion of Concept 1

Topic	Discussion
Noise	The output referred current noise of the amplifier is only determined by Rs, Ad, and the ADC, if the controller has the same property as a Nullor.
Flexibility	The parameters in the digital controller can be easily tuned to fulfill different requirements. This concept is highly flexible by tunning the parameters in the controller.
Accuracy	The feedback path determines the accuracy of the amplifier if the controller has the same property as a Nullor. By designing a high-accurate feedback path, the requirement of accuracy can be easily achieved.
Complexity	The complex point of this concept is the design of the digital compensation filter. This requires a very accurate model for the load and the output filter. If the model can not be accurately modeled, this concept requires an additional compensation circuit. The details of the compensation circuit are discussed in Section 3.4.6.
EMI	Since the switching frequency of this concept is fixed, it has a discrete spectrum. Therefore, this concept has a predictable EMI, which is easy to be analyzed.
Area	The area is small since it does not require any inner loop.
Cost	The following sections will further discuss this aspect.

2.3.2. Fixed frequency current mode control topology – Concept 2

Concept 2 uses an extra current feedback loop to reduce the order of the plant, as discussed in Section 2.2.3. A top-level model is presented in Figure 2.15.

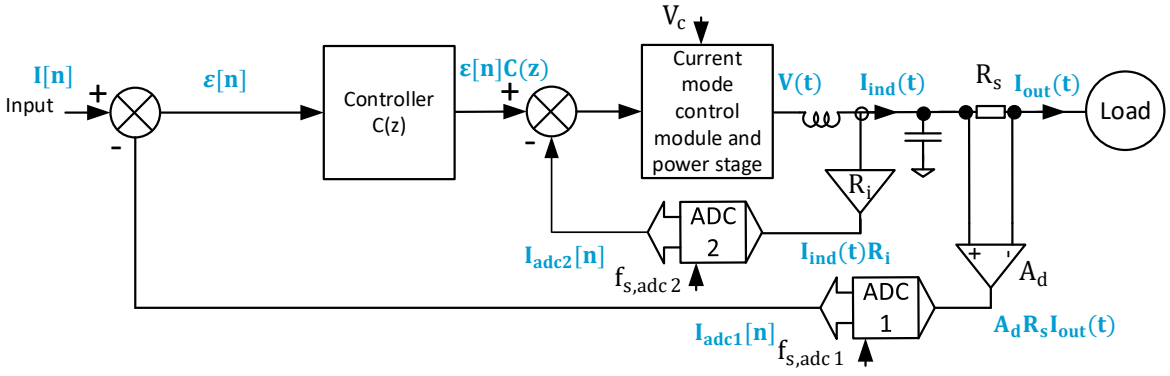


Figure 2.15 Digital power amplifier with the current mode control

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This concept requires:

1. An additional current sense circuit. Compared with the current sense circuit in the outer loop, its requirement for accuracy and noise is lower because the outer feedback loop can correct the error.

2. An additional ADC (ADC 2), the noise requirement of this ADC is lower than ADC1 since the control loop can suppress its noise. It requires a high sample rate to digitize without aliasing the ripple signal. However, its requirement for noise is low, as the outer feedback loop can correct the error.

The discussion of Concept 2 is as follows:

Table 2.3 Discussion of Concept 2

Topic	Discussion
Noise	According to the discussion in Section 2.3.1, the noise performance of concepts 1 and 2 are equal ideally.
Flexibility	The parameters in the digital controller can be easily tuned to fulfill different requirements. Compared with concept 1, the flexibility of concept 2 is at the same level.
Accuracy	The complex point of this concept is the design of the digital compensation filter and the current control module. As discussed in Section 2.2.3, the order of the plant can be decreased with one order by employing current mode control. Compared with Concept 1, the complexity of the compensation filter is lower. However, this concept gains more complexity in the current mode module design. Therefore, Concept 2 has a higher complexity compared with Concept 1.
Complexity	Compared with Concept 1, the area is larger since it requires an extra inner loop.
EMI	Since the switching frequency of this concept is fixed, it has a discrete spectrum. Therefore, this concept has a predictable EMI, which is easy to be analyzed.
Area	Compared with Concept 1, the area is larger since it requires an extra inner loop.
Cost	Compared with Concept 1, the cost is higher since it requires an extra inner loop.

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2.3.3. Self-oscillating fixed ripple current topology with analog inner loop – Concept 3

Concept 3 is a self-oscillating current driver with an analog ripple current control module, shown in Figure 2.16. The inner loop of the amplifier is in the analog domain. Since the controller is in the digital domain, the controller's output signal should be transferred to the analog domain via a DAC.

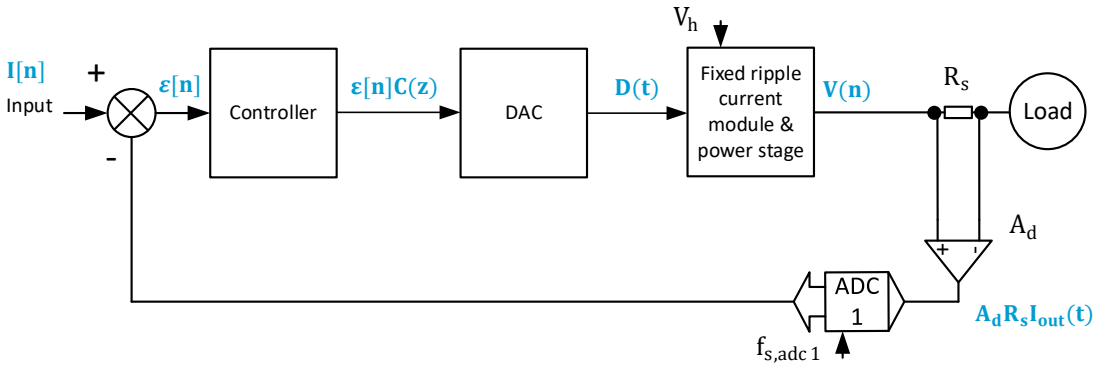


Figure 2.16 Fixed ripple current digital power amplifier with analog inner loop

Different from other concepts, this concept requires:

1. An analog fixed ripple current module. The details of the fixed ripple current module can be found in Section 2.2.3.

2. An additional DAC. The performance of this DAC is low because it is in the forward path of the control system. The negative feedback loop will reduce its artifact.

The discussion of Concept 3 is as follows:

Table 2.4 Discussion of Concept 3

Topic	Discussion
Noise	According to the discussion in Section 2.3.1, the noise performance of concepts 1, 2, and 3 are equal ideally.
Flexibility	The parameters in the digital controller can be easily tuned to fulfill different requirements. Concept 3 obtains more flexibility in its tunable fixed ripple current control module.
Accuracy	The complex point of this concept is the design of the digital compensation filter and the current control module. As discussed in Section 2.2.3, the order of the plant can be decreased with one order by employing current mode

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	control. Compared with Concept 1, the complexity of the compensation filter is lower. However, this concept gains more complexity in the current mode module design. Therefore, Concept 2 has a higher complexity compared with Concept 1.
Complexity	The complex point of this concept is the design of the digital compensation filter and the inner loop module. As discussed in Section 2.2.3, the order of the plant can be decreased with two orders by employing self-oscillating fixed ripple current control. Compared with Concepts 1 and 2, the complexity of the compensation filter is lower. Nevertheless, this concept gains more complexity in the inner loop design. The complexity can be regarded as the same after comparing the current mode control structure and the self-oscillating fixed ripple current control. Therefore, Concept 3 has a lower complexity compare with Concept 2.
EMI	Because of the spread spectrum, the Electromagnetic Interference (EMI) spectrum of the self-oscillating concepts is wider and will probably have lower energy levels than fixed-frequency concepts.
Area	Compared with Concept 1, the area is larger since it requires an extra inner loop.
Cost	Compared with Concept 1, the cost is higher since it requires an extra inner loop.

2.3.4. Self-oscillating fixed ripple current topology with digital inner loop – Concept 4

Concept 4 is the self-oscillating current driver with a digital ripple current control module.

Different from other concepts, this concept requires:

1. A digital ripple current module in the FPGA.

2. An additional ADC (ADC 2), the noise requirement of this ADC is lower than ADC1 since the control loop can suppress its noise. It requires a high sample rate to catch the ripple signal. However, its requirement for noise is low, as the outer feedback loop can correct the error.

3. An additional current sense circuit. It converts the ripple current signal to the ADC. Compared with the current sense circuit in the outer loop, its requirement for accuracy and noise is lower since the outer feedback loop can correct the error.

The discussion of Concept 4 is as follows:

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Table 2.5 Discussion of Concept 4

Topic	Discussion
Noise	According to the discussion in Section 2.3.1, the noise performance of concepts 1, 2, 3, and 4 are equal ideally.
Flexibility	The parameters in the digital controller can easily be tuned to fulfill different requirements. Concept 4 obtains more flexibility in its tunable fixed ripple current control module. Compared with Concept 3, this concept can even operate in fixed frequency mode by adjusting the module in the digital domain.
Accuracy	The complex point of this concept is the design of the digital compensation filter and the current control module. As discussed in Section 2.3.1, the order of the plant can be decreased with one order by employing current mode control. Compared with Concept 1, the complexity of the compensation filter is lower. However, this concept gains more complexity in the current mode module design. Therefore, Concept 2 has a higher complexity compared with Concept 1.
Complexity	Compared with Concept 3, it converts the complexity of the analog design to the digital design. Therefore, its complexity is relatively lower than Concept 4.
EMI	Because of the spread spectrum, the Electromagnetic Interference (EMI) spectrum of the self-oscillating concepts is wider and will probably have lower energy levels than fixed-frequency concepts.
Area	Compared with Concept 1, the area is larger since it requires an extra inner loop.
Cost	Compared with Concept 1, the cost is higher since it requires an extra inner loop.

2.4. Concept discussion and selection

Table 2.6 lists the score of all concepts in terms of different design aspects. Consequently, Concept 1 obtains the highest score.

Table 2.6 Digital power amplifier concepts comparison table

Design Aspect	**Weighted**	**Concept 1**	**Concept 2**	**Concept 3**	**Concept 4**
Low noise	2	0	0	0	0

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High flexibility	1	0	0	0	0
Low complexity	1	0	-	-	0
High accuracy	2	0	0	0	0
Predictable EMI (i)	1	+	0	-	-
Small area	1	0	-	-	-
Low cost	1	0	-	-	-
Score (ii)	/	+	---	----	---

All concepts can employ the cable capacitance compensation circuit. It is discussed in Section 3.4.6.

There are several reasons:

Firstly, Concept 1 can fulfill the requirements of the small-signal stability with the additional cable capacitance compensation module.

Secondly, the area and the cost of this concept is relatively smaller.

Thirdly, this concept has a fixed frequency switching scheme, which results in a known EMI.

In conclusion, Concept 1 is selected as the best concept of this assignment. It will be designed and developed in the following chapter.

2.5. Distribution of error budgets for selected concept

After determining the best concept, the applicable ADC should be selected and pre-ordered. Before that, the budget of the noise of the ADC needs to be designed.

The equivalent noise model of the digital power amplifier is presented in Figure 2.17.

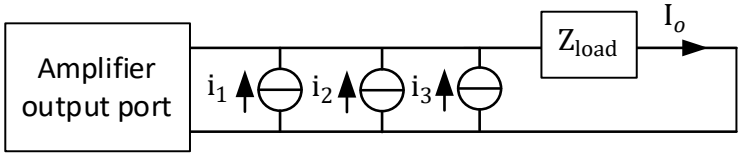


Figure 2.17 Top-level noise model of the amplifier

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The noise sources are:

1. i1: Equivalent output referred current noise of the current amplifier which contributes by the current sense circuit (Include R_{sense}). Its spectral density is represented by S_{i1} $[A^2Hz^{-1}]$
2. i2: Equivalent output referred current noise of the current amplifier contributes by the ADC. Its spectral density is represented by S_{i2} $[A^2Hz^{-1}]$
3. i3: Equivalent output referred current noise of the current amplifier, which contributes by the time quantization error from the digital PWM generator. Its spectral density is represented by S_{i3} $[A^2Hz^{-1}]$.

After a short component study, the following budget is assumed in Table 2.7. The component study shows that the noise level of the amplifier can achieve an output referred current noise of 22.64 nA/$\sqrt{\text{Hz}}$.

Table 2.7 Noise budget of the current driver

Noise source	**Budget of output referred current noise ($nA/\sqrt{Hz}$)**
i1	12
i2	15
i3	12
∑	22.64

Apart from the noise performance of the ADC, its latency directly relates to the control loop's stability. Besides, it is also related to the acquisition circuit structure, as some ADCs need a front-end amplifier to drive them. Several high-performance ADCs are compared in this section, and the best option is selected based on Table 2.8.

The requirements of the ADC:

1. Maximum delay 1.5us (With communication)
2. Easy drive (Less noise, complexity, and delay)
3. Maximum noise current density: 15 $nA/\sqrt{Hz}$

Table 2.8 ADC performance table

ADC	**Delay**	**Easy Drive?**	**Noise power****	**Output referred noise current density*****	**Sample rate**	**Price (1000+)**
AD4630	0.5us	Easy drive	17.7Vrms	10.6 $nA/\sqrt{Hz}$	2MSPS	$30.95
LTC2378-20	1us	Need extra drive	21.9Vrms	18.0 $nA/\sqrt{Hz}$	1MSPS	$33.93

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LTC2380-24	2us	Need extra drive	16.6Vrms	10.3 $nA/\sqrt{Hz}$	2MSPS	$36.75
AD7134	1.1us*	Easy drive	16.01Vrms	13 $nA/\sqrt{Hz}$	1MSPS	$17.85

*The ADC is operating at maximum Over Sample Rate (OSR).

** The noise specifications quantify the noise of the ADC itself, including aliasing, but the input signal is assumed noiseless.

*** Assume the input signal of the ADC is noiseless, the output referred current noise of the total ADC RMS noise can be expressed by:

$$\sqrt{S_{i3a}} = \frac{V_{n,rms}}{\sqrt{0.5 f_s}} {G_{cs}}^{-1} \tag{2.14}$$

Where $V_{rms,noise}$ is the total RMS noise voltage of the ADC, f_s is the sampling speed of the ADC and G_{cs} is the gain factor of the current sense current (Unit: V/I).

The gain factor of the current sense circuit is given by:

$$G_{cs} = \frac{V_{ADC,max}}{I_{max} + \sigma_{headroom}} \tag{2.15}$$

Where $V_{ADC,max}$ is the maximum differential input voltage of the ADC and I_{max} is the maximum current. Besides, σ_{margin} is the headroom, allowing the ADC to process the correct value still if the load current exceeds its maximum value. The noise is calculated by: $V_{ADC,max}$ = 5 V, I_{max} = 3 A, $\sigma_{headroom}$ = 0.1 A.

AD4630 is selected as the best solution for this assignment. Compared with other ADCs, it has several advantages: 1. It has the lowest latency. 2. It does not need the front-end stage. 3. It has the lowest output referred current noise.

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3. Detailed design

The outline of the detailed design procedure is:

1. Interpolate the required specifications and design considerations in Section 1.3 and Section 2.2.
2. Design the power stage and select the components to meet the power efficiency requirements.
3. Discuss the drive capability of the amplifier and design the current and voltage protection circuits.
4. Design the frequency compensation module to increase the stability of the amplifier if the amplifier is unstable.
5. Design the acquisition board, which contains signal sense circuits.

3.1. Summary of specifications

1) Functional requirements

I. Input and output impedance

The type of the amplifier is the current amplifier, its input impedance needs to be considered as zero, and the output impedance needs to be a proper value.

The minimal output impedance of the amplifier can be calculated from the static gain error and the load impedance, which follows Eq 2.16.

$$Static\ gain\ error\ (\%) = \frac{Z_{out} // Z_{load} - Z_{load}}{Z_{load}} \tag{2.16}$$

Where Static gain error is 0.5 %.

When the load impedance Z_{load} equals to its largest resistance value (50 Ω), the output impedance should be at the largest value, which equals 10 $k\Omega$.

II. Source to load transfer

The gain of the current amplifier is determined by the full-scale value of the ADC input.

2) Performance requirements

The performance requirements of the amplifier can be found in Table 1.1.

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3) Cost factors

The cost factor of the amplifier can be found in Section 1.3.

4) Operating conditions

Temperature range

Typical value 45 degree

EMI, ESD

It does not specify the required specifications.

3.2. Design of power stage

This section discusses the design of the power stage. Firstly, the maximum dissipation of the power stage is estimated. Secondly, the gate drivers and powerFETs are determined based on their FOM. Thirdly, the switching frequency is determined based on the losses equations and the component's datasheet. The fourth section presents the design of the output filter. The last section presents the consideration of the current sense resistor.

3.2.1. Estimation of maximum dissipation

In this assignment, the amplifier is designed as a full-bridge amplifier. There are the following reasons: 1. The loop gain in the current control loop is twice as large as the half-bridge design. 2. The full-bridge designs do not suffer power supply bus pumping with poorly designed switching amps. Although it will increase the complexity of the plant, the area, and the cost, it is acceptable for this project. An equivalent model of the full-bridge design in shown in Figure 3.1.

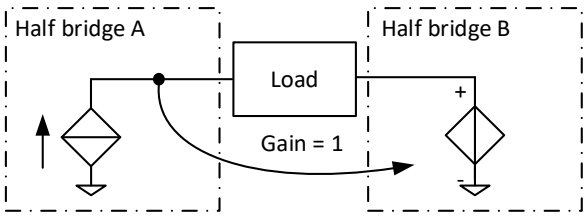


Figure 3.1 Equivalent model of the full-bridge concept

With the full-bridge design, the minimum power efficiency of the amplifier is 80%, which is calculated for: R_m = 5.5 Ω and I_{load} = 3 A. In this situation, the amplifier's output power is 50 W, and the maximum dissipation of the amplifier is calculated as 12.5 W.

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3.2.2. Selection of powerFETs and gate drivers

We proposed two figures of merit (FOM) for the component selection.

The requirements of the powerFETs consist: 1. Low cost. 2. Small size. 3. Low dissipation. Based on the requirement, the FOM for the powerFETs is designed as:

$$FOM_{fet} = \frac{P_{max}}{Q_{price,fet} A_{area,fet} P_{dis,fet}} \tag{2.17}$$

Where P_{max} is the maximum output power of the amplifier, $Q_{price,fets}$ is the price of the powerFET, $A_{area,fet}$ is the area of the powerFET and $P_{dis,fet}$ is the dissipation of the powerFETs.

The FOM for the gate drivers selection:

$$FOM_{dri} = \frac{1}{T_{c,dri} A_{area,dri} Q_{price,dri}} \tag{2.18}$$

Where $T_{c,dri}$ is the time delay of the gate drivers, $Q_{price,dri}$ is the price of the gate drivers, $A_{area,fet}$ is the area of the gate driver.

The dissipations related to the power FETs and the gate drivers are listed in Table 3.1. After comparing different powerFETs and gate drivers, the powerFET is selected as EPC2019, and the gate driver is selected as LMG1210RVRT.

3.2.3. Design of switching frequency

The maximum switching frequency is related to the MOS losses in Table 3.1.

Table 3.1 Power Losses in the power stage

Symbol	Description	Expression
P_c	MOS conduction losses	$P_c = 2I_{load}^2 R_{ds,on} \frac{T_{pwm} - 2t_d}{T_{pwm}}$
P_o	MOS output charge losses	$P_c = 16V_{sup}^2 C_{oss} f_{pwm}$
P_d	MOS body diode losses	$P_d = 2I_{load} V_F \frac{t_d}{T_{pwm}}$
P_s	MOS transition losses	$P_s = \frac{8}{3} t_s V_{sup} I_{load} f_{pwm}$
P_g	MOS gate-drive losses	$P_g = 4C_{iss} V_G^2 f_{pwm}$
P_{fets}	Sum of the losses in this table	

Where T_{pwm} is the cycle time of the power stage switching period and V_F is forward voltage through body diode is expressed as:

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$$V_F = \frac{kT}{q} \ln\left(\frac{I_{load}}{I_s}\right) \tag{2.19}$$

Based on the datasheet of the selected powerFETs and gate drivers, the losses in Table 3.1 are calculated for: drain-source on resistance $R_{ds,on} = 10$ mΩ, output capacitance $C_{oss} = 150$ pF, input capacitance $C_{iss} = 270$ pF, the switching time $t_s = 10$ ns, dead time $t_s = 11$ ns supply voltage $V_{sup} = 32$ V, $I_{load} = 3$ A. The maximum losses happen if the maximum current is delivered to the short load.

The maximum switching frequency can be calculated as:

$$f_{pwm} < \frac{P_{fets} - P_c}{16V_{sup}^2 C_{oss} + \frac{8}{3} t_s V_{sup} I_{load} + 2I_{load} V_F t_d + 4C_{iss} V_G^2} \tag{2.20}$$

Where P_{fets} is the budget of the dissipation. According to the component study, the maximum P_{fets} is assigned as 6.5 W and the maximum switching frequency is 1.0845 MHz. In the end, the switching frequency is selected as 1 MHz for easier calculation in the following design.

3.2.4. Design of output filter

Two factors need to be considered to design the output filter:

1. Corner frequency
2. The damping factor of the poles

The filter inductance and capacitance determine the corner frequency of the output filter. Since the output filter needs to attenuate the switching signal, the higher bound corner frequency is limited by the switching frequency. The input signal and amplifier bandwidth limit the lower bound.

The corner frequency is designed as a factor of 10 lower than the switching frequency. The output filter can filter high-frequency components efficiently with this frequency and does not significantly impact the control loop.

The output filter needs to be damped. There are two reasons: 1. Damping the filter can suppress the ringing of its output voltage. 2. The plant compensator is easier to compensate the poles which are introduced by the output filter.

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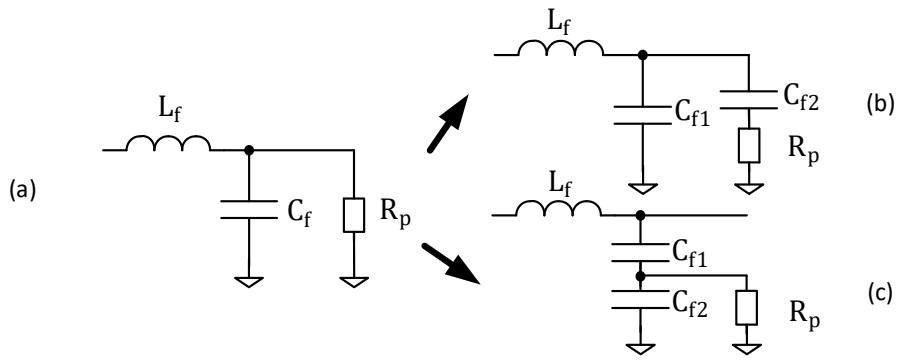


Figure 3.2 Equivalent model of the damped filter

There are several ways to damp the output filters, as shown in Figure 3.2. Figure 3.2 (a) shows that the output filter is damped by adding a parallel resistor R_p with the filter capacitor C_f. The quality factor of the filter equals to $Q_{filter,a} = \omega_{cutoff} C_f R_p$, where ω_{cutoff} is the cut off angular frequency of the output filter. To minimize the DC power loss of R_p, an additional resistor C_{f2} can be employed in series with R_p. Figure 3.2 (b) and Figure 3.2 (c) show two equivalent models for this approach. There also exists an active damping technique to avoid any power consumption. It can be realized by implementing an active R_p with an inner loop. But it will increase the cost and complexity of the circuit, which will not be considered as an attractive approach in this application.

The proposed passive damping output filter is presented in Figure 3.3. The filter inductance L_f is selected as 4.7 µF, the filter capacitances C_{f1} and C_{f2} are selected as 2.2 µF and 470 nF respectively, the damping resistor R_f is selected as 2.2 kΩ. The maximum losses of the inductors and damping resistor occur if the duty cycle is 50%. In this case, the maximum losses in the output inductor P_{Lf} are 2.3 W and the maximum loss in damping resistor P_f is 0.397 W.

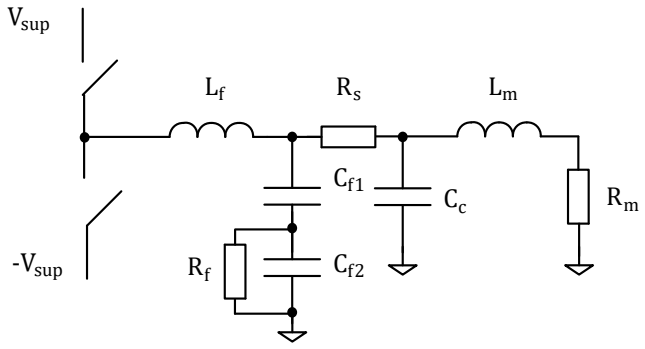


Figure 3.3 Plant of the load with the passive damped output filter

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3.2.5. Determine the maximum value of the current sense resistor

In the end, the maximum impedance of the current sense resistor can be calculated as 0.367 Ω, which is calculated by:

$$R_s \leq \frac{P_{Rs}}{I_{max}^2} = \frac{P_{totdis} - P_{fets} - P_i - P_{Rd}}{I_{max}^2} = 0.367\ \Omega \tag{2.21}$$

Where I_{max} is the maximum value of the load current 3 A.

The minimum value of the current sense resistor is limited by the noise requirement of the amplifier, which will be discussed in Section 3.4.1.

3.3. Design of static and dynamic drive capability

The amplifier needs protection currents to limit the maximum output current and voltage. This section will focus on the design of the protection circuits.

3.3.1. Current drive capability

One concept of the current protection circuit is shown in Figure 3.4. The current protection circuit measures the current flow from the supply to the power stage. Once the current exceeds its threshold value, the whole circuit will turn off to prevent any damage in the circuit. The maximum current through the load is $\frac{2V_{sup}}{R_m}$, Where the R_m is the load resistance. The circuit can procedure a current higher than 3A if the load resistance is lower than 21.3 Ω.

There are two possible cases that the output current may exceed the limitation of the components: 1. The switches are conducting at the same time. 2. Start-up phase (The phase that the circuit just starts to work).

Therefore, it is important to add protection circuits to limit the current drive capability. The topology of the overcurrent protection circuit is demonstrated in Fig 3.3. It prevents the current through the power supply from going above the designed value.

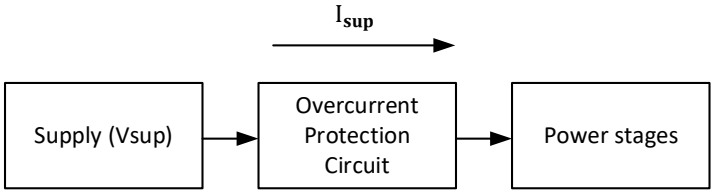


Figure 3.4 Block diagram of the overcurrent protection circuit

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3.3.2. Voltage drive capability

The circuit needs an overvoltage protection circuit to limit the overshoot voltage produced by the power stage. It can be designed with only two Transient Voltage Suppressors (TVS) to react to sudden or momentary overvoltage conditions. This topology is presented in Figure 3.5. Its design consideration can be found in [18].

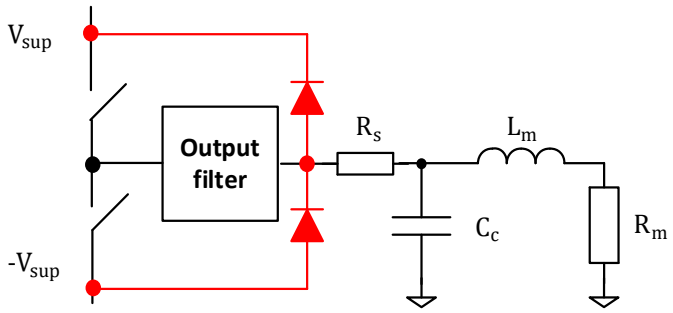


Figure 3.5 Plant of the load with overvoltage protection circuit (Red zone)

3.4. Design of controller

This chapter presents the design details of the controller. Firstly, the feasibility of the noise specifications is discussed based on Table 2.7. Secondly, the design equations and the architecture of the noise shaper are introduced. In the end, the digital limiters in the control loop for large-signal stability are illustrated.

3.4.1. Feasibility of noise specifications

In this section, the noise budgets in Table 2.7 are discussed and calculated. The first section introduces the equivalent model of the current sense circuit and calculates its noise performance. The operational amplifiers and the feedback resistors in the current sense circuit are selected based on the calculations. The second section illustrates the noise which contributes by the ADC. The third section discusses the quantization noise due to the limited duty cycle.

3.4.1.1. Noise of the current sense circuit

The top-level schematic design of the current sense circuit is demonstrated in Figure 3.6. A differential voltage amplifier transfers and amplifies the current through the current sense resistor Rs. The common-mode voltage is filtered by the digital isolator, which is at the output of the ADC. The differential voltage gain of the current sense circuit equals to $\frac{2R_2+R_1}{R_1}$.

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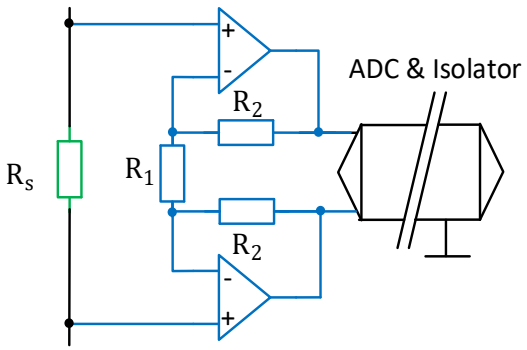


Figure 3.6 Equivalent model of the current sense circuit

With the schematic of the current sense circuit, its equivalent noise model is presented in Figure 3.7.

With the noise model, the output referred current noise of the current sense circuit is determined by:

$$S_{i1} = \frac{4kT}{R_{sense}} + \left(2S_{V_{eq}} + 0.25S_{Ieq}\left(R_{sense} + \frac{R_1 2R_2}{R_1 + 2R_2}\right)^2 + 4kT\frac{R_1 2R_2}{R_1 + 2R_2}\right)\left(\frac{1}{R_{sense}}\right)^2 \quad (2.22)$$

The current sense resistor is determined as 0.2 Ω. The operational amplifier is selected as ADA4898.

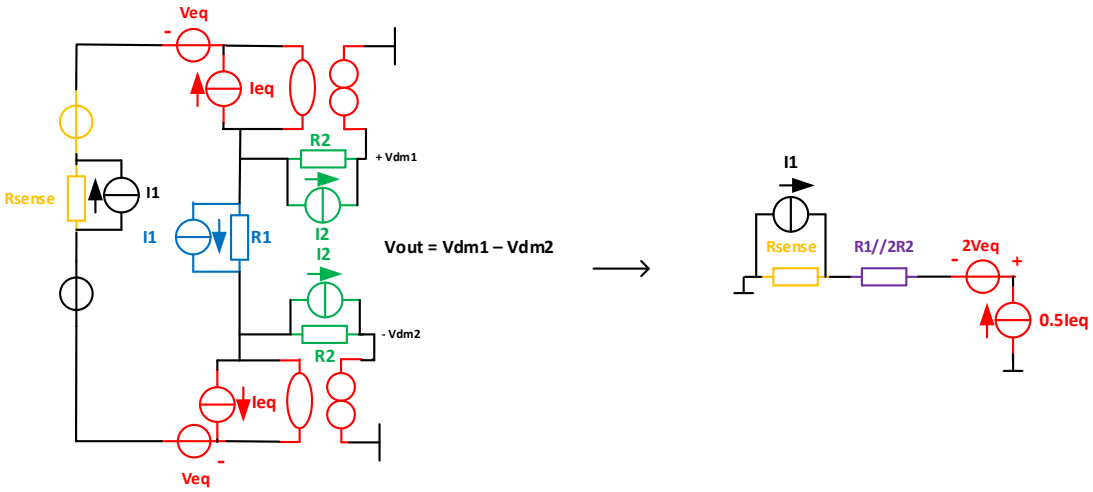


Figure 3.7 Equivalent noise model of the current sense circuit

Figure 3.8 shows the input-referred current noise and the output current of the current sense circuit versus R_1. The noise is calculated by: $R_{sense} = 0.2\Omega$, $R_2 = 0.5(\frac{V_{ADC,max}}{I_{max}+\sigma_{headroom}} - R_1)$, $T =$

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318 K. The output current is calculated by: $\frac{V_{ADC,max}}{R_1+2R_2}$. If the headroom of the input-referred current noise of the current sense circuit is 4.02 $\boldsymbol{nA/\sqrt{Hz}}$, R1 should be smaller than 121 Ω.

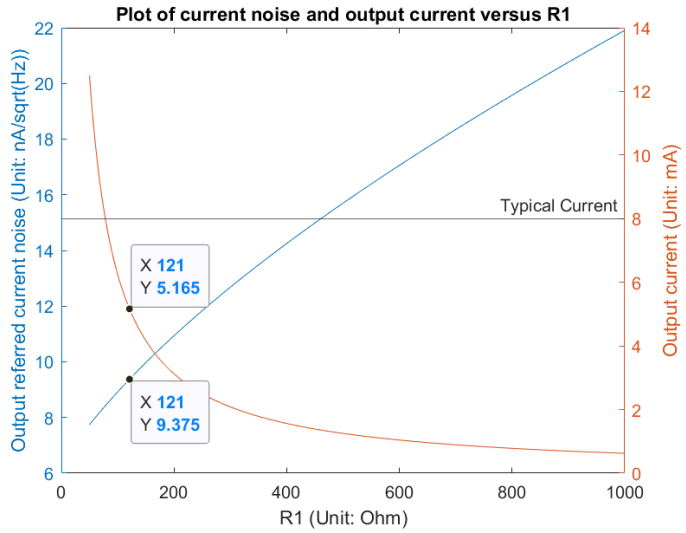


Figure 3.8 Plot of current noise and output current versus R1

3.4.1.2. Noise of the ADC

1. Noise of the ADC without noise aliasing

As discussed in Section 2.5, the output referred current noise of the digital power amplifier, which the ADC contributes is 10.6 nA/$\sqrt{\text{Hz}}$.

2. Noise of the ADC with noise aliasing

The RMS noise of the ADC in its datasheet has the precondition that the input signal is noise-less. After considering the noise from the front stage of the ADC, the ADC noise contribution to the spectrum of the total equivalent output current noise can be found as:

$$S_{i2} = S_{i2a} + S_{i2b} \tag{2.23}$$

where S_{i2a} is the contribution from the noise indicated in ADC's datasheet and S_{i2b} is the contribution from the noise comprises in the input signal of the ADC.

S_{i2b} can be calculated by:

$$S_{i2b} = \frac{V_{n,ADCin}^2}{0.5f_s} G_{cs}{}^{-2} \tag{2.24}$$

Where $V_{n,ADCin}$ is the input-referred RMS noise voltage of the ADC. It is calculated by:

$$V_{n,ADCin} = \sqrt{S_{n,ADCin}}\sqrt{NBW} \tag{2.25}$$

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Where $S_{n,ADCin}$ the input-referred noise voltage of the ADC and NBW is the bandwidth of the ADC input signal. The antialiasing filter can limit the bandwidth.

According to the noise budget of the ADC, the total RMS noise voltage at the input of the ADC should be smaller than 10.6uV.

3.4.1.3. Noise of the digital PWM generator

As discussed in Section 2.2.5, the output referred current noise as the noise generated by the digital PWM generator follows Eq 2.9. It is determined by the clock rate of the digital PWM generator and the NTF. This section is focused on determining the clock rate of the PWM generator and NTF.

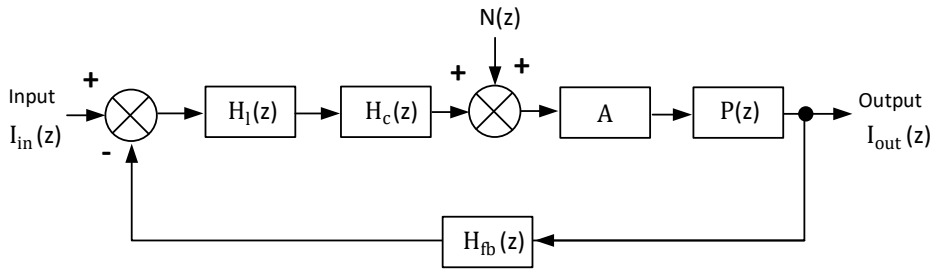


Figure 3.9 Equivalent model of the current driver

Figure 3.9 shows an equivalent linear model of the current driver. There are two assumptions at the start point to analyze NTF (NTF = $\frac{I_{out}(z)}{N(z)}$):

1. The plant compensator $H_c(z)$ can perfectly cancel the poles and zeroes in the plant $P(z)$, which makes $H_c(z)P(z) = 1$ at the band of the interest.
2. The gain of the feedback path $H_{fb}(z) = 1$ at the band of interest.

Therefore, the digital PWM generator contribution $\sqrt{S_{i3}}$ to the current noise of the total equivalent output current noise can be found as:

$$\sqrt{S_{i3}} = \sqrt{\frac{2}{3f_s^3}\left(\frac{2V_{ref}}{T_{sw}}\right)^2}\, NTF \approx \sqrt{\frac{2}{3f_s^3}\left(\frac{2V_{ref}}{T_{sw}}\right)^2}\frac{AP(z)}{1+AH_l(z)} \leq \sqrt{\frac{2}{3f_s^3}\left(\frac{2V_{ref}}{T_{sw}}\right)^2}\frac{AP_{max}(z)}{1+AH_{l,min}(z)} \qquad (2.26)$$

To meet the noise requirement, the magnitude of NTF should always be below its maximum value. Based on the discussion in Section 2.2.3, AP(z) can be modeled as a single-pole transfer function in the frequency range of 0 to 1kHz. $H_l(z)$ is the transfer to be designed. Assumed it is a roll-off function, the minimum value is determined when AP(z) is at its maximum value.

$$F_{max,f=1kHz}(R_m, L_m, z) = P_{max,f=1kHz}(R_m, L_m, z) \qquad (2.27)$$

Therefore, the minimum value of the noise shaper at 1kHz can be determined. The required $H_l(z)$ at the different master clock rates are summarized in **Error! Reference source not found.**. I

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t is one of the key requirements that the noise shaper needs to fulfill. After a short mathematic calculation, 128 MHz is selected as the clock frequency of the digital PWM generator. The details of its advantage and disadvantage are discussed in Section 5.2.

3.4.2. Noise shaper design

The noise shaper is the key module for the dynamic behavior and nonlinear behavior of the whole amplifier. The design flow for the noise shaper design progress contains three steps:

1. Design the continuous-time transfer function.

2. Determine the discrete-time transfer function.

3. Realize the discrete-time filter architecture based on its transfer function.

The design of the poles and zeros will be analyzed in the s domain, and the structure's design will be analyzed in the z domain.

There is one requirement for the minimum gain of the noise shaper when the sampling rate of the digital PWM generator is 128 MHz:

1. 54.71 dB at 1000 Hz. (From the requirement of noise shaper minimum gain)

The unity gain frequency of the closed-loop transfer function has two boundaries. The lower bound is limited by the source-to-load delay of the amplifier, while the latency limits the higher bound in the feedback path. Therefore, the desired range of the unity gain frequency is located in the range of 20kHz to 100kHz.

Assumed the unity gain frequency is 100kHz to obtain the highest loop gain at low frequency.

Table 3.2 Gain of the noise shaper with different orders

Order*	Loop gain at 1 kHz	Loop gain at 100 Hz
1	40dB	60dB
2	80dB	120dB
3	120dB	240dB

*The noise shaper is assumed as a chain of integrators. The order of the noise shaper equals the number of the integrators.

According to Table 3.2, it can be noticed that the first-order noise shaper is not applicable for this project. The order of the noise shaper should be at least second order. Compared with the

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second-order noise shaper, the third-order noise shaper will be a preferable solution. It results in a higher loop gain at low frequency and no steady-state error for a parabolic response.

Therefore, the order of the noise shaper is determined as three. The poles of the noise shaper prefer to be placed at 0 to obtain a maximum loop gain at low frequency.

In this assignment, the small-signal stability is analyzed with the phase and gain margin of the loop transfer. The Nyquist plot will be applied to prove the stability of the control loop.

The design of the noise shaper should take into account that the total phase shift of the loop will exceed 270°, which results in an unstable system. Hence, the design of the high order noise shaper should be designed in such a way that it shows a high-order behavior at low frequencies while turning back to a first-order response near the passing of the unity loop gain. Implementing zeroes in the noise shaper will be an option to stabilize the system.

Otherwise, adding zeroes (phantom zeroes) in the feedback loop can be another option to stabilize the system. In the digital system, add zeroes in the feedback loop will differentiate the output signal of the ADC, which may result in an excess signal at the output of the feedback path and requires a larger capability swing for the noise shaper input.

Adding the zeroes into the noise shaper is one of the solutions to obtain a stable system. The phase of the noise shaper is designed as a larger value which is 180 degrees.

$$H_l(s) = \frac{s^2 + 2\zeta\omega_0 s + \omega_0^2}{s^3\omega_0^2} \tag{2.28}$$

Where ω_0 is the natural angular frequency of zeros, and ζ is the damping ratio of the designed zeroes.

When the noise shaper is implemented Where $\arctan\left(\frac{2\zeta\frac{\omega}{\omega_0}}{1-\frac{\omega}{\omega_0}}\right)$ should be larger than 90 degrees to achieve a stable system. The system's damping factor and phase margin positively correlate with the step response's overshoot percentage.

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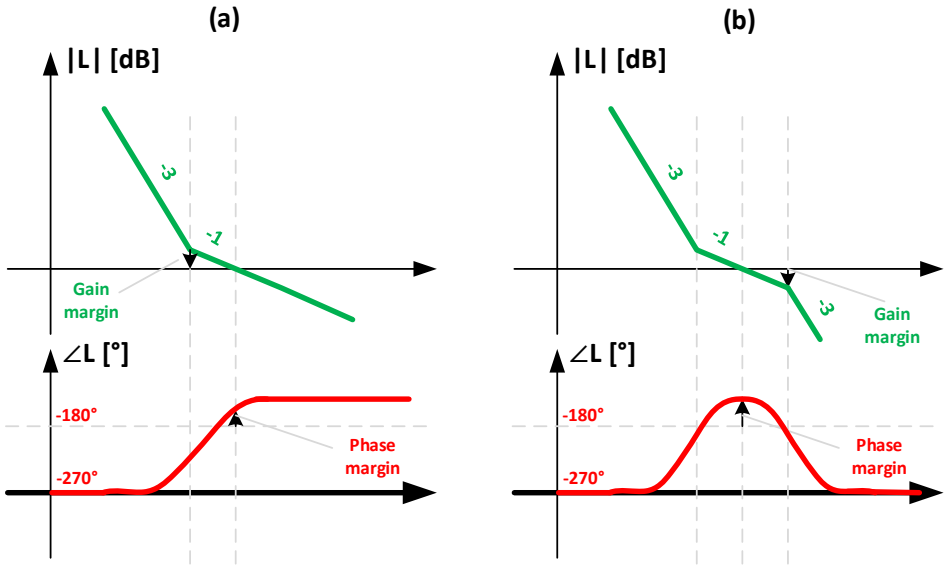


Figure 3.10 Bode plot of the noise shaper with -3/-1 slope characteristics and -3/-1/-3 slope characteristics

A loop gain response with a -3/-1 slope characteristic results in a big hump of phase above the intended open-loop bandwidth (Figure 3.10 (a)). A damped second-order filter could help to decrease the sensitivity to high-frequency noise without affecting stability. The response of the noise shaper (as shown in Figure 3.10 (b)) has a -3/-1/-3 slope characteristic, and the phase peak is tuned exactly at the intended open-loop bandwidth.

$$H_l(s) = H_{l1}(s)H_{l2}(s)H_{l3}(s) = \frac{a_0\omega_{02}^2(s^2 + 2\zeta_1\omega_{01}s + \omega_{01}^2)}{s^3\omega_{01}^2(s^2 + 2\zeta_2\omega_{02}s + \omega_{02}^2)} \tag{2.29}$$

Where $H_{fb}(s)$ is the transfer function of the noise shaper. The noise shaper is divided into three terms. The first term contains three DC poles which are annotated in red. The second term contains two complex zeroes, which are annotated in green. The third section contains two complex poles, which are annotated in blue.

With the noise shaper, the Fourier transfer of the loop transfer function can be expressed as:

$$|L(j\omega)| = \frac{A\sqrt{\left(1 - \frac{\omega}{\omega_{01}}\right)^2 + \left(2\zeta_1\frac{\omega}{\omega_{01}}\right)^2}}{(\omega)^3\sqrt{\left(1 - \frac{\omega}{\omega_{02}}\right)^2 + \left(2\zeta_2\frac{\omega}{\omega_{02}}\right)^2}} \tag{2.30}$$

The equation has two preconditions: 1. The plant compensator can perfectly cancel the poles and zeroes in the plant. 2. There is no delay in the control loop.

Where the magnitude of the loop transfer is calculated by:

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$$|L(j\omega)|_{dB} = \frac{A\sqrt{\left(1-\frac{\omega}{\omega_{01}}\right)^2 + \left(2\zeta_1\frac{\omega}{\omega_{01}}\right)^2}}{(\omega)^3\sqrt{\left(1-\frac{\omega}{\omega_{02}}\right)^2 + \left(2\zeta_2\frac{\omega}{\omega_{02}}\right)^2}} \tag{2.31}$$

The phase of the loop transfer equals to:

$$\angle L(j\omega) = -270° + \arctan\left(\frac{2\zeta_1\frac{\omega}{\omega_{01}}}{1-\frac{\omega}{\omega_{01}}}\right) - \arctan\left(\frac{2\zeta_2\frac{\omega}{\omega_{02}}}{1-\frac{\omega}{\omega_{02}}}\right) \tag{2.32}$$

Considering the delay in the control loop, and the Laplace transfer of the loop transfer function can be expressed as:

$$L(s) = A\frac{\omega_{02}^2(s^2 + 2\zeta_1\omega_{01}s + \omega_{01}^2)}{s^3\omega_{01}^2(s^2 + 2\zeta_2\omega_{02}s + \omega_{02}^2)}e^{-sT_d} \tag{2.33}$$

Where T_d is the delay in the loop, and it is estimated as 1.8 μs. It consists: 1. The delay of the ADC. 2. 2. The delay of the communication. 3. The delay of the switching stages and the current sense circuit. 4. The delay of the additional filters in the digital control loop.

Since the delay does not influence the magnitude of the transfer function but influences the transfer function's phase. The phase shift of the noise shaper is expressed as:

$$\angle L(j\omega) = -270° + arctan\left(\frac{2\zeta_1\frac{\omega}{\omega_{01}}}{1-\frac{\omega}{\omega_{01}}}\right) - arctan\left(\frac{2\zeta_2\frac{\omega}{\omega_{02}}}{1-\frac{\omega}{\omega_{02}}}\right) + 360°\frac{\omega}{2\pi}T_d \tag{2.34}$$

After designing the proper poles and zeros, the next step is converting the continuous-time transfer function into the discrete-time transfer function.

The discrete-time transfer function can be calculated through the bilinear transform or calculated by the equations of Eq 2.35 – Eq 2.38.

$$H_{l,design}(z) = \prod_{i=1}^{3} H_{li}(z) \tag{2.35}$$

The discrete-time transfer function of the first term in Eq 2.29 is calculated by:

$$H_{l1}(z) = \frac{a_0}{(z-1)^3} \tag{2.36}$$

The discrete-time transfer function of the second term in Eq 2.29 is calculated by:

$$H_{l2}(z) = \frac{z^2 - (a_{1a} + a_{2a})z + a_{1a}a_{2a} + b_{1a}a_{1a}a_{2a}}{1 - (a_{1a} + a_{2a}) + a_{1a}a_{2a} + b_{1a}a_{1a}a_{2a}} \tag{2.37}$$

Where $a_{1a} = a_{2a} = \cos(T_{ls}\omega_{01}\sqrt{1-\zeta_1^2})e^{-\zeta_1 T_{ls}\omega_{01}}$ and $b_{1a} = \frac{e^{-2\zeta_1 T_{ls}\omega_{01}}}{a_{1a}a_{2a}} - 1$

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T_{ls} is the sample rate of the digital system. ζ_1, ω_{01}, ζ_2, ω_{02} are the same as in Eq 2.30 – Eq 2.34.

The discrete-time transfer function of the third term in Eq 2.29 is calculated by:

$$H_{l3}(z) = \frac{1 - (a_{1b} + a_{2b}) + a_{1b}a_{2b} + b_{1b}a_{1b}a_{2b}}{z^2 - (a_{1b} + a_{2b})z + a_{1b}a_{2b} + b_{1b}a_{1b}a_{2b}} \quad (2.38)$$

Where $a_{1b} = a_{2b} = \cos(T_{ls}\omega_{02}\sqrt{1-\zeta_2^2})e^{-\zeta_2 T_{ls}\omega_{02}}$ and $b_{1b} = \frac{e^{-2\zeta_2 T_{ls}\omega_{02}}}{a_{1b}a_{2b}} - 1$

T_{ls} is the sample rate of the digital system. ζ_1, ω_{01}, ζ_2, ω_{02} are the same as in Eq 2.30 – Eq 2.34.

Eq 2.35 transfer function can be implemented in several ways. Firstly, the $H_{l1}(z)$ can be implemented as a cascade of integrators. Then combining $H_{l2}(z)$ and $H_{l3}(z)$ as a Biquad filter.

Secondly, combining $H_{l1}(z)$ and $H_{l2}(z)$ and implementing in Cascade-of-integrators with feedforward (CIFF) or Cascade-of-integrators with feedback (CIFB). Then realizing $H_{l3}(z)$ as a second-order digital low pass filter.

Thirdly, combining $H_{l1}(z)$, $H_{l2}(z)$, $H_{l3}(z)$ and implementing them as one filter.

$H_{l1}(z)$ and $H_{l2}(z)$ will dominant the performance of the small-signal stability. $H_{l3}(z)$ has a non-dominant effect on the control loop. Due to the difference of the priority, the third term $H_{l3}(z)$ can be designed after the $H_{l1}(z)$ and $H_{l2}(z)$ are designed. This assignment will focus on the second approach to implement the digital filter.

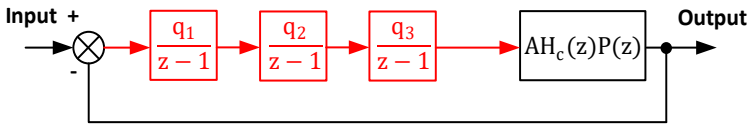


Figure 3.11 Chain of integrators

$H_{l1}(z)$ can be realized by cascading three integrators, which is presented in Figure 3.11. The complex zeroes can be realized by adding forward paths (Figure 3.12(a)) or feedback paths into the integrator chain (Figure 3.12(b)).

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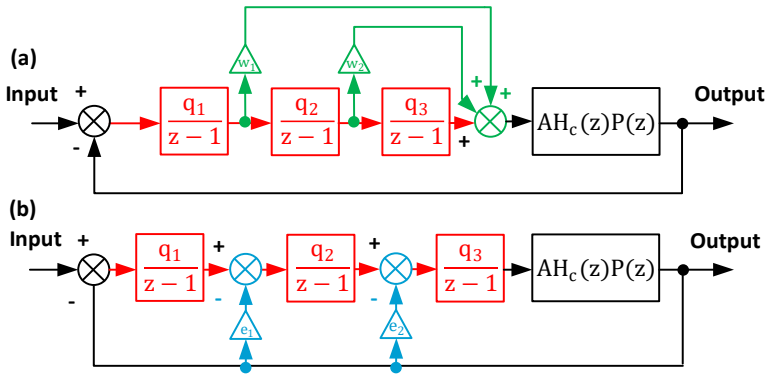


Figure 3.12 Different topology for realizing the discrete architecture

The transfer function of the feedforward architecture for $H_{l1}(z)$ and $H_{l2}(z)$ is:

$$H_{ciff}(z) = A\frac{q_1w_1(z-1)^2 + q_1q_2w_2(z-1)+q_1q_2q_3}{(z-1)^3} \tag{2.39}$$

The transfer function of the feedback architecture for $H_{l1}(z)$ and $H_{l2}(z)$ is:

$$H_{cifb}(z) = A\frac{q_3e_2(z-1)^2 + q_2q_3e_1(z-1)+q_1q_2q_3}{(z-1)^3} \tag{2.40}$$

This assignment will apply feedforward configuration instead of feedback configurations. The reasons are as follows:

1. The feedback structure has a critical disadvantage which comes from the large swing capability of the integrators. The input of the feedback path tracks the input signal and the output of the integrators, which carries a significant amount of input signal. However, this problem does not exist on the feed-forward structure since the signal component of the first integrator output is high pass filtered. Therefore, considering the effect of over-drive recovery discussed in Section 3.4.3, the feedforward structure results in less recovery time for a large DC or low-frequency input signal.

2. The signal must pass through three integrators in the feedback configuration, resulting in third-order low pass filtering at high frequencies. In the feedforward topology, the last two integrators are bypassed by the feedforward paths, which cause only one-order low filtering at high frequencies. Therefore, with the same NTF, the feedback topology results in more delay, taking more budget than the feedforward topology.

Therefore, feed-forward is chosen as the realization method for this assignment. The other two high-frequency poles are designed as a second-order low pass damped filter, annotated as blue in Figure 3.13.

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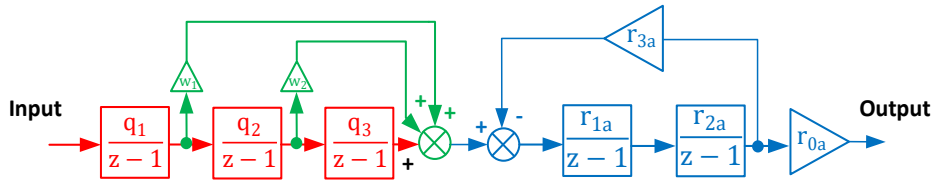


Figure 3.13 Proposed noise shaper for the digital power amplifier

The discrete-time transfer function of the proposed architecture is expressed as:

$$H_{l,model}(z) = H_{l1}(z)H_{l2}(z)H_{l3}(z) = \frac{r_{0a}r_{1a}r_{2a}(q_1w_1(z-1)^2 + q_1q_2w_2(z-1) + q_1q_2q_3)}{((z-1)^2 + r_{1a}r_{2a}(z-1) + r_{1a}r_{2a} - r_{1a}r_{2a}r_{3a})(z-1)^3} \quad (2.41)$$

To properly tune the coefficient of the noise shaper, there needs a Script to link Eq 2.35 with the equation above.

$$H_{l,design}(z) = H_{l,model}(z) \quad (2.42)$$

3.4.3. Digital limiters design

When the rate of change of the controller output signal $I_{o,c}$ is larger than the rate of the change of the reference signal I_{ref}, the PWM generator will stop modulating, and the system appears to be unstable. After a long time, the system will recover from this overdrive condition. The recovery time can be decreased by inserting limiters in the forward loop, effectively limiting the gain in the forward loop and saving overdrive recovery time. An Equivalent model of the current driver to analyze this effect is shown in Figure 3.14.

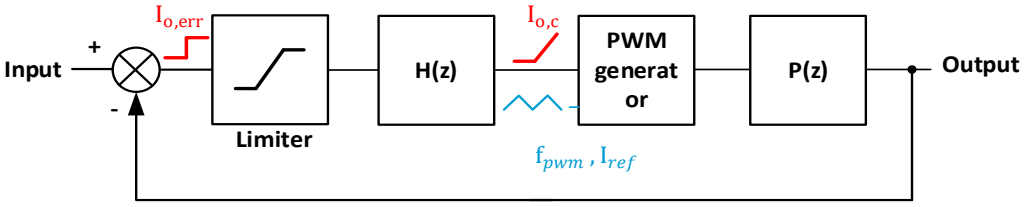


Figure 3.14 Large signal instability (Io,err: Error signal. Io,c: Controller output.)

The error detector output signal equals the difference between the input and feedback signal. A stable steady-state solution can only exist if the slopes of the red controller output signal are smaller than the slopes of the blue reference signal. This solution can be expressed as:

$$\left|\frac{dI_{ref}(t)}{dt}\right| > \left|\frac{dI_{o,c}(t)}{dt}\right| = \left|\frac{d(I_{o,err}(t) * h(t))}{dt}\right| \quad (2.43)$$

Where $\left|\frac{dI_{ref}(t)}{dt}\right|$ equals to:

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$$\left|\frac{dI_{ref}(t)}{dt}\right| = \left|\frac{2I_{ref}}{0.5T_{pwm}}\right| = 4\frac{f_{pwm}}{G_{pwm}}|V_{pwm}| \tag{2.44}$$

The amplitude of the reference triangle is related to the amplitude of the PWM output by the equivalent gain $G_{pwm} = \frac{|V_{pwm}|}{|I_{tri}|}$.

In this application, the transfer function of the controller is very complicated. It contains the noise shaper and the plant compensator, so it cannot be easily calculated. The maximum error signal value can be found by modeling and simulating the equivalent model in MATLAB.

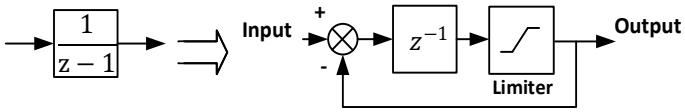


Figure 3.15 Proposed limiters in the noise shaper

Besides adding one limiter at the input of the controller, the proposed design can also combine with the following two approaches to save the overdrive recovery time: 1. Place the low-frequencies poles instead of DC poles to limit the DC gain. 2. Add limiters in the integrators of the noise shaper to effectively switch off the contribution of some integrators to the overall filter function before removing the excess signal, as shown in Figure 3.15.

Compared with the first solution, the second one has a better performance in shaping the time quantization errors after removing the excess signal. Therefore, the second solution will be applied to this assignment.

3.4.4. Tolerance of output filter impedance spread

As discussed in the last section, the plant compensator $H_c(z)$ can perfectly cancel the poles and zeros in the plant of the load $P(z)$. In the practical situation, the plant will have a difference from the designed plant. Therefore, the mismatch of the plant compensator will degrade the stability of the control system.

Because of the tolerance of the components, the filter inductance and capacitance in the practical situation will be different from their designed value. Therefore, the corner frequency and the damping performance of the output filter will be different.

Assume the plant compensator cannot compensate the output filter poles, but it can perfectly compensate other poles and zeroes. Then the magnitude equation of the loop gain can be estimated by:

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$$\left|L_{p,filter}(j\omega)\right|_{dB} = |L(j\omega)|_{dB} \frac{\sqrt{\left(1-\frac{\omega}{\omega_{03}}\right)^2 + \left(2\zeta_3 \frac{\omega}{\omega_{03}}\right)^2}}{\sqrt{\left(1-\frac{\omega}{\omega_{04}}\right)^2 + \left(2\zeta_4 \frac{\omega}{\omega_{04}}\right)^2}} \quad (2.45)$$

The phase equation of the loop gain can be estimated by:

$$\angle L_{p,filter}(j\omega) = \angle L(j\omega) + \arctan\left(\frac{2\zeta_3 \frac{\omega}{\omega_{03}}}{1-\frac{\omega}{\omega_{03}}}\right) - \arctan\left(\frac{2\zeta_4 \frac{\omega}{\omega_{04}}}{1-\frac{\omega}{\omega_{04}}}\right) \quad (2.46)$$

Where ω_{03} and ζ_3 are the angular frequency and damping factor of the zeroes in the plant compensator to compensate the poles of the output filter, ω_{04} and ζ_4 are the angular frequency and damping factor of the poles of the output filter.

In this assignment, the control loop is designed to tolerate the filter inductance, and capacitance varies ±30% from its designed value. It can be estimated at the beginning by calculating the gain margin and phase margin of the loop transfer based on Eq 2.45 and Eq 2.46.

3.4.5. Instability due to cable capacitance

The cable capacitance will influence the stability of the control loop. The current driver can be modeled as a current source that connects with the motor, as shown in Figure 3.16. Ideally, the zeroes of the motor can be canceled by the plant compensator. However, the load impedance will be varied due to the temperature variation, production tolerance. Therefore, the poles in the plant compensator can not perfectly cancel the zeroes of the motor, which will greatly decrease the stability of the system.

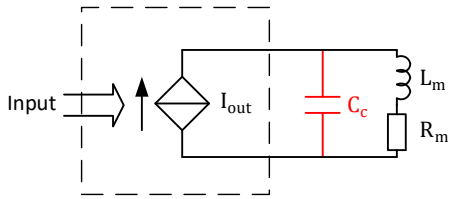


Figure 3.16 Equivalent model for the current driver with the load and the cable capacitance

Cable capacitance will resonant with the motor inductance at the frequency of Cc Lm. The quality factor of the resonant poles will be dramatically large as the cable capacitance is much smaller than Rm and Lm.

The damping factor of the resonant poles can be estimated as:

$$\zeta_{m,p} = \frac{1}{2R_m\sqrt{\frac{L_m}{C_c}}} \quad (2.47)$$

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According to Table 2.1Table 2.1, the frequency of the poles will be in the arrange of 40 kHz to 60kHz. These resonant poles will greatly influence the stability of the control loop, as shown in Figure 3.17.

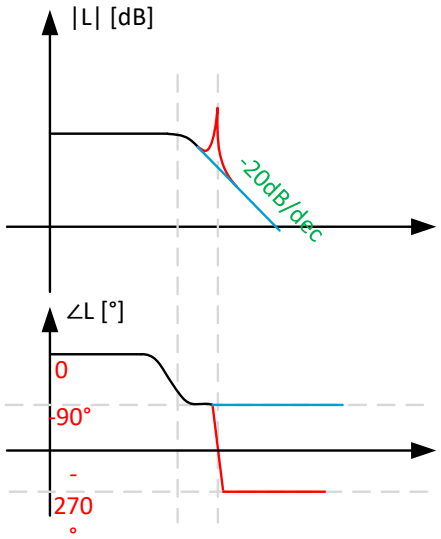


Figure 3.17 Effect of the resonant poles produced by the load and the cable capacitance (Red: Resonant due to the cable capacitance. Blue: Smooth transfer when there is no cable capacitance)

Although the plant compensator can compensate the resonant pairs, the system will be sensitive to the motor impedance variation.

If the plant compensator cannot perfectly cancel the resonant pairs which are introduced by the cable capacitance and motor inductance

The magnitude of the loop gain is

$$\left|L_p(j\omega)\right|_{dB} = \left|L_{p,filter}(j\omega)\right|_{dB} \frac{\sqrt{\left(1-\frac{\omega}{\omega_{06}}\right)^2 + \left(2\zeta_6\frac{\omega}{\omega_{06}}\right)^2}}{\sqrt{\left(1-\frac{\omega}{\omega_{05}}\right)^2 + \left(2\zeta_5\frac{\omega}{\omega_{05}}\right)^2}} \tag{2.48}$$

The phase of the loop gain is

$$\angle L_p(j\omega) = \angle L_{p,filter}(j\omega) - \arctan\left(\frac{2\zeta_5\frac{\omega}{\omega_{05}}}{1-\frac{\omega}{\omega_{05}}}\right) + \arctan\left(\frac{2\zeta_6\frac{\omega}{\omega_{06}}}{1-\frac{\omega}{\omega_{06}}}\right) \tag{2.49}$$

Where ω_{05} is the angular frequency of the poles for canceling the zeros of the motor, ζ_5 is the damping factor of the zeroes for canceling the zeros of the motor, ω_{06} is the angular frequency of the zeros of the motor and ζ_6 is the damping factor of the zeros of the motor.

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Since $C_c << R_m^2 L_m$, the damping factor of the zeroes of the motor $\zeta_{m,z}$ is greatly smaller than the damping factor of the zeroes in the plant compensator ζ_6. After calculating the Eq, it can be noticed that if $\omega_{05} < \omega_{06}$, the unity gain frequency of the loop gain $L_p(j\omega)$ will be greatly reduced. $\omega_{05} < \omega_{06}$ will be happened if the motor inductance is smaller than its estimated value. In this case, the system's stability will be dramatically influenced, becoming unstable.

There are three ways to minimize the effect of cable capacitance on the control loop in terms of Brute Force, active damping, and cable capacitance compensation.

1. Passive damping

The passive damping technique can increase the damping factor of the zeroes of the motor by paralleling the load with a passive resistor, as shown in Figure 3.18. It does not require any additional analog feedback circuit, and it is easy to implement. However, it has several disadvantages. Firstly, the resistor will create more dissipation and degrade the power efficiency. Secondly, the flexibility of the circuit is limited by the passive component. Thirdly, the damping factor will vary due to the passive components' tolerance and operation environment. Therefore, it is not a reliable option.

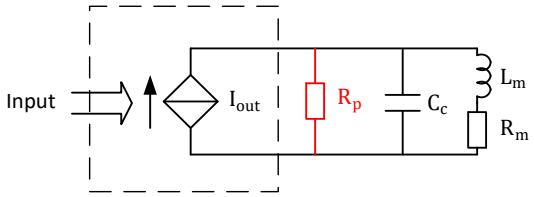


Figure 3.18 Equivalent model for the current driver with passive damping (Rp)

The DC power losses of the damping module can be effectively eliminated by adding a capacitor C_p in series with the passive resistor R_p. Figure 3.19 shows the equivalent model of this concept. The damping factor of the poles can be designed as:

$$Q_{pairs} = 2\pi f_{resonant} R_p C_c \tag{2.50}$$

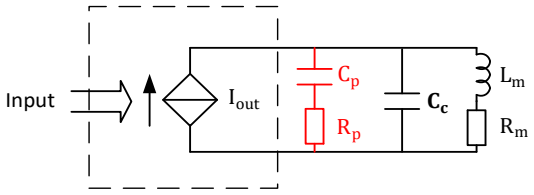


Figure 3.19 Equivalent model for the current driver with passive damping (Rp and Cp)(Cp > >Cc)

2. Active damping

The AC power losses of the damping module can be decreased by employing the active damping technique. This technique requires another inner loop to create an active resistor

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Rp. The damping factor of the resonant poles can be easily tuned with a digital inner loop. However, this technique still meets the issue of low reliability. Since the tolerance and DC bias characteristics of the passive capacitor Cp will degrade the damping performance.

The passive and active damping technique designs the amplifier's D and C using negative feedback for the current driver. An alternative called cable capacitance compensation also exists, which designs the D and C of the amplifier by applying positive feedback for the current driver.

3. **Cable capacitance compensation**

This technique can effectively decrease cable capacitance by compensating the current through the cable capacitance with an additional outer loop. It requires less dissipation and has higher flexibility compared with the passive damping technique. Unlike the active damping technique, it can move the location of the zeroes of the motor to a higher frequency. Since the zeroes are shifted to the high frequency, the mismatch of the pole-zero cancellation contributes less to the control loop.

The techniques are compared and ranked based on Table 3.3. In the end, the cable capacitance compensation is selected as the best solution, and it will be further designed in the next chapter.

Table 3.3 Comparison table for the options to minimize cable capacitance effect

Solutions	**Weight**	**Brute damping**	**Active damping**	**Cable capacitance compensation**
Power efficiency	1	-	0	0
Accuracy	1	-	0	0
Motor impedance variation sensitivity	2	-	-	+
Complexity	1	0	-	-
Flexibility	1	-	+	+
Score		- - - - -	- -	+ +

3.4.6. Cable capacitance compensation design and implementation

The cable capacitance can be compensated by adding a negative capacitive output impedance to the current amplifier. The output impedance of the amplifier can be designed with the transmission-1 matrix. By paralleling capacitive output voltage feedback, the transmission-1 matrix parameter C of the amplifier can be fixed. In this case, the output impedance of the amplifier is written as:

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$$Z_o = \frac{DZ_s + B}{CZ_s + A} = -C_c \tag{2.51}$$

Where A = 0, B = 0, C = -sC_c , D = 1. The output impedance is negative and capacitive.

Figure 3.20 shows the equivalent model of the cable capacitance compensation circuit. It requires an outer loop that consists of a voltage sense circuit and a digital feedback path.

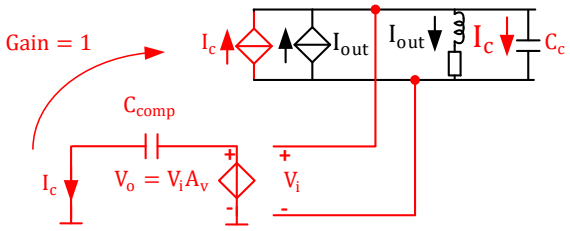


Figure 3.20 Equivalent model for cable capacitance compensation Black: Equivalent model of the current amplifier

Red: Equivalent model of the cable capacitance compensation module

The voltage sense circuit senses the voltage across the load and transfers it to the digital feedback path with a gain of A_v. The digital feedback path converts the voltage signal to the current signal through the cable capacitance.

With Eq 2.51, the compensation of the cable capacitance requires:

$$C_{comp} = \frac{C_c}{A_v} \tag{2.52}$$

This cable capacitance compensation circuit increases the high-frequency transfer from the output voltage to the input current. The equivalent input voltage noise of the voltage sense circuit can be converted into an equivalent output noise current of the current amplifier. Its contribution $S_{oi_{Ac}}$ to the spectrum of the total equivalent output current noise can be calculated as:

$$S_{oi_{Ac}} = 4\pi^2 f^2 A_{vs}^2 C_{comp}^2 S_{ov_{Av}} A_{uda}^2 \tag{2.53}$$

Where A_{vs} is the gain of voltage sense circuit, $S_{ov_{Av}}$ is the input-referred voltage noise of the voltage sense circuit, A_{uda} is the current gain of the current driver, C_{comp} is the digital compensation capacitance.

According to Eq 2.53, the contribution of the outer loop to the spectrum of the total equivalent output current noise is not dominant and can be ignored.

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3.5. Design of acquisition circuit

Figure 3.21 shows the concept of the voltage sense circuit and the current sense circuit. Both of them are referred to as the acquisition circuit. The data acquisition circuit contains the current sense circuit and the voltage sense circuit. The outputs of the acquisition boards are in series with the ADCs. The digital isolators are in series with the ADCs to isolate the high common-mode voltage at the inputs of the acquisition circuit.

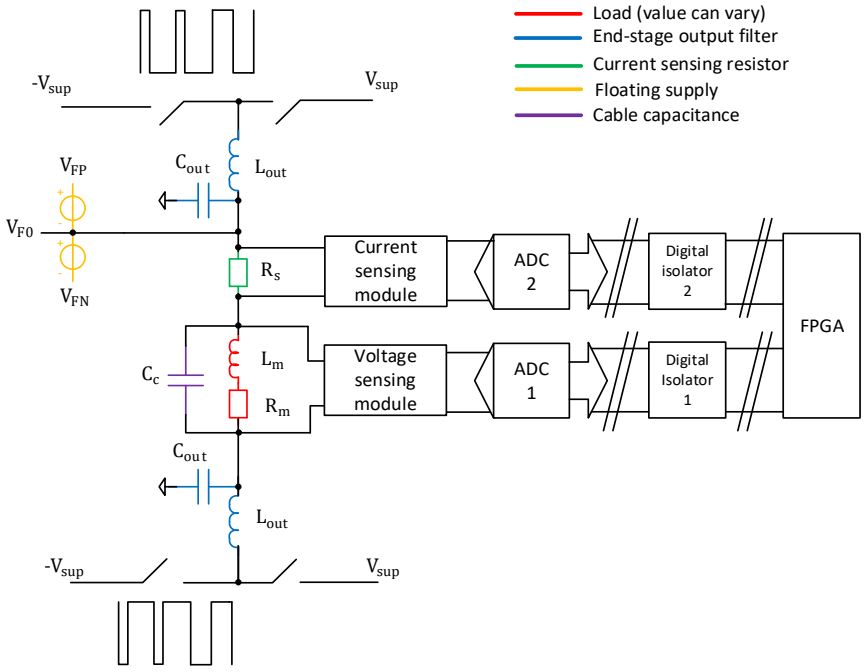


Figure 3.21 Overview of the analog circuits in the digital apmlifier

This circuit operates at the floating supplies, which are indicated as yellow areas. They provide ±5V and ±2.5V voltage to the floating ground, and the data acquisition circuits operate under them.

3.5.1. Current sense circuit

The budget of the amplifier The top-level concept of the current sense circuit is presented in Figure 3.22. The current sense circuit transfer and amplify the current through Rs. Besides, the ±32V common-mode voltage at the input of the current sense circuit is filtered by a digital isolator at the output of the ADC.

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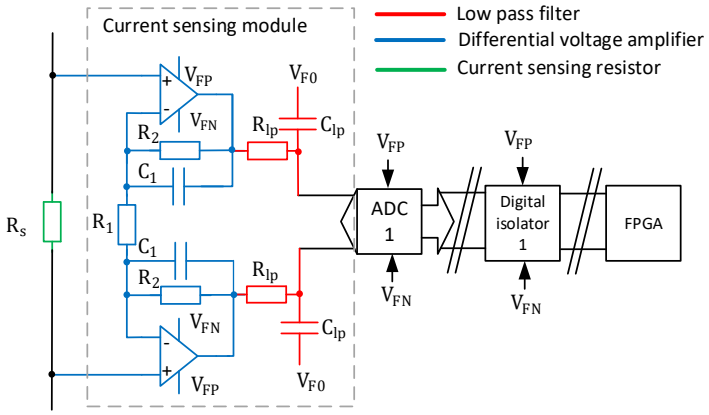


Figure 3.22 Current sense circuit

The antialiasing filter can effectively decrease the aliasing of the noise signal. It consists: 1. Low pass filter, which is annotated in red in Figure 3.22. 2. Current sense circuit with compensation capacitor C_1.

The capacitor C_{lp} is pre-charged to the previous sample before reconnecting. The equivalent noise bandwidth of the low pass antialiasing filter network will be:

$$NBW = \frac{\pi}{2}\frac{1}{2\pi R_{lp}C_{lp}} \tag{2.54}$$

The compensation capacitor C_1 causes a zero and a pole in the loop gain of the current driver. It behaves as a low pass antialiasing filter at a low frequency.

The frequency of the pole is calculated by:

$$\text{pole} = -\frac{1}{2\pi R_2 C_1} \tag{2.55}$$

The frequency of the zero is calculated by:

$$\text{zero} = -\frac{1}{2\pi\frac{0.5R_1R_2}{0.5R_1+R_2}C_1} \tag{2.56}$$

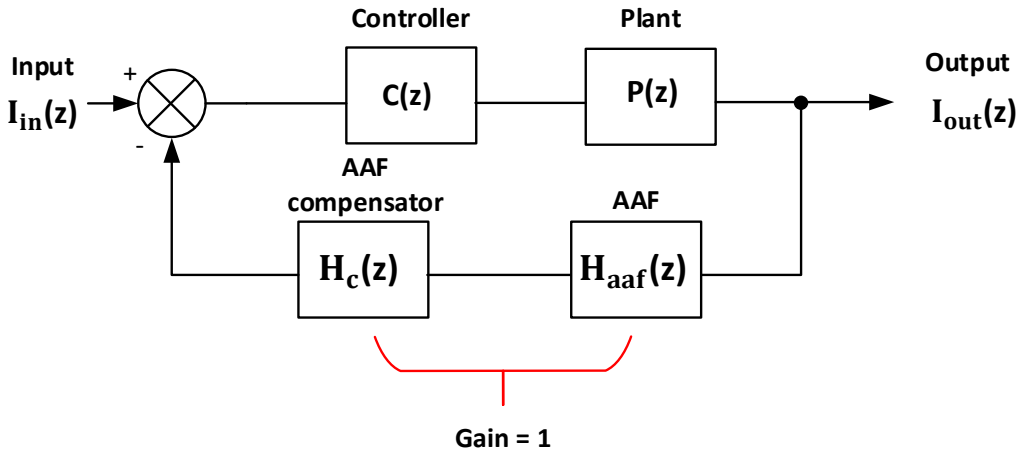
The total RMS noise voltage at the input of AD4630-20 will be:

$$V_{n,ADCin} = \sqrt{S_{n,ADCin}}\sqrt{NBW} \tag{2.57}$$

The compensation capacitance is selected as 3nF, and the input noise voltage at the input of AD4630-20 is designed as: 7.727 μV, which is calculated for R_1= 121 Ω, R_2 = 422 Ω, C_1 = 3nF, R_{lp}= 33 Ω, C_{lp} = 1nF.

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The pole and zero of the current sense circuit contribute to the loop gain transfer and influence the control system's stability. A digital Anti-aliasing filter (AAF) compensator can be applied at the output of the ADC. Its transfer function equals the inverse of the current sense circuit transfer function. Due to the tolerance of the capacitance C_1, the AAF compensator cannot perfectly cancel the effect of the current sense circuit. With similar calculations in Section 3.4.4, the capacitance C_1 can be ± 30% than its designed value. This will result in the maximum 1-degree reduction of the phase margin, which is ignorable.



3.5.2. Voltage sense circuit

The top-level concept of the current sense circuit is presented in Figure 3.23. The load current is transferred to a voltage signal and amplified by a voltage amplifier called the voltage sense circuit. This circuit operates at the floating supplies, which are indicated as yellow areas. Besides, the ± 32V common-mode voltage at the input of the voltage sense circuit is filtered by a digital isolator.

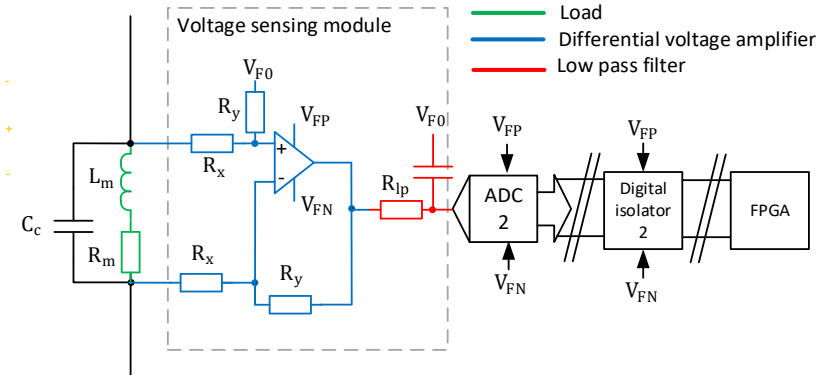


Figure 3.23 Voltage sense circuit

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As discussed in Section 3.4.6, the differentiator is implemented in the digital domain. It will be called the C compensator in the following sections. Because of the large resistor

The differential gain of the voltage sense circuit is given by:

$$A_{vs} = \frac{R_y}{R_x} \tag{2.58}$$

4. Modeling of the complete system

This chapter presents the simulation model and results of the proposed design. Section 4.1 introduces the details of the model. Section 4.2 illustrates the performance of the current driver.

4.1. Overview of the simulation model

Figure 4.1 illustrates the Simulink model of the noise shaper. It has the same structure as in Figure. Three integrators are annotated in red. Two feedforward paths are annotated in green. The second-order damped filter is annotated in blue.

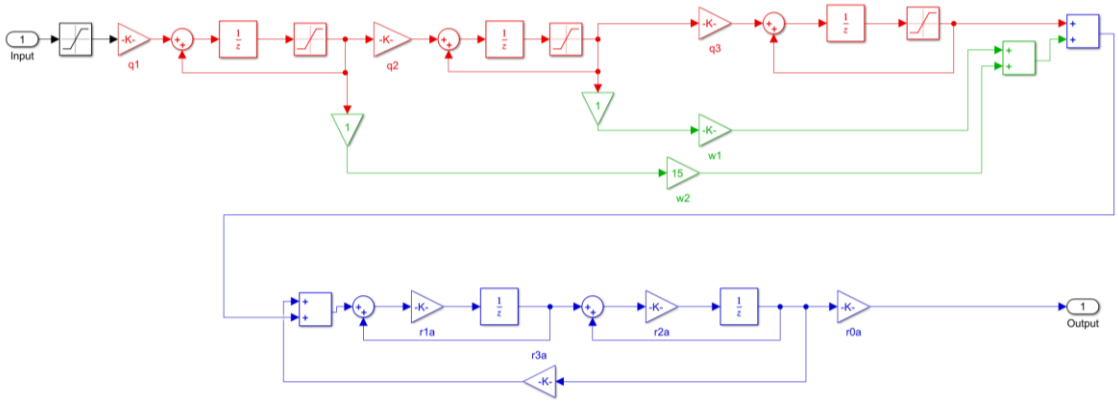


Figure 4.1 Model of the noise shaper

For the PWM generator, there are generally three models: 1. Model for quantization effect. Figure 4.2 shows the Simulink model of it. 2. Separate model for quantization and sampling. This is an intermediate model which in series a comparator at the output of Figure 4.2 to model the effect of sampling. 3. An integrated model for quantization and sampling. The third model is shown in Figure 4.3.

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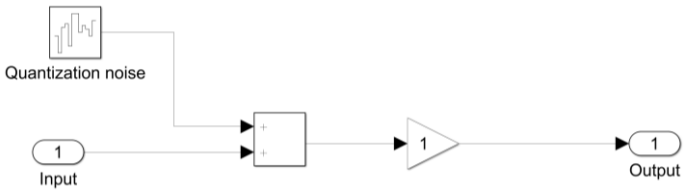


Figure 4.2 Equivalent model of digital PWM generator with quantization (Linear model)

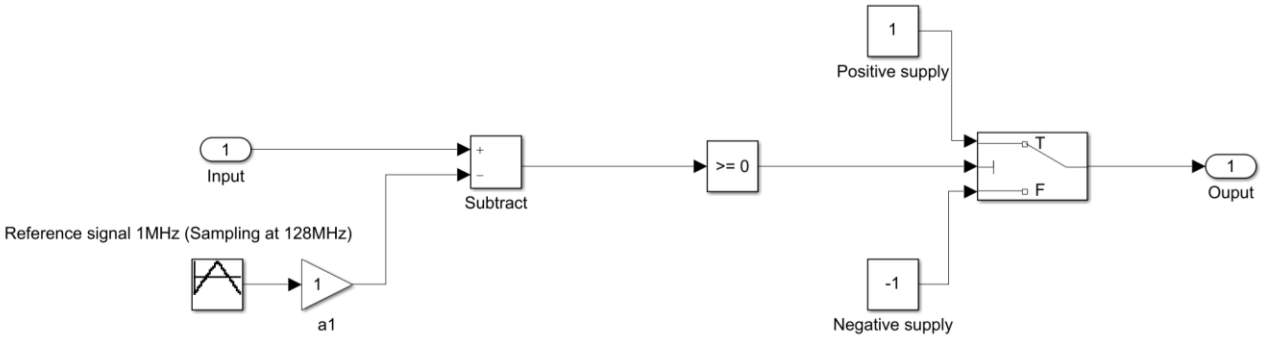


Figure 4.3 Equivalent model of digital PWM generator with quantization and sampling (Switching model)

There are two approaches to model the plant of the load:

1. Transfer function. It has been modeled in Section 2.2.3.
2. The electrical model.

Table 4.1 models for testing the performance of the proposed current driver

Simulation model	**Plant type**	**PWM generator type**	**Enable Voltage feedback**	**Full bridge**	**Simulation tests that have been applied to this model**
A	Transfer function	Linear model	No	Power stage gain*2 (*)	Pole zero plot, closed-loop response, Bode plot, Nyquist plot, small signal step response, cable capacitance compensation
B	Transfer function	Switching model	No	Power stage gain*2	Large signal test (**)

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C	Transfer function	Switching model	No	Power stage gain*2	Noise (***)
D	Electric	Switching model	No	Full bridge connection	Tolerance of the two output filter components

* After the half-bridge design is modeling, the full-bridge design can be obtained, doubling the stage's gain or halving the load impedance.

**Large signal test of the amplifier can be applied for ABCD model, but B model can is the most proper model because this model is the simplest model that can consider the effect of the ripples signal to the large signal stability.

***Noise test can be applied for ABCD models, but the C model is the most proper. Firstly, compared with model A and model B, the PWM generator has the characteristic of sampling effect. Secondly, compared with model D, its complexity is lower.

4.2. Simulation results

A. Loop gain transfer

Figure 4.4 shows the loop gain of the proposed design when there is no delay in the loop. In this simulation, the plant compensator perfectly cancels the poles and zeroes introduces by the plant.

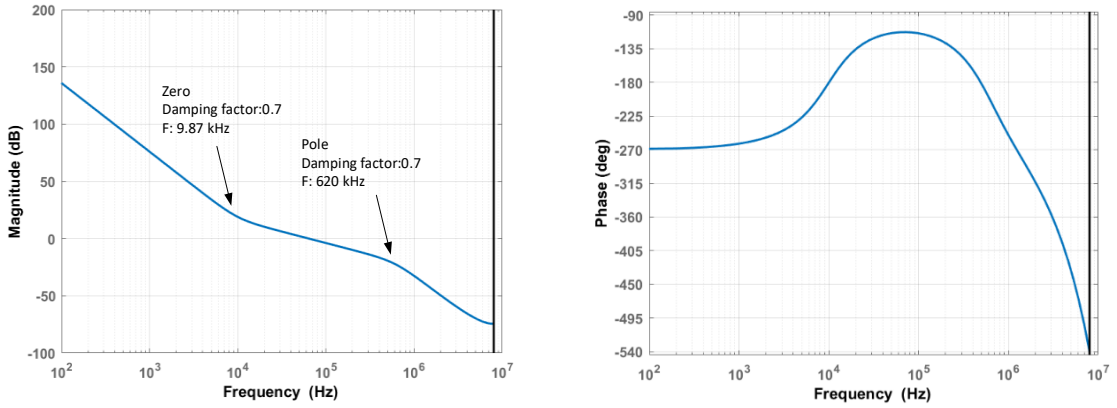


Figure 4.4 Bode plot of the loop gain (Delay= 0)

The response of the noise shaper has a -3/-1/-3 slope characteristic and the phase peak of the loop gain is tuned exactly at unity gain frequency 55 kHz. The phase margin of the loop gain is 62.3 degrees. The noise shaper contains Three DC poles, two zeroes at 9.87 kHz with a damping factor of 0.7, two poles at 620 kHz with a damping factor of 0.7.

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After considering the delay of 1.7 us in the feedback loop, the loop gain of the amplifier is shown in Figure 4.5. The unity loop gain frequency is tuned from 55 kHz to 51.1 kHz to gain more phase margin. The phase margin is 33.7 degrees. The loop gain frequency at 47.6dB is 2.7 kHz, so the noise requirement can be achieved when the frequency is smaller than 2.7 kHz. The magnitude of the loop gain at 1 kHz is 73.6dB.

Therefore, if the time quantization noise from the digital PWM generator is the only noise source in the amplifier, the output referred current noise density will be 1.95 $nA/\sqrt{Hz}$.

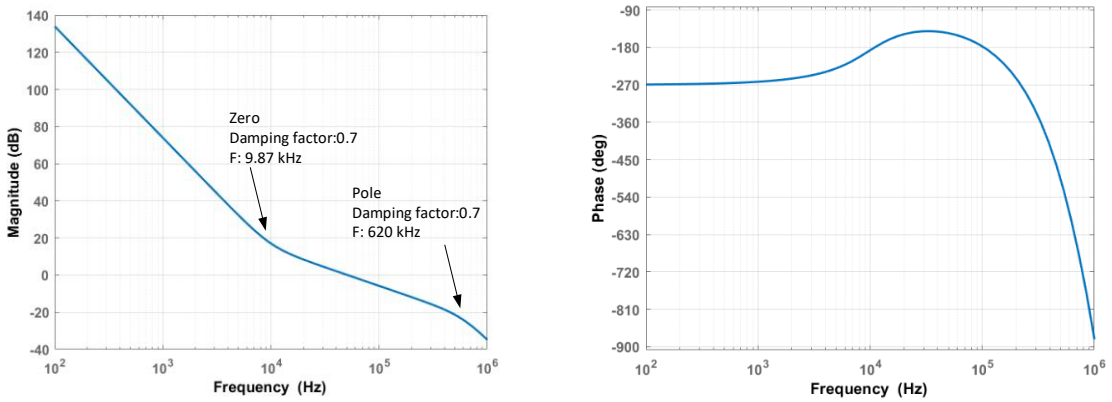


Figure 4.5 Bode plot of the loop gain (Delay= 1.7us)

Figure 4.6 shows the Nyquist bode plot of the control loop. It proves that the closed-loop system is stable.

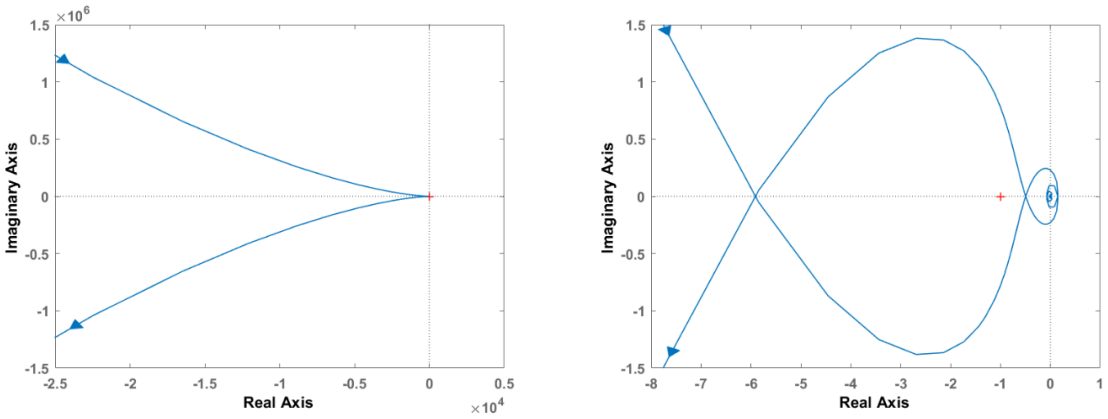


Figure 4.6 Nyquist plot of the loop gain

B. Input-to-output transfer

Butterworth filter is used as the input interpolation filter. The order of the Butterworth is determined as second-order, and the cut-off frequency is selected as 19 kHz.

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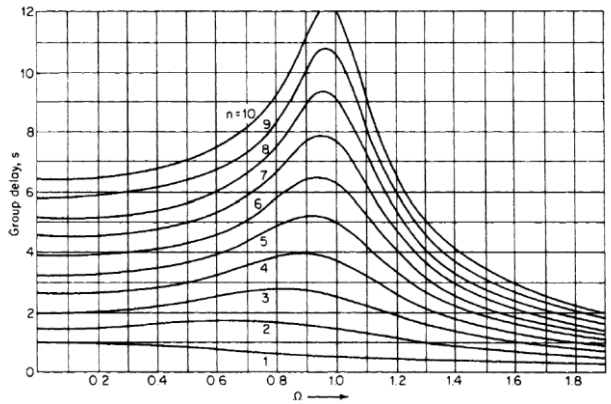


Figure 4.7 Group delay characteristics for Butterworth filter [19]

The Butterworth filter design is based on group delay characteristics for the Butterworth filter in Figure 4.7. Figure 4.8 shows the implementation of the Butterworth filter. This implementation is based on its standard form.

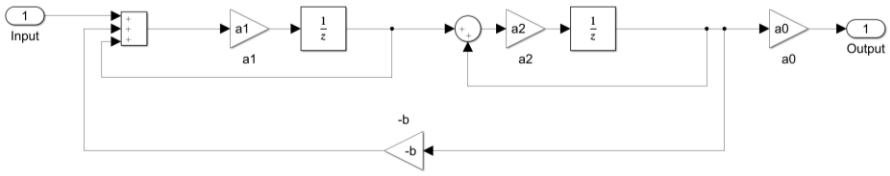


Figure 4.8 Simulink model of the input reconstruction filter

Combining with the input reconstruction filter, Figure 4.9 shows the amplifier's transfer (with the input reconstruction filter). The -3dB point of the amplifier is 26kHz.

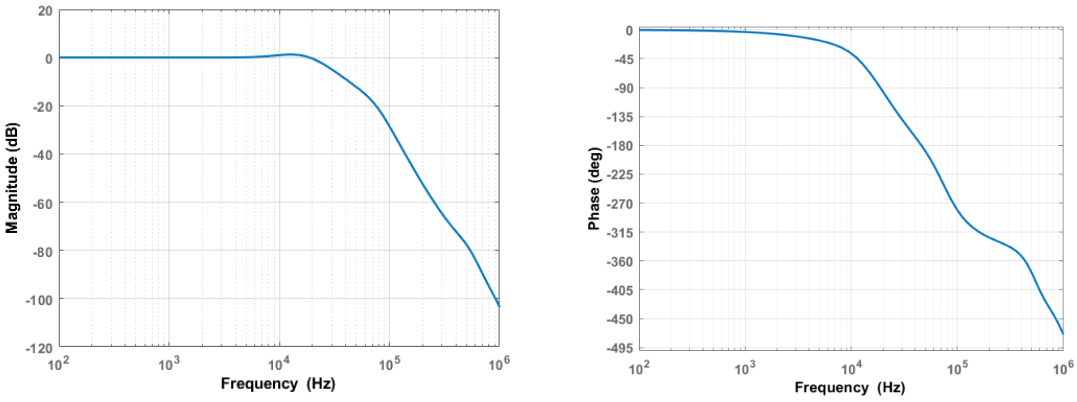


Figure 4.9 Small signal input-output transfer

Figure 4.9 presents the step-response of the current driver. The source-to-load delay of the amplifier is 11.8 us, and the overshoot percentage of the amplifier is 14%.

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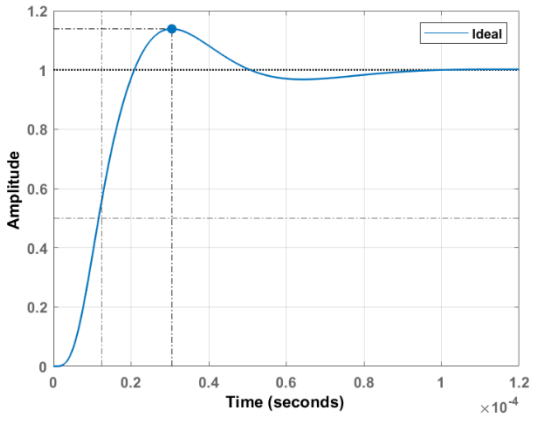


Figure 4.10 Small signal input-output transfer

C. Noise

Figure 4.11 shows the frequency spectrum of the output current (Blue) and the reference noise current (Black). The spectrum density of the reference is 12 $nA/\sqrt{Hz}$. In this model, the time quantization noise introduced by the PWM generator is the only noise source of the current driver. When the frequency is below 2.7 kHz, the output current noise of the amplifier achieves the required specification (12 $nA/\sqrt{Hz}$). According to the calculation result, at 1 kHz, the output referred current noise of the amplifier is at 1.95 $nA/\sqrt{Hz}$.

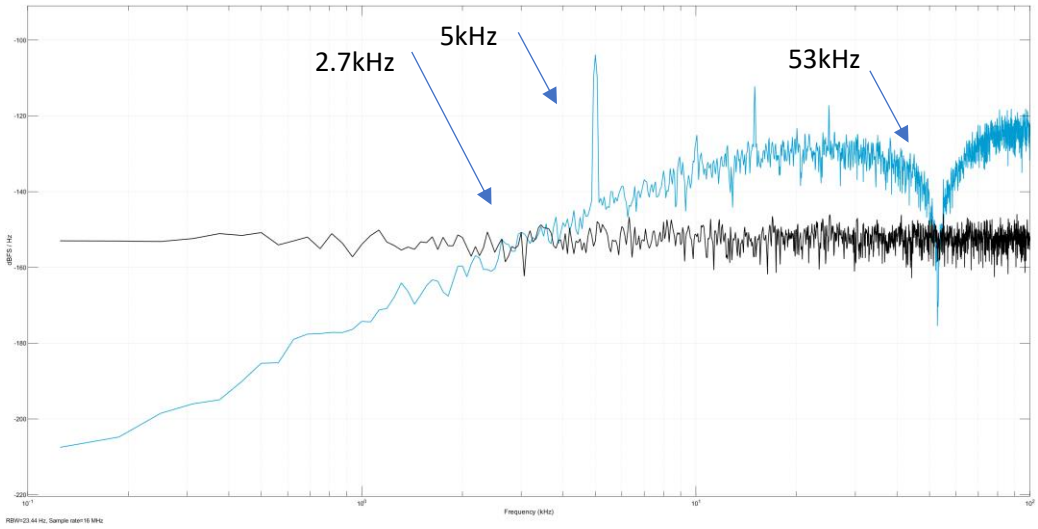


Figure 4.11 Frequency spectrum of the output current and the reference noise source

D. Large signal step-response

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Increase the bound of the limiters can effectively decrease the over drive recovery time of the step response. However, it will lead to a larger delay. The dash-line indicates the 20% overshoot percentage of the step response.

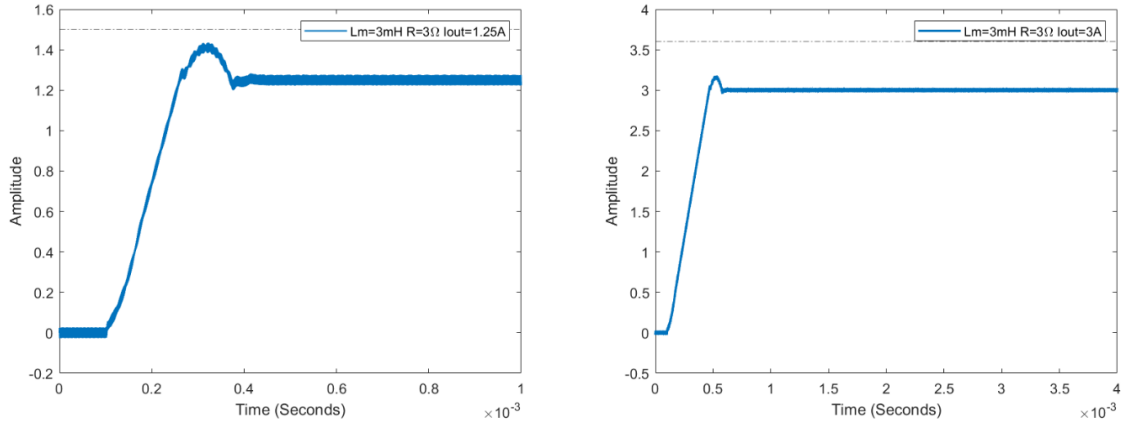


Figure 4.12 Step response of the amplifier whenL_m = 3mH, R_m = 3Ω (Left: I_{out} = 1.25A, Right: I_{out} = 3A)

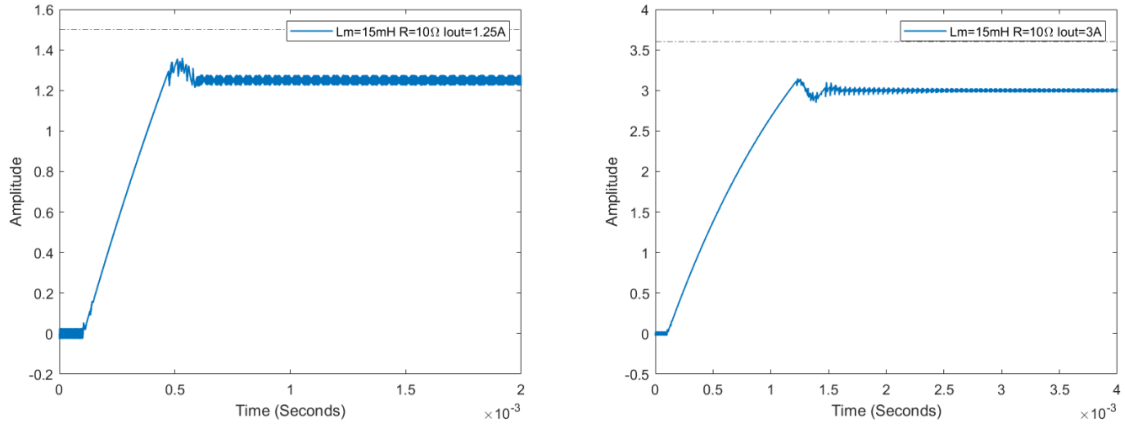


Figure 4.13 Step response of the amplifier when L_m = 15mH, R_m = 10Ω (Left: I_{out} = 1.25A, Right: I_{out} = 3A)

The maximum peak-peak value of the ripple current is 46.8mA. It can be calculated from Eq 2.2. In this case, the duty cycle of the output signal is 50%.) The frequency of the amplifier is 50%.

Except for the ripple current, which contains the switching signal, it can be observed that there is a chaotic ringing. This is the effect of the noise shaping that the ringing frequencies are at around the high frequency.

E. Tolerance of the output filter components

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This section tests the ability of the amplifier to tolerate the impedance spread of the output filter components. It is verified by simulating the small signal step response of the amplifier.

According to the calculations in Section 3.4.4, the filter capacitance $C_{f,r}$ and the filter inductance $L_{f,r}$ can be at least 40% of their design value $C_{f,d}$ and $L_{m,d}$. In the threshold value ($C_{f,r} = 0.6C_{f,d}$, $L_{f,r} = 0.6L_{f,d}$), the resulting control loop is stable with a gain margin of 3.39 dB with a phase margin of 51.9 degrees. For $C_{f,r} < 0.6C_{f,d}$ and $L_{f,r} < 0.6L_{f,d}$, the gain margin of the control loop will be unacceptable, and the control system is at the edge of the instability point.

Meanwhile, $C_{f,r}$ and $L_{m,r}$ can be at most 130% of $C_{f,d}$ and $L_{m,d}$. In the threshold value ($C_{f,r} = 0.6C_{f,d}$, $L_{f,r} = 0.6L_{f,d}$), the resulting control loop is stable with a gain margin of 3.39 dB with a phase margin of 19.6 degrees. For $C_{f,r} > 1.3C_{f,d}$ and $L_{f,r} > 1.3L_{f,d}$The control loop's phase margin will be unacceptable, and the control system is at the edge of the instability point.

Only the key simulation results are demonstrated in this section, and the rest are shown in Appendix A.

Figure 4.14 shows the step response of the amplifier when $C_{f,r} < C_{f,d}$, and $L_{m,r} < L_{f,d}$.

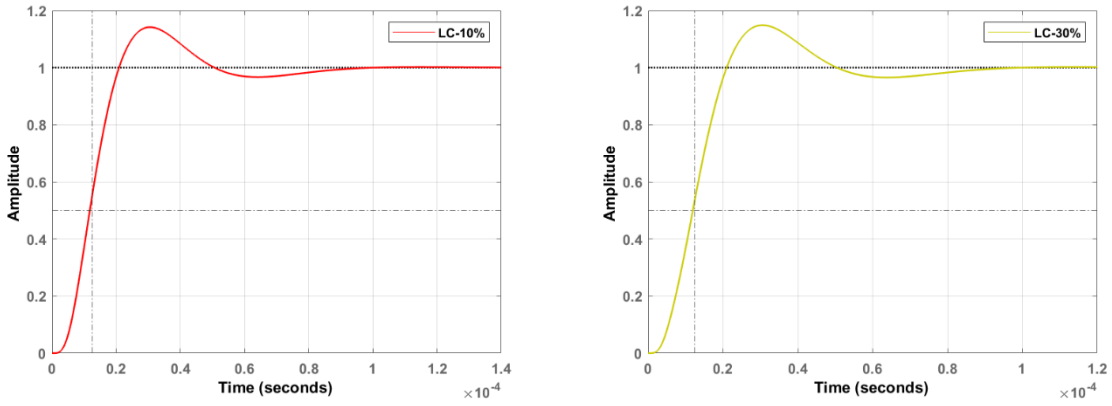


Figure 4.14 small signal step response of the amplifier(Left: $C_{f,r} = 0.9C_{f,d}$, $L_{f,r} = 0.9L_{f,d}$. Right: $C_{f,r} = 0.7C_{f,d}$, $L_{f,r} = 0.7L_{f,d}$)2

Figure 4.15 shows the step response of the amplifier when $C_{f,r} > C_{f,d}$, and $L_{m,r} > L_{f,d}$.

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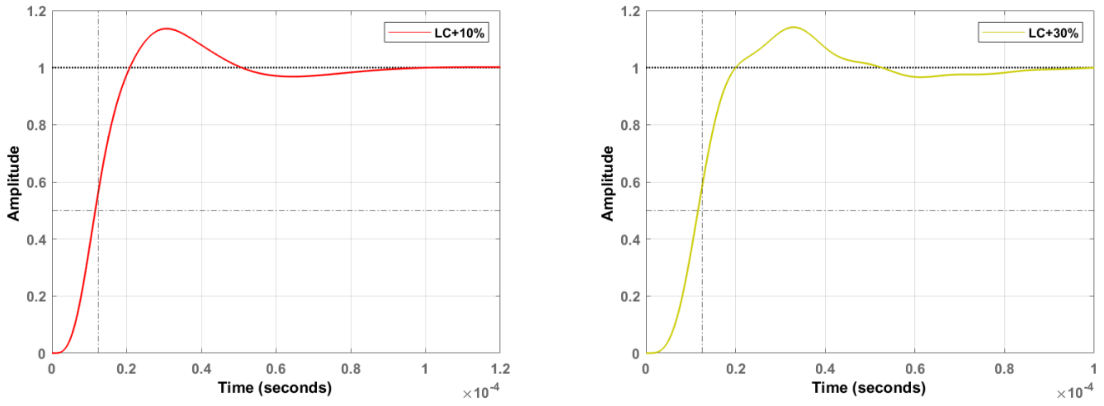


Figure 4.15 small signal step response of the amplifier (Left: $C_{f,r} = 1.1C_{f,d}$, $L_{f,r} = 1.1L_{f,d}$. Right: $C_{f,r} = 1.3C_{f,d}$, $L_{f,r} = 1.3L_{f,d}$)

F. Tolerance of the motor components (Without cable capacitance compensation)

This section tests the ability of the amplifier to tolerate the impedance spread of the motor. It is verified by simulating the small signal step response of the amplifier. This section is focused on evaluating the performance of the plant compensator. Therefore, the simulation model does not enable the cable capacitance compensation module.

According to the calculations in Section 3.4.5, the motor inductance $L_{m,r}$ at most 118% of its designed value $L_{m,d}$. In this case, the overshoot percentage will be 20%. When $L_{m,r} < L_{m,d}$, the system will become unstable.

Figure 4.16 shows the small-signal step response of the amplifier in the case of the motor inductance $L_{m,r}$ is larger than its designed value $L_{m,d}$.

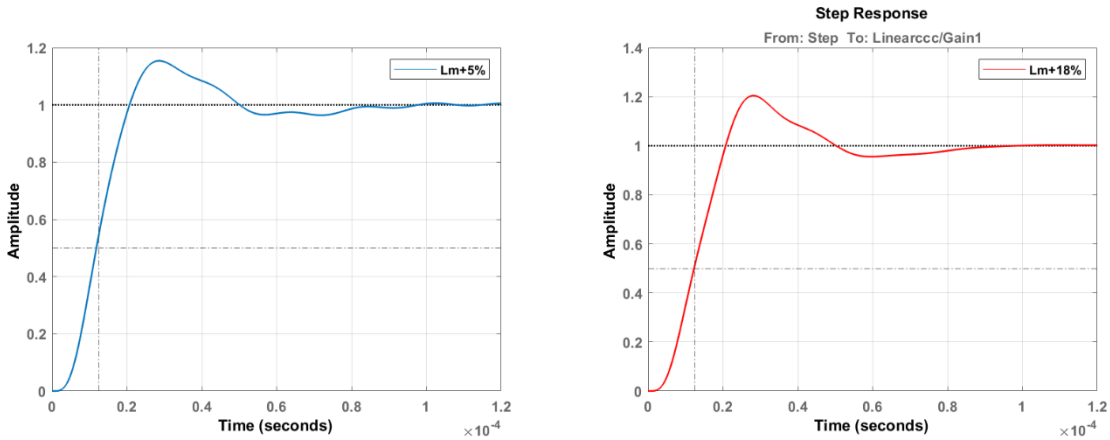


Figure 4.16 Step response of the amplifier when $L_{m,r} > L_{m,d}$

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G. Cable capacitance compensation

Before doing this simulation, the cable capacitance of the plant model in the plant compensator is tuned as 0, where the plant compensator does not compensate the contribution of the cable capacitance C_c. In this case, only the cable capacitance compensation circuit could minimize the effect of the cable capacitance. Figure 4.17 shows the contribution of the cable capacitance circuits. The left figure shows the small-signal step response of the amplifier if there is no compensation on the cable capacitance. The system becomes unstable, and the limiters are always clipping to limit the output signal. After activating the positive feedback loop (Cable capacitance compensation module), the cable capacitance is effectively compensated, and the system becomes stable.

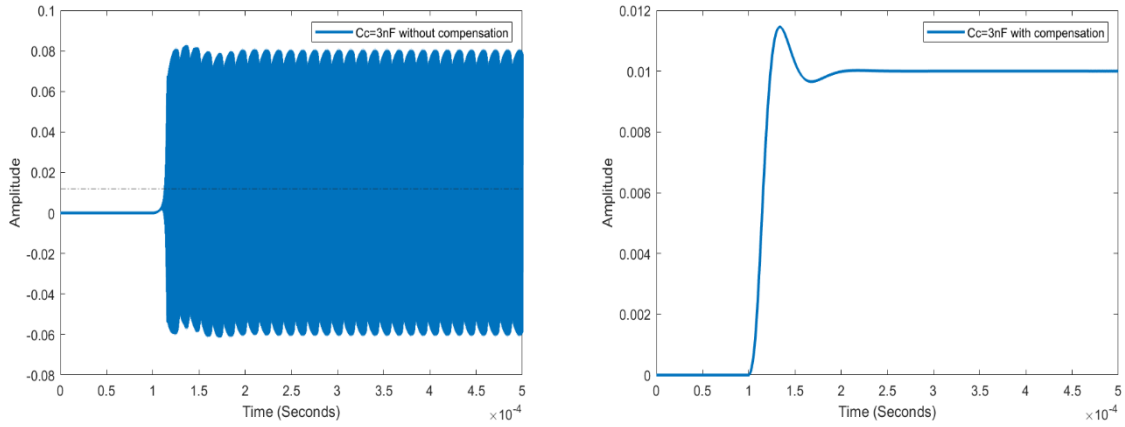


Figure 4.17 Step response of the amplifier when only the plant compensator compensates the effect of cable capacitance (setpoint input 10 mA)

When designing the C compensator in the voltage feedback loop, two important points need to be noticed: 1. The negative cable capacitance which is generated by the voltage feedback should never become larger than the real cable capacitance. Otherwise, the positive feedback will dominant the control system, and the system becomes unstable again. 2. When C_c= 3nF, the gain of the C compensator is too large, leading to the excess voltage at the output of the error detector. This issue can be solved by decreasing the frequency of the pole in the C compensator by means of degrading the performance of the differentiator) sC_c or activating the plant compensator.

The plant can only evaluate the cable capacitance compensation with the transfer function except for the plant with the electric model. The system will become unstable and can never be compensated. With the transfer-function-model plant, the system can be stable with a cable capacitance of 900 pF when there is no compensation for C_c. With the electric-model plant, the system can be unstable with only 10 pF when there is no compensation for C_c, as shown in Figure A. 5 of Appendix A. Therefore, it still needs to investigate what the issue is with the electric-model plant.

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5. Prototype

This chapter mainly focuses on the implementation of the proposed amplifier. Section 5.1 briefly introduces the global map of the proposed design. Section 5.2 presents the details of the firmware implementation of the amplifier. Section 5.3 illustrates the implementation process of the analog circuits.

5.1. System global map

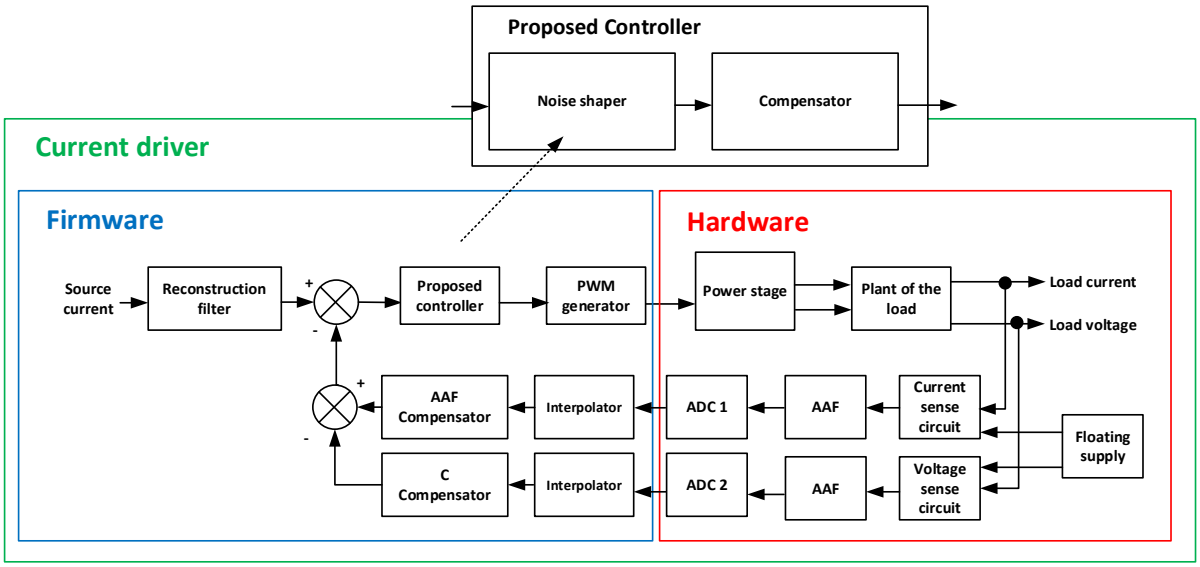


Figure 5.1 Final architecture of the digital amplifier

The prototype of the architecture is shown in Figure 5.1.

5.2. Digital loop implementation

The digital control loop and its data acquisition and data transfer must be implemented in an FPGA. The data acquisition module requires the use of an SPI controller. The SPI controller should be able to do SPI transactions by using echo-clock mode. This mode helps with hooking up the digital isolators and has less potential to meet potential issues.

The data transfer requires the FPGA can control the setpoint signal and has additional options for future debugging and error monitoring. The debugging module can be used during the prototype measurement part. The error monitoring module is used for collecting the data acquired from the data acquisition.

Sjoerd Burm mainly contributes to implementing the firmware. The details of the data acquisition module, debugging module, and error monitoring module can be found in his report. Due to the time limitation, the voltage feedback loop and the data capture blocks are not implemented into this assignment.

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This chapter focus on the details of the control loop implementation. The filters in the digital domain include Noise shaper, plant compensator, interpolator, reconstruction filter, AAF compensator, and C compensator.

The data must be sampled at a certain sample rate and calculated with a certain data type in the digital filters. They will be discussed as follows:

1. Sample rate

The sample rate in the PWM generator is selected as 128 MHz, which has been determined in Section 3.4.2.

The sample rate in the rest of the digital loop is determined as 16 MHz. The FPGA development kit limits the upper sample rate, while the control loop limits the lower bound. After discussing with team members, the sample rate was deemed necessary as 16 MHz.

2. Data type

The data type of the digital system is presented in Figure 5.2. The decisions to apply different data types for the digital circuits are as follows:

In general, floating-point calculating offers a wider range of numbers and more precision than fixed-point calculations. However, its calculation speed is slower than the fixed point. After discussing with the team, the data type in the digital filters is decided as the floating-point.

There are two types of float data type: 1. Single float. 2. Double float. The calculation speed of the double float data type is too slow to meet the time requirements. In this project, the digital filters (Except the plant compensator) are intended to use a single float data type.

The data type of the ADC output signal is fixed-point 24bit. Therefore, the output of the current feedback path requires a data type conversion block to convert the 24 bits fixed point signal to the single float signal.

The data type of the PWM generator is determined as 7 bits due to the limited clock rate. Therefore, the PWM generator requires a data type conversion block at its input.

The plant compensator had a problem working with the single floating data type. The behavior of the filter was unacceptable. Fortunately, after verification, the plant compensator with a fixed-point operation can behave properly. As discussed with team members, a fixed point of 64 bits with the comma separator at 32-bits was deemed accurate enough for the plant compensator. Therefore, the plant compensator requires a data type conversion block at its input.

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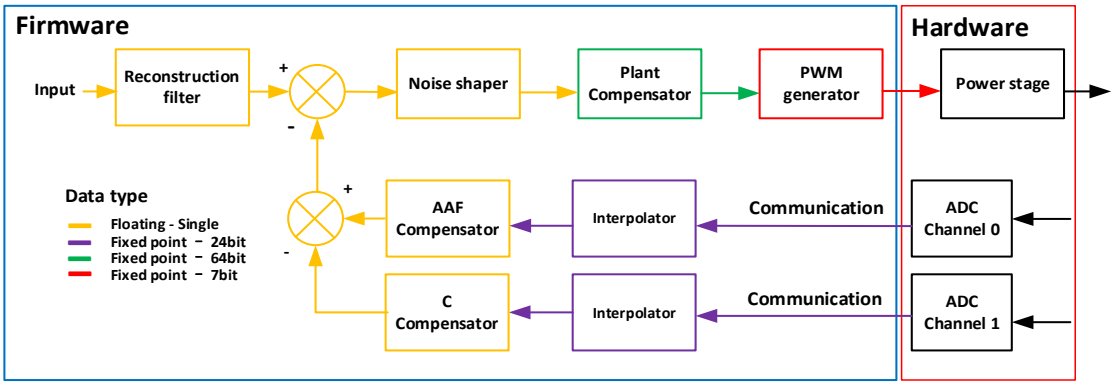


Figure 5.2 Data type in the digital circuits

The details of the noise shaper and the plant compensator are discussed in Section 3.4.2. The details of the reconstruction filter are discussed in Section 4.1. The details of the AAF compensator are discussed in Section 3.5.1. The details of the C compensator are discussed in Section 3.4.6.

The current feedback path and the voltage feedback path require an interpolator, which can up-sample the sample rate of the ADC output signal from 2 MHz to 16 MHz. The interpolator contains an up-sampler and an interpolation filter. Different types of interpolation filters are evaluated and discussed in [20]. After evaluation, the team decides to apply linear interpolation filters to this assignment. The total delay in the feedback path is within the delay budget, which is estimated in Section 3.4.2.

5.3. Analog circuits implementation

This section introduces the details of the implementation of the analog circuit. The hierarchical block diagram of the analog circuits is shown in Figure 5.3. The analog circuits include the power stage, the current protection circuit, data acquisition circuits, and the plant. The digital isolators isolate digital signals and transfer digital communication across an isolation barrier.

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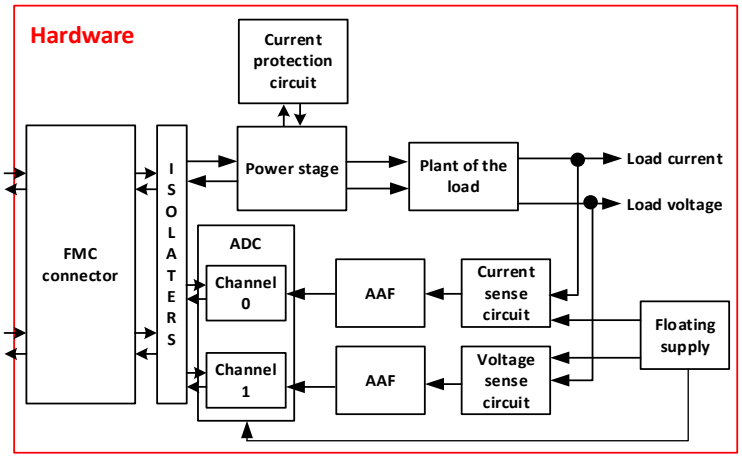


Figure 5.3 Hierarchical block diagram of analog circuits in the digital amplifier

The schematic and the layout design of the analog circuits is designed in the sequence in Table 5.1.

Table 5.1 Design flow of the analog circuits

Design type	**Step**	Description
Schematic design	**1**	Design the hierarchical block diagram.
	2	Design the current sense circuit and voltage sense circuit, which have been discussed in Section 3.5.
	3	Import the power stage circuit, current protection circuit, and the floating supply circuit.
	4	Determine the components in the analog circuits
	5	Determine the label name for all hierarchical labels in the design.
	6	Run Electrical Rules Checker (ERC) to check the connectivity of the schematic design. Choose the proper footprint and package for the components.
	7	Add Manufacturing Production Number (MPN) for all components and make the Bill of Material (BOM)
	8	Review and develop the design
Layout design	**1**	Determine the dimension of the board (Number of layers, length, width)
	3	Placement, routine, and run Design Rules Check (DRC).
	4	Review and develop the design

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6. Measurement

In this chapter, the measurements of the digital apmlifier are presented.

In the measurement phase, we need to test the functionalities of the digital amplifier. **Error! R eference source not found.** shows the hierarchical diagram of the amplifier. The measurement contains three phases: Hardware test, and communication test, amplifier performance test. Firstly, the hardware test includes the functional tests for the hardware of the amplifier. Secondly, the communication test will be held after the firmware is connected with the hardware. The firmware will provide a fixed duty cycle digital PWM signal to the power stage in this mode. Then the functionality of the ADC and PWM generator can be tested in this part. Thirdly, the performance of the amplifier will be tested. With the result of the amplifier, the proposed concept of the digital amplifier can be verified.

6.1. Measurement setup

The measurement of the amplifier consists of three phases: hardware test, communication test, and core performance test. This session mainly focuses on the core performance test of the amplifier. The core performance of the amplifier contains the noise performance, the source-to-load delay, the gain flatness, the gain accuracy, and the tolerance of the variation of the plant components.

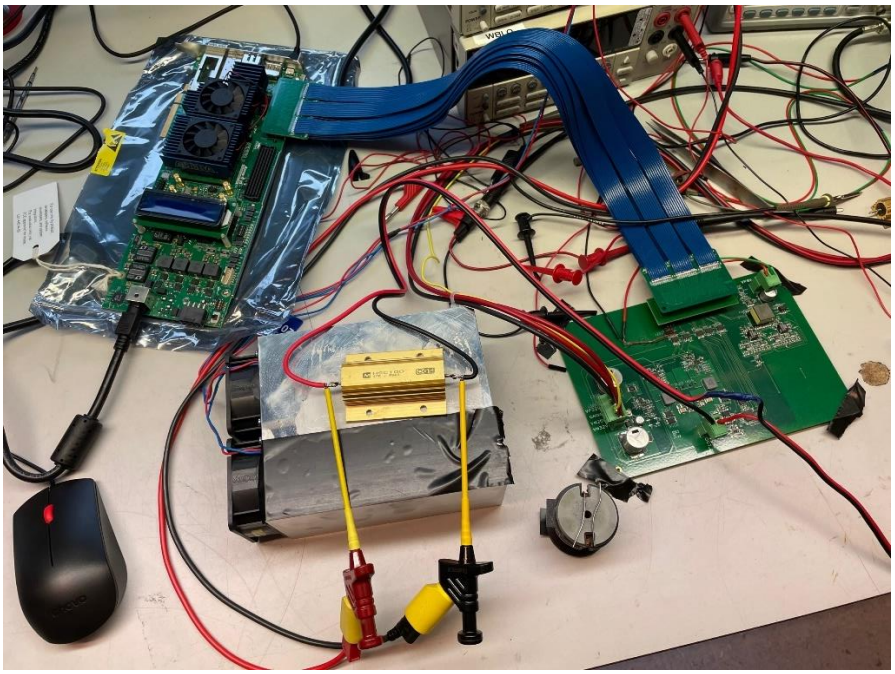


Figure 6.1 Experimental setup for the digital amplifier

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6.2. Current status of the measurement

According to the measurement results, the power stage, current protection circuit, the floating supplies operate properly. The accuracy of the current sense circuit and voltage sense circuit is desired when the floating supplies are properly connected. Some minor adjustments in the hardware design need to be updated in future assignments.

During the communication test, FGPA does not capture the data from the hardware successfully. There has a communication problem for the hardware and firmware part. The issue of the firmware is not known yet because of the limited time. Due to the time limitation, the main part of the communication and performance tests is not included in this project.

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7. Overall performance summary

Table 7.1 to Table 7.3 show the overall performance summary of this current driver. The values in the bracket are the required specifications.

Table 7.1. Overall performance summary of this current driver

Group	Symbol	Parameter	Condition	Min	Typ	Max	Unit
Dynamic behavior	f_b	Amplifier bandwidth	-	(20)	26	-	kHz
	τ	Source to load delay	-	-	-	11.8(12.5)	us
	δ	Step response overshoot	-	-	-	14 (20)	%
Inaccuracy and nonlinear behavior	σ_1	Static gain error	-	-	-	<0.5 (0.5)	%
	σ_2	Gain flatness	0 – 100 Hz	-	-	<0.1 (0.1)	%
	σ_3	Gain inaccuracy	-	-	-	<0.5 (0.5)	%
Efficiency	η	Power efficiency	-	84.4 (80)	-	-	%
Noise performance	i_e	The equivalent output referred current noise	0 – 1000 Hz	-	-	$15.35 * 10^{-9}$ $(26 * 10^{-9})$	$\mathrm{A}\sqrt{\mathrm{Hz}}^{-1}$

Table 7.3. Maximum component tolerance

Component in the plant	Variance (%)	
/	Positive	Negative
Filter inductance (Lf)	30	50
Filter capacitance (Cf)	30	50
Motor inductance	30	30
Motor resistance	>30	>30
Cable capacitance	60	0

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8. Conclusion and future work

A class-D flexible current driver with a digital control loop is presented in this project. Four different concepts are considered and ranked based on the design considerations. The proposed amplifier is designed and analyzed. While designing the amplifier, the feasibility of noise shaping, plant poles-zero compensation, and cable capacitance compensation is evaluated. The simulation and modeling show that the amplifier can meet all required specifications.

A measurement plan is made to test the amplifier before implementing the hardware and firmware part of the proposed amplifier. Due to the time limitations, the whole amplifier has not been able to do the evaluation. This decision was taken by the team. Besides the measurement of the performance, the future work comprises the following:

1. Increase the sample rate of the input signal. It will relieve the delay budget of the input reconstruction filter.
2. Design a program for automation of the design of the controller. It can be realized based on this work. See Section 3.4.
3. Update the minor adjustments in the analog circuits.
4. Make a design-in document for the future assignment.

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Reference

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Appendix A Simulation results

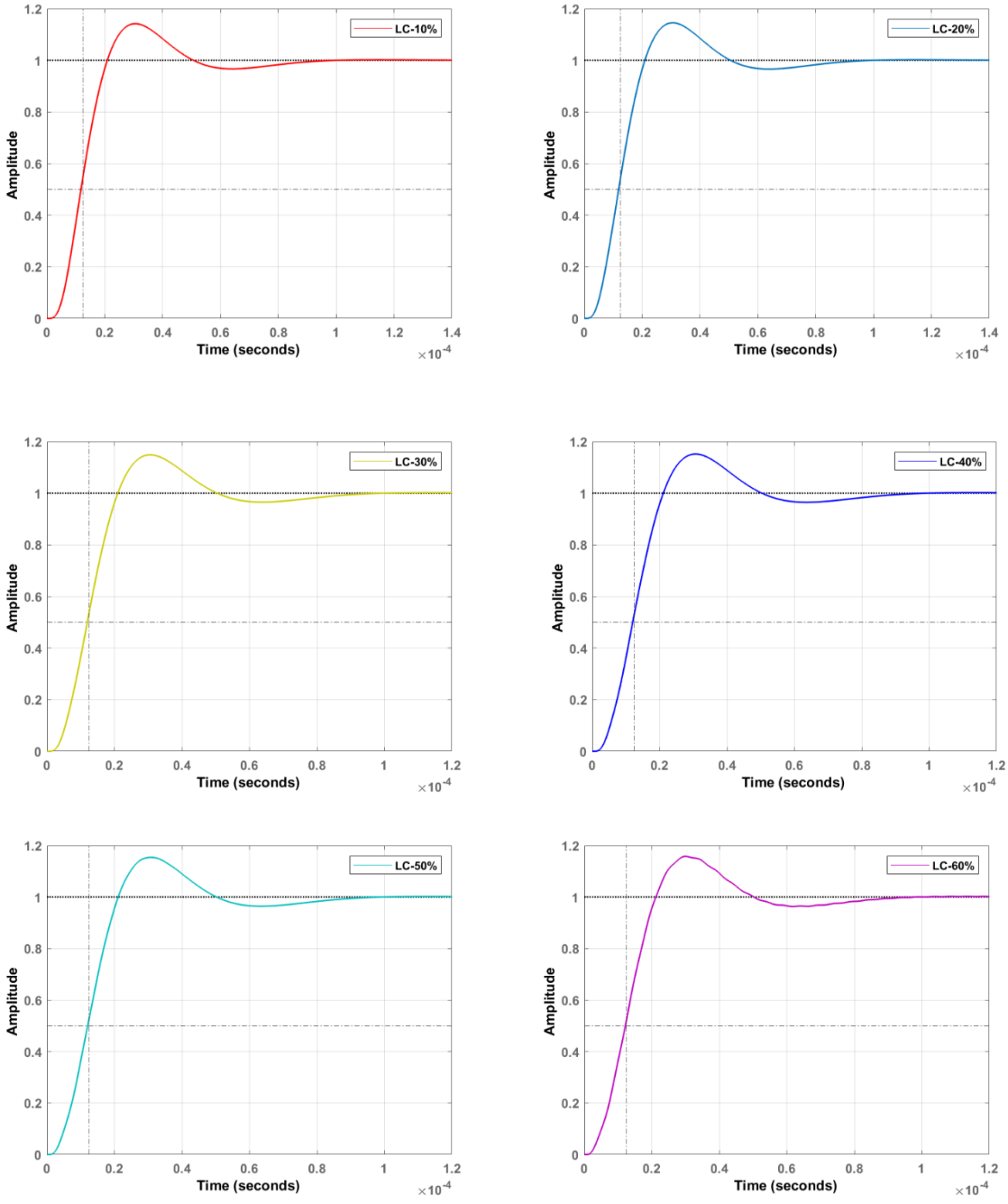


Figure A. 1 Step response of the amplifier when $C_{f,r} < C_{f,d}$, and $L_{m,r} < L_{f,d}$.

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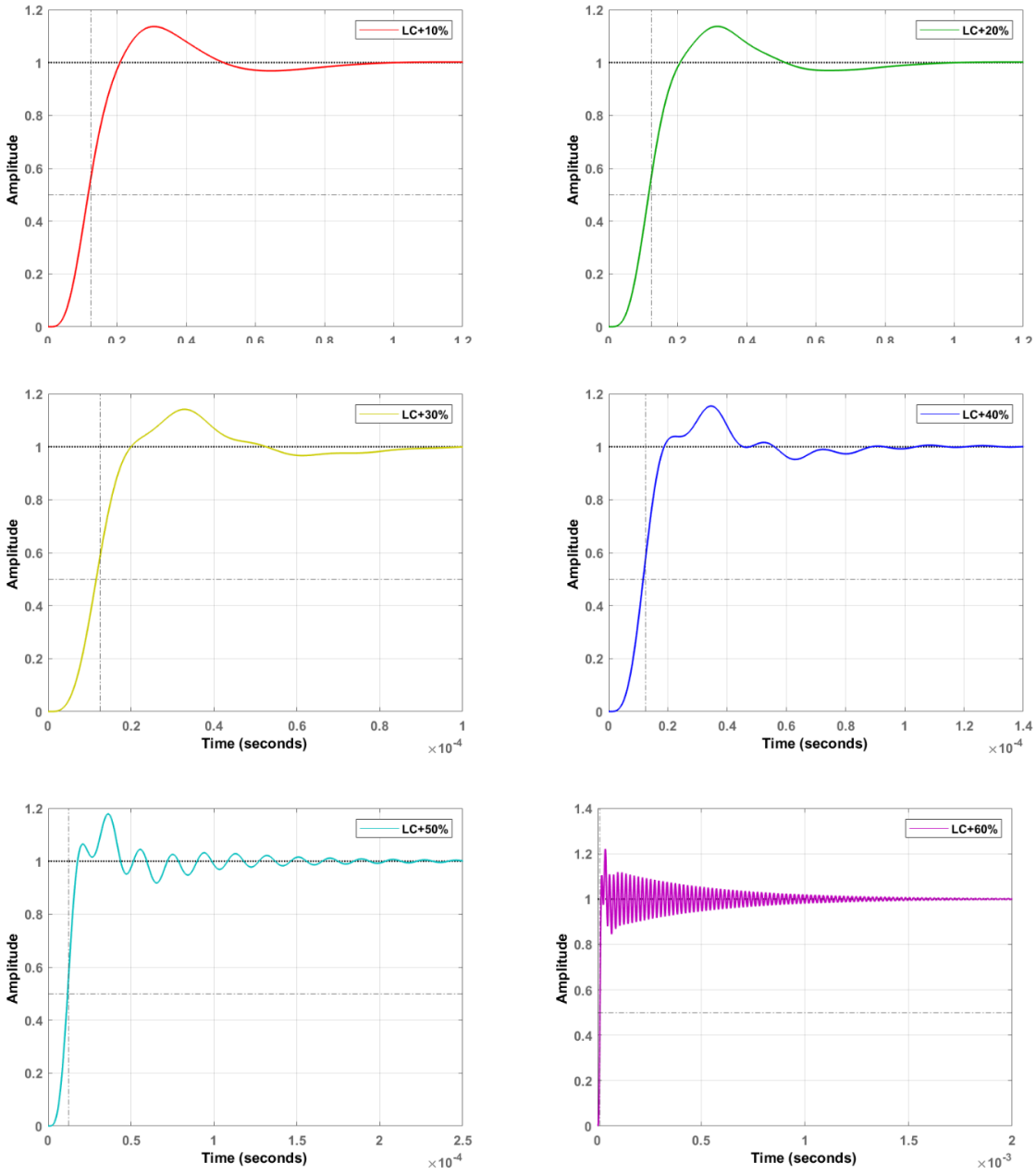
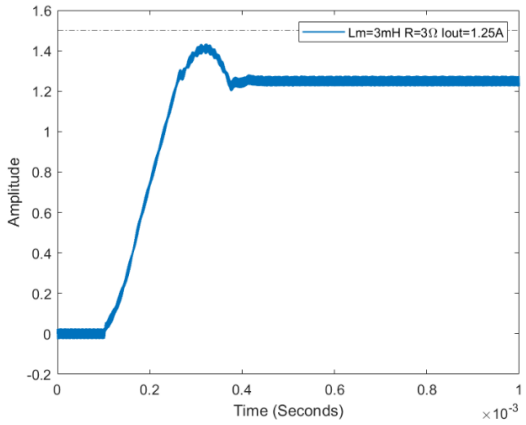
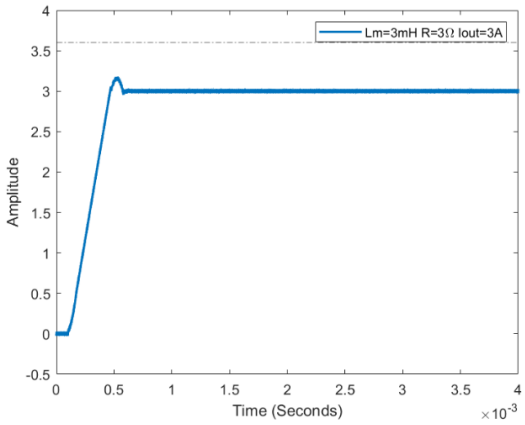
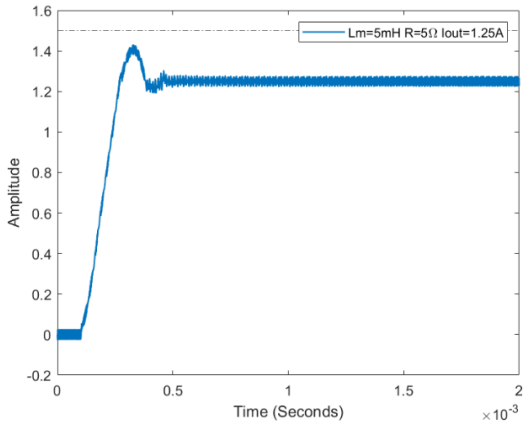


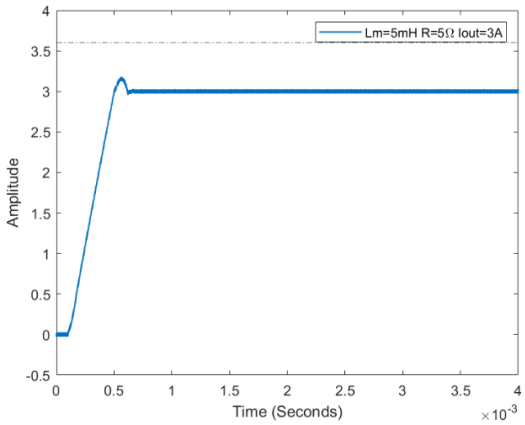
Figure A. 2 Step response of the amplifier when when $C_{f,r} > C_{f,d}$, and $L_{m,r} > L_{f,d}$.

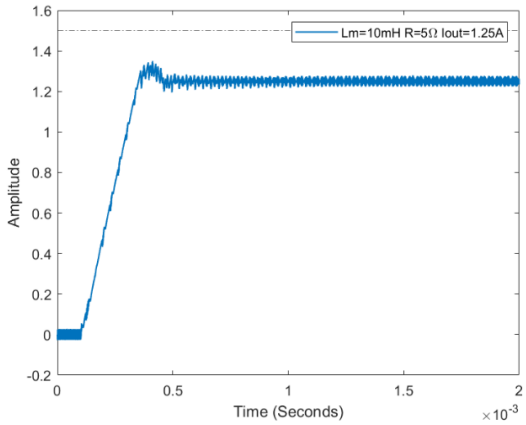
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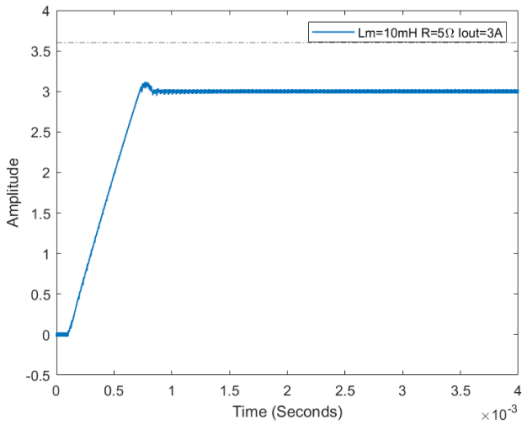












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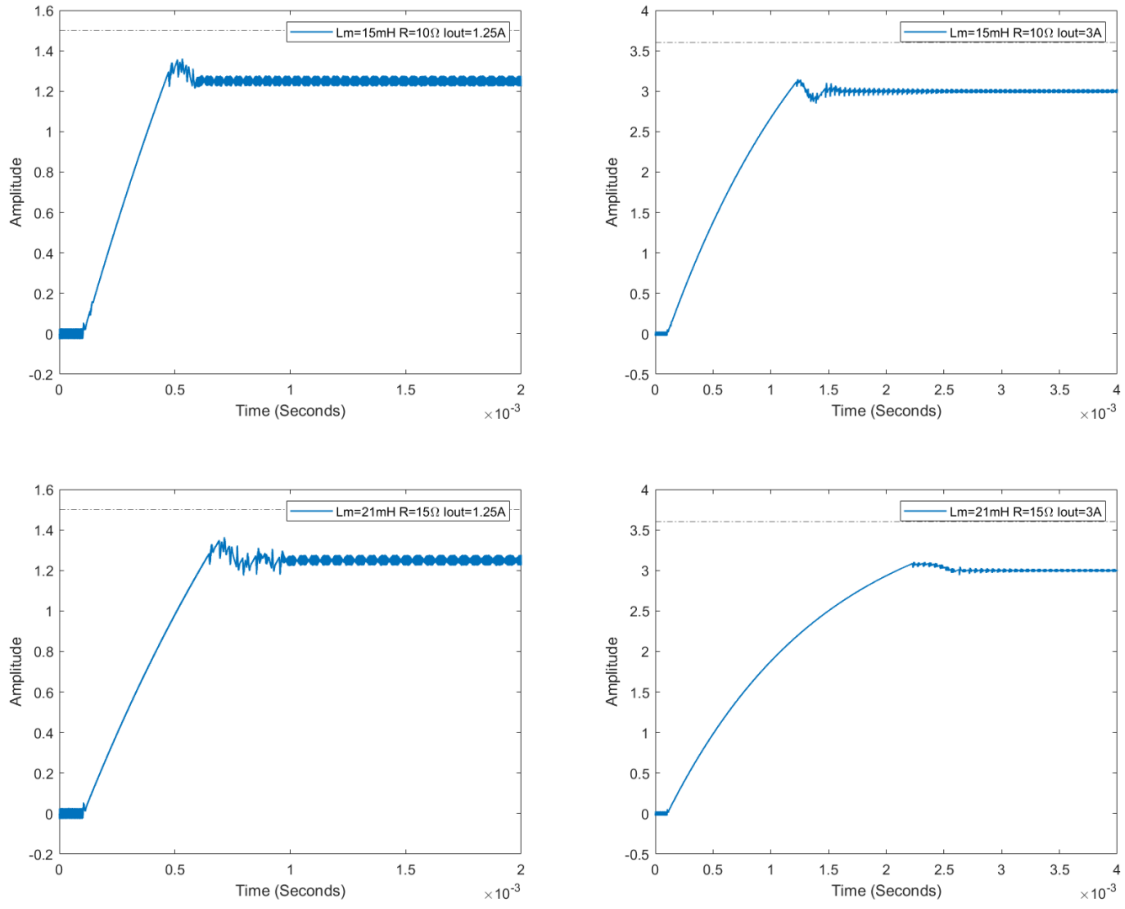


Figure A. 3 Large signal step response (Using Simulink model with large input signal)

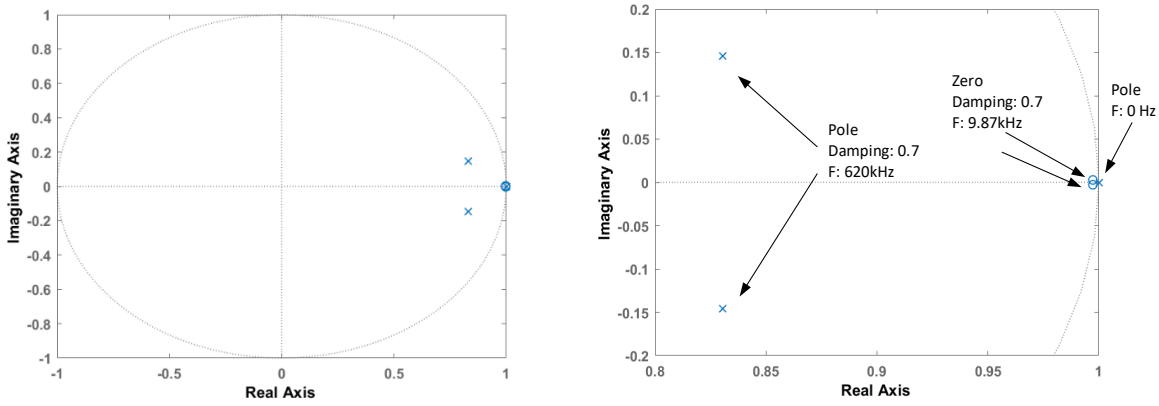


Figure A. 4 pole-zero plot of the noise shaper

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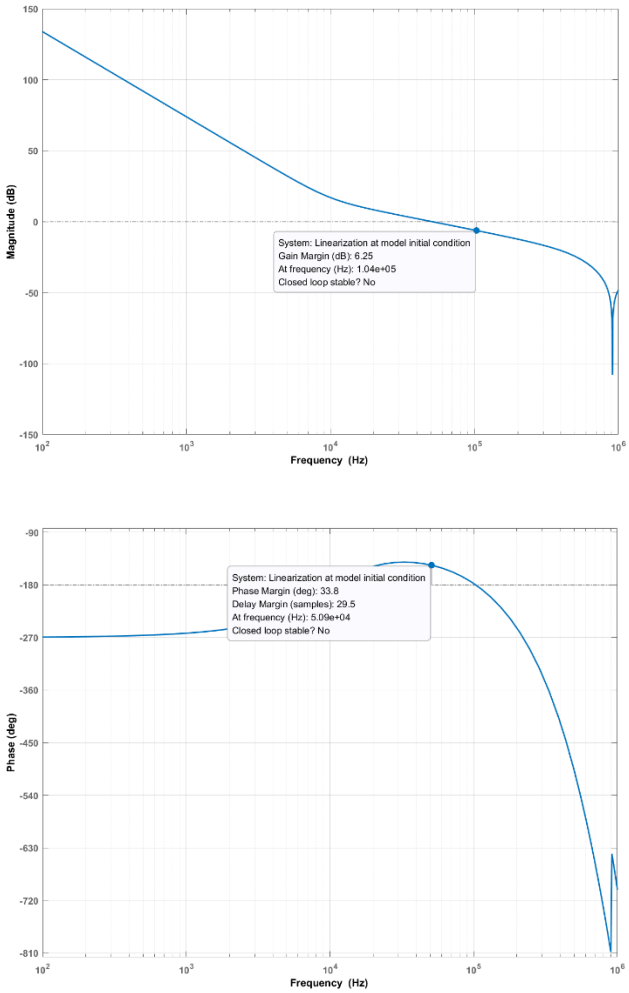


Figure A. 5 Transfer of the amplifier when the cable capacitance is 10 pF

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