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System in Package for Intelligent Lighting and Sensing Applications

Mingzhi DONG
董明智

Propositions

accompanying the dissertation

SYSTEM IN PACKAGE FOR INTELLIGENT LIGHTING AND SENSING APPLICATIONS

by

Mingzhi DONG

1. A successful system in package relies on accurate multi-physical analysis and robust fabrication process. The former makes it possible and the latter makes it real.
2. Silicon microfabrication provides new SiP designs with a fast validation tool, yet not necessarily best cost effectiveness.
3. The bottleneck of the miniaturization of particulate matter sensors will be the shrinking of the air flow generating system, which the silicon-based SiP approach cannot help much about.
4. Emerging development of Internet of Things (IoT) requires extensive integration of technology (IoT).
5. Scientific research never ceases to bring surprises no matter how well it has been planned.
6. Time management is not only about getting things done on time, but also about doing right things at right time.
7. The closer a specific technology is to one's life, the more motivated one feels to make contribution to the development.
8. To make one device work is science; to make one batch work is engineering.
9. Pursuing doctorate is a goal that serves to organize and measure one's best energies and skills, and challenge that helps achieve a better version of oneself.
10. Writing a thesis is not only a process of reviewing one's achievement, but also a process of reflecting on one's flaws and unfulfillment, thus leading to mixed feelings towards it.

These propositions are regarded as opposable and defendable, and have been approved as such by the supervisor prof. dr. G. Q. Zhang.

Stellingen

behorende bij het proefschrift

SYSTEM IN PACKAGE FOR INTELLIGENT LIGHTING AND SENSING APPLICATIONS

door

Mingzhi DONG

1. Een succesvol systeem in het pakket is gebaseerd op nauwkeurige multi-fysische analyse en robuuste fabricageproces. De voormalige maakt het mogelijk is en de laatste maakt het echt.
2. Silicon microfabrication biedt nieuw schip ontwerpen met een snelle validatie-instrument, maar niet per se de beste kosteneffectiviteit.
3. Het knelpunt van de miniaturisatie van fijn stof sensoren zullen het krimpen van de luchtstroom genererende systeem, dat de basis van silicium SiP aanpak niet veel over kan helpen.
4. Het onstaan van het "Internet of Things"(IoT) vereist extensieve intergratie van technologie (IoT).
5. Wetenschappelijk onderzoek zal altijd blijven verassen hoe goed het ook gepland is.
6. Tijdsmanagement gaat niet enkel en alleen over het op tijd af krijgen van zaken, maar ook over de juiste dingen op het juiste moment doen.
7. Hoe dichter een technolgie tot het eigen leven staat, hoe meer gemotiveerd iemand zich zal voelen om bij te dragen aan de ontwikkeling ervan.
8. Het laten functioneren van het product is aan de wetenschap; het maken van een partij is aan het ingineurswezen.
9. Het najagen van een doctoraat is een doel dat mede iemands vaardigheden en kunnen helpt organiseren en meten, en creert de mogelijkheid zichzelf te verbeteren.
10. Het schrijven van een thesis is niet alleen een proces waarbij iemands prestaties worden beoordeeld, maar ook een process van reflectie op iemands fouten en onvolkomendheden, wat leidt tot gemixte gevoelens jegens de thesis.

Deze stellingen worden opponeerbaar en verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotor prof. dr. G. Q. Zhang.

SYSTEM IN PACKAGE FOR INTELLIGENT LIGHTING AND SENSING APPLICATIONS

SYSTEM IN PACKAGE FOR INTELLIGENT LIGHTING AND SENSING APPLICATIONS

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K. C. A. M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 19 september 2016 om 10:00 uur

door

Mingzhi DONG

Master of Science, Tsinghua University
geboren te Fushun, China.

Dit proefschrift is goedgekeurd door de promotor:

Prof. dr. G. Q. Zhang

Samenstelling promotiecommissie:

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PREFACE

To my Mom

致：我的母亲

Mingzhi Dong
Delft, July 2016

CONTENTS

1

INTRODUCTION

1.1. BACKGROUND

Human beings have entered era of "intelligence" and we have seen enormous advances in many aspects of our daily life. The human society is quickly transformed by knowledge accumulation and technology innovation. Man effort goes especially towards a self-learning and self-sustainable environment. The concept of "smart device" has penetrated into cities and communities, houses and vehicles, as well as many industries [1–3]. As more and more smart devices are equipped in our surroundings or even on or in our body, two main requirements are raised towards the devices themselves: increased functionalities and increased miniaturization. These requirements happen to reflect the mainstream trend in microelectronics industry. For decades the microelectronics industry has been fueled by Moore's law and the outcome is today's powerful integrated circuit (IC) with more functionalities and smaller sizes than ever before [4]. The "smart" trend in our daily lives is possible because of the development in the microelectronic industry. On the other hand, the increased functionalities and miniaturization can also be achieved through system level integration which goes beyond the boundaries of Moore's law into the area of "More than Moore" (or MtM). MtM refers to all technologies enabling nondigital functions that do not simply scale with Moore's law, but provide additional value in different ways - to migrate from the system board-level into the package (or system in package, SiP) or onto the chip [5]. Such combination of digital function with complementary non-digital content is depicted in Figure 1.1. In the following paragraphs, two key enabling technologies for MtM, SiP and wafer level packaging (WLP), will be introduced.

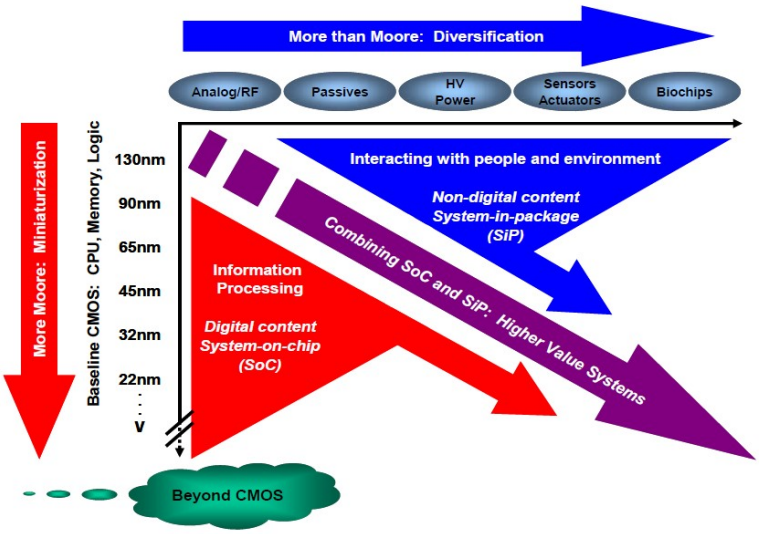

Figure 1.1: Dual trend in the International Technology Roadmap for Semiconductors (ITRS): diversification and miniaturization [6].

1.1.1. SiP TECHNOLOGY

In general, MtM requires higher density of functionality beyond chip level and this drives the integration of function to migrate from board-level to package-level. The concept of SiP has been gaining popularity due to its capability to fulfill the semiconductor industry demands for higher level of integration and lower costs. From the ITRS white paper, SiP is defined as “a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system. A SiP may optionally contain passive devices, MEMS (micro-electro-mechanical systems), optical components and other packages and devices" [7]. Figure 1.2 depicts the major categories of SiP structures [8].

SiP possesses many advantages as an enabling technology of MtM [7]. It provides smaller form factor compare with discrete individually packaged devices. SiP enhances the system performance by means of shorter interconnections and better shielding. More importantly, it reduces time-to-market through concurrent development of module and system, more design flexibility and easy redesign. For volume production, the concept of SiP also helps reduce the cost by eliminating the IC packaging process and increasing yield. Besides, SiP has the generic compatibility with heterogeneous integration of various die technologies including Si, GaAs, SiGe, SOI, MEMS, etc., providing great benefit for MtM system integration [9].

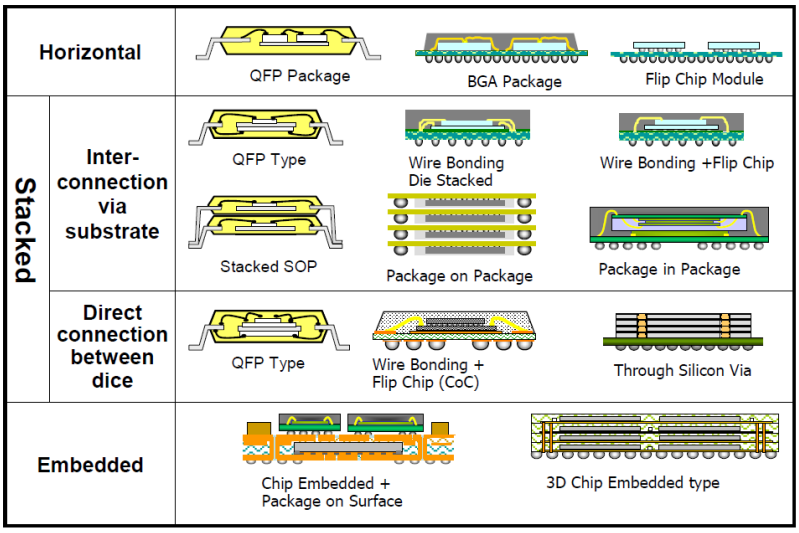

Figure 1.2: Examples of SiP structures which can be generally divided into three categories: horizontal placement, stacked structures, and embedded structures [8].

1.1.2. WAFER LEVEL PACKAGING

As more functionalities are integrated into one single package, the miniaturization of packaging becomes challenging. WLP has become a promising solution for highly integrated packaging [4]. WLP inherently enables the miniaturization of a package and thus a system since the achieved package owns almost the same size of the die. To realize 3D WLP, one of the key enabling technologies is the vertical interconnection between wafers, such as the most widely used through-silicon-via (TSV) approach. The attempt of implementing TSV technology into semiconductor industry has been trying for many years. However, due to many critical issues of this technology, the introduction into high volume manufacture has been hindered [10]. Different TSV players provide varied solution based on their unique technical strength, whereas the applications of TSV can be broadly categorized into three types [10]:

(a) vertical interconnection to the backside of the wafer, with no die stacking, enabling chip-scale-packaging (CSP) by eliminating the reserved space for input/output (I/O) pads;

(b) 2.5D integration, or TSV-enabled interposer technology, while the Si interposer acts as a packaging substrate for multiple dies mounted side-by-side on it; and

(c) 3D integration, where active dies are equipped with TSVs and stacked on each

other to form a die stack, which is expected to be the ultimate application of TSVs.

The WLP design equipped with TSV will become clear in following chapters of this thesis. Different from conventional TSV, dedicated process is oriented by the smart device applications and serves in the silicon interposer of 2.5D integration.

1.2. APPLICATIONS ENABLED MTM

1.2.1. FUNCTION ENRICHMENT IN SOLID STATE LIGHTING

Solid state lighting (SSL) refers to "a type of lighting that uses semiconductor light emitting diodes (LEDs), organic light emitting diodes (OLED), or polymer light emitting diodes (PLED) as sources of illumination rather than electrical filaments, plasma (used in arc lamps such as fluorescent lamps), or gas" [11]. Among all, LEDs are most used light source currently and gaining increasing interest from various applications due to the many advantages over traditional incandescent light source such as, "lower energy consumption, longer lifetime, improved physical robustness, smaller size, and faster switching" [12].

Traditionally the LED chips are packaged individually and used as discrete devices in systems. Nowadays, however, intelligent lighting applications require the LED package or module to deliver more functionalities while maintain small form factor. Currently available technologies for LED packaging are inherited from traditional IC industry that when applied to LEDs can often not fulfill the requirements. Common practice for consumer electronics in terms of packaging and assembly is mother circuit board plus packaged discrete devices. The problems of such solution for intelligent lighting applications are quite evident. First of all, the bulkiness of board level assembly hinders some application scenarios where the space is restricted. To reduce the system size, getting rid of the device package can be one way. As mentioned in Section 1.1, novel packaging methods are gaining popularity. Second of all, thermal management is crucial for LED applications because the heat density of the LEDs is relatively high. For applications to which form factor or cost is of little concern, the thermal issue can be solved by using large and complicated heat dissipation system. In other cases, neither the size nor the cost is affordable. Traditional board level assembly exhibits serious thermal issues for LED applications when more functionalities, meaning more components, are integrated. Last but not least, the market never stops seeking cheaper solutions. There is little room for cost reduction in the field of traditional packaging besides reducing material cost. Cost economical process for massive production is one direction where endeavors are kept inputting.

To find solutions for the aforementioned issues, attempts have been continuously made [13]. One direction is the adoption of silicon in the packaging and silicon-based SiP. The popularity of silicon comes from its unique features over other candidate materials, including high thermal and mechanical properties and compatibility with IC / MEMS processing. Moreover, the involvement of silicon means introducing semiconductor process into the LED packaging field. One of the obvious benefits of such introduction is the fact that tradition IC industry has developed a whole set of cost control strategy. Process-wise, technology like wafer level processing can greatly reduce the cost. Facility-wise, currently existed IC fabrication and packaging lines are accessible for emerging applications. Some key progresses will be reviewed in this section to show the technical directions.

As early as the year of 2006, Tsou developed a silicon-based packaging platform with embedded solder interconnections for LEDs (Figure 1.3 (a)) [14]. The presented novel package design was enabled by silicon micromachining and proved to enhance the reliability and thermal management of high power LED packages. Clearly stated in the paper was that the technique could help achieve low-cost process by incorporating the advantages of traditional IC and MEMS packaging together, such as batch processing. Lee's research group has done extensive investigations on WLP process for LED applications. Wafer level lens molding process is fulfilled by integrated deep reactive-ion etching (DRIE) trenches without using any mold. Such process can be implemented into LED encapsulation as well as optical lens molding, as shown in Figure 1.3 (b) [15–17]. Wafer level phosphor printing process is developed or white LED packaging with improved conformity [18], followed by further integration of phosphor printing with moldless encapsulation (Figure 1.3 (c))[19]. A recent progress demonstrates feasible integration of copper-filled TSVs for 3D interconnection (Figure 1.3 (d))[20], which proves to be a complete packaging process for LED packaging.

In industry, novel LED packaging technologies have also been demonstrated by various products. Philips demonstrated a fabrication technique for a multi-LED, multi-color module package (Figure 1.4 (a))[21]. This effort proves to be a first step towards high power LED packaging compatible with high working temperature. In 2007, Hymite released its new product HyLED^{TM}, a silicon wafer packaging solution for high brightness (HB) LEDs (Figure 1.4 (b))[22]. As stated in the paper, the solution provides excellent thermal performance and satisfying reliability. TSMC and its subsidiary VisEra announced their new packaging technology for HB LEDs based on 8-inch wafer production line (Figure 1.4 (c))[23–26]. In 2012, Toshiba proposed a novel WLP technology for white LEDs (Figure 1.4 (d))[27]. The technology was claimed to achieve extremely low

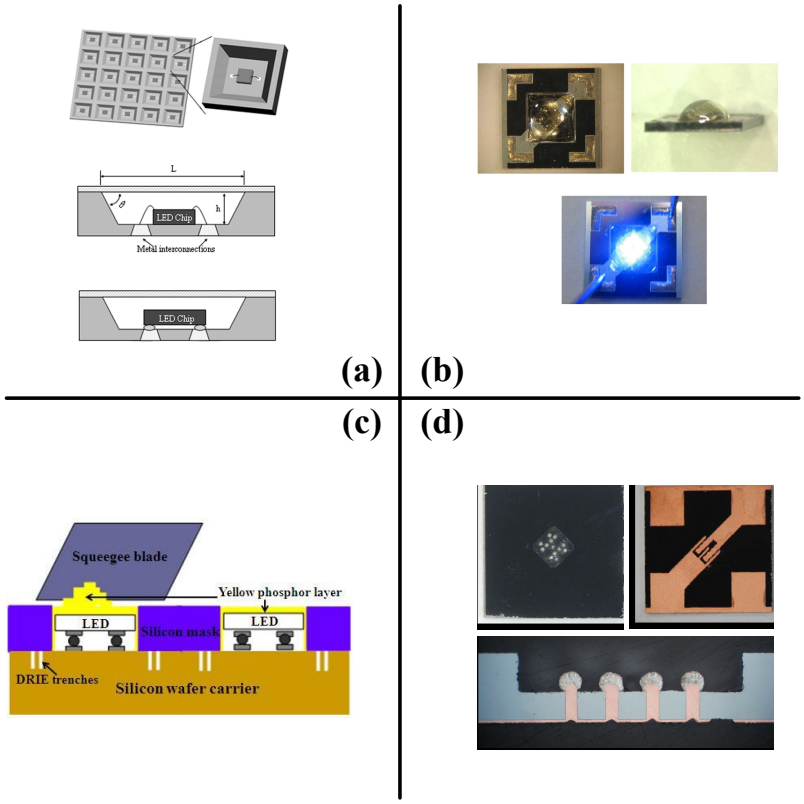

Figure 1.3: Silicon-based WLP for LEDs: (a) silicon-based packaging platform with embedded solder interconnections [14]; (b) wafer level LED encapsulation [15–17]; (c) wafer level phosphor printing [19]; (d) WLP for LEDs with integrated TSVs [20].

cost and small size and the package was confirmed to display enough robustness and excellent thermal performance.

Though most of the above efforts provide wafer level or batch process, the output is mainly single LED package with no integrated functionality. Since one of the advantages of the silicon material is to enable direct integration of intelligence, using silicon simply as packaging substrate or submount seems to be a waste of talent. Samsung presented a new concept of multi-chip LED package with integrated thermal trenches and electrodes in silicon substrate (Figure 1.5 (a))[28]. The design was proved to provide enhanced thermal performance as well as improved light efficiency. LG Innotek demonstrated WLP design for white LEDs with multi-chip LEDs (Figure 1.5 (b))[29]. It made

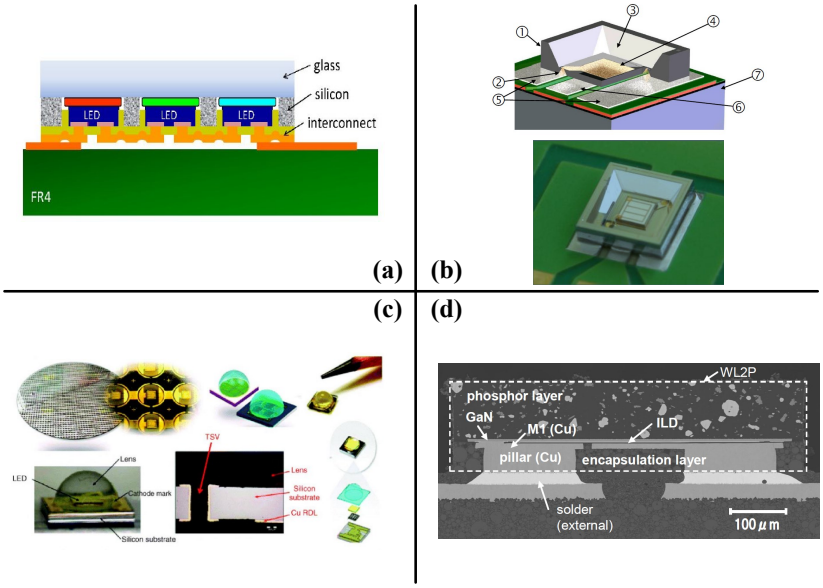

Figure 1.4: Industrialized silicon packaging for LEDs: (a) multi-LED, multi-color module package [21]; (b) silicon-based HB LED package from Hymite [22]; (c) silicon-based HB LED package from TSMC [23, 24]; (d) WLP for white LEDs [27].

a further step of silicon integration by fabricating Zener diode in the silicon submount to facilitate thermal management of the LEDs. Similarly, EV Group also demonstrated the integration of Zener diode in their total solution of silicon-based WLP for HB-LEDs (Figure 1.5 (c))[30]. NXP made further attempt in the same direction (Figure 1.5 (d))[31]. Instead of silicon, a piece of PCB is used to demonstrate the design concept. The proposed LED SiP consists of LEDs, driver dies, and passive components, all of which are hosted on a QFN (quad-flat no-leads)-like package. In the following chapters of this thesis, silicon-based packaging platform for LED packages will be presented and a fully integrated SiP for smart LED module will be demonstrated.

1.2.2. MINIATURIZATION OF PARTICULATE MATTER SENSOR

Particulate matter, or PM, is the term for a mixture of solid particles and liquid droplets found in the air [32]. With the increase of human activities, both living and manufacturing, over-exhausted particles in the air has become serious issue to human health [33–36]. More and more researches indicate that long-time exposure to particle polluted air is linked to many diseases. To avoid unhealthy exposure, people have demanding

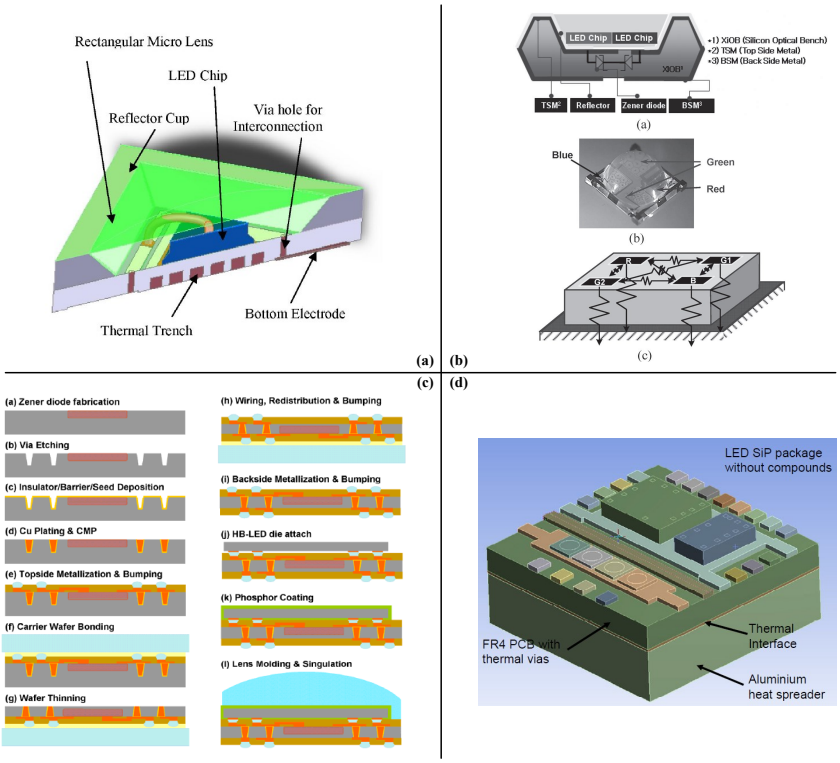

Figure 1.5: Industrial attempt for system integration in silicon packaging for LEDs: (a) multi-chip LED package with integrated silicon-based thermal trenches and electrodes [28]; (b) WLP for white LEDs with multi-LEDs [29]; (c) silicon-based WLP for HB-LEDs with integrated Zener diode [30]; (d) PCB-based SiP for LED module [31].

desire to monitor the air quality, preferably at economical cost. In general, the finer the particles are, the more damage they will pose on human bodies because the deeper they can penetrate into the body. Real-time monitoring fine particles in the atmosphere has been a quite hot topic.

In laboratories, scientists have plenty of tools and methods to measure the particle concentration in sampled air. However, tools that do not require much professional knowledge or complicated operational procedures are not widely available. Especially, when required high measuring accuracy, few candidates can deliver satisfying performances. Different principles can be employed for measuring PM concentration, among which the optical methods, such as light scattering method, are most widely used in low cost monitors. The Sharp GP2Y1010 sensor is among the first commercial dust sensors with small size and low cost that to some extent can be used to monitor PM concentra-

tion [37]. Plenty of literatures are available online about the characterization and validation of this sensor and all validate that for this sensor PM concentration can be detected but only through careful calibration with trustable reference monitors. For instance, the TECO research group has conducted extensive validation of the Sharp sensor using their customized toolkit [38–41]. Some open access resource also demonstrates the application of the Sharp sensor [42]. Similar sensor from Shinyei (PPD42NS) has also been investigated on the performance and the characterization [43–48]. DSM501 is another dust sensor module from Samyoung but so far no validation results are available online [49]. In the evaluation report from US Environmental Protection Agency in 2014, several inexpensive portable PM monitors were evaluated at field conditions [50], and the same agency also provide a guidance for the selection of such sensors for personal use [51].

Silicon-based microfabrication provides the possibility of making very small devices and thus attracts increasing research interest for miniaturization of PM sensors [52]. Beside the optical methods, other methods including film bulk acoustic resonator(FBAR) [53], electrical low pressure impactor (ELPI) [54] and I-shaped bulk acoustic resonator (IBAR) [55] have also been investigated and sensors based on these methods are realized by silicon microfabrication, as shown in Figure 1.6. Beside the feasibility of miniaturization, the silicon-based process will enable further integration, as described in Section 1.1, and provide more benefits such as cost effectiveness. In this thesis, silicon microfabrication enabled PM sensor design will be presented with design optimization and full characterization.

1.3. RESEARCH OBJECTIVE

This thesis focuses on developing novel SiP approach serving the need of MtM. The proposed approach is designed to serve applications with such requirements as highly integrated functionality but compact form factor, multi-physical design involved but simple fabrication process required, high reliability but low cost. These challenging trade-offs are the main obstacles that this research is set to overcome. One of the research approach employed in this thesis is the combination of the development of common design rules and the demonstration of specific applications. The design rules deal with the shared elements or aspects in the development of individual applications, and provide a technology platform for related applications. More considerations need to be taken into account when it comes to certain application based on the common platform. Multi-physical design will be intensely addressed in this thesis as it is the most challenging part in such system design, whereas the most valuable novelty of this research to the whole community.

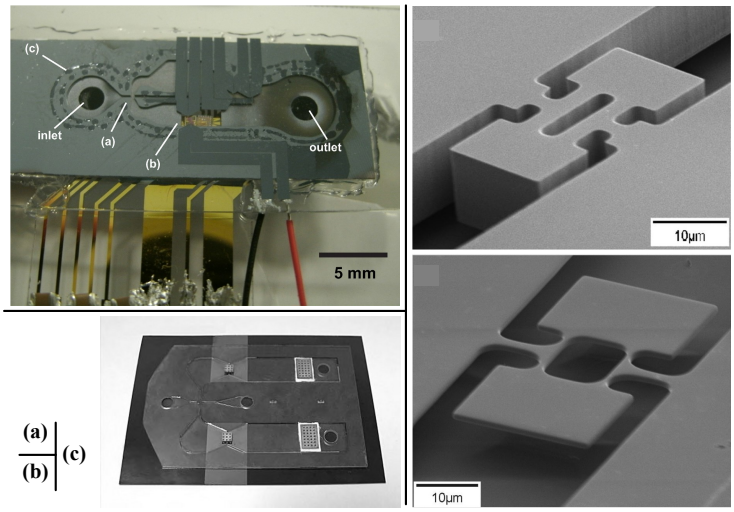

Figure 1.6: Silicon microfabrication enabled miniaturized PM sensor based on different operation methods: (a) FBAR [53]; (b) ELPI [54]; (c) IBAR [55].

1.4. THESIS OUTLINE

The rest of this thesis is structured as follows. Chapter 2 focuses on the silicon-based packaging design for SSL applications. Simulation assisted thermal analysis is firstly presented on three subjects: remote phosphor, integrated IC and stacked submounts. In a white LED package, phosphor acts as the color converter and the degradation of its performance highly depends on the working temperature. The remote phosphor design is an effective approach to improve the lifetime of phosphor and the LED module. Smart LED modules include LEDs, ICs, controllers and even sensors. The temperature of IC chips is strongly affected by the LEDs, the main source of heat. Thermal design is also conducted on a stacked silicon submount module, proposed approach for 3D SiP for SSL applications. Optical analysis is performed for silicon-based LED packaging to evaluate the light effect of silicon substrate. Some key processes widely used in silicon-based SSL packaging are also presented in Chapter 2. Special treatment is needed for metallization in deep cavity to obtain high quality of fabrication. Vertical interconnection is another enabling design for system integration. Conventional TSV does not always fit the need of heterogeneous integration. More dedicated and cost effective approach is presented in Chapter 2. As important parts of a electronic system, passive devices cost comparable area with ICs. Different designs for embedding passive devices into silicon submount are demonstrated at the end of Chapter 2. Based on the analysis in Chapter 2, Chap-

ter 3 focuses on fulfilling a miniaturized 3D SiP design for a smart lighting module. The multi-physical analysis is firstly performed based on the specific features of the application, covering thermal management, optical optimization and interconnection design. The SiP module is realized by silicon microfabrication and WLP process. Full characterization is conducted and the module shows satisfying performance in terms of thermal and optical parameters, proving the presented SiP design as promising approach for miniaturization of smart lighting application.

With the increasing public awareness of the impact of PM on human health, real-time monitoring of PM exposure level has attracted more interest than ever before. Chosen as another application scenario of MtM, miniaturized PM sensor is realized and presented in Chapter 4. Multi-physical analysis is needed for PM sensor design, but with more focus on enabling high sensitivity and accuracy of the measurement. Silicon microfabrication is used to realize the sensor. The testing results reveal that the sensor displays excellent performance, including high sensitivity and accuracy, low power consumption and compact size. In Chapter 5, an integrated virtual impactor (VI) is added to the PM sensor to enable detection of PM concentration in different size fractions. The design of the VI is optimized by both theoretical and simulation analysis. Systematic characterization and calibration is explained in detail in this chapter.

In Chapter 6 the main conclusions of this thesis are summarized. The achievement of this thesis opens more room for future potential applications as well as further technology development. An outlook towards the future work is also given at the end of the thesis.

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2

SILICON-BASED PACKAGING FOR SSL APPLICATIONS

Applications such as SSL embrace multi-physics design requirement. Besides optical consideration, thermal management is of great importance. This chapter focuses on the silicon-based packaging design for SSL applications. Simulation assisted thermal analysis is firstly presented on three key elements of SSL packages: phosphor, integrated IC and submount. In a white LED package, phosphor is used to convert color and the degradation of its performance links to the working temperature. The remote phosphor design is analysed and optimized. Smart LED module integrates LEDs, drivers, controllers and even sensors into a single package. The temperature of integrated ICs is strongly affected by LEDs, the main source of heat. Thermal analysis is also conducted on a structure of stacked silicon submounts, proposed approach for 3D SiP for SSL applications. Optical analysis is performed on silicon-based LED package to evaluate the light effect of the silicon submount. Several key processes development and optimization are also presented in this chapter. Metallization in cavity, commonly used in silicon -based packaging, needs special treatment to obtain high quality of fabrication. Another key enabling design is the interconnection within the integrated system. Conventional TSV does not always fit the need of heterogeneous integration. More robust and cost effective approach is presented in this chapter. As important parts of a electronic system, passive devices cost comparable area with ICs. Different designs for embedding passive devices into silicon submount are demonstrated at the end of this chapter.

Parts of this chapter have been published in Journal of Semiconductors **34**, 5 (2013) [1] and Proceedings of 9th China International Forum on Solid State Lighting (ChinaSSL) (2012)[2, 3].

2.1. INTRODUCTION

SSL, represented by LEDs, has been rapidly replacing the traditional luminaires due to longer lifetime and lower energy consumption. For decades, man effort has been put into increasing light output of LED chips and reducing the cost to make the LED bulbs competitive with traditional luminaires. Recently, increasing need for smart lighting has emerged in our daily life that is made possible by the introduction of the LED itself and the need for cost reduction. Compared with other light sources, LEDs provide more colorful and tunable light. In era of MtM, smart lighting applications is embracing the trend of increased functionality and miniaturization. From the aspect of electronic packaging, new supporting technologies need to be developed.

Current approach for lighting system integration, like Philips hue bulbs, is based on standard printed circuit board (PCB) assembly [4]. The intrinsic bulkiness of this approach obstructs further function enrichment and miniaturization. Besides, thermal management of such system is extremely challenging. SiP technology has recently emerged and already shown potential in applications of radio frequency (RF) and networking. So far, SiP design for lighting system is quite new. Gielen proposed a design of intelligent integration of LED system, in which standard PCB was used as packaging substrate [5]. However, for LED applications, the main barriers for the implementation of PCB or other polymer-based substrates are insufficient thermal dissipation and coefficient of thermal expansion (CTE) mismatch-induced issues, such as unexpected warpage.

This chapter presents silicon-based packaging design for miniaturization of SSL applications. Thermal analysis is conducted on key elements of SSL packages. Optical effect of silicon submount is evaluated. Several dedicated process for SSL packaging are developed and presented. The design rules discussed in this chapter will be implemented and further demonstrated in Chapter 3 and can be used for other related applications, such sensor and MEMS packaging. The rest of this chapter is structured as follows. Section 2.2 discusses the simulation assisted thermal design on proposed SSL packaging. Optical design is presented in Section 2.3. Section 2.4 demonstrates several process development and a brief summary is given in Section 2.5.

2.2. THERMAL DESIGN

Thermal management is of great significance for SSL applications. At the device and packaging level, thermal design must be well taken care of so that the performance and lifetime of the whole system is guaranteed. In a LED package, materials with quite differ-

ent thermal properties are dealt with when it comes to thermal management. To better understand the thermal effect on different materials and thus reduce the thermal impact on key components, simulation based analysis has been conducted. In the following section, discussions will focus on thermal design for three main elements in LED packages: phosphor, integrated IC and silicon submount. The thermal analysis in this chapter mainly focuses on the effect of the dimensional parameters. Material property also plays significant role in the thermal management and this chapter will also investigate the effect of the thermal interface material (TIM) that is widely used in SSL packages and modules.

2.2.1. REMOTE PHOSPHOR

Phosphor plays an important role in white color LEDs. The property and degradation of phosphor highly depends on the working temperature, which is affected by heat generated by LED dies and phosphor itself [6, 7]. In most of current white LED products, phosphor is directly applied onto LED dies, known as direct phosphor. The problem with direct phosphor is the thermal degradation of phosphor material due to the contact with LED dies, the temperature of which can be as high as 100 °C. The term of remote phosphor stands for the way of placement of phosphor element within a white LED module. Unlike traditional blue light based white LED where the phosphor is applied on LED chips directly, in remote phosphor design the phosphor element is positioned remotely from the LED source, thus heating of the phosphor by the LED is reduced, ensuring excellent spectral stability over time. It has already been applied into some commercialized products, like Philips MasterLED lamps [8]. Although the solution is effective against fast phosphor degradation, it is, however, facing the difficulty of integration and miniaturization. Again take Philips, the design of remote phosphor is good enough for regular lighting but may not easily be integrated into smaller LED modules which is probably the direction of next generation LED development. Another point to be noticed is that current remote phosphor solutions consume large amount of phosphor material which is of higher and higher price, meaning the cost is another driving force for developing new remote phosphor technologies.

In our design, we propose a preform-based remote phosphor solution. In this approach, all LEDs and related driver circuitry are first encapsulated by polymer based material and then another preformed phosphor film is mounted on top. By this means, the phosphor and the LEDs are separated by a thin layer of polymer which acts as a thermal barrier to reduce the thermal impact on the phosphor.

MODULE DESCRIPTION

Phosphor is commonly used in LED package to convert the original light from the LED chips to get more colorful light or white light. Blue LEDs and red LEDs are usually used as light sources in the LED packages. Since individual LED acts as a point light source, to get conformal light output, multiple LEDs are placed in a package or luminaire. As a representative, a module consisting of thirteen LEDs is analysed in this section. Nine blue LEDs are arranged in a three-by-three array and four red LEDs form a two-by-two array, as shown in Figure 2.1. The cross-sectional structure is shown in Figure 2.2. All the LEDs are bonded onto a silicon substrate through TIM and then encapsulated by silicone. A layer of 3 μm oxide on silicon substrate is also taken into consideration. The phosphor power is mixed with silicone and then cured to form a layer of 500 μm on top of LEDs area. The whole module is attached onto an aluminum heat sink for heat dissipation. Dimensions of the module are listed in Table 2.1.

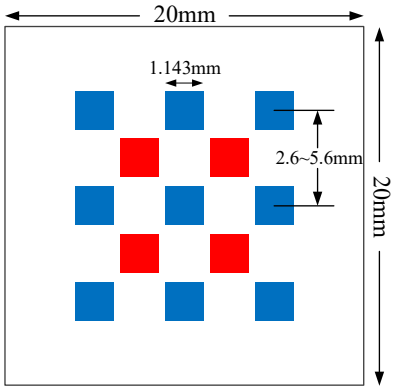

Figure 2.1: Layout of LEDs in the module (not to scale): nine blue LEDs (three-by-three array) and four red LEDs (two-by-two array).

SIMULATION MODEL

Finite element analysis (FEA) is a fast and effective way of investigating the effect of multiple systematic parameters and their interactions on the performance of a system. To evaluate the impact of the dimension of the LED module on the temperature distribution, FEA is firstly conducted by COMSOL [9] and the module of *heat transfer in solids* is used. The heat transfer mode considered in the analysis is conduction and convection while radiation that causes negligible effect is ignored. The heat is transferred through

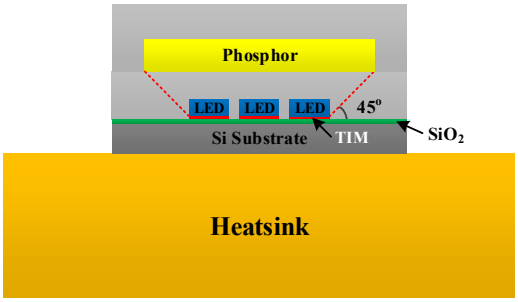

Figure 2.2: Cross-sectional view of the LED module (not to scale).

Table 2.1: Dimension of the LED module.

Component	Dimension
LED die	1143 µm × 1143 µm × 150 µm
LED module	20 mm × 20 mm × (1.5 ~ 3.5) mm
Heat sink	100 mm × 100 mm × 10 mm
TIM layer (thickness)	10 µm
Phosphor (thickness)	500 µm
Si substrate (thickness)	525 µm

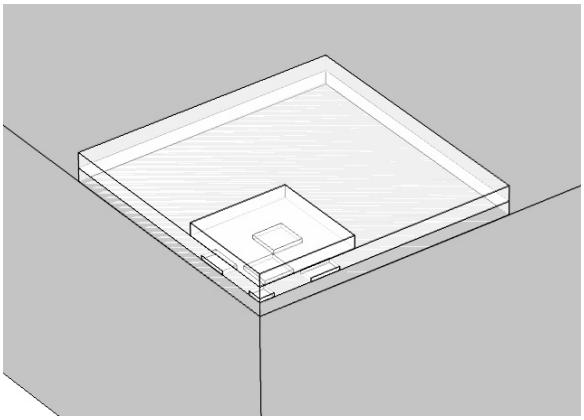

Figure 2.3: Quarterly simulation model for thermal analysis of LED module with remote phosphor.

conduction between inner material boundaries and the outer boundary of the module is naturally convected with air unless a fixed temperature is set on some surface to simulate

the heat sink. The initial temperature of the module is set at room temperature (20 °C). Given the symmetry of the module, a quarterly model is simulated to save computation time, as shown in Figure 2.3. The horizontal / vertical distance between the centers of neighboring LEDs (hereinafter mentioned as pitch) determines the heat density within the module as well as the size of the whole module. The thickness of silicone encapsulant over LEDs (hereinafter mentioned as silicone thickness) affects the heat transferring between the phosphor and the LEDs. The area of the phosphor layer is linked to the amount of the phosphor consumed in each module and thus relates to the cost. To better absorb the light from the LEDs, the area of phosphor is larger than the projected LEDs area to cover as wide range of emitting angle as possible. The LEDs emit beam-like light and the light intensity peaks along the emitting axis. As the viewing angle moves away from the emitting direction, the light intensity drops quickly [10]. To simplify the parameter setting in the modelling, the angle of 45° is chosen, shown in Figure 2.2, as the effective emitting angle. Any light beyond this angle is ignored. Such optical simplification does not affect the thermal simulation.

For the simulation, 1W LED is considered and the light efficiency is assumed to be 30 %, typical value for LEDs of high quality [11], that is, 70 % of the whole power is converted into heat and dissipated to the ambient. The phosphor itself can also generate heat when converting light. Typically, the conversion efficiency of commonly used phosphor is around 90 % [12], which is also used in our simulation. The ranges of pitch and silicone thickness are listed in Table 2.2. The properties of materials are listed in Table 2.3.

Table 2.2: Range of variables for simulation.

Variable	Range
Pitch	1.3 - 2.8 mm
Silicone thickness	0.5 - 3.5 mm

RESULTS AND DISCUSSION

Firstly, the effect of the pitch is investigated while the silicone thickness is set as 600 µm. Figure 2.4 shows a typical temperature distribution of the LED module.

The temperature of the phosphor is affected by the heat generated by LEDs and the phosphor itself. Even though the phosphor is encapsulated in silicone, the heat sink is still the dominant heat passage for phosphor due to the higher conductivity of heat sink material. This makes the heat generated inside the phosphor not easily get dissipated, so the temperature inside the phosphor is higher than LEDs.

Table 2.3: Thermal property of the materials used in the simulation.

Material	Thermal conductivity (W/(m×K)) [13]
LED (Al_2O_3)	35
Si	130
SiO_2	1.4
Silicone	0.22
TIM	10
Al	160

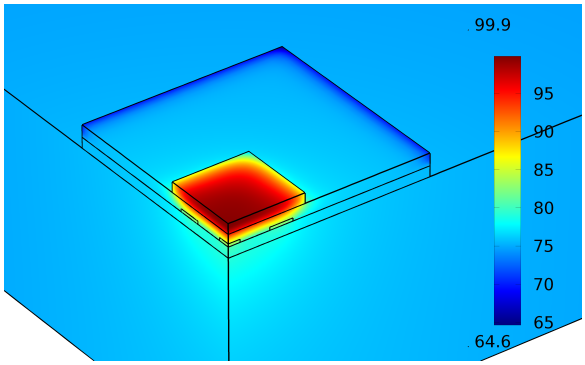

Figure 2.4: Temperature distribution of the LED module (pitch = 1.3 mm, silicone thickness = 0.6 mm).

Figure 2.5 shows the temperature of phosphor and LEDs with various pitches. According to the simulation results, with increasing pitch the maximum temperature of phosphor is decreased dramatically meanwhile the temperature of LEDs only shows slight decrease. Based on this fact, we can conclude that the main reason for the reduction of the phosphor temperature is the decrease of the heat generation density and increase of the total cooling surface of phosphor because the area of phosphor layer increases as a function of the pitch. When the phosphor layer area is large enough, in this case, when the pitch is larger than 2.8 mm, so that the self-generated heat is negligible, the maximum temperature of phosphor goes down close to the temperature of LEDs.

The second part of the simulation is to find out the relation between the silicone thickness and the phosphor temperature. With fixed pitch, the silicone thickness also shows impact on phosphor temperature according to the simulation results. Figure 2.6 shows the temperature of phosphor with different silicone thickness. With the increase of silicone thickness, the maximum temperature goes up first and then drops with further increase of silicone thickness. The silicone layer between the phosphor and the

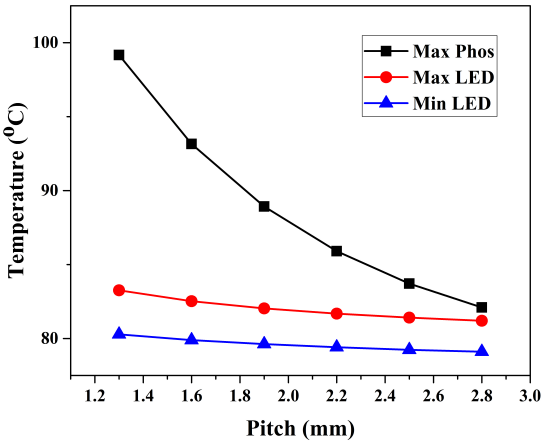

Figure 2.5: Temperature change with pitch: maximum temperature of phosphor (black); maximum (red) and minimum (blue) temperature of LEDs.

LEDs can affect the phosphor temperature from two aspects: this silicone layer can increase the thermal resistance of the heat passage between the phosphor layer and the heat sink; also the silicone layer will change the phosphor layer area which is directly linked with the heat-generation density and cooling surface area. Therefore, with increasing the silicone thickness, on one hand the thermal resistance will increase and thus tend to increase the phosphor temperature, on the other hand, the increased phosphor layer area which is a function of silicone thickness, lowers the heat-generation density inside the phosphor and enlarges the cooling surface which leads to lower phosphor temperature. In our case, before the silicone thickness reaches 1.5 mm the increase of thermal resistance dominates the trend of phosphor temperature and with further increased silicone; the factors that tend to cool down the phosphor are dominant. A temperature peak of around 90 °C appears at silicone thickness of 1.5 mm. Based on the above discussion, if enough room in vertical direction, thicker silicone layer, for our case thicker than 1.5 mm, is preferred. Otherwise, for products the size of those is highly limited vertically, designers should be aware of the trend of phosphor temperature and choose proper silicone thickness to avoid the peak value of phosphor temperature.

2.2.2. INTEGRATED IC

In conventional SSL module, packaged LEDs and driver ICs are assembled on PCBs, as shown in Figure 2.7. The type of the board can be metal-core PCB (MCPCB) or FR (flame

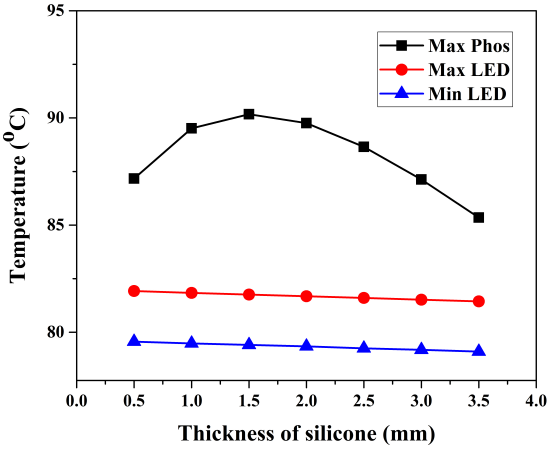

Figure 2.6: Temperature change with silicone thickness: maximum temperature of phosphor (black); maximum (red) and minimum (blue) temperature of LEDs.

retardant) 4-based PCB. However, with the increasing need for smaller and smarter lighting products, one potential solution is to integrate more components with LEDs, such as drivers, controllers and even sensors into a single package or module. The problem that comes with more integrated and compact packages is the thermal management of IC chips inside the packages. LEDs are the main source of heat in a LED module. When working, the LED temperature can be as high as 100 °C or even more for high power LEDs, while regular IC chips cannot withstand such high temperature. Typically, IC chips are designed to work under 85°C.

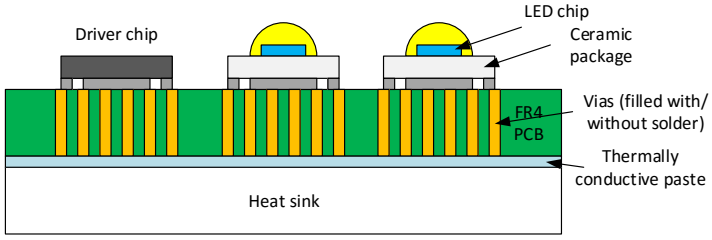

Figure 2.7: Crosss-sectional view of a conventional SSL module: packaged LEDs and ICs are separately mounted on PCB while the whole assembly is connected with a heat sink through TIM.

To solve this problem, there are two potential solutions: one is to enhance the ther-

mal tolerance of ICs and the other is to reduce the thermal impact of LEDs on ICs. The IC industry is a relatively mature industry and re-designing commonly used ICs would be neither cost-effective nor time-effective. In this section, we focus on finding out ways of reducing thermal impact of LEDs on ICs. The temperature distribution for integrated LED module is investigated and compared with the conventional SSL module.

SIMULATION MODEL

A nine-LED module integrated with four driver chips is used for simulation. For conventional SSL module, all LEDs are first packaged on ceramic substrates by a thin layer of TIM and then assembled with ICs (simulated as silicon) on a piece of PCB, as shown in Figure 2.8. For the integrated module, all the LEDs and driver ICs are mounted on a silicon substrate using TIM and then encapsulated by silicone, shown in Figure 2.9. The silicon substrate is attached on a piece of PCB through TIM. Quarterly model is simulated due to the symmetry of the module structure. The main dimensions of the models are listed in Table 2.4 and the thermal conductivity of the materials are listed in Table 2.5.

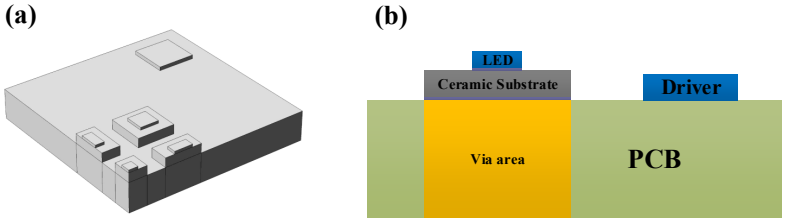

Figure 2.8: A conventional SSL module with nine LEDs and four ICs: (a)quarterly 3D model; (b) cross-sectional view.

Table 2.4: Demensions of simulation model.

Layer	Dimension
PCB	10 mm × 10 mm × 1.6 mm
Ceramic substrate	2 mm × 2 mm × 0.5 mm
Silicon substrate	12 mm × 12 mm × 0.8 mm
LED chip	1 mm × 1 mm × 150 µm
Driver chip	2 mm × 2 mm × 200 µm
LED distance	1 mm
Silicone thickness	1 mm

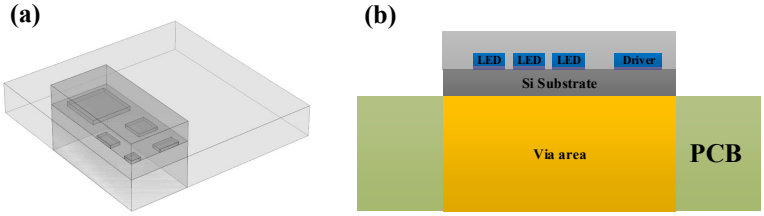

Figure 2.9: A integrated SSL module with nine LEDs and four ICs: (a)quarterly 3D model; (b) cross-sectional view.

Table 2.5: Material properties used in modelling.

Material	Thermal conductivity (W/(mK)) [13]
Ceramic substrate	25
FR4	0.3
FR4 + vias	10
TIM	50

To simulate the heat sink, the temperature of the backside PCB is fixed at 50 °C [14]. The PCB area under the LED packages and driver chips is with metal-filled via (effective thermal conductivity is set as 10 K/(mW)). The power of the driver chip is consumed as 0.5 W.

RESULTS AND DISCUSSION

Figure 2.10 shows the temperature distribution of a conventional SSL module with the LED power of 1 W. There is a 15-20 °C drop from the LED (90 °C) to the PCB (around 70 °C). The temperature of the IC (69 °C) is slightly higher than the PCB / heat sink, but still much lower than the LED. If LEDs with higher power (2 W) are used, the temperature of the IC is not increased at all, while the temperature of the LEDs reaches 130 °C. Due to the thermal separation between the LEDs and the ICs, the thermal impact from the LEDs is not a serious issue for the ICs in conventional SSL modules. Actually, in many products the driver chips are put on a separate PCB, which makes the concern even less serious or eliminated.

In the case of integrated SSL module, the same LED power (1 W) results in lower LED temperature (76 °C) than the one in the conventional module, as shown in Figure 2.11. This is due to the higher thermal conductivity of silicon substrate over the ceramic (Al_2O_3) substrate in traditional LED packages. Most of the heat generated in LEDs is

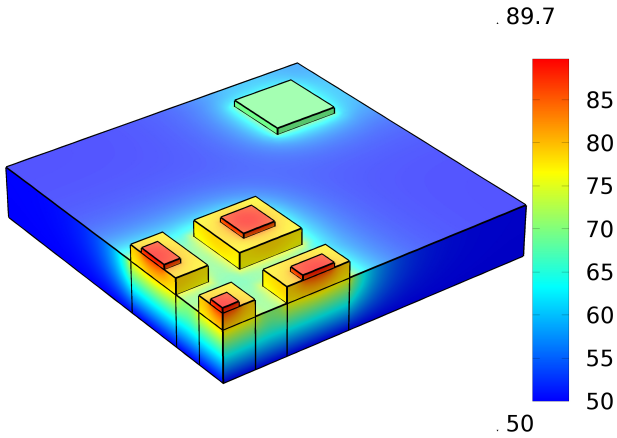

Figure 2.10: Temperature distribution of conventional SSL module with the LED power of 1 W.

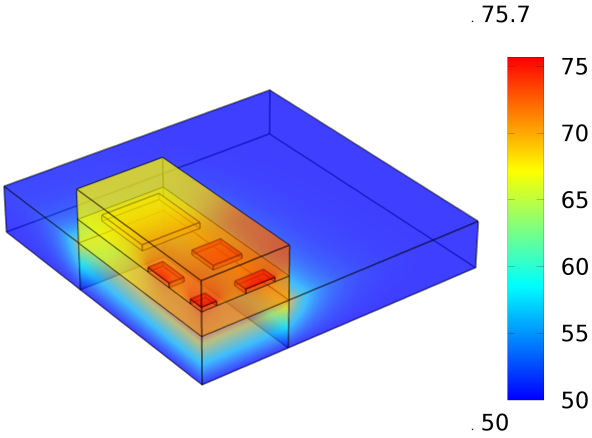

Figure 2.11: Temperature distribution of integrated SSL module with LED power of 1 W.

conducted through the substrate to the heat sink. The integrated IC also shows similar temperature (68 °C) which does not seem to be impacted by the LEDs. When the power of LEDs increases to 2 W, the temperature of the LEDs and the ICs are 98 °C and 81 °C, respectively. Compared with traditional SSL module, LEDs still benefit from silicon while the ICs suffer from the same silicon substrate. The high thermal conductivity of silicon can transfer heat in lateral direction and behaviors like a bridge of heat between the LEDs and the ICs. The simulation results are summarized in Table 2.6.

Although silicon-based WLP provides the benefit of miniaturization, the thermal in-

Table 2.6: Results of the thermal simulation.

Power of the LEDs		1 W	2 W
Temperature of conventional	LED	90	130
SSL module (°C)	IC	69	69
Temperature of conventional	LED	76	98
SSL module (°C)	IC	68	81

teraction between LEDs and ICs within SSL modules can be harmful. From the thermal management aspect, setting some thermal separation structure on the path of heat transfer can be effective approach. Figure 2.12 displays one possible design: based on the integrated SSL module, a trench is formed in the silicon substrate between the LEDs and the ICs; the encapsulant (for instance, silicone) fills the trench and acts as a thermal barrier duo to its lower thermal conductivity. Simulation result shows that by adding such thermal barrier the temperature of the ICs is reduced to 62 °C from 68 °C when the power of the LEDs is 1 W. Meanwhile, the temperature of the LEDs is slightly increased (1 °C). The thermal barrier blocks the heat generated by the LEDs from conducting laterally, which helps protect the integrated ICs from thermal damage and meanwhile lowers the efficiency of thermal dissipation of the LEDs. This trade-off needs to be considered especially when high power LED application involves.

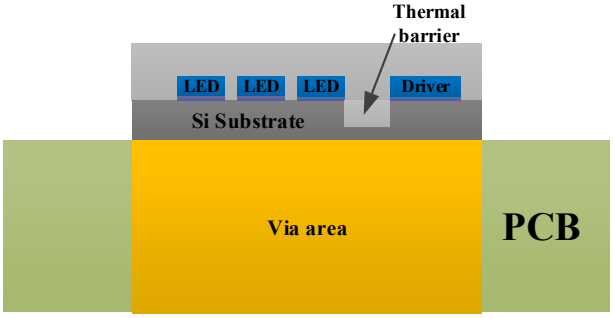

Figure 2.12: Silicone filled trench enabled thermal barrier design for integrated SSL module: the trench is formed in the silicon substrate and filled by silicone during encapsulation.

2.2.3. STACKED SILICON SUBMOUNTS

As the integration level and miniaturization increases for applications like SSL, the packaging extends from 2D structure to 3D. Chips, substrates and packages can all be stacked [15]. When substrates are stacked in a SSL package, thermal issue can be more serious. One of the benefits that silicon substrate provides is the high thermal conductivity (130 W/mK) over polymer-based laminates (0.2 W/mK). In this section, thermal analysis is studied between silicon and polymer PCB. TIM, as thermal grease for die attach and substrate stacking, is widely used in SSL packages. The effect of TIM property on the temperature of the package is also investigated in this section.

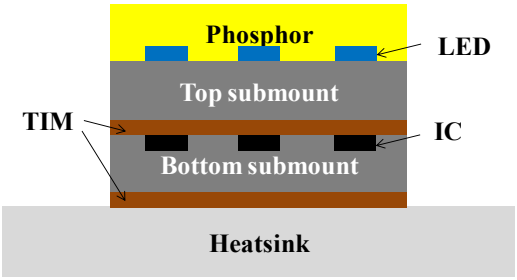

Figure 2.13: Cross-sectional view of integrated SSL module (not to scale): a stack of silicon submount with LEDs integrated on the top and ICs integrated on the bottom.

Figure 2.13 shows the structure of the proposed module with stacked silicon submounts. The top submount carries all the LEDs which are encapsulated with a layer of phosphor. The driver circuit components are embedded on the bottom submount. The two submounts are glued with TIM and the whole stack is adhered to a heat sink by the same TIM.

Table 2.7 summarizes the dimension and the material properties. The module contains 36 LEDs which are form into a 6×6 array and the total power is 6 W, of which 5.7 W consumed on the LEDs and 0.3 W on the driver circuit. For the simulation, the luminous efficiency of the LEDs are still set as 70 % and natural convection is set between the outer surface of the module and the ambient air with an initial temperature of 20°C.

The temperature distribution of the module is simulated with silicon and PCB as submounts, respectively, and the result is shown in Figure 2.14. The thermal conductivity of TIM is set as 5 W/mK. It is evident that silicon submount shows much higher efficiency of heat dissipation. The temperatures of the LEDs and ICs in each case are summarized in Table 2.8. The LEDs and ICs integrated on silicon submounts show much lower tem-

Table 2.7: Modelling parameters: thermal conductivity and dimension.

Material	Thermal conductivity (W/(mK)) [13]	Dimension (mm^2)	Thickness (mm)
Phosphor (Silicone)	0.22	17 × 17	1.0
LED	35	1 × 1	0.2
Silicon	130	17 × 17	0.5
PCB	0.5	17 × 17	0.5
TIM	1 ~ 30	17 × 17	0.1
Heatsink	50	100 (diameter)	2.0

perature than those on PCB submount. It is also noted that with silicon as submount, the temperature of the ICs is almost the same as the LEDs while in the case of PCB the LEDs show much higher temperature than the ICs because the heat dissipation from the LEDs through the ICs to the heat sink is blocked by lower thermal conductivity of the PCB.

Table 2.8: Simulation results of modules with different submounts.

	Silicon		PCB	
	LED	IC	LED	IC
Temperature (°C)	89	88	144	109

The effect of the TIM property on the module temperature is also investigated. Normally used TIM has a thermal conductivity of 1 ~ 10 W/mK [13]. Some newly developed material is claimed to have higher thermal conductivity over 30 W/mK [16]. For the simulation, the thermal conductivity is tuned between 1 to 30 W/mK, and the resulted maximum temperature of the module is depicted in Figure 2.15. Again, the silicon enabled module shows lower temperature. However, for both cases, the maximum temperature does not show obvious drop with increased thermal conductivity of TIM. This result shows that as long as the TIM layer is thin enough compared with other material layer, it is not the bottleneck on the path of the thermal dissipation. But if too much TIM is applied underneath the LEDs, especially for modules with poorly thermally conductive materials, such as the PCB submount, the situation can be made even worse.

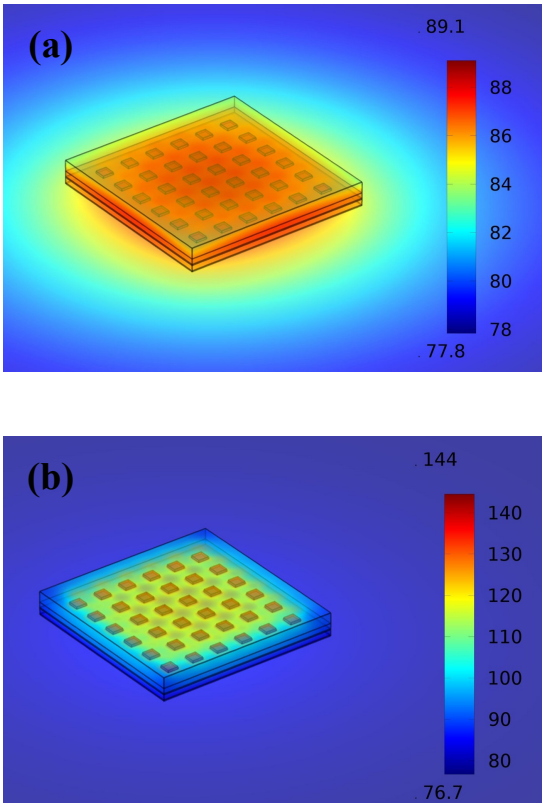

Figure 2.14: Temperature distribution of modules with stacked submounts: (a) silicon submount; (b) PCB submount.

2.2.4. CONCLUSION

Silicon has higher thermal conductivity than most of the materials that are normally used as packaging substrate, such as ceramic, polymer-based laminates (PCB), MCPCB, etc. For SSL modules, silicon substrate can greatly ease the thermal issue due to fast spread of heat through silicon both vertically and laterally and help reduce the temperature of the LEDs whose performance and lifetime are highly linked with the temperature. When ICs are integrated with LEDs on the same silicon substrate, silicon cannot stop the heat transfer between the LEDs and the ICs, and in most cases this is not welcomed. If the thermal impact on the ICs is not acceptable, additional thermal barrier structure can be designed to block the heat from the LEDs.

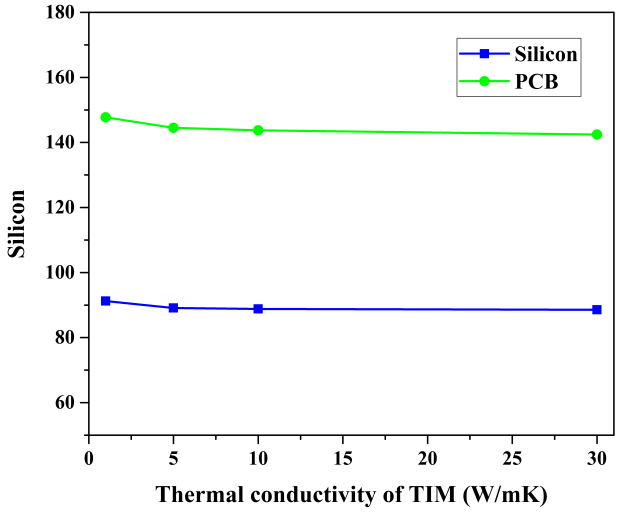

Figure 2.15: The change of LED temperature with different TIMs.

2.3. OPTICAL DESIGN

For SSL applications, optical design plays a significant role in the packaging design. To enhance the efficiency of light extraction from the light source, design of optical components, such as light reflector and lens, must be well taken care of. In most of the SSL modules, package plays a role of bridging the light source (LEDs) and the ambient. A properly designed package can make best of the light emitted from the LEDs and enhance the light efficiency of the whole module. Inside a SSL package, the substrate is usually not considered as an optical part, but it does affect the light effect of the package and the module. It is inevitable that the packaging substrate absorbs part of the light so one of the direction that endeavor has been put into is to increase the reflectivity of the substrate material. This can be achieved by modifying the topology of the substrate surface, or by depositing a layer of highly reflective material. In this section, we focus on the evaluation of silicon submount in terms of the light effect. A multi-LED module is selected as the analysis object. Different submount topologies that are evaluated include:

a. planar surface submount, where all LEDs are mounted on a planar submount,

b. Single cavity reflector, where all LEDs are mounted in one big cavity, and

c. Individual cavity reflector, where each LED is mounted inside one cavity of its own.

The cross-sectional schematics of the three structures with key dimensions are shown in Figure 2.16. In the range of visible light, silicon has a reflectivity of 30 ~ 40 % and the rest is either transmitted or absorbed [17]. To increase the reflection of silicon surface, a thin layer of aluminum is deposited. Among all metals, aluminum has second highest reflectivity, above 95 %, only lower than silver [18].

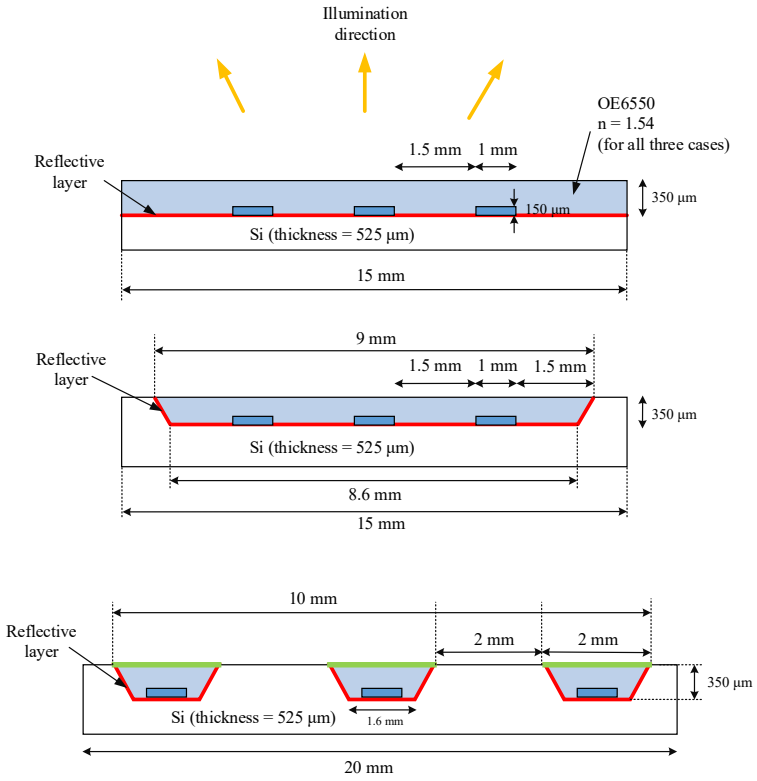

Figure 2.16: Cross-sectional view of SSL module with different topologies (top to down): planar design, single cavity reflector and individual cavity reflector.

TracePro is used to simulate the light effect of each structure [19]. In each model, nine LEDs are simulated as light source and transparent silicone is molded on top as encapsulation. The wavelength of the LEDs is 650 nm and the total radiant flux is 10 mW. The absorption in the silicone is 3 % and light loss of each reflection is 5 % [20]. The representative ray tracing results are shown in Figure 2.17. More illustratively, the distribution of light intensity for each design is drawn in Figure 2.18.

The light emitting angle is defined as two times of the angle in the light intensity

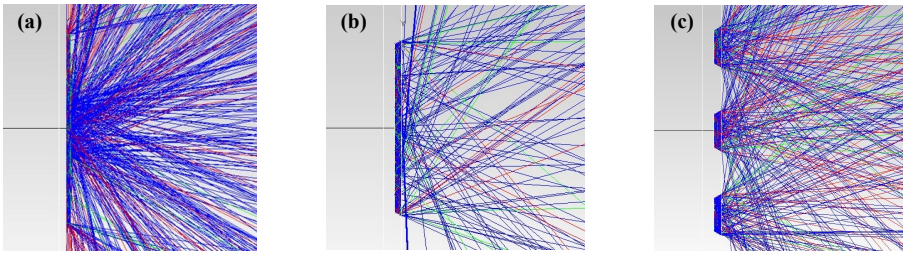

Figure 2.17: Light ray tracing results (side view), (a) planar design, (b) single cavity reflector, and (c) individual cavity reflector.

distribution curve where the light intensity drops to 50 % of the maximum value. From the result shown in Figure2.18, the light emitting angle is 180°, 135°and 110°for the three structures, respectively. The planar design gives the widest light emitting angle and lowest light efficiency. Because there is no light focusing structure, incident light with big angle of incidence has high chance of being reflected back by the flat surface of silicone. After multiple internal reflection, a big portion of light is either lost or escaped from the edge of the module, none of which contributes to the light extraction. For both structures with cavity reflectors, the light emitting angle is greatly narrowed down, namely, focused. Also, the angled sidewall of the cavities helps the light emitting through the surface of silicone and reduces the internal loss of light. When it comes to light emitting efficiency, the ratio of luminous flux to total radiant flux, as listed in Table 2.9, individual cavity reflector design shows the highest efficiency (74 %), more than twice of the one of the planar design.

Table 2.9: Light emitting efficiency and angle for each design.

Design	Light emitting efficiency (%)	Light emitting angle (°)
Planar design	37	180
Single cavity reflector	51	135
Individual cavity reflector	74	110

2.4. FABRICATION PROCESS

The stacked silicon submount process mainly consists of two parts: the fabrication of submount and module assembly. The fabrication process can be basically fulfilled by standard silicon microfabrication process. Among all, some processes are intensively

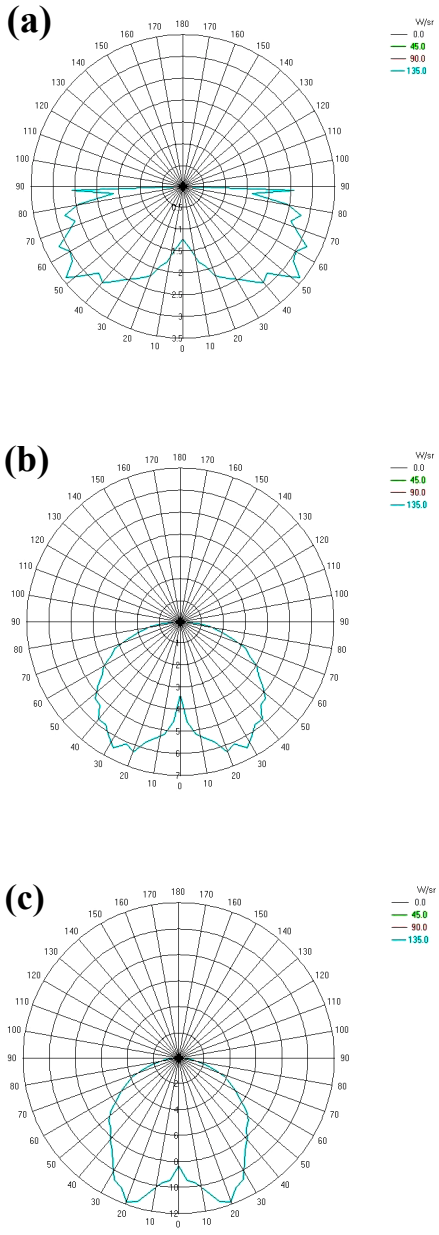

Figure 2.18: Distribution of light intensity: (a) planar design, (b) single cavity reflector, and (c) individual cavity reflector.

used for applications like SSL where multiple heterogeneous chips are integrated based on silicon submount. This section will explain some representative processes which will be implemented into specific application development in later chapters.

2.4.1. METALLIZATION IN CAVITY

As packaging substrates, silicon submounts act as carriers of all the circuitry components, including bare die ICs, discreet passive devices, and even small outline packages. To make best of real estate of the submount surface and increase the packaging density, sometimes part of the components are placed into indented cavities beneath the submount surface. One way to make cavities out of silicon is to use wet etch process. Silicon wafer with an orientation of <100> can be anisotropic etched by KOH solution, forming cavities with angled side walls [21], as shown in Figure 2.19. KOH wet etching process gives many advantages over other approach of cavity forming. The dimension of the cavities is highly controllable and the surface of the cavities shows relatively low roughness. Another feature of KOH-etched cavity is that the angle between the side wall of the bottom of the cavity is very accurate, enabling uniformity among different samples from different batches. The angled sidewall, for instance, can enhance the light extraction, which is of great significance for lighting applications. Moreover, wet etching process is very cost-effective because it does not require complicated equipment and process control and it is batch process with high productivity while consumes only cheap materials.

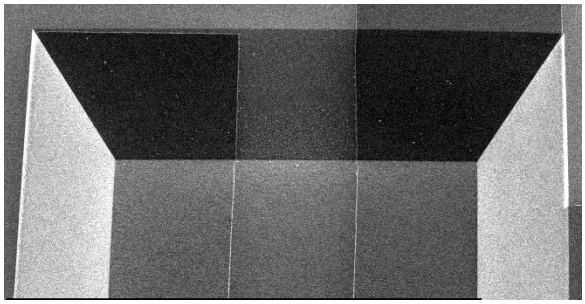

Figure 2.19: SEM image of KOH wet etched cavity in silicon.

One of the challenge of the implementation of wet-etched cavity is the metallization patterning inside the cavities. Most of the cavities that are used to embed chips have depth of over 100 µm, which makes it difficult to pattern materials using normal photo lithography. To overcome such difficulty, first of all, photoresist must be coated on the wafer by spray coating rather than spin coating. Due to the topology of the etched surface, normal spin coating results in insufficient coverage of photoresist inside the cav-

ities. For deep cavities, multi-step spray coating might be needed to achieve sufficient thickness of photoresist. Normal photo lithography can be used for patterning the photoresist with prolonged exposure time. One thing that needs to be taken into account is the minimum trace width or spacing, also known as the feature size, should be at least comparable with the cavity depth, if not bigger. Otherwise, lithography techniques may not be adequate to achieve patterning with good quality. Other technologies, for instance, 3D printing, can be used to fulfill the metallization inside the cavities.

2.4.2. DEDICATED TSV PROCESS

As the silicon submounts are stacked to form a 3D module or system, vertical interconnection between stacked submounts are necessary to fulfill electrical signal transmission. As a hot research topic, through-silicon-via (TSV) technology has been investigated and implemented for a while [22]. Due to the high cost and complexity of the process, TSV technology so far has only been successfully used in high-end and high I/O count applications, such as stacked memories, FPGA, etc. Some emerging applications, like sensors, have as well tried to adopted TSV process, mainly to reduce the form factor of the products for specific applications, such as wearable electronics. For these applications, the density of the TSVs is usually low and the size of the TSVs can be tens of micrometers or even bigger. To better serve the vertical interconnections of such applications, in this section, modified TSV forming process is presented.

The proposed vertical interconnections are realized by a two-step process: etching-based via forming and the filling of conductive material, as shown in Figure 2.20. To minimize the cost of process, the silicon etching part can be mostly or fully realized by wet etching process which presents high controllability and uniformity as well as low cost. Dry etching process may also be supplemented only if necessary. The filling of conductive material into the via avoids the metal plating process in standard TSV process, which gives most of the issues on cost reduction as well as reliability [22]. The proposed two-step process of TSV displays high flexibility for applications like SSL and will be further demonstrated in a specific application in Chapter 3.

2.4.3. EMBEDDED PASSIVE DEVICE

Passive devices, including resistors, capacitors, diodes, etc., consists more than 50 % of the real estate on PCB for most application circuits. Most of the passive devices used in consumer electronics are surface mount type, enabling the integration of them into a compact system-in-package. The state-of-the-art of embedded passive technology includes embedded device into packaging substrates or PCBs, either rigid or flexible ones

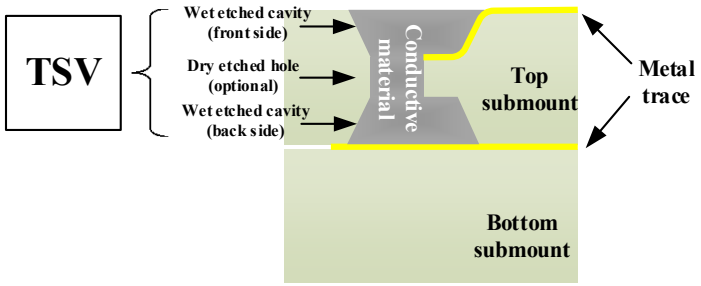

Figure 2.20: Cross sectional schematic of modified TSV: etching-based via forming and filling of conductive material.

[23]. Compared with discrete passives, embedded or integrated passive devices show increased electrical performance and reliability, reduced size and cost [24].

In our proposed approach, the integration of passive devices is realized through assembly based process. After the silicon submount is prepared, the cavity for hosting the passive devices is finished with metal electrodes. Conductive material needs to be dispensed on the electrodes. At least two kinds of materials can be selected, solder paste and conductive adhesives. For solderable electrodes, such as copper, nickel or gold, solder paste is the best interconnection material. Reflow process can be used to melt the solder and then cool down to form solid solder joints. However, aluminum, which is widely used for traces and electrodes, requires special solder paste to realize the soldering process simply because aluminum is easily oxidized. Also to form reliable intermetallic compound between aluminum and solder metal, higher soldering temperature is required, which for some applications, is unfavorable. Conductive adhesives can be an alternative of solder. Silver based conductive glue has been widely used to form electrical interconnections between IC bare dies and electrodes. These glues contain polymeric solvents which require a curing process at certain temperature. Figure 2.21 shows schematics of typical passive devices embedded into silicon submount.

2.5. SUMMARY

The above discussed design methods and optimization results aim to assist the design of SSL application, but can be implemented into related applications such as smart sensor

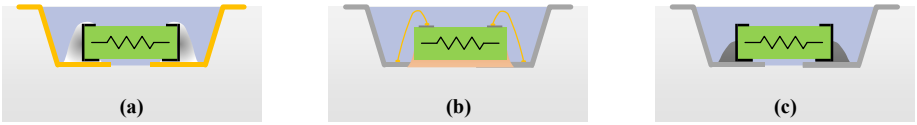

Figure 2.21: Cross sectional schematic of embedded passive device structure: (a) solderable pads with SMT device; (b) non-solderable pads with wire-bondable device; and (c) non-solderable pads with SMT device.

and MEMS device packaging. In the following chapters, specific application design will be discussed in details using the design rules demonstrated in this chapter as guidance.

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3

3D SiP Enabled Smart SSL Module

With the coming of intelligence era, integrated smart electronic systems have been in urgent need. To achieve packages with small form factor, 3D integration and WLP technology have been continuously investigated. Focusing on the applications such as MEMS and sensor systems, a dedicated 3D wafer level SiP design is developed and presented in this chapter. The proposed SiP design is based on stacked silicon submounts. As packaging submounts, silicon is proved beneficial for SSL applications in terms of thermal management. The design of the SiP is presented from several aspects including function, circuit, thermal, optical and interconnections. The fabrication and packaging process is explained in detail in this chapter. The developed SiP module shows good performance according to the testing results. The proposed 3D SiP is proved suitable for SSL applications.

Parts of this chapter have been published in Microelectronics International **32**, 2 (2015) [1] and *Electronic Components and Technology Conference (ECTC)*, 2014 IEEE 64th (pp. 1192-1197). IEEE[2].

3.1. Introduction

With the increasing demand for miniaturization of portable electronics, higher function integration level and lower cost are major challenges in the semiconductor industry. SiP technology is one of the fastest emerging technologies offering highly flexible and low-cost integration and packaging solutions [3, 4]. As the era of intelligence comes, smart electronics have penetrated into many aspects of our daily life, from ambient intelligence to wearable electronics on human bodies [5–7]. These smart electronic systems consist of not only multiple ICs but also passives, sensors, actuators, etc., all of which can be integrated into a single compact package by means of SiP technology. The SiP technology has already been implemented in various applications, including portable electronics, wireless products [8], sensor systems [9] and smart lighting systems [10]. To further increase the integration level, 3D SiP-based integration has become a widely investigated topic. 3D integration provides opportunity for miniaturization, high bandwidth, low power and high performance [11–14].

The design of 3D SiP involves multiple elements, including packaging substrate, interconnections, components and so on. Among all, the packaging substrate is the core element that links all other elements within SiPs. The substrate does not only act as electrical interconnection between the chips, but also provides mechanical protection, thermal dissipation as well as optical functionality for lighting applications [15]. Therefore, the selection of substrate material is of great significance for 3D SiP design. Polymer laminates are widely used in consumer electronics due to the low cost. However, the implementation of polymer-based substrates into 3D integration and SiP has been obstructed by the material drawbacks such as mismatched CTE with the chips, insufficient thermal conductivity and difficult manufacturing of high density interconnection. From this perspective, silicon makes a well-suited candidate for packaging substrates. Moreover, silicon-based packaging process is inherently compatible with IC/MEMS processes, helping open up new opportunities for 3D heterogeneous integration. The silicon-based 3D integration, represented by silicon interposer, has attracted research interest recently [16–19]. Most of the technologies have been developed for 3D IC integration accommodating high density TSVs. Unlike IC integration, most MEMS systems and sensor applications do not require high density of interconnections, meaning more dedicated and cost-effective solution needs to be developed.

In this chapter, a 3D SiP design is developed based on stacked silicon submounts for a smart SSL application. More detailed design and fabrication process will be explained. Also, testing and characterization results will be discussed. This chapter is outlined as follows. The proposed packaging concept and design will be explained in Section 3.2

and the packaging process will be presented in Section 3.3. In Section 3.4, testing and characterization will be discussed and the results will be analysed. At last, main conclusions and outlooks towards future work is given in Section 3.5.

3.2. CONCEPT AND DESIGN

THE proposed SiP design is developed for applications such as smart SSL modules and inherently, the design rule discussed in this section can be implemented into a wider range of applications.

3.2.1. MODULE DESCRIPTION

The functionality of proposed module is adopted from a commercialized LED lamp. In the lamp, the functional system is realized by board level assembly using PCB as the mother board. The light source contains two independent chains each of which emits warm white (3000 K) and cold white (6500 K) light, respectively. The brightness of each chain can be adjusted with an infrared-based remote controller synchronously or independently so that the whole module can provide light with variable color temperatures as well as different brightness. The controlling is done by an infrared controller. The aim of this chapter is to miniaturize the system by 3D SiP approach. The realized SiP module should possess very compact form factor and flexibility for integration into a wide range of applications including different forms of lighting products at different application scenarios.

The proposed 3D SiP is based on stacked silicon submounts, as shown in Figure 3.1. The module is a double-layer structure using silicon as submount for each layer. The dimension of the module is 17 mm × 17 mm and the thickness is less than 2 mm. The top submount carries all the LEDs encapsulated with phosphor. The driver and control circuitry is embedded into the bottom submount and encapsulated with glob-top. The vertical interconnection between the two submounts is realized by modified TSV as described in Chapter 2. The two layers are bonded using TIM. The interconnections between the two layers also play as I/Os to external circuitry. To enhance the light extraction, the individual cavity reflectors are formed on the top submount and coated with aluminum.

3.2.2. CIRCUIT DESIGN

Figure 3.2 shows the circuit of the module. Two LED chains are designed with different color temperatures as described in Section 3.2.1. Linear drivers are used to limit the

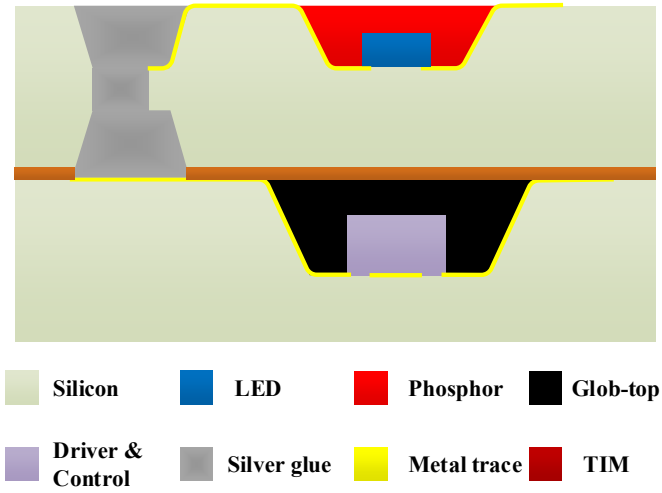

Figure 3.1: Cross-sectional diagram of the 3D SiP module (not to scale): the LEDs are embedded in reflector cavity on the top submount, while the driver and control is embedded into the bottom submount; the two submounts are bonded with TIM and electrically connected by modified TSVs.

currents passing each LED chain. Pulse width modulation (PWM) is used to switch on / off the LEDs and thus adjust the brightness. A micro control unit (MCU) receives commands from an infrared receiver and sends the PWM signal to the switches on the driver paths. As mentioned in Section 3.2.1, this circuit is used in a commercialized lamp and adopted in this chapter to demonstrate the development of 3D SiP design. No optimization towards the electrical characteristics of the circuit is conducted because it is beyond the scope of this thesis.

To ease the complexity of the module design, the power supply part (shadow highlighted in Figure 3.2) in the circuit is not integrated in the module due to the bulkiness of the components. Only bare dies are used in the design together with the surface mount type passive devices (SMDs).

3.2.3. Submount Design

Silicon submount is the key element in proposed SiP design. It links all the aspects of the whole design, including circuit, thermal, optical and interconnections design.

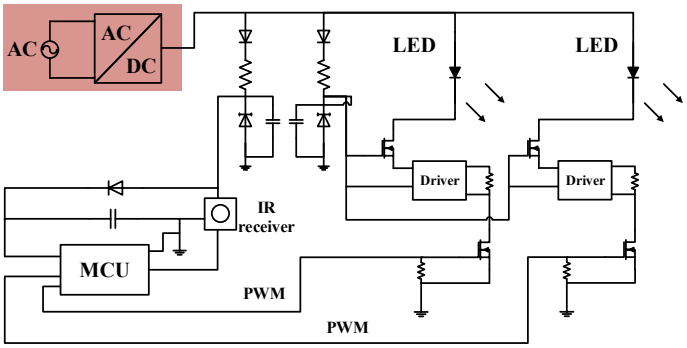

Figure 3.2: Schematic of the smart LED module adopted from a commercialized lamp. The power supply (highlighted) is kept out of the 3D SiP.

ELECTRICAL DESIGN

Due to the semiconductor property of silicon, the insulation between substrate and the circuit must be properly designed to prevent dielectric breakdown at high voltages. For instance, the voltage on the substrate can go up to 250 V for lighting applications. In our design, silicon oxide (SiO_2) is used as insulator. The breakdown electric field strength of SiO_2 is about 5 ~ 10 MV/cm. A SiO_2 layer with the thickness of 1 μm should withstand voltages as high as 500 V. In case of the defect from the growth of SiO_2 layer, such as pin holes, the thickness of SiO_2 layer in our design is always set thicker, 3 μm for example, to be safe.

For the circuit trace and pad material, two kinds of metals that are widely used in IC industry, aluminum (Al) and copper (Cu), are studied. The metal affects the strength of the interconnection between the chips and the submount. Al provides higher strength for wire bonding interconnections than Cu according to our test which will be explained in details in the following paragraphs. For bare dies, wire bonding is the mainstream method for die level interconnection and Al pads are expected to show higher reliability than Cu. However, for surface mount type components, such as most of the passive devices, reflow soldering is used for connecting them to the submount. Soldering on Al is much more difficult than that on Cu, requiring special solder material and higher process temperature. Instead, conductive adhesive has to be used to form the interconnections, such as silver glue, even if it shows lower conductivity and reliability compared to solder. Another concern of the trace design is the electromigration due to high current density in the metal. The typical current density at which electromigration occurs in Al or Cu traces is 10^6 to 10^7 A/cm^2 [20]. According to this value, a metal trace with

width of 100 µm and thickness of 2 µm can withstand at least 2 A current without obvious degradation. In our design, a metal layer with the thickness of 2 µm is deposited on the insulation layer. The minimum width of circuit trace is 100 µm. Since each metal shows pros and cons, we try both of them in our design.

For smart control circuitry, signal with frequency of up to kHzs usually exists. The PWM control signal in our module has a frequency of 1 kHz. This frequency is set by the pre-programmed MCU provided by the supplier. And since the linear driver is used to control the LEDs, as long as the frequency of PWM signal is above 200 Hz which causes flickering, it meets the requirement of the LED application. In the layout design, the PWM control signal traces are kept wide and short and apart from each other, as indicated in Figure 3.3.

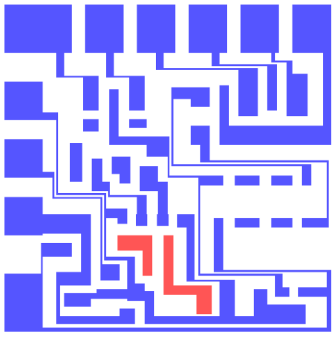

Figure 3.3: Trace layout of the driver and control circuitry (red highlighted part: PWM control signal with frequency of 1 kHz).

Thermal design

The thermal performance of stacked submount structure has been analysed in Chapter 2. Silicon helps reduce the module temperature due to fast heat conduction through it. For a silicon-based stack, the TIM layers between the submounts and and the heat sink do not limit the heat dissipation as long as their thickness is small. The analysis in Chapter 2 is implemented into the design in this chapter. Moreover, the analytical result will be validated by the experimental testing in Section 3.4 of this chapter.

Optical design

As discussed in Chapter 2, reflector cavity in the silicon submount and the coating of reflective aluminum layer enhance the light effect. In our module, individual reflector cavity is adopted on the top silicon submount. To be compared with, a modified planar

design is also used in our design. As shown in Figure 3.4, the one on the right is the individual cavity structure. Each cavity hosts one LED as well as the phosphor. Neighbouring LEDs are encapsulated with phosphor of different color temperatures. The structure on the left, on the other hand, has a planar surface of the submount; but two dam rings of reflective glue are formed around the LEDs, acting as reflective sidewall and reservoir for phosphor. The LEDs within the smaller dam ring consist one chain with the same phosphor, while the LEDs between the two dam rings belong to the other chain with different color temperature. By adding the reflective dam ring, the light effect is expected to improve compared with the original planar design described in Chapter 2. The details of the cavity fabrication and phosphor dispensing will be explained in Section 3.3.3.

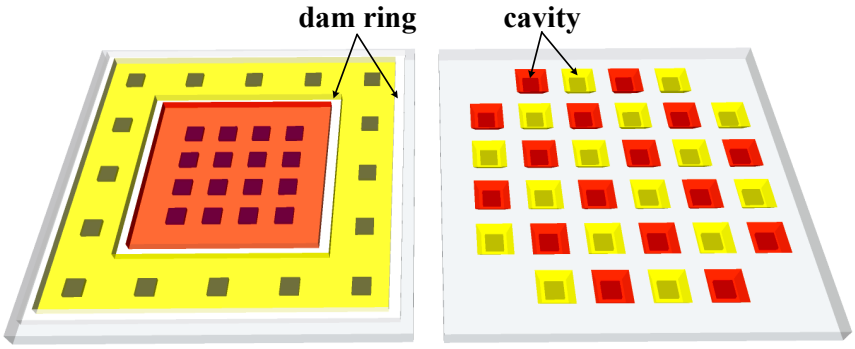

Figure 3.4: Structures of the top submount: modified planar design (left) and individual reflector cavity for each LED (right).

INTERCONNECTION DESIGN

To realize proposed SiP modules, the interconnection process development and optimization in multiple levels are carried out: component to submount, submount stacking and module to external I/Os.

As discussed previously, two kinds of metals, Al and Cu, are used to make circuit traces (pads). For Cu, an additional thin layer (100 nm) of gold (Au) is deposited on top to prevent Cu oxidation. All the bare dies in the module need wire bond connection to the submount. Au wire (0.8 mil diameter) is bonded on both Al pads and Cu/Au pads using the same process parameters. Pull test is conducted to compare the bonding strength of Al and Cu/Au pads. The result is shown in Figure 3.5, revealing that Al pads provide stronger connection with Au wire than Cu/Au pads.

For the passive SMDs, reflowed lead-free solder paste is used to connect to the Cu (Au) pads while conductive silver glue is used for Al pads because soldering on Al requires

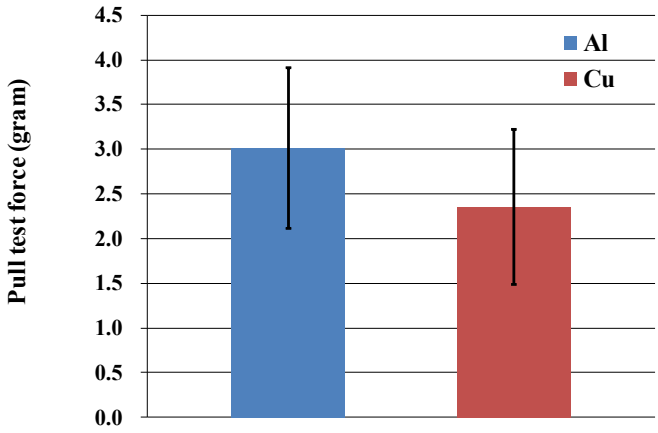

Figure 3.5: Result of pull test for evaluation of wire bonding strength: Al pads show stronger connection than Cu/Au pads.

special solder and much higher soldering temperature. Compared with reflowed solder, silver glue gives slightly higher resistance (around 0.1 ohm per connection joint). To achieve lowest resistance, soldering on Cu-based metallization is suggested.

Cavities are designed on the bottom submount to embed the components. Moreover, additional cavities can also be fabricated on the back side of the top submount in case that some components on the bottom submount extrude the cavity due to higher thickness. All these cavity designs aim to minimize the total thickness of the stacked module.

The interconnection between the two submounts is formed by conductive silver glue filled TSVs as we already explained in Chapter 2. Here we show the structure again in Figure 3.6 for easy reading. The TSVs are fabricated in the top submount at the corresponding locations to the pads that need to be connected. The TSV fabrication process will be explained in Section 3.3.3. Conductive silver glue fills the TSVs, connecting the metal pads on top and bottom submounts. Meanwhile, the upper surfaces of the filled TSVs can be used to connect with external I/Os.

3.3. Fabrication and Assembly

In this section, the fabrication and assembly process of silicon submounts is discussed in details. The presented SiP is realized by silicon-based microfabrication and packaging process. To realize the proposed SiP module, process optimization has been carried out

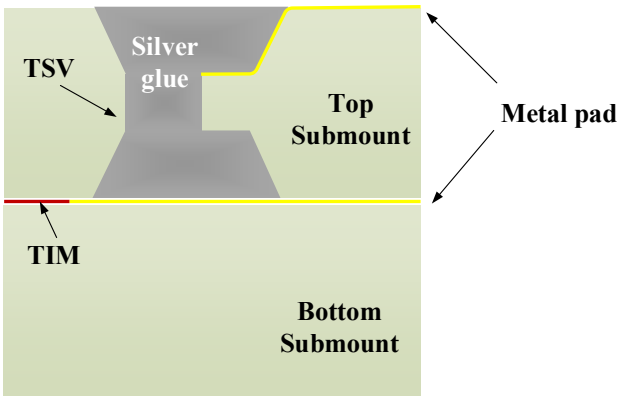

Figure 3.6: Modified TSV design for interconnection between submounts: same design as described in Chapter 2 and shown here for easy reading.

for each step.

3.3.1. TOP SUBMOUNT

The top submounts are fabricated on 800 µm-thick 4 inch double-side polished p-type, <100> orientation, silicon wafers. The process begins by depositing 400 nm of silicon nitride on both sides of the wafer by low pressure chemical vapour deposition (LPCVD) at 850 °C. This layer is then patterned with contact lithography using spin-coated positive photoresist and etched in fluorine plasma etcher to form a hard mask for wet Si etching. Afterwards the resist is removed by oxygen plasma ashing (Figure 3.7(a)). Cavities are etched in the bulk Si using 33% KOH solution at 85 °C to the depth of 250 µm (Figure 3.7(b)). The size of the cavities ranges from 1.6 mm to 3.4 mm. The approximate etch rate (ER) is determined from the laboratory logbook. After etching for 2 hours a more accurate ER is determined by measuring the cavity depth with stylus profiler. The calculated ER is 1.47 µm/min and total etching time is 2 h 50 min. The nitride masking layer is then removed in boiling (157 °C) phosphoric acid. Afterwards a SiO_2 masking layer of 4 µm is coated by plasma enhanced chemical vapor deposition (PECVD) (Figure 3.7(c)). The oxide layer is then patterned using dry etching at the TSV opening locations inside the cavity. DRIE process is carried out for the formation of TSVs, followed by removing the oxide masking layer (Figure 3.7(d)-(e)). Adixen AMS100 system is used for DRIE, Bosch process with alternating etching and passivation steps. The etching/passivation step durations are 7/3 s using SF_6 and C_4F_8 gasses respectively. The gas flow rates are 700

sccm for SF_6 and 250 sccm for C_4F_8. Source power is set to 2000 W and platen temperature -10 °C. These etching conditions result in approximate ER of 5 µm/min. Afterwards the wafer surface is again covered with a SiO_2 layer, using wet thermal oxidation. The thickness of this layer is 3 µm to prevent dielectric breakdown at high voltages (Figure 3.7(f)). Al is then sputtered by physical vapour deposition (PVD) for the interconnections between the ICs as well as reflective layer on the front side of the submounts with layer thickness of 2 µm (Figure 3.7(g)). Because the submounts contain many etched cavities, spray-coated positive photoresist, with the nominal thickness of 9 µm on the top surface, has to be used for metal patterning. The thickness of the resist layer at the top and bottom edges of the cavities is investigated using SEM imaging. Top edge measured thickness is approximately 2.2 µm, which is sufficient for wet or plasma etching of Al. Resist buildup at the bottom corner is approximately 16 µm which is patterned by using prolonged exposure and development times. The Al layer is wet etched using commercially available etchant PES (mixture of phosphoric (H_3PO_4), acetic (AcOH) and nitric (HNO_3) acids, with ratios of 77:19:4 respectively) and the submounts are finalized by removing the photoresist with O_2 plasma (Figure 3.7(h)). It should be pointed out that some of the bare dies assembled on the bottom submount have larger thickness so they will extrude from the cavities and form uneven surface of the bottom submount. The backside cavities on the top submount are used to cover those higher dies when the submount bonding is conducted so that the total thickness of the submount stack is kept as low as possible. The submount assembly process will be discussed in detail in Section 3.3.3.

3.3.2. Bottom Submount

The bottom submounts are fabricated with similar process. The wafers used are single-side polished, <100>, with the thickness of 525 µm. The KOH cavities are etched only on the front side to the depth of 400 µm using the same recipe (Figure 3.8(a)-(b)). A SiO_2 isolation layer of 3 µm thickness is thermally grown after the nitride masking layer is removed (Figure 3.8(c)).

Metal layers are then sputtered by PVD. Two different metals are used for the fabrication, namely Al and Cu with same layer thickness of 2 µm. The processing steps for both metals will be discussed separately. Al is deposited directly on thermal SiO_2, as shown in Figure 3.9(a). As for the top submount fabrication process, spray-coated positive photoresist is used for metal patterning. After developing, it is observed that some of the structures, covered by the mask, are ruined due to light reflection from the metalized sidewalls of cavities during exposure (Figure 3.10(a)). This phenomenon is not observed

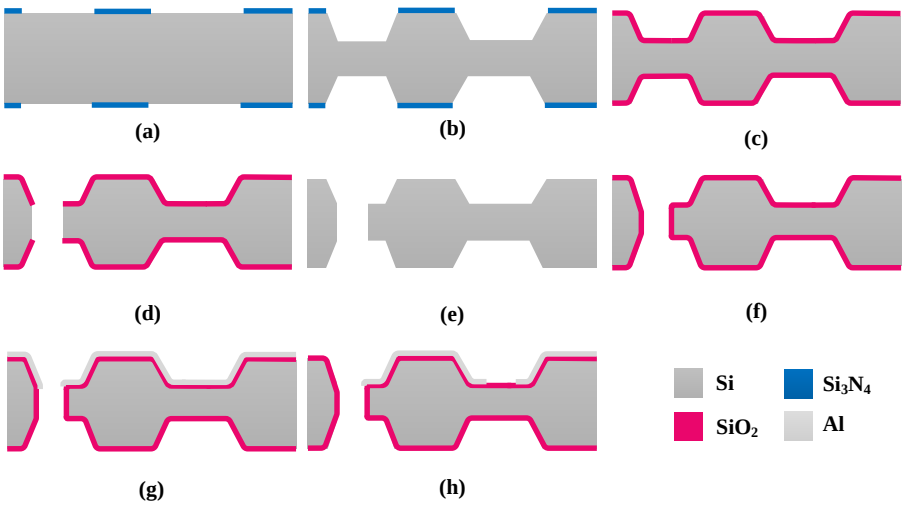

Figure 3.7: Fabrication process flowchart of top silicon submounts: (a) silicon nitride masking layer deposition and patterning; (b) cavity etching by KOH; (c) silicon nitride removal and silicon dioxide deposition; (d) TSV etching; (e)(f) silicon dioxide removal and re-deposition; (g)(h) aluminum deposition and patterning.

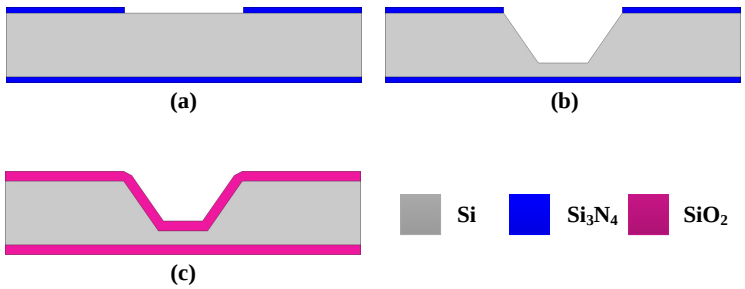

Figure 3.8: Cavity formation process of bottom silicon submounts: (a) silicon nitride deposition and patterning; (b) cavity etching by KOH; (c) silicon nitride removal and silicon dioxide growth.

in the fabrication of top submounts because the cavities are not so deep as the ones of the bottom submounts. An anti-reflective coating consisting of 50 nm TiN and 15 nm of PECVD SiO_2 is deposited to solve the resist damage issue (Figure 3.9(b)). TiN is well-known to absorb light emitted by mercury lamps, used in contact aligners with i, h, g spectral lines [21], while the thin oxide layer is used to improve photoresist adhesion to the substrate. A SEM image of patterned photoresist without reflection induced damage is shown in Figure 3.10(b). After resist patterning the thin oxide layer is etched with a

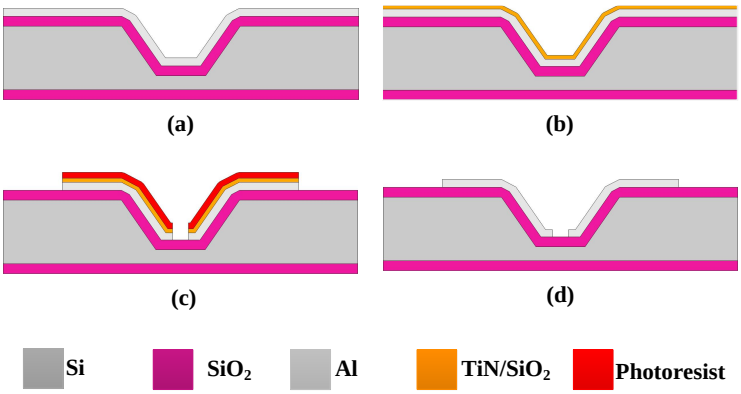

Figure 3.9: Metallization process of bottom submount with Al: (a) Al deposition; (b) anti-reflective coating; (c) Al patterning; (d) masking layers removal.

short dip in buffered hydrofluoric acid (BHF). TiN/Al stack is patterned using an inductive coupled plasma- reactive ion etching (ICP-RIE) etcher using Cl based plasma with end point detection (Figure 3.9(c)). Photoresist mask is then stripped with O_2 plasma. The Al based submounts are finalized by removing the anti-reflective layer from the interconnect surface by another short BHF dip followed by short RIE etch step for etching of SiO_2 and TiN, respectively (Figure 3.9(d)). It is not necessary to protect the thermal oxide (bottom and backside of wafer) during BHF dip steps because only approximately 15 nm would be etched which is insignificant considering the initial thickness of 3 µm.

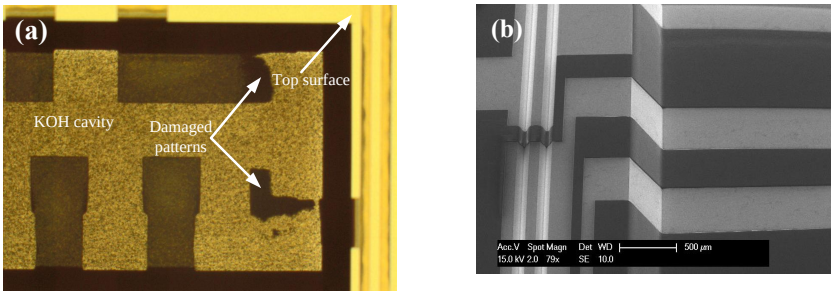

Figure 3.10: (a) Damaged photoresist patterns due to reflection from sidewalls; (b) SEM image of patterned photoresist, using anti-reflective coating.

Ti/TiN (10/40nm) barrier/adhesion layer is sputtered prior to Cu PVD (Figure 3.11(a)). The above mentioned anti-reflective coating (TiN/SiO_2) is also used for patterning Cu.

After spray coating and patterning, the photoresist is additionally hard-baked in an oven at 150 °C for 30 min, to improve adhesion to the substrate. Cu is patterned using entirely wet chemical processes. As with Al process, the patterning starts with BHF dip to remove the thin SiO_2 resist adhesion layer. Afterwards TiN anti-reflective layer is etched in ammonia, hydrogen peroxide and deionization (DI) water solution with the ratio of 1:4:4. It is not possible to use plasma etching for TiN removal due to possible Cu contamination of the etching tool.

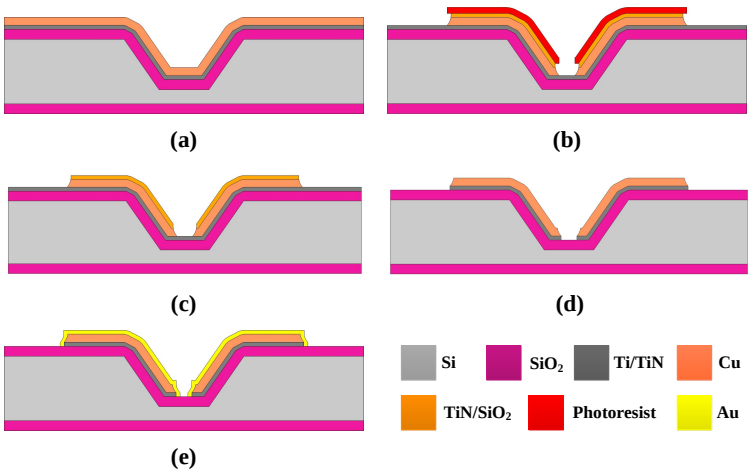

Figure 3.11: Metallization process of bottom submount with Cu: (a) barrier/adhesion layer deposition prior to Cu; (b) Cu patterning; (c) photoresist remoal; (d) SiO_2 and Ti/TiN removal; (e) electroless Au plating.

Bulk Cu layer is etched using sodium persulfate and DI water with a very small amount of sulfuric acid (Figure 3.11(b)). The photoresist is then removed with NMP (N-methyl-2-pyrrolidone) at 70 °C (Figure 3.11(c)). Then BHF and TiN etching solutions are used again to remove the thin SiO_2 and the TiN on top of Cu and the Ti/TiN layers under the Cu (Figure 3.11(d)). To prevent oxidation of Cu, the interconnections are finalized with electroless Au plating of 100 nm (Figure 3.11(e)). During electroless plating process Au conformally adheres only to Cu surfaces, so no additional lithography steps are necessary.

3.3.3. ASSEMBLY

The top submount only carries LED dies. The assembly of LEDs is done by standard die bonding and wire bonding process. Epoxy-based thermal conductive glue is predispensed onto the pads of the submount. The LEDs are then picked and placed onto

the pads using commercially available die bonder. The assembly is baked at 150 °C for 2 hours to cure the die-attach glue. Afterwards, wire bonding is conducted. The LED dies used in the module are blue LEDs with two electrodes on the top surface. Au wire of 0.8 mil diameter is used for bonding the LEDs to the submount. Both the die bond and wire bond process is achieved at wafer level. Then the wafer is diced into dies.

To get white light, yellow and red phosphor are used to convert the blue light. In the module, yellow phosphor is used to get cold white light (6500 K), while mixture of yellow and red phosphor is used for warm white light (3000 K). The phosphor powder is dispersed into silicone before being applied on the LEDs. For the submount with cavities, the phosphor is directly dispensed on top of LEDs. For the modified planar design, the dam rings are dispensed to form reservoirs prior to phosphor dispensing, as indicated in Figure 3.12(a). The dam material is single-component epoxy-based polymer with curing condition of 100 °C for 30 min. After the phosphor dispensing, the assembly is baked at 150 °C for 2 hours to cure the phosphor. The assembled top submount is singulated and each of the two designs are shown in Figure 3.12(b).

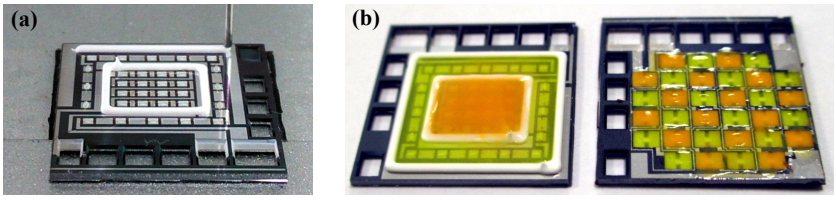

Figure 3.12: (a) dam ring formation process; (b) assembled top modules: modified planar design (left) and individual cavity design (right).

The driver and control circuit components were assembled on the bottom submounts, including both the SMD passives and bare die ICs. For the submount with Al trace (pads), all the interconnections were formed by silver glue. The silver glue was first dispensed on the pads and then the components were picked-and-placed on top, followed by glue curing process. For the submount with Cu trace (pads), first the SMDs were attached to the pads using pre-dispensed solder paste. Then the submount was heated to 200 °C for 10 seconds to melt the solder paste. Then the bare die ICs were attached to the submount using the same process as used for the Al submount. For both type of submount assembly, wire bonding was carried out on all bare dies, followed by glob-top encapsulation to protect the bond wires, as shown in Figure 3.13.

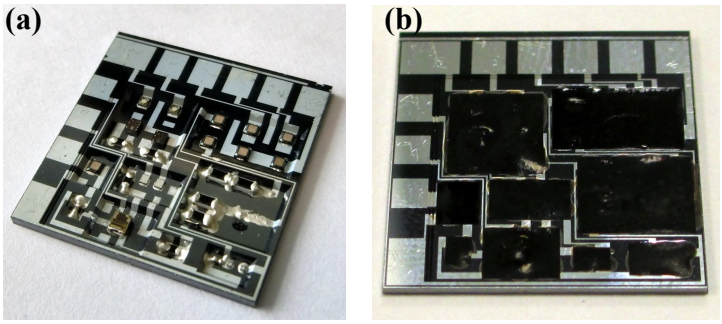

Figure 3.13: Assembled bottom submount with aluminum traces and pads: (a) before encapsulation; (b) after encapsulation.

3.3.4. MODULE INTEGRATION

The stacking of submounts consists of two parts: mechanical bonding and electrical connection. The two submounts are bonded using two-component thermal grease with the thermal conductivity of 30 W/mK. The thermal grease is dispensed on top of bottom submount first. Then the top submount is aligned with and pressed onto the bottom one. The thickness of the thermal grease layer should be maintained small to reduce thermal resistance. The submount stack is baked at 80 °C for 2 hours to strengthen the thermal grease. Silver glue is then filled into the TSVs using a syringe, connecting the corresponding pads from the top to the bottom submount. To connect the module to external circuit, wires are also connected out from silver glue-filled TSVs (Figure 3.14). The stacking process is conducted at chip level.

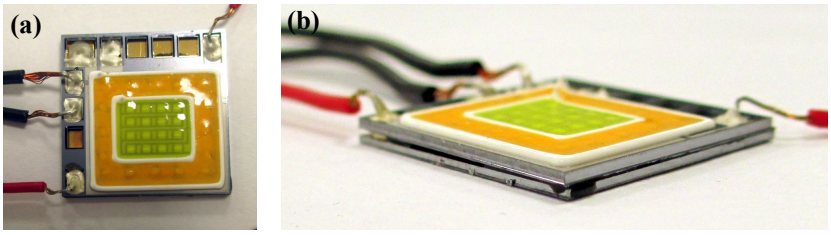

Figure 3.14: Fully assembled module with external I/O connections: (a) top view; (b) side view.

3.4. Testing and Characterization

To evaluate the design, multiple tests are conducted on the modules, including function validation, thermal test and optical test. Detailed results will be discussed as follows.

3.4.1. Function validation

According to the design, the current passing the LEDs is limited by the driver to be under 65 mA. Increasing DC voltage is applied to the module while the total current (two chains) is monitored. As shown in Figure 3.15, the total current is stabilized at 138 mA after the input voltage reached 53 VDC, showing correct electrical characteristics.

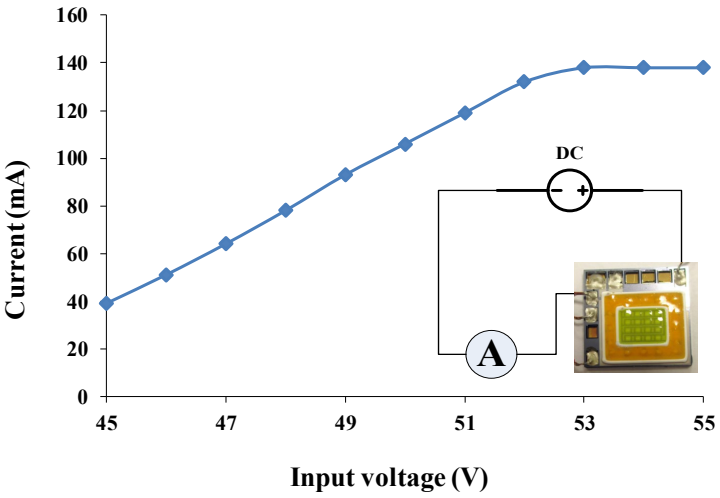

Figure 3.15: I-V curve of the SiP module and the testing setup schematic (inset).

The stacked module is assembled with external protection PCB for testing, as shown in Figure 3.16. Controlled by an infrared remote controller, the brightness of each LED chain can be adjusted independently. Since the two LED chains emit light with different color temperature, both the brightness and color temperature of the bulb is tunable. The controller can also switch on / off the bulb from distance.

3.4.2. Thermal test

The temperature of the assembled module is firstly measured. The module is adhered on a metal heat sink by TIM, as shown in Figure 3.17. The input voltage is 50 VDC and the

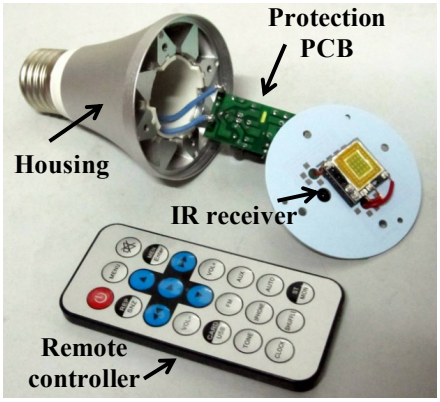

Figure 3.16: Assembled bulb with the SiP module and infrared remote controller.

input power is 6 W. The temperature is measured at room temperature of 25 °C by a thermal infrared imager. The highest temperature of 80.8 °C appears on the LED locations but the temperature of the LEDs should be slightly higher than the surface temperature. In Chapter 2, a similar situation has been simulated and the temperature of the LEDs is 89 °C , a little higher than the measurement result. When the module is assembled with better designed heat sink, like most of the bulbs, the temperature is expected to be lower.

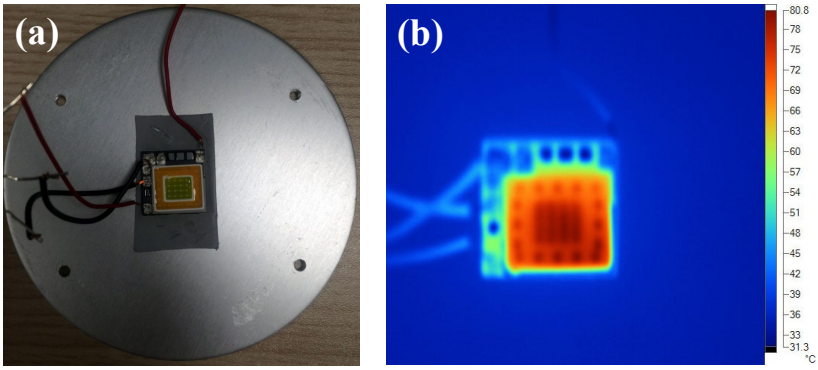

Figure 3.17: Infrared image of the working module: the highest temperature is 80.8 °C .

The temperature of the working bulbs (without the cap) are also measured by the infrared imager. Figure 3.18 shows the temperature distribution. The hotspots display the highest temperature of 52 ~ 54 °C (on the surface). From the simulation results of

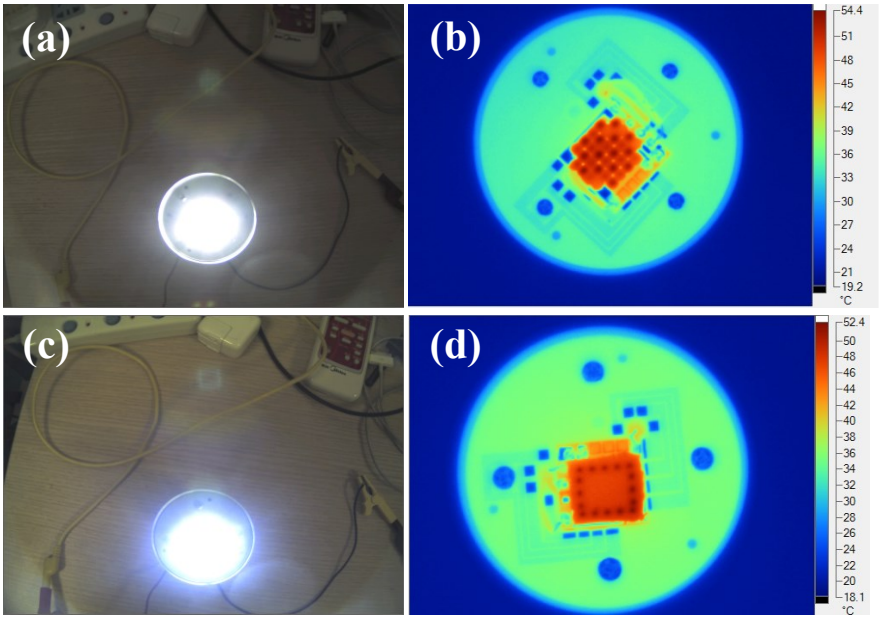

Figure 3.18: Temperature distribution of the SiP module inside working bulbs without the cap: individual cavity design ((a) and (b)); modified planar design ((c) and (d)).

Chapter 2,the temperature of the LEDs is higher than the module surface by about 3 ~ 4 °C. Then the temperature of the LEDs inside the working bulbs is estimated as 55 ~ 58 °C. Given the environmental temperature of 20 °C and the input power of 6 W, the total thermal resistance from the LEDs to ambient is as 6 K/W. For lighting bulbs, this thermal resistance is very reasonable. In terms of thermal management, the two designs of the top submount, planar or cavity, show comparable performance.

3.4.3. Optical test

The light output measurement is carried out on unstacked top submounts and stacked module, respectively, by integrating sphere. To test the top submount, a 48 VDC is directly applied on the module without connecting the driver. The total current throughout the module and the light output are measured. For the stacked module, the same voltage of 53 VDC is applied as used in the function validation in Section 3.4.1. The measurement results are listed in Table 3.1. The low and high color temperatures are supposed to be 3000 K and 6500 K, respectively. From the measurement results, devi-

ation exists and may be caused by the phosphor preparation process. To get accurate color temperature, the composition of the phosphor needs to be accurately controlled and the dispensing needs to be conducted carefully to get conformal phosphor coating. However, the tuning of color temperature of the phosphor is beyond the scope of this thesis. The stacked module shows less light output than single top submount because the effective power allocated on the LEDs is lower due to power consumption of the driver and control circuit. It should be noted that the modified planar design of the top submount shows comparable light output with the cavity design. It proves that the dam rings play similar roles as a single cavity reflector as discussed in Chapter 2. Though we do not evaluate the uniformity of the light emitting from the module, it is obvious that the cavity design should provide more conformal light because LEDs with different types of phosphor are alternately placed on the submount and light with different color temperature is mixed better.

Table 3.1: Optical test results of unstacked submounts and stacked module

Sample	Planar TS[a]			Cavity TS			Stacked module with cavity TS
	Low CT[b]	High CT	Mixed	Low CT	High CT	Mixed	Mixed
Input voltage (V)	48	48	48	48	48	48	53
Input current (mA)	65	71	140	71	63	140	138
Light output (lm)	147	249	393	191	211	399	329
CT (K)	2526	6590	4683	2863	7021	4309	3803

[a] top submount
[b] color temperature

3.5. CONCLUSIONS AND OUTLOOKS

A novel 3D SiP based on stacked silicon submount technology is successfully developed and demonstrated by a smart SSL module application. The stacked module consists of multiple layers of silicon submounts which can be designed and fabricated in parallel and thus increase the production efficiency and lower the cost. The fabrication and assembly process is compatible with standard MEMS process and can be realized by available clean room equipments. 3D stacking design offers higher level of integration

and miniaturized form factor of package and module. The fabrication, assembly as well testing can all be conducted at wafer level, thus reducing the cost and improving the yield. Instead of implementing Cu-filled TSV technology, the presented design adopts a cost-effective way of interconnection, making it suitable for applications such as smart sensors or wearable electronics.

One of the common concerns of wafer level packaging is the wafer warpage, which tends to introduce cracking or delamination during back-end processing or dicing. To transfer the presented process to larger size substrates, such as 6-inch or even 8-inch wafers, processing parameters must be carefully designed and controlled to ensure the minimum warpage. In the presented process, silver glue filled TSV is implemented. Considering the CTE mismatch between silver and silicon, the TSV interconnections would encounter reliability issue in the long term field use. The lower density of TSV in our design makes this issue less severe; nevertheless, further investigation needs to be conducted. To further increase the integration density of SiP, research efforts need to be put into two directions. One is the double-side processing of silicon submounts which can help reduce the package size as well as further shorten the vertical interconnection that leads to improved system performance. The other direction could be to integrate more heterogeneous devices, such as MEMS sensors, into SiP. The packaging strategy needs to be modified to accommodate the needs of MEMS packaging [13, 22].

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4

SILICON MICROFABRICATION BASED PM SENSOR

With the increasing public awareness of the impact of PM on human health, real-time monitoring of PM exposure level has attracted more interest than ever before. While a great deal of effort has been put into the miniaturization of PM sensors, a wider range of applications is still hindered by big form factor and high cost. In this chapter a novel design of PM sensor based on silicon microfabrication is presented. Silicon microfabrication and assembly process enables relatively small form factor and low cost. The operation principle of the sensor is light scattering, an indirect way of measuring PM concentration. Silicon-based microfluidic channel serves as air flow path including the sensing chamber where the light scattered by aerosol particles is detected. The chips are integrated in the form of bare dies, reducing the size of the whole system compared with PCB assembly of packaged devices. The sensor has a compact size of $15 \times 10 \times 1\ mm^3$*, enabling easy integration into portable and wearable electronics. The light source in the sensor consumes less than 5 mW of power and the total power consumption is still low enough to make it suitable for battery-powered devices. In-lab and field testing has shown that the sensor can achieve an accuracy of less than* $5\ \mu g/m^3$ *and prompt response (within seconds) to particle concentration changes. Detailed design, fabrication as well as testing results will be explained in this chapter.*

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4.1. INTRODUCTION

AIRBORNE particulate matter monitoring has aroused numerous attention in the past decades due to the negative impact of particles on human health [2, 3]. With the increasing public health awareness, standards and rules for exposure limits of PM have been formulated by different governments and organizations. In most of current standards, the quality of the air is documented by the particle mass concentration in size fractions up to 2.5 µm ($PM_{2.5}$) or 10 µm (PM_{10}), e.g. in the EU the 24-hour limit value of PM_{10} is 50 µg/m^3 and in US the 24-hour limit value of PM_{10} and $PM_{2.5}$ is 150 µg/m^3 and 35 µg/m^3, respectively [4–6].

While high demand has been posed on continuous personal monitoring of PM exposure levels, the currently available PM monitors lack either the portability due to big form factor or measurement accuracy. Generally, methods of measuring PM concentration can be categorized into two types: direct methods and indirect methods. Direct methods collect PMs on either a physical filter or a sensing element, and then analyse the output caused by the captured PMs. The most reliable output is the mass of the PMs obtained by weighing the filter [7]. Conventionally the density of the PMs on the filter can also be analysed by β-ray, known as β-ray attenuation method (BAM) [8, 9]. When a sensing element is used to collect PMs, the PM concentration is usually calculated by the shift of some parameter of the sensing element caused by the increment of PMs. Such methods include tapered element oscillating microbalance (TEOM) [10], quartz crystal microbalance (QCM) [11], surface acoustic wave (SAW) [12], and film bulk acoustic resonators (FBAR) [13]. These methods also differ in the way the PMs are collected. Gravimetric collecting is a passive way, relying on the gravity of the PMs. To accelerate the collecting process, more active approach has been adopted. Electrostatic precipitation method charges the PMs and measures the current carried by them [14]. Thermal precipitation method can also be used to speed the collection of PMs [13]. Indirect methods analyse some parametric change generated by the existence of PM without physically capturing them. Light scattering is the most widely used methods in portable PM monitors [15–17]. Compared with direct methods, light scattering enables continuous real-time monitoring of particle concentration. Moreover, light scattering provides the possibility of making simple and compact sensors enabling a wider range of applications. In this chapter, we present the design and fabrication of a miniaturized PM sensor, and demonstrate the performance of the sensor by laboratory testing. The proposed sensor uses light scattering method to analyse the particle mass concentration. Compared with currently available commercialized PM sensors, our proposed sensor has relatively small form factor (15 mm × 10 mm × 1 mm) and low power consumption, enabling easy inte-

gration into a portable or even wearable device, such as cell phones or smart watches. The presented sensor is an upgraded version of the prototype previously developed by our group and shows enhanced performance [18]. The rest of this chapter is structured as follows: Section 4.2 describes the principles of operation of our sensor and the design of the sensor. The microfabrication and assembly process of the PM sensor is described in detail in Section 4.3. Section 4.4 describes the experimental testing and presents the experimental results. Finally, Section 4.5 summarizes the features of the sensor and possible improvement aspects and discusses future work.

4.2. SYSTEM DESIGN

The operation principle of the proposed sensor is light scattering. In general, PMs scatter light when illuminated and thus cause incident light diverted from its original direction. The intensity of the scattered light links to the concentration of PM so by analysing the former the latter can be calculated. Light scattering has wide application to chemistry, biology and physics [19]. Figure 4.1 illustrates a schematic of the sensor with the functions of each component. The sensor consists of a sensing unit and control circuitry. In this section, the design of each component will be explained in details.

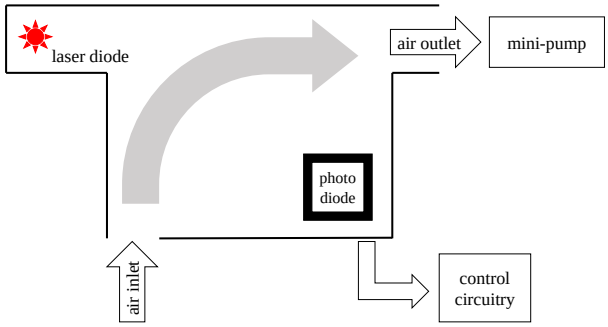


Figure 4.1: Schematic of the sensor components. The main part is the sensing unit, hosting a light source and a photodiode inside the sensing chamber, connected with the control circuitry and a mini-pump.

4.2.1. THE SENSING UNIT

The sensing unit is formed by two stacked silicon submounts, with the size of 15 mm × 10 mm × 1 mm, the fabrication of which will be discussed in Section 4.3. The bottom silicon submount hosts the chip elements as well as the interconnections. A red light laser diode with a wavelength of 650 nm is used as a light source in this work. A photodiode (T1670P, Vishay Inc.), used as light receiver, is placed into a cavity. On each submount, two pairs of light source and receiver are assembled for design redundancy as well as easing the sensor testing. Laser diodes with different wavelengths can be mounted on each side of the sensor to accommodate wider range of particle size and composition. On the edge of the bottom submount, metal pads are placed for connecting all the chips with external control circuitry. The top submount contains air flow channels with inlet and outlet. When the two submounts are stacked, a sealed sensing chamber is formed with light source and receiver in between, as illustrated in Figure 4.2. No physical or virtual filter is designed in this sensor so no particle size selection will be applied. The readings of this sensor will represent the total airborne particle mass concentration.

Light scattering based PM monitors have been commercialized while miniaturization of such is rarely available from literatures or products. Different from most commercialized particle monitors [15], in our miniaturized sensor the light source and receiver are placed in the same chamber without using optics except for a short channel collimating the diverted light from the laser diode. Though the laser diode and photodiode are placed in such a way that no direct light incidents on the photodiode, light can still be reflected onto the photodiode inevitably by the inner surface of the chamber. The PMs will scatter the incident light when they pass through the chamber with the air flow. Due to the light scattering effect, the photodiode is expected to receive more light. Figure 4.3 illustrates the light scattering effect of aerosol particles.

To find out the correlation between the particle presence and the intensity of the light received by the photodiode, optical simulation is first conducted. In theory, different scattering mechanisms apply to the particles with different size fractions [20]. Relative size of a scattering particle is defined by *size parameter*, the ratio of its characteristic dimension and incident wavelength

$$x = \frac{2\pi r}{\lambda}, \tag{4.1}$$

where r is its characteristic length (radius) and λ is the wavelength of the incident light [21]. Assumed as spheres, particles with diameter of 2 μm or above (x » 1, considering red light with wavelength of 650 nm) act as geometric optics, scattering light according

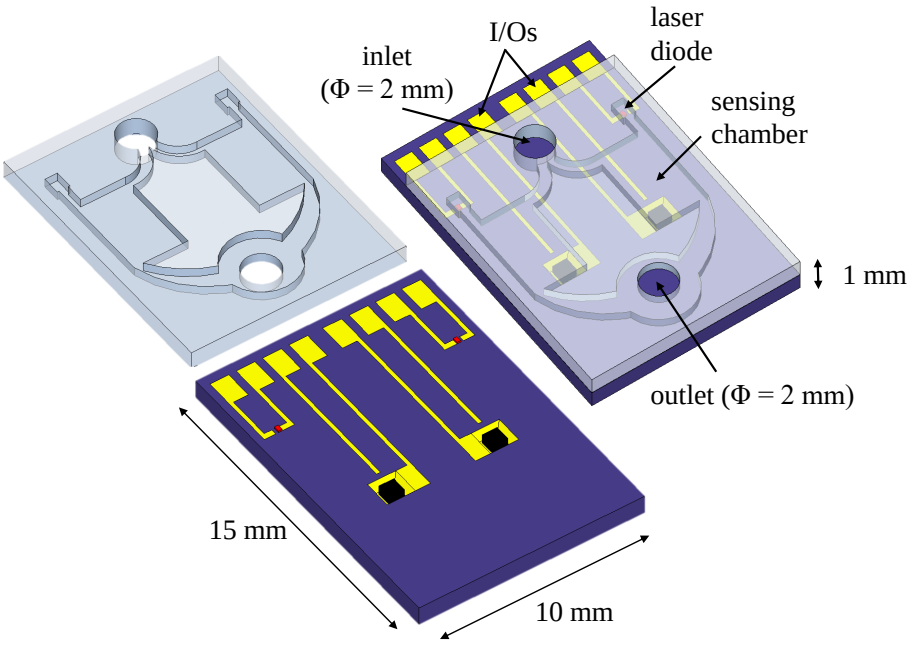


Figure 4.2: Layout of the sensing unit. Bottom submount accommodates chips and electrical connections while top submount forms air channel and sensing chamber by stacking onto the bottom half.

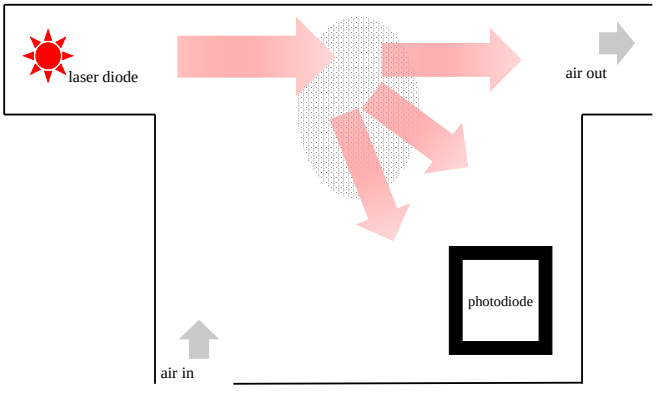


Figure 4.3: Schematic of light scattering effect of aerosol particles passing through the sensor.

to their projected area. Rayleigh scattering applies to the particles with very small size (r < 20 nm, x « 1). The intensity of light scattered by small spheres of diameter d and refractive index n from light of wavelength λ and intensity I_0 is given by

$$I = I_0 \frac{1+\cos^2\theta}{2R^2}\left(\frac{2\pi}{\lambda}\right)^4\left(\frac{n^2-1}{n^2+2}\right)^2\left(\frac{d}{2}\right)^6, \tag{4.2}$$

where R is the distance between the observation point to the particle and θ is the scattering angle. For particles with sub-micrometer size (100 nm ~ 1 μm, x ≈ 1), Mie scattering mechanism predominates the scattering effect. This scattering produces a light pattern like an antenna lobe, with a sharper and more intense forward lobe for larger particles. Unlike the Rayleigh scattering strongly favoring short wavelength, Mie scattering is not very wavelength dependent. Since Rayleigh scattering only dominates for nano-particles, for PM sensor, geometric optics scattering and Mie scattering are mainly of concern. Because Mie scattering is not very wavelength dependent, and geometric optics scattering does not favor specific wavelength, the wavelength of the light source used in the sensor should not affect the sensitivity. Both visible light and infrared have been used in commercialized PM monitors.

Table 4.1: Key outputs of ray tracing simulation.

	Total flux (W)	Flux/emitted flux (%)	Incident rays
Without PM	3.88×10^{-7}	0.01	14
With PM	3.44×10^{-5}	0.96	18

TracePro is used to analyze the light scattering of particles in this work. This software uses geometric models to trace the light rays so it is only suitable for analyzing coarse particles, i.e., diameter of 2 μm and above [22]. The inner surface of the chamber is simulated as silicon with tunable reflectivity. Red light with wavelength of 650 nm is modelled as the beam light source. The particles are simulated as distributed spheres with a diameter of 2.5 μm and a reflective surface. Representative results are shown in Figure 4.4 and key outputs are summarized in Table 4.1. The spatial distribution of the particles has significant influence on the scattered light intensity and in some cases, i.e., listed in Table 4.1, the scattered light dominates the total light received by the photodiode. Also noted from the simulation is the impact of the reflectivity of the chamber on the light distribution.

It was found that the intensity of the light received by the photodiode could be dramatically affected by the surface reflectivity. In one of the simulation models, 5 % in-

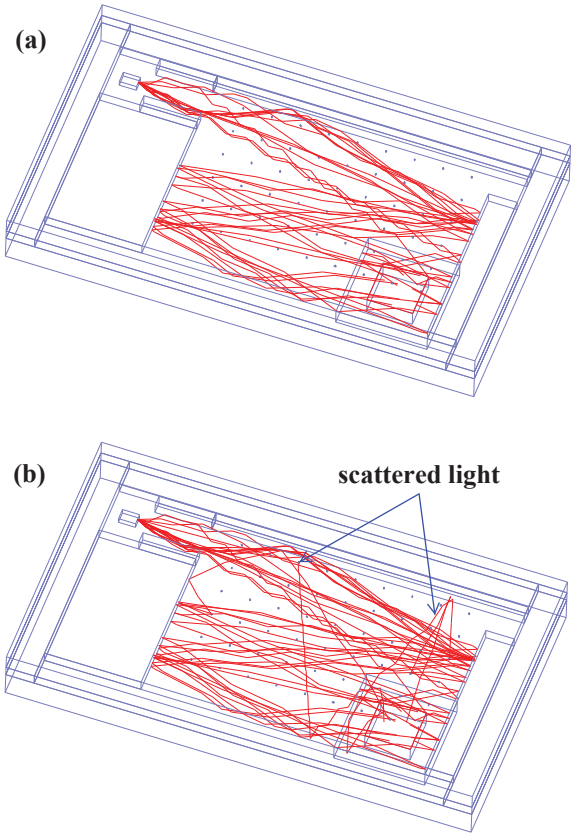


Figure 4.4: Ray tracing simulation result: more light is received by the photodiode in the case where PM presents (b) than the one without any PM (a). Only light rays received by the photodiode are shown.

crease of the surface reflectivity (from 20 % to 25 %) doubles the intensity of the light received by the photodiode as shown in Figure 4.5. This may imply that the output of the photodiode in real application can be significantly influenced by the property of the material of which the sensor is made out. Another factor that has been noticed to affect the output of the photodiode is the dimension of the sensing chamber. As explained earlier this section, the chamber reflects light to the photodiode no matter whether the PMs exist or not. So the dimension of the chamber will shift the baseline of the output of the photodiode. In the simulation, the power of the laser diode is set as 5 mW, and Figure 4.6 shows the output of the photodiode with varied dimension of the sensing chamber. If the sensing chamber is shortened by 0.5 mm from 3.5 mm in the direction of emitted light, the output of the photodiode is increased by more than 100 %, mostly due to the

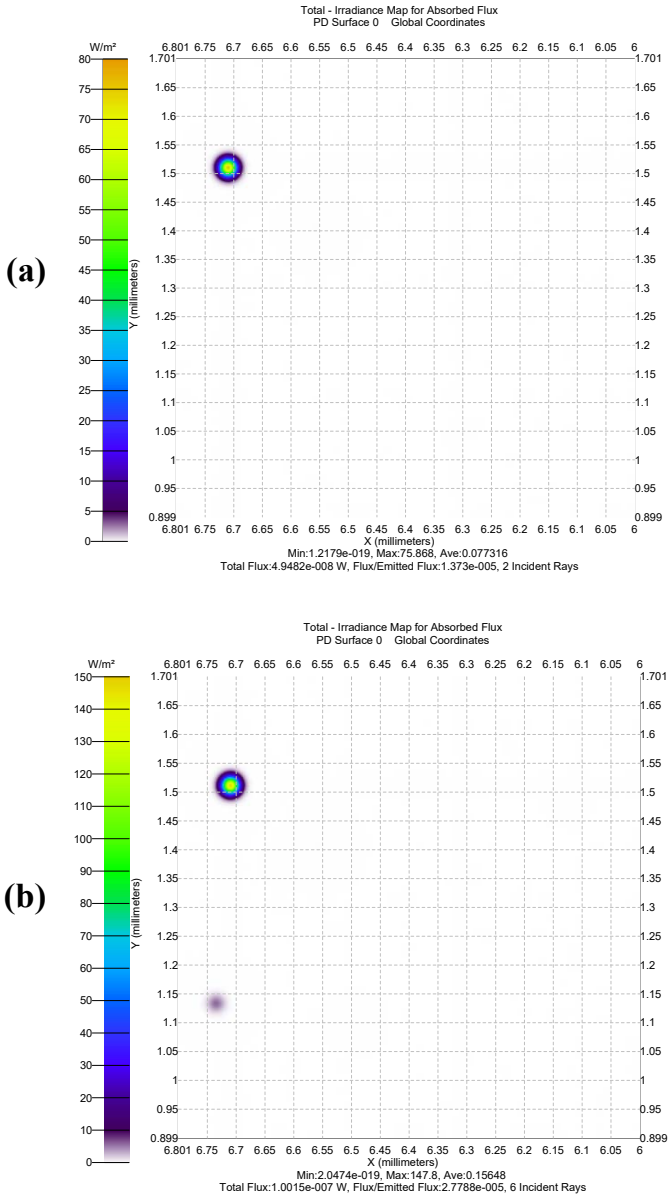


Figure 4.5: Map of light rays received by the photodiode (with PM) at different reflectivity: (a) 20 %, (b) 25 %. 5 % increase of reflectivity doubles the light intensity.

increase of the baseline of the photodiode. To make the output of the photodiode fall into a certain range for better sensing, both the material and structural factors need to be tuned with matching readout circuitry. Moreover, other factors such as the power and

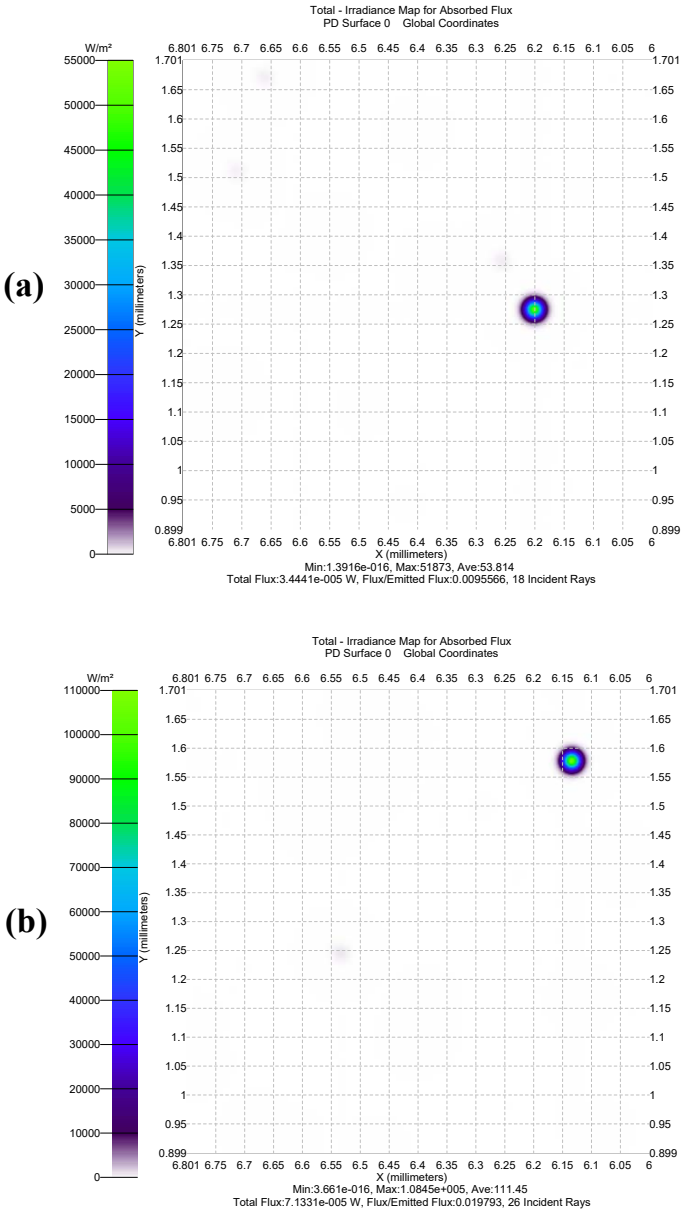


Figure 4.6: Map of light rays received by the photodiode (with PM) at different sensor dimension: (a) 3.5 mm long, (b) 3 mm long. 0.5 mm shrink of long side increases more than 100 % of the light intensity.

wavelength of the light source, the specification of the photodiode, the air flow rate, and even the performance of the supporting circuitry should all have impact on the sensor

performance.

4.2.2. CONTROL CIRCUITRY

The customized control circuit functions as the driver of the light source and the readout circuit of the photodiode. Figure 4.7 shows the schematics. A constant current driver IC is used to power on the laser diode. A PWM signal, generated by a micro-controller unit (MCU), switches on / off the driver at a proper frequency. An amplifier IC together with a RC loop amplifies the light current generated by the photodiode and then sends it to the MCU, where the analog signal is converted to digital signal. The converted digital signal can be read out by an external device, i.e., a personal computer, through a serial port (RX and TX).

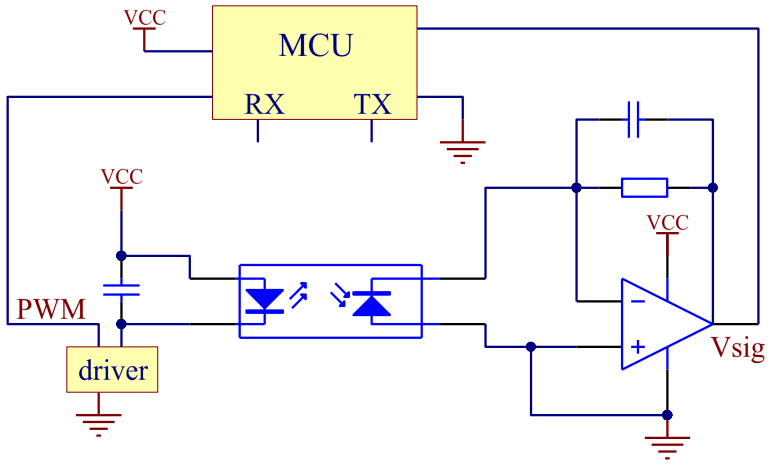


Figure 4.7: Schematics of the control circuit of the PM sensor.

4.3. FABRICATION AND ASSEMBLY

The sensing unit has been fabricated through silicon micromachining and packaging process. As mentioned beforehand, the sensing unit consists of a silicon submount stack. The fabrication of submounts is firstly conducted and then the assembly of submounts is carried out.

4.3.1. BOTTOM SUBMOUNT

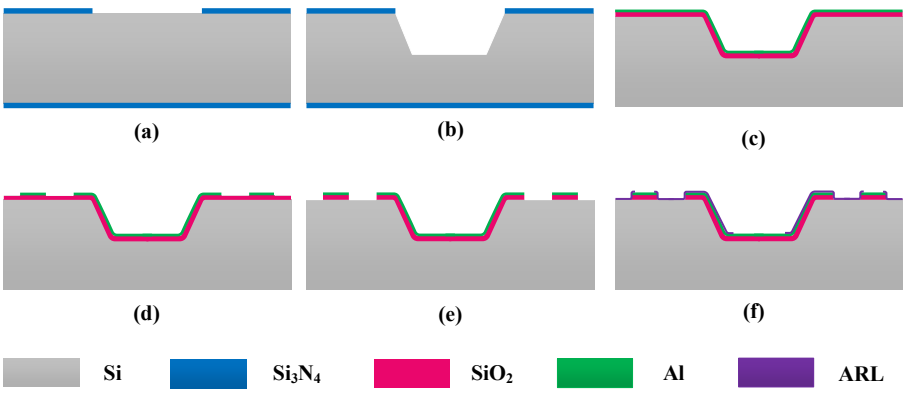


Figure 4.8: Fabrication process flow of bottom silicon submounts: (a)mask layer patterning (b) silicon wet-etching (c) insulation and metallization (d) metal trace patterning (e) insulation layer patterning (f) ARL coating.

The bottom submounts are fabricated on 500 µm-thick 4-inch p-type, <100> orientation, silicon wafers. The process starts by depositing 200 nm of silicon nitride on top side of the wafer by low pressure chemical vapor deposition (LPCVD) at 850 °C. This layer is patterned with contact lithography using spin-coated positive photo resist and etched in fluorine plasma etcher to form a hard mask for wet Si etching. Afterwards the resist is removed by oxygen plasma etching (Figure 4.8(a)). Cavities are etched in the bulk Si using 40% KOH solution at 80 °C to the depth of 300 µm (Figure 4.8(b)). The approximate etch rate (ER) is 50 µm/h and total etching time is 6 h. The nitride masking layer is then removed by plasma etching. Afterwards a SiO_2 isolation layer of 3 µm is coated by plasma enhanced chemical vapor deposition (PECVD). Al is then sputtered by physical vapour deposition (PVD) for the interconnections between the ICs on the submount with layer thickness of 1 µm (Figure 4.8(c)). Because the submount contains deep etched cavities, spray-coated positive photoresist, with the nominal thickness of 9 µm on the top surface, has to be used for metal patterning. The Al layer is dry etched using plasma etcher and the submounts are finalized by removing the photoresist with O_2 plasma (Figure 4.8(d)). An anti-reflective layer (ARL) on top of the silicon submount surface is then coated. To do this, the oxide isolation layer is dry-etched after the Al etching to expose the silicon wafer surface (Figure 4.8(e)). Then a lift-off process step is conducted to form the anti-reflective layer. Negative photoresist is coated on the wafer and patterned to expose most of the wafer surface except for the electrodes for IC interconnections. Then a layer

stack of $TiO_2/SiO_2/TiO_2/SiO_2$ is deposited by evaporation. The thickness of each layer in the layer stack is determined according to the light source parameters. The photoresist lift-off is done by boiling the wafer in acetone (Figure 4.8(f)).

4.3.2. TOP SUBMOUNT

The top submounts only contain microfluidic channels and inlet and outlet through holes. The wafers used are double-side polished, <100>, with the thickness of 500 µm. A SiO_2 masking layer of 300 nm is first thermally grown. The oxide layer on the front side of the wafer is patterned using dry etching (Figure 4.9(a)). Deep reactive ion etching (DRIE) process is carried out for the formation of micro-fluid channels (Figure 4.9(b)). Then the wafer is flipped and the oxide layer on the back side is patterned (Figure 4.9(c)). DRIE process is again conducted to form the through holes (Figure 4.9(d)), followed by removing the oxide masking layer (Figure 4.9(e)). Same as bottom wafers, an anti-reflective layer can be optionally coated on the front side of the wafer (Figure 4.9(f)).

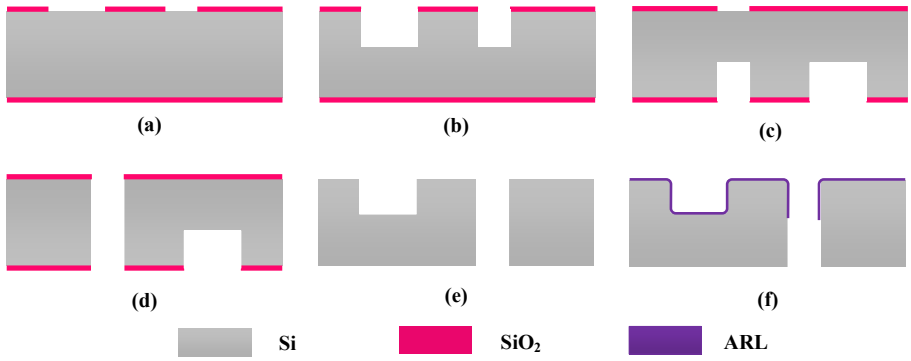


Figure 4.9: Fabrication process flow of top silicon submounts: (a) front side mask layer patterning (b) front side DRIE (c) back side mask layer patterning (d) back side DRIE (e) mask layer removal (f) ARL coating.

4.3.3. FINAL ASSEMBLY

The submount silicon wafer is singulated into chips. The assembly process consists of bare die IC connection, submount stacking and external connection. The bare die laser diode and photodiode are placed on the bottom submount and connected with electrode by conductive silver adhesive. Wire bonding is used to connect upper electrodes of bare dies to the submount pads. Then, the top submount is aligned and mounted on the bottom submount by adhesive bonding. To further prepare for the later sensor test-

ing, the assembly is mounted on a piece of PCB, through which the I/Os of the sensor would be connected to the control circuit board. A fraction of plastic pipe is glued over the air outlet to connect with a micro-pump, which pulls the air from inlet to outlet by negative pressure leading to air flow rate of 20 mL/min. Figure 4.10 shows an assembled sensor ready for testing.

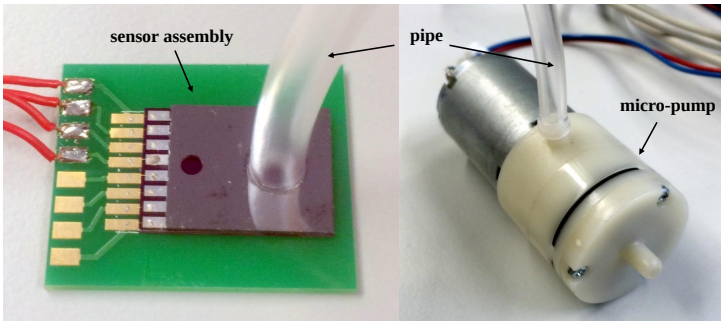


Figure 4.10: Sensor assembly connected with micro-pump for testing.

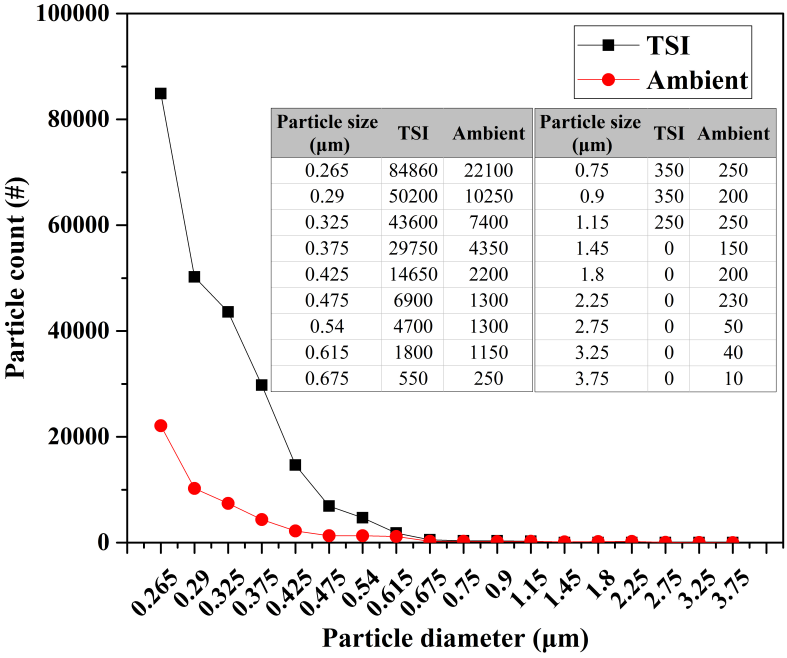
4.4. TESTING AND CHARACTERIZATION

The assembled sensors are tested under laboratory conditions to evaluate their performances. Different types of particles are used to evaluate the sensor performance and calibration is also carried out with reference particle counter.

4.4.1. TESTING SETUP

The sensors are tested in a 25 m^3 environmental chamber. A calibrated portable aerosol spectrometer (OPC 1.109, GRIMM Inc.) is used as reference for real-time particle concentration monitoring. The GRIMM monitor has been widely used and proved as a trustable particle concentration monitor with a deviation factor of max. 3% [23–25]. Both the GRIMM monitor and tested sensors are placed in the middle of the testing chamber. An aerosol generator (Model 3076, TSI Inc.) is used to generate very fine salt (NaCl) aerosols. The TSI aerosol generator consists of a Collison-type atomizer that gen-

erates aerosols of constant particle size and a diffusion dryer to dry and remove water vapor from aerosol [26]. Figure 4.11 shows the size distribution of the particles generated by TSI aerosol generator (black curve). It is noted that the particle size concentrates at submicron range and most of the particles are with a diameter of 0.5 µm or below. This distribution resembles the scenario of ambient air. The fine particles always outnumber the coarse ones in natural air condition, while the particular size distribution highly depends on the types of particles and local weather conditions and so on. In comparison, Figure 4.11 also shows a particle size distribution of ambient air dust in our office on the same day. As discussed above, submicron particles dominate the size fraction. Different from the particles generated by the TSI atomizer, ambient air in the office contains more coarse particles (> 1 µm) while less fine particles although in both cases the total particle concentration is around 10 µg/m^3.



Particle size (µm)	TSI	Ambient	Particle size (µm)	TSI	Ambient
0.265	84860	22100	0.75	350	250
0.29	50200	10250	0.9	350	200
0.325	43600	7400	1.15	250	250
0.375	29750	4350	1.45	0	150
0.425	14650	2200	1.8	0	200
0.475	6900	1300	2.25	0	230
0.54	4700	1300	2.75	0	50
0.615	1800	1150	3.25	0	40
0.675	550	250	3.75	0	10

Figure 4.11: Typical size distribution of aerosol particles: TSI atomizer (black) and indoor ambient air (red). Inset summarizes the particle amounts for each case.

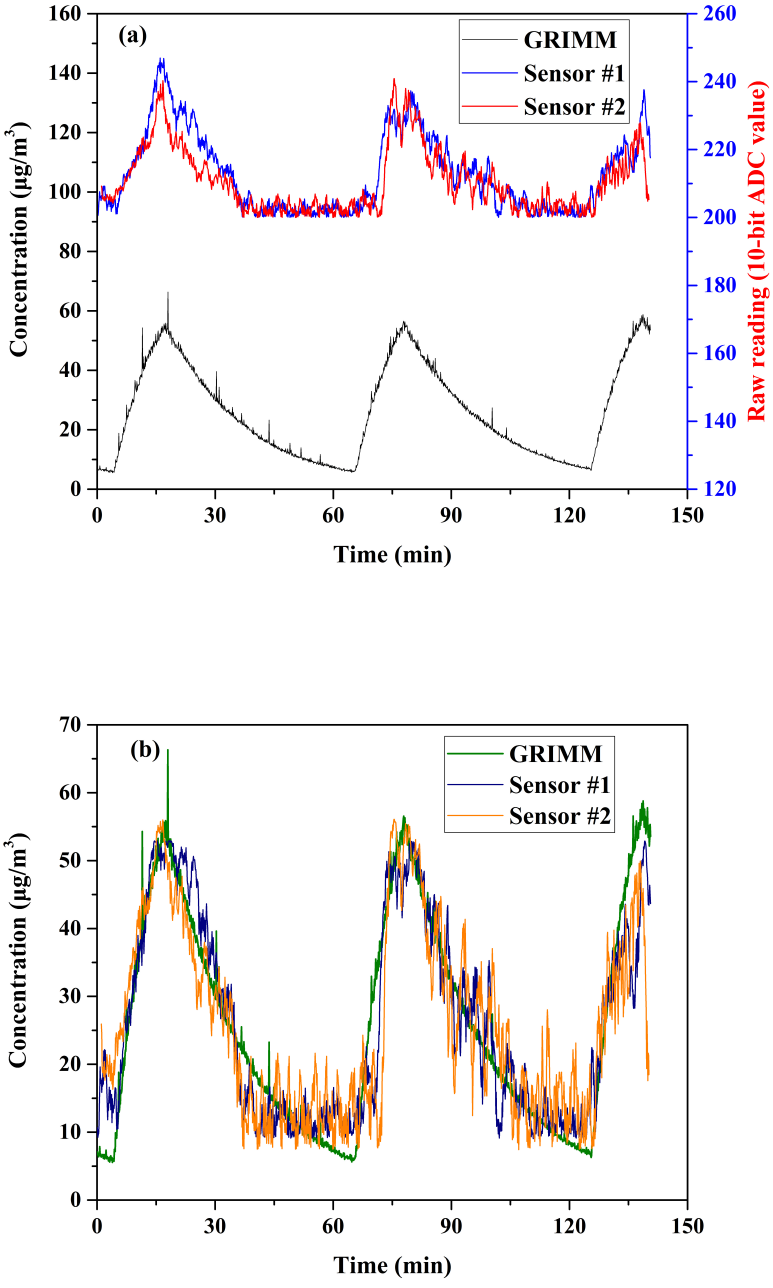


Figure 4.12: Representative readings from the tested sensors and the reference monitor: (a) raw data, (b) calibrated data.

4.4.2. TESTING RESULTS

During the testing, the aerosol generator works periodically with each working cycle consisting of a 15-minute on-time and 45-minute off-time. The sensors are sampled at a frequency of 16 Hz. The GRIMM monitor, however, is preset to give a reading every 6 seconds. Therefore, we average the sensor measurements to fit this lower sampling interval. Figure 4.12 (a) shows the sample data from two tested sensors and the reference aerosol monitor. The x-axis represents the elapsed time from the beginning of the test and plotted on the y-axis is the raw data of the tested sensors (10-bit ADC-values, upper curves) and the PM concentration measured by the GRIMM monitor (in $\mu g/m^3$, lower curve). During the aerosol generator on-period, the particle concentration in the testing chamber rises and peaks around 55 $\mu g/m^3$ according to the GRIMM monitor readings. After the generator is switched off, the concentration slowly drops to under 10 $\mu g/m^3$. Our sensors clearly catch the concentration change but the lower detection limit is observed. Both linear and polynomial regression analysis with different polynomial orders are conducted between the readings of our sensor and the GRIMM reference. To evaluate the quality of curve fitting, the *Standard Deviation (SD)* and *Mean Absolute Error (MAE)*

$$MAE = \frac{1}{n}\sum_{i=1}^{n}|f_i - y_i|, \tag{4.3}$$

are computed and the results are summarized in Table 4.2 in which the polynomial order of 1 stands for linear regression. Also listed in Table 4.2 are the values of *R-square* of the regression analysis. According to the regression result, the best fitting is achieved by the 3^{rd} degree and 2^{nd} degree polynomial regression for sensor *#1* and sensor *#2*, respectively. The achieved measurement accuracy reaches 4.38 $\mu g/m^3$ and 5.80 $\mu g/m^3$, respectively.

Table 4.2: Results of regression analysis.

Polynomial order		1	2	3	4
SD $(\mu g/m^3)$	Sensor *#1*	6.35	5.91	**5.81**	15.35
	Sensor *#2*	8.11	**7.72**	21.05	39.50
MAE $(\mu g/m^3)$	Sensor *#1*	4.74	4.43	**4.38**	14.29
	Sensor *#2*	6.27	**5.80**	19.48	38.44
R-square	Sensor # 1	0.836	0.858	0.863	0.867
	Sensor *#2*	0.730	0.756	0.770	0.776

The best polynomial fitting curves are shown in Figure 4.13 and accordingly the calibrated readings of the sensors are depicted in Figure 4.12 (b), which indicated the lower

detection limit under described testing conditions is around 10 $\mu g/m^3$. The existence of lower detection limit could be caused by the noise of the whole detecting system, consisting of photodiode, signal amplifier, analog/digital signal convertor and readout I/O. The actual output signal may be buried into the noise when the particle concentration is extremely low. In this sense, a more dedicated readout circuitry with cancelled noise would lead to an expanded detection range in the lower concentration direction.

Another test we carry out on the sensors is an indoor dust test. Both the GRIMM monitor and our sensor is placed in the office while the floor is swept by a broom. This test means to resemble the indoor air pollution scenario and to test the response of our sensors. The same calibration procedure is applied to raw data from the tested sensor and the calibrated readings are shown in Figure 4.14 with the reference readings from the GRIMM monitor. As the broom sweeps across the room, the PM concentration can reach as high as 200 $\mu g/m^3$. Due to the uneven spatial distribution of the PM in the room, the measurement of our sensor is not fully overlapped with the one from the GRIMM monitor. But the measurement results still show that our sensor possesses good capability of fast and reliable detection of indoor airborne particles.

4.5. CONCLUSION

Significant health risk caused by particulate matters has stimulated increasing need for portable or wearable PM monitors with real-time monitoring. In this chapter we present a novel approach of minimizing PM sensor based on light scattering and fulfilled by silicon microfabrication process. The laboratory testing results indicate that an accuracy of less than 6 $\mu g/m^3$ has been achieved. The compact form factor of our sensor makes it possible to ingrate into handheld electronics, such as smart phones or watches. The low power light source (less than 5 mW) used in the sensor and the low required air flow rate both help reduce the power consumption of the sensor, which is suitable for battery-powered devices. Possible future work includes the investigation of the effects of environmental factors, such as temperature and relative humidity, on the performance of the sensors. Furthermore, designated electronic circuits with efficient calculation algorism for reading out the photodiode signal would also help reduce the measurement noise and enhance the sensitivity and accuracy of the sensor.

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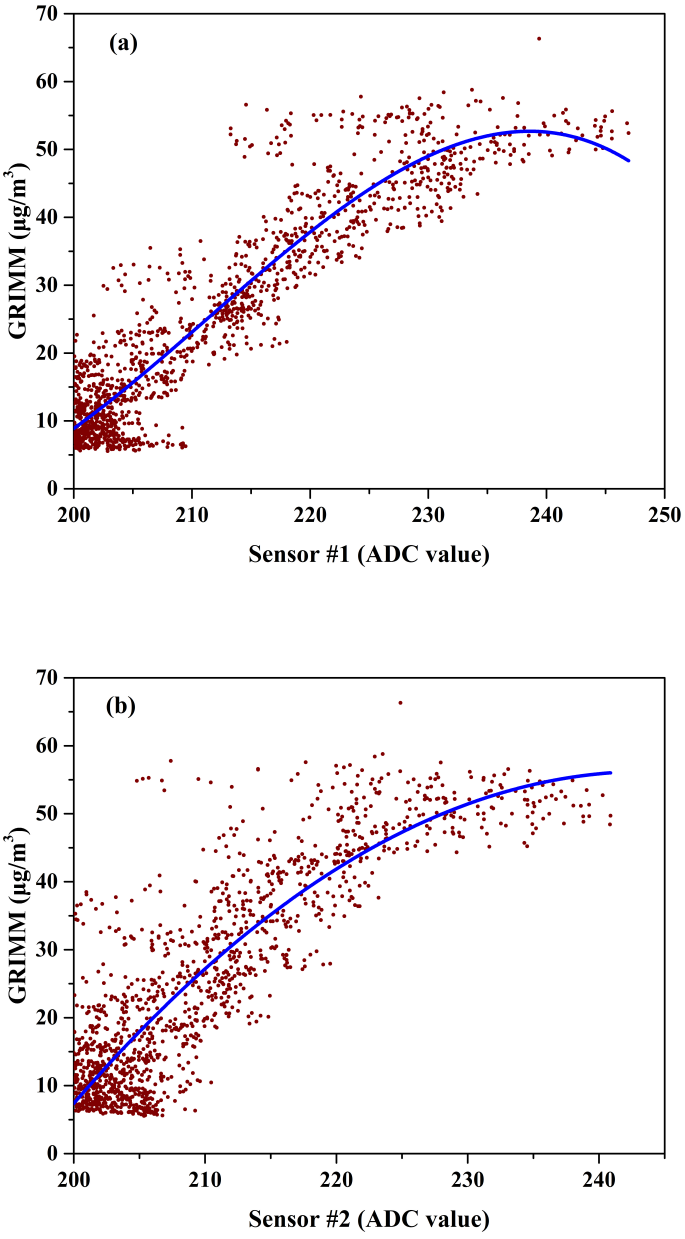

Figure 4.13: Result of optimized polynomial regression.

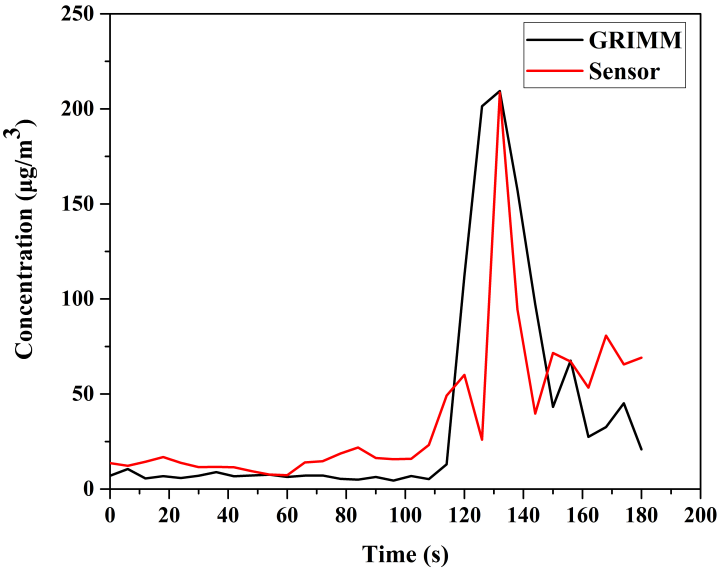

Figure 4.14: Indoor dust testing result. The tested sensor (red curve) shows fast and accurate response to indoor aerosol particle concentration change.

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5

INTEGRATED VIRTUAL IMPACTOR ENABLED $PM_{2.5}$ SENSOR

As more and more researches show that fine particles (diameter of 2.5 μm and below) pose risk on human health, an increasing need for monitoring fine particles has emerged. A minimized sensor designed for measuring $PM_{2.5}$ is presented in this chapter. Based on previous sensor development, the new $PM_{2.5}$ sensor maintains the same size of only 15 × 10 × 1 mm^3. A virtual impactor (VI) has been integrated as a particle size selector to filter out large particles. The design of the VI is optimized by simulation assisted analysis. The sensor is realized by similar silicon microfabrication and the adding of VI does not make the process more complicated. Metal bonding process is adopted for assembling the sensor and proved to enhance the sensor performance. Testing results show that the sensor performs comparably with advanced PM monitors. Potential improvement in future work has been presented in this chapter to give guidance for further optimization of the sensor performance.

5.1. INTRODUCTION

As more and more researches find, particle pollution in the air can cause serious health issues to human beings [1–4]. The damage caused by the inhaled particles is directly linked to their size. Fine particles less than 10 µm in diameter pose the greatest problems, because they can get deeper into our lungs, and some may even get into the bloodstream [5]. In the field of air pollution monitoring, particles in different size fractions are of concern, such as PM_{10} and $PM_{2.5}$. According to the International Standards Organisation (ISO), PM_{10} and $PM_{2.5}$ is defined as particles which pass through a size-selective inlet with a 50 % efficiency cut-off at 10 µm aerodynamic diameter and 2.5 µm aerodynamic diameter, respectively [6]. When monitoring the PM concentration, people need to know the information on the size of the PMs preferably.

Since the PM concentration is expressed by size fraction, it is not necessary to measure the size of PMs individually. Instead, an easy approach is to separate PMs according to their size into different fractions. To do this, there are two main types of ways: physical filtering and fluidic separation [7]. A physical filter acts as a mesh allowing only small particles to pass through while blocking out the large ones. By altering the mesh size, particles can be separated into multiple size fractions. Filters are widely used in air purifying systems to obtain clean air and the most widely known one is the HEPA (high efficiency particulate air) filter [8]. In the applications of biology and chemistry, membrane based filters are widely used to group particles by their size [9, 10]. Membranes have porous structure that acts like micro-mesh and separates particles. Fluidic separation relies on the inertia of the particles. When particles flow with air, it is possible to manipulate their trajectory by diverting air flow. The inertia of particles, linked with particle mass (size), will affect the path and thus separate the particles. Most widely used inertia approach includes impactor, cyclone and virtual impactor [11].

In this chapter, we present the design of a VI enabled $PM_{2.5}$ sensor and evaluation of the performance. The VI design is optimized by simulation assisted analysis and the sensor is realized by silicon microfabrication. The miniaturized sensor has same small size as the one presented in Chapter 4 and the microfabricated VI enables very low air flow rate and thus helps maintain very low power consumption. The rest of this chapter is organized as follows: Section 5.2 demonstrates the sensor design and the fabrication. The testing and characterization is described in Section 5.3. Section 5.4 explains several aspects of future improvement and provides recommendations for potential industrialization of developed sensor.

5.2. DESIGN AND FABRICATION

The particle separation method adopted in the sensor is integrated VI. The micro-hole structure in the physical filters makes air difficult pass through and thus results in high power consumption. Inertia based methods, on the contrary, require relatively low air flow to separate the particles. The miniaturization of cyclonic separation is challenging because it needs a cylindrical structure to speed the air rotating. Compared with conventional impactor, VI does not trap large particles inside it and thus reduces the possibility of clogging. Some other methods are also proposed to separate particles in the air, such as ultrasonic approach [12], but they all show design complexity for the sensor miniaturization. Several recent researches have shown that the integration of VI enables efficient particle separation and meanwhile maintains small form factor [13, 14].

Figure 5.1 illustrates 3D schematic of proposed $PM_{2.5}$ sensor. The VI is integrated in the microfluidic channel. Airborne particles enter the sensor from the air inlet and pass the VI through a jet. Large particles go directly to the outlet through via the minor flow channel, while the small particles instead divert with the major flow into the sensing chamber. Figure 5.2 displays the air flow path throughout the sensor. The VI is adjusted in such a way that only one air outlet is needed in the design. Detailed explanation of the design and fabrication follows in later sections.

5.2.1. VIRTUAL IMPACTOR

The virtual impactor is a subclass of the conventional inertial impactor. In conventional impactor, air is accelerated through a nozzle and directed at an impaction plate or surface, as shown in Figure 5.3(a). Large particles with sufficient inertia will be separated from the air stream and impacted on the impaction plate while small particles instead are able to follow the diverted the air flow. In virtual impactor, the impaction plate is replaced with a collection probe through which a slow jet of air is moving, as Figure 5.3(b) shows. The air flow moving in the collection probe consists only a small fraction of the total flow, known as “minor flow”, removes large particles from the total flow. Meanwhile, the major portion of the flow, known as “major flow”, is diverted carrying mostly small particles with low inertia [11, 15].

The separation (collection) efficiency is defined as the ratio of the concentration of the particles with specific size in the major flow to that in the original total air flow. The particle size, of which the separation efficiency is equal to 50 %, is defined as the cut-point of the VI. One characteristic of a virtual impactor is that particles smaller than the cut-point of the impactor remain in both the major and minor flows. Therefore, if the minor flow is 10 % of the total flow, then 10 % of the small particles will remain with the

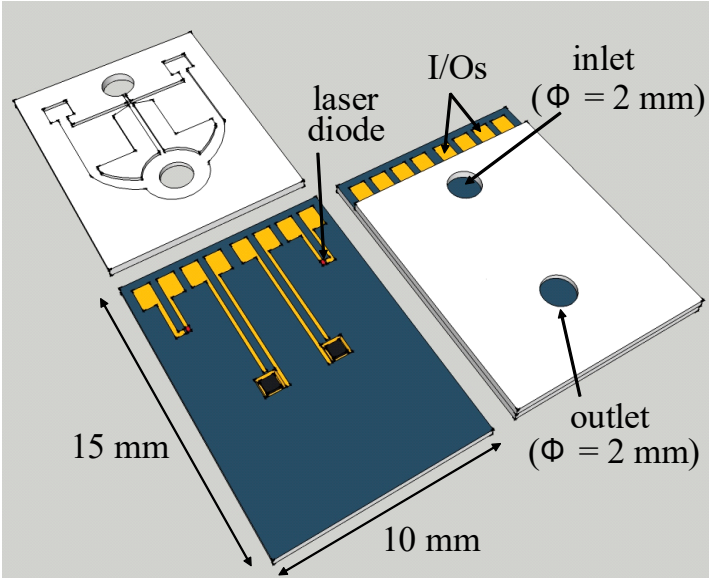

Figure 5.1: 3D schematic structure of the $PM_{2.5}$ sensor: chips are mounted on the bottom submount, and the microfluidic channel with integrated VI is formed on the top submount.

minor flow. Meanwhile, particles larger than the cut-point become concentrated in the minor flow [15].

The separation efficiency curve is determined by the ratio of major and minor flow and the physical dimension of the impactor. From [16], the cut-point is defined as

$$d_p = \sqrt{\frac{9\mu W^2 D(Stk_{50})}{\rho_p Q C_c}}, \tag{5.1}$$

where μ is the dynamic viscosity of the air, W and D is the width and depth of the VI, respectively, ρ_p is the particle density, Q is the total volumetric flow rate through the air inlet, and Stk_{50} is the Stokes number, which is recommended to be 0.59 for rectangular jet impactors [13]. The Cunningham correction factor, also known as slip correction factor, C_c, for particles larger than 1 µm is defined as

$$C_c = 1 + \frac{2.52\lambda}{d}, \tag{5.2}$$

where d is the particle diameter and λ is the length of the mean free path of the air.

In our design, the cut-point is selected as 2.5 µm. According to Equation 5.1, the only

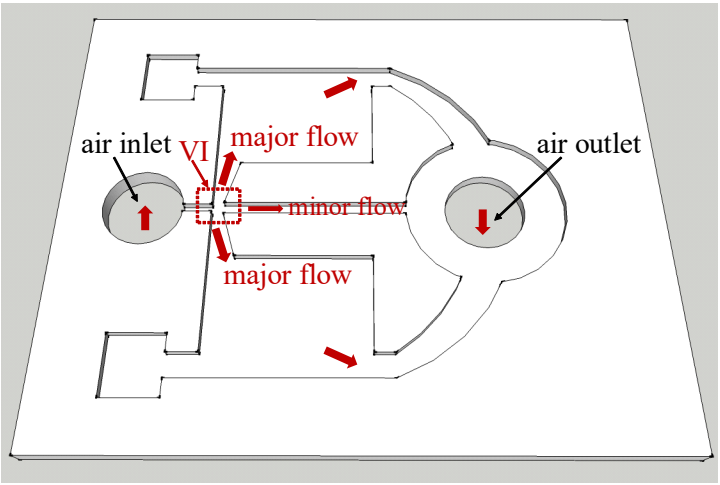

Figure 5.2: Schematic diagram of the air flow path inside the $PM_{2.5}$ sensor: air enters the sensor from the inlet and passes the VI, then gets separated The major flow passes the sensing chamber with $PM_{2.5}$ while the minor flow flushes out the larger PMs.

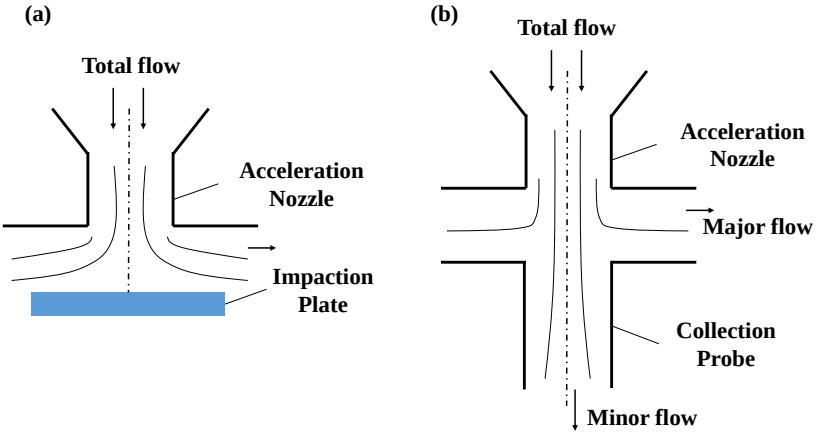

Figure 5.3: (a) Conventional plate (or jet) impactor and (b) virtual impactor (redrawn from [11]).

variables are the width of VI W, the depth of VI D and the total air flow rate Q, meanwhile, the ratio $\frac{W^2 D}{Q}$ remains constant. Since the VI is the bottleneck on the path of air flow in term of the air pressure drop, and less air pressure drop means less power consumption, the design of the VI is going to be optimized to minimize the air pressure drop. For an

incompressible and Newtonian fluid in laminar flow flowing through a long cylindrical pipe of constant cross section, the Hagen-Poiseuille equation applies for the calculation of pressure drop across the pipe [17]. According to the Hagen-Poiseuille equation, the pressure drop is defined as

$$\Delta P = \frac{8\mu LQ}{\pi r^4}, \tag{5.3}$$

where L and r is the length and the radius of the tube, respectively. For non-circular tubes, the term *hydraulic radius* can be used to make such calculation in the same way as for a round tube. It is defined as

$$R_h = \frac{A}{P}. \tag{5.4}$$

where A is the cross sectional area and P is the wetted perimeter of the cross-section. For circular tube,

$$R_h = \frac{1}{2}r; \tag{5.5}$$

for rectangular tube,

$$R_h = \frac{WD}{2(W+D)}, \tag{5.6}$$

where W and D is the width and depth of the cross section, respectively. Replace r with R_h in Equation 5.3, we have

$$\Delta P = \frac{\mu LQ}{2\pi {R_h}^4}. \tag{5.7}$$

For rectangular tube, the pressure loss can be expressed as

$$\Delta P = \frac{\mu LQ}{2\pi}\frac{16(W+D)^4}{W^4D^4}. \tag{5.8}$$

Since the ratio W^2D/Q is constant for our sensor, we have

$$\Delta P \propto \frac{L(W+D)^4}{W^2D^3}. \tag{5.9}$$

To minimize the Equation 5.8. For a given D, W can be expressed as aD, where a is a constant coefficient. Then,

$$\Delta P \propto \frac{(a+1)^4}{a^2}\frac{L}{D}. \tag{5.10}$$

Only when $a = 1$, ΔP reaches the minimum value, meaning square tube suffers least pressure loss. For a square tube, hydraulic radius $R_h = 1/4W$, then Equation 5.9 can be rewritten as

$$\Delta P \propto \frac{L}{R_h}, \tag{5.11}$$

or

$$\Delta P \propto \frac{L}{W}. \tag{5.12}$$

Understandably, shorter and wider channel gives lower air pressure drop. The dimension of VI is optimized using finite element simulation conducted by COMSOL. The optimization approach is as follows: given a tentative dimension of the whole channel and targeted cut-point (2.5 µm in this case), the total flow rate is calculated according to Equation 5.1. Then both the applied pressure and the topology of the channel are adjusted to obtain the cut-point at the calculated air flow rate. Table 5.1 lists the variables used in the calculation.

Table 5.1: Variables of the VI design.

Variable	Value
W	200 µm
D	200 µm
µ	1.8×10^{-5} Pa·s
λ	0.066 µm
ρ_p	1.2 g/cm^3
Stk_{50}	0.59

In one of the designs, the cross section of the VI is selected as a square with length of side of 200 µm. According to Equation 5.1, the needed air flow rate is 6.9 mL/min. Figure 5.4 shows the particle traces obtained from the simulation. Fine particles (1 µm) smaller than the cut-point remains in both the major and minor flows while larger particles are concentrated in the minor flow and barely collected in the major flow. The simulated particle collection efficiency curve is drawn in Figure 5.5, from which the 2.5 µm cut-point can be obviously located. From the simulation result, we find out that the total air flow rate is 6.5 mL/min, slightly lower than the theoretical value, and the major and minor flow consists 82.5 % and 17.5 % of the total flow rate, respectively.

The VI microfluidic channel is fabricated by silicon micromachining, the process of which will be discussed in the following section. Figure 5.6 shows the SEM image of the VI structure. In Table 5.2, key dimensions of the design are listed.

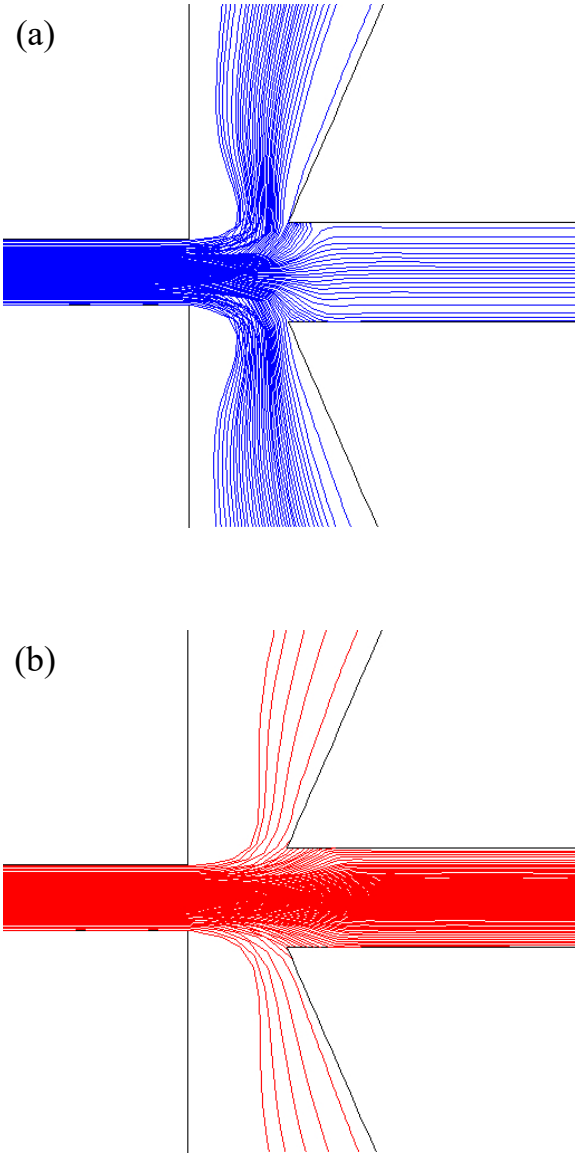

Figure 5.4: Particle traces simulation for particles with diameter of (a) 0.5 µm and (b) 5 µm.

5.2.2. OPTICAL DESIGN

The working principle of the sensor is light scattering. Inside the sensing chamber of the sensor, incident light from the light source is reflected by the walls. If the reflected light

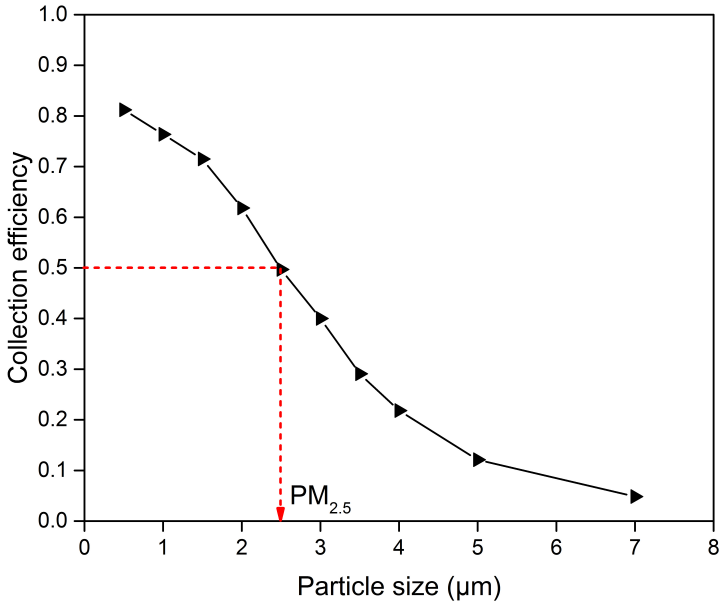

Figure 5.5: Particle collection efficiency curve obtained by simulation in COMSOL: cut-point is 2.5 μm.

Table 5.2: Key dimensions of the microfluidic channel in the $PM_{2.5}$ sensor.

Key parts	Length of VI injet	Width of the VI	Depth of the VI	Width of the major flow channel	Width of the minor flow channel
Dimension (μm)	1000	200	200	300	300

is too intense, the relatively weak scattered light may be covered. One of the reasons that a laser diode is used as the light source is that light beam from a laser diode is much more focused than other light emitting diodes and a constrained light beam reduces direct illumination on the photodiode. In the wavelength range of visible light, smooth silicon surface reflects about 30 % to 40 % of the incident light. To further reduce the reflection of the chamber walls, anti-reflective material can be coated on the surface. In the field of solar cells, such material is known as transmission enhancing material serving to increase the absorption of the light illuminated onto the solar cell surface. For the matter of our sensor, such material could be directly used although the reason behind this is slightly different.

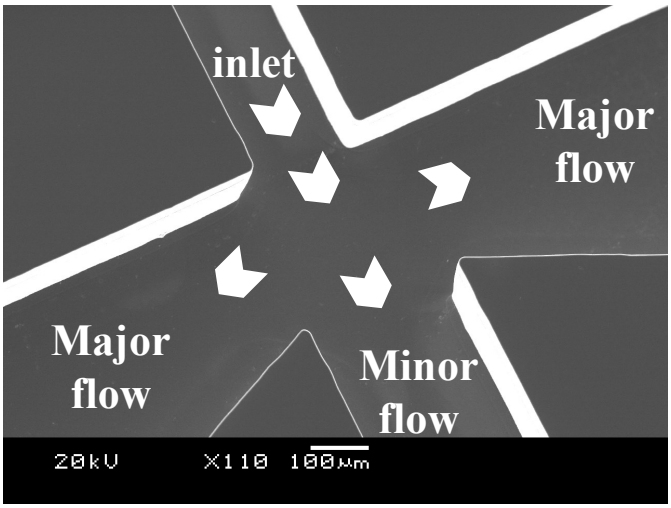

Figure 5.6: SEM image of microfabricated VI.

The material we have investigated is a layer stack structure, consisting of TiO_2/SiO_2 film pairs with silicon wafer as the substrate material. The purpose of the film stack is to reduce the reflectivity of the silicon surface at specific wavelength. Given the substrate material property, in our case it is silicon, and the wavelength of the illuminating light, some commercial software can calculate the required thickness of each layer in the stack. For example, two pairs of TiO_2/SiO_2 are needed on top of silicon wafer at wavelength of 650 nm and 750 nm. Table 5.3 lists the calculated layer thicknesses. Usually, the more pairs the stack has, the more accurate the calculated surface reflectivity will be. Considering the feasibility of material deposition, two-pair configuration is most used in our process. The deposition process of ARL has been discussed in Chapter 4. Figure 5.7 demonstrates the measured reflectivity on silicon wafers with different ARL configurations. As reference, the reflectivity of bare silicon wafer is also shown [18]. The reflectivity is dramatically reduced by the ARL material. At each targeted wavelength, the reflectivity drops as low as less than 2 % which means almost no reflection occurs on the surface. If a specific reflectivity is needed, the configuration of the layer stack needs to be tuned accordingly.

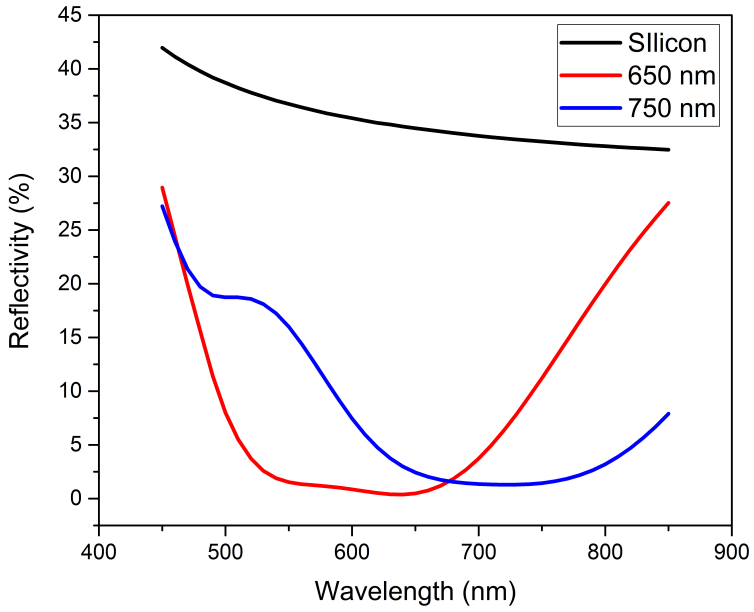

Figure 5.7: Measured reflectivity of silicon wafers with different ARL coating: 650 nm (red curve), 750 nm (blue curve) and bare silicon (black curve [18]).

Table 5.3: Configuration of different ARLs.

Targeted wavelength (nm)	TiO_2 (nm)	SiO_2 (nm)	TiO_2 (nm)	SiO_2 (nm)
650	66.40	88.06	108.43	84.83
750	73.13	138.85	126.53	98.48

5.2.3. SUBMOUNT FABRICATION

Similar as the process explained in last chapter, the $PM_{2.5}$ sensing unit is fabricated by silicon microfabrication. The improvement in the process flow will be highlighted in this section. Accordingly, the assembly process is upgraded as well.

BOTTOM SUBMOUNT

The structure of bottom chip is not affected by adding the VI. Same process can be adopted as described in last chapter. The anti-reflective layer (ARL) can still be optionally coated to tune the surface reflectivity as explained in last section (Figure 5.8(a)). To improve the submount bonding quality, metal bonding process is used to bond top submount with the bottom one. To achieve this, a bonding ring is formed during the microfabrication. Lift-off process is used for the deposition of the bonding metal. A thick layer

of photo resist is coated and patterned first, as shown in Figure 5.8(b). A layer of SiO_2 with thickness of 2 µm is deposited by PECVD. The bonding ring will cross the underneath aluminum traces so this SiO_2 layer acts as insulation layer between the two metal layers. Afterwards, a stack layer of Ti/Au with thickness of 50/200 nm is deposited on top by e-beam evaporation (Figure 5.8(c)). The photo resist is then removed by wet etching in acetone (Figure 5.8(d)). The fabricated submount is also shown in Figure 5.9.

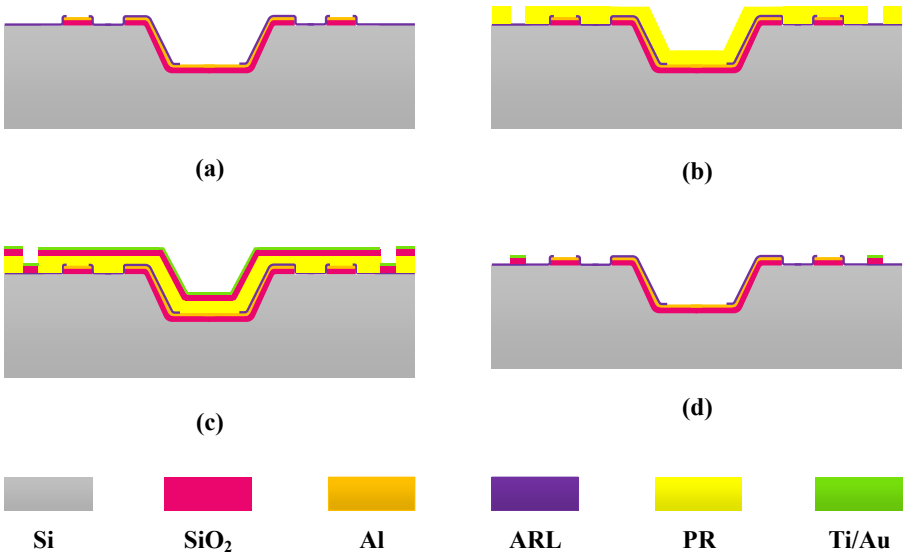

Figure 5.8: Fabrication process flow of bottom silicon submounts: (a) ARL coated (b) thick photo resist coated and patterned (c) silicon dioxide and Ti/Au deposition (d) photo resist lift-off.

TOP SUBMOUNT

The process flow of top submount remains the same because only the microfluidic structure is changed and the whole structure is still formed by DRIE process. The same process has been added to form the bonding ring pattern. The pattern on top submount is identical with the one on the bottom submount and same lift-off process is used, as shown in Figure 5.8. Fabricated submount is also shown in Figure 5.10. Due to the uneven topology of the top submount, the photo resist was not properly developed so that defects of metal pattern are noticed around the edge of dry etched cavity.

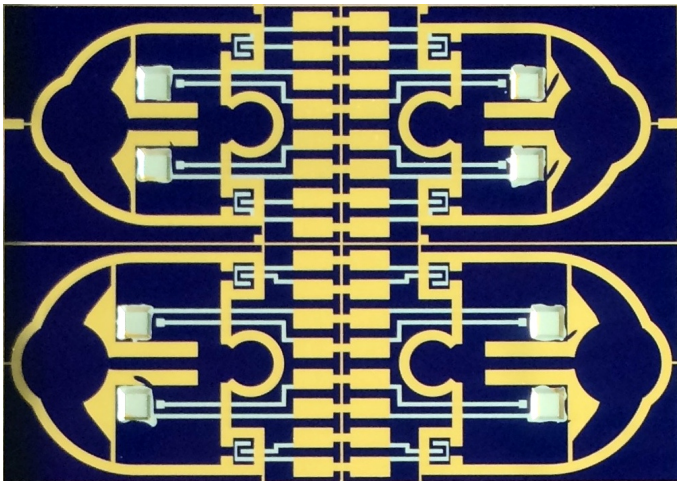

Figure 5.9: Fabricated bottom silicon submount with metal bonding ring.

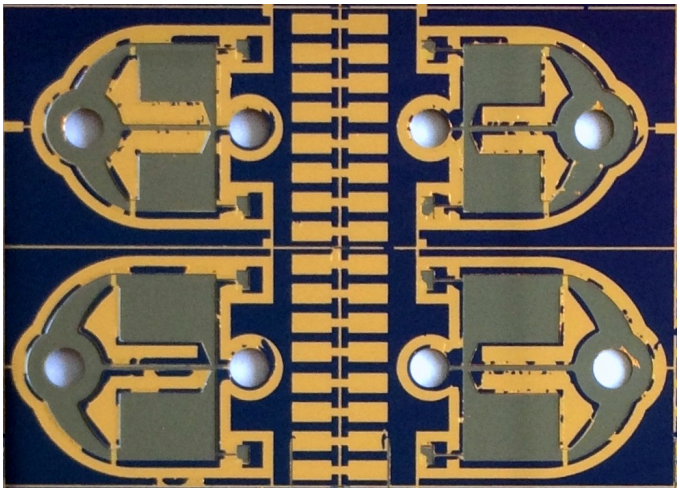

Figure 5.10: Fabricated top silicon submount with metal bonding ring.

5.2.4. PACKAGING AND ASSEMBLING

The same assembly process is used for die attach and die bonding. After assembling all the dies, the submount bonding is conducted with wafer bonder. The top and bottom submount are first aligned and then the submount pair is bonded at 350 °C for 30 mins under the pressure of 1.5 MPa. Metal bonding is expected to provide more solid adhesion and better sealing between submounts so that the air flow will be better controlled and interference of ambient light should be further eliminated.

5.3. TESTING AND CHARACTERIZATION

The same testing setup is used as in Chapter 4. Both lab testing and field testing have been conducted on sample sensors. The calibration is only done with lab testing data.

5.3.1. LAB TESTING

After collecting raw data from the sensors, both linear and polynomial regression analysis with different polynomial orders are conducted towards the GRIMM reference. The *SD* and *MAE* are computed and summarized in Table 5.4 in which the polynomial order of 1 stands for linear regression. Also listed in Table 5.4 are the values of *R-square* of the regression analysis. According to the regression result, the best fitting is achieved by the linear regression. The achieved measurement accuracy reaches 2.55 $\mu g/m^3$. The linear fitting result is shown in Figure 5.11 and the calibrated curve is drawn in Figure 5.12 together with the GRIMM readings.

Table 5.4: Results of regression analysis.

Polynomial order	1	2	3
SD ($\mu g/m^3$)	3.33	3.32	3.30
MAE ($\mu g/m^3$)	**2.55**	2.57	2.59
R-square	0.942	0.943	0.943

Compared with the sensors demonstrated in Chapter 4, the $PM_{2.5}$ sensor shows better performance in terms of sensing accuracy (from 4.38 $\mu g/m^3$ to 2.55 $\mu g/m^3$). The enhancement can be contributed by several factors. The integration of VI filters out coarse particles and narrows down the size range of sensed particles. Since coarse particles and fine particles scatter the light in varied ways, a confined measuring range gives better estimation of particle mass concentration. The improved packaging approach also helps reduce the noise introduced by ambient light and possible air leakage from the gap between submounts. The VI microstructure also helps shield the ambient light entering from the air inlet since the VI part is much narrower than the rest of the channel.

5.3.2. FIELD TESTING

An assembled sensor was also tested in the office environment. The air ventilation in the office is controlled by central ventilation system of the whole office building. The $PM_{2.5}$ sensor is used to monitor the air in the office for more than one hour. As shown in Figure 5.13, the particle concentration in the office follows a cyclic trend with a period of around 15 mins. Although the fluctuation is not much, the trend is quite evident. The

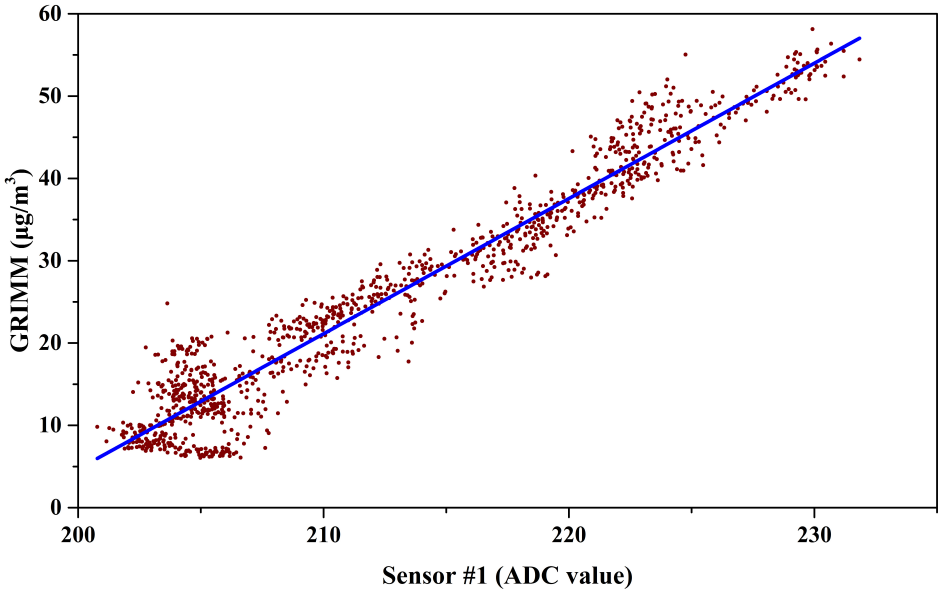

Figure 5.11: Linear regression of readings from the $PM_{2.5}$ sensor.

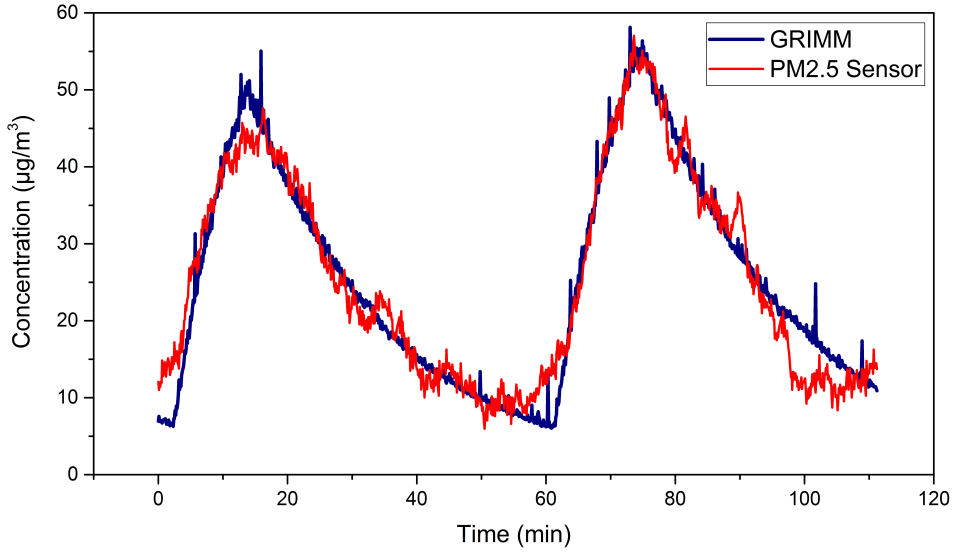

Figure 5.12: Representative readings from the $PM_{2.5}$ sensor (calibrated data) and the reference monitor.

result shows that the $PM_{2.5}$ sensor is suitable for indoor air quality monitoring.

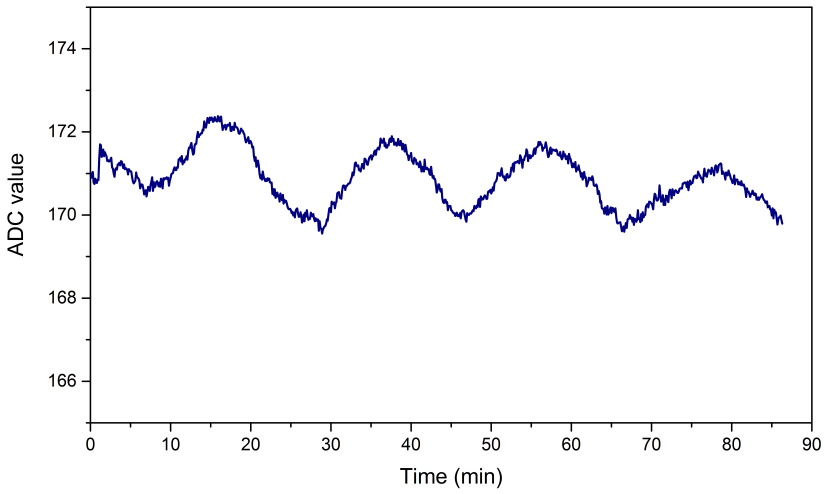

Figure 5.13: Sensor readings from a field test: central ventilated office room.

5.4. DISCUSSION AND RECOMMENDATION

The results have proved the design concept of the $PM_{2.5}$ sensor feasible and satisfying. To enhance the performance of the sensor, some potential aspects can be foreseen at this moment.

1) Particle deposition/clogging

During testing, some sensors give slowly shifting (increasing) output. This may be explained by the change of the reflectivity of the inner surface or characteristics of the photodiode, both due to deposition of particles. To prevent the direct contact of photodiode with the particles, the bare die photodiode can be encapsulated, for instance, by silicone. If the deposition of particles inside the sensor cannot be easily eliminated, some compensation algorism can be implemented, instead.

2) The fan/pump

So far, the sensing unit can be fabricated with very small form factor. However, to provide required constant air flow, extra device is still needed, such as a mini-pump mentioned in above sections. To make stand-along product, the air flow generator must be integrated, or even better, eliminated. Our test results show that without connecting any air flow generator, the PM sensor (without VI) can still detect the air quality change due to the ventilation system. The $PM_{2.5}$ sensor instead can not response well without connecting with the pump due to inadequate air flow passing through the sensor limited

by the narrow VI micro-channel.

Moreover, it is very possible and cost-effective to make such sensors based on cheaper material forming methods, such as injection molding or 3D printing. Development needs being done closely with: 1) substrate supplier and 2) packaging house.

The requirement for packaging substrates includes precise dimension and controlled surface roughness, i.e., reflectivity at certain light wavelength. The substrate should provide the main housing of the sensor, as well as metal traces for electrical interconnections. The supplier should possess capability of precise polymer forming (molding) and metallization on polymer (such as molding compound). The packaging process is not challenging, only involved is die-attach and die-bond. Besides, some customized assemble process may be needed, such as parts gluing and dicing.

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6

CONCLUSIONS AND OUTLOOK

This thesis presents a novel SiP design as a solution for system integration of intelligent applications. With era of intelligence coming, highly integrated smart modules and systems are in high demand while currently available technology does not always fit the needs of emerging applications. The research conducted and presented in this thesis aims to provide a designated solution to bridge the technology gap as well as promote wider range of the intelligent applications.

6.1. CONCLUSIONS

6.1.1. MULTI-PHYSICAL DESIGN

Development of intelligent systems always embraces multi-physical design because such systems deliver functionalities of various domains and require interactions with the surroundings in different ways. For instance, optical design is involved in lighting applications together with thermal, electrical and mechanical design. MEMS-based sensors need proper structural (mechanical) design together with electrical circuitry design. When SiP design is employed, the aforementioned design aspects become more challenging because the compact form factor poses additional limitations on the freedom of design.

Thermal management, among all design considerations, is especially critical for SSL applications. In the design presented in this thesis, first of all, silicon is the material used as the packaging substrate, which provides thermal benefits. Remote phosphor is an effective approach to reduce the thermal damage of phosphor from the LEDs. The analysis presented in Chapter 2 reveals the key parameters that need to be optimized for the design of remote phosphor in SiP modules. The thermal management further ex-

tends to the interaction among different components within a system, mainly between the heat sources and the heat sensitive components. For integrated smart lighting system, electrical components including active ICs and sensors are inevitably affected by the heat from the LEDs. In Chapter 2, simulation assisted analysis is conducted to help understand the influence of heat on different components within a compact integrated system. Recommendations are given on the design of a smart LED module to reduce the thermal impact by using thermal resistant material or by adding thermal separation structure. The silicon-based 3D SiP design for a smart LED module in Chapter 3 is proved more thermally effective.

The optical design and analysis are covered from Chapter 2 through Chapter 5 in this thesis, regarding both lighting oriented application and light-based sensing application. For general lighting applications, optical design is the core of the development of the system; while for optical sensors, optical design is critical to guarantee the sensitivity and accuracy. The analysis in Chapter 2 and Chapter 3 reveals that silicon-based reflector cavity structure helps enhance the efficiency of light extraction for SSL modules. To optimize the performance of PM sensors, the effect of both structural parameter and material property is investigated in Chapter 4 and Chapter 5. The optimal dimension and material property help achieve high sensitivity of PM sensors.

For many intelligent applications, supporting circuitry enables interactions between the hardware and the surroundings (including people). Therefore, the electrical design should always be taken into account for the system design. In the applications presented in Chapter 3 and Chapter 4, the customized circuitry is integrated with the process of silicon microfabrication and optimized by packaging process.

6.1.2. SILICON MICROFABRICATION PROCESS

This thesis presents a SiP design using silicon as packaging substrate (submount). The fabrication of the silicon substrates is one of the key enabling technologies. In this thesis, the fabrication of the silicon substrates is mainly realized by MEMS process and some customized processes are modified to better suit the need of selected applications in this thesis.

The microfabrication of silicon guarantees accurate dimensions for micro-structure design, which is beneficial for optics related applications. In the lighting module design presented in Chapter 2 and Chapter 3, the reflector cavity structure is proved effective to enhance the light effect. Besides, the MEMS process is batch process, thus intrinsically leading to high uniformity and reproducibility. The 3D structure out of silicon is mainly realized by etching. The silicon etching includes isotropic and anisotropic etch-

ing and both are implemented in the presented SiP design. For instance, cavity structure, fulfilled by anisotropic (wet) etching, is widely used in the presented design and the function includes light reflector, phosphor reservoir, component embedding and vertical interconnections. Anisotropic etching is used to form the micro-fluidic channels in Chapter 4 and Chapter 5. By combining the two types of etching, modified TSV process is developed in Chapter 2 and implemented into SSL module development in Chapter 3. It is proved to be more suitable approach for vertical interconnections in applications with low I/O counts. On the other hand, the micro-machined cavity in silicon submount presents challenge for the fabrication of the SiP module, especially the fabrication of the silicon submounts. When the cavity is used for embedding components, metallization inside the cavity is often needed. As presented in Chapter 2 and Chapter 3, to achieve good quality of metal patterning, photoresist needs to be spray-coated and prolonged exposure and development time is used.

6.1.3. SMART SSL MODULE

A full miniaturization design of a smart LED module is demonstrated in Chapter 3 enabled by proposed 3D SiP approach. Detailed multi-physical analysis is shown with simulation results. The optimization of the module design covers thermal, optical, electrical and structural aspect of the system design. Developed silicon microfabrication process is successfully implemented into the fabrication of silicon submounts of the smart LED module. 3D interconnection and embedded component are fulfilled by means of WLP process. The module prototype is fully characterized and delivers all designed functionality as well as good thermal and optical performance, proving the proposed 3D SiP design promising approach for miniaturization of smart lighting modules.

6.1.4. MINIATURIZATION OF PM SENSOR

The developed SiP design is also implemented into the miniaturization of PM sensors. Light scattering is selected as the operation principle of the PM sensor due to its capability of continuous monitoring, easy maintenance and low power consumption. Light scattering and microfluidics analysis are conducted to optimize the design parameters, including the sensor dimension, the optical property of the sensor material, the control circuitry and so on. In Chapter 4, the complete design of the PM sensor is presented with well tested performance. The miniaturized sensor owns a dimension of $15 \times 10 \times 1$ mm^3 and consumes less than 5 mW of power, while achieves accuracy of less than 5 μg/m^3. To capture information on fine particles, i.e., $PM_{2.5}$, a VI is integrated into the PM sensor, as presented in Chapter 5. The reason for choosing VI as the particle separator

is that compared with other candidate methods, the VI presents least design complexity, requires no additional power consumption, and possesses small form factor. The design of the VI is proved effective for particle size separation. The $PM_{2.5}$ sensor achieves high level of sensing accuracy, less than 3 $\mu g/m^3$, while maintaining the same compact size and low power consumption. The silicon-based SiP design is very suitable for integrated smart sensor applications.

6.2. OUTLOOK

SiP has great potential of integrating multiple components into a single compact package, which meets the need of "More-than-Moore" trend: function enrichment of highly integrated systems. The attempt made in this thesis is expected to provide better understanding towards the SiP technology and its potential implementation in intelligent applications. To make this promising technology prosperous in wider range of applications, constant input is always in need.

For large volume production, cost is always a driver for technology evolvement. To build the intelligent world, a massive net of intelligent devices are needed. Enabled by novel material and process development, more cost economical solutions are created to meet the fast growing need of smart devices. Within semiconductor industry, aforementioned technologies such as WLP and SiP have been serving the goal of reducing cost. Besides, emerging low cost technologies are also seeking opportunities to play their role. For instance, 3D printing technology, also known as additive manufacturing (AM), has already shown its great potential in many applications [1–3]. There is no reason that this technology should not benefit the microelectronics industry. Some attempts have already been made to bridge a traditional industry with the rising technology [4–6]. Using same low cost materials, injection molding technology, which has been used for encapsulant in the field of packaging for years [7, 8], can also contribute in new ways. For example, with the development of metallization-on-polymer technology, polymer-based packaging substrate can be made by molding [9, 10].

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SUMMARY

As we enter era of "intelligence", an increasing number of smart devices are being equipped around us. Such devices reflect the emerging need in microelectronics industry: increased functionality and miniaturization. As Moore's law gradually meets its bottleneck, the concept of "More-than-Moore" (MtM) is proposed to address this issue by migrating board level system assembly to package level system integration. System in package (SiP) technology emerges as a promising solution for increasing the level of integration. Together with other novel packaging technologies, such as wafer level packaging (WLP), SiP shows great potential for providing intensely integrated functional system with miniaturized form factor. This thesis aims to develop novel SiP design and implement it into intelligent applications such as solid state lighting (SSL) and particulate matter (PM) sensor.

The proposed SiP design in this thesis is enabled by multi-physical analysis. Applications such as SSL and sensor packaging often involve integration of heterogeneous components. To address all the interactions among the system components, multi-physical analysis assisted design is intensively presented in this thesis. Finite element analysis is employed for thermal, optical as well as microfluidic analysis. The implementation of the proposed SiP design into specific applications is realized by silicon-based microfabrication and WLP. Dedicated fabrication processes are developed in this thesis for SSL application and PM sensor. Each application is prototyped by the SiP design and characterized by systematic testing and analyzing.

Chapter 2 focuses on the development of a silicon-based packaging design for SSL applications. For SSL applications, multi-physics analysis is enabling step for the development. Besides optical consideration, thermal management is of great significance as well. In Chapter 2, simulation assisted thermal analysis is conducted on two key elements of SSL packages: phosphor and integrated IC. Silicon has higher thermal conductivity than most of the materials that are normally used as packaging substrate, such as ceramic and polymer-based printed circuit board (PCB). The analysis in Chapter 2 reveals that for SSL modules, silicon substrate can greatly ease the thermal issue due to fast spread of heat both vertically and laterally and help reduce the temperature of the LEDs whose performance and lifetime are highly linked with the temperature. When

integrated circuits (ICs) are integrated with LEDs on the same silicon substrate, silicon cannot stop the heat transfer between the LEDs and the ICs. If the thermal impact on the ICs is not acceptable, additional thermal barrier structure can be designed to block the heat from hitting the ICs. Optical analysis is performed on a multi-chip LED module to evaluate the light effect of the silicon submount. The analysis shows the cavity reflector with reflective aluminum coating improves the efficiency of light extraction. Several key processes development and optimization are also presented in Chapter 2. Metallization in cavity, commonly used in silicon -based packaging process, needs special treatment to obtain high quality of fabrication. Another key enabling design is the interconnection within the integrated system. Conventional TSV does not always fit the need of heterogeneous integration. More robust and cost effective approach is presented in Chapter 2. As important parts of an electronic system, passive devices cost comparable area with ICs. Different designs for embedding passive devices into silicon submount are demonstrated at the end of Chapter 2. In Chapter 3, a dedicated 3D SiP design is demonstrated for a smart LED module application. Detailed multi-physical analysis is presented covering thermal management, optical analysis, and circuit and interconnection design. Full process flow is shown in Chapter 3 for the fabrication of silicon substrates, as well as the packaging and assembly of the module. The 3D design of this module is realized by stacking two silicon submounts, each of which is integrated with circuit components. The fabrication of the submounts is an implementation of the processes explained in Chapter 2. The prototyped module is tested from multiple aspects, including functional validation, thermal and optical test. According to the testing results, the 3D SiP module delivers all designed function and shows good thermal and optical performance. The proposed 3D SiP design is proved as a suitable solution for smart SSL applications.

With the increasing public awareness of the impact of PM on human health, real-time monitoring of PM exposure level has attracted more interest than ever before. In Chapter 4, a miniaturization design of PM sensor is presented. The operation principle of the sensor is light scattering, an indirect way of measuring PM concentration. Optical analysis is conducted towards enhancing the sensitivity of the sensor. Both simulation and experiment are carried out to optimize the dimension and the surface material property. The silicon-based SiP is also employed in the design of the PM sensor and is realized by silicon microfabrication and WLP. The micromachining of the silicon submount enables the miniaturization of the PM sensor. The realized sensor has a compact size of $15 \times 10 \times 1$ mm^3, enabling easy integration into portable and wearable electronics. The light source in the sensor consumes the power of less than 5 mW and the total power consumption is still low enough to make it suitable for battery-powered devices.

The sensor is tested under multiple testing conditions, including in-lab chamber test and field real-time test. All the testing results show that the sensor displays a high accuracy of less than 5 $\mu g/m^3$ and prompt response (within seconds) to particle concentration changes. The light scattering is proved to be an effective method for PM concentration measurement and suitable for miniaturization of PM sensor together with the 3D SiP approach.

As more and more researches show that finer particles (diameter of 2.5 µm and below) pose more risk on human health, an increasing need for monitoring fine particles has emerged. Chapter 5, based on the miniaturized PM sensor developed in Chapter 4, presents a design for miniaturized $PM_{2.5}$ sensor. A virtual impactor (VI) is integrated at the air inlet as particle size selector. By applying required air flow rate, the VI can filter out particles larger than 2.5 µm while transport smaller particles into the sensing micro-chamber. The dimension of the VI is optimized by theoretical analysis and finite element analysis. The sensor is also realized by silicon microfabrication and moreover, the adding of VI does not increase the complexity of the whole fabrication process. As the PM sensor presented in Chapter 4, the $PM_{2.5}$ sensor maintains the same compact size. Improved silicon bonding process is demonstrated in Chapter 5 and proved to improve the sensitivity of the sensor. In both Chapter 4 and Chapter 5, polynomial regression analysis is carried out for calibrating the data from the sensor with the reference. Such analysis proves to be a simple yet effective algorism for calibrating our sensor. The $PM_{2.5}$ sensor shows an accuracy of 2.55 $\mu g/m^3$. Recommendations are also given for further cost reduction and thus potential industrialization at the end of Chapter 5.

Chapter 6 summarizes the main conclusions achieved in this thesis and gives an outlook for future work.

SAMENVATTING

Nu we het tijdperk van “intteligentie” binnentreden, zien we steeds meer intelligente apparaten om ons heen verschijnen. Zulke apparaten reflecteren de nood die leeft in de industrie van micro electronica: toenemende functionaliteit en miniturizatie. Nu de wet van Moore steeds meer word bedreigd word het concept “More-than-Moore” (MtM) geintroduceerd om de problemen die komen bij het migreren van board level system assembly naar package level system intergration op te lossen. System in package (SiP) technologie blijkt een verassende en veelbelovende oplossing voor het toenemede niveau van intergratie. Samen met andere zogenaamde “novel packaging” technologiën zoals “wafer level packaging” (WLP), toont Sip groot potentiaal voor het faciliteren van intensief geintergreerde functionele systemen met geminiaturizeerde vorm factor. Deze thesis richt zich op het ontwikkelen van een niew SiP ontwerp en het implementeren ervan in intelligente toepassingen zoals “solid state lighting” (SSL) en “particulate matter” (PM) sensoren.

Het geopperde ontwerp voor SiP in deze thesis wordt mogelijk gemaakt door een multi-fysische analyse. Toepassingen zoals SSL en sensor verpakking vereisen vaak intergratie van hetrogene componenten. Om alle interacties tussen onderdelen te adresseren wordt de multi-fysische analyse uitvoerig gepresenteerd in deze thesis. Finite element analyse wordt toegepast voor zowel termische, optische en microfluidische analyses. De implimentatie van het voorgestelde SiP ontwerp in specifieke toepassingen wordt gerealizerd met op silicium gebaseerde microfabricatie en WLP. Toegewijde fabricageprocessen worden ontwikkeld in deze thesis voor de SSL en PM sensor. Elke toepassing word getest aan de hand van het SiP ontwerp en gekarakteriseerd door systematische testen en analyses.

Hoofdstuk 2 legt de focus op de ontwikkeling van een op silicium gebaseerd verpakkings ontwerp voor SSL toepassingen. Voor SSL toepassingen staan multi-fysische analyses de ontwikkeling toe. Naast optische in acht neming wordt ook thermisch management als erg belangrijk geacht. In hoofdstuk 2 wordt tevens een thermische analyse uitgevoerd die wordt ondersteund door een simulatie. De simulatie wordt uitgevoerd op de twee belangerijkste elementen van SSL verpakkingen, namelijk fosfor en geintergreerde IC. Silicium heeft een hogere thermische geleidingscappaciteit dan de meeste

materialen die normaliter worden gebruikt als verpakkings substaat, zoals keramiek en op polymeer gebaseerde printplaten (PCB). De analyse in hoofdstuk 2 onthult dat voor SSL modules, silicium substaat met gemak het thermisch probleem can verlichten dat ontstaat door het snelle verspreiden van hitte zowel vertical als lateraal. Hierdoor wordt het reduceren van de temperatuur van de LED's eenvoudig gemaakt waar dat erg belangrijk is aangezien de prestaties en levensduur van een LED sterk van de temperatuur af hangt. Wanneer geintergreerde circuits (ICs) worden geintergreerd met LED's op hetzelfde silicium substaat kan silicium de hitteoverdracht niet voorkomen tussen de LED's en de ICs. Als de termische impact op de ICs als niet acceptabel wordt ervaren, kan een eventueel additionele thermische barriere worden ontworpen om de ICs van deze warmte af te schermen. Een optische analyse is uitgevoerd op een multi-chip LED module om het verlichtings effect van het silicium submount te evalueren. De analyse laat zien dat de cavity reflector met een reflecterende coating van aluminium de efficientie van licht extractie verbeterd. Verscheidende kern processen, ontwikkelingen en optimalisaties worden tevens gepresenteerd in hoofdstuk 2. "Metallization in cavity", regelmatig toegepast in silicium gebaseerde verpakkings processen, heeft een speciale behandeling nodig om een hoge fabricagekwaliteit te bereiken. Een ander belangrijk aspect dat het ontwerp mogelijk maakt is de interconnectie binnen het geintergreerde systeem. Conventionele TSV voldoen niet altijd aan de benodigdheden van hetrogene intergratie. Een meer robuust en kosten effectieve aanpak wordt geprestenteerd in Hoofdstuk 2. Als belangrijke onderdelen van een elektronisch systeem, kosten passieve apparaten vergelijkbare hoeveelheden ruimte met ICs. Verschillende ontwerpen voor het inleggen van passieve apparaten in een silicium submount worden geprestenteerd aan het einde van hoofdstuk 2.

In hoofdstuk 3 wordt een toegewijd 3D SiP ontwerp gedemonstreerd voor de toepassing van een slimme LED module. Tevens wordt een gedetailleerde multi-fysische analyse met betrekking tot termisch management, optische analyse, circuit en "interconnection design" gepresenteerd. Een uitvoerige process flow wordt gepresenteerd voor de fabricatie van silicium substaten en de verpakking en assemblage van de module. Het 3D ontwerp van de module wordt gerealizeerd door twee silicium submounts op elkaar te plaatsen, waarvan elke is geintergreerd met circuit componenten. De fabricage van de submounts is een implimentatie van het process dat in hoofdstuk 2 aan bod is gekomen. Het prototype module wordt getest op verschillende aspecten als een fuctionele validatie, een thermische en een optische test. Volgens de resultaten voldoet de 3D SiP module en laat een goed resultaat zien voor zowel de thermische als optische prestaties. Het voorgestelde 3D SiP ontwerp heeft zich als geschikte oplossing voor slimme

SSL applicaties bewezen.

Met toenemend publieke bewustijn van de impact van PM op de menselijke gezondheid, wekt het real-time meten van PM blootstelling steeds meer interesse. In hoofdstuk 4 wordt een miniatuur ontwerp van een PM sensor gepresenteerd. Deze werkt op het principe van het verstrooien van licht, wat een indirecte manier is om de concentratie van PM te kunnen meten. Een optische analyse is uitgevoerd om de sensitiviteit van de sensor te verbeteren. Zowel een simulatie als een expiriment zijn uitgevoerd om de dimensies en de eigenschappen van het oppervlaktemateriaal te optimalizeren. De op silicium gebaseerde SiP wordt ook op het onterwerp van de PM sensor toegepast en wordt gerealiseerd door silicium microfabricatie en WLP. Het verkleinen van de silicium submount stelt het verkleinen van de PM sensor in staat. De sensor heeft hiermee een compacte grootte van $15 \times 10 \times 1$ mm^3, wat het intergreren van deze sensor in zogenaamde "wearables" versimpeld. De licht bron van de sensor verbruikt slechts 5 mW en het totale verbruik van e sensor is nog steeds laag genoeg voor de toepassing met een batterij. De sensor is getest onder meerdere condities waaronder een test in een laboratorium als een veldtest. De resultaten tonen dat de sensor accuraat is tot 5 µg/m^3 met een zeer snelle reactie op veranderende concentraties in de omgeving (enkele seconden). De verstrooiing van licht heeft bewezen een effectieve methode te zijn om de concentratie van PM te meten en is tevens geschikt om geminiaturiseerd te worden samen met de 3D SiP benadering.

Naarmate meer en meer onderzoek laat zien dat kleinere deeltjes (diameter van 2.5 µm en lager) een risico meebrengen voor de menselijke gezondheid, wordt de nood om deze deeltjes te meten van alsmaar groter belang. Hoofdstuk 5, gebaseerd op de miniaturisatie van van de PM sensor uit hoofdstuk 4, bevat een ontwerp voor een geminiaturiseerde PM2.5 sensor. Een zogenaamde "virtual impactor" (VI) wordt geinstalleerd bij de luchtinlaat waar het deeltjes op grootte zal filteren. Door het toepassen van een vereist luchtdebiet, kan de VI filter deeltjes groter dan 2.5 µm filteren terwijl het deeltjes kleiner dan dat door kan laten naar de meetkamer. De dimensies van de VI zijn geoptimaliseerd aan de hand van een theoretische analyse en finite element analyse. De sensor wordt tevens gerealiseerd door silicium microfabricatie en daarnaast compliceert het toevoegen van de VI het fabricageprocess niet. Net als de PM sensor zoals gepresenteerd in hoofdstuk 4, zal de $PM_{2.5}$ sensor zijn compacte grootte behouden. Het verbeteren van het silicium bindings process is gedemonstreerd in hoofdstuk 5 en heeft bewezen de sensitiviteit van de sensor te verbeteren. Voor zowel hoofdstuk 4 als hoofdstuk 5, is een zogenaamde "polynomial regression" analyse uitgevoerd voor het kalibreren van de data met de referentie. Deze analyse toont zich als een simpele doch effectief algorisme

voor het kalibreren van de sensor. De $PM_{2.5}$ sensor heeft een nauwkeurigheid van 2.55 $\mu g/m^3$. Verdere aanbevelingen met betrekking tot het reduceren van de kosten en dus het versimpelen van potentiele industrializatie worden aan het einde van hoofdstuk 5 voorgedragen.

Hoofdstuk 6 bevat een samenvatting van de conclusies bereikt met deze thesis en werpt een blik op toekomstige ontwikkelingen.

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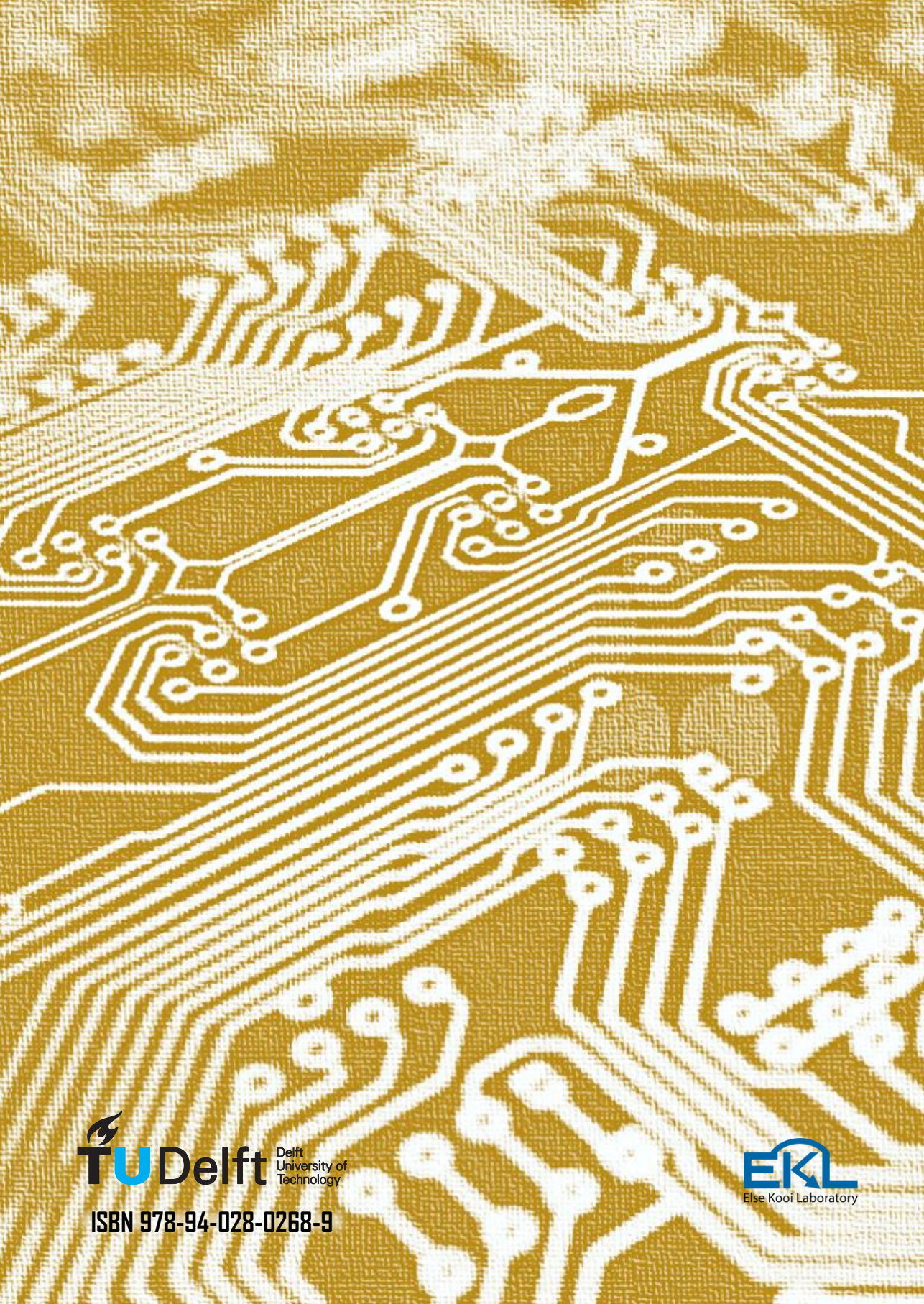

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