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Fanout of 2 Triangle Shape Spin Wave Logic Gates

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Having multi-output logic gates saves much energy because the same structure can be used to feed multiple inputs of next stage gates simultaneously. This paper proposes novel triangle shape fanout of 2 spin wave Majority and XOR gates; the Majority gate is achieved by phase detection, whereas the XOR gate is achieved by threshold detection. The proposed logic gates are validated by means of micromagnetic simulations. Furthermore, the energy and delay are estimated for the proposed structures and compared with the state-of-the-art spin wave, and 16 nm and 7 nm CMOS logic gates. The results demonstrate that the proposed structures provide energy reduction of 25%-50% in comparison to the other 2-output spin-wave devices while having the same delay, and energy reduction of 43x-0.8x when compared to the 16 nm and 7 nm CMOS counterparts while having delay overhead of 11x-40x.

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I. INTRODUCTION

The information technology revolution caused rapid increase of the amount of raw data, together with the requirements of efficient computing platforms for their processing[1]. CMOS downscaling has been efficient to meet these requirements[2]; however, CMOS downscaling becomes very difficult due to different walls: (i) leakage wall[3], (ii) reliability wall[4], and (iii) cost wall[3,4], which implies that Moore's law will come to the end soon. Hence, different technologies have been explored recently, e.g., graphene devices[5], memristors[6], and spintronics[2]. One of the spintronics technologies is Spin Wave (SW) technology, which stands apart as one of the most promising technologies because[2,7–9]: (i) It consumes ultra-low power because SW computing is based on wave interference without the need for charge movement. (ii) It has an acceptable delay determined by the group velocity of the spin wave. (iii) It is highly scalable because the SW wavelength can reach down to the nanometer range at rf-frequencies. Hence, the design of spin wave based logic gates is of great interest.

Given the potentially low energy consumption of the SW based computing paradigm, a large number of different SW logic gate structures have been presented[10–21]. The first experimental work using SW amplitude detection is considered to be a Mach-Zehnder interferometer based NOT gate[21], while XNOR, NAND, NOT, and NOR gates based on a Mach-Zehnder interferometer were also suggested[10,11]. Furthermore, transmission line based NOT, OR, and AND gates were presented[14151617], and parallel voltage controlled re-configurable nano-channels based XNOR and NAND gates were discussed[12]. Bent waveguides and transmission lines were utilized to design (N)AND, (N)OR, XOR, Majority Gates[13,18]. In addition, it was suggested that a (N)OR gate can be built with a crossbar structure[19]. However, the previous works' gates don't provide more than one output, which is a crucial gate feature for an efficient utilization of SW based technology to build larger circuits. Moreover, if the spin wave logic gate output is taken as input for multiple following logic gates in a circuit, then the logic gate must be replicated multiple times which gives significant energy overhead. While the previously mentioned proposals don't provide more than one output, it has been suggested in[22,23] that by adding one arm and making use of one extra transducer, a fanout of 2 is achieved. However, this proposal requires an extra cell to excite spin waves and thus again results in energy overhead. Furthermore, the spin waves must be excited at different energy levels which might add energy overhead and complexity to the gate design. In short,

the aforementioned designs will add relatively large energy overhead and complexity to the designs in order to achieve the fanout of 2.

The aforementioned limitations are solved in this paper and a Fanout of 2 (FO2) triangle shape 3-input Majority gate and a 2-input XOR gate are proposed. The fanout is enabled without the need for an extra transducer and all spin waves are excited at the same energy level resulting in a relatively large energy saves. The main contributions of this work are:

- Developing and designing FO2 logic gates: FO2 3-input Majority gate is proposed. Also, it is possible to make use of this structure to implement 2-input (N)AND, and (N)OR gates by making one of the inputs as control input and the other two as data inputs. Moreover, 2-input X(N)OR structure is proposed by removing the third input.

- Validating the proposed logic gates functionality: MuMax3 software is used to validate the logic gates structures.

- Demonstrating the superiority: The proposed logic gates are evaluated and compared with the state-of-the-art SW, and 16 nm and 7 nm CMOS logic gates. The results demonstrate that the proposed logic gates save energy of 25%-50% in comparison with the state-of-the-art SW logic gates while having the same delay. In addition, the proposed SW logic gates provide energy reduction of 43x-0.8x when compared to the 16 nm and 7 nm CMOS counterparts while having delay overhead of 11x-40x.

The rest of the paper is organized as follows. Section II gives the basics and the fundamentals of the spin wave based technologies and the spin wave computing paradigm. The next Section III explains the proposed fanout of 2 Majority and XOR gates. Section IV provides the simulation setup, results and performance evaluation of the proposed gates, in addition to the discussion about variability, and thermal noise effects. Finally, the paper is concluded in Section V.

II. SW TECHNOLOGY BACKGROUND

This section provides the basic spin-wave theory and spin-wave based computation paradigm.

A. Spin Wave Fundamentals

Magnetic materials can be utilized for memory or computing aims by making use of the magnetization state. For instance, spintronic memory device are based on the magnetization orientation which can take two stable states representing either logic 0 or 1. It is also possible to exploit the dynamical behavior of the magnetization. This magnetization dynamics is expressed by equation 1 which is known as the Landau-Lifshitz-Gilbert (LLG) equation[2425]:

$$\frac{d\vec{M}}{dt} = -|\gamma|\mu_0 \left(\vec{M} \times \vec{H}_{eff}\right) + \frac{\alpha}{M_s}\left(\vec{M} \times \frac{d\vec{M}}{dt}\right), \tag{1}$$

where γ is the gyromagnetic ratio, α the damping factor, $\vec{M}$ the magnetization, M_s the saturation magnetization, and $\vec{H}_{eff}$ the effective field which is equal to the summation of the external field, the exchange field, the demagnetizing field, and the magneto-crystalline field.

For weak perturbations, equation 1 can be linearised and has wave-like solutions. These solutions are known as spin waves and can be seen as collective excitations of the magnetization. As indicated in Figure 1, SWs are characterized by a wavelength λ, a wave number k ($k = 2\pi/\lambda$), a phase ϕ, an amplitude A, and a frequency f. The wavelength and frequency respectively characterise the spin precession period in space and in time. The relation between f and k is the dispersion relation of the wave and is crucial for the design of any spin wave device[26].

Different spin wave types exist; each with its own features. The direction of wave propagation with respect to the direction of the static magnetization determines which SW type is excited[27]. These waves are formed when the static magnetization orientation is out-of-plane and results in isotropic spin wave propagation in the plane. Note that this is not the case for the other spin wave types. Therefore, FVSW are promising for circuit design as the same propagation behavior in different directions is required inside the circuit[27]. While this holds true for many SW based circuit design but some logic elements make use of the non-reciprocity and the anisotropy (non-reciprocity is strongly sought in the acoustic waveguide domain, the spin wave multiplexer makes use of the spin wave anisotropy).

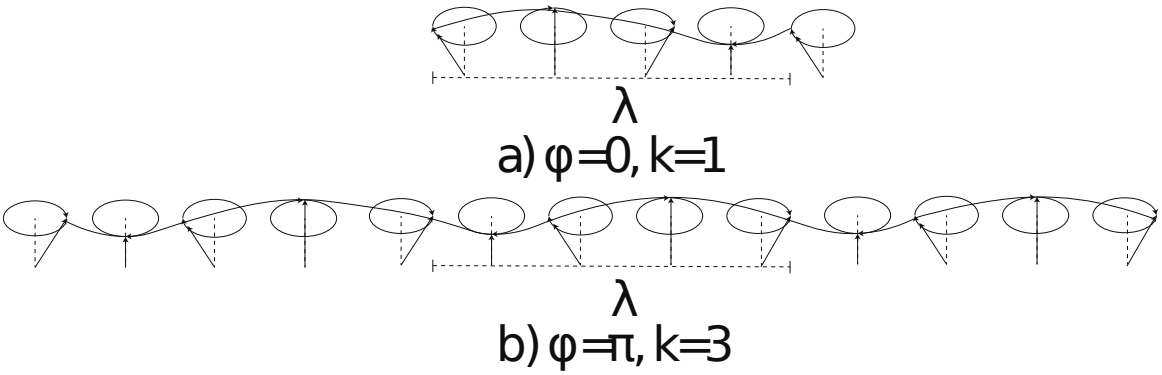

FIG. 1. Spin Wave Parameters.

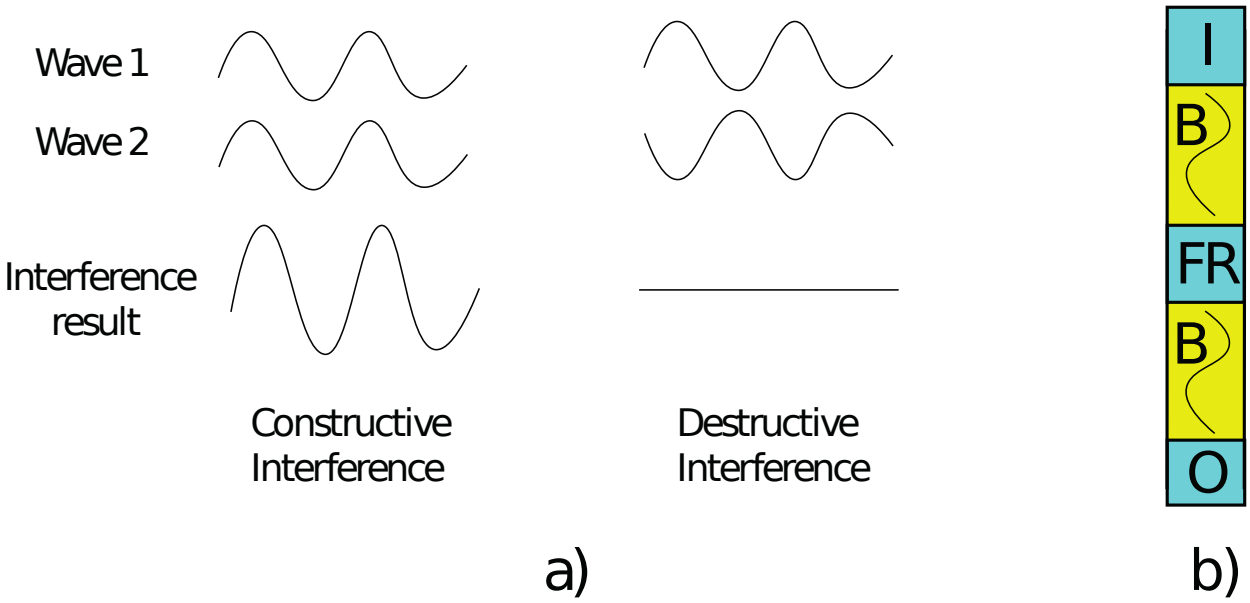

FIG. 2. a) Spin Wave Device, b) Constructive and Destructive Interference.

B. Spin Wave Computing Paradigm

As any other waves, also SWs interfere with each other. This fundamental phenomenon can be utilized for direct logic function evaluations without requiring the traditional Boolean algebra formalism[7]. Generally speaking, after their generation, multiple SWs coexist and interact in various ways, depending on their amplitude, wavelength, phase, and frequency within the same waveguide[7]. The simplest case, but with the highest practical relevance due to its natural support for majority function evaluation, occurs when SWs with the same amplitude, wavelength, and frequency are interacting[7]. For example, if two such SWs interfere, the resulting SW amplitude is dependent on the phase difference: SWs with the

same phase interfere constructively and SWs with different phases interfere destructively, i.e., no output SW is generated, as indicated in Figure 2a. It is clear that if SWs carry digital information this can be processed by means of those interference patterns. For example, the interference of an odd number equal amplitude and wavelength SWs having phases of 0 or π results in a majority function evaluation. Note that the Full Adder (a fundamental processor design building block) carry out is computed as a 3-input majority and most of the error detection and correction schemes rely on n-input majorities[7].

Conceptually speaking, a SW device includes 4 stages: SW creation, propagation, processing, and detection. In the first stage, spin waves are excited in the localised excitation region and then they propagate through the waveguide. When traveling through the waveguide the SW can be manipulated or exposed to different factors within the so-called Functional Region and finally a detector is required to produce the output value[7,28,29]. A generic SW device is presented in Figure 2b.

III. FO2 SW LOGIC GATES

In the following lines, the proposed triangle shape fanout of 2 Majority and XOR gates are described.

A. Proposed FO2 SW Majority Gate

We developed a novel triangle shape fanout of 2 (FO2) 3-input Majority gate (MAJ3) structure, illustrated in Figure 9. The device consists of 3 inputs I_1, I_2, and I_3 corresponding to the excitation cells and 2 outputs O_1 and O_2 corresponding to the detection cells. Depending on the used method, excitation and detection cells can be voltage encoded or current encoded cells. Many existing options can be used for the excitation and detection cells, e.g., microstrip antennas[7,28,30], magnetoelectric cells[7,31–33], spin orbit torques[7,34,35]. In contrast to the ladder shape structure[22], the proposed triangle shape structure doesn't need the replication of one of its inputs to enable fanout capability and thus is more energy efficient as will be demonstrated in the performance evaluation subsection (Subsection IV D).

To simplify the interference pattern, the width of the waveguide must be equal or less than wavelength λ. All SWs are excited with the same amplitude and frequency to obtain

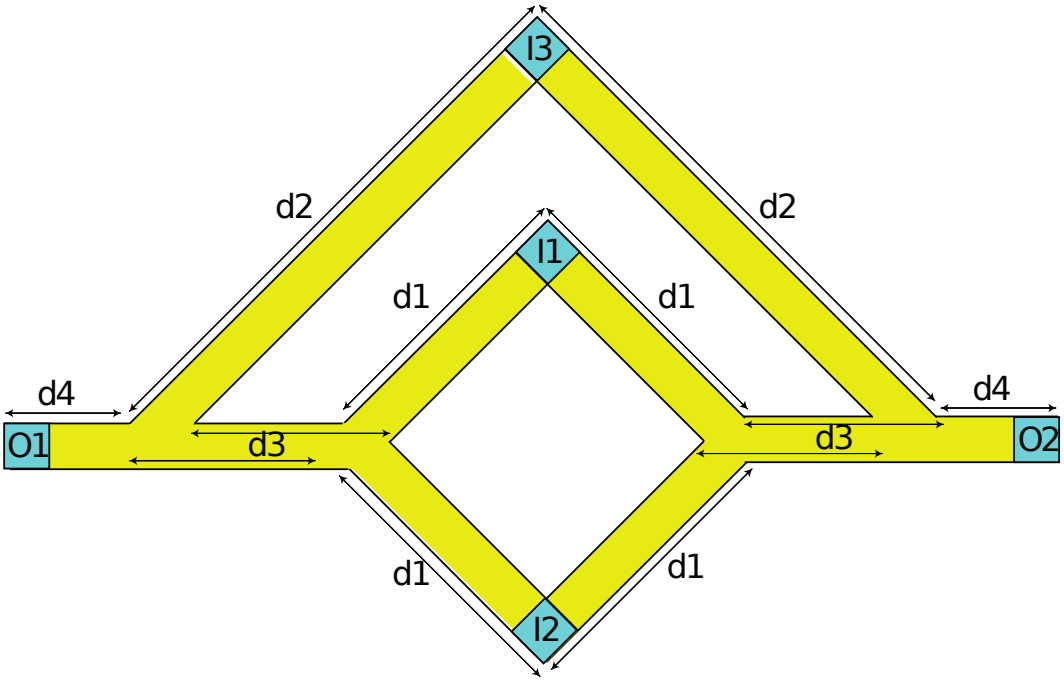

FIG. 3. Fan-out of 2 MAJ3 Gate.

the desired pattern at the interference point. The proposed structure is generic and its dimensions are indicated in Figure 3. The structure dimensions must be chosen accurately to provide the desired functionality. For example, if the desired interference is to constructively interfere if the SWs have the same phase and destructively interfere when SWs are out of phase, then dimensions d_1, d_2 and d_3 must be nλ (where n=0,1,2,3,...). Whereas if the opposite behaviour is desired, such that the SWs interfere destructively when they have the same phase and constructively interfere when they are out of phase, then the dimensions d_1, d_2 and d_3 must be (n+1/2)λ.

The logic gate provides a fan-out of 2 because of the structure symmetry. The outputs O_1 and O_2 must be captured at the same distance (d_4) from the last interference point. Furthermore, this distance must be chosen precisely such that if the desired output has to give logic inversion then d_4 must be (n+1/2)λ, whereas if the desired results has to give the non-inverted output then d_4 must be nλ.

The proposed gate operates as follows: (i) At I_1, I_2, and I_3, SWs are excited with the suitable phase (0 for logic 0 and phase π for logic 1). (ii) The excited SWs at I_1 and I_2 propagate diagonally until reaching the crossing points where they interfere with each other constructively or destructively depending on their phases. (iii) The resulting SWs propagate

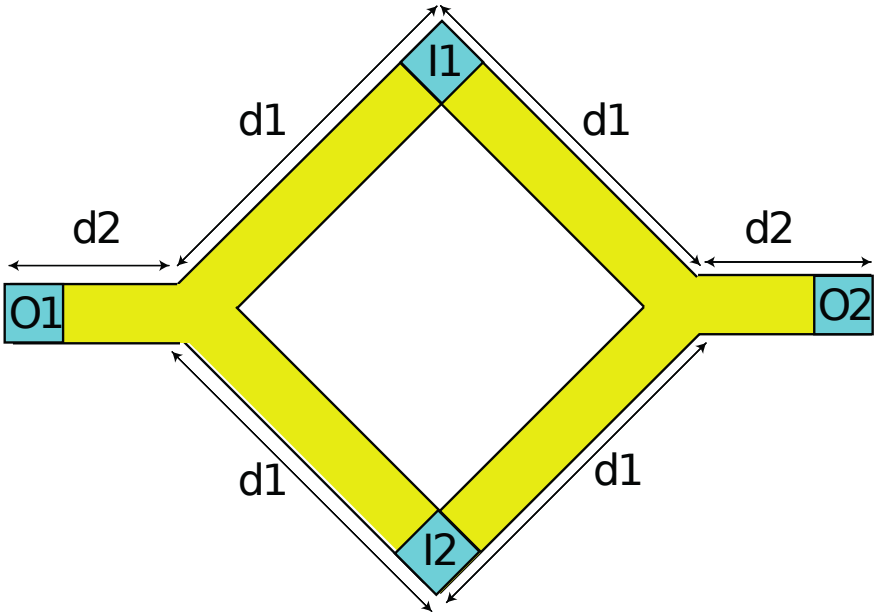

FIG. 4. Fan-out of 2 XOR Gate.

to interfere constructively or destructively at both interfering points with the SW excited at I_3. (iv) Once the resulted SWs reach the outputs O_1 and O_2, they are interpreted by means of phase detection. Depending on a predefined phase, phase detection is performed as follows: a 0 SW phase corresponds to a logic 0 and a phase of π to logic 1. Because of the symmetry and the SWs' isotropic propagation through this structure, the two SWs reaching O_1 and O_2 are identical, which means that a fanout of 2 is achieved.

Furthermore, the proposed structure can be utilized to implement (N)AND and (N)OR gates of I_1 and I_2 if I_3 is fixed to logic 0 for (N)AND gate and logic 1 for the (N)OR gate realization.

Moreover, we note that, if only one MAJ3 gate is required the structure can be simplified by removing one of its sides either the right or left one. Also, the gate fan-out capabilities can be extended beyond 2 by using directional couplers[36] to split the spin wave into multiple arms and using repeaters[37] to regenerate a strong SW in the different waveguides. Additionally, more inputs can be added below I_2 or above I_1 and I_3.

B. Proposed FO2 SW XOR Gate

It is interesting to note that the triangle structure is versatile and becomes an XOR gate by removing the third input as depicted in Figure 4. While the operation principle and the

design stpdf are the same as in the previous case, threshold-based detection must be utilized to obtain the XOR functionality. The threshold detection is based on a predefined threshold such that if the received SW magnetization is larger than the predefined threshold, this is logic 0, and logic 1 otherwise. If the XNOR is desired, the condition can be flipped such that if the received SW magnetization is larger than the predefined threshold, this is logic 1, and logic 0 otherwise.

The same design stpdf hold true for the XOR gate except for the output detection because it depends on threshold detection and thus the SW amplitude is the important one in this case. Therefore, the output must be detected as close as possible from the last interference point and thus d_2 must be as small as possible to capture stronger spin wave.

IV. SIMULATION SETUP AND RESULTS

This section provides the simulation setup, simulation results as well as performance evaluation and discussion about the variability and thermal noise impact.

A. Simulation Setup

We validated the structure by means of MuMax3[38] simulations using a 50 nm wide $Fe_{60}Co_{20}B_{20}$ waveguide with thickness of 1 nm. The spin wave wavelength is chosen to be 55 nm which is larger than the waveguide width and therefore results in clear interference patterns. Once the wavelength is determined, the dimensions of the device in Figure 3 can be calculated and become d_1=330 nm, d_2=880 nm, d_3=220 nm, and d_4=55 nm. Likewise, the dimensions of the device in Figure 3 can be determined to be d_1=330 nm, and d_2=40 nm. Moreover, from the SW dispersion relation and for $k=2\pi/\lambda$=50 rad/μm, a SW frequency of 10 GHz was determined. In addition, the following parameters are used: magnetic saturation M_s=1100 kA/m, exchange stiffness A_{ex}=18.5 pJ/m, damping constant α=0.004, and perpendicular anisotropy constant k_{ani}= 0.832 MJ/m^3[39].

B. Performed Simulations

Two main experiments are performed: (i) FO2 Majority gate implementation, and (ii) FO2 X(N)OR implementation.

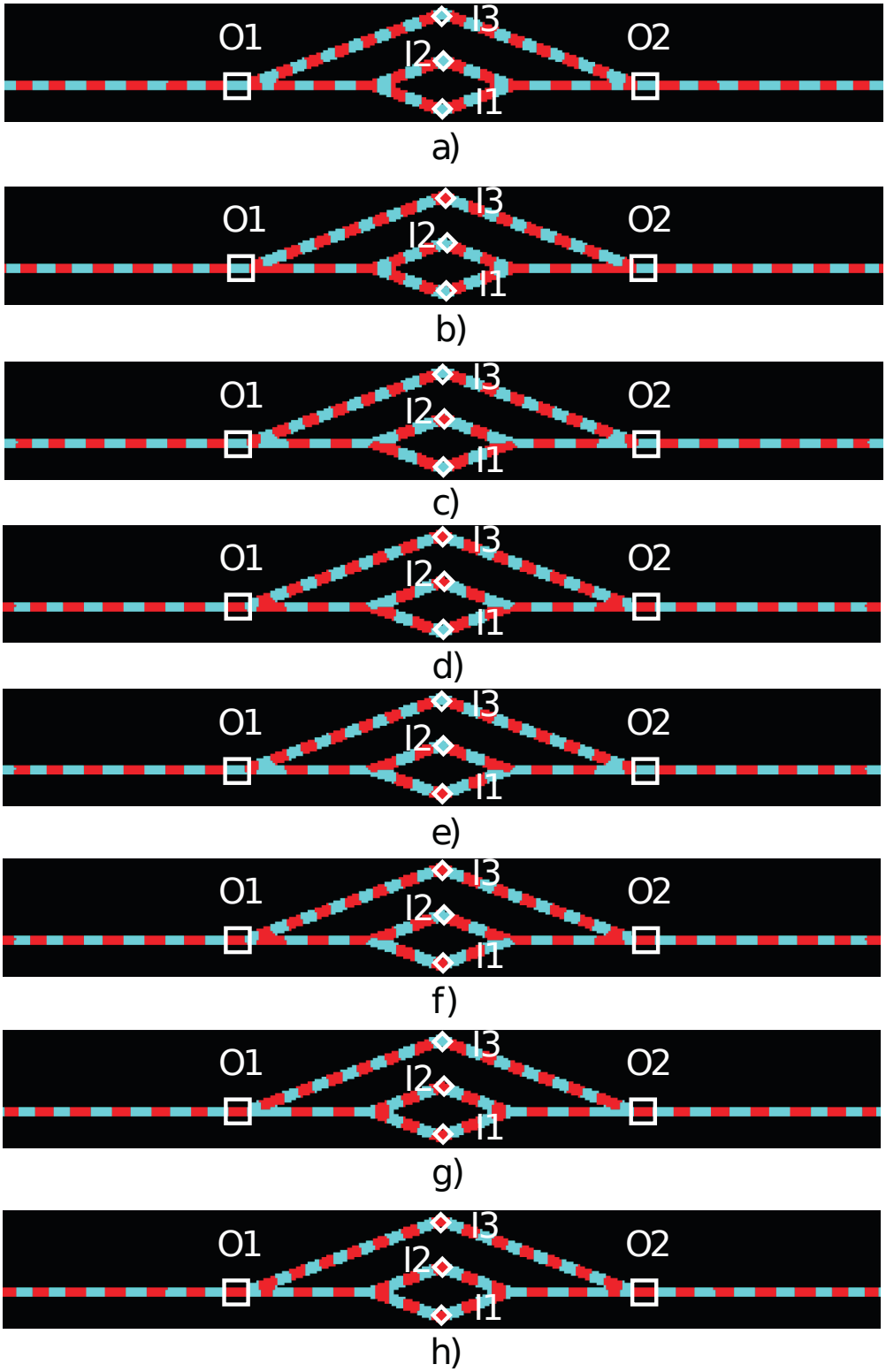

FIG. 5. Fan-in of 3 Fanout of 2 Majority Gate MuMax3 Simulation.

TABLE I. Fan-in of 3 Fanout of 2 Majority Gate Normalized Output Magnetization.

Cases			O_1	O_2
I_3	I_2	I_1		
0	0	0	1	1
0	0	1	0.083	0.084
0	1	0	0.16	0.16
0	1	1	0.164	0.164
1	0	0	0.164	0.164
1	0	1	0.16	0.16
1	1	0	0.083	0.084
1	1	1	1	1

TABLE II. Fan-in of 2 Fanout of 2 XOR Gate Normalized Output Magnetization.

Cases		O_1	O_2
I_2	I_1		
0	0	0.99	1
0	1	≈ 0	≈ 0
1	0	≈ 0	≈ 0
1	1	1	1

- 3-input FO2 Majority gate implementation: The three inputs I_1, I_2 and I_3 are used to generate spin waves that propagate through the waveguide. The interference results are captured at O_1 and O_2 based on phase detection.

- 2-input FO2 X(N)OR implementation: here two inputs I_1 and I_2 are used instead of three as in the previous case. Threshold detection is utilized to capture the output.

C. Simulation results

3-input FO2 Majority gate implementation based on phase detection

Figure 5 a to h present the MuMax3 simulation results for the 3-input 2-output Majority gate for $\{I_1,I_2,I_3\}$=$\{0,0,0\}$, $\{0,0,0\}$,$\{0,0,1\}$,$\{0,1,0\}$, $\{0,1,1\}$, $\{1,0,0\}$, $\{1,0,1\}$, $\{1,1,0\}$, and $\{1,1,1\}$, respectively, where blue represents logic 0 and red logic 1. This clearly indicates the correct functionality of the FO2 MAJ3 gate. O_1 and O_2 provide logic 0 for the input patterns $\{I_1,I_2,I_3\}$=$\{0,0,0\}$,$\{0,0,1\}$,$\{0,1,0\}$, and $\{1,0,0\}$, whereas they provide logic 1 for the input combinations $\{I_1,I_2,I_3\}$=$\{0,1,1\}$,$\{1,0,1\}$,$\{1,1,0\}$, and $\{1,1,1\}$.

To demonstrate the equivalence of the two outputs, i.e. FO2 achievement, we extracted the output SWs energy from MuMax3 simulations for all possible input patterns. The normalized magnetization values at O_1 and O_2 are presented in Table I. From this table, it is seen that the outputs are the same for all cases, which implies that a fanout of 2 has been successfully achieved.

2-input FO2 X(N)OR implementation based on threshold detection

Table II presents the triangle shaped XOR gate normalized magnetization values at the outputs O_1 and O_2 and for different input combinations $\{I_1,I_2\}$ = $\{00,01,10,11\}$.

As it is clear from Table II, an XOR or XNOR logic gate can be implemented if a suitable threshold is chosen to detect logic 0 and logic 1 at the outputs. The appropriate threshold in this case is 0.5 because for $\{I_1,I_2\}$ being $\{0,0\}$ and $\{1,1\}$ magnetization are approximately 1 while they are approximately 0 when the inputs are $\{0,1\}$ and $\{1,0\}$. By applying the aforementioned principle to obtain XOR on the data in Table II, the outputs O_1 and O_2 are logic 0 at $\{I_1,I_2\}$=$\{0,0\}$ and $\{1,1\}$ because their amplitude is larger than 0.5 and they (O_1 and O_2) are logic 1 at $\{I_1,I_2\}$=$\{0,1\}$ and $\{1,0\}$ because their magnetization are less than 0.5. As stated previously, the XNOR can be captured by flipping the condition. Thus, both FO2 XOR and FO2 XNOR can be captured from the proposed structure.

D. Performance Evaluation and Discussion

In this Subsection, we evaluate the energy of the proposed logic gates and discuss the variability and thermal effect.

Performance Evaluation

The proposed 2-input FO2 XOR and 3-input FO2 Majority gates are evaluated in terms of energy and delay and compared with the state-of-the-art spin wave[22,23], 16 nm CMOS[40], and 7 nm CMOS[41]. To evaluate the performance and to make fair comparison with[23], the following assumptions are made: (i) ME cells are used to excite and detect SWs. (ii) The energy consumption and delay of the ME cells are 34.4 nW and 0.42 ns, respectively[42]. (iii) SWs propagation delay in the waveguide is neglected. (iv) SWs propagation loss can be neglected in comparison with the loss in the transducers. (v) The output is passed directly to be used by another SW gate. (vi) Pulse signals are used to excite SWs with pulse duration 100 ps. Note that the energy consumption in[23] are re-evaluated based on 100 ps pulse signal excitation in order to make a fair comparison. Due to the early stage development of SW technology, these assumptions might be optimistic and they might need re-evaluation in the near future.

Furthermore, it was assumed that a 3-input CMOS Majority gate is built from 4 NAND gates[40,41]. In addition, the energy and delay were estimated with respect to the provided numbers in[40,41] for the XOR and MAJ gates calculations.

Table III presents the evaluation results. As it can be observed from the Table, the proposed Majority gate is 13x and 20x slower than the 16 nm, and 7 nm CMOS counterparts, respectively, but provides 11x, and 1.6x energy consumption reductions in comparison with 16 nm, and 7 nm CMOS counterparts, respectively. Also, the proposed XOR gate saves 43x, and 0.8x energy in comparison with 16 nm, and 7 nm CMOS counterparts, respectively, and is 13x, and 40x slower than 16 nm, and 7 nm CMOS XOR gate. Also, note that SW gates use less number of devices than CMOS which means small real estate chip area. To conclude, SW might lose at the end against CMOS, but the economical benefits will determine which one will win especially that SW technology still is immature technology. Note that assessment and evaluation of complex circuits which were designed using SW

TABLE III. Performance Comparison.

Designs	CMOS[40,41]				SW[23]		This work	
Technology	16nm CMOS		7nm CMOS		SW		SW	
Implemented function	MAJ	XOR	MAJ	XOR	MAJ	XOR	MAJ	XOR
Used cell No.	16	8	16	8	6	6	5	4
Delay (ns)	0.03	0.03	0.02	0.01	0.4	0.4	0.4	0.4
Energy (aJ)	466	303	16.4	5.4	13.7	13.7	10.3	6.9

technology are available in[42]. For example, the evaluation results in[42] for 32-bit hybrid CMOS-SW divider showed that the area-delay-power product is 800x better than 32-bit 10 CMOS divider. This indicates that although SW technology is slow technology but the power and area improvements is much higher and will compensate the slowness[42]. However, SW technology is still immature technology, and these benchmarks might need re-evaluation in the future.

On the other hand, when comparing with the SW Majority gate[22], the proposed triangle shape Majority structure saves 25% energy while keeping the same delay. Also, the proposed XOR structure saves 50% energy while keeping the same delay when compared with the SW XOR gate in[22,23]. This is because of the fact that extra ME cells are required to enable the fanout capability in[22,23]. We also note that, for proper gate operation in the ladder shape structure[22,23], inputs may have to be excited at different energy levels depending on whether they have a straight path to the outputs or face bent regions at the edges. In contrast, the proposed triangle shape structure doesn't require an extra ME cell to achieve the fanout capability, which saves energy and allows for equal energy inputs excitation. Note that the complexity of fabricating such devices are not clear until now due to the early stage development of spin wave based technology.

Variability and Thermal Effect

Validating the proposed logic gates and proofing the concept are the main targets of this paper. Thus, variability and thermal noise effect were not taken into account. However, waveguide trapezoidal cross section and edge roughness effects were examined in[36]; furthermore, it was presented in[36,43] that the gate functionality is correct in their presence.

Moreover, thermal noise was introduced in micromagnetic simulations of majority gates[36,43]. It was demonstrated that the gates function correctly at different temperatures and the different temperature has only limited impact. Although we expect that the variability and thermal noise will have limited effect on the gate, it will not disturb the gate functionality. We will explore deeply the variability and thermal noise effects on the proposed gates in the near future.

V. CONCLUSIONS

Novel FO2 spin wave Majority and XOR gates were proposed in this paper. It was demonstrated that by using phase detection, a Majority gate is implemented, whereas the XOR is implemented by threshold detection. Also, the proposed logic gates were validated by means of MuMax3 simulations. The proposed logic gates were assessed and compared with the state-of-the-art spin wave, and 16 nm and 7 nm CMOS logic gates. Our evaluation indicated that the proposed logic gates save 25%-50% energy while having the same delay with respect to the state-of-the-art spin wave counterparts. Whereas the result indicated that the proposed logic gates decrease the energy consumption of 43x-0.8x when compared to the 16 nm and 7 nm CMOS counterparts while having delay overhead of 11x-40x.

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