3D Microelectrode Integration in Muscle-on-Chip Device

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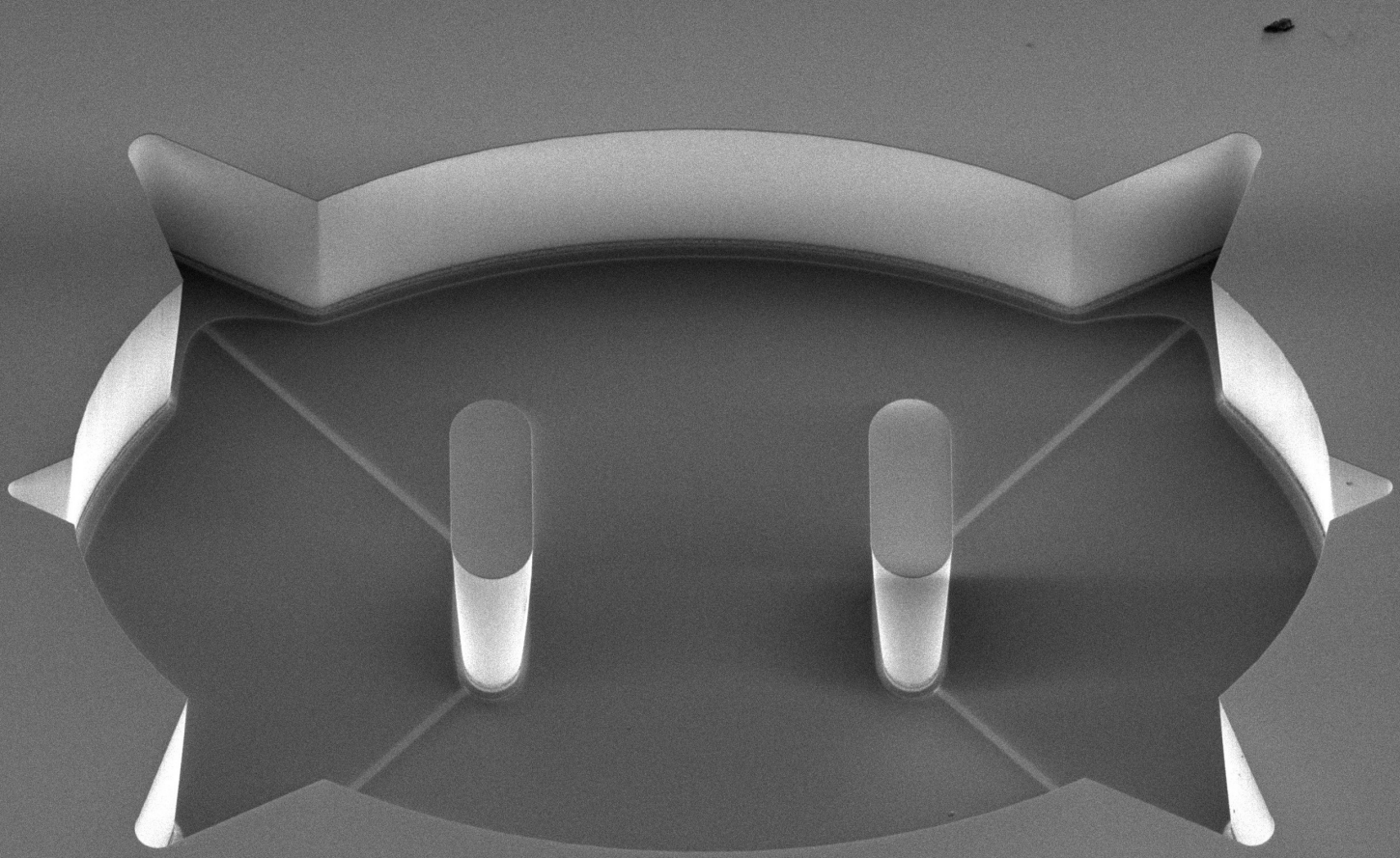

Delft University of Technology

TU Delft

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TU Delft

bi/ond. Nourishing, Stimulating and Monitoring Cells

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I feel extremely lucky to have so many incredible people surrounding me, encouraging me to be the best version of myself. Always there for support and also to enjoy this experience to its fullest. Delft will always have a bit of myself on it and I can't wait to see where we will all end knowing for sure that our paths will cross again.

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Abstract

The current drug development process is a costly effort both in terms of budget and time. Organ-on-Chip (OoC) technologies are rapidly developing and are used for various applications and studies that aim to reduce the costs of this process. They represent the convergence between tissue engineering and microfluidic technology to provide researchers with an *in vitro* tool that can better recreate the environmental conditions in which cells would normally develop *in vivo*. One of the applications of this tool is the implementation of such platforms to study heart and muscle tissue. Electrical stimulation of this tissue is of great importance for these studies. There exist different ways in which these cells can be electrically stimulated such as microelectrode arrays (MEAs) or external electrodes. These methods pose several challenges that need to be addressed.

The scope of this project is to implement 3D microelectrodes into an already existing device from the company Bi/ond to electrically stimulate the cells developing inside. This approach aims to solve the existing challenges in current methods for the electrical stimulation of tissue. This project succeeded in developing such 3D microelectrodes although the functionality of the device could not be proven. However, several approaches were also studied and propositions were made on how to continue with this project.

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Introduction

1.1. The current drug development process

Discovery and development of new drugs is a long and costly process. The average time for a new drug to come out to the market nowadays is around 10-15 years with a budget of between 1-2 billion $[1]. A general overview of the process for the development of a new drug can be seen in Figure 1.1. It can be seen that more than 90% of clinical drug development fails to pass the required thresholds to be implemented and introduced into the market. Even if a drug has been approved, it may be retracted from the market after its approval based on new discoveries on the side effects of such drug.

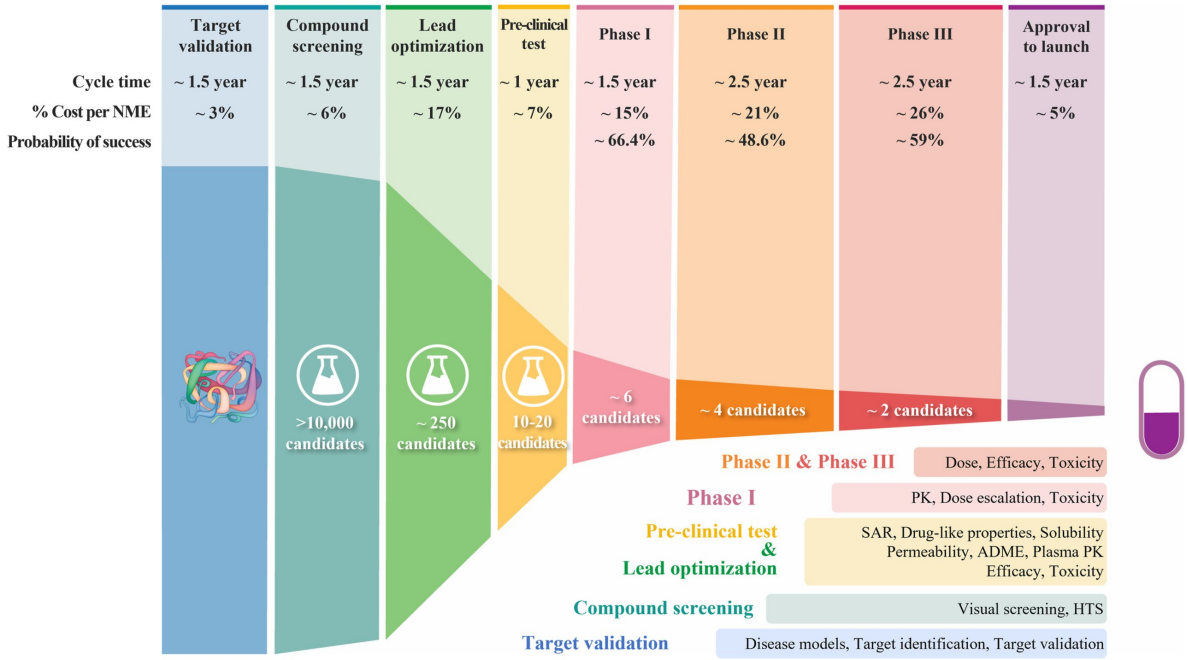


Figure 1.1: Drug development process [1].

Despite the new strategies and procedures adopted by the industry, if this trend is continued, the time and cost for the development of new drugs will only increase over the years [2]. This can be seen in Figure 1.2 where data from past years of how many drugs were put into the market per billion $ is shown. Decreasing both costs and time in this process is of vital importance for both industry and

society, and more and more new ideas are arising to give solutions to this problem.

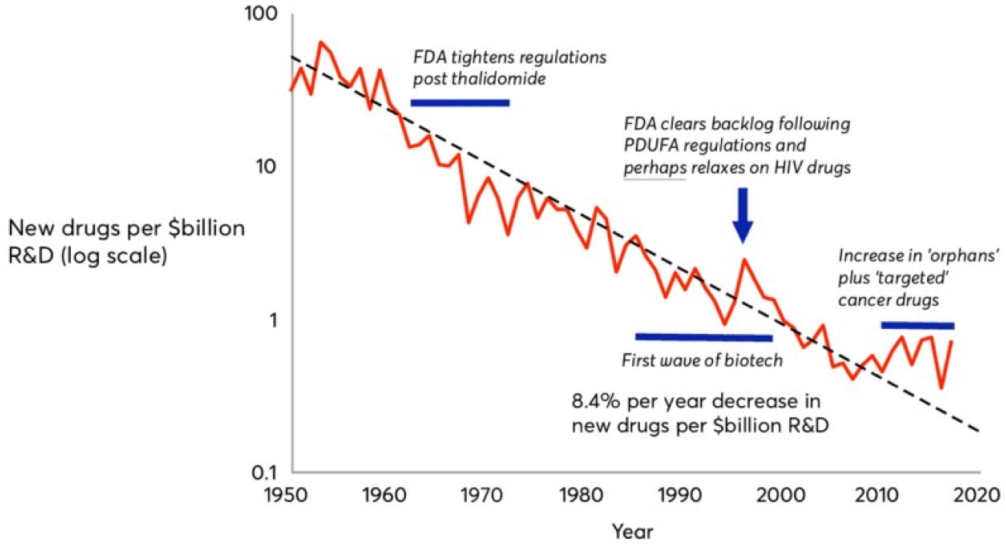


Figure 1.2: Trend of cost of drug development [3].

One of the major bottlenecks of the industry which contributes to the high costs and long times is patient recruitment and retention during clinical trials. Frequently, this results in noteworthy delays in commencing the study and increases expenses for conducting the trial. The intricacy of the protocol is an additional aspect that adds to the prolongation of drug development timelines and amplification of associated expenses [4]. Other factors that affect current drug development processes include the heightened expectations from regulatory agencies, increased safety requirements along with the requirement for conducting a greater number of market-focused, pre-approval studies to ensure a competitive drug label.

All these factors are leading the drug research industry into an unsustainable situation as pharmaceutical companies are not able to keep up with the high demands of both time and costs for the development of new drugs that once approved and put into the market may or may not be as profitable as expected.

1.1.1. Current methods

There are many different methods used in the drug development process to determine whether a certain drug is safe and effective for its intended use. These methods vary depending on what stage a certain drug is in the general timeline of such a process. At early stages of development, the most used method consists of *in vitro* experimentation using cell cultures in Petri dishes or multi-well plates to study the effect of different compounds. *In vitro* experimentation allows the researchers to manipulate specific compounds in well-controlled experiments. It allows them to target specific biochemical cascades and therefore be able to better understand specific variable responses in such an environment. This is done to be able to predict future responses in further studies such as in animal experimentation and ultimately in human clinical trials. *In vitro* studies also allow researchers to tune specific parameters at will which enables them to have a broader view of the responses of cells to certain compounds [5].

Overall, *in vitro* experimentation using Petri dishes present the following advantages [6]:

- Controlled environment: this tool allows researchers to tune different parameters of the environmental conditions of the cells at will such as temperature, pH, nutrient availability and exposure to stimuli.
- Cost-effective: *in vitro* experimentations require less costly investment than *in vivo* experimentation,

specially regarding costs associated to animal care, housing and maintenance.

- Higher throughput: using Petri dishes allows the researchers to scale up the number of experiments that can be done at once thanks to the ease of use of this particular tool. This condition allows to conduct screening of large numbers of compounds quickly and efficiently.
- Reduced animal use: using Petri dishes has reduced the amount of animals used during experimentation, as many compounds are discarded initially from the study because of their ineffectiveness before even testing them *in vivo*.

However, this practice also has some disadvantages [6] [7]:

- Lack of complexity: cell cultures in Petri dishes lack the complexity of full human bodies, thus cells might behave differently *in vitro* compared to *in vivo* even when subjected to the same stimuli at cellular level.
- Limited physiological relevance: the cells in the Petri dish are not exposed to the same physiological conditions as inside the body such as flow, hormones, etc.
- Lack of interaction with other cells: the cells cultured in a Petri dish are isolated and do not have contact with other types of cells. This way the interactions between cells that occur *in vivo* can not be replicated *in vitro*.
- Difficulty in translating results: the results do not always represent what will happen *in vivo* and therefore can result in false positives or false negatives in drug development.
- Inability to model some diseases: certain diseases require dimensional structure (3D) that the 2D approach of the Petri dishes can not provide.

An overview of these advantages and disadvantages can be seen in Table 1.1.

Table 1.1: Advantages and Disadvantages of using *in vitro* Petri dishes testing.

Advantages	**Disadvantages**
• Controlled environment • Cost-effective • Higher throughput • Reduced animal use	• Lack of complexity • Limited physiological relevance • Lack of interaction with other cells • Difficulty in translating results • Inability to model some diseases

All these factors have led the industry to try find alternative ways and methodologies to test the compounds and check their efficacy. An alternative technique that is used nowadays is the implementation of organoids in studies. Organoids are structures that are artificially created through the three-dimensional (3D) culturing of stem cells. These structures consist of various cell types that originate from stem cells or organ progenitors, and they undergo a process of self-organization through cell sorting and lineage commitment that is spatially restricted, similar to the process that occurs *in vivo* [8]. The use of organoids provides a more complex environment than *in vitro* studies with Petri dishes. They also provide different cell types and come from virtually any patient. They can also be used in high-throughput studies [9].

Although organoids present some advantages when compared with *in vitro* 2D cell cultures in Petri dishes, this tool also has some challenges that need to be tackled such as lack of high-fidelity cell types, limited maturation, atypical physiology, lack of arealization and necrotic core for large sizes [10].

Another practice used in drug development is animal testing. It has great advantages over the previously mentioned methods. The main advantage that animal models present is that the whole organism is studied. Interaction between different cell types and the influence of other factors inside the body, such as hormones, can be measured and studied. Nevertheless, current animal testing models present certain problems and challenges [11] [12]. The main concern with this practice is the lack of

resemblance of these animal models to the human body in most cases. Some compounds that work on animal models fail to do so when passed to clinical trials because of the physiological differences between the animals used in these tests and humans [13]. The complexity of such *in vivo* trials and their related costs also increase greatly when compared with *in vitro* testing.

Ethical dilemmas and considerations are also a great burden of this practice [14]. Nowadays, awareness for the well-being of the animals used in experimentation is rising [15]. This leads to even more impediments to the use of animals in research and researchers look for different options.

1.2. Introduction to Organ-on-Chip

To better understand the scope of this project, it is important to first introduce the idea behind Organ-on-Chip (OoC). Organ-on-Chip is a novel technology that is born from the convergence of tissue engineering and microfluidic technology [16]. This convergence allows OoC devices to mimic key aspects of human physiology by controlling cell environment and maintaining tissue-specific functions [17]. This is possible thanks to the implementation of microfluidic channels and chambers that allow certain factors, such as temperature, humidity, or pH [18], to be tuned as desired for the specific purpose of the device. By mimicking the environmental conditions in which cells would normally develop *in vivo*, OoC tries to improve current drug development research as well as reduce animal experimentation thereby used. These microfluidic models aim to resemble the structure and function of human organs so that they can be used as research tools. OoC can be seen as a bridging technology that enables the possibility to work with complex cell structures by optimizing the microenvironment through improved engineering to ensure accurate and meaningful results during research [17].

OoC technology aims to have an influence in the fields of cosmetic, food, and chemical industries in both production and testing. It presents as a plausible alternative to animal testing, eliminating the ethical concerns around the use of animals. This technology was selected as one of the top ten emerging technologies in 2016 [19] [20] and has been growing at a fast rate in funding, interest, publications, and commercial devices over the years. Many companies like Mimetas and start-ups such as Bi/ond are focused on developing this technology even further to create novel devices which will have a great impact on current drug development processes and studies.

It is important to acknowledge that most OoC devices resemble a single organ, although some platforms aim to recreate several organs all in one device [21]. There is a very distinctive difference between single OoCs and multiple OoCs [17]. The main challenge of the latter is to create a culture medium that will both nourish all the different tissues as well as leading to the formation of all desired tissue types. Transportation of such medium inside these multi-OoC devices is also a major challenge [22]. These Multi-OoCs are at the moment individual OoCs devices linked by tubes and microchannels [23]. Their objective is to create realistic *in vitro* models closer to systemic (organismal) complexity of the human body by controlling volume ratios and flow rates [24]. Nevertheless, further research regarding single-organ OoC devices is needed for their final implementation in the drug development process.

1.3. Advantages & disadvantages of OoCs over conventional methods

As a result of all the facts described previously in section 1.1, alternative methods are being studied to overcome the challenges presented by current research methods. OoC aims to help in this process and reduce both cost and time in the drug development process. OoC devices have several advantages over current conventional methods which make them an attractive tool for researchers.

One of the main advantages of using OoC devices is that it enables a similar physiology to the human body for the cells to develop. These devices offer the possibility of creating *in vitro* 3D culture environments in which 3D tissue culture can develop and provide organ-level functions [17].

This leads to a more accurate representation of the environmental conditions in which human cells would develop *in vivo*. The different physiological processes that occur inside a living organism can be mimicked. Therefore, the interactions between the tissue being studied and its surroundings can give the researchers more meaningful data when compared with traditional *in vitro* studies. It can help them better predict the efficacy and performance of the different compounds being tested. One example of this is the study of blood vessels. When using a Petri dish, the cells lay on a flat surface which is a very different setting compared to the real blood vessels which look like a round tube. In OoC devices the researchers can create a round tube in which the blood vessel cells can grow and develop. It also allows the researchers to study different kinds of vessels as by tuning the diameter of the tube, it can resemble arteries, veins and even capillaries [18].

Another main advantage of using OoCs technologies specifically over animal models is the elimination of ethical concerns regarding animal experimentation [25]. If this technology proves to be sufficiently accurate and reliable, it could replace animal testing in the future as a whole [26]. This would be a great advance in drug research as it would eliminate all the costs related to maintenance of the animals being studied which represent a significant amount of the budget spent in the drug development process [18]. There have been serious advancements in this topic which can be seen in how the FDA (U.S. Food and Drugs Administration) has now allowed OoC devices to be sufficient in some cases in the study of new drugs instead of animal testing for the approval of these new drugs [27] [28] [29].

Even though OoCs devices are a great tool for researchers, they also present some disadvantages. The first drawback relates to the presence of surface effects. Given the small volumes of the fluid involved, these surface effects dominate over volume effects. This can potentially result in a lower quality analysis and the potential adsorption of some desired products. Additionally, due to the existence of laminar flow at the intersection of multiple fluids, there may be inadequate mixing of the relevant fluids. Another constraint associated with these platforms is the requirement of special instruments in certain experiments to ensure the reliability of the results [30].

1.4. Materials used in OoC devices

There are many materials used in OoC devices. Materials and structure of these devices vary greatly depending on their purpose. Some OoC devices might need more flexible materials than others, such as the Lung-on-Chip from Emulate [31] in which the lung cells are seeded on top of a flexible membrane so that they are subjected to both tensile and compressive stresses that mimic expansion and contraction of alveoli. Another important feature of the materials used in OoC devices is that if the material is in contact with cells or with a cell culture medium, it needs to be biocompatible to not damage the tissue. In Table 1.2, several materials are listed along with their advantages, drawbacks, and where they are used [17]:

1.5. Heart- & Muscle-on-Chip

OoC devices are being currently used for recreating a wide variety of organs [20]. They span from liver-on-chip [32] to intestine-on-chip [33]. As mentioned earlier, the use of these devices is to recreate the environmental conditions in which the cells would normally develop through an *in vitro* platform. The use of OoCs helps the researchers obtain more accurate results than conventional *in vitro* methods which results in higher quality research and a higher success rate.

These devices are also being used specifically for heart and muscle studies adopting the name of Heart- and Muscle-on-Chip devices. They represent a great asset for the recent breakthroughs and development in this area [34]. This field is of great interest as the leading cause of death in the United States according to the Center for Disease Control and Prevention is cardiovascular diseases [34]. The limited availability of applicable and efficient *in vitro* models has significantly restricted research studies in this area. Cardiovascular toxicity is responsible for the majority of phase I drug failures and the subsequent withdrawal of approved medical products. Nearly half of the drugs introduced in the

Table 1.2: Most common materials used in OoCs, advantages, disadvantages and main purpose.

Material	Advantages	Drawbacks	Experimental model
PDMS	• Gas- permeability • Optical transparency • Elasticity • Biocompatibility	• Absorption of small molecules • Difficulty in mass production	• Disease modelling • Mechanical and chemical stimuli • Electrode patterning
Thermoplastics	• Optical transparency • Mass production • Cost- effectiveness • Low absorption	• Rigidity • Difficulty in producing complex structures • Low gas permeability	• Drug screening • Large- scale experimentation
3D printing resins	• High mechanical and thermal properties • Low cost • Complexity and design freedom	• Autofluorescence • Opacity • Toxicity in some cases • Low permeability • Surface roughness	• 3D design modelling • Rapid prototyping
Glass	• Optical transparency • Inert • Biocompatibility • Low autofluorescence	• Laborious fabrication • Fragile • Expensive	• Electrode patterning
Silicon	• Low absorption • Generation of high-resolution channels on the nanoscale	• Laborious fabrication due to need for clean- room facilities • Expensive for small volumes	• On-chip sensors • Formation of diffusive barriers

pharmacology market since the 1990s have been recalled due to cardiovascular complications [34]. The development of accurate *in vitro* models in the field of cardiac and skeletal muscle cells is therefore of great interest to the scientific community and especially to the pharmacological industry.

1.5.1. Cardiac & Skeletal muscle physiology

The muscle cells inside the body can be divided into three main groups: cardiac, skeletal, and smooth muscle tissue [35]. Each one of them shows different characteristics, physiology, and functions. In this project, we will only focus on cardiac and skeletal muscle tissue. To better understand how heart- and muscle-on-chip devices work, it is important to first comprehend how these tissues are arranged, how they work inside the human body and the related complications that may occur.

About 40% percent of the human body weight is made up of skeletal muscle, which is composed of multiple individual fibers that are bundled together to form a muscle spindle. This arrangement gives the skeletal muscle a striated appearance. Each muscle fiber is made up of predominantly actin and myosin fibers that are enclosed in a cell membrane (sarcolemma), and these fibers are responsible for the contraction and relaxation of the muscle. The contraction in this type of muscle is voluntary [36]. Skeletal muscle wasting is a significant health concern that can result from various factors such as genetic disorders, autoimmune diseases, lack of use due to aging or disability, space travel, sports injury, trauma or tumor removal. If left untreated, these conditions can severely reduce strength and mobility [37].

The myocardium, also known as the cardiac muscle, is a striated muscle that contracts involuntarily and surrounds the chambers of the heart. It is made up of individual cardiomyocytes, which have a similar structure to skeletal muscle and include cytoskeletal and contractile elements that are linked by intercalated discs. These highly adherent complexes permit rapid electrical transmission between cardiac muscle cells, causing them to contract in unison [38] [39]. The initiation of a contraction cycle begins with the depolarization of the cell membrane, triggered by the action potential. This depolarization leads to the entry of calcium into the cardiomyocyte, subsequently activating muscle contraction. Within the cell, a calcium-induced calcium release occurs, resulting in the binding of troponin C to calcium. This interaction causes troponin C to disengage from the actin-binding sites, enabling actin to bind with myosin. The interaction just described is responsible for sarcomere shortening. As the myosin head exerts force, it pulls the actin filaments, ultimately leading to a muscle contraction (Figure 1.3)[40]. This mechanism of contraction is the same in skeletal muscle cells. The main complications related to cardiac muscle cells are: cardiomyopathy, a cardiac dysfunction associated with a disorder

of the myocardium, heart failure, where the myocardium's structural and functional defects lead to a reduction in both the filling of the ventricles and ejection of blood during systole, and myocarditis which is the inflammation of the myocardium often triggered by acute rheumatic fever or viral infections [41].

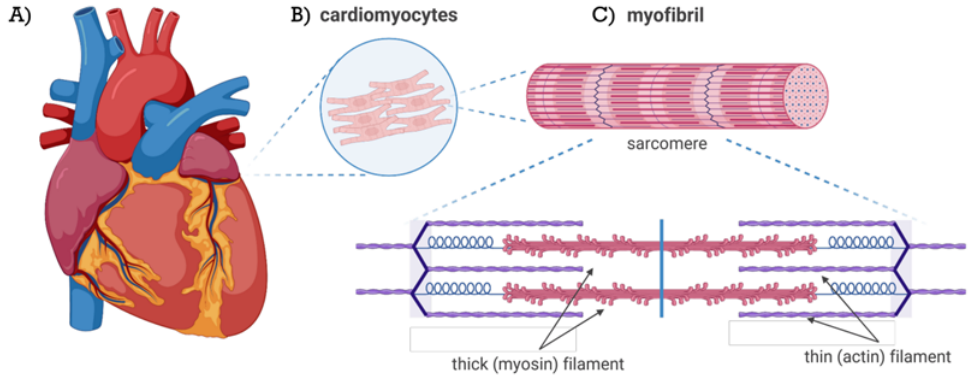


Figure 1.3: Human heart anatomy a) Macroscopic structure of the heart; b) Detailed view of a cardiomyocyte; c) Individual myofibril structure within a muscle fiber; s) Magnified representation of a sarcomere structure, comprising thick and thin filaments responsible for generating contraction forces. [40].

The most important feature of these two types of cells when deciding how to design a device is how they are structured inside the human body. They present a very similar structure in which individual fibers group together to form the muscle tissue. This arrangement is used by the researchers to create both Heart- and Muscle-on-chip devices.

1.5.2. Electrode-electrolyte & electrode-cell interaction

As mentioned earlier, the contraction of the muscle cells starts with the depolarization of the cell membrane. This depolarization occurs when the cell detects a change in potential in its surroundings which triggers cell response in the form of muscular contraction. This change in potential in the surrounding of the cell can be replicated with the use of electrodes which mimic this change of potential in the surroundings of the cell. By applying an electric field, we can stimulate the cells thus inducing muscular contraction. For this to occur, both the electrode-electrolyte and electrode-cell interaction are of great importance. They need to be understood and taken into account. Such interactions have been studied extensively in literature [42][43][44].

One of the major facts that needs to be considered is that in metals and semiconductors, the charge is carried by electrons and holes. However, in the electrolyte, the charge is carried by ions. This means that the main event occurring at the interface between the electrode and the electrolyte is a transduction of charge transport from electrons to ions. Because of this transduction, the electrode-electrolyte interface exhibits two main mechanisms of charge transfer. The first mechanism is a non-Faradaic reaction, where there is no transfer of electrons between the electrode and the electrolyte. Non-Faradaic reactions involve electrode polarization and the redistribution of charged species within the electrolyte. On the other hand, the second mechanism is a Faradaic reaction, which involves the transfer of electrons from the electrode to the electrolyte. This results in the reduction or oxidation of the chemical species within the electrolyte [42].

Regarding the non-Faradaic reactions, they can be modeled as a simple electric capacitor which in this case is called the double layer capacitor (C_{dl}). This phenomenon occurs because of three main reasons. The first one relates to the charge redistribution that occurs as metal ions in the electrolyte combine with the electrode. This results in a plane of charge at the surface and an opposing plane of charge, as counterions, in the electrolyte. The second reason is attributed to certain chemical species present in the electrolyte that selectively adsorb onto the solid electrode, creating a charge separation effect. An example of this are halide anions. Lastly, the third reason is because of the

existence of polar molecules like water in the electrolyte that may exhibit a preferential orientation at the interface, leading to a net separation of charge due to the collective alignment of these polar molecules [42].

Faradaic reactions occur when a charge is injected from the electrode to the electrolyte, leading to reduction and oxidation processes. These redox reactions modify the characteristics of the electrolyte changing its properties in terms of pH and ion concentration. The model of such phenomena can be represented as a resistor. When making the model and equivalent electrical circuit of the Electrode-electrolyte interaction, the resistance of the electrolyte itself needs to also be taken into account. The model that best resembles this behavior is the Randles cell which is depicted in Figure 1.4 where R_2 represents the resistance of the electrolyte, C_1 corresponds to the double layer capacitance and the R_1 corresponds to the Faradaic reactions. The main difference between these two mechanisms of reactions is that the non-Faradaic reactions are reversible. This means that the effects it produces can be reversed and the original state can be restated. In the case of the Faradaic reactions, they are irreversible which means that the original state can not be achieved after this reaction. One main drawback of the Faradaic reactions is that as current is injected into the electrolyte, the electrolyte itself undergoes irreversible processes such as hydrolysis. These reactions have a big impact on the condition and characteristics of the electrolyte in terms of its pH and can be detrimental to the cells developing in it. This is why for this project's scope, it is important to keep these mechanisms in mind when applying certain stimulation to the system.

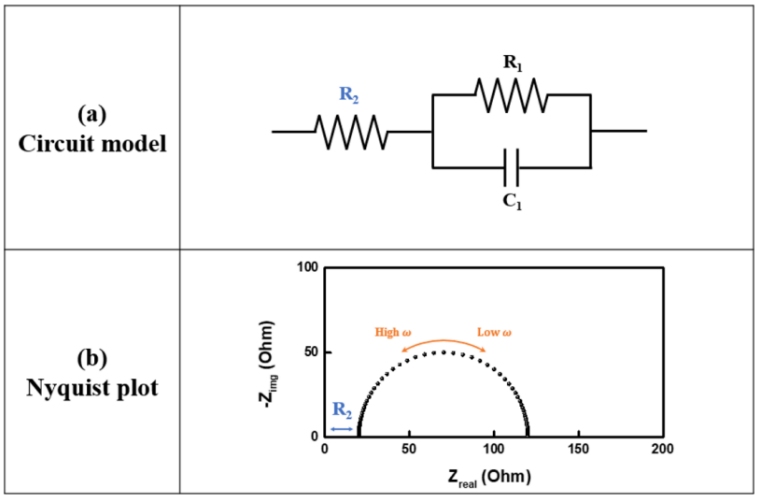


Figure 1.4: a) Equivalent circuit and b) Nyquist plot of a simplified Randles cell [45].

Regarding the electrode-cell interaction, the main concern regards the necessary input that the electrodes need to provide for the cells to be stimulated. As previously mentioned, muscle cells react to changes in the potential in their surroundings, specifically at the membrane of the cells. Therefore, as only stimulation is needed, the electrodes must only be polarized to achieve this objective. This means that there is no need to inject current into the electrolyte for the stimulation of the muscle cells and therefore the only reactions of interest for the scope of this project are the non-Faradaic reactions.

1.5.3. State of the Art

Some research groups have already been working with Muscle-on-Chip and Heart-on-Chip devices. There are, however, differences in how they approached the design of the devices as well as how they measured different parameters and characteristics of the cells.

One group of researchers aimed to make contractility assays using muscular thin film (MTF) technology [46]. MTFs refer to engineered mono-layers of muscle cells grown on an elastic film. They have been utilized to assess various muscle types' contractile characteristics, such as systolic and diastolic stresses. In their work, they show how the MTF assay which was originally created for heart-on-chip [47] can also be adapted to smooth muscle. Their main approach to asses the contractility of the muscle cells is as follows:

An MTF is created with muscle cells only on one of the sides of the elastic film. This MTF is attached to a glass surface only from one end of its structure. This disposition makes the MTF bend upwards when the cells are contracting. If the device is looked at from the top using a microscope, a change in the length of the MTF can be seen. Several images were taken at different time points. The images capturing MTFs in a flat position on the glass were employed for determining the film length (L). Meanwhile, images or videos depicting bent MTFs were utilized to compute the length of the film projection on the horizontal plane (x). The radius of curvature (r) of the films was numerically calculated at each time point using equation 1.1.

$$x = \begin{cases} rsin(\frac{L}{r}) & \in \frac{2L}{\pi} < x < L \\ r & \in \frac{L}{2\pi} < x < \frac{2L}{\pi} \end{cases} \tag{1.1}$$

They use both image processing software, such as ImageJ, and MatLab to process the recordings of the cells when contracting. In Figure 1.5, a representation of how they implemented this idea with the addition of some microfluidic channels is depicted. For the stimulation of the cells, they used some external electrodes that need to be implemented into the system thanks to the assembly of some inlets and outlets as can be seen in Figure 1.5(a).

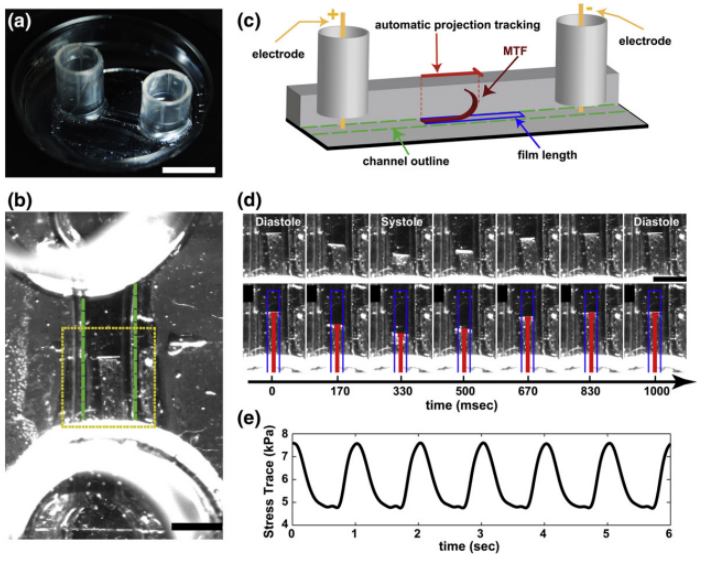


Figure 1.5: Device employing MTFs (a) Image of the top view of a fluidic channel, with a scale bar of 10 mm; (b) Image of a fully assembled microfluidic device featuring the thin film inside, with the channel highlighted in green and a scale bar of 2 mm; (c) Schematic representation of the microfluidic channel with the embedded MTF; (d) Top row—time-lapse images illustrating the bending of the thin film during a complete cycle (area outlined in yellow in (b)); bottom row—time-lapse images displaying the bending film with the x-projection marked in red, and the film length denoted in blue; (e) An illustrative output of contraction stress data for the film over time (paced at 1 Hz). [46].

In this approach, the muscle cells are grown on an MTF to measure the contractility of the cells. Because of the use of MTFs, the cells are grown in a monolayer on top of an elastic thin film which already gives the researchers a more multi-cellular pharmacological response when comparing it with standard contractility assays on most lab-on-a-chip devices which are based on single cells within microfluidic channels [48]. Regarding the stimulation of the muscle cells, external electrodes are used in the whole device to excite the muscle cells for their contraction.

There is another type of technology used in this field which is called Biowire. This technology has been adopted by some research groups for the maturation of cardiomyocytes from human embryonic and induced pluripotent stem cells (hESC and hiPSC, respectively). This technology is based on a wire structure within the device. A well is created to facilitate the maturation and development of the cells. Across this well, a trench is placed to provide a mold for cell differentiation. This wire allows the cells to be aligned and grow into adult cardiomyocytes [49]. Notably, researchers were able to incorporate electrical stimulation during the maturation process through external electrodes that were implemented afterwards.

Other groups of researchers have opted for a different device design. The implementation of two pillars that serve as an anchor for the muscle cells is one of the most used designs in heart-on-chip and muscle-on-chip devices. The main idea behind this design is that the pillars serve as anchoring for the muscle cells to attach. They also induce uniaxial alignment of the cells. This in return makes the muscle cells grow in what is called a muscle bundle around the pillars [18] [37] [34]. This structure can be seen in Figure 1.6. This muscle bundle is then able to contract spontaneously (heart tissue) or when stimulated (skeletal muscle), and this contraction is transferred onto the pillars. The main materials used in the formation of these pillars are polymers and one of the most used polymers is polydimethylsiloxane (PDMS). PDMS has many advantages. It is a flexible transparent biocompatible material used often in the biomedical field and microfluidic technology [50]. Due to its flexibility, some research groups use this deflection of the pillars as a measurement to calculate contractility of the muscle bundle around the pillars using optical tools [34] [51].

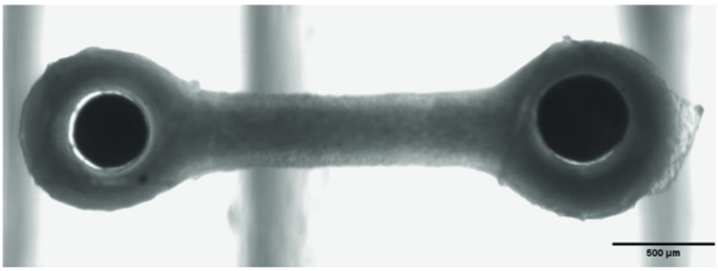
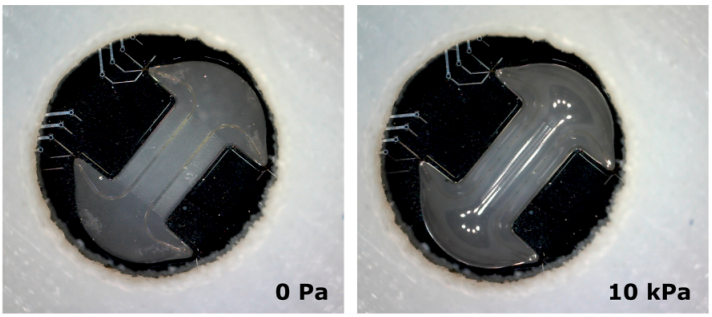


Figure 1.6: Top view of 3D heart tissue made from human stem cells, that has formed around two elastic micro-pillars (top side has black colour) [18].

The stimulation in this approach is usually similar to the one previously mentioned. The most common technique for electrical stimulation involves using a pair of external electrodes to establish a consistent electrical field between them. However, when applying stimulation to a large group of cells, the resolution of the resulting electrical field may be compromised. This is mainly due to the distance between the microelectrodes and the cells which need to be excited. To overcome this limitation, different approaches can be followed. One of them is to use microelectrode arrays (MEAs) capable of generating localized electrical fields to stimulate each individual cardiomyocyte [34] necessary for certain applications such as when trying to stimulate specific regions of the muscle bundle to see how the contraction propagates through the tissue. Another approach used by some researchers is the addition of two platinum parallel wires at the sides of the chamber to induce the electric field [51].

One significant device in terms of fabrication processes is the Cytostretch [52], which played a pivotal role in introducing Silicon-based fabrication techniques in OoC devices. In the fabrication of this device, Si is employed as a mold into which PDMS is poured to create a PDMS membrane, utilizing a technique known as soft lithography. This device demonstrated the compatibility of Silicon-based fabrication methods with OoC devices, paving the way for diverse applications and advancements in

various fields. The Cytostretch offers several advantages, including low-cost manufacturing on a larger scale. The PDMS layer can be manipulated and tuned for the desired characteristics so that it would promote certain cell differentiation and also provide mechanical stimuli to the cells. This can be seen with an example in Figure 1.7 where the PDMS membrane is stretched when subjected to some air pressure on one of its sides. Additionally, this device incorporates MEAs for monitoring and stimulating the cells within the platform.



(a) (b)

Figure 1.7: (a) Cytostretch device with the embedded MEA module in its relaxed state. (b) The Cytostretch device undergoing inflation through the application of an air pressure of 10 kPa on the membrane's posterior side [52].

The work of Milica Dostanic at TUDelft showcases the integration of various technologies in a miniature sensorized platform designed for engineered heart tissue [40]. Her research encompasses significant aspects, including the device's structure, incorporation of electrodes and sensors, and utilization of a two-pillar approach for structural support during cell maturation. Milica used the same fabrication techniques as the ones used during the development of the Cytostretch. To prevent cell detachment, modifications were made to the overall geometry of the pillars, while the platform itself was reduced in size, resulting in a decreased number of cells within the device. Her work highlights the implementation of electrodes that enter the well where the cells are seeded, providing electrical stimulation to the system. Additionally, she integrated force sensors in the form of capacitive sensors. These sensors were able to measure changes in capacitance resulting from the tilting and deformation of the pillars at their base during cell contraction. Figure 1.8 shows the top view of such a device with the microelectrodes inside the well around the pillars where tissue maturation occurs.

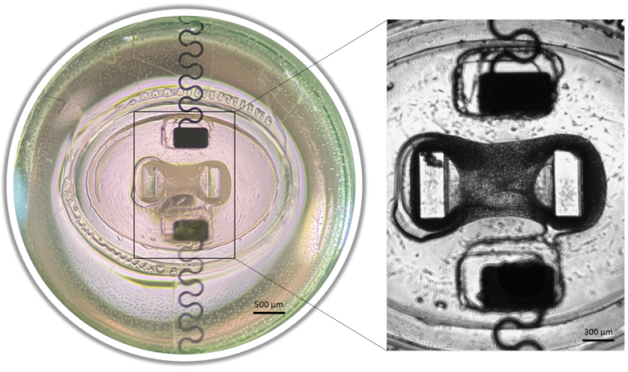


Figure 1.8: Cultivation of engineered heart tissue (EHT) on the platform incorporating integrated pacing microelectrodes [40].

The company Bi/ond has developed a novel muscle-on-chip device called the MUSbit. One key difference between Bi/ond's muscle-on-chip device compared to others is that the pillars inside the well are not made out of a polymer but are made of silicon (Si). A schematic of its structure can be seen in Figure 1.9. This can be done as Bi/ond uses integrated circuit (IC) microfabrication techniques to create and manufacture their device. Bi/ond has developed this idea even further and has implemented some electrodes into their device for the recording and stimulation of the tissue being grown inside the well. They call this new device the Let-it-bit and it can be seen in Figure1.10 where the electrodes come

in proximity to the tissue from outside the well.

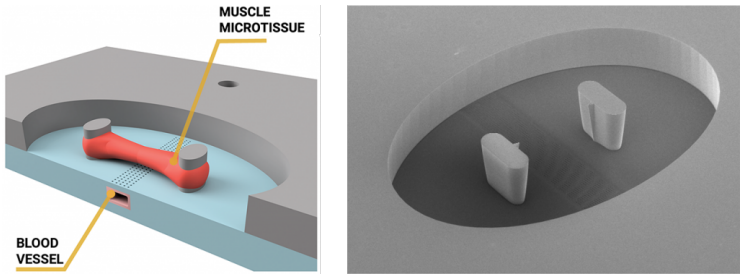


Figure 1.9: MUSbit device from Bi/ond [53].

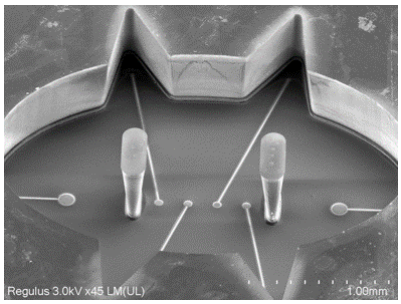


Figure 1.10: Let-it-bit prototype from Bi/ond [54].

Another research group has recently made a new approach in terms of microelectrode implementation inside muscle and heart-on-chip devices. In their approach, they make use of conductive hydrogel pillars. They then connect these pillars to gold (Au) electrodes on the bottom glass substrate of their device [51]. They use these Au electrodes for the recording of the signals produced by the cardiomyocytes when they are stimulated. The schematic of the structure of the device can be seen in Figure 1.11.

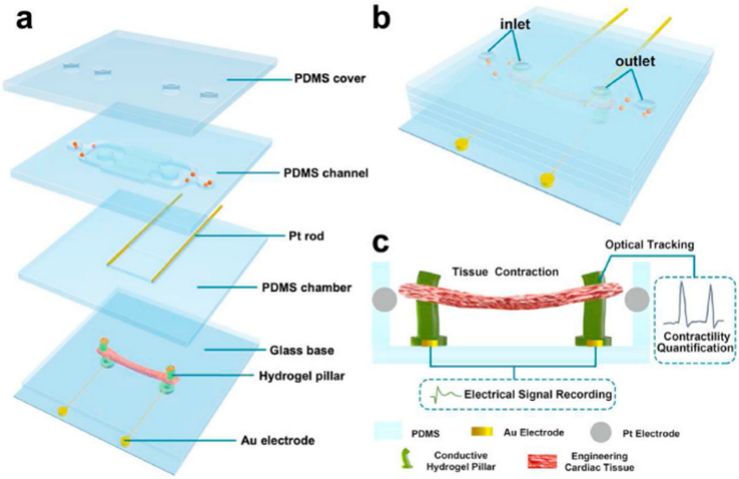


Figure 1.11: Art-on-chip configuration and features. (a) Diagram illustrating the chip device, encompassing inlet/outlet ports, microchannel, PDMS culture chamber, Pt rods, and glass base integrated with Au and conductive hydrogel pillar electrodes. (b) Three-dimensional representation of the heart-on-a-chip device. (c) Side view schematic depicting the cardiac tissue, hydrogel pillar electrodes, and culture chambers (not to scale) [51].

Overview

In most cases, the electrical stimulation of the muscle cells in OoC devices is done via external electrodes that are inserted into the device after fabrication. Recent developments have made it possible to implement these electrodes into the chips themselves which gets rid of the need for external

electrodes. However, these electrodes implemented in the devices for stimulation are far away from the cells themselves [34]. This leads to the need to input higher voltage and energy to the system so that this change in potential can be sensed by the muscle cells across the electrolyte cultured media for their stimulation. The use of higher voltage and energy values can be detrimental to the cells themselves but also to the electrolyte in which it is transmitted [42]. Only in one of the cases found in literature, did a group of researchers attempt to use the actual pillars for another function apart from giving the structure which the cells will grow around [51]. In this case, they used conductive hydrogel pillars as a measurement tool to measure the response signal of the cells when stimulated.

Nevertheless, significant opportunities remain for the exploration of novel ideas and approaches to enhance the existing devices in this field, considering that the development of this particular application is still in its early stages.

On Table 1.3 a comparison between the different devices previously mentioned is presented.

Table 1.3: Comparison in between already existing devices.

Device	Electrical Stimulation	Mechanical Stimulation	Measurement method	Technologies used	Materials
MTF Device [46]	External electrodes	None	Image processing	Muscular Thin Film Technology	Glass, PDMS
Cytostretch [52]	Embedded MEA	Pneumatic	Embedded MEA	Silicon-based fabrication Soft Lithography	Silicon PDMS Metals
Dostanic's [40]	Embedded microelectrodes	None	Capacitive sensors	Silicon-based fabrication Soft Lithography	Silicon, PDMS, Metals
Bi/ond's device [53]	Only in the Let-it-bit	None	Optical tracking	Silicon-based fabrication Soft Lithography	Silicon, PDMS, Metals
Hydrogel device [51]	Embedded electrodes	None	Optical Tracking Electric signal recording	Photolithography Lift-off	Conductive hydrogel, PDMS, Metals

1.6. Research question

As mentioned before, most of the Muscle-on-chip devices use the pillar structure so that the cells can grow around them and form a bundle. This allows for a better alignment of the muscle bundles as well as helps with the correct maturation of the seeded cells into actual skeletal muscle cells or in other cases cardiomyocytes [18]. As found in literature, the majority of these pillars are made of polymers. The company Bi/ond, on the other hand, has opted to make the pillars of the chip out of Si.

The scope of this project is to use the already designed platform for muscle-on-chip made by the company Bi/ond and integrate 3D microelectrodes that can stimulate the muscle cells. In previous prototypes, such as the Let-it-Bit, the microelectrodes were integrated into the well and are 2D electrodes. 3D microelectrodes present some major advantages over 2D microelectrodes thus this implementation would be a major improvement in this area. These advantages will be explained in the following chapter of this report.

The new approach aims to solve the problem arising from 2D microelectrodes and thereby leads us to the following research question: **How to implement 3D microelectrodes in a Muscle-on-Chip device from Bi/ond for the stimulation of the muscle cells?**

This research question acts as the main driver of the work that will follow in my master thesis. Several sub-questions need to be answered before this objective can be achieved:

1. What kind of design will these 3D microelectrodes have?

2. What materials will be used for the implementation of such electrodes?
3. How to interact with the electrodes once they are implemented inside the device?
4. Do the metal lines withstand possible stresses in the system?
5. How to make the signal travel from the silicon pillar to the electrolyte?

1.7. Outline of the Report

This report contains 6 chapters. Chapter 1 served as an introduction and motivation for this project where the current approaches in industry are discussed. Chapter 2 refers to all the fundamentals on which this project is based. Chapter 3 relates to the design of the final device and the device considerations taken into account. Chapter 4 describes the fabrication process of such a device and also explains the different challenges encountered and how were they overcome. Chapter 5 describes the electrochemical characterization of the device alongside the results. Finally, in chapter 6, the conclusion of this project is presented as well as some recommendations for future work related to this topic.

2

Background

This chapter will focus on the approach followed in this project to implement 3D microelectrodes into the Muscle-on-Chip device developed by Bi/ond. It is therefore important to remark the main characteristic of the platform from this company. Bi/ond's platform differs from others in that they use silicon as one of the base structural materials for the development of their device. The common trend amongst other companies and research groups is to only use flexible materials such as polymers.

There are different ways to implement 3D microelectrodes into an OoC platform. Various ideas have already been studied by other research groups, especially in the field of Microelectrode Arrays (MEAs) [55]. These approaches could provide 3D microelectrodes into the system at the expense of space inside the well. Although these options could be a possibility for the scope of this project, the existence of the silicon pillars inside the device also gives new possibilities. The pillars are necessary for structural purposes so that the muscle bundle can form around them. As these pillars are already inside the platform, this project will study the possibility of using these pillars not only as structural support for the development of the muscle cells but also as electrodes for the stimulation of such cells. Silicon is a semiconductor and because of its properties, it can conduct electricity under certain conditions. If the pillars of the system can be also used as the electrodes themselves, some problems regarding the distance between the electrodes and the tissue that needs to be stimulated would be solved. It would also solve several problems that arise from using external electrodes.

One of the problems regarding the use of electrodes for stimulation is that they usually are not near the cells (both 2D or 3D electrodes). This being the case, the signal needed for an action potential (AP) and consequently a contraction of the muscle bundle needs to be larger the further the electrodes are. This is to ensure that the signal can reach the muscle bundle with enough energy to create the AP as it needs to travel through the medium to reach the cells. This creates Faradaic irreversible reactions at the electrode-electrolyte interface which leads to changes in the electrolyte and the culture medium that could be detrimental for the tissue as explained in Section 1.5.2. This issue can also cause hydrolysis in the medium itself which can produce foaming, disturbing the optical window of the well. By making the pillars the electrodes themselves, the stimulation of the muscle cells can be done directly at their place of anchoring so this problem would be solved. The amplitude of the electrical signal would not need to be so high thus avoiding both irreversible Faradaic reactions at the electrode-electrolyte interface and the production of foam because of hydrolysis.

If Faradaic reactions do occur at the interface between the electrode and the electrolyte, some current will be injected into the electrolyte. This current injection would generate heat that will dissipate inside the electrolyte increasing its temperature. If this temperature change is sufficiently big, it could be detrimental to the tissue.

On the other hand, a challenge regarding the use of external electrodes for the stimulation of the cells is that this implementation usually requires the need for an additional device. This makes the use of the Muscle-on-Chip platform more complex for the user. The integration of such electrodes already on the device facilitates the handling and usage. The implementation of external electrodes into the well can also reduce the optical window of the well as more components are added to the system. If the pillars inside the well are therefore used not only for the structural support of the muscle cells but also as the stimulation platform, fewer components would be present in the field of view when studying the muscle cells.

Another major disadvantage of using external electrodes for the stimulation of the cells is the possible disturbance that the cells might experience when implementing such electrodes. When culturing cells, biologists try to interact with the cells as little as possible as any disturbance could lead to changes in their maturation process and even cell death. Ideally, every measurement or action related to the cells would be performed inside an incubator where the external conditions of the cells remain constant and under control. Therefore, if the electrodes are already implemented inside the system, less disturbance would be made to the cells when performing electrical stimulation.

Because of these reasons, the approach of this project is to test whether the silicon pillars can be used as electrodes for the stimulation of the muscle bundle. To do so, contact with the pillars inside the well must be implemented so that the signal can be transmitted. As the pillars are released on top of the PDMS membrane, the option chosen in this project was the development of a certain track that would contact the base of the pillars from underneath. This path must therefore be able to conduct an electrical signal that would then go through the Si pillar to stimulate the muscle cells. Metal lines were then explored to make this connection as depicted in the simple schematic in Figure 2.1. This approach is completely novel in that the pillars are used for the electrical stimulation of the muscle cells and not only for structural purposes.

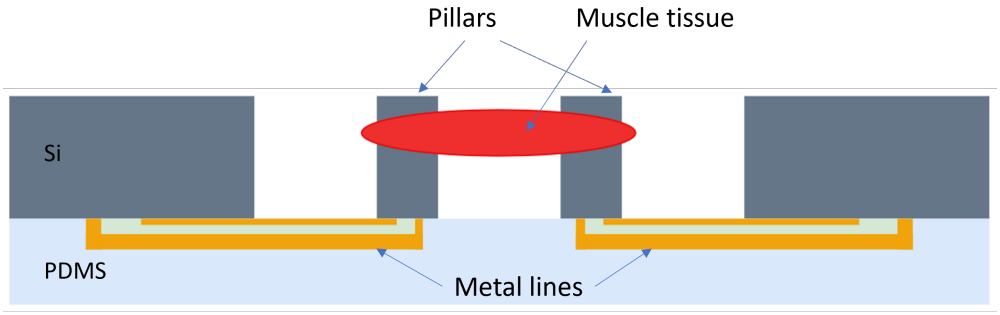


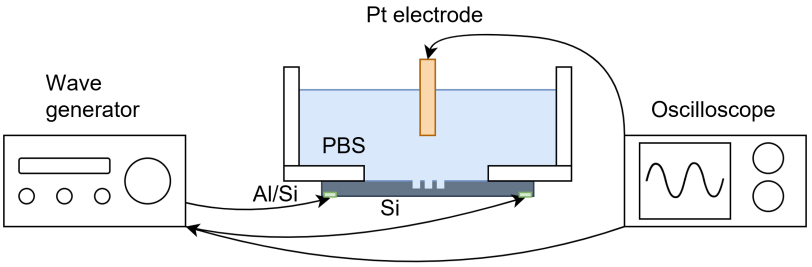
Figure 2.1: Schematic representation of the approach of this project for the implementation of 3D microelectrodes in a Muscle-on-Chip device.

2.1. Interface between Si and electrolyte

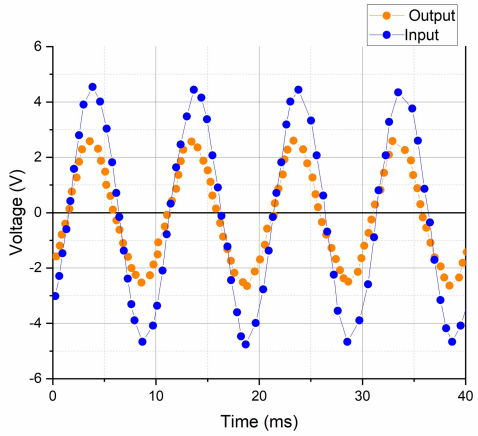
The first step of this project is to determine whether the silicon pillars can transmit a signal into an electrolyte. In this manner, the silicon pillars would act as the electrodes. To prove the feasibility of this idea, a simple test was made. A MUSbit [53] device from Bi/ond was used. Al/Si was deposited in the four corners of the chip in the shape of contact pads. To do so, photomasks already designed by the company were used. The chip was then wire-bonded to a PCB so that there could be contact between the exterior and the silicon chip.

This way, the whole silicon chip would be connected thanks to the Al/Si contact pads and the well would be exposed. Then, using a signal generator (Agilent 33120A), a sinusoidal wave of 1Hz and 5 Vpp (Voltage peak-to-peak) was applied to the silicon chip. The well of the chip was filled with phosphate-buffered saline solution (PBS) and an external platinum electrode connected to an oscilloscope was used to measure the the signal inside the well.

Two probes were used in the oscilloscope. One of them was used to measure the actual signal that was being input to the silicon wafer. The second probe was connected to the external platinum electrode that was inserted inside the well of the chip. The reading of the oscilloscope is depicted in Figure 2.2. The blue signal refers to the applied signal to the system, it is the input wave. The yellow signal is the one referring to the platinum electrode inserted inside the well.



(a) Schematic for the set up of the measurement.



(b) Data reading from the oscilloscope.

Figure 2.2: Simple measurement done with a wave generator and an oscilloscope.

From this result, it can be concluded that a signal was measured inside the electrolyte inside the well. The signal measured was greatly attenuated but the same pattern could be seen. It is true that in this case, it was the whole silicon chip that provided the signal to the electrolyte instead of just one of the silicon pillars. Nevertheless, this result states that it is possible to transfer a signal from bulk silicon into an electrolyte thanks to an Al/Si connection.

2.2. Material Selection for the metal lines

This section will focus on the materials chosen for the realization of this project. As previously stated, the approach of this project is to contact the silicon pillars inside the well with metal lines so that they can become electrodes for the stimulation of the muscle cells. There is a variety of options from which to choose both in terms of wafer selection and metal selection. Regarding the metal selection, certain requirements are needed. First of all, the metal must have good electrical conductivity to ensure the transmittance of the signal. Secondly, it must be compatible with the IC-manufacturing techniques employed at Else Kooi Laboratory (EKL) clean room. This means that the metal must be considered a "Green Metal" so that the wafers are not considered contaminated once the metal is deposited and can be processed in the majority of the machines. Lastly, it must be an available material inside the facilities of EKL for its ease in manufacturing. Due to these requirements, three different metals were explored in this project: aluminum/silicon (Al/Si), titanium (Ti), and titanium nitride (TiN).

Aluminum is a metal commonly used in microfabrication because of its great properties in which its electrical conductivity is especially remarkable [56]. One of the main downsides of using this metal is that when in contact with silicon, it diffuses into the silicon which could have detrimental consequences depending on the purpose of the device [57]. The diffusion of aluminum inside this device, for example, could prove detrimental if previous steps of ion implantation or epitaxial layers are performed before metal deposition as it would create shortcuts in the structures. To avoid this kind of behavior, it is standard that instead of using pure aluminum as a metal for the metallization of devices, aluminum with a 1% concentration of silicon is employed. This doping of the aluminum with silicon helps avoid spiking and diffusion of the metal into the wafer. Al/Si is therefore widely used in the semiconductor industry as well as in many microfabrication processes. It is also easily accessible inside the clean room and the recipes related to this metal have been standardized, making it easier to work with. The main disadvantage related to the use of Al/Si is its high oxidation rate. This leads to a rapid formation of an aluminum oxide layer on the surface of the metal when exposed to air. Unfortunately, aluminum oxide is not considered biocompatible. Consequently, in the event of contact with cells, it has been observed to cause cellular degradation, as evidenced in prior tests conducted by the biologists at Bi/ond. Therefore, if this metal was to be used, it must never be in contact with the culture medium in which the cells are developing. Another disadvantage of this metal is its high etching rate in hydrofluoric acid (HF) solution. As later shown, a final HF bath step is required for the release of the silicon pillars on top of the PDMS membrane. A process already provided by Bi/ond. If Al/Si were to be exposed to this chemical, it would be removed from the device.

Another metal widely used in microfabrication is Ti. Although it presents a much lower electrical conductivity than Al [58], its use in the biomedical field is well extended. It is a highly biocompatible material that is employed in many implants and has recently been used in some microelectrode applications both as substrate and as the contacting metal with tissue especially for neuronal applications [59] [60]. Ti also presents great ease of manufacturing and availability which makes it an interesting option worth studying. Ti also oxidizes quite rapidly which could have a detrimental effect on its electrical conductivity and presents a similar etching rate in HF to Al.

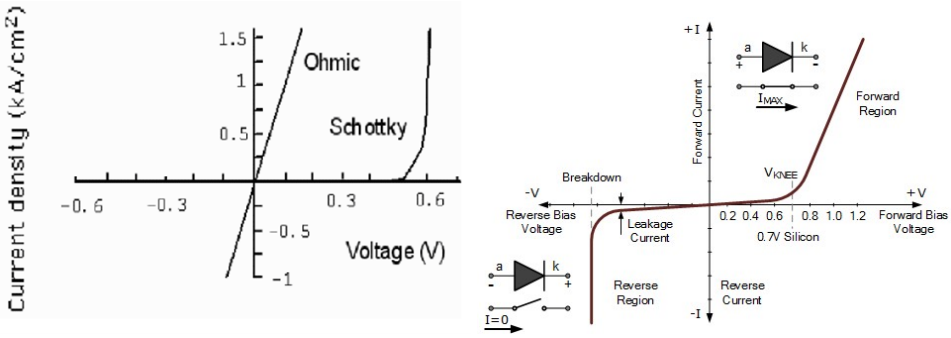
Lastly, TiN was also studied in this project as one of the possibilities for the metallization of the metal lines. TiN is an alloy of Ti with worse electrical conductivity than Ti [55]. Previous research groups have used this metal for the fabrication of microelectrodes for neural and cardiac cell recording and stimulation [61]. One remarkable property of TiN is that it has a slow etching rate in HF solution which could be beneficial at later stages of the process as a final HF bath step is needed for the release of the pillars.

Although other metals were also considered, these three metals were finally selected to be studied based on their fulfillment of the requirements. Their interaction with different Si wafers was studied. Initially, standard Si wafers were chosen, both p-type and n-type wafers with a resistivity of 1-5 Ω·cm. High-resistivity wafers were also later studied in combination with the best metal from the previous results. These high-resistivity wafers, both n-type and p-type, present a resistivity of 5-10 Ω·cm.

2.2.1. Contact to the Silicon pillars

Silicon, being a semiconductor, gives rise to certain phenomena when in contact with metals due to the difference in their energy levels [62]. This disparity results in the formation of a Schottky barrier, which permits the conduction of current in a specific direction and inhibits the flow of current at low voltages and in the reverse direction [63]. This Schottky barrier is not ideal for the system of this device as it would require a higher voltage to be applied to transmit the signal. If high voltages are applied, then there is injected current into the electrolyte which is not desired for the correct stimulation of the muscle cells as it would alter the characteristics of the culture medium. There are certain techniques employed in industry to improve the metal-semiconductor contact and eliminate the effect of the Schottky diode [64] [65] [66] [67]. The contact between the metal and the silicon pillar should be as ohmic as possible. This way, the signal can be transmitted with ease. The difference between an ohmic contact and a Schottky diode in terms of their I-V curve can be appreciated in Figure 2.3. Note that the

ohmic contact presents a more linear shape when compared with the Schottky diode curve.



(a) I-V curve for Schottky diode and Ohmic contact [68]. **(b)** Schottky diode showing the breakdown voltage [63].

Figure 2.3: I-V curves of the Schottky diode phenomena.

One of the main characteristics of the Schottky diode in Si is that the increase in current flow always occurs at the same voltage, this is 0.6-0.7 V (as depicted in Figure 2.3). This is a specific characteristic related to the energy band structure of bulk silicon due to its crystalline structure. The Schottky diode appears as both the metal and Si have different energy levels thus charge carriers can not flow as easily from one material to the other. Another characteristic of such phenomena is the existence of a breakdown voltage. This breakdown voltage is a diode parameter that specifies the maximum reverse voltage that can be applied without inducing a significant exponential rise in the diode's leakage current [69]. When studying the interaction between the three metals listed before and the different Si wafers, these two characteristics will be searched. For this purpose, Van der Pauw structures were utilized to study the interaction of the metals and the Si wafers at the interface.

2.3. Van der Pauw structures

The use of Van der Pauw structures is a common method in microfabrication for the study of resistivity of materials used in a process flow, typically in the form of thin films. This technique consists of a 4-point electrical measurement on a substrate. The original Van der Pauw structure is used so that a current is forced in between two of the points and the voltage is measured at the other two points. In the case of this project, this method was changed. As in this project what was of interest was the study of the junction between different metals and Si, a certain voltage is induced in between two of these points, and the current is measured at the other two points. The points in which the voltage is applied need to be adjacent to be able to measure the current properly. A sweep of voltage is applied between two of these points and the current is measured at the two other points. A schematic of such setup can be seen in Figure 2.4.

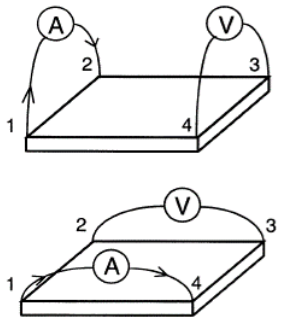


Figure 2.4: Set-up for van der Pauw measurement [70].

To make use of this method, the structure needs to be defined on top of the Si and the metal needs to be deposited. To reduce possible diffusion of the metal into the silicon, the surface area of

contact between the metal and the silicon wafer was shaped in the form of small squares arranged as a mesh. This way the total contact area is reduced. A top view of the final design for this experiment can be seen in Figure 2.5. PECVD Silicon oxide (SiO_2) was used as the insulation layer so that the metal would only be in contact with the silicon wafer underneath both layers at the small squares depicted in Figure 2.5.

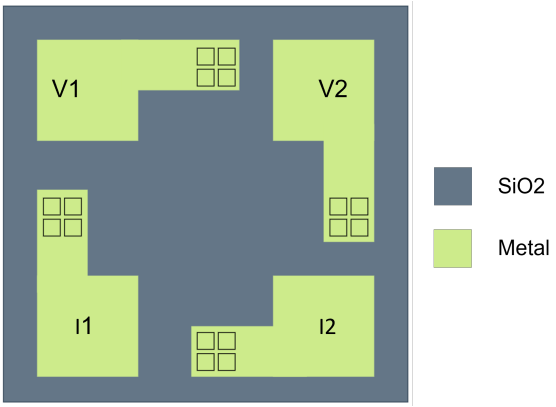


Figure 2.5: Van der Pauw structure used in the test.

The big square metal lines are made so that the probe can easily be positioned on top of it to make contact for the measurements. To fabricate such a structure, the following process flow was carried out. Its 2D representation can be seen in Figure 2.6. This 2D process flow only depicts the flow for one of the pads. The final structure of the Van der Pauw consists of 4 of these pads as seen in Figure 2.5. The full flow chart can be found in Annex C.

For the tests with the Van der Pauw structures, single-side polish (SSP) wafers are used. Both n-type and p-type wafers are tested so that the interaction between the different metals and different wafers can be studied. The process starts with the definition of the zero layer on the wafer so that the alignment markers are on top of the wafer. For this process, the first step is to coat the wafer with 1.4 μm of photoresist (Megaposit SPR3012 [71]) using the EVG120 coater. Afterward, the wafer is exposed using the ASML PAS 5500 waferstepper with a dose of 140 mJ/cm^2 to define the alignment markers on top of the wafer. In the next step, the wafer is developed using the EVG120 developing station in a single puddle process. Finally, the alignment markers are etched with dry etching in the tool Trikon Omega 201 plasma etcher. At the end of this sequence, the photoresist is stripped using oxygen plasma in the Tepla Plasma 300 and is cleaned in the standard Si cleaning line at EKL. This standard Si cleaning line consists of 5 different steps and will be detailed later in Chapter 4.

This is when we get to Figure 2.6a. At this point, the deposition and definition of the insulation layer need to be done. 500 nm of plasma enhanced chemical vapour deposition (PECVD) SiO_2 are deposited on top of the wafer to create the insulation layer in between the metal and the Si bulk (Figure 2.6b). Then, the wafers are coated in the EVG120 with 2.1 μm of photoresist (Megaposit SPR3012). Afterward, the wafer is exposed in the ASML PAS 500 to the photomask called **CO** to define the contact openings between the metal and the Si. The wafer is exposed to 260 mJ/cm^2. Later on, the wafer is developed with a single-puddle process in the EVG120 developing station. The SiO_2 exposed by the openings in the photoresist is then dry-etched in the Drytek Triode 384T plasma etcher using the standard oxide etch recipe. The final steps of this part of the process are the stripping of the photoresist in the Tepla Plasma 300 and the cleaning of the wafer in the standard Si cleaning line (Figure2.6c).

The best possible contact between the metal and the silicon wafer is desired. If the wafer is left exposed to air, a thin layer of native oxide forms on its surface. Removal of this native oxide layer is therefore necessary before the deposition of the metal. To do so, a Marangoni cleaning step is done. This process is detailed in Chapter 4.

After this, deposition of the metal is done. In all cases with the three different metals, the same step was performed. 500 nm of the metal are sputtered on top of the wafer using the Trikon Sigma 204

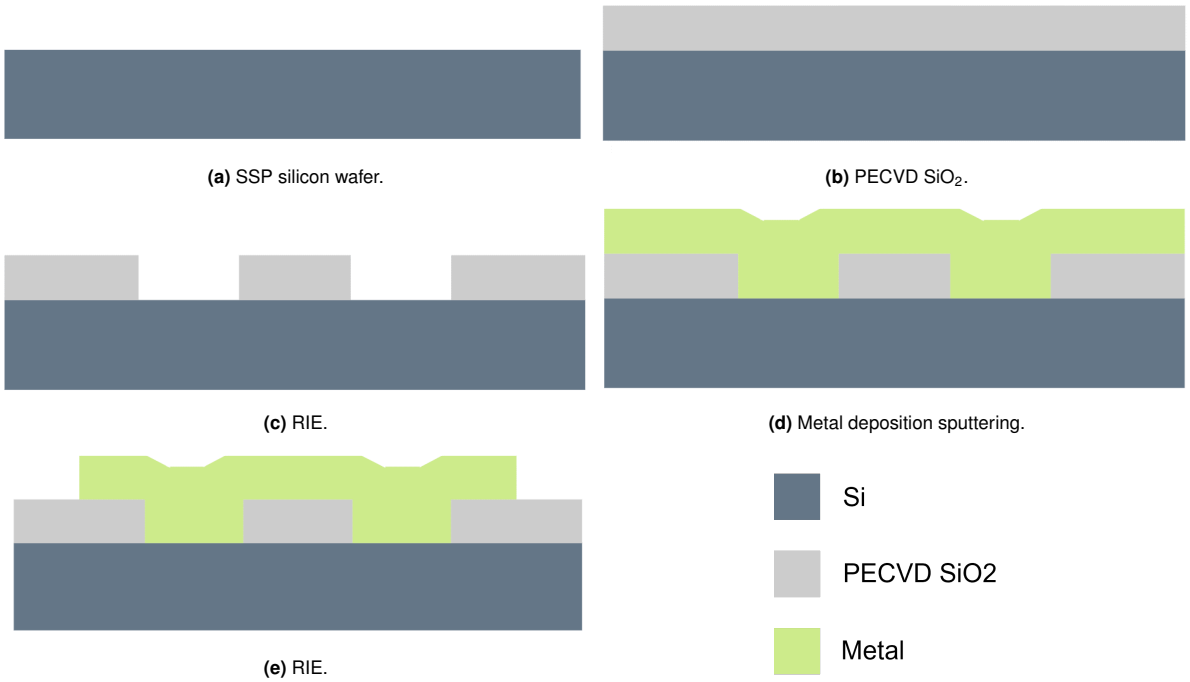


Figure 2.6: 2D process flow for the Van der Pauw structures for a single pad.

sputter coater (Figure 2.6d). All metals were deposited at 350 °C. Then, the wafer is coated with 2.1 μm of photoresist Megaposit SPR3012 in the EVG120 coater. The wafer is then exposed using the ASML PAS 500 using the photomask called **NO** with 260 mJ/cm^2 energy. After the exposure, the wafer is developed in a single-puddle process in the EVG120 developing station. Now the metal needs to be defined and etched. The wafers are put into the Trikon Omega 201 plasma etcher for dry etching of the metals. As three metals are studied in this test, three different recipes are used in the Trikon Omega 201 plasma etcher, one for each metal. Finally, the photoresist is stripped in the Tepla Plasma 300 and the wafer is cleaned. In this case, as the wafer has metal deposited on top, the wafer must undergo the cleaning line devoted to green metals. To avoid cross-contamination, specific carrier wafers are used in this cleaning line. This process of green metals cleaning line is detailed in Chapter 4. After the end of this process, the wafers are ready for the electrical measurements.

2.3.1. Measurement set up

The shape of the Van der Pauw structures can be seen in Figure 2.5. In this structure, 4 contact pads can be appreciated. Those are the four contacts in which the probes from the measurement tool will land. The measurements were made using a Cascade probe station (CAS31). This station can be seen in Figure 2.7.

As stated before, the measurements were done using a 4-point measurement arrangement. A certain voltage sweep was set in between two of these points. Important to note that these two points need to be adjacent to each other. The current is then measured in the other two points and can be extracted. 3 different voltage ranges were made. From -1 to 1 V, from -2 to 2 V, and from -5 to 5 V. These ranges were chosen so that there could be a study of the interaction between the metal and the silicon at different voltages so that the shape of the curve could give more information about the interface both at low and high voltages.

In order to have an accurate representation, 3 different samples/chips were measured for each one of the voltage ranges. The three measurements were then averaged and then the final result was studied. In order to measure the current correctly at points I1 and I2 (seen in Figure 2.5), a voltage of 0 V must be biased at these points so that only the current flow is measured. The parameters used

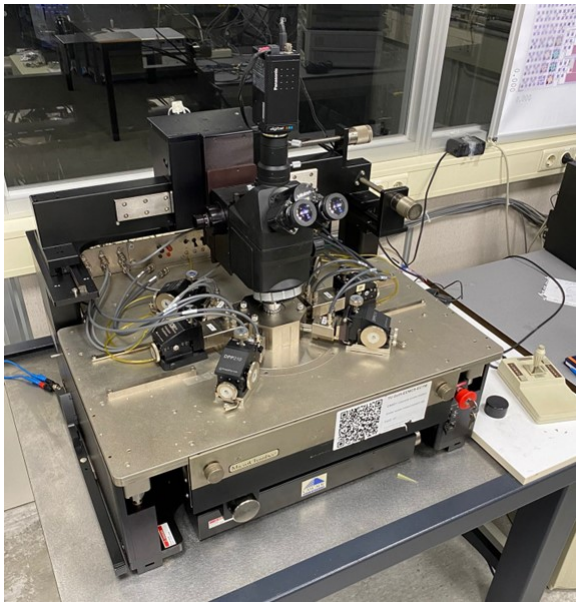


Figure 2.7: Cascade probe station (CAS31).

during the test can be seen in Table 2.1.

Table 2.1: Parameters used in the Cascade probe station.

Parameters	**Input: V1**	**Input: V2**	**Output: I1**	**Output: I2**	**Input: V in I1**	**Input: V in I2**
Mode	V	V	I	I	V	V
Unit	HRMSU3	HRMSU1	HRMSU5	HRMSU6	HRMSU5	HRMSU6
Compliance	100.0m	100.0m	100.0m	100.0m	100.0m	100.0m
Sweep type	Linear	None	None	None	None	None
Values for Sweep	(-1, 1)V (-2, 2)V (-5, 5)V	None	None	None	None	None
Value	Sweep	0V	-	-	0V	0V
- Node	Ground	Ground	Ground	Ground	Ground	Ground

Based on the structure design, the equivalent circuit shown in Figure 2.8 can be obtained regarding the different resistances the current must surpass to close the circuit. This is in the case an Ohmic contact is established. The total equivalent resistance can then be obtained through Equation 2.1 where R_t is the total resistance, R_{pad} corresponds to the resistance of the metal pads, R_c describes the contact resistance in between the metal and the silicon wafer, and R_{bulk} represents the resistance of the bulk of the silicon wafer. In case there is no Ohmic contact and instead there are some diodes present, the equivalent circuit model would look like depicted in Figure 2.9. These representations are true in direct current (DC) measurements of the Van der Pauw (VDP) structures.

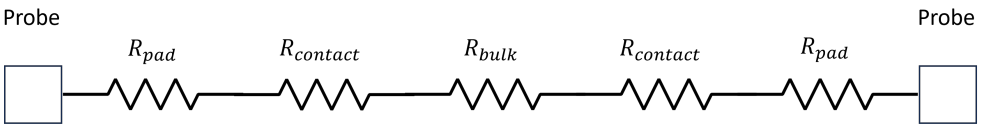


Figure 2.8: Equivalent circuit of the connection in the VDP structure Ohmic contact.

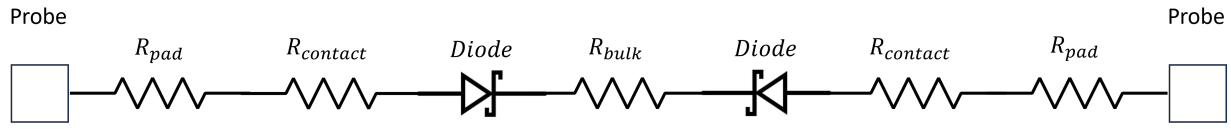


Figure 2.9: Equivalent circuit of the connection in the VDP structure diodes present.

$$R_t = 2 \cdot R_{pad} + 2 \cdot R_c + R_{bulk} \tag{2.1}$$

In this project several assumptions were made regarding this approach. The silicon wafer is considered homogeneous thus the resistance of the bulk should be equal in all the wafers regardless of what metal is deposited on top. To prove this assumption, the readout measurements in both the vertical and the horizontal lines (I1 and I2) should be equal. The second assumption is that the resistivity of the metal is so low in comparison with the resistivity of the silicon wafer that the values of the resistance of the metal pads can be neglected.

With these assumptions, if the I-V measurements for the different combinations of metals and silicon wafers are obtained, a comparison between the contact resistances of the different metals with the silicon wafers can be withdrawn.

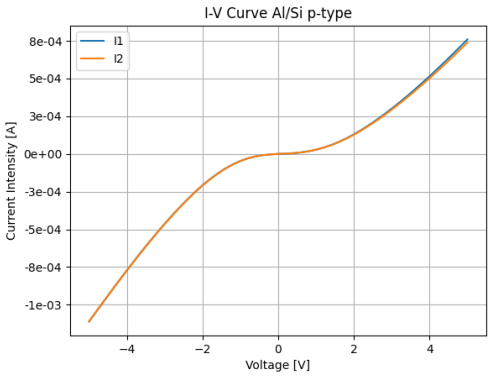
To obtain the resistance from the I-V plots, Ohm's law was used (Equation 2.2) using the first derivative of the curve. Then this first derivative was plotted against the voltage sweep so the resistance of the interface was plotted as a function of the voltage applied.

$$I = \frac{V}{R} \rightarrow R = \frac{\Delta V}{\Delta I} \tag{2.2}$$

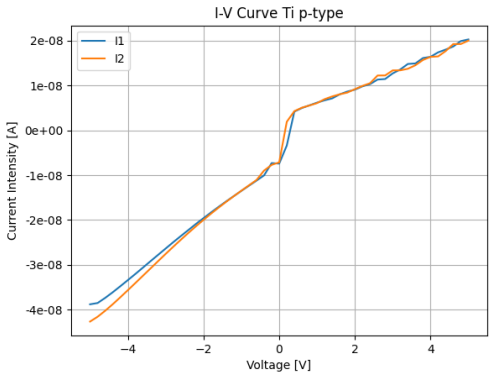
2.3.2. Results & Discussion

As mentioned previously, three I-V measurements were made for each one of the voltage sweeps in three different chips and averaged. The data obtained from the Cascade probe station was retrieved and handled thanks to a python code that I developed. The results obtained in the range of -5 to 5 V will be shown as that is the range which gives the most information.

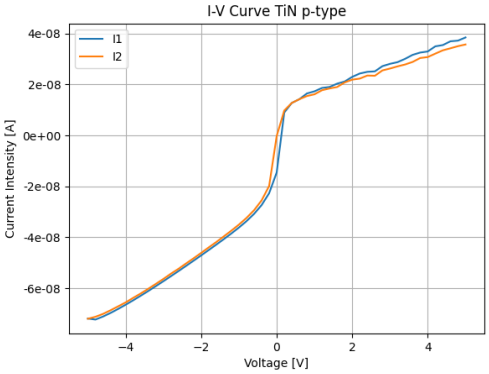
The results obtained from the standard p-type wafers will be presented first. The measurements regarding the different metals can be seen in Figure 2.10. When making a comparison, several differences can be appreciated. The first thing that can be seen is the difference in shape. The curve corresponding to the Al/Si has a very different shape when compared with the shape of Ti and TiN. In terms of linearity, the curve from Al/Si is the closest to the straight line that we want to achieve corresponding to an Ohmic contact. Another main difference that can be appreciated when comparing these 3 graphs is the scale of the results. Looking at the graph of Al/Si, the values of the current measured are in the range of 10^{-5} whereas, in the case of Ti and TiN, they are in the ranges of 10^{-9} and 10^{-8} respectively. This is three to four orders of magnitude difference. It is also interesting to see that none of these graphs show the standard Schottky diode behavior. Neither the breakdown voltage nor the 0.6-0.7 V threshold is seen in the I-V measurement. This can be appreciated when looking at the range of -1 to 1 V depicted in Figure 2.11. The characteristic asymmetry for the I-V curve of a diode is also missing. It can also be seen that both the measurements of I1 and I2 have very similar values thus confirming the initial assumption of homogeneous wafer.



(a) I-V curve Al/Si on p-type (-5,5)V.



(b) I-V curve Ti on p-type (-5,5)V.



(c) I-V curve TiN on p-type (-5,5)V.

Figure 2.10: Results for the standard p-type wafer 1-5 Ω·cm.

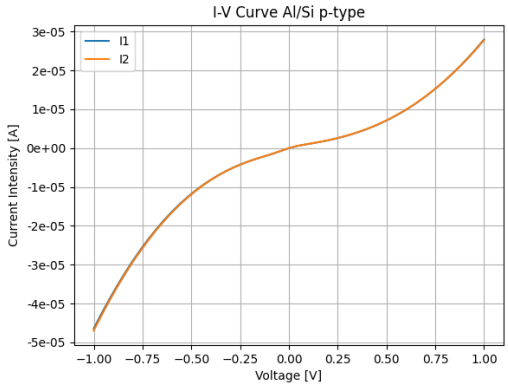
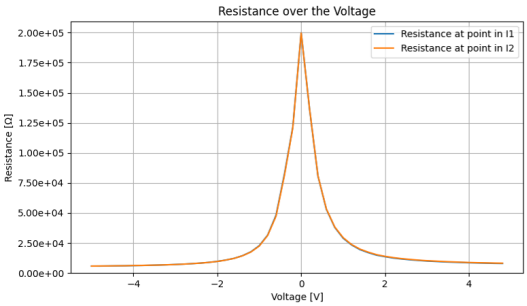
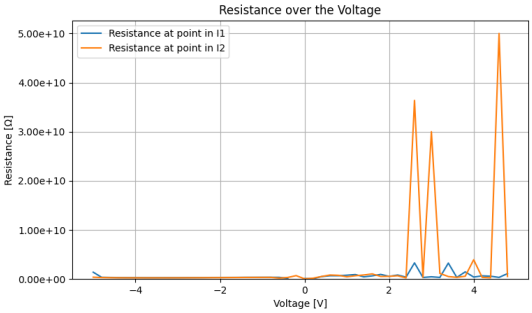


Figure 2.11: Results of the range of -1 to 1 V for Al-Si on a p-type wafer.

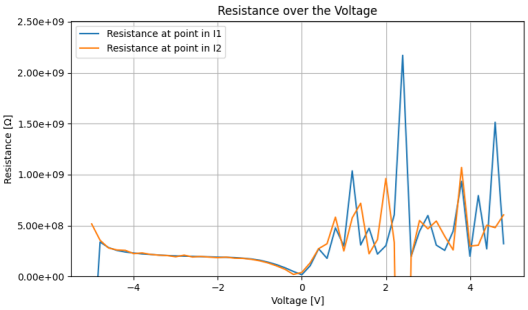
The data obtained from these plots was then used to calculate the resistance as a function of the applied voltage. The final results can be seen in Figure 2.12. When looking at these results, only the one related to the Al/Si looks attractive. In the case of the Ti and TiN, the behavior of the I-V curve is an indicator of what the measurement system tries to give as output because it is not capable of measuring any current through the system with accuracy. This was also seen in previous research regarding the study of Ti which confirms these findings [72]. This fact was consulted with the lab technician and it was stated that the values were too small for the measurement system to sense them. There was some limitation regarding the measurement system.



(a) Resistance Al-Si p-type (-5,5)V.



(b) Resistance Ti p-type (-5,5)V.



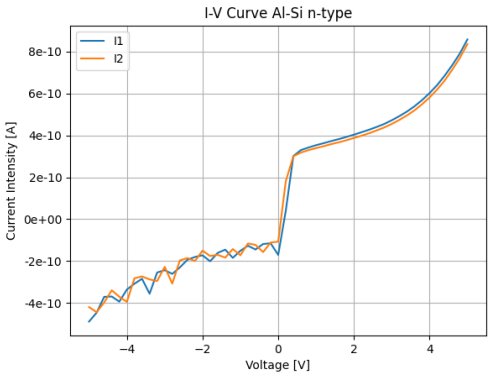
(c) Resistance TiN p-type (-5,5)V.

Figure 2.12: Results for the standard p-type wafer 1-5 Ω·cm of the resistance against voltage.

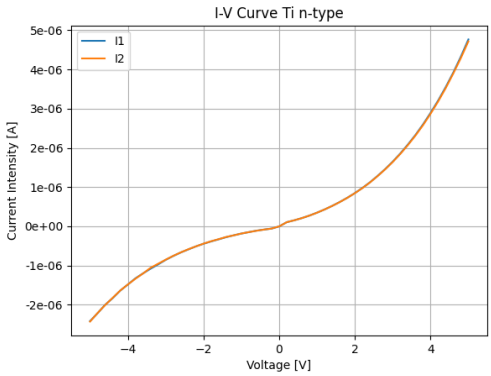
Focusing our attention on the result of the Al/Si, it becomes evident that the system's resistance undergoes alteration when the values approach 0 V. When higher values of voltage are reached, the resistance becomes relatively constant. This kind of behavior relates to an ohmic contact, particularly at higher voltages.

The change of resistance at lower voltages can be related to the fact that there are not only resistive components at the contact between Al/Si and Si but also some other unknown components. This would explain the change in resistance at lower voltages.

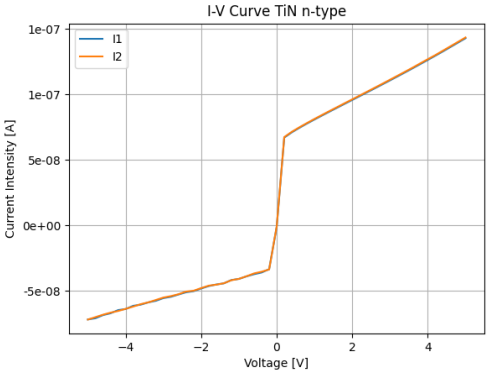
The interaction of these 3 metals was also studied with a different type of wafer. In this case, a n-type wafer. Again, we are mostly interested in the range of -5 to 5 V. The results for all three metals will be presented and compared. These results can be seen in Figure 2.13.



(a) I-V curve Al/Si on n-type (-5,5)V.



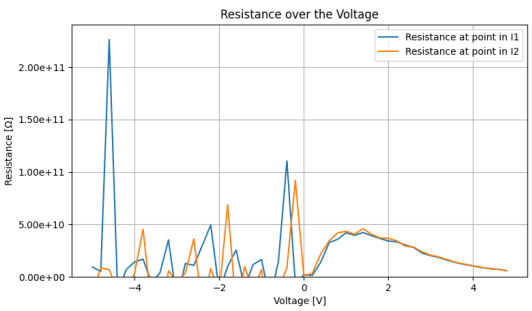
(b) I-V curve Ti on n-type (-5,5)V.



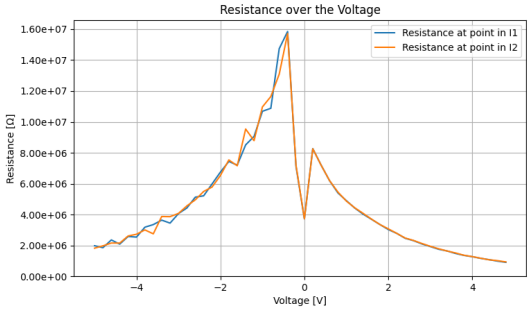
(c) I-V curve TiN on p-type (-5,5)V.

Figure 2.13: Results for the standard n-type wafer 1-5 Ω·cm.

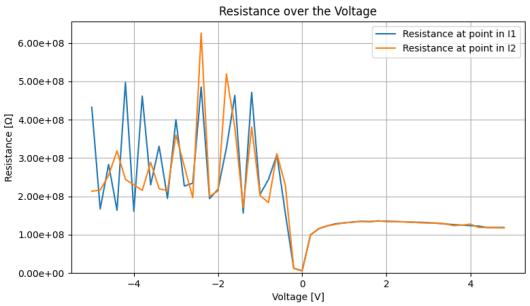
When looking at these results, similar problems arise in the case of Al/Si and TiN where the values are so small that the measurement system is not capable of providing a valid output. In the case of the n-type wafers, the curve geometry that most resembles the ohmic contact is for Ti. The resistance against voltage measurements regarding this interaction, illustrated in Figure 2.14, also supports this condition. Only the results obtained for Ti gave a reasonable output. For higher voltages, similar behavior can be appreciated in terms of a relatively constant resistance in the case of Ti.



(a) Resistance Al-Si n-type (-5,5)V.



(b) Resistance Ti n-type (-5,5)V.

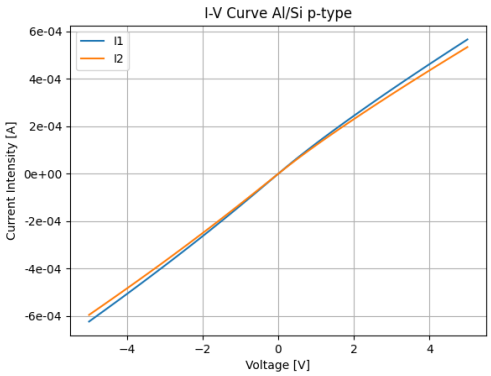


(c) Resistance TiN n-type (-5,5)V.

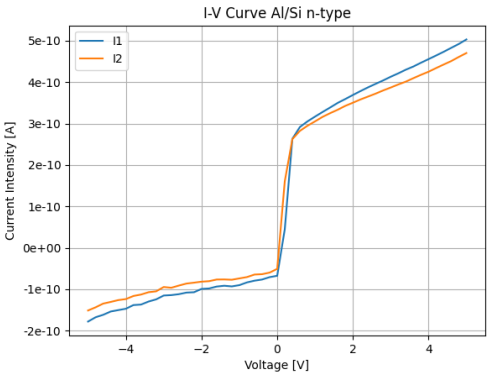
Figure 2.14: Results for the standard n-type wafer 1-5 Ω·cm of the resistance against voltage.

Based on all the results obtained from these measurements and data analysis, when comparing the results for Al/Si on a p-type wafer and the results for Ti on a n-type wafer, the combination that gave better results in terms of resistance over voltage was the Al/Si on top of p-type wafer. Therefore, this combination of both metal and silicon wafer was selected for further study and development in this project.

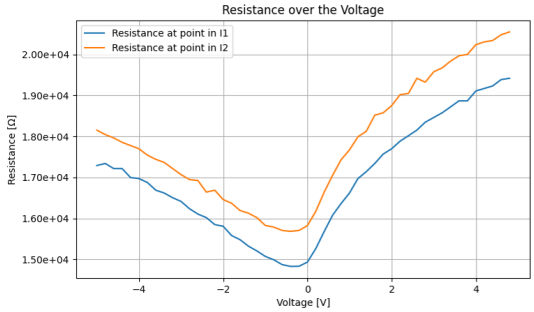
Regarding the high-resistivity wafers, as Al/Si was the metal giving the most promising results, Al/Si was deposited on these wafers and measured their I-V curves. The results can be seen in Figure 2.15 where both the I-V curves and the resistance over the voltage are plotted.



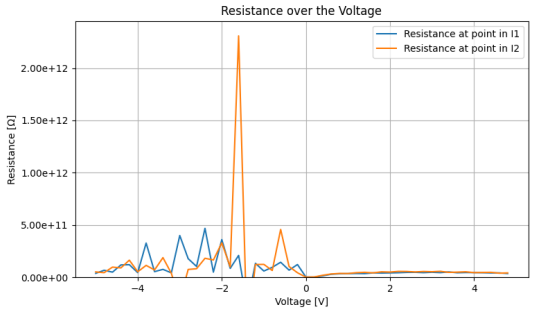
(a) I-V curve Al-Si p-type (-5,5)V high resistivity.



(b) I-V curve Al-Si n-type (-5,5)V high resistivity.



(c) Resistance Al-Si p-type (-5,5)V high resistivity.



(d) Resistance Al-Si n-type (-5,5)V high resistivity.

Figure 2.15: Results for the high-resistivity wafers both p-type and n-type.

Looking at these results, it seems that the p-type high-resistivity wafer presents a better ohmic contact with the Al/Si. Nevertheless, due to the difficult availability of these wafers inside the clean room, the standard p-type silicon wafer was selected.

The next chapter will discuss the device design and the different considerations taken into account for the development of this project.

3

Device Design

The final goal of this project is to integrate 3D microelectrodes into the Muscle-on-Chip device developed by the company Bi/ond. This Chapter will describe and explain the device design and the decisions made before the microfabrication. The device's material selection, thicknesses, and geometries will also be explained. The process flow will also be detailed.

3.1. Silicon pillars as electrodes

Based on the results obtained at the early stages of the project, detailed in Chapter 2, it was decided to implement Al/Si as the metal for contacting the base of the pillars inside the device. This way, the pillars of the platform would be able to serve not only as structural support but also as the electrical stimulation electrodes for the cells growing inside the well. A schematic of such an approach is depicted in Figure 2.1.

3.2. Device design considerations

3.2.1. Contacting the base of the pillars

The main goal of this project, as previously stated, is to make the silicon pillars the electrodes of the platform for the stimulation of the muscle cells. The main framework, the well with the pillars inside, in which this approach is studied, has already been developed by Bi/ond in collaboration with the master student Shriya Rangaswamy [73]. Shriya's thesis revealed that the optimal configuration for implementing metal lines inside the well was to adopt a turtle-shaped pattern. The metal lines also need to be straight instead of meandering, as explored in her project. An illustration of this design can be seen in Figure 3.1. This design allows access to the interior of the well through three entry points on each side (a total of 6 entry points).

When establishing the contact between the metal lines and the pillars, it is of great importance to determine the configuration of this connection. In the course of this project, four distinct design approaches were examined. One of the main considerations in shaping the contact between the metal lines and the pillars was the preservation of the pillars' available surface area to ensure their structural integrity. The pillars need to maintain stability on the membrane both during the fabrication process and when subjected to the contractions of muscle cells. This is why two primary design concepts were explored concerning the configuration of the metal lines at the base of the pillar. From now on, this structure will be referred to as "electrode".

One of the designs has a circle-shaped electrode at the end of the metal line. This way, the

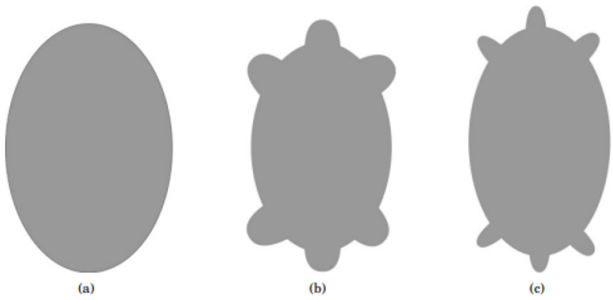
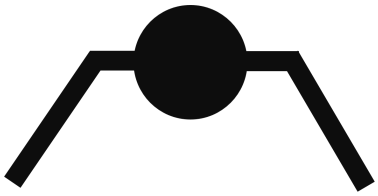
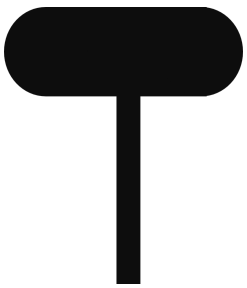


Figure 3.1: Mask designs studied in Shriya's thesis. (a) Oval geometry; (b) Turtle geometry with extensions for meanders; (c) Turtle geometry with extensions for straight lines. The figures are not drawn to scale [73].

surface occupied by the electrode at the base of the pillar is around one-third of the total surface area. The free surface of the base of the pillar not in contact with the electrode will be the one in contact with the membrane underneath giving it its structural stability. The second approach was using a bean-shaped electrode at the end of the metal line. This second approach increases the area that the metal has with the pillar itself but it reduces the surface area available for the pillar for its support. Both approaches have their advantages and disadvantages as a bigger surface area of the electrode at the base of the pillar would help with the contact between both materials but it reduces the area the pillar has for its stability.

The second parameter that varied across the different designs was the number of metal lines that made contact with the bottom part of the pillar. As there are three entry points on each side from which the metal lines can access the interior of the well, two different concepts were explored. The initial one was to use a single metal line to contact the base of the pillar. This design is simpler and has the least impact in the field of view of the microscope. The second approach was the implementation of 2 metal lines for the contact at the base of the pillar. The incorporation of two metal lines, rather than just one, served as a safeguard against electrode loss in the event of metal line breakage. If one of the metal lines broke during fabrication and/or handling, the presence of the second intact metal line would ensure the functionality of the electrode. A visual representation of these four distinct approaches can be found in Table 3.1.

Table 3.1: 4 different designs for contacting the base of the pillars.

Circle 1 line	Circle 2 lines	Bean 1 line	Bean 2 lines
			

3.2.2. Addition of trenches for dicing of the wafer

The final device has a layer of PDMS at the back side of the silicon wafer. This layer acts as the support membrane in which the metal lines lie and also where the Silicon pillars are released. The Muscle-on-Chip device developed by Bi/ond is diced manually because if the dicer inside the clean room at EKL is used to dice the wafer, the stress to which the PDMS is subjected is high enough that metal lines would break. This is why while manufacturing, the dicing of the chips is manual. To

improve this process, trench lines were implemented in the mask design of the turtle-shape with the pillars. The addition of these trench lines allows easier manual dicing as it gives some guidelines for the wafer to break. These trench lines are 5 μm wide and are located at the borders of each chip. This way, a mesh containing the different chips is created on the wafer which allows an easier manual dicing for the operator. A representation of these trench lines can be seen in Figure 3.2. The inclusion of these trenches further enhances the uniformity of chip sizes by facilitating a consistent dicing process. By incorporating these trenches, the operator does not need to dice the wafer by hand using a diamond-tipped been based on visual judgment, which would otherwise result in inconsistent chip sizes.

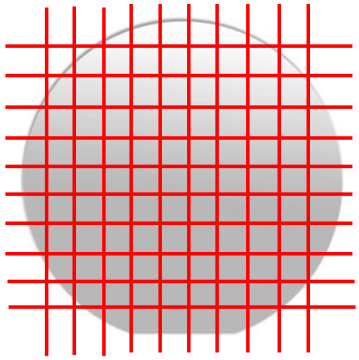


Figure 3.2: Silicon wafer with trench lines (image not to scale).

3.2.3. Encapsulation of the metal lines

One of the main considerations when implementing metal lines into any microdevice is ensuring their proper encapsulation. The metal must not come into contact with its surroundings to prevent signal loss. Moreover, it is even more critical to avoid exposing the metal to the cell culture medium if the metal is not biocompatible. Such exposure could prove detrimental to the developing tissue within the platform. Various techniques can be employed for this purpose, and in this project, silicon nitride (SiN_x) was selected as the material for encapsulating the metal lines. Several factors influenced this selection. Firstly, SiN_x exhibits a significantly slower etching rate when subjected to wet HF etching compared to silicon oxide (SiO_2) [74]. This property makes it an excellent insulator of the metal lines in this approach as wet HF etching will be employed for the release of the pillars on top of the PDMS membrane. Another main advantage of using SiN_x is that as it is a ceramic material, it can withstand higher temperatures than other materials used for the encapsulation of metal lines in microfabrication such as Polyimide (PI). Because of this property, subsequent sputtering of the metal can be performed at higher temperatures. Sputtering of metals at higher temperatures has two main advantages:

1. At higher temperatures, the sputtering process is much faster thus reducing overall fabrication time.
2. By increasing the temperature of the process, the metal atoms have more energy which allows them to arrange in a more compact manner leading to a reduced resistivity.

Protection of the metal lines at the base of the pillars

It is essential to keep in mind that certain metals, such as Al/Si, exhibit a fast etching rate when exposed to HF solutions, while others, like TiN, are less susceptible to etching of HF. Given this characteristic, proper insulation of the metal lines must exist, especially at the base of the pillars, to prevent HF from eroding the metal. SiO_2 will be etched during the HF wet etching process, which means it can not come into contact with the metal. Such contact would result in the metal being exposed to the HF solution once the SiO_2 layer is removed. This full encapsulation needs to be reflected when designing the corresponding photomask so that it is only the SiN_x layer in contact with the metal.

3.2.4. Connection of the electrodes with the outside

During the designing process of the device, there needs to be a way in which the electrodes can be accessed from the outside. This way, a signal can be introduced into the platform for the stimulation of the muscle cells. For this purpose, contact pads have been incorporated into the device design. These contact pads are made of the same metal as the one deposited for the metal lines. The function of these contact pads is to enable wire bonding between them and a printed circuit board (PCB). Two different designs for the contact pads were made. One featuring two metal lines coming out of it and one with a single metal line. To ensure minimal stress on the metal lines, they must enter the well through the turtle-shaped structures, which accounts for specific dimensions incorporated into the mask designs. Figure 3.3 provides a simplified schematic representation of these contact pads along with their corresponding metal lines.

(a) 1 metal line. **(b)** 2 metal lines.

Figure 3.3: Schematic for the design of the contact pads (image not to scale).

3.3. Process flow design

This section of the report will focus on the process flow design carried out in this project. All the device design considerations previously mentioned are taken into account for this step. Throughout the whole explanation, a 2D diagram is used so that it is easier to follow for the reader. This 2D diagram can be found in Figure 3.4.

The process starts with a 4-inch double-side polished 525 μm-thick silicon p-type (Boron doped) wafer. The first step is to create the zero layer on the back side of the wafer. This step defines the alignment markers for further alignment during the process. Then, PECVD SiO_2 is deposited on both sides of the wafer. On the front side, the thickness needs to be of 1.5 μm as it will serve as the landing layer for a later step of Deep Reactive Ion Etching (DRIE). On the back side of the wafer, the SiO_2 needs to be of 5 μm as it will serve as a hard mask for the DRIE. This corresponds to Figure 3.4b.

The PECVD SiO_2 is then etched through dry etching. On the front side, the PECVD SiO_2 is etched with the openings in which the metal would be in contact with the silicon wafer. On this side, certain squares are defined to reduce the surface contact area of the metal with the silicon pillar. On the backside of the wafer, the PECVD SiO_2 is etched to define the turtle-shape well with the pillars inside and the trench lines that will help with manual dicing later on. These steps can be seen in Figure 3.4c. Then, 200 nm PECVD SiN_x are deposited on the front side of the wafer to conform to the first insulation layer of the metal lines. Afterwards, this layer is defined through dry etching. As explained in section 3.2.3, the metal lines need to be fully encapsulated in the SiN_x so that the metal is not exposed during the final HF bath. This also applies to the base of the pillar. This can be seen as the SiN_x layer is in contact with the silicon wafer and stands between the opening for the metal to contact the silicon pillar and the SiO_2 layer. This is depicted in Figure 3.4e.

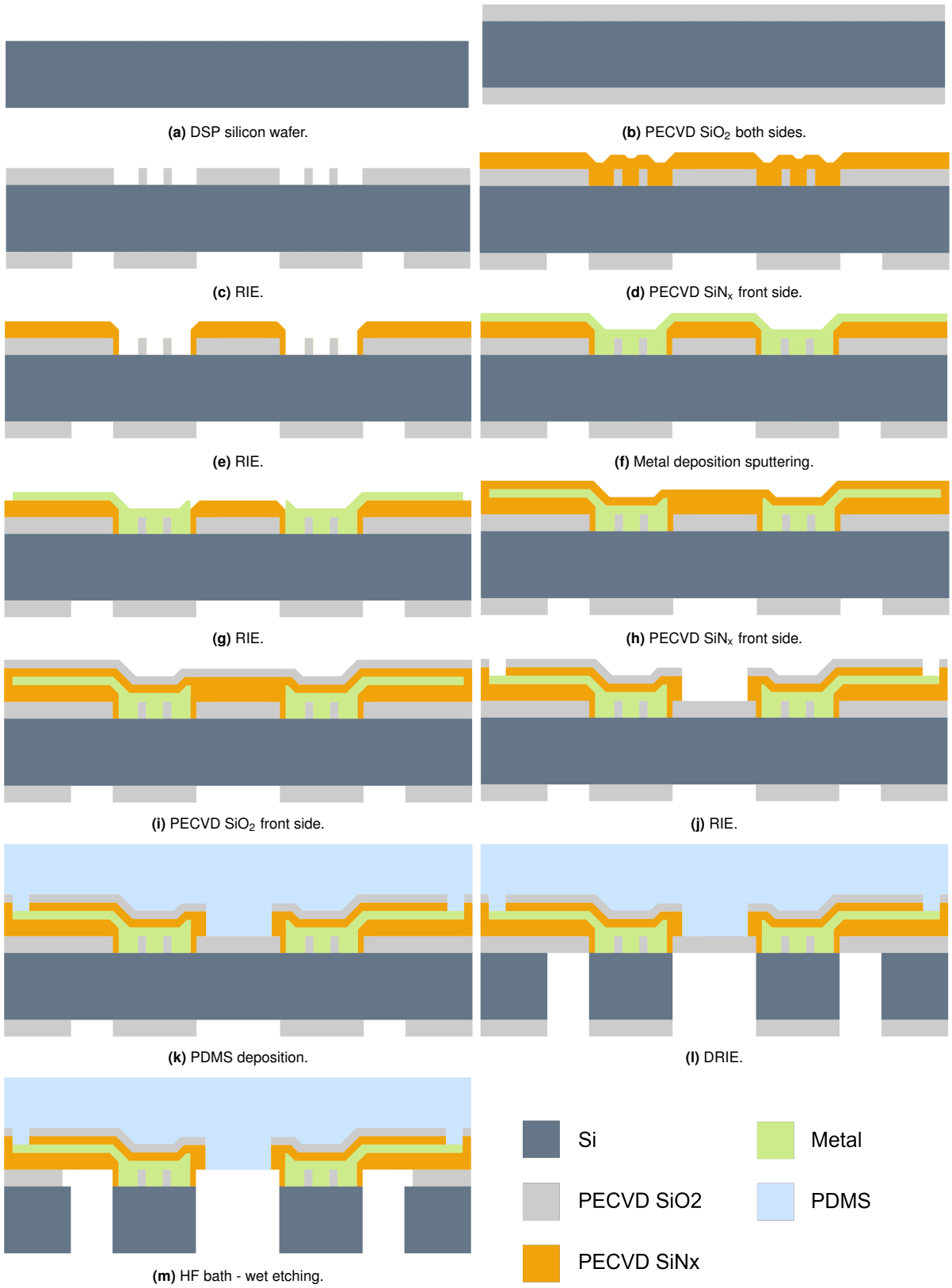


Figure 3.4: 2D process flow for the whole device.

The following step of the process is the deposition of the metal on the device. 500 nm of Al/Si are deposited through sputtering on the front side of the wafer. This process was conducted at 350 °C (Figure 3.4f). Then, the metal is dry etched to define the metal lines, the contact pads and the 4 different designs that will contact the base of the pillars (Figure 3.4g). The geometry and explanation behind all these structures are explained in section 3.2.1 and section 3.2.4. Then, 200 nm PECVD SiN_x are deposited on the front side of the wafer for final encapsulation of the metal. Afterwards, 100 nm PECVD SiO_2 are deposited on top of the SiN_x (Figure 3.4i). This is to improve the future adhesion between PDMS and the wafer.

Once this is done, the definition of the insulation of the metal lines and the openings of the contact pads is performed by dry etching both the thin layer of SiO_2 and the SiN_x as depicted in Figure 3.4j. The next step of the process is to deposit a layer of 250 μm of PDMS on the front side of the wafer (Figure 3.4k). Now the wafer is ready for the DRIE and is etched to define the turtle-shape well with the pillars inside and the trenches for dicing on the back side of the wafer. This can be seen in Figure 3.4l. Finally, the last step of the process is to release the silicon pillars on top of the PDMS membrane. This is done in an HF bath as depicted in Figure 3.4m. This concludes the process flow for the fabrication of this device.

3.4. Mask Design

Because of the process flow for manufacturing this device, certain design considerations were made to ensure the correct microfabrication of the Muscle-on-Chip at hand. These design choices were taken into account when designing the masks that would later be used during the microfabrication. The design choices are as mentioned previously in this chapter. The geometry of the electrodes at the base of the pillars, the incorporation of the trenches for the dicing, the correct encapsulation of the metal lines, and the implementation of contact pads. 6 foil masks were designed for the development of this project. All features and structures were designed with a 5 μm overlay error to counter possible misalignment during manufacturing.

In this project, foil masks were selected for use rather than glass masks. The decision to opt for foil masks was primarily based on cost efficiency, considering that this project is in the prototyping phase. This choice was made to manage the project budget more effectively. It also serves as a means to verify whether the design functions as intended. Additionally, if adjustments to the masks are required, utilizing foil masks minimizes the associated costs.

However, it is worth noting that there are certain disadvantages associated with the use of foil masks in comparison to glass masks. One limitation is that the minimum feature size achievable with foil masks is 5 μm. Given that the smallest feature in this device is also 5 μm, this limitation does not negatively impact the overall process. Another drawback of foil masks pertains to their composition, which involves ink granules. This composition can result in less defined fine features in the structures, leading to surface roughness and somewhat irregular lines. These kinds of imperfections can be appreciated under an electron microscope as will be shown in Chapter 4.

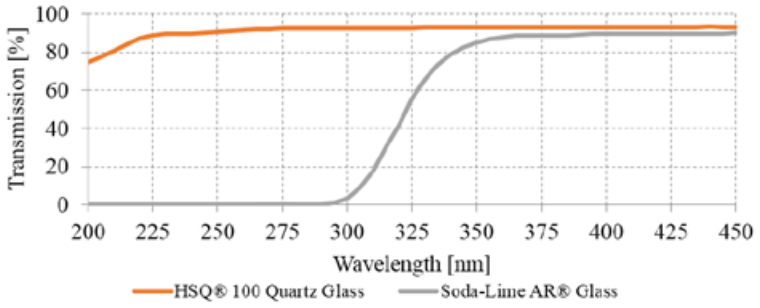


Figure 3.5: Transmission coefficient of Quartz glass and Soda-Lime glass [75].

The foil masks arrive in an A3 format. The corresponding masks need to be cut and to be used, attached to a glass holder with tape on its corners. This glass holder was made of quartz glass instead of Soda-Lime. This is because both materials have different transmission coefficients. This transmission coefficient is dependent on the wavelength that is employed during the exposure of the photomask. Soda-Lime glass has a very low transmission coefficient at wavelengths around 300nm (depicted in Figure 3.5). This is the range in which the mask aligner in the clean room works therefore, to avoid any complications regarding the exposure of the photoresist, a quartz glass holder was selected.

Even though foil masks present several advantages, I advise using glass masks in future work. Their price compared with foil masks outweighs the complications and final features that are translated into the devices.

The next chapter will describe the fabrication process, what were the challenges encountered and how were they overcome.

4

Device fabrication

In this chapter the microfabrication steps will be described and explained. The final process flow for the fabrication of the device will be detailed at first followed by the results of such process. The challenges encountered at different steps of the process will be explained afterwards. The whole process flow chart can be found in Appendix D with all the details regarding each single step.

4.1. Process steps

In this section of the chapter, the final optimized process flow will be detailed. The process starts with a 4-inch double-side polished 525 μm-thick silicon p-type (Boron doped) wafer. This process applies methods to both sides of the wafer thus it is of extreme importance to keep track of which side of the wafer each process step needs to be done on. The first step of the fabrication is the creation of the zero layer. In this step, the alignment markers are etched on the silicon wafer on the back side. This fact means that most of the process steps in this flow will be backside alignment. For doing this, the EVG120 coater station is used and 1.4 μm of photoresist (Megaposit SPR3012) are deposited. Afterwards, the wafer is exposed using the ASML PAS5500/80 automatic wafer stepper with energy set to 140 mJ/cm^2. Then, the wafer is developed using the EVG120 Coater station in a single-puddle developer. Finally, the alignment markers are dry etched in the tool Trikon Omega 201 plasma etcher. At the end of this sequence, the photoresist is stripped using oxygen plasma in the Tepla Plasma 300 and is cleaned in the standard Si cleaning line at EKL. This standard cleaning line consists on 5 different steps:

1. Immerse the wafers for 10 minutes at room temperature in a 99% concentration HNO_3 solution.
2. Rinse the wafers using the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
3. Immerse the wafers for 10 min at a temperature of 100ºC in a 69% concentration HNO_3 solution.
4. Repeat step number 2. Rinse the wafers using the Quick Dump with the standard program until the resistivity is 5 MΩ.
5. Use the Avenger Ultra-Pure 6 to rinse and dry the wafers.

Next step is to deposit SiO_2 on both sides of the wafer. On the front side, the thickness needs to be of 1.5μm as it will serve as the landing layer for a later step of Deep Reactive Ion Etching (DRIE). On the back side of the wafer, the SiO_2 needs to be of 5 μm as it will serve as a hard mask for the DRIE. Both oxide layers are PECVD SiO_2 layers deposited by the Novellus Concept One PECVD reactor. The thicknesses of the SiO_2 on both sides are measured thanks to the Woollam Ellipsometer to make sure that the right thicknesses of the material have been deposited. This corresponds to Figure 4.1a. Then,

on the front side of the wafer, 3.1 μm of photoresisit AZ ECI 3027 [76] are deposited on top. The front side of the wafer is then exposed using the SUSS MicroTec MA/BA8 mask aligner using the foil mask named **Oxide 1** with soft contact back-side alignment (as the alignment markers are in the back side of the wafer). The photoresist is exposed to 500 mJ/cm^2 and afterwards, the wafer is developed in the EVG120 in a single-puddle. The PECVD SiO_2 on the front side of the wafer is then etched with dry etching in the DryTek Triode 384T plasma etcher using the standard oxide etch recipe. Afterwards, the photoresist is stripped in the Tepla Plasma 300 and cleaned in the standard Si cleaning line.

On the back side of the wafer, the one with 5 μm of SiO_2, 3.1 μm of photoresist AZ ECI 3027 are deposited. Then, the wafer is exposed using the SUSS MicroTec MA/BA 8 mask aligner using the mask named **Oxide Turtle**. This mask not only defines the well and its pillars but also the trench lines added to the design of the device to help with the later manual dicing of the wafer. In this case, 865 mJ/cm^2 energy is required for the correct exposure of the photoresist using the hard-contact front side alignment recipe. Afterwards, a triple-puddle recipe is performed in the EVG120 Coater in the developing station. Once the photomask is in place on the front side of the wafer, the PECVD SiO_2 is etched inside the Drytek Triode 384T plasma etcher using once again the standard silicon oxide etching recipe. Then, the photoresist is stripped from the wafer using the Tepla Plasma 300 and then cleaned in the standard Si cleaning line. These steps can be seen in Figure 4.1b.

(a) PECVD SiO_2 deposition. **(b)** RIE of PECVD SiO_2.

Figure 4.1: PECVD SiO_2 definition.

Afterwards, the first layer of the insulation needs to be deposited. PECVD 200 nm of silicon nitride (SiN_x) are deposited on the front side of the wafer using the Novellus Concept One PECVD reactor (Figure 4.2a). Later on, 3.1 μm of photoresisit AZ ECI 3027 are deposited on top using the EVG120 Coater. The front side of the wafer is then exposed in the SUSS MicroTec MA/BA8 mask aligner using the foil mask named **SiN - 1** with soft contact back-side alignment and with energy 500 mJ/cm^2. Afterwards, the wafer undergoes a step of developing in a single-puddle recipe. The PECVD SiN_x is then etched using the Drytek Triode 384T plasma etcher using the standard SiN_x etch recipe. Next, the photoresist is stripped using the Tepla Plasma 300 and the wafer is then cleaned in the standard Si cleaning line. Till this point, we are step seen in Figure 4.2b.

(a) PECVD SiN_x deposition. **(b)** RIE of PECVD SiN_x.

Figure 4.2: First layer of insulation definition.

Before metal deposition, the best contact possible is wanted between the metal and the silicon wafer. Therefore, a Marangoni process was made. This process gets rid of the native oxide layer forming on top of the silicon exposed and also creates a protective layer that ensures that no native oxide will form on the silicon surface over a limited amount of time. This Marangoni process is as follows:

1. Immersion in 0.55% HF at ambient temperature is performed for 4 minutes.
2. Rinsing process using deionized water (DI) water is performed.
3. Lastly, the wafers are subjected to some isopropyl alcohol (IPA) gas that creates a temporal protective layer preventing the silicon from oxidizing.

The following step of the process is the deposition of the metal on the device. 500 nm of Al/Si are deposited on the front side of the wafer using the TRIKON SIGMA 204 sputter coater. This process was done at 350 °C (Figure 4.3a). Then, 3.1 μm of photoresisit AZ ECI 3027 are deposited on top using the EVG120 Coater. The front side of the wafer is then exposed in the SUSS MicroTec MA/BA8 mask aligner using the foil mask named **Metal** with soft contact back-side alignment and with energy 500 mJ/cm^2. Following the exposure, the wafer is developed using a single-puddle recipe in the EVG120 developing station. Afterwards, the exposed Al/Si is dry etched using the Trikonn Omega 201 plasma etcher. The final steps in this part of the process are first to strip the photoresist using the Tepla Plasma 300. Afterwards, the wafer needs to undergo a cleaning process but as we have deposited metal on top of it, it now needs to go through the clean line devoted to Green Metals. This cleaning process consists on the following steps:

1. Immerse the wafers for 10 minutes at room temperature in a 99% concentration HNO_3 solution.
2. Rinse the wafers using the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
3. Final step is to use the Avenger Ultra-Pure 6 to rinse and dry the wafers.

(a) Al/Si sputtering deposition. **(b)** RIE of Al/Si.

Figure 4.3: Definition of metal lines.

Up to this point, the process wafer is at step seen in Figure 4.3b. To check for the correct deposition of the metal, a test was performed.

Continuity of the metal line after deposition

Continuity of the metal line after its deposition was one of the main concerns regarding this process. If the metal lines are not continuous, then contact between the contact pads and the base of the pillars is not possible. The continuity of the metal line could be affected by the height step of the metal at the base of the pillar. It needs to make a step of around 1.7 μm (1.5 μm of SiO_2 + 200 nm of SiN_x). To check for this continuity, a simple resistance measurement was performed along the metal lines using a voltmeter. One of the probes was put on the contact pad and the second probe was put at either the circle or bean shape at the end of the metal line underneath the base of the pillar as depicted in Figure 4.4. 3 different measurements on 3 different chips were conducted on each one of the 4 different designs. The results can be seen in Table 4.1.

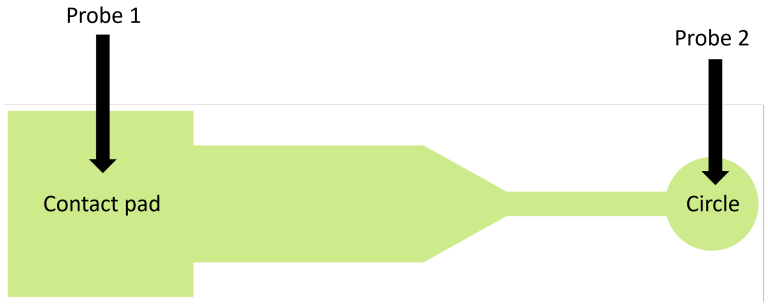


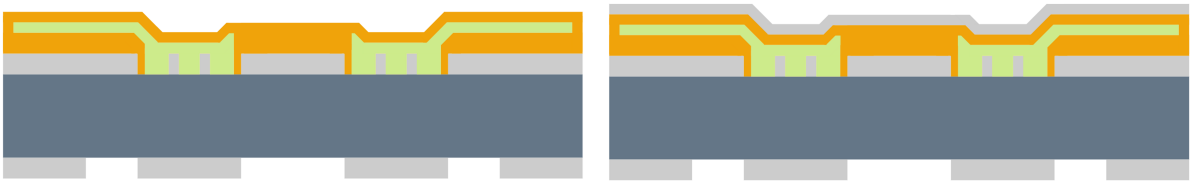
Figure 4.4: Schematic for testing continuity of metal.

Table 4.1: Results for the Continuity of the metal test.

Design	Measurement 1 (Ω)	Measurement 2 (Ω)	Measurement 3 (Ω)
Circle single line	15	11.6	10.5
Bean single line	11.3	11.1	12.0
Circle double line	8.5	9.5	11.4
Bean double line	8.7	8.0	8.3

A control measurement was also made in which the probes where placed where there was no metal at all and the voltmeter could not give any value. Based on the results obtained, it can be determined that the metal line was continuous as the resistance obtained is very small and lies in between the expected values (which should be below the hundreds of Ω). It is also interesting to note that the structures with 2 metal lines present a lower resistance as in their case there is more surface area in which the signal can be transmitted.

Once the metallization is complete, the second layer of insulation needs to be deposited to fully encapsulate the metal lines. 200 nm of PECVD SiN_x are deposited on the front side of the wafer using the Novellus Concept One PECVD reactor. The wafer is now at step seen in Figure 4.5a. Once the encapsulation is complete, a final thin layer of 100 nm of PECVD SiO_2 is deposited on top of the PECVD SiN_x (Figure 4.5b). This is to improve the future adhesion between PDMS and the wafer.



(a) PECVD SiN_x deposition. **(b)** PECVD SiO_2 deposition.

Figure 4.5: Deposition of the final encapsulation layers.

After this very thin layer of oxide is deposited, the definition of the encapsulation of the metal lines needs to be done. For this purpose, the wafer is coated on the front side with 3.1 μm of photoresist AZ ECI 3027 in the EVG120 coater. Afterwards, it is exposed using the SUSS MicroTec MA/BA8 mask aligner to the foil mask named **SiN - 2** with 500 mJ/cm^2. Then, the wafer is developed with a single-puddle recipe in the EVG120 developing station. Once the photoresist mask has been defined, the wafer is etched in the Drytek Triode 384T plasma etcher using the standard silicon nitride etch recipe. As both the etching of SiO_2 and SiN_x use similar chemistry, only one recipe is needed for the full dry etching of both layers. Then, the photoresist is stripped using the Tepla Plasma 300 and the wafer is cleaned in the Green Metals cleaning line. Now the wafer is in step seen in Figure 4.6 where the metal lines are defined and encapsulated on top of the front side of the wafer. It is also important to note that at this step, not only the metal lines are defined but also the openings on the contact pads.

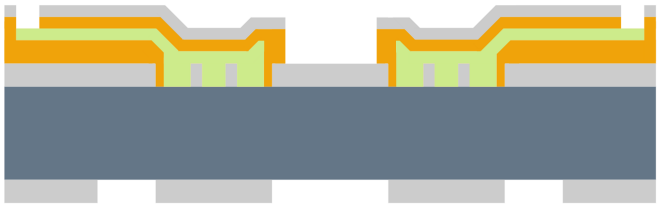


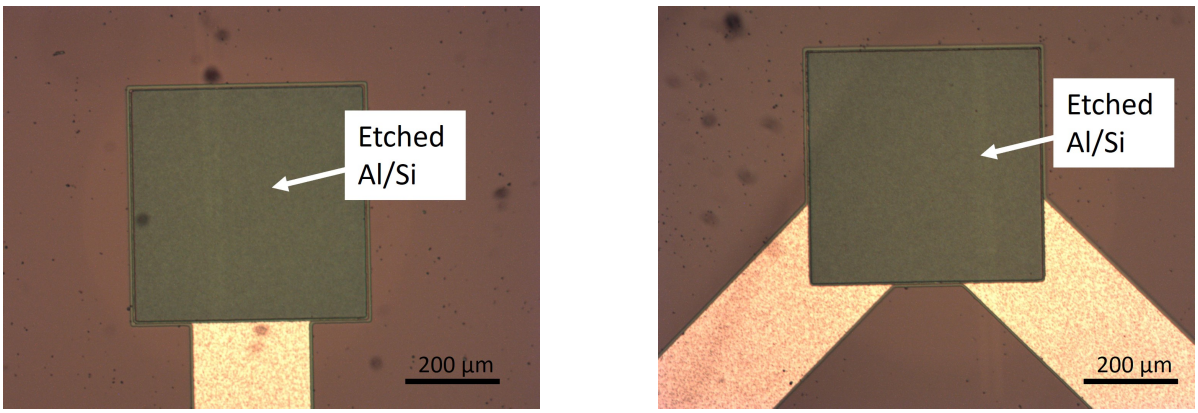
Figure 4.6: Final layer of insulation definition and contact pad opening.

The definition of the insulation presented one of the major challenges, as detailed below.

Definition of the insulation

One of the most challenging steps of the process was the definition of the insulation for the metal lines. SiN_x was chosen as the insulation material for the metal lines based on its low etching rate in HF and its biocompatibility [77]. The metal lines lie on top of a layer of SiO_2 that acts as a landing layer for the DRIE process. The challenge arises because the chemistry used for the dry etching of SiN_x and SiO_2 are very similar. As a consequence, the recipe used to etch uniformly SiN_x also etches SiO_2 in a non-uniform manner. At the beginning of the project, an initial layer of only 1 μm of SiO_2 was designed as the landing layer for the DRIE process. This thickness was more than enough to act as a landing layer. The problem came when the insulation of the metal lines needed to be defined at step seen in Figure 4.6. If the wafer is overetched, then there will be a non-uniform layer that acts as landing layer for the DRIE. This means that some locations of the wafer would have a thinner layer of SiO_2 which could be etched during the DRIE exposing the PDMS which is undesired for the machine. On the other hand, if the wafer is not etched enough, even a few nm of SiN_x can lead to a poor adhesion of PDMS to the wafer which makes it unsafe to perform the DRIE.

The first attempt to solve this problem was to introduce an intermediate step in which almost all 400 nm of SiN_x was etched using dry etching and then use phosphoric acid (H_3PO_4) for wet etching the last remaining nanometers of SiN_x. H_3PO_4 has a much higher etching rate on SiN_x than SiO_2 thus initially it seemed like a good idea. The main problem regarding this approach is that the contact pads with Al/Si were also exposed to this wet etching and the metal was completely removed from the contact pads. Therefore this was not a plausible solution. An image of the wet etched contact pads can be seen in Figure 4.7.



(a) Etched contact pad 1 metal line.

(b) Etched contact pad 2 metal lines.

Figure 4.7: Etching of the contact pads after H_3PO_4 bath.

The second approach was to try to find the exact amount of time needed during the dry etching in the Drytek Triode 384T plasma etcher. The idea was to remove all the SiN_x from the desired locations but to have a SiO_2 layer thick enough so that it could be used as a landing layer. For this approach, several dummy wafers were prepared with a stacked layer of 1 μm of SiO_2, 400 nm of SiN_x and a final layer of 100 nm of SiO_2. Then, these wafers were introduced inside the Drytek Tryode 384T plasma etcher with different etching times. Every time a wafer came out of the plasma etcher, the thicknesses at different points of the wafer were measured thanks to the Reflectometer. At the end of the process, it was stated that the optimum time was 1 minute and 5 seconds. The main problem with this approach was that the etching rate was not consistent enough thus in some wafers all the SiN_x was removed but in some wafers, there were still a few nm of SiN_x left. This led to poor adhesion of the PDMS on the wafer. This could be appreciated when trying to peel off the PDMS using some tweezers, as can be seen in Figure 4.8 where the PDMS was removed easily.

Due to the failure of the previous attempts, it was decided to increase the thickness of the SiO_2 layer that acts as the landing layer and increase the time for the etching up to 1 min and 12 seconds. This way, even if there were some overetch, the thickness of that landing layer would be sufficient.

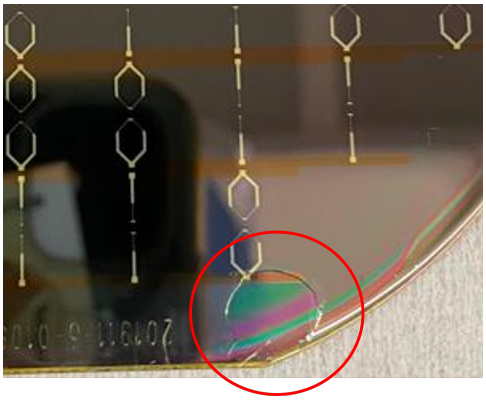
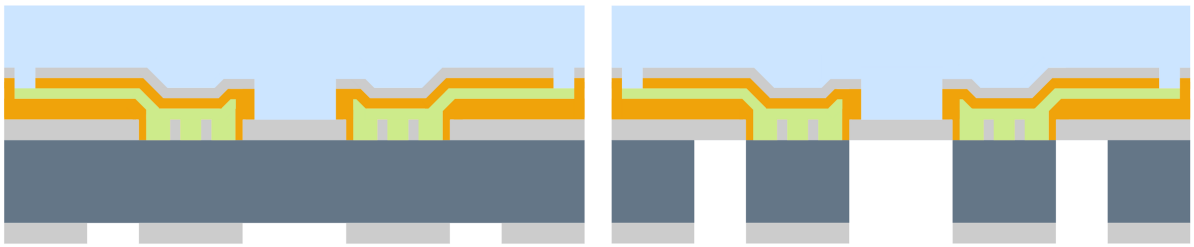


Figure 4.8: Poor adhesion of PDMS to the wafer.

Once the metal lines are fully encapsulated and the contact pad openings are defined, a layer of 250 μm of PDMS is deposited on the front side of the wafer (Figure 4.9a). Now the wafer is ready for the DRIE which will create the well and the pillars inside of it. The process of DRIE needs to be performed on the back side of the wafer where the hard mask of 5 μm of PECVD SiO_2 is in place. Because of this, the side of the wafer in contact with the chuck of the machine, the front side, has PDMS. PDMS is not a material that can be used as a substrate for the chuck of the machine thus a carrier wafer needs to be employed. This carrier wafer consists of a single-side polished wafer, which already contains some dicing lines, on top of which at least 200 nm of Al/Si had been deposited. Al/Si can not be etched by the DRIE, so it makes it a perfect stopping layer in case the wafer is fully etched alongside the PDMS membrane. The reasoning behind those dicing lines is to avoid the creation of a vacuum between the process wafer and the carrier wafer which would make it very difficult to separate both wafers after the process. As the DRIE will be performed to etch through the entire thickness of the wafer, the landing layer of such a process needs to be thick enough. This is to prevent the DRIE from reaching the PDMS which could result fatal for the machine itself. That is the reason why the front side of the wafer has a layer of 1.5 μm of SiO_2. The DRIE is performed on the back side of the wafer in the Rapier Omega i2L DRIE etcher. This step can be seen in Figure 4.9b.



(a) PDMS deposition. **(b)** DRIE.

Figure 4.9: Deposition of PDMS and DRIE.

Tapering of the pillars

After the DRIE, some of the wafers presented a certain condition. In some of them, the metal electrodes at the base of the pillars were exposed. This phenomenon occurred because the pillars were thinner at the base than at the top. In microfabrication, this phenomenon is called "reverse tapering". The reduction of the pillars at the base was not accounted for in the device design which was only accounting for misalignment errors. An example of this phenomenon can be appreciated in Figure 4.10 where the arrows indicate where the exposure of the metal is. The base of the pillar is smaller than the electrode itself thus the metal electrode would be exposed to the inside of the well.

This tapering causes a major issue for the device. The main drawback is that as the metal electrodes are exposed, the metal will be etched when performing the HF bath (Figure 3.4m). If this is the case, then the connection between the Si pillar and the exterior would be lost and no signal would be able to be transmitted. One of the reasons for this tapering can be attributed to the low thermal

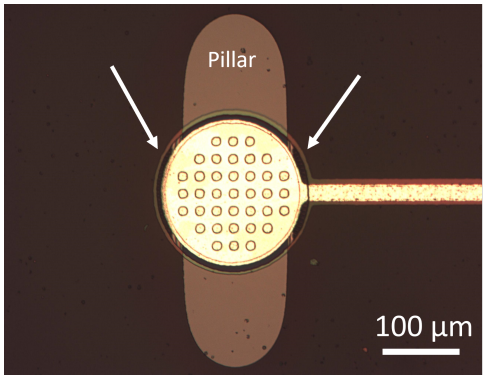


Figure 4.10: Example of Tapering of the pillar. Arrows indicate exposure of the metal.

dissipation that the wafer has. On the front side of the wafer (the part of the wafer in contact with the chuck of the machine), there is a layer of PDMS which has very low thermal conductivity. This makes the wafer heat up after every cycle of the Haber-Bosch process [78] used during the DRIE. This increase in temperature can be one of the causes of such reverse tapering as the etching is not homogeneous due to the temperature difference. Another reason that could affect the tapering of the pillars is the conditioning of the chamber. It is of great importance that the conditions of the chamber are controlled and are standard so that the process can be reproducible.

To solve the problem regarding the heating of the wafer, stopping the process at certain cycles was proposed. This would provide time for the heat to dissipate. Because of the low thermal conductivity of PDMS, it would mean that the process wafers would need to be stopped for long periods of time. This approach was not pursued as it would mean even longer process times at this step which is already time-consuming. Owing to this fact, the problem regarding the conditioning of the chamber was tackled. Before undergoing the DRIE on the process wafers, certain recipes were used on some dummy wafers so that the conditioning of the chamber could be tuned. At the end of these recipes on the dummy wafers, certain cleaning steps of the chamber were also performed. This way the conditioning of the chamber was optimal for the processing of the wafers.

The results of this conditioning of the chamber are evident to be sufficient for avoiding the tapering of the pillars as can be seen in the final results in Figure 4.22. In this case, the full electrode remains underneath the base of the pillar thus not being exposed to the inside of the well. In this manner, the metal electrodes are protected against the HF bath.

When the wafer has been etched through DRIE, the process wafer is separated from the carrier wafer. Then, the last step of the process remains. The release of the Si pillars on top of the PDMS membrane. For this to occur, the wafer undergoes a bath of HF 5% concentration. This process wet etches the SiO_2 that was used as a landing layer for the DRIE but also the SiO_2 used as a hard mask on the back side of the wafer. This final step can be seen in Figure 4.11 and concludes with the fabrication of the chips containing the Muscle-on-Chip devices with 3D microelectrodes integrated.

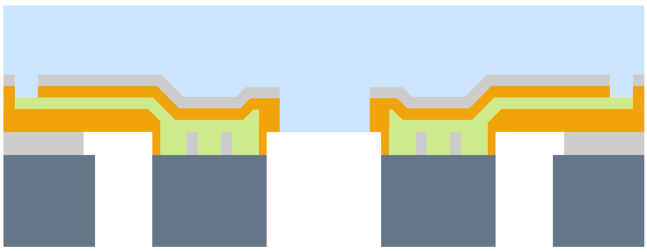


Figure 4.11: 2D schematic after HF bath.

4.2. Results

The results of the process previously detailed and explained will now be presented. In Figure 4.1, a representation of the etching of the layers of SiO_2 both on the front side and on the back side of the wafer can be seen. The front side of the wafer shows the openings in which the metal will contact the Si pillar. It has some squares in an array to reduce the surface area of contact between the metal and the Si pillar. An optical image of the final results can be seen in Figure 4.12.

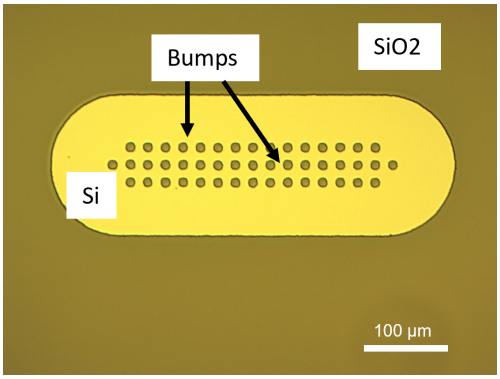


Figure 4.12: Wafer after the dry etching of the SiO_2 (front side).

The back side of the wafer has the SiO_2 layer that will serve as a hard mask for the DRIE. This oxide mask has both the turtle-shape well, with the two pillars inside of it, and the trenches that will help with the dicing of the wafer. An optical microscope image of part of this structure can be seen in Figure 4.13.

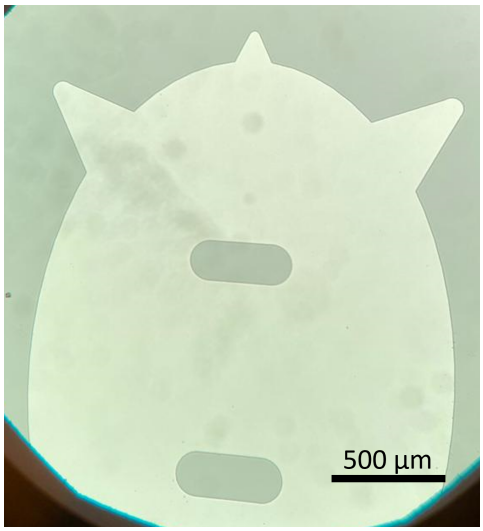
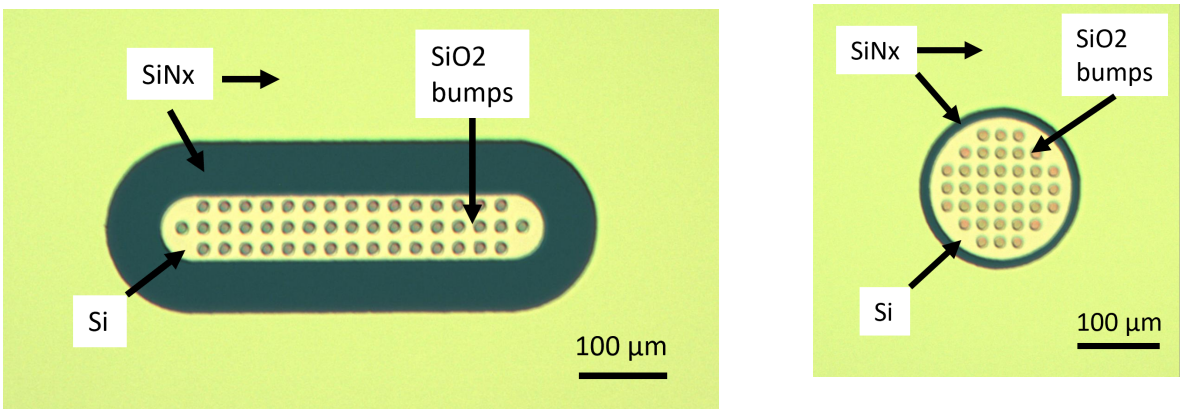


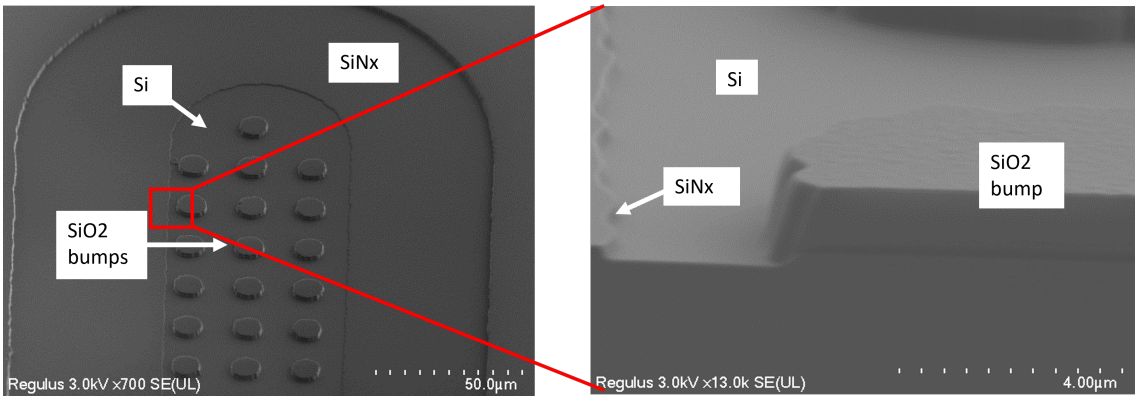
Figure 4.13: Turtle shape structure.

Figure 4.2 represents the etching of the first layer of insulation made of SiN_x. As mentioned in section 3.2.3, it is of great importance that the insulation layer of SiN_x is the only layer in contact with the metal and not the SiO_2. This is to avoid etching of the metal during the HF bath. In Figure 4.14 an optical image of how the first insulation layer is deposited can be appreciated. Note that indeed, the SiN_x is the one that delimits the contact openings for the metal to interact with the base of the pillar. This way, during the HF bath, the metal is always covered by the insulation layer of SiN_x. This structure can be better appreciated under a scanning electron microscope (SEM) where the cross section can be obtained in order to see the stack up layer of such process as seen in Figure 4.15.

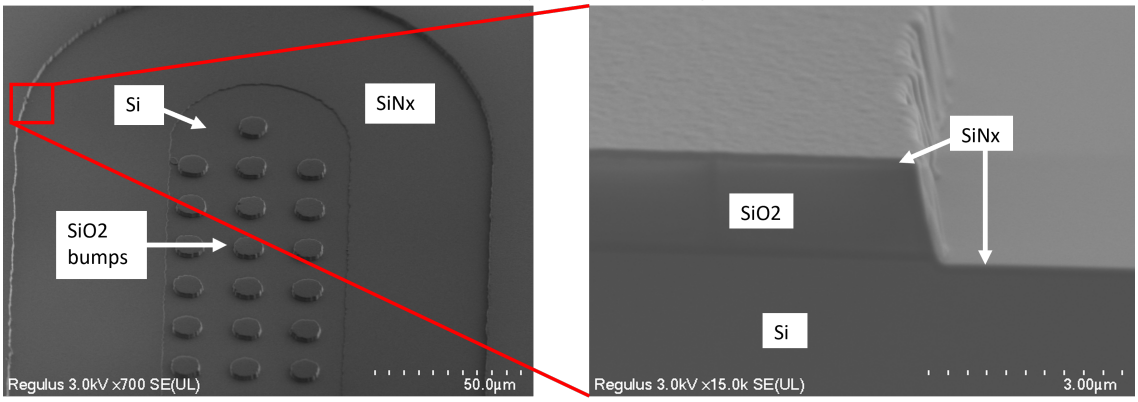


(a) Bean shape. **(b)** Circle shape.

Figure 4.14: Result of first insulation layer definition (front side).



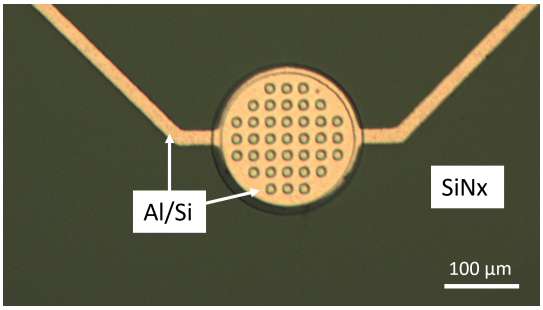
(a) SEM image with the SiO_2 bump.



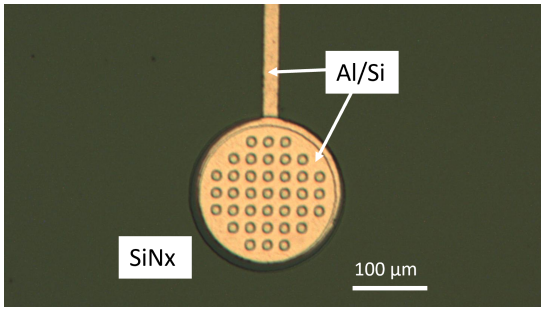
(b) SEM image with the SiO_2 and SiN_x stack up layer.

Figure 4.15: SEM images of the first insulation layer.

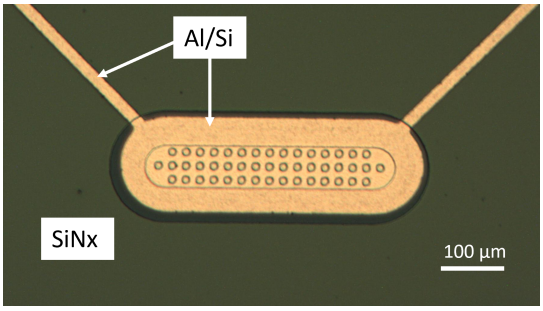
After the first insulation layer is done, metal deposition and definition are performed (depicted in Figure 4.3). At this moment the contact pads are also defined as they are made from the same material. The result of such metal deposition and definition can be seen in Figure 4.16 regarding the four different designs. Concerning the contact pads, there are two different designs. One design with a single metal line and the other one with two metal lines. An image of such contact pads can be seen in Figure 4.17.



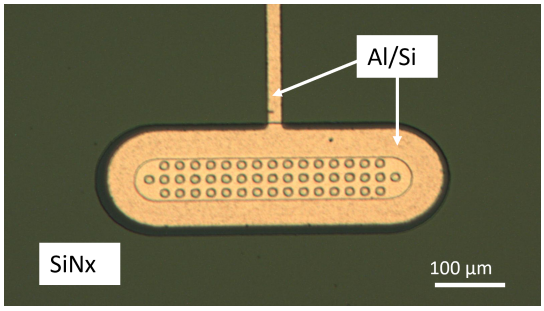
(a) Circle double line.



(b) Circle single line.

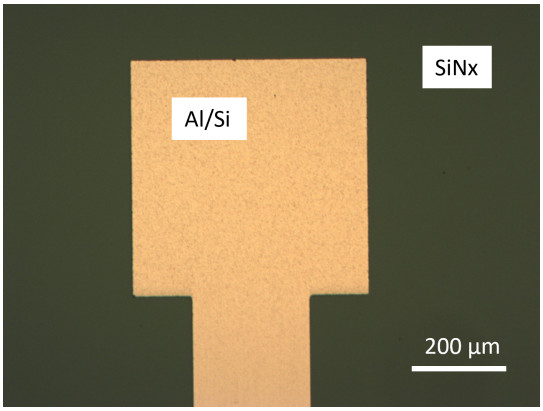


(c) Bean double line.

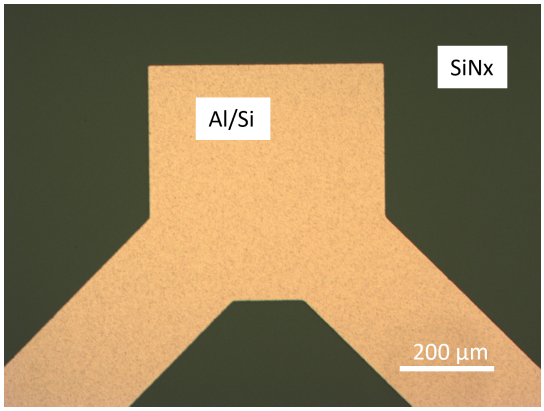


(d) Bean single line.

Figure 4.16: Result of metallization of the device at the base of the pillar (front side).



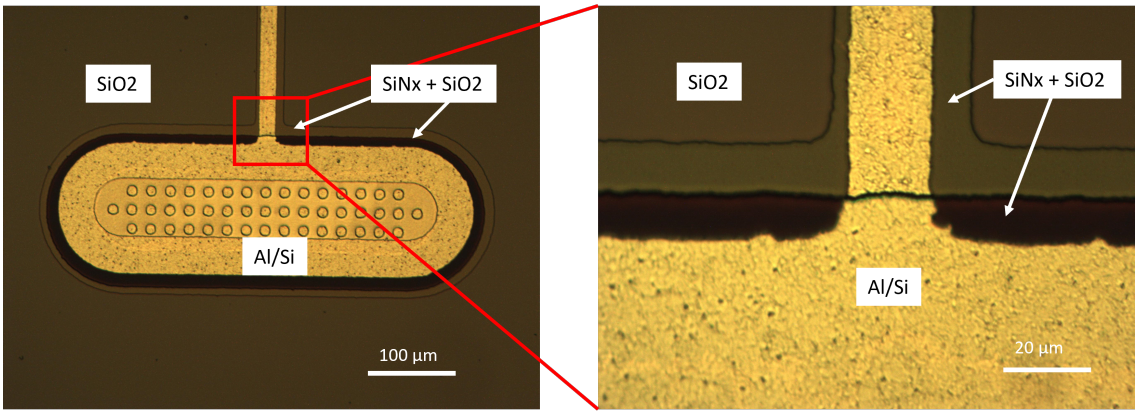
(a) Single line contact pad.



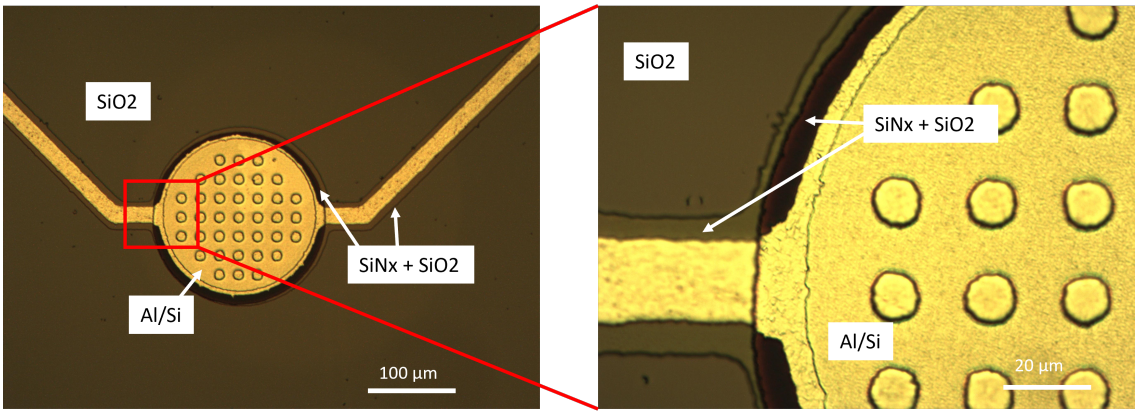
(b) Double line contact pad.

Figure 4.17: Contact pads after the metal etching.

Once the metallization has been completed, the encapsulation of such metal needs to be finalized. This is the step depicted in Figure 4.6. The result of such etching can be seen in Figure 4.18 where two examples are used. One with the design of bean single line and another one with circle double line design. The lines seen at the junction between the electrode and the metal line are due to the step difference in the layers. This is better appreciated in the SEM images that follows. The contact pads were also encapsulated with the SiN_x and the SiO_2 as seen in Figure 4.19.

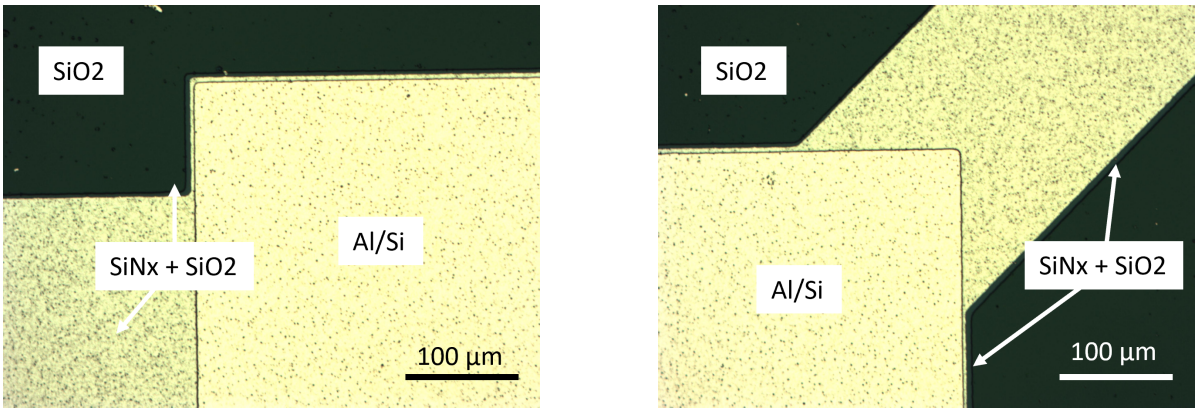


(a) Bean single line structure.



(b) Circle double line structure.

Figure 4.18: Structures after the final encapsulation of the metal.

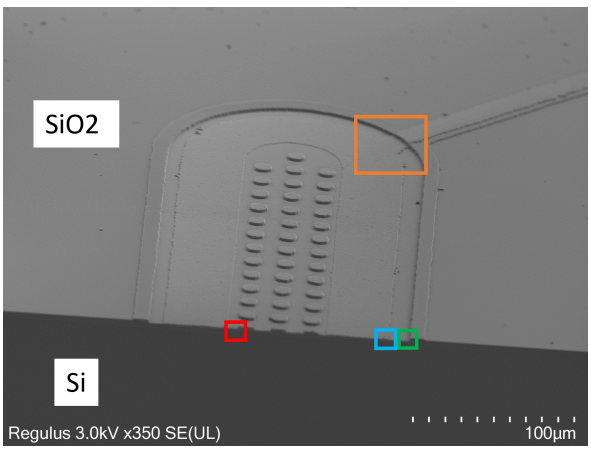


(a) Contact pad single line.

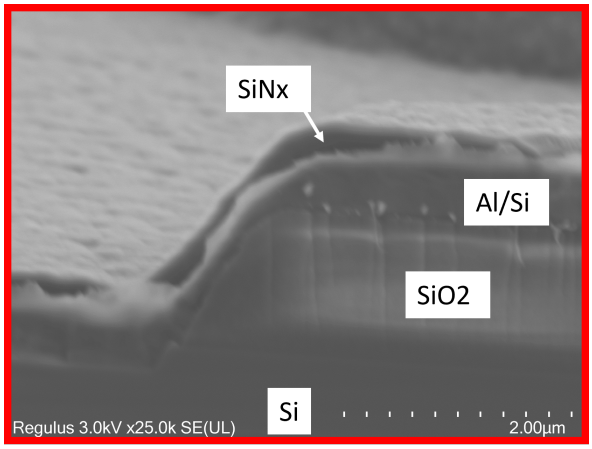
(b) Contact pad double line.

Figure 4.19: Contact pads after the metal etching.

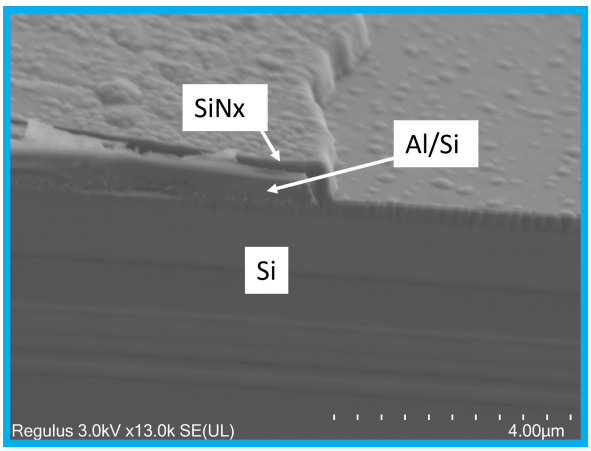
This stack up layer is interesting to see under the SEM microscope where the different layer materials can be appreciated thanks to a cross-section image. Note that these images were taken before the deposition of the thin layer of SiO_2 (which improves adhesion to the PDMS membrane). The base of the pillars can be seen in Figure 4.20. It is of great interest to see the different layers at the SiO_2 bumps as it can give us an idea of how the metal is continued at the interface with the Si pillar. It is also important to see how the metal encapsulation is done underneath the pillar in order to make sure that the metal is fully covered by SiN_x and therefore protected for the HF bath.



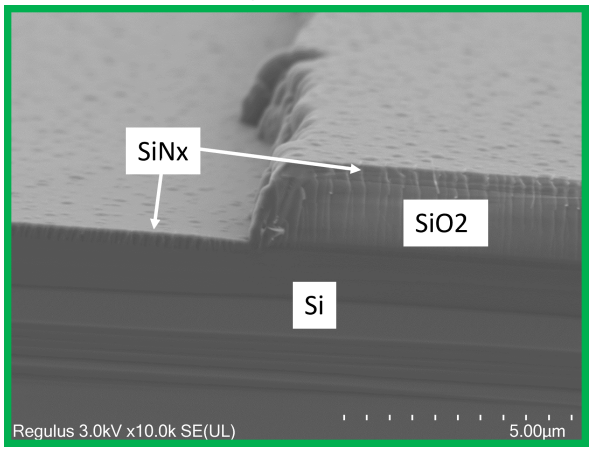
(a) General overview after SiN_x-2 etch.



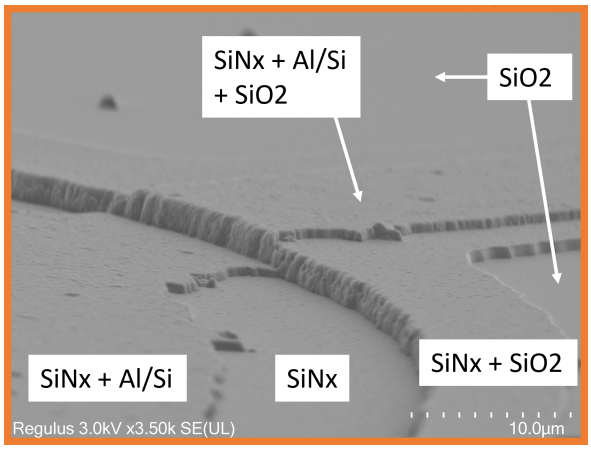
(b) Bump after SiN_x-2 etch.



(c) Inner part of electrode after SiN_x-2 etch.



(d) Outer part of electrode after SiN_x-2 etch.



(e) Metal line after SiN_x-2 etch.

Figure 4.20: SEM images of a bean double line structure after SiN_x etch for full encapsulation of the metal.

The encapsulation of the contact pads can be seen in Figure 4.21. When imaging the cross-section at the contact pad, a gap in between the insulation layer and the metallization was noticed. This is depicted in Figure 4.21. This air gap does not represent an issue for the device but it should be taken into account in case there is something wrong during the microfabrication.

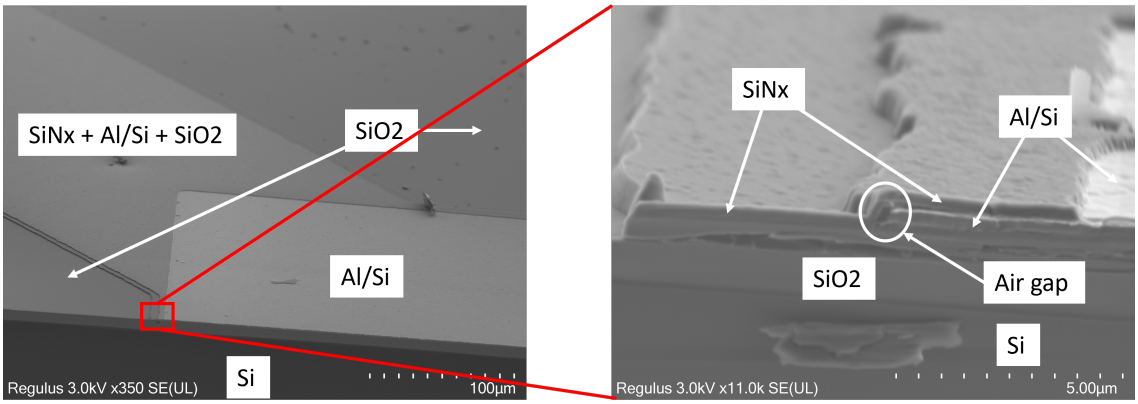
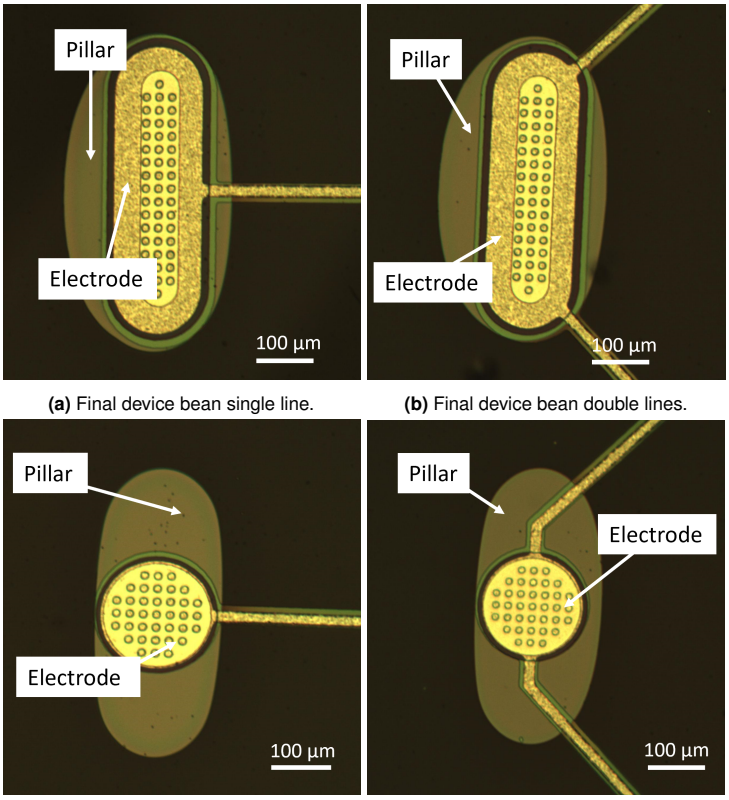


Figure 4.21: SEM image of the contact pad after SiN_x etch for full encapsulation of the metal..

After the encapsulation of the metal and its definition, the layer of PDMS is deposited. Afterwards, the wafers are etched using DRIE and finally, they undergo an HF bath to release the pillars on top of the PDMS membrane. The final result is the contact at the base of the Si pillar with a metal electrode. Examples of the results at the base of the pillars are shown in Figure 4.22 with all the different 4 designs. SEM images were also taken to show the final result of the turtle-shape well with the pillars inside. The two approaches of both a single and double metal line can be seen in Figure 4.23.



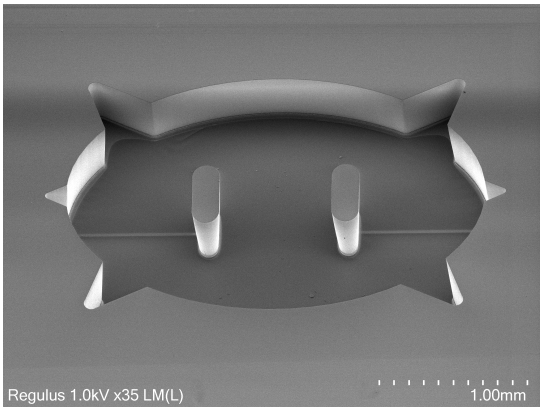
(a) Final device bean single line.

(b) Final device bean double lines.

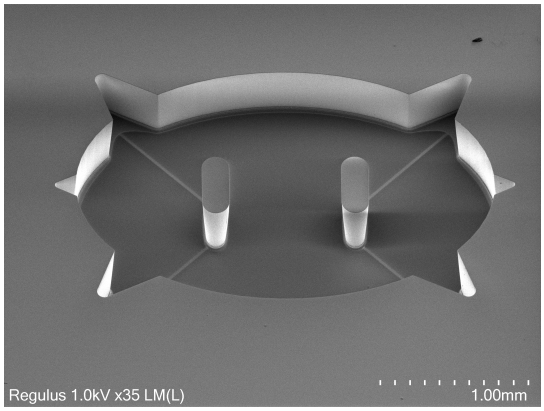
(c) Final device circle single line.

(d) Final device circle double lines.

Figure 4.22: Result at the base of the pillars of the final devices.



(a) Final device with one metal line.



(b) Final device with two metal lines.

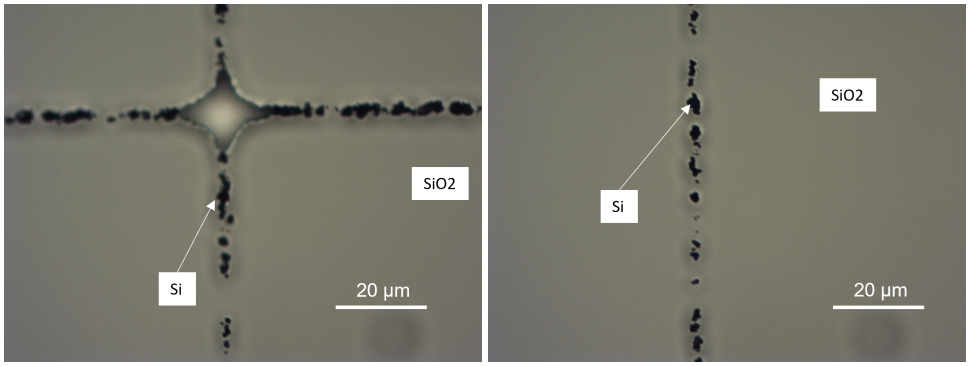
Figure 4.23: SEM images of the final device.

4.3. Challenges

Throughout the fabrication process, several challenges were encountered. These challenges were solved in different ways. This section of the chapter will focus on which were these challenges and how were they addressed.

4.3.1. Definition of the trenches

During the step depicted in Figure 4.1, for the back side of the wafer, the same parameters were used as in the previous mask used for the front side. 500 mJ/cm^2 soft-contact front side alignment and developed with a single-puddle. After this, the wafer was put inside the Drytek Triode 384T plasma etcher for 13 minutes but the trenches were not properly defined. An example of such trenches can be seen in Figure 4.24.



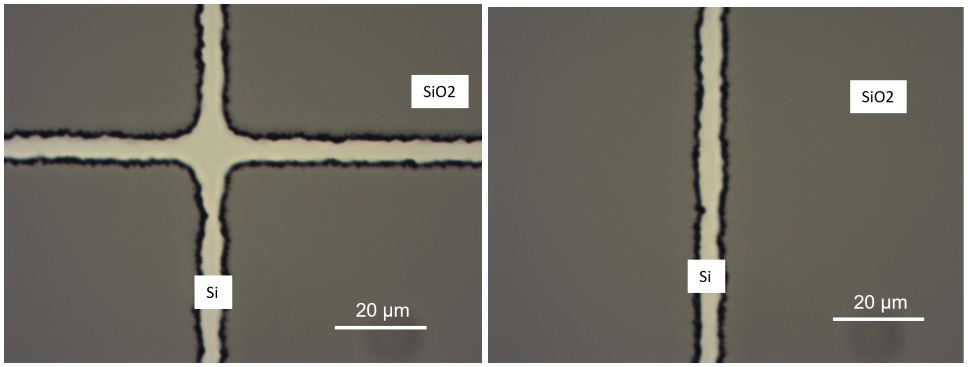
(a) Intersection of trenches.

(b) Vertical trench.

Figure 4.24: Result of the trenches after dry etching of the SiO_2.

The reasoning behind this poor etching of the SiO_2 is that the trench lines were not properly transferred on the photoresist mask. The photomask used in this step is a foil mask which has a maximum definition of 5 μm. As the trench lines are exactly of this thickness, the granules of ink used for the creation of the foil mask interfere with its profile at small features. The incorrect etching of such trenches in the Hard mask of SiO_2 could contribute to that after the DRIE, these trenches might not help during the manual dicing but actually be detrimental to the design. These incorrect trenches could lead to the creation of individual points on the surface that could serve as breaking points on the wafer and crack the wafer in an undesired manner.

To improve the transfer of the profile from the photomask on top of the photoresist, different approaches were made. The dose of the exposure was increased up to 865 mJ/cm^2 and instead of using soft-contact, hard-contact was employed. As the trench lines were so thin, a single-puddle recipe was not enough for the correct development of the photoresist in these structures because the developer was not able to penetrate deep enough. A reduction of thickness of the photoresist layer was also not an option as it was necessary to ensure that the photoresist would not be etched during the dry etching of the SiO_2 in the Drytek Tryode 384T plasma etcher. Therefore, a triple-puddle was necessary for the correct transfer of the profile from the foil photomask to the photoresist. The results can be seen in Figure 4.25 where the trenches etched on the SiO_2 hard mask can clearly be appreciated.



(a) Intersection of trenches. **(b)** Vertical trench.

Figure 4.25: Result of the trenches after dry etching of the SiO_2 optimized.

4.3.2. Teflon walls

One of the results of employing the Haber-Bosch process during DRIE is the deposition of a thin layer of Teflon on the side of the walls. This Teflon layer is also deposited on the walls of the pillars as a passivation layer [78]. Teflon is an insulator, thus if this layer remains on top of the walls of the Si pillars, they will be insulated from the medium. This thin layer of Teflon is therefore a major issue if the Si pillars are wanted to be used as electrodes.

Teflon can be removed using oxygen plasma [79][80]. There are different tools at our disposal inside the clean room. The main limiting factor when choosing which tool to employ is the PDMS membrane on top of the front side of the wafer. PDMS can not be exposed to high temperatures as its properties, especially its elasticity, change drastically [81]. One of the tools that can be used is the Tepla Plasma 300 which is typically utilized for the stripping of the photoresist. Unfortunately, the recipes used in this machine are set to high temperatures, above 100 °C. This temperature would affect the PDMS membrane which as a result could lead to the rupture of the metal lines that lie on top.

The Rapier Omega i2L used for the DRIE can also create an oxygen plasma in its chamber. The temperature of this oxygen plasma can be controlled and can be set to a lower temperature such as 25 °C. The PDMS layer would not be affected by this plasma due to its low temperature making this approach ideal for our purposes. Therefore, once the DRIE has been done on the wafers, a final step in which oxygen plasma is applied to the chamber is performed. This way the Teflon layer is removed from the surface walls of the pillars exposing the Si to the medium inside the well. This was checked and confirmed later by Bi/ond's process engineer.

4.3.3. HF bath

The final step of the process is a 5% concentration HF bath to remove the landing layer of SiO_2 used during the DRIE. This way the pillars are released on top of the PDMS layer. The first problem that was encountered at this step was determining the times for each one of the steps of such an HF bath. This process requires the preparation of 3 different stations. The first one is the solution of 5%

concentration of HF. There is also a station of Triton-X and a final station with DI water for rinsing. The purpose of the station with Triton-X is to increase the wettability of the wafer, especially inside the well. The whole process of such a bath is as follows:

1. First, all the wafers/chips are submerged in the Triton-X solution for 5 minutes.
2. In the second step, the wafers are transferred into the 5% bath for 4 minutes.
3. The final step is to rinse with DI water the wafers/chips for 10 minutes.

This process is repeated at least two times. After each iteration, visual inspection is done to check if all the SiO_2 has been removed from inside the well. The way it can be seen is if there are any refraction at the bottom of the well. If that is the case, it means there is still some SiO_2 remaining, thus a new iteration is needed. After this process, there may be some HF residues on the wafers/chips. As HF is an extremely dangerous chemical, correct handling is essential for safety. To remove these possible residues of HF on the wafers/chips, the samples are introduced in a vacuum oven and left there overnight.

Although these were the initial parameters used in such a process, in previous tests it was seen that the time of the HF bath was too long as it led to also the etching of the metal lines. For that reason, the times of such steps were tuned. In the first iteration of the process, instead of performing a bath for 4 minutes, 3 minutes were employed. In case there was still some oxide left, in the next iteration, the HF bath was reduced to 2 minutes and 30 seconds. In case there is more SiO_2 left, smaller times should be used for the next iteration although it was not needed in this case.

When performing this step of HF bath, two other main concerns arise. The first one relates to the stability of the pillars. By removing the SiO_2 landing layer, some support of these pillars is also removed and could result in the detachment of such pillars from the PDMS layer. In the case of this project, the pillars are not only released on top of the PDMS layer but they also have some electrodes and metal lines at their base. The existence of these electrodes at the base of the pillars could also affect the stability of the pillars either making them more prone to detach or to remain. The second concern that arises refers to the stability of the metal lines. When the SiO_2 landing layer is removed, some stresses could act on the PDMS membrane which could lead to the breakage of the metal lines. It is also a possibility that if the metal lines are broken, this breakage could open a crack in which the HF could come into contact with the metal and etch it leading to the loss of that metal line.

For the study regarding these two concerns, several chips that were properly etched after the DRIE were selected. These chips had metal electrodes underneath the base of the pillars thus the metal was protected from the HF bath, so no tapering was seen in them. These two concerns were studied for the four different designs. The number of chips that were able to be recovered from the process wafer is as follows: 6 chips with the design of a circle with 1 metal line, 7 chips with circle geometry and 2 metal lines, 5 chips with bean geometry and 1 metal line, and finally, 5 chips with bean geometry with 2 metal lines.

The whole wafer has 52 chips. As 23 chips remained, it resulted in a yield of **44.23%** after the DRIE etching.

Stability of the pillars

All the chips were processed using the previously mentioned tuned process steps for the HF bath. A total of 23 chips were studied. As each chip has two Si pillars in its well, there are a total of 46 Si pillars. Following the HF bath treatment, all the chips were examined to determine whether the pillars had been detached or not. The results yielded a positive outcome as all 46 pillars remained intact and attached to the PDMS membrane, indicating that they remained within the chip wells. Therefore, in terms of pillar stability, there is a yield of **100%**.

These results were compared to Bi/ond's process for the fabrication of the MUSbit device. In this process, there were always several pillars that detached from the PDMS membrane. The loss of these pillars made the devices unusable as the muscle cells would not have any place for anchoring

and development. The results from this test even suggest that the addition of the metal electrodes underneath the base of the pillars could also improve pillar stability as in this case, none of the pillars detached from the PDMS membrane.

Survival of the metal lines

After the chips had undergone the HF bath and thus the release of the Si pillars on top of the PDMS membrane, the chips were examined to check whether the metal lines had survived. As the device needs both pillars to be connected to metal lines, only those chips that had all their metal lines intact were taken into consideration. The results can be seen in Table 4.2.

Table 4.2: Results for the survival of the metal lines test.

Design	Initial chips with intact metal lines	Final chips with intact metal lines	Yield
Circle single line	6	3	50%
Circle double line	7	3	42.86%
Bean single line	5	1	20%
Bean double line	5	2	40%

During the inspection of the devices, different cracks appeared in the metal lines. In one of the cases, a whole metal line was broken and detached from its place. This can be seen in Figure 4.26 where one of the metal lines of the device was completely detached and then misplaced somewhere else in the well.

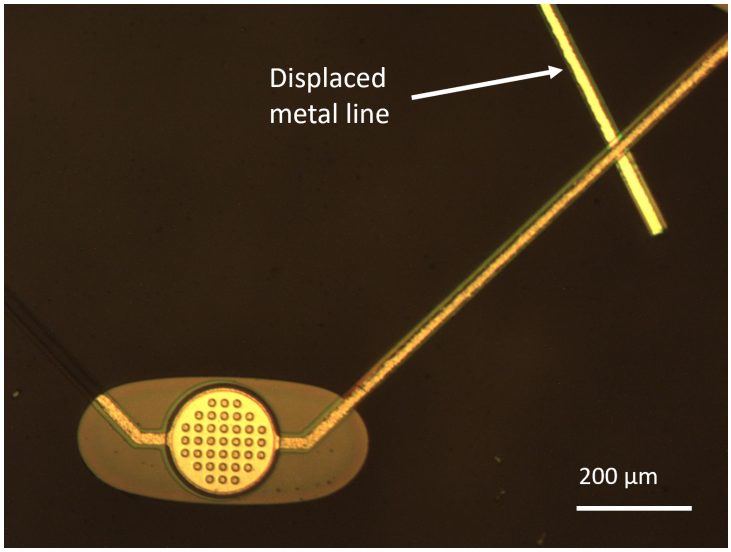
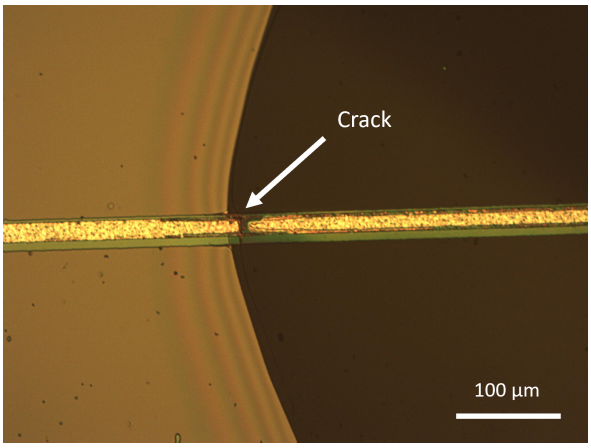


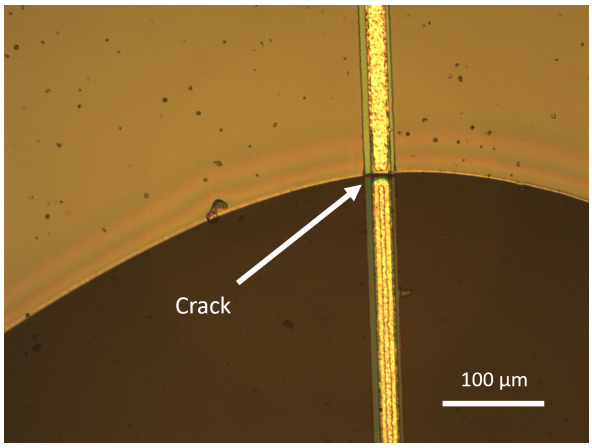
Figure 4.26: Displaced metal line after HF bath.

Other cracks appeared in some of the chips. These cracks mainly appeared at the edge of the pillars or at the edge of the well. These cracks can be seen as pointed out in Figure 4.27. The appearance of these cracks also led to the contact of metal with the HF which consequently etched the metal at some points. The etching of the metal can also be appreciated under an optical microscope as shown in Figure 4.28. One interesting case is depicted in Figure 4.27d in which one of the metal lines is broken but the other one remains intact. This is an example of the functionality of the design with two metal lines as that electrode is indeed still functional. The cracks at the edge of the well are correlated to the bad definition of the turtle shape after the DRIE. In the case of cracks underneath the base of the pillars, they can be attributed to when the pillar is released on top of the PDMS membrane. This process may exert some stress at the edges which can cause the cracking of the metal.

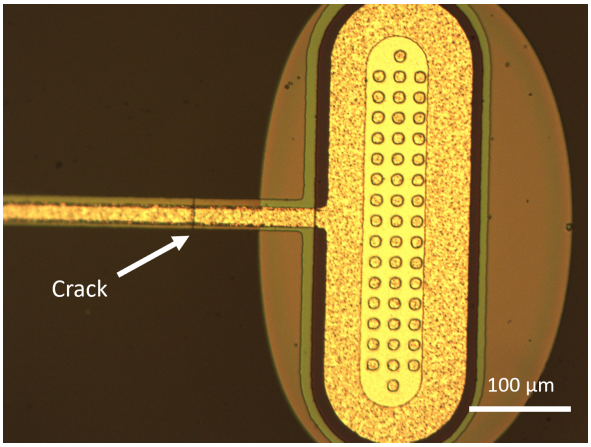
The next chapter will describe the electrochemical characterization performed on the final devices obtained after the fabrication.



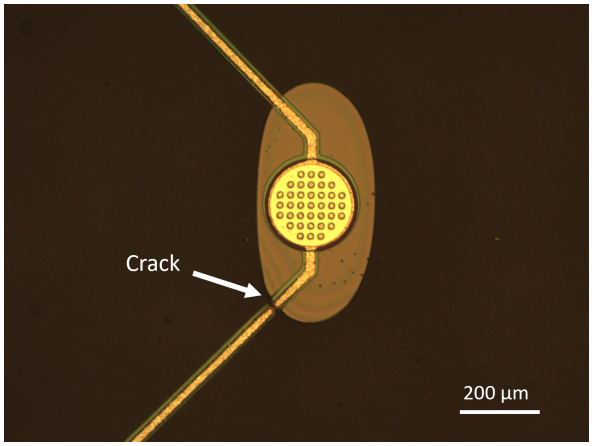
(a) Line crack at the edge of the well.



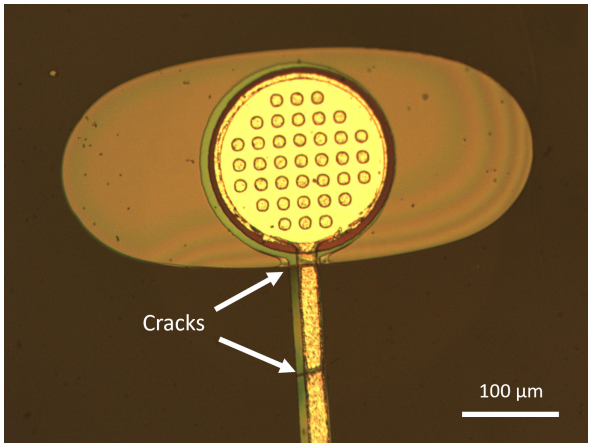
(b) Line crack at the edge of the well.



(c) Bean shape single line crack.

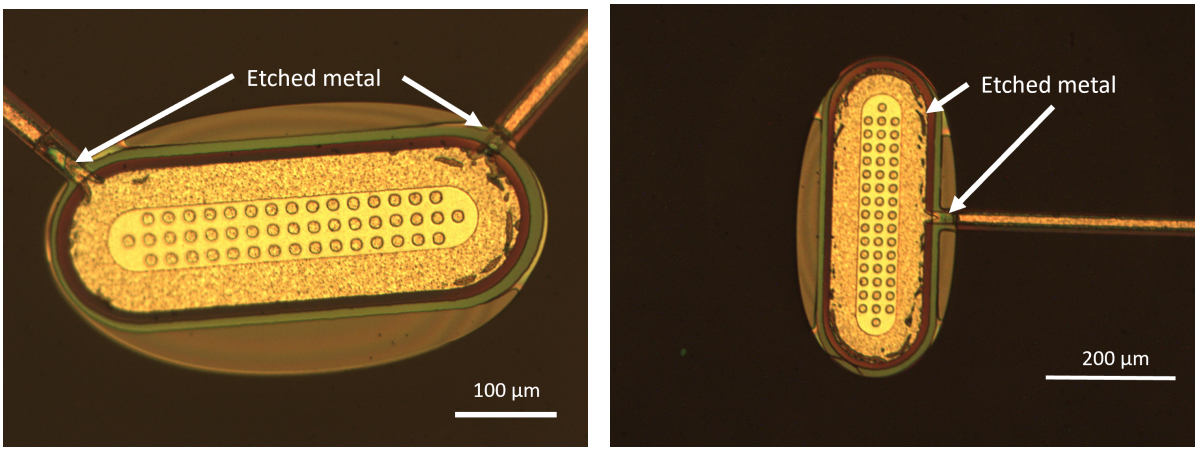


(d) Circle double line crack.



(e) Circle single line crack.

Figure 4.27: Optical images of the base of the pillars after HF bath.



(a) Bean double line metal etched.

(b) Bean single line metal etched.

Figure 4.28: Examples of metal etched because of cracks.

5

Electrochemical Characterization

This chapter will focus on the work done once the device has been fabricated. Once the electrodes are in contact with the pillars at their base, the electrochemical characterization of such electrodes can be performed. This refers to electrochemical impedance spectroscopy (EIS). Cyclic voltammetry (CV) and voltage transient (VT) measurements were also scheduled in this project but due to some complications, they could not be performed. Before this characterization, preparation of the samples is needed so that the electrodes can be accessed and therefore measured. At the end of this chapter, a section regarding the use of the final devices for some testing performed at Bi/ond will be shown.

5.1. Experimental set up

To perform the electrochemical characterization, a three-electrode cell set up was used. The electrochemical measurements were performed with a potentiostat, Autolab PG-STAT302N from Methrom. A three-electrode cell set up is composed of the following:

1. A working electrode in which the measurements are being taken (WE).
2. A reference electrode that has a known potential (RE).
3. A counter electrode (CE).
4. An electrolyte through which the signal is transmitted.

The reference electrode must be non-reactive so that the data can be compared with existing literature but most importantly because no reaction is desired at the RE. For this project, a silver/silver chloride (Ag/AgCl) electrode was used as the RE. The sizes of the different electrodes are also of great importance. The counter electrode must be considerably larger in surface compared to the working electrode being studied [82]. In this project, a platinum wire was used as the CE. The electrolyte chosen for this experiment was a phosphate-buffered saline solution (PBS) as it is the standard electrolyte used in this type of measurements

It is also important to determine the positioning of these electrodes during the electrochemical analysis. The distance between the working electrode and the counter electrode must be significantly bigger than the distance between the working electrode and the reference electrode. The reasoning behind this is that the applied signal is being supplied to the electrolyte through the working electrode and then it must flow and travel through the electrolyte till it flows through the counter electrode to close the circuit. Therefore, the closer the reference electrode is to the working electrode the more accurate the measurements. A schematic of the arrangement of these components is shown in Figure 5.1.

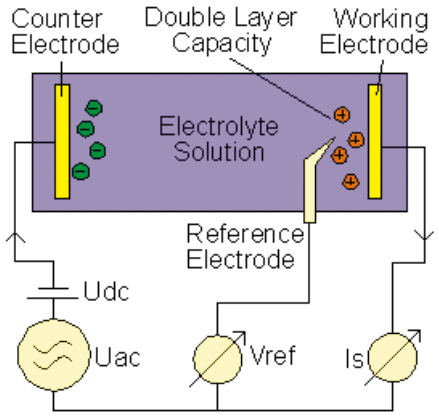
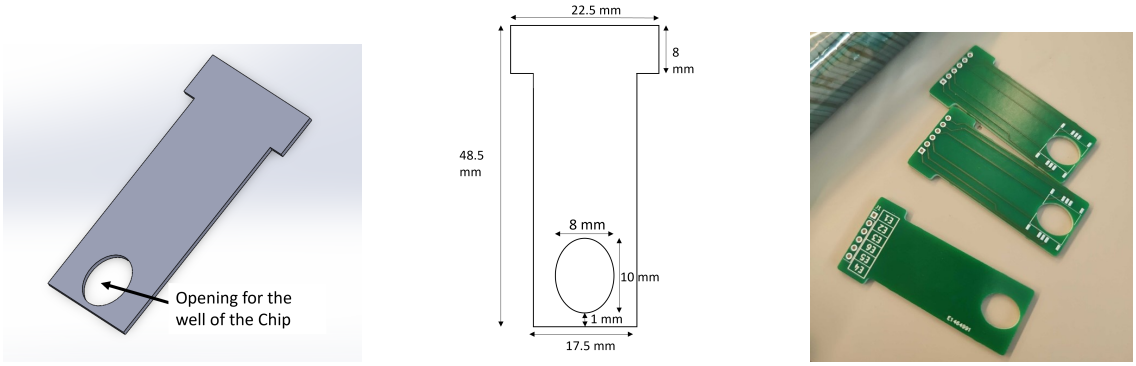


Figure 5.1: Schematic representation of a 3 electrode cell set up [82].

All the electrodes need to be submerged in the electrolyte for the measurement to take place. As this is the case, the chip must be submerged inside the electrolyte. For this purpose, a specially designed printed circuit board (PCB) was made. As the positioning of the electrodes themselves is also of great importance, a 3D-printed flask cup was designed to hold the different electrodes in the same position during each measurement. This minimized the variability between measurements related to the positioning of the electrodes.

5.1.1. PCB Design & 3D-printed flask cup

As the chip needs to be submerged inside the electrolyte, the PCB to which it will be attached and wired bonded also needs to fit inside the flask of the solution. The positioning of the chip is also important, thus a way of implementing this PCB in the flask at the same position every time must be done. Because of these requirements for the design, a final T-shape was chosen for the mechanical design of the PCB. This way the upper part of the T-shape PCB can be used for holding the PCB in place while the rest can be submerged inside the electrolyte. The top part of the PCB will also have some contacts to which some cables can be soldered for the connection with the potentiostat. The contact pads are on one side of the chip whereas the opening of the well is on the other side. Therefore, an opening for the well of the chip must be done on the PCB so that the well can be in contact with the electrolyte and the pads can be wire bonded to the PCB's contact pads. A schematic of such a design can be seen in Figure 5.2 alongside its dimensions. The thickness of the PCB is standard (2 mm).

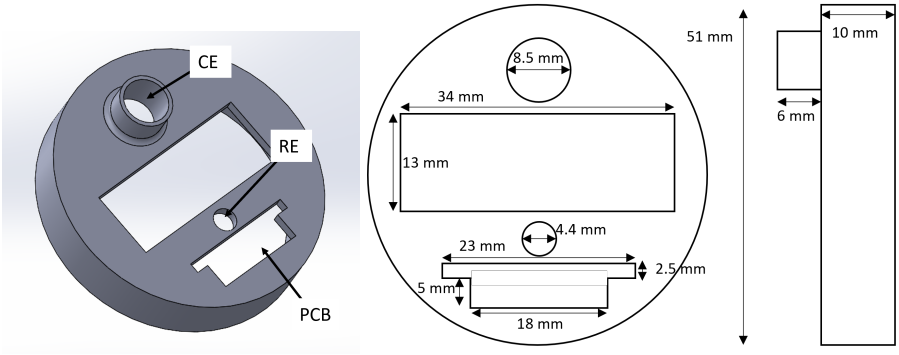


(a) PCB design schematic. **(b)** Dimensions of the PCB. **(c)** Final PCBs.

Figure 5.2: PCB design.

Regarding the positioning of the different components of the 3 electrode-cell set up, a 3D-printed flask cup was designed to hold everything in the same position during each measurement. The flask cup has an aperture in which the T-shape PCB can be inserted and secured. It has a small hole

next to the holder of the PCB so that the reference electrode can be introduced close to the working electrode. The holder for the counter electrode was made taller to make sure that it would go vertically inside the electrolyte. A schematic of such a 3D-printed flask cup can be seen in Figure 5.3. Finally, a representation of how these two components interact with each other can be seen in Figure 5.4.



(a) 3D printed holder schematics. **(b)** 3D printed holder dimensions.

Figure 5.3: 3D printed holder design.

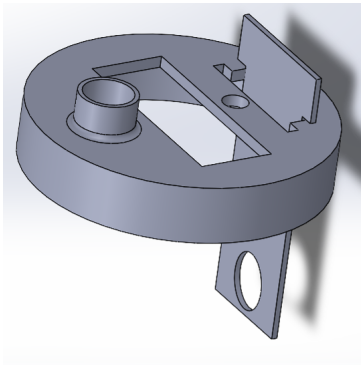


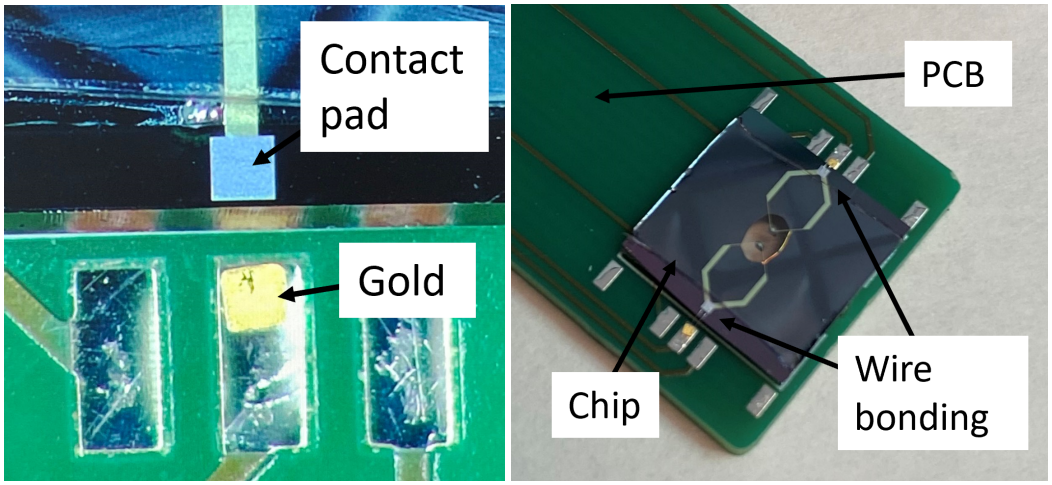
Figure 5.4: Assembly of both the PCB and the 3D printed holder.

5.1.2. Wire bonding

When the fabrication process is completed, the wafer is diced manually to recover the chips. This is done with ease thanks to the trenches already implemented in the design of the device. The wafer is diced manually by just applying small pressure on the sides of the wafer so that it can be broken following the lines of the trenches. The PDMS on top of the contact pads is cut with a scalpel and removed using tweezers so that the contact pads are exposed.

The chips are then ready to be attached to the PCB. This is done thanks to an adhesive which is placed around the opening in the PCB. It is important to remember that the contact pads of the chip, which are on the front side of the wafer, need to be aligned with the contact pads of the PCB. This makes the opening of the well to be inside the opening of the PCB.

The contact pads of the PCB were made of nickel and not of gold. This fact made it difficult to wire bond the device to the PCB with the available tools. To solve this issue, small gold pads were soldered on top of the nickel pads of the PCB and then the wire bonding was performed. As the contact pads were big enough, two wire connections were made in each of the contact pads to ensure a connection. This can be seen in Figure 5.5.

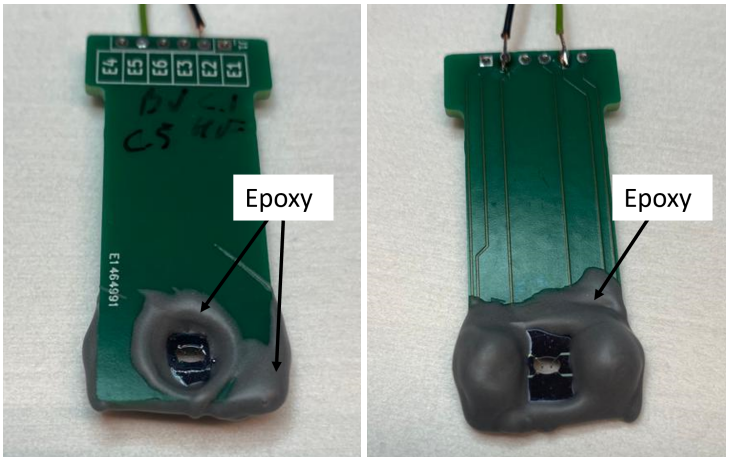


(a) Soldered gold pads for wire bonding. **(b)** Wire bonding of the chip to the PCB.

Figure 5.5: Wire bonding of the chip to the PCB.

5.1.3. Sample preparation

Now that the chips are wire bonded to the PCBs, proper insulation of such connection must be performed. Hot glue was deposited on top of the pads with a glue gun to insulate the wire bonding. This way the connection would be covered and insulated from the electrolyte. To make sure that no electrolyte was in contact with the contact pads, epoxy was applied over the hot glue and in the interior part of the well at the junction between the chip and the PCB. This way, the contact pads are in principle fully insulated from the electrolyte and the only possible way for the signal to be transmitted is through the well containing the Si pillars. An example of such insulation with both the epoxy and the hot glue can be seen in Figure 5.6.



(a) **(b)**

Figure 5.6: Encapsulation of the contact pads. a) Front side. b) Back side.

To be able to connect the PCB to the potentiostat, cables were soldered at the contact pads on the top part of the PCB. This way, using crocodile clamps, all the different electrodes needed for the correct measurement could be connected with the measurement tool.

The final set up for the measurements with the 3-electrode cell can be appreciated in Figure 5.7. The measurements were performed inside a grounded Faraday cage to minimize the disturbances from other equipment inside the laboratory. This way accurate measurements are ensured.

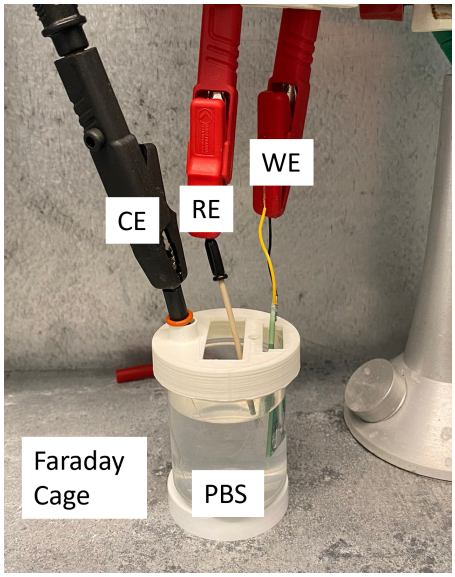


Figure 5.7: 3 electrode cell set up inside a Faraday cage.

5.2. Electrochemical Impedance Spectroscopy

Electrochemical impedance spectroscopy (EIS) is a robust method employed to examine the interfacial characteristics of the electrode surface. This technique involves the investigation of the system's response to the application of a low amplitude AC signal. EIS is performed by imposing a sinusoidal excitation voltage with a specified low amplitude (ranging from 0.01 to 0.2 V), between the working and the counter electrode. The measurements are conducted over a wide range of AC frequencies that can vary from less than 1 mHz to greater than 1 MHz. This allows the study of both slow and fast kinetic processes [83]. The combination of the measurements over the frequency range provides the final results of the spectrum for the impedance of the electrode.

Impedance, in contrast to resistance, is distinct in that resistance in DC circuits strictly follows Ohm's law, illustrated in Equation 5.1 where E is the potential (V), I is the current (A) and R is the resistance (Ω). The electrochemical cell's response exhibits a pseudo-linear behavior, introducing a phase shift as the current responds to the sinusoidal pattern signal at the applied frequency. Consequently, the excitation signal is depicted as a function of time as seen in Equation 5.2 where E_t is the potential at time t, E_0 is the amplitude of the signal and ω is the radial frequency where $\omega = 2 \cdot \pi \cdot f$, being (f) the applied frequency.

$$E = IR \tag{5.1}$$

$$E_t = E_0 \cdot sin(\omega t) \tag{5.2}$$

Within a linear system, the signal experiences both a phase shift (ϕ) and exhibits an amplitude distinct from I_0. as described in Equation 5.3:

$$I_t = I_0 \cdot sin(\omega t + \phi) \tag{5.3}$$

Combining all these equations, the impedance of the whole device can be obtained using Equation 5.4:

$$Z = \frac{E}{I} = \frac{E_0 \cdot sin(\omega t)}{I_0 \cdot sin(\omega t + \phi)} = Z_0 \frac{sin(\omega t)}{sin(\omega t + \phi)} \tag{5.4}$$

Equation 5.4 simplifies into Ohm's law when there is no phase shift (ω=0), this would represent a resistor [83]. However, a capacitor presents a different behavior which has an imaginary component expressed in Equation 5.5 where j is the imaginary unit and C is the capacitance:

$$Z = \frac{1}{j\omega C} \tag{5.5}$$

EIS measurements can be represented in two different manners, using a Bode plot or a Nyquist plot. The impedance has both a real part (Z_{real} or Z') and an imaginary part (Z_{imag} or Z"). The Bode plot illustrates the impedance's magnitude and phase shift as a function of frequency. These expressions can be appreciated in Equation 5.6 and Equation 5.7 [84]. On the other hand, the Nyquist plot is the plotting of the real part on the 'X' axis and the imaginary part on the 'Y' axis, note that the imaginary part is negative. An example of such plots can be seen in Figure 5.8.

$$|Z| = \sqrt{Z'^2 + Z''^2} \tag{5.6}$$

$$\phi = arctan(\frac{Z''}{Z'}) \tag{5.7}$$

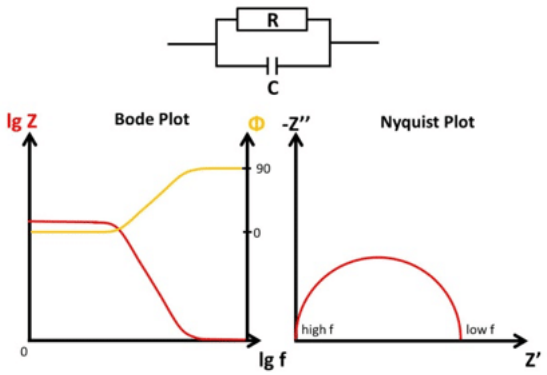


Figure 5.8: Example of both a)Bode plot and b)Nyquist plot of the equivalent circuit of a capacitor and a resistor in parallel [85].

The measurements obtained during the EIS are associated with the electrode/electrolyte interface which can then be simulated or compared with equivalent electrical circuits. This interaction was already explained in section 1.5.2. Thanks to the Nyquist plot, these electrical components of the equivalent circuit can be determined. Each electrical component represents a certain curve and therefore can be distinguished in the results. Some examples of these curves with their corresponding equivalent circuits can be appreciated in Figure 5.9. For this project, I am expecting similar results to the ones shown in Figure 5.10. This is because the interface between the silicon pillar and the electrolyte should have the effect of the double layer capacitance, the resistor implying Faradaic reactions, there might be some additional effects in the system depicted as the Warburg impedance [86] and also the resistance from the electrolyte itself.

For the correct interpretation of the measurements, there is a value of great interest. In the Bode plots, the value obtained at 1 kHz is analyzed. This value is chosen for several reasons. At around 1 kHz, the impedance is often most sensitive to charge transfer processes at the electrode-electrolyte interface. It also represents an intermediate frequency that balances capturing rapid capacitive behavior (occurring at high frequencies) and slower charge transfer processes (occurring at low frequencies).

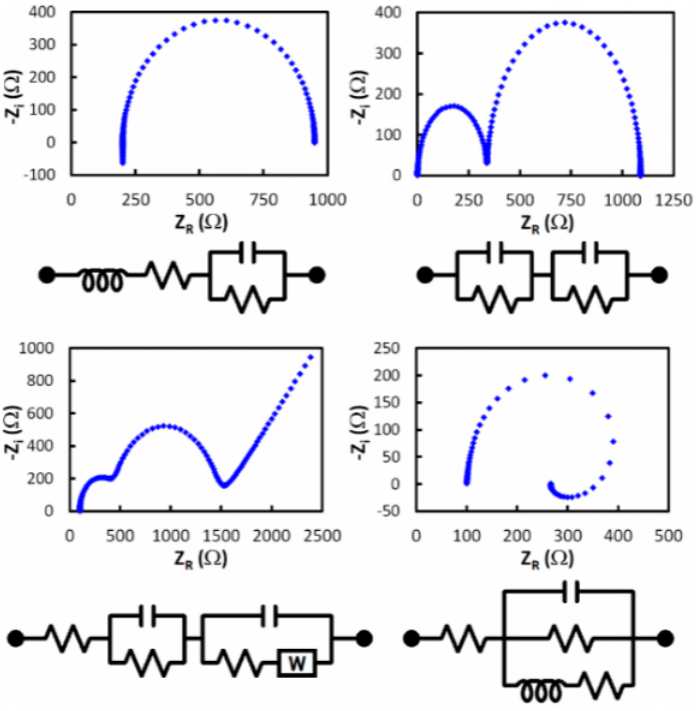


Figure 5.9: Example of both experimental and simulated impedance spectra (Nyquist plots) [83].

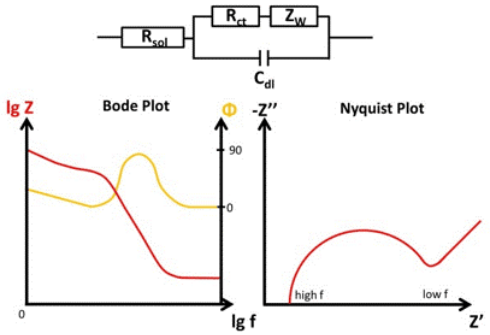


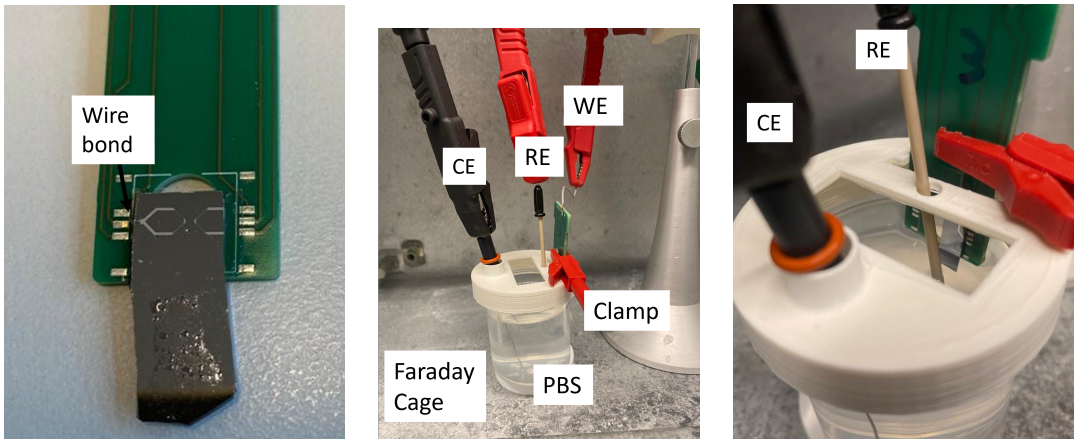
Figure 5.10: Expected result a)Bode plot and b)Nyquist plot of the equivalent circuit [85].

Therefore, it provides information about the system's capacitive and resistive components. It is also widely used in research and industry for comparing different devices and interactions. This allows for easier reproducibility and comparability.

5.2.1. Preliminary measurement to support fundamentals

To better support the fundamentals of this project and its approach, a simple EIS measurement was performed to study the transmittance of a signal from silicon into the electrolyte. Al/Si was deposited on top of both p-type and n-type silicon wafers. It was patterned to leave parts of the silicon wafer exposed so that it could be in contact with the electrolyte for correct measurement. These wafers were then diced manually in such a way that they had a shard geometry in which some Al/Si remained on the top part and only silicon would be in the bottom part. The metal was then contacted with wire bonding and only the silicon part was submerged inside the electrolyte solution, in this case, PBS. Then, 3 different EIS measurements were performed in such structures and then averaged. In this case, insulation of the contact pads and the wire bond was not needed as the structure will not be fully

submerged. Only the silicon part was in contact with the electrolyte. Such set up can be seen in Figure 5.11. The crocodile clamp attached to the PCB was there to make sure that only the silicon part of the shard was submerged and not the metal.



(a) Wire bond of the shard structure to PCB. **(b)** Experimental set up. **(c)** Experimental set up close up.

Figure 5.11: Set up overview of the preliminary measurement. In picture c) it can be appreciated that only silicon is in contact with electrolyte.

The measurements performed showed that indeed, a signal is measured inside the electrolyte for both the n-type and p-type. The impedance at 1 kHz was equal to **47.2 k**Ω and **236.8** Ω respectively. The full results can be found in Appendix B. The low impedance obtained might be related to the large surface area that the silicon electrodes have in this case.

To simulate the final arrangement and functioning of the device, another test was carried out in which both the working electrode and the counter electrode were silicon shards. This was done for the p-type wafer. The result of the impedance at 1kHz is equal to **17.8 k**Ω. The full results can be found in Appendix B. Both these results support that the fundamentals on which this project has been based are correct and indeed, the silicon pillars inside the well of the device should be able to transmit a signal into the electrolyte.

This set up and measurement was also applied to a platinum wire which acted as the working electrode. This way a comparison can be made between the two materials. Platinum was chosen as a comparing material as many times in literature this metal was used for the external electrodes implemented for stimulation. In this case, the average impedance at 1 kHz of the platinum wire was equal to **130.5** Ω. The full results can be found in Appendix B. In this case, both the working electrode and the counter electrode are made of platinum. This is why there is such a big difference in the results when comparing it with a set up in which both electrodes are made of silicon.

5.2.2. Method

Once all the chips were adhered on the PCB, wire bonded, insulated, and the cables had been soldered for the connection with the tool, 3 different measurements of EIS were performed on each electrode pillar. This means that every chip, as it has two pillars, was subjected to 6 different measurements, 3 on each pillar. The range of the frequency sweep was from 1 Hz to 100 kHz. This range is sufficient to study both the slow and rapid reactions happening at the electrode-electrolyte interface.

Before submerging the chip in the PBS solution, a pre-treatment using isopropyl alcohol (IPA) was done inside the chip's well. This was done to improve the wettability of the well as well as the Si pillars to make sure that the electrolyte would be in contact with the pillars once submerged in the PBS. After letting the IPA inside the well for approximately 3 minutes, nitrogen gas was used to dry it before finally submerging the chip in the PBS. As nitrogen is an inert gas, it won't have any influence on the

surface properties of the Si pillars.

Once the measurements were done, the results were recovered, and the data was treated thanks to a Python code I developed. The results were then averaged and plotted (both the Bode and the Nyquist plot). The value of the impedance at exactly 1 kHz was then extracted thanks to interpolation of the graph obtained. These measurements were made taking into account the different device designs already explained in Chapter 3.

After these measurements had been done, a breaking test was performed. Two different tests were done in this regard. The first one was to simply apply some small pressure on the PDMS membrane so that the metal lines would break. The breakage of the metal lines was then checked under an optical microscope. Once the metal lines had been broken, 3 EIS measurements were performed as previously mentioned.

The second breaking test performed implied the removal of the pillar itself to which the measured electrode was connected. Then, 3 EIS measurements were performed as in the previous cases. It is important to note that these breaking tests were not performed on the same chips but on different samples. This way it was ensured that there would be no influence between these tests.

5.3. Results & Discussion

In this section of the report, the results obtained from the samples will be presented and discussed. As mentioned previously, the samples were immersed in PBS, and EIS was performed using a three-electrode cell setup. Both the Bode and the Nyquist plots were obtained. Measurements were made in all four different device designs. The results across the four different device designs were very similar in all cases. The results for the 4 different designs can be seen in Figure 5.12. A table with all the numerical values of the results can be seen in Table 5.1.

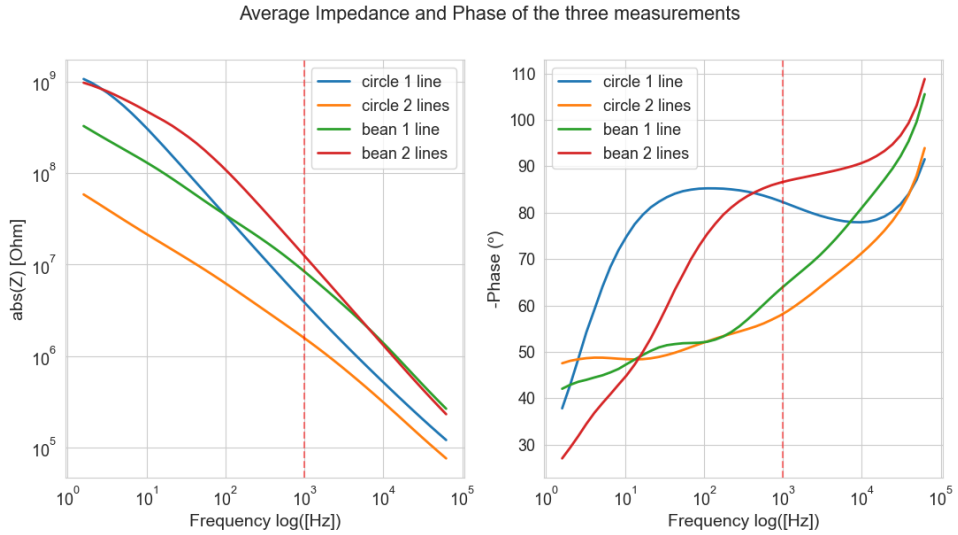
Table 5.1: Results for the EIS at 1 kHz.

Design	Averaged Impedance	Averaged phase (Degrees)
Circle single line	3.7 MΩ	82.34
Circle double line	1.6 MΩ	58.12
Bean single line	8.3 MΩ	64.04
Bean double line	12 MΩ	86.7

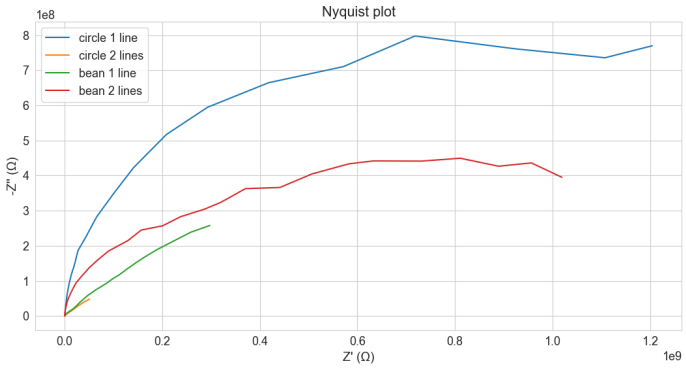
This data give us the following information. It appears that the impedance at 1 kHz is extremely high, in the order of MΩ. Looking at the geometry of the Bode plot, it looks like a straight line with little to no change in its geometry for both low and high frequencies. This tells us that the type of reaction occurring at the electrode surface does not change over the whole frequency spectrum. The phase plots present how the phase increases as the frequency increases as well. No sudden changes in the phase are seen nor any remarkable minimum or maximum that could indicate a change in the reaction phenomena happening at the interface.

Regarding the Nyquist plots, they show no typical behavior that would be expected at the electrode-electrolyte interface. No key parameters can be extracted from such graphs to indicate any behavior or the tools to create an equivalent electrical circuit. There is some kind of arch forming which flattens out in one of its extremes. If the line had been straight and with an approximate angle of 45 degrees it could be related to the Warburg impedance [86]. Nevertheless, this behavior only shows when in series connection with a previously existing resistor which in this case can not be appreciated.

The breaking tests were also performed to check whether the physical breakage of the metal lines or the removal of the pillar would cause any change in the previous measurements. The results obtained for the breakage of the metal lines in the previously measured circle shaped with 2 metal lines are depicted in Figure 5.13.



(a) Bode plot.



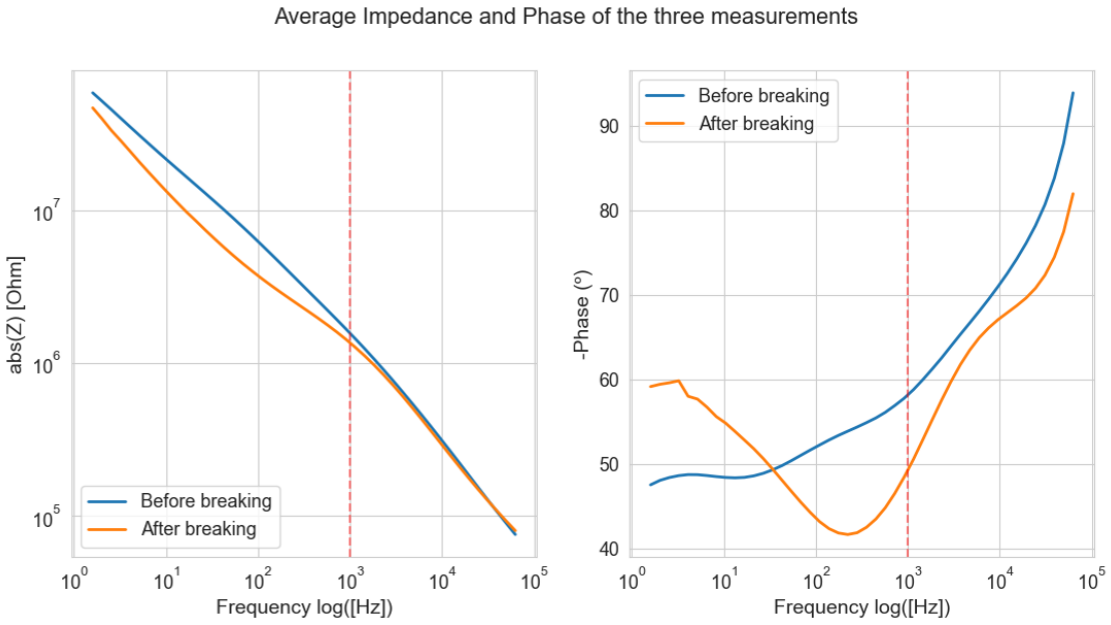
(b) Nyquist plot.

Figure 5.12: EIS measurements of the 4 different designs.

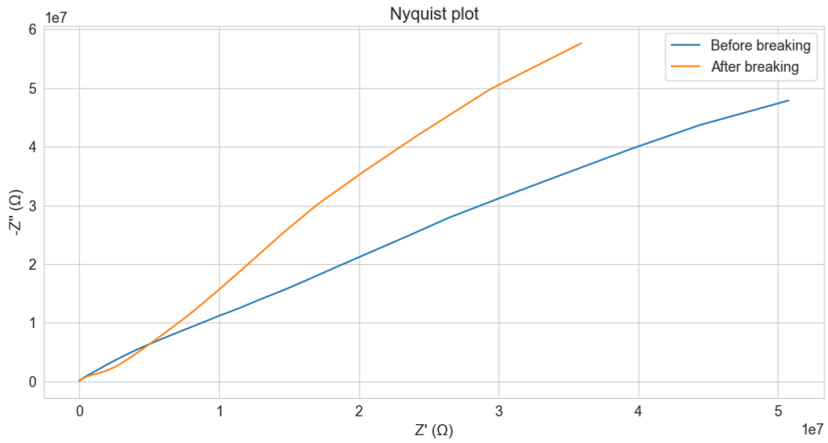
When comparing both the previously done measurements with the measurements done after breaking the metal lines there are barely any noticeable differences. Only the phase curve presents a different geometry. This change in the geometry of the phase curve can also be appreciated in a change of the slope of the impedance where a small change can be seen. Nevertheless, the absolute values in terms of impedance and phase remain relatively similar with no major differences. Similar results were obtained when performing the breaking test of removing the silicon pillar.

All these experimental results lead me to the conclusion that in fact what I am measuring through the potentiostat is an open circuit. This means that the results I am obtaining do not come from the electrodes inside the well of the chip but from the internal circuitry of the measurement system which is trying to give an output during the measurement. This fact inevitably leads us to question why are we measuring such open circuit and what factors could have caused this outcome.

To elucidate where the cause may be, a recapitulation of the signal pathway is first explained. This is done to try to pinpoint the stage of the process that could have led to these results. A diagram of the different points where a problem might have occurred can be seen in Figure 5.14. First of all, the connection of the potentiostat to the PCB containing the samples and the corresponding interconnect lines inside the PCB to its contact pads may be affected. To check for this cause, a voltmeter was used to probe one extreme of the cable soldered to the PCB (the one to which the crocodile clamp will be attached to connect with the potentiostat) and the contact pad of the PCB close to the chip. A simple resistance measure was performed and it was seen that there was no disruption in such connection as



(a) Bode plot.



(b) Nyquist plot.

Figure 5.13: EIS measurements before and after breaking the metal lines for circle shape with 2 metal lines.

the resistance obtained was very low, in the order of Ω.

The second stage that the signal must take to access the electrolyte is to go through the wire bonding between the PCB contact pads and the contact pads inside the chip. This wire bonding was performed using standard procedure and proper attachment to both pads was assured after visual inspection with an optical microscope. Encapsulation of the wire bonding was done using hot glue over the connection. This way the electrolyte would not be in contact with the contact pads. To make sure the wire bonding was fully insulated, an additional layer of epoxy was also applied. Unfortunately, an inspection of the wire bonding after the insulation was impossible as neither the epoxy nor the hot glue was sufficiently transparent to appreciate the connections. One possibility for the high impedance of the measurement, thus the open circuit, could be that the metal line of the wire bonding was broken upon curing of the insulation materials thus no signal would be able to go through the Al/Si contact pads on the chip. This possibility was tested and will be explained later on in this report.

Then, the signal would have to travel from the contact pad of the chip through the metal line to the base of the pillar. This connection was checked previously as stated in section 4.1 where continuity of the metal lines was assured through a resistance measurement using a voltmeter. It could also be

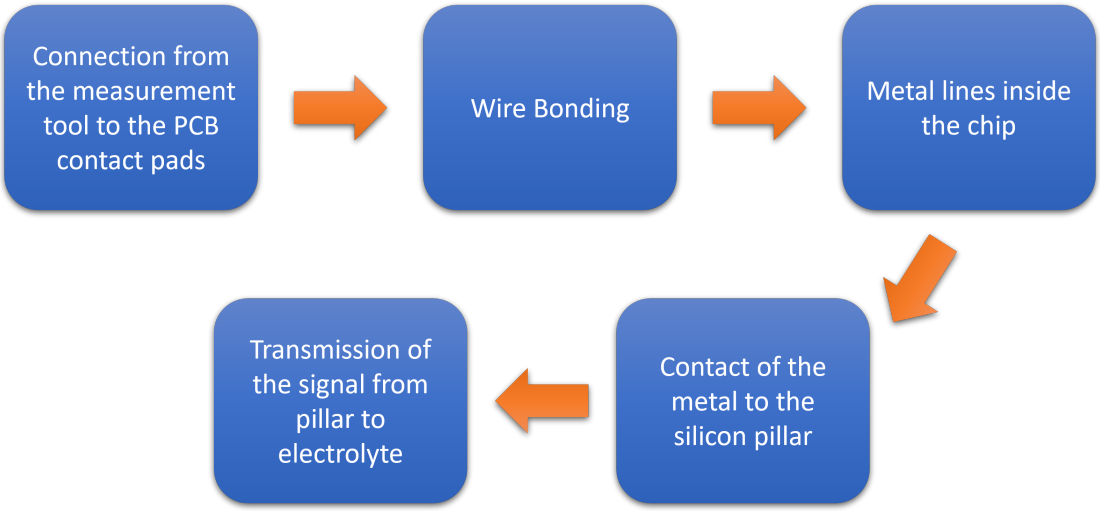


Figure 5.14: Diagram of the different steps the signal must go through inside the system.

that the metal lines might have broken during the manipulation of both the chip and the PCB. To ensure that this was not the case, before every EIS measurement, the samples were inspected under an optical microscope to check whether the metal lines had suffered any damage just before the measurement.

The next stage the signal encounters is the interface between the metal line (made of Al/Si) and the silicon pillar. This interface should be ohmic enough for the signal to be transmitted from the Al/Si to the Si pillar as was seen in the results obtained in Chapter 2 where different combinations of both metal and silicon wafers were studied. The geometries of the structures in contact are different and it might be the cause of a higher resistance than expected thus no signal is transmitted into the Si pillar and consequently, unable to travel through the electrolyte.

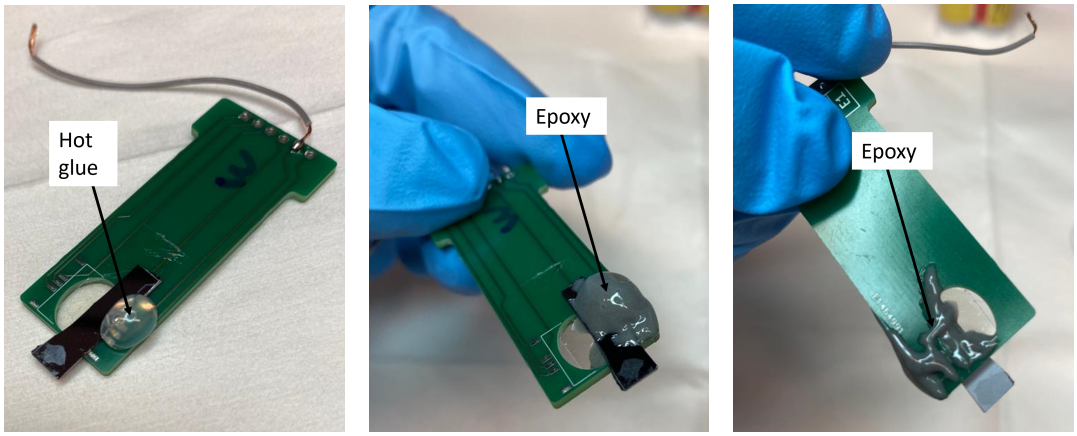
Lastly, the signal must be able to be transmitted from the Si pillar into the electrolyte. The teflon walls that were discussed in section 4.3.2 are supposed to be removed thanks to treatment with oxygen plasma. It is a possibility that the teflon walls were not fully removed with such oxygen plasma treatment thus insulating the Si pillars from the electrolyte. This must not be the case as the final step of oxygen plasma inside the Rapier has been verified by Bi/ond so that no teflon remains on the silicon pillars surface.

Further analysis in terms of CV and VT was scheduled as part of this project but due to time constraints and some major challenges when performing the EIS measurements, this study could not be performed. These challenges can be found in the appendix A.

5.3.1. Testing for wire bond stability after insulation

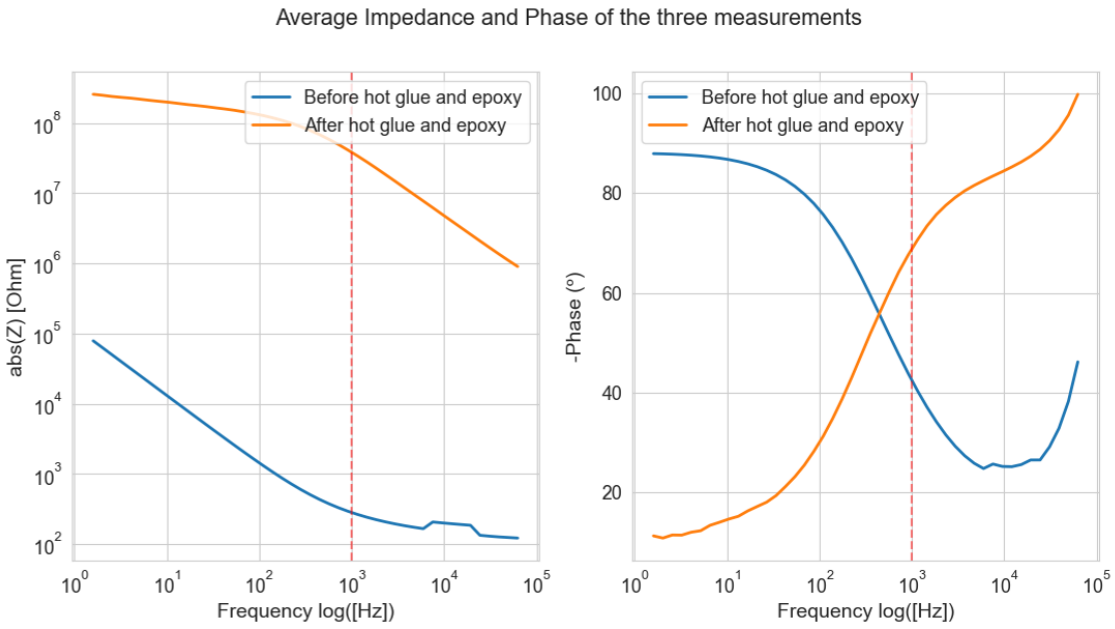
As mentioned previously, a test was performed to check whether the wire bonding insulation could be the cause of the final results obtained in this project. This test consisted of using the same structures employed in section 5.2.1. These structures were silicon wafers on which Al/Si was deposited on top and patterned so that silicon was exposed. These wafers were manually diced using a diamond tip pen to adopt a geometry in which only the silicon would be in contact with the electrolyte. As seen in section 5.2.1, a certain signal was measured during EIS.

To reproduce the conditions in which the final devices were handled, one of the samples was selected. First, a control EIS measurement was made to make sure that the wire bonding was intact and indeed I obtained the same measurements as before. Then, hot glue was applied on top of the contact pad using a glue gun. Finally, the same epoxy used to insulate the final devices was also applied and let it be cured overnight. Images of this sample preparation can be appreciated in Figure 5.15.

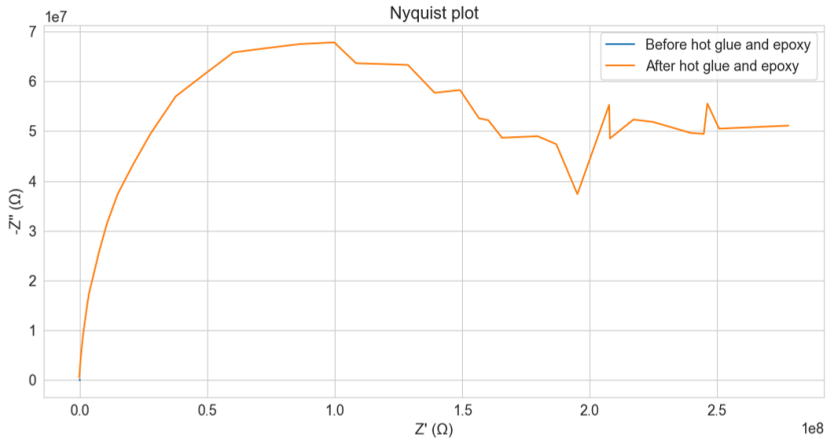


(a) Hot glue on top of contact pad. **(b)** Epoxy on contact pad front side. **(c)** Epoxy on contact pad back side.

Figure 5.15: Sample preparation for the testing of wire bonding stability.



(a) Bode plot.

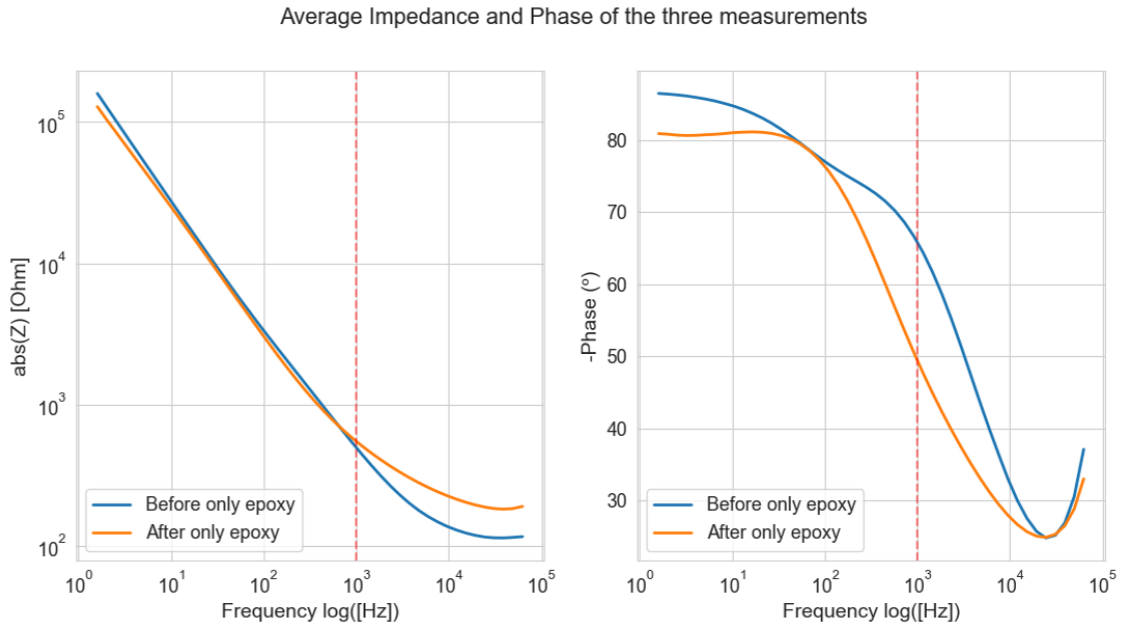


(b) Nyquist plot of a p-type wafer after insulation of contact pads.

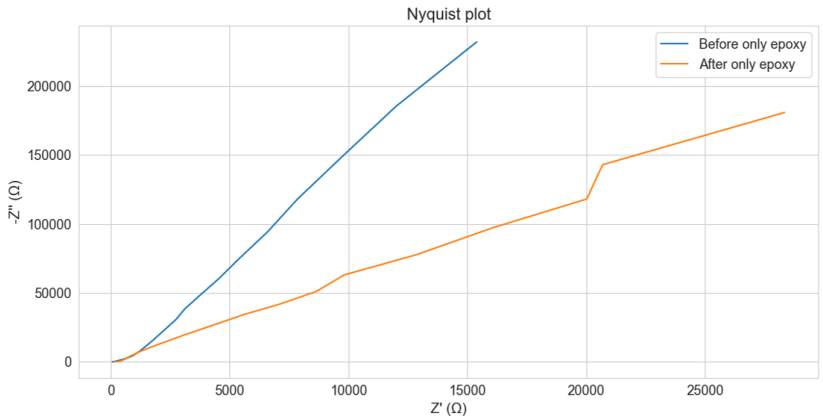
Figure 5.16: EIS measurements before and after insulation of contact pads with both hot glue and epoxy.

Once the epoxy was cured on top of the contact pads, an EIS measurement was performed using the set up already explained in section 5.2.1 where only the silicon is in contact with the electrolyte. The results can be seen in Figure 5.16.

As seen from the results, the final values and the geometry of the plots resemble the results obtained from the final devices. There is also a very big difference between the results obtained before the insulation of the contact pads and afterwards. The impedance increases from the range of hundreds of Ω to MΩ. It can be concluded that the application of the hot glue and the epoxy made a big impact on the measurements for this test. These results can not be extrapolated to the results obtained regarding the final devices as the conditions are different. What can be extracted from these results is that the insulation of the contact pads plays an important role when performing EIS measurements as it can affect the stability of the wire bonding. Hence, the problem regarding the final devices might be related to this step.



(a) Bode plot.



(b) Nyquist plot.

Figure 5.17: EIS measurements before and after insulation of contact pads with only epoxy.

To check which one of the materials applied for the insulation was the one making this influence, a second test was made in which the sample instead of being insulated by both hot glue and epoxy, it was only insulated with epoxy. The purpose was to see whether the results obtained after the curing of

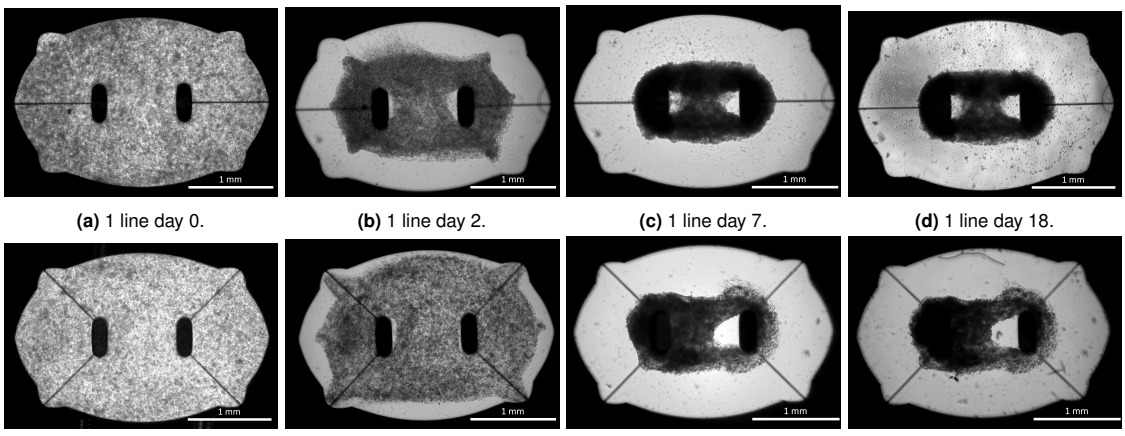
the epoxy were the same as the ones obtained before the insulation. The results can be seen in Figure 5.17.

As seen in the plots, the values remain almost identical. This leads to the conclusion that the epoxy does not have that much of an influence on the measurement and that the major player in the increase of the impedance after insulation of the contact pads might be indeed the hot glue. These results can not be ultimately conclusive as it is still possible that the wire bonding might have broken during the handling of the samples. It is also a possibility that as the insulation is a manual process, the wire bond suffers damage upon application. Nevertheless, these results indicate that proper insulation of the contact pads and the wire bond is of great importance when making the measurements.

5.3.2. Results from testing performed at Bi/ond

After the final devices had been manufactured, some of these were sent to the team at Bi/ond for further testing. The first testing performed was regarding the manipulation of such chips and their integration in already designed PCBs platforms designed by the company. The purpose of this test was to check whether by attaching and manipulating the final chips with their platforms, the metal lines would break.

From the 12 chips that I provided to the engineering team, none of them suffered any breakage of their metal lines during attachment and manipulation. These results state that my final devices are compatible with the process flow of the company and do not suffer any damage from their standard procedure. The next test performed was a biocompatibility test in which the biology group seeded cells inside the well of my final device to see whether the system was biocompatible and their protocols could be used on my devices. Bundle formation was achieved upon the completion of their developed protocol without the need to make any changes. The results can be seen in Figure 5.18 where bundle cell formation can be seen at different time points. This result states that my devices are indeed biocompatible and what is also important, compatible with the biological protocols developed at Bi/ond.



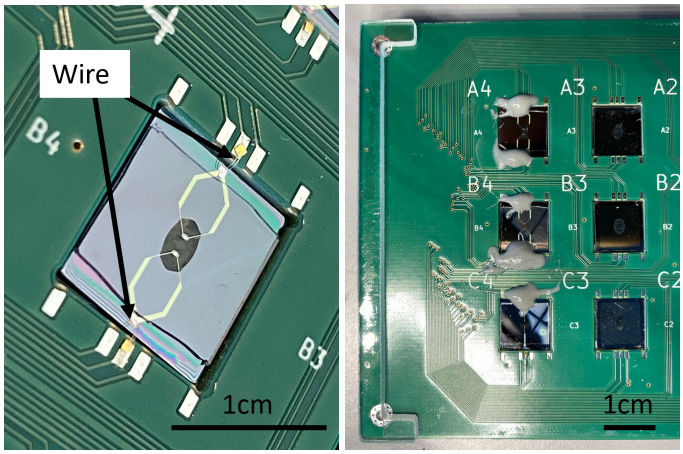
(a) 1 line day 0. **(b)** 1 line day 2. **(c)** 1 line day 7. **(d)** 1 line day 18.

(e) 2 lines day 0. **(f)** 2 lines day 2. **(g)** 2 lines day 7. **(h)** 2 lines day 18.

Figure 5.18: Images taken with an optical microscope from the biological test.

Stimulation of the cells was also attempted once the muscle bundle was finally formed around the pillars. For this purpose, I wire-bonded the chips used for the biological test to a PCB before the seeding of the cells which can be seen in Figure 5.19. Epoxy was also applied to protect the wire bonding. Unfortunately, no contraction of the cells was appreciated when a signal was input through the metal lines contacting the base of the pillars. This result was expected based from the previous results obtained in section 5.3, and tends to confirm the conclusion.

One interesting result from the tests performed at Bi/ond concerned the stability of the metal lines during the maturation of the muscle cells. The chips were placed, wire bonded and insulated with epoxy on the PCB provided by the company. After this was done, visual inspection under an optical



(a) Wire bonding in bi/ond's PCB. **(b)** Epoxy applied.

Figure 5.19: Images of the wire-bonding and protection on the bi/ond's PCB.

microscope ensured that all the metal lines inside the chip remained intact before the seeding of the cells. These chips were only inspected again before the stimulation test after the muscle bundle was formed. Visual inspection under an optical microscope showed that many of these metal lines that were intact before seeding, were broken. There were only two checkpoints in which these metal lines were checked, before the seeding of the cells and before the stimulation of the muscle bundle. Sometime in between this period, the metal lines were damaged and broken. This means that during the maturation of the muscle cells, something happened. It is not sure if it can be due to the handling of the PCB which might resulted in the breaking of the metal lines or because the formation of the muscle bundle added some stresses to the system that the metal lines were not able to withstand. Nevertheless, this information is worth studying in the future.

6

Conclusion & Future work

Current drug development processes pose various challenges for the pharmacological industry in terms of time consumption and the amount of money that needs to be invested. New approaches need to be implemented in this field so that research and development can keep growing. Organ-on-Chip devices present a viable and promising platform for such experimentation to be done reducing costs, time and avoiding ethical matters concerning *in vivo* experimentation. Heart- and muscle-on-chip devices are currently being developed and their full capabilities are yet to be defined. Much research has been conducted on this matter giving rise to new questions and new alternatives that need to be explored. The use of novel technology can help improve current devices and develop new ones to make more accurate, stable and significant platforms for the *in vitro* study of both heart and muscle tissue. This project's objective was to implement 3D microelectrodes in a Muscle-on-Chip device from Bi/ond for the stimulation of the muscle cells.

In this project, the Si pillars of Bi/ond's Muscle-on-Chip platform were attempted to be used not only as structural support for the cells but also as the stimulating electrodes for the system. The design and fabrication were done to achieve this objective. In terms of fabrication, the objective was accomplished as the device was able to be made. Regarding the electrochemical characterization of such devices, several challenges were encountered. The final results of such characterization showed that what was being measured was an open circuit instead of the Si pillars inside the well of the chip. Several tests were performed to elucidate where the cause of these results might be.

It was seen that the connection between the measurement system and the PCB used was correct. The continuity of the metal lines inside of the chip was also correct. Based on the preliminary tests performed in this project, a signal was able to be transmitted from the metal to silicon and from silicon to the electrolyte. The major issue came from the insulation of the contact pads during the measurements. It was seen that this insulation might have had an impact on the measurements taken as it could be the cause of a breakage in the wire bond connecting the chip to the PCB thus interrupting the transmittance of the electrical signal. Another cause that could affect the transmittance of the signal might be the geometry of the electrodes at the base of the pillars as the tests previously done were made with a different geometry because of the timeline of the project.

Overall, this project led to the design and fabrication of 3D microelectrodes inside Bi/ond's Muscle-on-Chip device for the stimulation of the muscle cells. This approach would solve many complications arising from the implementation of external electrodes into the system. The different tests and measurements performed led me to conclude that the measurements were not coming from the Si electrodes themselves. Thus, the functionality of the device could not be proven yet. However, the problem was studied and several discoveries were made from which to continue the development of such device.

6.1. Future work

The first thing to do in future work regarding this project is the optimization of the insulation of the contact pads. In the current experimental set up, the chip is completely submerged in the electrolyte thus proper insulation is required. It was seen that the way insulation is done can have a great impact on the final measurements. There were some major differences between using both hot glue and epoxy, and using only epoxy as the insulation layer. Therefore, I advise that in future steps, only epoxy is used for the insulation if the experimental set up is to remain the same.

Another approach would be to change the experimental set up in a way that the chips would not have to be fully submerged in the electrolyte to make the measurements. This could mean the addition of an extra external well around the central well of the chip. This would mean that the electrolyte could be conserved inside this well instead of having the electrolyte all around the chip.

The substitution of the wire bonding with other techniques could also be an option in this case. There are other ways in which to make a connection between the contact pads of the chip and the contact pads of the PCB. This for example could mean conductive adhesives, clamping or even soldering. These types of connections are known to be stronger than wire bonding thus increasing the stability of such connections.

It is also possible that the high impedance also comes from another source. The connection between the electrode and the base of the pillar is one of the key points of this project. This connection was studied using Van der Pauw structures at the early stages of this project. The geometry of such contact was different from the geometry finally designed for the final devices. This connection might be not as good as it is thought to be thus more studies in this area must be performed looking at different sizes and geometries.

In terms of fabrication, reducing the surface area of the electrodes underneath the base of the pillar could increase the yield of manufacturing. One of the main problems regarding the fabrication was the tapering of the pillars during DRIE. When this happened, the metal of the electrodes was exposed to the well and was etched during the HF bath. By reducing the surface area of the electrodes, it is ensured that even if the pillars are tapered, the metal would not be exposed to the HF thus it would not be etched away during that process.

From the final tests performed at Bi/ond, it was seen that some of the metal lines were broken from the point the cells were seeded inside the device. This breakage could be due to the handling of the platform but also because of some stresses that the cells might be exerting on the pillars while they mature. These stresses might be the cause of the line breaks. A study of how much force these cells exert on the pillars must be performed to anticipate whether the metal lines would be able to survive it. One way to quantify the limit stress for metal lines could be the use of simulation programs to try to recreate this situation. This way, different thicknesses and shapes of the metal lines could be developed.

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A

Problems encountered during EIS measurements

This appendix document will give the reader insight into the problems encountered at the measurements phase of the project. Ideally, EIS, CV, and VT measurements were planned for the scope of this project for the full electrochemical characterization of the Si pillars acting as the stimulation electrodes for the system. An explanation of the different challenges encountered during the realization of such measurements will be provided following the timeline that occurred during the project.

When the final devices were obtained after the fabrication process, they were attached on top of the PCBs and wire bonded to them using the small gold pads on top of the Al contact pads of the PCB mentioned in section 5.1.2. Initially, the insulation of such contact pads was done only with hot glue applied with a glue gun. I tried to ensure that the whole contact pad was covered and that neither the contact pads, on the PCB and the chip, nor the wire bond were exposed. This insulation is depicted in Figure A.1

Then, I followed the same experimental set up described in chapter 5 in which the chip is fully submerged inside the PBS solution in a three-electrode cell set up for the measurement. The results of such measurements are depicted in Figure A.2.

These results showed very promising as the impedance was relatively low at 1 kHz in all of the different designs as seen in Table A.1. I also performed some cyclic voltammetry (CV) and voltage transient (VT) measurements on these samples and everything looked within the parameters of what was expected. The problem arose when performing the breaking test. When the metal lines were broken manually, an EIS measurement was performed. The results were almost the same as the ones before breaking the metal lines which told me that what I was measuring was not my silicon pillars but something else.

Table A.1: Results of EIS with just hot glue as insulation.

Design	Averaged Impedance	Averaged phase (Degrees)
Circle single line	5.4 kΩ	12.26
Circle double line	10.7 kΩ	4.28
Bean single line	4.8 kΩ	3.47
Bean double line	4.4 kΩ	3.47

Thinking about what I could be measuring in the EIS, due to the low impedance, I thought about the insulation of the contact pads. As the chip is fully submerged in the electrolyte, if the contact pads are not fully insulated, the electrolyte might be in contact with the contact pad itself. Because the

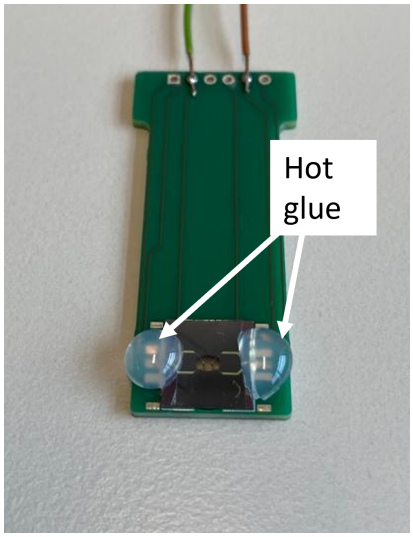


Figure A.1: Sample with only hot glue as insulation for the contact pads.

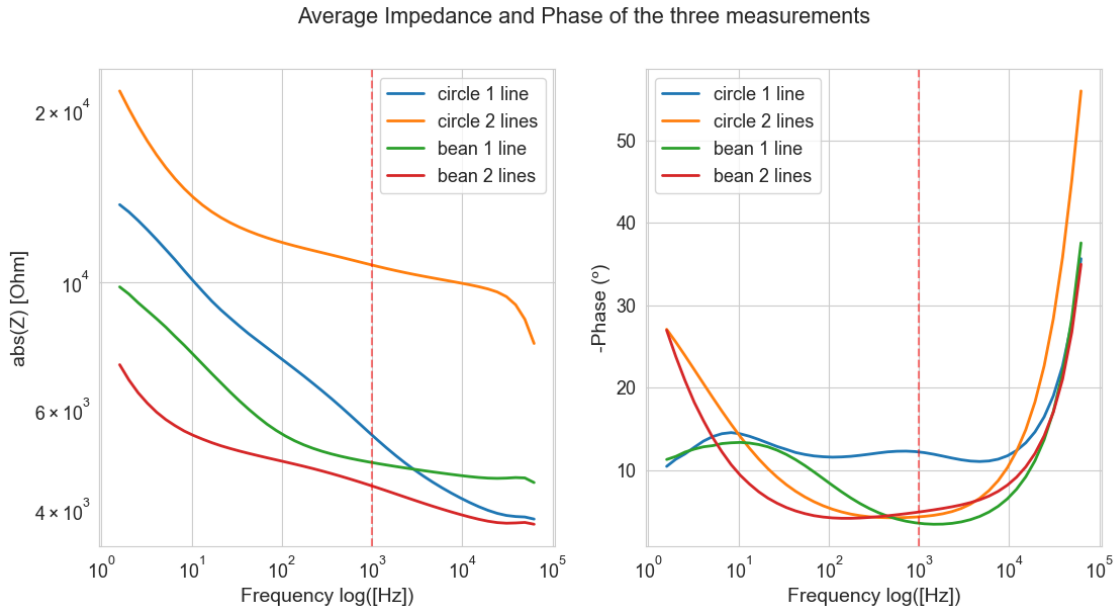
contact pads have a much lower impedance than the silicon pillars, there would be a leakage current flowing through the contact pads into the electrolyte. To prove this idea, I decided to cover the back of the chip fully with hot glue to make sure that no electrolyte was in contact with the contact pads on the back side of the PCB. The application of the glue in the back side can be seen in Figure A.3b. With this new insulation layer I made an EIS measurement. The results are depicted in Figure A.3a. It can be seen that the impedance has increased considerably when comparing it with previous results. Therefore, it led me to think that indeed what I was measuring was some leakage current flowing from the contact pads.

Because of these results, I wanted to see if the well was contributing to the measurement of the signal. To test this, I put some hot glue just on top of the well so it would be covered as seen in Figure A.5b. The results from the EIS of this set up can be seen in Figure A.4a.

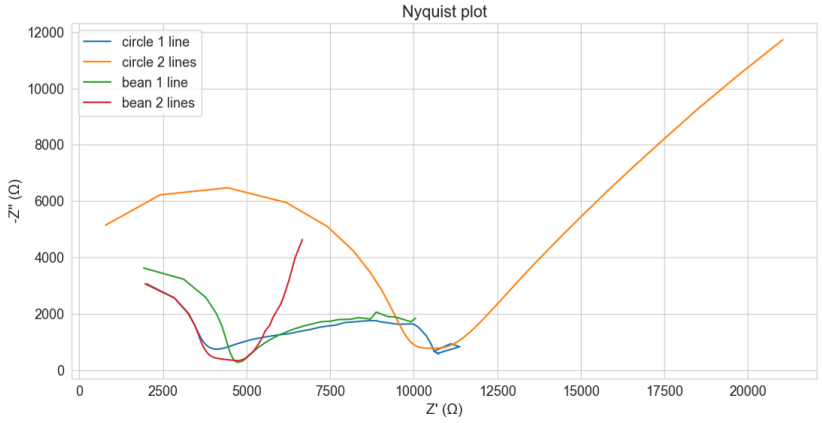
In this case, the impedance increases considerably again. Even though the impedance was high, I wanted to check if there might have been any other leakage current coming from the chip. What I did was to fully cover the whole front side of the chip with hot glue and perform a new EIS measurement. An image of the application of the hot glue all over the front side can be seen in Figure A.5a and the results in Figure A.5a.

The new increase in the impedance in this setting led me to think there was not only leakage current in the back side of the PCB but also in the front side. This is the reason why with in the other samples described in Chapter 5 I decided to apply epoxy both on the front and on the back side of the chip. Regarding the front side, it would be only applied in the junction between the chip and the PCB as the well needs to be exposed to the electrolyte.

To make sure that what I was measuring was indeed the contact pads of the PCB instead of the silicon pillars, I made an EIS measurement in which I submerged the PCB with the gold pad but no chip on it. This way, what I measured was the interface between the electrolyte and the contact pad in the PCB. The results can be seen in Figure A.6. The results are similar in value to what I was obtaining at the beginning thus leading me to think that in fact, it was the contact pads what I was measuring in the first measurements.

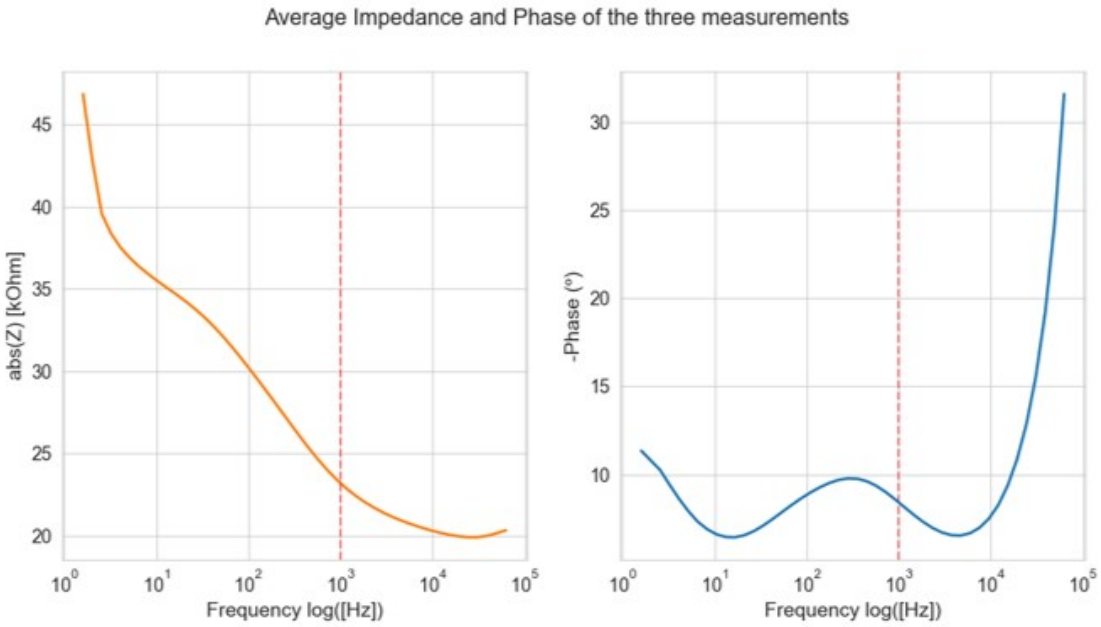


(a) Bode plot.



(b) Nyquist plot.

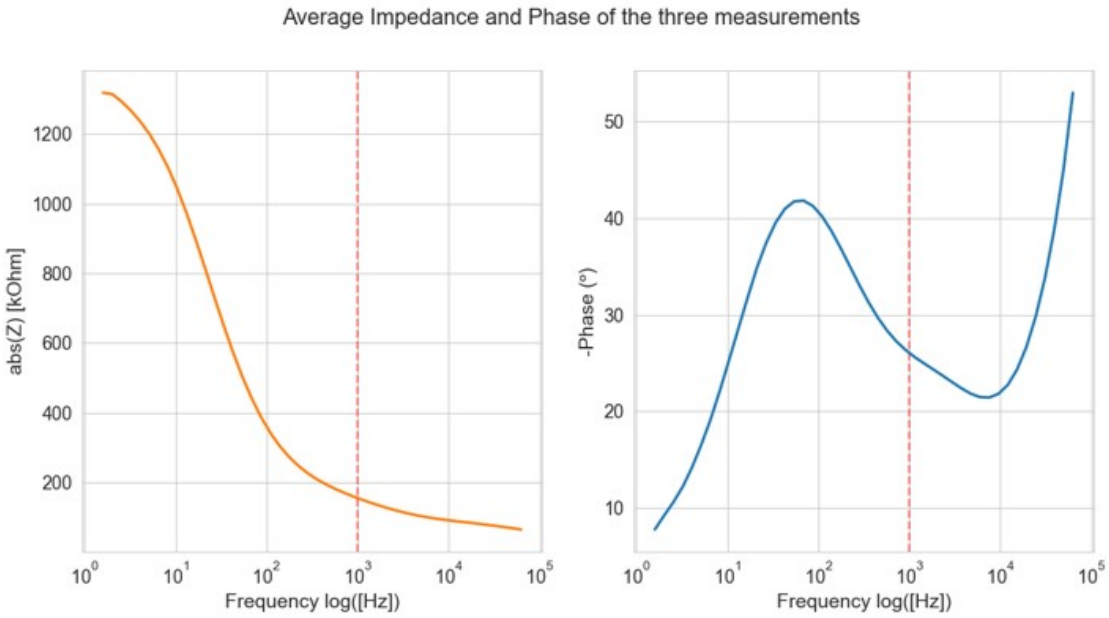
Figure A.2: EIS measurements of the 4 different designs after the insulation of contact pads with just hot glue.



(a) EIS of the sample with hot glue all over the back.

(b) Hot glue applied in the back.

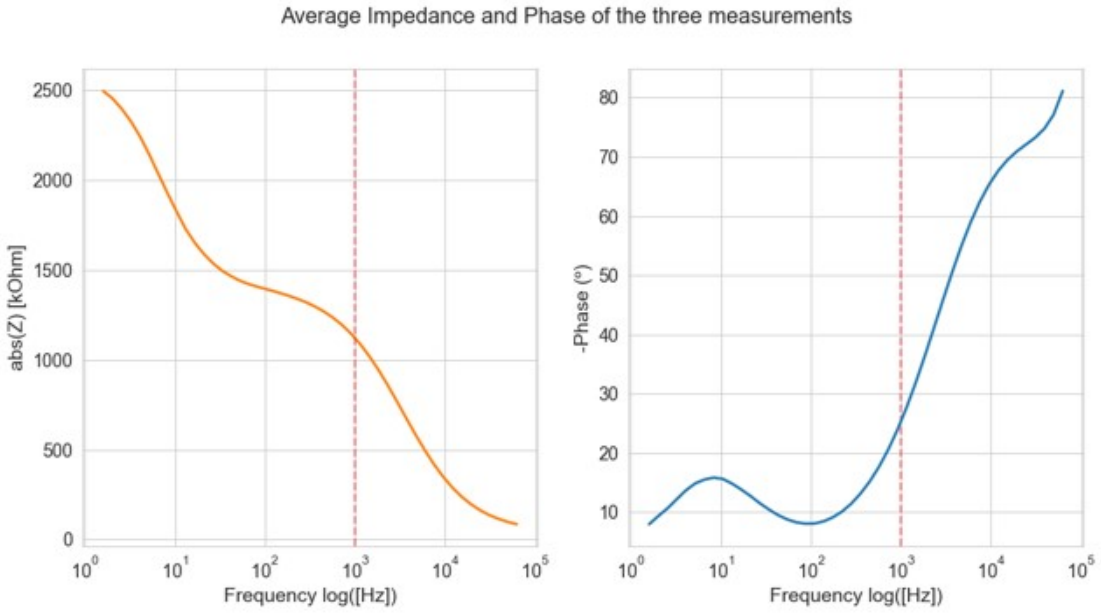
Figure A.3: EIS measurements of the sample with hot glue in the back.



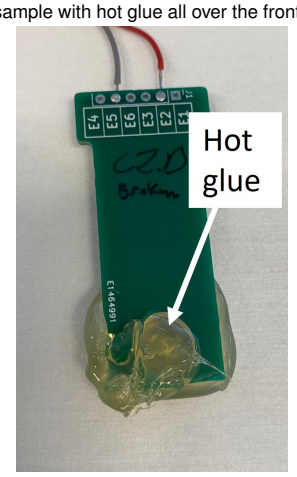
(a) EIS of the sample with hot glue all over the back and inside the well.

(b) Hot glue applied in the well.

Figure A.4: Bode plot and image of the application of hot glue in the back side and inside the well.

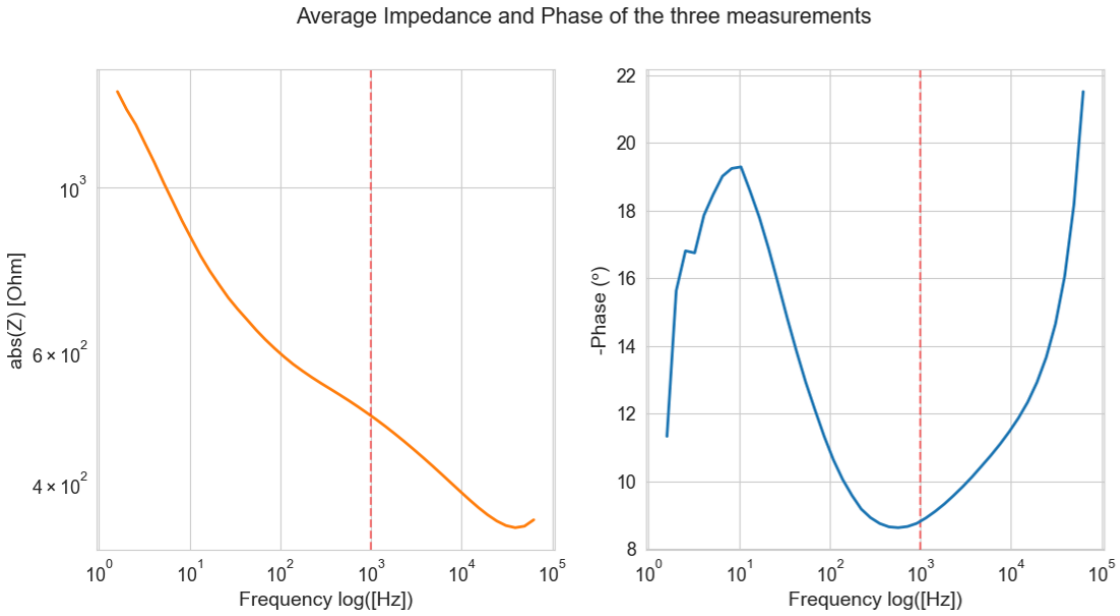


(a) EIS of the sample with hot glue all over the front and back side.

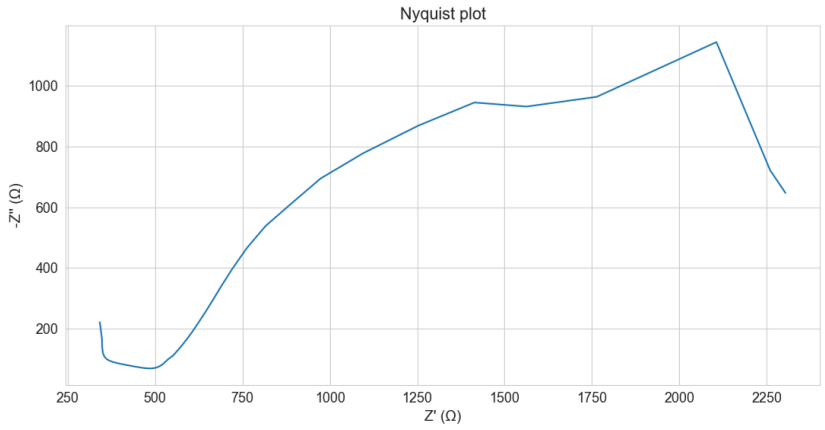


(b) Hot glue applied in the front side.

Figure A.5: Bode plot and image of the application of hot glue in the front and in the back side.



(a) Bode plot.



(b) Nyquist plot.

Figure A.6: EIS measurements of the contact pads with gold on them.

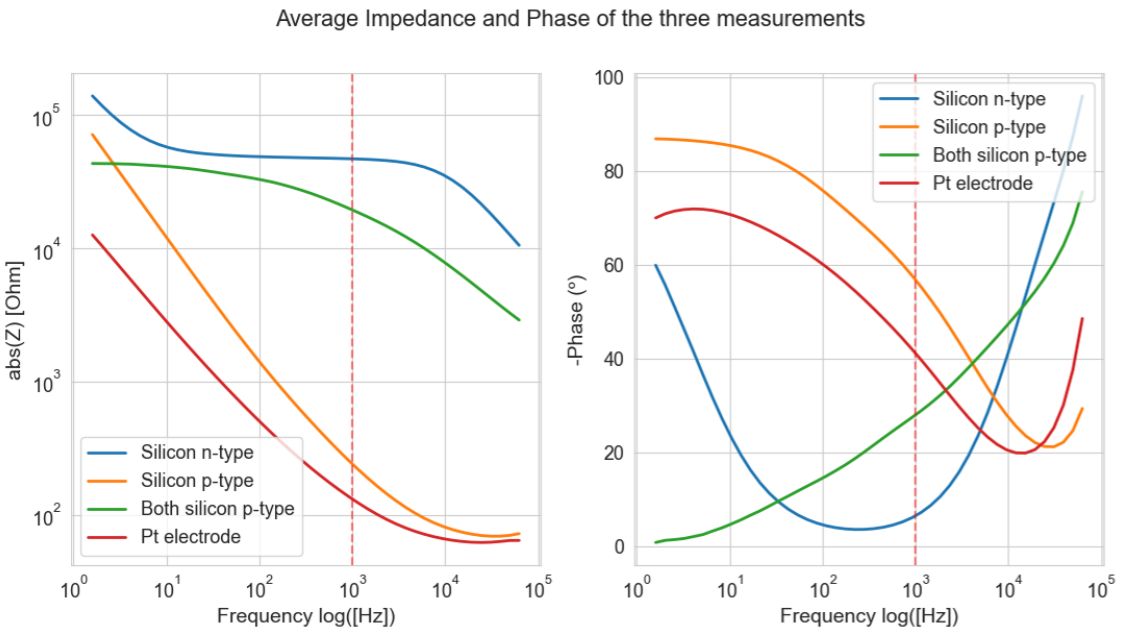
B

Preliminary EIS results & Platinum wire results

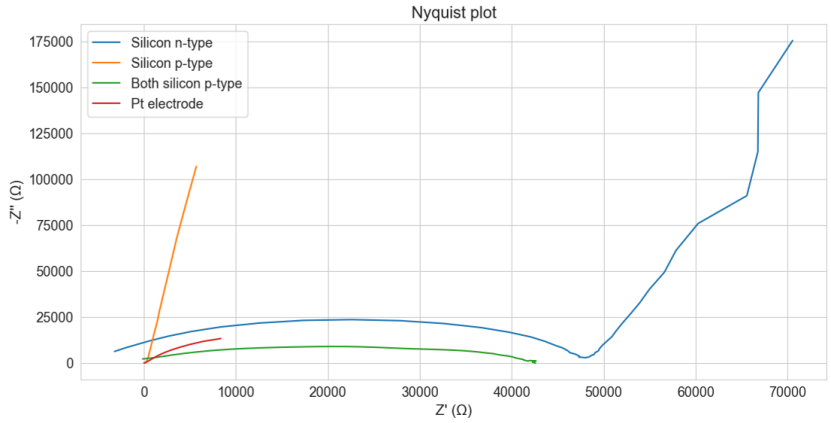
This appendix document contains the results obtained during EIS measurements performed during the tests described in section 5.3.1. These results can be found in the graphs in Figure B.1 and Table B.1

Table B.1: Results of EIS with the different wafer shards at 1 kHz

Wafer shard	Averaged Impedance	Averaged phase (Degrees)
P-type	236.9 Ω	57.12
N-type	47.2 kΩ	6.29
CE and WE P-type	19.5 kΩ	27.99
Pt wire	130.6 Ω	41.45



(a) Bode plot



(b) Nyquist plot

Figure B.1: EIS measurements of the different measurements performed with different wafers and the platinum wire

C

Van der Pauw structures test flowchart

Van der Pauw Structures Test

FLOWCHART

BATCH INFORMATION			
NAME OF OWNER :	Ramón Carballás Boluda	MASK SET :	PDM 16
NAME OF MENTOR :	Massimo Mastrangeli	MASK BOX :	269A and 269 B
RUN NUMBER :		DIE SIZE :	10 by 10 mm
WAFER AMOUNT :	8	START DATE :	/ /
SUBJECT TO PCC :	no	PCC APPROVED :	n.a.

DELFT UNIVERSITY OF TECHNOLOGY
ELSE KOOI LABORATORY

Adress	:	Feldmannweg 17, 2628 CT Delft, The Netherlands
P.O. Box	:	5053, 2600 GB Delft, The Netherlands
Phone	:	+31 - (0)15 - 2783868
Fax	:	+31 - (0)15 - 2622163
Website	:	www.tudelft.nl/ewi/onderzoek/faciliteiten/else-kooi-lab

GENERAL RULES

CLEANROOM BEHAVIOUR

❶ Always follow the "**Security and Behavior**" rules when working in the EKL laboratories.

❷ Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible!

❸ Use cleanroom gloves when working with vacuum equipment. Do not touch the inside or carriers with bare hands.

❹ Always check equipment and process conditions before starting a process. Do **NOT** make unauthorized changes!

❺ Directly notify the responsible staff member(s) when there are problems with the equipment (like malfunction or contamination). Flip the status card on the machine over to **DOWN** to warn other users. Also change the status of the system to **DOWN** in the "Phoenix Living Database" system.

❻ **DO NOT TRY TO REPAIR OR CLEAN EQUIPMENT YOURSELF**, and **NEVER** try to refresh a contaminated etch or cleaning bath! Only authorized staff members are allowed to do this.

WORKING WITH CMOS INCOMPATIBLE MATERIALS

❶ Substrates, layers and chemicals which are not CMOS compatible may cause contamination of bathes, equipment, wafer boxes, etc.. Using these materials in the class 100 and SAL cleanroom without permission is **FORBIDDEN.**

❷ The use of CMOS incompatible materials for processing in the class100 and SAL cleanroom must **ALWAYS BE EVALUATED** and **APPROVED** by your mentor and the EKL contamination officer.

❸ Wafers that are contaminated may **NEVER** be processed in any of the bathes or equipment without permission. Special precautions may be required, like the use of a separate container, a special substrate holder or a wafer carrier.

❹ You **MUST** work according to the rules described in the **Preventive Cross Contamination** (PCC) document, available on the "EKL Sharepoint webpage", and the **Materials** database from the "Phoenix Living Database" system.

CLEANING OF WAFERS

Wafers must always be cleaned before performing a **COATING, FURNACE, EPITAXY** or **DEPOSITION** step if they were stored for 4 hours or more.

Use the correct cleaning bathes:

- Acetone ⇨ To remove photoresist that is not used as a mask for ion implantation or plasma etching.
- Tepla stripper ⇨ To remove ion bombarded photoresist after implantion or plasma etching.
- HNO_3 99% $(Si)^+$ ⇨ For importing wafers that were processed outside the class100 or SAL cleanroom, and that were **not** in contact with metal layers. **APPROVAL** for importing is needed.
- HNO_3 99% (Si) ⇨ To remove organic material from wafers which were not in contact with metal layers.
- HNO3 69.5% (Si) ⇨ To remove (possible) metal particles caused by wafer handling.
  It is **NEVER** allowed to use this bath for wet etching or stripping of metal layers!
- HNO_3 99% $(green\ metals)^+$ ⇨ For importing wafers that were processed outside the class100 or SAL cleanroom, and that were in contact with "green" metals. **APPROVAL** for importing is needed.
- HNO_3 99% (green metals) ⇨ To remove organic material on wafers which are or have been in contact with "green" metals (e.g.: Al, Al(1%Si), Ti, Mo, Zr, …).

Note:
- The above described cleaning procedures are only valid for CMOS compatible wafers with CMOS compatible materials on them. **For all other wafers follow the PCC rules and check the Phoenix Materials database.**
- Wafers do **NOT** have to be cleaned **after** a furnace, epitaxy or deposition step if the next process step will be performed immediately, unless the wafers are covered with particles.

FURNACE RESTRICTIONS

Wafers that are covered with photoresist or a metal layer may **NEVER** be processed in any of the furnaces. This also applies for wafers from which a metal layer has been removed by etching. Only alloying in tube C4 is allowed for wafers with an aluminium layer.

MEASUREMENTS

Always perform all the measurement and inspection steps, and **write down the results in your journal and in the logbooks that can be found at some of the equipment**. The results are used to monitor the processes and/or equipment.

It is possible to measure directly on your (CMOS compatible) process wafers with the following Class 100 equipment:

- The WOOLLAM and the KEYENCE microscope. The Woollam is used for thickness measurements of transparent layers, and the Keyence is used for 3D surface metrology. The measurements are non-destructive and without contact to the wafer surface.
- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface, which can be destructive for certain structures. It is a **contact** measurement.
- The Hitachi SEM, which can be used for inspection of your wafers and for width, depth or thickness measurements.

Note: ▪ After a **contact** measurement **cleaning of the wafer** is required for further processing.
▪ An extra wafer must be processed when other measurements are required (like sheet resistance and junction depth measurements). These wafers can not be used for further processing.

STARTING MATERIAL

Use **Single SIDE** polished **LOW RESISTIVITY (LRES)** wafers, with the following specifications:

Type:	p / boron
Orientation:	<100>
Resistivity:	1-5 Ωcm
Thickness:	525 ± 15 μm
Diameter:	100 mm

Zero layer definition:

1. COATING

Tool(s):	EVG120 system
Location:	CR 100 - Tunnel 1B (Litho)
Recipe name(s):	**1-Co - 3012 - zero layer – No EBR**
Settings:	No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "1-**Co - 3012 - zero layer – No EBR**".

2. ALIGNMENT AND EXPOSURE

Tool(s):	ASML PAS5500/80 automatic wafer stepper
Location:	CR 100 - Tunnel 1B (Litho)
Recipe name(s):	**Litho\ZEFWAM** | Energy: 140mJ/ cm2
Settings:	mask – COMURK

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **mask COMURK** with job **Litho\ZEFWAM** | Energy: 140mJ/ cm2

3. DEVELOPING

Tool(s):	EVG120 system
Location:	CR 100 - Tunnel 1B (Litho)
Recipe name(s):	**1-Dev - SP**
Settings:	No EBR

Use the developer station of the EVG120 system to develop the wafers. The process consists of: ▪ a post-exposure bake at 115 °C for 90 seconds

- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

4. INSPECTION

Visually inspect the wafers through a microscope:

- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

5. WAFER NUMBERING

Use the glass pen in the lithography room to mark the wafers with the **BATCH** and **WAFER** number.
Write the numbers in the photoresist, just above the waferflat. Always do this after exposure and development. It is **NOT** allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

6. PLASMA ETCHING: Alignment markers into Silicon

Tool(s): Trikon Ωmega 201 plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **urk_npd | 20ºC**
Settings: standard

Process conditions from chamber recipe URK_ETCH:						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

7. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

8. CLEANING: HNO_3 99% and 69.5%

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 100ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the red dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

OXIDE DEFINITION

9. PECVD DEPOSITION: 500 nm of SiO2

Tool(s): Novellus Concept One PECVD reactor
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **.xxx_siostd**
Settings: Define a certain time to deposit specific thickness of oxide.

Process conditions from recipe .xxx_siostd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ = 3150/205/6000 sccm	2.2 Torr	1000 W	0 W	400 °C	7.2 sec

Note: ▪ The layer thickness depends on the station deposition time (SDT), which can be calculated from the average deposition rate during recent recipe usage. This can be found in the logbook of the system.
- An extra test wafer can be deposited for measurements and etch tests.

10. MEASUREMENT: Oxide thickness

Tool(s): Woollam Ellipsometer
Location: CR 100 - Tunnel 2 (Metrology)
Recipe name(s): **follow the instructions from the manual**
Settings: Follow instructions from the manual.

Expected layer thickness: 500 nm

11. COATING

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3012 – 2.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3012 – 2.1µm – No EBR** ".

12. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80 automatic wafer stepper
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **Diesize_10mm\DIE10x10_4IMG\ID: 2** | Energy: 260mJ/ cm2
Settings: mask – COMURK

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **mask CO** with job **Diesize_10mm\DIE10x10_4IMG\ID: 2** | Energy: 260mJ/ cm2

13. DEVELOPING

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of: ▪
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

14. INSPECTION

Visually inspect the wafers through a microscope:

- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

15. PLASMA ETCHING: 500 nm Silicon Oxide

Tool(s): Drytek Triode 384T plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **stdoxide**
Settings: Define a certain time to etch specific thickness of oxide.

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
The etching depth is tuned by the time.

Use recipe **stdoxide** to etch **500 nm** thick SiO2 layer.

Process conditions from recipe: stdoxd					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	1 min 15 sec

16. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

17. CLEANING: HNO_3 99% and 69.5%

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 100ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the red dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

METAL DEPOSITION AND DEFINITION

18. WET ETCHING: Oxide dip etch. Marangoni system to remove native oxide and do Marangoni drying

Process conditions		
Etch	0.55% HF	Use wet bench "0.55% HF" at ambient temperature, and the carrier with the black dot for 4 minutes
Rinse	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the black dot to the carrier with the black dot of the Avenger
Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dot.

19. METALLIZATION: 500 nm Al (with 1%Si)

Tool(s): TRIKON SIGMA 204 sputter coater
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **AlSi_500nm_350C**
Settings: Use a target clean recipe first if the deposition chamber hasn't been used for a long time or if it has deposited some other kind of material before in the same department. Temperature at 350 ºC with an Ar flow of 100 sccm

Use the TRIKON SIGMA 204 sputter coater for the deposition of an aluminium metal layer on the wafers.
The target must exist of 99% Al and 1% Si, and deposition must be done at 350 °C with an Ar flow of 100 sccm. Follow the operating instructions from the manual when using this machine.

Use recipe **"AlSi_500nm_350C"** to obtain a **500 nm** thick layer.

Visual inspection: the metal layer must look shiny.

20. COATING

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3012 – 2.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3012 – 2.1µm – No EBR** ".

21. ALIGNMENT AND EXPOSURE

Tool(s): ASML PAS5500/80 automatic wafer stepper
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **Diesize_10mm\DIE10x10_4IMG\ID: 2** | Energy: 260mJ/ cm2
Settings: mask – COMURK

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **mask NO** with job **Diesize_10mm\DIE10x10_4IMG\ID: 2** | Energy: 260mJ/ cm2

22. DEVELOPING

Tool(s): EVG120 system

Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

23. INSPECTION

Visually inspect the wafers through a microscope:
- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

24. PLASMA ETCHING:

Tool(s): Trikon Ωmega 201 plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **al05_350 | 25ºC**
Settings: standard

Process conditions from chamber recipe al05_350:						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	Cl_4/HBr = 30/40 sccm	5 mTorr	50 W	500 W	25 °C	0'15"
2. bulk etch	Cl_2/HBr = 30/40 sccm	5 mTorr	40 W	500 W	25 °C	0'50"
3. overetch	Cl_2/HBr = 15/30 sccm	5 mTorr	40 W	500 W	25 °C	endpoint

25. LAYER STRIPPING: Photoresist

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

26. CLEANING: HNO_3 99% metal

Tool(s): Wet bench, modules "HNO_3 99% (metal)", QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red and yellow dot for the cleaning in HNO_3 99% and rinse 1, use the wafer carrier with the black dot for the Avenger Ultra pure.

Note **Do not perform a "HNO_3 69,5% 110C (Si)" cleaning step!**

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature

Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red and yellow dot to the carrier with the black dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dot.

D

Final device flowchart

3D Microelectrode Integration in Muscle-on-Chip Device

FLOWCHART

BATCH INFORMATION			
NAME OF OWNER :	Ramón Carballás Boluda	MASK SET :	PDM 16
NAME OF MENTOR :	Massimo Mastrangeli	MASK BOX :	269A and 269 B
RUN NUMBER :		DIE SIZE :	10 by 10 mm
WAFER AMOUNT :	4	START DATE :	/ /
SUBJECT TO PCC :	no	PCC APPROVED :	n.a.

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GENERAL RULES

CLEANROOM BEHAVIOUR

❶ Always follow the "**Security and Behavior**" rules when working in the EKL laboratories.

❷ Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible!

❸ Use cleanroom gloves when working with vacuum equipment. Do not touch the inside or carriers with bare hands.

❹ Always check equipment and process conditions before starting a process. Do **NOT** make unauthorized changes!

❺ Directly notify the responsible staff member(s) when there are problems with the equipment (like malfunction or contamination). Flip the status card on the machine over to **DOWN** to warn other users. Also change the status of the system to **DOWN** in the "Phoenix Living Database" system.

❻ **DO NOT TRY TO REPAIR OR CLEAN EQUIPMENT YOURSELF**, and **NEVER** try to refresh a contaminated etch or cleaning bath! Only authorized staff members are allowed to do this.

WORKING WITH CMOS INCOMPATIBLE MATERIALS

❶ Substrates, layers and chemicals which are not CMOS compatible may cause contamination of bathes, equipment, wafer boxes, etc.. Using these materials in the class 100 and SAL cleanroom without permission is **FORBIDDEN.**

❷ The use of CMOS incompatible materials for processing in the class100 and SAL cleanroom must **ALWAYS BE EVALUATED** and **APPROVED** by your mentor and the EKL contamination officer.

❸ Wafers that are contaminated may **NEVER** be processed in any of the bathes or equipment without permission. Special precautions may be required, like the use of a separate container, a special substrate holder or a wafer carrier.

❹ You **MUST** work according to the rules described in the **Preventive Cross Contamination** (PCC) document, available on the "EKL Sharepoint webpage", and the **Materials** database from the "Phoenix Living Database" system.

CLEANING OF WAFERS

Wafers must always be cleaned before performing a **COATING, FURNACE, EPITAXY** or **DEPOSITION** step if they were stored for 4 hours or more.

Use the correct cleaning bathes:

- Acetone ⇨ To remove photoresist that is not used as a mask for ion implantation or plasma etching.
- Tepla stripper ⇨ To remove ion bombarded photoresist after implantion or plasma etching.
- HNO_3 99% $(Si)^+$ ⇨ For importing wafers that were processed outside the class100 or SAL cleanroom, and that were **not** in contact with metal layers. **APPROVAL** for importing is needed.
- HNO_3 99% (Si) ⇨ To remove organic material from wafers which were not in contact with metal layers.
- HNO3 69.5% (Si) ⇨ To remove (possible) metal particles caused by wafer handling.
  It is **NEVER** allowed to use this bath for wet etching or stripping of metal layers!
- HNO_3 99% (green metals)$^+$ ⇨ For importing wafers that were processed outside the class100 or SAL cleanroom, and that were in contact with "green" metals. **APPROVAL** for importing is needed.
- HNO_3 99% (green metals) ⇨ To remove organic material on wafers which are or have been in contact with "green" metals (e.g.: Al, Al(1%Si), Ti, Mo, Zr, …).

Note:
- The above described cleaning procedures are only valid for CMOS compatible wafers with CMOS compatible materials on them. **For all other wafers follow the PCC rules and check the Phoenix Materials database.**
- Wafers do **NOT** have to be cleaned **after** a furnace, epitaxy or deposition step if the next process step will be performed immediately, unless the wafers are covered with particles.

FURNACE RESTRICTIONS

Wafers that are covered with photoresist or a metal layer may **NEVER** be processed in any of the furnaces. This also applies for wafers from which a metal layer has been removed by etching. Only alloying in tube C4 is allowed for wafers with an aluminium layer.

MEASUREMENTS

Always perform all the measurement and inspection steps, and **write down the results in your journal and in the logbooks that can be found at some of the equipment**. The results are used to monitor the processes and/or equipment.

It is possible to measure directly on your (CMOS compatible) process wafers with the following Class 100 equipment:

- The WOOLLAM and the KEYENCE microscope. The Woollam is used for thickness measurements of transparent layers, and the Keyence is used for 3D surface metrology. The measurements are non-destructive and without contact to the wafer surface.
- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface, which can be destructive for certain structures. It is a **contact** measurement.
- The Hitachi SEM, which can be used for inspection of your wafers and for width, depth or thickness measurements.

Note: ▪ After a **contact** measurement **cleaning of the wafer** is required for further processing.
▪ An extra wafer must be processed when other measurements are required (like sheet resistance and junction depth measurements). These wafers can not be used for further processing.

STARTING MATERIAL

Use **Double SIDE** polished **LOW RESISTIVITY (LRES)** wafers,
with the following specifications:

Type:	p / boron
Orientation:	<100>
Resistivity:	1-5 Ωcm
Thickness:	525 ± 15 μm
Diameter:	100 mm

Zero layer definition:

1. COATING ·Back side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3012 - zero layer – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "1-**Co - 3012 - zero layer – No EBR**".

2. ALIGNMENT AND EXPOSURE • Back side

Tool(s): ASML PAS5500/80 automatic wafer stepper
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **Litho\ZEFWAM** | Energy: 140mJ/ cm2
Settings: mask – COMURK

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose **mask COMURK** with job **Litho\ZEFWAM** | Energy: 140mJ/ cm2

3. DEVELOPING • Back side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: No EBR

Use the developer station of the EVG120 system to develop the wafers. The process consists of: ▪ a post-exposure bake at 115 °C for 90 seconds

- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

4. INSPECTION • Back side

Visually inspect the wafers through a microscope:

- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

5. WAFER NUMBERING • Back side

Use the glass pen in the lithography room to mark the wafers with the **BATCH** and **WAFER** number.
Write the numbers in the photoresist, just above the waferflat. Always do this after exposure and development. It is **NOT** allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

6. PLASMA ETCHING: Alignment markers into Silicon • Back side

Tool(s): Trikon Ωmega 201 plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **urk_npd | 20ºC**
Settings: standard

Process conditions from chamber recipe URK_ETCH:						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

7. LAYER STRIPPING: Photoresist • Both sides

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

8. CLEANING: HNO_3 99% and 69.5% · Both sides

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 100ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the red dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

FIRST OXIDE LAYER TO DEFINE PILLARS AND ETCHING IN SILICON

9. PECVD DEPOSITION: 1.5 µm of SiO2 ·Front side

Tool(s): Novellus Concept One PECVD reactor
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **.xxx_siostd**
Settings: Define a certain time to deposit specific thickness of oxide.

Process conditions from recipe .xxx_siostd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ = 3150/205/6000 sccm	2.2 Torr	1000 W	0 W	400 °C	21.2 sec

Note: ▪ The layer thickness depends on the station deposition time (SDT), which can be calculated from the average deposition rate during recent recipe usage. This can be found in the logbook of the system.
▪ An extra test wafer can be deposited for measurements and etch tests.

10. MEASUREMENT: Oxide thickness • Front side

Tool(s): Woollam Ellipsometer
Location: CR 100 - Tunnel 2 (Metrology)
Recipe name(s): **follow the instructions from the manual**
Settings: Follow instructions from the manual.

Expected layer thickness: 1.5 µm

11. COATING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3027 – 3.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
▪ a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
▪ spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
▪ an automatic edge bead removal with a solvent
Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3027 – 3.1µm – No EBR** ".

12. ALIGNMENT AND EXPOSURE • Front side

Tool(s): SUSS MicroTec MA/BA8 mask aligner
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **BSA_soft_contact**
Settings: mask – Oxide 1 | Energy: 500mJ/ cm2 **|** time of exposure: 22.3 sec

Expose **mask Oxide1** with job **BSA_soft_contact** | Energy: 500 mJ/ cm2 (time = energy divided by the intenisity of lamp) be careful with the energies depending of the thickness of the photoresist

13. DEVELOPING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of: ▪
a post-exposure bake at 115 °C for 90 seconds
▪ developing with Shipley MF322 with a single puddle process
▪ a hard bake at 100 °C for 90 seconds
Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

14. INSPECTION • Front side

Visually inspect the wafers through a microscope:

- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

15. PLASMA ETCHING: 1.5 µm Silicon Oxide • Front side

Tool(s): Drytek Triode 384T plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **stdoxide**
Settings: Define a certain time to etch specific thickness of oxide.

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
The etching depth is tuned by the time.

Use recipe **stdoxide** to etch **1.5 µm** thick SiO2 layer.

Process conditions from recipe: stdoxd					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	3 min

16. LAYER STRIPPING: Photoresist • Both sides

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

17. CLEANING: HNO_3 99% and 69.5% • Both sides

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 100ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the red dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

THESE FOLLOWING STEPS ARE TO DEFINE THE OTHER SIDE OF THE WAFER

18. PECVD DEPOSITION: 5 µm of SiO2 • Back side

Tool(s): Novellus Concept One PECVD reactor
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **.xxx_siostd**
Settings: Define a certain time to deposit specific thickness of oxide.

Process conditions from recipe .xxx_siostd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ = 3150/205/6000 sccm	2.2 Torr	1000 W	0 W	400 °C	65.4 sec

Note: ▪ The layer thickness depends on the station deposition time (SDT), which can be calculated from the average deposition rate during recent recipe usage. This can be found in the logbook of the system.
▪ An extra test wafer can be deposited for measurements and etch tests.

19. MEASUREMENT: Oxide thickness • Back side

Tool(s): Woollam Ellipsometer
Location: CR 100 - Tunnel 2 (Metrology)
Recipe name(s): **follow the instructions from the manual**
Settings: Follow instructions from the manual.

Expected layer thickness: 5 µm

20. COATING • Back side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3027 – 3.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3027 – 3.1µm – No EBR** ".

21. ALIGNMENT AND EXPOSURE • Back side

Tool(s): SUSS MicroTec MA/BA8 mask aligner
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **FSA_hard_contact**
Settings: mask – OxideTurtle | Energy: 865mJ/ cm2 **|** time of exposure: 44.4 sec

Expose **mask OxideTurtle** with job **FSA_hard_contact** | Energy: 865 mJ/ cm2 (time = energy divided by the intenisity of lamp) be careful with the energies depending of the thickness of the photoresist

22. DEVELOPING • Back side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)

Recipe name(s): **Dev – TP1**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev – TP1**".

23. INSPECTION • Back side

Visually inspect the wafers through a microscope:
- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

24. PLASMA ETCHING: 5 µm Silicon Oxide • Back side

Tool(s): Drytek Triode 384T plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **stdoxide**
Settings: Define a certain time to etch specific thickness of oxide.

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
The etching depth is tuned by the time.

Use recipe **stdoxide** to etch **5 µm** thick SiO2 layer.

Process conditions from recipe: stdoxd					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	13 min

25. LAYER STRIPPING: Photoresist • Both sides

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

26. CLEANING: HNO_3 99% and 69.5% • Both sides

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 100ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the red dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

FIRST SiN LAYER TO ENCAPSULATE THE METAL LINE

27. PECVD DEPOSITION: 200 nm of SiN ·Front side

Tool(s): Novellus Concept One PECVD reactor
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **xxnm_std_sin**
Settings: Define a certain time to deposit specific thickness of oxide.

Process conditions from xxnm_std_sin:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/NH_3$ = 1000/280/1800 sccm	2.8 Torr	320 W	480 W	400 °C	8.25 sec

Note: ▪ The layer thickness depends on the station deposition time (SDT), which can be calculated from the average deposition rate during recent recipe usage. This can be found in the logbook of the system.
▪ An extra test wafer can be deposited for measurements and etch tests.

28. COATING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3027 – 3.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3027 – 3.1µm – No EBR** ".

29. ALIGNMENT AND EXPOSURE • Front side

Tool(s): SUSS MicroTec MA/BA8 mask aligner
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **BSA_soft_contact**
Settings: mask – SiN -1 | Energy: 500mJ/ cm2 | time of exposure: 22.3 sec

Expose **mask SiNx 1** with job **BSA_soft_contact** | Energy: 500mJ/ cm2

30. DEVELOPING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

31. INSPECTION • Front side

Visually inspect the wafers through a microscope:
- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

32. PLASMA ETCHING: 200 nm Silicon Nitride • Front side

Tool(s): Drytek Triode 384T plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **stdSiN**
Settings: Define a certain time to etch specific thickness of silicon nitride.

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
The etching depth is tuned by the time.

Use recipe **stdSiN** to etch **200 nm** thick SiNx layer.

Process conditions from recipe silicon nitride:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6 = 65 sccm	130 mTorr	250 W	8 Torr	30 sec

33. LAYER STRIPPING: Photoresist • Both sides

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

34. CLEANING: HNO_3 99% and 69.5% • Both sides

Tool(s): Wet bench, modules HNO_3 99%, HNO_3 69.5% 110ºC, QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red dot for the cleaning in HNO_3 99%, rinse 1, HNO_3 69.5% and rinse 2, use the wafer carrier with the red dot for rinse 3. Check if temperature of the HNO_3 69.5% is 110ºC

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Clean 2	HNO_3 69.5%	Immerse the wafers for 10 min. Temperature is 100ºC
Rinse 2	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red dot to the carrier with the red dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

MARANGONI

35. WET ETCHING: Oxide dip etch. Marangoni system to remove native oxide and do Marangoni drying

Process conditions		
Etch	0.55% HF	Use wet bench "0.55% HF" at ambient temperature, and the carrier with the black dot for 4 minutes
Rinse	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the black dot to the carrier with the black dot of the Avenger
Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dot.

Note: Metallization must be performed immediately after drying

DEPOSITION OF METAL LINE

36. METALLIZATION: 500 nm Al (with 1%Si) • Front side

Tool(s): TRIKON SIGMA 204 sputter coater
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **AlSi_500nm_350C**
Settings: Use a target clean recipe first if the deposition chamber hasn't been used for a long time or if it has deposited some other kind of material before in the same department. Temperature at 350 ºC with an Ar flow of 100 sccm

Use the TRIKON SIGMA 204 sputter coater for the deposition of an aluminium metal layer on the wafers.
The target must exist of 99% Al and 1% Si, and deposition must be done at 350 °C with an Ar flow of 100 sccm. Follow the operating instructions from the manual when using this machine.

Use recipe **"AlSi_500nm_350C"** to obtain a **500 nm** thick layer.

Visual inspection: the metal layer must look shiny.

37. COATING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3027 – 3.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas

- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3027 – 3.1µm – No EBR**".

38. ALIGNMENT AND EXPOSURE • Front side

Tool(s): SUSS MicroTec MA/BA8 mask aligner
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **BSA_soft_contact** | Energy: 500mJ/ cm2 **|** time of exposure: 22.3 sec
Settings: mask – Metal

Expose **mask - Metal** with job **BSA_soft_contact** | Energy: 500mJ/ cm2

39. DEVELOPING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of: ▪ a post-exposure bake at 115 °C for 90 seconds

- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

40. INSPECTION • Front side

Visually inspect the wafers through a microscope:

- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

41. PLASMA ETCHING: Define the metal line • Front side

Tool(s): Trikon Ωmega 201 plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **al05_350 | 25ºC recipe to etch Al/Si**
Settings: standard to etch away **500 nm** of Al/Si

Process conditions from chamber recipe al05_350:						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	HBr/ Cl_2 = 40/30 sccm	5 mTorr	50 W	500 W	25 °C	0'15"
2. bulk etch	HBr/ Cl_2 = 40/30 sccm	5 mTorr	40 W	500 W	25 °C	0'40"
3. overetch	HBr/ Cl_2 = 30/15 sccm	5 mTorr	40 W	500 W	25 °C	endpoint

42. LAYER STRIPPING: Photoresist • Both sides

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.

Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

43. CLEANING: HNO_3 99% metal • Both sides

Tool(s): Wet bench, modules "HNO_3 99% (metal)", QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red and yellow dot for the cleaning in HNO_3 99% and rinse 1, use the wafer carrier with the black dot for the Avenger Ultra pure.

Note **Do not perform a "HNO_3 69,5% 110C (Si)" cleaning step!**

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red and yellow dot to the carrier with the black dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dot.

DEPOSITION OF SECOND LAYER OF SiN FOR ENCAPSULATING THE METAL LINE

44. PECVD DEPOSITION: 200 nm of SiN ·Front side

Tool(s): Novellus Concept One PECVD reactor
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **xxnm_std_sin**
Settings: Define a certain time to deposit specific thickness of oxide.

Process conditions from xxnm_std_sin:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/NH_3$ = 1000/280/1800 sccm	2.8 Torr	320 W	480 W	400 °C	8.25 sec

Note: ▪ The layer thickness depends on the station deposition time (SDT), which can be calculated from the average deposition rate during recent recipe usage. This can be found in the logbook of the system.
▪ An extra test wafer can be deposited for measurements and etch tests.

Note that the wafer must not leave the chamber in between these two steps. They must be done one after the other everything in vaccum

DEPOSITION OF SAMLL LAYER OF OXIDE

45. PECVD DEPOSITION: 100 nm of SiO2 ·Front side

Tool(s): Novellus Concept One PECVD reactor
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **.xxx_siostd**
Settings: Define a certain time to deposit specific thickness of oxide.

Process conditions from recipe .xxx_siostd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ = 3150/205/6000 sccm	2.2 Torr	1000 W	0 W	400 °C	1.5 sec

Note: ▪ The layer thickness depends on the station deposition time (SDT), which can be calculated from the average deposition rate during recent recipe usage. This can be found in the logbook of the system.
▪ An extra test wafer can be deposited for measurements and etch tests.

Be careful with the minimum time inside the Novellus (tryout 100 nm)

ETCHING OF SiN AND SiO2 TO OPEN CONTACT PADS AND REMOVE IN WELL

46. COATING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3027 – 3.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
▪ a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
▪ spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
▪ an automatic edge bead removal with a solvent
Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3027 – 3.1µm – No EBR** ".

47. ALIGNMENT AND EXPOSURE • Front side

Tool(s): SUSS MicroTec MA/BA8 mask aligner
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **BAS_soft_contact** | Energy: 500mJ/ cm2 **|** time of exposure: 22.3 sec
Settings: mask – SiNx 2

Expose **mask SiNx 2** with job **BAS_doft_contact** | Energy: 500 mJ/ cm2

48. DEVELOPING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Dev - SP**
Settings: Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of: ▪
a post-exposure bake at 115 °C for 90 seconds
▪ developing with Shipley MF322 with a single puddle process
▪ a hard bake at 100 °C for 90 seconds
Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

49. INSPECTION • Front side

Visually inspect the wafers through a microscope:
▪ No resist residues are allowed.
▪ Check the linewidth of the structures.
▪ Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

50. PLASMA ETCHING: 100 nm Silicon Oxide and 400 nm Silicon Nitride • Front side

Tool(s): Drytek Triode 384T plasma etcher
Location: CR 100 - Tunnel 3 (Plasma)
Recipe name(s): **stdSiN**
Settings: Define a certain time to etch specific thickness of oxide.

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
The etching depth is tuned by the time.

Use recipe **stdSiN** to etch 400 nm thick SiNx layer and also the thin layer of 100 nm SiO2 on top.

Process conditions from recipe silicon nitride:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6 = 65 sccm	130 mTorr	250 W	8 Torr	1 min 12 sec

51. LAYER STRIPPING: Photoresist • Both sides

Tool(s): Tepla Plasma 300
Location: CR 100 - Tunnel 5
Recipe name(s): **program 1**
Settings: standard

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

52. CLEANING: HNO_3 99% metal • Both sides

Tool(s): Wet bench, modules "HNO_3 99% (metal)", QDR, Avenger Ultra pure-6
Location: CR 100 - Tunnel 5
Recipe name(s): **Default recipe for the Avenger Ultra pure-6 rinse/dry tool**
Settings: Use the white wafer carrier labelled with the red and yellow dot for the cleaning in HNO_3 99% and rinse 1, use the wafer carrier with the black dot for the Avenger Ultra pure.

Note **Do not perform a "HNO_3 69,5% 110C (Si)" cleaning step!**

Process conditions		
Clean 1	HNO_3 99%	Immerse the wafers for 10 min. Temperature is room temperature
Rinse 1	DI water	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Wet transfer		Use the transfer system next to the HN to move the wafers from the carrier with the red and yellow dot to the carrier with the black dot of the Avenger
Rinse 3/Dry	DI water	Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dot.

DEPOSITION OF THIN PHOTORESIST

53. COATING • Front side

Tool(s): EVG120 system
Location: CR 100 - Tunnel 1B (Litho)
Recipe name(s): **1-Co - 3027 – 3.1µm – No EBR**
Settings: No EBR

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump ▪ a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**1-Co - 3027 – 3.1µm – No EBR** ".

54. ALIGNMENT AND EXPOSURE • Front side

Tool(s):	SUSS MicroTec MA/BA8 mask aligner
Location:	CR 100 - Tunnel 1B (Litho)
Recipe name(s):	**BAS_soft_contact** | Energy: 500mJ/ cm2 | time of exposure: 22.3 sec
Settings:	mask – Small photoresist

Expose **mask Small photoresist** with job **BAS_soft_contact** | Energy: 140mJ/ cm2

55. DEVELOPING • Front side

Tool(s):	EVG120 system
Location:	CR 100 - Tunnel 1B (Litho)
Recipe name(s):	**1-Dev - SP**
Settings:	Standard

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "1-**Dev - SP**".

56. INSPECTION • Front side

Visually inspect the wafers through a microscope:
- No resist residues are allowed.
- Check the linewidth of the structures.
- Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

DEPOSITION OF PDMS

57. DEPOSITION OF PDMS: Done by Bi/ond 250µm • Back side

RELEASE OF THE PILLARS ON THE PDMS MEMBRANE

58. DRIE ETCHING: 525 µm of Si • Back side

Tool(s):	Rapier Omega i2L DRIE etcher
Location:	CR 100 - Tunnel 2
Recipe name(s):	**0EKL_smooth_xxx**
Settings:	665 cycles

Use the Rapier Omega i2L DRIE etcher
Use the recipe: **0EKL_smooth_xxx** to etch **525 µm** of Si

59. WET ETCHING: HF 5% bath • Both sides

Tool(s):	Wet benches in CR10000
Location:	CR 10000
Recipe name(s):	**releasing the PDMS membrane**
Settings:	the quantities of the

- Go to the Wet benches in CR10000, prepare a solution of 5 % HF.
- Submerge the wafer in the solution for 3 minutes
- Rinse in DI water and dry