A GaN-based Power Factor Correction Converter

for Electric Vehicle Charging

Dingsihao Lyu

Technische Universiteit Delft

TU Delft Delft University of Technology

Challenge the future

A GaN-based Power Factor Correction Converter

for Electric Vehicle Charging

by

Dingsihao Lyu

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Company supervisor:	Ir. Stefan Raaijmakers,	ABB
Educational daily supervisor:	Dr. Z. Qin	
Thesis committee:	Prof. dr. ir. P. Bauer,	TU Delft
	Prof. dr. Arno Smets,	TU Delft
	Dr. ir. Gautham Chandra Ram Mouli,	TU Delft

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Preface

Because of its superior conduction and switching performance, and falling price, Gallium Nitride (GaN) power semiconductor device is expected to bring improvements to the power electronics system, including higher efficiency and higher power density.

How will the new semiconductor device benefit the rapidly growing Electric Vehicle (EV) charging application, where high efficiency, high power density are two of the most important design requirements? In order to verify the match between the new semiconductors and the EV charger application, hardware demonstration needs to be carried out. In this thesis project, the design of a GaN-based, high switching frequency, single-phase, $2KW$ PFC converter for EV charging will be introduced. The operation principle and control of the converter will be explained, and the hardware demonstration results will be shown. The test results prove the high-efficiency, high-frequency advantages of the new technology. This thesis is undertaken in collaboration with ABB.bv.

In truth, I could not have finished the project without the support from many people. First of all, my parents, who offered unwavering support with love. Secondly, my supervisor in ABB, Stefan Raaijmakers, who provided valuable advice and guidance throughout the project, and helped me with the hardware layout. Moreover, my educational supervisor Dr. Zian Qin, who gave critical feedback through the project, and helped me with the thesis writing. Thank you all for your help.

Lyu
Delft, August, 2019

Contents

1

Introduction

1.1. Thesis Background

The development of power electronics is driven by 1. the ”push” from innovations of the technology itself, which includes improvements in power semiconductor devices, circuits or topologies, control, passive components, and packaging technology, etc; 2. the ”pull” from the requirements of the applications that it is used in[1].

Technology Push: Development of Wide Band-Gap Power Semiconductor

Wide BandGap (WBG) materials, especially Gallium Nitride (GaN) and Silicon Carbide (SiC), are gaining more and more attention in the field of power electronics. Due to the different material properties and the structures compared to the silicon counterparts, the new devices promise to break the physical limits of the well-established Si components in terms of voltage blocking capability, maximum operation temperature, conduction and switching characteristics. These advantages make WBG device a strong competitor to its silicon counterpart, and bring better efficiency and higher power density to the power electronics system with WBG devices theoretically [2] [3] [4] [5], especially in the applications of automotive, industrial motor drives, PV inverters, UPS for data centers, and tractions, etc., where the requirement for efficiency and/or power density is crucial. Moreover, with the increasing production and the falling costs of the SiC and GaN substrate wafer, the price of the WBG devices is expected to fall [6]. While SiC power semiconductors are believed to be more suitable for high power applications, GaN power semiconductors are targeting high switching frequency power conversion applications, according to their respective material properties[1]. This thesis will be focusing on GaN device only.

Application Pull: Demands of Electric Vehicle Charger

Among the many attempts to reduce the emission from the transportation sector, electrifying transportation is one of the promising approaches with many benefits. Electric Vehicles (EVs) not only have better performance than combustion engine vehicles because of the use of the more efficient power train and electric motors, but most importantly, could it protect the environment by utilizing the renewable energy from the solar panels and wind turbines, and by minimizing tailpipe emissions[7].

The development of EV charging infrastructure, or EV charger, is one of the essential actions that is needed to promote EVs. EV charger is a power conversion device that converts the AC voltage from the grid to a regulated DC voltage and transfers power to charge the battery of EVs. Figure 1.1 shows the electrical connection of an EV charger with two-stage structure, where the front-end Power Factor Correction (PFC) converter serves the function of rectifying AC voltage to a certain DC voltage while improving power factor simultaneously, and the cascaded DC-DC converter further regulates the DC voltage from the output of the PFC converter to a tightly regulated DC voltage to charge EV battery.

There are three most important requirements for EV charger, namely low cost, high efficiency, and high power density.

Low cost is an important measure to all commercial power electronics applications. The cost in a power electronics system mainly includes the cost of active and passive components, mechanical parts (PCB and connectors), thermal parts (heatsink and/or forced cooling systems), etc. While the cost

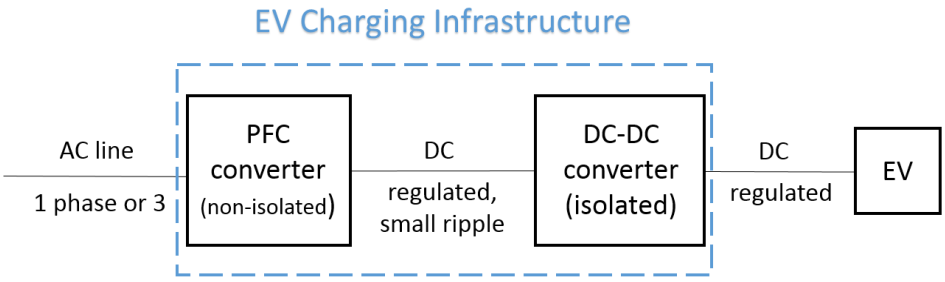


Figure 1.1: Electrical connection of the grid, EV charger and EV

of the active components is heavily determined by the maturity of the technology and the difficulty in manufacturing, the cost of the passive components, as well as the thermal parts, are heavily determined by the size and volume of magnetic and thermal parts. In order to have a lower cost, the primary step is to choose a suitable topology with least bill of materials. Furthermore, cost reduction could be achieved by increasing the switching frequency to reduce the inductance value needed, which potentially reduce the volume of the magnetic components, and by improving the efficiency of the system, so that the losses generated is less and as a result, the size of thermal parts could be reduced [1].

High efficiency is the common goal of power electronics applications. High efficiency means fewer losses dissipated, and this is not only a benefit for an EV charger itself since it will lead to less thermal stress, which could bring lower thermal parts cost and longer lifetime of components, but also does it mean great savings of electricity consumption worldwide[1]. Efficiency is determined by the loss generated on the active and passive components, including the AC switching losses (switching losses on transistors, core loss and AC winding loss on passive components, reverse recovery loss from transistors and diodes) and DC conduction losses on transistors, windings, and PCB traces. The measures that could be taken to increase efficiency include: 1. reduce DC loss by choosing transistor with lower $R_{ds(on)}$ and thicker conductor for winding; 2. reduce AC loss by choosing transistor with faster switching performance and suitable core material for specific frequency range, and apply good design of passive components to minimize AC winding losses.

High power density is preferred in EV charger application because of the limitation of space in vehicles (in the case of an on-board charger) or in wallboxs (in the case of a wallbox charger). Power density could be increased by pushing the switching frequency higher so that the size of the bulky passive components could be reduced.

1.2. Problem Description and thesis objective

For the EV charger suppliers, GaN power semiconductor device is needed to stay competitive, because the superior conduction and switching performance of the GaN power semiconductors, and the dropping price in long term, meet the requirements of the rapidly developing electric vehicle charging application.

In order to practically verify the ability of GaN power transistor of delivering more efficient and higher power density EV charger solution, and understand the design difficulties of the new semiconductors device, technology prototype development, and benchmark testing are demanded. In this thesis project, a design of a single-phase, $2KW$ PFC converter for electric vehicle charging application is entailed for this purpose.

The following research questions need to be answered to achieve the goal:

- **What is the suitable topology for the GaN-based single-phase, $2KW$ PFC?**

  A suitable topology for the PFC converter has to be chosen based on the requirements of 1. low cost, 2. high efficiency, and 3. high power density. The utilizing of GaN transistor has to be considered as well. A literature review of the PFC topologies is needed.

- **What is the optimal operation mode and control strategy?**

  In order to take the most advantage of the new device and the topology, and achieve better efficiency, high power density while keeping the cost low, an optimal operation mode, and the corresponding control strategy need to be chosen. They should give benefit to high-frequency operation.

- **What are the difficulties of practical implementation? And how to accommodate them?**

  In practical power converters there exist various non-ideal behaviours, with which negative effects are brought to the operation. In order to make a practically working converter, the possible non-ideal behaviours need to be identified, and taken into consideration in the design. Their impacts to be understood, and modifications on the control strategy should be made to accommodate them.

This thesis project is carried out in collaboration with ABB B.V.

1.3. Thesis Layout

Chapter 2 presents the comparison of PFC topologies. Various conventional PFC topologies are reviewed with cost and efficiency as the criteria. The limitations of the conventional topologies are analyzed, and improved topologies are reviewed. The advantages of GaN HEMT are introduced, following by the analysis on GaN totem-pole topology. This chapter explains the suitable converter topology for GaN EV charger.

Chapter 3 introduces the operation principle of totem-pole topology for both AC-DC and DC-AC operations with mathematical analysis on the circuit states i.e., the inductor current and switching node voltage.

Chapter 4 performs analysis of resonant transient by using state-plane, and based on the analysis, the ZVS timing control method with controllable ZVS margin of the totem-pole converter is explained, and simulation is carried to demonstrate the feasibility of the control method.

Chapter 5 investigates non-ideal practical issues brought by actual components, mainly the timing issue and circuit parameter issue. The impacts of these non-ideal behaviours are analyzed and demonstrated by simulation. Accordingly, the method of accommodating them to bring the optimal performance is proposed, and comparison simulation is carried out to verify the feasibility.

In **Chapter 6** the hardware demonstration is shown. Firstly, the test set-up is introduced, along with the design difficulties of GaN transistor. secondly, the set-points testing results including the switching waveform and thermal images of the converter are shown and interpreted, efficiencies are measured and recorded.

Chapter 7 concludes this thesis and discusses recommendations derived from the results of this thesis for future research.

2

Comparison of PFC Topologies

2.1. Power Factor Correction

From the electrical point of view, an AC Electrical Vehicle (EV) charger converts the AC voltage from the grid to a regulated DC voltage to charge EVs.

Firstly, the AC voltage provided by the power grid needs to be rectified to a DC voltage. Conventionally this process is done by using a simple full-bridge diode rectifier, cascaded with a big filtering capacitor. However this will result to the drawing of highly distorted current from the grid, which gives a poor power factor[8], Bringing negative effects to the grid as well as to the load, such as injecting harmonic current, causing voltage distortion to the grid, requiring increased V-A rating of the utility equipments[9], slow varying rippled dc output at load end, low efficiency and requiring larger size of AC and DC filters.

In order to maintain good power quality and fulfill the requirement set by various standards such as *EN61000-3-2*, *Energy Star*, etc. [10], Power-Factor-Correction (PFC) circuits are needed to perform the AC-to-DC transition, improving the utility interface of power electronics equipment.

2.2. Design Requirements

- **input voltage**: line input, $f = 50Hz$, $V_{rms} = 230V$
- **output voltage**: $400V \pm 20V$
- the input current has to comply to EN 61000-3-2

There mainly exit two categories of PFC, depending on whether active components are used: *passive* PFC by adding passive components (inductors and capacitors) to the diode bridge rectifier; and *active* PFC, by using a power electronic converter for current shaping.

2.3. Passive PFC

Passive PFC improves the waveform of the current drawn from the grid by adding inductors and capacitors to the conventional diode bridge recitifier. Paper [11] and [12] investigated the feasibility of different passive LC filters for single-phase full-bridge applications, in [13], a LCD filter as a passive PFC circuit is investigated. It is found that the passive PFC is a high cost-effective ratio way to comply the IEC 1000-3-2, EN 61000-3-2 regulation. This approach has some advantages such as simplicity and reliability, however, some obvious disadvantages also exist:

- Even thought the current shape is improved, but there still exists relatively large phase shift between the line voltage and the current drawn, thus the power factor is limited to go better.
- Because of the operation at line frequency, the passive components are bulky, and sometimes needs special mechanical design in order to meet the shock and vibration requirement[14].

- The average DC output voltage is significantly depended on the line voltage and the power drawn by the load[14].

The disadvantages listed above limit the usage of passive PFC, and it is suitable only in low power level cases less than $300 - 400W$, preferably with voltage doubler[12][13][14][15]. Moreover, the market trend of rising cost of copper and magnetic material and falling cost of semiconductor devices has made the active PFC approach a more preferable choice even in cost-sensitive applications [10]. In the EV charging scenario, where regulated output voltage, and high power level (several KW) is desired, active PFC is a more attractive approach.

2.4. Active PFC

Active PFC applies a power electronic converter cascaded to a bridge rectifier, and by controlling the switching of the power electronics converter, the input current shape could be forced to be proportional to the line voltage.

Active PFC converters could be divided into two categories: *single-stage PFC* and *two-stage PFC*. The two-stage PFC converter only acts as a front-end to shape the input current and provides a loosely regulated DC output voltage, leaving the strict DC voltage regulation to the cascaded DC-DC converter. Figure 1.1 is a typical two-stage PFC arrangement. While the single-stage PFC is a more integral approach, performing dual function of AC-DC rectifying with current shaping, as well as DC-DC voltage regulation, thus reduced one power processing stage. Figure 2.1 shows a electrical connection diagram of a charging system using a single-stage PFC approach.

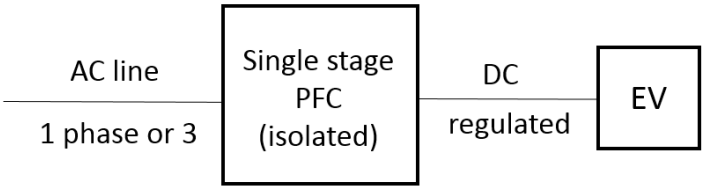


Figure 2.1: The single-stage approach integrating AC-DC PFC and DC-DC regulation

Several studied have been carried out to compare these two different approaches. In [14] [16] [15] [17] and [18], detailed comparison between the single-stage PFC converter and the two-stage PFC converter has been done. It is found out that:

- The capacitance value of the bulk capacitor in a single-stage PFC is much larger than a two-stage PFC in order to meet a certain hold-up time requirement.
- The current ratings of the switches and the rectifiers are higher in a single-stage PFC compared to those of a two-stage PFC with the same output power, which reversely rises the cost and loss. The worst case is the unavailability of components, especially in Discontinuous-Conduction-Mode (DCM) or Boundary-Conduction-Mode (BCM), where the peak current could be more than twice larger than the average current value.
- For the applications that has large range of input voltage, the single stage PFC converter will accordingly has a large range of voltage over the bulk capacitor, which calls for higher voltage rating, so more expensive capacitors compared to the two-stage PFC.
- For the reason above, the single stage PFC is not necessarily cheaper and more efficient compared to the two-stage PFC.

In summary, the single stage PFC is more attractive at narrow input voltage range, and low power levels (less than 700 to $800W$) cases[15] where the components are still available and not expensive, while the efficiency could be as good as two-stage approach. The two-stage PFC is a better choice when the input voltage has a large range, and the power level goes above thousand watts. For a EV charger, even thought the input voltage range is relatively narrow compared to a universal input, because the charger is designed only for one specific market, but the power level is up to several thousands watts high. Moreover, due to the increasing power level of charging, there is a trend to

increase the output voltage level of the EV charger which bringing a large output voltage range (200 to $1000V$) [7], thus the two-stage PFC is a preferable choice. Last but not the least, the most popular type of battery, lithium-ion batteries require low voltage ripple, which is not feasible with single-stage PFC because it has large low frequency ripple in the output[19]. This thesis only focus on the single phase, non-isolated, two-stage PFC approach.

Basic Topologies for PFC: Boost, Buck, Buck-Boost, Cuk, Sepic and Zeta

Many basic topologies have to the potential to be utilized for power-factor-correction purpose. are investigated to check their potential to perform Power-Factor-Correction. In the study of [20], various basic topologies are compared for their possibilities for performing Power-Factor-Correction when working in Discontinuous-Conduction-Mode (DCM), including the basic *buck*, *boost*, *buck-boost*, *Cuk*, *Sepic*, and *Zeta* converters; in [21], the PFC performance of a basic buck and a boost converter operating under Boundary-Conduction-Mode (BCM) are compared.

Boost Converter for PFC

Boost converter is popularly used converter in PFC especially in the case where the output voltage is desired to be higher than the peak of the line voltage[22]. Figure 2.2 shows the circuit diagram for the conventional boost PFC converter.

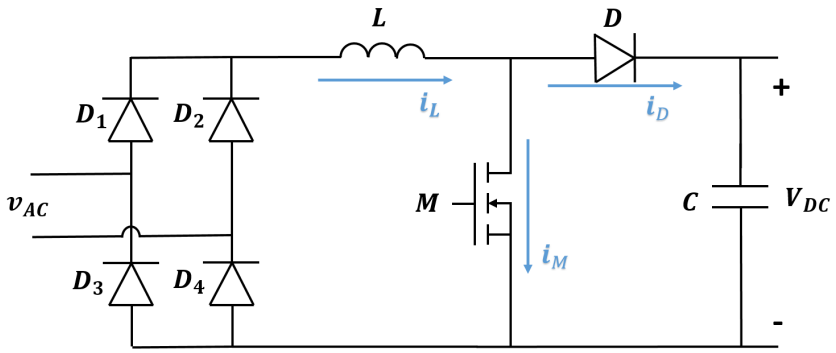


Figure 2.2: Conventional boost PFC converter

The reason this circuit is called boost PFC is that it is simply a boost converter formed by the switch M, diode D, inductor L and capacitor C cascaded to a full-bridge diode rectifier. And the current shaping is performed by controlling the switch of the boost converter according to the input voltage shape. The conventional boost PFC topology is one of the most simple topologies (the others are buck and buck-boost) that calls for the least components.

Figure 2.3 shows the waveform of a boost converter operating in BCM.

From figure 2.3 some observations could be drawn regarding to the rating of the components and the performance limitations.

1. In order to maintain an average current value $I_{L(average)}$, the peak value of the inductor current $I_{L(peak)}$ has to be twice as large as $I_{L(average)}$ (for CCM is smaller, for DCM is even larger). This arises the concern of choosing a switch, diode and inductor with proper current ratings.

2. The switch and the diode have to block the voltage of V_{out} (usually set to be around $400V$). This means the voltage rating of the two components should be larger than V_{out}. Moreover, this high blocking voltage would result to large turn-off losses on the switch.

3. Operating in BCM (and in DCM) has the inherent advantages that the turn-on of the switch is Zero-Current-Switching (ZCS), which would give smaller turn-on loss. and the diode would not suffer from the reverse recovery issue because the current flowing through the diode drops to zero when the diode is turned off. In CCM, reverse recovery of the diode takes up a large part of the switching losses especially when operating in high switching frequency.

In short summary, the conventional boost converter is cost-effective (1 switch, 1 diode, 1 inductor, 1 capacitor) solution for the applications which require the output voltage of PFC to be larger than

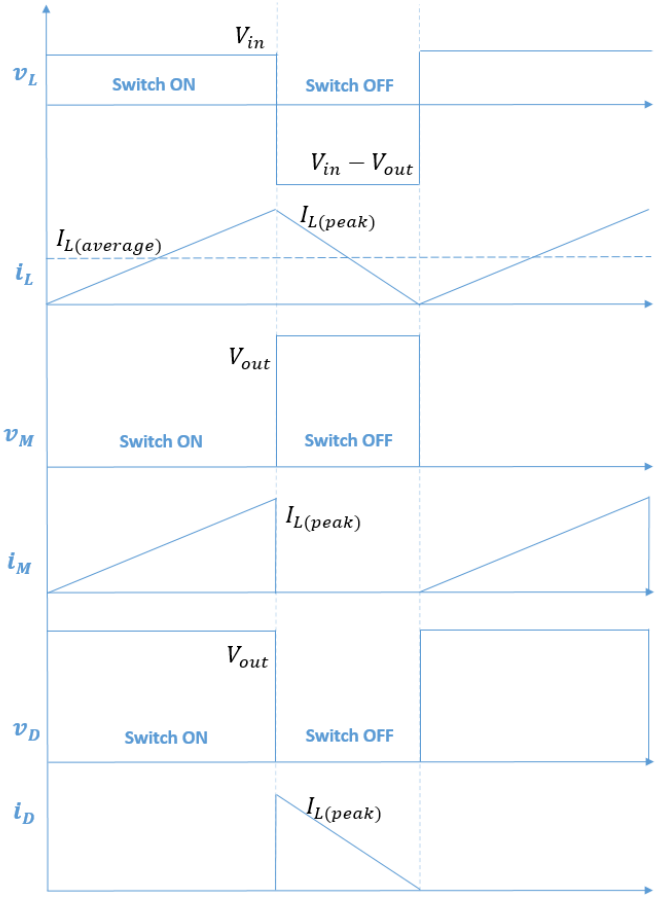


Figure 2.3: the operation waveform of a boost converter in BCM

the peak of the line voltage. However, because of the high blocking voltage, the voltage rating of the switch and the diode is high, and the turn-off loss of the switch is correspondingly potentially high.

Buck Converter for PFC

Buck converter could be applied for PFC where the output voltage of the PFC is desired to be less than the peak value of the line voltage. Figure 2.4 shows the circuit diagram of a conventional buck PFC converter. And figure 2.5 shows the waveform of a buck converter that operates in BCM.

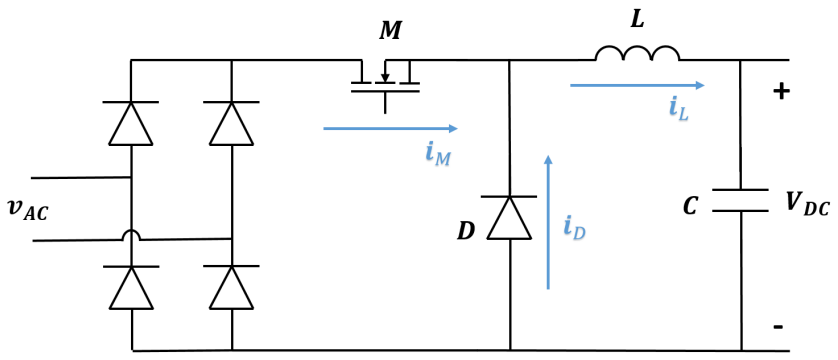


Figure 2.4: Buck converter for PFC

Compared with conventional boost PFC, the buck PFC calls for the same components, however from figure 2.5 it can be seen that, the blocking voltage V_{in} on the switch as well as the diode is smaller than that of a boost PFC (V_{out} around $400V$). This means lower voltage rating components could be used,

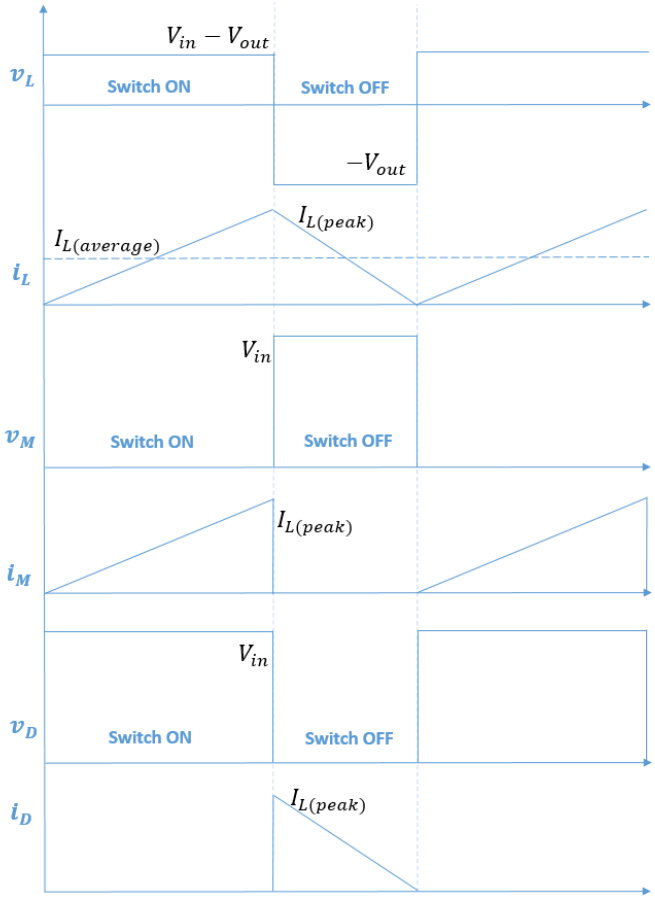


Figure 2.5: the operation waveform of a buck converter in BCM

which is usually cheaper, and the turn-off loss on the switch is theoretically less. However, the drawback of the buck PFC is obvious: it can only operate when the output voltage is lower than the input voltage, due to this reason the current shaping is inherently discontinuous around the zero-crossing point of the line voltage, causing current distortion which is bad for THD[20][21]. Most importantly, since the requirement of this project is to have a around $400V$ output voltage, thus buck PFC is not a candidate in this project.

Buck-Boost Converter for PFC

Figure 2.6 shows a buck-boost PFC circuit, and figure shows the operational waveform in BCM.

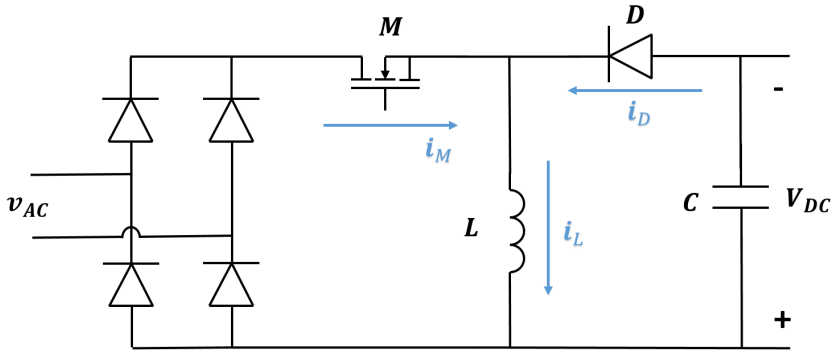


Figure 2.6: Buck-Boost converter for PFC

The buck-boost topology has merits such as the ability to produce either higher or lower output

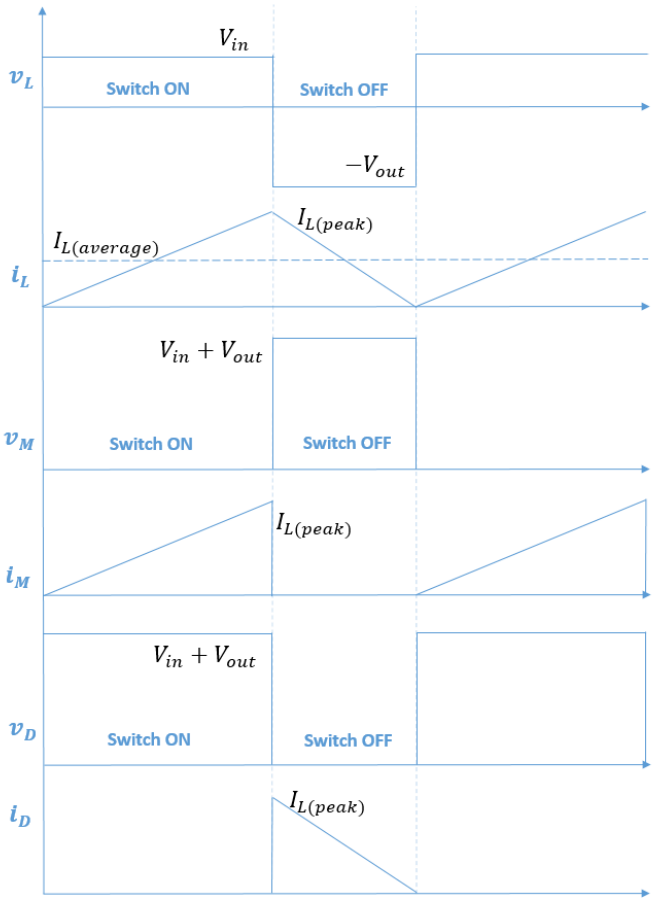


Figure 2.7: the operation waveform of a buck-boost converter in BCM

voltage, and continuous shaping of the input current like boost converter, which buck converter lacks. However, several drawbacks limit the application of this topology for PFC.

1. From figure 2.7, it can be seen that the blocking voltage ($V_{in} + V_{out}$) on the switch as well as that on the diode are even higher than those of the boost PFC, resulting to higher voltage ratings of components and higher turn-off loss on the switch.
2. The output voltage has reverse polarity in respect of the common terminal at input.
3. Since all the power has to be stored in the inductor before transferred to the output, the requirement for the inductor is higher than the previous 2 topologies, in which the power could be directly transfer to the output during certain time period within a cycle.

Cuk, SEPIC, Zeta

These topologies are generally considered as buck-boost variants based on electric circuit principles such as duality [23], thus similar to the buck-boost topology, there is no direct path for the energy transferring, it has to be stored before transferring to the output, resulting to high component stress[24]. Moreover, they all call for addtional passive components, which increases the cost and complexity. In [20] it is found that due to the input V-I characterisitcs of these converters, the input current waveform is naturally distorted, which is not favorable for PFC.

In conclusion, some characteristics for these basic topologies could be drawn:

- *Boost*: As long as the output voltage is larger than the peak of the line voltage, boost converter is able to provide continuous regulation on the input current, and the current shape could be really close to sinusoidal shape. However, cannot perform when the output voltage is lower than the peak of line voltage.

- *Buck*: Unable to operate when the input voltage is less than the output voltage, thus naturally causing the discontinuity of the input current. If the output voltage is required to be larger than the peak of the line voltage, buck couldn't be used.
- *Buck-Boost*: Could provide continuous regulation on the input current independent of the output voltage level, and the current shape could be perfectly sinusoidal. However drawbacks are: the output voltage does not share a common ground with the input voltage, the switch is floating, and the naturally high switching voltage stress ($V_{in} + V_{out}$) calls for higher voltage rating switch. These reasons make the buck-boost converter not a really popular choice.
- *Cuk, Sepic and Zeta*: the current drawn is usually distorted from a sinusoidal shape to some extent, thus do not have a very good current shaping ability, and the additional passive components rise the cost and complexity.

Based on the features listed above, it could be seen that among all the basic topologies, *boost* is the most preferable topology for a PFC converter, especially in the cases where the output voltage of the PFC converter is always larger than the peak value of the line voltage. Thus, the boost-type PFC will be further investigated, and possible modifications will be introduced for the purpose to break the limitation of the conventional boost converter..

2.5. The Limitations of Conventional Boost PFC

In chapter 2.4, the conventional boost PFC circuit operating in BCM is investigated. The good current shaping ability, least components count, easy control and high reliability make the conventional boost topology popular in PFC application. However, there are four limiting factors that come from this topology which prevents the boost PFC from achieving very high efficiency, high switching frequency.

The switching loss from the switch.

The switching loss is highly dependent on the operation mode of the boost converter, because the current and voltage states during switching transient differ with operation modes. The turn-on loss in the conventional boost converter could be reduced by operating in BCM or even in DCM, because the current flowing through the switch will be zero when turning on, as depicted in figure 2.3, this is so-called Zero-Current-Switching (ZCS). however, ZCS turn-on does not necessarily mean zero turn-on loss. In fact, because of the discharging of the parasitic output capacitance c_{oss} of the switch during turn-on, there will be some additional channel current generated and flows inside the switch, which causes turn-on loss. Zero turn-on loss is only possible with the employment of Zero-Voltage-Switching (ZVS).

The turn-off loss however, is potentially high in BCM and DCM boost PFC, due to the large peak value of the current when turning off. One modification that could be made in order to reduce the turn-off loss, is to add a output capacitor in parallel with the switch, so that when turning off, the rising of the voltage over the switch V_{DS} is delayed, thus effectively reduce the overlap of current and voltage during turning off, which means a smaller turn-off loss. If the additional output capacitor is chosen to be larger enough, the turn-off loss could be fully eliminated. However, this additional parallel capacitor will effectively increase the C_{oss}, which will accordingly increase the turn-on loss if ZVS is not achieved.

Fortunately, it is relatively easy to achieve ZVS or Reduced-Voltage-Switching in the conventional boost topology when operating in BCM, by applying the *valley-switching* method. Due to the resonance between the boost inductance and the parasitic capacitance from the switch, diode and inductor after the boost inductor is fully demagnetized, the voltage over the switch V_{DS} would oscillate with a resonant frequency determined by the resonant inductance, capacitance value. If the switch is controlled to turn on when V_{DS} is at the minimum value (the valley point), the turn-on loss could be reduced[25][26]. This switching method is called *valley switching*. With a duty cycle larger than 0.5, ZVS could be achieved; otherwise, reduced voltage switching is achieved.

In a short conclusion, the turn-on loss of a conventional boost converter could be drastically reduced by operate the converter in BCM-VS mode to achieve reduced voltage switching or even ZVS. Moreover, if ZVS could be reached, additional parallel capacitor could be added to the switch, which acts as a lossless snubber circuit that only reduces the turn-off loss without adding turn-on loss. In this way, the switching loss of the conventional boost converter could be reduced to the minimum. However, reducing switching losses bring some drawbacks:

1. Operating in BCM or even DCM will result to the large current ripple, which not only poses threat on the components, but also increases the winding loss, core loss on the inductor.
2. Adding the parallel capacitor as lossless snubber will limit the switching frequency.

A shortcut exists nowadays with the rapid development of wide bandgap materials, especially GaN and SiC. The new semiconductor transistor made of GaN will have a much faster turn-on and turn-off transients, bringing much smaller switching losses. In fact, the turn-off loss in a GaN transistor is much smaller than the turn-on loss [2]. Thus by using GaN transistor in a BCM-VS boost PFC, both turn-on and turn-off loss could be largely reduced (turn-on reduces by ZVS, turn-off reduces by using GaN).

The reverse recovery loss from the diode D.

In the minority carrier devices, as a power diode is, the change of conduction state, i.e., from conduction state to blocking state, or vice versa, would need certain amount of time to sweep the remaining minority carriers in the PN junction, this time is called *reverse recovery time*, and the amount of charge that needs to be removed is called *recovered charge* Q_{RR}. And accompanied with this process, an extra current with reverse direction is generated, leading to dissipation in both diode and switch [27], this loss is called *reverse recovery loss* P_{RR}. In the CCM operation of the boost PFC, the reverse recovery of the power diode D will effectively increase the current flowing through the switch i_M during the turn-on of M, leading to the increasing of turn-on loss on M. And this problem increases as the switching frequency is pushed higher.

Different approaches could be taken to reduce the reverse recovery loss. Firstly, various boost converter with different active snubber circuits are proposed for the purpose of reducing the reverse recovery loss in CCM [28]. The advantage of this approach is that it not only reduces the reverse recovery loss from the rectifier diode, but also provide either ZCS or ZVS to the boost switch. However, this active approach to reduce reverse recovery loss comes with the increasing of cost and control complexity.

A more effective way is to operate the boost converter in BCM or DCM. As illustrated in figure 2.3, the current flowing through the diode D, i_D drops to zero every time the diode turns off, i.e., the switch turns on, thus no reverse recovery current would be generated [27]. However, due to the nature of BCM and DCM operation, the current through the inductor will have a peak value that is twice or even larger than the average current, calling for higher current rating switch and diode, and leading to the increased loss on the inductor, as already discussed before.

With the emerging of SiC diodes, the design could be made much easier, simply because SiC diode does not, or only have very little reverse recovery charge[4]. Thus if SiC diode is used as rectifier, no active snubber is needed to reduce the reverse recovery loss. Thus with the using of SiC diodes, high switching frequency (relatively high) CCM boost PFC becomes feasible.

The losses on the inductor L.

The size and rating of a magnetic component are determined by the losses in the component [9], thus it's important to know where do the losses in the inductor come from and what are the factors that make influence.

The losses on the inductor could be divided into 1). the losses from the core and 2). the losses from the windings.

- Hysteresis loss (Core).

  Hysteresis loss comes from the hysteresis characteristic of magnetic core materials. Figure 2.8 shows a B-H characteristic of a magnetic core material with hysteresis.

  If the flux in the core is time varying, energy is needed to magnetize and de-magnetize the core, which will dissipates in the core and causing temprature rising of the core.

  Conventional method of calculating the hysteresis loss generated per unit volume is using Steinmetz equation[9][30]:

  $$P_{hys} = k \cdot f^a \cdot \hat{B}^d \tag{2.1}$$

  where P_{hys} is the calculated hysteresis loss per unit volume, f is the switching frequency, $\hat{B}$ is the peak value of the magnetic flux density if it does not have time average value (purely AC waveform), and k, a, d are constant parameters depending on the material.

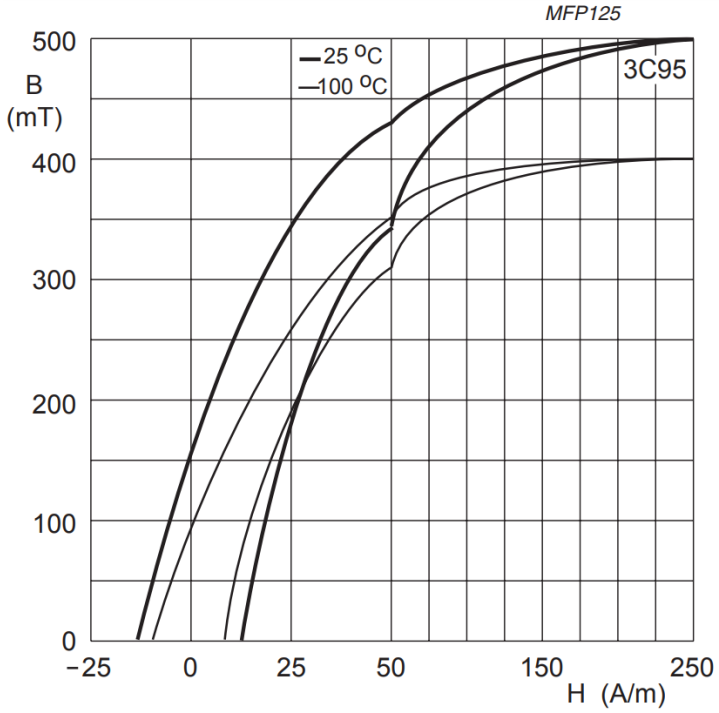


Figure 2.8: B-H loop of the ferrite material $3C95$[29]

As a primary indication, equation 2.1 tells the fact that the hysteresis loss generally increases with 1). higher switching frequency f, 2). peak magnetic flux density value $\hat{B}^d$, which, according to Ampere's law, is positively related to the peak value of the current that flows through the winding, and 3). core material K, a, d.

Equation 2.1 only holds its accuracy in the cases where sinusoidal excitation is applied. However in most power electronics applications, the flux waveform is non-sinusoidal, the boost converter is an example, whose excitation current is triangular. Thus, a modified Steinmetz equation is presented to meet the need for estimating the hysteresis loss of non-sinusoidal excitation [31][32][33]. Figure 2.9 shows the hysteresis loss for triangular excitation (begins from zero, ends at zero) with varying duty cycle δ. A ratio of $\frac{2}{\pi^2}\frac{1}{\delta(1-\delta)}$ needs to be applied to the conventional Steinmetz equation results. The reason for this difference is because the hysteresis loss is in fact propotional to the rate of change of induction dB/dt, instead of switching frequency f [33]. For different triangular excitation current with the same frequency, dB/dt varies with different duty cycle, thus the hysteresis loss will be different.

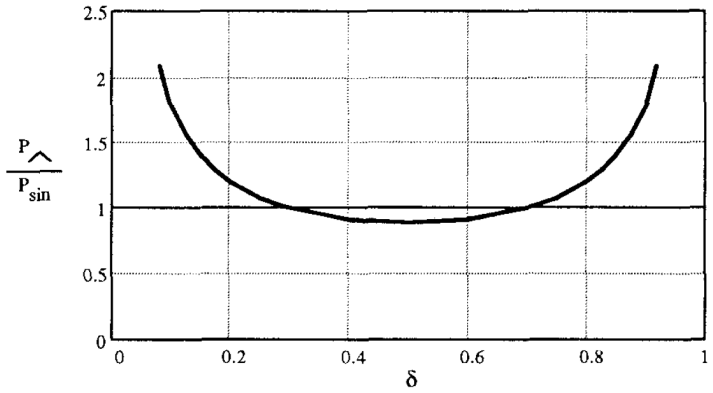


Figure 2.9: Hysteresis loss of triangular current with a sinewave current as reference[31]

But generally, it's the converter's switching frequency and peak value of magnetic flux density that dominantly determine the core loss. This brings the competition between the CCM operation and BCM operation.

- Eddy current loss (Core).

  Since ferrite magnetic material will be used, the eddy current loss would be largely eliminated due to the very large resistivity in ferrites. Thus for the simplicity of analysis, eddy current loss here is not considered.

- DC conduction loss (winding).
- Skin effect (winding).

The losses on the diode rectifier bridge

As illustrated by figure 2.2, the conventional boost converter has a rectifier bridge which consists of four diodes for the purpose of rectifying the $50HZ$ AC voltage v_{AC} to the alternating $100HZ$ DC voltage. In the positive cycle of v_{AC}, the input current would flow through D_1, the cascaded boost converter, and flow back via D_4, for the negative cycle the current flows through D_2, the boost converter and D_3. Thus the current will always need to flow through two bridge diodes and the boost converter. Provided that the bridge diode usually has a forward voltage drop around $1.1V$, considerably loss would be generated on the diodes especially when the input voltage is low.

Taking a $2KW$ PFC as an example. During the low input voltage ($200V-15\%$) time period, assuming the power factor is unity, the rms value of the input current is calculated as:

$$I_{in(rms)} = \frac{P}{V_{in(rms)}} = \frac{2000}{170} = 11.76A$$

Thus the loss generated on one single diode due to the forward voltage drop could be calculated as:

$$P_{diode} = I_{in(rms)} \times V_f = 11.76 \times 1.1 = 12.94W$$

This not only contributes to an overall efficiency drop of around 0.65%, but also rises up the temperature on the diodes and makes them hot spots which require additional thermal design[10][34].

2.6. The Improvements: Derivatives of Boost PFC

In order to solved the problems of the conventional boost converter mentioned in the last section, and to achieve higher efficiency, higher power delivering ability and higher power density, various improvement methods are proposed, and accordingly, many new topologies based on the conventional boost topology are proposed.

2.6.1. Boost PFC with Snubber Circuit

In order to solve the reverse recovery issue brought by the boost recitifier diode (Syc Rec) when operating in CCM as described in chapter 2.5, the turn-off rate of the current through the boost rectifier, di_f/dt, needs to be controlled. Figure 2.10 shows an example of how the recovered charge value Q_{RR} of a diode changes with different di_f/dt as reference[35].

It is clear from figure 2.10 that the smaller di_f/dt is, i.e, the slower the diode is turned off, the smaller Q_{RR} will be. Since the reverse recovery loss is directly proportional to Q_{RR}[28], the reverse recovery loss could be reduced by achieving a smaller di_f/dt value. This is usually done by adding snubber circuits to the conventional boost topology.

M. M. Jovanovic, et al. conducts a throughout review of boost PFC with different passive / active snubber circuits [28]. All of the active snubber approaches reported in [28] not only reduce the reverse recovery loss, but also offer ZCS or ZVS to the main switch, moreover, some of them also provide the possibility of soft-switching the snubber switch. Figure 2.11 shows an example of a boost converter with lossless active snubber that provides ZVS for both boost and snubber switches.

However, the reduction of reverse recovery loss comes with the increasing cost, because at least one more switch, one more passive component and additional diodes are needed. And the active switch also calls for more complex control method.

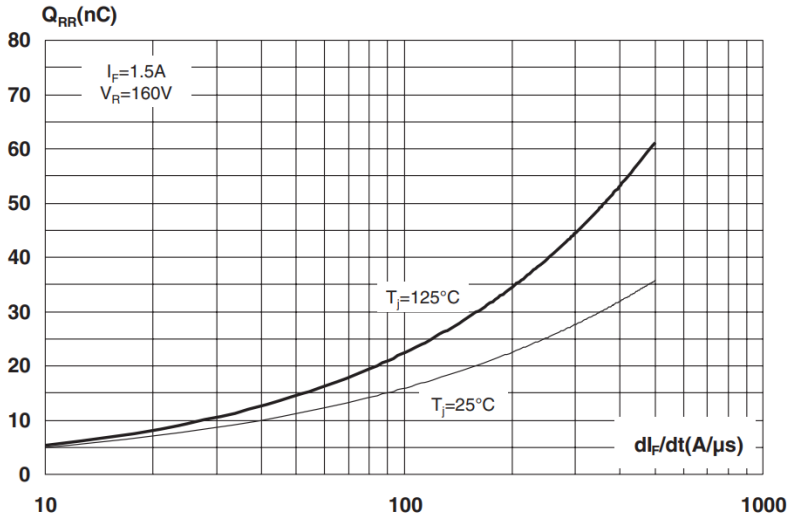


Figure 2.10: Reverse recovery charge V.S. di_f/dt [35]

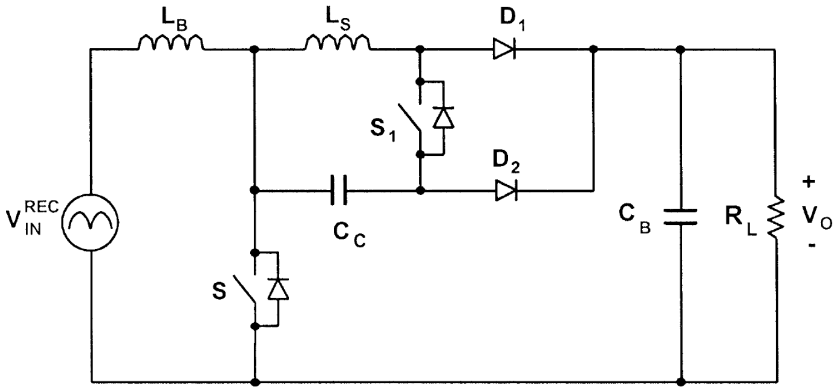


Figure 2.11: Boost converter with active snubber that features ZVS of both boost and snubber switches[28]

2.6.2. Interleaved Boost PFC

The large current ripple that flows through the inductor, which has a peak value of two times or even larger than the average current $I_{average}$, is an inherent drawback of operating the boost PFC in BCM or DCM, as clearly indicated in figure 2.3. This large input current ripple brings problems such as 1). the increased complexity of the designing of the input EMI filter, 2). the larger inductor core losses as is discussed in section 2.5, and 3). the larger conduction loss on the switch, diode, and Effective Series Resistance (ESR) of the bulk capacitor due to the larger RMS current value.

In order to solve these problems, the interleaved power conversion technique is introduced in [36]. The basic principle is to parallel two or even more identical boost converters together, and operate them with a specific phase difference among each other, so that:

1. The input current is shared by the parallel converters, resulting to less component stress and lower loss on each converter. This potentially increases the power level.
2. The input current ripple is largely reduced and the effective frequency of the ripple is increased, bringing the saving in EMI filtration and energy storage.
3. The ripple current that is fed to the output capacitor and load could be largely reduced, leading to a more robust and cheaper design[10].

Figure 2.12 shows the circuit diagram of a PFC by interleaving two boost converters. L_1, M_1 and D_5 form a boost converter, and L_2, M_2 and D_6 form another. These two boost converters operate

separately, but are synchronized to keep out-of-phase.

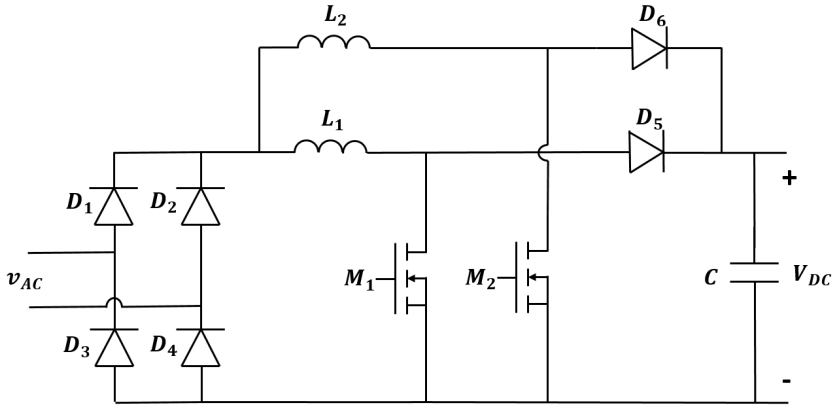


Figure 2.12: Interleaving two boost converters for PFC

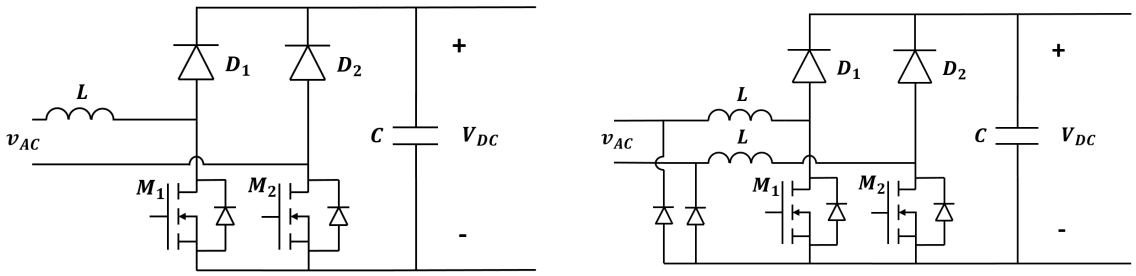
The drawback of the interleaving method is the larger component count and more sophisticated control schemes.

2.6.3. Bridgeless Boost PFC

As described in section 2.5, the inevitable losses on the diode bridge becomes the bottleneck of achieving higher efficiency when other parts of the converter are optimized. In order to solve this problem, various *bridgeless* topologies are proposed[10][37][38]. The basic idea of "bridgeless" is to reduce the number of diodes on the rectifier bridge by combining the boost converter with the rectifier bridge, and operating the main switch in such a way that it performs dual-function of both rectifying and boost switching.

Basic Bridgeless Boost PFC

Figure 2.13a shows the circuit diagram of a basic bridgeless boost PFC[37].



(a) Basic bridgeless boost PFC

(b) Two-boost bridgeless PFC

Figure 2.13: bridgeless boost PFC topologies

Instead of a separate rectifier bridge and a boost converter stage as shown in figure 2.2, the basic bridgeless boost PFC shown in figure 2.13a combines the rectifier bridge and the boost stage by replacing two rectifier diodes with switches, and putting the inductor in the input side of the bridge.

It is clear from figure 2.13a that, there are only two semiconductor components on the current path by using this bridgeless topology (M_1 & M_2 or D_1 & M_2 for the positive half-cycle, M_1 & M_2 or D_2 & M_1 for the negative half-cycle), thus the conduction loss on one diode is saved. Moreover, this topology is cheap because only one more switch is required. However, the major drawback of this topology is the significantly increased common mode EMI generated[10][37][38][39], which makes this basic bridgeless topology infeasible for practical use.

Two-Boost Bridgeless PFC

To accommodate this common mode EMI issue in the basic bridgeless boost PFC, a low frequency path should be provided to connect the ac source with the positive or negative terminal of the output[37].

Figure 2.13b shows the two-boost bridgeless configuration, which allows the connection of the output ground and the ac source, thus reduces the common-mode EMI generated. However, this two-boost bridgeless topology calls for higher cost compare to the basic bridgeless configuration, because two more diodes and one more inductor are needed. Moreover, the utility rate of the magnetic components are also low, since each of them is active for only half line cycle.

Totem-Pole bridgeless PFC

Another modification on the basic bridgeless boost PFC is the *totem-pole* bridgeless topology as shown in figure 2.14, by exchanging the position of D_1 and M_2. The diodes D_1 and D_2 are line frequency diodes, which could be replaced by active switches for reducing conduction losses. The two switches M_1 and M_2 form a high frequency switching leg.

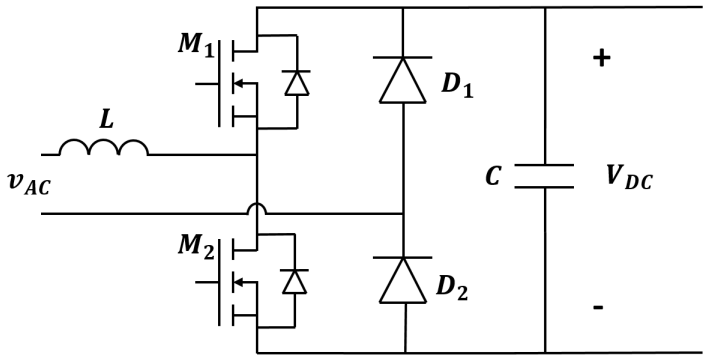


Figure 2.14: Totem pole bridgeless PFC

This totem-pole topology requires minimum components count as the basic bridgeless topology does, and it also have better EMI behaviour compared to the basic bridgeless topology, because the output and the ac source are always connected through D_1 (negative line cycle) or D_2 (positive line cycle). It is also worth to mention that, by replacing the diodes with switches, the totem-pole topology could provide bidirectional operation.

However, it is impractical to have totem-pole topology operate in CCM mode due to reverse recovery issue brought by the body diodes if Si MOSFETs are used[37][3]. For this reason, the totem-pole topology doesn't receive enough attention until the wide-bandwidth semiconductor components are introduced.

2.6.4. Interleaved Bridgeless Boost PFC

Combining the merits of both interleaved PFC and bridgeless PFC, the interleaved bridgeless PFC offers high efficiency, high power delivering ability and potentially high power density. Figure 2.15 shows the circuit diagram of the interleaved totem-pole bridgeless boost PFC. L_1, M_1, M_2 and the two line-frequency diodes form a totem-pole converter, L_2, M_3, M_4 and the two diodes form another, and these two totem-pole converters work out-of-phase in such a way, that the current ripple could be largely cancelled.

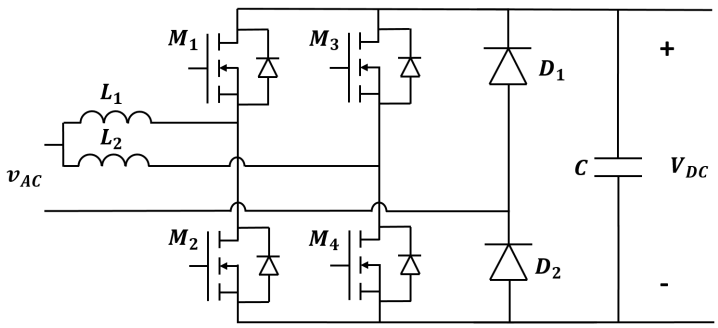


Figure 2.15: Interleaved totem-pole bridgeless PFC

The drawback of this topology, is the cost and the increased complexity of control.

2.7. Wide BandGap (WBG) device: GaN HEMT

GaN switch is the key in the totem-pole topology PFC. With the use of GaN switches in the fast switching leg, BCM and CCM operation modes become possible, and at the same time, higher efficiency and power density would be provided if proper design is achieved. There are mainly three features that make GaN switches and totem-pole topology a good combination [1] [2] [40] [41]:

1. Lower figure of merits merit ($R_{DS(on)} \cdot Q_G$)
2. Faster switching
3. Zero reverse recovery charge

And all these features oriented from the properties of the material. WBG materials have larger band-gap, which will bring more stable lattice structure and consequentially, changes of its physical properties. figure 2.16 shows the comparison of material properties of Si, SiC and GaN.

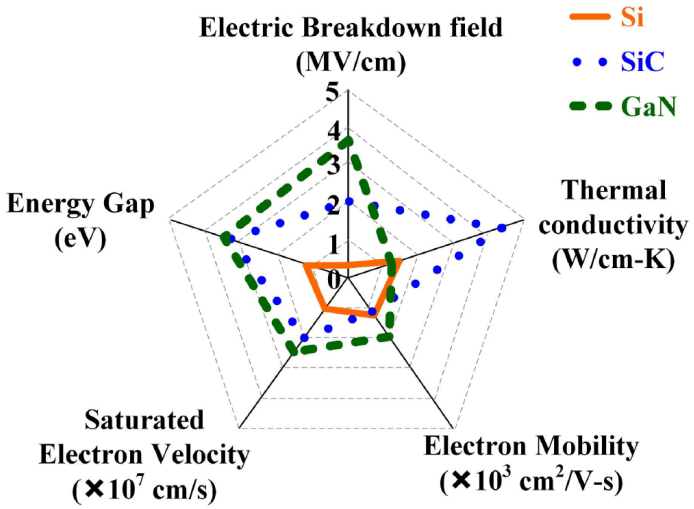


Figure 2.16: Material properties of Si, SiC and GaN[5]

Lower Figure of Merits Merit

GaN switch has lower figure of merits merit, i.e., lower $R_{ds(on)}$ as well as Q_G, because of the higher electrical breakdown field and higher electron mobility.

Because of the higher critical field E_{crit}, i.e., the electrical field above which the impact ionization will happen if this field is applied on the semiconductor device, GaN devices have higher breakdown voltage. And in order to build the higher E_{crit} in a certain drift region, the doping of the region needs to be higher, which provides lower on-state resistance in a unipolar device. Moreover, the higher electron mobility μ_n also contributes to the reduction of $R_{ds(on)}$. Thus higher blocking voltage and lower $R_{ds(on)}$ is achieved at the same time.[1]. For the comparison, the characteristics of a MOSFET ($coolMOS^{TM}$ $P6$, $IPx60R125P6$ from INFINEON) and a GaN HEMT ($GS66508B$ from GaN systems) are listed in table 2.1, and both of them have the same voltage and current rating. It can be seen that the $R_{DS(on)}$ of GaN HEMT is less than half of the value of MOSFET.

	$R_{DS(on)}@25°C$ $(m\Omega)$	$R_{DS(on)}@150°C$ $(m\Omega)$	Q_G (nC)	$C_{o(tr)}$ (pF)	Q_{rr} (nC)
IPx60R125P6	113	293	56	398	7000
GS66508B	50	129	5.8	142	0

Table 2.1: Comparison of GaN HEMT and Si MOSFET

Due to the same reason, for the same blocking voltage rating, thinner drift region could be achieved by using GaN material, which means the size of the GaN device could be smaller while having comparable voltage blocking capability. And the smaller size of the device means smaller parasitic capacitance, including C_{gs}, C_{gd} and C_{ds}. From table **??** it is clear that both Q_G and $C_{o(tr)}$ of the GaN HEMT are significantly smaller than that of a MOSFET.

overall, the Figure Of Merits (FOM) $R_{DS(on)} \times Q_G$ of GaN HEMT is much smaller than Si components', bringing less conduction loss as well as switching loss, leading to higher potential to achieve higher efficiency.

Fast Switching transients and low switching losses

Because of the small parasitic capacitance due to the reduce of the chip size, and higher electron saturation velocity brought by the 2-D electron gas (2DEG) formed in AlGaN/GaN heterostructures, GaN HEMTs are capable of faster switching while having low switching losses[1] [4] [42]. Even though these characteristics benefit both hard-switching and soft-switching application, Zero Voltage Switching (ZVS) turn-on is still a preferred, because of the higher switch-on loss compared to the switch-off loss. Figure 2.17 shows the comparison between the switch-on loss and the switch-off loss.

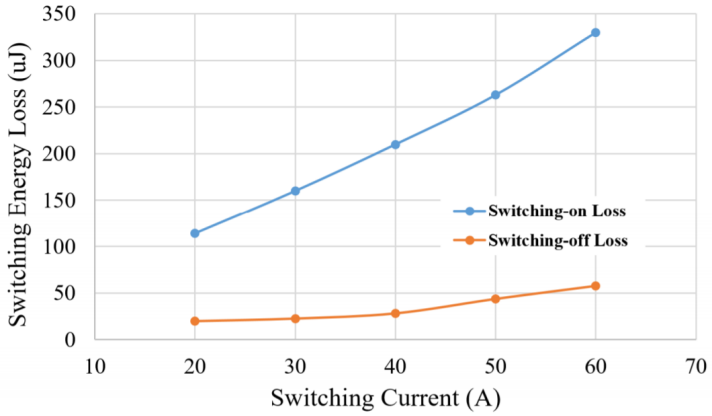


Figure 2.17: Switching energy of GS66516T Vs. Switching Current, @$V_{but} = 400V$ [2]

Different Reverse Conduction

GaN HEMT could perform reverse conduction like a Si MOSFET, but the mechanism is different. Instead of a body diode exists and conducts the reverse current from source to drain when the MOSFET is off, in the case of GaN HEMT, the negative VDS will turn on the device with the drain behaving as a source and the source as a drain, and the current conducts through the 2DEG [2]. The voltage drop during off-state reverse conduction could be expressed as below, where $V_{GS(off)}$ is the off-state gate-source bias voltage.

$$V_F = V_{GS(th)} + V_{GS(off)} \tag{2.2}$$

It could be seen that the voltage drop on the device is larger than that on a intrinsic body diode of a MOSFET (below 0.7V), especially when a negative bias gate voltage is needed for stable turn-off. figure 2.18 show the relation between the off-state gate bias voltage, the duration of dead time, and the reverse conduction loss, where $V_{DR_{off}}$ is the equal to $V_{GS(off)}$. This requires to have a shorter reverse conduction time in order to reduce the reverse conduction loss.

Moreover, due to the different reverse conduction mechanism, GaN HEMT has zero reverse recovery loss during switching [5]. This would not only benefit the half-bridge hard switching operation, but is also helpful for soft-switching operation since the deadtime required to ensure ZVS could be reduced.

2.8. Totem-Pole topology with GaN transistor

By replacing the two MOSFETs by GaN transistors, the performance of the totem-pole topology could be largely improved. Firstly, the zero reverse recovery loss of the GaN transistor enables the topology to operate in CCM, and eases the ZVS design for BCM and DCM, making totem-pole PFC versatile in all

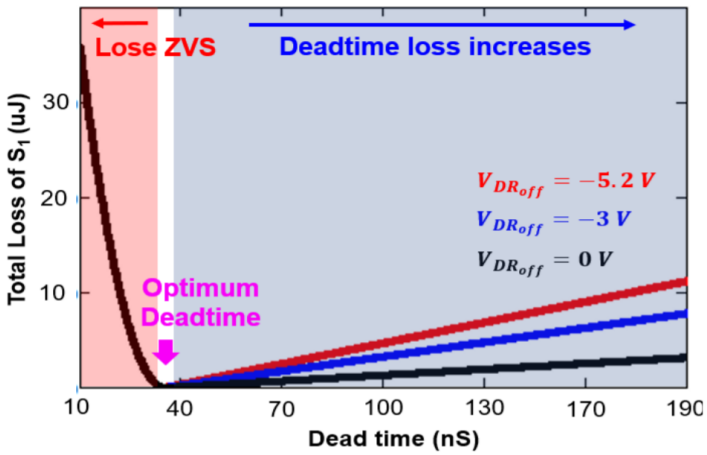


Figure 2.18: Relation between total loss and deadtime of GS66516B at $I_d = 10A$, $25°C$

operation modes. Secondly, fast switching transients and low switching losses enable the totem-pole converter to operate in higher switching frequency while simultaneously maintain good efficiency, and this helps to achieve a system-level improvement, smaller volume thus higher power density. Last but not the least, the intrinsic low $R_{ds(on)}$ characteristic of GaN transistors further improve the efficiency by reducing conduction losses.

These advantages brought the utilization of GaN transistor, along with the low cost, high efficiency, good EMI behaviour, and bidirectional operation ability, make totem-pole PFC one of the most popular cost-efficiency solution for single phase, low power (1-5kW) PFC application [3].

2.9. Conclusion

In the last section, three main approaches that aim to improve the performance of the conventional boost converter are reviewed. The first approach is to reduce the reverse recovery loss brought by the diodem, especially when operating in CCM, by adding active snubber circuit. The second is parallel two identical converters and operate them out-of-phase to reduce the current ripple. The third approach is to combine the fuction of rectifing and boost switching, thus achieving "bridgeless", reducing the losses on the rectifier bridge. Based on these three methods, boost PFC with snubber circuit, the interleaved boost PFC, bridgeless boost PFC, and interleaved bridgeless boost PFC are introduced. With the utilizing of GaN transistors, totem-pole bridgeless PFC stands out as a cost-efficiency solution for the single phase, low power application. By achieving ZVS in the operation, the frequency could be pushed higher while keeping efficiency good, thus makes it possible to increase the power density of the system. Moreover, totem-pole topology gives the possibility to operate bidirectional.

Thus the totem-pole topology with the implementation of GaN transistors, operating with ZVS at high frequency is chosen to design the single phase, 2KW, low cost, high efficiency and high power density PFC converter.

3

Operation Principle of Totem-Pole Topology

The totem-pole topology is formed by a fast-frequency leg and two line-frequency diodes. During a positive / negative AC half-cycle, one of the line-frequency diode conducts, and the two fast-switching transistors together with the main inductor perform similar operation as a conventional boost converter, shaping the input current by the alternatively turning on and off the two transistors.

In order to achieve ZVS in totem-pole PFC, the output capacitors of the switches as well as those of the switching node need to be charged / discharged prior to the turn-on action, which calls for inductive energy. Moreover, synchronous rectifiers must be used, i.e., the line-frequency diodes D_1 & D_2 in figure 2.14 need to be changed to active switches. This is because D_1 & D_2 must allow current to flow in both directions, as will be explained in the following section.

3.1. Detailed AC-DC Operation Sequences

Figure 3.1 shows how the current changes from conducting through M_2 to M_1 in the positive half-cycle, and figure 3.2 shows how it changes from M_1 back to M_2 in the positive half-cycle. These two figures together represent one whole switching cycle in the positive half-cycle. Figure 3.3 shows the resulting waveform.

Phase 1: Current positive, M_2 & D_2 on.

Assuming the operation of the totem-pole PFC circuit begins when the inductor current I_L (later on be abbreviated as *current*) flows out from the AC source and into the switching leg (later on note as *positive* direction), and M_2 and D_2 are conducting, as shown in figure 3.1a

In this phase, the output is maintained only by the capacitor C, and the energy from the source directly supplies the inductor L, resulting to the linear rising of current I_L as indicated by:

$$v_{ac} = L\frac{di_L}{dt} \tag{3.1}$$

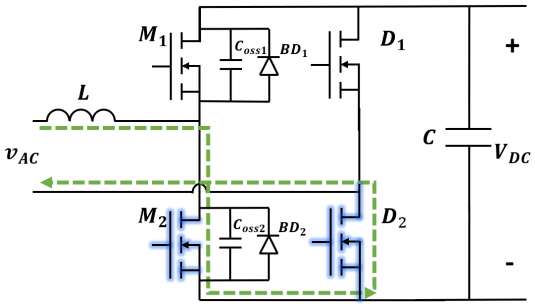
This is identical to the case of a conventional boost converter when the main switch conducts.

Phase 1 ends when I_L reaches its peak value, and M_2 turns off.

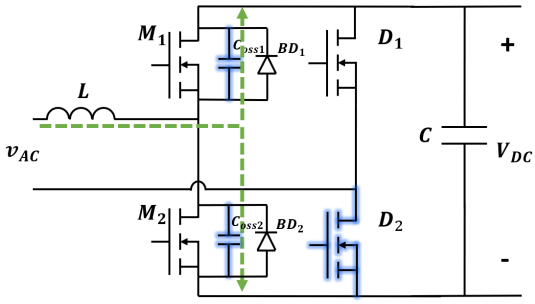
Phase 2: Current reaches the peak value, M_2 turns off, C_{oss} charges / discharges

Just like a conventional boost converter, after the main switch, which in this case is M_2, turns off, the rectifier switch M_1 needs to be turn-on as a complementary operation. However in order to achieve ZVS turn-on of M_1, the output capacitance of M_1 needs to be discharged, while the output capacitance of M_2 needs to be charged, before the turn-on action applies.

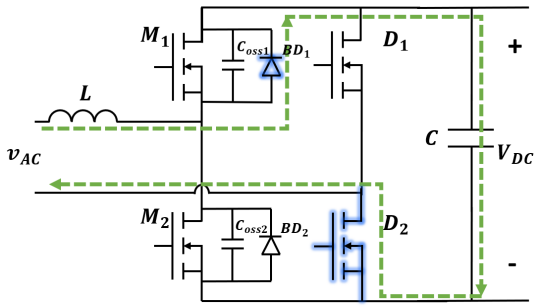
This phase is the charging / discharging period of the output capacitance of the two switches. After M_2 turns off once after I_L reaches its peak value, the inductive current starts to charge C_{oss2} and



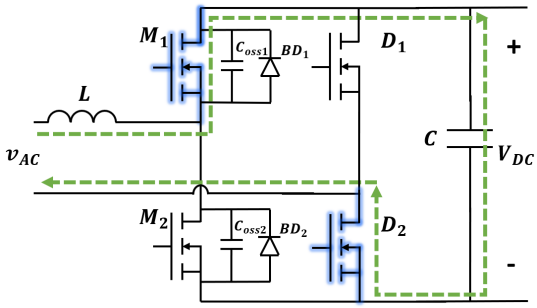
(a) Phase 1, current positive, switch (M_2) on



(b) Phase 2, current positive, switch (M_2) off, C_{oss} charging / discharging

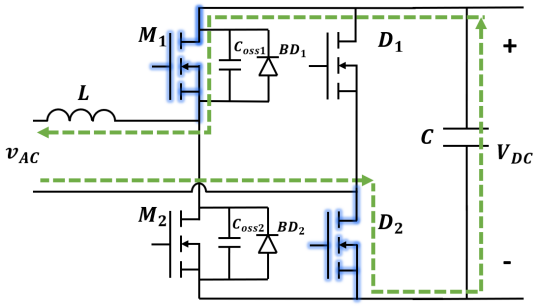


(c) Phase 3, current positive, freewheeling through BD_1

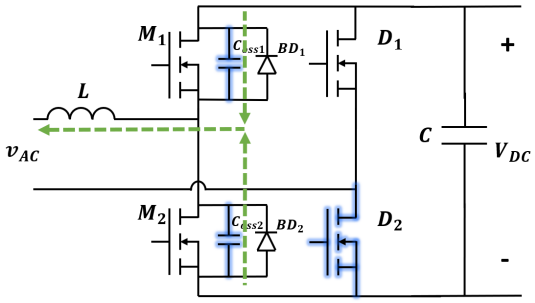


(d) Phase 4, current positive, switch (M_1) on

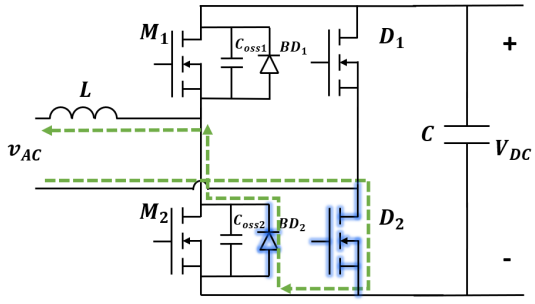
Figure 3.1: Detailed operating sequence of totem-pole 1: transient from M_2 to M_1



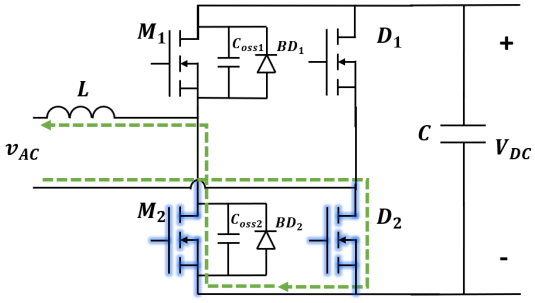
(a) Phase 5, current negative, switch (M_1) on



(b) Phase 6, current negative, switch (M_1) off, C_{oss} charging / discharging



(c) Phase 7, current negative, freewheeling through BD_2



(d) Phase 8, current negative, switch (M_2) on

Figure 3.2: Detailed operating sequence of totem-pole 2: transient from M_1 to M_2

discharge C_{oss1} as shown in figure 3.1b, causing the voltage of the middle point of the switching leg V_{HB} rise from 0 to V_{DC}.

In order to fully charge / discharge C_{oss}, the inductive energy provided by the inductor should be

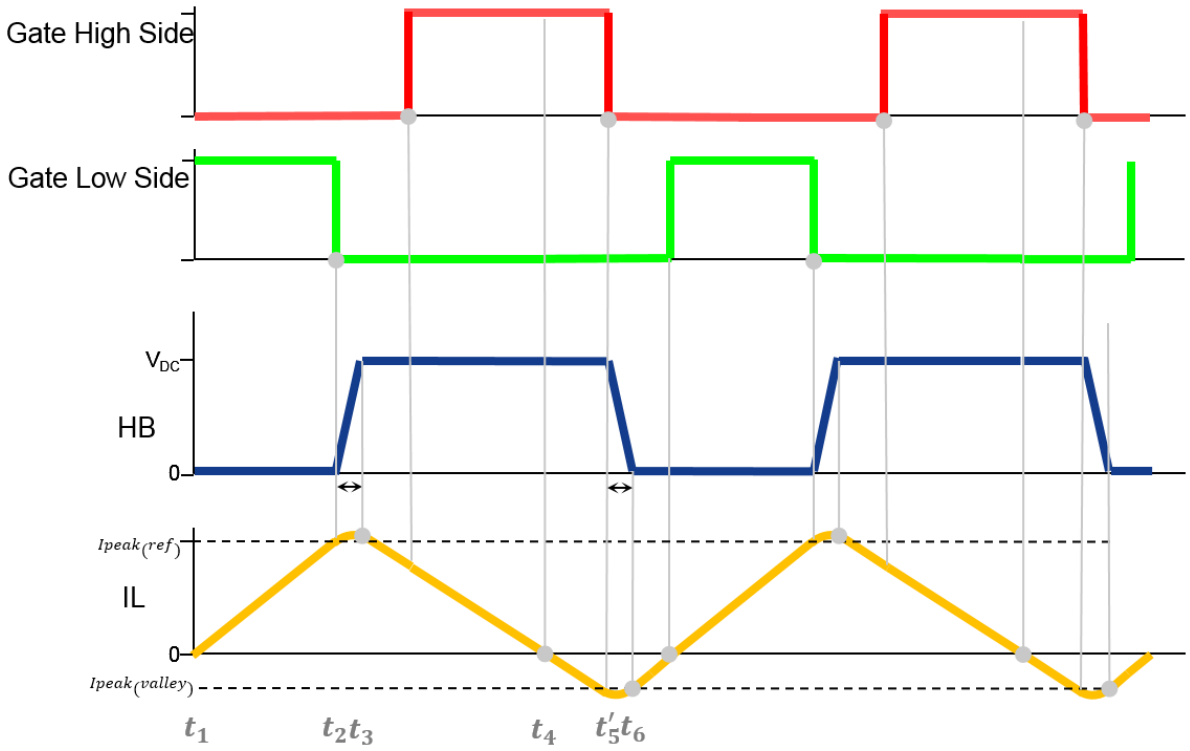


Figure 3.3: The operation waveform of the totem-pole converter

large than the capacitive energy associated with the output capacitance, which gives:

$$\frac{1}{2}LI^2 \geq \frac{1}{2}C_{oss}V^2 \tag{3.2}$$

$$I \geq \sqrt{\frac{C_{HB}}{L}V} \tag{3.3}$$

Due to the fact that during this phase, the current I_L is at its peak value (except when the AC line is in the zero-crossing region), the charging / discharging period is quite short, and V_{HB} will have a high dv/dt.

Phase 2 ends when the charging / discharging finishes, and V_{HB} reaches the value of V_{DC}.

Phase 3: Current freewheels through BD_1

This phase is the freewheeling phase before M_1 turns on. After V_{HB} rises to V_{DC}, which also means the voltage over M_1 drops to zero, BD_1 conducts, the current flow to the output stage, as shown in figure 3.1c. During this phase, current I_L starts to decrease linearly once the inductor is connected to the output stage, as indicated by:

$$-(V_{DC} - v_{AC}) = L\frac{di}{dt} \tag{3.4}$$

Since the body diode usually has a higher voltage drop than the switch itself, this phase brings additional conduction loss. Thus it is preferable to shorten this phase.

Phase 3 together with phase 2 gives the dead time between the turn-off of M_2 and the turn-on of M_1, in which phase 2 is necessary, but phase 3 brings additional conduction loss and should be minimized.

Phase 4: Current positive, M_1 turns on, taking over the current.

After the dead time, M_1 turns on and the current shifts from the body diode BD_1 to M_1, achieveing ZVS turn-on of M_1, as shown in figure 3.1d.

Current continues to decrease linearly in this phase, until it drops to zero.

Phase 5: Current drops to zero and reverse direction

In a conventional BCM operation mode of a boost converter, the recitifier switch (in this case, M_1) should be turned off immediately after the current drops to zero, and turns on the main switch M_2. However, as stated before, the output capacitance of the fast switching leg needs to be charged / discharged before the switching actions take place, for the purpose to achieve ZVS turn-on.

In order to do so, two different operation modes could be applied, depending on whether to turn off M_2 or keep it on.

The first one is ***valley switching***. In valley switching operation, M_1 is turned off once the positive current drops to zero, while still holding M_2 off. By doing so, the resonance between the inductor L and the two output capacitors C_{oss1} & C_{oss2} will happen, with the initial condition that, the initial current through the inductor $I_{L0} = 0A$, and the initial voltage at the mid-point $V_{HB0} = V_{DC}$. By applying equations of series-resonant circuit, the time-related inductor current $i_L(t)$, and the time-related mid-point voltage $v_{HB}(t)$ could be derived:

$$i_L(t) = I_{L0} cosw_0(t - t_0) + \frac{v_{AC} - V_{HB0}}{Z_0} \cdot sinw_0(t - t_0) \tag{3.5}$$

$$v_{HB}(t) = v_{AC} - (v_{ac} - V_{HB0}) \cdot cosw_0(t - t_0) + Z_0 I_{L0} sinw_0(t - t_0) \tag{3.6}$$

After substituting the initial values:

$$i_L(t) = \frac{v_{AC} - V_{DC}}{Z_0} \cdot sinw_0 t \tag{3.7}$$

$$v_{HB}(t) = v_{AC} - (v_{AC} - V_{DC}) \cdot cosw_0 t \tag{3.8}$$

where w_0 is the angular resonance frequency which is determined by the inductance value L and the sum of the output capacitance C_{oss}:

$$w_0 = 2\pi f_0 = \frac{1}{\sqrt{2LC_{oss}}} \tag{3.9}$$

And Z_0 is the characteristic impedance that is calculated by:

$$Z_0 = \sqrt{\frac{L}{2C_{oss}}} \tag{3.10}$$

Equation 3.7 and 3.8 indicate that:

1. The inductor current i_L will start to oscillate around $0A$ following a $-sin$ waveform, with an amplitude of $\frac{V_{DC} - v_{AC}}{Z_0}$, and a frequency of $\frac{1}{2\pi\sqrt{2LC_{oss}}}$
2. the mid-point voltage v_{HB} will start to oscillate around v_{AC}, with an amplitude of $V_{DC} - v_{AC}$. The peak value of v_{HB} during oscillation is V_{DC}, and the valley value is $2v_{AC} - V_{DC}$.

From the observation above it is clear that, if $v_{AC} < \frac{1}{2}V_{DC}$, the valley value will be below $0V$, which means ZVS could be achieved by simply waiting for a half resonant cycle, so that the voltage drops to $0V$ and be latched at $0V$ because of the anti-parallel body diode, and turning on M_2. This is so-called *valley switching*.

If $v_{AC} > \frac{1}{2}V_{DC}$, the valley value of v_{HB} cannot be smaller than $0V$, thus by applying valley switching, only *reduced-voltage-switching* could be achieved. There will still be a certain amount of power associated with the output capacitance be dissipated as loss during the turn-on process, which could be calculated as:

$$P_{RVS} = C_{oss} \cdot (2v_{AC} - V_{DC})^2 \tag{3.11}$$

In order to reduce this loss when $v_{AC} > \frac{1}{2}V_{DC}$, another operation mode is introduced: ***extended valley switching***[43][44]. Different from the basic valley switching method, where the rectifier

switch, i.e., the switch that acts like the diode in the conventional boost topology (in this case, M_1) turns off immediately after the inductor current drops to zero, the rectifier switch is kept on for an extended time. The result is that i_L continues decreasing linearly as it does in the previous phase to a negative value $I_{negative}$, so that when M_1 is turned off after this extended time, the inductor and the output capacitors starts to resonate, and the negative current is able to fully charge / discharge the output capacitor, thus achieve ZVS.

Reflected on the mathematic representation of the resonant phenomenon, this extended valley switching brings an initial value of inductor current: $I_{L0} = I_{negative}$, while $V_{HB0} = V_{DC}$. Thus similar to the previous analysis of resonant, $i_L(t)$ and $v_{HB}(t)$ during the resonance could be derived as:

$$i_L(t) = I_{negative} cosw_0(t) + \frac{v_{AC} - V_{DC}}{Z_0} \cdot sinw_0 t \tag{3.12}$$

$$v_{HB}(t) = v_{AC} - (v_{AC} - V_{DC}) \cdot cosw_0 t + Z_0 I_{negative} sinw_0(t) \tag{3.13}$$

Figure 3.2a illustrates the extended reverse conduction period of the rectifier switch.

The detailed analysis of ZVS operation of totem-pole PFC would be in the next chapter, where state-plane is used to explain the resonant phenomenon and to calculate the requirement of achieving ZVS.

Phase 6: current reaches the negative peak value, M_1 turns off, C_{oss} charges / discharges

When the current drops to the negative peak value, M_1 turns off, the negative current starts to charge C_{oss1} and discharge C_{oss2} as shown in figure 3.2b, causing the voltage of the middle point of the switching leg V_{HB} drops from V_{DC} to $0V$. Similar to phase 2, the inductive energy has to be large enough to accomplish this transition, equation 3.3 should be met.

There are two approaches to make the negative current. A direct approach is to set a negative current reference. The inductor current is sensed and compared to this preset negative current reference, and the turn-off of M_1 only happens when I_L drops below the negative reference value. Another indirect approach is to set a certain delay time between the detection of I_L drops to zero and the turning off of M_1, so that the current continues to decrease to a negative value before M_1 turns off, and this value is determined by the delay time. However Since the current sensing is needed in both approaches, thus the latter one does not provide any advantage over the former one.

Different from phase 2, this phase lasts much longer, because the amplitude of this negative current is much smaller than the positive peak value. If the negative current has a large amplitude, the RMS value of the inductor current would increase, which brings more losses. Thus the negative current needs to have an amplitude as small as possible to avoid bringing much additional loss, but at the same time, needs to be sufficient for completing the charge / discharge process.

Phase 7: Current freewheels through BD_2

Once after phase 6 finishes, V_{HB} drops to $0V$ (practically V_{HB} will be $-V_{F(BD2)}$, because of the voltage drop on the body diode), which also means the voltage over M_2 drops to zero, and the current starts to freewheeling through BD_2 before M_2 turns on, as shown in figure 3.2c. And the current also starts to rise up linearly from a negative initial value, because the output stage is disconnected with the input, and the source starts to directly supply the inductor. The rising is ruled by the equation 3.1.

Phase 7 together with phase 6 gives the dead time between the turn-off of M_1 and the turn-on of M_2, in which phase 6 is necessary, but phase 7 brings additional conduction loss and should be minimized.

Phase 8: Current negative, M_2 turns on, taking over the current.

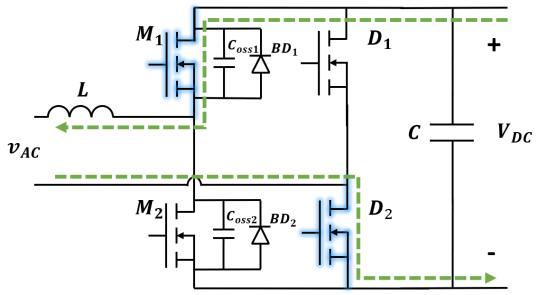
After the dead time, M_2 turns on and the current shifts from the body diode BD_2 to M_2, achieveing ZVS turn-on of M_2, as shown in figure 3.2d.

Current continues to rise up linearly in this phase, until it reaches zero and become positive, i.e., enter phase 1 again.

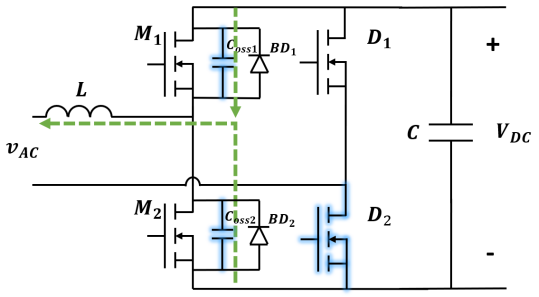
3.2. Detailed DC-AC Operation Sequences

Figure 3.4 together with 3.5 represent one whole switching cycle in the positive half-cycle of the AC line.

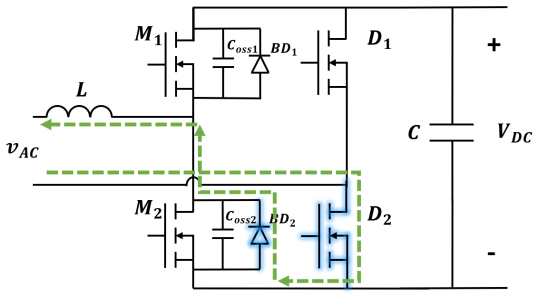
Different from AC-DC operation, in the DC-AC operation, the positive direction of the inductor current is defined as the direction that flows out from the DC side, and flows into the AC source.



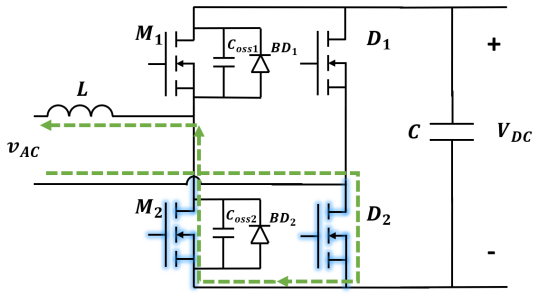
(a) Phase 1, current positive, switch (M_2) on



(b) Phase 2, current positive, switch (M_2) off, C_{oss} charging / discharging



(c) Phase 3, current positive, freewheeling through BD_1



(d) Phase 4, current positive, switch (M_1) on

Figure 3.4: Detailed operating sequence of totem-pole 1: transient from M_2 to M_1

Phase 1: Current positive, M_2 & D_2 on.

Assuming the operation of the totem-pole PFC circuit begins when I_L (later on be abbreviated as *current*) flows in the positive direction, and M_1 and D_2 are conducting, as shown in figure 3.4a.

In this phase, the DC side directly provides energy to the inductor as well as the AC side. the voltage applied on the inductor is $V_{DC} - v_{AC}$, resulting to the linear rising of current I_L as indicated by:

$$V_{DC} - v_{AC} = L\frac{di_L}{dt} \tag{3.14}$$

This is identical to the case of a conventional buck converter when the main switch conducts.

Phase 1 ends when I_L reaches its peak value, and M_1 turns off.

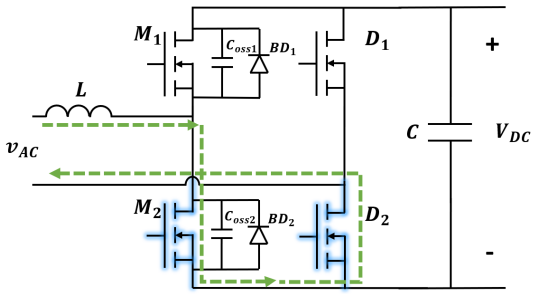
Phase 2: Current reaches the peak value, M_1 turns off, C_{oss} charges / discharges

This phase is the charging / discharging period of the output capacitance of the two switches. After M_1 turns off once after I_L reaches its peak value, the inductive current starts to charge C_{oss1} and discharge C_{oss2} as shown in figure 3.4b, causing the voltage of the middle point of the switching leg V_{HB} drops from V_{DC} to 0.

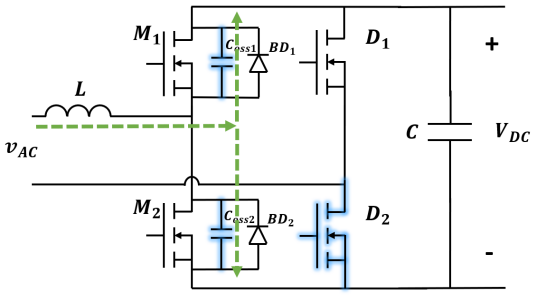
The minimum inductive current needed to fully charge / discharge C_{oss} could be calculated by equation 3.3

Due to the fact that during this phase, the current I_L is at its peak value (except when the AC line is in the zero-crossing region), the charging / discharging period is quite short, and V_{HB} will have a high dv/dt.

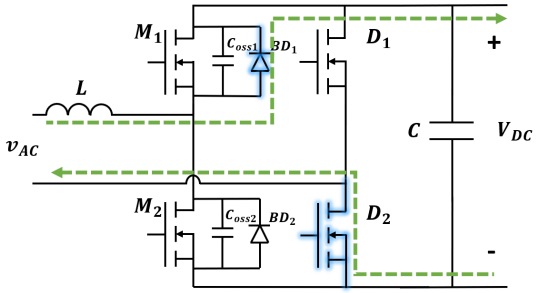
Phase 2 ends when the charging / discharging finishes, and V_{HB} drops to zero.



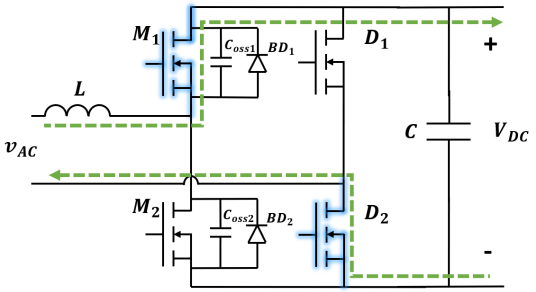
(a) Phase 5, current negative, switch (M_1) on



(b) Phase 6, current negative, switch (M_1) off, C_{oss} charging / discharging



(c) Phase 7, current negative, freewheeling through BD_2



(d) Phase 8, current negative, switch (M_2) on

Figure 3.5: Detailed operating sequence of totem-pole 2: transient from M_1 to M_2

Phase 3: Current freewheels through BD_2

This phase is the freewheeling phase before M_2 turns on. After V_{HB} drops to zero, BD_2 is able to conduct, the current freewheels through BD_2 to the AC side, as shown in figure 3.4c. During this phase, current I_L starts to decrease linearly since the voltage applied on the inductor is a negative v_{AC}, as indicated by:

$$-v_{AC} = L\frac{di}{dt} \tag{3.15}$$

Since the body diode usually has a higher voltage drop than the switch itself, this phase brings additional conduction loss. Thus it is preferable to shorten this phase.

Phase 3 together with phase 2 gives the dead time between the turn-off of M_1 and the turn-on of M_2, in which phase 2 is necessary, but phase 3 brings additional conduction loss and should be minimized.

Phase 4: Current positive, M_2 turns on, taking over the current.

After the dead time, M_2 turns on and the current shifts from the body diode BD_1 to M_1, achieveing ZVS turn-on of M_1, as shown in figure 3.4d.

Current continues to decrease linearly in this phase as it does in the last phase, until it drops to zero.

Phase 5: Current drops to zero and reverse direction

This phase is critical for achieving ZVS turn-on of the main switch (in this case, M_1). At the beginning of this phase, the current decreases to zero. In order to achieve ZVS turn-on of M_1, valley switching or extended valley switching needs to be used.

In valley switching operation, M_2 is turned off once the positive current drops to zero, while still holding M_1 off. By doing so, the resonance between the inductor L and the two output capacitors C_{oss1} & C_{oss2} will take place, with the initial condition that, the initial current through the inductor $I_{L0} = 0A$, and the initial voltage at the mid-point $V_{HB0} = 0V$. By applying equations of series-resonant circuit, the time-related inductor current $i_L(t)$, and the time-related mid-point voltage $v_{HB}(t)$ could be derived:

$$i_L(t) = I_{L0} cosw_0(t - t_0) + \frac{v_{AC} - V_{HB0}}{Z_0} \cdot sinw_0(t - t_0) \tag{3.16}$$

$$v_{HB}(t) = v_{AC} - (v_{ac} - V_{HB0}) \cdot cosw_0(t - t_0) + Z_0 I_{L0} sinw_0(t - t_0) \tag{3.17}$$

After substituting the initial values:

$$i_L(t) = \frac{v_{AC}}{Z_0} \cdot sinw_0 t \tag{3.18}$$

$$v_{HB}(t) = v_{AC} - v_{AC} \cdot cosw_0 t \tag{3.19}$$

Equation 3.18 and 3.19 indicate that:

1. The inductor current i_L will start to oscillate around $0A$ following a $-sin$ waveform, with an amplitude of $\frac{v_{AC}}{Z_0}$, and a frequency of $\frac{1}{2\pi\sqrt{2LC_{oss}}}$
2. the mid-point voltage v_{HB} will start to oscillate around v_{AC}, with an amplitude of v_{AC}. The peak value of v_{HB} during oscillation is $2v_{AC}$, and the valley value is $0V$.

From the observation above it is clear that, if $v_{AC} > \frac{1}{2}V_{DC}$, the peak value will be mathematically larger than V_{DC}, which means ZVS could be achieved by simply waiting for around a half resonant cycle, so that v_{HB} rises to V_{DC} and be latched at V_{DC} because of the anti-parallel body diode, and turns on M_1. This is so-called *valley switching* (even though we are waiting for the peak of v_{HB}).

If $v_{AC} < \frac{1}{2}V_{DC}$, the peak value of v_{HB} cannot reach the value of V_{DC}, thus by applying valley switching, only *reduced-voltage-switching* could be achieved. There will still be a certain amount of power associated with the output capacitance be dissipated as loss during the turn-on process, which could be calculated as:

$$P_{RVS} = C_{oss} \cdot (V_{DC} - 2v_{AC})^2 \tag{3.20}$$

In order to reduce this loss when $v_{AC} < \frac{1}{2}V_{DC}$, extended valley switching should be used. In extended valley switching mode, the rectifier switch M_2 is kept on for an extended time. The result is that i_L continues decreasing linearly as it does in the previous phase to a negative value $I_{negative}$, as illustrated in figure 3.5a. When M_2 is then turned off after this extended time, the inductor and the output capacitors starts to resonant, but this time with an initial value of $I_{L0} = I_{negative}$, while $V_{HB0} = 0$.

Thus similar to the previous analysis of resonant, $i_L(t)$ and $v_{HB}(t)$ during the resonance could be derived as:

$$i_L(t) = -I_{negative} cosw_0(t) + \frac{v_{AC}}{Z_0} \cdot sinw_0 t \tag{3.21}$$

$$v_{HB}(t) = v_{AC} - (v_{AC} - V_{DC}) \cdot cosw_0 t - Z_0 I_{negative} sinw_0(t) \tag{3.22}$$

The detailed analysis of ZVS operation of totem-pole PFC would be in the next chapter, where state-plane is used to explain the resonant phenomenon and to calculate the requirement of achieving ZVS.

Phase 6: current reaches the negative peak value, M_2 turns off, C_{oss} charges / discharges

When the current drops to the negative peak value, M_2 turns off, the negative current starts to discharge C_{oss1} and charge C_{oss2} as shown in figure 3.5b, causing the voltage of the middle point of the switching leg V_{HB} to rise from $0V$ to V_{DC}. Similar to phase 2, the inductive energy has to be large enough to accomplish this transition, equation 3.3 should be met.

Phase 7: Current freewheels through BD_1

Once after phase 6 finishes, and V_{HB} rises up to V_{DC}, which also means the voltage over M_1 drops to zero, the current starts to freewheeling through BD_1 before M_1 turns on as shown in figure 3.5c, and the current also starts to rise up linearly from a negative initial value, because the output stage is disconnected with the input.

Phase 7 together with phase 6 gives the dead time between the turn-off of M_2 and the turn-on of M_1, in which phase 6 is necessary, but phase 7 brings additional conduction loss and should be minimized.

Phase 8: Current negative, M_2 turns on, taking over the current.

After the dead time, M_1 turns on and the current shifts from the body diode BD_1 to M_1, achieveing ZVS turn-on of M_1, as shown in figure 3.5d.

Current continues to rise up linearly in this phase, until it reaches zero and become positive, i.e., enter phase 1 again.

4

State-Plane Analysis of Resonance & The Control Method

In the last chapter, the necessity of *valley switching* and *extended valley switching* for ZVS turn-on of the main switch is explained. However, even though time-domain representation like 3.12 and 3.13 are derived to describe the resonant process, the calculation of the amplitude of $I_{negative}$ that is required to achieve ZVS is still not straight forward.

In this chapter, a ***state plane*** is used to interpret the resonant transient. Based on the state plane, the calculation of $I_{negative}$ as well as the dead-time that is required to finish the resonant transient could easily be derived. Last but not the least, an improved control method that is independent of timing is proposed based on the state plane analysis.

4.1. Operation of Totem-Pole Converter in State Plane

In both valley switching or extended valley switching case, the resonance takes place between the inductor L and the capacitor associated with the mid-point C_{HB}, which consists of the two output capacitors of the switches C_{oss1} & C_{oss2}, and stray capacitance associated with the half-bridge switching node. And the AC voltage source is in series with L and C_{HB}. These three components form a resonant tank as illustrated in figure 4.1, where $i_L(t)$ is the resonating current with the initial value of I_{L0}, $v_{HB}(t)$ is the resonating voltage over the capacitor, which in our case, is also the voltage at the mid-point, with an initial value of V_{HB0}. v_{AC} could be seen as a constant voltage source, since the line frequency is much lower than the resonant frequency.

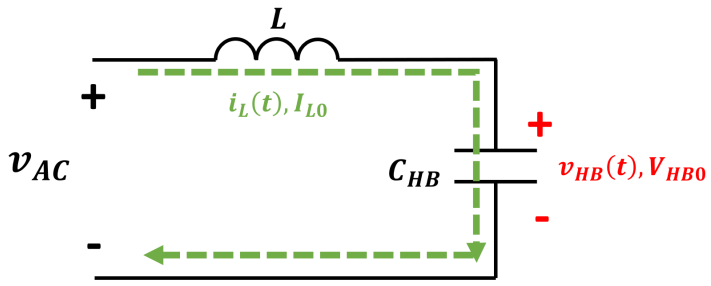
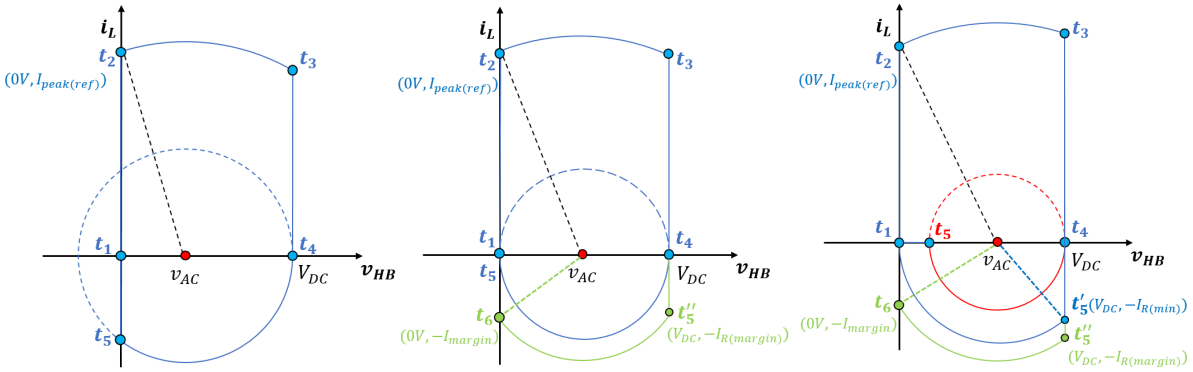


Figure 4.1: The resonant tank during transition

By knowing the all the parameters of the resonant tank as shown in figure 4.1, the resonance in steady state could be described by the two states, the current through the inductor $i_L(t)$ and the voltage over the capacitor $v_{HB}(t)$. However, instead of describing the two states in time domain separately like equations 3.7 3.8 3.12 3.13, a state plane combines the information of the two state into one coordinate system by using them as the two axis (for example, using v_{HB} as x axis, i_L as y-axis), ignoring the time information (The reason why the time information could be ignored here is that, the

resonance has a settled frequency f_r, thus the angle between two points in the state plane hides the time information). However, it is always possible to calculate the time information based on the circuit operation condition.

Figure 4.2 shows the state-plane illustration of one whole switching cycle of the AC-DC operation of totem-pole PFC converter, corresponding to the operation sequences as described before. Important time points are labelled in order to better explain the state-plane. The initial point t_1 is chosen as $i_L = 0A$ and $v_{HB} = 0V$.



(a) $v_{AC} < \frac{1}{2}V_{DC}$ (b) $v_{AC} = \frac{1}{2}V_{DC}$ (c) $v_{AC} > \frac{1}{2}V_{DC}$

Figure 4.2: State plane illustration of AC-DC operation, with different v_{AC} level

- **t_1 to t_2, phase 1**

  In this period, i_L rises continuously until t_2 when it reaches the peak reference value $i_{peak(ref)}$ and M_2 turns off, while the half-bridge node voltage v_{HB} holds at $0V$. This period corresponds to Phase 1 defined in chapter 3 and figure 3.1a. The current rising time period of this phase $T_{on} = t_2 - t_1$ is determined based on equation 3.1:

  $$T_{on} = \frac{i_{peak(ref)}L}{v_{AC}} \tag{4.1}$$

  Figure 4.3 shows the peak reference value of the current $i_{peak(ref)}$ when the power rating is $2KW$, and the on conduction time of the main switch T_{on} that is required to reach $i_{peak(ref)}$, with different L value.

  From figure 4.3b, it is clear that T_on stays constant throughout the time, while with larger L, T_{on} is longer.

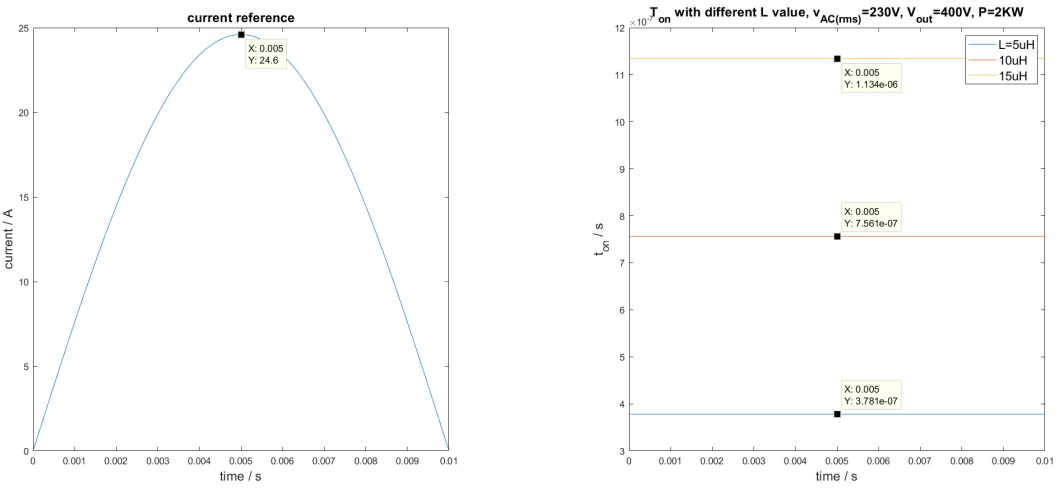
  There are two information that indicates the turning-off of the lower side switch:

  - if $i_L = i_{peak(ref)}$
  - if the on-time of M_2 has reached T_{on} after current crossing zero from negative value.

- **t_2 to t_3, phase 2**

  Right after i_L reaches the peak reference value and M_2 turns off, the resonant starts between L and C_{HB}, with v_{AC} being the applied voltage over the resonant tank, as depicted in figure 4.1. Reflected on the state-plane, the trajectory of this resonant phase begins at point t_2, following an arc with $(v_{AC}, 0A)$ as the center, the distance between the center and the beginning point t_2 as radius, and ends at where $v_{HB} = V_{DC}$, moving with a constant angular speed of $w_0 = \frac{1}{\sqrt{LC_{HB}}}$, as shown in equation 3.9. Note that in order to plot the resonant trajectory as a round circle instead of an ellipse, one of the two states should be normanized according to characteristic impedance 3.10, either by converting the voltage information to current information by dividing the voltage by Z_0, or by converting the current information to voltage, by multiplex the current with Z_0.

  This period corresponds to Phase 2 defined in chapter 3 and figure 3.1b. And this resonant period T_{rpeak} also calls for the minimum dead time between the turn-off of M_2 and the turn-on of M_1.



(a) peak current reference $i_{peak(ref)}$ for 2KW power rating(b) the on conduction time of the main switch T_{on}

Figure 4.3: $i_{peak(ref)}$ & T_{on}

T_{rpeak} could be calculated based on the angle information of this resonant arc. The angle of the arc from t_2 to t_3 in radians ϕ_{peak} could be calculated by :

$$\phi_{peak} = \pi - arctan(\frac{I_{peak(ref)} \cdot Z_0}{v_{AC}}) - arccos(\frac{V_{DC} - v_{AC}}{\sqrt{v_{AC}^2 + (I_{peak(ref)} \cdot Z_0)^2}}) \tag{4.2}$$

After getting the angle of the resonant arc, the resonant time T_{rpeak} in order to make V_{HB} rise up to V_{DC}, i.e., fully charge C_{HB} could be calculated by:

$$T_{rpeak} = \frac{\phi_{peak}}{w_0} \tag{4.3}$$

Figure 4.4 shows the peak resonant period T_{rpeak} with different L value through the time.

It could be seen from figure 4.4 that, when $1ms < t < 9ms$, i.e., when the AC line voltage is high, T_{rpeak} is very short and stays in a small range, from $18.9ns$ to $6.2ns$. However, when $t < 1ms$, i.e., when the AC line voltage is low, T_{rpeak} would be much longer, for example when $L = 15uH$, T_{rpeak} could be as large as $102.4ns$.

The reason is, when v_{AC} is low, $i_{peak(ref)}$ would be less accordingly, which in returen means less inductive energy that is needed to charge / discharge C_{HB}, so the resonant period will be longer.

In figure 4.4, when $t < 0.4ms$ and $t > 9.6ms$, T_{rpeak} stops increasing. This is the extreme scenario where v_{AC} is too low, where the inductive energy would be insufficient to finish the resonant transient, resulting to reduced voltage turn-on of the rectifier switch. Reflected on the state plane, after t_2, the trajectory of resonance will not be able to reach the vertical line where $v_{HB} = V_{DC}$, because v_{AC} and $i_{peak(ref)}$ is too small that the radius of the trajectory is less than $V_{DC} - v_{AC}$.

$$(i_{peak(ref)} \cdot Z_0)^2 + v_{AC}^2 < (V_{DC} - v_{AC})^2$$

This could be further derived into:

$$i_{peak(ref)} < \frac{\sqrt{V_{DC}^2 - 2V_{DC}v_{AC}}}{Z_0}$$

In order to prevent causing addtional turn-on loss, the solution is to keep both switches open when v_{AC} is too low. The exact level of v_{AC} varies with the power level, based on which the $i_{peak(ref)}$ varies. The higher the power level, the lower the v_{AC}.

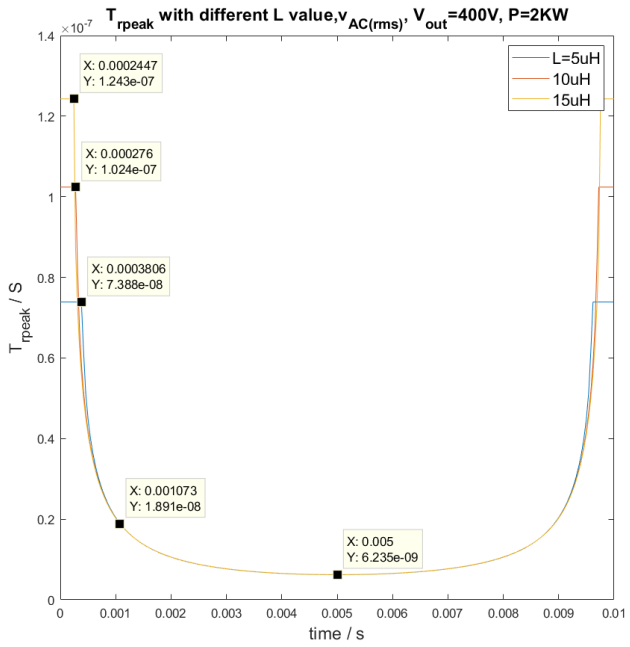


Figure 4.4: The peak resonant transition time: T_{rpeak}

Moreover, at t_3 when the resonant period is finished, the inductor current will have a different value than $I_{peak(ref)}$, noted as I_{rpeak}. Depends on the value of v_{AC}, I_{rpeak} could either be less (when $v_{AC} < \frac{1}{2}V_{DC}$) or larger than $I_{peak(ref)}$ (when $v_{AC} > \frac{1}{2}V_{DC}$). Equation 4.4 shows how I_{rpeak} could be calculated:

$$I_{rpeak} = \frac{\sqrt{(I_{peak(ref)} \cdot Z_0)^2 + 2V_{DC} \cdot v_{AC} - V_{DC}^2}}{Z_0} \tag{4.4}$$

There are two information that indicates the turning-on of the upper side switch:

- if $v_{HB} = V_{DC}$
- if the dead time after turning-off the main switch has reached T_{rpeak}

However, the actual turning-on of the rectifier switch could be applied after t_3, the two conditions above indicate the optimal turning-on, where the current freewheeling time is the minimum.

- t_3 **to** t_4**, phase 3** & **4**

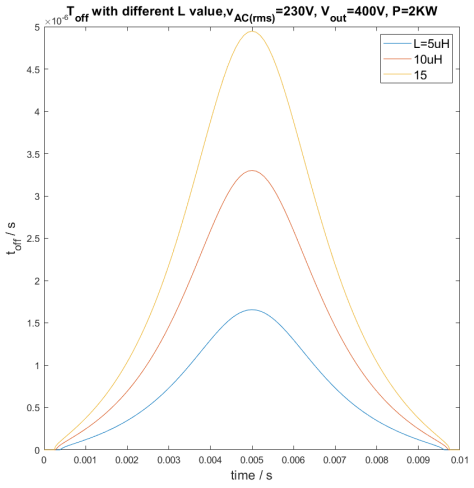
After t_3, v_{HB} fully resonants to V_{DC}, the body diode BD_1 could start freewheeling before M_1 being turned on, or M_1 could be turned on, depending on the actual dead time inserted between the turn-off of M_2 and the turn-on of M_1. But either way will lead to the linear decreasing of i_L, until i_L drops to $0A$ at t_4. This period corresponds to phase 3 and 4. The current decreasing duration T_{off} could be calculated based on equation 3.4 as:

$$T_{off} = \frac{i_{rpeak} L}{V_{DC} - v_{AC}} \tag{4.5}$$

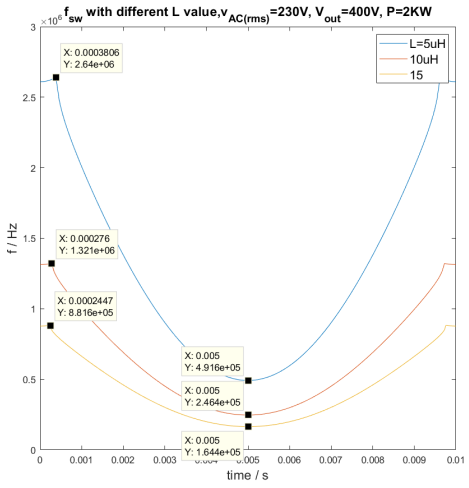
Figure 4.5a shows T_{off} with different L value through the time. It is clear from the figure that, the lower the v_{AC}, the shorter the T_{off}. And when v_{AC} is too low, T_{off} drops to zero. The reason is the same as what prevents T_{rpeak} from increasing during too low v_{AC}: the inductive energy during low v_{AC} is insufficient, making the ZVS of the rectifier switch impossible.

Together with T_{on}, the switching frequency with zero transient time, i.e., totally hard-switching, could be calculated. Figure 4.5b shows the result. And it could be seen that the switching frequency is higher with lower v_{AC}; and with less inductance value, f_{sw} would be generally higher. And similar to figure 4.5a, the switching frequency ceases increasing when v_{AC} is too low, resulting to the abrupt change in figure 4.5b.

table **??** record this hard-switching frequency for different inductance value and different v_{AC}, with the condition that $V_{DC} = 400V$, $P = 2KW$, $C_{HB} = 384pF$. It is clear that the increasing of $f_{sw(hard)}$ is proportional to the decreasing of L.



(a) T_{off}



(b) f_{sw} without considering transient time

Figure 4.5: T_{on} & f_{sw} without valley switching

	$f_{sw(hard)}$ MIN	$f_{sw(hard)}$ MAX
L=5uH	$2.64MHz$	$491.6KHz$
L=10uH	$1.32MHz$	$246.4KHz$
L=15uH	$881.6KHz$	$164.4KHz$

Table 4.1: The hard-switching frequency

- **t_4 to t_5: natural valley-switching**

  If the M_1 is turned off once the current drops to zero, the natural valley-switching would take place, and the state-plane trajectory will follow a partial of an circle with $(v_{AC}, 0A)$ as center, $V_{DC} - v_{AC}$ as radius, moving with a constant angular speed of w_0.

  When $v_{AC} \leq \frac{1}{2}V_{DC}$, the resonant trajectory could be able to reach $v_{HB} = 0V$, as shown in the blue partial circle t_4 to t_5 in figure 4.2a and 4.2b, indicating that by simply waiting for a certain period of resonant time, C_{HB} could be fully discharged and M_2 is possible to be ZVS turned-on in the following phase. However when $v_{AC} > \frac{1}{2}V_{DC}$, the resonant trajectory would not reach $v_{HB} = 0V$, as shown as the red half-circle in figure 4.2c, which means only reduced voltage switching of M_2 could be achieved.

- **t_4 to t_5': extended valley-switching**

  if M_1 is hold on even the current drops to zero, the current will continue to decrease to negative value $-I_R$ with the same changing rate as equation 3.4 indicates. This corresponds to figure 3.2a

  In the case where $v_{AC} > \frac{1}{2}V_{DC}$, By letting the current decrease to negative value before turning off M_1, the possibility of reaching $v_{HB} = 0V$ in the following resonant phase is provided, and thus ZVS turn-on of M_2 could be achieved. Illustrated In figure 4.2c, after t_4, M_1 is held on for

an additional reverse conduction time T_R until t_5' where the current reaches $-I_{R1}$. Thus after t_5' when M_1 turns off, the state-plane trajectory would follow the blue arc till t_1, where it exactly reaches the point where $i_L = 0A$ and $v_{HB} = 0V$. This is the *extended valley switching*.

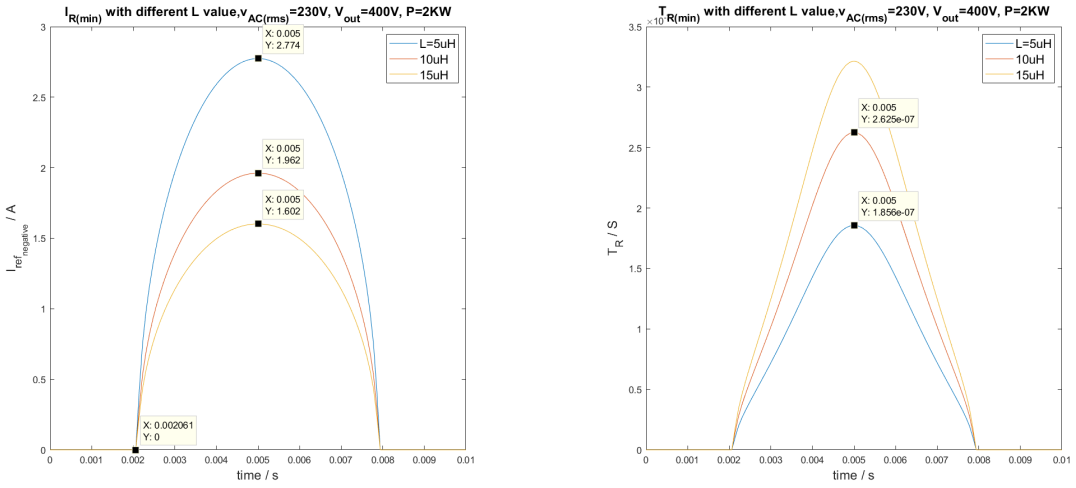
According to the value of v_{AC}, the value of the required negative current I_R which is necessary to achieve ZVS varies. the minimum negative current $I_{R(min)}$ that is just enough to fulfill ZVS could be calculated based the geometrical relation as illustrated in figure 4.2c as:

$$I_{R(min)} = \frac{\sqrt{2V_{DC} \cdot v_{AC} - V_{DC}^2}}{Z_0} \tag{4.6}$$

and the additional reverse conduction time $T_{R(min)}$ of the rectifier switch in order to achieve $I_{R(min)}$ could be calculated as:

$$T_{R(min)} = \frac{I_{R(min)} L}{V_{DC} - v_{AC}} \tag{4.7}$$

Figure 4.6 shows $I_{R(min)}$ and $T_{R(min)}$ through the time, with different inductance value. It can be seen that negative current is required once v_{AC} exceeds $\frac{1}{2}V_{DC}$, and with a larger v_{AC}, more negative current and longer reverse conduction time is required.



(a) $I_{R(min)}$ (b) $T_{R(min)}$

Figure 4.6: $I_{R(min)}$ & $T_{R(min)}$

There are two information that indicates the turning-off of the rectifier switch when using extended valley switching:

- if $i_L = -I_{R(min)}$
- if the reverse conduction time (after current crossing zero from positive value) of the rectifier switch has reached $T_{R(min)}$

- **After t_5': phase 6**

In this phase, the resonance starts between L and C_{HB}, with v_{AC} being the applied voltage over the resonant tank. Reflected on the state-plane, the trajectory of this resonant phase begins at point t_5', following an arc with $(v_{AC}, 0A)$ as the center, the distance between the center and the beginning point t_5' (v_{AC}) as radius, and ends at where $v_{HB} = 0V$, moving with a constant angular speed of w_0.

This period corresponds to phase 6 in chapter 3 and figure 3.2b. And this resonant period $T_{rvalley}$ also calls for minimum dead-time between the turn-off of the rectifier switch and the turn-on of the main switch.

The angle of the arc from t_5' to t_1 could be calculated as:

$$\phi_{valley} = \pi - arctan(\frac{I_{R(min)} \cdot Z_0}{V_{DC} - v_{AC}}) \tag{4.8}$$

Accordingly, the resonant time $T_{rvalley}$ could be calculated by:

$$T_{rvalley} = \frac{\phi_{valley}}{w_0} \tag{4.9}$$

Figure 4.7 shows $T_{rvalley}$ through the time with different L value when extended valley switching is applied. It can be seen that when $v_{AC} < \frac{1}{2}V_{DC}$, natural valley switching is enough for for ZVS, thus $T_{rvalley}$ could be set equal to a half resonant period. When $v_{AC} > \frac{1}{2}V_{DC}$, extended valley switching starts, $T_{rvalley}$ becomes less because of the negative i_L.

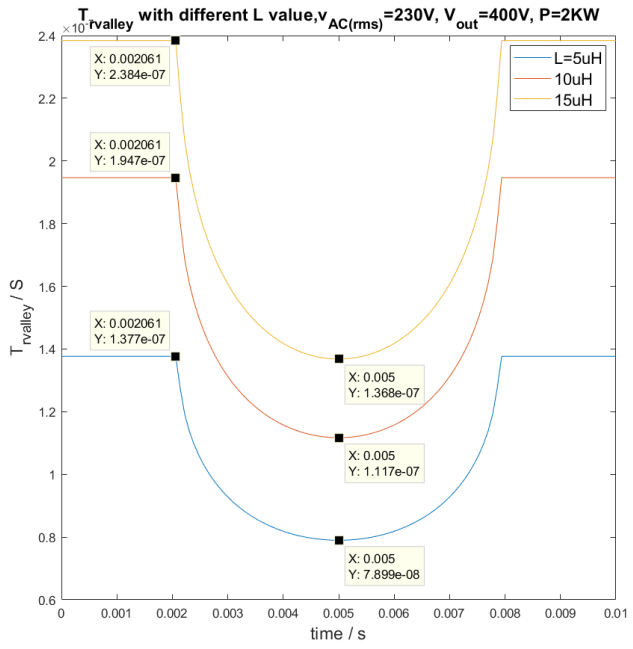


Figure 4.7: The valley resonant transition time: $T_{rvalley}$

There are two information that indicates the turning-on of the main switch:

- if $v_{HB} = 0V$
- if the dead-time after turning off the rectifier switch has reached $T_{rvalley(margin)}$

4.2. Simulation Verification of the Ideal Timing Calculation

In order to verify the ideal timing calculation, an ideal simulation model has been built, as shown in figure 4.8. The switches are ideal with $1m\Omega$ on-resistance, the C_{oss} of the switches are represented by ideal capacitor model, the body diodes are added using ideal diode model with $0.1V$ forward voltage drop, the gate driving signals are the exact copy of PWM signals, the C_{para} is the parasitic capacitance associated with the inductor, together with C_{oss} forms the half-bridge node capacitance C_{HB}. The output is set to be $400V$ for the reason that only the steady state operation is of interest in this thesis.

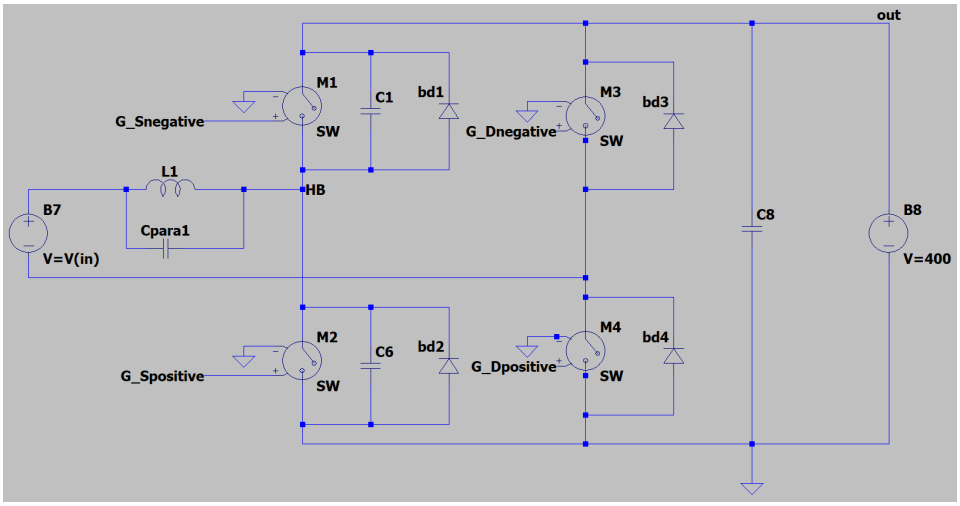


Figure 4.8: Ideal simulation model with ideal switches, without gate driver, without ZCD circuit

V_{in}	V_{out} (V)	P_{out} (W)	L (μH)	C_{HB} (nF)	timing signal
230V AC	400	2000	15	668	perfect timing, no margin

The parameters of the simulation are recorded in the table below:

Timing signals for this specific case is calculated, and based on which a Look-Up-Table is constructed with v_{in} and V_{out} as the input, the five timing signals as output, as shown in figure 4.9. And the timing signals are then processed by logic blocks to generate the PWM signals for the high-frequency switching leg. Note that there should be another input for the LUT block to indicate the power level, thus to set the current reference. But in the simulation, the power is set to be 2KW, so the power input is neglected for the simplicity.

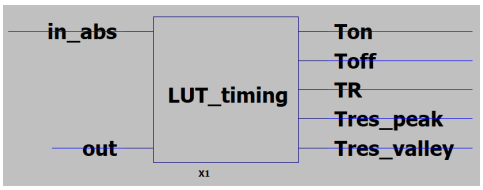


Figure 4.9: The LUT block in LTspice simulation

Figure 4.10 shows the overall current shape for one line cycle, in which the brown line is the current through the inductor i_L, and the turquoise line is the peak current reference $I_{peak(ref)}$.

It can be seen from figure 4.10 that the current strictly follows the peak reference value and forms a sinusoidal envelope. As for the valley shape of the current, it is clear that the negative current value starts to decrease as v_{AC} increases, and then increases after v_{AC} becomes larger than $\frac{1}{2}V_{out}$. The reason for this is because that, in the range where $v_{AC} < \frac{1}{2}V_{out}$, ZVS could be achieved using natural valley switching, without additional reverse conduction time. Until the point where $v_{AC} = \frac{1}{2}V_{out}$, T_R starts to increase so that the current is forced to become more negative for the purpose of having sufficient inductive energy.

Figure 4.11 4.12 4.13 shows some local details at $t = 1ms$, $t = 3ms$, $t = 5ms$, where the red line is the gate voltage for the upper-side GaN switch, the green line is for the Lower-side, the blue line is the scaled-down half-bridge voltage $v_{HB}/V_{out} \times 6$, and the brown line is i_L.

From these three figures, it could be seen that, the current will rise up to the reference value after the main switch hold conducting for T_{on}; and T_{rpeak} is almost the same as the time that is needed for v_{HB} to rise from $0V$ to V_{out}. In figure 4.11 where v_{AC} is less that half of V_{out}, $T_{rvalley}$ is set to be half resonant period, and it can be seen that V_{HB} could be able to drop to zero after turning off the rectifier switch and before the turning on of the main switch, and still have some time margin. This

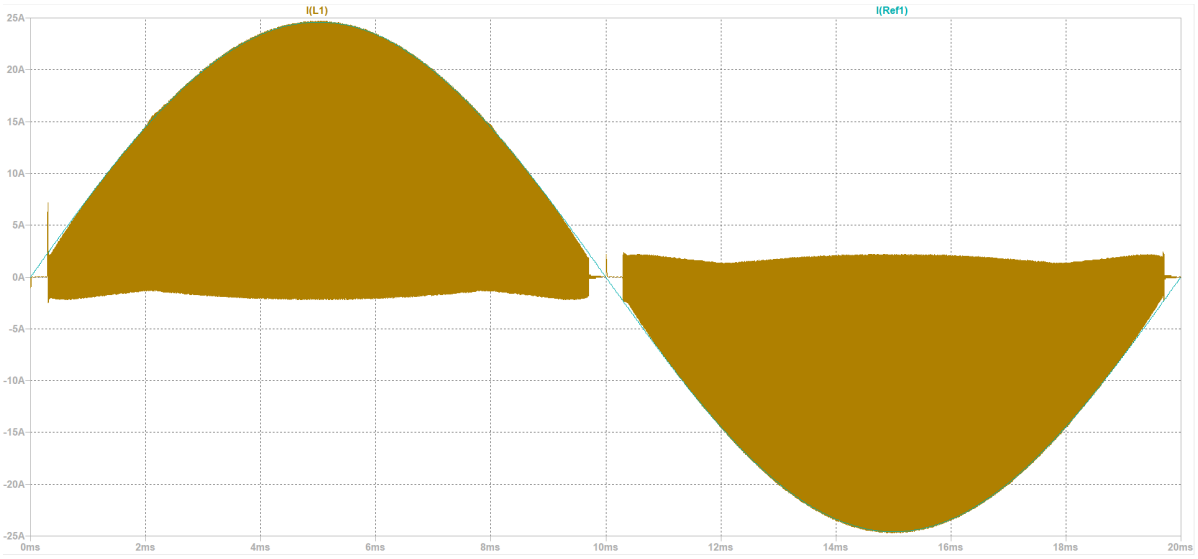


Figure 4.10: Overall current shape, for ideal model, 15μH, no margin timing

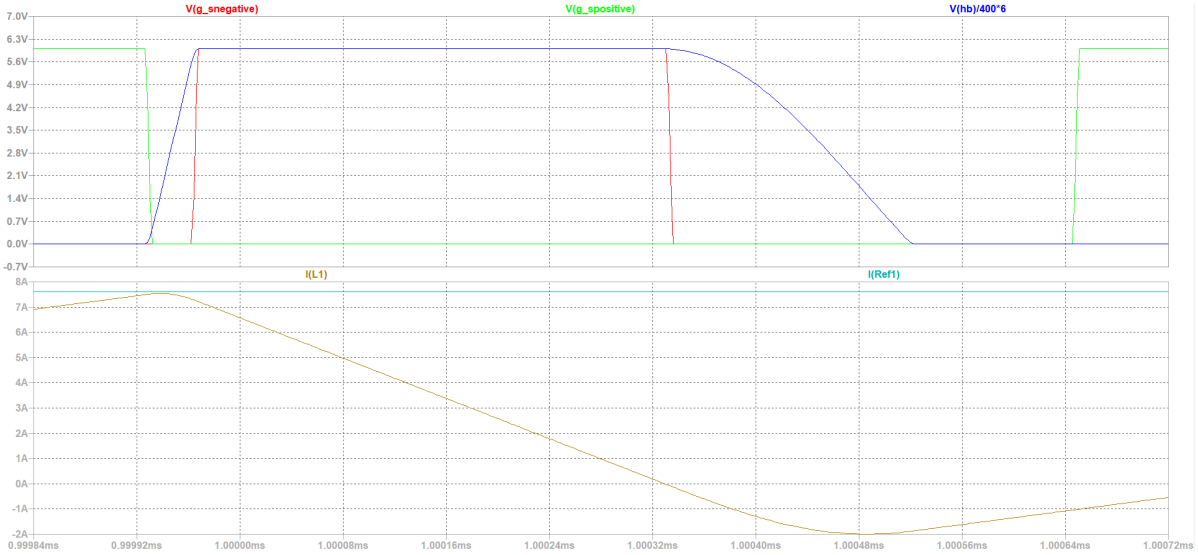


Figure 4.11: Details @1ms, for ideal model, 15μH, no margin timing

is because during low v_{AC}, natural valley switching could be able to achieve ZVS. In figure 4.12 4.13 where $v_{AC} > \frac{1}{2}V_{out}$, the T_R and $T_{rvalley}$ are exactly the time needed that makes the current drops to a certain negative value, and ensuring the fully charge/discharge of the HB node, as reflected on the waveform that the blue line decreases from the peak value to zero resonantly between the turn-off of the upper switch and the turn-on of the lower switch.

Figure 4.14 shows the peak and valley details of the state plane of i_L and V_{HB} at around $t = 5ms$. It can be seen from this figure that the peak and valley transient periods end exactly when V_{HB} reaches V_{out} and $0V$ respectively. The state plane corresponds well with the blue line in figure 4.2c, which represents the case where T_R is designed to make the exact amount of negative current $I_{R(min)}$, and $T_{rvalley}$ is exactly the time needed to have V_{HB} swing to zero.

This simulation demonstrate the feasibility and accuracy of the foregoing timing calculation method, by applying the PWM signals that are made out of the timings, to a ideal simulation model, where all the components are ideal.

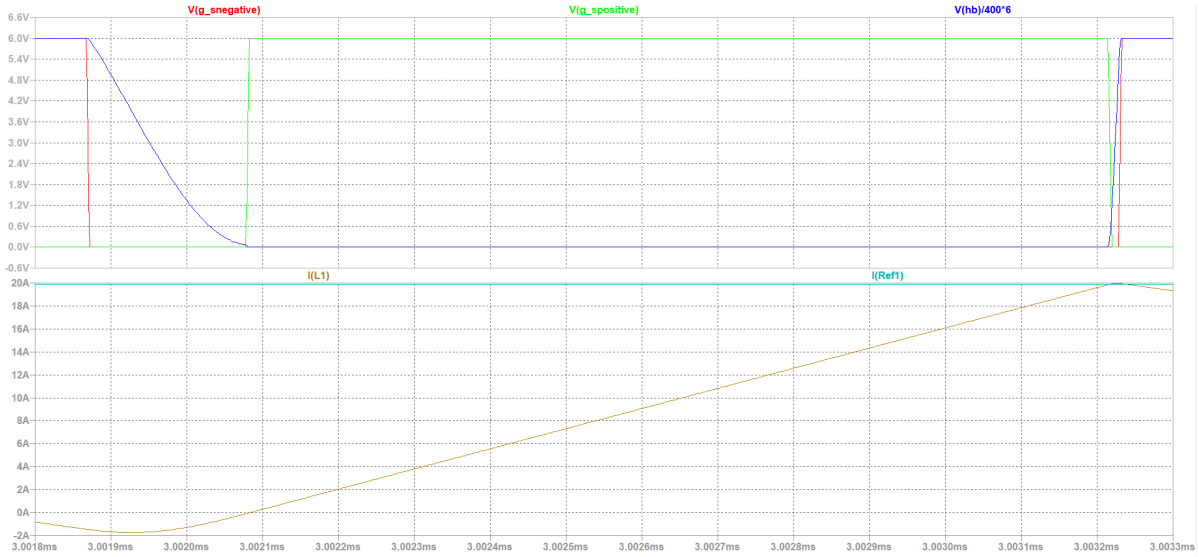


Figure 4.12: Details @3ms, for ideal model, 15μH, no margin timing

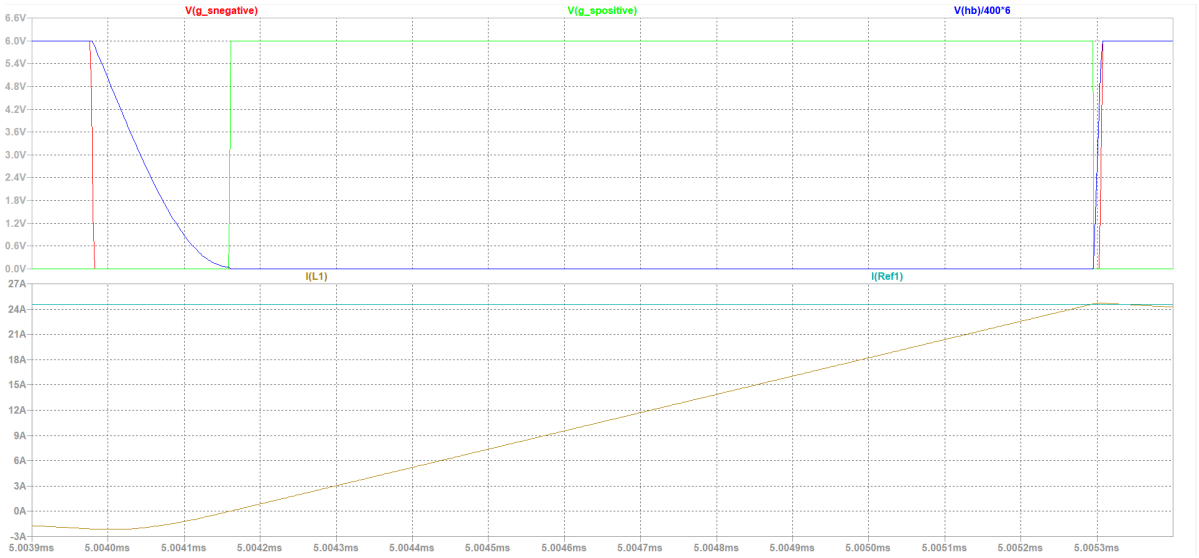
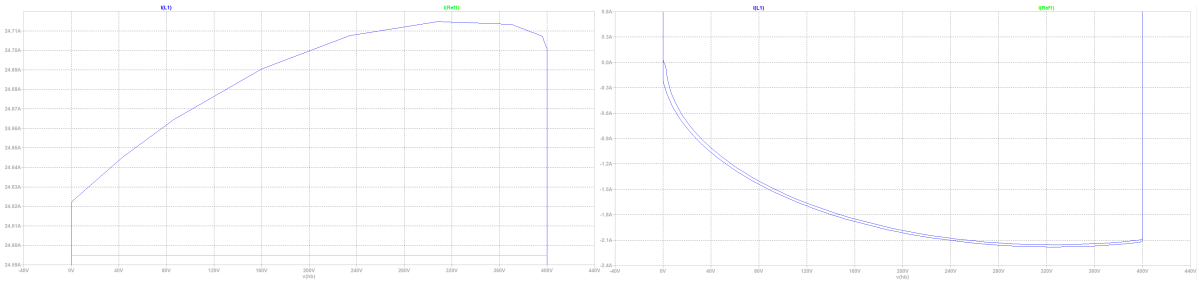


Figure 4.13: Details @5ms, for ideal model, 15μH, no margin timing



(a) Peak details (b) valley details

Figure 4.14: peak and valley details of the state plane @5ms, for ideal model, 15μH, no margin timing

4.3. The Limitation of ideal timing calculation

In more realistic case, components have various non-ideal behaviour that bring variation to the operational environment based on which the timings are calculated. If a set of timing signals are applied

on a different operation environment than that is designed for, deviation of operation would happen, causing problems such as the lost of ZVS, increasing of EMI, additional conduction / reverse conduction loss, etc.

In order to demonstrate the limitation of the perfect timing, a simulation is done as a comparison to the ideal case as shown in the previous section, by applying the perfect timing signals in a more realistic model, in which the ideal components are replaced by non-ideal models.

Figure 4.15 shows a more realistic simulation model which includes the gate driver circuitry (as well as the). The isolated gate driver IC $ADuM4121$ is used as an example, of which the input is the PWM signals that are directly used to drive the gates in the previous simulation, and the bipolar output is the actual gate driving signal, with $6V$ as high, and $-2.8V$ as low, for the purpose of preventing false switching.

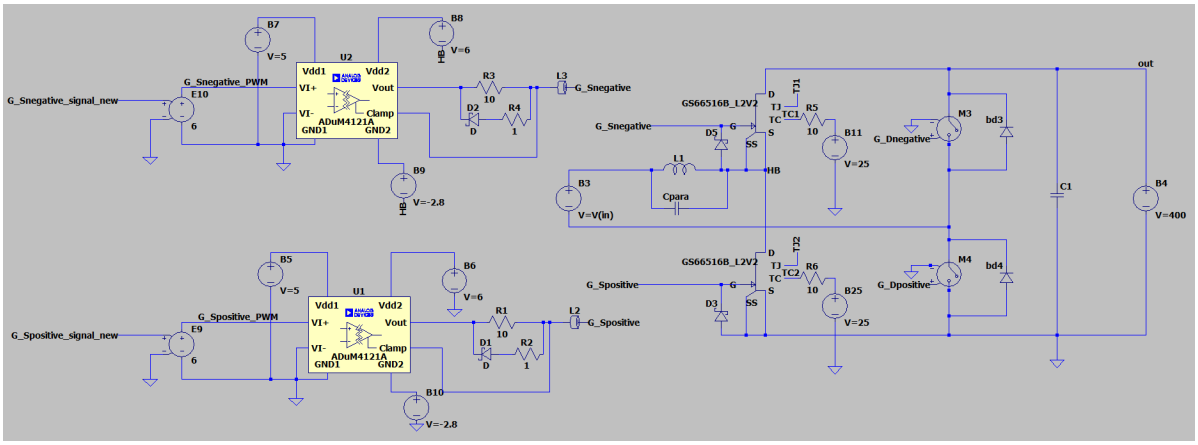


Figure 4.15: A more realistic model containing gate driver circuitry

Figure 4.16 shows the overall current shape for one line cycle, in which the brown line is the current through the main inductor, and the turquoise line is the peak current reference value.

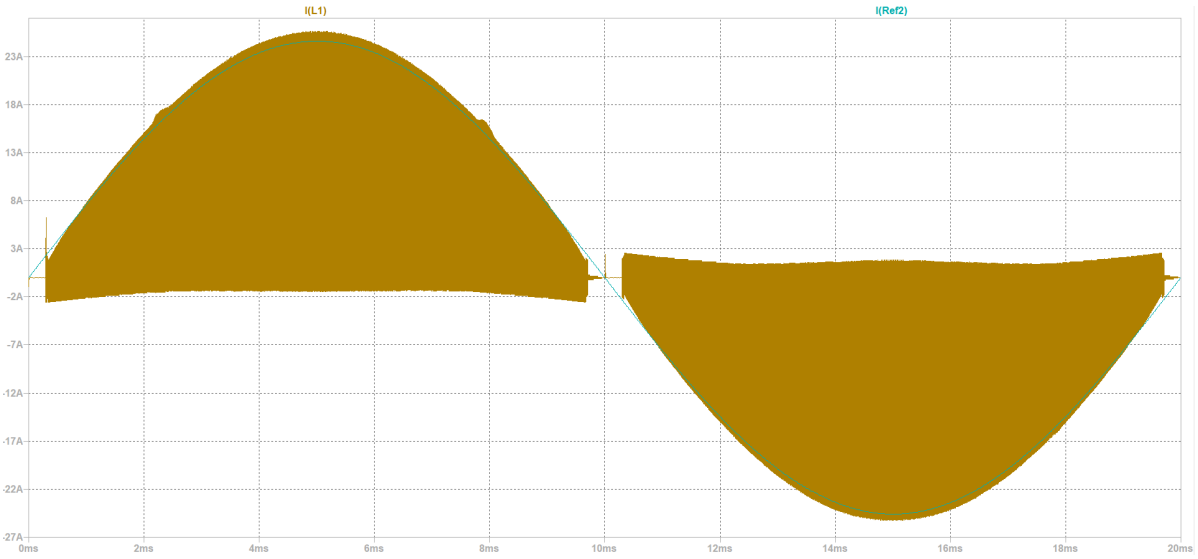


Figure 4.16: Overall current shape, for model with gate driver, $15\mu H$, no margin timing

Comparing with figure4.10, it is clear that the current in figure 4.16 has larger peak value that surpassing the current reference, and smaller value at the valley.

Figure 4.17 4.18 4.19 show the local details at $1ms$, $3ms$, $5ms$, where the red line is the gate voltage for the upper-side GaN switch, the green line is for the Lower-side, the blue line is the scaled-down half-bridge voltage v_{HB}, and the brown line is the inductor current. Moreover, the gray line is the PWM

signal for the lower-side, and the purple line is the PWM signal for the upper-side.

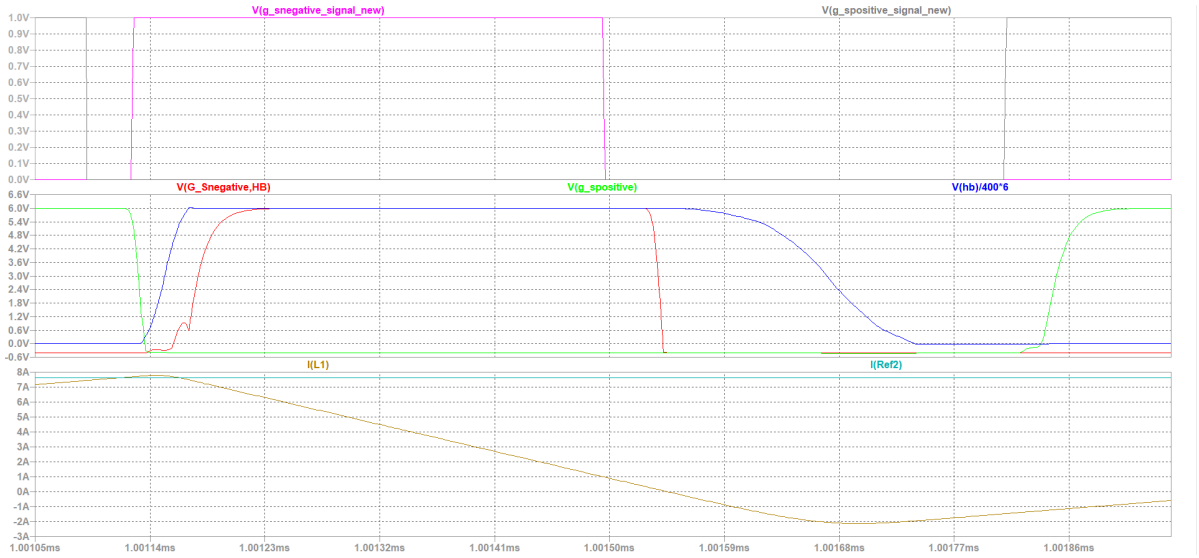


Figure 4.17: Details @1ms, for model with gate driver, 15μH, no margin timing

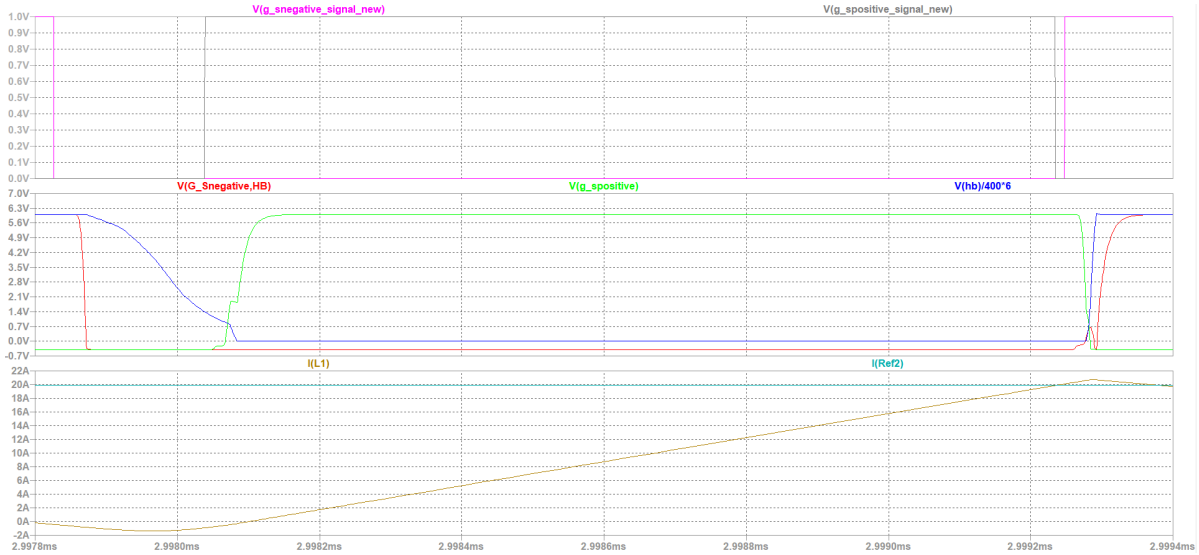


Figure 4.18: Details @3ms, for model with gate driver, 15μH, no margin timing

It is clear from the three figures that there exists time difference between the rising and falling of the PWM signals, and the rising and falling of the actual gate voltage. This time difference is caused by the propagation delay of the gate driver. And because of the delay, the timings been actually applied(the green line and red line) would be different from the expected ones(the gray and purple line). Consequently, the operation will deviate from expectation, causing additional losses in several ways.

In this specific simulation where $ADuM4121$ is uses, the ZVS turn-on of the lower-side GaN switch is lost, as could seen from the figure 4.18 4.19 that, the blue line v_{HB} does not fall to zero when the lower side GaN switch turns on. Moreover, Miller Plateau comes into existence in the gate voltage of the lower-side GaN switch. This results to additional turn-on loss, gate driver loss and noise all at the same time.

Figure 4.20 shows the state plane details at $5ms$, where the green line is the peak current reference value. From figure 4.20a, the actual peak current value when the main switch is turned off, is larger than reference (instead of $24.6A$, it goes up to $25.5A$). This is caused by too long T_{on}. From figure

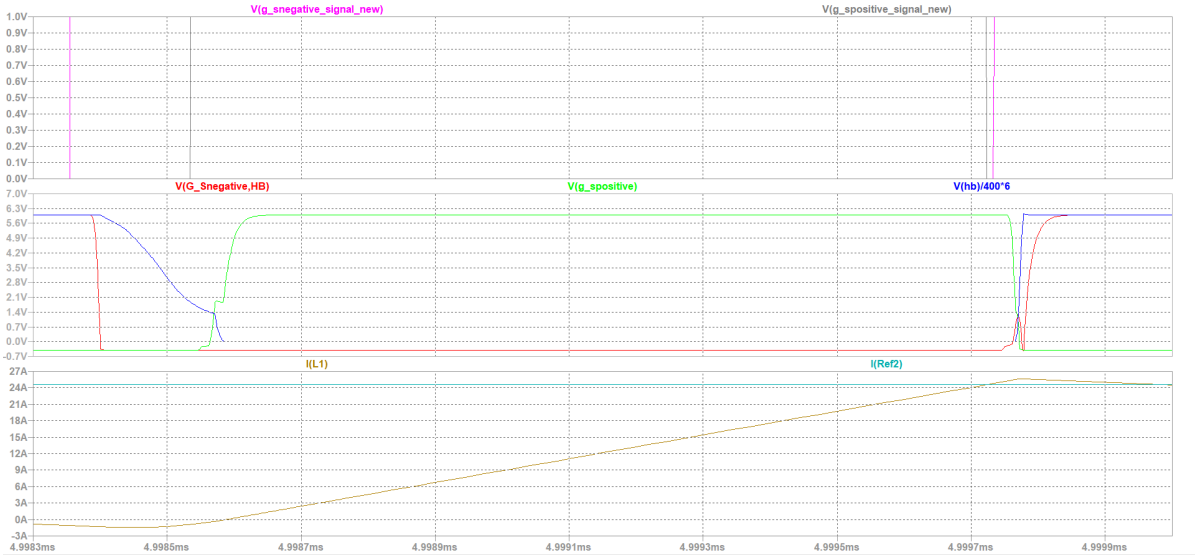
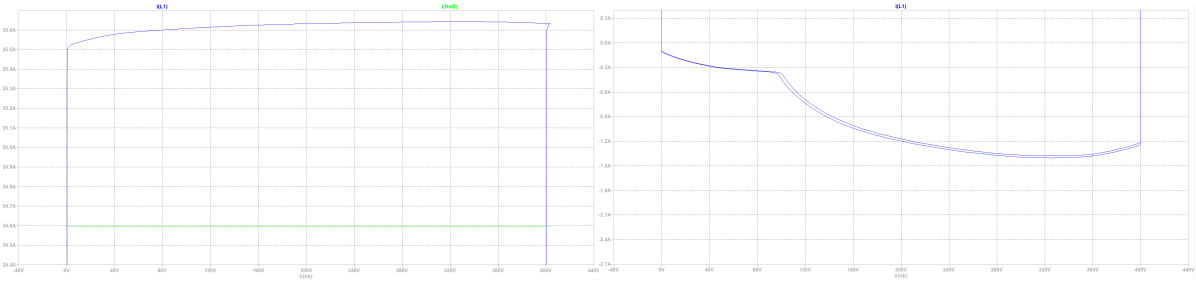


Figure 4.19: Details @5ms, for model with gate driver, 15μH, no margin timing

4.20b, it could be seen that when the lower-side switch is turned on, the voltage on the switch is around $100V$ instead of $0V$. The energy associated with the half-bridge capacitance C_{HB}, $\frac{1}{2}C_{HB}100^2$ will be dissipated as heat during turn-on.



(a) Peak details

(b) valley details

Figure 4.20: peak and valley details

In short conclusion, By simply applying the ideal timing signals, the risk of losing ZVS turn-on of the transistors are high due to the propagation delay issue brought by the gate driver.

This stimulates to investigate what are the critical non-ideal behaviours that exist in practical circuit, what are their impacts on the operation of the converter, and accordingly, how to accommodate them so that the converter could still have the promised high frequency and efficiency.

4.4. Extended Valley Switching with Safety Time Margin

As shown in figure 4.2b and 4.2c, the green trajectory indicates how I_R could be controlled to create safety time margin for the ZVS turn-on of the main switch.

Instead of keep the rectifier switch on for $T_{R(min)}$ after i_L crossed zero from positive value, it is kept on for a longer period of time, noted as $T_{R(margin)}$, so that the current will reach a more negative value $I_{R(margin)}$ instead of $I_{R(min)}$, illustrated as point t_5'' in both figures.

By doing so, at t_6 when the resonant transient is finished, i_L still has a negative value $-I_{margin}$, and this negative current will freewheel through the body diode of the main switch, clamping v_{HB} at zero. Figure 3.2c shows the circuit state for this case. i_L would start to increase linearly once it begins to freewheel through the body diode of the main switch according to equation 3.1. The time period after the t_6 and before i_L rises to zero at t_1, is the safety margin time T_{margin} in which v_{HB} is clamped at $0V$. As long as the main switch is turned on during T_{margin}, ZVS is fulfilled.

According to equation 3.1, the relation between the magnitude of I_{margin} and the duration of safety margin time T_{margin} could be established. If a certain amount of T_{margin} is needed, then correspondingly the required I_{margin} could be calculated as:

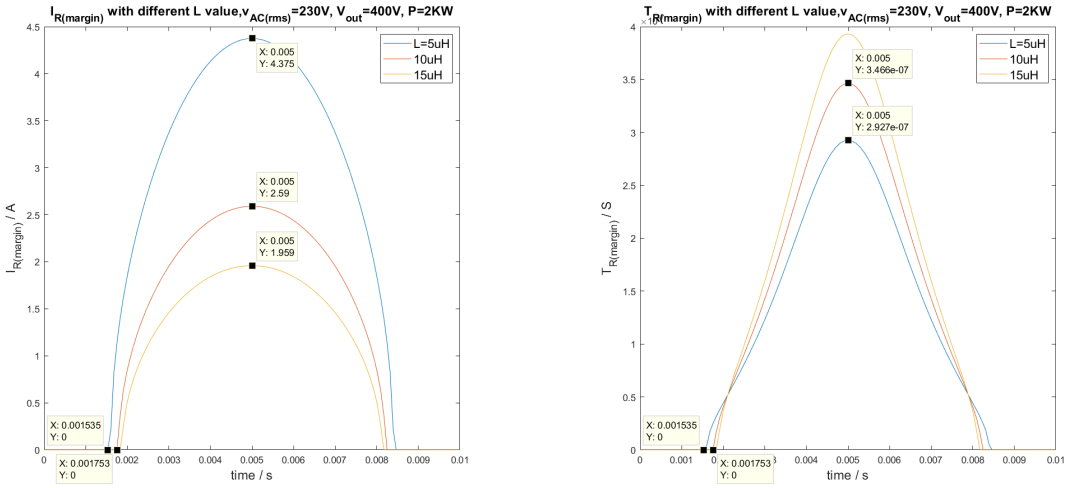
$$I_{margin} = T_{margin} \cdot \frac{v_{AC}}{L} \tag{4.10}$$

Based on the value of I_{margin}, $I_{R(margin)}$ and $T_{R(margin)}$ could be calculated:

$$I_{R(margin)} = \frac{\sqrt{2V_{DC} \cdot v_{AC} - V_{DC}^2 + (I_{margin} \cdot Z_0)^2}}{Z_0} \tag{4.11}$$

$$T_{R(margin)} = \frac{I_{R(margin)} \cdot L}{V_{DC} - v_{AC}} \tag{4.12}$$

Figure 4.21 shows $I_{R(margin)}$ and $T_{R(margin)}$ through the time, with different inductance value. Compared to figure 4.6, it can be seen that negative current is required even before v_{AC} exceeds $\frac{1}{2}V_{DC}$, and the amplitude is larger at the same v_{AC} value. These are caused by the time margin requirement.



(a) $I_{R(margin)}$ (b) $T_{R(margin)}$

Figure 4.21: $I_{R(margin)}$ & $T_{R(margin)}$

Thus, if a safety time margin for ZVS, T_{margin} is desired, the two information that indicates the turning-off of the rectifier switch will be changed into:

- if $i_L = -I_{R(margin)}$
- if the reverse conduction time of the rectifier switch has reached $T_{R(margin)}$

Accordingly, the resonant time between the turn-off of the rectifier switch and the turn-on of the main switch will be shorten, noted as $T_{rvalley(margin)}$, and it could be calculated by following equations:

$$\phi_{valley(margin)} = \pi - arctan(\frac{I_{margin} \cdot Z_0}{v_{AC}}) - arctan(\frac{I_{R(margin)} \cdot Z_0}{V_{DC} - v_{AC}}) \tag{4.13}$$

$$T_{rvalley(margin)} = \frac{\phi_{valley(margin)}}{w_0} \tag{4.14}$$

Figure 4.22 shows $T_{rvalley(margin)}$ through the time with different L value when extended valley switching with ZVS margin is applied.

Thus, if a safety time margin T_{margin} is desired, the two information that indicates the turning-on of the main switch will be changed into:

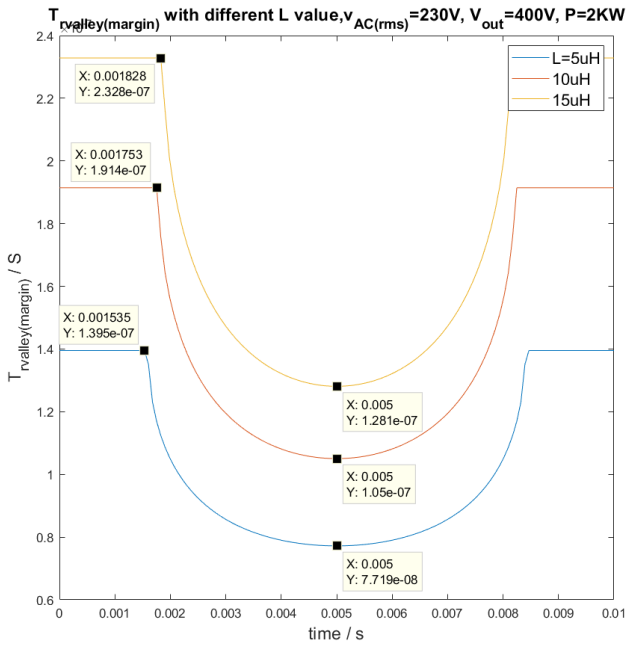


Figure 4.22: The valley resonant transition time with ZVS margin: $T_{rvalley(margin)}$

- if $v_{HB} = 0V$
- if the dead-time after turning off the rectifier switch has reached $T_{rvalley(margin)}$

4.5. Control Methods Based on State Plane Analysis

Based on the arguments in the previous section, the turn-on and turn-off of both switches could be illustrated in a state plane in figure 4.23. Depends on the conditions how the turn-on and turn-off of the switches are determined, there are three possible control methods.

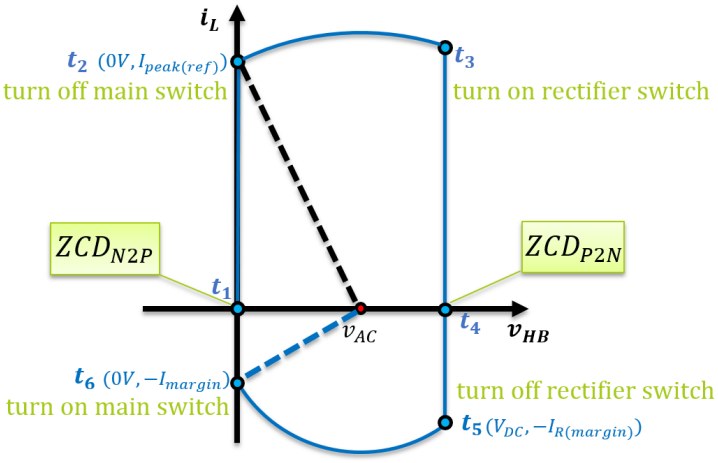


Figure 4.23: The turn-on and turn-off of the two switches in state plane

4.5.1. Current Detection Control (Hysteresis Current Control)

In this control method, the turn-off of both switches is determined by current sensing and instant current comparison. and the turn-on of both switches is based on the turn-off signal and resonant transient timing.

- the turn-off of the main switch is true once the inductor is detected to be equal or larger than the positive current reference value.

$$if\ (i_L \geq I_{peak(ref)}),\ Gate_{mainswitch} = low \tag{4.15}$$

- the turn-on of the rectifier switch is true after the turn-off of the main switch and the peak resonant time T_{rpeak}

$$if\ (t_{dead} = T_{rpeak}),\ Gate_{rectifierswitch} = high \tag{4.16}$$

- the turn-off of the rectifier switch is true when the inductor current is detected to be equal or less than the reverse current reference.

$$if\ (i_L \leq I_{R(margin)}),\ Gate_{rectifierswitch} = low \tag{4.17}$$

- the turn-on of the main switch is true after the turn-off of the rectifier switch and the valley resonant time $T_{rvalley}$

$$if\ (t_{dead} = T_{rvalley}),\ Gate_{mainswitch} = high \tag{4.18}$$

4.5.2. Timing Control, with ZCD as Synchronization Signal

In this control method, the turn-on and turn-off of both switches are based on the pre-calculated timing signals: T_{on}, T_{rpeak}, T_{off}, T_R, and $T_{rvalley}$. A Zero-Current-Detection signal(marked as ZCD) is needed in order to synchronize the timing signal and prevent run-away. Figure 4.24 shows the timing signal sequence for two switching cycle, the inductor current i_L, and the function of the ZCD signal.

The operation run-away is caused by the deviation of the actual states of converter(current, voltage) after applying the timing signals, to the theoretical expected states of the converter, which is in return caused by the non-ideal behaviours of the components. For instance, if i_L is supposed to rise up to zero right after $T_{rvalley}$ finishes, so that following $T_{rvalley}$, the main switch could be turned on for T_{on}, and i_L could reaches $I_{peak(ref)}$ as expected, since T_{on} is defined as the time needed for i_L to rise from $0A$ to $I_{peak(ref)}$. However, if the actual i_L at the end of $T_{rvalley}$ is not zero but still negative, as shown in figure 4.24 at point A, then consequently, if T_{on} is applied right after it, i_L would not reach $I_{peak(ref)}$ after T_{on} at point B. This derivation of i_L will result to undesired additional loss because of the insufficient i_{rpeak} and excess $i_rvalley$ as illustrated by the dashed line in figure 4.24.

The ZCD_{N2P} signal will act as a synchronous signal that prevents this timing mismatch phenomenon by synchronizing the start of every switching cycle, i.e., the start of the T_{on} signal to be the same moment where the current rise up to zero from negative value. As shown in figure 4.24, after the main switch turns on after point A where $T_{rvalley}$ ends, it take some time for i_L to actually rise up to zero at point A'. Then after receiving the ZCD_{N2P} signal, the main switch will be held-on for T_{on} from that moment on, no matter how long it have already been conducting before(A to A'). Thus in such a way, i_L will be able to reach $I_{peak(ref)}$ at B', and the valley peak of the current will not be too negative.

After adding the ZCD signal as synchronization signal, the turn-on and turn-off of the switches could be determined by:

Alternatively, ZCD_{P2N} signal could also be used to ensure the reverse conduction period T_R starts exactly after the current drops to zero. Theoretically, either ZCD_{N2P} or ZCD_{P2N} could be used, or even both. But Practically, it is optimal to always use the ZCD signal of the slower slope for better sensing. During the range $v_{AC} < \frac{1}{2}V_{out}$, it is better to use ZCD_{N2P}, otherwise ZCD_{P2N} is better.

- the turn-off of the main switch is true once the conduction time of the main switch has reached T_{on}, starting from the moment when the current crosses zero from negative value to positive, i.e., $ZCD_{N2P} = true$

$$if\ (ZCD_{N2P} = true\ \&\ t_2 - t_1 \geq T_{on}),\ Gate_{mainswitch} = low \tag{4.19}$$

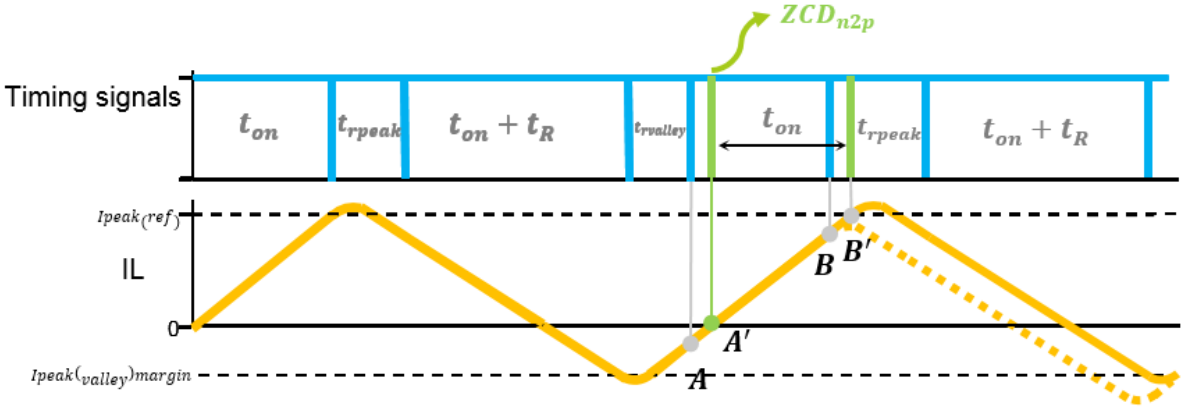


Figure 4.24: The ZCD signal as synchronization signal

- the turn-on of the rectifier switch is true after the turn-off of the main switch and the peak resonant time T_{rpeak}

$$if\ (t_{dead} = T_{rpeak}),\ Gate_{rectifierswitch} = high \tag{4.20}$$

- the turn-off of the rectifier switch is true when the reverse conduction time of the rectifier switch has reached T_R, starting from the moment when the current crosses zero from positive value to negative, i.e., $ZCD_{P2N} = true$

$$if\ (ZCD_{P2N} = true\ \&\ t_5 - t_4 \geq T_R),\ Gate_{rectifierswitch} = low \tag{4.21}$$

- the turn-on of the main switch is true after the turn-off of the rectifier switch and the valley resonant time $T_{rvalley}$

$$if\ (t_{dead} = T_{rvalley}),\ Gate_{mainswitch} = high \tag{4.22}$$

Note that with the aiding of the ZCD signals, the T_{off} timing is not necessary anymore.

4.5.3. Current & Voltage Detection Control (Adaptive Dead-time Control)

In this control method, the turn-off of both switches are determined by current sensing and instant current comparison. The turn-on of both switches are determined by sensing and comparing the half-bridge node voltage v_{HB}.

- the turn-off of the main switch is true once the inductor is detected to be equal or larger than the positive current reference value.

$$if\ (i_L \geq I_{peak(ref)}),\ Gate_{mainswitch} = low \tag{4.23}$$

- the turn-on of the rectifier switch is true when the half-bridge node voltage is detected to be equal to the voltage of the DC bus.

$$if\ (v_{HB} = V_{out}),\ Gate_{rectifierswitch} = high \tag{4.24}$$

- the turn-off of the rectifier switch is true when the inductor current is detected to be equal or less than the reverse current reference.

$$if\ (i_L \leq I_{R(margin)}),\ Gate_{rectifierswitch} = low \tag{4.25}$$

- the turn-on of the main switch is true when the half-bridge node voltage is detected to be equal to 0V.

$$if\ (v_{HB} = 0V),\ Gate_{rectifierswitch} = high \tag{4.26}$$

The requirement of high-speed current sensing and better noise immunity pose challenges on the practical implementation of the *hysteresis current control* and the *current & voltage control* method, especially in the scenario that the switching frequency would be around $1MHz$, because more expensive high-speed devices, and more complex circuits will be needed. Moreover, the variable current reference calls for high on-the-fly computing power. Thus, the two methods are more suitable for low-frequency case (around $100KHz$).

The timing control method requires a pre-calculated Look-Up-Table (LUT), which could output the stored timing signals (T_{on}, T_{rpeak}, T_{off}, T_R, and $T_{rvalley}$) according to different circuit conditions (v_{AC}, V_{DC}, and expected output power). High-speed variable current sensing is avoid, instead, Zero-Current-Detection (ZCD) circuit is needed as a feedback signal, to synchronize the timing signals, which could be easier implemented in terms of complexity of circuit. And the use of LUT reduces the on-the-fly computing stress.

Based on the comparison, the timing control method is chosen to because it is a more cost-effective approach in high-frequency case. FPGA is chosen as the processor, because of its features of high-speed operation and parallel processing. The former feature ensures the operation in high switching-frequency case, while the latter one gives the potential to control several converters at the same time, which effectively reduces the cost. Figure 4.25 shows the implementation of the control in FPGA. The detected v_{AC} and V_{DC} signal will be first converted into digital signal via a integrated Analogy-to-Digital-Converter (ADC), and then together with the expected output power value P, the corresponding timing signals could be got by searching in the preset LUT that is already stored in the FPGA. At the same time, the ZCD signal is also fed into the FPGA, and together with all the timing signals, the PWM signals for the two fast-switching switches could be generated after logic circuitry.

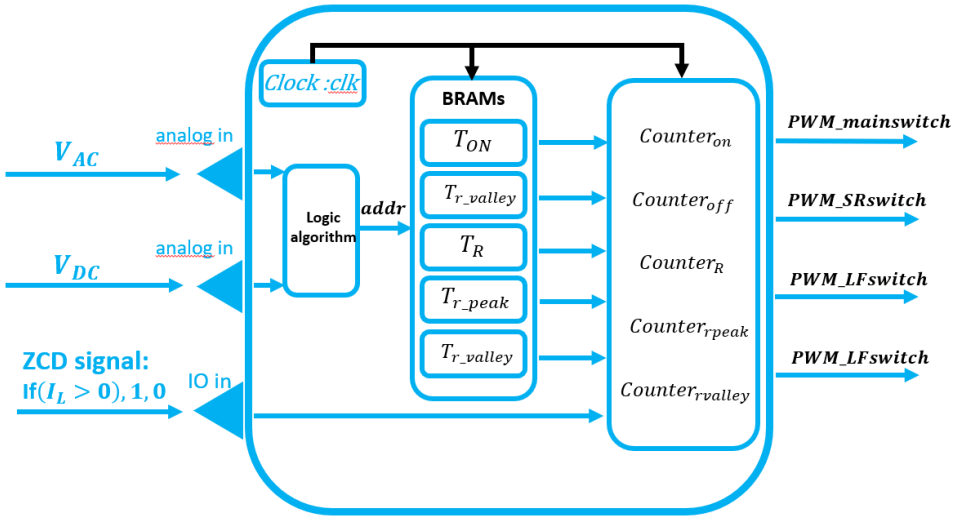


Figure 4.25: The control implementation in FPGA

5

Practical Issues & Solutions

The non-ideal behaviours brought by the components could be divided into two categories, one is ***non-ideal timing***, another is ***non-ideal parameter value***. Within each of the categories there exists several sub-classes and their specific cases. Figure 5.1 gives an overview of the non-ideal behaviours.

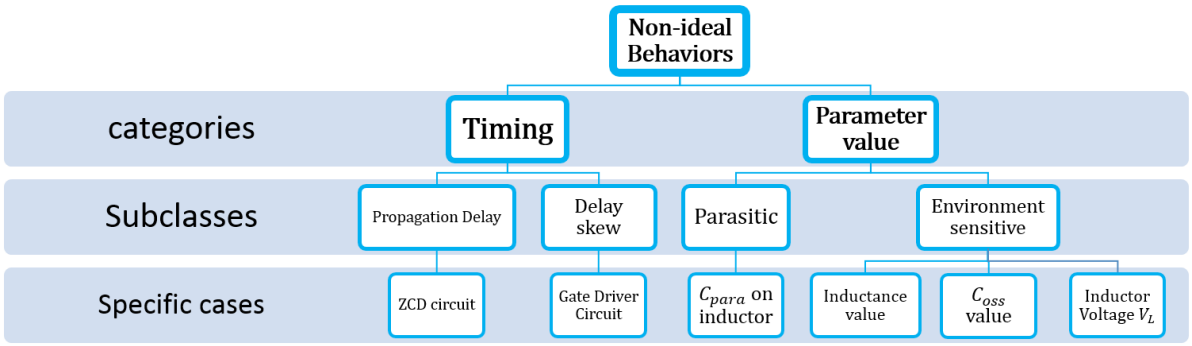


Figure 5.1: The classification of non-ideal behaviours

The causes of the non-ideal behaviours, their impacts on the operation of the converter, and accordingly, the accommodation methods to diminish the impacts are investigated in the following sections.

5.1. Non-ideal Timing

Since the control method of the totem-pole converter is timing-based, any non-ideal timing of the control signals would cause error to the operation of the converter, bringing risk of efficiency reduction.

However in reality, electronics components, especially those who are on the transmission path of control signal, bring inevitable non-ideal timing phenomenons by introducing propagation delay to the signal been transmitted, as well as delay skew.

The propagation delay of a component, T_D, is the length of time which starts when the input to this component becomes stable and valid to change, to the time that the output of the component is stable and valid to change. T_D will have impact on the operation because the receiving of the signal of interest is later than expected, thus the action that is triggered by this signal would take effect later than desired.

5.1.1. ZCD Circuit Propagation Delay

Figure 5.2 show the diagram of the Zero-Current-Detection circuit. The circuit mainly consists of three part Figure 5.2 show the diagram of the Zero-Current-Detection circuit. The circuit mainly consists of three parts: a sense resistor R_s, which could also be replaced by two anti-parallel Schottky diodes; a rail-to-rail comparator which changes its output from one rail to another once I_L changes direction; a signal isolator which isolates the controller and the power circuit.

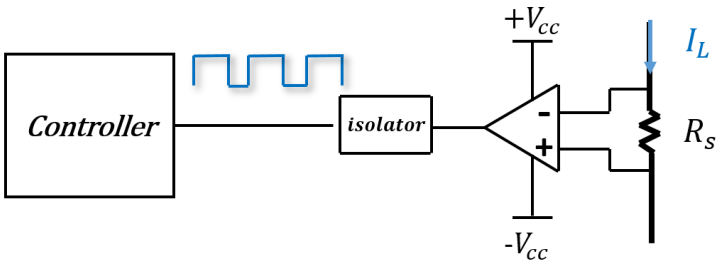


Figure 5.2: Diagram of ZCD circuit

The $T_{D(ZCD)}$ in the ZCD circuit comes from the comparator as well as the isolator, and it will cause additional losses brought by hard-switching loss and conduction loss.

Assuming the negative to positive zero-crossing signal ZCD_{n2p} is been used as the synchronization signal. Because of this $T_{D(ZCD)}$, the ZCD signal will be later than expected, as illustrated as figure 5.3. Instead of receiving the ZCD signal at point A, certain propagation delay is added so that the signal is received at A', where i_L is already a certain positive value. Then i_L will continue to rise linearly for a time period of $T_o n$, resulting to the excessive i_L value at B' when the main switch is turned off. This in turn has an influence on the valley value of i_L, making it not reach the desired value.

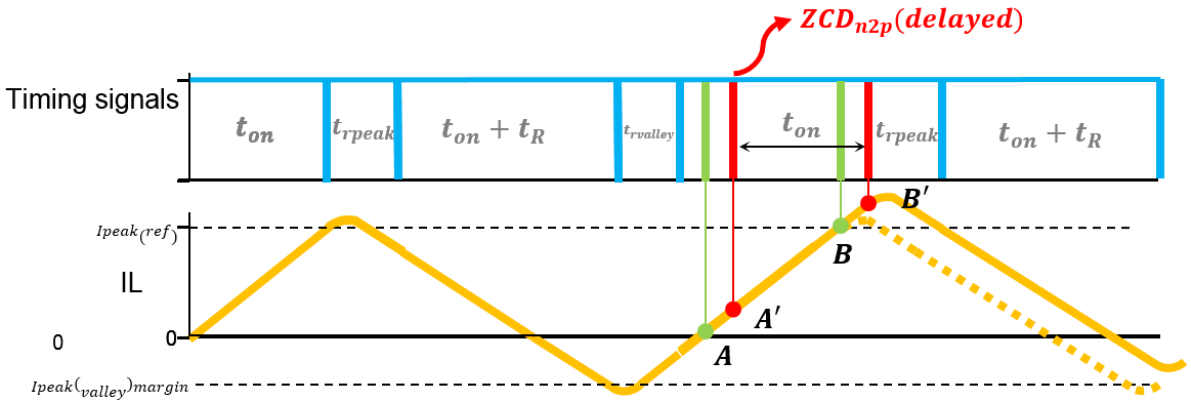


Figure 5.3: The effect of the propagation delay in the ZCD circuit

In order to show the effect of the propagation delay of the ZCD circuitry, a simulation is carried out as comparison to the perfect simulation, by manually adding a $13ns$ delay (the value $13ns$ is because of the delay from the actual components selection, comparator: $ADCMP600$, digital isolator: $ADuM210N$) to the ZCD signals.

Figure 5.4 5.5 5.6 show some local details at $t = 1ms$, $t = 3ms$, $t = 5ms$, where the red line is the gate voltage for the upper-side GaN switch, the green line is for the Lower-side, the blue line is the scaled-down half-bridge voltage $v_{HB}/V_{out} \times 6$, and the brown line is i_L.

Different from figure 4.11 4.12 4.13, with the propagation delay from ZCD circuitry, V_{HB} is not able to drop to zero during $T_{rvalley}$ anymore when $v_{AC} > \frac{1}{2}V_{out}$, as shown in figure 5.5 and 5.6, which means ZVS turn-on of the main switch is lost. This is because the $I_{peak(ref)}$ is higher than expected due to $T_{D(ZCD)}$, resulting to the insufficient I_R when T_R ends. The reason why V_{HB} could still drop to $0V$ in figure 5.4 is because the effect of $T_{D(ZCD)}$ could be tolerated by the ZVS margin of the natural valley switching.

Figure 5.7 shows the peak and valley details of the state plane of i_L and V_{HB} at around $t = 5ms$. It can be seen that due to T_{DZCD}, i_L exceeds $I_{peak(ref)}$ (instead of $24.6A$, it is $24.88A$), and the main switch is turned on at $40V$ instead of $0V$, causing additional switching loss.

In the case where the negative to positive zero-crossing signal ZCD_{n2p} is used as the synchronization signal, the solution to this problem is to shorten the conduction time of the main switch, by reducing the T_{on} value to $T_{on} - T_{D(ZCD)}$. In the case where ZCD_{p2n} is used as synchronization signal, the solution is to shorten the reverse conduction time of the rectifier switch, by reducing the T_R value to

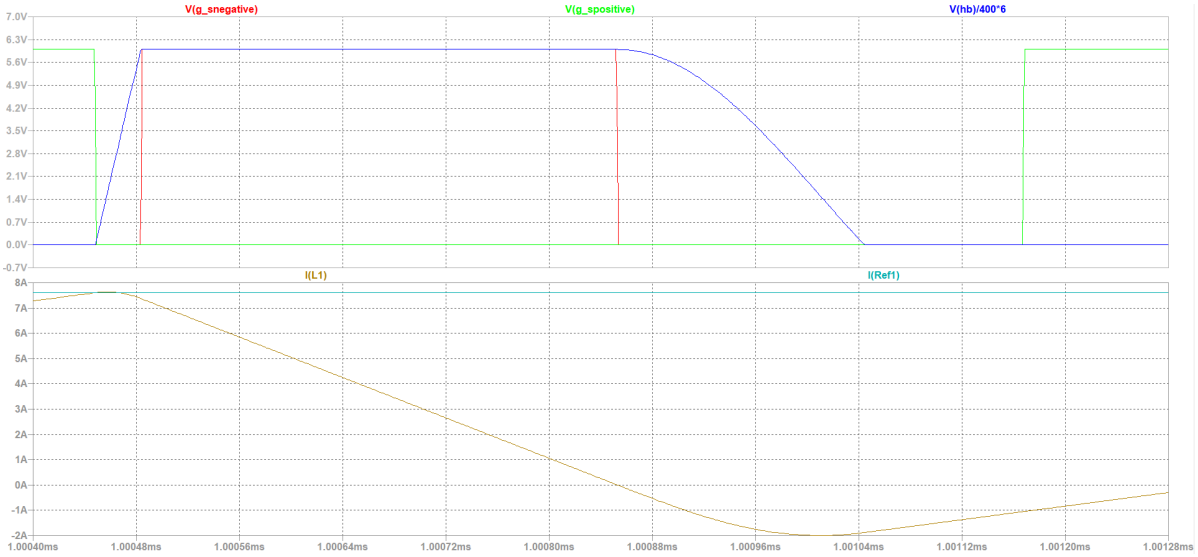


Figure 5.4: Details @1ms, for ideal model with ZCD delay, 15μH, no margin timing

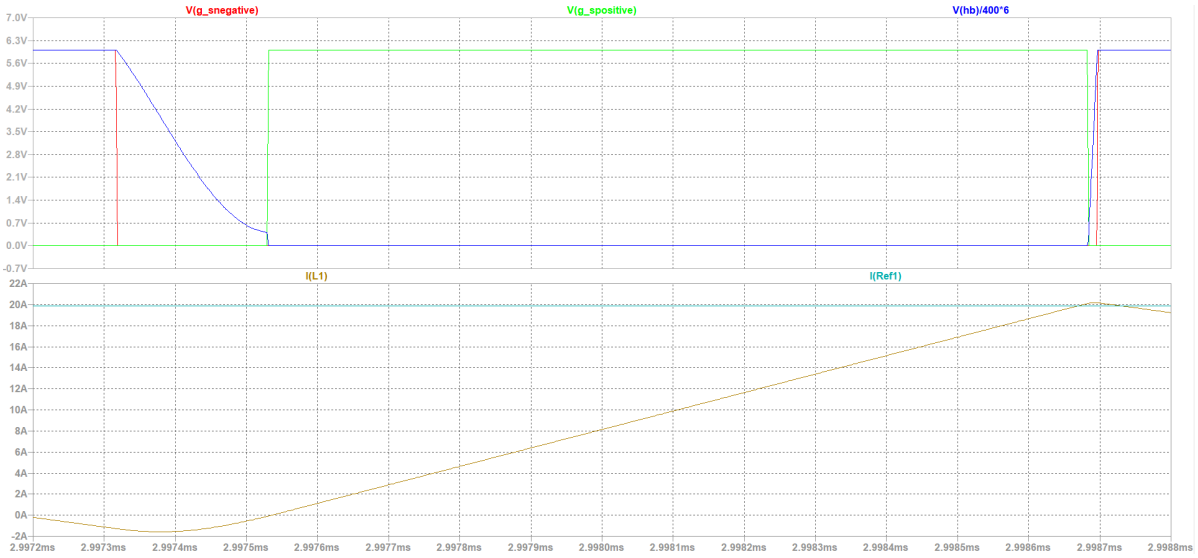


Figure 5.5: Details @3ms, for ideal model with ZCD delay, 15μH, no margin timing

$T_{on} - T_{D(ZCD)}$. The value of $T_{D(ZCD)}$ could be estimated based on the datasheets of the comparator and the isolator. The ZCD circuit on the actual demo board is populated with the comparator $ADCMP600$, and the digital isolator $ADuM210N$, with typically $5ns$ and $7ns$ propagation delay with the specific supply voltage[45][46]. Thus $T_{D(ZCD)}$ could be roughly estimated to be $13ns$. This value would vary with the changing of operation environment, such as the value of the supply voltage of the components, the input overdrive voltage of the comparator, and the temperature at which the components operate in, etc. The value of $T_{D(ZCD)}$ could be tested on the actual circuit afterwards.

5.1.2. Gate Driver propagation delay

The gate driver brings certain delay T_D between the PWM signal been sent to the input of the gate driver, and the actual gate driving voltage out from the gate driver. The rising propagation delay t_{DLH} may be defined as the time difference between the input edge rising above the input logic high threshold V_{IH} to the output rising above 10% of its final value. And the falling propagation delay t_{DHL} may be defined as the time difference between the input edge falling below the input logic low threshold V_{IL} to the time output falls below 90% of its high level. Figure 5.8 illustrates the rising and falling propagation

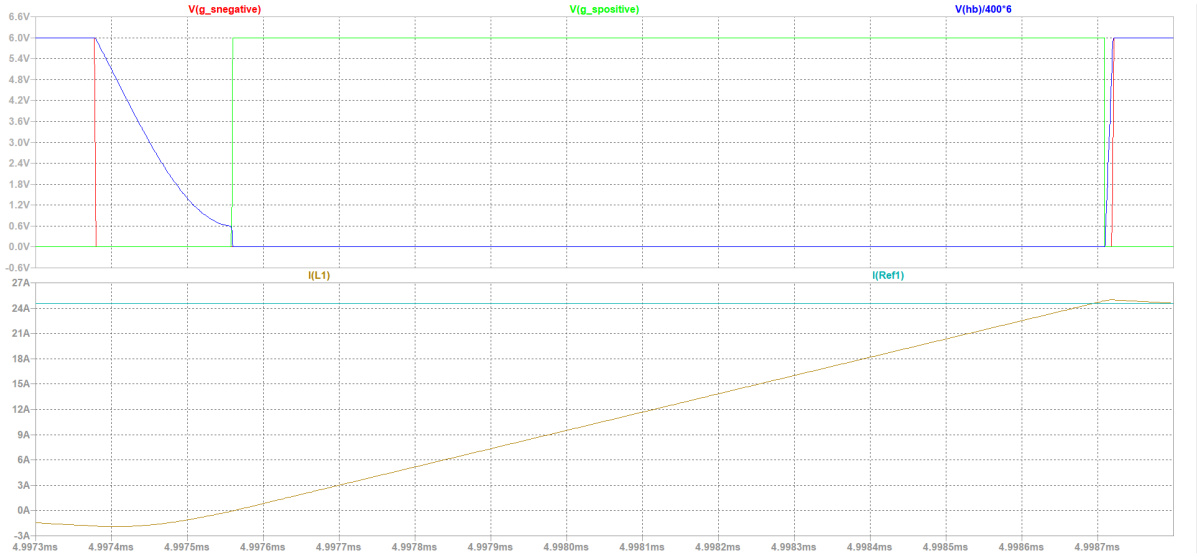
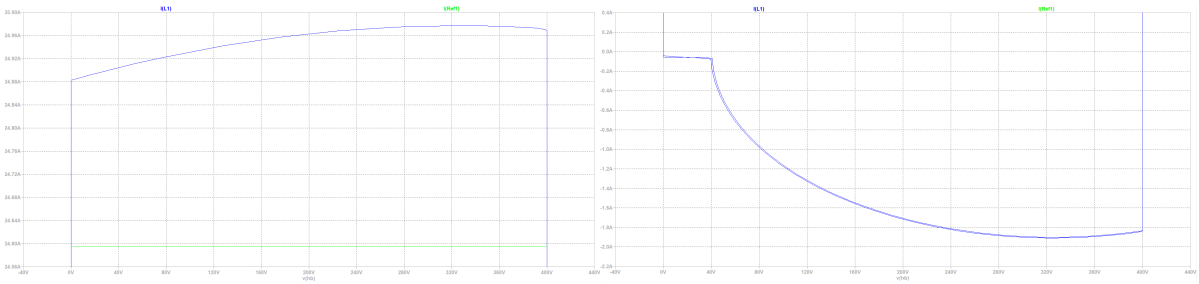


Figure 5.6: Details @5ms, for ideal model with ZCD delay, $15\mu H$, no margin timing



(a) Peak details (b) valley details

Figure 5.7: peak and valley details of the state plane @5ms, for ideal model with ZCD delay, $15\mu H$, no margin timing

delay of the gate driver, where the upper waveform is the PWM input of the gate driver, and the lower waveform is the output gate voltage of the gate driver.

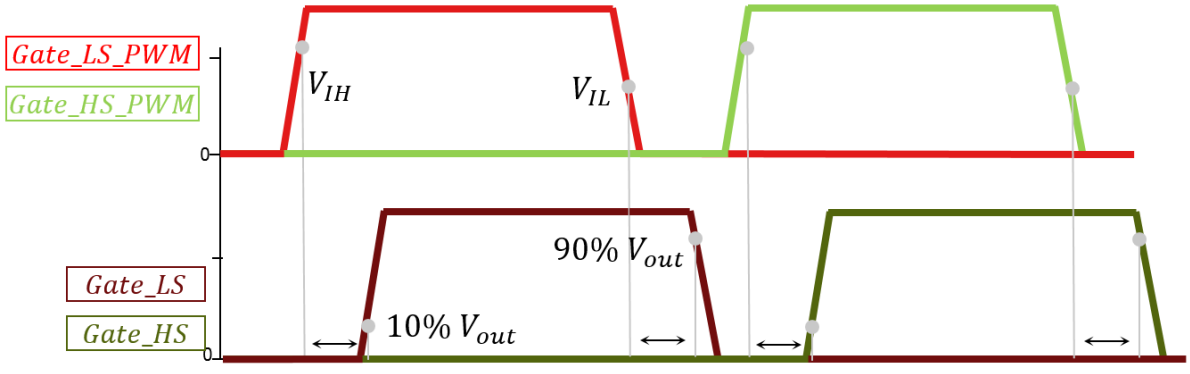


Figure 5.8: Propagation delay of gate driver

The T_D in half-bridge gate driver comes from the slow high voltage level shifter (for high-side driving), and the deglitching and filtering circuitry, which is to avoid noise triggering in the output. Many available isolated half-bridge drivers nowadays have T_D less than $100ns$. For example, $Si827x$ from SILICON LABS has a propagation delay typically less than $60ns$[47], and $ADuM4121$ from ANALOG DEVICES has delay less than $53ns$[48].

The direct impact of the propagation delay of gate driver is that the switch will be turned on and off latter than intended. Assuming that $t_{DLH} = t_{DHL}$, i.e., the duration of the PWM signal is the same as the output driving signal. In the scenario where v_{AC} is in the first quadrant of a line cycle, the overall delay of the PWM signal will cause one switching cycle to happen at a higher than expected v_{AC}. The consequence is that the inductive energy might be insufficient during both the peak and valley resonant transition period and ZVS turn-on of switches would lost, bringing additional turn-on loss. The additional turn-on loss will be determined by the difference between the v_{AC} that is expected to be and the actual v_{AC} when the switching action takes place. And fundamentally, it is determined by the value of T_D.

However, based on the fact that the propagation delay is less than $100ns$ if proper gate driver is implemented, there will only be a very small increment of v_{AC}, Δv_{AC} for the switching actions. To be specific, v_{AC} will increase $9.7mV$ at t=1ms after $100ns$, where its initial value is $100.5234V$; and it will increase $3.2mV$ at t=4ms after $100ns$, where its initial value is $309.3493V$. Such small variation of v_{AC} only causes trivial energy change, because the capacitive energy increment ΔE_{cap} brought by Δv_{AC} is so small, that it only takes about 0.02% of the initial capacitive energy. Thus the propagation delay within the level of $100ns$ will not bring apparent impact on the efficiency, nor the ZVS performance of the converter. For simplicity consideration, the compensation of this propagation delay will not be used.

5.1.3. Gate Driver Propagation delay Skew and Pulse Width Distortion

Delay skew t_{skew} is the time difference between the output transitions on two different parts when reacting to the same input signal in the same operating condition. Pulse Width Distortion (PWD) is the possible difference between rising and falling propagation delay on the same part. Thus, pulse width distortion $(PWD) = |t_{DLH} - t_{DHL}|$. The two phenomenons together, will not only change the pulse width duration of one PWM signal, making T_{on} and $T_{off} + T_R$ longer or shorter, but also will change the dead-time between two PWM signals, making T_{rpeak} and $T_{rvalley}$ longer or shorter, having profoud influence on the timing signals.

Among the many possible scenarios, there are two worst scenarios that pose risk of cross-conducting and fail of ZVS: Figure 5.9 illustrates the first scenario, in which the T_on is extended by $t_{DHL(HS)} - t_{DLH(HS)}$ (pulse width distortion of the high-side switch), T_{rpeak} is extended by $t_{DLH(LS)} - t_{DHL(HS)}$ (delay skew of the two switch and pulse width distortion of each switch), while $T_{off} + T_R$ is shortened by $t_{DLH(LS)} - t_{DHL(LS)}$ (PWD of the low-side switch), and $T_{rvalley}$ is shortened by $t_{DHL(LS)} - t_{DLH(HS)}$.

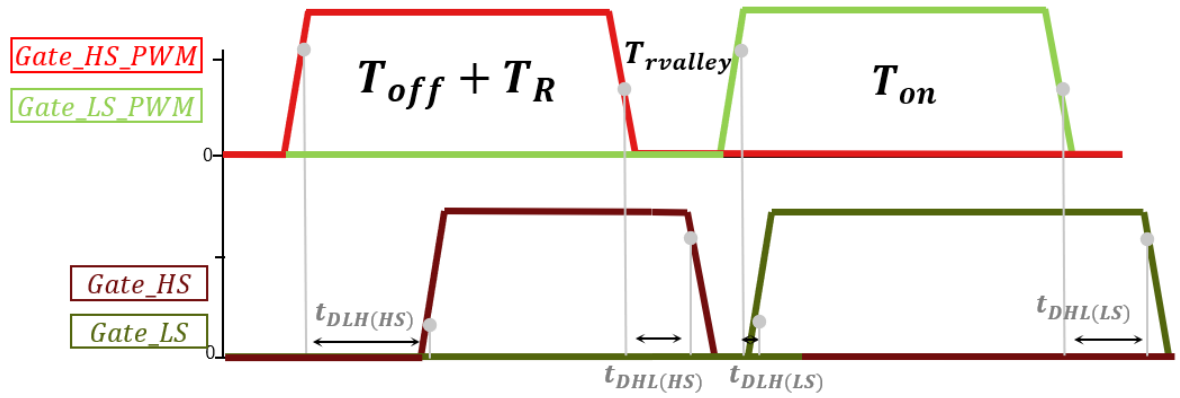


Figure 5.9: Gate driver effect: T_{on} and T_{rpeak} is extended, $T_{off} + T_R$ and $T_{rvalley}$ is shortened

The impacts are:

1. The shortened $T_{rvalley}$ will lead to hard turn-on of the main switch, or even cross conduction of the fast switching leg when the original transition period is very short.
2. the extended T_{on} will lead to excessive I_{peak} and insufficient I_R, which makes the first consequence worse.

Figure 5.10 shows the second scenario, in which both the $T_{rvalley}$ and T_{rpeak} are extended, and $T_{off} + T_R$ and T_{on} are shortened.

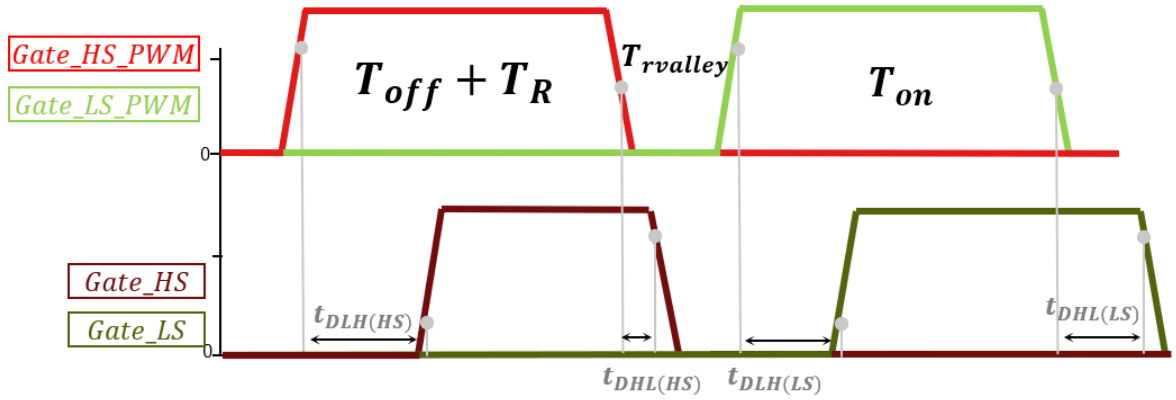


Figure 5.10: Gate driver effect: $T_{rvalley}$ and T_{rpeak} is extended, T_{off} + T_R and T_{on} is shortened

The consequences are:

1. The extended resonant transition, especially $T_{rvalley}$, will lead to hard switching-on of the main switch.
2. the shortened $T_{off} + T_R$ will lead to insufficient I_R, which makes the first consequence worse.

The simulation as shown in figure 4.15 in the previous section demonstrates the first scenario. After adding the gate driver circuit, as can be seen from figure 4.20a that i_L clearly exceeds $I_{peak(ref)}$ when the main switch turns off, and from figure 4.20b that the mains switch is turned on at $V_{HB} = 100V$. The junction temperature T_j of the two GaN switches are recorded using the temperature measurement in the LTspice model. In the case where no gate driver is added, and the perfect timing with zero margin is applied, T_j of the upper-side and the lower-side GaN switch rises by $3°C$ and $3.1°C$ after $20ms$ (one line cycle) respectively. In comparison, the temperature increment after adding gate driver circuit is $3.4°C$ and $3.6°C$ respectively, which is about 15% additional loss that mainly comes from the hard turn-on.

In order to prevent cross-conduction, both $T_{rvalley}$ and T_{rpeak} need to have an additional resonant transition time T_{safety} on the basis of the ideal calculation, which could be calculated by

$$T_{safety} = t_{DHL(max)-t_{DLH(min)}} \tag{5.1}$$

According to the datasheet of $si827x$:

$$t_{DHL(max)} = t_{DLH(max)} = 60ns$$

$$t_{DHL(min)} = t_{DLH(min)} = 20ns$$

Thus T_{safety} could be set to be $40ns$.

Meanwhile, in order to ensure ZVS could still be achievable with T_{safety} in the case where the $T_{rvalley}$ is extended, the safety margin time for ZVS, T_{margin}, should be set to be:

$$T_{margin} = T_{safety} + (t_{DLH(max)} - t_{DHL(min)}) \tag{5.2}$$

For the case in which $si827x$ is used, T_{margin} could be set to be $80ns$

Last but not the least, the excessive I_{peak} and insufficient I_R brought by the Pulse-Width-Distortion (PWD) of a gate driver could be solved by reducing or increasing the T_{on} or $T_{off} + T_R$ by PWD, after measuring the specific PWD. However, the typical Pulse-Width-Distortion is within the range of $10ns$[47] [48], thus this consideration is more relaxed.

By introducing both T_{safety} and T_{margin}, cross conduction of the two fast-switching switches could be prevent, and the resonant transient periods T_{rpeak} and $T_{rvalley}$ could be controlled to be abundant for ZVS even with the worst case delay mismatch, with the premise that the PWD is small that it would not bring noticeable variation to T_{on} and $T_{off} + T_R$.

A propagation delay testing for the gate driver could be conducted prior to the actual operation in order to get a more precise propagation delay information. This test could be done by applying PWM signal to the gate driver and test the output of it.

5.2. Non-ideal Parameter Values

Unlike the timing issue as discussed in the last section, non-ideal parameters would not directly change the timings, however, it will change the operation environment in which the converter is operating, this will also have significant effect on the performance.

The parameters that determine the operation environment includes:

- the half-bridge capacitance value C_{HB}, which consists of C_{oss} from the switch and C_{para} from the other part of the circuit board;
- the inductance value L of the main inductor;
- the voltage over the inductor V_L

5.2.1. Non-ideal C_{para} value

When two electrical conductors at different voltages are close together, the electric field between them causes electric charge to be stored on them. The parasitic capacitance, or stray capacitance associated with the half bridge (HB) is the unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other. The larger the C_{para}, the more inductive energy is needed in order to charge / discharge the capacitance, which means longer reverse conduction time T_R, and longer resonant transient period T_{rpeak}, $T_{rvalley}$, which would increase the rms value of i_L, as well as THD of the input current to some extent.

One of the sources of C_{para} is the inductor. Depending on the way the winding is formed, C_{para} of an inductor could range from $2pF$ to several hundredth pF. In order to reduce the stray inductance brought by the inductor winding structure, a structure shown in figure 5.11 is used, for the purpose of minimize the overlapping area between electrical conductors at different voltages.

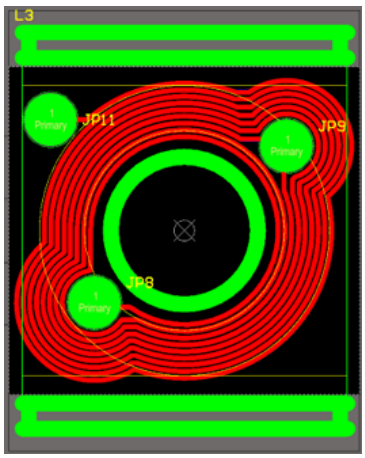


Figure 5.11: Planar inductor winding layout

The red lines are copper traces with $0.07mm$ thickness, $0.81mm$ width that form the winding of the inductor, and the green parts includes the sectional view of the ER64 core, and three connectors, from which two of them could be used to have different number of turns. All number of turns are in the same layer, thus the conductors with different voltages have the minimum overlapping area. the same sheet of layer could be stacked up together through the connectors, so that the current capability of the winding could be improved without additional stray capacitance, because even though there are overlapping between different layers, there is no voltage difference between them.

After minimize the stray capacitance of the inductor, a $300pF$ C_{para} from the PCB board is still took into consideration during timing calculation for design margin.

5.2.2. Inductor Voltage V_L

Together with the inductance value L, the voltage across the inductor, V_L will directly determine the inductor current i_L according to equation 3.1. Ideally, V_L equals to v_{AC} when main switch is on, or $V_{DC} - v_{AC}$ when the rectifier switch is on. However, there exists voltage drop on the on-conduction

resistance of switches $R_{ds(on)}$, and DC resistance of the inductor R_L. The effect of this deviation of V_L will result to insufficient I_{peak} and excessive T_{valley}.

During the T_{on} where the main switch is on, V_L will be less than v_{AC} by the voltage drop on $R_{ds(on)}$ (from the main switch, as well as the line frequency switch) and R_L. Based on equation 3.1, the current changing rate will be smaller with less V_L, thus after a settled T_{on}, the current value at the end of T_{on} will be less than desired. This might cause the lost of ZVS turn-on of the rectifier switch if T_{rpeak} does not have margin.

During the T_{off} where the rectifier switch is on, and i_L is still positive (it's relative concept, during positive line cycle, positive i_L means it is positive value; during negative line cycle, positive i_L means it is negative value), V_L will be larger than $V_{out} - v_{AC}$ by the voltage drop on $R_{ds(on)}$ and R_L. Thus after a settled T_{off}, the voltage will have a larger decrease than expected.

During the T_R where the rectifier switch is on, and i_L is negative (it's relative concept, during positive line cycle, negative i_L means it has negative value; during negative line cycle, negative i_L means it is positive value), V_L will be less than $V_{out} - v_{AC}$ by the voltage drop on $R_{ds(on)}$ and R_L. Thus after a settled T_R, the voltage will have less decrease than expected.

The effect would get more significant when the current is high, and the duration of the rising and falling of the current is longer, i.e., when v_{AC} is large. Since i_L is low, and duration is short during T_R, the effet during T_{off} will be dominant.

In order to minimize the impact of the deviation of V_L, the fundamental measure is to reduce the resistance on the path. The switches have settled $R_{ds(on)}$ that can only be changed by choosing another switch, but the series resistance on the inductor could be reduced by paralleling conductors. After reducing resistance from the source, the problem could be accommodated by designing the T_{rpeak} to be longer in order to finish peak resonant transient.

Comparing the effect of the deviation of V_L to the effect of the ZCD delay, it can be observed that they compensate each other to some extent.

5.3. L & C_{oss} Error

The inductance value L and the output capacitance value C_{oss} would vary with the operation environment and condition. Due to the non-linear relationship between the magnetic field strength $H(A/m)$ and the magnetic flux density $B(Tesla)$ described by the $B-H$ curve, as shown in figure 2.8. the inductance value decreases gradually as i_L increase, until when i_L is too high that the inductor saturates and the inductance value decreases dramatically.

The output capacitance of the transistor C_{oss} is the main part of C_{HB}, and its value depends heavily on the drain-source voltage V_{ds} at which the transistor operates. Figure 5.12 shows the typical C_{oss} vs V_{DC}

It could be seen from figure 5.12 that C_{oss} will drop as V_{DC} increases, and in low V_{DC} below $200V$, C_{oss} varies in a large range. This is not an issue when looking at steady state operation, since V_{DS} would be maintained at around $400V$. However, during the start-up transition where the output voltage is building-up from low value, the variation of C_{oss} would lead to the lost of ZVS turn-on of the switches.

In order to reduce the impact of the variation of L, the inductor could be designed in such a way that the maximum magnetic flux density B_{max} is well below the saturation value, so that the inductor could operating in a more linear region in which the inductance value would have minimum variation. Moreover, during the calculation of timing, a 10% variation could be took into consideration for more reliable operation, by using 90% of the inductance value for calculation. (however, this will bring more conduction loss, cause it will lead to larger I_{peak} and I_{peak})

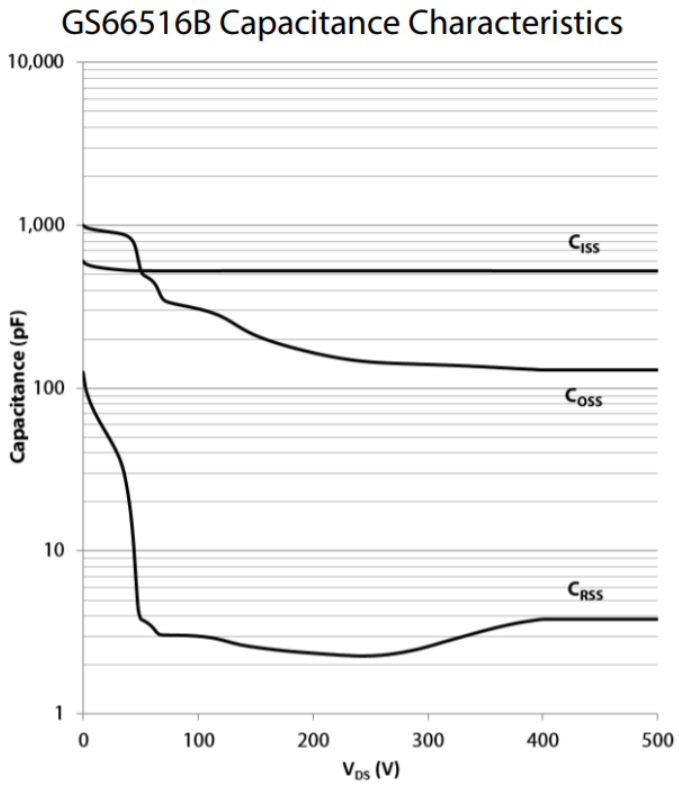


Figure 5.12: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

6

Hardware Implementation and Verification

In order to demonstrate the feasibility of the GaN totem-pole topology, and the timing control method together with the non-ideal consideration for achieving ZVS, a GaN totem-pole converter is built, a $20\mu H$ inductor and a $9\mu H$ inductor are built (the inductance value is measured using portable LCR meter: BK Precision, model 879B). Two sets of set-point tests will be carried out. The set-point test is done by operating the converter with specific input and output voltage using DC power supply and electronic load. And by performing multiple set-point tests with different input voltage, the feasibility of the converter to operate through the AC input voltage could be demonstrated indirectly.

Figure 6.1 shows the hardware test set-up.

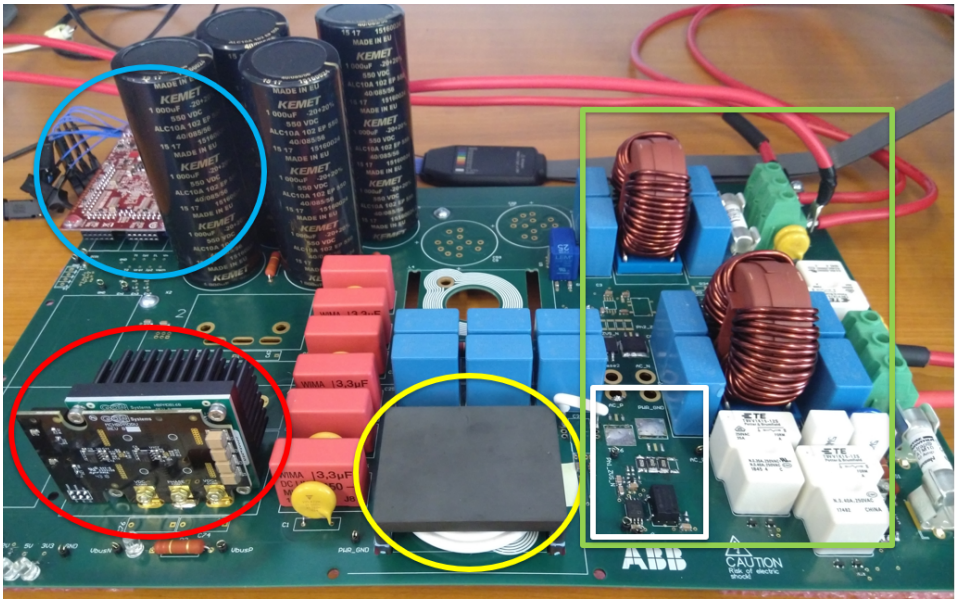


Figure 6.1: Test set-up

In the green square area in figure 6.1 is the AC input and DC output connectors, and filters that consist of CM choke and capacitors. The AC input is supplied by a power supply, and the output is connected to an electronic load. In the white square area is the ZCD circuitry (comparator: $ADCMP600$, digital isolator: $ADuM210N$), which is constructed as shown in figure 5.2. Next to the ZCD circuitry lays the PFC inductor (core material: 3F36, shape: ER64). In the red circle area is the GaN half-bridge power module from $GaN\ Systems$[49] [50]. On this power module there are two 650V, 60A GaN transistor $GS66516B$[51] to form a half-bridge switching leg, and two isolated gate drivers with

optimal layout to drive the transistors [47]. In the blue circle area is the FPGA controller board (Cora Z7)[52].

6.1. Practical ZCD Signal Processing and Protection

In section 4.5.2, the Zero-Current-Detection function is explained, and the ZCD circuitry is given in figure 5.2. According to the states of the output of the comparator (high or low), the direction of i_L could be indicated. In this test set-up, the ZCD circuitry is constructed in such a way that the ZCD signal is high when i_L flows out from AC input into the switching leg, and is low when the direction is reversed. But in order to detect the moment when the current crosses zero, it is the rising edge (POSEDGE) or falling edge (NEGEDGE) of the output signal should be monitored. This is done by an *EDGE detecting* function in the control algorithm. Figure shows the *EDGE detecting* function on work, in which the red line is the comparator output that is sent into the FPGA, the blue and green line are the POSEDGE and NEGEDGE of the comparator output respectively. After this, the two EDGE signals could be used as ZCD signals that indicateds when the current crosses zero.

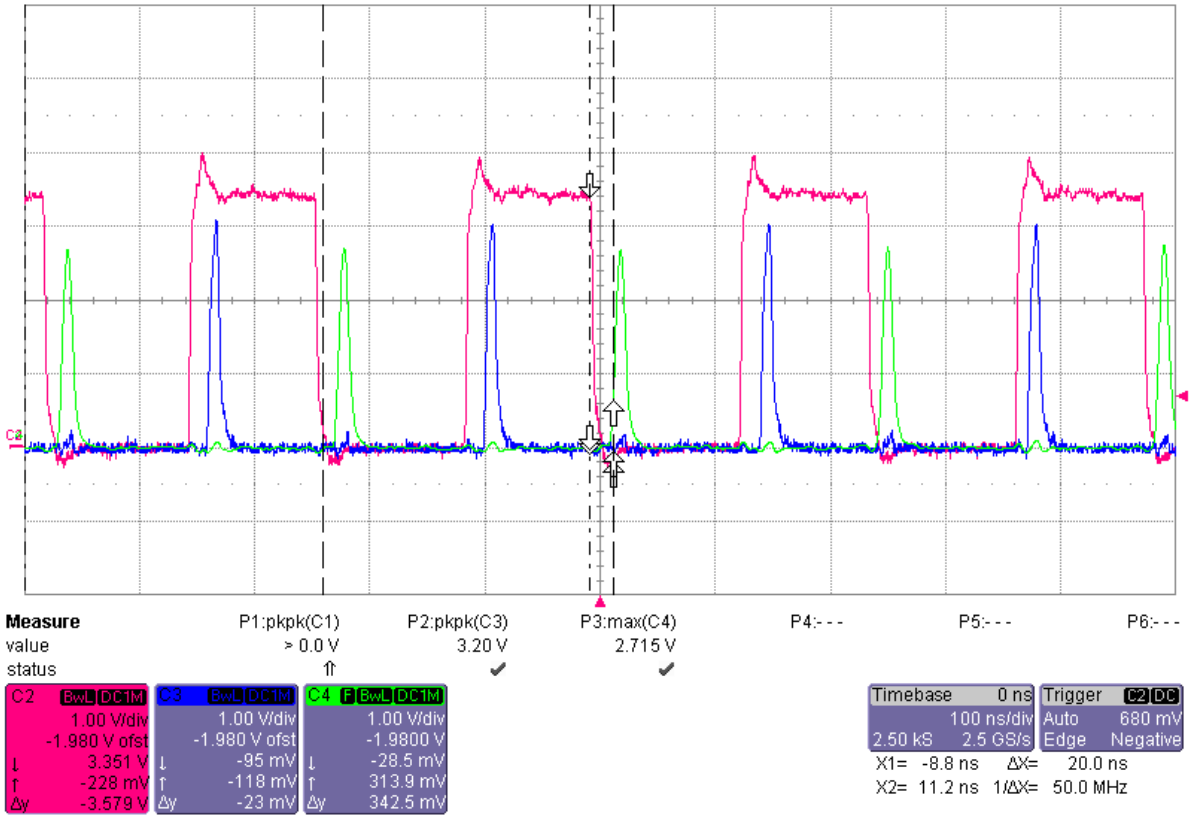


Figure 6.2: EDGE detecting function

It could be notice that there exists around 20ns delay between the EDGE signals and the actual edges of the comparator output. This is due to the algorithm of the EDGE detecting. In practical application, there will be another 40ns delay between the detecting of the EDGE signals and the actual moment when the EDGE signals are utilized to regulate the PWM signals. The reason for this remains to be investigated. These delays could be easily compensated by reducing the value of T_{on} and T_R. In this test, the $60ns$ delay of the POSEDGE is compensated by reducing the duration of T_{on} by 7 clock cycles ($56ns$), while the delay of the NEGEDGE is kept. The reason is to have more margin for the ZVS during the valley.

In the processing of ZCD signals, protection algorithms are needed to ensure the switching cycles are synchronized by the ZCD signals, and that the noise of the output of the comparator does not false trigger the EDGE signals. If the switching cycle is not synchronized by ZCD signals, i_L would drift away since the timing calculation have certian error. And if the noise of the ZCD signals are too big, the

switches have risk of false turning on if there is no protection.

In order to prevent i_L drifting away, the switching action is only allowed to continue if both POSEDGE and NEGEDGE signals are detected during each switching cycle. Otherwise the switching will cease. In order to prevent false triggering, only the first POSEDGE or NEGEDGE signal is used during each switching cycle.

Figure 6.3 and 6.4 together illustrate the protection function on work, in which the blue and green line are the PWM signal for the main switch and rectifier switch respectively, and the red line is the output of the comparator that has been sent to the FPGA.

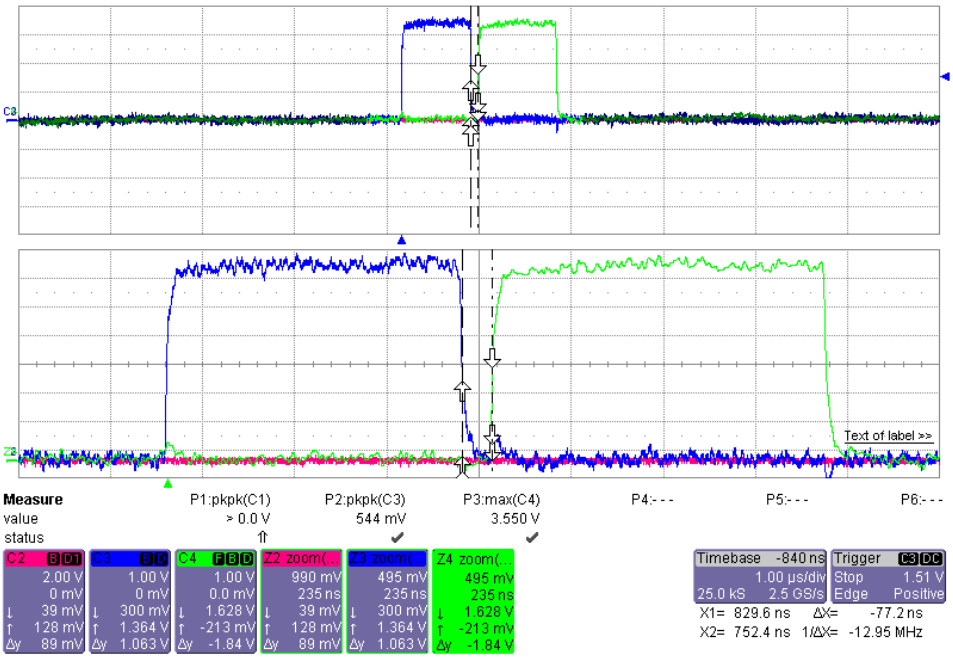


Figure 6.3: PWM signals without detecting ZCD signals within one switching cycle

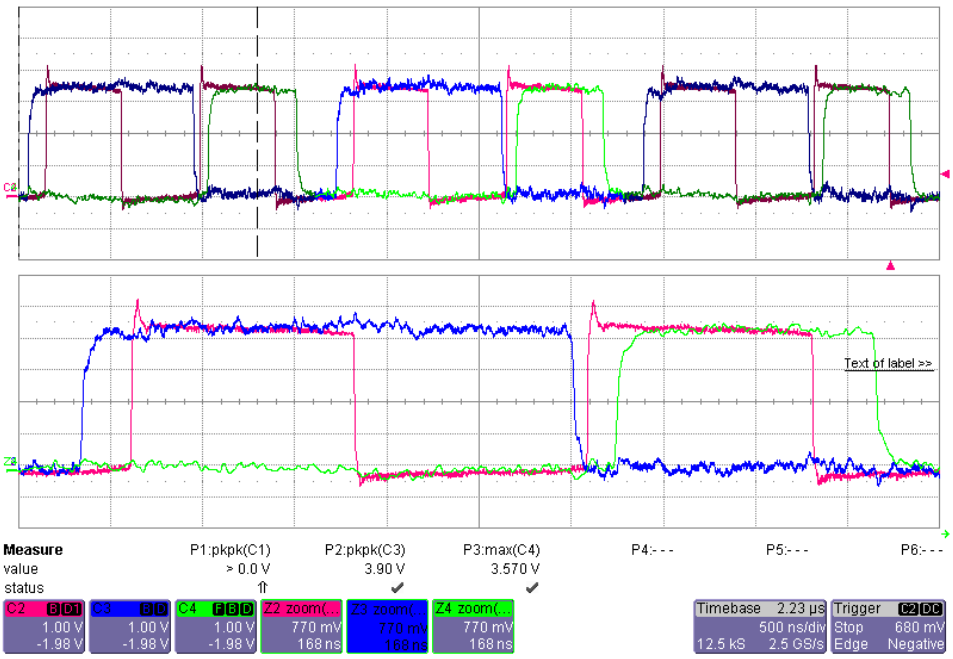


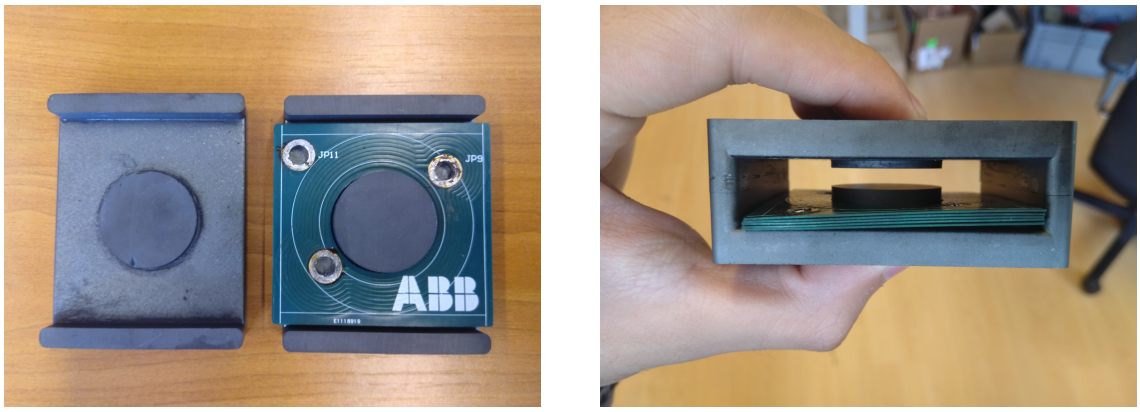
Figure 6.4: PWM signals with ZCD signals detected within one switching cycle

From figure 6.3 it could be seen that the PWM does not continue when ZCD is not detected within one switching cycle, and the controller would try to start switching in every $0.5s$. If ZCD is detected in one switching cycle, the switching continues as shown in figure 6.4.

With these protection algorithms, the converter would operate safer and more stable.

6.2. 20uH tests

The $20\mu H$ inductor design uses 5 PCB winding sheets in parallel as windings. with 8.5 number of turns, and 3mm air gap in the center of the inductor, as shown in figure 6.5. The DC resistance of the windings is $33m\Omega$.



(a) Top view (b) Side view

Figure 6.5: 20uH inductor

The LUT for $20\mu H$, $2KW$ is calculated and stored in the BRAM of the controller board. Table 6.1 shows the timing signals for each of the testing points.

input voltage V	T_{on} (ns)	T_{rpeak} (ns)	T_{off} (ns)	T_R (ns)	$T_{rvalley}$ (ns)	frequency (KHz)
100	1512	88	504	0	384	402.6
200	1512	64	1552	88	304	284.0
300	1512	56	4552	440	216	147.5

Table 6.1: $20\mu H$ LUT timing signals

$200V$ input to $400V$ output

This test demonstrate the scenario where the $v_{AC} = 200V$. Figure 6.6 shows the waveform for a whole switching cycle. The efficiency is 96.2% while is switching frequency is $288.0KHz$. Table 6.2 records the switching frequency, power level and efficiency for $20\mu H$ testing. The efficiency is calculated according to the power read from the input power supply and output electronic load, and subtracts the losses on the input and output fuses based on table A.1, and the loss from the $200K\Omega$ output resistor, but the losses from ancillary resistors are included.

input votlage (V)	input power (W)	efficiency $(\%)$	switching frequency (KHz)
300	/	/	/
200	1556	96.33	288.0
100	315	93.28	368.7

Table 6.2: Test results $@v_{AC} = 300V,\ 200V,\ 100V, 20\mu H$ LUT

From figure 6.6 it could be seen that the current rises from $0A$ to $18.5A$ after $T_{on} = 1512ns$. According to the equation 3.1, the actual inductance value could be calculated as below. This indicates

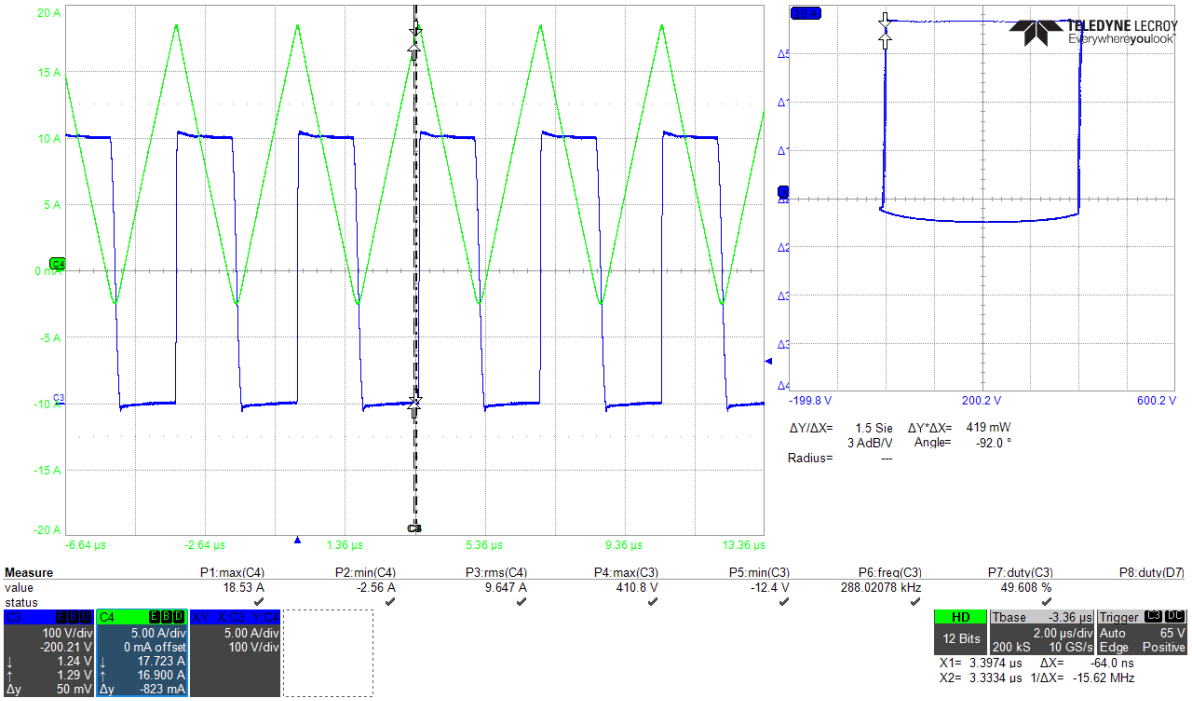


Figure 6.6: 200V input voltage, overall waveform

that the measurement of the LCR meter has error.

$$L = V\frac{dt}{di} = 16.35\mu H \tag{6.1}$$

Figure 6.7 and 6.8 shows respectively the detail of the peak and valley transient period for the case $v_{AC} = 200V$. From figure 6.7 it could be seen that within $T_{rpeak} = 64ns$, V_{HB} rises from 0V to 400V and been clamped at 400V until T_{rpeak} ends and the rectifier switch turns on with ZVS. In figure 6.8, within $T_{rvalley} = 304ns$, V_{HB} drops from 400V to zero, and been clamped by the body diode of the main switch for around $40ns$ before the main switch been turned on with ZVS, and there remains $22ns$ as ZVS margin before i_L rises up to zero.

$100V$ input to $400V$ output

This scenario is to demonstrate the case of the converter operating the low v_{AC} and low power case.

Figure 6.9 shows the waveform of a whole switching cycle. The switching frequency is around $368.7KHz$, and the efficiency is 93.0%. In figure 6.9, it could be seen that the current rises from $0A$ to $9.4A$ during $T_{on} = 1512ns$. By applying equation 3.1 and using the measurement data from figure 6.9, the actual inductance value could be calculated to be $16.09\mu H$, which aligns with the calculation in test where $V_{AC} = 200V$.

figure 6.10 and 6.11 show the peak and valley resonant transient of this case respectively. It can been seen that ZVS is fulfilled for both GaN transistors, according to the V_{HB} waveform. And in figure 6.11, V_{HB} drops to zero and been clamped by the body diode of the main switch for around $143ns$, and there remains more than $200ns$ ZVS margin time till the current reverse back to zero. This long margin time is brought by the natural valley switching and the way how $T_{rvalley}$ in low v_{AC} is calculated. As been explained in chapter 3, when v_{AC} is less than $\frac{1}{2}V_{DC}$, the converter could achieve ZVS by natural valley switching without addtional T_R. Moreover, $T_{rvalley}$ is calculated as half of one resonant cycle, and this gives abundant ZVS margin.

Figure 6.12 shows the thermal image of the board $@v_{AC} = 100V,\ 20\mu H,\ 368KHz,\ 4.8A(rms)$. It could be seen that the hottest spot is the winding of the inductor, being $58.1°C$, while the core is only $30.8°C$. The power module's temperature is around 32 degree on the surface. The ZCD sense resistors (1X50mOhm) is $42.1°C$. The 220K resistor near the power module is also a hot spot, with the

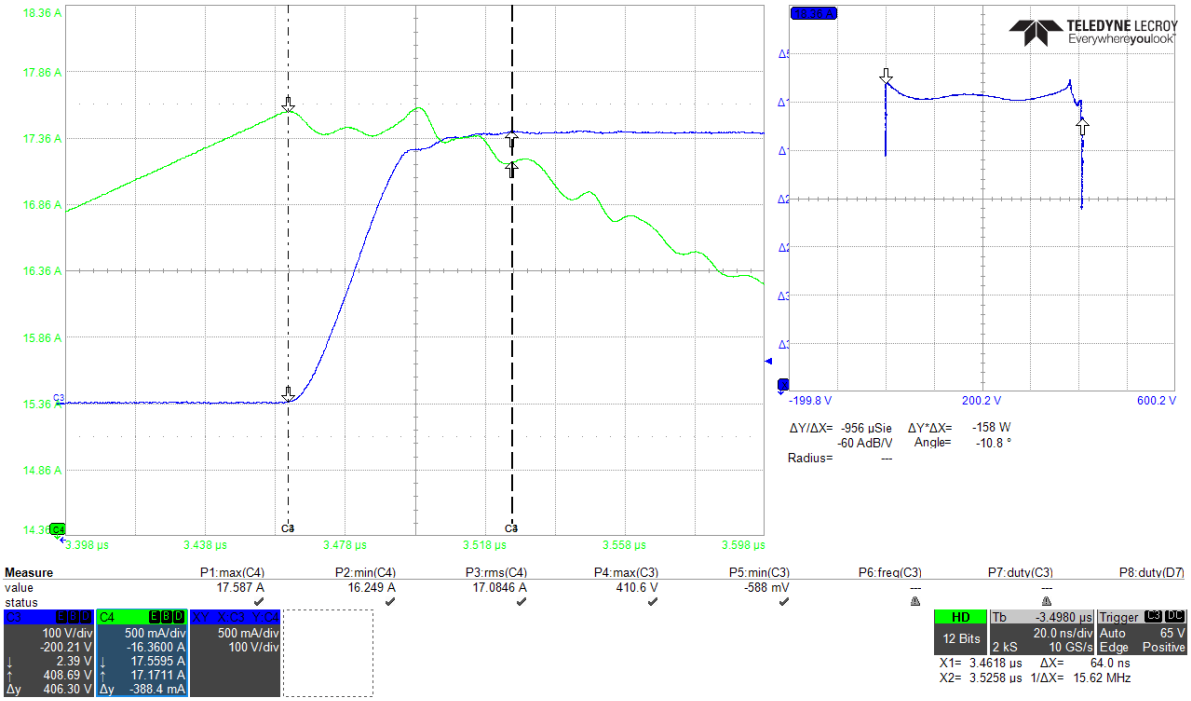


Figure 6.7: 200V input voltage, peak resonant transient zoom-in

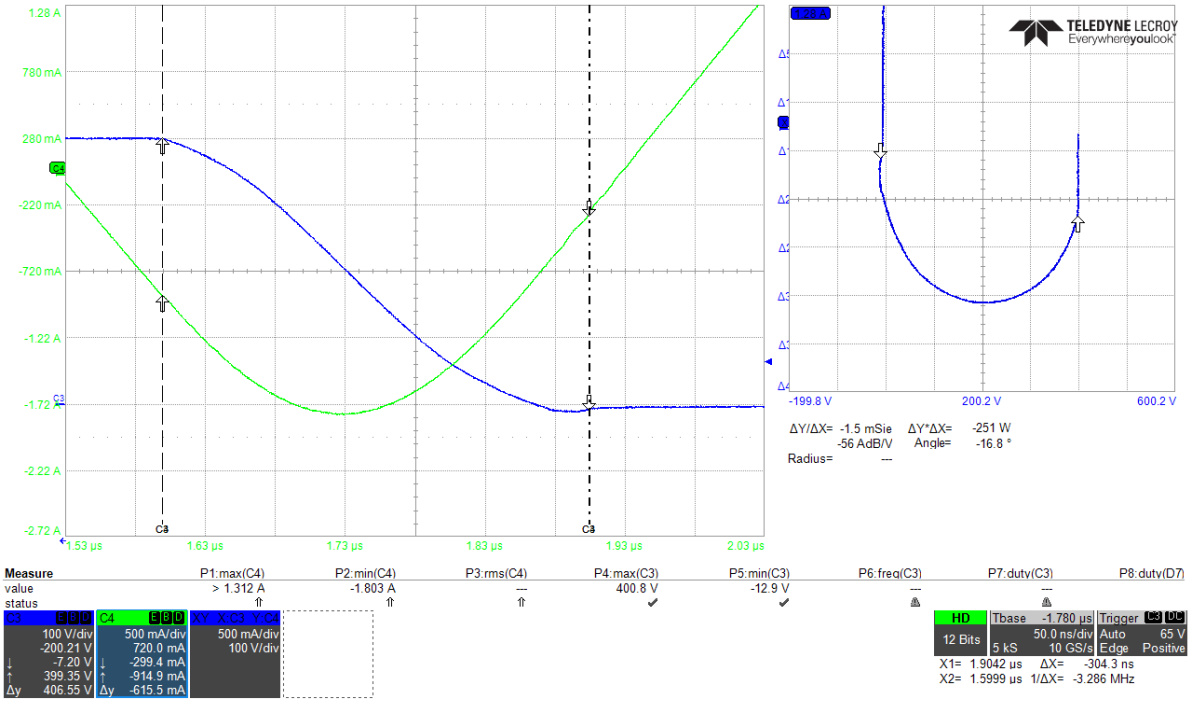


Figure 6.8: 200V input voltage, valley transient zoom-in

temperature of $54.0°C$, and together with losses on the input and output fuses (not shown in figure) contribute to the total losses.

The temperature of the winding being the hottest indicates the winding loss takes up a large part of the total losses. According to the DC resistance and the rms value of the current that passes through, the DC loss on the winding could be calculated as:

$$P_{DC(winding)} = R_{DC(winding)} \times I^2_{L(rms)} = 0.033 \times 4.8^2 = 0.76W. \tag{6.2}$$

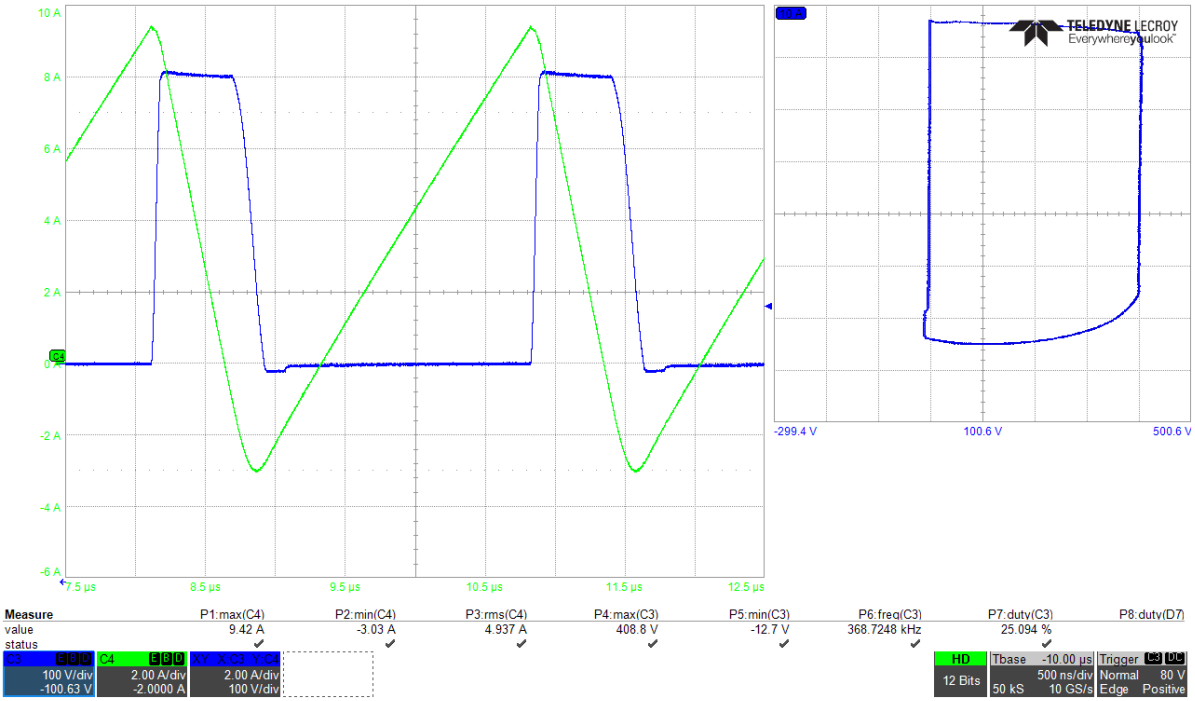


Figure 6.9: 100V input voltage, overall waveform

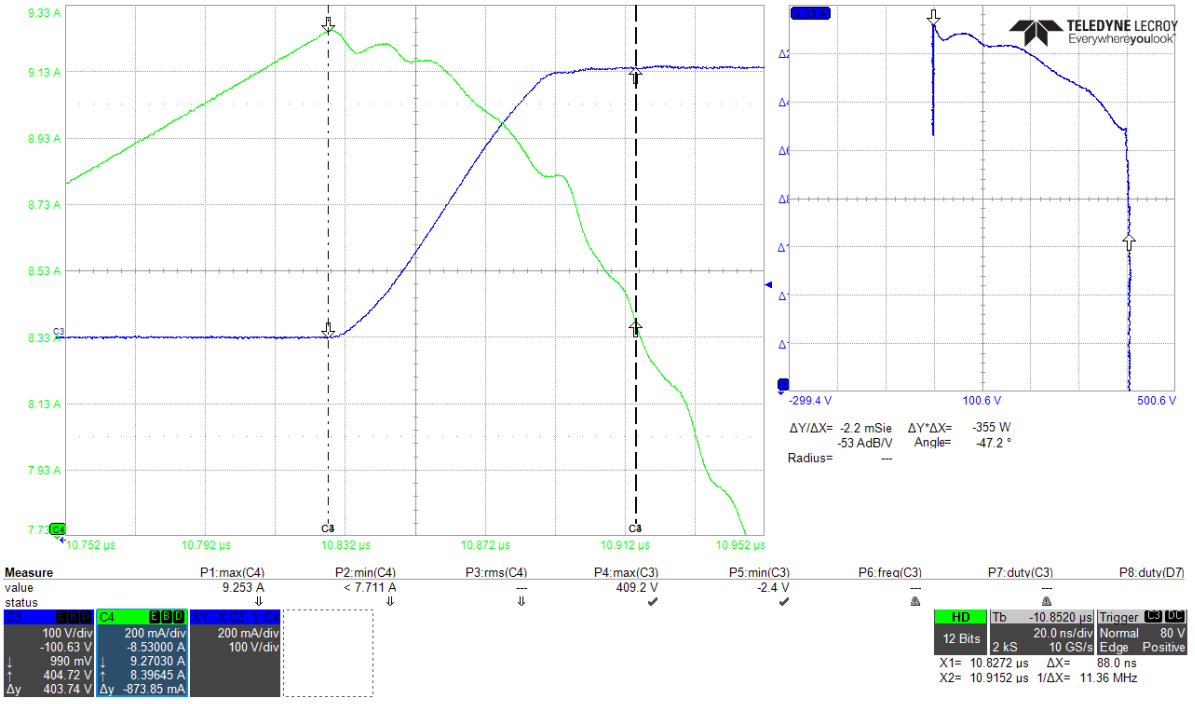


Figure 6.10: 100V input voltage, peak resonant transient zoom-in

There reason why the winding is suffering from high loss dissipation is proximity effect. Proximity effect happens when conductors are carrying high frequency alternating current. The alternating current in a conductor will generate changing magnetic field, which will interface with the conductors nearby, causing eddy current on them and affecting the current distribution inside the conductors shown as figure 6.13a, resulting to larger AC winding losses [53]. The changing magnetic field could also come from the core. In this inductor design, the proximity effect issue is not taken into consideration, and

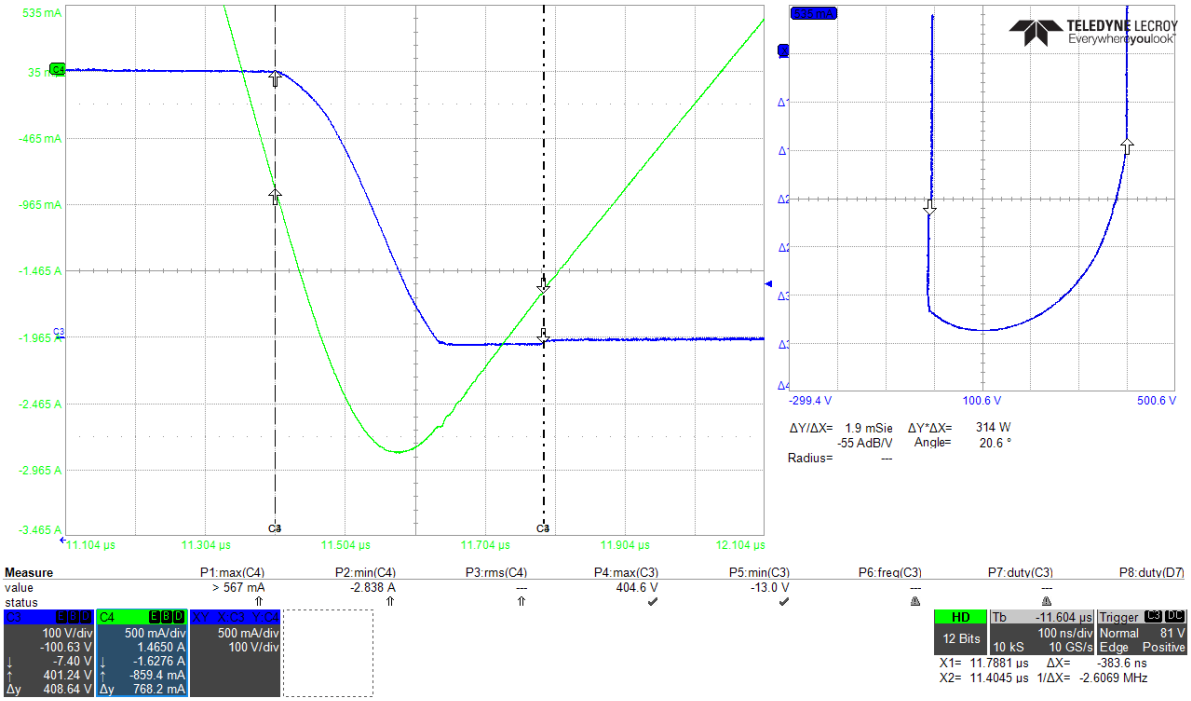


Figure 6.11: 100V input voltage, valley transient zoom-in

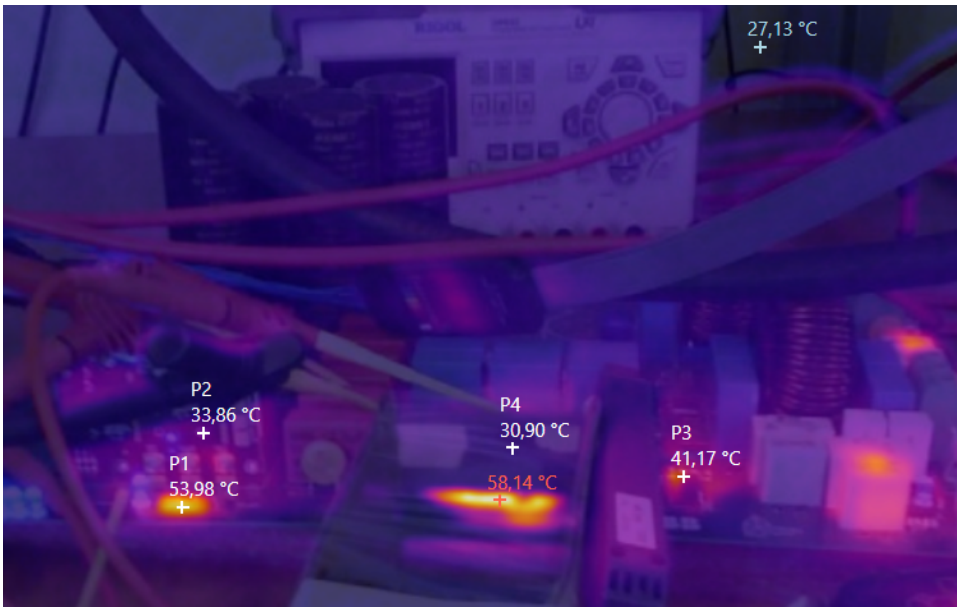
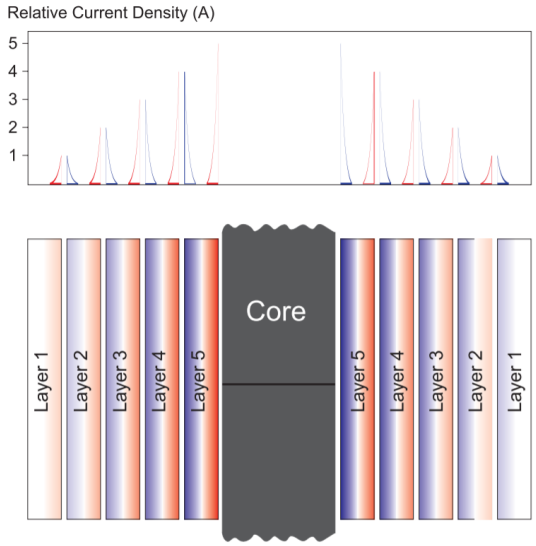


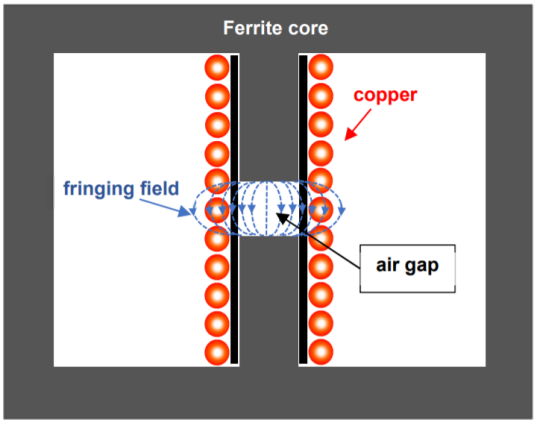
Figure 6.12: Thermal image overall, 20uH, @$v_{AC} = 100V$

the conductors are extremely close to each other, with $0.25mm$ distance between each turn, for the purpose of constraining the winding to be within the core area, so that the leakage could be minimized. The $3mm$ air gap in the center of the inductor, also brings fringing effect that contributes to the proximity effect due to the magnetic field that fringes out from the air gap. Figure 6.13b illustrates the interface of the conductor by the fringing magnetic field from the gap.

In order to reduce the proximity effect as well as the fringing effect, the number of turns could be reduced, the distance between the conductors could be increased, and the the air gap could be smaller or using laminated air gap.



(a) Current distribution due to proximity effect [53]

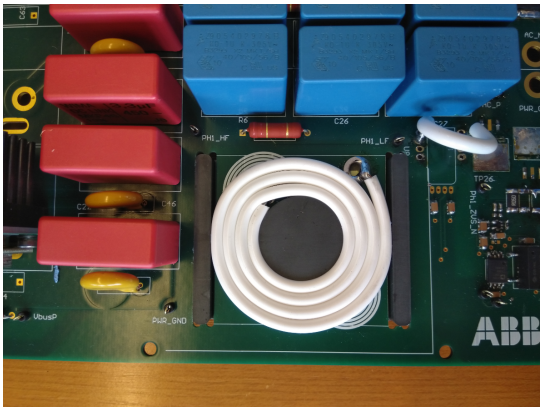


(b) fringing effect[54]

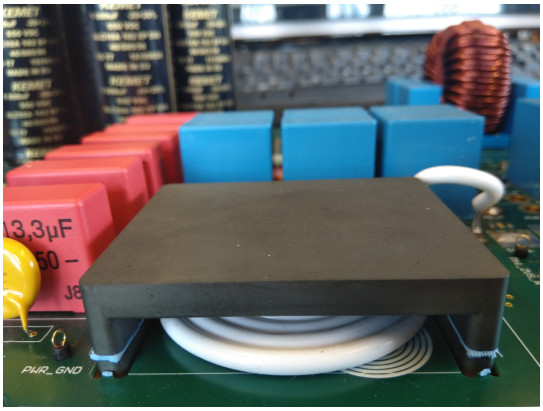
Figure 6.13: Causing factors of the AC Winding losses on the $20\mu H$ inductor

6.3. 9uH tests

For the purpose of investigating the high frequency operation ability of the converter, and also of improving the proximity issue of the inductor, a $9\mu H$ inductor is built using copper wire, with 3.5 number of turns, and 2mm air gap distributed on three legs. Figure 6.14 shows the actual construction.



(a) Top view



(b) Side view

Figure 6.14: $9\mu H$ inductor

The LUT for $9\mu H$ inductance is applied. Table 6.3 records the timing signals. Figure 6.15-6.17 show the switching waveforms $@v_{AC} = 300,\ 200,\ 100V$. It could be observed that the in all set-point tests, ZVS turn-on is achieved for both GaN switches.

input voltage V	$T_{on}\ (ns)$	$T_{rpeak}\ (ns)$	$T_{off}\ (ns)$	$T_R\ (ns)$	$T_{rvalley}\ (ns)$	frequency (KHz)
100	680	88	216	0	256	808.1
200	680	64	696	88	184	582.1
300	680	56	2056	344	136	305.2

Table 6.3: $9\mu H$ LUT timing signals

From figure 6.15 6.16 6.17 the actual inductance value could be calculated to be around $6.8\mu H$.

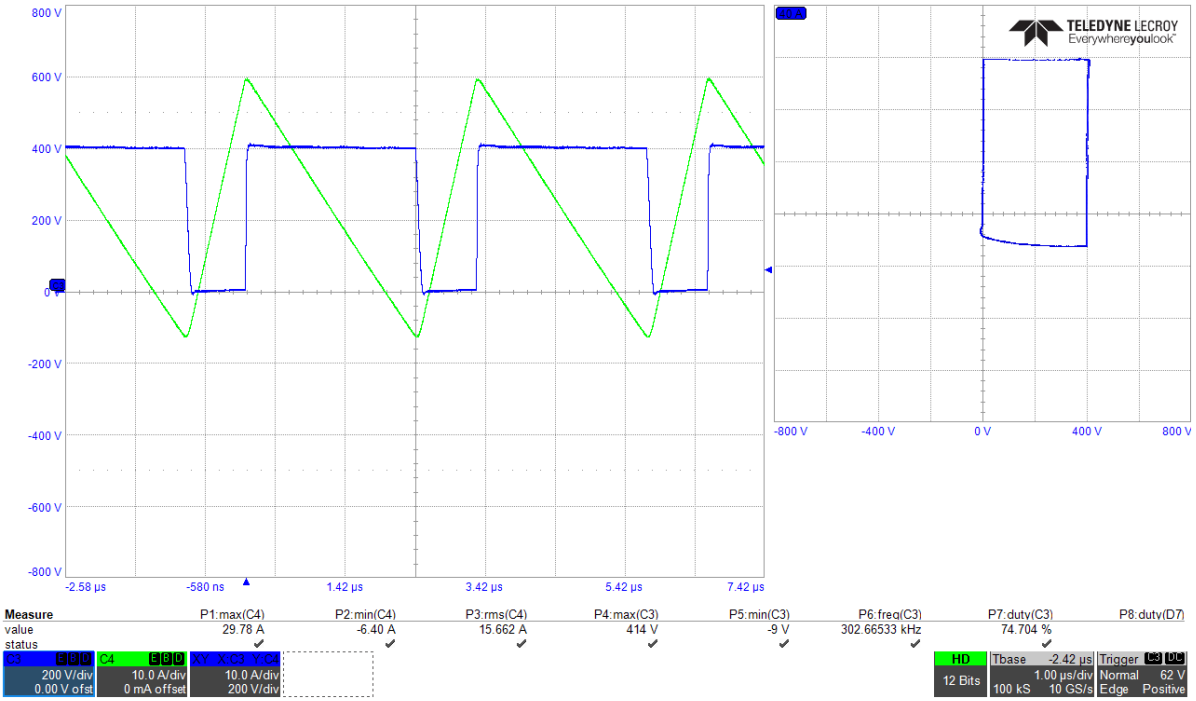


Figure 6.15: 300V input voltage, overall waveform, $9\mu H$ LUT

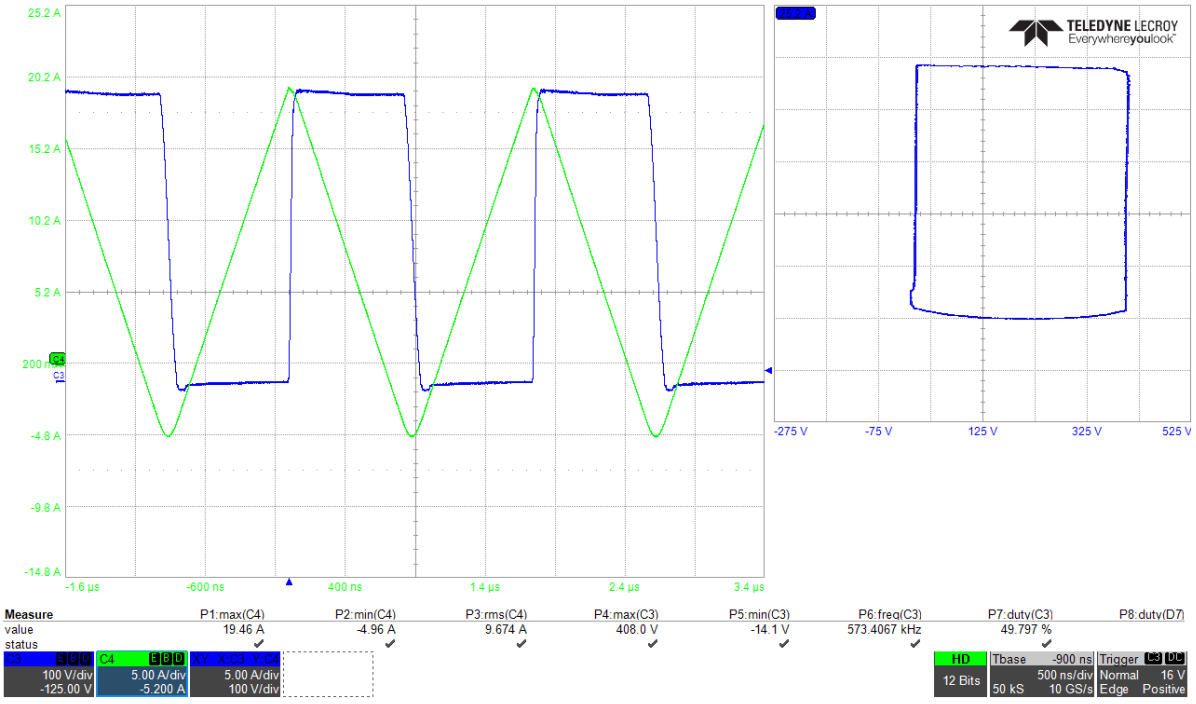


Figure 6.16: 200V input voltage, overall waveform, $9\mu H$ LUT

Figure 6.18 shows the overall thermal image of the board @$v_{AC} = 100V$, $9\mu H$, $714.3KHz$, $4.8A(rms)$. The power module temperature is $35.3°$, the core temperaure is $34.3°$, and the winding temperature is even lower, being $31.7°$. Comparing to the $20\mu H$ test shown in figure 6.12, the winding temperature is $24.2°$ cooler, with almost double switching frequency and similar rms value. This indicates that by reducing the number of layers, increasing the distance between conductors, and reduce the air gap, the proximity issue could be improved, and the AC losses on the winding could be reduced.

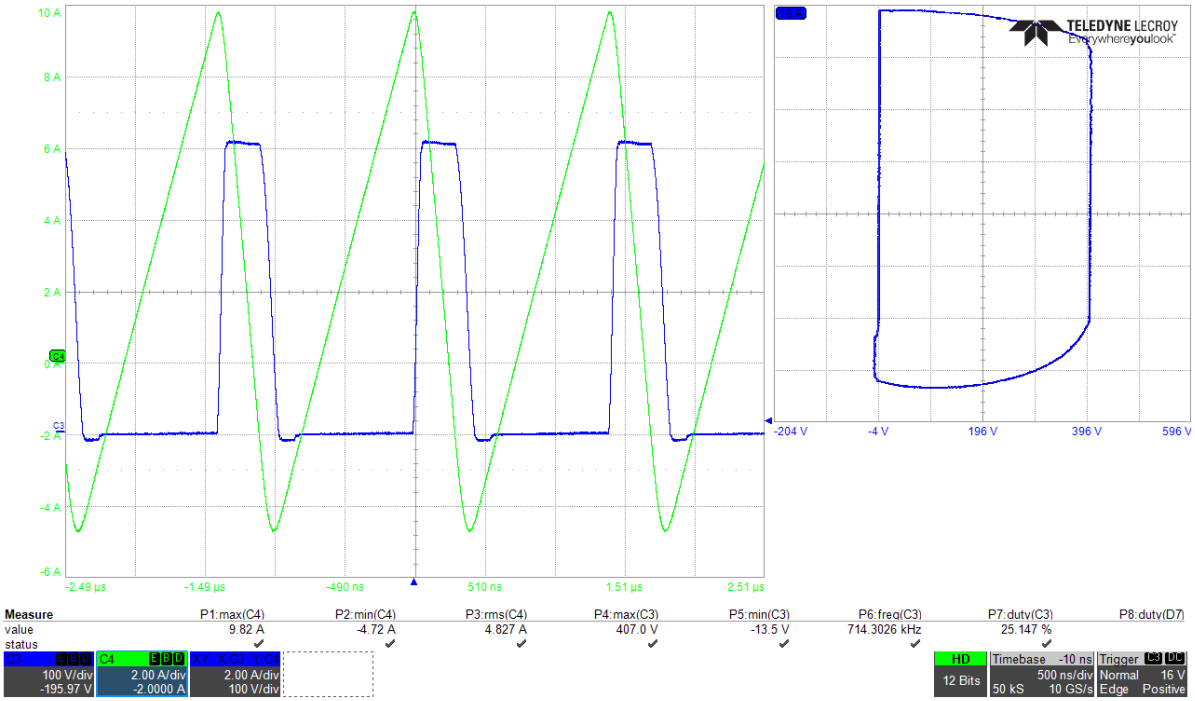


Figure 6.17: 100V input voltage, overall waveform, $9\mu H$ LUT

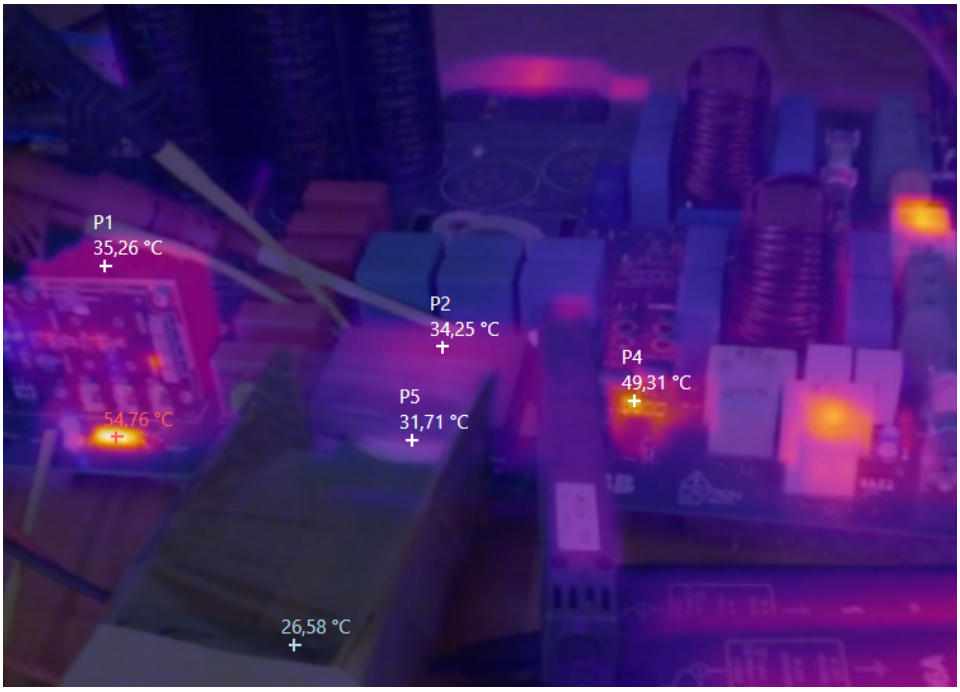


Figure 6.18: Thermal image overall, 9uH, $@v_{AC} = 100V$

Table 6.4 records the switching frequency and efficiency for these tests.

6.4. 9uH tests, with actual 6.8uH LUT

As explained before, the inductance measurement from the LCR meter is actually higher than actual. For a more accurate evaluation, a $6.8\mu H$ LUT is made according to the inductance calculation and applied. Table 6.5 shows the timing signals for each of the testing points.

input votlage (V)	input power (W)	efficiency (%)	switching frequency (KHz)
300	3453	98.83	303.4
200	1418	97.40	573.4
100	245	88.37	714.4

Table 6.4: Test results $@v_{AC} = 300V,\ 200V,\ 100V, 9\mu H$ LUT

input voltage V	$T_{on}\ (ns)$	$T_{rpeak}\ (ns)$	$T_{off}\ (ns)$	$T_R\ (ns)$	$T_{rvalley}\ (ns)$	frequency (KHz)
100	512	88	160	0	216	1020
200	512	64	528	88	152	743.6
300	512	56	1560	320	120	389.3

Table 6.5: $6.8\mu H$ LUT timing signals

$300V$ input to $400V$ output

This testing point is to demonstrate the high AC input voltage, high power case. Figure 6.19 shows the waveform of a whole switching cycle, in which the green line is the current through the inductor i_L, and the blue line is the half-bridge mid-point voltage V_{HB}. In the right-hand side of the figure is the state plane, with X-axis being V_{HB}, and Y-axis being i_L.

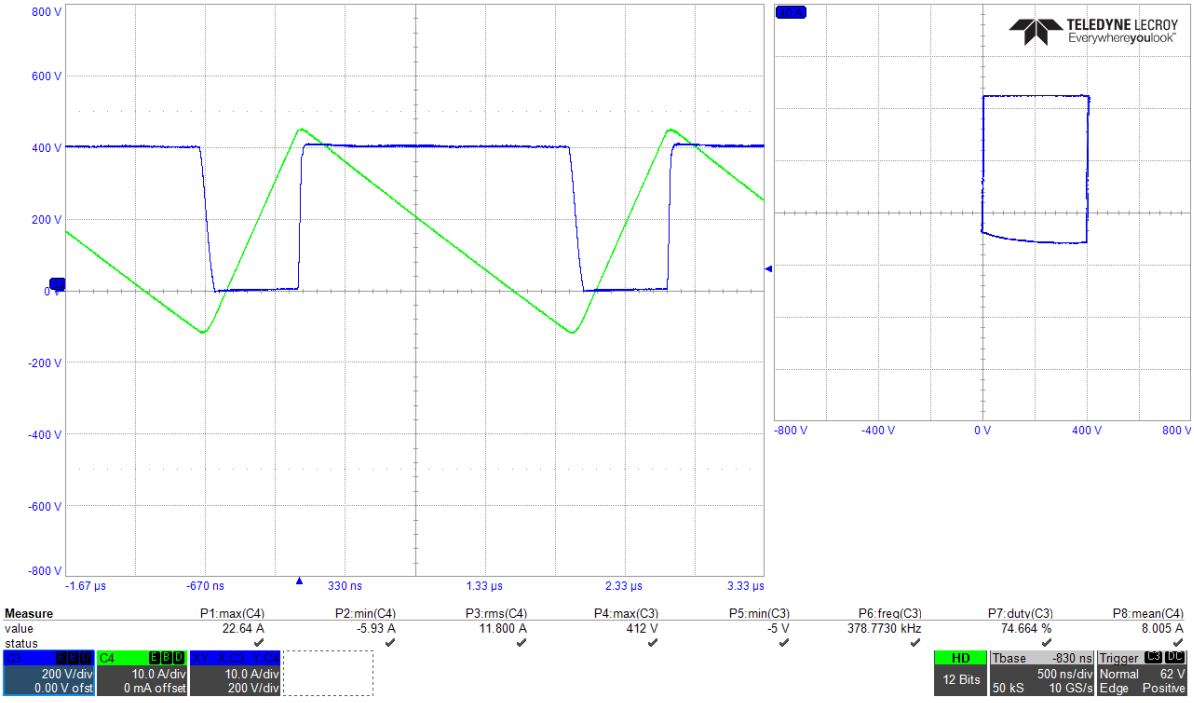


Figure 6.19: 300V input voltage, overall waveform

Figure 6.20 and 6.21 shows respectively the detail of the peak and valley transient period.

From figure 6.20, it can be seen that, within $T_{rpeak} = 56ns$, V_{HB} rises from 0V to 400V and been clamped by the body diode of the rectifier. Once T_{rpeak} is over, the rectifier switch could have ZVS turn-on. In figure 6.21, it can be seen that V_{HB} starts to drop from $400V$, till it becomes zero and been clamped by the body diode of the main switch within $T_{rvalley} = 120ns$. Once after $T_{rvalley}$ is finished, the main switch is turned on with ZVS, and there is around $30ns$ ZVS margin till the current reverse back to zero.

table 6.6 records the switching frequency, power level and efficiency for this case. The efficiency is calculated according to the power read from the input power supply and output electronic load, and subtracts the losses on the input and output fuses based on table A.1, and the loss from the $200K\Omega$ output resistor, but the losses from ancillary resistors are included. The efficiency $@v_{AC} = 300V$ is

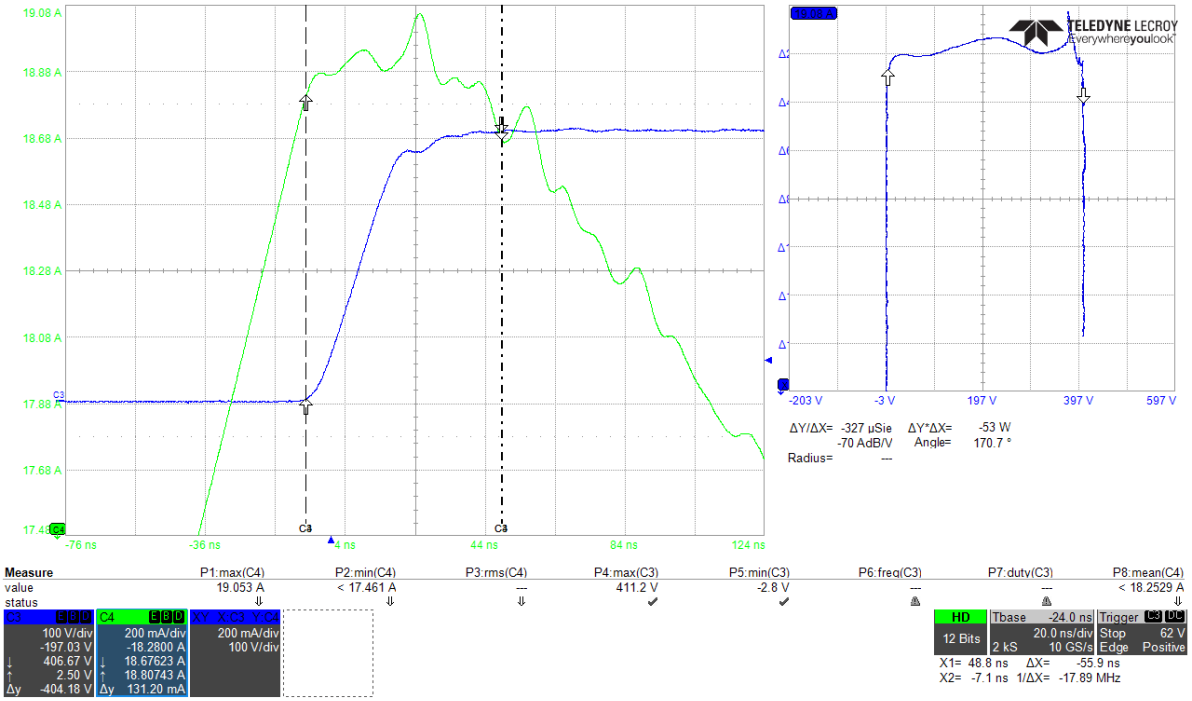


Figure 6.20: 300V input voltage, peak resonant transient zoom-in

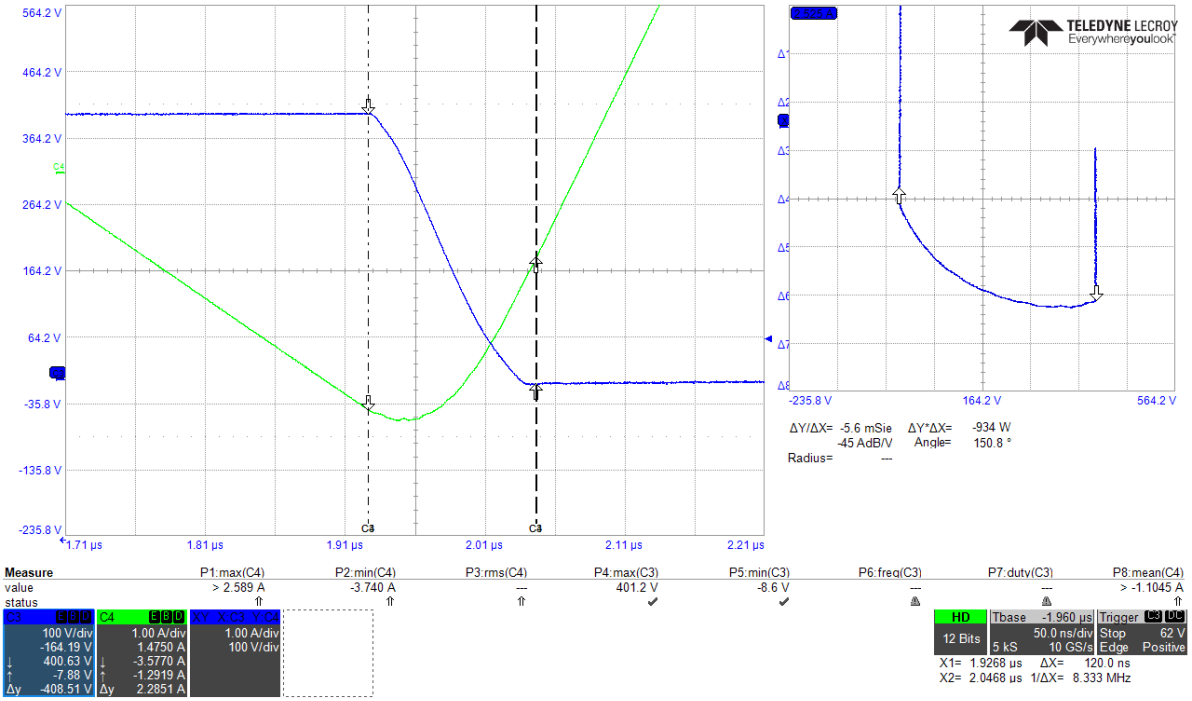


Figure 6.21: 300V input voltage, valley transient zoom-in

98.8%, including the loss on the fuses and some ancillary resistors, while the switching frequency is $378.8KHz$.

Figure 6.22 shows the thermal image of the board $@v_{AC} = 300V$. It could be seen that the power module's temperature is around 41 degree on the heatsink. The ZCD sense resistors (3X50mohm in parallel) is $58.2°C$, being the hottest spot. The input and output fuses, and the 220K resistor near the power module are also hot spots, with the temperature of $53.7°C$, $41.7°C$ and $56.9°C$, and they all

input votlage (V)	input power (W)	efficiency (%)	switching frequency (KHz)
300	2428	98.79	378.8
200	921	97.30	683.0
94	93	/	822.4

Table 6.6: Test results $@v_{AC} = 300V,\ 200V,\ 100V$, $6.8\mu H$ LUT

contribute to the total loss.

Figure 6.22: Thermal image overall, $@v_{AC} = 300V$

Figure 6.23 shows the thermal image specifically on the inductor. It could be seen that the temperature of the core is $33.7°C$, and the inner inner part of the winding get hotter ($42.6°C$) than the outer part. This could be caused by the fringing effect brought by the 1mm airgap in the center of the core.

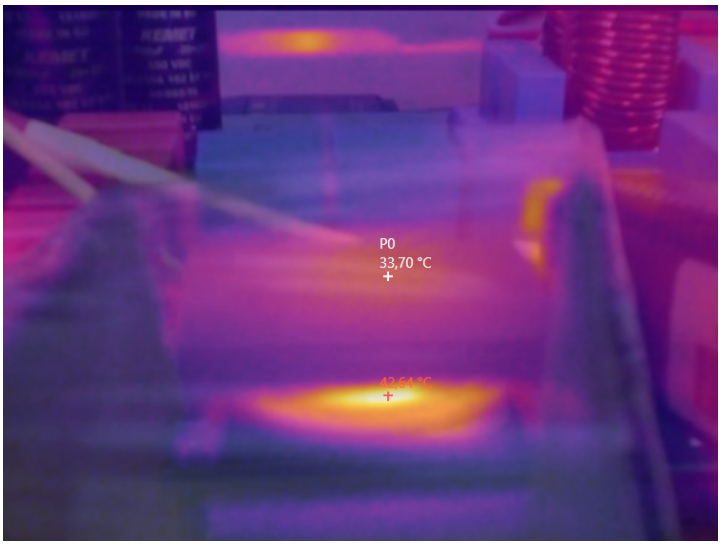


Figure 6.23: Thermal image for the inductor, $@v_{AC} = 300V$

$200V$ input to $400V$ output

This test demonstrate the scenario where the $v_{AC} = 200V$. Figure 6.24 shows the waveform for a whole switching cycle. The efficiency is 97.2% while is switching frequency is $683.0KHz$.

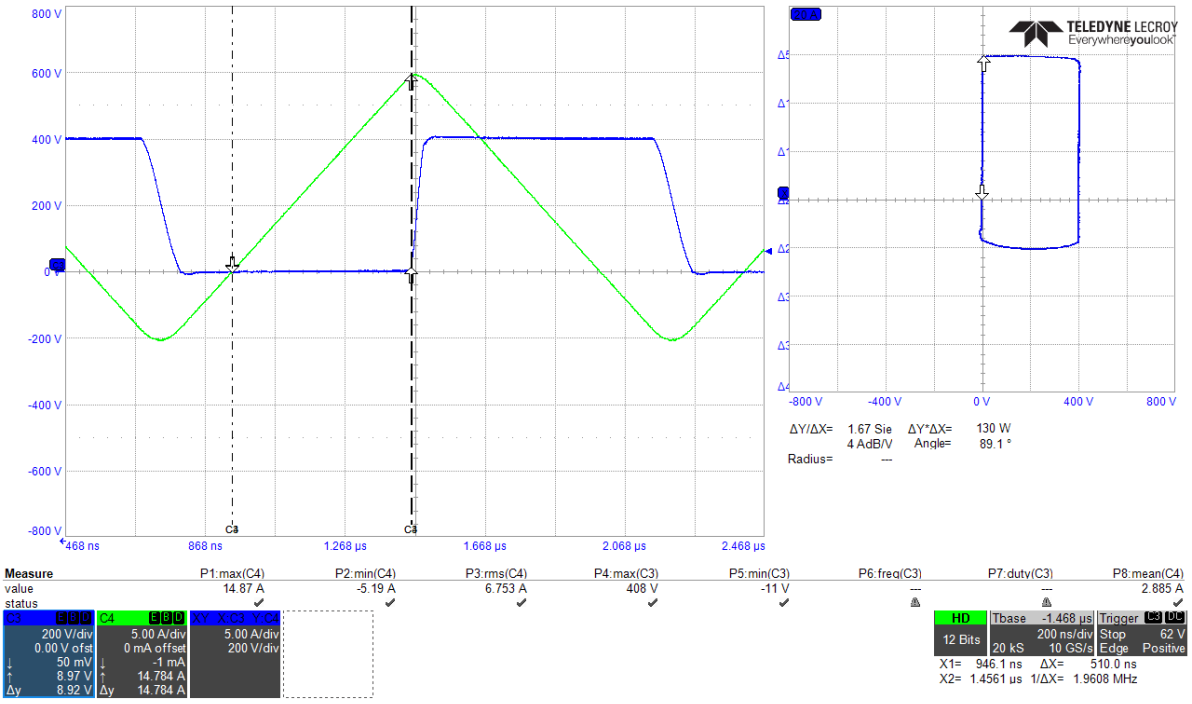


Figure 6.24: 200V input voltage, overall waveform

Figure 6.25 and 6.26 shows respectively the detail of the peak and valley transient period for the case $v_{AC} = 200V$.

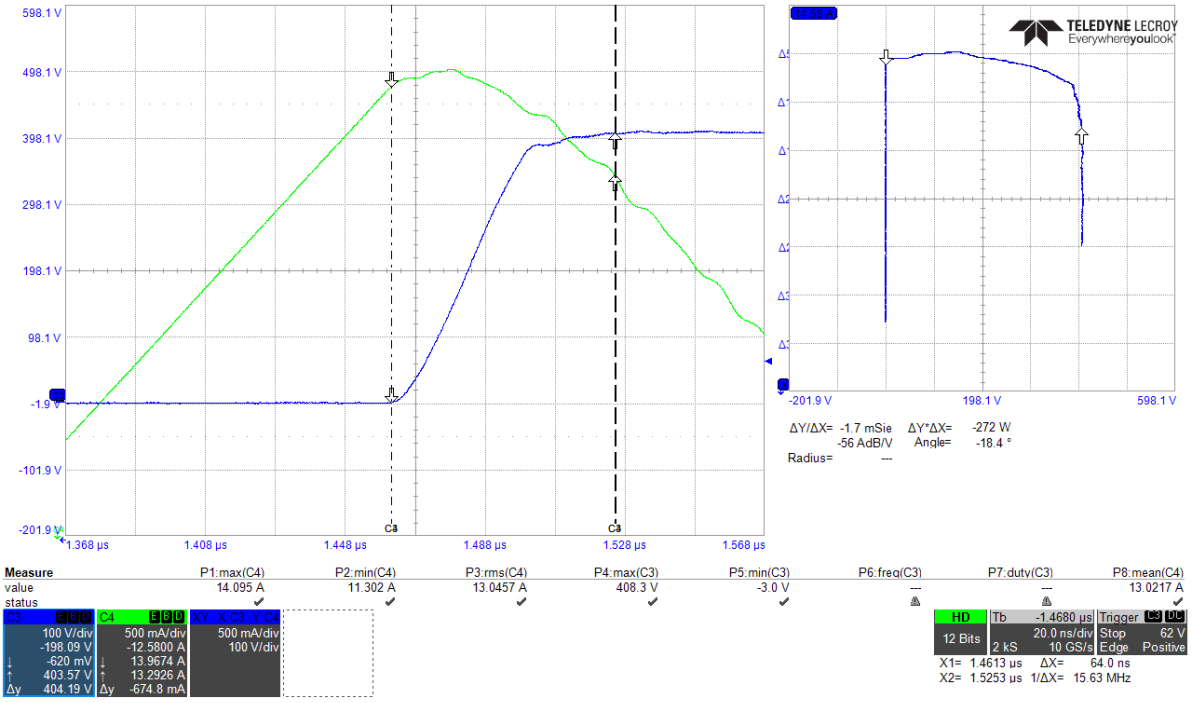


Figure 6.25: 200V input voltage, peak resonant transient zoom-in

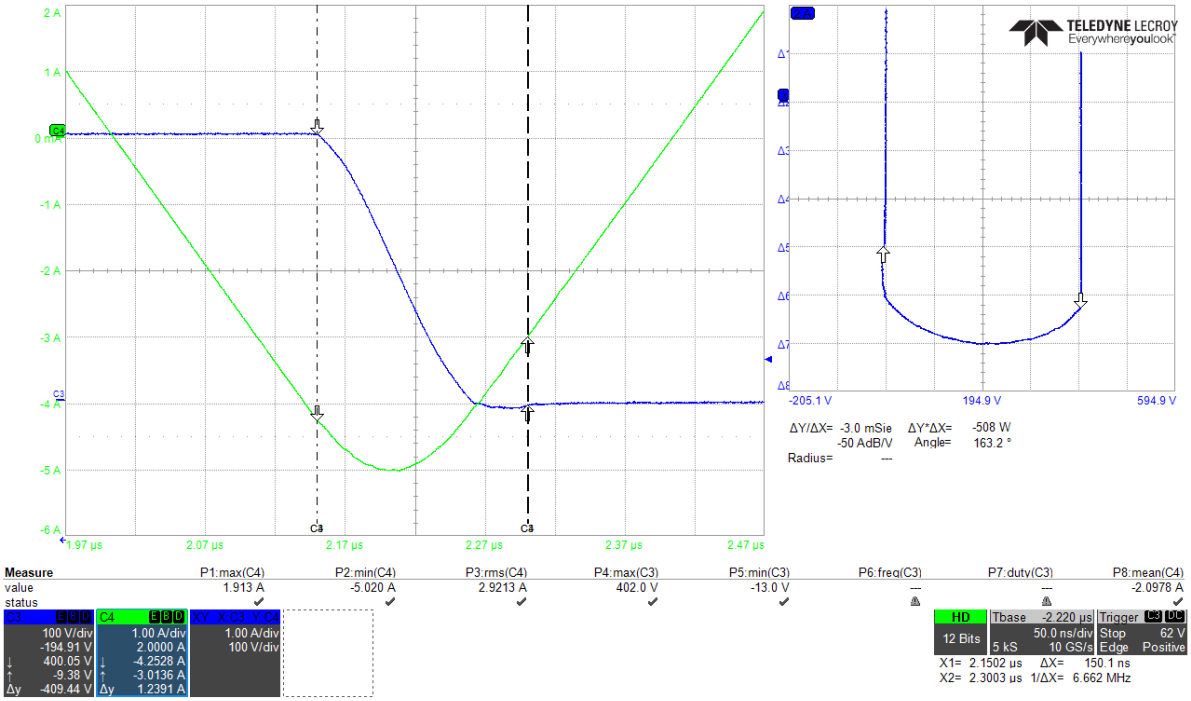


Figure 6.26: 200V input voltage, valley transient zoom-in

From figure 6.25 it could be seen that within $T_{rpeak} = 64ns$, V_{HB} rises from 0V to 400V and been clamped at 400V until T_{rpeak} ends and the rectifier switch turns on with ZVS. In figure 6.26, within $T_{rvalley} = 152ns$, V_{HB} drops from 400V to zero, and been clamped by the body diode of the main switch for around $38ns$, and there remains $100ns$ as ZVS margin before i_L rises up to zero.

Figure 6.27 show the thermal image of the board. It can be seen that the temperature on heatsink of the power module is $37.98°C$, which is around $3°C$ cooler than the case $@v_{AC} = 300V$. Figure 6.28 shows the temperature of the inductor specifically. The temperature of the core is $34.6°C$, while the inner part of the core is $38.7°C$. Comparing with the previous scenario, the input power $921W$ is much lower than $2428W$ $@v_{AC} = 300V$, but the frequency $683KHz$ is much higher than $378.8KHz$ $@v_{AC} = 300V$. The fact that the ferrite core has even higher temperature tells that the core losses $@200V$ is higher than $@300V$. This contributes to the efficiency drop to 97.2% as record in table 6.6.

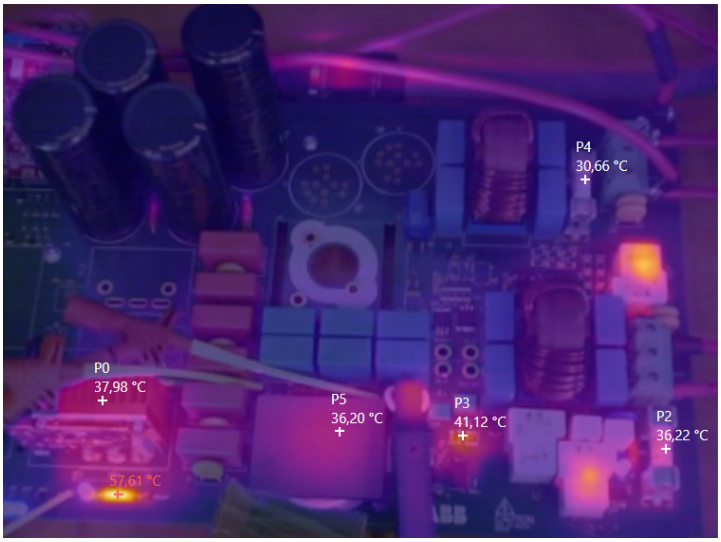


Figure 6.27: Thermal image overall, $@v_{AC} = 200V$

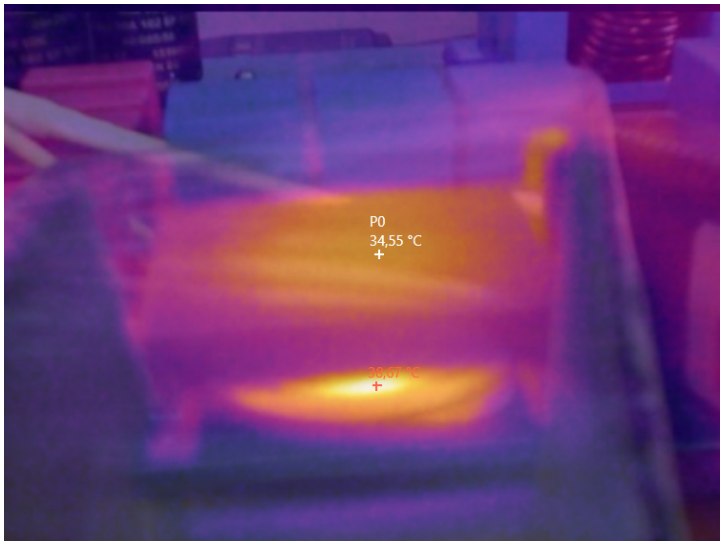


Figure 6.28: Thermal image for the inductor, @$v_{AC} = 200V$

$100V$ input to $400V$ output

This scenario is to demonstrate the case of the converter operating the low v_{AC} and low power case. However in this scenario, since the power and thus the current is low, the ZCD circuitry would have increased difficulty detecting the zero current crossing, since the voltage drop on the sense resistor would be much smaller. During this test, the output is maintained by an external power supply in order to have a stable operation, and the input votlage is $94V$ instead of $100V$.

Figure 6.29 shows the waveform of a whole switching cycle. The switching frequency is around $822.4KHz$.

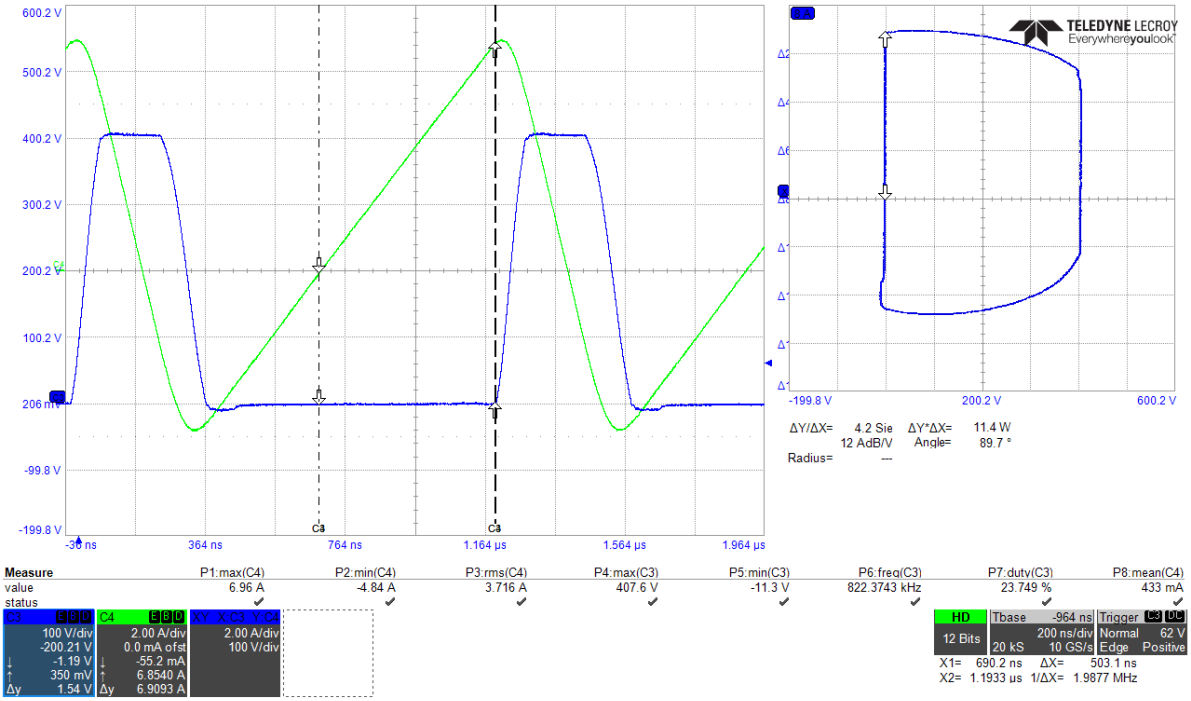


Figure 6.29: 94V input voltage, overall waveform

figure 6.30 and 6.31 show the peak and valley resonant transient of this case respectively. It can been seen that ZVS is fulfilled for both GaN transistors, according to the V_{HB} waveform.

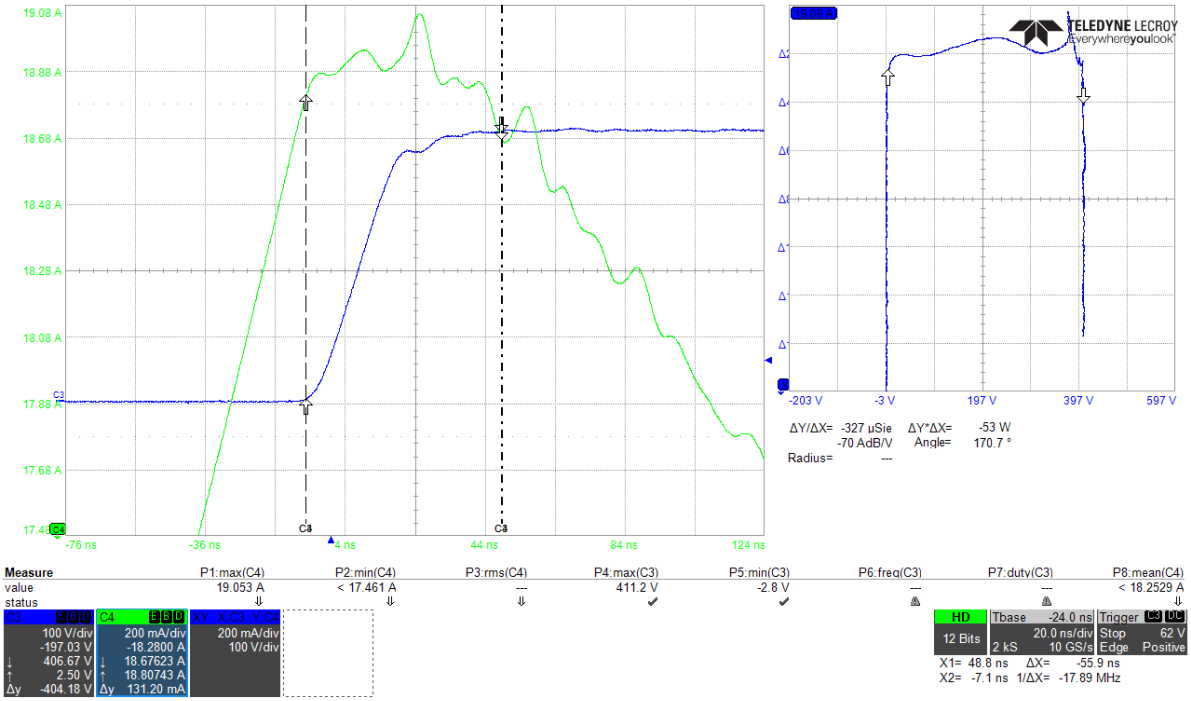


Figure 6.30: 94V input voltage, peak resonant transient zoom-in

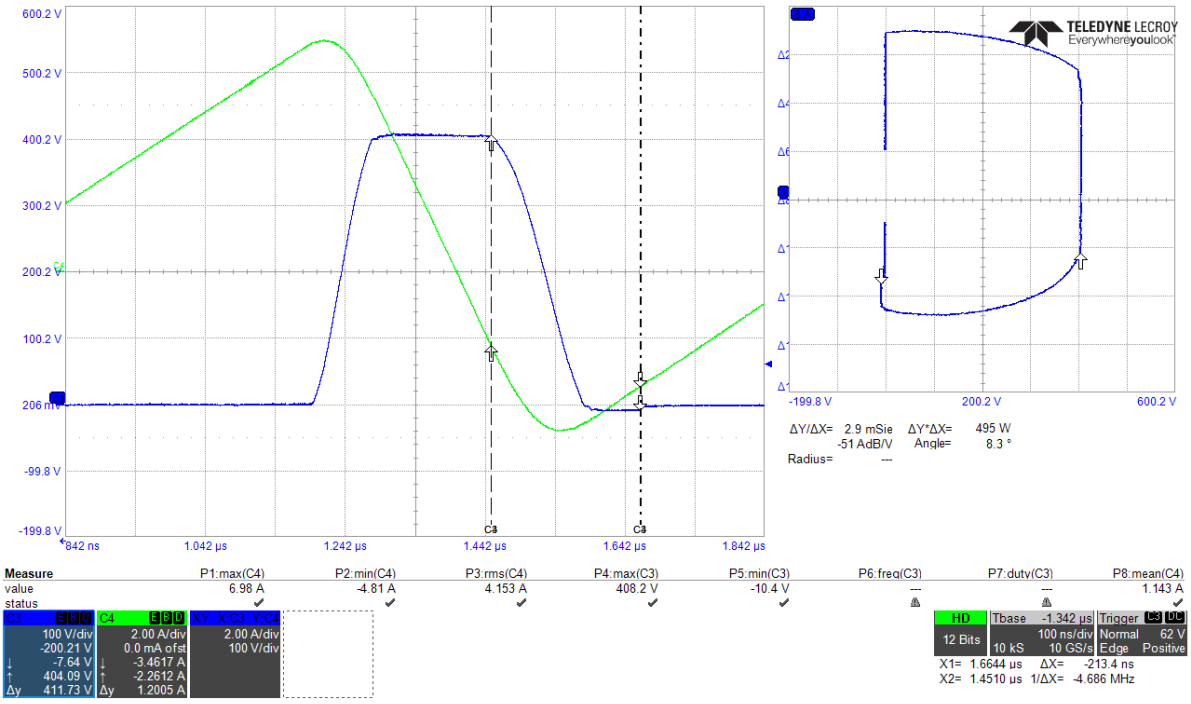


Figure 6.31: 94V input voltage, valley transient zoom-in

And from figure 6.31, V_{HB} drops to zero and been clamped by the body diode of the main switch for around $77ns$, and there remains more than $200ns$ ZVS margin time till the current reverse back to zero. This long margin time is brought by the natural valley switching and the way how $T_{rvalley}$ in low v_{AC} is calculated. As been explained in chapter 3, when v_{AC} is less than $\frac{1}{2}V_{DC}$, the converter could achieve ZVS by natural valley switching without addtional T_R. Moreover, $T_{rvalley}$ is calculated as half of one resonant cycle, and this gives abundant ZVS margin.

Based on the efficiency measurement on each testing points, an efficiency graph with different input voltage value for different LUTs and inductance could be made as figure 6.32, where the horizontal axis is the value of the input voltage v_{AC} in volts, and the vertical axis is the efficiency in percentage. It can be seen that the efficiency is the highest when v_{AC} is high, frequency is relatively low, and power is high. With smaller v_{AC}, the switching frequency increases, so does the ratio between the AC losses and the total losses. The AC losses include switching loss on the transistors, core loss and AC winding losses. As a result, the efficiency drops.

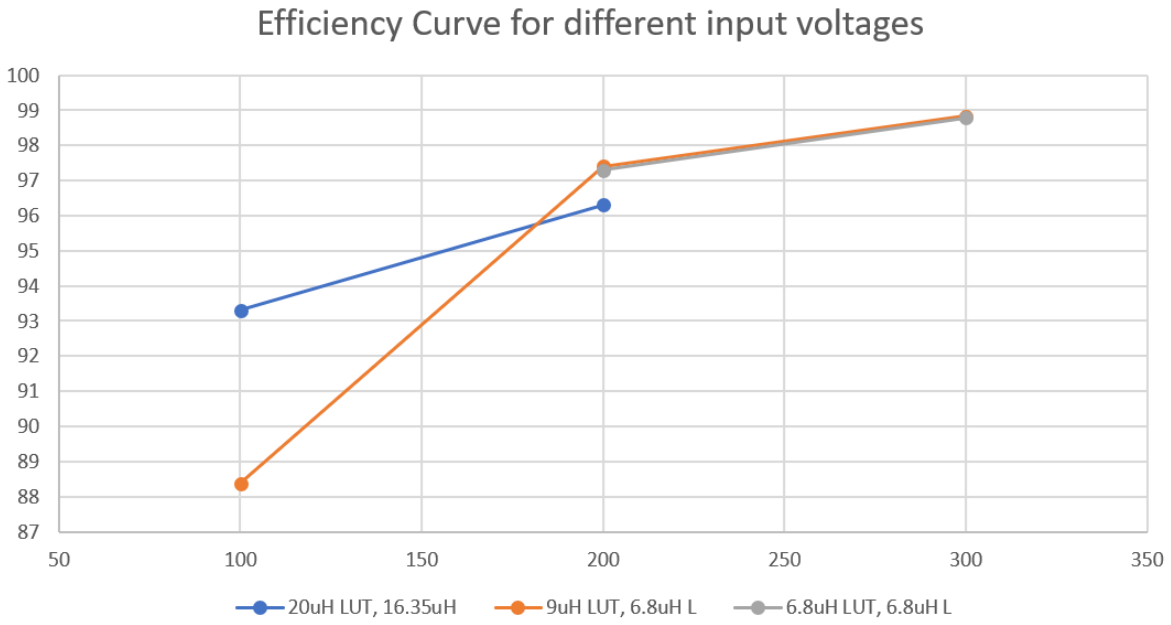


Figure 6.32: Efficiency curve with different input voltage value

The test points $@v_{AC} = 300V, 20\mu HLUT$ and $@v_{AC} = 100V, 6.8\mu HLUT$ are missing. The reason for the test point $@v_{AC} = 300V, 20\mu HLUT$ missing is that the single $50m\Omega$ current sense resistor got too hot (above $90°$) during the test, and test was stopped for preventing possible damage. The test could be done after adding more sense resistors in parallel so that the loss dissipated on them is lower. The reason for the test points $@v_{AC} = 100V, 6.8\mu HLUT$ missing is that, the converter is only able to maintain the steady-state operation with an external power supply to keep the output voltage to be $400V$ in this test, and the converter stopped working without the external power supply for the output.

7

Conclusion

A high efficiency, high switching frequency, single-phase, $2KW$ GaN-based totem-pole PFC converter for EV charging is designed and built. GaN HEMTs are used together with totem-pole topology and ZVS control method, in order to push the switching frequency to around $1MHz$, while still having good efficiency. Set-point testings at low, medium, high input voltage are done to verify the feasibility of the design. The test results demonstrate that:

1. **Good efficiency is achieved while operating at high frequency in the GaN-based ZVS totem-pole converter.**

   With the switching frequency no less than $378KHz$, the converter has efficiency up to 98.8% in set-point testings. This indicates that the design with GaN HEMTs exhibits superior performance in high-frequency applications, because of the low turn-off loss, low $R_{ds(on)}$, low parasitic capacitance, and zero reverse recovery loss. Moreover, the ZVS turn-on of the GaN HEMTs benefits the high-frequency operation by eliminating turn-on loss.

2. **The improved ZVS control strategy with non-ideal behaviour accommodation method could ensure the ZVS turn-on of the GaN transistors.**

   By considering the issues of non-ideal timing and inaccuracy of circuitry parameters, the safety and ZVS margin could be designed using state plane analysis and implemented in the control strategy to provide better ZVS performance. The experiment results show that with the improved ZVS control, ZVS turn-on of the two GaN HEMTs is achieved in all test scenarios.

3. **The potential of achieving high power density is shown.**

   The converter is able to operate at high switching frequency up to $822.4KHz\ @v_{AC} = 100V$, and $378.8KHz\ @v_{AC} = 300V$. As a result, the inductance is as small as $6.8\mu H$. The fact that the temperature of the core is below $50^{\circ}C$ during operation, and that there is unused winding area demonstrate the potential to construct a smaller inductor that could help increase the power density.

4. **The design of the magnetic components is crucial to the high-frequency application.**

   With the ability of high-frequency operation of the GaN transistor been demonstrated, the magnetic component becomes the key to the overall system performance. As shown from the experiment results, the inductor could be the primary source of losses. A trade-off exists between the AC core loss and the AC winding loss.

There are several parts of the design that could be improved:

1. **The loss calculation**. In the design process, the loss estimation mostly relies on simulation. Even though it indicates the losses in a specific simulation, but it is not as versatile and flexible as mathematical calculation, because it is limited by the simulation scenarios, and it is more time-consuming. Future work is to have detail mathematical calculation of the losses, including switching and conduction loss of the switch, core loss and winding loss of the inductor.

2. **Inductor design**. There are three parts that could be improved regarding the inductor design. Firstly, the size of the inductor could be reduced. In this specific design, the core shape is selected as $ER64$. The inductor finally made still have a large winding area left unused, and the core is well below $40°C$ during operation, thus it is possible to choose a smaller core shape and thus increase the overall power density. Secondly, the air gap could be reduced. In this specific design, in order to have a small operational B_{max}, thus smaller core loss, the air gap is designed to be quite large, with relatively more number of turns. However, the drawback is the fringing effect brought by the large air gap. The magnetic flux that bends out from the air gap would interface with the windings, inducing voltage on the conductor, generate eddy current, and eventually leading to higher AC loss of the winding. Thirdly, the proximity effect could be reduced by changing the winding structure. Finite element analysis could be performed to design an optimal winding structure. Last but not least, the wire of the inductor could be changed to have smaller DC and AC losses.

3. **The calculation of** $T_{rvalley}$. In the currently using timing calculation method, $T_{rvalley}$ is kept constant to be half resonant period when natural valley switching is sufficient for ZVS. This will lead to excessive body diode reverse conduction time, bringing more conduction losses. Thus $T_{rvalley}$ could be optimized to be more precise so that the reverse conduction time and thus the associated loss could be reduced.

There are some specific topics that are worth future investigation:

1. **The AC operation of the converter**. The voltage sensing and Analog-Digital-Conversion for the controller need to be added, and AC input test should be conducted.

2. **Interleaved totem-pole PFC**. By paralleling another inductor and fast-switching leg, an interleaved totem-pole PFC could be constructed. With a 180 degree phase shift, the interleaved topology could largely reduce the current ripple that flows through the inductor and reduce the current stress on components, leading to fewer inductor losses, smaller EMI filter, and smaller output capacitance theoretically.

3. **The variable on-conduction time** T_{on}. Due to the negative current that is needed for ZVS turning-on of the main switch, the average current value is lower than simply I_{peak}. This would make the power level less than expected. In this design, this effect of negative valley current is not addressed, and T_{on} is kept constant. In order to deliver the same power with a negative current value at the valley, T_{on} needs to be larger than $2\times I_{average}$ and variable with the change of I_{valley}. Solving this issue will also solve the problem that during very low v_{AC}, the peak resonant transient lacks inductive energy for ZVS.

4. **Low power control scheme**. When the power is low, the control method currently using will lead to higher switching frequency, and thus lower efficiency due to higher switching loss, AC winding and core losses. In order to maintain good efficiency in low power scenario, special control scheme could be adapted. A possible approach is burst mode, in which the switching is heavily discontinuous, so that the effective switching frequency could be largely reduced.

5. **Benchmark testing against Si design**. A Si counterpart design could be made to compare the performance of the semiconductor devices.

A

Appendix

Table shows the power dissipation on the input & output fuses(ATM10, 10A fuse, MERSEN / FERRAZ SHAWMUT).

conducting current (A)	voltage drop (mV)	power dissipation (mW)
1	14.4	14.4
2	29.2	58.4
3	45.4	136.2
4	62.9	251.6
5	82.3	411.5
6	104.3	625.8
7	127.2	890.4
8	153.9	1231.2
9	181.9	1637.1
10	215.4	2154.0
11	265.5	2920.5
11.5	300.1	3451.2

Table A.1: Power dissipation on fuse, with different current

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