Temperature-Based MPPT Circuit for a Tumbling PocketQube: Design and Experimental Performance Analysis

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Temperature-Based MPPT Circuit for a Tumbling PocketQube: Design and Experimental Performance Analysis

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Summary

PocketQubes are a young technology that brings with it a vast amount of research opportunities. These pico-satellites consist of standardised units (P) of 5x5x5 cm. Currently, the Delfi team at the Delft University of Technology is developing the next 3P PocketQube mission. One of the goals of this mission is to continue to advance this satellite technology by learning from the challenges encountered in the previous PocketQube.

The focus of this research is on the power generation system of the satellite. In the previous Delfi mission, a Maximum Power Point Tracking (MPPT) technique called Perturb and Observe was used to extract as much power as possible from the small solar cells. However, it did not generate as much power as expected due to the tumbling of the satellite. Therefore, various other MPPT methods were researched and a technique was found that will likely be more suitable for a tumbling PocketQube: temperature-based MPPT. Based on the temperature of the solar cell, this method calculates the voltage at which the cell will generate the most amount of power (V_{MPP}) using a linear equation. The objective of this research is to design, manufacture and test a prototype circuit that implements this method so that its performance can be investigated. Based on this, the viability of using this method on a PocketQube can be evaluated.

The prototype consists of three separate Printed Circuit Boards (PCBs). One houses the solar cells and temperature sensors and is mounted on a test stand in front of a powerful lamp that mimics the sun. The second PCB is a demo circuit board for a Direct Current to Direct Current converter (DC-DC converter), which is used to convert the power from the solar cells to the correct voltage for the battery. In addition, it can limit the voltage of the solar cells so that they operate at their Maximum Power Point (MPP). The last PCB is the link between the other two and also connects to the load. Furthermore, it houses the control circuit that drives the solar voltage limit set by the DC-DC converter based on the temperature measurement that comes from the PCB with the solar cells.

This prototype was tested with a resistive load while the aforementioned lamp was illuminating the solar cells. By varying the load resistance, the demanded power could be varied. In this way, the performance of the circuit could be measured while operating under, at, and over the MPP. The solar cells could also be cooled down using Peltier modules on the test stand and were heated by the radiation of the lamp, allowing for different temperature environments. The irradiance was also rapidly varied by dropping an opaque plastic sheet between the lamp and the solar cells. Measurements were made with an oscilloscope or using digital multimeters present on the PCB with the control circuit.

In general, the circuit functions as intended and promises to be a viable option for the power generation system of a tumbling PocketQube. It adapts rapidly to changes in irradiance and demanded power from the load, and it keeps up with changes in temperature. It also achieves an overall efficiency of more than 80%, occasionally reaching more than 85%. One major flaw remains: the temperature gradient of the limit set by the DC-DC converter does not exactly match the temperature gradient of the V_{MPP} of the solar cells. However, this can likely be solved by placing all circuitry on the same PCB. In addition, small tweaks to the design, such as decreasing the volume, and more tests should be performed before this circuit can fly on the next PocketQube.

Acknowledgements

Firstly, I would like to thank Stefano for his outstanding supervision throughout this project. I greatly appreciate the time you invested in guiding me, providing insightful feedback, and giving me many opportunities to learn and improve my engineering skills. I am very glad that I approached you for a thesis project, as I thoroughly enjoyed the experience and could not have imagined a better supervisor. I would also like to thank Sevket for always being available to answer technical questions and for consistently offering valuable feedback as well.

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- Bavo Vlyminckx
May 2026

Contents

List of Abbreviations

ADI Analog Devices, Inc.

COTS Commercial Off-The-Shelf

DC Direct Current

DC-DC converter Direct Current to Direct Current converter

DET Direct Energy Transfer

FB Feedback

INA Instrumentation Amplifier

LDO Low-Dropout

LEO Low Earth Orbit

MPP Maximum Power Point

MPPC Maximum Power Point Control

MPPT Maximum Power Point Tracking

NTC Negative Temperature Coefficient

Op-Amp Operational Amplifier

P&O Perturb and Observe

PCB Printed Circuit Board

PTC Positive Temperature Coefficient

TI Texas Instruments

V_{MPP} Voltage at the Maximum Power Point

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1 Introduction

In the last two decades, CubeSats have become increasingly popular because their small size allows researchers and universities to conduct space missions at a relatively low cost [1][2]. In addition, they provide a platform for students to gain hands-on experience with complete missions of real satellites [3]. As the miniaturisation trend continued in the space industry, the Delfi team from TU Delft took this innovation a step further and started the development of PocketQubes. These pico-satellites consist of units that have a standard size: 1P is a cube of 5x5x5 cm [4]. Therefore, their volume is one eighth of the volume of CubeSats, which presents numerous new challenges: the small size heavily constrains the volume of critical subsystems of the satellite. For example, there is less space for solar panels, decreasing the amount of generated power. In addition, the smaller attitude control system is less powerful, leading to higher tumbling rates in the order of multiple degrees per second [4].

The first PocketQube designed by TU Delft, which can be found in Figure 1.1, is Delfi-PQ: this is a 3P PocketQube that was launched in 2022. Since the Delfi team is currently working on the next PocketQube mission [5], it is important to look back at Delfi-PQ to learn from both its successes and failures. This experience can be critical to the success of the next mission. One major problem was found considering the power generation system of Delfi-PQ. This system did not work completely as intended, as less power was generated than expected during the mission. Therefore, the aim of this research is to find and work out a solution to the problem with the current power generation system. In this way, the next Delfi PocketQube will have more electrical power available to achieve its mission.

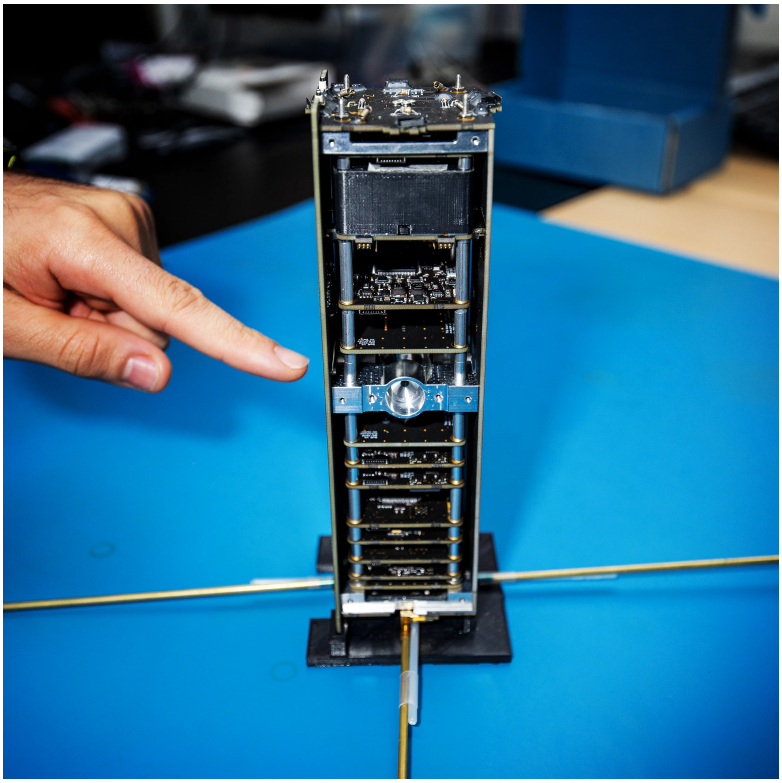


Figure 1.1: A partially integrated Delfi-PQ [6].

The PocketQube uses solar cells to charge its central battery. To generate enough power to keep the satellite running, a Maximum Power Point Tracking (MPPT) technique is used. These techniques ensure that the operating point of a solar cell moves with changes in temperature or irradiance in such a way that the solar cell generates as much power as possible under all environmental conditions [7]. To resolve the problem found on Delfi-PQ, first background information on state-of-the-art MPPT techniques is needed. With this knowledge, the power generation system of Delfi-PQ can be evaluated to determine what went wrong. Afterwards, a decision can be made on whether the issue can be easily fixed or whether an entirely new system needs to be designed.

This report is structured in the following way. In chapter 2, background information on power system architectures and MPPT techniques is discussed. Using this information, a solution is proposed to the problem of Delfi-PQ's power generation system in chapter 3. Here, a research objective, research questions, and a hypothesis for the remaining research are also formed. Subsequently, the methodology used to work out the solution is presented in chapter 4. Afterwards, the proposed solution is tested and the corresponding results are discussed in chapter 5. Based on these results, a conclusion is drawn in chapter 6. Finally, in chapter 7, recommendations are given on how to further develop the proposed solution.

2 Background Information

MPPT techniques are used to extract as much power as possible from a solar cell. To understand how they could be employed on the PocketQube, an overview of the satellite's power system architecture is given in section 2.1. Then, a brief explanation of solar panels is given in section 2.2. Finally, in section 2.3, numerous MPPT methods are evaluated.

2.1. Power System Architecture

To power all electrical components on the PocketQube, solar cells will be used. However, it is not advisable to simply connect the solar cells to these loads. The voltage produced by the cells can vary with environmental conditions and may not be compatible with the loads. In addition, when the satellite is in eclipse, no power will be produced and all electrical components will become inactive. Some loads can also become inactive when more power is required than the cells can generate, even when not in eclipse. Therefore, it is essential to include a battery that can provide additional energy when the solar cells do not produce enough power. This battery can be recharged when the cells produce more than is required by the loads.

When designing any part of a satellite power system, it is important to first consider how the solar cells, battery, and loads are connected to each other. Various options are briefly explained in subsection 2.1.1. Then, the power system architecture of the PocketQube will be discussed further in subsection 2.1.2.

2.1.1. Properties of Power System Architectures

There are various ways to categorise power system architectures of satellites [8]. For brevity and clarity, the two most influential properties will be discussed here. These are the regulation of the Direct Current (DC) bus and the interface between the solar cells and the rest of the power system.

DC-bus Regulation

There are three main ways to regulate the voltage of the DC-bus. Firstly, an unregulated or battery regulated bus, which is shown in Figure 2.1, has the battery terminals connected directly to the bus, without any regulation in between [9]. Therefore, the voltage of the bus can swing as the battery is being charged or discharged. This means that voltage regulators are needed to adequately condition the voltage level from the bus before it reaches the electrical loads.

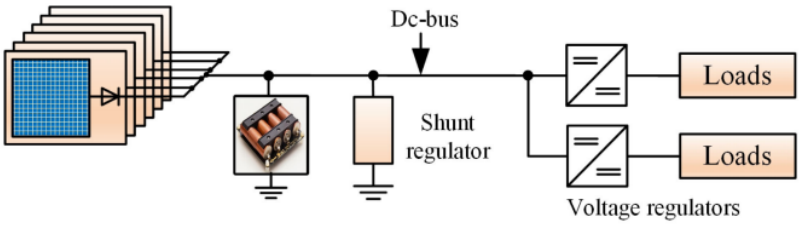


Figure 2.1: DET architecture with an unregulated bus [8].

A regulated bus, on the other hand, has a fixed voltage. Therefore, it has a (dis)charge regulator in between the battery and the DC-bus to decouple their voltages, as shown in Figure 2.2. Each voltage regulator has some loss in efficiency, so this (dis)charge regulator slightly decreases the overall efficiency of the electrical storage on the satellite [10]. Additionally, these regulators will achieve their highest efficiency only at a specific operating point [11]. Therefore, care must be taken in selecting a regulator to maximise its efficiency throughout all operating points of the complete power system.

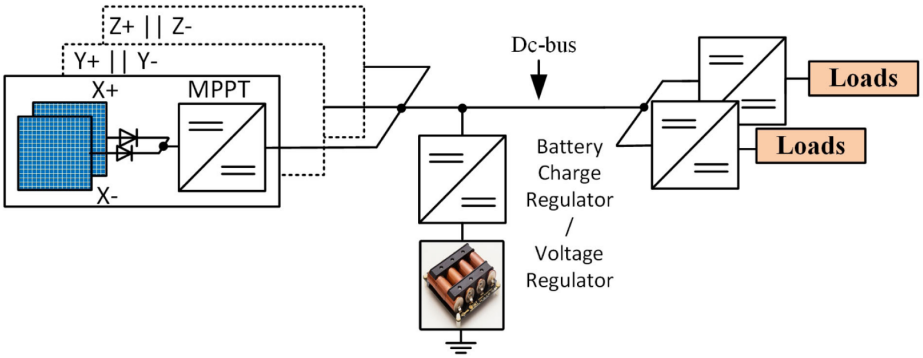


Figure 2.2: MPPT architecture with a regulated bus [8].

A sun-regulated or partially regulated architecture, which is shown in Figure 2.3, also has a battery charging regulator in between the DC-bus and the battery. However, there is an additional diode that connects the battery to the bus. In this way, during the sun-lit period, the battery is being charged through the regulator, and the voltage of the DC-bus is fixed. However, during the eclipse period, the battery provides power directly through the diode, so now the battery dictates the bus voltage [9]. Since the power does not have to go through the charging regulator, there are no conversion losses when discharging the battery, so the efficiency is increased.

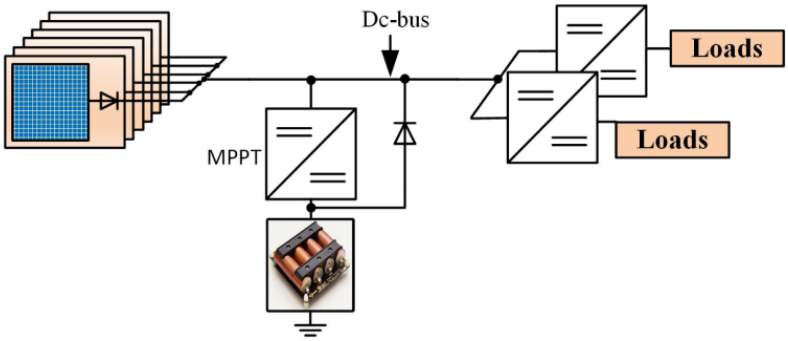


Figure 2.3: DET-MPPT hybrid architecture with a sun-regulated bus [8].

Interface of Solar Cells

The interface between the solar cells and the rest of the power system is another important design choice. One solution is to connect the solar cells to the bus through a diode. The diode prevents energy flowing from the bus back to the solar panels [12]. This method is called Direct Energy Transfer (DET), and an architecture that implements DET is shown in Figure 2.1. DET is a simple and therefore robust solution. In addition, it is an efficient way to connect solar cells to the rest of the power system, especially in a stable environment such as on a large satellite in geostationary orbit [13].

Another way to interface with the solar cells is by implementing MPPT. MPPT uses a Direct Current to Direct Current converter (DC-DC converter) to adapt the impedance of the electrical load to the impedance at which the solar cells generate the maximum amount of power [9]. Thus, a DC-DC converter, which is essentially a voltage regulator, is needed between the DC-bus and the solar cells, as shown in Figure 2.2. This adds an additional regulator to the power system, which reduces the overall efficiency. However, MPPT can ensure that the solar cells produce the maximum amount of power at all times [12]. This results in an overall increase in efficiency, especially in a rapidly changing environment such as on a tumbling satellite in Low Earth Orbit (LEO) [14]. Note that MPPT is more complex than DET and therefore can be less reliable [15]. A more in-depth explanation of MPPT can be found in section 2.2 and 2.3.

2.1.2. Architecture of the PocketQube

Due to the limited size of the PocketQube, only a small area of solar cells is available to produce power. Therefore, the efficiency of the power system is the highest priority so that all electrical loads can be powered. One paper [16] compares different bus regulation topologies using an efficiency index that covers a full LEO cycle, where a higher index indicates a higher efficiency. They calculated an efficiency index of 69 to 74 for a fully regulated DC-bus, while an unregulated or sun-regulated bus achieved an index of 75 to 82. In addition, an unregulated bus is more reliable due to its lower component count and because it has fewer single points of failure than a (sun-)regulated bus [17].

Other researchers [18] compared the efficiency of MPPT and DET architectures, specifically for CubeSats. They also took into account the constraints these small satellites have on their attitude control. Their results show that despite the additional DC-DC converter, MPPT topologies are overall more efficient, reaching an efficiency of 85% to 90%. DET architectures, on the other hand, only reached efficiencies of 70% to 82%. This is because the DET architectures lose efficiency by not always operating at the point where the solar cells generate the maximum amount of power. Additionally, they showed that for architectures that include MPPT, an unregulated DC-bus is 5% more efficient than a regulated bus.

In conclusion, an architecture with an unregulated bus and MPPT for the solar cells, as shown in Figure 2.4, promises the highest efficiency. This architecture was used on Delfi-PQ [19], and before the start of this work, it was decided that it will be used again on the next PocketQube.

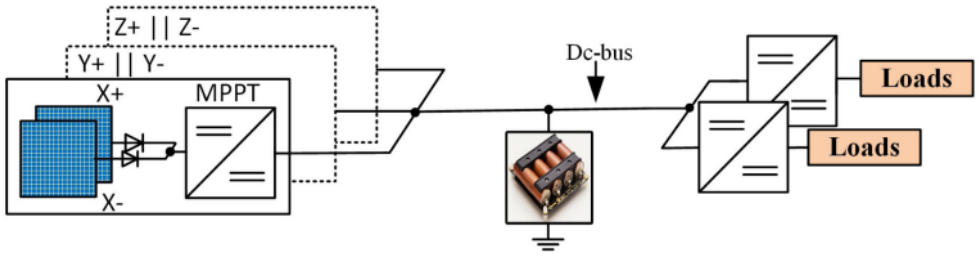


Figure 2.4: MPPT architecture with an unregulated bus [8].

2.2. Workings of a Solar Cell

A solar cell converts sunlight into electrical energy by making use of the photovoltaic effect [20]. A model of this process, which involves the equivalent circuit of a solar cell, is briefly presented in subsection 2.2.1. Afterwards, the performance of a solar panel and its relation to its environment is further investigated in subsection 2.2.2. This is done by discussing graphs that plot the generated power or current in function of the voltage of the solar cell.

2.2.1. Equivalent Circuit

The simplest equivalent circuit of a solar cell would be a current source with a diode in parallel. These two components make up the ideal model that ignores any losses [20]. However, losses do occur in practice, and these are modelled by a parallel (R_{sh}) and series (R_{s}) resistor, as shown in Figure 2.5. The parallel resistor models the mechanical defects in the semiconductor, while the series resistance takes into account the ohmic losses on the path of the electrons through the solar cell [21]. To increase the performance of the solar panel, R_{sh} should be as high as possible, while R_{s} should be minimal.

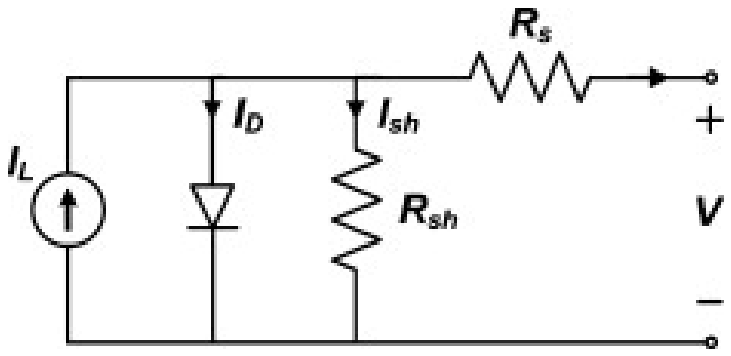


Figure 2.5: Equivalent circuit of a solar cell [21].

This equivalent circuit results in a mathematical model given in Equation 2.1 [20]. Here, I_{out} is the output current of the complete solar cell, which is the current the load will see. This is the current we want to calculate in function of the output voltage V. I_{L} is the current generated by the photovoltaic effect. a is the modified ideality factor of the diode, and I_{o} is the saturation current of the diode.

$$I_{\text{out}} = I_{\text{L}} - I_{\text{D}} - I_{\text{sh}} = I_{\text{L}} - I_{\text{o}} \left[e^{\left(\frac{V + I_{\text{out}} R_{\text{s}}}{a}\right)} - 1 \right] - \left(\frac{V + I_{\text{out}} R_{\text{s}}}{R_{\text{sh}}} \right) \tag{2.1}$$

From this equation, it can be deducted that the output current of the solar cell in function of the output voltage is determined by these parameters: I_{L}, I_{o}, a, R_{sh} and R_{s}. These parameters can be obtained, but this requires numerically solving a large set of non-linear equations. These equations also depend on temperature and solar irradiance, and the parameters themselves can also change over time due to the degradation of the solar cell in space [21]. On top of that, this formula for the output current requires the output current to be known, making it a recursive equation. This all makes it difficult to accurately model in real-time a solar cell that experiences a changing environment, especially throughout the complete life-time of a cell on a satellite [22].

2.2.2. Maximum Power Point

A more practical way to look at the performance of a solar cell is by plotting Equation 2.1 on a current vs. voltage graph, as shown in Figure 2.6. On this graph, also the power is plotted in function of voltage. This is easily calculated using $P = I \cdot V$.

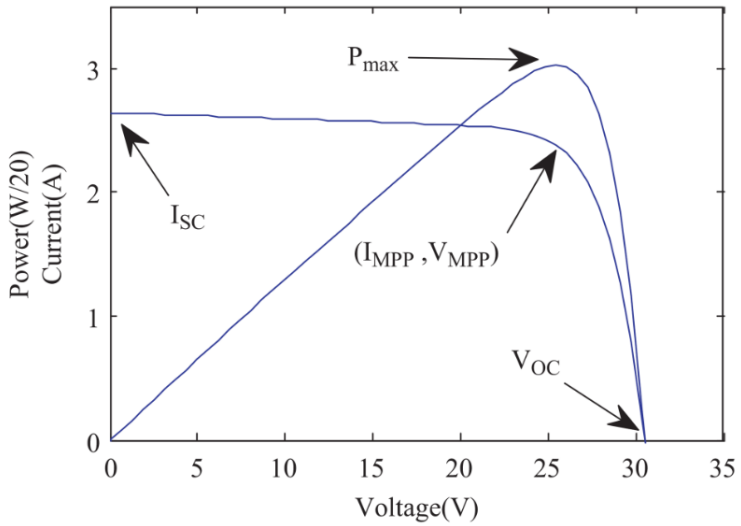


Figure 2.6: I-V and P-V curve of a solar cell [23].

The I-V curve shows all the possible operating points that this solar cell can operate at under one set of environmental conditions. However, as can be observed from the P-V curve, these operating points do not result in equal power generation. The point in which the highest amount of power is generated for these environmental conditions is called the Maximum Power Point (MPP) [23]. At this point (P_{max}), the solar cell is operating at its highest power efficiency.

The I-V and P-V curves of a solar cell are influenced by the environmental conditions surrounding the solar panel. The main parameters that need to be taken into account are solar irradiance and temperature [24]. Figure 2.7 shows the effect that these parameters have on the P-V curve. As can be observed, increasing temperature decreases the power, and also decreases the Voltage at the Maximum Power Point (V_{MPP}). On the other hand, an increase in solar radiation increases the generated power, and has an almost negligible impact on the V_{MPP}.

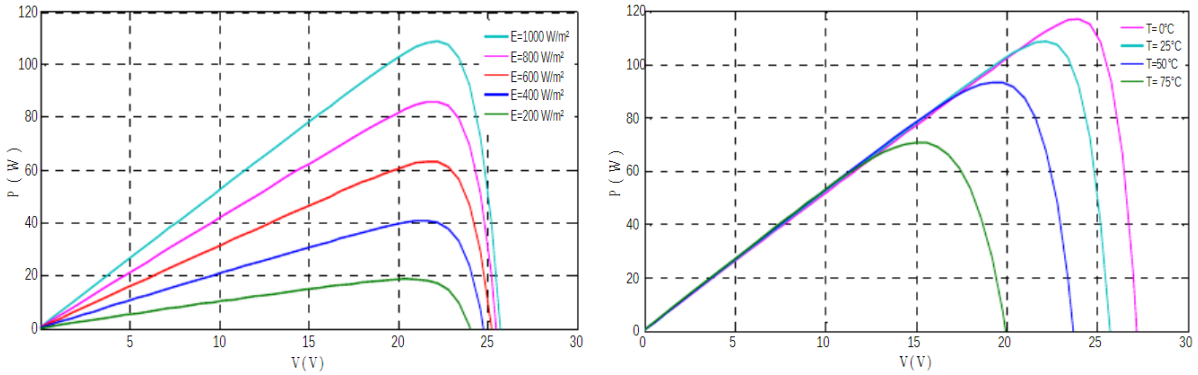


Figure 2.7: Influence of solar irradiance (left) and temperature (right) on the P-V curve [24].

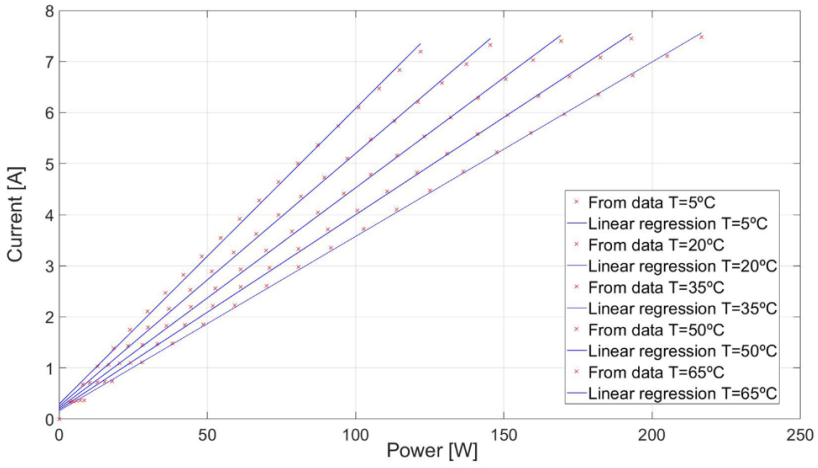


Figure 2.8: Linear regressions through MPPs under the same temperature, but different irradiances [25].

This last relation can be further highlighted by Figure 2.8. Here, a linear regression is made through a set of MPPs that were measured at the same temperature, but at different irradiances. This was repeated for multiple sets that were each measured at a different temperature. Figure 2.8 shows a current versus power graph. Since power is current times voltage, a straight line on this graph means that the voltage stays constant. As can be observed, these linear regressions closely follow the MPPs. Therefore, when the temperature remains constant, the voltage of the MPP also remains mostly constant, even under changing solar irradiance. This means that the V_{MPP} could be obtained by measuring only the temperature of the solar cell, without the need to calculate the generated power.

2.3. MPPT Techniques

MPPT has various possible implementations. In subsection 2.3.1, the general hardware set-up required to implement MPPT will first be explained. Then, from subsection 2.3.2 to subsection 2.3.6, a number of relevant methods will be explained and their strengths and weaknesses will be discussed.

2.3.1. Fundamental Operational Principles

As explained in subsection 2.2.2, a solar panel generates the maximum amount of power only at one specific operating voltage (V_{MPP}) that changes with environmental conditions. Therefore, the goal of MPPT is to adjust the operating voltage as closely as possible to the V_{MPP}. To understand how this can be achieved, an explanation is first needed on the operating point of a solar cell.

Consider the case where a resistor (R_{LOAD}) is directly connected between the terminals of a solar cell. Under certain environmental conditions, the solar panel will have a certain I-V curve, which is represented on the left of Figure 2.9. Additionally, R_{LOAD} will be displayed as a straight line on an I-V plot since $I = \frac{1}{R_{LOAD}}V$. This is shown on the middle plot of Figure 2.9. The point in which these two graphs coincide, as shown in the right plot of Figure 2.9, will be the operating point of the solar cell [7]. If either the load resistance or the environmental conditions change, one of the graphs will shift and the operating point will change.

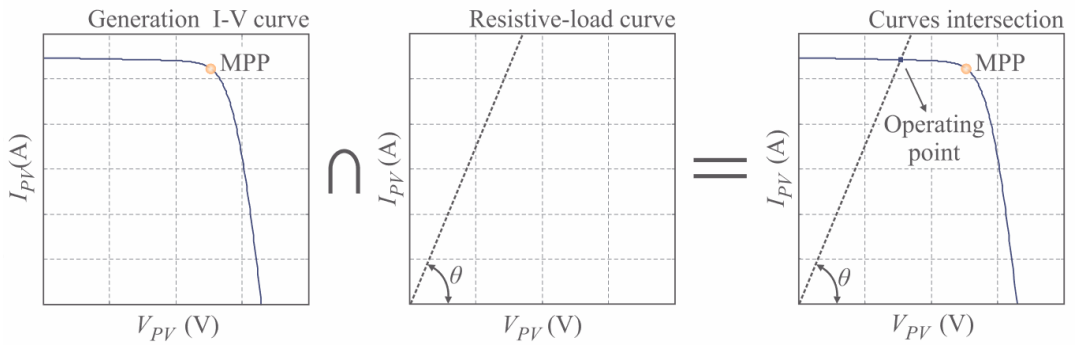


Figure 2.9: Influence of the environmental conditions and the load resistance on the operating point of the solar panels [7].

With this simple set-up of a resistor connected to a solar cell, it is unlikely that the operating point of the cell will coincide with its MPP, especially under a changing environment. Therefore, a DC-DC converter is added between the solar panel and the load, as shown in Figure 2.10. A DC-DC converter can alter the DC voltage level between its input and output. If its input voltage is increased compared to the output voltage, the input current decreases, since power must remain constant (without losses). The opposite is true when the input voltage is decreased [26]. In this way, the converter can effectively alter the load resistance as seen by the solar cell. The duty cycle (D) of the converter determines how much the apparent resistance is altered. If it is managed correctly, the converter can always change the load curve so that it coincides with the MPP of the cell, increasing the efficiency of the power system.

A problem still remains in finding the V_{MPP} and subsequently determining the desired duty cycle of the DC-DC converter. It is technically possible to measure the temperature and irradiance of the solar cell and determine the V_{MPP} based on these parameters. However, it is difficult to accurately measure the environmental conditions of the solar cell, especially the irradiance. On top of that, correctly determining

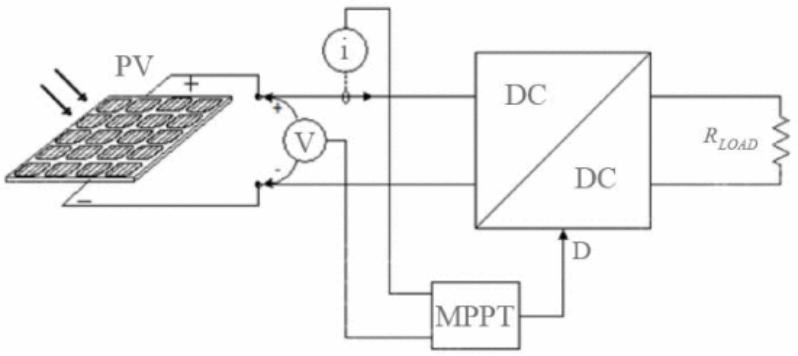


Figure 2.10: General layout of an MPPT system [27].

the V_{MPP} based on these conditions requires a detailed model. This model also has to adapt over time, since the solar panels will degrade due to e.g. radiation [22]. Therefore, MPPT techniques have been developed to determine the V_{MPP} in a different way: by measuring the voltage and current of the solar cell. These values are the input of an algorithm that calculates the required duty cycle of the DC-DC converter so that the solar cells operate at their MPP. Various algorithms exist and they will be discussed in the following sections.

2.3.2. Constant Voltage and Constant Current Methods

Based on the P-V curves shown in Figure 2.7, a relation can be deducted between the V_{MPP} and the open circuit voltage. This relation can be approximated to be linear, independent of the environmental conditions. Therefore, the V_{MPP} can be assumed to always be a constant fraction of the open circuit voltage [28].

Based on this relation, a simple control algorithm can be constructed [29]: first, the solar panel is disconnected from the power system, and the open circuit voltage is measured. Then, the V_{MPP} is calculated by multiplying the open circuit voltage with the constant factor. Afterwards, the solar panel is connected to the power system again, and the duty cycle of the DC-DC converter is adjusted so that the voltage on the solar panels matches the V_{MPP}. This algorithm is then repeated at a set interval.

A similar method exists that senses the short circuit current instead of the open circuit voltage. This is possible since the current at the MPP can also be approximated as a constant fraction of the short circuit current of the solar panel [28]. Thus, a similar algorithm can be constructed. The main difference is that after the solar panel is disconnected from the power system, it has to be shorted to measure the short circuit current [29]. This increases the complexity and, therefore, the constant voltage method is used more often than the constant current method.

Both of these methods are simple to implement while having relatively high efficiencies: one paper [30] reports an overall efficiency of 92.4% for the constant voltage method and 93.4% for the constant current method. However, a major drawback of both methods is that the solar panel needs to be disconnected at each interval. This leads to some efficiency loss, as well as a short interruption of the power supply [31]. This has especially a big impact when there is only one solar panel illuminated. In that case, the power flowing towards the MPPT circuit, and afterwards the battery, will drop to zero once in every cycle of the algorithm. Care must be taken to ensure that the MPPT circuit, battery, and the rest of the power system are able to handle this.

2.3.3. Perturb and Observe

Perturb and Observe (P&O) is another common MPPT method used in space and on the ground. The basic idea of P&O is to find the local maximum of the power curve presented in Figure 2.6. It does this by slightly altering the voltage of the solar cell, and checking if this perturbation brought the operating point closer to the MPP [23]. Based on this observation, the operating voltage is further adjusted.

The algorithm behind P&O [29], shown in Figure 2.11, starts by measuring both the voltage and current of the cell for this time step. Based on this, the power generated at this time step can also be calculated. This power value is then compared to the power generated in the previous time step. If the power did increase, then the voltage was likely perturbed in the correct direction. Therefore, if the voltage was increased before this time step, the voltage should be further increased, and in the other case it should be further decreased. In case the power decreased as compared to the previous time step, the voltage should be adjusted in the opposite direction as the perturbation. The correct change in voltage is then accomplished by adjusting the duty cycle of the DC-DC converter adequately. All these steps are then repeated at the next time step.

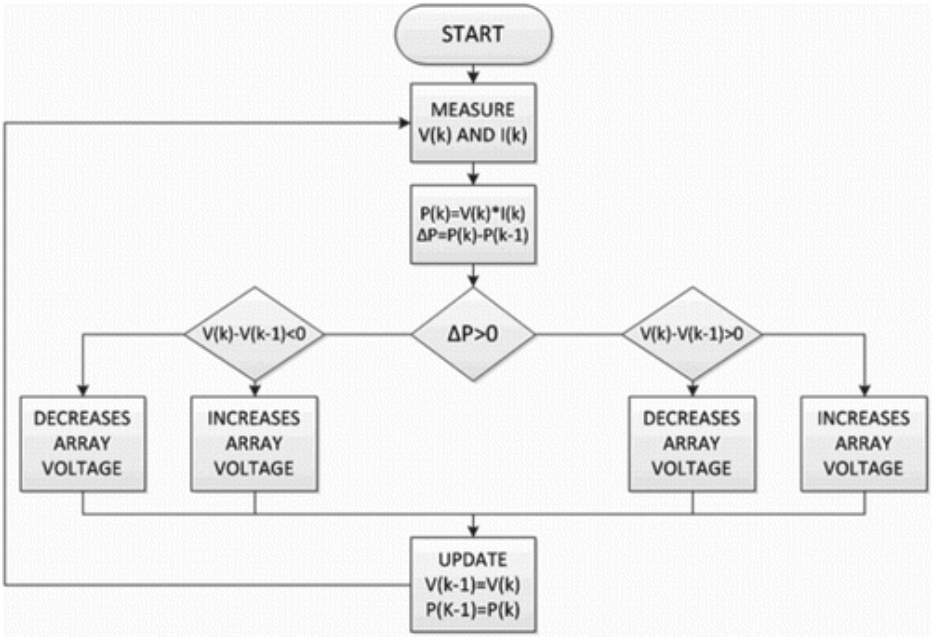


Figure 2.11: A flowchart of the P&O algorithm [29].

There are two parameters that should be tuned to optimise the performance of the algorithm: the time step between each execution of the algorithm, and the size of each perturbation in the cell voltage [32]. The shorter the time step, the faster the algorithm will converge to the MPP, but the more computational power is needed. Next, if the size of the perturbation is too small, the algorithm will take long to converge. However, if it is too large, it will constantly overshoot the MPP, inducing oscillations in the power supply. Thus, care must be taken to tune and test these parameters to increase the efficiency of the P&O algorithm [33].

P&O is a popular algorithm because it is still relatively simple to implement but obtains higher efficiencies than the constant voltage or current methods [34]. Two papers [30, 35] have calculated P&O's efficiency and got results between 95% and 98%. Another reason for its popularity is that only two

measurements are needed [36]: a voltage and a current measurement. One disadvantage is that the power will oscillate around the MPP. This is because it is unlikely that the algorithm will land exactly on the MPP, unless the step size is small [28]. However, a small step size will likely lead to a too slow algorithm.

The main disadvantage of P&O is that it can become confused in rapidly changing environmental conditions [37], such as in a tumbling satellite. For example, when a perturbation step is made away from the MPP, but in the same moment the irradiance increases substantially, the produced power can still have increased. This will lead the algorithm to think that the perturbation brought the operating point closer to the MPP [38]. Therefore, the next perturbation will again move away from the actual MPP. If the irradiance would continue to increase, then this pattern could repeat itself, pushing the operating point further and further away from the MPP. This could reduce the tracking efficiency of the algorithm by 20% when tumbling at 6° per second [39]. For reference, the tumbling rate of Delfi-PQ was designed to be between $5°$ and $10°$ per second [4].

2.3.4. Incremental Conductance

Incremental conductance is another widely used MPPT technique that tries to locate the MPP by finding the derivative of the P-V curve. As can be deduced from Figure 2.6, the derivative of power with respect to voltage is zero at the MPP. Therefore, Equation 2.2 can be derived [36].

$$\frac{dP}{dV} = \frac{dIV}{dV} = I + V\frac{dI}{dV} = 0 \tag{2.2}$$

From this equation it follows that if $\frac{dI}{dV} = -\frac{I}{V}$, the solar panels are operating at their MPP [36]. However, if $\frac{dP}{dV} = I + V\frac{dI}{dV} > 0$, and thus $\frac{dI}{dV} > -\frac{I}{V}$, it means the slope on the P-V curve is positive, meaning the operating voltage is lower than the voltage at the MPP. On the other hand, if $\frac{dI}{dV} < -\frac{I}{V}$, the operating voltage should be decreased to reach the MPP.

In practice, the derivative $\frac{dI}{dV}$ is calculated numerically by first calculating ΔI and ΔV separately. This can be seen at the top of Figure 2.12, which shows the complete algorithm to implement the incremental conductance method. The left hand side of the algorithm determines whether or not to increase the operating voltage based on the formulas that were explained above. However, when $\Delta V = 0$, the equations blow up to infinity. Therefore, the right hand side of the algorithm is needed: when the voltage is constant but the current increases, the power will also increase. Therefore, the operating point will move straight upwards on the P-V curve. This can be interpreted as a (infinitely) positive derivative. A positive derivative means the operating voltage is lower than V_{MPP}, so the voltage will be increased. The opposite is true for when the current decreases. One paper does suggest that the right hand side is not needed, since it is unlikely the $\frac{dI}{dV}$ will exactly equal $-\frac{I}{V}$ [40].

Incremental conductance is the second-most popular MPPT technique, after P&O [40]. Similarly, it only uses one current and one voltage measurement. It also has a high efficiency: two papers [30, 35] report an efficiency between 95% and 99%. However, its implementation is slightly more complex [41]. Another similarity with P&O is that the time step and the perturbation step have to be tuned in order for the algorithm to work optimally [29]. This fixed step size will again result in oscillations around the MPP [42]. Additionally, incremental conductance can also get confused in a rapidly changing environment such as on a tumbling PocketQube, contrary to the general consensus in literature [40]. This confusion can result in an update of the operating voltage in the wrong direction, reducing efficiency [43].

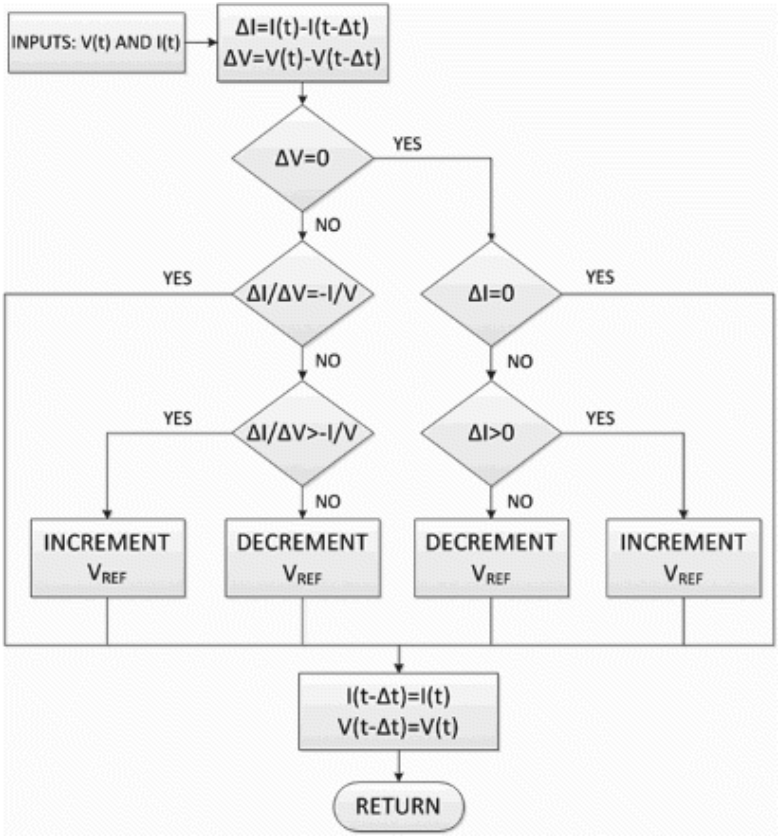


Figure 2.12: A flowchart of the incremental conductance algorithm [29].

A lot of similarities have been pointed out between P&O and incremental conductance. One paper investigated these similarities, and even concluded that these methods are in essence equivalent to each other [41]. They even suggest that incremental conductance should be regarded as a specific implementation of P&O.

2.3.5. Temperature-Based MPPT

An MPPT technique that is less common in literature is one based on temperature. As discussed in subsection 2.2.2, the solar irradiance has a negligible impact on V_{MPP}, while temperature has a large impact. Therefore, the assumption can be made that the V_{MPP} can be found purely by measuring the temperature of the solar cell [44].

In total, two measurements are then needed: the temperature of the solar cell, and the voltage across the cell [45]. The temperature sensor is usually put on the back of the solar cell to get an accurate measurement by being as close to the solar cell as possible. The temperature decides what the operating voltage of the PV cell should be, and the voltage measurement can then be used for closed loop control.

In order for this technique to be implemented, a relation needs to be found between the temperature and the V_{MPP} of the solar cell. This relation can be approximated with a linear equation, shown here as Equation 2.3 [45].

$$V_{MPP} = V_{MPP}^{STC} + (T - T^{STC})\mu_V \tag{2.3}$$

Here, T^{STC} is the temperature at standard conditions, which has a pre-defined value set by the manufacturer. V_{MPP}^{STC} is then the V_{MPP} at the same standard conditions. Finally, μ_V linearly relates the change in temperature, T, to the change in V_{MPP}. By utilising this equation, the desired operating voltage of the solar cells can be quickly found by measuring the temperature of the cell.

Having determined the desired operating voltage, there are two ways to achieve that voltage. One method [44] compares the desired voltage with the voltage that is across the solar cell at that moment, as shown in Figure 2.13. The difference between these voltages is then converted to a change in duty cycle using Equation 2.4.

$$\Delta D = (V_{solar} - V_{MPP})k_{\Delta D} \tag{2.4}$$

Here, ΔD is the change in duty cycle, and $k_{\Delta D}$ is a constant scaling factor. This scaling factor has to be tuned correctly, since this decides the step size of the change in duty cycle each iteration. Therefore, a larger value for this constant results in a quicker convergence to the V_{MPP}. However, if the value is too large, oscillations may occur.

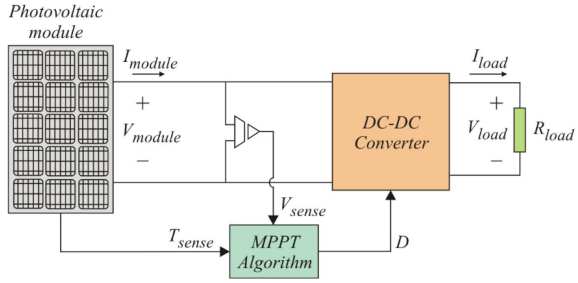


Figure 2.13: Temperature-based MPPT using a measurement of the solar cell voltage [44].

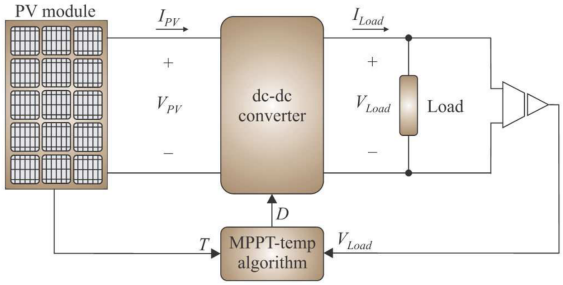


Figure 2.14: Temperature-based MPPT using a measurement of the load voltage [7].

Another method [7] measures the voltage across the load instead, which can be seen in Figure 2.14. This way, the gain G of the DC-DC converter can be calculated immediately using Equation 2.5.

$$G = \frac{V_{load}}{V_{solar}} = \frac{V_{load}}{V_{MPP}^{STC} + (T - T^{STC})\mu_V} \tag{2.5}$$

Depending on the type of DC-DC converter that the designer selects, there exist different equations to relate this gain G to the desired duty cycle D [26]. Examples of these equations can be found in Equation 2.6 to 2.8.

$$\text{Buck Converter:} \qquad D = G \tag{2.6}$$

$$\text{Boost Converter:} \qquad D = 1 - \frac{1}{G} \tag{2.7}$$

$$\text{Buck-Boost, SEPIC, Cuk and Zeta Converter:} \qquad D = \frac{G}{1+G} \tag{2.8}$$

Temperature-based MPPT requires only simple circuits, is robust, and converges quickly due to its linear nature [20, 25]. There are also little to no oscillations around the MPP [7]. In addition, the rapidly changing irradiance experienced on a tumbling satellite does not need to be taken into account. Instead, only the effect of temperature is measured, which varies relatively slowly due to the thermal mass of the satellite. Thus, this MPPT method will be inherently more stable [44]. The main disadvantage is that the

coefficients of the linear equation need to be known accurately. These coefficients can be found on the datasheet of the cell. For example, the datasheet of the 3G30A solar cell [46] gives $V_{MPP}^{STC} = 2409mV$, $T^{STC} = 28°C$, and $\mu_V = -6.7mV/°C$. However, they will change due to degradation of the solar cell, and small variations can exist between cells, so it is advised to test every cell separately [25, 47].

One paper [39] has already performed experiments on two solar cells. Their goal was to investigate the feasibility of this MPPT method by comparing the behaviour of the cells to the linear formula shown in Equation 2.3. The results seem promising, as they predict an efficiency of $95-99$% for a fully functioning MPPT circuit. Additionally, they found no significant influence of irradiance on the accuracy of finding the V_{MPP}. This leads them to conclude that tumbling of the satellite, even at rates greater than $10°/s$, will not have a major impact on the efficiency of this method. In their paper, a physical MPPT circuit has not been implemented yet. Therefore, this is one of their main recommendations for future work.

2.3.6. Other MPPT Techniques

Numerous more MPPT methods exist [48], including variations on already mentioned techniques. A common addition to both P&O and incremental conductance methods is a variable or adaptive step size. Here, the perturbation step size is increased when the operating point of the solar cell is far away from the MPP, and gets smaller as the MPP is approached [49]. This results in the MPP being approached faster, and oscillations around the MPP are also reduced [49, 50]. However, in case only the size of the perturbation step is changed and not its direction, the algorithm can still get confused in rapidly changing environments, as explained in subsection 2.3.3. Additionally, the extra logic needed to control the variable step size adds complexity to the MPPT method. It should be investigated if these disadvantages are worth the improvement in efficiency, since one paper [49] found that the efficiency of P&O increased by less than 1% after implementing a variable step size.

One paper tries to overcome the confusion of P&O and incremental conductance due to the environment [38]. They propose to take two measurements in each cycle of the algorithm. For one of these measurements, the duty cycle of the DC-DC converter is not changed, so that the influence of only the environment is measured. In the other measurement, the MPPT algorithm does change the duty cycle, meaning the influence of both the environment and the MPPT is measured. In the assumption that the change in the environment does not differ between the two measurements, the influence of only the MPPT method can be extracted. This is a good improvement for these two algorithms, since the paper found it improved the efficiency of P&O with 5%. However, the extra measurement increases the time needed for each cycle. Additionally, the complexity of the algorithm is increased as well, since additional calculations are needed.

Other methods make use of neural networks to model the behaviour of the solar cell [51]. These networks can have as inputs the voltage, current, solar radiation or temperature that the solar cell experiences. Usually it is a combination of these factors that are used as the input. The output is often directly the required duty cycle of the DC-DC converter. These techniques can reach high efficiencies of 98%, but this does require a large amount of data to train the neural networks [51]. Each solar panel can also be slightly different, meaning they all require their own training data. Additionally, the solar cell will degrade over time, which means the network should ideally be trained again after a certain amount of time [48]. This is, however, not possible for space missions. Furthermore, these methods require many computations for each cycle as compared to e.g. P&O, making them highly complex [43].

3 Research Objective

Delfi-PQ deployed P&O as its MPPT algorithm due to its ease of implementation, as discussed in subsection 2.3.3. In addition, this technique promises a high efficiency without requiring many resources. Another important factor in the decision was the availability of the integrated circuits that are needed for MPPT. This is because the integrated circuits had to be able to handle low operating voltages, since each solar cell had its own MPPT circuit.

Delfi-PQ was also designed to minimise its tumbling rate down to 5-10 degrees per second [4]. However, this rate still resulted in relatively quick changes in the solar irradiance. As explained in subsection 2.3.3, the P&O algorithm can get confused in a rapidly changing environment, which was the case here. The specific integrated circuit that performed MPPT on Delfi-PQ updated the operating point of the solar cells every two seconds only. This meant that the satellite could have rotated 20 degrees between updates, resulting in a large difference in irradiance. This led to a large shift in the MPP between updates, which caused the MPPT circuit to become confused, reducing the power generation efficiency of Delfi-PQ. Because the tumbling rate will likely remain similar for the next PocketQube, it is recommended to use a different MPPT algorithm altogether.

New MPPT Algorithm

Selecting a different MPPT method for a PocketQube is no easy feat. The choice is heavily limited by the constraints that are inherent to the design of a PocketQube [52]: firstly, the small volume limits the available space for the circuitry itself. This small form factor also leads to a small surface area that is available for solar panels. This pushes the need for a highly efficient MPPT method, to extract as much energy as possible given the little size of the solar panels. Next, because of the limited size of the attitude control system, tumbling is highly likely to occur in a PocketQube. Therefore, the MPPT method should be resilient against this. Additionally, the computational power is also limited, since micro-controllers take up a non-negligible volume inside the satellite. Finally, the integrated circuits and other hardware necessary for the MPPT method need to be compatible with the low voltages that are common in PocketQubes.

In section 2.3, alternative state-of-the-art MPPT methods were discussed in detail. One of these methods, incremental conductance, was deemed equivalent to P&O and is therefore discarded as an option. Other adaptations of P&O and incremental conductance generally increase the complexity of the algorithm, with only a few percent increase in efficiency. Since a PocketQube has highly limited resources, this is not advised either. This also holds for other complex MPPT algorithms, like the intelligent methods that make use of neural networks. Furthermore, having interruptions in the power supply caused by constant voltage or current methods is sub-optimal too.

The proposed algorithm is therefore the MPPT method based on temperature, which was presented in subsection 2.3.5. This algorithm is simple and reliable and only needs to keep up with changes in temperature, which are relatively slow. The irradiance has a negligible effect on the V_{MPP}, which means that tumbling will not significantly affect the power generation efficiency. The only sensors required to implement this method are a temperature and voltage sensor. Additionally, the coefficients of a linear equation relating the V_{MPP} to temperature have to be obtained from the manufacturer or

through experimental analysis. As mentioned in subsection 2.3.5, one paper [39] has been able to extract these coefficients through experiments, and the results look promising. However, they did not fully implement an MPPT circuit yet, which is the recommended next step in confirming the validity of this method.

Research Objective and Questions

While researching MPPT methods, no examples were found of CubeSats or PocketQubes that employ the MPPT method based on temperature. Therefore, it is essential to first confirm whether this method is adequate for the next Delfi PocketQube. The following research objective is thus proposed:

To investigate the performance of a temperature-based MPPT technique for a tumbling PocketQube in LEO by implementing and experimentally testing an MPPT circuit using solar cells in different temperature and irradiance environments.

The research objective then leads to the following main research question:

How performant is a temperature-based MPPT circuit in extracting power from solar cells on a tumbling PocketQube in LEO?

Since the main research question is still relatively broad, a set of sub-questions is proposed:

- *What is the average efficiency of the complete power generation system?*
- *How quickly does the MPPT circuit respond to changes in the temperature of the solar cells?*
- *How quickly does the MPPT circuit respond to changes in irradiance hitting the solar cells?*
- *How can the temperature of the solar cells be measured accurately?*
- *What is the operational temperature range of the MPPT circuit?*
- *How can the MPPT circuit be tested in the lab so that the test conditions resemble a tumbling PocketQube in LEO?*

Hypothesis

Based on the literature research discussed in chapter 2, temperature-based MPPT is a promising technique. This is also the reason why it is proposed as a replacement for the P&O technique deployed on Delfi-PQ. It is expected to perform well when practically implemented. Therefore, the formal hypothesis for this research is as follows:

Because variations in temperature occur substantially slower than variations in irradiance on the solar cells of a tumbling PocketQube, a temperature-based MPPT circuit can sufficiently quickly track the MPP and extract an adequate amount of power from the solar cells.

The hypothesis presented above will be investigated in this report. For this, first a circuit needs to be designed that implements temperature-based MPPT. After manufacturing this circuit, it should be tested on solar cells that are similar to the cells of the next PocketQube. The results of these tests will be used to answer the research questions and to prove or disprove the hypothesis.

4 Methodology

In this chapter, the design of the complete MPPT circuit will be covered. First, in section 4.1, a high-level overview of the circuit is given, and a list of requirements is made. Here, it is also explained that the prototype will consist of three separate Printed Circuit Boards (PCBs). Then, the design and production of these three PCBs is discussed in section 4.2, 4.3 and 4.4. Finally, the set-up to test the MPPT circuit is also explained in section 4.5.

4.1. Systems Design

The first step in the design was to look at the big picture. How would the MPPT circuit fit in with the rest of the satellite? How would its different components interface with each other? How could the circuit be tested before launch? These important questions are tackled in this section. To answer them, a Functional Flow Diagram was made, based on which a set of requirements is presented in subsection 4.1.1. Afterwards, the schematic of the overall architecture of the MPPT circuit is discussed in subsection 4.1.2.

4.1.1. High-Level Requirements

Firstly, it is important to consider where the MPPT circuit will be integrated. The circuit is meant to maximise the power output of the solar cells on a PocketQube. These solar cells are the 3G30A Triple Junction Solar Cell Assembly from AZUR SPACE, shown in Figure 4.1 [46]. In addition, the satellite will have an unregulated power bus, as discussed in section 2.1. This was decided on the satellite level, before the start of this work, and thus can not be changed. The output of the MPPT circuit will be this unregulated bus, which is directly connected to the battery of the satellite. The circuit can thus be regarded as the link between the solar cells and the battery of the PocketQube. The battery will most likely consist of two supercapacitors in parallel. The current choice for these supercapacitors is the LIB1840Q4R0118 from CDA, shown in Figure 4.2 [53].

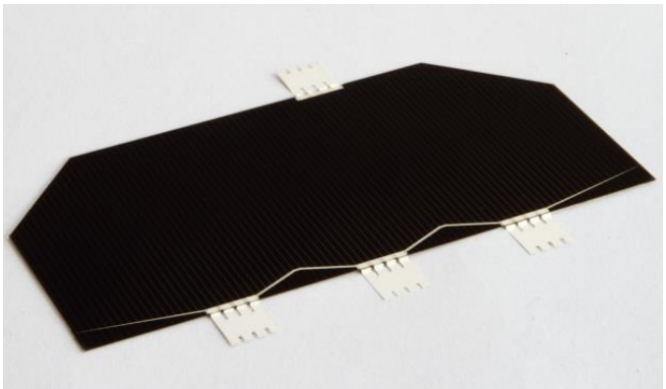


Figure 4.1: The 3G30A solar cells from AZUR SPACE that will be used on the PocketQube [46].

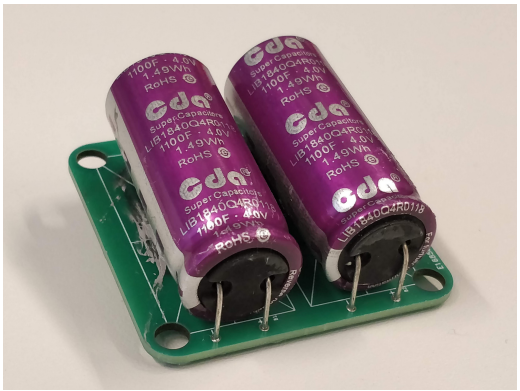


Figure 4.2: Two LIB1840Q4R0118 supercapacitors that will make up the battery of the PocketQube.

Functional Flow Diagram

Before a set of requirements for the MPPT circuit can be made, an overview of the functionality of the circuit should be considered. The main functions can be extracted from the literature study, as discussed in subsection 2.3.5. Since this circuit will be integrated into a PocketQube as mentioned above, some additional functionalities emerge. A Functional Flow Diagram that includes the general functions of the circuit is shown in Figure 4.3. The rationale for these functions can be found in Table 4.1.

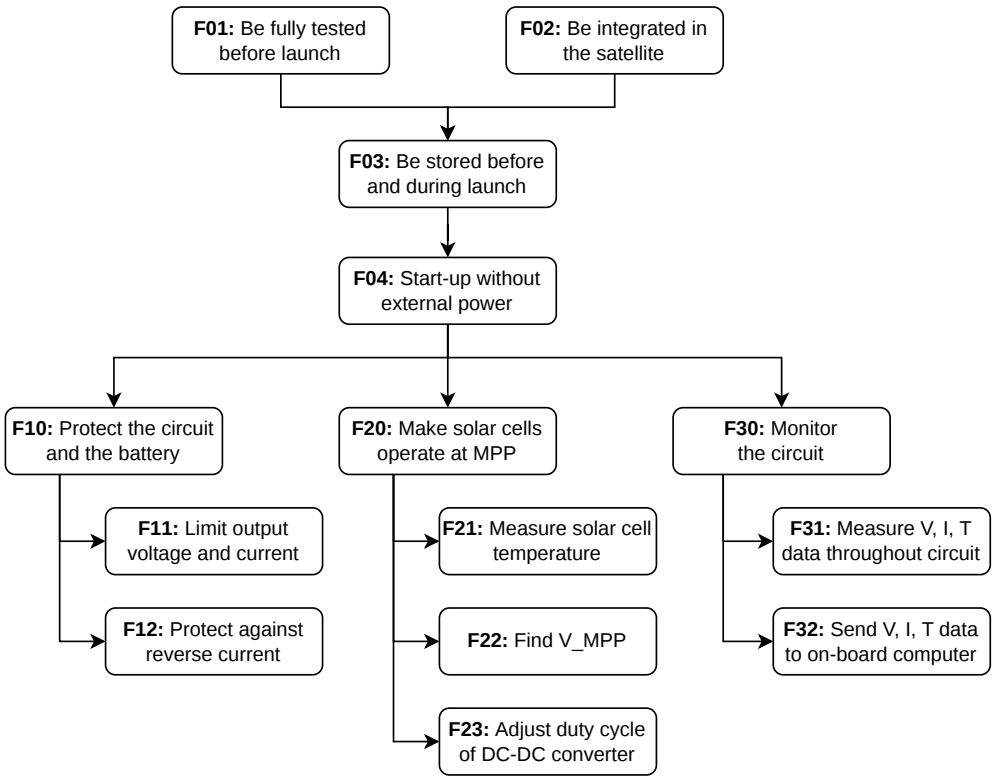


Figure 4.3: The high-level Functional Flow Diagram of the complete MPPT circuit.

Table 4.1: Rationale of each function shown in the Functional Flow Diagram in Figure 4.3.

F01	To ensure the functionality of the circuit when operational.
F02	The circuit will optimise the power generation of this satellite specifically.
F03	The satellite will be stored in the deployer for possibly several months before launch.
F04	The battery will likely be fully drained at launch.
F10	To ensure the correct operation of the power system, and therefore the entire satellite.
F11	To protect the battery of the satellite.
F12	To protect the MPPT circuit and prevent draining the battery.
F20	This is the main function of the MPPT circuit.
F21	The desired operating voltage (V_{MPP}) changes based on the temperature of the solar cell.
F22	The V_{MPP} can be calculated based on the temperature measurement.
F23	To ensure that the solar cells operate at the V_{MPP}.
F30	To be able to diagnose the circuit and debug possible problems.
F31	To measure the data that can show whether or not the circuit operates nominally.
F32	To allow the desired data to be eventually sent to ground stations.

Circuit Requirements

From the Functional Flow Diagram, a set of requirements is constructed, which can be found in Table 4.2. The requirements have a hierarchical structure starting with REQ-000, from which all requirements branch out. This hierarchy is also visible in the identifier of the requirement. Requirements with a number that is a multiple of 100 are direct children of REQ-000. All other requirements are one level lower, with their first digit corresponding to their parent. A parent requirement can only be fully met if all requirements below it are also met. To give more context for each requirement, a rationale is given for each of them. The parent requirement(s) are also given, as well as the function from the Functional Flow Diagram it is related to, if applicable.

Table 4.2: High-level requirements for the temperature-based MPPT circuit.

Identifier	Requirement	Rationale	Parent Reqs.	Verification Method
REQ-000	The TwinSat PocketQubes shall have MPPT circuits for their solar cells.	Needed to compensate for the relatively small surface area of the solar panels as compared to the electrical power requirement of the satellite.		Review of Design
REQ-100	The MPPT circuit shall optimize the efficiency of the power generation of the solar cells on the PocketQube.	This is the main goal of MPPT.	REQ-000, F20	Test
REQ-101	The MPPT circuit shall operate based on real-time voltage and temperature measurements of the solar cells.	MPPT based on temperature is more stable than P&O, which performed sub-optimally on Delfi-PQ.	REQ-100, F21, F22	Review of Design
REQ-102	For any combination of temperature and irradiance, the output power of the MPPT circuit shall be at least 80% of the theoretical maximum power produced by the solar cell(s) at that temperature and irradiance, when more power is demanded than the cell(s) can produce.	This ensures the power requirement of the satellite, which is derived from the assumed satellite power budget, is met on average.	REQ-100, F23	Test, Analysis
REQ-103	The MPPT circuit shall be able to operate within a temperature range of $-40^{\circ}C$ to $60^{\circ}C$.	Based on data obtained from Delfi-PQ, and including a margin of $4^{\circ}C$.	REQ-100	Review of Design
REQ-104	The MPPT circuit shall respond in less than $900ms$ between 10% power and 90% power produced.	The PocketQube has a maximum tumble rate of $10^{\circ}/s$, so it will go from zero to maximum irradiance in 9 seconds. A safety margin of 10 is applied to this, and it is assumed the temperature will vary slower than the irradiance.	REQ-100	Test
REQ-200	The MPPT circuit shall be integrated in the TwinSat PocketQube.	The MPPT circuit will be designed specifically to operate in this satellite.	REQ-000, F02	Test
REQ-201	The MPPT circuit shall have two versions: one compatible with one 3G30A solar cell and one compatible with two 3G30A solar cells in series.	These are the two options of how the solar cells ([46]) are grouped on the satellite, and each group will have its own MPPT circuit.	REQ-200	Test

Identifier	Requirement	Rationale	Parent Reqs.	Verification Method
REQ-202	The MPPT circuit shall send housekeeping data to the on-board computer of the PocketQube.	This data can then be sent down to the ground for checking the health and performance of the MPPT circuit.	REQ-200, F30, F31, F32	Test
REQ-203	The MPPT circuit shall have dimensions (LxWxH) of $TBD \times 20 \times 3.4mm$.	This is the available volume on the back of the satellite's solar panel PCBs. The available length is the full solar panel length minus the length of the reflector, electrical power system and battery PCBs.	REQ-200	Inspection
REQ-204	The MPPT circuit shall limit its output voltage to a maximum of $4.0V$.	This is the rated voltage of the battery (LIB1840Q4R0118 [53]).	REQ-200, F10, F11	Test
REQ-205	The MPPT circuit shall limit its output current to a maximum of $1.2A$.	In the power system, the connectors have the lowest rated current of $1.2A$.	REQ-200, F10, F11	Review of Design
REQ-206	The MPPT circuit shall have reverse current protection at its output.	This is to prevent consuming power from the battery as well as protecting the MPPT circuit.	REQ-200, F10, F12	Test
REQ-300	The MPPT circuit shall be tested on the ground using flight solar cells.	To have highly representational tests that can ensure the MPPT circuit works adequately before it is launched.	REQ-000, F01	Inspection
REQ-400	The MPPT circuit shall be able to be indefinitely stored without power while integrated in the flight-ready PocketQube.	The satellite could be stored for months at the launch provider before launch, at which point the battery will be fully drained for a long time as well.	REQ-000, F03	Test
REQ-401	The MPPT circuit shall autonomously start up after the deployment of the PocketQube.	All other systems on the satellite require power from the MPPT circuit to work, so the MPPT circuit cannot rely on other systems for a start-up signal or similar.	REQ-400, F04	Test
REQ-402	The MPPT circuit shall operate using only the power provided by the solar cells.	This includes start-up, since the batteries will likely be fully drained at launch. It is also more reliable for the circuit to not be dependent on any other system of the satellite.	REQ-400, F04	Test

4.1.2. Overall Architecture

Based on the Functional Flow Diagram and the requirements, a preliminary high-level architecture of the complete MPPT system was constructed. This architecture can be found in Figure 4.4. It is divided in three main components that correspond to the three functions F21, F22, and F23, respectively: the solar cells with their temperature measurement, the control circuit that calculates the V_{MPP}, and the DC-DC converter that ensures the solar cells operate at this V_{MPP}.

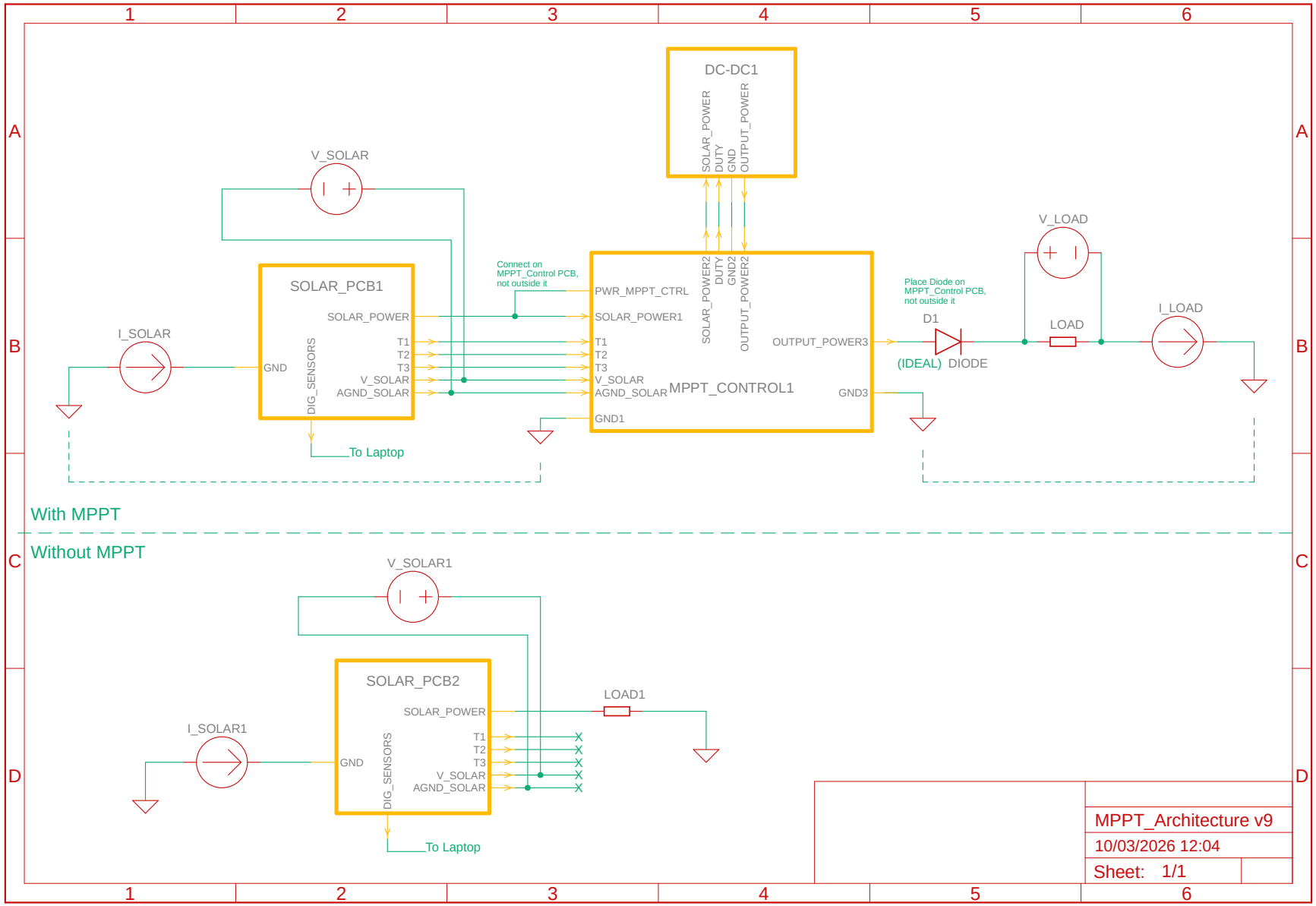


Figure 4.4: Overall Architecture of the MPPT Circuit including the solar cells and a load.

Since it is unlikely that a newly designed electronic circuit functions 100% as intended, it was anticipated that multiple versions of the circuit would have to be designed. Therefore, it is possible that earlier versions do not meet all requirements, since only the final version needs to comply with all of them. The architecture shown in Figure 4.4 is more tailored towards the first version of the circuit. The main focus of this prototype was put on its testability and ease of use, since the prototype has to be extensively tested to assess the performance of the MPPT method. This includes being able to easily make adjustments to the circuit to enhance the debugging process. This can be achieved by increasing the space between the components on the PCB so that resoldering components becomes easier. However, this can affect whether the prototype circuit meets the volume requirement (REQ-203).

In addition, a test set-up used to characterise the solar cells already exists, as will be explained in section 4.5. Ensuring that the MPPT prototype is compatible with this set-up would decrease the time required to implement the necessary modifications to the set-up. The test stand was designed to house a PCB with two solar cells on its front side. The back side is pushed against a heat sink that can cool the PCB to test at lower temperatures. This means that no electrical components can be placed on the back side. There is also little space on the front, which limits the amount of circuitry on this PCB.

Because of the reasons mentioned above, it was decided to have a modular prototype, as shown in Figure 4.4. The three modules correspond to the three main components mentioned above and will be referred to as the Solar Cell PCB, the MPPT Control PCB, and the DC-DC converter. Outside of these modules, there is an electrical (resistive) load, as well as multimeters that can measure the voltage and current, and thus the power, coming from the solar cells and going to the load. This data will be logged on a laptop in order to investigate the efficiency and feasibility of the MPPT system.

Solar Cell PCB

The first module, the Solar Cell PCB, acts as one of the exterior walls of the satellite and will thus house the solar cells. As indicated by REQ-201, the solar cells will be grouped by either one or two cells. Therefore, the Solar Cell PCB should be able to accommodate at least two cells. This PCB will also be integrated into the existing test stand, which, due to its size constraints, limits the number of solar cells to a maximum of two. Thus, the Solar Cell PCB will have exactly two solar cells. In addition, the temperature sensors required for the MPPT method will also be placed on this PCB.

The remaining area on the Solar Cell PCB is too limited to place control circuitry here. Debugging any circuitry on this PCB would also be inconvenient, since it is integrated on the test stand. Thus, all control circuitry will be placed on the MPPT Control PCB. This means that the power and data from the Solar Cell PCB need to be transferred to the MPPT Control PCB, as is also shown in Figure 4.4. In addition to the connections for the temperature sensor(s) and the solar power, two separate pins are used to measure the voltage of the solar cells from the MPPT Control PCB. Since a negligible amount of current will flow through these two pins and their respective wires, there will be essentially no voltage drop over these wires, increasing the accuracy of this so-called Kelvin voltage measurement.

An additional connector is placed on the PCB for the I2C signals coming from the digital temperature sensors. These sensors can easily read out and log the temperature of the solar cells during tests. They will be placed close to the analogue temperature sensors so that their data matches closely.

MPPT Control PCB and DC-DC converter

The second module is the MPPT Control PCB, which will be the brain of the MPPT system. It will receive the solar power and temperature data from the Solar Cell PCB, so one of its connectors will be equivalent to one of the connectors on the Solar Cell PCB. As the MPPT Control PCB requires power to perform its function, it will use some of the solar power from the same connector. In this way, it can be proven that the MPPT circuit can operate without requiring power from anywhere other than the solar cells, as is required by REQ-402.

Using the temperature and voltage data from the solar cells, the MPPT Control PCB shall find the V_{MPP} of the cells (REQ-101). In order to ensure that the solar cells operate at this V_{MPP}, a DC-DC converter is needed to adjust the resistance as seen by the solar cells, as explained in subsection 2.3.1. This will cause the solar cells to operate at a different voltage and, if managed well, at their V_{MPP}.

The DC-DC converter is the third module in the overall architecture. Whether this will be a custom DC-DC converter placed on the MPPT Control PCB, or a Commercial Off-The-Shelf (COTS) converter on a separate demo circuit board, at least for the prototype, is decided in subsection 4.3.1. In either case, it will be connected to the rest of the system only through the MPPT Control PCB. Therefore, this connection needs to include the incoming power from the solar cells, as well as the ”converted” power that comes back from the converter and that will eventually go to the load. In addition, a signal is needed that will control the duty cycle of the DC-DC converter based on the desired V_{MPP} as calculated by the MPPT Control PCB.

After the converted power arrives back at the MPPT Control PCB, it will pass through an ideal diode: this is necessary to protect the MPPT system from reverse current coming from the battery (REQ-206). An ideal diode would be preferable to a regular diode, because it has a substantially lower voltage drop of around $15mV$ instead of $700mV$ for a regular diode. This is a significant difference because the output voltage of the circuit is only $4.0V$. After going through the ideal diode, the power will flow to a final connector on the MPPT Control PCB, to which a load can be connected.

Power Measurements and Solar Cell Characterisation

To assess the feasibility of the MPPT system, it is important to measure the efficiency of the entire circuit. Therefore, the power generated by the solar cells should be measured and compared to the power going to the load. To perform these two power measurements, four multimeters are needed, since both a voltage and a current measurement are needed to calculate one power measurement. In Figure 4.4, these multimeters are called V_Solar and I_Solar for the solar cell measurements and V_Load and I_Load for the load measurement, respectively.

As mentioned in subsection 2.3.5, the temperature-based MPPT method depends on the linear relation between the V_{MPP} of the solar cells and their temperature. This relation can usually be found on the datasheet of the solar cells. However, it is beneficial to confirm this relation experimentally because variations between cells can exist. This was achieved in previous work [39] by connecting a variable resistive load directly to the solar cells and performing a sweep through various resistances.

To actually obtain the temperature relation, multimeters are needed to measure the power from the solar cells. These can be the same multimeters that are used to obtain the efficiency of the MPPT circuit. This can also be seen in the bottom of Figure 4.4, which shows the architecture needed to perform this characterisation of the solar cells.

4.2. Solar Cell PCB

The first PCB that will be designed is the Solar Cell PCB, which houses the solar cells and temperature sensors. In subsection 4.2.1, the design of this PCB is explained, including the interfaces with the rest of the circuit. Afterwards, in subsection 4.2.2, the production of this PCB is covered. The technique for attaching the solar cells to the Solar Cell PCB is also shown there.

4.2.1. Design of Solar Cell PCB

As mentioned in subsection 4.1.2, the Solar Cell PCB will have two solar cells. However, the MPPT circuit should be compatible with two cells in series, as well as one cell on its own (REQ-201). Therefore, the Solar Cell PCB will allow testing in three different configurations. In one configuration, only the left solar cell provides power. In the second, the solar cells are connected in series and both provide power. The 3rd configuration only has the right solar cell connected.

Temperature Measurement

For each configuration, the temperature of the corresponding solar cell(s) should be measured as closely as possible. Therefore, it was decided to put three temperature sensors on the PCB: one to the left of the left cell, one between the cells, and one to the right of the right cell. This setup was chosen because it allows for flexibility: the three sensors are located over the entire width of the PCB. In addition, both solar cells have two temperature sensors that are positioned close to them. This can be useful in multiple cases. In the lab setup, the sensors can be checked against each other to make sure they give reliable data. On the satellite, this allows for redundancy. This could also decrease the impact of a temperature gradient across a solar cell. By averaging the signal from the sensors surrounding the cell, the average temperature of the cell can be obtained.

The temperature sensors need to match the temperature of the solar cells as closely as possible. Therefore, the sensors will be placed close to the solar cells, on the outside of the satellite. Thus, they will be subjected to the harsh environment of outer space, with nothing in the way to protect them. This limits the number of viable types for the sensor. There are highly linear devices that would be easy to implement, such as the LMT87-Q1 from Texas Instruments (TI) [54]. However, these are active devices that are more susceptible to failures due to radiation [55]. Therefore, it was decided to instead use passive temperature sensors: thermistors.

For a given configuration, not all temperature sensors can provide useful data. For example, when testing only the left solar cell, the temperature sensor all the way on the right of the Solar Cell PCB is not relevant. Therefore, each configuration has their own subset of temperature sensors that will be read out. These include the two sensors that surround the connected solar cell(s), which can be useful

Table 4.3: Overview of the connected temperature sensors for each configuration.

Configuration	Temperature Sensor 1 (Surrounding Left)	Temperature Sensor 2 (Closest to Cell(s))	Temperature Sensor 3 (Surrounding Right)
Left Solar Cell	Left Sensor	Left Sensor	Middle Sensor
Both Solar Cells	Left Sensor	Middle Sensor	Right Sensor
Right Solar Cell	Middle Sensor	Right Sensor	Right Sensor

to obtain the average temperature across the cell. In addition, the sensor closest to the corresponding cell will also be read out. An overview of which temperature sensor is connected for each configuration is given in Table 4.3.

Selecting the Configuration

All three configurations should be tested, and switching between the configurations should therefore be convenient to facilitate the testing process. One option is to have all the necessary connections for all three configurations in one connector on the PCB. Then, for each configuration, a separate cable is made that only connects to the relevant pins for that configuration. The other side of this cable then connects to the MPPT Control PCB. In this way, the desired configuration can be selected by simply connecting the Solar Cell PCB to the MPPT Control PCB with the correct cable.

Another option is to have three separate connectors, each with the same number of pins, on the Solar Cell PCB: one for each configuration. Then, by careful design of the pinout of these three connectors, only one cable is needed between the Solar Cell PCB and the MPPT Control PCB. Therefore, by simply connecting this cable to the correct connector, the desired configuration and its required connections can be selected. The three connectors would be placed in logical locations on the Solar Cell PCB: the connectors for the one-cell configurations would be placed on the same side as their respective solar cell. The connector for the two cells in series would be placed in the middle of the PCB.

Both options are convenient and do not require much time to switch between configurations. However, for the first option, it is difficult to differentiate between the different configurations by simply looking at the test setup. Furthermore, a problem could arise in case there is a difference between MPPT Control PCBs when dealing with one cell as compared to two cells in series. In this scenario, a cable meant for a single cell configuration could accidentally be connected to a MPPT Control PCB meant for two cells in series, which could harm the circuitry. Something similar could also happen with the second option by connecting the cable to the wrong connector. However, because of the location of the connectors on the PCB, it is visually easier to notice this possible mistake and correct it before any harm occurs. Therefore, it was decided to implement the second option.

Schematic of the Solar Cell PCB

The schematic of the Solar Cell PCB can be found in Figure 4.5. In the top left of the schematic, the three connectors for the three configurations are shown. Each 10-pin connector, which is from the Hirose DF52 Series [56], follows the same logic for its pinout. Pins 1 and 10 connect to the power and ground of the respective solar cell(s). As can be seen in the bottom left of Figure 4.5, the solar cells are always connected in series to each other. Thus, for the configurations where only one cell is connected, the other cell is left floating. Pins 2 and 9 also connect to the power and ground of the cells, but these connections are meant for the Kelvin measurement of the cells. Therefore, they will split off from the actual power path as close to the cells as possible to obtain the most accurate measurement.

The remaining pins are used to connect the relevant temperature sensors, as shown in Table 4.3. As explained above, the temperature sensors will be thermistors, which means that they each have two terminals. Therefore, each temperature sensor uses two pins of the connector, so that all thermistor terminals have a direct connection to the MPPT Control PCB. This allows for more flexibility in the integration of the thermistors into the control circuit. Since it is not yet known exactly which thermistor will be used, a common ”0603” size was selected as a placeholder.

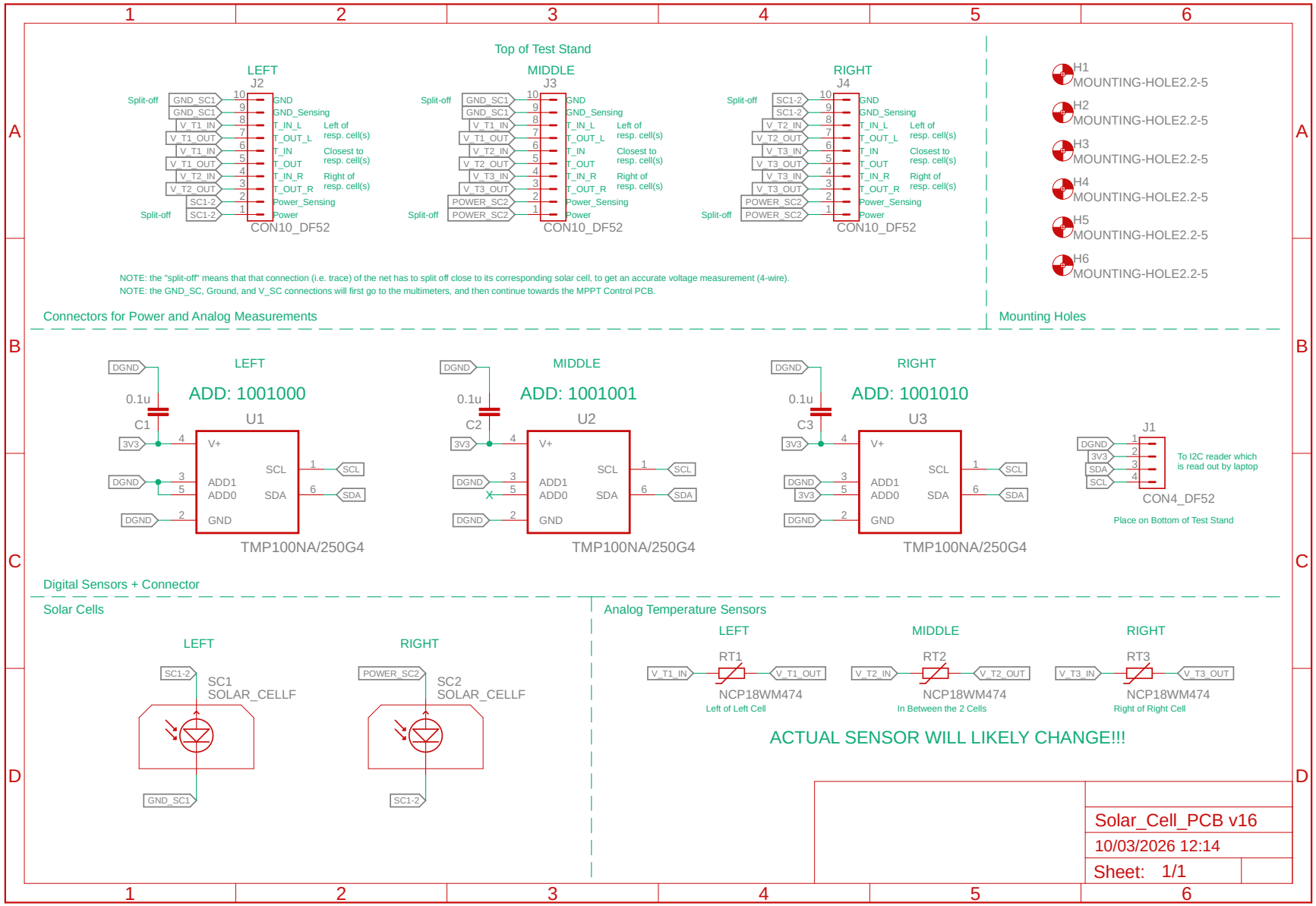


Figure 4.5: Schematic of the Solar Cell PCB.

In the middle of Figure 4.5, the TMP100 digital temperature sensors are shown [57]. As discussed in subsection 4.1.2, they will be placed close to the thermistors so that they are representative of each other. These digital sensors were selected because they have flown on Delfi-PQ and are thus proven to work. In order to read out these sensors, a separate 4-pin DF52 connector [56] is added to the schematic. This connector provides power to these sensors and also has two pins to send the I2C signal out of the PCB. These devices also need different addresses so that the I2C bus can differentiate between them. This is achieved by having different connections to the ADD0 and ADD1 pins for each sensor.

Layout of the Solar Cell PCB

With the schematic now completed, the layout of the Solar Cell PCB could be made. This can be found in Figure 4.6, rotated $90°$ clockwise to fit better on the page. The size of the PCB is mainly determined by the solar cells since two cells need to fit. However, the test stand also limits the size and dictates the placement of the mounting holes, leading to a small available area around the solar cells. This is similar to the flight version of the Solar Cell PCB, which will also have limited space. Fortunately, only connectors and thermal sensors need to be placed next to the solar cells, so all components still fit on the front side of the PCB, which is $190mm$ x $55mm$. As explained above, the thermistors and digital temperature sensors are placed around the cells at the edges of the PCB, as well as in the middle between the cells.

The three connectors used to switch between configurations are placed at the top of the Solar Cell PCB (at the right of Figure 4.6). To minimise traces that cross each other, the digital connector is placed at the bottom of the PCB. In this way, the digital nets occupy the bottom half of the PCB, while the analogue nets occupy the top half. Some traces between the solar cells and the three connectors at the top are made wider to decrease the temperature rise because they carry the full current of the solar cells. These traces are $1.27mm$ wide, which, according to the IPC-2221A standard [58], leads to a temperature increase of only $0.93°C$ with a current of $1A$, which is almost double the current that the solar cells can produce.

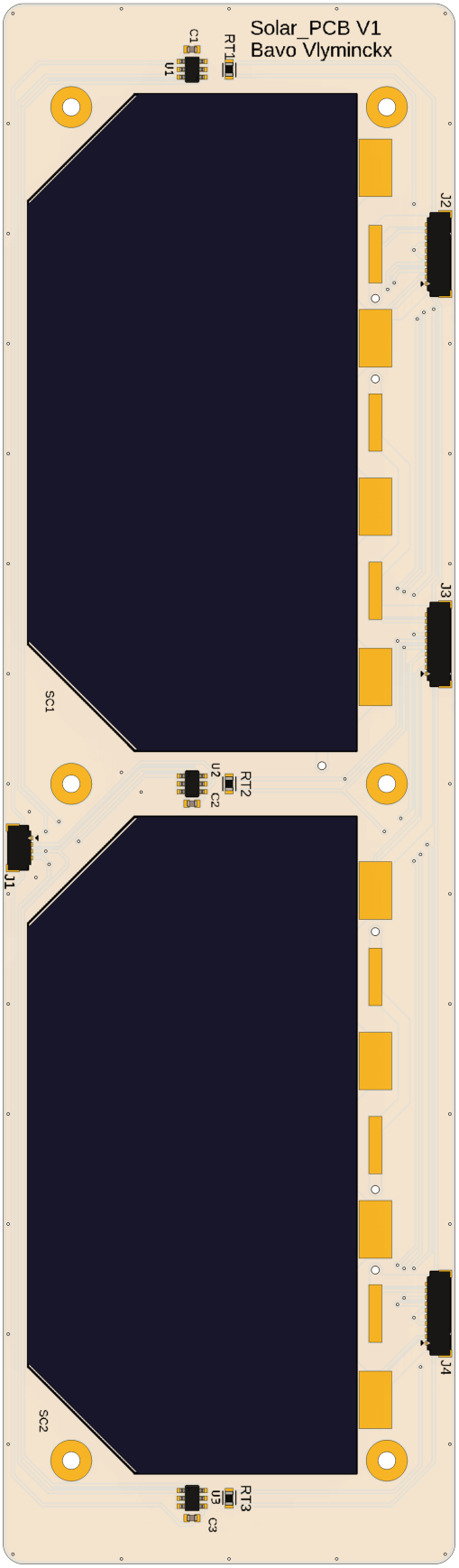


Figure 4.6: Layout of the Solar Cell PCB.

The Solar Cell PCB also has a ground plane on both copper layers. This ground plane connects to the digital ground and is meant to decrease the noise on the PCB. Another strategy to reduce noise is via fencing. Here, vias are placed around the edge of the PCB in regular intervals to block electromagnetic interference. A general rule of thumb is to space the vias at 1/10th of the wavelength of the interference, or less. In this case, the interference comes mainly from the satellite radio transmitter, which operates at $430MHz$. This results in a wavelength of $\sim 700mm$, and thus a via spacing of less than $70mm$.

4.2.2. Production of Solar Cell PCB

After the layout of the Solar Cell PCB was completed, the PCB could be ordered, as well as the components that will populate it. Since the Solar Cell PCB only has a small number of components, they were soldered by hand. However, attaching the solar cells is not as simple as soldering their connectors to the correct pads on the PCB. The connectors are not robust and are placed only on one side of the cells. Thus, the rest of the cell should also be structurally attached to the PCB.

Attachment Technique for Solar Cells

A new technique was tried to bond the cells to the Solar Cell PCB using double-sided tape, specifically CV4-1161-5 tape from NuSil Technology [59]. This technique first needed to be tested on spare or broken cells to gain confidence in the process. For this, a hard sheet of see-through plastic was used. This allowed for a clear view on either side of the tape to see if bubbles of air were trapped. These bubbles are highly undesirable because they reduce the bonding force and locally reduce the thermal dissipation from the solar cell to the PCB underneath it, which could cause hotspots. In addition, these bubbles could rupture in the vacuum of space, which could damage the solar cells.

The first tests included taping two pieces of hard plastic to each other for an even better visual on the tape. Afterwards, broken cells from previous projects were taped on the same large sheet of plastic, as can be seen in Figure 4.7. The first step was to apply the tape to the solar cell. The tape was applied starting from a corner, as shown in Figure 4.8, and was slowly pushed down and away from this corner. In this way, possible air bubbles could be pushed away during the application of the tape. Then, the solar cell with the tape was taped on the larger sheet in a similar manner: starting from a corner and pushing air bubbles away while pushing down. This second step was performed with minimal bending because the solar cells are not highly flexible.

Figure 4.7: All tests performed on a see-through plastic sheet to verify the use of double-sided tape to bond solar cells to a PCB.

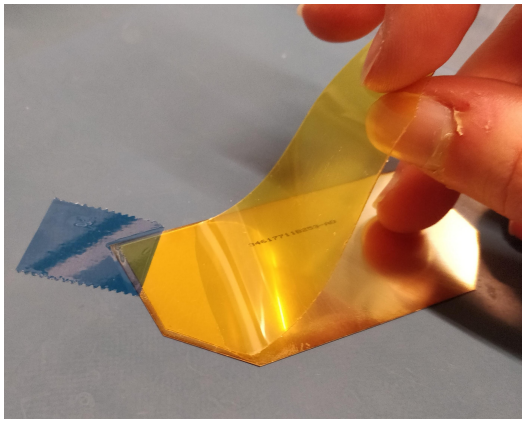


Figure 4.8: Process of applying the double-sided tape to a solar cell.

When taping the small pieces of plastic to the larger sheet, almost no bubbles were observed. This is likely due to the flexibility of the plastic: it could be bent more, making it easier to push away possible air bubbles. In addition, more pressure could be applied to push away the bubbles, because the plastic does not break easily. More care needed to be taken when taping the solar cells because they will crack when bent too much or when too much pressure is applied.

The result of the taping of four cells is shown in Figure 4.9. Some air bubbles appeared, which are highlighted with the red circles. The two cells at the bottom of the figure were taped first. They show various bubbles, which appear mainly at the edges of the tape. This is caused by the tape being cut to the correct shape using scissors. This leads to a rough edge of the tape, allowing air to enter from these edges. It is therefore recommended to cut the tape using a sharp knife. Another factor contributing to the bubbles is dirt being present on the cells. The two cells at the top of the figure were cleaned before the tape was applied, significantly reducing the number of bubbles.

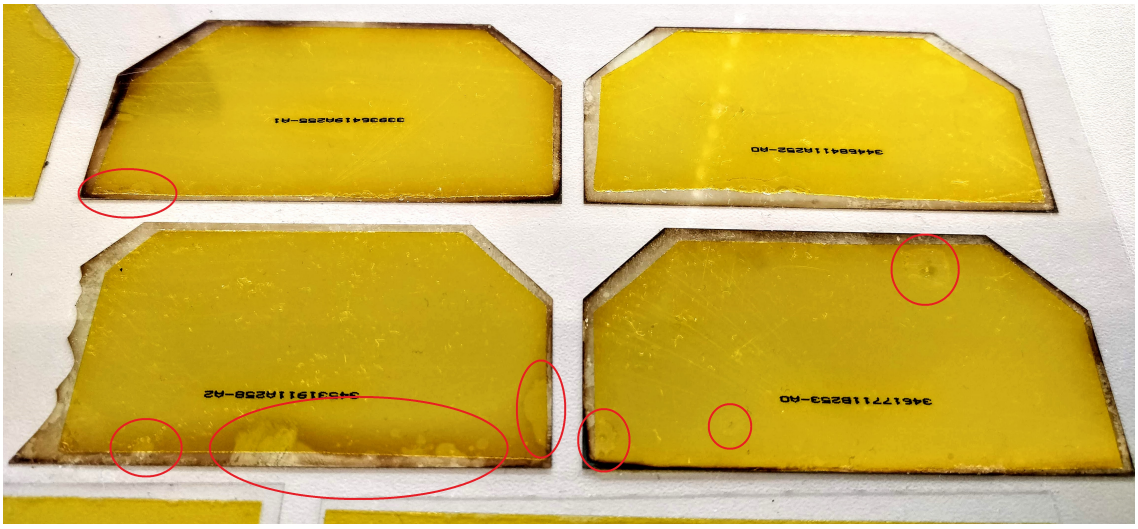


Figure 4.9: Air bubbles are visible under the double-sided tape between the solar cells and the plastic sheet.

Assembly of the Solar Cell PCB

After confidence in the technique was gained, it was time to bond the solar cells used for the test setup to the Solar Cell PCB. These cells are the same type as those that will fly on the satellite: the 3G30A cells from AZUR SPACE [46]. They come with four connectors: one for a bypass diode and three that connect to the ground of the cells. The back of the cell is made of metal and is the power connection of the cell.

As can be seen in Figure 4.6, all connectors for the solar cell are located above the cell. The three ground connectors of the cells correspond to three of the pads on the Solar Cell PCB. However, the connectors are too long and are therefore cut shorter, as shown in Figure 4.10. The parts of the tabs that are cut are then soldered at two locations on the back of the cells to make a power connector. This is achieved by applying some solder paste on the back of the solar cell, specifically RA 10 SN62BAS86 10K 25G solder paste from Henkel Corporation [60]. The tabs are then placed on top of the paste, after which heat is applied using a soldering iron to melt the solder paste. This is shown in Figure 4.11. These new connectors line up with the power pads on the Solar Cell PCB. The bypass connector is not needed and is therefore removed completely.

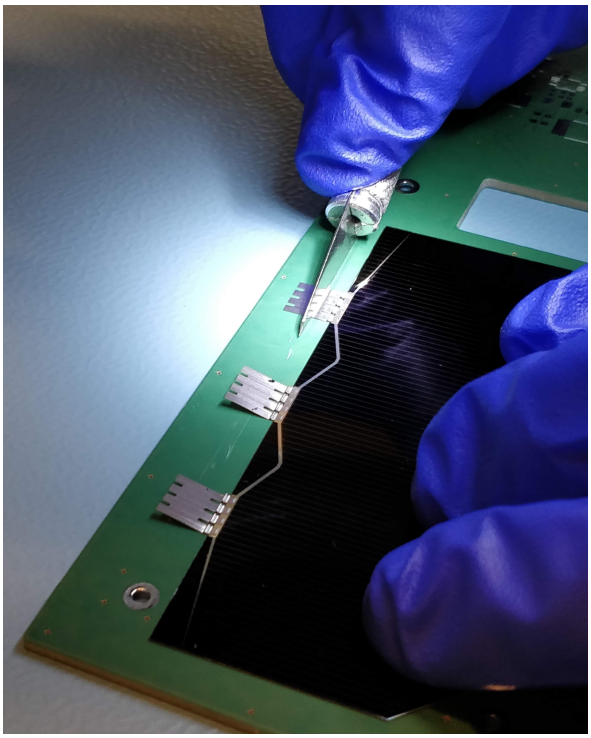


Figure 4.10: The connectors of the solar cells are cut shorter.

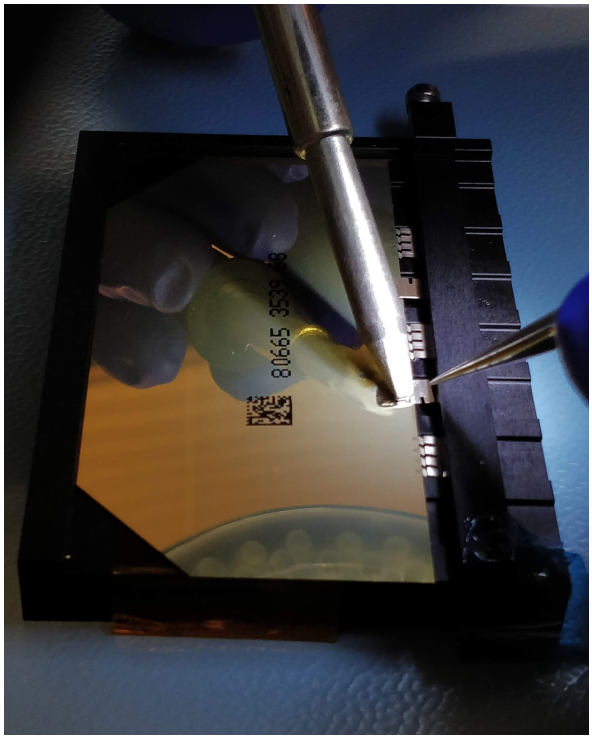


Figure 4.11: Soldering power connectors for the solar cells.

With the correct connectors that match the Solar Cell PCB, the cells can be taped. A small cut-out is made in the tape around the power connectors so that the tape is only applied to the flat backside of the cells. Then, with the technique explained above, the cells are bonded to the PCB. After the cells are taped, the connectors are soldered to their corresponding pads. At this point, it was realised that a wrong footprint for the cells was selected in the PCB design software, leading to smaller ground pads. All connectors could still be soldered to the pads, but it is advised for future PCBs to select a footprint with larger ground pads for easier manufacturing. A picture showing the assembled Solar Cell PCB is shown in Figure 4.12.

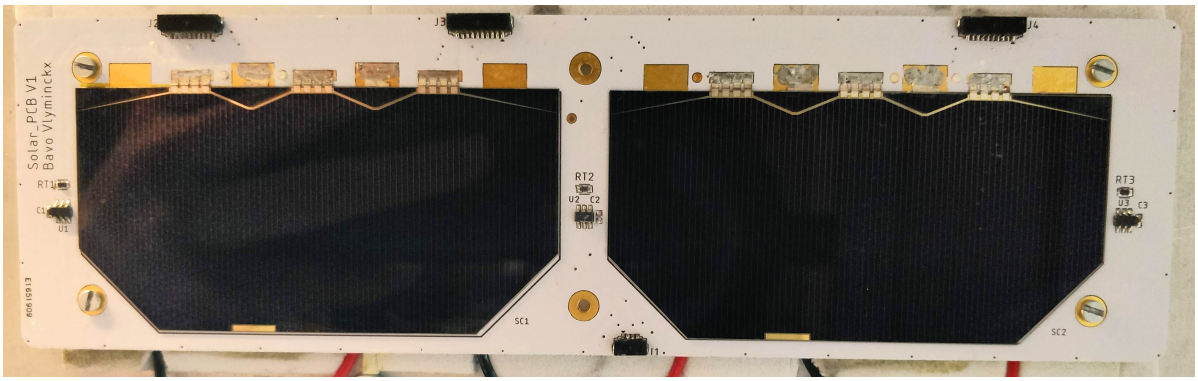


Figure 4.12: The fully assembled Solar Cell PCB, which is here bolted to the test set-up.

4.3. DC-DC Converter

With (the first version of) the Solar Cell PCB designed and assembled, two large parts remain to be designed: the MPPT Control PCB and the DC-DC converter. First, the design of the converter was considered, because the way it is controlled can have a significant impact on the design of the MPPT Control PCB.

As mentioned in subsection 4.1.2, the main function of the DC-DC converter is to ensure that the solar cells operate at the V_{MPP} by effectively altering the resistance as seen by the solar cells. It should be possible to control this behaviour of the DC-DC converter from the MPPT Control PCB. The DC-DC converter also needs to be compatible with the voltages seen in the rest of the circuit. In addition, the efficiency of the DC-DC converter should be high enough so that the overall efficiency of the circuit remains above 80% while complying with all other requirements set in subsection 4.1.1.

Firstly, the type of DC-DC converter that is most suitable for this application is determined in subsection 4.3.1. Then, the inner workings of an initial device is investigated in subsection 4.3.2. Afterwards, the compatibility of this device is discussed in subsection 4.3.3, and a solution to the compatibility issues is proposed. Finally, in subsection 4.3.4, the integration of the selected DC-DC converter into the rest of the circuit is discussed.

4.3.1. DC-DC Converter Topology

There are three main types of DC-DC converters: the Buck, Boost, and Buck-Boost converters. In essence, the Buck converter has a high voltage on its input, which is converted to a lower voltage on its output. Since power (without losses) stays constant and $P = V \cdot I$, the current at the output will be higher than at the input. On the other hand, a Boost converter has a higher voltage, and thus lower current, on its output as compared to its input. Finally, a Buck-Boost converter can achieve both a higher and a lower voltage at its output as compared to its input.

As mentioned in subsection 4.1.1, the MPPT circuit will be the link between the solar cells and the battery of the satellite. Therefore, the main DC-DC converter of the circuit needs to be compatible with the voltages of both of these components. Firstly, the battery of the next Delfi satellite will consist of two LIB1840Q4R0118 supercapacitors connected in parallel. This means that the battery, which is essentially the output of the DC-DC converter, will operate between $2.7V$ and $4.0V$ [53]. Secondly, the satellite will have the 3G30A solar cells from Azur Space. These cells have a V_{MPP} of $2.409V$ at $28°C$ and a temperature gradient of the V_{MPP} of $-6.7mV/°C$ [46]. Based on data from previous missions, the operating temperature of the solar cells can swing significantly from $-40°C$ to $60°C$ (REQ-103). This means that the operating voltage of the solar cell, which is essentially the input voltage of the DC-DC converter, can be anywhere between $\sim 2.2V$ and $\sim 2.9V$.

Thus, in the configuration with one cell, the input voltages are lower than the maximum output voltage of $4.0V$, so the DC-DC converter should be able to boost its input voltage. In addition, the highest possible input voltage ($2.9V$) is higher than the minimum output voltage ($2.7V$), so the DC-DC converter should also be able to decrease its input voltage, although only slightly. Therefore, a buck-boost converter would be ideal, but perhaps a boost converter could also work.

However, in the case of two cells, the input voltage is doubled and will be between $\sim 4.4V$ and $\sim 5.8V$. These voltages are higher than the maximum output voltage of $4.0V$, so in this case the

DC-DC converter has to decrease its input voltage. In order to keep the design process simple, it would be beneficial to have a similar design for both the one-cell and the two-cell configuration. Therefore, as a starting point for the design, a Buck-Boost converter will be used since this type of converter can be used in both cases under all conditions.

Custom versus COTS DC-DC Converter

After determining the type of DC-DC converter, the next step in the design is to determine how this DC-DC converter can be controlled so that it forces the solar cells to operate at the desired voltage. One option is to design a DC-DC converter from scratch. This would allow for 100% flexibility in the overall design, and would allow for direct control of the duty cycle of the converter.

As explained in subsection 2.3.5, the required (change in) duty cycle can be obtained relatively easily: one way is to find the difference in actual and desired voltage around the solar cells. Multiplying this difference with a scaling factor already results in a desired change in duty cycle. Careful tuning of this scaling factor is required to avoid too slow convergence, or overshooting of V_{MPP} and oscillations around the V_{MPP}.

Another method allows for a direct calculation of the desired duty cycle. Here, the desired gain of the converter, which is defined as the output voltage divided by the input voltage, is first calculated. The input voltage is the desired V_{MPP}, while the output voltage can be obtained by measuring the voltage across the load. When the DC-DC converter topology is known, the relation between the gain and the duty cycle is also known [7]. Therefore, the duty cycle can be obtained directly. A more in-depth explanation of these two methods can be found in subsection 2.3.5.

It is feasible to implement these methods to control a custom DC-DC converter. The second method would likely require a microcontroller to solve the equation to calculate the desired duty cycle, which would increase the complexity. However, designing a custom DC-DC converter from scratch would be a difficult task in itself [61]. Considering the time frame of the thesis and all other tasks that have to be performed, it was deemed not feasible to also design a custom DC-DC converter.

4.3.2. Initial DC-DC Converter

Since a custom DC-DC converter was excluded as an option, a COTS converter will be used. In previous work [39], the LTC3119 Buck-Boost converter [62] was investigated. This converter has a wide input and output voltage range, making it compatible with the the battery (REQ-204). Furthermore, it can handle currents of well over $0.5A$, making it compatible with the solar cells [46]. It can also achieve efficiencies of more than 90%, which can result in a high efficiency of the entire circuit (REQ-102). In addition, it has a built-in Maximum Power Point Control (MPPC) function, which will be explained below. In short, this function could significantly reduce the complexity of the control circuit. For these reasons, the LTC3119 will be considered as a first option for the DC-DC converter of this MPPT circuit.

Internal Control of the LTC3119's Gain

The block diagram of the LTC3119 can be found in Figure 4.13. In the top right of the diagram, between pins SW1 and SW2 (indicated by ”1”), the inductor of the DC-DC converter is placed. Below that, four switches (”A”, ”B”, ”C”, and ”D”, located around ”2”) can be found that control the current flowing through the inductor and towards the output. Varying the duty cycle of these switches changes the gain of the converter [62].

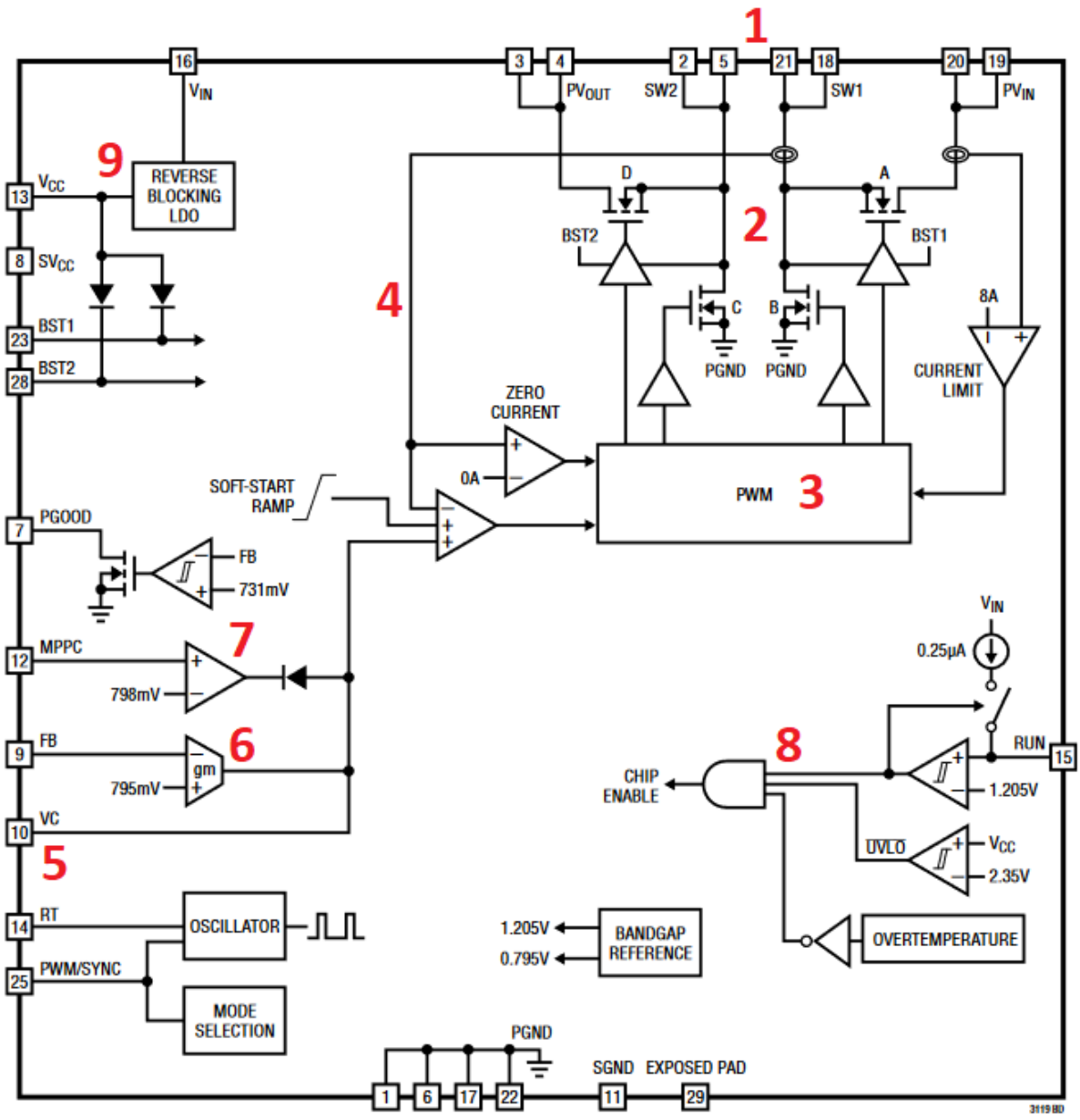


Figure 4.13: Block diagram of the LTC3119 Buck-Boost Converter [62].

The Pulse Width Modulator (”3”), or PWM for short, which is located below the switches, controls the duty cycle of the switches based on an internal average current control loop [62]. The feedback line of this control loop is indicated by number ”4”. Correctly driving this PWM is key to ensuring that the solar cells work at their V_{MPP}. In addition to the feedback line, the PWM is internally directed by a current limit, reverse current protection, and a soft start during the device start-up [62].

The only external access to the PWM is through the VC pin (”5”) of the LTC3119. The voltage at this pin therefore controls the average current through the inductor: the higher the VC pin voltage, the higher the commanded inductor current [62]. Since solar cells are a resistive source, increasing the inductor current reduces the voltage across the cells. Therefore, increasing the VC pin voltage decreases the solar cell voltage, and vice versa. The VC pin is normally only used for compensation of the control loop of the DC-DC converter, but it could technically also be used to directly control the gain.

External Control of the LTC3119's Gain

Instead of controlling the gain through the VC pin, it is usually controlled through two different pins: the Feedback (FB) and MPPC pins. The FB pin is designed to set the desired output voltage. This can be achieved using a simple voltage divider between the output power line of the DC-DC converter and the FB pin, as shown in Figure 4.14.

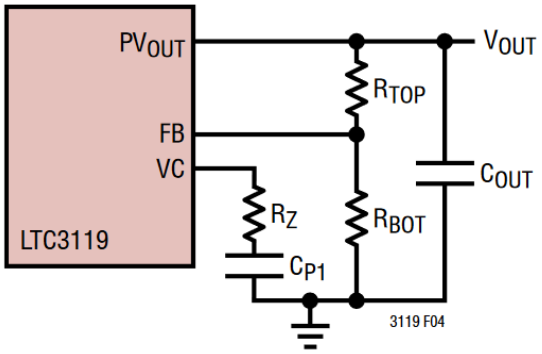


Figure 4.14: A voltage divider between the output voltage and the FB pin of the LTC3119 sets the desired output voltage [62].

Inside the device, the voltage at the FB pin is connected to the negative (inverting) input of a transconductance amplifier (”6” in Figure 4.13). Here, the voltage is compared to a constant voltage of $795mV$. If the FB pin voltage is below $795mV$, the output of the transconductance amplifier is positive. Since this positive output is connected to the VC pin, the VC voltage increases. A higher VC voltage results in a lower input voltage, but also a higher output voltage. Essentially, the gain of the converter increases. The higher output voltage results in a higher FB pin voltage through the voltage divider, until the FB pin voltage reaches $795mV$ again. In case the FB pin goes higher than $795mV$, the opposite happens, and the output voltage is decreased accordingly.

The MPPC pin works in a relatively similar manner. As shown in Figure 4.15, a voltage divider is placed between the input power line and the MPPC pin. So, instead of regulating the output voltage, this pin regulates the input voltage. Therefore, this pin is instead connected to the positive (non-inverting) input of the amplifier (”7” in Figure 4.13). In this way, if the input voltage drops too low, the MPPC pin voltage also drops below the $798mV$ that it is compared to. This results in a drop in the VC voltage, which in turn causes the input voltage to increase again to the desired value. In essence, this decreases the gain of the converter.

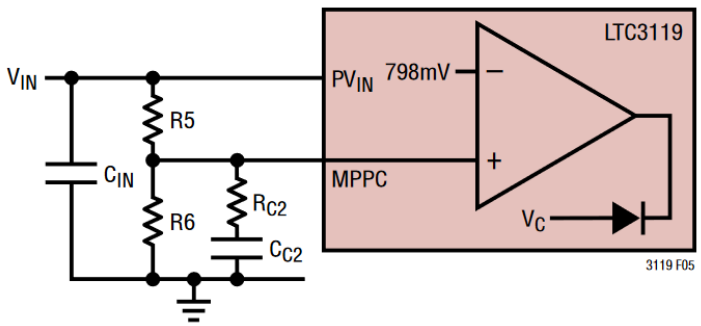


Figure 4.15: A voltage divider between the input voltage and the MPPC pin of the LTC3119 sets the desired input voltage [62].

Difference between the FB Pin and MPPC Pin

One major difference between the operation of the FB pin and the MPPC pin is the diode between the MPPC amplifier and the VC pin. When the voltage at the MPPC pin is higher than $798mV$, the output of the MPPC amplifier will be positive. However, the diode will block any current flowing to the VC pin, which means that the MPPC pin does not have any effect on the gain when the input voltage is above the programmed input voltage. The MPPC function will only become active when the input voltage is too low. This essentially means that the MPPC function acts as a lower limit for the input voltage.

The result of this lower limit can be shown by looking again at the P-V diagram of a solar cell, found in Figure 4.16. Firstly, when no load is attached to the output of the DC-DC converter, the FB pin will still force $4V$ on the output. When looking at the operating point of the solar cell, it will be close to the open circuit point (V_{OC}) in the bottom right of the P-V graph. It will not be exactly at this point since the DC-DC converter will still consume some power to regulate the output voltage.

When the load resistance decreases, the FB pin will continue to regulate the load voltage to $4V$. Since $I = U/R$, the output voltage stays constant, and the resistance decreases, the load current will increase, as will the required power. Due to the increase in current at the output, the average inductor current that runs through the DC-DC converter should increase, and therefore the solar cell should also produce more current. Again, since a solar cell is a resistive source, its voltage will drop because of the increased current. Therefore, on the I-V curve and also the P-V curve, the operating point will move up (more current/power) and slightly to the left (lower voltage). As long as the solar cell voltage remains above the programmed lower limit for the input voltage of the converter, the MPPC function will not be active. Therefore, as long as the solar cells operate in the green part of the curve shown in Figure 4.16, the FB pin will be the main driver.

If the required output power keeps rising (i.e. load resistance keeps decreasing), the operating point will continue to move up and to the left until the solar cell voltage drops so low that the MPPC function will take over. In the datasheet of the LTC3119, it is stated that the MPPC function has priority over the FB function [62]. Therefore, it is impossible to lower the input voltage below the programmed value. Thus,

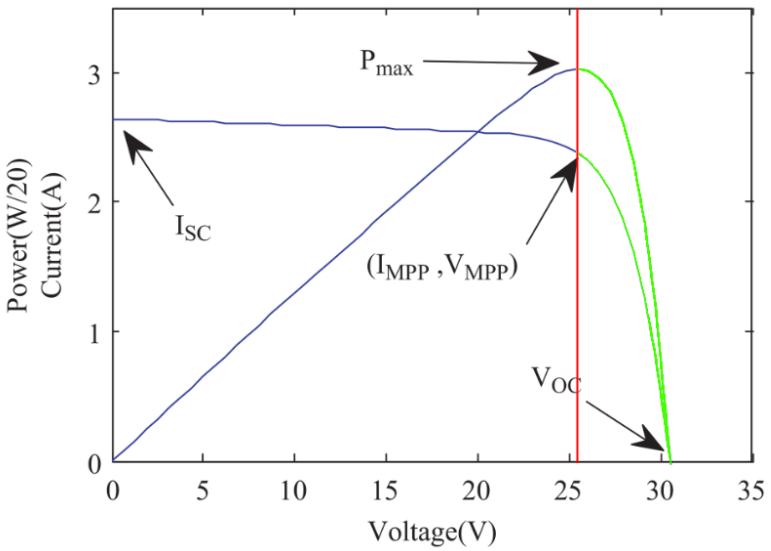


Figure 4.16: P-V curve of a solar cell showing the operating points when limited by the MPPC function [23].

if the MPPC voltage divider is set so that the lower limit of the input voltage corresponds exactly to the V_{MPP}, the solar cells will continue to produce the maximum amount of power, even if the output power keeps increasing beyond what the solar cells can produce. In this case, the lower limit, represented by the red line on Figure 4.16, prevents the operating point from moving further to the left when the load demands more power. If the MPPC function would not be present, the operating point would be pushed further to the left beyond the MPP. In this case, the solar cell voltage would continue to decrease, causing an undesired decrease in the power generated by the cells.

When the MPPC function is active, the input power to the DC-DC converter stays constant. Therefore, the output power cannot increase any further, even if the output resistance continues to decrease. Since the output power stays constant but the resistance decreases further, the output voltage will start to drop, while the output current will continue to increase. This can be derived from the following power equations: $P = U^2/R$ and $P = I^2 \cdot R$. To keep the power constant while decreasing the resistance, the voltage can compensate by decreasing too, while the current compensates by becoming larger.

4.3.3. Problems with the Initial DC-DC Converter

The LTC3119 is rated for input voltages ranging from $2.5V$ to $18V$. In addition, it is stated that after start-up, the input voltage can drop as low as $250mV$. This is somewhat confusing information. Looking again at Figure 4.13 next to number ”8”, there are only three requirements necessary to enable the DC-DC converter: the temperature should be within the operating range, the RUN pin voltage should be above $1.205V$, and the VCC voltage should be at least $2.35V$. As long as these three conditions are met, the input voltage (PV_{IN}) can be as low as $250mV$, even during start-up.

The reason the datasheet [62] states that the input voltage can only go down to $250mV$ ***after*** start-up, is because it is assumed that V_{IN} is connected directly to PV_{IN}. In this case, the voltage at V_{IN} should be at least $2.5V$ before the VCC voltage reaches the required $2.35V$. This is because VCC is powered by V_{IN} through an internal Low-Dropout (LDO) regulator (”9” on Figure 4.13), which can have a dropout voltage of up to $150mV$ [62]. Then, the datasheet proposes to bootstrap the VCC voltage from the output of the DC-DC converter. In this way, the VCC voltage can be maintained above $2.35V$, but only after start-up when the output voltage is high enough.

Fortunately, these assumptions made by the datasheet do not have to be followed. If V_{IN} is not directly connected to PV_{IN}, it is possible to have different voltages at these pins. Therefore, if V_{IN} is supplied with $2.5V$ or more at all times (and the RUN pin voltage is greater than $1.205V$), PV_{IN} can drop down to $250mV$, also during start-up. In this case, bootstrapping VCC is also not necessary.

This detail is important, since in the case of one solar cell, the input voltage could drop below $2.5V$. The requirements state that the MPPT circuit should be able to fully power itself, even in the case of one cell (REQ-402). As explained above, the PV_{IN} voltage can be below $2.5V$ at all times if necessary. However, one problem remains: how to ensure that V_{IN} is above $2.5V$, even when the solar cell operates below that voltage?

Proposed Solutions

Multiple options were considered to solve the problem of needing a voltage above $2.5V$. The first option is to find a different DC-DC converter altogether. In this case, a converter with a lower required input voltage should be found that either has an MPPC pin (or similar), or has its VC pin (or similar)

exposed so that the MPPC functionality can be recreated using external components. The second option involves splitting the power coming from the singular solar cell into two paths: one path continues without modifications toward the input (PV_{IN}) of the LTC3119, while the other path can be boosted to a higher voltage to power the V_{IN} pin of the converter. This can be achieved in two ways: using a charge pump, or using a small DC-DC boost converter with an inductor.

A charge pump is a type of DC-DC converter that uses capacitors as energy storage elements instead of inductors [63]. Some charge pumps can only invert their input voltage, or only double it, and thus do not regulate their output voltage. However, other devices do have a regulated output, similar to inductor-based DC-DC converters. Both types of charge pumps will be considered as an option to boost the voltage to power the V_{IN} pin. For the unregulated charge pumps, the voltage doubler pumps in particular will be considered. This is because when the solar cell voltage would be doubled, it would be exactly the same as in the two-cell configuration, increasing the similarity between the two circuits.

Trade-off between the Proposed Solutions

All five options mentioned above were investigated, and a search was performed for the components required for these options. Afterwards, a trade-off was performed between the proposed solutions. The trade-off criteria are the complexity of the implementation of the solution, the availability of the required components on the market, the overall power consumption of the solution, and the volume required to fit all components. These criteria are scored relative to the circuit for the two-cell configuration. The qualitative result of the trade-off can be found in Table 4.4 and is discussed in more detail below the table. The colours in the table represent how well the option scores: dark green indicates the highest score, while red represents the lowest score.

Table 4.4: Trade-off between the solutions for the incompatibility of the LTC3119 with the one-cell configuration.

Solution	Additional Complexity	Availability	Additional Power Loss	Additional Volume
New DC-DC converter with MPPC pin	Very Simple	None	None	None
New DC-DC converter with VC pin only	Very Complex	Low	Low	Medium
Voltage Doubler Charge Pump	Simple	Low	High	Low
Regulated Output Charge Pump	Simple	Low	High	Low
Boost Converter with Inductor	Simple	High	Low	Medium

The ideal solution would be to find a different DC-DC converter that works at sufficiently low input voltages and has an MPPC pin. If the efficiency of this converter would be comparable to that of the LTC3119, no additional power losses would occur. Furthermore, no additional volume would have to be used for a boost converter, and the complexity would remain the same as when using the LTC3119. However, not one DC-DC converter was found with a lower input voltage than the LTC3119 while still having an MPPC pin, which means that this solution is unfortunately not possible.

Some DC-DC converters with a sufficiently low input voltage and an exposed VC pin were found, although the required output current of $0.5A$ made it more difficult. The LT3154 [64] and the LTC3113 [65] both have a similar architecture as the LTC3119 and are thus viable replacements. However, their reduced input voltage means they are not compatible with the two-cell configuration. Therefore, two different converters are needed for the two configurations, which is not ideal. Furthermore, the functionality of the MPPC pin of the LTC3119 now needs to be recreated using additional components, which take up volume and consume some power. Ensuring the stability of this custom MPPC function also dramatically increases the complexity of this solution.

A voltage doubler charge pump is simple to implement, since it consists of only one integrated circuit and some external capacitors, which also leads to a small volume. However, after an extensive search, only a few voltage doublers were found that operate at voltages below $2.5V$. Most of these, such as the MAX828/MAX829 [66] and the LTC1046 [67], require external diodes to double the voltage. Only the MAX864 [68] and MAX865 [69] can operate at voltages as low as $1.5V$ without the need for external diodes. However, all components mentioned above can either not provide enough output current to power the LTC3119 (about $17mA$ [62]), or have a low efficiency of under 70% at this required current. Therefore, these charge pumps score low on availability, as well as on power consumption.

Considering the charge pumps that have a regulated output voltage, two interesting devices were found: the MAX1595 [70] and MAX1759 [71]. Both devices can provide enough output current for the LTC3119, while operating at an input voltage of $1.8V$ and $1.6V$, respectively. Both devices can operate with only three external capacitors needed, which means that the complexity and required volume are low. However, both devices have a low efficiency, ranging from 50% to 80%, depending on the input voltage. Therefore, they score poorly on the power consumption.

Compared to charge pumps, substantially more boost converters with an inductor can be found that operate at a low input voltage. These include the MAX17220–MAX17225 [72], ADP1607 [73], LTC3525 [74], and TLV61220A [75]. All four devices can operate with an input voltage below $1V$ while providing more than enough output current. They all approach an efficiency of 90%, with the MAX17220–MAX17225 even approaching 95%. They are also easy to implement in the rest of the circuit because they only need an external inductor, as well as a bypass capacitor on the input and the output. Some devices also require a voltage divider to set the output voltage, while the LTC3525 has a fixed output voltage. The MAX17220–MAX17225 can set its output voltage using a single selector resistor. The only downside of these devices is the need for a relatively large inductor.

Result of the Trade-off

From Table 4.4 it can be concluded that the inductor-based boost converter is the best solution. A new DC-DC converter is either not available on the market or would be too complex to implement, and the charge pumps are not efficient. The boost converter scores good on all criteria, with only the volume being slightly sub-par due to the need for an inductor. The LTC3119 will thus be used in the design for both configurations, while the inductor-based boost converter is added only for the one-cell configuration. Using this boost converter, the voltage at the V_{IN} pin will always be above $2.5V$, ensuring that the LTC3119 can operate using only the power coming from the solar cells (REQ-402).

The boost converter selected for the circuit is the MAX17223ELT+ [72]. This device has the highest efficiency of the converters mentioned above. In addition, it still has the ability to select an output

voltage, increasing its flexibility. This selection also requires only one resistor, minimising the required volume. According to its datasheet, the accompanying inductor that results in the highest efficiency is the XFL4020-222 [76], which is a $2.2uH$ inductor with a size of $4mm$ by $4mm$. In case this inductor is too large to meet the volume requirement (REQ-203), a smaller inductor can be selected at a later stage in the design, although this could reduce the efficiency of the converter.

4.3.4. Integration of the DC-DC Converter

Now that it is decided to use the LTC3119 for both the one-cell and the two-cell configuration, its integration with the rest of the system needs to be worked out. To further speed up the design process, it was decided to search for a demo circuit board of this DC-DC converter. In this way, the likelihood of hardware bugs would be significantly reduced, since a demo board would already have been tested and proven to work. One demo board featuring the LTC3119 exists, the DC2129A [77], and the feasibility of its integration in the rest of the circuit will be discussed in this subsection.

Schematic of the Demo Circuit Board

The schematic of the DC2129A can be found in Figure 4.17. In the top left of the schematic, four connectors are shown: two connected to ”VIN” and two connected to ”GND”. The connectors with the ”-S” indication are test points and are meant to sense the respective voltage. The other connectors are female banana plugs, which are used to supply the power from the solar cells to the DC-DC converter. On this power supply line, the necessary input capacitors for the LTC3119, with a total value of $23\mu F$, are present, as dictated by its datasheet [62]. However, it is mentioned that when making use of the MPPC function, an even higher input capacitance of more than $100\mu F$ is needed.

The ”VIN” connector supplies the solar power towards the PV_{IN} pin of the LTC3119, but also to its V_{IN} pin. As explained in subsection 4.3.3, this is a problem in the case of a single solar cell. Therefore, the trace connecting the V_{IN} pin to the PV_{IN} pin should be interrupted, while preserving the connection between PV_{IN} and the ”VIN” connector. This can be achieved by drilling out a via on the demo board.

In the top right of the schematic, similar connectors can be found for ”VOUT” and ”GND”. These are used to connect to the power converted by the DC-DC converter. In reality, only one of the ”GND” connections will be used, since both of these ”GND” connections are shorted together on the demo board. Before the ”VOUT” connector, a large amount of bypass capacitors can be found, which are used to stabilise the output of the LTC3119.

Between ”VOUT” and ground, a voltage divider can be found, made up of resistors R1, R2, and R3. This voltage divider is connected to the FB pin and, as explained in subsection 4.3.2, controls the output voltage. By default, the demo board has an output voltage of $5V$. However, REQ-204 dictates that the output voltage should be $4V$. This can be adjusted by replacing one of the resistors in the voltage divider.

Another important feature of the demo board is the resistor between the ”RT” pin and ground. This resistor determines the switching frequency of the DC-DC converter. The default resistor on the demo board has a value of $105kOhm$ which corresponds to a switching frequency of $746kHz$. This also has an effect on the inductor selection, since a higher switching frequency allows for a smaller inductor, but also causes a decrease in efficiency.

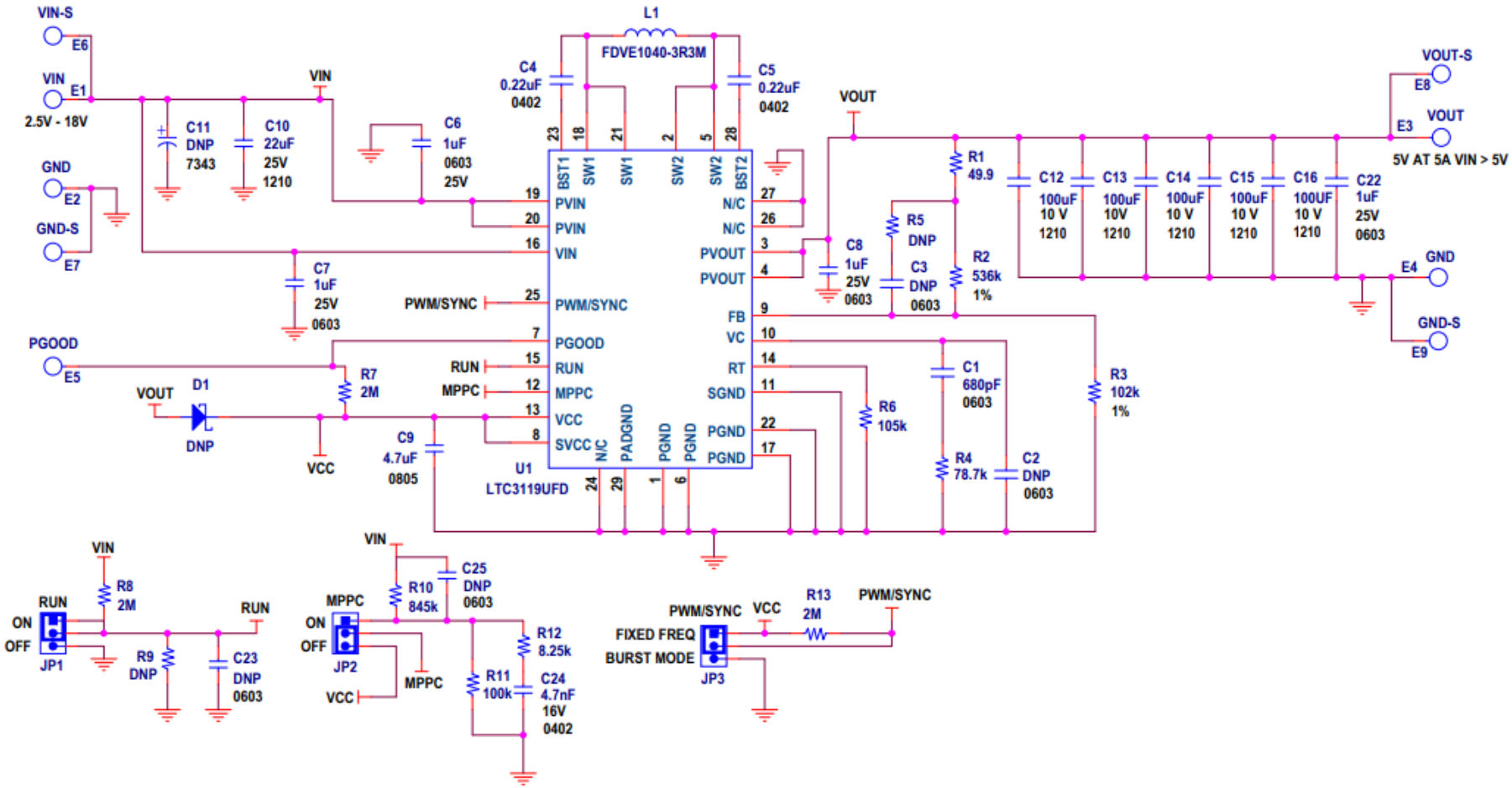


Figure 4.17: Schematic of the DC2129A, the demo circuit board of the LTC3119 [77].

The inductor on the demo board (”L1”) has a value of $3.3\mu H$, which is a good compromise between the size of the inductor and efficiency, according to the datasheet [62]. The value of the inductor also has an influence on the stability of the control loop of the converter. To ensure stability, a compensation network consisting of a capacitor and a resistor in series is connected to the VC pin. Based on the inductor value, as well as the input voltage, the output voltage, and the load of the DC-DC converter, the values of the components of the compensation network can be calculated [62].

Functional Modes of the Demo Circuit Board

At the bottom of the schematic, three circuits can be seen. These all have a connector with three pins, and by shorting either the top two or bottom two pins together, certain functions can be activated or deactivated. The left-most circuit can be used to short the RUN pin to ground by shorting the bottom two pins together. This would then deactivate the DC-DC converter, since the device is only active when the RUN pin voltage is above $1.205V$. When the top two pins are shorted, the RUN pin is being pulled high towards the ”VIN” voltage, ensuring that the device is active.

The circuit on the right can be used to switch between ”Burst” mode and ”Fixed Frequency” mode. When the two top pins are shorted together, the ”PWM/SYNC” pin is pulled high towards VCC. In this case, the DC-DC converter will operate at the frequency set by the resistor at the ”RT” pin. If the bottom two pins are shorted, Burst mode is activated, which means that at lower currents/loads, the device will go into a sleep state when the output voltage is at the correct value. As soon as the output voltage deviates too much, the LTC3119 wakes up again to correctly regulate the voltage, after which it will return to its sleep mode. In this sleep mode, the device consumes less power, which increases efficiency when operating at these light loads.

Finally, the middle circuit is used to enable or disable the MPPC function. As explained in subsection 4.3.2, a voltage divider can be placed between the input power line and the MPPC pin to set the desired minimum input voltage. On Figure 4.17, this voltage divider is made up of resistors R10 and R11. In parallel with resistor R11, another compensation network is present to keep the MPPC control loop stable. By shorting the two top pins of the connector together, the MPPC pin is connected to the voltage divider that sets the desired input voltage, activating the MPPC functionality. On the other hand, when the two bottom pins are shorted, the MPPC pin is pulled high toward the VCC voltage. This ensures that the MPPC pin does not drop below the $798mV$ it is compared to, essentially disabling the MPPC function.

Modifications to the Demo Circuit Board Required for Integration

In the current configuration, the MPPC circuit can only set one fixed minimum voltage as dictated by the voltage divider. However, the requirements state that the minimum input voltage should correspond to the actual V_{MPP}, which changes with the temperature of the solar cell (REQ-101). Therefore, a control circuit shall be designed that can provide the correct voltage at the MPPC pin based on the real-time temperature and voltage of the solar cell. This also requires the removal of resistor R10 to ensure that the control circuit has full control over the voltage at the MPPC pin. Resistor R11 is kept to maintain the functionality of the MPPC loop compensation.

An overview of the necessary modifications to the demo board is given in Table 4.5. In addition, in Table 4.6, the required connections between the demo board and the control circuit are given. These connections are similar to those proposed in the initial architecture in subsection 4.1.2: the input and

output power, as well as the ground connection, are the same. Next, instead of a signal that directly controls the duty cycle, a voltage corresponding to the V_{MPP} is supplied through the MPPC connection. Finally, one new connection is added: the V_{IN} connection to provide power to the DC-DC converter in the configuration with one solar cell.

Table 4.5: Required Modifications to the DC2129A demo board and their rationale.

Modification	**Rationale**
Adjust FB voltage divider	To force $4V$ instead of $5V$ at the output (REQ-204).
Increase the input capacitance	To ensure stability of the MPPC control loop.
Remove resistor R10	To give the control circuit full control over the MPPC voltage.
Disconnect V_{IN} from PV_{IN}	To ensure the LTC3119 stays operational when connected to a single solar cell, as explained in subsection 4.3.3.

Table 4.6: Required Connections to the DC2129A demo board and their rationale.

Connection	**Rationale**
PV_{IN}	Solar power connection to the input of the DC-DC converter (pin PV_{IN}).
V_{IN}	Power supply to enable the LTC3119 (pin V_{IN}).
GND	Ground connection for the LTC3119 and all the surrounding circuitry.
PV_{OUT}	Converted power coming from the output of the DC-DC converter (pin PV_{OUT}).
MPPC	The voltage calculated by the control circuit that will be supplied to the MPPC pin in order to set the correct minimum input voltage of the DC-DC converter.

4.4. MPPT Control PCB

Following section 4.3, it is clear how the desired operating voltage can be imposed on the solar cells. It can be achieved by supplying the correct voltage to the MPPC pin of the LTC3119. However, one more question remains: How can this desired MPPC voltage be calculated and produced?

As discussed in subsection 2.3.5, the temperature-based MPPT method is governed by a linear equation. This equation relates the V_{MPP} of the solar cell to its temperature. For clarity, it is repeated here in Equation 4.1 [45].

$$V_{MPP} = V_{MPP}^{STC} + (T - T^{STC})\mu_V \tag{4.1}$$

The main function of the MPPT Control PCB is then to solve the above equation. Based on the temperature data (T) it receives from the Solar Cell PCB, it should determine the desired V_{MPP}. To accomplish this, the other parameters in the equation also need to be known. These are the standard temperature (T^{STC}), the V_{MPP} at this standard temperature (V_{MPP}^{STC}), and the coefficient relating the change in V_{MPP} to the change in temperature (μ_V). As a starting point for the design of the MPPT Control PCB, the values for these parameters were obtained from the datasheet of the solar cells. However, it is advisable to also experimentally obtain these parameters by testing the actual flight solar cells. In this section, it will be explained how exactly the MPPT Control PCB will solve the above equation based on this data, and how it will supply the corresponding MPPC voltage to the DC-DC converter.

Firstly, in subsection 4.4.1, the temperature sensor that will provide the temperature data will be selected. Then, a conceptual design of the control circuit is proposed in subsection 4.4.2. Afterwards, in subsection 4.4.3, the conceptual design is filled in with realistic electronic components. Then, in subsection 4.4.4, actual devices were selected for each component of the circuit. There, it is also discussed how these devices will be supplied with power. In subsection 4.4.5, the tolerances of the selected devices and their influence on the operating voltage of the solar cells are discussed. Based on these tolerances and including the power consumption of all devices, the power efficiency of the circuit is calculated in subsection 4.4.6. Afterwards, the schematic and layout of the MPPT Control PCB are presented in subsection 4.4.7. Finally, in subsection 4.4.8, the production of this PCB is discussed.

4.4.1. Temperature Sensor

The first step in the design of the control circuit is the selection of the temperature sensor because it will impact the rest of the design. As discussed in subsection 4.2.1, the sensor will be a thermistor. However, there are two types of thermistors: Negative Temperature Coefficient (NTC) and Positive Temperature Coefficient (PTC) thermistors. As their names imply, the resistance of NTC thermistors decreases with increasing temperature, whereas the resistance of PTC thermistors increases with temperature. To decide between these two types, their use-case needs to be considered. For that, a closer look needs to be taken to Equation 4.1, which relates the V_{MPP} to the temperature of the solar cell.

Thermistor Selection

It is important to note that the V_{MPP}, which is a voltage, has a linear relationship with temperature (T), as shown by Equation 4.1. Therefore, a thermistor should be found that linearly relates temperature to voltage. However, only the resistance of a thermistor changes with temperature. To convert this change in resistance to a change in voltage, the thermistor is placed in a voltage divider. Thus, when comparing the linearity of NTC and PTC thermistors, it is not as important to check how linearly their

resistance changes with temperature. Instead, it is more important that the change in output voltage of the voltage divider in which the thermistor is placed is linear with respect to temperature. This is exactly what was investigated in an application note from TI [78]. They placed an NTC thermistor and their TMP61 [79] PTC thermistor in the bottom part of a voltage divider, as shown on the left side of Figure 4.18. On the right side of the same figure, the output voltage of the voltage divider is plotted versus temperature, and a first-order polynomial is fitted on both data sets.

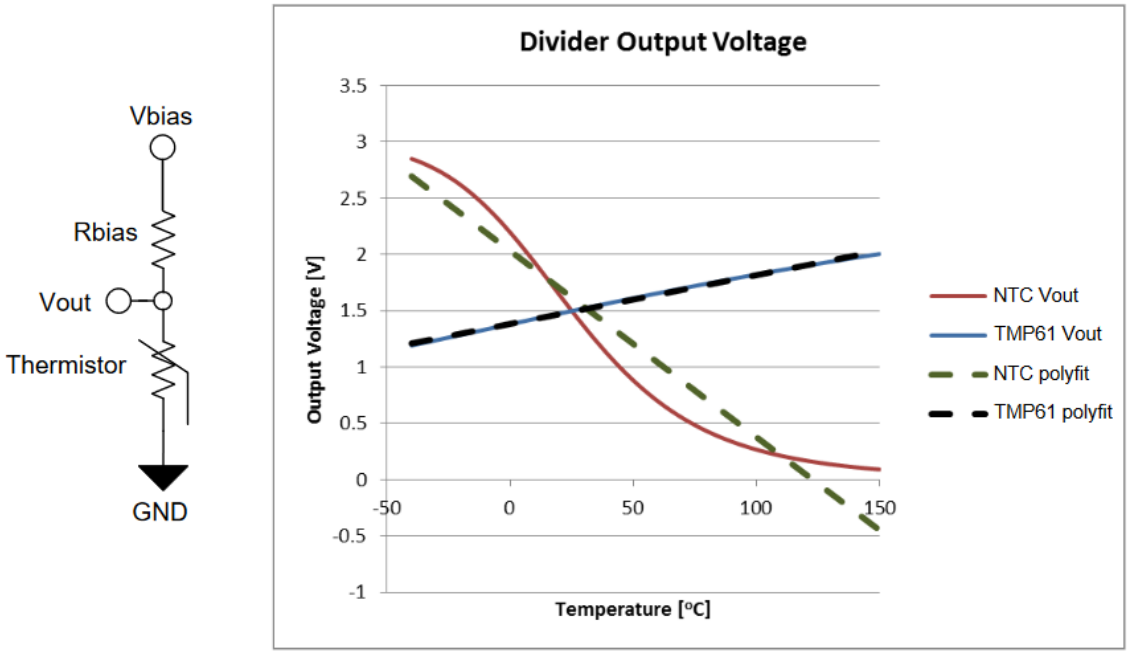


Figure 4.18: Comparison of the linearity of NTC and PTC thermistors [78].

As can be seen in Figure 4.18, the NTC data set deviates far from its linear fit. On the other hand, the TMP61 data set has barely any deviation from its linear fit over the full temperature range of $-40°C$ to $150°C$. This makes the TMP61 an ideal fit for this application.

It is clear that PTC thermistors such as the TMP61 are more linear than NTC sensors. Therefore, other linear PTCs were looked for to compare the TMP61 with. The best alternative found is the TFPT thermistor from Vishay [80]. However, this thermistor still underperforms the TMP61 because it has a higher resistance tolerance over the entire temperature range of ±3% compared to ±1.5% for the TMP61. In addition, the TFPT sensor in the 0603 package only has a resistance of at most $1kOhm$, while the TMP61 has a resistance of $10kOhm$. This means that the TMP61 will consume less power because a lower current will run through it at the same supply voltage.

A spreadsheet made by TI [81] also exists where the exact variant of the TMP61 sensor can be selected, as well as the supply voltage of the voltage divider. Based on this, the spreadsheet gives the parameters of a fourth-order polynomial that precisely relates the resistance of the thermistor to its temperature. This further eases the design process when using the TMP61. Due to all the reasons mentioned above, the TMP61 thermistor is selected for the MPPT circuit.

Linearity of the Thermistor

To further characterise the linearity of the TMP61, a spreadsheet was made in which the output voltage of the voltage divider with the thermistor was calculated per degree Celsius. The datasheet of the TMP61 recommends always having a $10kOhm$ resistor at the top of the voltage divider and the thermistor at the bottom of the divider [79]. The formula to then calculate the output voltage of this voltage divider is given in Equation 4.2.

$$V_{out} = V_{supply} \cdot \frac{R_{thermistor}}{10kOhm + R_{thermistor}} \tag{4.2}$$

Here, $R_{thermistor}$ is then calculated for every temperature using the fourth-order polynomial provided by TI. The temperature range of interest is $-60°C$ to $80°C$. This includes a margin of $20°C$ with respect to the expected temperature range of $-40°C$ to $60°C$ (REQ-103). The bias voltage of the divider is initially set at $4.36V$. The reason why this bias voltage was chosen will be explained below. The resulting output voltage versus temperature graph can be found in Figure 4.19 in blue. This figure also includes a linear fit in green. The difference between the linear fit and the actual output voltage (i.e. the error) is shown in orange. Note that the vertical axis on the left corresponds to the output voltage and the linear fit, while the vertical axis on the right corresponds to the error.

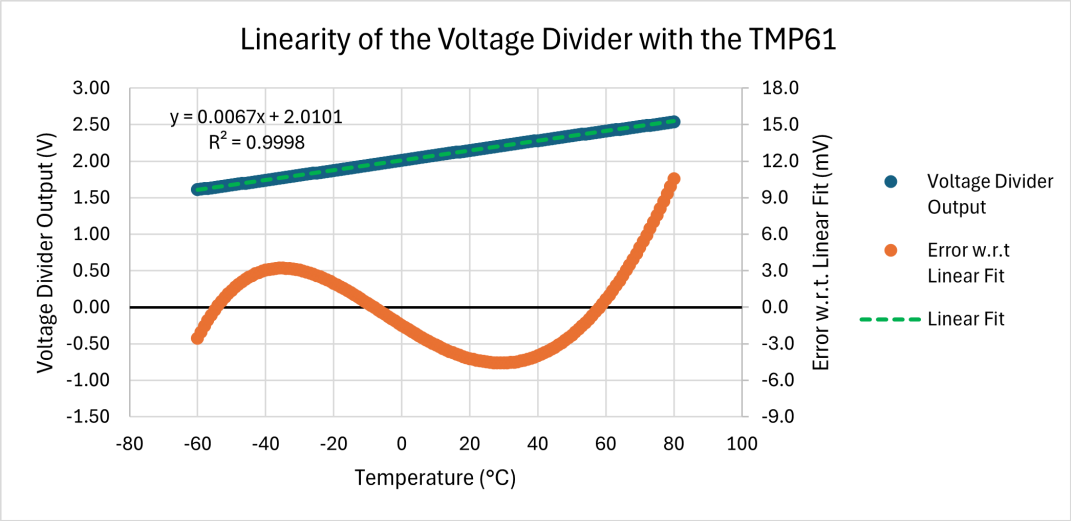


Figure 4.19: The output voltage of the voltage divider with the thermistor and its error compared to a linear fit in function of temperature with a bias voltage of $4.36V$.

As can be seen in Figure 4.19, the output voltage is highly linear: the linear fit has an R2 value of 0.9998, and a slope of $6.7mV/°C$. This slope has the same absolute value as the change of the V_{MPP} of the solar cells with respect to temperature, which is denoted by μ_V in Equation 4.1 and is equal to $-6.7mV/°C$. This is the reason why the bias voltage of $4.36V$ was initially chosen, since it makes evaluating the linearity of the sensor easier.

Figure 4.19 also shows that the error between the linear fit and the output voltage of the voltage divider remains below $6.7mV$ for almost the entire temperature range. It is slightly higher only for temperatures above $70°C$. Keeping in mind the μ_V, this means that the temperature error of the TMP61 will only be $1°C$ or less for most of the temperature range. This corresponds to a decrease in power of less than 0.3% compared to the MPP, which shows that the TMP61 is highly linear and thus a good choice.

4.4.2. Conceptual Design of the Control Circuit

In subsection 4.4.1, it was decided to use the TMP61 because it generates a linear change in voltage with respect to temperature when incorporated into a voltage divider. Now, it needs to be investigated how this sensor can be used to correctly adjust the voltage at the MPPC pin of the DC-DC converter so that the solar cells will operate at the V_{MPP}. The design concept of a circuit that can accomplish this is presented in this subsection.

Block Diagram of the Design Concept

As explained in subsection 4.3.2, the MPPC pin acts as a lower limit for the input voltage of the DC-DC converter. When the voltage at the MPPC pin drops below $798mV$, the DC-DC converter will adapt its duty cycle so that the input voltage will increase. Therefore, by placing a voltage divider in between the input voltage (i.e. the solar cell voltage) and the MPPC pin, any desired lower limit can be set for the solar cell voltage.

Ideally, this lower limit would be the V_{MPP} of the solar cell. Taking into account a temperature range of $-60°C$ to $80°C$, the average temperature of the solar cells will be $10°C$. The V_{MPP} at this temperature can be calculated using Equation 4.1, where $T^{STC} = 28°C$, $V_{MPP}^{STC} = 2409mV$, and $\mu_V = -6.7mV/°C$. These values were obtained from the datasheet of the solar cells [46] and result in a V_{MPP} of $2530mV$ at $10°C$. Dividing this value by $798mV$ (the voltage at which the MPPC functionality becomes active) results in a voltage divider value between the solar cell voltage and the MPPC pin of 3.17.

Of course, the V_{MPP} changes with temperature, so a correction should be added on top of the voltage divider output, before the MPPC pin. This can be achieved using the TMP61. However, the slope of the temperature measurement should then be equal to $\mu_V/3.17 = -2.11mV/°C$. In this way, when the temperature changes by $1°C$, the temperature correction adjusts the MPPC voltage with $2.11mV$. The DC-DC converter will then adjust the solar cell voltage by $2.11mV \cdot 3.17 = 6.7mV$, at which point the MPPC voltage will return to $798mV$. Thus, a $1°C$ change in temperature will result in a $6.7mV$ change in the operating point of the cell, which is exactly the same amount as the V_{MPP} has shifted. In order for the TMP61 to operate with this slope, its bias voltage should be lowered to $1.384V$. This ideal bias voltage was found using the same spreadsheet as for investigating the linearity of the TMP61.

The temperature correction now has the correct slope, but not yet the correct offset. At the average temperature of $10°C$ and a bias voltage of $1.384V$, the output voltage of the TMP61 is $0.654V$. However, at this temperature, the temperature correction should be equal to zero. Therefore, a constant offset of $0.654V$ should be subtracted from the temperature correction. This offset voltage can be achieved by having an additional voltage divider with the same bias voltage, which then divides that bias voltage with a factor of $1.384V/0.654V = 2.11$.

The reasoning explained above can be summarized in a block diagram, which can be found in Figure 4.20. On the right side of this figure, the voltage divider between the solar cell voltage and the MPPC pin is present. As explained above, this divider tries to force the V_{MPP} at $10°C$ on the solar cell. On the left side, the temperature correction is added. By having a bias voltage of $1.384V$ over the voltage divider with the TMP61, the temperature correction has the correct V_{MPP} versus temperature slope. Finally, on the top of the figure, a third voltage divider is present. This divider produces a fixed offset voltage that is subtracted from the temperature correction, to ensure that the temperature correction is zero at $10°C$.

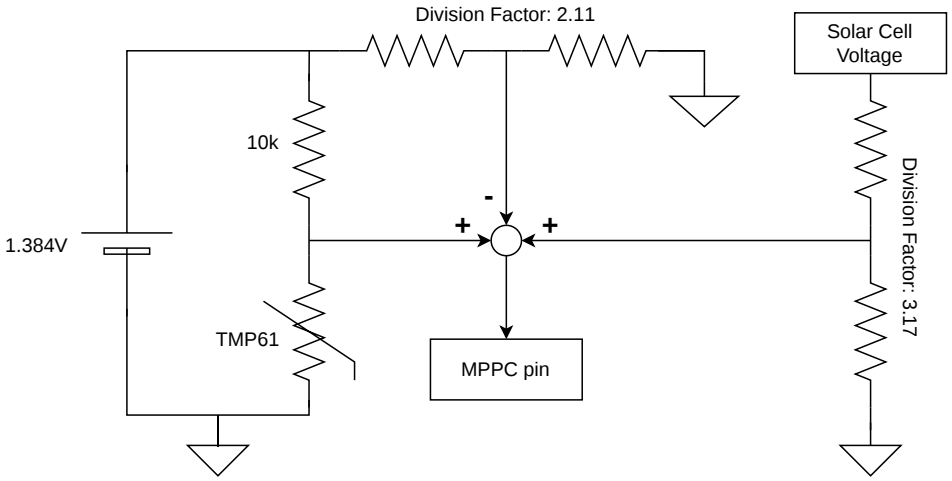


Figure 4.20: Block diagram of the design concept of the MPPT control circuit.

The Signs of the Voltage Dividers

Careful attention must be paid to determine whether the output voltages of these three voltage dividers should be added or subtracted in the calculation of the MPPC voltage. Firstly, the voltage divider from the solar cell voltage is essentially equivalent to the divider shown in Figure 4.15. It ensures that when the input voltage drops too low, the MPPC voltage also drops below $798mV$. This then results in the DC-DC converter adapting its duty cycle to increase the input voltage again. Thus, in order for the lower limit of the input voltage to work adequately, the MPPC voltage should decrease when the solar cell voltage decreases. Therefore, the output voltage of this voltage divider should have the same sign as the solar cell voltage, meaning that its sign should remain positive, as shown in Figure 4.20.

Next, the sign of the temperature correction should be determined. Since the V_{MPP} of the solar cells decreases with increasing temperature, the lower limit set by the MPPC pin should also decrease with increasing temperature. However, because the voltage at the MPPC pin is compared to a constant voltage, the only way to decrease the lower limit is by adding a positive offset to the MPPC voltage. When a positive offset of, for example, $50mV$ is added, the MPPC pin voltage would become $798mV + 50mV = 848mV$. This essentially allows the solar cell voltage to drop $50mV \cdot 3.17 = 158.5mV$ lower than without this positive offset. When the solar cell voltage then decreases with $158.5mV$, the output of the solar cell voltage divider lowers with $50mV$. At this point, the MPPC pin reaches $798mV$ again, activating the lower limit. Thus, adding a positive offset to the MPPC voltage decreases the lower limit of the solar cell voltage.

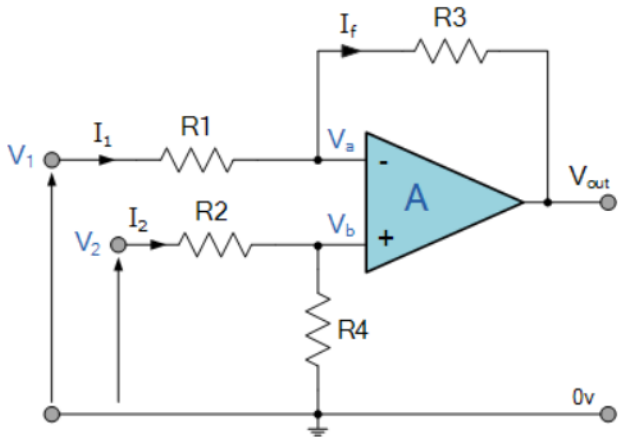
Now, with increasing temperature, the lower limit set by the MPPC pin should decrease, meaning that the offset added to the MPPC pin should increase. This can be achieved with the PTC voltage divider: with increasing temperature, the resistance of the PTC thermistor will increase. Because the thermistor is placed at the bottom of the voltage divider, an increase in its resistance will result in an increase in the output voltage of this divider. Therefore, the temperature correction can be added to the MPPC voltage, which is thus correctly displayed in Figure 4.20. Since the temperature correction is added, the constant offset produced by the third voltage divider should be subtracted from the MPPC voltage. In this way, it can compensate for the wrong offset produced by the temperature correction. Thus, all the signs shown on Figure 4.20 are correct.

4.4.3. Refining the Control Circuit

The block diagram shown in Figure 4.20 does not represent a realistic circuit. For example, it is assumed that the output voltages from the different voltage dividers can simply be added or subtracted from each other. Furthermore, the values mentioned on the block diagram are very precise. Therefore, in this subsection, the block diagram will be refined and filled in with realistic electronic components.

Adding and Subtracting the Voltage Divider Outputs

Starting in the middle of Figure 4.20, a device needs to be found that can add and subtract voltages. The go-to device for this is an Operational Amplifier (Op-Amp), which has two inputs (one inverting, one non-inverting) and one output. In this case, a differential Op-Amp circuit [82] is needed, which includes a feedback loop from the output of the Op-Amp to the inverting input. Then, the output is essentially the difference between the two inputs, multiplied by a gain that can be set with external resistors, as shown in Figure 4.21. Two of these Op-Amps can then be used in series to correctly add or subtract the voltages from the three voltage dividers.



$$R_1 = R_2, R_3 = R_4;$$

$$V_{out} = \frac{R_3}{R_1}(V_2 - V_1)$$

Figure 4.21: Differential Op-Amp circuit with external resistors to set the gain [82].

When inspecting Figure 4.20 again, it can be seen that the voltage dividers for the thermistor and for the constant offset essentially form a resistive bridge circuit. This means that the difference between their outputs will be small. In addition, this difference is exactly the correction that needs to be added to the output of the solar cell voltage divider. Thus, the differential voltage of the bridge circuit is important, and not necessarily the common-mode voltage.

An Op-Amp can be used to extract this differential signal using a differential Op-Amp circuit. However, due to the feedback loop, the common mode signal and its noise will still be present at the output of the Op-Amp. Therefore, an Instrumentation Amplifier (INA) can be used instead [83]. An INA also has an inverting and non-inverting input, and an output, like an Op-Amp. The difference is that an INA has a buffer stage at its inputs. This results in the feedback resistors being isolated from the input, meaning that the common mode is better rejected. In addition, the input resistors have large resistances and are precision matched, increasing the accuracy of the measurement.

An INA is thus better at rejecting the common mode voltage and extracting only the differential signal, which is ideal for reading out bridge measurements [83]. This differential signal is then multiplied by

a gain. This gain (G) can usually also be set using one or two external resistors, but these are also isolated from the inputs to increase gain accuracy. After the gain is applied, the signal is added to a reference voltage. An INA thus has three inputs ($IN+, IN-$ and REF), instead of the two inputs of an Op-Amp. The transfer function of an INA is then given by Equation 4.3 [84].

$$V_{out} = G \cdot (V_{IN+} - V_{IN-}) + V_{REF} \tag{4.3}$$

As explained before, the thermistor and constant-offset voltage dividers form a bridge circuit, so they can be connected to the non-inverting and inverting inputs of the INA, respectively. Looking again at Figure 4.20, the solar cell voltage divider can be regarded as a reference voltage and can thus be connected to the reference input. In this way, all three outputs of the voltage dividers can be added or subtracted correctly using a single INA, instead of two Op-Amps. Therefore, less volume is required while increasing the accuracy. In case all values mentioned on Figure 4.20 remain the same, the gain of this INA should be equal to 1.

Voltage Reference

Next, the voltage reference needs to be investigated further. For low voltage applications, the most common voltage reference type is the bandgap reference [85]. This reference is based on the bandgap energy of silicon, which is approximately $1.2V$. Therefore, $1.25V$ is the lowest value for voltage references that are commonly available. Higher values are also available; the most common ones are $2.5V$, $3.3V$ and $5V$.

However, Figure 4.20 shows that a reference of $1.384V$ would be ideal, but this value is not readily available. This can be solved by changing the gain of the INA. Since the goal of an INA is to *amplify* the difference in its inputs, most INAs available on the market have a gain greater than or equal to 1. When the gain of the INA increases, the voltage reference should decrease to compensate. Thus, the voltage reference must be lower than $1.384V$. This leaves only one option for the reference, which is $1.25V$. In that case, the gain of the INA should be $1.384V/1.25V = 1.107$. The new value of the voltage reference influences both the thermistor voltage divider and the constant-offset divider, since both are powered by the reference. However, since both outputs of these voltage dividers are multiplied by the gain of the INA, no other values in Figure 4.20 must be adapted.

Resistors of the Voltage Dividers

The final parts of Figure 4.20 that need to be discussed are the voltage dividers themselves. For optimal operation, the divider with the thermistor has to have a $10kOhm$ resistor at the top and the thermistor at the bottom [79], so nothing changes there. For the other two dividers, precise division factors are needed. In addition, to ensure that the MPP is followed as closely as possible, the resistors in these dividers should have high accuracies.

A series of resistors was found that has a tolerance of $\pm 0.05\%$: the "ERA-3ARW" series from Panasonic [86]. It was chosen because it is the cheapest series with this high accuracy in a package size as small as 0603, while still having numerous options for the resistance values. Then, a combination of resistor values in this series was looked for that would result in a division factor close to 3.17 for the solar cell voltage divider, as calculated in subsection 4.4.2. When the top resistor has a value of $33kOhm$ and the bottom resistor has a value of $16kOhm$, the division factor would be $1 + 33k/16k = 3.0625$.

In the case of two cells in series, it would be beneficial for this divider to have a division factor exactly double with respect to the single cell configuration. In that case, the bottom resistor can remain at $16kOhm$, while the top resistor will have a value of $82kOhm$. Then, the division factor would be $1 + 82k/16k = 6.125$, which is twice the division factor in the case of a single cell. Thus, by only changing one resistor, the control circuit can be adapted for either one or two solar cells.

Since the division factor of the solar cell voltage divider has slightly changed, the slope of the solar cell and the thermistor do not match anymore. Using the spreadsheet with which the linearity of the TMP61 was characterised, the slope of the thermistor was found to be $1.909mV/°C$ when biassed with $1.25V$. On the other hand, the slope of the solar cell after the voltage divider is $-6.7mV/°C$ / $3.0625 = 2.188mV/°C$. This difference can be compensated for again with the gain of the INA. The gain should then be equal to $2.188mV/°C$ / $1.909mV/°C = 1.146$.

The constant offset now also has to be updated. When no temperature correction would be applied, the solar cell voltage divider would enforce a lower limit of $0.798V \cdot 3.0625 = 2.444V$. Using Equation 4.1, this corresponds to a temperature of the solar cells of $22.8°C$. At this temperature, the output of the thermistor voltage divider is $0.616V$, which should be equal to the output of the constant-offset voltage divider. Thus, the offset divider should have a division factor of $1.25V/0.616V = 2.03$. Since this factor is almost equal to 2, this voltage divider can be made from two $10kOhm$ resistors to complete the bridge circuit with the thermistor divider. For even higher accuracy, a $300Ohm$ resistor can be put in series with the top $10kOhm$ resistor of the offset divider.

Multiple modifications have been made to the original block diagram shown in Figure 4.20. These modifications, which were explained in this subsection, are summarised in an updated block diagram, which can be found in Figure 4.22.

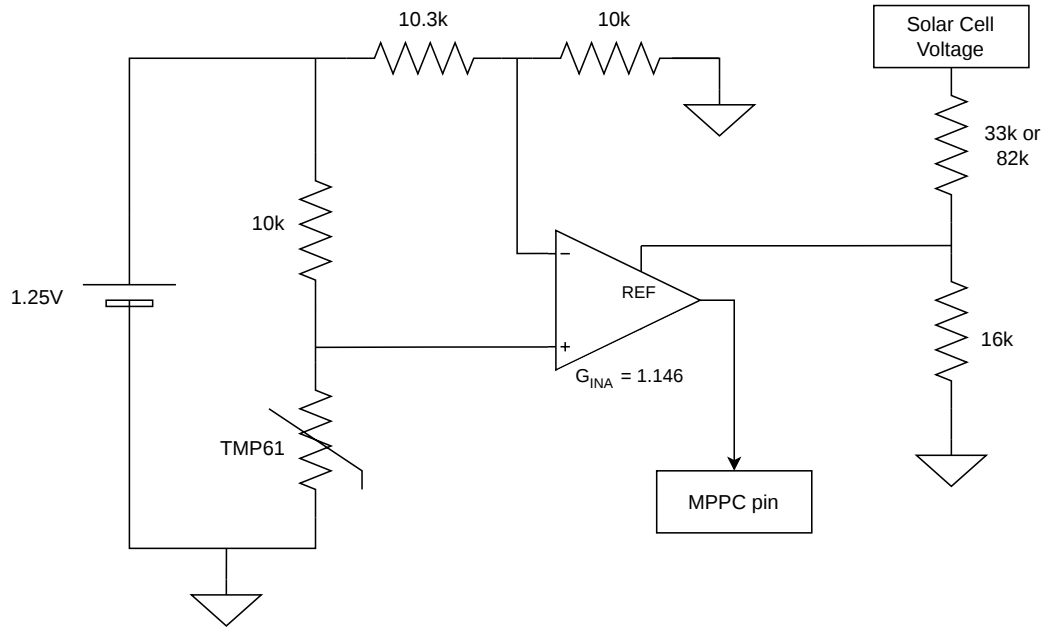


Figure 4.22: Updated block diagram of the control circuit with realistic values for the resistors and the voltage reference.

4.4.4. Populating the Control Circuit

Looking at Figure 4.22, the actual thermistor and resistors have already been decided. Now, the actual devices for the voltage reference and the INA have to be selected. It is important to note that all devices that were considered in this design, including the DC-DC converter and all resistors and capacitors, can operate throughout the entire temperature range as specified in REQ-103.

Supply Voltage for the INA and Voltage Reference

Before selecting the devices, it is important to consider how the voltage reference and the INA will be powered. To keep the complexity of the circuit as low as possible, it would be convenient to power them from the same voltage rail as the DC-DC converter. In this way, the smallest number of voltage regulators is needed.

In the one-cell configuration, the boost converter can produce a stable supply voltage that powers the DC-DC converter, and thus also the voltage reference and INA. However, in the two-cell configuration, the LTC3119 is powered directly by the solar cells, which can swing from $4.4V$ to $5.8V$. It is possible to find a voltage reference and INA that can operate at these voltages as well. However, it is preferred to have a stable supply voltage to increase the accuracy of the voltage reference especially, as will be explained in subsection 4.4.5.

To obtain this stable supply voltage while minimising the number of components, the VCC pin of the DC-DC converter can be used. This pin provides a regulated voltage of $3.7V$ that is produced by an internal LDO regulator inside the LTC3119. This internal regulator is powered by the V_{IN} pin, as explained in subsection 4.3.3. Because the voltage of two solar cells never drops below $4.4V$, and the dropout voltage of this internal regulator is less than $150mV$, the VCC pin will remain stable at $3.7V$ for the two-cell configuration. It can also drive external circuitry up to $10mA$, which should be sufficient current for an INA and a voltage reference. This power then needs to be delivered from the VCC pin on

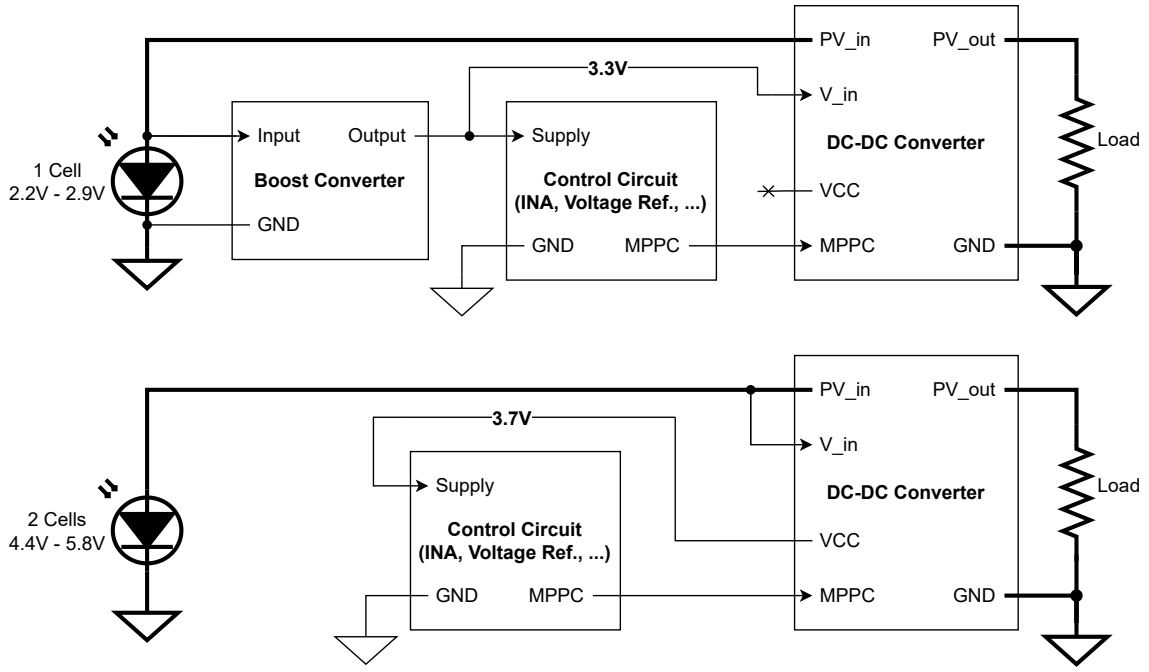


Figure 4.23: Summary of the difference in the supply voltage between the one-cell (top) and two-cell (bottom) configuration.

the DC2129A demo board to the components on the MPPT Control PCB. This requires an additional connection between the demo board and the MPPT Control PCB, on top of the connections already presented in Table 4.6.

For the one-cell configuration, the VCC pin will not be used because the boost converter can already provide a stable voltage. Otherwise, the power for the INA and the voltage reference would also pass through two voltage converters (the boost converter and the internal LDO regulator), which would reduce efficiency. It is possible for the MAX17223ELT+ to produce a supply voltage of $3.7V$ so that it is the same as for the two-cell configuration. However, this supply voltage powers the DC-DC converter, which consumes more power when V_{IN} is higher [62]. Thus, a lower supply voltage would be more power efficient. On the other hand, the boost converter can essentially only increase the voltage of the solar cell. The V_{MPP} of a single cell can go up to $2.9V$, but when less power is required than the MPP, the operating voltage of the cell can go even higher. Therefore, a supply voltage of $3.3V$ was chosen for the one-cell configuration. This means that it shall be possible for the voltage reference and INA to be powered by $3.3V$ and $3.7V$ to be compatible with both configurations.

To further clarify the difference in the supply voltage between the two configurations, two simplified schematics were drawn, which can be found in Figure 4.23. The one-cell configuration can be found at the top of the figure, with the two-cell configuration displayed below.

Selection of the INA

Now that the problem of the supply voltage has been solved, the search for the two components can start. For the INA, various features are required. Firstly, it shall have an adjustable reference voltage that can be set from an external voltage. In addition, its gain shall be precisely adjustable to achieve the desired gain of 1.146. For some INAs, its gain is determined by the ratio between two resistors. This is a preferred feature, since this can be substantially more flexible and precise than setting the gain using the usual single resistor. Besides these features, the accuracy and power consumption of the device are also important properties.

The main producers of INAs are TI and Analog Devices, Inc. (ADI). First, the INAs sold by TI were filtered on a supply voltage of $3.3V$ to $3.7V$, and a gain around 1.146. The remaining INAs were then checked for how their gain can be set. Most of them could set the gain with only one resistor,

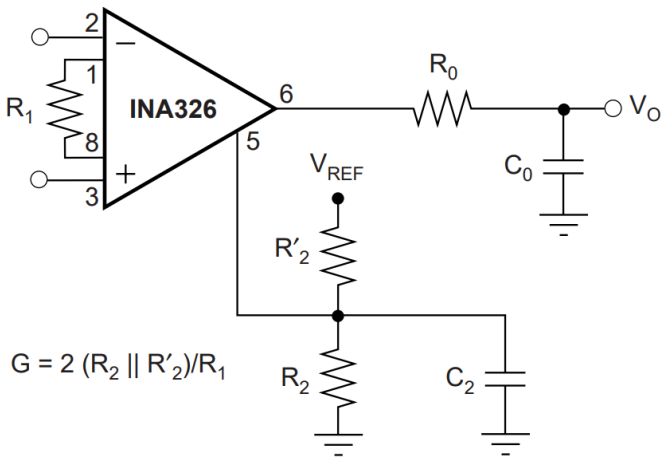


Figure 4.24: The gain of the INA326 is affected by the voltage divider that sets the reference voltage [87].

which is suboptimal. Therefore, only two candidates remained: the INA326/INA327 [87], and the INA337/INA338 [88].

A closer look was taken at the datasheets of these INAs, which have a highly similar architecture. It was found that one of the resistors that set the gain is connected between the reference pin and ground, while the other resistor is connected to two pins dedicated for this resistor (R_1 in Figure 4.24). Furthermore, the reference voltage can be set by a voltage divider (R_2' and R_2). This voltage divider corresponds to the solar cell voltage divider shown in Figure 4.22. However, the resistance of this divider will therefore have an effect on the gain, which is shown by the gain equation displayed in Figure 4.24. Since the values of R_2' and R_2 have already been decided, as explained in subsection 4.4.3, the only variable in the gain equation becomes R_1. Therefore, the INAs from TI offer less flexibility to set the gain and are thus not the ideal solution.

The INAs from ADI were also filtered on the supply voltage and the gain. However, many options still remained. Therefore, it was decided to filter further on components that are "Recommended for New Designs" by ADI themselves. This guarantees that the component will remain in production in the coming years. This additional filter resulted in four options. Two of these INAs can only set their gain digitally, which would unnecessarily increase the complexity of the design. This leaves only two options: the AD8237 [89] and the AD8420 [90].

Between the two INAs, the AD8420 has a wider supply voltage range from $2.7V$ and $36V$, and has a slightly lower quiescent current of at most $110\mu A$. The AD8237, on the other hand, has a supply range of $1.8V$ to $5.5V$, which still perfectly fits the supply voltages of $3.3V$ and $3.7V$. The slightly higher quiescent current of $150\mu A$ is also still negligible compared to the overall current generated by the solar cells. Furthermore, the AD8237 is more precise than the AD8420 because it has a lower offset voltage ($75\mu V$ vs. $125\mu V$), a significantly lower input bias current ($1nA$ vs. $30nA$), and a lower gain error (0.005% vs. 0.02%). The influence of these errors is explained further in subsection 4.4.5. All other specifications are similar between the devices, so the AD8237 is thus the preferred component.

Setting the Gain of the AD8237

The gain of the AD8237 is set by two resistors: one between the V_{out} pin and the FB pin ($R2$ in Figure 4.25), and one between the FB pin and the REF pin ($R1$). The REF pin is also the input for the reference voltage as set by the solar cell voltage divider. The resistance of this divider will therefore influence the gain as well, similarly to the INAs from TI discussed above. This is shown in Figure 4.25, which also shows the gain equation when considering the resistance of the divider for the reference voltage. However, in the case of the AD8237, the resistance of *both* of the original gain resistors can still be chosen to obtain the desired gain. This allows for the desired flexibility and precision of the gain, while still having the reference voltage set by a voltage divider.

Using the gain equation shown in Figure 4.25, the values for the gain resistors can be obtained. In the case of two solar cells, the parallel combination of the resistors in the solar voltage divider equals $(1/82k + 1/16k)^{-1} = 13.39k$. To obtain a gain of 1.146, the minimum value of $R1$ can be calculated by setting the value of $R2$ to zero. Then, $R1 = (0 + 13.39k)/(1.146 - 1) = 91.69k$. The gain resistors will be selected from the same "ERA-3ARW" series of resistors that make up the three voltage dividers. This limits the available resistance values: the resistors with the highest value in this series are $91k$ and $100k$. The $91k$ is below the minimum value, so $R1$ has to be $100k$.

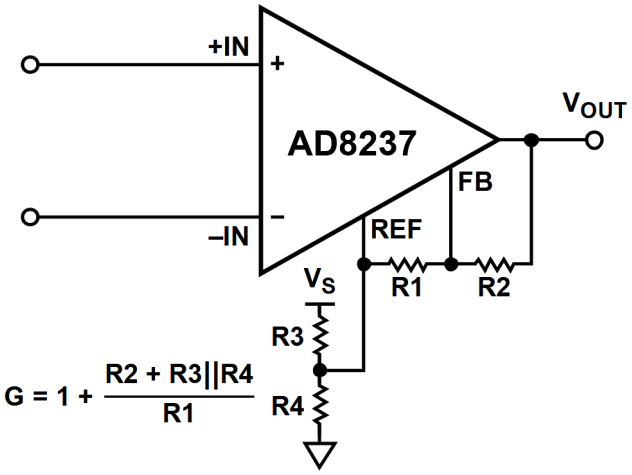


Figure 4.25: The gain of the AD8237 is affected by the voltage divider that sets the reference voltage [89].

With $R1$ known, the desired $R2$ can be calculated: $R2 = 100k \cdot (1.146 - 1) - 13.39k = 1.224k$. The closest resistance value available in the "ERA-3ARW" series is $1.2k$, which is only $24Ohm$ lower than the desired value. Selecting this resistor would result in a gain of 1.1459, which is almost exactly the desired gain. Similar calculations were performed for the one-cell configuration. In this case, the minimum value of $R1$ is $73.75k$, which leaves four options from the "ERA-3ARW" series: $75k$, $82k$, $91k$, and $100k$. For each of these options, the optimal value for $R2$ was calculated to obtain a gain as close as possible to 1.146. The best combination was $R1 = 82k$ and $R2 = 1.2k$, resulting in a gain of 1.1460, exactly matching the target value. This combination has the added benefit of using resistance values that have been used before in the circuit, minimising the amount of different resistance values.

The combinations of resistors for both configurations fall within the recommended resistance range as specified by the datasheet of the AD8237 [89]. In addition, the AD8237 has the desired transfer function as stated in Equation 4.3. This function also remains valid over all temperatures and operating points of the circuit due to the true rail-to-rail capability of this device. The AD8237 thus has all the desired functionality. Only the accuracy of the device remains to be further investigated, which will be done in subsection 4.4.5.

Selection of the Voltage Reference

With the INA selected, only the voltage reference remains to be found. The most important feature of the voltage reference is its accuracy. This is needed to make sure the V_{MPP} is closely followed: the more stable the voltage reference, the more reliable the temperature measurement will be, since the thermistor is powered by the reference. The power consumption of the device is also an important factor in achieving a high overall system efficiency.

A similar strategy was followed as for finding the INA. Again, the main producers of voltage references are TI and ADI. For both companies, the selection of voltage references was first filtered on the supply voltage of $3.3V$ to $3.7V$, as well as the desired output voltage of $1.25V$. The remaining devices were ranked based on their initial accuracy. Many high-precision devices are available, but only two had an accuracy of less than $\pm 0.05\%$. These are the REF70 from TI [91], and the MAX6070/MAX6071 from ADI [92].

The REF70 has by far the highest accuracy of ±0.025% and a low temperature drift coefficient of $2ppm/°C$. Its downside is its high power consumption with a quiescent current of up to $7.5mA$. The MAX6070/MAX6071, on the other hand, has a slightly worse accuracy of ±0.04% and a temperature coefficient of $6ppm/°C$. However, its power consumption is considerably lower because it has a quiescent current of only $260\mu A$. Both devices can provide sufficient current to the load, which consists of the two voltage dividers for the temperature correction.

Both devices also have an Output Force and an Output Sense pin. The Output Force pin is the usual output at which the $1.25V$ is provided and where the current necessary to power the load comes from. The Output Sense pin can be regarded as a feedback pin. It should be connected to the Output Force line at the location on the PCB where the $1.25V$ is exactly needed. In this way, the Output Sense pin can compensate for a possible voltage drop between the Output Force pin and the load.

The MAX6071 has a similar sense pin for the ground to account for a voltage difference between the ground at the voltage reference and the ground at the load. The MAX6070, on the other hand, has a filter pin instead of the ground sense pin. When a capacitor is connected between this filter pin and ground, the noise at the output will be reduced. Because the voltage reference can likely be placed right next to the voltage dividers it will power, and because there can be some noise introduced in the system by the DC-DC converter, it is likely more beneficial to have a filter pin than a ground sense pin. Therefore, from this point on, only the MAX6070 will be compared with the REF70.

If only the accuracy of the reference had to be considered, the REF70 would be selected. However, the only reason for the high precision is to closely follow the V_{MPP} so that as much power as possible is extracted from the solar cells. Therefore, the overall efficiency of the system needs to be taken into account, which includes the power consumption of the voltage reference. The power loss caused by the imperfect accuracy of both references will be compared with their power consumption in subsection 4.4.6, after which the selection between these two devices will be made.

4.4.5. Accuracy of the Control Circuit

The complete control circuit is now populated with actual devices, except for one remaining choice between two options for the voltage reference. The next step is to evaluate the circuit and quantify how accurately the solar cell voltage will follow the V_{MPP} with changing temperatures. This can be achieved by considering the manufacturing tolerances of each device in the circuit. The corresponding calculations were performed in a spreadsheet and are discussed in more detail in this subsection.

The Ideal Case

Firstly, the ideal case where the tolerances are ignored was calculated per degree Celsius between $-60°C$ and $80°C$. For each temperature, the resistance of the thermistor was calculated using the fourth-order polynomial provided by TI. Then, similar to the linearity spreadsheet, the output voltage of the thermistor voltage divider (V_{IN+}) was calculated, again using Equation 4.2.

The division factors of the remaining voltage dividers were then calculated by $factor = 1+R_{top}/R_{bottom}$. For the constant-offset voltage divider, the offset (V_{IN-}) was then obtained by dividing $1.25V$ by the correct division factor. The gain of the INA (G) was also calculated using the equation shown on Figure 4.25. These values were then used to find the lower limit of the input voltage of the DC-DC converter (PV_{IN}) for each temperature. This was calculated by solving Equation 4.3 for V_{REF} and then rewriting

V_{REF} to PV_{IN} by including the division factor of the solar cell voltage divider (F_{REF}). This results in Equation 4.4. Here, V_{out} is the output voltage of the INA, which is connected to the MPPC pin. When the MPPC function is active, the voltage at the MPPC pin is equal to $0.798V$. Therefore, when calculating the lower limit, V_{out} is set equal to $0.798V$.

$$PV_{IN} = F_{REF} \cdot [V_{out} - G \cdot (V_{IN+} - V_{IN-})] \tag{4.4}$$

The expected (ideal) lower limit voltage was then plotted with respect to temperature. On the same graph, shown in Figure 4.26, the V_{MPP} with respect to temperature is displayed. The V_{MPP} graph essentially plots Equation 4.1 with the parameters given in the datasheet of the solar cell. The two curves should be as similar as possible and, as can be seen in Figure 4.26, they are almost indistinguishable. However, when plotting only the difference between these two curves, some error is still visible. When comparing this error with the error in the linearity of the temperature sensor shown in Figure 4.19, they are almost identical: the difference between these errors always remains under $1mV$. This means that the error in the ideal lower limit is mainly a by-product of the fourth-order nature of the thermistor. Note that this graph is representative of the configuration for one solar cell. In the case of two cells, the graph looks essentially identical, except that the values on both vertical axes are doubled.

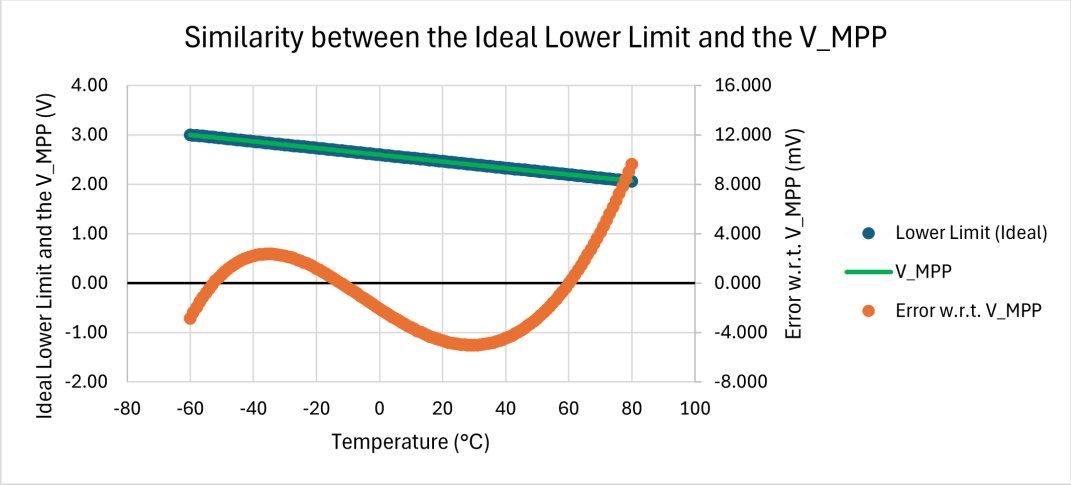


Figure 4.26: The ideal case of the expected lower limit voltage compared to the V_{MPP} of the solar cells versus temperature. The mismatch between these curves is also shown.

The non-linearity of the thermistor is not the only error in the system. Each component has inaccuracies that are caused by manufacturing tolerances. Thus, for each component in the system, the upper and lower bounds of their errors are calculated based on these tolerances, which are given in the datasheet of each device.

Tolerances of the Voltage Reference

Firstly, the two voltage references will be discussed. Their tolerances that cause inaccuracies are summarised in Table 4.7. The initial accuracy of the devices is given as a percentage, while the other errors are given in ppm (per $^{\circ}C$, V, or mA). These are all relative errors with respect to the output voltage of the reference. For the initial accuracy, the absolute error can be obtained by first converting the percentage to a ratio by dividing it by 100. Then, this ratio is multiplied with the output voltage, in this

Table 4.7: Comparison of the tolerances of the two selected voltage references [91][92].

	REF7012QFKHT	**MAX6070**AAUT12+T
Initial Accuracy	0.025%	0.04%
Temperature Drift	$2ppm/°C$	$6ppm/°C$
Line Regulation	$30ppm/V$	$125\mu V/V = 100ppm/V$
Load Regulation	$15ppm/mA$	$150\mu V/mA = 120ppm/mA$
Thermal Hysteresis	$18ppm$	$85ppm$
Long-term Drift	$35ppm$	$35ppm$

case $1.25V$. The absolute error caused by the other effects can be calculated in a similar manner: the ratio is obtained by dividing the value in ppm by one million, after which it is multiplied with $1.25V$. For the temperature drift, the ratio should also be multiplied with the temperature range of the device. Finally, all these absolute errors can be summed to obtain the overall error of the voltage reference.

Line regulation refers to the error in the output voltage caused by variations in the supply voltage of the voltage reference [85]. Therefore, having a stable supply voltage is beneficial. In the case of one cell, the voltage reference will be powered by the boost converter, as discussed in subsection 4.4.4. This converter has a tolerance of ±1.5% on its output voltage of $3.3V$, which corresponds to ±$50mV$ [72]. In the case of two cells, the supply voltage is produced by the VCC pin of the DC-DC converter, which has a tolerance of ±$150mV$ [62]. Therefore, this second tolerance was chosen with which a conservative value for the error due to line regulation will be calculated. Since the datasheet of the references expresses the line regulation error in $\mu V/V$ or ppm/V, the absolute error can be calculated by multiplying the corresponding ratio with the ±$150mV$ mentioned above and then multiplying this with the output voltage of $1.25V$.

Load regulation is an inaccuracy in the output voltage caused by a change in the output current [85]. Since the voltage reference only powers two voltage dividers, the load current can be precisely calculated by dividing $1.25V$ by the parallel combination of the resistances of the voltage dividers. This results in a load current of approximately $0.125mA$. Again, this is then multiplied with the corresponding ratio, as well as the $1.25V$, to obtain the absolute error caused by load regulation.

Thermal hysteresis is defined as the shift in the output voltage of the voltage reference after the component has been cycled through its entire operational temperature range. This error is based on only one cycle because the error settles relatively quickly after a few cycles [93]. However, to remain conservative, the value of this error was doubled to account for the effect of additional thermal cycles.

A similar approach was followed for the long-term stability of the voltage references. The output voltage will drift over time, and this is usually measured by the manufacturer over a period of 1000 hours, since the largest portion of the long-term drift occurs during that time [85]. However, since the circuit will likely operate for more than 1000 hours, this error will be doubled to maintain a worst-case estimate.

Tolerances of the Resistors

Continuing with the resistors [86], they have a resistance tolerance of ±0.05% at room temperature. In addition, their resistance also changes with temperature by ±$10ppm/°C$. By multiplying this value with the difference between the minimum/maximum operating temperature and room temperature, the

largest error due to this effect can be calculated. This should then be added to the initial tolerance of ±0.05% to obtain the largest possible error for the resistors. By multiplying this relative error with the resistor value, the absolute value of the error is obtained.

These resistance tolerances will have an impact on the division factors of the voltage dividers. The worst case occurs when the top resistor has the maximum positive error while the bottom resistor has the maximum negative error, or vice versa. The first situation would result in the highest division factor, while the second situation would result in the lowest. This can be derived from the formula to calculate the division factor of a voltage divider: $factor = 1+R_{top}/R_{bottom}$. The same reasoning was also applied to the resistors that set the gain of the INA, resulting in an initial minimum and maximum gain.

Similarly to the resistors, the thermistor [79] also has a resistance tolerance, which is ±1% at room temperature, but is extended to ±1.5% when looking at its entire operating range. In addition, it also has a long-term drift error: after 1000 hours of continuous operation, an additional error of -1% to $+1.2$% could be observed. Since the circuit shall likely operate for more than 1000 hours, this value is multiplied with a safety factor of 2, similarly to the voltage reference. Again, these errors are summed and then multiplied with the resistance value of the thermistor to find its absolute error.

Tolerances of the INA

Finally, the tolerances of the INA [89] will be investigated. The gain of the AD8237 has an initial accuracy of ±0.005%, which also varies with temperature by ±$0.5ppm/°C$. In addition, the non-linearity of the gain introduces an error of ±$3ppm$ for gains below 10. The gain error also increases with the common-mode voltage by ±$15ppm/V$. Here, a conservative value of $1V$ was used for the common-mode voltage. All these relative inaccuracies should be added together and then multiplied with the initial maximum gain determined by the error of the resistors to find the final absolute gain error.

The INA also has some inaccuracies that originate from its input pins, one of which is the input offset voltage. In case the voltages at the input pins are exactly equal, the INA will still internally measure a difference of this offset voltage [94]. The AD8237 [89] has a maximum input offset voltage of ±$75\mu V$. In addition, the offset voltage can vary with ±$0.3\mu V/°C$.

Another non-ideal effect occurring at the input pins is the input bias current. This is a small current that flows in or out of the input pins. Since this current will also flow through the resistors connected to the input pins, the voltage at these pins will be altered [94]. The maximum input bias current of the AD8237 is ±$1nA$ [89]. To convert this to a voltage at the input pins, this current should then be multiplied with the input resistance. The input resistance is the parallel combination of the resistors in the voltage divider connected to the input pin.

The error in the input voltage caused by the offset voltage and the bias current should be added together. Since these affect the input, the error should be multiplied with the gain of the INA to find the error in the output voltage. The maximum gain is then used to ensure that the worst possible output voltage error is obtained.

The output of the INA is connected to the MPPC pin of the DC-DC converter. This pin also induces an inaccuracy in the system. The constant $0.798V$ to which the MPPC pin is compared has a tolerance of ±$24mV$ that should be taken into account [62]. This tolerance seems rather large and, if correct, can induce a large error in the operating voltage of the solar cells.

Combined Effect of All Tolerances

The errors induced by all the tolerances of each component mentioned above should be taken into account when calculating the lower limit of the solar cell voltage set by the DC-DC converter. The lower limit in the ideal case was calculated using Equation 4.4. Now, two additional lower limits are obtained: the minimum and maximum possible lower limits. For the minimum value, each error that contributes to a lower solar cell voltage was included in the calculation. The opposite was done to obtain the maximum value.

For example, to calculate the minimum lower limit, the lowest possible value for V_{out} should be used in the calculation. In addition, the highest possible value for V_{IN+} should be used. This can be explained by looking at Equation 4.4. Here, V_{out} has a positive sign, while V_{IN+} has a minus sign in front of it. Thus, a lower value for V_{out} and a higher value for V_{IN+} will both result in a lower value for the lower limit PV_{IN}.

Including all errors in the calculation for the lower limit results in the graph shown in Figure 4.27. This graph shows the V_{MPP} in function of temperature, as well as the typical expected lower limit, similar to Figure 4.26. In addition, the expected minimum and maximum lower limits, which take into account all tolerances of the devices, are displayed. The graph in Figure 4.28 shows the difference between the three values for the expected lower limit and the V_{MPP}, thus showing the typical, minimum and maximum error with respect to the V_{MPP}.

The typical value follows the V_{MPP} very closely, but a clear difference can be seen between the minimum and maximum values. These errors become as large as $\pm 135mV$, which is an error in voltage of more than 6%. This means that the solar cells might operate at a voltage that differs up to 6% from the V_{MPP}. To investigate where this relatively large error comes from, a breakdown is made of the contribution of each component to this error. This breakdown is displayed in Figure 4.29.

As can be seen in Figure 4.29, the largest contributor by far is the MPPC pin of the DC-DC converter, followed by the thermistor. As discussed in subsection 4.4.1, the TMP61 was the most accurate and linear thermistor that could be found. The only way to decrease its error is to calibrate each sensor separately, which would be time consuming. The error of the MPPC pin could also be removed with

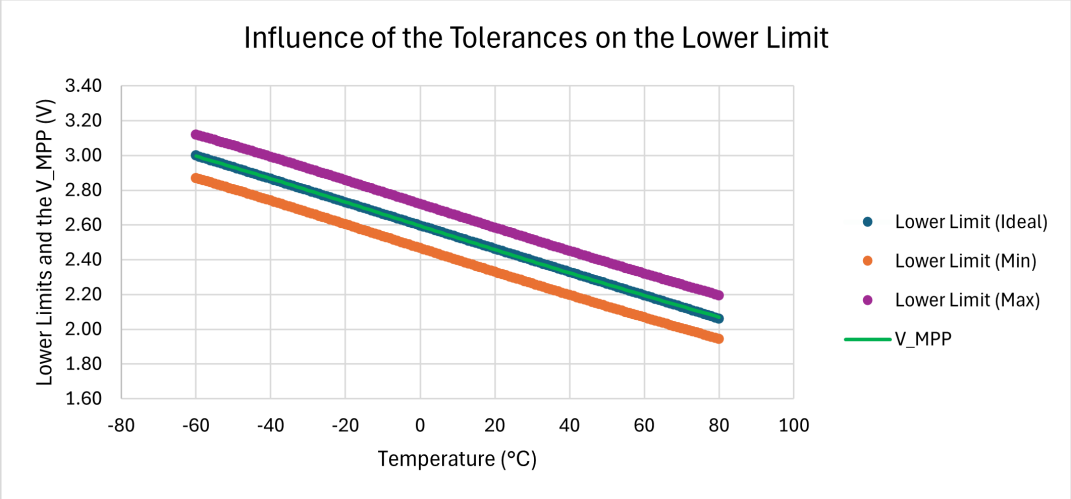


Figure 4.27: The typical, minimum, and maximum expected lower limit voltage compared to the V_{MPP} of the solar cells.

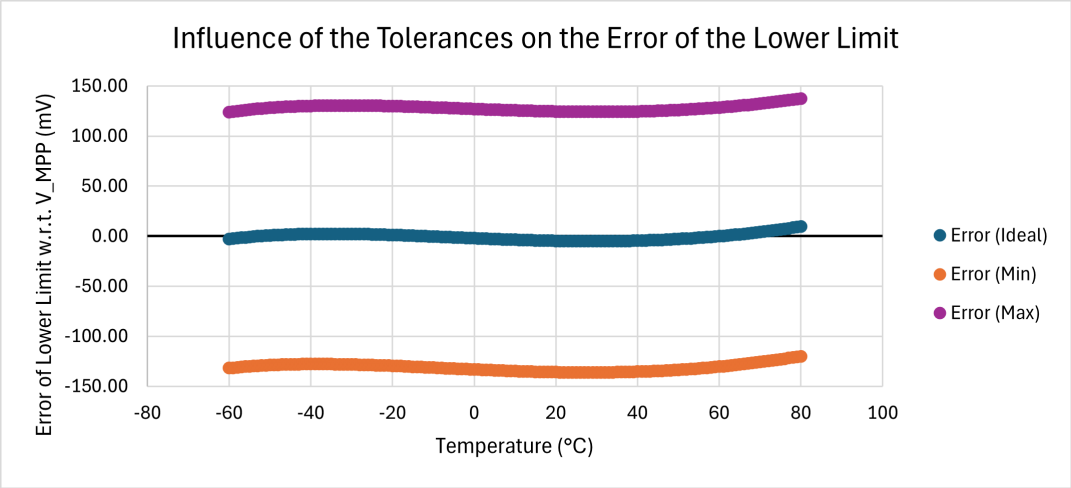


Figure 4.28: The typical, minimum, and maximum error between the expected lower limit and the V_{MPP} of the solar cells.

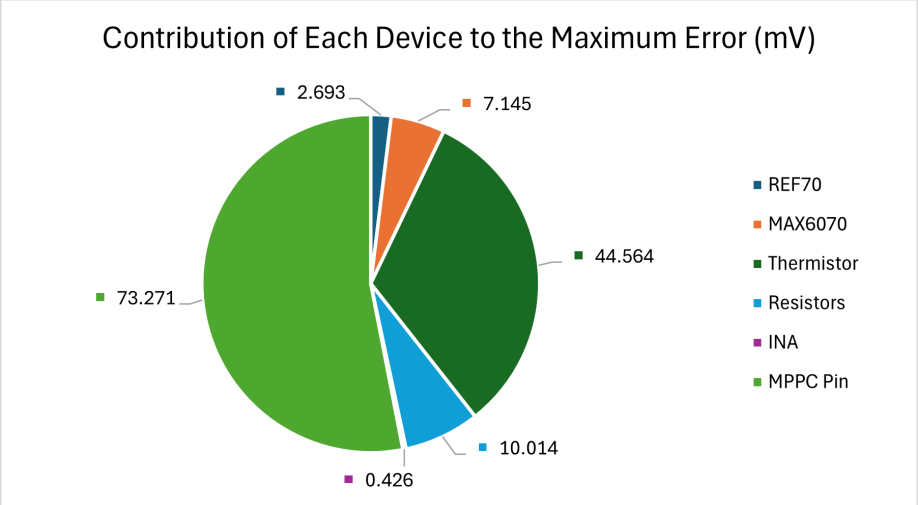


Figure 4.29: A breakdown of the maximum error between the expected lower limit and the V_{MPP} per component in the circuit. Both options for the voltage reference are included, so their contribution can be compared.

calibration. Here, it would be easier, since only one resistor in the constant-offset voltage divider would have to be replaced to account for the offset in the MPPC pin. However, in subsection 5.1.1, it will be investigated how accurate the MPPC pin is in practice and whether this calibration is necessary.

Both the REF70 and MAX6070 voltage references are also included in Figure 4.29. Of course, in the final circuit, only one of these devices will be used, so only one of these errors should then be taken into account. They are both included here only for the purpose of comparison. It is clear that the MAX6070 introduces a larger error than the REF70, but it is still relatively low compared to the error induced by the PTC. All other components introduce only a relatively small error, especially the AD8237. Therefore, these components can offer the desired functionality while maintaining high accuracy. To better quantify this accuracy, the error of the components will be converted to a power loss in subsection 4.4.6. There, it will be further investigated whether the components are a good fit for this circuit.

4.4.6. Power Efficiency of the Complete Circuit

The graphs shown in subsection 4.4.5 give an idea of how accurately the lower limit voltage set by the DC-DC converter will follow the V_{MPP}. However, the effect of the errors on the overall efficiency of the circuit is not immediately clear. This, together with the power consumption of all the components, will be further investigated in this subsection.

Power Consumed by Each Component

In order to obtain the power efficiency of the circuit, the power consumed by the various components first needs to be calculated. The power consumption of the voltage dividers can be obtained by $P = U^2/R$, where P is the power consumption, U the supply voltage of the voltage divider, and R the combined resistance of both resistors in the divider. To account for the worst-case scenario, the lowest resistance value of the PTC (at the lowest temperature of $-60°C$) was used, as well as the highest value for the voltage reference and the solar cell voltage.

Next, the power consumed by the voltage reference, including the two voltage dividers it powers (see Figure 4.22), needs to be calculated. This can be achieved by looking at the current flowing through the reference. For a series reference voltage, the input current is equal to the output current added to the quiescent current of the device [85]. Here, the output current is the current consumed by the two dividers. The input current is then multiplied with the supply voltage of the reference to obtain its input power. The supply voltage, as explained in subsection 4.4.4, is $3.3V$ in the case of one cell and $3.7V$ in the case of two. The power consumed by only the reference is then found by subtracting the power of the voltage dividers from the input power of the voltage reference.

The power consumed by the INA is simply its quiescent current multiplied with its supply voltage. Then, in the case of one cell, the output power of the boost converter is found by adding the input power of the INA and the voltage reference to the power consumed by the V_{IN} pin of the DC-DC converter (see Figure 4.23). This pin consumes up to $20mA$ and is powered by the same $3.3V$ supply, thus consuming $66mW$ [62]. The input power of the boost converter is then the total output power divided by its efficiency of 93% according to its datasheet [72]. The power consumed only by the converter itself is then simply its input power minus its output power.

In the case of two cells, the supply voltage of the INA and the voltage reference is taken from the VCC pin of the DC-DC converter, as again shown in Figure 4.23. This pin is the output of an LDO voltage regulator inside the LTC3119. The input of this regulator is the V_{IN} pin. So, to calculate the input power of the V_{IN} pin, a similar approach can be used as with the input power of the voltage reference. However, the quiescent current of this internal regulator is not mentioned in the datasheet of the LTC3119 [62]. Contrary to the voltage reference, the load current of this regulator is substantially larger than its quiescent current. A typical quiescent current would be tens to hundreds of μA, while the load current is tens of mA. This is because the VCC pin also provides the power for the internal circuitry of the LTC3119. Therefore, the power consumed by the internal regulator (ΔP) can be calculated using the equations shown below.

$$\Delta P = P_{IN} - P_{OUT} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT}$$

Assumption: $I_{IN} \approx I_{OUT}$, since $I_{IN} = I_{OUT} + I_Q$ and $I_Q << I_{OUT}$, with I_Q being the quiescent current. Therefore:

$$\Delta P = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

Here, V_{IN} is the highest possible V_{MPP}, which occurs at $-60°C$. This value was chosen to account for the worst case. V_{OUT} is $3.7V$, and I_{OUT} is the total current consumed by the voltage reference and the INA.

The DC-DC converter itself also consumes power. The LTC3119 has an efficiency of around 90% in the operating conditions of this system [62]. To account again for the worst-case, the highest possible input power is used in the calculation. This is the V_{MPP} at the lowest temperature ($-60°C$) multiplied with the current at the MPP, which is taken to be $500mA$ [46]. The power consumed by the DC-DC converter is then 10% of this input power.

Finally, an ideal diode will be present after the output of the DC-DC converter, as mentioned in subsection 4.1.2. It was decided to use legacy hardware for this component. The LTC4415 [95] has previously flown on Delfi-PQ and is therefore proven to work in flight. Its supply voltage range should be between $1.7V$ and $5.5V$, and this can be provided from the output voltage of the DC-DC converter, which is $4V$. The LTC4415 has an efficiency of more than 98%. This efficiency should be applied to the output power of the DC-DC converter. The ideal diode will thus consume $2\% \cdot 90\% = 1.8\%$ of the power produced by the solar cells.

Power Loss due to Inaccuracy of the Lower Limit Voltage

The power losses caused by all components in the circuit have been covered above. However, one final power loss is caused by operating away from the MPP. When the operating voltage of the solar cell decreases below the MPP, the current will slightly increase, as can be seen on the I-V curve in Figure 4.16. Therefore, a conservative estimate of the power loss caused by the largest negative error in the lower limit of the solar cell voltage can be obtained. This can be achieved by multiplying this minimum lower limit of the solar cell voltage with the current at the MPP. Subtracting this worst-case produced power from the typical produced power by the solar cells results in the power loss caused by the negative error.

On the other hand, when the operating voltage increases beyond the V_{MPP}, the current generated by the solar cell starts to decrease rapidly, which then causes the power to decrease as well. Because the relation between the current and voltage of the solar cell is difficult to obtain, it is hard to find the exact decrease in current, and thus the corresponding power loss. Therefore, it is assumed that close to the peak of the power curve, within the range of the minimum and maximum errors, the power curve is symmetric around the MPP. Following from this assumption, the largest positive error in voltage can also be subtracted from the typical value, and the resulting voltage can then be multiplied with the current at the MPP. This results in an estimate of the produced power when taking into account the largest positive error. Again, this can be subtracted from the typical produced power to obtain the power loss.

Power Loss Evaluation

All power losses are summarised in Table 4.8. The loss of each component is listed separately, as well as the loss due to the error between the lower limit set by the DC-DC converter and the V_{MPP} ("V_{MPP} Error"). This is done for both the one-cell and the two-cell configuration. In addition, the circuit containing the REF70 is compared to the circuit with the MAX6070 for both configurations. The differences in power losses due to the different voltage references are also presented separately. This difference is defined as the power loss in the REF70 circuit minus the losses in the MAX6070 circuit. To

Table 4.8: Summary of the power losses in the complete circuit for the one-cell and the two-cell configuration in order to compare the two possible voltage references.

	One-Cell Config. Power Loss [mW]			Two-Cell Config. Power Loss [mW]		
Component	**REF70**	**MAX6070**	**Difference**	**REF70**	**MAX6070**	**Difference**
Voltage Ref.	25.038	1.146	23.892	28.095	1.307	26.788
Voltage Dividers	0.359	0.359	0.000	0.543	0.543	0.000
INA	0.495	0.495	0.000	0.555	0.555	0.000
Boost Converter or Internal LDO	6.903	5.105	1.798	17.897	1.265	16.632
Ideal Diode	26.987	26.987	0.000	53.975	53.975	0.000
DC-DC converter	149.930	149.930	0.000	299.860	299.860	0.000
V_{MPP} Error	67.132	68.761	-1.629	135.439	138.698	-3.259
Total	276.845	252.784	24.061	536.364	496.203	40.161

better visualise the importance of each loss, they are also presented in pie charts shown in Figure 4.30. These pie charts only show the power loss breakdown for the one-cell configuration, but this is highly similar to the configuration for two cells.

The clear majority of the power loss is caused by the DC-DC converter. This is expected because almost all of the power produced by the solar cells goes through this device. An estimated 10% of this power will be lost due to the efficiency of the LTC3119, so to obtain an overall system efficiency of over 80%, this error should be the largest. The ideal diode also has a relatively large error, but, similar to the DC-DC converter, this component is crucial to the operation of the circuit.

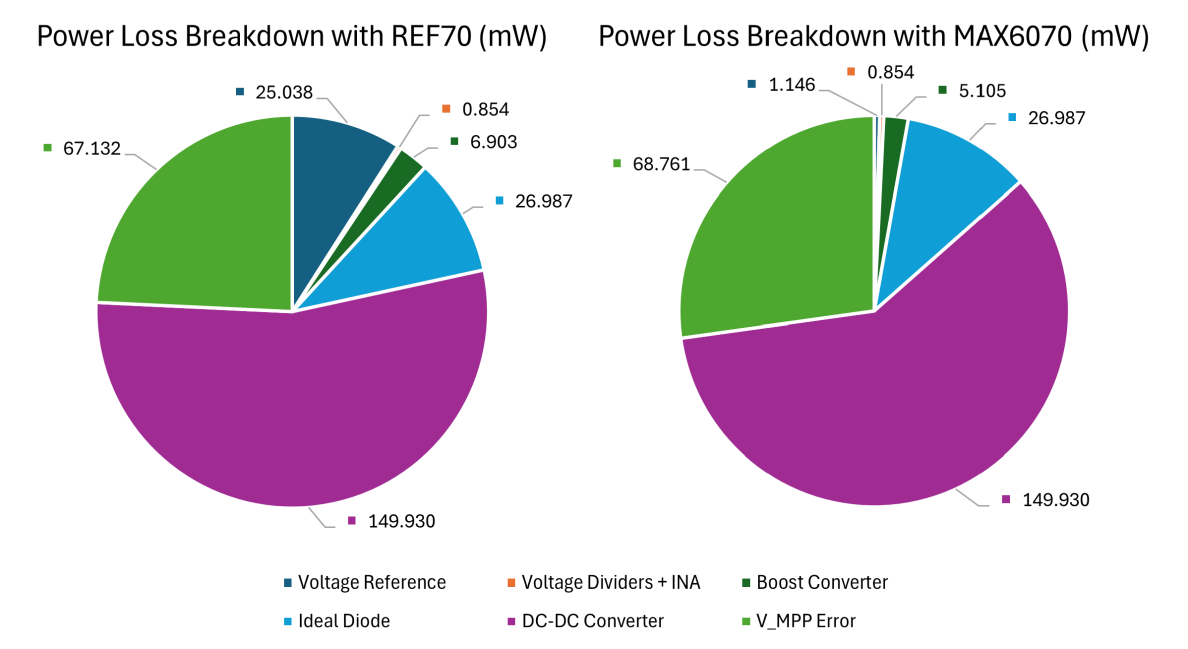


Figure 4.30: Visual comparison between the power loss breakdown of the circuit with the REF70 (left) and the MAX6070 (right) for the one-cell configuration.

The error in the lower limit also contributes significantly to the power losses. Here, the circuit containing the REF70 scores slightly better than the MAX6070. However, the REF70 consumes much more power to operate. In total, this results in a power consumption that is $24mW$ higher than with the MAX6070. For the two-cell configuration, it is even higher. Thus, it can be concluded that the MAX6070 is the preferred device and therefore, the REF70 will be discarded.

When the MAX6070 is selected, the components responsible for the temperature correction consume little power: they are almost not visible on the pie chart in Figure 4.30. Thus, the biggest area of improvement remains the error in the lower limit. As mentioned in subsection 4.4.5, the MPPC pin has the largest contribution to this error. However, calibration can be performed to eliminate this error. Without this error, the "V_{MPP} Error" decreases to $31.933mW$ for the one-cell configuration and to $65.004mW$ for the two-cell configuration. This more than halves this error, resulting in a total power loss of $215.95mW$ (instead of $252.784mW$) and $422.51mW$ (instead of $496.203mW$), respectively.

The resulting pie chart of this power loss distribution is shown in Figure 4.31. It shows that the control circuit itself, so without the irremovable ideal diode and DC-DC converter, only has a small contribution to the power loss when the MPPC pin error is ignored. In this way, the control circuit contributes 18.08% to the power loss for the one-cell configuration, and only 16.25% for the two-cell configuration.

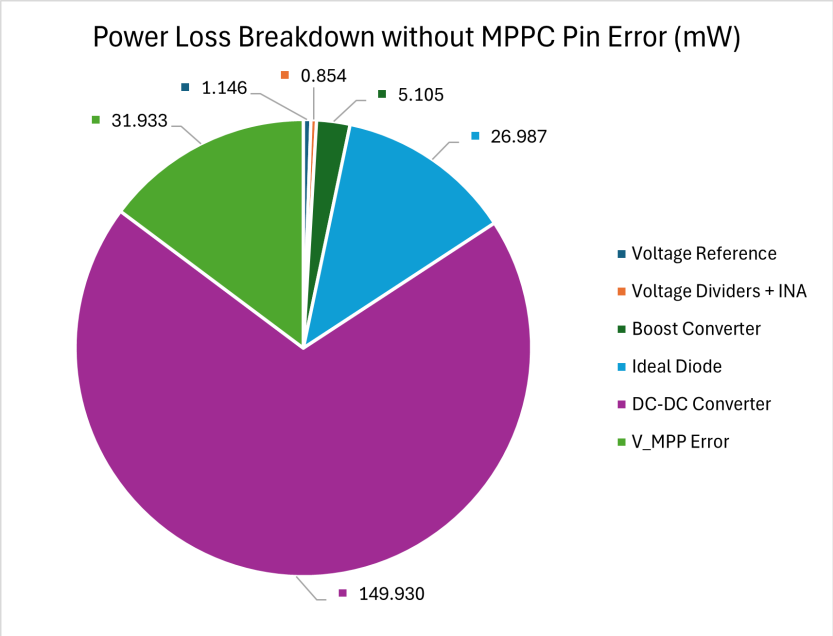


Figure 4.31: Power loss breakdown of the circuit with the MAX6070 for the one-cell configuration, with the MPPC pin error ignored.

Power Efficiency versus Temperature

The total power loss can be converted to a percentage of the total power produced by the solar cell. This was done for each temperature in the operating range. The error in the lower limit was calculated for each temperature, as well as its corresponding power loss. The power consumption of all components was assumed to be constant over temperature, and the worst case of this consumption was added afterwards. The total power loss was then divided by the ideal maximum power (the MPP) generated at each temperature to obtain the efficiency of the system.

The graph showing this efficiency over temperature for the one-cell configuration is given in Figure 4.32. As can be seen, the efficiency stays above 80% at all temperatures, satisfying REQ-102. In addition, when the error originating from the MPPC pin is eliminated, the efficiency even remains above 85%. For the two-cell configuration, these efficiencies are even slightly higher. This essentially verifies the design. Thus, the next step is to proceed with the schematic and layout of the MPPT Control PCB. Afterwards, the circuit can be manufactured and tested so that it can also be validated.

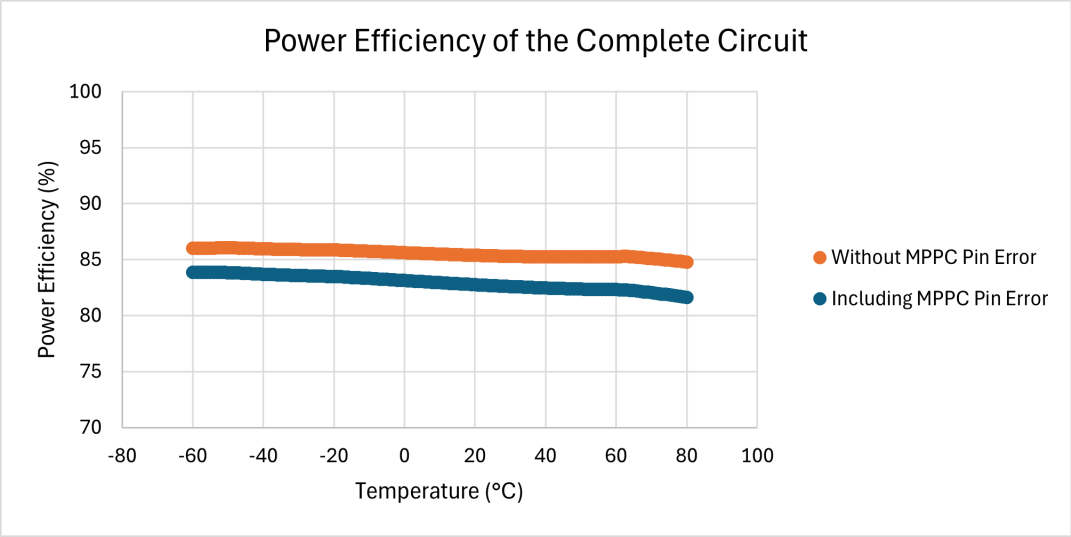


Figure 4.32: The power efficiency of the complete circuit over temperature for the one-cell configuration. The efficiency is also shown with the error at the MPPC pin ignored.

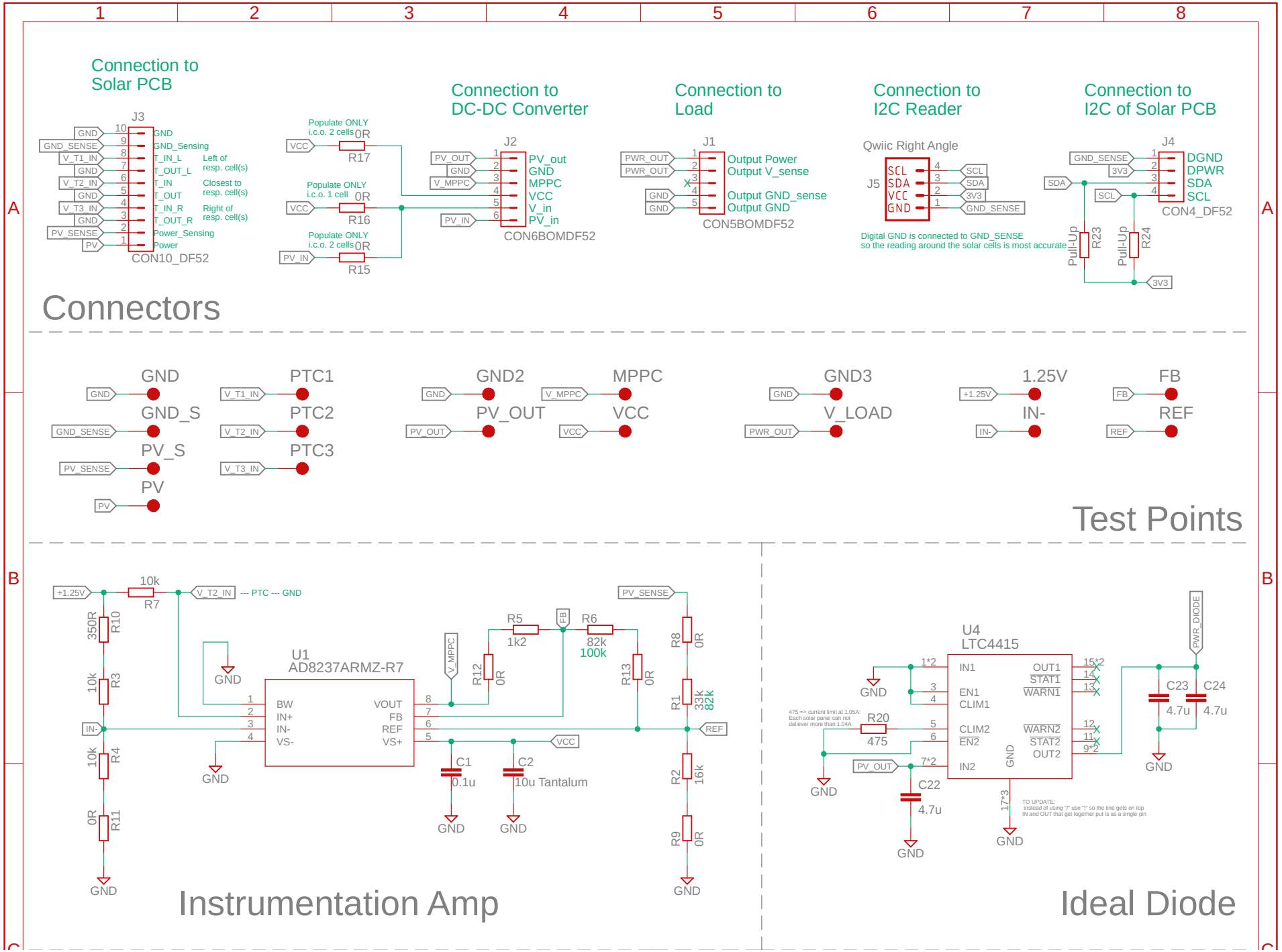
4.4.7. Schematic and Layout of the MPPT Control PCB

Throughout section 4.4, the circuit has gradually been developed and populated with components. Now that most design decisions have been made, a schematic can be created for the MPPT Control PCB. The schematic, which can be found in Figure 4.33, was too large to fit on one page and is therefore split over two pages. A detailed explanation of the schematic and the layout of the PCB is given in this subsection.

Only one schematic is presented, while there should be two different circuits: for the one-cell and for the two-cell configuration (REQ-201). However, since these two circuits are similar in most aspects, it was decided to design only one PCB that is compatible with both circuits. Having to order one PCB instead of two also has the added benefit of decreasing the cost. The distinction between the two configurations is then made by populating the PCBs differently. This will be clarified further in this subsection while discussing the schematic in more detail.

Schematic of the Connectors

At the top of Figure 4.33, all the connectors present on the MPPT Control PCB are shown. On the left, the connection to the Solar Cell PCB is presented. This is essentially a copy of one of the three 10-pin connectors on the Solar Cell PCB. From here, the solar power enters the MPPT Control PCB, as well as the voltage measurement of the solar cell(s), and the connections to the thermistors. As shown in Figure 4.22, one side of the thermistors is connected to ground, which is also indicated here in Figure 4.33. The other side is then the output of the thermistor voltage divider.


Connection to Solar PCB
J3
GND
GND_SENSE
V_T1_IN
V_T2_IN
V_T3_IN
PV_SENSE
PV
T_IN_L
T_OUT_L
T_IN
T_OUT
T_IN_R
T_OUT_R
Power_Sensing
Power
Left of resp. cell(s)
Closest to resp. cell(s)
Right of resp. cell(s)
CON10_DF52
Connection to DC-DC Converter
Populate ONLY i.c.o. 2 cells
Populate ONLY i.c.o. 1 cell
R17
R16
R15
0R
J2
PV_OUT
V_MPPC
PV_IN
PV_out
MPPC
V_in
CON6BOMDF52
Connection to Load
J1
PWR_OUT
Output Power
Output V_sense
Output GND_sense
Output GND
CON5BOMDF52
Connection to I2C Reader
Qwiic Right Angle
J5
SCL
SDA
3V3
Digital GND is connected to GND_SENSE so the reading around the solar cells is most accurate
Connection to I2C of Solar PCB
J4
DGND
DPWR
CON4_DF52
Pull-Up
R23
R24
Connectors
GND
GND_S
PV_S
PV
PTC1
PTC2
PTC3
GND2
MPPC
PV_OUT
VCC
GND3
V_LOAD
1.25V
IN-
FB
REF
Test Points
+1.25V
10k
R7
V_T2_IN
--- PTC --- GND
350R
R10
10k
R3
IN-
10k
R4
0R
R11
U1
AD8237ARMZ-R7
BW
IN+
IN-
VS-
VOUT
FB
REF
VS+
V_MPPC
R12
R5
1k2
R6
82k
100k
R13
PV_SENSE
R8
R1
33k
82k
R2
16k
R9
C1
0.1u
C2
10u Tantalum
Instrumentation Amp
U4
LTC4415
IN1
EN1
CLIM1
CLIM2
EN2
IN2
OUT1
STAT1
WARN1
WARN2
STAT2
OUT2
GND
PWR_DIODE
R20
475
C22
4.7u
C23
C24
4.7u
4.7u
Ideal Diode

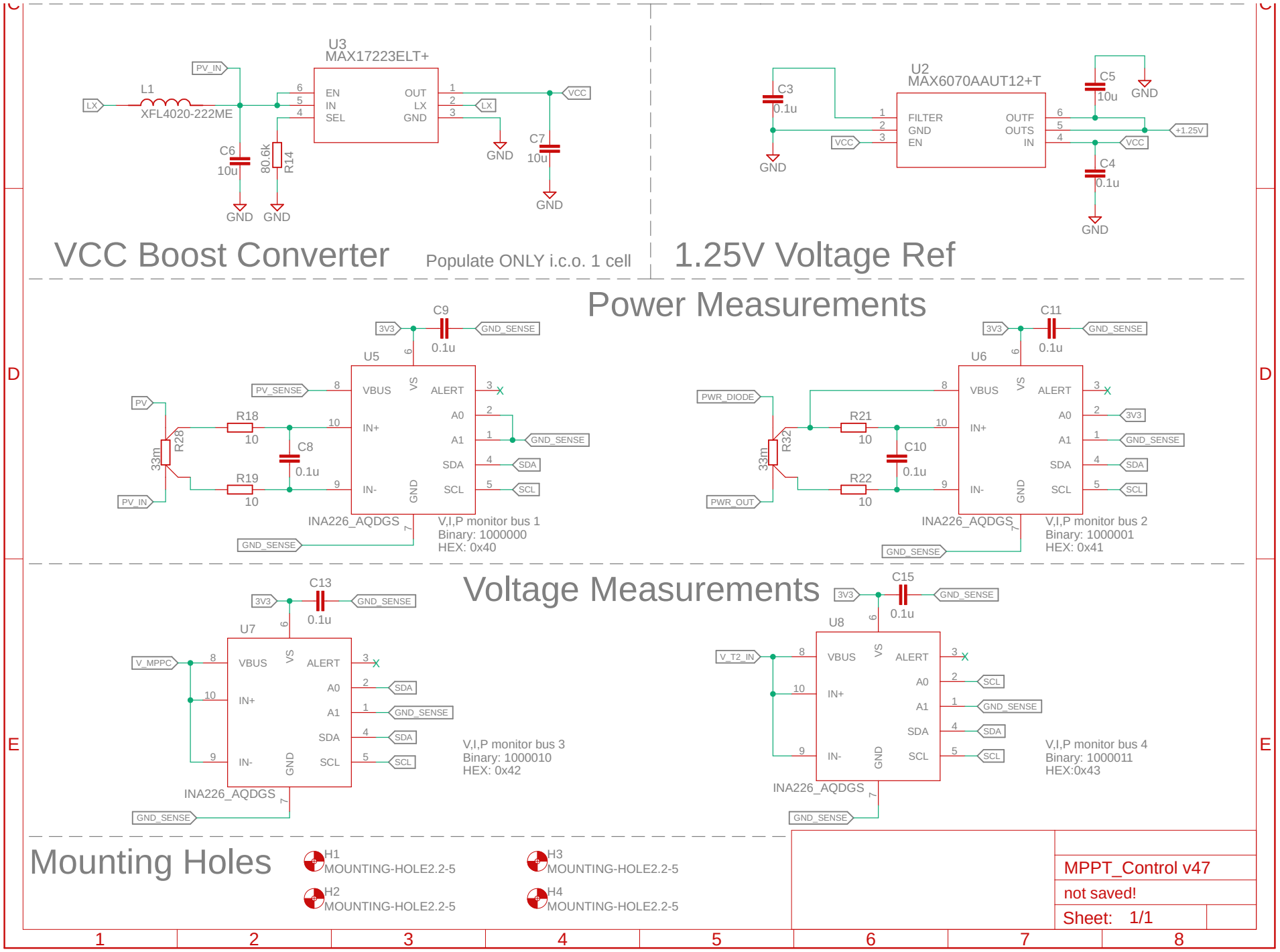


Figure 4.33: The electrical schematic of the MPPT Control PCB.

Proceeding to the right, the connection with the DC-DC converter is shown. As explained in Table 4.6, five pins are needed: for the incoming power, the returning power, a ground connection, the MPPC connection, and a separate pin that provides power to the V_{IN} pin of the LTC3119 to make sure it continues to operate, even when the voltage of the solar cell drops too low. However, as discussed in subsection 4.4.4, a sixth pin is needed to connect to the VCC pin of the LTC3119.

As explained in subsection 4.4.4, in the case of two cells, the VCC pin can provide power to the INA and the voltage reference and is therefore connected to the VCC net of the MPPT Control PCB. The V_{IN} pin can also be directly connected to the solar cells, because their combined voltage will always be above $2.5V$. However, in the case of one cell, the boost converter is necessary to boost the voltage of one cell above $2.5V$. This boosted voltage is then the VCC net of the MPPT Control PCB for the one-cell configuration and will also power the V_{IN} pin of the LTC3119. The connection from the VCC pin to the MPPT Control PCB for one cell is thus not needed. Figure 4.23 also shows these connections more clearly. To make the correct connection for the respective configuration, zero-Ohm resistors (jumpers) can be populated or left out. It is indicated on the schematic when to populate which jumper.

Next, the load connector is shown. For this, four pins were desired. Two for connecting to the load (one pin for ground and one for power) and two for having the possibility of performing a Kelvin measurement of the load voltage using an external multimeter. However, because the I2C connectors already have four pins, it was decided to have a connector with five pins for the load, with one pin remaining unused. In this way, it is impossible to plug in any cable incorrectly.

Finally, the two I2C connectors are shown. The connector on the right is used to link the I2C bus of the Solar Cell PCB with the bus of the MPPT Control PCB. Here, pull-up resistors are also present to ensure that the I2C bus functions correctly. The other I2C connector will link the bus to an I2C reader. This reader can then be plugged into a USB port on a laptop to read out all the data from the digital sensors linked to the bus. This connector is the same type as the one on the I2C reader. In this way, a pre-made cable can be used between them. All other connectors are from the same Hirose DF52 Series [56] as the connectors of the Solar Cell PCB.

Schematic of the Control Circuit Components

Below the test points, the INA is displayed. Surrounding it, the three voltage dividers can be found, as explained in Figure 4.22. For the thermistor divider, only the upper half is shown here, because the bottom half is on the Solar Cell PCB. For simplicity, it was decided that for the prototype of the MPPT Control PCB, only the thermistor closest to the respective solar cell(s) will be used for the temperature correction. Therefore, only the ”V_T2_IN” connection of the Solar Cell PCB connector is used.

All other voltage dividers consist of four resistors instead of the usual two. In most cases, these extra resistors are also jumpers and thus have no influence on the output voltage of the divider. The reason they are added to the circuit is to have the option to precisely adjust the division factor of the dividers by replacing these jumpers with (small value) resistors. This might turn out to be necessary after performing tests on the MPPT Control PCB. The solar cell voltage divider and the divider that sets the gain of the INA each also have a resistor that has two values written next to it. As explained in subsection 4.4.3 and 4.4.4, this is needed to be compatible with both the one-cell and the two-cell configuration. The green value represents the value needed in the two-cell configuration.

All connections of the INA [89] and the surrounding voltage dividers are routed according to Figure 4.22. In addition, the ”BW” pin should be connected to ground in order for the INA to have a gain close to one. Furthermore, the ”VS-” and ”VS+” pins supply power to the INA, and are thus connected to ground and VCC, respectively. Close to the ”VS+” pin, bypass capacitors are also present.

Next to the INA, the ideal diode [95] can be found. Only one channel is needed, in this case channel 2, so channel 1 is disabled by connecting all its related pins to ground. Channel 2 is enabled by pulling its ”EN2” pin to ground as well. A $475Ohm$ resistor is also connected to pin ”CLIM2” to limit the current through the diode to $1.05A$ to meet REQ-205. This current limit is only there in case of a failure, because the maximum current that could be produced by the circuit is $\sim 1.05A$. This happens when two cells operate at their MPP while the battery is at its lowest voltage of $2.7V$. Finally, bypass capacitors are placed close to the input and output pins of channel 2, and all other pins can be left floating.

Next, the boost converter [72] is presented. Again, this device and its surrounding resistor, inductor, and capacitors should be populated only in the one-cell configuration. The value of the resistor was chosen so that the output voltage of the converter would be the desired $3.3V$, as explained in subsection 4.4.4. The inductor was chosen to optimise the efficiency of the converter, as advised by the datasheet. Bypass capacitors are also included to smooth out the output voltage (VCC).

On the right side of the boost converter, the voltage reference [92] can be found. As explained above, it is powered by the VCC net. Its bypass capacitors are shown, as well as a capacitor between the ”FILTER” pin and ground. This additional capacitor further reduces the noise on the output. The ”OUTS” pin (Output Sense) can be connected to the trace coming out of the ”OUTF” pin (Output Force) at exactly the location on the PCB where the $1.25V$ is needed. The Output Sense can then compensate for a possible voltage drop in the Output Force trace.

Schematic of the Digital Multimeters

Below the boost converter and the voltage reference, two digital power sensors are displayed. It was decided to use digital sensors instead of four external multimeters, as discussed in subsection 4.1.2, to simplify the data-gathering process. However, the connectors on the MPPT Control PCB can still provide the connections required to make power measurements using external multimeters.

The digital power sensors measure the power coming from the Solar Cell PCB, and the power coming out of the ideal diode before it goes to the load. By subtracting these two power measurements from each other, the total power loss of the circuit, and thus its efficiency, can be obtained, as discussed in subsection 4.1.2. To measure the power, a voltage and current measurement are needed. The current is obtained by measuring the voltage drop over a shunt resistor. To have an accurate voltage measurement of the solar cells, their voltage is measured between the ”PV_SENSE” pin and the ”GND_SENSE” pin of the connector towards the Solar Cell PCB. Since all digital sensors should connect to the same ground, they are all grounded to ”GND_SENSE”.

The digital power sensors are both an INA226 [96]. These sensors were also used on Delfi-PQ and are therefore selected here again. On the MPPT Control PCB, they are powered and read out through the I2C connector. The same is true for the digital voltage sensors below, which are also INA226s. They are used to measure the MPPC voltage and the output voltage of the thermistor voltage divider. These four sensors are all on the same I2C bus and should therefore all have a different address. This can be achieved by having unique connections to the address pins ”A0” and ”A1”.

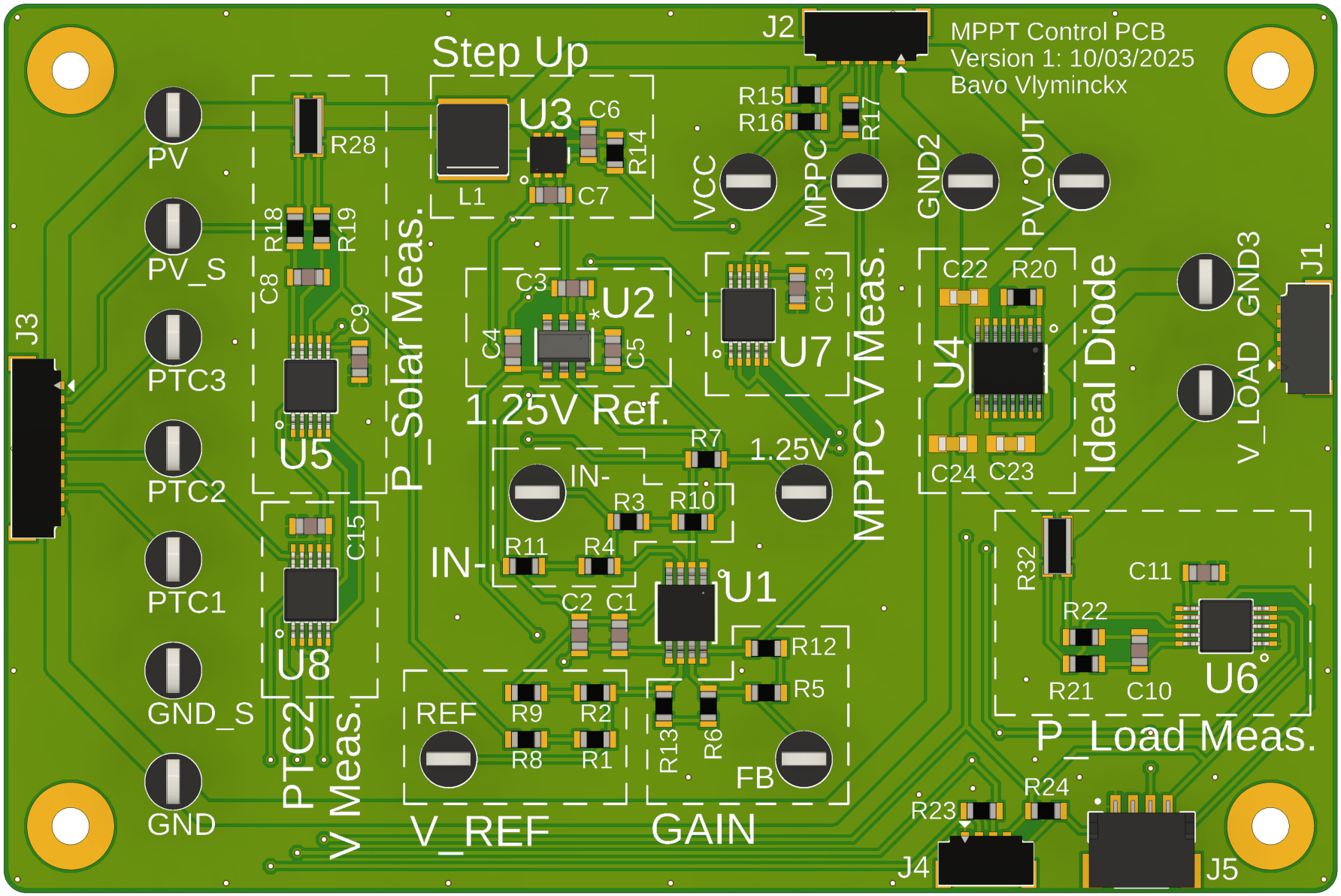


Figure 4.34: The layout of the MPPT Control PCB.

Layout of the MPPT Control PCB

After the schematic was completed, the layout could be created. It can be found in Figure 4.34. The total size of the MPPT Control PCB is $76mm$ x $51mm$. The Solar Cell PCB connector is placed on the left, the connector towards the DC-DC converter at the top, the load connector on the right, and the two I2C connectors at the bottom of the PCB. Each connector also has testing points for each relevant pin positioned close-by. The same is true for the input pins of the INA.

The components that are grouped together on the schematic are also grouped in the layout. This is indicated by the rectangles with the dashed lines. Each rectangle is also named for extra clarity. Only the group with the INA is subdivided into even more groups to make the distinction between the different voltage dividers. To keep a clear layout that is easy to debug if necessary, more space than necessary was left between the components and the groups. This means that the volume requirement (REQ-203) is not satisfied for the prototype. However, this version is not fully representative of the final circuit, since the DC-DC converter is not on this PCB. Therefore, it was decided to focus on the ease of manufacturing and replacing components, rather than adhering to the strict volume requirement.

Similarly to the Solar Cell PCB, the MPPT Control PCB has a ground plane on both layers. This ground plane is again connected to the ground of the digital sensors, which, as explained above, is also connected to the ”GND_SENSE” pin of the Solar Cell PCB connector. The MPPT Control PCB also has via fencing for shielding purposes. Furthermore, the traces and vias are the same size as on the Solar Cell PCB. The traces that carry the full current of the solar cells are also increased in size.

4.4.8. Production of MPPT Control PCB

Since the MPPT Control PCB has significantly more components than the Solar Cell PCB, it was decided to not solder it by hand. Instead, a stencil was ordered together with the MPPT Control PCB that has holes precisely at the same locations as the pads of the PCB. Thus, when the stencil is placed on top of the Solar Cell PCB, solder paste can be smeared over the stencil and will only be applied to the

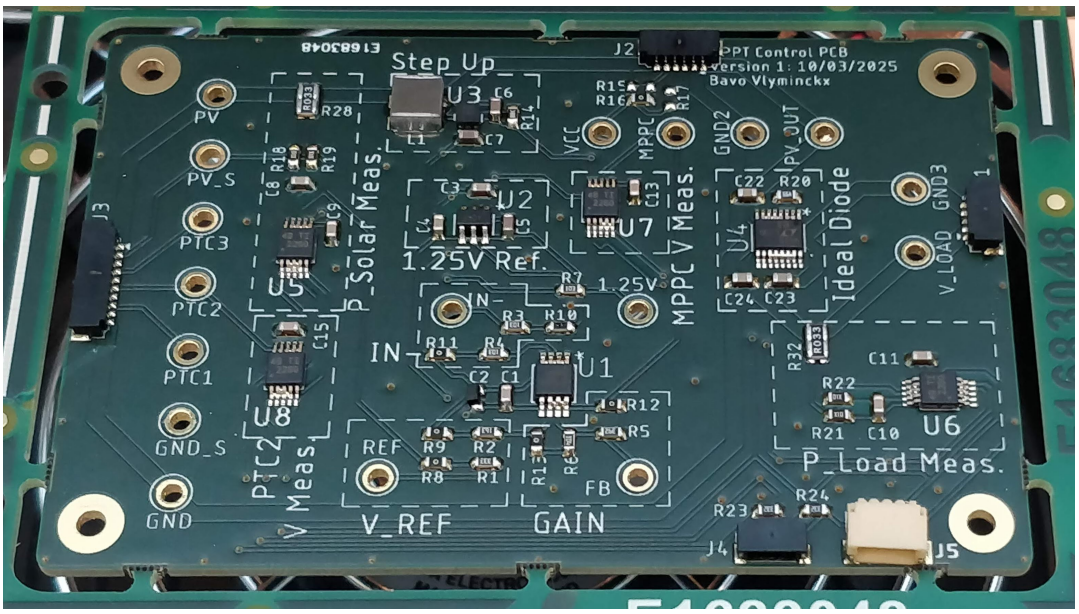


Figure 4.35: The Solar Cell PCB is soldered using a reflow oven.

pads. All components can then be placed on top of the solder paste at their correct location. After this, the populated PCB can be placed in a reflow oven to solder the components. The result is shown in Figure 4.35. As can be seen in this figure, the testing points are still missing. This is because they are through hole components and can therefore not be soldered using the reflow oven. For this reason, they were soldered by hand at the end.

When inspecting the soldered PCB closer, it can be concluded that most components are soldered well. However, the devices that have pins close to each other (U1 and U4 to U8) often had pins shorted. This can be clearly seen in Figure 4.36. This is due to the application of too much solder paste, which is likely caused by the stencil not being pressed down enough on the PCB.

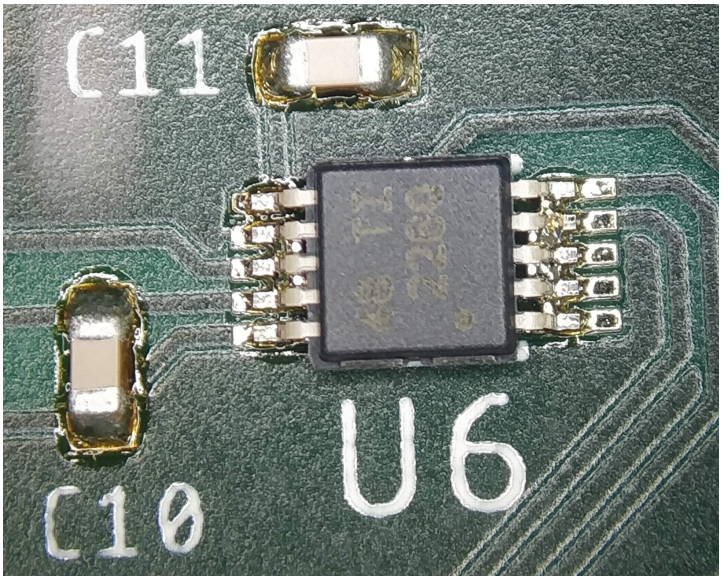


Figure 4.36: Many components had shorted pins after being soldered in the reflow oven.

It was also noticed that the pads of the boost converter (U3) are too small. Its pins are only accessible on the underside of the device [72]. Therefore, having pads that stick out from underneath this component allows the pad to be heated with a soldering iron which would allow the solder to melt. This is useful when the component would not be soldered adequately by the reflow oven and needs to be resoldered manually. Thus, for future versions, the pads of the boost converter should be made larger.

4.5. Test Set-up

After the acquisition and manufacturing of the Solar Cell PCB, the demo board with the LTC3119, and the MPPT Control PCB, it is time to test these PCBs to validate the design. For this, an existing test set-up will be reused. This set-up was built during previous work on solar cells [39]. In this work, it was verified that the V_{MPP} changes linearly with temperature.

Modifications to the Original Test Set-up

To test this linear relationship, a set-up was needed that could regulate its temperature. Therefore, the central part of the set-up consists of three Peltier modules that are held between two aluminium plates. These modules move heat from one (cold) plate to the other (hot) plate. A PCB that can accommodate two solar cells was bolted to the cold aluminium plate, while the hot plate is cooled by three fans. Each of the three Peltier modules has its own power supply, while the three fans are powered by a fourth power supply. This assembly is bolted to a PC monitor stand to hold it upright.

About one metre away from the solar cells, a powerful stage lamp is placed. This is the artificial sun that can mimic the solar radiation in LEO. This lamp will also quickly heat up the test set-up when turned on. Therefore, the set-up only needs cooling capabilities to regulate its temperature. To further reduce the rate at which the test stand heats up due to the lamp, a heat shield covers the entire set-up, except for the solar cells. This shield is made from cardboard and wrapped in baking paper to resist the heat.

The old set-up had only one temperature sensor on the PCB with the solar cells. This sensor could be read out using an Arduino that sent the data to a laptop. The solar cells were connected to two multimeters to measure their current and voltage. These multimeters were also read out using a laptop. From here, the solar power would flow directly to a resistive load called the Rheostat, which has a variable resistance of $1Ohm$ to $10Ohm$. By sweeping through this resistance range, the MPP of the solar cells could be found. This was repeated at different temperatures to find the relation between the V_{MPP} and temperature.

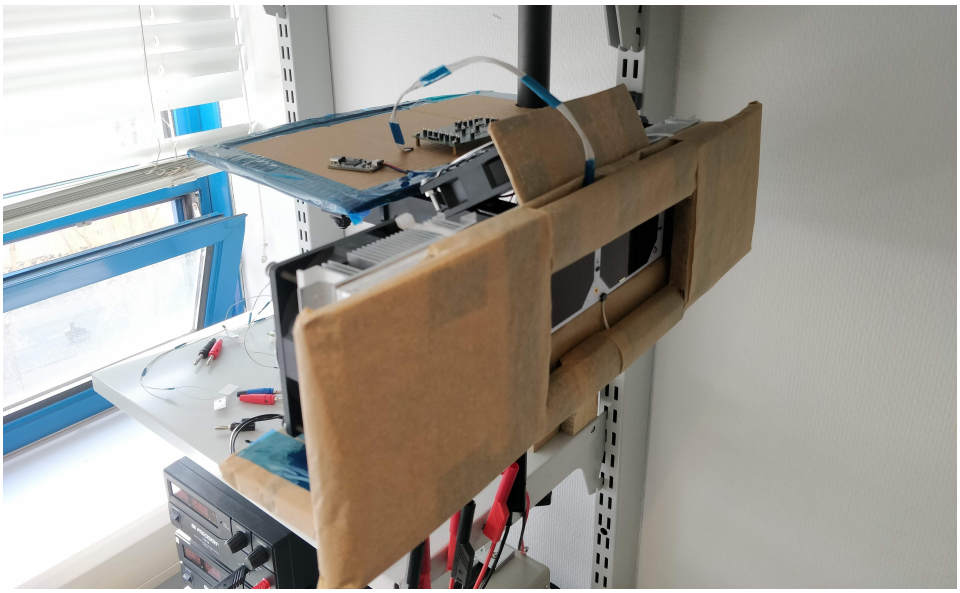


Figure 4.37: A new heat shield and platform to place PCBs on was made for the test set-up.

For the new set-up, some modifications were needed. Firstly, a new, more sturdy heat shield was made that could be bolted to the set-up, instead of taped on like the previous shield. In addition, a small platform was made from cardboard directly behind the test stand, on which the demo board and the MPPT Control PCB could be placed. The original PCB with the solar cells is also replaced by the Solar Cell PCB. New thermal paste was applied between the cold plate and the Solar Cell PCB to ensure it could be properly cooled. The new test stand is shown in Figure 4.37.

Integration of the MPPT Testing Circuit

As mentioned in subsection 4.4.7, the data from the digital sensors on the Solar Cell PCB and the MPPT Control PCB will be read using a COTS I2C reader. The reader used here is the ”Adafruit FT232H” [97] and will connect to the I2C bus via the MPPT Control PCB and send the data over USB to a laptop. On this laptop, the data can then be read by a Python script. The FT232H will also be placed on the small platform behind the test stand. The cable between the FT232H and the MPPT Control PCB can be a COTS cable, since the connectors on both PCBs are the same.

All other connectors are from the Hirose DF52 Series [56]. Pre-crimped cables compatible with these connectors were bought, so assembling cables became trivial. The cable between the Solar Cell PCB and the MPPT Control PCB, as well as the cable connecting the I2C bus between these PCBs, simply connects each respective pin of its two connectors to each other. The cable between the load and the MPPT Control PCB has two pins populated with the pre-crimped cables that both connect to a banana plug: one for power and one for ground.

The connector between the MPPT Control PCB and the demo board has six pre-crimped cables inserted into the DF52 connector on the side of the MPPT Control PCB. Three of these connect on the other side to a banana plug: one for the solar power flowing to the DC-DC converter, one for the converted

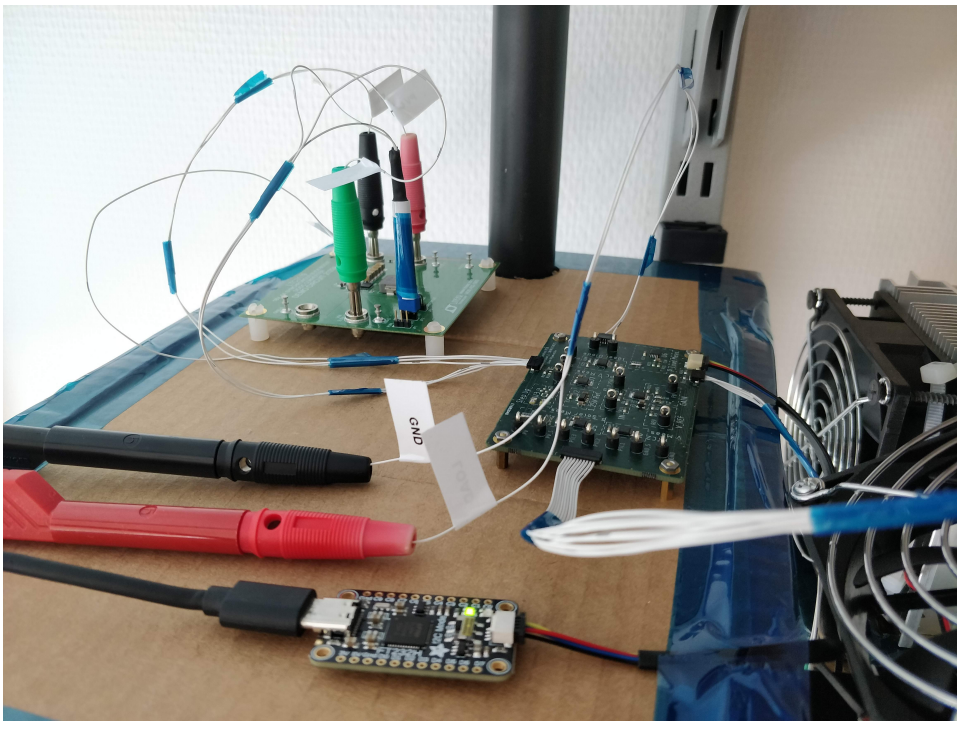


Figure 4.38: The MPPT Control PCB with all cables attached necessary to test the full MPPT circuit.

power flowing back, and one for ground. These banana plugs can be plugged into the demo board in their respective sockets. The ”VIN” connection is soldered to a capacitor pad right next to the ”VIN” pin. For the MPPC and VCC connections, a custom connector was made that is compatible with the 3-pin connector on the demo board that can enable or disable the MPPC function. The top two pins are shorted and connect to the MPPC cable, while the bottom pin connects to the VCC cable. A picture showing the MPPT Control PCB with all these cables attached to it is shown in Figure 4.38.

The above explanation shows how the complete MPPT circuit is integrated. However, as explained in subsection 4.1.2, the solar cells also need to be characterised. For this, the solar cells should be directly connected to the load, only with two multimeters in between to measure the power, as shown in the bottom of Figure 4.4. Thus, a separate 10-pin connector could be made that can connect the Solar Cell PCB to multimeters and then to the Rheostat.

However, the MPPT Control PCB already has a digital power sensor between the connectors going to the Solar Cell PCB and the demo board. Therefore, a cable was made that is compatible on one side with the connector that normally goes to the demo board. On the other side, it simply has two banana plugs: one for power and one for ground. These banana plugs can connect to the Rheostat, while the power measurement can be done using the digital sensor to characterise the cells.

The digital sensors present on the MPPT Control PCB can be used to measure the solar power, the power going to the load, and the PTC and MPPC voltages. However, other voltage measurements might be needed to debug the PCBs. In addition, it is interesting to see how much noise is present on certain voltages. Therefore, an oscilloscope with four voltage channels is placed next to the test set-up. A picture showing the complete set-up can be found in Figure 4.39.

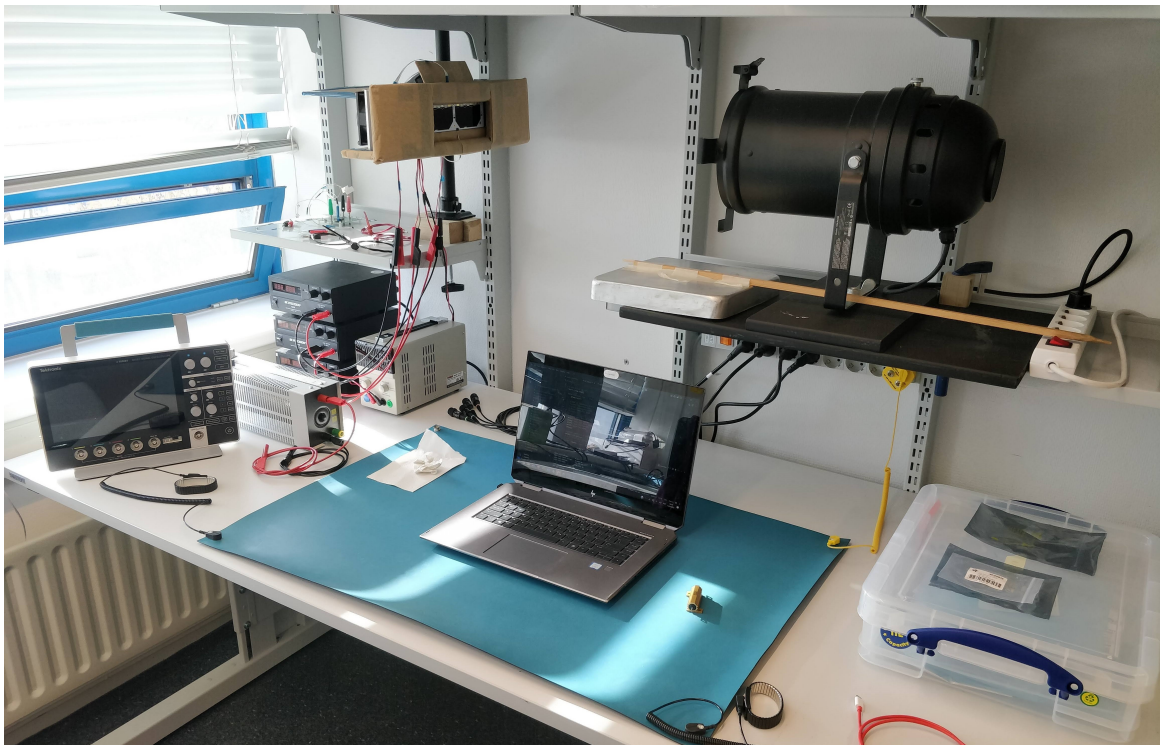


Figure 4.39: The full test set-up, including the lamp on the right, the test stand with the solar cells on the left, power supplies for cooling underneath the test stand, and the Rheostat and an oscilloscope to the left of the power supplies.

5 Results and Discussion

To validate the design of the circuit, it should be extensively tested. Therefore, in section 5.1, the MPPT circuit will undergo various tests that will highlight the remaining problems. Afterwards, in section 5.2, the requirements are revisited and an overview of which requirements are met is presented.

5.1. Prototype Test Results

Various tests will be performed on the prototype circuit. Firstly, in subsection 5.1.1, simple checks will be done to ensure that all components are correctly connected to each other. Then, the efficiency of the circuit will be tested under various conditions in subsection 5.1.2. Here, a problem was found that was further investigated in subsection 5.1.3 and eventually resolved in subsection 5.1.4. Afterwards, in subsection 5.1.5, the circuit will be further characterised. Finally, the accuracy of the lower limit set by the MPPC pin will be investigated in subsection 5.1.6.

5.1.1. Initial Multimeter Measurements

Before testing the complete circuit, the MPPT Control PCB was tested separately to ensure that it would not damage the other parts of the system. Firstly, continuity checks were performed between all voltage rails of the MPPT Control PCB to check for short-circuits. After no problems were found, the MPPT Control PCB was connected to the Solar Cell PCB and the lamp was turned on. While the lamp was on, the voltages at the power rails were measured and all showed the designed values.

The correct voltages on the MPPT Control PCB meant that it was time to connect the DC-DC converter to it. However, no load was connected to the output of the converter yet. Again, when the lamp was turned on, all voltages were still at their designed values, including an output voltage of the DC-DC converter of $4V$. Subsequently, a high resistance load was connected to the output, which means that the solar cells will still operate under their MPP, but now with current flowing through the entire circuit. The output of the DC-DC converter remained at $4V$, with a current of $400mA$ from the solar cells. For reference, the solar cells produce around $500mA$ when operating at their MPP.

To investigate the accuracy of the MPPC pin, a lower resistance load was connected, which requires more power from the solar cells than they can produce (around $1.2W$ each). As explained in subsection 4.3.2, the MPPC pin acts as a lower limit for the solar voltage when more power is required than can be produced. Thus, with a low resistance load, the MPPC pin should remain at $798mV$, even when the required power continues to increase. This was investigated with various low resistance loads, and the MPPC pin always remained at $798mV$ exactly. Therefore, the graphs in subsection 4.4.6 that exclude the error at the MPPC pin are more accurate, even without calibrating the circuit.

Finally, the functionality of the ideal diode was tested. For this, the battery of the satellite was charged and connected to the output of the circuit. The lamp was also turned off, so the solar cells did not produce any power. Since the ideal diode can be powered through any of its input or output pins [95], the battery should activate the diode through its output pin. This was also observed: the output of the ideal diode was at $4V$, the battery voltage, while the input of the ideal diode remained at $0V$. Thus, it can be concluded that the ideal diode works and that the circuit is protected from reverse current.

The circuit has been shown to produce the correct output voltage when fully integrated. Therefore, in the following subsection, the functionality and efficiency of the complete circuit will be further tested. These tests were performed both for the configuration with one cell and with two cells. However, for conciseness, only the data for the one-cell configuration will usually be shown. Only relevant differences between the two configurations will be mentioned.

5.1.2. Initial MPPT Functionality Test

After ensuring that all connections are routed as intended, the functionality of the circuit can be tested. The goal of this first test is to demonstrate the functionality of the MPPC pin. It needs to be investigated that the input voltage of the DC-DC converter is limited to the desired voltage, which is the V_{MPP}. This test will therefore check whether the behaviour of the MPPC pin is as expected and whether the control circuit forces the correct voltage onto the solar cells.

The test is performed in the following way. The Rheostat, which is essentially a variable resistor, is connected to the output of the MPPT Control PCB. Then, by sweeping through the resistance range of the Rheostat while the lamp is illuminating the solar cells, measurements can be taken while the cells operate under, at, and over the MPP. These measurements are made by the digital multimeters on the MPPT Control PCB. They measure the voltage and current at the solar cells, as well as at the load. These results are shown in Figure 5.1. Based on this, the power produced by the cells and consumed by the load are calculated. By comparing these, the efficiency of the entire circuit is calculated, which is displayed in Figure 5.2.

For the first tests, it was decided to not solder the thermistors on the Solar Cell PCB yet. Instead, a fixed, $10kOhm$ resistor was soldered in place of the PTCs. This means that the circuit always wants to force the same voltage onto the solar cells when the load demands more power than the cells can provide. This simplifies the testing process, since one variable, the temperature, does not yet need to be taken into account. For the TMP61, $10kOhm$ corresponds to a temperature of $27.6°C$. At this temperature, the V_{MPP} of the cells is $2.411V$. This is thus the voltage at which the solar cells should operate when the demanded power is higher than the cells can produce. More details about the test set-up can be found in the list below.

Summary of the Test

- **Test Type:** Resistance sweep, solar cells operate under, at, and over the MPP
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat
- **Configuration:** Left cell, thermistor fixed at $10kOhm$, DC-DC converter in fixed frequency mode
- **Measured:** Voltage, current, and power at the solar cell and load, overall power efficiency

Explanation of the Results

The solar cell voltage shown in Figure 5.1 behaves as according to the explanation in subsection 4.3.2. When the load resistance is high, and thus the demanded power is low, the solar voltage is higher than the V_{MPP}. As the power demand increases when moving to the right, the solar voltage decreases. At some point, the solar voltage drops so low that the MPPC pin activates. From this point on, the solar cell voltage remains essentially constant due to the lower limit set by the MPPC pin. As a consequence, the load voltage starts to decrease. This is not a problem as long as it does not decrease below $1.7V$

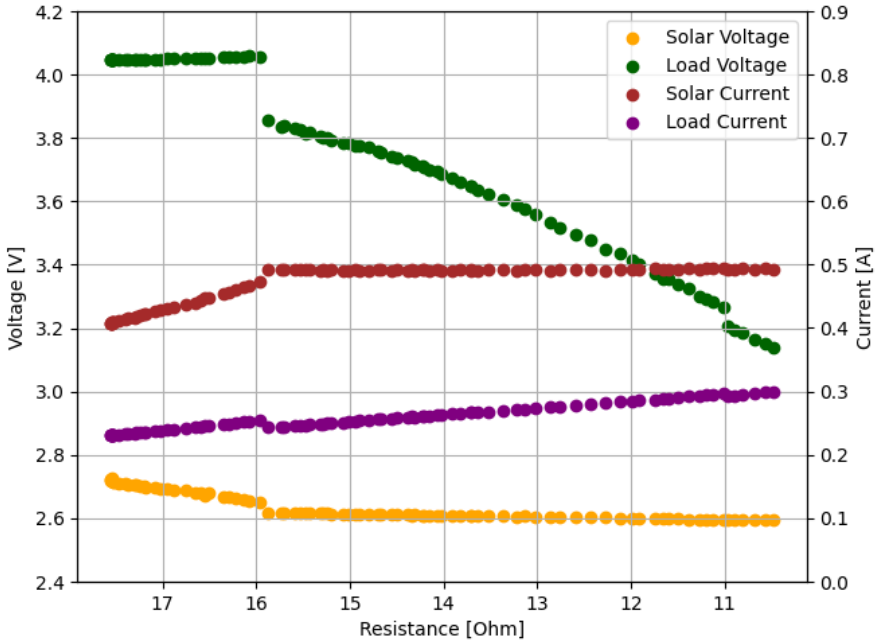


Figure 5.1: Voltage and current measurements of the solar cell and load while sweeping the load resistance.

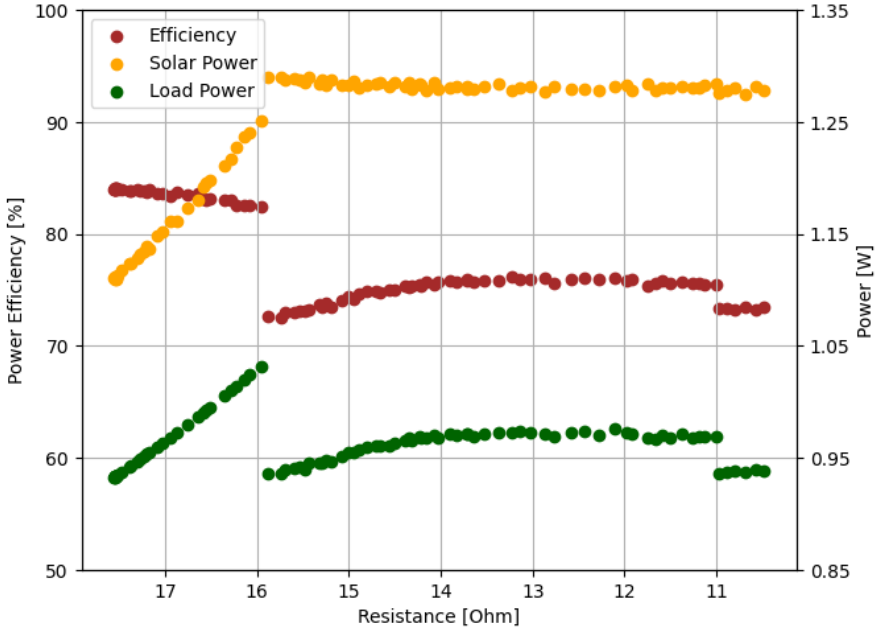


Figure 5.2: Power (efficiency) measurements of the solar cell and load while sweeping the load resistance.

because the ideal diode needs at least $1.7V$ to operate, as explained in subsection 4.4.6. Looking at Figure 5.1, this is unlikely to occur as there is still large margin before $1.7V$ is reached. Figure 5.2 also shows expected behaviour: both the input and output power increase until the MPPC pin activates. Afterwards, they remain fairly constant because the solar power should now be close to the MPP.

The circuit appears to operate mostly as designed. However, the solar voltage at which the MPPC pin activates is too high. As mentioned above, the solar cell voltage should be limited to $2.411V$, while here

it is limited to $2.6V$. This can in part be explained by the fact that the solar cells, the control circuit, and the DC-DC converter are all on different PCBs. They are connected by wires that have a resistance, so when current flows through them, a voltage drop occurs over the wires. This also causes a discrepancy between the grounds of the different PCBs.

The digital multimeters are connected to the digital ground of the Solar Cell PCB. Because only a small amount of current flows through this ground, there is a significant difference between the digital and regular ground of the MPPT Control PCB. This difference will also change with the amount of current flowing through the wires between the PCBs. Therefore, it is difficult to accurately measure the absolute value of a voltage using the digital multimeters. It is still possible that the control circuit calculates the lower limit incorrectly, but this is difficult to know for certain. Therefore, it is recommended that the next version of this MPPT circuit will consist of a single PCB so that all grounds are the same.

Another undesirable behaviour is visible in both Figure 5.1 and 5.2: each curve jumps in y-value around the transition between operating under the MPP and operating over it. This is especially visible in the voltage and power curve of the load, as well as in the overall efficiency. This results in the efficiency being partly below 80%, which violates the efficiency requirement (REQ-102). Therefore, it is important to first find the cause of this jump before continuing to evaluate and characterise the circuit.

5.1.3. Investigating the MPPC Transition Problem

In the previous subsection, an unexpected jump in voltages was observed that occurs at the transition point between the cells operating below the MPP and operating above the MPP. Therefore, the differences between these regions need to be further investigated. By comparing the workings of the circuit in these two regions, it is likely that the cause of this jump will be found.

In essence, only one part of the circuit changes at this transition point: the activation of the MPPC pin. As explained in subsection 4.3.2, the MPPC pin only has an influence on the VC pin, and therefore on the duty cycle of the DC-DC converter, when the voltage at this pin is too low. The reason for this is the diode in between the VC pin and the output of the comparator behind the MPPC pin. This diode prevents the MPPC pin from influencing the VC pin voltage when the voltage at the MPPC pin is above $798mV$. Only after the transition point, when the MPPC voltage drops below $798mV$, the diode allows the MPPC pin to influence the VC voltage.

Thus, the only difference between the two regions on either side of the jump in voltages is whether the MPPC pin has control over the VC voltage. Therefore, the next test will investigate the MPPC and VC voltages around the transition point. In addition, the solar cell voltage and load voltage will also be measured since the jump in these voltages is what is being investigated in the first place. These measurements will be made using an oscilloscope to obtain more detailed results.

Summary of the Test

- **Test Type:** Oscilloscope measuring at the MPPC transition
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat
- **Configuration:** Left cell, thermistor fixed at $10kOhm$, DC-DC converter in fixed frequency mode, Rheostat at $\sim 15Ohm$ (i.e. at the transition point)
- **Measured:** Voltage at solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green)

Explanation of the Results

Both Figure 5.3 and 5.4 show the four measured voltages at the transition point. These plots are actually identical; they only have a different order of plotting because the curves overlap. It can be said with certainty that the middle of the plot is the transition point, since the drop in the load voltage is equal to the jump shown in Figure 5.1. Thus, on the left side of the graph, the MPPC pin is not active, while it is active on the right side.

To better understand these two figures, the periodic wave in the load voltage needs to be explained first. This wave has a period of $10ms$ and is mostly observed on the right side of the figure, at which point the MPPC pin is active. The wave is caused by the lamp that illuminates the solar cells. This lamp is powered by a wall socket that operates at $50Hz$. To obtain DC power from this socket, the lamp likely has a full-bridge rectifier, or similar. This rectifier still has a ripple on its output that now has twice the frequency of the wall socket. This means a frequency of $100Hz$, which exactly corresponds with the $10ms$ wave in the load voltage.

When the MPPC pin is not active, only the FB pin has control. This pin ensures that the load voltage remains at $4V$, and can operate at a substantially higher frequency than $100Hz$. Therefore, the wave is not visible in the load voltage when the MPPC pin is not active. In this case, however, the wave is visible on the solar cell voltage, albeit more chaotic due to a high amount of noise on this voltage. When the MPPC pin is active, on the other hand, the solar cell voltage is now controlled by the circuit. This means that the wave disappears from the input voltage, but now becomes visible on the output voltage, because the FB pin no longer has full control.

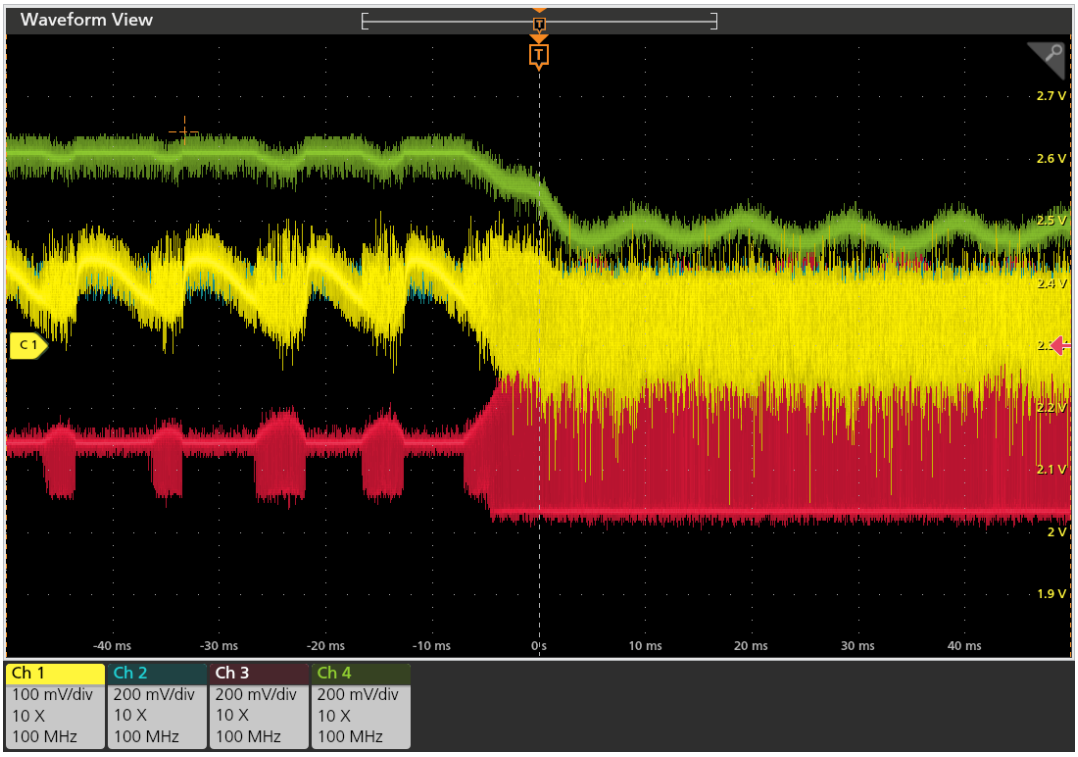


Figure 5.3: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) around the MPPC transition point.

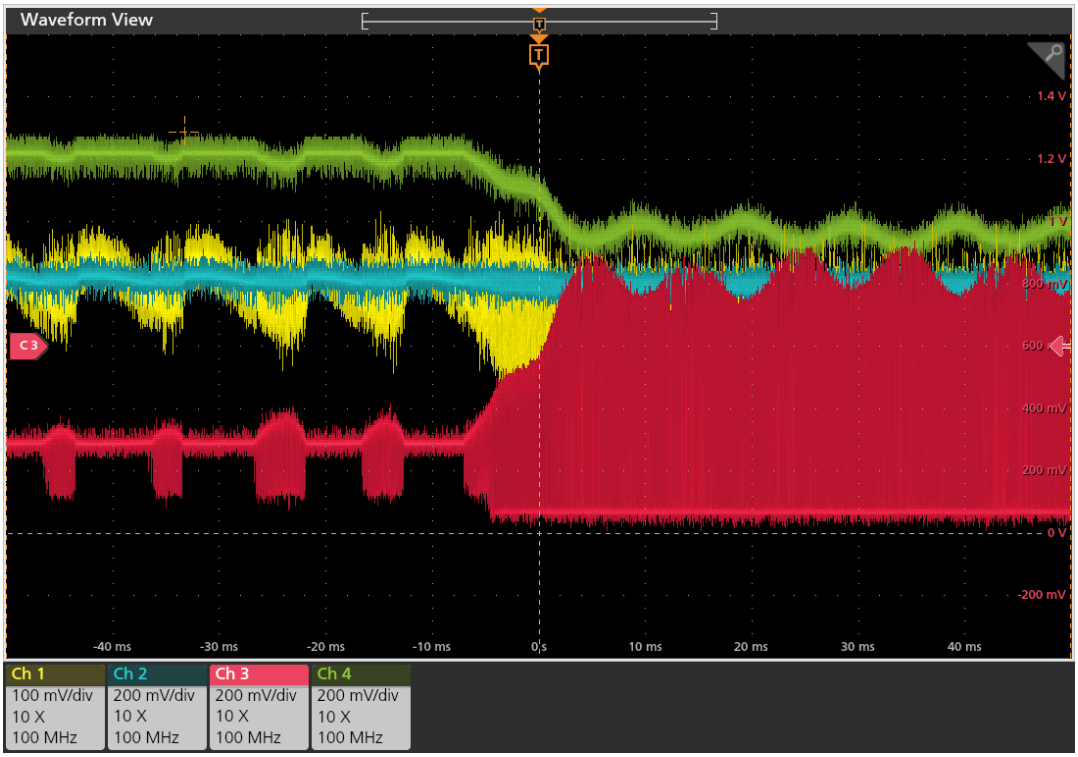


Figure 5.4: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) around the MPPC transition point.

This $10ms$ wave actually comes in handy because it makes it possible to observe the behaviour of the circuit at the transition. On the left side of Figure 5.3, the load voltage is kept at $4V$ by the FB pin. However, due to the wave, at some points the solar cell provides less power than the load requires. At these points, the MPPC pin will activate. This is clearly demonstrated by the reaction of the VC pin. The large ”blocks” of noise on the VC pin show that the activation of the MPPC pin has a large effect on the VC voltage. When the MPPC pin is active, the load voltage also drops slightly, as predicted in subsection 4.3.2.

A large amount of noise is present on the VC voltage when the MPPC pin is activated. The VC voltage controls the duty cycle and therefore also the solar cell voltage. This explains why the solar voltage is so noisy, especially on the right side of the graph. Here, the MPPC pin is fully activated and stays active, resulting in an enormous amount of noise on the VC pin and thus also on the solar cell voltage. This noise on the VC voltage is especially large compared to the noise when only the FB pin is active.

Zooming in on the VC Voltage

To better understand the origin of the noise on the VC pin, the VC voltage was zoomed in on the time scale while the MPPC pin is active. The resulting graph is presented in Figure 5.5, which shows an interesting behaviour of the system. All four voltages, but especially the solar and VC voltages, follow a sort of oscillatory pattern. During a large part of this repeating pattern, the VC voltage is at its minimum. This happens because the solar cell voltage is below the limit set by the MPPC pin. When the VC voltage is at its lowest possible voltage, the current through the inductor of the DC-DC converter decreases, possibly even to zero. This causes the output capacitors to discharge, slowly lowering the output voltage. At the same time, the solar cell can charge the input capacitors, which occurs more quickly because of the lower input capacitance.

Figure 5.5: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) close to the MPPC transition point at a smaller time scale.

When the voltage of the solar cell reaches again above the lower limit, the MPPC function deactivates. Consequently, the VC voltage rises rapidly and actually reaches its maximum possible value. This causes the inductor to conduct a large amount of power again, more than the solar cell can provide. Therefore, the solar voltage quickly drops. When it eventually drops below the lower limit, the MPPC function reactivates. The VC voltage then reacts by decreasing sharply to its minimum value again, and the cycle repeats.

The behaviour described above is, in essence, desired. When the voltage of the solar cell is too low, the MPPC function activates and pushes the solar voltage above the lower limit. However, this MPPC control loop acts too quickly and appears unstable. The VC pin should not drop to its minimum value when the solar voltage is too low. Instead, it should adapt gradually to changes in the voltage of the solar cell and the MPPC pin, so that the solar voltage itself also changes more gradually and oscillates less. Thus, the reaction of the VC pin to the activation of the MPPC pin must be slowed down.

5.1.4. Resolving the MPPC Transition Problem

In subsection 5.1.2, it was found that the overall efficiency of the circuit jumps at the MPPC transition point, leading to a decreased efficiency. Then, in subsection 5.1.3, it became clear that this jump around the transition point is caused by noise on the VC pin of the DC-DC converter. When zooming in, it was found that this pin reacts too quickly and needs to be slowed down. In this subsection, a solution that can reduce or possibly remove these jumps is proposed and tested.

The easiest way to slow down the VC pin is by adding a larger capacitance to this pin. However, this will slow down the FB pin as well, since the output of the FB pin is also connected to the VC pin.

This is not desirable because the FB loop should operate quickly to prevent the output voltage from overshooting $4V$ so that the battery will not be damaged. In addition, when only the FB pin is active, the DC-DC converter appears stable. This can be seen in Figure 5.3, where the solar voltage, and especially the VC voltage, is significantly less noisy when only the FB pin is active.

Thus, no capacitance should be added to the VC pin. In addition, the input of the DC-DC converter, which is the solar voltage, already has a capacitance greater than $100\mu F$. Therefore, the only remaining option is to slow down the MPPC pin voltage. This can be achieved with a low-pass RC filter. Interestingly, when observing the intended use of the MPPC pin, an RC filter is already present there. This consists of a capacitor from the MPPC pin to ground, as well as the resistors that make up the voltage divider that sets the lower limit. These are shown on the original schematic of the demo circuit board (Figure 4.17) as C24 and as R10 and R11, respectively.

Because the MPPC function follows a dynamic V_{MPP} that changes with temperature, it is not desired to have a fixed lower limit. Therefore, resistor R10 was removed to give the control circuit full control over the MPPC voltage, as explained in subsection 4.3.4. In essence, this removed the resistance from the RC filter that keeps the MPPC control loop stable. This desired resistance can be restored by placing a resistor in series between the output of the control circuit and the MPPC pin. However, this means that R11 also must be removed. Otherwise, this series resistor will essentially form a voltage divider together with R11, which would modify the output of the control circuit before it reaches the MPPC pin. According to the datasheet of the DC-DC converter [62], the series resistor should be between $50kOhm$ and $250kOhm$. After performing experiments with various resistance values in this range, the optimal values were found to be $60kOhm$ for the configuration with one cell and $120kOhm$ for two cells.

After removing R11 and restoring the RC filter with a resistor in series between the output of the INA and the MPPC pin, the stability of the circuit can be tested. This is done similarly to subsection 5.1.3: by using an oscilloscope to observe the behaviour of the circuit at the transition point. The same voltages are measured to obtain a direct comparison.

Summary of the Test

- **Test Type:** Oscilloscope measuring at the MPPC transition
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat
- **Configuration:** Left cell, thermistor fixed at $10kOhm$, DC-DC converter in fixed frequency mode, Rheostat at $\sim 15Ohm$ (i.e. at the transition point), $60kOhm$ resistor in series in front of the MPPC pin
- **Measured:** Voltage at solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green)

Explanation of the Results

When observing Figure 5.6, it is immediately clear that the noise in the solar cell voltage and the VC voltage is reduced substantially compared to Figure 5.3. It was difficult to obtain on the oscilloscope the exact moment of the full transition, so the behaviour after the transition is shown in Figure 5.7. In this plot, the same substantial reduction in noise is visible. The VC voltage is still more noisy when the MPPC function is active compared to when only the FB pin is active, but it is now significantly lower than before the fix. The solar cell voltage now has almost the same amount of noise regardless of whether the MPPC pin is active.

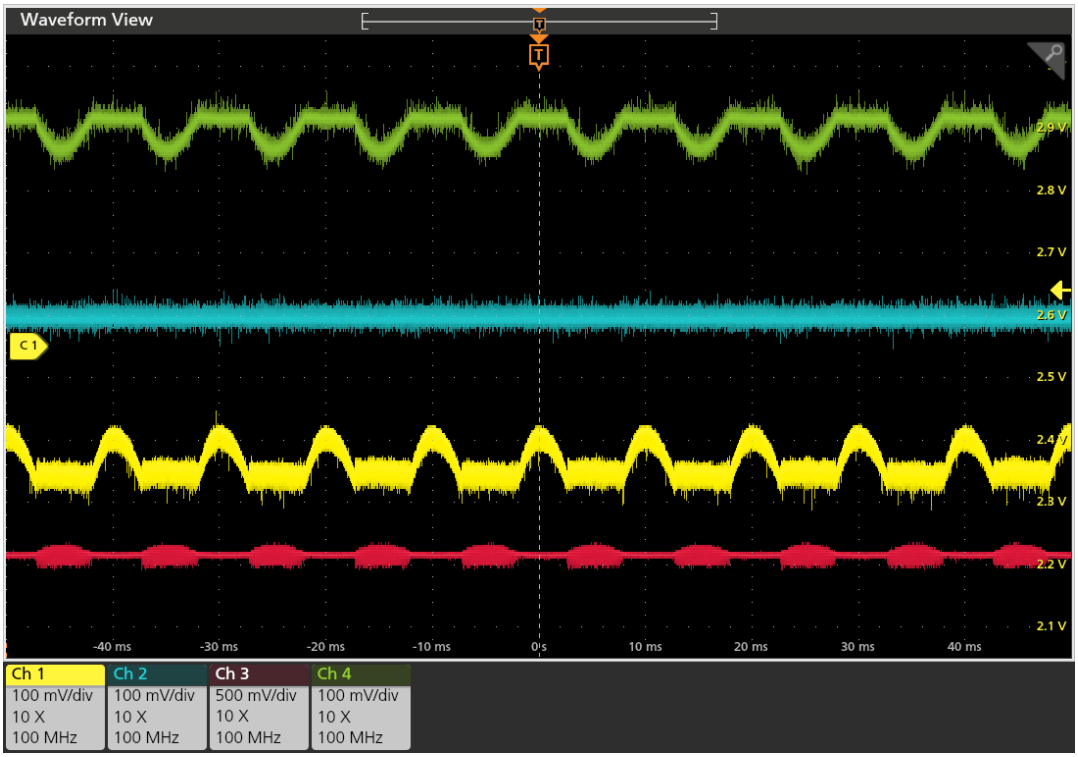


Figure 5.6: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) around the MPPC transition point after restoring the RC filter in front of the MPPC pin using a $60kOhm$ resistor.

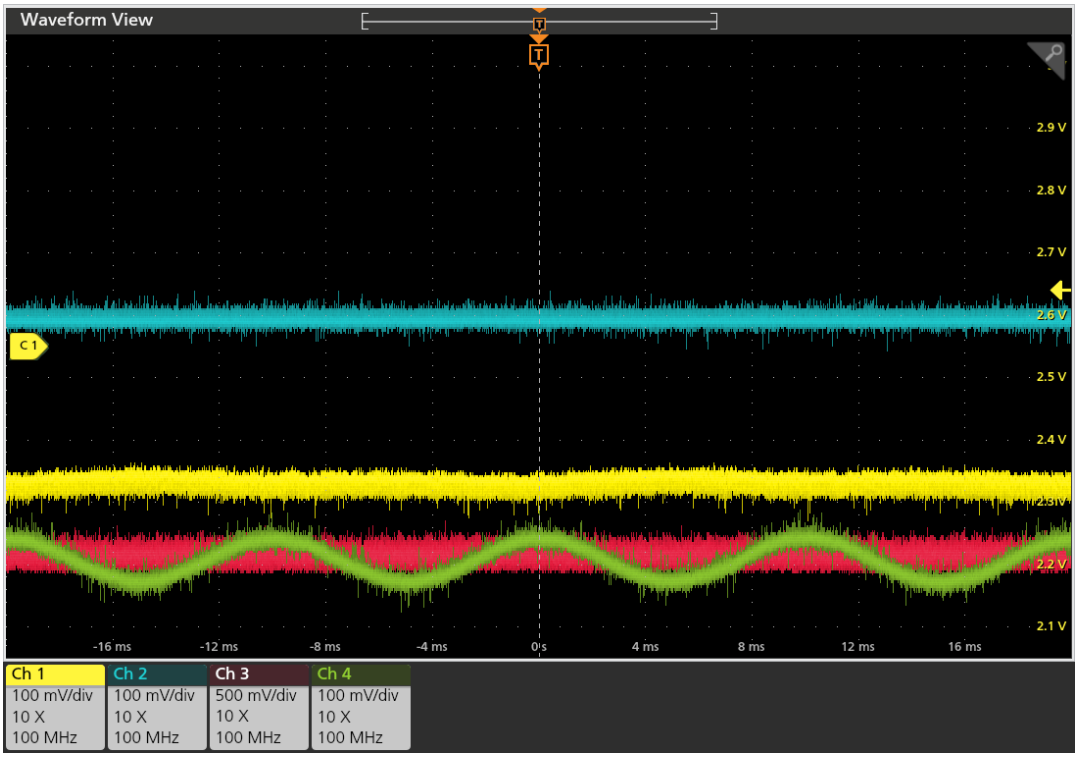


Figure 5.7: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) when the MPPC pin is active after restoring the RC filter in front of the MPPC pin using a $60kOhm$ resistor.

When zooming in on the time scale, the improvement becomes even clearer. In Figure 5.8, the voltage at the VC pin appears to be stable, although some white noise remains. In addition, the solar cell voltage is approximately a straight line, which means that it is highly stable. This is an enormous improvement compared to Figure 5.5, where both voltages oscillate and appear unstable.

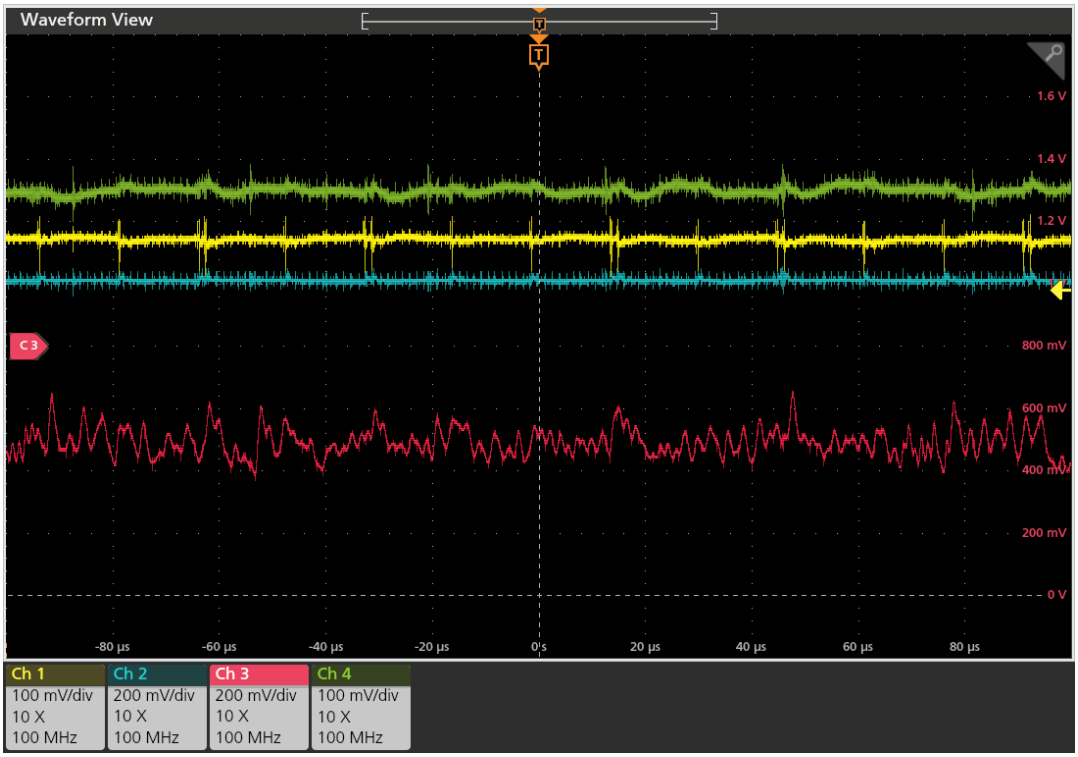


Figure 5.8: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) close to the MPPC transition point at a smaller time scale after restoring the RC filter in front of the MPPC pin using a $60kOhm$ resistor.

Effect of the Proposed Solution on the Circuit Efficiency

With the VC pin appearing stable, the efficiency of the overall circuit can be measured again. This is done below in the exact same way as in subsection 5.1.2; the only difference is the removal of R11 and the addition of the $60kOhm$ resistor.

Summary of the Test

- **Test Type:** Resistance sweep, solar cells operate under, at, and over the MPP
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat
- **Configuration:** Left cell, thermistor fixed at $10kOhm$, DC-DC converter in fixed frequency mode, $60kOhm$ resistor in series in front of the MPPC pin
- **Measured:** Voltage, current, and power at the solar cell and load, overall power efficiency

Explanation of the Results

In both Figure 5.9 and 5.10, all jumps that could be observed in subsection 5.1.2 are no longer visible. Besides this, all desired functionalities are still present. Therefore, it can be safely concluded that this problem concerning the jumps in the graphs is resolved. In addition, the overall efficiency of the circuit

now remains above 80% at all times. For the configuration with two cells, the efficiency even remains above 85% for almost the entire range of resistances. At first glance, this would mean that the efficiency requirement (REQ-102) is satisfied. However, this efficiency measurement does not take into account how well the MPP is tracked. This will be further elaborated upon in section 5.2.

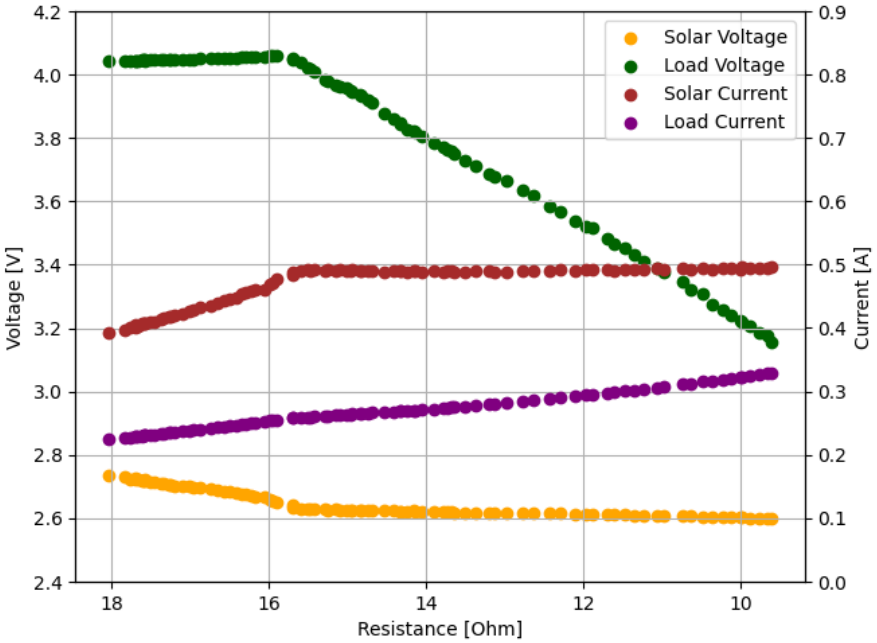


Figure 5.9: Voltage and current measurements of the solar cell and load while sweeping the load resistance after restoring the RC filter in front of the MPPC pin using a $60kOhm$ resistor.

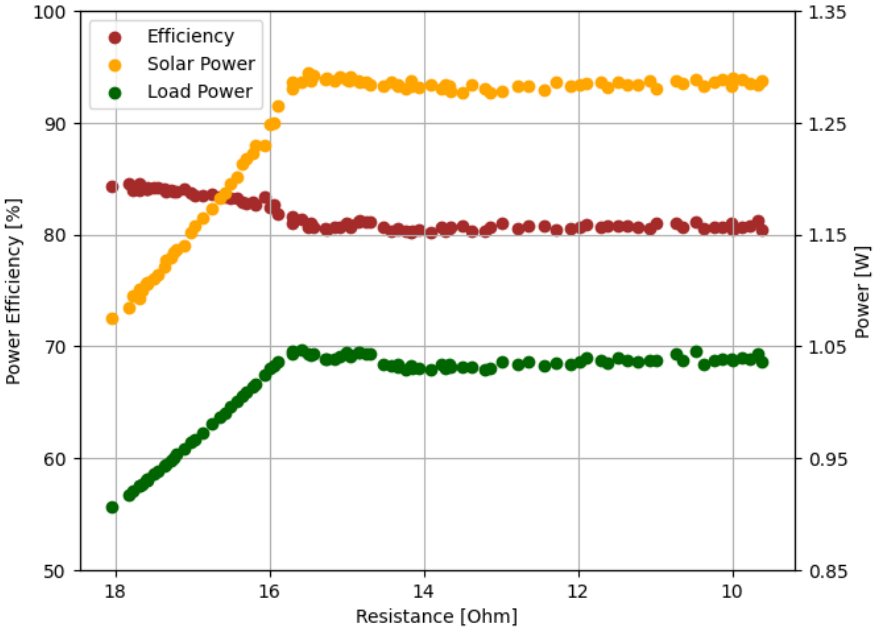


Figure 5.10: Power (efficiency) measurements of the solar cell and load while sweeping the load resistance after restoring the RC filter in front of the MPPC pin using a $60kOhm$ resistor.

5.1.5. Characterising the MPPT Circuit

The circuit now behaves mostly as expected, except for the absolute value of the solar cell voltage when the MPPC pin is active. However, as explained in subsection 5.1.2, this might be due to the difference in ground between the three PCBs, and should be further tested with the next iteration when all circuitry is on the same PCB. Therefore, the remaining tests for this iteration are mainly used to characterise the circuit to determine how well it performs its functions.

Start-up and Shut-down Behaviour

The first characterisation test is to investigate how quickly the circuit responds to changes in irradiance. This was tested using an opaque black sheet of plastic that was held in front of the lamp to block its light from hitting the solar cells. By quickly dropping this sheet, the solar cells quickly go from zero to maximum irradiance. This is faster than simply turning the lamp on because the lamp takes some time to reach its maximum illumination. In addition, a cut-out was made in the sheet. In this way, the irradiance can quickly go from zero to the maximum twice in a row. A picture of the opaque sheet in action can be found in Figure 5.11. To investigate how quickly the circuit reacts, the voltages of the solar cell and the load are measured. The voltages of the MPPC pin and the VC pin are also measured to obtain a better understanding of the behaviour of the circuit.

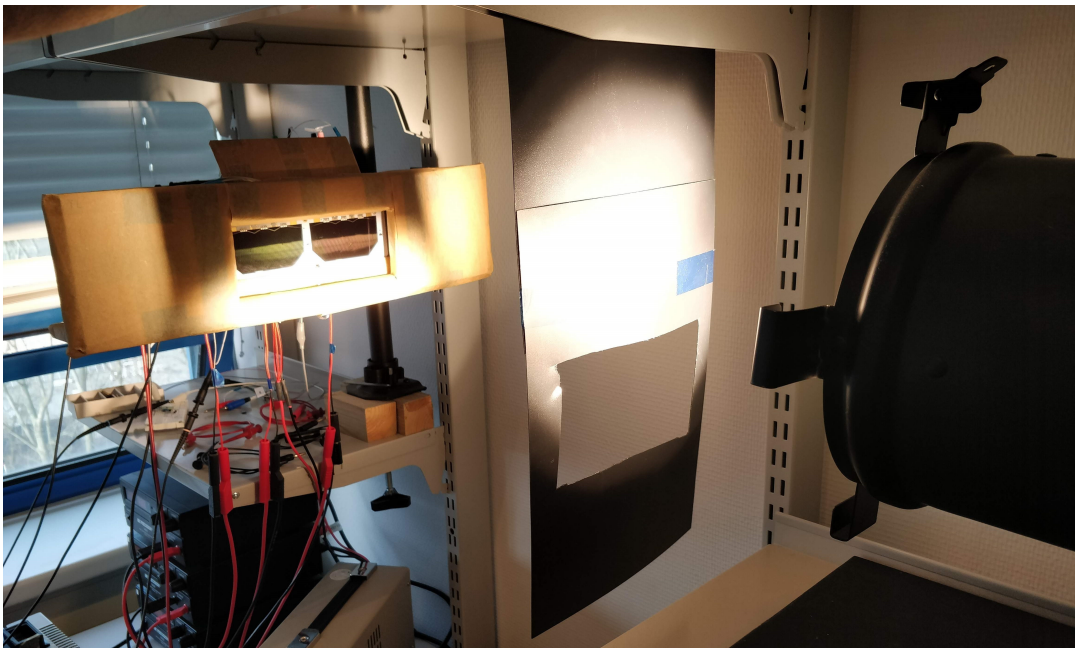


Figure 5.11: The opaque black sheet is used to quickly vary the irradiance as seen by the solar cells.

Summary of the Test

- **Test Type:** Oscilloscope measuring while an opaque sheet is dropped in front of the lamp
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat
- **Configuration:** Left cell, thermistor fixed at $10kOhm$, DC-DC converter in fixed frequency mode, Rheostat at $\sim 17Ohm$, $60kOhm$ resistor in series in front of the MPPC pin
- **Measured:** Voltage at solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green)

Explanation of the Results

On the left side of Figure 5.12, the sheet blocks all light from the lamp. However, there is still a small voltage on the solar cells. This is caused by the lights in the room. All other voltages are at zero at this point, so the lights in the room cannot provide enough energy to power the circuit. Just before $-80ms$, the MPPC voltage jumps to its correct value in accordance with the solar voltage at that point. Thus, from here, the circuit starts to receive more power, which means that this can be regarded as the point where the lamp starts to illuminate the cell.

After this point, the solar cell voltage starts to rise quickly, with the MPPC voltage increasing accordingly. Then, the VC voltage suddenly wakes up, marking the start-up of the DC-DC converter. At this point, the solar voltage stops increasing because the load is now demanding power through the DC-DC converter. Interestingly, the VC voltage appears quite noisy here, similar to when the MPPC pin is active. However, the load is $17Ohm$, which should not require the MPPC pin to be active. This can be explained by the output capacitors of the DC-DC converter: they demand a large amount of power to be charged to $4V$. As soon as they are charged and the load voltage reaches $4V$, the MPPC pin deactivates and the noise on the VC voltage decreases again.

The load voltage reaching $4V$ marks the end of the start-up process of the circuit. This occurs just before $-30ms$, which means that the start-up process takes approximately $50ms$ in total. This is the duration the circuit needs to adapt from almost zero irradiance to the maximum irradiance it will experience in space and includes the start-up duration of all components in the circuit. The circuit should therefore take even less time for smaller changes in irradiance. Thus, the circuit comfortably meets the response time requirement (REQ-104).

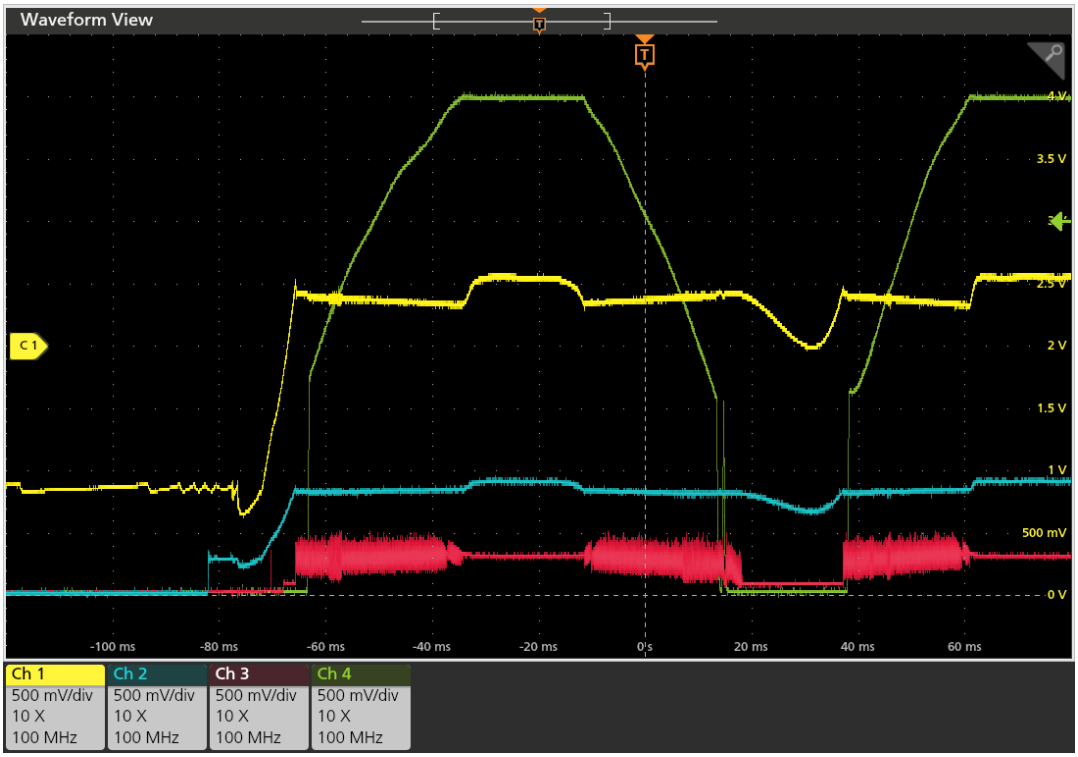


Figure 5.12: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) while an opaque sheet is dropped in front of the lamp to measure start-up and shut-down behaviour.

During shut-down, similar behaviour is seen from the circuit. As soon as the light from the lamp is blocked, the solar cell cannot generate the power required by the load. Therefore, the MPPC pin activates to prevent the solar voltage from decreasing, which is shown by the increase in the noise on the VC voltage. At the same time, the load continues to drain the energy from the system, causing the load voltage to drop, eventually to $0V$. Afterwards, the solar voltage also starts to decrease and would eventually reach the same level as on the left side of the graph. This is not the case here because the opaque sheet fell further down and no longer blocks the lamp. As can be observed in the graph, the circuit has no problem dealing with these quick changes in irradiance and further acts as expected.

Response to a Dynamic Load

The circuit can adapt quickly to changes in irradiance, but how fast does it respond to changes in the power demand from the load? To test this, the load was set at $11Ohm$, which means that it requires a large amount of power. Then, while the lamp was illuminating the solar cell, the load was unplugged and plugged back in. This means that the circuit went from a high power demand to almost zero power demand almost instantaneously, and vice versa. Again, similar oscilloscope measurements were taken to observe the behaviour of the circuit during this change in power demand.

Summary of the Test

- **Test Type:** Oscilloscope measuring while a high power demand load is suddenly connected
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat is unplugged and plugged back in
- **Configuration:** Left cell, thermistor fixed at $10kOhm$, DC-DC converter in fixed frequency mode, Rheostat at $\sim 11Ohm$, $60kOhm$ resistor in series in front of the MPPC pin
- **Measured:** Voltage at solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green)

Explanation of the Results

Before the load is connected at $0ms$, the output is an open circuit and is stable at $4V$, as shown in Figure 5.13. The VC voltage is not noisy and the solar cell voltage is steady. After the load is connected, the solar voltage drops rapidly as a result of the increased power demand. However, after approximately $1ms$, the VC voltage becomes more noisy, indicating that the MPPC pin is activated. After this, the solar voltage quickly returns to its minimum allowed voltage, as dictated by the MPPC pin, after which it remains stable again. Because the load requires more power than the solar cell can provide, the load voltage also decreases. However, this occurs slower than the decrease in the solar cell voltage, due to the larger capacitance at the output of the circuit.

The circuit does not appear to become unstable at any point, and the output voltage remains below $4V$ at all times. This means that REQ-204 is satisfied and, therefore, the battery will not be at any risk during sudden load changes. When the load was unplugged, the resulting graph is essentially a mirrored version of Figure 5.13. Here, the circuit remains stable as well and all voltages remain within their limits. Thus, the circuit can handle large and sudden changes in the power demand of the load and adapts well within $2ms$.

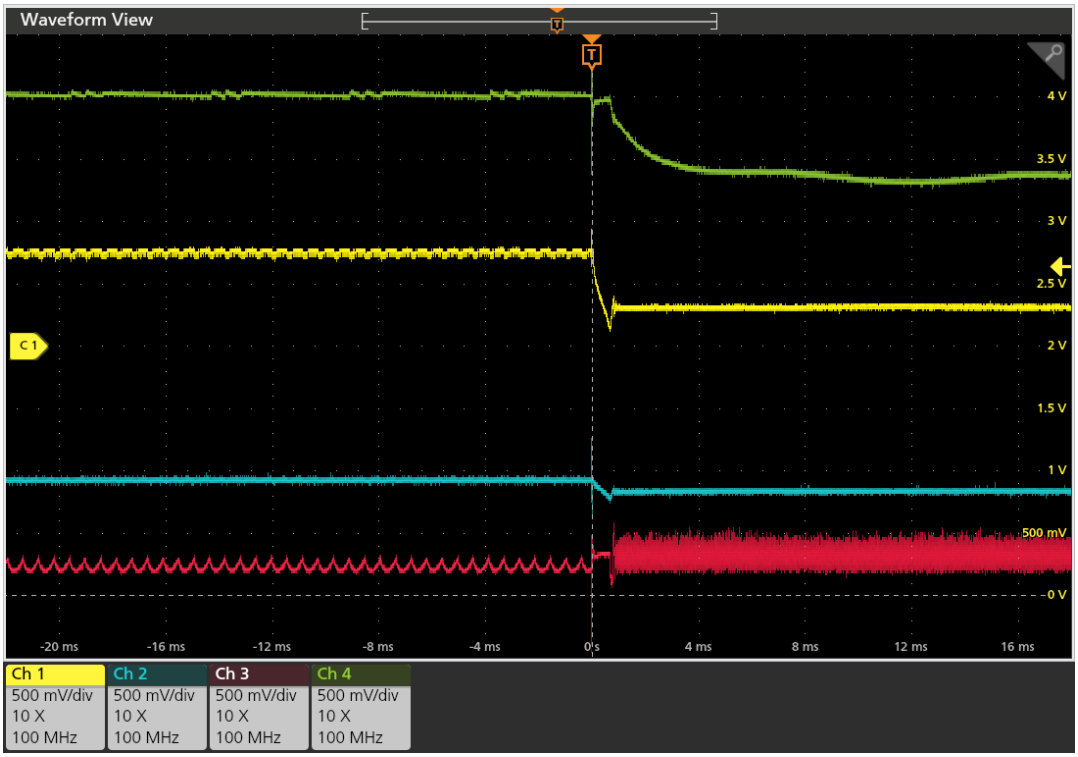


Figure 5.13: Voltage at the solar cell (yellow), MPPC pin (blue), VC pin (red), and load (green) while a high power demand load is suddenly connected.

Remaining Noise in the Circuit

Some noise still remains in the system, besides the noise on the VC pin when the MPPC pin is active. This noise can be observed when looking closely at Figure 5.8. Here, spikes can be observed approximately every $15\mu s$, especially in the voltage of the solar cell. Zooming in even further, smaller spikes are observed that occur about 15 times every $20\mu s$. Therefore, these smaller spikes have a frequency of approximately $750kHz$, which is exactly the operating frequency of the DC-DC converter. The larger spikes, on the other hand, can be linked to the boost converter which boosts the supply voltage for the control circuit of the configuration with one solar cell.

Thus, the DC-DC converter and the boost converter produce the largest amount of noise in the circuit. To prevent the noise they generate from propagating through the rest of the circuit, feed-through filters could be placed around both components. In this way, the filters can act as ”noise barriers” that contain the noise to only the area in which these two components are located. This can be achieved with only three feed-through filters. The first filter should be placed between the output power of the DC-DC converter and the input of the ideal diode. The second filter should be located between the solar cell (after the shunt resistor that is used to measure the current) and the input of the DC-DC converter (before where the power path splits to the boost converter). The final filter should be placed after the output of the boost converter (or after the VCC pin of the DC-DC converter in the case of two cells) and before the supply pins of the components in the control circuit.

With these three feed-through filters, one connection to the DC-DC converter actually remains unshielded: between the output of the INA and the MPPC pin. However, placing a filter here will make the MPPC control loop unstable again. Therefore, only three filters were added to the MPPT Control PCB.

The feed-through filter chosen here is the YFF21PC1A475MT000N [98]. This component was selected because it can filter noise at frequencies as low as $300kHz$ while still being rated for $10V$ and $4A$.

After the three filters were installed, an almost indistinguishable improvement could be seen in the noise. However, the MPPT Control PCB was not designed with the intention of adding these filters. Therefore, their connections were suboptimal. In particular, their ground was connected through relatively long wires instead of being soldered directly to a ground plane as is recommended. Therefore, the filters were likely not as effective as nominally. Thus, it is recommended that additional tests are performed to assess these filters in the next iteration of the circuit.

Burst Mode versus Fixed Frequency Mode

The final characterisation test was to investigate the difference between the burst mode and the fixed frequency mode of the DC-DC converter. Start-up tests and efficiency tests were performed while operating in both modes. No observable differences were found between the two modes. Therefore, it was decided to keep the DC-DC converter in burst mode from now on because it can achieve higher efficiencies when operating at low currents. This may occur when there is a high angle of incidence between the sun and the solar cells, causing a decrease in generated current.

5.1.6. Thermistor Tests

After characterising the circuit and gaining confidence in its operation, the actual temperature sensors can finally be tested. Therefore, the $10kOhm$ resistors that were soldered on the Solar Cell PCB are removed and replaced with the TMP61 thermistors. For these tests, the data of the configuration with two solar cells is shown.

The goal of the thermistors is to adapt the lower limit set by the MPPC pin based on the temperature of the solar cell. To investigate this function, the voltage of the solar cell should be measured over a wide range of temperatures. This temperature range can be achieved by first cooling the Solar Cell PCB using the Peltier modules of the test set-up. Then, the lamp can simply heat the Solar Cell PCB until an adequate temperature range is achieved. Meanwhile, the solar voltage can be measured using the digital multimeters of the MPPT Control PCB. In addition, the current from the solar cells can be measured and used to calculate the power generated by the cells. The output voltage of the voltage divider with the thermistor (PTC Voltage) can also be measured to ensure that the PTC itself behaves as expected.

Summary of the Test

- **Test Type:** Thermistor test over a wide temperature range
- **Connections:** MPPT Control PCB connected to Solar Cell PCB, DC-DC converter, Rheostat
- **Configuration:** Both cells, thermistor soldered, DC-DC converter in burst mode, Rheostat at $\sim 4Ohm$, $60kOhm$ resistor in series in front of the MPPC pin
- **Measured:** Voltage, current, and power at solar cells, voltage at thermistor voltage divider

Explanation of the Results

Firstly, all measurements in Figure 5.14 appear to be linear. In particular, the voltages of the solar cells and the thermistor voltage divider are highly linear. For both voltages, the R^2 of their linear fit

is higher than 0.999 over a temperature range of almost $50°C$. This justifies the choice for the TMP61 thermistor that was made based on its linearity. Next, the absolute value of the power generated by two cells should be around $2.4W$ at room temperature, which is also the case here. It slightly decreases with increasing temperature, which is expected due to the decreasing V_{MPP}. Thus, at first glance, the circuit behaves as expected.

However, on closer inspection, the slopes of the linear fits of the thermistor and solar voltage are incorrect. As explained in subsection 4.4.3, the slope of the thermistor voltage should be $1.909mV/°C$, while here it is $2.155mV/°C$. In addition, the slope of the solar voltage should be $-13.40mV/°C$ for two cells, while here it is only $-10.29mV/°C$.

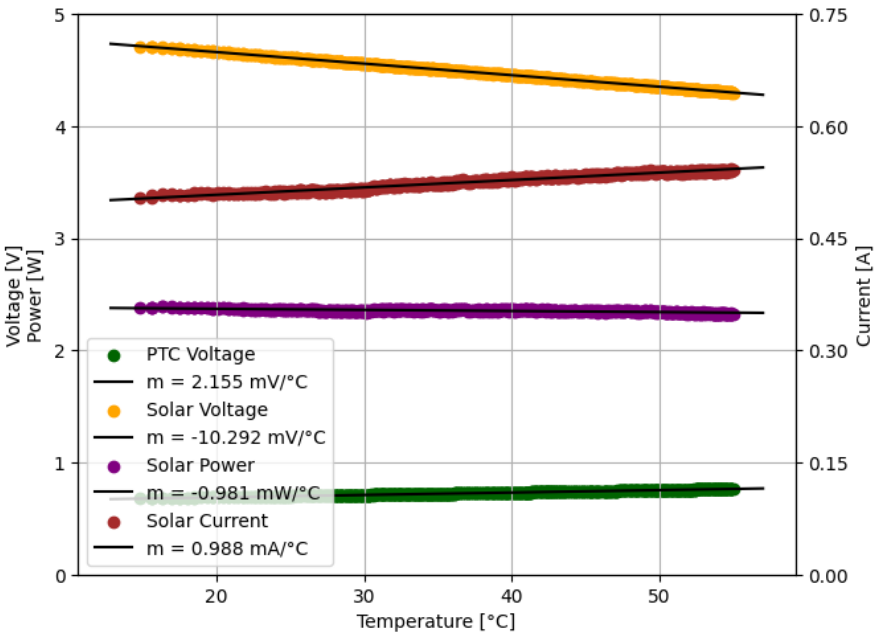


Figure 5.14: Measurements of the voltage, current and power of the solar cells and the voltage of the thermistor voltage divider over a wide temperature range after soldering the thermistor to the Solar Cell PCB.

Correcting the Slope of the PTC Voltage

For the thermistor voltage, this discrepancy can be explained by the difference in ground between the Solar Cell PCB and the MPPT Control PCB. This difference was measured using a multimeter while varying the load resistance, which varies the current flowing through the wires between the two PCBs. The difference in ground was found to be very linear with the current, which means that it was caused by the resistance of the wires between the two PCBs, which was found to be $0.2364Ohm$.

On the MPPT Control PCB, the digital and analogue grounds are separated. They are both connected through two separate wires to the Solar Cell PCB, which is where the grounds are connected to each other. Through the wire that connects the analogue ground, a current of around $500mA$ can flow, resulting in a non-negligible voltage drop of up to $\sim 120mV$ due to the resistance of the wire. However, through the digital ground, only a small amount of current flows, resulting in a negligible voltage drop. This causes the difference between the grounds, with the digital ground being lower than the analogue ground on the MPPT Control PCB.

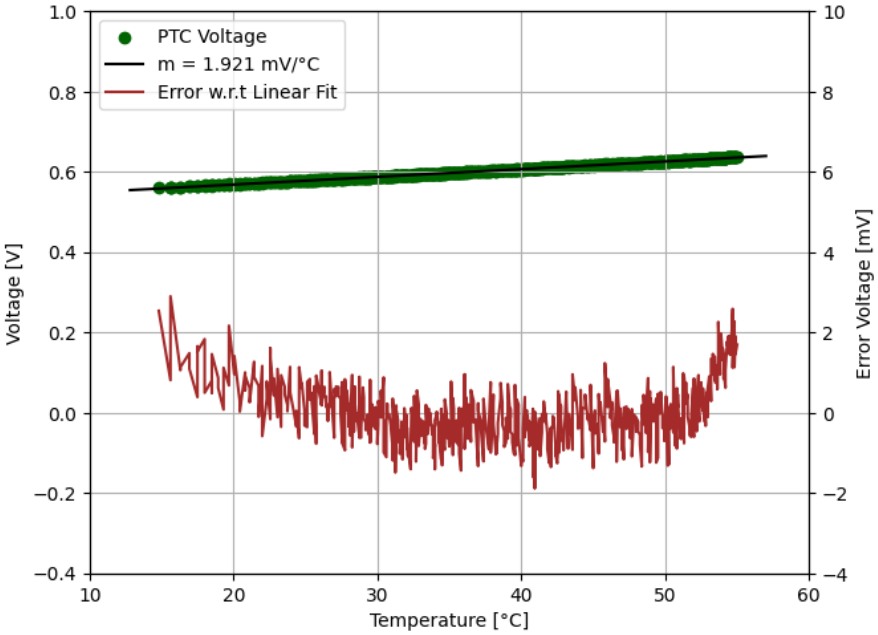


Figure 5.15: The corrected voltage measurement of the output of the thermistor voltage divider and its error with respect to its linear fit over a wide temperature range after soldering the thermistor to the Solar Cell PCB.

It is important to take this difference between the grounds into account because the thermistor voltage divider connects to the analogue ground, while the digital multimeter measuring this voltage connects to the digital ground. Therefore, the thermistor voltage measures higher than it is in reality. To correct for this discrepancy, the voltage drop over the analogue ground can be calculated for each measurement. This is simply the resistance of the wire ($0.2364Ohm$) multiplied with the current through this wire, which is also measured by the digital multimeter. This voltage drop is then subtracted from the measured thermistor voltage to obtain the corrected thermistor voltage.

This corrected thermistor voltage is shown over the entire temperature range in Figure 5.15. It is still highly linear, with an R^2 of its linear fit of more than 0.998. The error with respect to this linear fit is also shown: it remains within approximately $\pm 2mV$, with $13.4mV$ corresponding to an error of $1°C$ in the case of two cells. In addition, the slope of the linear fit is now $1.921mV/°C$, which is only $0.012mV/°C$ or 0.63% away from the desired slope. Therefore, it can be concluded that the TMP61 thermistor behaves as designed.

Analysing the Solar Cell Voltage

Unfortunately, it is not possible to correct the solar voltage in the same manner. The DC-DC converter is connected through another set of wires from the MPPT Control PCB, and its ground behaves in unpredictable ways, making it difficult to correct it. Therefore, it is again recommended to place the DC-DC converter on the same PCB as the control circuit in the next version. In this way, the uncertainty caused by the discrepancies in the ground can be completely eliminated. This might completely solve the problem of the incorrect slope of the solar voltage. However, if the incorrect slope is still present in the next version, the debugging process will still be easier as all ground potentials will be equal.

For now, the solar voltage will be analysed assuming that the measurements shown in Figure 5.14 are correct. Based on this data, it can be evaluated whether the efficiency requirement (REQ-102) is met.

As mentioned above, the slope of the solar voltage is observed to be $-10.29mV/°C$, while it should be $-13.40mV/°C$ instead, resulting in an error of $3.11mV/°C$. Assuming the solar voltage is at the V_{MPP} at $10°C$, which is the middle of the temperature range and thus the best-case scenario, the difference between the solar voltage and the V_{MPP} will be $155.5mV$ at the edges of the temperature range.

To translate this error in the solar voltage to a power loss, the same assumption is made as in subsection 4.4.6: the current produced by the solar cells remains constant close to the MPP. Therefore, the power loss is simply the error in the solar voltage multiplied by the current produced at the MPP, which is $0.5A$. This results in a power loss of $77.75mW$, which is ~ 3.2% of the power produced by the solar cells ($\sim 2.4W$). Revisiting Figure 5.10, a reduction in efficiency of 3.2% would mean that the circuit would operate with an efficiency of ~ 78%, resulting in REQ-102 not being met.

5.2. Validation of Requirements

After extensively testing the MPPT circuit, the original requirements presented in Table 4.2 should be revisited. It should be investigated which requirements are met and which ones are not, so that it is clear what improvements should be made for the next design iteration. It should be noted that the prototype prioritised the investigation of the performance of the temperature-based MPPT method, as well as the testability of this prototype. Therefore, it is possible that some requirements have not been met, as explained in subsection 4.1.2. Table 5.1 shows a list of all requirements and whether or not they are met, including a rationale.

Table 5.1: Checklist of the requirements for the temperature-based MPPT circuit with rationale for why they are (not) met.

Identifier	Requirement	Met?	Rationale for (not) meeting requirement
REQ-000	The TwinSat PocketQubes shall have MPPT circuits for their solar cells.	No	Child requirements REQ-100 and REQ-200 are not fully met.
REQ-100	The MPPT circuit shall optimize the efficiency of the power generation of the solar cells on the PocketQube.	No	Child requirement REQ-102 (efficiency) is not met.
REQ-101	The MPPT circuit shall operate based on real-time voltage and temperature measurements of the solar cells.	Yes	The circuit is fully analogue and operates based on the thermistor voltage and solar cell voltage, as shown in subsection 4.4.3.
REQ-102	For any combination of temperature and irradiance, the output power of the MPPT circuit shall be at least 80% of the theoretical maximum power produced by the solar cell(s) at that temperature and irradiance, when more power is demanded than the cell(s) can produce.	No	The efficiency of the circuit (output power divided by input power) was proven to be above 80% in subsection 5.1.4. However, after analysing the slope of the solar cell voltage with respect to temperature in subsection 5.1.6, the V_{MPP} is not tracked accurately enough, resulting in an overall efficiency as low as $\sim 78\%$.
REQ-103	The MPPT circuit shall be able to operate within a temperature range of $-40°C$ to $60°C$.	Yes	All components can operate at these temperatures, as mentioned in subsection 4.4.4.
REQ-104	The MPPT circuit shall respond in less than $900ms$ between 10% power and 90% power produced.	Yes	The circuit adjusted from almost no irradiance to maximum irradiance in approximately $50ms$, as shown in subsection 5.1.5.
REQ-200	The MPPT circuit shall be integrated in the TwinSat PocketQube.	No	Child requirements REQ-202 (housekeeping data) and REQ-203 (volume) are not met.
REQ-201	The MPPT circuit shall have two versions: one compatible with one 3G30A solar cell and one compatible with two 3G30A solar cells in series.	Yes	The circuit works with the configuration for one cell and two cells, since all tests have been performed in both versions, as explained in subsection 5.1.1.
REQ-202	The MPPT circuit shall send housekeeping data to the on-board computer of the PocketQube.	No	Housekeeping data is currently being sent to a laptop, as explained in section 4.5, but has not yet been tested with the on-board computer.
REQ-203	The MPPT circuit shall have dimensions (LxWxH) of $TBD \times 20 \times 3.4mm$.	No	The prototype was optimised for testability, so the volume was intentionally increased as discussed in subsection 4.1.2. The next version can be made smaller.
REQ-204	The MPPT circuit shall limit its output voltage to a maximum of $4.0V$.	Yes	The DC-DC converter limits the output voltage to $4.0V$, as discussed in subsection 5.1.1.
REQ-205	The MPPT circuit shall limit its output current to a maximum of $1.2A$.	Yes	The ideal diode limits the output current to less than $1.05A$, as discussed in subsection 4.4.7.

Identifier	Requirement	Met?	Rationale for (not) meeting requirement
REQ-206	The MPPT circuit shall have reverse current protection at its output.	Yes	When the battery was connected to the output of the circuit, the ideal diode prevented reverse current, as explained in subsection 5.1.1.
REQ-300	The MPPT circuit shall be tested on the ground using flight solar cells.	Yes	The Solar Cell PCB is equipped with flight solar cells, as explained in subsection 4.2.2. All tests presented in section 5.1 were performed using these cells.
REQ-400	The MPPT circuit shall be able to be indefinitely stored without power while integrated in the flight-ready PocketQube.	Yes	All child requirements are met, and the circuit was at times unpowered for weeks in between tests but remained fully functional when testing resumed.
REQ-401	The MPPT circuit shall autonomously start up after the deployment of the PocketQube.	Yes	The circuit starts up as soon as the solar cells receive enough irradiance to power the circuit, as shown in subsection 5.1.5.
REQ-402	The MPPT circuit shall operate using only the power provided by the solar cells.	Yes	During each test performed in section 5.1, the complete analogue MPPT circuit was powered solely by the solar cells. In the test set-up, external power supplies are only needed for the sensors measuring housekeeping data and for cooling, as shown in section 4.5.

As can be observed in Table 5.1, six out of seventeen requirements are not met. However, REQ-000, REQ-100 and REQ-200 are not met only because not all of their child requirements are met. Therefore, only three requirements remain: REQ-102 (efficiency), REQ-202 (housekeeping data), and REQ-203 (volume). These will be discussed in more detail below.

Efficiency of the Circuit

Considering REQ-102, it was shown in subsection 5.1.4 that the efficiency of the circuit was always higher than 80%. However, this efficiency is simply the output power of the circuit divided by the power generated by the solar cells. Therefore, it does not take into account whether the cells actually operate close to their MPP. In subsection 5.1.6, it was observed that the solar voltage did not have the correct slope with respect to temperature. This means that the MPP is not well tracked, at least not over the entire temperature range, resulting in an overall efficiency as low as $\sim 78\%$. This was deemed too difficult to solve with the prototype because the grounds of the different PCBs did not match.

In addition, the difference in the ground potentials means it is also hard to determine whether the solar voltage has the correct offset. If the slope were correct, the offset should be such that the solar voltage always follows the V_{MPP}. In particular, according to the datasheet of the solar cells [46], their voltage should be $2.409V$ at $28°C$. But, with the slope already being incorrect for the prototype, and the measurements from the digital multimeters not being accurate, the offset can also not be found. Therefore, for the prototype, it is hard to accurately determine how far away from the MPP the solar cells actually operate and what the corresponding effect on the efficiency is. For now, the analysis performed in subsection 5.1.6 assumed that the measurements of the digital multimeters are correct, which resulted in the efficiency requirement not being met.

To verify the efficiency requirement, all circuitry should first be placed on the same PCB so that all grounds are equal. Then, the slope and offset of the solar voltage can be evaluated again. If they closely

match the designed values, the circuit works as intended and is verified. Using the difference between the designed values and the measured ones, it can be calculated again how far away from the MPP the solar cells operate and what the effect is on the efficiency, similarly to the analysis in subsection 5.1.6. If the slope and offset do not closely match the expected values, it should be investigated why and a solution should be found.

Afterwards, the efficiency requirement can be validated using experimental data from the solar cells. For this, numerous solar cell characterisation tests should be performed so that the MPP is found at different temperatures and irradiances. Based on this data, the slope and offset of the solar voltage can be experimentally validated. This also allows for calculating how close to their MPP the solar cells operate in practice. Following from this, the efficiency requirement can finally be experimentally validated. This is the most important fix for the next version of the circuit. Again, it is not possible to test this with the prototype because the difference in ground potentials will result in inaccurate measurements.

Another benefit of placing all circuitry on one PCB is that the wires between the PCBs and their resistance will be removed. For example, the wire between the Solar Cell PCB and MPPT Control PCB has a resistance of $0.2364Ohm$. A current of $0.5A$ flows through it, resulting in a power loss of $\sim 60mW$, which is almost 5% of the power produced by one cell. This loss is currently not being measured, since the solar power is measured on the MPPT Control PCB. However, the wires to the DC-DC converter have similar resistances, so the overall efficiency will likely increase when combining the PCBs.

Required Modifications for the Next Version

REQ-202 is already close to being met: housekeeping data has been collected and sent to a laptop using the I2C protocol. The remaining problem is that integration with the on-board computer of the satellite has not been considered yet. However, this integration should not pose major issues: the on-board computer will likely have an I2C connection to which the housekeeping data can be sent. This connection can then be made possible by adjusting the current I2C connector of the MPPT Control PCB. Afterwards, it should be tested whether the on-board computer can read out all housekeeping data to validate this requirement.

As explained in subsection 4.1.2, the focus of the prototype MPPT circuit was to easily perform tests and debug the circuit. Therefore, the volume requirement (REQ-203) was not a priority for the prototype and was therefore not yet met. Thus, for the next version, the overall volume of the circuit should be reduced so that this requirement will be met. Then, if the efficiency and housekeeping data requirements are also satisfied as explained above, all requirements will be met.

Sending housekeeping data to the on-board computer is a feature that does not interfere with the other functions of the circuit and should therefore not be difficult to implement. Thus, only two requirements could pose some problems: the efficiency requirement (REQ-102) and the volume requirement (REQ-203). It is already discussed above how to meet the efficiency requirement. To meet the volume requirement, 0402 components could be used instead of 0603, and all components can be placed closer together. In addition, the test points will not be necessary in the flight version. The $0Ohm$ resistors in the voltage dividers around the INA can also be removed, unless they need to be replaced with resistors that have a specific value necessary to follow the MPP more closely. Removing other components is likely not possible, so if the volume requirement is still not met, it could be possible to move some components to other PCBs in the PocketQube.

6 Conclusion

As discussed in chapter 3, the MPPT algorithm used on Delfi-PQ, P&O, was deemed to be sub-optimal for a tumbling PocketQube. Therefore, a new algorithm is proposed: temperature-based MPPT. The objective of this research was then to investigate the performance of a temperature-based MPPT circuit that is intended to be used on the next PocketQube. To achieve this, a prototype version of this circuit was designed and manufactured. Then, this prototype was tested with flight solar cells in different temperature and irradiance environments to evaluate whether it would be a viable replacement for the P&O technique used on the previous PocketQube.

At the start of the design process, requirements were formulated for the eventual flight version of the circuit. However, the prototype version prioritised testability and performance of the core functionalities. These core functionalities correspond more to the research questions posed in chapter 3, while the remaining requirements are more related to the integration of the circuit into the satellite. This eventually resulted in the prototype version not meeting the housekeeping data and volume requirements.

Considering the performance of the circuit, it can be concluded that the temperature-based MPPT circuit looks promising, but further development is necessary. Firstly, the circuit is compatible with both one solar cell and two cells in series in the desired temperature range of $-40°C$ to $60°C$. The circuit was also tested in rapidly changing environments by quickly varying the irradiance, as well as the load at the circuit output. It showed that it only needs approximately $50ms$ to adapt from zero to maximum irradiance. It can also react to large changes in power demand in under $2ms$. Because the lamp, which simulates the sun in the test set-up, heats the solar cells relatively slowly during tests, the circuit also appeared to adapt instantaneously to changes in temperature. However, it is not yet validated how closely the output of the thermistor matches the actual temperature of the solar cells.

The power efficiency of the circuit is higher than 80% and even reaches 85% in the case of two cells. This is promising but does not take into account how closely the solar cells actually operate to their MPP. When investigating this, it was noticed that the voltage of the solar cells changes highly linearly with temperature, which is desired. This is the result of a highly linear thermistor, proving that this is an adequate way to measure the temperature. However, the slope of this linear function is not equal to the designed value, resulting in overall efficiencies as low as 78%, which does not meet the required 80%. This is an important flaw with the prototype and should be resolved in the next version, as explained in more detail in chapter 7.

The prototype promises efficiencies of over 80%, possibly even over 85%, while being able to quickly react to changing environments and power demands. Therefore, the main performance metrics have been quantified, which means that the research objective has been met and that the research questions have been answered. Only one major flaw remains in the incorrect value for the slope of the solar voltage with respect to temperature. However, after solving this efficiency issue in the next version as explained in section 5.2, the circuit will be able to produce the adequate amount of power in a rapidly changing environment. This means that the hypothesis posed in chapter 3 is proven to be correct and therefore the circuit will be a viable option and should become ready to fly on the next PocketQube mission.

7 Recommendations

As mentioned in chapter 6, the temperature-based MPPT circuit has high potential, but some adaptations are necessary for the next version. Throughout this report, numerous recommendations have been proposed. For clarity, they will all be repeated here.

The two main recommendations go hand in hand. The accuracy of the tracking of the MPP should be further investigated and the DC-DC converter should be placed on the same PCB as the control circuit. Currently, the MPP tracking is not accurate because the slope of the solar voltage with respect to temperature is incorrect. This may be caused by a difference in the ground potential between the DC-DC converter and the control circuit. Therefore, placing these on the same PCB will remove the difference in the ground potential, possibly solving the problem of the incorrect slope. However, if the slope problem still remains, at least the debugging process will be easier in the next version. This is because all measurements will now be made with respect to the same ground potential, making all measurements more accurate.

When the slope of the solar voltage has been fixed, its offset should also be examined. That is, at $28°C$, the solar voltage should be limited to $2.409V$, which is the V_{MPP} mentioned on the datasheet of the solar cells. This measurement will now also be more accurate due to the correct ground potential. If the offset is correct, it can be said that the circuit operates as designed and that the MPP is accurately tracked.

However, the actual flight solar cells have not yet been fully characterised. Therefore, the next recommendation is to experimentally obtain the slope and offset of the V_{MPP} from the solar cells by testing at different temperatures and irradiances. This characterisation should be performed without the DC-DC converter connected, as explained in section 4.5. These tests can then be used to confirm the accuracy of the datasheet and the tolerances of the solar cells. If needed, the slope and offset of the circuit can be adjusted to match the experimental data. Again, this will only be accurate when the control circuit and the DC-DC converter share the same ground plane.

With the slope and offset of the V_{MPP} experimentally obtained, it is also possible to accurately measure how far away the solar cells operate from the MPP. Therefore, the loss in power from not operating exactly at the MPP can be calculated with more accuracy. These measurements are also made possible by the ground potential being uniform. This power loss can then be taken into account when calculating the efficiency of the entire circuit, which allows for the validation of the efficiency requirement.

When placing the control circuit and the DC-DC converter on the same PCB, it is important not to forget to include the resistor in series between the output of the INA and the MPPC pin to restore the low-pass RC filter. The values used now are $60kOhm$ for the one-cell configuration and $120kOhm$ for the two-cell configuration. However, it should be tested again in the next version to confirm whether these values are optimal. In addition, it can be interesting to increase the values of the resistor and capacitor in this RC filter to further slow down the MPPC control loop. This will increase the reaction time of the circuit, but it might further reduce the noise on the VC pin, which could lead to an increase in efficiency. Thus, a trade-off can be made between the reaction time and the efficiency of the circuit.

Another measure to reduce noise are the LC filters. As explained in subsection 5.1.5, these filters were placed around the DC-DC converter and the boost converter to contain the noise that these components produce. However, the prototype PCB was not designed with these filters in mind. Therefore, they were not well grounded, reducing their effectiveness. Thus, in the next version, it is recommended to include these filters in the design and test their effectiveness when grounded as intended. Another recommendation for the PCB layout is to increase the size of the pads of the boost converter so that they stick out from underneath the component. This makes it easier to manually resolder this device. In addition, the ground pads of the solar cells should also be made larger to facilitate soldering.

As explained in more detail in section 5.2, other additional features are also necessary to meet all requirements. Importantly, the volume of the circuit should be reduced. It should also be made possible to send housekeeping data from the MPPT circuit to the on-board computer of the PocketQube. In addition, two features that have not been mentioned before should be added to the circuit to ensure its reliable operation. Firstly, a Remove-Before-Flight switch should be added that disconnects the solar cells before the satellite is inserted into the deployer. Secondly, a kill switch should be included that disconnects the solar cells until the satellite is ejected from the deployer.

Finally, more tests are recommended to fully validate the circuit for use on the PocketQube. Vibration and radiation tests are useful to investigate the reliability of surviving the launch and the harsh space environment, respectively. In addition, the reaction time to changes in temperature should be further tested. This might be achieved by spraying cooling spray on the thermistor (and the solar cells) to quickly drop the temperature, which would also allow for testing at lower temperatures. Next, it should be investigated how closely the temperature of the thermistor matches the solar cell temperature. This might be achieved using a thermal camera. If needed, the thermistors could be placed in a different location on the PCB to reduce measurement errors. To more realistically test the reaction of the circuit to changes in irradiance, a rotating test set-up for the solar cells could also be made. This would more accurately simulate the tumbling of the PocketQube in the lab.

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A Initial Planning of the Thesis

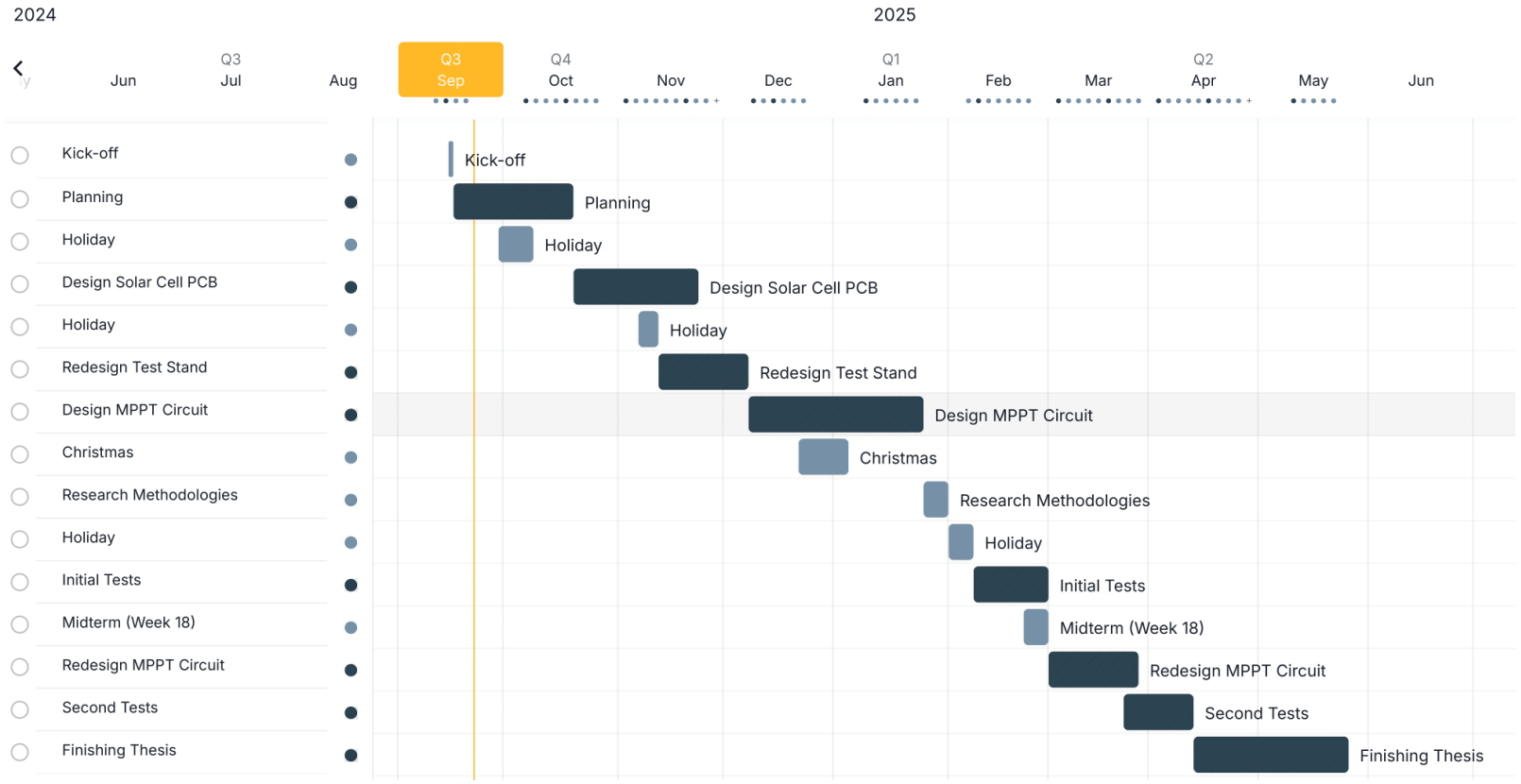

Figure A.1: Gantt chart with the main work packages of the thesis.

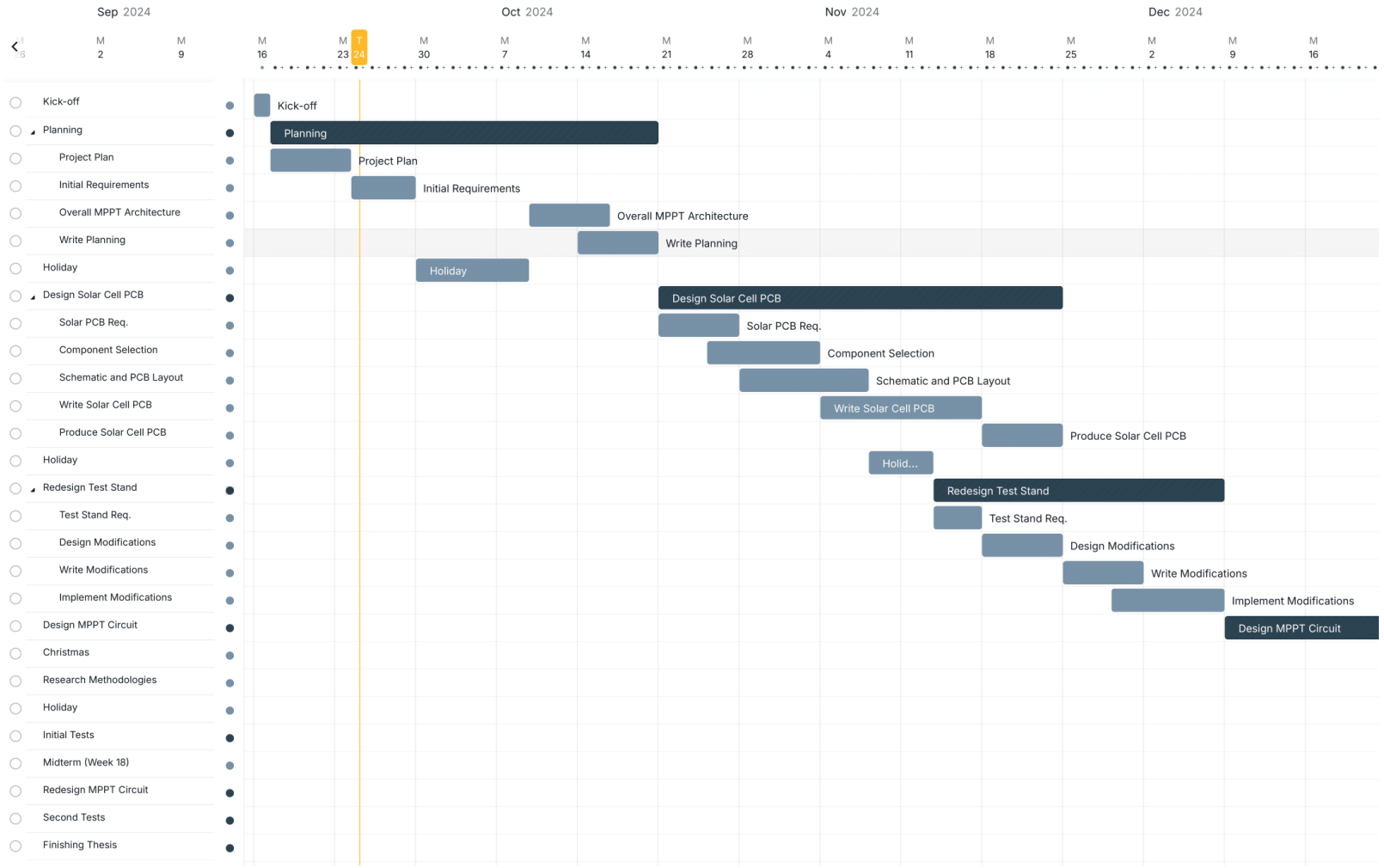

Figure A.2: Gantt chart with all the work packages of the thesis (part 1).

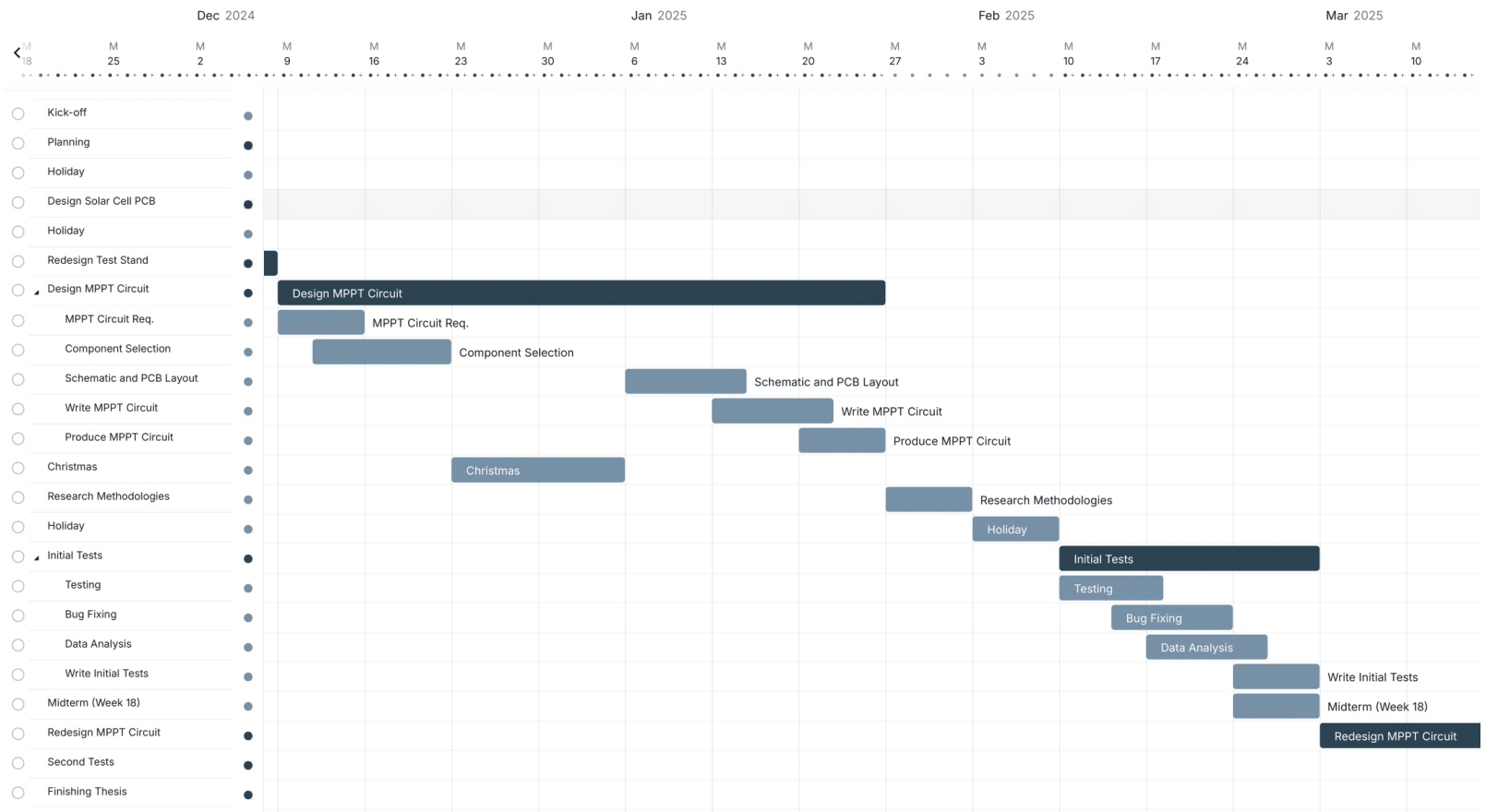

Figure A.3: Gantt chart with all the work packages of the thesis (part 2).

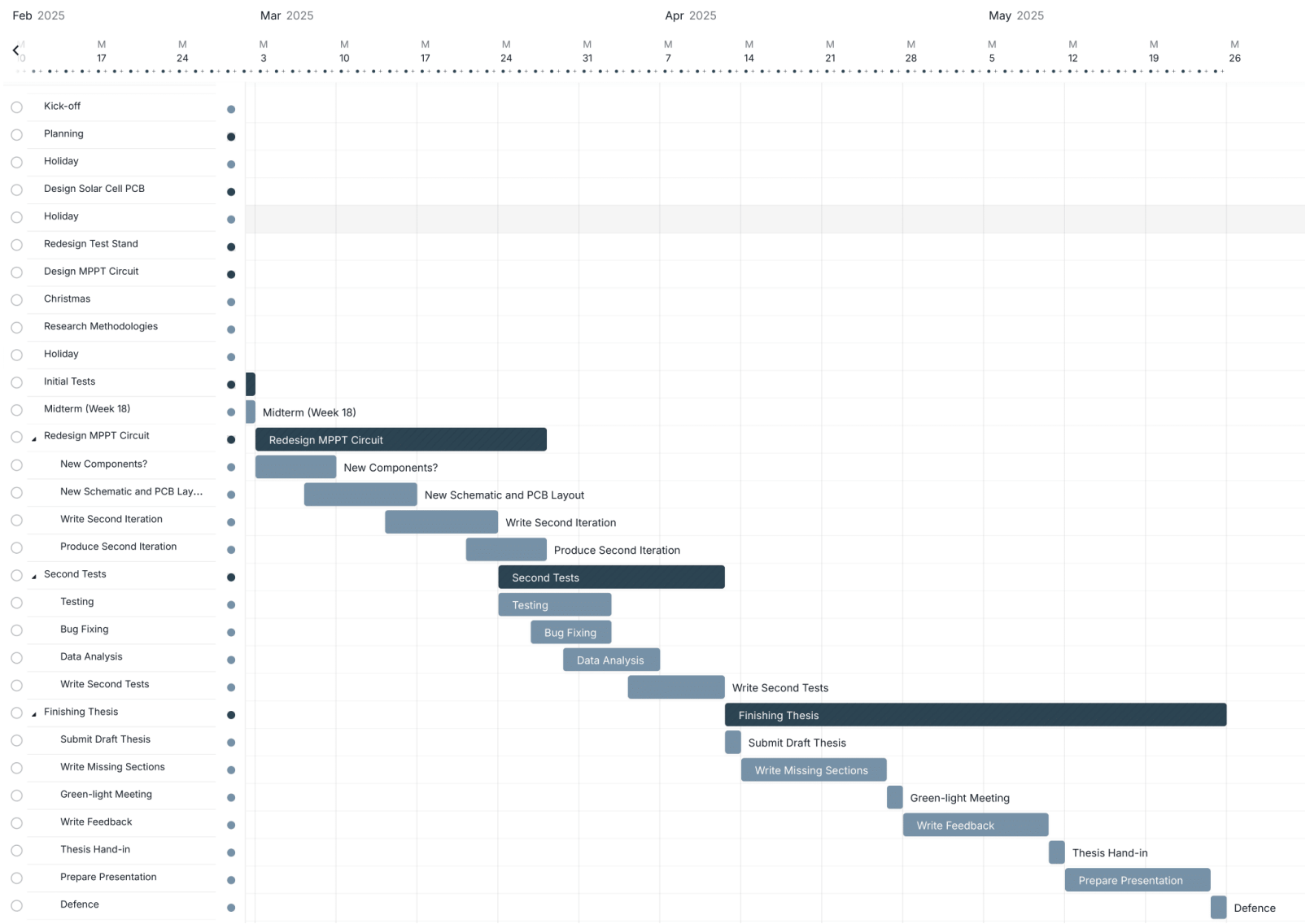

Figure A.4: Gantt chart with all the work packages of the thesis (part 3).