Surface-Passivated High-Resistivity Silicon as a True Microwave Substrate

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***Abstract*—This paper addresses the properties of a surface-passivated (enhanced) high-resistivity silicon (HRS) substrate for use in monolithic microwave technology. The detrimental effects of conductive surface channels and their variations across the wafer related to the local oxide and silicon/silicon–dioxide interface quality are eliminated through the formation of a thin amorphous layer at the wafer surface. Without passivation, it is found that the surface channels greatly degrade the quality of passive components in HRS by masking the excellent properties of the bulk HRS substrate and by causing a spread in parameters and peak values across the wafer. Moreover, it is seen that the surface passivation leads to excellent agreement of the characteristics of fabricated components and circuits with those predicted by electromagnetic (EM) simulation based on the bulk HRS properties. This is experimentally verified for lumped (inductors and transformers) and distributed (coplanar waveguide, Marchand balun) passive microwave components, as well as for a traveling-wave amplifier, through which also the integration of transistors on HRS and the overall parameter control at circuit level are demonstrated. The results in this paper indicate the economically important possibility to transfer microwave circuit designs based on EM simulations directly to the HRS fabrication process, thus avoiding costly redesigns.**

***Index Terms*—High-resistivity silicon (HRS), inductors, Marchand balun, substrate passivation, transformers, traveling-wave amplifier (TWA).**

I. Introduction

THE RECENTLY demonstrated performance levels of SiGe HBTs [1] and RF/CMOS [2] have manifested the potentials of silicon technology in communications [3], automotive [4], and broad-band [5] applications. This, however, brings several technological issues in focus that may form bottlenecks, in particular the considerable losses in the conventional silicon substrates [6]. Currently, resistivities of at most 10–20 $\Omega\cdot$ cm [low-resistivity silicon (LRS)] are being used. This corresponds to conductivities that lead to considerable substrate losses and, thus, to excessive attenuation of integrated transmission lines [7] and reduced quality (Q) factors of on-chip inductors [8]. III–V-based processes have ideal substrates in that respect, but these lack other important properties such as high thermal conductivity and high and frequency-independent permittivity that qualify silicon as a true microwave substrate [7]. High-resistivity silicon (HRS) has, therefore, been investigated for use in integrated circuit fabrication processes. Two major obstacles have, however, been identified, which are: 1) since bulk losses are nearly eliminated, losses associated with parasitic surface channel formation become noticeable [9], [10] and 2) the electrical isolation of integrated devices becomes difficult due to the wide space–charge regions associated with the very light doping level of the HRS. A solution for the latter issue has been reported for CMOS device integration [12], but was not yet demonstrated for the integration of bipolar transistors. The first issue is new in silicon technology, as far as high-frequency (HF) applications go. Note though that so-called surface channel stoppers have been used in silicon integration processes for a long time to improve the electrical isolation of integrated devices through additional doping at the wafer surface in between devices. That concept, however, is not applicable for the integration of HF passive components since additional doping would give an even stronger contribution to the substrate losses. One, therefore, has to explore other ways to suppress surface-channel formation in HRS because they can considerably add to the losses of integrated passive components. Those surface channels build up at the silicon/silicon–dioxide interface as a result of either oxide contamination, interface states, or electrical biasing between a metal structure above the field oxide and the silicon [10]. These are all fairly local effects that are not entirely predictable and the associated variations in the electrical characteristics of the passive components makes the effect of such surface channels an even more serious issue. Under such circumstances, the circuit design may become a very difficult task, requiring several costly redesign cycles. In this paper, we show that application of a recently introduced surface passivation technique [13], [14] will not only lead to a higher quality of the passive components, but also to an improvement of the parameter control to such a degree that design transfer from simulation to hardware

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TABLE I
DIMES-04 TRANSISTOR PARAMETERS

	HV BJT	HF BJT
A_E (μm^2)	20x1	20x1
Beta	100	100
BV_{CEO} (V)	8.0.	4.0
V_A (V)	38	12
C_{EB} (fF)	85	88
C_{BC} (fF)	60	90
C_{Sub} (fF)	200	120
f_T @3V(GHz)	13	25

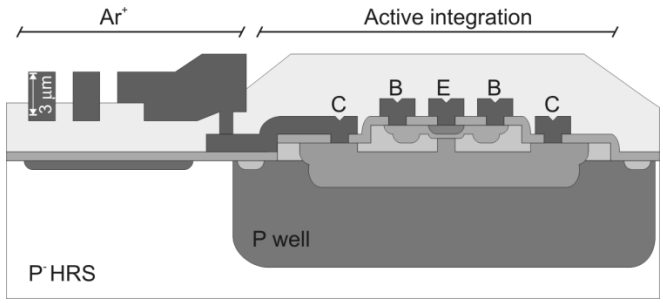

Fig. 1. Schematic cross section of the passive and active device structures in DIMES-04 [15] on SP HRS.

implementation in a single cycle becomes feasible. Besides giving a description of the surface passivation technique for HRS, in Section II, we will also introduce a fabrication process for dense integration of advanced bipolar transistors on HRS substrates. In Section III, we discuss the impact of surface effects, as well as of surface passivation, on the characteristics of lumped (inductor, transformer) and distributed (transmission line, Marchand balun) passive components, while particularly addressing parameter variations across the wafer. Lastly, the results for a 7.5-GHz traveling-wave amplifier (TWA) are described in Section IV with focus on the efficiency of design implementations.

II. DEVICE AND COMPONENT INTEGRATION

The in-house university bipolar process DIMES-04 ($f_T \sim 25/13$ GHz) was derived from the former DIMES-03 process ($f_T \sim 15$ GHz) [15] and has been used here for the fabrication of the microwave passive components and the TWA. HF and high-voltage (HV) transistors are available (Table I).

The bipolar active npn device in DIMES-04 is fully implanted with less than 10% spread in the main device parameters over the wafer. The often observed higher spread in current gain associated with polysilicon emitter processes is thus avoided. The active circuits presented in this paper are, therefore, fabricated in a technology that exhibits excellent parameter control. The fabrication process, which was designed for low-resistivity p-type LRS (2–5 $\Omega\cdot$ cm) substrates, has been transferred to p-type HRS substrates having a resistivity of 2000–4000 $\Omega\cdot$ cm. Since the very high silicon resistivity results in excessively wide space–charge regions (in the 20-μm range) of the collector–substrate junctions and low integral p-type doping between neighboring n-type regions placed in the substrate, a special p-well isolation structure has been developed for dense integration of the transistors. A 3-μm-deep boron-doped p-well with a peak doping concentration of 2×10^{15} cm^{-3} is created by implantation and thermal annealing prior to the implantation of the n^+ sub-collector regions and blanket deposition of the n-type layer, in which the active devices are built [15]. Outside the silicon device regions, this n^- silicon layer is removed by trench etching so that the passive components can be placed directly on the HRS substrate where substrate losses are the lowest. The p-well provides a vertically increased p-type doping level under each transistor and narrow collector–substrate space–charge regions, while laterally a p^+ channel stopper is implanted after removal of the lightly doped n-type layer. A schematic of the active and passive integration structure is shown in Fig. 1. Since the well doping is comparable to that of the LRS substrate for which the DIMES-04 process was originally designed, all transistor characteristics including the collector–substrate capacitance remained virtually unchanged (Table I). For the integration of passive components a two-level aluminum (Al) interconnect process with a 3-μm-thick top Al layer is used, as also shown in Fig. 1.

Without special surface passivation, the substrate losses were still considerably above the theoretical minimum values due to the presence of conductive channels that build up at the wafer surface right beneath the silicon/silicon–dioxide interface. These channels result from positive (ion) charges in the isolating oxide, from (positive) states at the silicon/silicon–dioxide interface, or from a bias between a metal layer and the substrate [10]. According to the metal–oxide–semiconductor (MOS) theory, either a majority carrier accumulation layer or an inversion layer in combination with a depletion region can be formed, depending on the specific conditions. With the low silicon-doping level, the flat-band voltage is very low so that the bias difference between the cases of accumulation and inversion/depletion is very small [11]. That means that the chances for the presence of an accumulation or inversion surface channel and more losses than those associated with the bulk silicon are high. Given the local variations of both the oxide contamination level and the distribution of interface states, such additional losses also vary considerably across the wafer. It was, therefore, essential to apply a surface passivation technique in order to suppress these effects for minimum loss and best possible parameter control. Surface-passivated high-resistivity silicon (SP HRS) can be achieved by forming a thin silicon layer having a very high density of traps within the bandgap of silicon. This leads to a very high recombination rate and a reduced rate of impurity ionization. Consequently, accumulation, depletion, and inversion layer formation will be prevented and the additional source of loss will be eliminated. Such a high trap density can be achieved through a high-dose implantation of a neutral impurity, such as argon [13], [14] into the silicon surface region or by depositing a thin highly defective silicon layer such as poly-crystalline silicon [9] or amorphous silicon [16] onto the wafer. For the experiments presented in this paper, we used an implantation of argon at a dose of 10^{15} cm^{-2} to form the SP HRS [16].

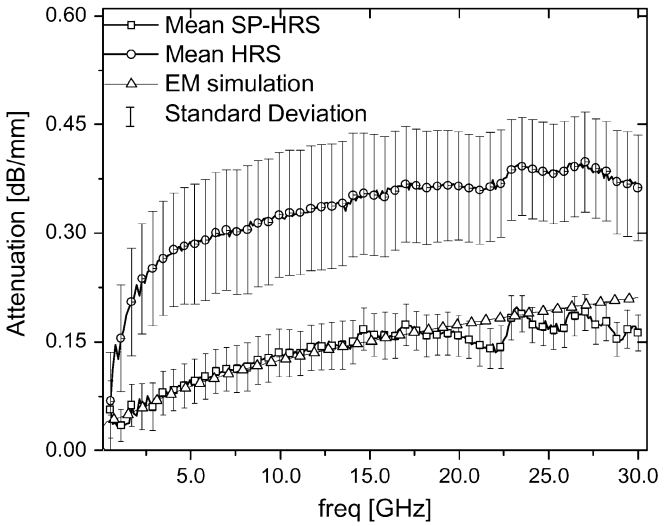

Fig. 2. Comparison of the attenuation constant for CPWs on HRS and SP HRS to an EM simulation based on HRS bulk properties (33 samples considered).

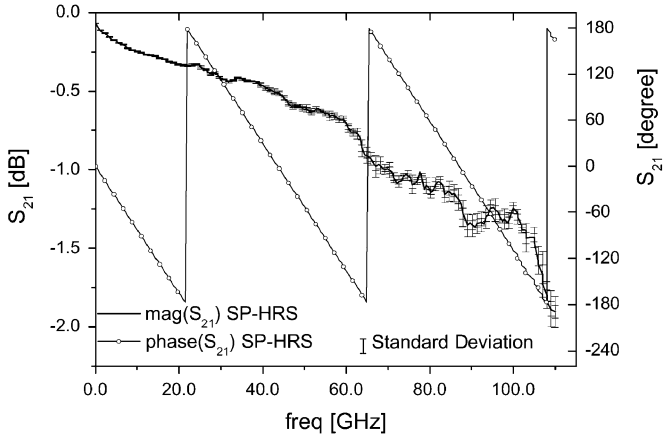

Fig. 3. Measured S_{21} magnitude and phase of a 3-mm CPW on SP HRS up to 110 GHz.

III. Characterization of Passive Components

Here, we discuss the improvements achieved with HRS and SP HRS wafers for four types of RF and microwave passives, i.e., transmission lines, inductors, transformers, and a coupled-line Marchand balun. Almost all comparisons between the two types of substrates are performed on the same wafer having an unpassivated wafer section and a section that was passivated by performing the argon implantation. All structures have been analyzed by using Agilent's electromagnetic (EM)-field simulator Momentum. Measurements were done by using an HP 8510 vector network analyzer (VNA) for the two-port structures, while an HP 8753E VNA in conjunction with an ATN four-port test set was used for testing the three- and four-port structures. The on-wafer measurements were performed with Cascade air coplanar (ACP) probes.

A. Transmission Lines

The impact of surface effects and surface passivation on transmission lines was studied by using coplanar waveguides (CPWs). CPWs are particularly sensitive to the surface properties since the EM field is concentrated at the silicon/silicon–dioxide interface [10]. The measured and simulated attenuation constants for both HRS and SP HRS are compared in Fig. 2, in which the standard deviation from the mean value is plotted for 33 dies measured over the wafer. This has been calculated as

$$SD(f) = \frac{1}{n-1}\sum_{i=1}^{n}\left[X_i(f) - \bar{X}(f)\right]^2 \qquad (1)$$

where $\overline{X}$ is the mean value and n is the number of measured samples.

It is obvious that both the average attenuation and the spread in attenuation over the wafer are greatly improved for SP HRS as compared to HRS. Moreover, there is very good agreement between the EM simulation and the measurements on SP HRS, with a noteworthy reduction from 0.35 to 0.15 dB/mm at 15 GHz for the mean measured attenuation on HRS and SP HRS, respectively. Fig. 3 shows the S_{21} measurement for a 3-mm-long CPW up to 110 GHz. It is obvious that the line length is approximately 5/2 λ at 110 GHz, representing a loss of 1.7 dB. This data leads to a loss in the order of 0.17 dB for a $\lambda/4$ line at 110 GHz (often used in higher harmonic termination). This low value of insertion loss is comparable to those achieved in III–V technologies [17], making the use of low-attenuation CPWs in silicon technology feasible over the full range of microwaves.

B. Inductors

Integrated spiral inductors have become important components for integrated RF circuits, but the Q achievable in standard silicon technology is still lagging behind the values achieved on GaAs substrates or on printed circuit boards (PCBs). Multimetal-layer structures and thick metallization schemes can effectively be used to reduce the ohmic losses of the metal spiral coil structure [8]. Substrate losses in the commonly used LRS are still the main reason that adequately high-Q values at sufficiently high frequencies cannot easily be reached in silicon technology. Migration from LRS to HRS is, therefore, a logical step. It has been found that HRS provides some improvement in Q, though by far, not as much as expected from EM simulations [18]. As for the CPWs, this is believed to be caused by the surface charge if no surface passivation is present. A small library of inductors on HRS and SP HRS was designed, fabricated, and measured to verify the significance of the surface passivation and to test the expected good consistency of EM simulation and measurement on SP HRS. The geometry of the spiral coils was optimized by using a physics-based simulation tool [19], while the final EM analysis of the layout was performed in Momentum. The geometrical dimension and inductance values of the experimental inductors are summarized in Table II. The values of the implemented inductors were chosen to have an impedance $Z = j \cdot \omega \cdot L$ of the order of the reference impedance of the measurement setup at the frequency at maximum Q (e.g., 50 Ω at 3 GHz) since this contributes to minimize measurement error.

The measured Q factors (average values and variations) for SP HRS and HRS substrates are shown in Fig. 4 with an apparently good agreement of simulated results and SP HRS data.

TABLE II
INDUCTORS' LIBRARY DEFINITION

L [nH]	Turns	Outer radius [μm]	Line width [μm]	Line spacing [μm]
3.2	2	230	37	4.6
3.8	2	321	49.5	5
4.4	2	345	42.5	4.6
5.0	2	368	37.8	4.1

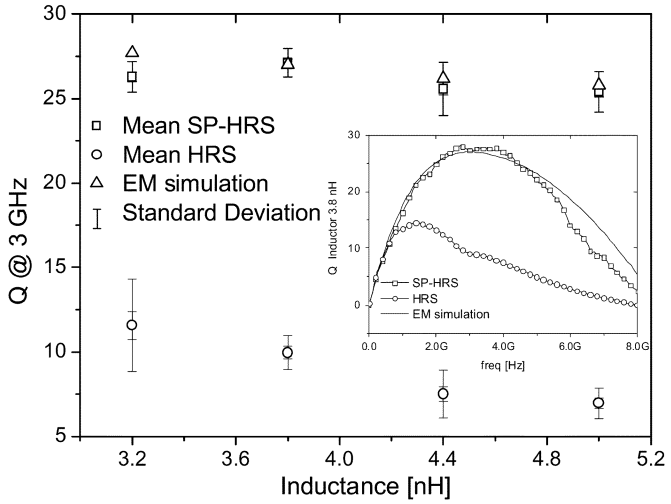

Fig. 4. Q factors of various inductors on HRS and SP HRS, as well as simulated data from Agilent's Momentum with HRS bulk properties as input parameters (20 samples considered for SP HRS and 12 samples for HRS). The Q factors versus frequency of 3.8-nH inductors on HRS, SP HRS, and from the EM simulation are shown in the inset.

Note that the much greater Q of devices built on SP HRS compared to the HRS ones is a direct consequence of the optimization being done for the SP HRS case. The inductor coils were large and the inductors were, therefore, particularly sensitive to substrate losses. This design was not optimum for the HRS wafer with the lossy surface channels.

C. Planar Transformers

Planar transformers are currently of great interest to the monolithic-microwave integrated-circuit (MMIC) design community since they can provide interstate matching in single-ended, as well as differential configurations [20]. Furthermore, their applicability as a feedback element or balun allows for novel on-chip design techniques, resulting in higher circuit performance [21]. The use of transformer libraries is practically not exploitable as the geometry of the transformer (i.e., its turn ratio and its primary and secondary inductance) depends strongly on the circuit implementation. A high degree of simulation accuracy is thus necessary to avoid multiple design cycles. Moreover, since the inductance impedance is finite, the structure has to be designed and optimized [22] for the effective loading condition and the specific frequency of operation. A transformer, having an inter-winded topology [20], [23], has been integrated by using the interconnect scheme of the DIMES-04 fabrication process on HRS and SP HRS substrates. The primary and secondary windings were adjacent.

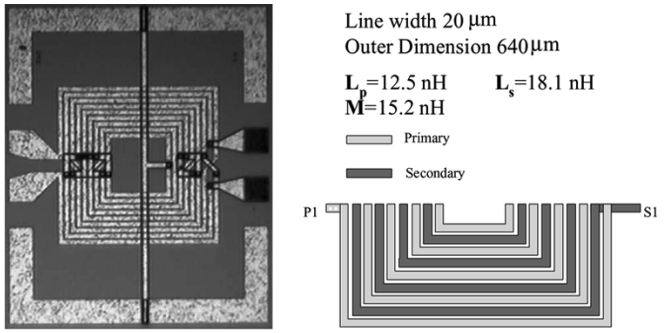

Fig. 5. (*left*) Plan-view photograph of inter-winded transformer. (*right*) Winding scheme and measured primary, secondary, and mutual inductance.

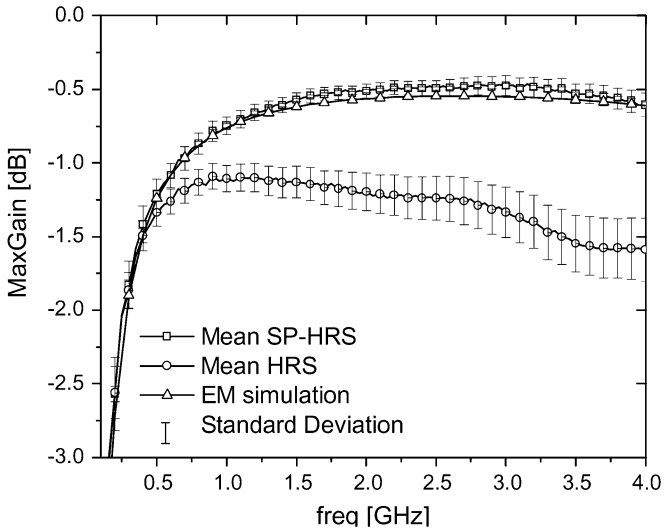

Fig. 6. Comparison of maximum available gain of transformers built on HRS and on SP HRS to the corresponding EM simulation based on HRS bulk properties (22 samples considered).

The microphotograph and the arrangement of the windings are both shown in Fig. 5.

The structure facilitates a very high magnetic coupling, given by $k = M \cdot (L_p \cdot L_s)^{-0.5}$ and $M = (Y_{11}^{-1} - Z_{11}) \cdot Z_{22} \cdot \omega^{-1}$ with M the mutual inductance, L_p and L_s the primary and secondary inductances, and Y_{ii} and Z_{ii} the admittance and impedance parameters, respectively [22]. The measured coupling factor was $k = 0.93$ for this particular transformer. It is important to note that transformer losses in the passband of these structures are caused both by losses in the metal windings and in the conductive silicon substrate [22], [24]. A more practical figure-of-merit for use by the circuit designer than the k factor is the loss under conjugate matching conditions at both the primary and secondary windings. We, therefore, have analyzed the improvement associated with the surface passivation in SP HRS compared to the HRS wafers by considering the maximum available gain given by (2)

$$\begin{aligned} \text{MaxGain} &= \left|\frac{S_{21}}{S_{12}}\right|(q - \sqrt{q^2 - \Delta}) \\ q &= \frac{(1 - |S_{21}|)^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|} \\ \Delta &= S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \end{aligned} \tag{2}$$

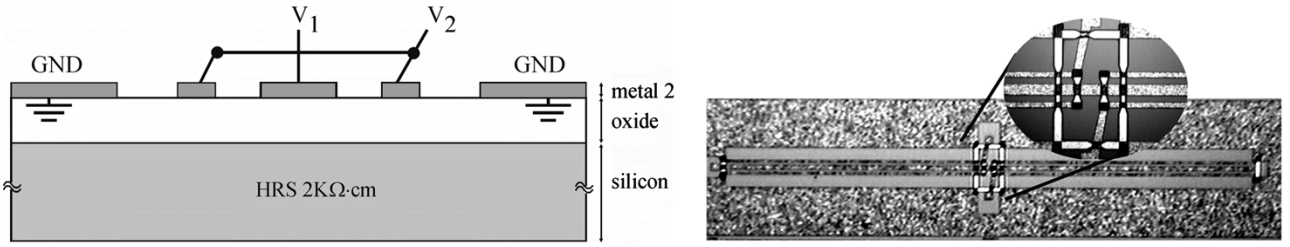

Fig. 7. (*left*) Marchand balun cross section. (*right*) Microphotograph of the integrated structure.

where S_{ij} are the scattering parameters. The measurement results were based on a custom calibration method involving on-wafer calibration of the four-port test set [25]. Fig. 6 shows a remarkable reduction of the average value and the spread in loss values for SP HRS, as compared to HRS. Also, there was very good agreement of the SP HRS data with the EM simulation. Note that with SP HRS, an improvement of 1 dB is achieved at 3.5 GHz, yielding only 0.5-dB insertion loss.

D. Marchand Balun

A common way to implement baluns at high frequencies is to use distributed structures. Such components are usually implemented in III–V process technologies since they are particularly sensitive to substrate losses. Here, we show that the SP HRS substrate allows for a silicon implementation of a Marchand balun with a performance comparable to that achievable in III–V technology [26]. A simplified cross section and a plan-view photograph of a planar coupled-line Marchand balun is shown in Fig. 7.

The design procedure used for the three coupled-line sections is similar to that in [27]. The final layout optimization was done by using ADS Momentum. The experimental verification of the Marchand balun was arranged as a back-to-back configuration of two identical balun structures avoiding multiple three-port measurements since a multiport line-reflect-match (LRM) calibration substrate and supporting software were not available at the time of measuring. The data shown in Fig. 8 present the losses of two cascaded baluns.

A clear improvement of more than 2 dB is seen for the SP HRS substrate as compared to HRS, yielding less than 1-dB loss for a single balun structure. Also, the data spread over the wafer for this component confirmed the much reduced surface effects achieved by the SP HRS. The discrepancy between measurement and simulation in the low-frequency behavior of the SP HRS balun (5–12.5 GHz) can be explained by the fact that the substrate presents not only lower losses for the fundamental TEM mode, but also for the parasitic modes (not completely dumped by the air bridges), yielding deviations from the simulated/expected transfer characteristic.

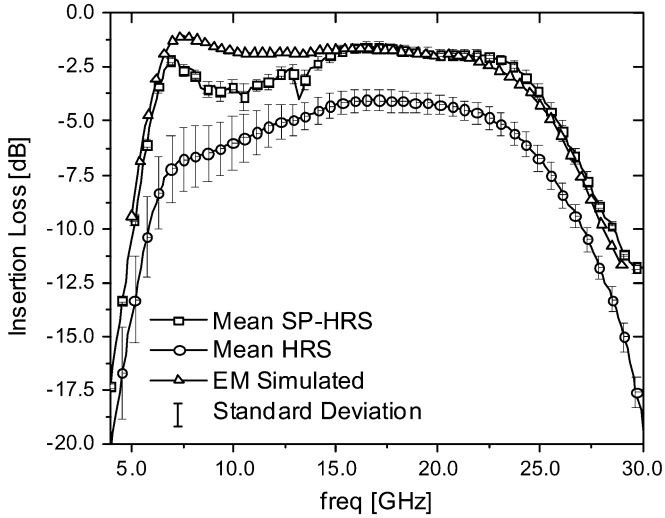

Fig. 8. Comparison of integrated Marchand balun back-to-back insertion loss on HRS and on SP HRS to the corresponding EM simulation based on HRS bulk properties (ten samples considered).

IV. Microwave Circuit Characterization

As mentioned in Section III, the design of a distributed circuit is traditionally considered to be the domain of III–V-based technologies. Besides the inherently higher operating frequencies of the GaAs- and InP-based active devices for a given breakdown voltage, as compared to their silicon counterparts, this hegemony is also due to the insulating nature of a III–V substrate that facilitates straightforward integration of the essential low-loss passives.

To demonstrate that the proposed SP HRS technology has the potential to become a valid alternative to the III–V-based solution, we have implemented a TWA by using the DIMES-04 fabrication process on both SP HRS and HRS. In Fig. 9, the schematic layout and chip photograph of the integrated two-stage TWA are given. The active stage is based on an emitter–follower–cascode topology in order to reduce the impact of the series resistance of the bipolar transistor on the artificial base and collector lines [28]. To implement the artificial transmission lines in a compact form, lumped inductors have been favored over transmission lines.

This choice can be motivated by the fact that, at frequencies below 10 GHz, for a given dc series resistance of the metallization, inductors are able to provide a much higher inductance than the lengthy transmission lines otherwise needed at these frequencies. Note that, even with HRS, the circuit design is quite complicated since layout parasitics can easily lead to unexpected amplifier characteristics. To overcome these problems, an extensive EM modeling of the entire layout, excluding the semiconductor devices, has been performed in ADS Momentum. By using the two-stage emitter–follower–cascode configuration, we achieved

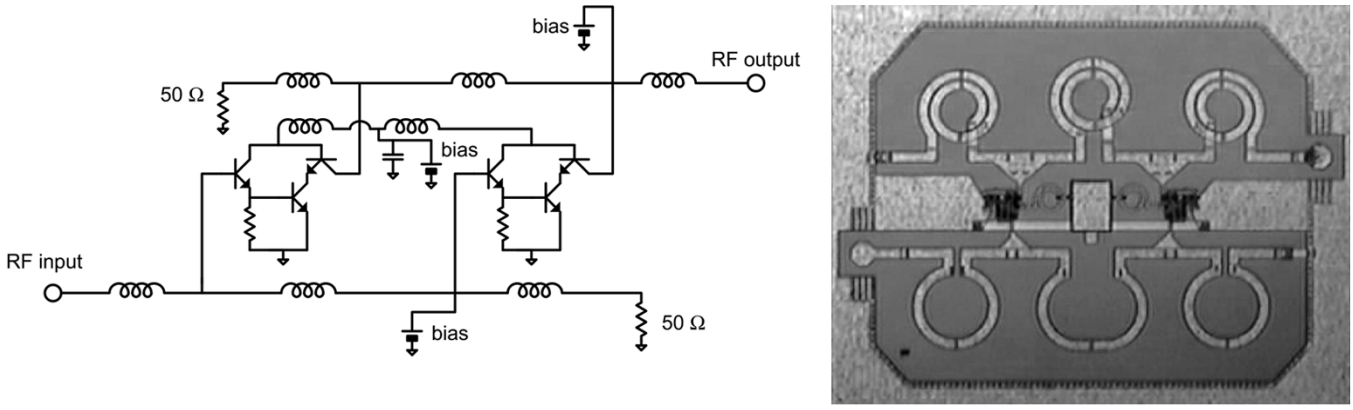

Fig. 9. Schematic and photograph of the fabricated TWA. Total chip area is $2242 \times 2099\ \mu\mathrm{m}^2$.

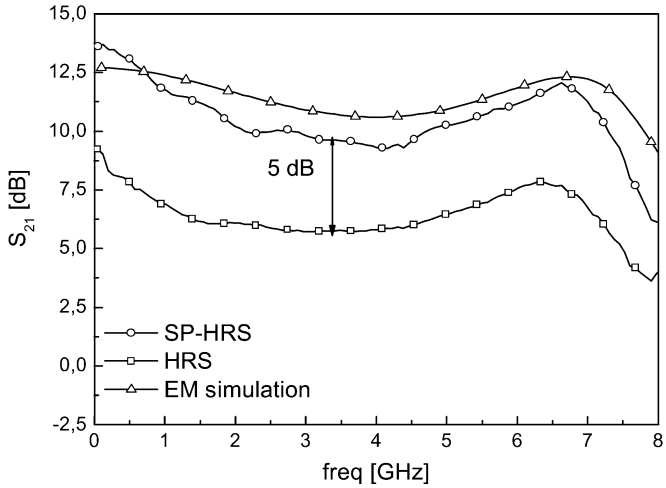

Fig. 10. On-wafer measured characteristics of the distributed amplifier on HRS and on SP HRS in comparison to EM simulation based on HRS bulk properties.

TABLE III
COMPARISON OF TWA'S BUILT-IN DIFFERENT TECHNOLOGIES

Technology - Device	f_{-3dB} [GHz]	f_T [GHz]	Gain [dB]	f_{-3dB}/f_T
InP - HEMPT [29]	92	130	13	0.70
InP - HBT [30]	74	150	13	0.49
SP-HRS	**75**	**13**	**10**	**0.57**

a 10-dB flat gain and a 7.5-GHz bandwidth (Fig. 10). Note that this result was achieved by using the HV transistor of the DIMES-04 process technology, having an $f_T = 13$ GHz only (Table I).

A clear improvement of the in-band gain for the SP HRS implementation of the amplifier with respect to standard HRS is noted. No spreading analysis is attempted for this device because it is not possible to separate the contribution of active devices to the overall spreading.

Such information may, therefore, be misleading. In Table III, the fabricated amplifier is compared to state-of-the-art circuits realized in III–V technologies. From Table III, it is evident that, in spite of the much lower f_T, the realized design has a figure-of-merit ($f_{-3\,\mathrm{dB}}/f_T$) comparable to that of state-of-the-art III–V TWA circuit results.

V. CONCLUSION

The results presented and discussed in this paper have provided evidence that surface passivation is essential to fully leverage the excellent properties of HRS as a microwave substrate. Surface passivation not only greatly reduces the effective substrate loss, but also lowers the spread of the characteristics of the integrated passive components. This has been demonstrated for spiral inductors and transformers, CPW transmission lines, and Marchand baluns. Migration of an npn bipolar transistor integration process from LRS to HRS substrates is possible without any significant shift in device characteristics by using a p-well structure that leads to a raised p-type doping near the collector–substrate junction isolation. Integration of transistors and passive components with controlled characteristics has been demonstrated for a TWA circuit featuring 7.5-GHz bandwidth at only 13-GHz transistor cutoff frequency. The excellent agreement of the characteristics of the measured passive components and the TWA fabricated on SP HRS with the simulated characteristics based on EM simulation and HRS bulk properties marks the main conclusion from this study: surface-passivated HRS is a true microwave substrate that can accurately be described by its bulk properties so that the transfer from layout simulation to chip integration can be achieved in one single cycle, thus allowing for fast design realization at low cost.

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