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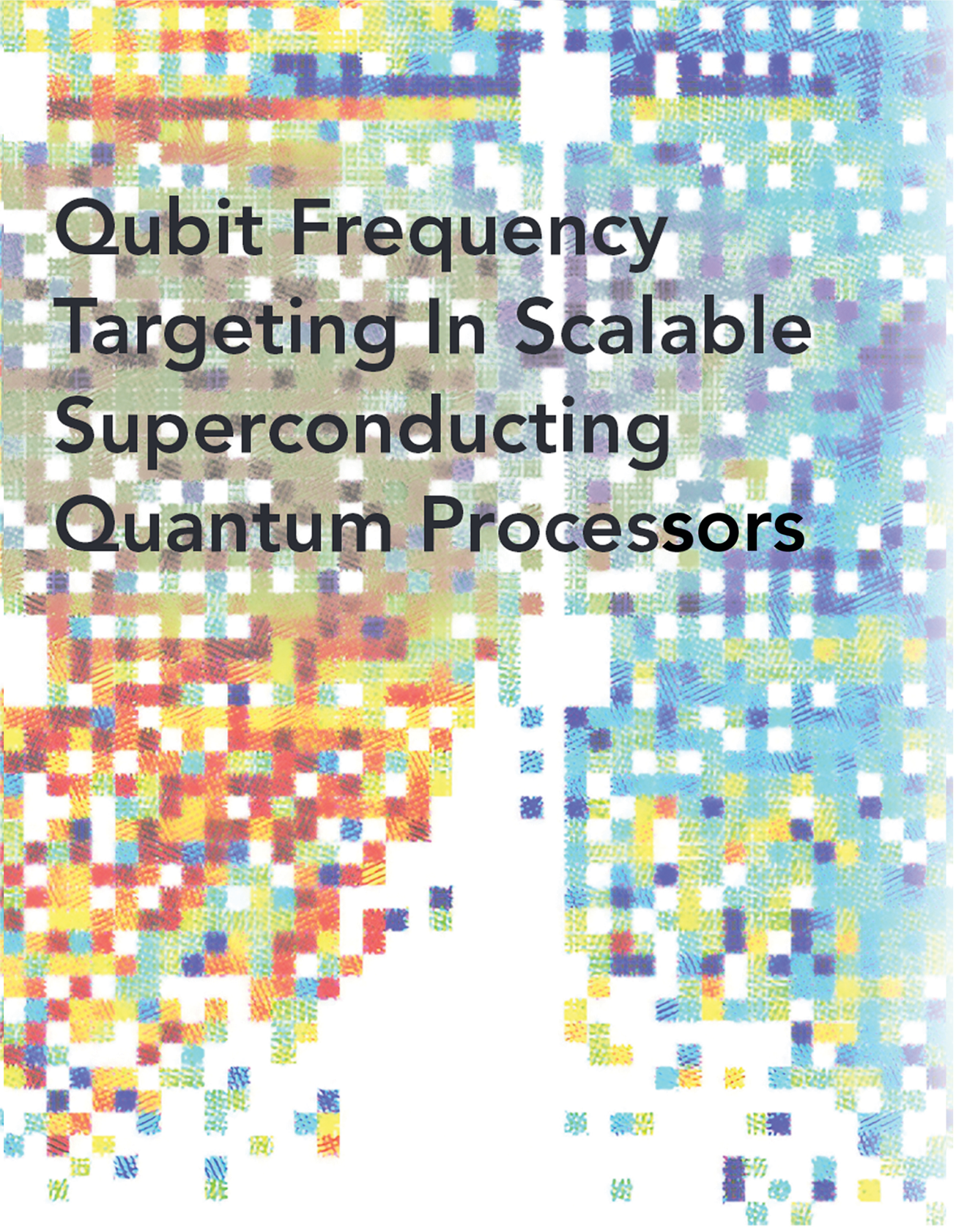

Qubit Frequency Targeting In Scalable Superconducting Quantum Processors

Nandini Muthusubramanian

Propositions

accompanying the dissertation

Qubit frequency targeting in scalable superconducting quantum processors

by

Nandini MUTHUSUBRAMANIAN

1. Contact resistance between the interface of Josephson junctions and superconducting metallization layer is an overlooked source of dielectric losses (Chapter 5 of this thesis).
2. Conductance variation of Josephson junctions increases with substrate roughness (Chapters 4 and 5 of this thesis).
3. Dolan-bridge junctions exhibit better intra-sample reproducibility whereas bridgeless Manhattan-style junctions show superior batch-to-batch reproducibility (Chapters 4 and 5 of this thesis).
4. Shadow evaporation of Josephson junctions will always hinder scalability of superconducting qubits (Chapters 5 and 7 of this thesis).
5. Atmospheric water vapour is an important driver of temporal variation in Al/AlO_x/Al Josephson junctions (Chapter 6 of this thesis).
6. Post-fabrication strategies for tuning junction conductance will become the mainstay of future qubit frequency targeting efforts (Chapter 6 of this thesis).
7. Love is to life what entanglement is to atoms.
8. Ego is justified only during the growth spurts of adolescence and the lengthy journey of a PhD.
9. Choosing to overlook the accomplishments and sacrifices of scientists is a better alternative to weaponizing their work.
10. Quantum computing industry has a once-in-a-generation opportunity to make the circular economy of critical metals a reality.

These propositions are regarded as opposable and defendable, and have been approved as such by the promotors Prof. Dr. L. DiCarlo and Prof. Dr. L. Kuipers.

Qubit frequency targeting in scalable superconducting quantum processors

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Dissertation

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by

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Keywords: Josephson junction, superconducting, qubit, fabrication, frequency, scalability …

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Cover by: Nandini Muthusubramanian. **Front:** Heatmap of a TSV wafer dataset with Dolan-bridge Josephson junctions. **Back:** Artistic rendition of an SEM image of an non-connectorized SQUID loop designed for Dolan-bridge junctions and a flux-bias line.

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”For a solitary animal egoism is a virtue that tends to preserve and improve the species; in any kind of community it becomes a destructive vice.”

Erwin Schrödinger: What is Life?

CONTENTS

LIST OF SYMBOLS

$\hbar$	Reduced Planck constant
$\Delta(T)$	Superconducting energy gap (eV)
k_{B}	Boltzmann constant
δ	Josephson phase
Φ_0	Magnetic flux quantum
E_J	Josephson energy (GHz)
λ_{L}	London penetration depth (nm)
T_{c}	Critical temperature (K)
I_{c}	Critical current (mA)
G	Conductance (μS)
A_{overlap}	Designed JJ overlap area ($\mu\mathrm{m}^2$)
G_{n}	Normal-state conductance (μS)
Φ_{ext}	External magnetic flux
E_{c}	Charging energy (MHz)
α	Anharmonicity (MHz)
M	Superconducting gap constant (GHz/mS)
T_1	Qubit relaxation time (μs)
T_2	Qubit dephasing time (μs)
v_{p}	Phase velocity (m/s)
f_{01}	Qubit transition frequency (GHz)
g	Resonator-qubit coupling strength (MHz)
$\Delta_{\mathrm{r}-01}$	Resonator-qubit detuning (MHz)
Δ_{ji}	Qubit pair detuning (MHz)

L_{k}	Kinetic inductance (pH)
Q_{i}	Internal quality factor
Q_{e}	External quality factor
A'_{overlap}	Actual JJ overlap area ($\mu\mathrm{m}^2$)
W_{b}	JJ bottom electrode designed width (nm)
W_{t}	JJ top electrode designed width (nm)
$f_{\mathrm{q,pred}}$	Predicted qubit frequency (GHz)
$f_{\mathrm{q,meas}}$	Measured qubit frequency (GHz)
$f_{\mathrm{r,des}}$	Designed readout resonator frequency (GHz)
$f_{\mathrm{r,meas}}$	Measured readout resonator frequency (GHz)
d	Radial distance (mm)
H	Top resist height (nm)
W'_{b}	JJ bottom electrode actual width (nm)
W'_{t}	JJ top electrode actual width (nm)
T_{b}	Designed JJ bottom electrode thickness (nm)
T'_{b}	Actual JJ bottom electrode thickness (nm)
S_{a}	Areal surface roughness
μ_G	Mean of conductance ($\mu\mathrm{S}$)
$\Delta\mathrm{G}$	Conductance change ($\mu\mathrm{S}$)
w_0	Beam radius ($\mu\mathrm{m}$)
w'_0	Final beam radius ($\mu\mathrm{m}$)
z_{R}	Rayleigh range ($\mu\mathrm{m}$)
P_{L}	Laser optical power (mW)
$P_{\mathrm{L,max}}$	Maximum laser optical power (mW)
I	Laser intensity ($\mathrm{mW/cm}^2$)
τ	Laser irradiation time (min)
$\mu_{\Delta G}$	Mean conductance change ($\mu\mathrm{S}$)
$\sigma_{\Delta G}$	Standard deviation of conductance change ($\mu\mathrm{S}$)

Δf_{q} Qubit frequency change (MHz)

σ_f Frequency targeting precision (MHz)

T_{RTA} Rapid thermal annealing process temperature ($^{\circ}\mathrm{C}$)

LIST OF ACRONYMS

SQP	Superconducting quantum processor
QEC	Quantum error correction
JJ	Josephson junction
VIO	Vertical input/output
TSV	Through-silicon via
SEM	Scanning electron microscopy
RT	Room temperature
TLS	Two-level system
BCS	Bardeen-Cooper-Schrieffer
SIS	Superconductor–insulator–superconductor
SQUID	Superconducting quantum interference device
RSFQ	Rapid single flux quantum
RCSJ	Resistively and capacitively shunted junction
CPB	Cooper-pair box
cQED	circuit quantum electrodynamics
SNR	Signal-to-noise ratio
CPW	Coplanar waveguide
CPHASE	Controlled-phase
CZ	Controlled-Z
CR	Cross-resonance
TEM	Transverse electromagnetic mode
TL	Transmission line
FBL	Flux-bias line
RR	Readout resonator
QND	Quantum non-demolition
PF	Purcell filter
VNA	vector network analyser
PCB	Printed circuit board
SMP	Subminiature push-on
ALD	Atomic layer deposition
UV	Ultra-violet
TCB	Thermocompression bonding
GDSII	Graphic design system II
IPA	isopropanol
HMDS	Hexamethyldisilazane
XPS	X-ray photoelectron spectroscopy
AFM	Atomic force microscopy
BSS	Beam step size
EOL	End-of-line
DRIE	Deep reactive-ion etching

TDMAT	Tetrakis(dimethylamino)titanium
RIE	Reactive-ion etching
CAD	Computer-aided design
NMP	N-methylpyrrolidone
HSQ	Hydrogen silsesquioxane
MIBK	Methyl isobutyl ketone
MMA	Methyl methacrylate
PMMA	Poly(methyl methacrylate)
PMGI	Poly(dimethylglutarimide)
JTWPA	Josephson travelling wave parametric amplifier
CD	Critical dimension
AOI	Automated optical inspection
CCD	Charge-coupled device
APS-TASQ	Automated probe station for thermal annealing of superconducting qubits
ROI	Region of interest
SI	Supplementary information
CV	Coefficient of variation
DUT	Device under test
RSD	Residual standard deviation
FG	Forming gas
EIA	Environmentally-induced ageing
AB	Airbridge
LA	Laser annealing
RTA	Rapid thermal annealing
PSU	Power safety unit
PID	Proportional-integral-derivative

SUMMARY

Superconducting qubits are a leading platform holding potential for realization of fault-tolerant universal quantum computation. However, experimental demonstration of quantum fault tolerance may require scaling up to hundreds of physical qubits (Chapter 1).

The non-linearity of superconducting qubits emerges from current-phase relation in superconducting tunnel junctions, better known as Josephson junctions (Chapter 2). The transmon is a special case of the charge qubit with a large parallel shunt capacitance which results in suppression of charge noise sensitivity at the cost of reduced anharmonicity. The resonance frequency of a transmon depends on the charging energy contributed by the total capacitance of the circuit and the non-linear inductive energy of a Josephson junction. This inductance is in turn directly proportional to the room-temperature conductance of the tunnel junctions, determined by the junction area and thickness of the tunnel barrier. The manipulation of superconducting artificial atoms by strongly coupling to microwave photons is achieved using circuit quantum electrodynamics. In planar superconducting circuits, on-chip transmission lines based on coplanar waveguide geometry is routinely employed to manipulate and readout the qubit states (Chapter 3).

The QuSurf architecture for a full-stack quantum computer features an extensible surface code comprising flux-tunable qubits with four-port connectivity to nearest neighbours. The first distance-3 logical qubit requires a 2D lattice of 17 qubits to perform quantum error correction. At the hardware level, we concurrently pursue a short-term low-overhead and a long-term high-overhead strategy with lateral and vertical input/output signal routing respectively (Chapter 3). The usefulness of a superconducting quantum processor depends on three main fabrication metrics, the physical yield of individual components, how well it matches the chip design specifications and its susceptibility to environmentally-induced decoherence (Chapter 4). Due to the nanometer-scale of Josephson junctions, it is particularly challenging to reliably target a desired qubit frequency within a margin of 50 MHz.

This thesis outlines the current fabrication bottlenecks which limit scalability with a focus on increasing the precision of qubit frequency targeting. The addition of through-silicon vias for vertical routing of signals and increasing the density of on-chip components add layers of complexity to this problem, which necessitates testing two variants of Josephson junctions with subtle differences in the fabrication process and its geometry. The primary objective is to systematically identify and quantify the sources of deviation affecting fabrication of the two Josephson junctions variants. To determine the causes of spread in Josephson junctions aside from intrinsic variations in the tunnel barrier, room-temperature conductance measurements are compared for thousands of test junction structures fabricated at wafer-

scale. (Chapter 5). We also develop customized fabrication tools and techniques to achieve selective or global tailoring of qubit frequencies (Chapter 6). The thesis concludes with a summary on the factors identified in this work which impacts qubit frequency targeting, a reflection on the limitations of this work and an outlook on specific aspects of scalability of superconducting qubits in the near future (Chapter 7).

SAMENVATTING

Supergeleidende qubits zijn een toonaangevend platform met potentie voor de realisatie van fouttolerante universele kwantumberekening. Echter, voor de experimentele demonstratie van kwantum fouttolerantie is mogelijk een opschaling naar honderden fysieke qubits vereist (hoofdstuk 1).

De niet-lineariteit van supergeleidende qubits komt voort uit de stroom-faserelatie in supergeleidende de tunneljunctie, beter bekend als Josephson-junctie (hoofdstuk 2). De transmon is een speciaal geval van de ladingsqubit met een grote parallelle shuntcapaciteit die resulteert in onderdrukking van de gevoeligheid voor ladingsruis, ten koste van een reductie in de anharmoniciteit. De resonantiefrequentie van een transmon hangt af van de ladingsenergie die wordt bijgedragen door de totale capaciteit van het circuit en de niet-lineaire inductieve energie van een Josephson-junctie. Deze inductie is op zijn beurt evenredig met de geleiding bij kamertemperatuur van de tunneljunctie, bepaald door het oppervlak en de dikte van de tunnelbarrière. De manipulatie van supergeleidende kunstmatige atomen door sterke koppeling aan microgolffotonen wordt bereikt met behulp van circuitkwantumelektrodynamica. In vlakke supergeleidende circuits worden transmissielijnen gebaseerd op coplanaire golfgeleiders regelmatig gebruikt om de qubit-toestand te manipuleren en uit te lezen (hoofdstuk 3).

De QuSurf-architectuur voor een full-stack kwantumcomputer beschikt over een uitbreidbare oppervlaktecode bestaande uit flux-verstelbare qubits verbonden met de dichtstbijzijnde buren. De eerste logische qubit met afstand 3 foutcorrectie vereist een 2D-rooster van 17 qubits om kwantumfoutcorrectie uit te voeren. Op hardwareniveau streven we gelijktijdig een kortetermijnstrategie met lage overhead en een langetermijnstrategie met hoge overhead na, met respectievelijk laterale en verticale input/output-signaalroutering (hoofdstuk 3). Het nut van een SQP hangt af van drie belangrijke fabrication metrieken: de fysieke opbrengst van individuele componenten, hoe goed deze overeenkomt met de specificaties van het chipontwerp en de gevoeligheid ervan voor door de omgeving veroorzaakte decoherentie (hoofdstuk 4). Vanwege de nanometerschaal van Josephson-juncties is het bijzonder uitdagend om op betrouwbare wijze een gewenste qubit-frequentie binnen een marge van 50 MHz te targeten.

Dit proefschrift schetst de huidige knelpunten in de fabricage die de schaalbaarheid beperken met de nadruk op toename de precisie van qubit-frequentietargeting. De toevoeging van door-silicium via's (TSV's) voor verticale I/O en het vergroten van de dichtheid van componenten op de chip voegen lagen van complexiteit toe aan dit probleem, wat het testen van twee varianten van Josephson-juncties noodzakelijk maakt met subtiele verschillen in het fabricatie proces en de geometrie. Het voornamelijke doel is het systematisch identificeren en kwantificeren van de bronnen

van afwijkingen die de fabricage van de twee Josephson-junctie varianten beïnvloeden. Om de oorzaken van verspreiding in Josephson-juncties te bepalen, afgezien van de intrinsieke variaties in de tunnelbarrière, worden geleidingsmetingen bij kamertemperatuur vergeleken voor duizenden teststructuren die op waferschaal zijn vervaardigd. (hoofdstuk 5). We ontwikkelen ook aangepaste fabricagegereedschap en -technieken om selectieve of globale afstemming van qubit-frequenties te bereiken (hoofdstuk 6). Het proefschrift wordt afgesloten met een samenvatting van de factoren die in dit werk zijn geïdentificeerd en die van invloed zijn op de qubit-frequentietargeting, een reflectie op de beperkingen van dit werk en een kijk op specifieke aspecten van de schaalbaarheid van supergeleidende qubits in de nabije toekomst (hoofdstuk 7).

தொகுப்புரை

குறை சகிப்புநிலை உடைய உலகளாவிய குவாண்டக் கணினியியலின் ஆற்றல்வளத்தைக் கையாளும் முன்னணி இயங்குதளமாக மிகைக்கடத்து குவைய இரும நிலைகள் (குவாண்டம் பிட் எனப்பெறும் க்யூபிட்கள்) உள்ளன. எனினும் குவையம் (குவாண்டம்) குறை சகிப்புநிலை சோதனை செயல்முறை அளவீட்டில் நூற்றுக்கணக்கில் இயற்பியல் சார்ந்த குவைய இரும நிலைகள் (க்யூபிட்கள்) தேவைப்படலாம். (இயல் 1)

மிகைக்கடத்து குவாண்ட இரும நிலைகளின் (க்யூபிட்கள்) நேரியல் சார்பின்மை ஜோசப்சன் சந்திப்புகள் எனவும் வழங்கப் பெறும் மிகைக்கடத்து சுரங்க சந்திப்பு-களில் மின்னோட்டம் - பிரிவு தொடர்பிலிருந்து வெளிப்படும். (இயல் 2)

ட்ரான்ஸ்மோன் என்பது, பெரிய இணைத்தட தாங்குதிறனுடன் கூடிய, இணக்கமின்மையின் குறைந்த அளவில், இரைச்சல் உணர்திறனில் ஒடுக்கத்தை விளைவிக்கும் ஒரு சிறப்பு வகையான மின்னூட்டு குவைய இரும நிலை (க்யூபிட்) ஆகும். ட்ரான்ஸ்மோனின் அதிர்வு இடைவெளி, மின்சுற்றின் மொத்த-தாங்குதிறனும், ஒரு ஜோசப்சன் சந்திப்பின் நேரியல் சார்பற்ற தூண்டு ஆற்றலும், பங்களிக்கும் மின்னேற்ற ஆற்றலை அடிப்படையாகக் கொண்டது. இத்தூண்டல், முறைப்படி (வரும்போது), சந்திப்பு பரப்பு மற்றும் சுரங்கத் தடுப்பின் தடிப்பு மூலம் தீர்மானிக்கப் பெற்ற, அறைவெப்பநிலையில் சுரங்க சந்திப்புகளின் கடத்துத்திறனுக்கு நேர்விகிதச்சார அளவில் உள்ளது. மிகைக்கடத்து செயற்கை அணுக்களை நுண்ணலை ஒளியன்களோடு (போட்டோன்ஸ்) வலிமையாகப் பிணைத்த கையாளுகை, மின்சுற்று குவையம் (குவாண்டம்) மின்னணு-இயக்கத்தைப் பயன்படுத்தி சாதிக்கப் பெறுகிறது. சமத்தள மிகைக்கடத்து மின்சுற்றுகளில் ஒருதள அலைவழிகாட்டி வடிவியலின் அடிப்படையில் நுண்சில்லு (on-chip) பரிமாற்ற வரிகள், இரும (க்யூபிட்) நிலைகளைக் கையாளவும் படிக்கவும், வழக்கமாக செயல்படுத்தப் பெறுகிறது. (இயல் 3)

ஒரு முழு குவிய குவையம் (குவாண்டம்) கணினிக்கான க்யூஸ்ர்ப் கட்டமைப்பு, அருகமை உறுப்புகளோடு நான்கு-முனை இணைப்புடன் கூடிய பெருக்கு (ஃப்ளக்ஸ்) ஒத்திசைக்கக் கூடிய அல்லது சீர் செய்யக் கூடிய க்யூபிட்ஸ் உள்ளடக்கிய ஒரு நீட்டிக்கக் கூடிய மேற்பரப்பு குறியீட்டைத் தோற்றுவிக்கிறது. முதல் தூர - 3 தர்க்க ரீதியிலான க்யூபிட்டுக்கு குவைய பிழை திருத்தம் நிகழ்த்துவதற்கு 17 க்யூபிட்டுகளின் இரு பரிமாண பின்னல் தேவைப்படுகின்றது. குறுக்கும் நெடுக்குமான உள்ளீடு / வெளியீடு முறையே சைகை / சமிக்ஞை செல்வழித்தடத்துடன் கூடிய கணினி வன்பொருள் நிலையில் ஒரு குறுகிய கால குறைந்த செலவீன மற்றும் நீண்ட கால உயர் செலவீன செயல் நெறிமுறையை ஒரே நேரத்தில் தொடர்ந்து செய்கிறோம். (இயல் 3)

ஒரு SQP-யின் பயன்பாடு மூன்று முக்கியமான அளவுகோல்களால் அமைகிறது, தனிப்பட்ட கூறுகளின் இயற்பியல்சார் விளைவு, நுண்சில்லு வடிவமைப்பு தரவரைவுகள் மற்றும் சுற்று-ச்சூழல் தூண்டும் சீர்குலைவிற்கான ஆட்படு-

மை ஆகியவற்றிற்கு எவ்வாறு பொருந்துகிறது என்பதை அடிப்படையாகக் கொண்டது. (இயல் 4) ஜோசப்சன் சந்திப்புகளின் மீநுண்ணளவி அளவுகோல் காரணத்தால் 50 MHz எல்லைக்குள் ஒரு விரும்பிய க்யூபிட் அதிர்வெண் நம்-பத்தக்க இலக்கை அடைவது குறிப்பிட-த்தக்க சவாலாக உள்ளது.

இவ்வாய்வு க்யூபிட் அதிர்வெண் இலக்கை அடைவதில் துல்லியத்தை அதி-கப்படுத்தும் கவனத்துடன் கூடிய அளவிடுதலைக் கட்டுப்படுத்தும் மின்- பு-னைவு சிக்கல்களை வரைகோடிட்டுக் காட்டுகிறது. நிலைக்குத்தான I/O மற்-றும் நுண்சில்லு கூறுகளின் அடர்த்தி அதிகரிப்பிற்கான சிலிக்கான் வழிமூல (TSV) கூட்டல், பிரச்சினையின் பெரும் சிக்கலின் அடுக்குகளைக் கூடுதலாக்-குகின்றன. இப்பிரச்சினை, புனைவு செயல்முறையிலும் மற்றும் அதன் வடி-வியலிலும் உள்ள நுண்ணிய வேறுபாடுகள் கூடிய ஜோசப்சன் சந்திப்புகளின் இரு மாற்றுருகளின் சோதனை இன்றியமையாததாகிறது. ஜோசப்சன் சந்-திப்புகளின் இரு மாற்றுருகளின் புனைவைப் பாதிக்கும் பிறழ்ச்சி மூலங்க-ளை முறையாக அடையாளம் காணுதலும் அளவிடுதலும் முதன்மையான நோக்-கம் ஆகும். சுரங்க தடுப்பின் உள்ளாழ்ந்த வேறுபாடு-களிலிருந்து தனித்த ஜோ-சப்சன் சந்திப்புகளில் பரவுதலின் காரணங்களை தீர்மானிக்க, அறைவெப்-பநிலை கடத்துதிறன் அளவைகள், வேபர் அளவில் புனையப்பெற்ற ஆயிரக்-கணக்கான சோதனை சந்திப்பு அமைப்புகளுக்காக ஒப்பிடப்பெறுகின்றன. (இயல் 5) தேர்தெடுக்கப்பெற்ற அல்லது உலகளாவிய க்யூபிட் அதிர்வெண்க-ளின் இணைப்பை சாதிக்க நாங்கள் மேலும் தனி-ப்பயனாக்க புனைவு கரு-விகளையும் மற்றும் நுட்பங்களையும் உருவாக்கு-கிறோம். (இயல் 6) இப்ப-ணியில் க்யூபிட் அதிர்வெண் இலக்கடைவதில் தாக்கங்கள் ஏற்படுத்துவதில் அடையாளம் காணப்பெற்ற காரணிகள், இப்பணியின் எல்லை வரையறை-கள் பற்றிய சிந்தனைகள் மற்றும் அடுத்து வருங்காலத்தில் மிகைக்கடத்து க்-யூபிட்களின் அளவீடுகளின் சிறப்பு அம்சங்கள் பற்றிய ஒரு கண்ணோட்டம் ஆகியவற்றின் தொகுப்புடன் இவ்வாய்வு நிறைவுறுகிறது. (இயல் 7)

TRANSLATION KEY

குறை சகிப்புநிலை : fault-tolerant; ஆற்றல்வளம் : potential; குவாண்டக் கணி-னியியல் : quantum computation; மிகைக்கடத்து குவைய இரும நிலைகள்: super-conducting qubits; நேரியல் சார்பின்மை : non-linearity; மின்னோட்டம் - பிரிவு தொடர்பு : current-phase relation; மின்னூட்டு குவைய இரும நிலை : charge qubit; அதிர்வு இடைவெளி : resonance frequency; இரைச்சல் உணர்திறன் : noise sensitivity; இணக்கமின்மை : anharmonicity; ஒடுக்கம் : suppression; இணைத்தடம் : parallel shunt; சுரங்கம் : tunnel; சந்திப்புகள் : junctions; தாங்குதிறன் : capacitance; மின்-சுற்று : circuit; சந்திப்பு பரப்பு : junction area; சுரங்கத் தடுப்பின் தடிப்பு : tunnel barrier thickness; அறைவெப்பநிலை: room temperature; நேரியல் சார்பற்ற : non-linear; தூண்டு ஆற்றல் : inductive energy; அணுக்கள் : atoms; நுண்ணலை : microwave; ஒளியன்கள் : photons; மின்னணுஇயக்கம் : electrodynamics; சமத்தள : planar; ஒருதள : co-planar; அலைவழிகாட்டி : waveguide; வடிவியல் : geometry; நுண்-சில்லு : on-chip; பரிமாற்ற வரிகள் : transmission lines; கட்டமைப்பு : architecture; இரு பரிமாண பின்னல் : 2-dimensional lattice; அருகமை உறுப்புகள் : nearest neighbours; இணைப்பு : connectivity; பெருக்கு (ஃப்ளக்ஸ்) : flux; ஒத்திசைக்கக் / சீர் செய்யக் கூடிய : tunable; மேற்பரப்பு குறியீடு : surface code; தர்க்க ரீதியி-லான : logical; பிழை திருத்தம் : error correction; உள்ளீடு / வெளியீடு : input /

output; சைகை / சமிக்ஞை : signal; செல்வழித்தடம் : routing; இயற்பியல்சார் விளைவு : physical yield; நுண்சில்லு வடிவமைப்பு : chip design; தரவரைவுகள் : specifications; சுற்றுச்சூழல் தூண்டும் : environmental inducing; சீர்குலைவ : decoherence; ஆட்படுமை : susceptibility; மீநுண்ணளவி : nanometer; எல்லை : margin; அதிர்வெண் : frequency; இலக்கை அடைவது : target; துல்லியம் : precision; அளவிடுதல் : scalability; மின்புனைவு : current fabrication; அடர்த்தி : density; கூறுகள் : components; பரவுதல் : spread; கடத்துதிறன் : conductance.

1

INTRODUCTION

Quantum computing, heralded by the conceptualization of qubits in the 1980s, has evolved into a multidisciplinary field at the intersection of mathematics, computer science, and quantum mechanics. The chapter gives a brief overview of recent technical and engineering breakthroughs in scalability, error correction and fault-tolerant quantum computing. It touches upon the hardware-agnostic metric of quantum volume as a meaningful framework for evaluating the performance of different quantum hardware platforms. The second half of the chapter describes the structure and research questions addressed by this thesis.

1

1.1. SUPERCONDUCTING QUBITS: FROM CONCEPT TO COMMERCIALIZATION

Qubits, the fundamental unit of quantum information, have been engineered using different physical implementations such as superconducting circuits, optical quantum systems, trapped ions, neutral atoms, quantum dots to name a few. During the 1980s, the hybridization of mathematics, computer science and quantum mechanics brought to fruition the idea of a quantum mechanical computing automaton [1–3]. Quantum computing is probabilistic since each qubit registers a wave function with the superposition of the $|0\rangle$ and $|1\rangle$ states, whereas classical computing is deterministic where each bit registers either 0 or 1. The pure state of a two-level quantum system is expressed as a superposition of two energy eigenstates $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ where α and β are complex amplitudes such that $|\alpha|^2 + |\beta|^2 = 1$. The prospect of quantum advantage in computing is demonstrated by the exponential speed up of Shor's algorithm for prime number factoring, which can break public-key cryptography schemes such as the Rivest-Shamir-Adleman (RSA) cryptosystem [4, 5]. Several technical and engineering advances in the field have enabled improved coherence times, monolithic scaling of physical qubits, fast quantum non-demolition readout and active depletion, fidelity in qubit state preparation and universal gate operation [6–11]. Current research progress by academic groups worldwide and industrial giants like IBM and Google is pushing the envelope on realization of fault-tolerant quantum computing using this platform. Superconducting quantum processors (SQP) have scaled to enable key demonstrations of quantum-computational advantage [12] and milestone demonstrations of quantum error correction [13–15] on the road to fault-tolerant quantum computing. The first commercial development of a 1000-plus qubit device with the ytterbium-171 neutral atom platform was announced by Atom Computing in late 2023 [16]. Each quantum hardware platform comes with a host of strengths and limitations; necessitating a hardware-agnostic metric introduced by IBM called *quantum volume* [17] to assess the computational capability of a quantum computer. It is mathematically represented as

$$V_Q = \max_{n<N} \left(\min \left[n, \frac{1}{n\varepsilon_{\text{eff}}(n)} \right]^2 \right),$$

where N is the number of physical qubits, ε_{eff} is the effective error rate, influenced by the necessary gate overhead in scenarios where all-to-all connectivity, full parallelism and appropriate gate set are unavailable, thereby encompassing errors arising from both single and two-qubit gates. However there is still debate in the community with regards to QV being a catch-all metric to accurately predict a quantum computer's performance. Volumetric benchmarking is an intuitive and meaningful framework for visualizing multiple circuits as application-oriented benchmarks such as, but not limited to quantum Fourier transform, variational quantum eigensolver and Deutsch-Jozsa algorithm [18]. Examples of volumetric benchmarking are shown in Fig. 1.1, where the *circuit width* implies the number of physical qubits and the normalized *circuit depth*, which refers to the depth of the circuit after transpilation to a standard gate set, which comprises of some single and two-qubit gates

with all-to-all connectivity. The result fidelity is characterized by comparing the probability distributions of the observed outcomes to the ideal outcomes for a given circuit. The result fidelity is high for all wide and shallow circuits using the Quantinuum-H1.1 processor due to its all-to-all connectivity featuring up to five parallel two-qubit gate operations. The current world-leader in achieving the highest quantum volume (524,288) to date is the Quantinuum H-1 trapped ion using the quantum charged couple device architecture containing $N = 20$ physical qubits [19].

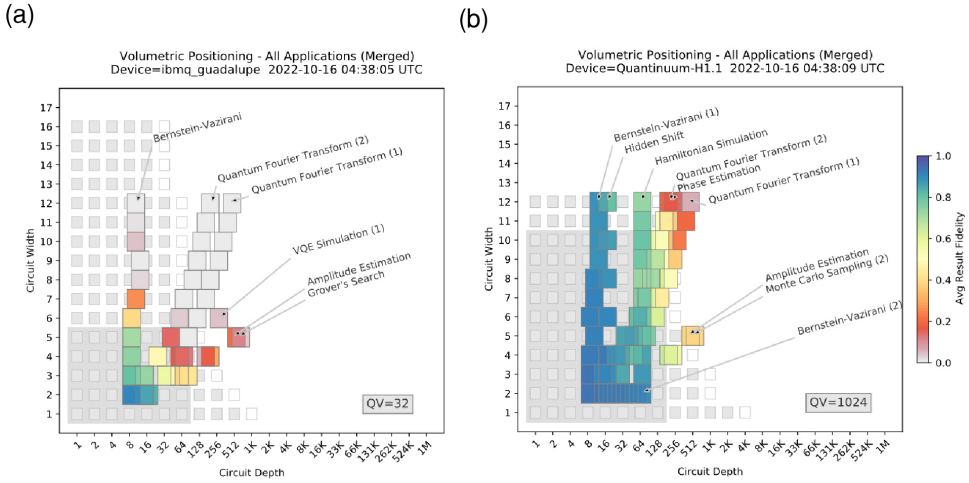


Figure 1.1: Quantum algorithms- and application-oriented performance benchmarking using the quantum volume framework plotted in a circuit width $\times$ depth volumetric space (a) IBM Guadalupe 16-qubit superconducting quantum processor with a measured $V_Q = 32$ (b) Quantinuum-H1.1 12-qubit trapped-ion quantum processor with a measured $V_Q = 1024$. Reprinted from Lubinski *et al.* 2023 [18] under Creative Commons CC BY 4.0 license.

1.2. QUANTUM FAULT TOLERANCE

Classical error correction codes for information theory enabled the development of high-performance classical computing, telecommunications and a myriad of other applications. The classical Hamming codes, for instance, represents a pioneering example of error correction in classical information processing [20]. Invented by Richard Hamming in 1950 during his post at Bell Telephone Laboratories[1], the **Hamming(7,4)** code is a linear error-correcting code that can detect and correct single-bit errors in transmitted data. It operates by encoding 4 data bits into a 7-bit codeword, where the additional 3 bits are parity-check bits that can correct any

[1] Now known as Nokia Bell Labs

single-bit error, or detect all single-bit and two-bit errors. This method significantly improves the reliability of data transmission in classical systems.

Quantum information however cannot be duplicated similar to classical information due to the no-cloning theorem, therefore the computation time is directly limited by the decoherence rate of physical qubits. This led to the exploration of quantum error correction (QEC) strategies such as repetition codes which provide redundancy by storing the arbitrary state of a qubit in a system of highly *entangled* qubits [21]. A long standing goal towards scalability of quantum computers is demonstration of fault-tolerant computing, which involves repeated detection and correction of both bit- and phase-flip errors on data qubits [13]. An important milestone toward this goal is the realization of an error-corrected quantum memory in the form of a logical qubit constructed by entangling large 2D arrays of physical qubits woven in a surface-code fabric, such that errors can be detected and corrected through the stabilizer formalism [22]. Cardinal states are specific logical states within this encoding that are chosen as reference states for the stabilizer measurements. In a stabilizer code, the stabilizer generators are operators that commute with each other and include the Pauli operators (X, Y, Z) raised to some power. The cardinal states are the eigenstates of these stabilizer generators, and they are used to define the logical basis for the code [13, 23, 24].

The number of errors that can be detected and corrected per QEC cycle is proportional to increasing *code distance* denoted as *d* in this chapter, which determines the length of the shortest error chain that cannot be detected. Additionally, it corresponds to the length of the shortest logical operator [25]. Therefore, a distance-three surface code can detect *d* - 1 errors and correct (*d* - 1)/2 errors [13]. Recently, innovative schemes incorporating *flag qubits* have been proposed for the implementation of error correction protocols, aiming to minimize the utilization of ancilla qubits in measuring the stabilizer generators of the codes [26–28]. The concept behind flag error correction involves employing additional ancilla qubits that act as flags, signalling when the occurrence of $v \leq t$ faults leads to a data qubit error with a weight greater than v, where $t = \left\lfloor \frac{(d-1)}{2} \right\rfloor$ [27]. The flag information can then be combined with the error syndrome. Whether flag protocols would be suitable for superconducting qubits is yet to be demonstrated, as state measurement and reset operations are slower compared to gate times [29].

Other leading quantum hardware platforms, such as trapped-ion circuits have demonstrated logical single-qubit Clifford gate operations on a logical qubit [30] in a transversal manner, fault-tolerant preparation and stabilizer measurementof a *Bacon-Shor*[2] logical qubit [31], entangling operations on two logical qubits using lattice surgery [3] [33] and fault-tolerant universal gate sets using ancillary flag qubits [34].

[2] Distance-three subsystem error-correcting code implementing the [9,1,3]Bacon-Shor code involving 9 physical qubits for encoding 1 logical qubit.

[3] Groups of physical qubits arranged in a planar lattice that can be split and merged [32]

1.3. THESIS OBJECTIVES: ROLE OF NANOFABRICATION IN SCALABILITY

When it comes to superconducting qubits, maintaining precise control over the operating frequencies of qubits becomes essential to mitigate errors and propel towards fault-tolerance capabilities. Poor qubit frequency targeting is a primary cause of crosstalk induced by microwave drives [13] and can limit gate speeds. It also increases residual ZZ coupling in processors (Chapter 3 and 4) with always-on qubit-qubit coupling [13, 14, 24], making gate fidelity and leakage dependent on the state of spectator qubits [35]. Qubit frequency targeting is therefore, a fundamental challenge which must be solved systematically for the successful realization of fault-tolerant computing. A popular proverb goes as, *A good craftsman does not blame his tools*. A prudent interpretation of this proverb is that a good craftsman identifies the tools' limitations and improvises or constructs better ones. I believe this thesis is built on this interpretation: to understand what fabrication tools and techniques limits us from scaling the physical qubit count, introduces deviations from designed specifications and improving qubit quality.

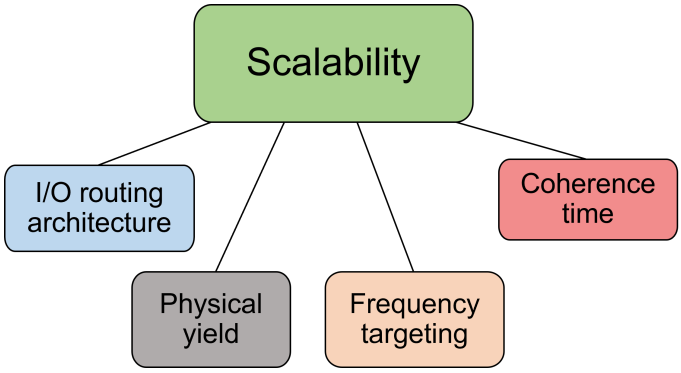


Figure 1.2: The key aspects of research and development in nanofabrication of superconducting qubits in the path towards scalability, which are explored in this work.

The non-linearity of superconducting qubits arise from Josephson junctions (JJ), comprising of two aluminium electrodes sandwiching a thin aluminium oxide (AlO_x) tunnel barrier, the physics of which is elaborated in Chapter 2. This thesis focuses on the superconducting qubit variant known as *transmon*. The second half of Chapter 2 also briefly describes how single and two-qubit gates are constructed using transmon qubits.

Owing to the complexity of the path towards scalability of superconducting qubits, our quantum hardware fabrication efforts are bifurcated into two platforms employing the same quantum plane: the rapid prototyping, scalability-limited planar approach and the scalable vertical input/output (VIO) approach with higher fabrication complexity, described in Chapter 3. This chapter motivates the need for through-silicon vias (TSVs) for vertical routing of signals [36–39] and for suppression of resonance modes arising from the increased size of SQPs and their packaging. I provide a detailed overview of the fabrication processes used for planar and TSV-integrated devices.

Scaling SQPs is a multi-faceted endeavour which must address multiple device performance metrics in tandem such as device yield, bridging the gap in specifications of circuit components between design and fabrication and high coherence times. In chapter 4, I quantify these metrics based on statistics from devices designed, fabricated and characterized by our group. We also introduce a customized suite of image-processing based metrology tools to quantify physical yield of SQP components and automate detection of dimensional or structural deviations from the nominal chip specifications. The main research question of this thesis on factors which affect qubit frequency targeting is elaborated in Section 4.2.

The transition from die-level to wafer-scale fabrication and the associated challenges in qubit frequency targeting forms the basis of Chapter 5. This chapter delves into the interplay between wafer-scale fabrication and the robustness of the shadowing mechanism which differentiates the geometry of Josephson junctions two two types: Dolan-bridge junctions and bridgeless Manhattan-style junctions. A distinct centre-to-edge gradient in conductance is observed in all the wafers fabricated with Manhattan-style junctions. A geometric model based on the centre-to-edge spatial variation of deposited electrode widths of Manhattan-style junctions due to the resist shadowing effect is proposed. The manifestation of this spatial variation is further compared between three variants of planar substrates using a nominal overlap area. Scanning electron microscopy (SEM) images of several junctions are acquired from each planar wafer variant to extract the actual overlap area in order to test the validity of the model. Furthermore, the introduction of TSVs breaks the planarity of the wafer surface, which complicates the reliable fabrication of Josephson junctions. This is the first study of its kind which systematically benchmarks the spread in JJ conductance and consequently qubit frequency with increasing complexity of the substrate plane. Another crucial finding from this work is the role of contact resistance between the Al/AlO_x/Al-base metallization interface. I further verify the role of contact resistance in exacerbating spread of room-temperature (RT) conductance from both die-level and wafer-scale studies.

While understanding the sources of variability in qubit frequency is interesting from a scientific viewpoint, it is equally important to address the problem with out-of-the-box engineering solutions to push forward scaling efforts. In Chapter 6, we explore an 'out-of-fabrication' strategy using localized laser annealing of qubit JJs for selective qubit frequency trimming without intrinsic effect on qubit coherence. I give an overview of the interfacial properties of the Al/AlO_x/Al tunnel barrier which give rise to the formation of two-level system (TLS) defects. The ability to modify the junction conductance by thermally-induced structural rearrangement of the AlO_xtunnel barrier prompted a deeper investigation on understanding the mechanism of *ageing* of junctions, characterized by a time-dependent decrease in tunnel-barrier transparency. We uncover the causes behind JJ ageing by simulating the annealing using the technique of rapid thermal annealing. In this process, we uncover a modality for reproducible JJ *anti-ageing*, characterized by an increase in conductance post-annealing.

2

EVOLUTION OF SUPERCONDUCTING QUBITS

What are the origins of superconducting qubits? In this chapter, we take a deep dive into the physics of Josephson junctions which constitute the heart of a superconducting qubit. The Josephson effect *is a macroscopic quantum mechanical phenomenon, which is exploited to construct a two-level system by careful addition of capacitive, resistive or inductive elements to the Josephson junction circuit. A superconducting artificial atom is realized by isolating the two lowest energy levels* $|0\rangle$ *and* $|1\rangle$ *to execute quantum gate operations. Quantum gates in superconducting circuits can operate on either single qubits or entangle pairs of qubits by applying microwave pulses with variable parameters, including amplitude, pulse shape, duration, timing, and phase. However, the act of measuring and manipulating the qubit state introduces channels for relaxation and dephasing, leading to errors in the information encoded in individual qubits. This necessitates the need for implementing quantum error correction protocols.*

2.1. THE JOSEPHSON EFFECT

The Josephson junction (JJ) is a superconducting tunnel junction, comprising two superconducting islands sandwiching a weak superconductor or a thin insulator that exhibits negligible dissipation and a large non-linear inductance. The non-linear properties of JJs give rise to anharmonicity in the degeneracy of its energy-level spacings when cooled below the critical temperature (T_c) of the superconductor. This is a fundamental requirement for engineering a controllable two-level system (TLS) that constitute a quantum bit, also known as qubit. It is named after Brian Josephson who presented a theory on quantum tunnelling in superconductor-insulator-superconductor junctions [40]. JJs find applications in diverse fields such as superconducting quantum interference device (SQUID)-based magnetometers, transition-edge sensors [41, 42], superconducting tunnel junction-based cryogenic photon detectors [43–45] and rapid single flux quantum (RSFQ) logic [46] to name a few.

The Bardeen-Cooper-Schrieffer theory (BCS) [47] describes superconductivity arising due to the condensation of Cooper pairs. Below the T_c of the superconductor, second-order correlations between electrons of opposite spin are mediated by quanta of lattice distortions called *phonons*. The density of states in a superconductor is described by the wave function

$$\psi(\vec{r},t) = |\psi(\vec{r},t)|e^{i\theta(\vec{r},t)}, \tag{2.1}$$

where $\vec{r}$ is the spatial variable and θ is the global phase of the superconductor. At the critical temperature T_c, the free energy of the normal and superconducting states are equal. The energy gained upon forming the condensate gives rise to an energy gap between the condensate below the Fermi energy and quasiparticles such as electron and hole-like excitations above, which scales with the T_c of the superconductor as, $\Delta(T=0) = 1.76 k_B T_c$. The energy required to break a single Cooper pair is equal to that required for the macroscopic condensate. The existence of this energy gap was first confirmed by quantum tunnelling experiments with superconductors [48], leading to the prediction of the Josephson effect [40]. Under the condition that the insulating tunnel barrier is just a few nanometers thick typically between ≈1-2 nm [49], quantum tunnelling in JJs occurs through two regimes. At zero-bias voltage, Cooper pair tunnelling gives rise to a persistent direct current (dc) by utilizing the degree of freedom in phase. However, on applying a finite voltage at $T \ll T_c$, there is no flow of current until the condition $eV = 2\Delta$ is met, resulting in Cooper pairs breaking down giving rise to quasiparticle current [50, 51].

To understand the implications of the Josephson effect, consider the simple case of two superconductors separated by a thin insulating barrier, with ψ_1 and ψ_2 describing the wave functions of the left and right leads respectively (Fig. 2.1) [52]. The junction is assumed to be a basic lumped element circuit which has uniform cross-sectional distribution of current density and phase difference. The coupled functions are related according to Schrödinger equation as

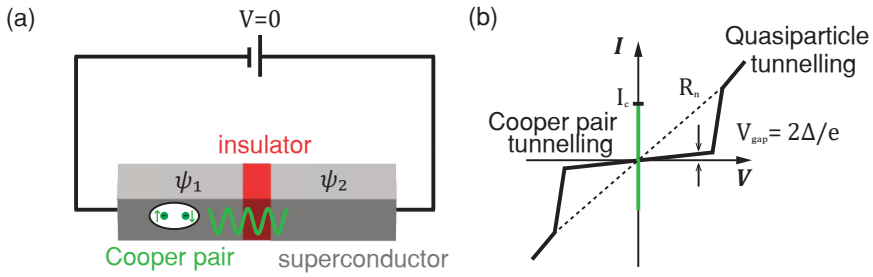


Figure 2.1: (a) Schematic of superconducting leads separated by a thin insulating barrier. (b) Schematic of current-voltage characteristics of a superconductor–insulator–superconductor (SIS) junction. The Cooper pair tunnelling current shown in green is observed at $V = 0$ and the quasiparticle tunnelling current is seen for $|V| > 2\Delta$. The resistance arising from quasiparticle tunnelling is R_{n}.

$$\begin{aligned} i\hbar\frac{\partial\psi_1}{\partial t} &= E_1\psi_1 + K\psi_2 \\ i\hbar\frac{\partial\psi_2}{\partial t} &= E_2\psi_2 + K\psi_1, \end{aligned} \tag{2.2}$$

where K is a constant corresponding to the coupling across the barrier and E_1, E_2 are the lowest energy states on either lead. According to the theory of Ginzburg and Landau based on second-order phase transitions which describes ψ as an order parameter, Eq. 2.1 can be rewritten as

$$\begin{aligned} \psi_1 &= \sqrt{n_1}e^{i\theta_1} \\ \psi_2 &= \sqrt{n_2}e^{i\theta_2}. \end{aligned} \tag{2.3}$$

where n_1, n_2 are the number density of Cooper pairs and θ_1, θ_2 are the phases. The gauge-invariant phase difference of the wave functions due to the weak link, also termed as *Josephson phase* is

$$\delta = \theta_1 - \theta_2 - \frac{2\pi}{\Phi_0}\int_1^2 \vec{A}\cdot d\ell, \tag{2.4}$$

where $\vec{A}$ is the magnetic vector potential and $\Phi_0 = h/2e \approx 2.07 \times 10^{-15}$ Wb is the *superconducting (magnetic) flux quantum*. From the Ginzburg-Landau order parameter, it is understood that the phase difference and number variable are canonically conjugate variables which satisfy the commutation relation $[\delta, n] = i$ and Heisenberg's uncertainty principle $\Delta\delta\Delta n \geq 1$ [53].

By substituting ψ_1 and ψ_2 in Eq. 2.2, we obtain the equation that describes the *dc Josephson effect*

$$\hbar\frac{\partial n_1}{\partial t} = -\hbar\frac{\partial n_2}{\partial t} = 2K\sqrt{n_1 n_2}\sin(\theta_2 - \theta_1), \tag{2.5}$$

$$-\hbar\frac{\partial}{\partial t}(\theta_2 - \theta_1) = U_2 - U_1. \tag{2.6}$$

Since $\frac{\partial n}{\partial t} = I$, Eq. 2.5 can be compactly written as

$$I = I_c \sin\delta(t), \tag{2.7}$$

where $I_c = 2K\sqrt{n_1 n_2}/\hbar$ is the maximum current at zero voltage that can be sustained until superconductivity vanishes, also called the critical current. When a finite voltage V is applied across the leads, the energy levels shift such that $U_2 - U_1 = 2eV$, this gives the second relationship describing the time evolution of phase

$$\begin{aligned}\frac{\partial\delta}{\partial t} &= \frac{2eV(t)}{\hbar}\\ V &= \frac{\Phi_0}{2\pi}\frac{\partial\delta}{\partial t},\end{aligned} \tag{2.8}$$

On applying a DC voltage V_0, the Josephson current oscillates with a frequency f, this phenomenon is termed as the *ac Josephson effect*

$$f = \frac{2eV_0}{h} \tag{2.9}$$

From this relationship we can define the Josephson constant K_J as $2e/h = 483597.9\ \mathrm{GHz/V}$, which was used to define the standard volt V_{90} [54].

To understand the time evolution of the Josephson current [55], we differentiate Eq. 2.7 and replace $\partial\delta/\partial t$ with Eq. 2.8,

$$\frac{\partial I}{\partial t} = I_c\cos\delta\frac{2\pi}{\Phi_0}V. \tag{2.10}$$

The proportional term relating $\partial I/\partial t$ and V describes the *Josephson inductance*,

$$L = \frac{\Phi_0}{2\pi I_c\cos\delta} \tag{2.11}$$

The $1/\cos\delta$ dependence of L indicates the non-linearity of this variable. The inductance at zero bias is independent of the phase difference, $L_0 = \Phi_0/2\pi I_c$. The energy stored in the JJ due to the electrical work done in changing the phase can

be obtained as

$$\begin{aligned} \Delta E &= \int_1^2 IV\ dt \\ &= \int_{\theta_1}^{\theta_2} I_c \sin\delta\ d\left(\Phi_0 \frac{\delta}{2\pi}\right) \\ &= -\frac{\Phi_0 I_c}{2\pi}\cos\delta \\ &= -E_J \cos\delta, \end{aligned} \tag{2.12}$$

where E_J is the *Josephson coupling energy*.

2.1.1. CRITICAL CURRENT

The critical current I_c introduced in Eq. 2.7 is an elementary property of a superconductor which quantifies the maximum current that can be electrically transported with zero resistance. From a thermodynamic standpoint, the critical current is determined by the kinetic energy of the current carried by the superconductor as it tends towards the free energy difference between the superconducting and normal states [56]. Recently, it has been shown that the critical current of superconducting thin films can be described solely from the two characteristic lengths of superconductors namely London penetration depth λ_L (λ_L) and coherence length ξ_0 (ξ_0) [57]. It is a complex parameter influenced by various factors such as elemental purity, junction geometry, temperature, external magnetic field, the amplitudes of the order parameters in the metal and the tunnel barrier properties [58]. A very important relation which describes the temperature dependence of I_c known as the Ambegaokar-Baratoff (AB) formula [59] is widely applicable in the field of superconductivity

$$I_c(T) = \frac{\pi}{2}\frac{\Delta(T)}{eR_n}\tanh\left(\frac{\Delta(T)}{2k_B T}\right), \tag{2.13}$$

where R_n is the *normal-state resistance*. At $T = 0$, this formula reduces to a much simpler form $I_c = \pi\Delta(0)/2eR_n$. The normal-state conductance (G_n) (inverse of resistance $1/R_n$) of an SIS junction depends on the material properties and device geometry such that $G_n \propto \sigma A$, where σ is the conductivity and A is the cross-sectional area of the overlap region. These relations are used to directly estimate the critical current of Josephson junctions from room-temperature resistance measurements. Assuming a constant resistivity, adjusting the overlap area of the JJ electrodes becomes the controlling factor for achieving specific values of I_c. The designed overlap area ($A_{overlap}$) essentially acts as the tuning parameter, allowing for the targeted manipulation of I_c.

2.1.2. SUPERCONDUCTING QUANTUM INTERFERENCE DEVICE

Superconducting quantum interference device (SQUID) is a flux-to-voltage transducer with a single (rf SQUID) or two Josephson junctions (dc SQUID) connected

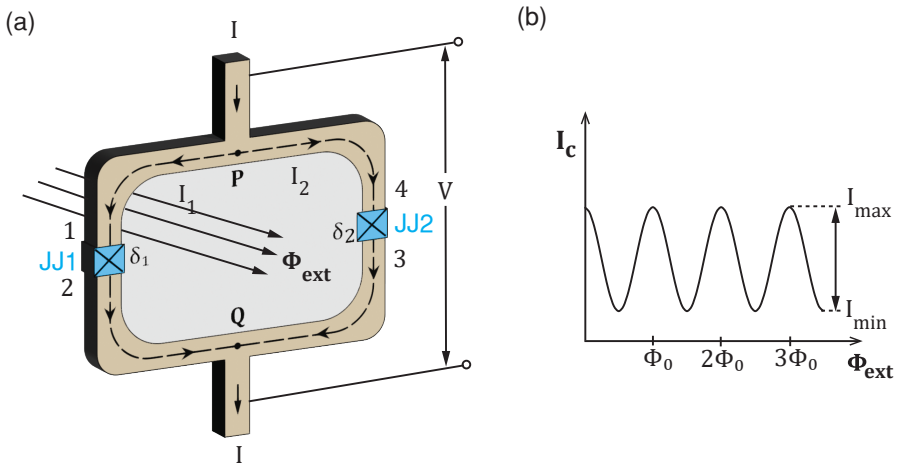


Figure 2.2: (a) Schematic of a dc SQUID with two Josephson junctions connected by a superconducting loop. (b) Critical current (I_c) vs. external magnetic flux (Φ_{ext} of a DC SQUID.

by a superconducting loop. The periodicity of the output voltage from the applied flux corresponds to one flux quantum Φ_0 [50, 60]. SQUIDs find versatile applications, ranging from biomedical imaging techniques such as magnetic resonance imaging to gravitational wave detection [61], as it can act as a sensor for any physical quantity which can be converted to magnetic flux. It is the most sensitive instrument realized so far to measure negligibly small magnetic fields. The reason for this high sensitivity is directly due to the Josephson effect and fluxoid quantization on applying a small external magnetic field.

Developed in 1964 [62], the dc SQUID consists of two SIS junctions placed in a superconducting loop which behaves identical to a single junction, as shown in Fig. 2.2. The principle of operation is based on the dc Josephson effect, where the current splits equally across the two branches. On applying an external flux Φ_{ext}, a screening current, I_s circulates around the loop shielding the interior bulk of the superconductor from electromagnetic fields up to the characteristic penetration depth λ_L. Flux quantization occurs in a superconducting loop or ring in integral multiples of the flux quantum

$$\Phi = k\left(\frac{2\pi\hbar}{2e}\right) = k\Phi_0. \tag{2.14}$$

The total current I through the loop is the sum of currents $I_1 = I/2 + I_s$ and $I_2 = I/2 - I_s$ through nominally identical junctions with phase difference δ_1 and δ_2, as shown in Fig. 2.2(a). It can also be written in terms of δ and I_c

$$I = I_c \sin\delta_1 + I_c \sin\delta_2 = 2I_c \cos\left(\frac{\delta_1 - \delta_2}{2}\right) \sin\left(\frac{\delta_1 + \delta_2}{2}\right). \tag{2.15}$$

We apply the same approach as Eq. 2.4 by taking the differences of the global phase across the tunnel barriers 1-2 and 3-4 and integrating $\nabla\theta$ around the closed path **PQ**

$$\oint_C \nabla\theta \cdot d\ell = 2\pi k = (\theta_2 - \theta_1) + (\theta_3 - \theta_2) + (\theta_4 - \theta_3) + (\theta_1 - \theta_4). \tag{2.16}$$

The second and fourth terms of Eq. 2.16 correspond to difference in current density, which is omitted. The first and third terms of the phase differences can be expressed as

$$\delta_2 - \delta_1 = 2\pi k + \frac{2\pi\Phi}{\Phi_0}. \tag{2.17}$$

Substituting in Eq. 2.15, the total current in the SQUID loop is

$$I = 2I_c \cos\left(\frac{\pi\Phi}{\Phi_0}\right) \sin\left(\delta_1 + \frac{\pi\Phi}{\Phi_0}\right). \tag{2.18}$$

If L is the inductance of the loop, the total flux in the SQUID loop is the sum of the external flux and the flux generated by the circulating currents $\Phi_s = LI_s$

$$\Phi = \Phi_{ext} + \Phi_s \approx n\Phi_0. \tag{2.19}$$

In the general case, the flux produced by the screening current is negligible, the total flux is equal to Φ_{ext}. The current-voltage (I-V) characteristic of the DC-SQUID is shown in Fig. 2.2(b), where $I_c = I_{max}$ for the flux $\Phi_{ext} = n\Phi_0$ and $I_c = I_{min}$ corresponds to $\Phi_{ext} = (n+1/2)\Phi_0$. The maximum current in the SQUID occurs when the derivative of the current with respect to δ_1 vanishes, resulting in periodic variation of the current as a function of Φ_{ext}

$$I_{max} = 2I_c \cos\left(\frac{\pi\Phi_{ext}}{\Phi_0}\right). \tag{2.20}$$

The total inductive energy of the loop is

$$E_{J,eff} = -E_{J,1}\cos\delta_1 - E_{J,2}\cos\delta_2, \tag{2.21}$$

where $E_{J,1}$ and $E_{J,2}$ are the respective Josephson energies of the two junctions. Using trigonometric identities, Eq. 2.21 can be reduced to a single cosine

$$E_{J,eff} = -(E_{J,1} + E_{J,2}) \cos\left(\frac{\Phi_{ext}}{2\Phi_0}\right) \sqrt{1 + d^2 \tan^2\left(\frac{\Phi_{ext}}{2\Phi_0}\right)}, \tag{2.22}$$

where $d = \frac{E_{J,1} - E_{J,2}}{E_{J,1} + E_{J,2}}$ is the junction asymmetry parameter [63]. This additional degree of freedom allows tunability of E_J, a feature heavily exploited in superconducting qubits.

2.2. SUPERCONDUCTING TWO-LEVEL SYSTEM

The Josephson effect and flux quantization are macroscopic quantum phenomena manifested by the coherent sum of microscopic variables governed by the laws of quantum mechanics [64]. Unlike Josephson tunnelling which concerns individual Cooper pairs, macroscopic quantum tunnelling involves all the Cooper pairs in a superconducting condensate that are associated with the universal phase difference δ, thus implying its quantum nature [65]. The experimental validation of energy-level quantization was demonstrated in the 1980s through experiments on current-biased JJs [66]. The next milestone of realizing *superposition* of two quantum states thereby creating a quantum bit or *qubit* was achieved in the late 1990s [67, 68]. By manipulating degrees of freedom in the quantum variables describing superconducting circuits namely the phase difference δ, charge number n or the magnetic flux threading a loop Φ a superconducting two-level system is engineered.

2.2.1. RCSJ MODEL

To describe current-voltage properties of JJs on applying a finite bias voltage, the device is modelled with a shunt capacitance C due to the parallel-plate capacitor configuration of the JJ and a shunt resistance R describing the external circuit, hereby referred to as the resistively and capacitively shunted junction (RCSJ) model [69, 70]. The total capacitance $C = C_J + C_s$ comprises the self-capacitance of the junction (C_J) and the shunt capacitance (C_s). The RCSJ model was widely adopted for analysis of junction dynamics and for computer-aided design of practical JJ circuits due to its simplicity and relatively good agreement between theory and experiments. However the quantitative validity of this model is restricted to a narrow temperature range just below T_c [71].

On applying a bias current I_b, the dynamics of the phase difference δ can be described by the generalized Kirchhoff's law summing the flow of current through all the circuit elements (See Fig. 2.3(a)). Therefore the current through the JJ is the Josephson current I, $I_d = CV$ is the displacement current across the junction capacitance, $I_{qp} = V/R$ is the dissipative quasiparticle current through the shunt resistor and I_N is the noise current due to Johnson noise of the shunt resistor at temperature T with spectral density $S_I(f) = 4k_B T/R$

$$I + I_N(T) = I_c \sin\delta + \frac{V}{R} + C\frac{dV}{dt}. \tag{2.23}$$

On applying Eq. 2.8 here gives a second-order differential equation

$$I + I_N(T) = I_c \sin\delta + \underbrace{\frac{\Phi_0 C}{2\pi}\frac{d^2\delta}{dt^2}}_{\text{particle mass}} + \underbrace{\frac{\Phi_0}{2\pi R}\frac{d\delta}{dt}}_{\text{friction force on particle}}. \tag{2.24}$$

This description is analogous to a particle moving along the coordinate δ in an effective periodic potential U,

$$U(\delta) = -E_J(\cos\delta + X\delta), \tag{2.25}$$

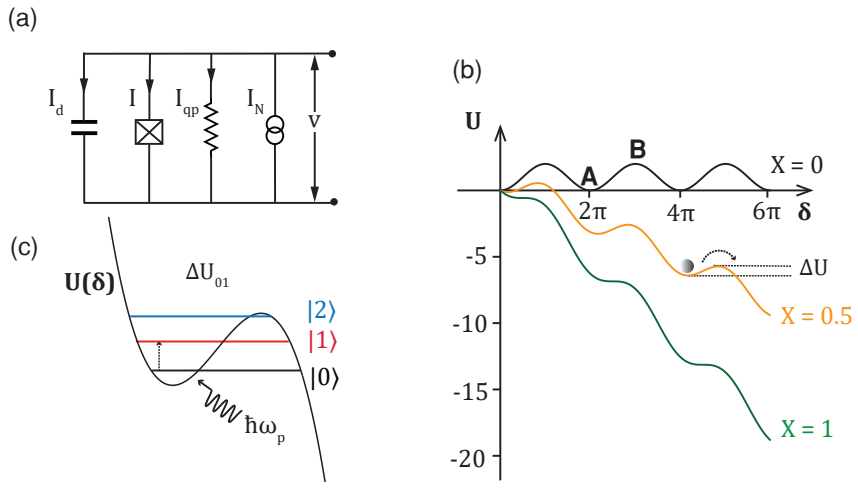


Figure 2.3: (a) Circuit model of Josephson junctions with a shunt capacitance C and resistance R. (b) Potential energy (U) vs phase difference (δ) for current-biased JJ. On increasing X, the potential tilts giving rise to the 'washboard' profile, resulting in the escape of the particle from the bottom of the potential well. The energy difference (ΔU) between **A** and **B** corresponds to the energy barrier. (c) Cubic potential energy landscape of the current-biased JJ. The anharmonicity of the potential results in unequal spacing of the energy levels.

where $X = I_b/I_c$ is the normalized bias current [72]. At the initial state when $V = 0$, the particle is trapped in an energy minimum with phase difference δ_0 shown by point **A** in Fig. 2.3(b). The addition of a dc current causes the junction phase to oscillate within the boundary of the washboard potential well, also called as cosine potential until $X > 1$, ultimately resulting in its *escape* across the energy barrier ΔU at point **B**. The barrier height is approximated by a cubic form $\Delta U(I) = \frac{4\sqrt{2}}{3} E_J (1-X)^{3/2}$ with non-degenerate energy spacings which tends to zero as $I \to I_c$. Depending on the height of ΔU, several quantized energy levels may be accommodated in the potential well with the lowest energy transition $\Delta U_{01} = \hbar\omega_p$. However due to the cubic potential, the higher energy transitions such as ΔU_{n-n+1} $(n \in 0, 1, 2, \ldots)$ are not integer multiples of ω_p [72]. The anharmonicity of the current-biased JJ owing to the dominant effect of the coupling energy E_J is a crucial feature for realizing the *phase qubit* [73].

The oscillation frequency of the particle at the bottom of the well is termed as the *plasma frequency* of the junction which is dependent on the Josephson inductance L and capacitance of the circuit

$$\omega_p = \frac{1}{\sqrt{LC}} \approx \sqrt{\frac{2eI_c}{\hbar C}} \left[1 - X^2\right]^{\frac{1}{4}}. \tag{2.26}$$

The dissipation through the shunt resistance causes damping of the oscillation in the potential well, described by the *quality factor*

$$Q = \omega_{\mathrm{p}} RC \tag{2.27}$$

When the shunt capacitance and/or resistance is small such that $Q \ll 1$, the junction is overdamped and does not exhibit hysteretic behaviour. Conversely, the junction is underdamped when $Q \gg 1$ which shows hysteretic behaviour [58, 72].

2.2.2. CHARGING EFFECTS IN JOSEPHSON JUNCTION

Until the advent of modern microfabrication techniques, early experimental studies on JJs were performed using large junctions with cross-sectional area in the range of 100 μm^2 with capacitances of 1 pF. Studies on small JJs of dimensions 0.01 μm^2 and capacitance 0.5 fF gave insight on Coulomb blockade in single-electron tunnelling (SET), Bloch oscillations and the competition between charging and Josephson effects [74–77]. When a JJ of a very small area is cooled to a temperature $T \ll T_{\mathrm{c}}$, secondary macroscopic quantum effects are observed where both δ and $q = 2en = CV$ act as quantum mechanical operators. The Hamiltonian of the current-biased JJ in this case is

$$H = 4E_{\mathrm{c}} n^2 - E_J \cos\delta - \frac{\Phi_0}{2\pi} I_{\mathrm{b}} \delta, \tag{2.28}$$

where $E_{\mathrm{c}} = 2e^2/2C$ is the *charging energy* of the junction, C is the effective capacitance and I_{b} is the external bias current. On applying an external bias current in the overdamped regime, the particle moves down the washboard potential by means of *phase diffusion* rather than escaping over the energy barrier. This is analogous to Brownian motion of a particle of mass M moving in a potential U [78]. To observe Coulomb blockade, three conditions must be satisfied [58, 77, 79].

- The total capacitance of the circuit must be designed such that $E_{\mathrm{c}} \gg k_{\mathrm{B}} T$ is the dominant energy to minimize thermal fluctuations of the charge number.
- The quasiparticle tunnelling resistance R_{qp} must exceed the inverse of the conductance quantum $G_0^{-1} = h/2(2e^2) = 6.5\ \mathrm{k\Omega}$ to minimize quantum fluctuations of the particle number.
- The effective frequency-dependent impedance of the electromagnetic environment $Z(\omega)$ due to the metal leads must exceed G_0^{-1} at high frequencies of the order $E_{\mathrm{c}}/\hbar$ to suppress the deleterious effects of quantum fluctuations of the environment.

In the small junction limit, the Josephson energy almost scales with the charging energy ($E_{\mathrm{c}} \sim E_J$) where $E_J \leq k_{\mathrm{B}} T$, eliciting both Josephson tunnelling and Coulomb blockade effects [80]. The consequence of operating in the condition $E_J/E_{\mathrm{c}} < 1$ is the increased sensitivity to phase fluctuations from thermal noise due to coupled degrees of freedom with the electromagnetic environment.

2.2.3. COOPER-PAIR BOX

To observe quantum mechanical effects in a JJ circuit under the regime $E_J \ll E_c$, the above mentioned bottlenecks are circumvented by isolating a superconducting island which connects to a high-impedance charge reservoir through a Josephson junction, called a Cooper-pair box (CPB) [81, 82]. The chemical potential of the island is tuned by a gate voltage V_g coupled through a gate capacitance C_g by the tunnelling of Cooper pairs through the JJ, having a capacitance C_J, depicted in Fig. 2.4(a). This part of the circuit determines the background offset charge induced on the island by the electromagnetic environment given by $n_g = C_g V_g/2e$, where n_g is a continuous variable.

The island is in ground state if it comprises only even number of electrons, i.e., all electrons are paired. The island possesses odd number of electrons in the event of quasiparticle excitations with energy above the superconducting gap $\Delta(T)$. If N_{eff} is the effective number of charge states that can be excited, at a crossover temperature $T_{\text{cr}} \approx \Delta(T)/k_B \ln N_{\text{eff}}$ the probability of quasiparticle tunnelling events is low [83]. This leaves the total number of excess Cooper pairs in the island n with a net charge $q = -2en$ as the only discrete variable so it is elevated to a quantum mechanical operator, denoted by $\hat{n}$. The Hamiltonian of the CPB is obtained by modifying Eq. 2.28

$$H_{\text{CPB}} = 4E_c(n - n_g)^2 - E_J \cos\delta, \tag{2.29}$$

where the effective capacitance for E_c is the sum of C_J and C_g. From the commutation relation $[e^{i\delta}, n] = e^{i\delta}$, the relationship between the phase and charge basis is $e^{\pm i\delta}|n\rangle = |n+1\rangle$. Using the identity $\cos\delta = \frac{e^{i\delta}+e^{-i\delta}}{2}$, the CPB Hamiltonian can be rewritten in the charge basis as,

$$H_{\text{CPB}} = \sum_n \left[4E_c(n - n_g)^2 |n\rangle\langle n| - \frac{E_J}{2}(|n+1\rangle\langle n| + |n\rangle\langle n+1|) \right]. \tag{2.30}$$

The charging energies $4E_c(n-n_g)^2$ of two adjacent charge states $n = 0$ and $n = 1$ in the island are degenerate at $n_g = 1/2$, similar to the half-integer flux quantization condition required for flux qubits. At these points, the Josephson coupling to the island produces an avoided crossing shown in Fig. 2.4(b), resulting in the two lowest energy levels of the system separated by energy E_J which can be manipulated as a *charge qubit* [67]. While operating at this so-called *sweet spot*, the CPB qubit is insensitive to offset charge noise [84]. Additionally the E_J can be tuned by replacing the single JJ with a flux-threaded dc SQUID loop [85].

2.2.4. TRANSMON

The transmission-line shunted plasma oscillation qubit, abbreviated as *transmon* evolved from the CPB [87]. The rationale behind the improved design stems from the extreme sensitivity of the CPB energy levels to fluctuations in offset charge outside of the narrow $n_g = m + 1/2, (m \in 1, 2, \ldots)$ degeneracy point, captured by the charge dispersion. In order to decrease the offset charge noise, a large shunt capacitance C_s is coupled to both the superconducting island and the charge reservoir aside from increasing the gate capacitance C_g as shown in Fig. 2.5(a). The

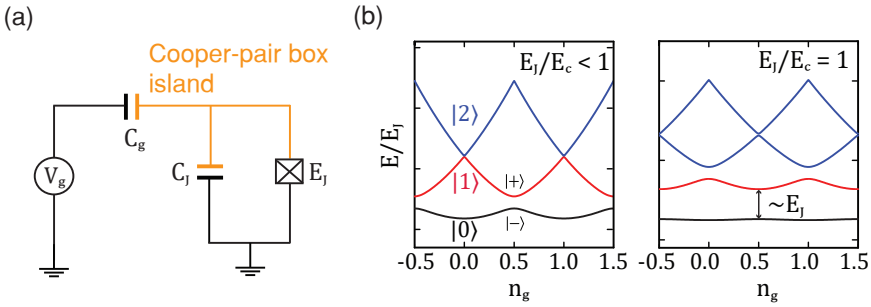


Figure 2.4: (a) Circuit of a single Cooper pair box consisting of the superconducting island, charge reservoir and JJ. The orange line represents the island connected between the gate voltage V_g with a capacitance C_g and the JJ with self-capacitance C_J and Josephson coupling energy E_J. (b) Energy levels of the CPB as a function of the offset charge n_g for n extra Cooper pairs on the island. At $n_g = 1/2$, the weak Josephson coupling lifts the degeneracy of the two lowest energy levels by level separation E_J. Figure (b) reprinted with permission from You and Nori (2005) [86]. Copyright 2023 AIP Publishing.

charge parabolas at half-integer values of n_g flatten out with increasing E_J/E_c ratio as shown in Fig. 2.5(b). This modification suppresses charge noise exponentially, with a caveat that it decreases the anharmonicity following a weak power law. Therefore, the transmon is a CPB in the regime $E_J/E_c \geq 1$ with charge fluctuations on the order of one. The magnitude of anharmonicity is largely determined by the shunt capacitance since C_J and C_g are relatively small, $\alpha = E_{12} - E_{01} \sim -E_c$, where E_{01} and E_{12} are the energy level spacing between the eigenstates. The plasma frequency of the transmon is $\omega_p = \sqrt{8E_J E_c}/\hbar$, therefore the magnitude of the transition frequency corresponding to E_{01} is

$$\hbar\omega_{01} = \sqrt{8E_J E_c} - E_c. \tag{2.31}$$

The transmon qubit's dephasing time, influenced by charge noise, is proportional with E_J/E_c, however this also introduces a limitation. It is inferred by [87] that higher derivatives of eigenenergies related to n_g become infinitesimally small in a transmon circuit. As a result, broader concepts like quantum capacitance lose their usefulness, even though they are effective at the CPB sweet spot [88, 89]. This implies the impossibility of implementing a charge-based qubit readout, swapping it with instead, *dispersive readout* via a cavity.

For practical design and fabrication considerations, the Josephson coupling term in Eq. 2.31 is replaced by the normal-state conductance $G_n\,(1/R_n)$ based on Eq. 2.12 and 2.13

$$\hbar\omega_{01} = \sqrt{8E_c M G_n} - E_c, \tag{2.32}$$

where the term M encompasses the constants and the energy gap $\Delta(T = 0)$. In order to fabricate a transmon resonant at $6.0\,\mathrm{GHz}$ with a designed $E_c = 280\,\mathrm{MHz}$, the

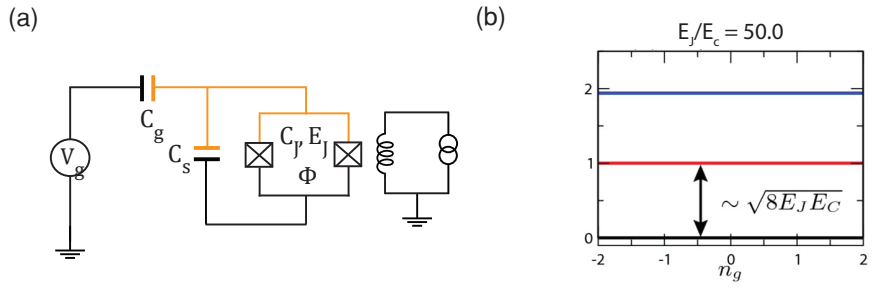


Figure 2.5: (a) Schematic of a tunable transmon circuit with a SQUID loop replacing the single junction. (b) Energy eigenstates of the $m = 0, 1, 2$ versus charge offset n_g in a transmon. Figure (b) reprinted with permission from Koch *et al.* (2007) [87]. Copyright 2023 by the American Physical Society.

unknown variables are calculated from these relations, resulting in $E_J = 17.6$ GHz, $G_n = 123.68\ \mu$S and $M_{\text{init}} = 142.34$ GHz/mS. The relative insensitivity of the transmon to flux and charge noise along with the ability to tune the qubit parameters using dedicated control lines fabricated on a chip makes it an excellent candidate for integrating it with large-scale superconducting circuits. Additionally, tunability of transmon qubits is achieved by applying a magnetic flux Φ threading the SQUID loop. The addition of $1/f$ noise on the magnetic flux causes fluctuations in f_{01} in tunable transmons, which results in dephasing. This can be partially mitigated by incorporating asymmetric JJs [90]. The designed overlap area A_{overlap} of one JJ is at least 1/3rd that of the other, this gives rise to two sweet spot operating points. The remainder of this thesis focuses on the development of transmon-based superconducting quantumprocessors with symmetric JJ pairs.

2.2.5. NOISE IN SUPERCONDUCTING QUBITS

The observation and thereby control of superconducting quantum circuits is possible by isolating it from the external environment by means of a single degree of freedom. The macroscopic nature of the superconducting qubit superposition state eventually decays over time by equilibrating with environmental noise sources arising from thermal and quantum fluctuations. The Caldeira-Legget model firstly addressed the problem of dissipation in quantum mechanical systems as a Brownian particle immersed in a bath of interacting harmonic oscillators [91]. In Josephson junction-based circuits, resistive elements give rise to voltage and current noise with a Johnson-Nyquist power spectrum which linearly couple to the quantum state of interest [92]. The dynamics of qubit decoherence is described by two time constants borrowed from terminology in nuclear magnetic resonance spectroscopy, namely the longitudinal relaxation time T_1 and transverse dephasing time T_2 [93]. The relaxation time T_1 is characterized by loss of energy from $|1\rangle$ state due to thermal activation or spontaneous emission. The dephasing time T_2 is characterized by loss of

phase difference δ between the eigenstates. The qubit relaxation is experimentally measured by exciting the qubit with a drive tone resonant at ω_{01} and observing the temporal decay of the amplitude of *Rabi oscillations* between the ground and excited states of the qubit with a probability P_1. This cyclical behaviour of a two-level system is observed across a multitude of quantum systems subjected to an external driving field [94]. The dephasing time is further differentiated into the intrinsic dephasing of the qubit T_2, measured using the Hahn spin echo technique [95] and the dephasing of the qubit and its detuning T_2^* , measured using Ramsey oscillations [96]. If the spectral density of the noise sources is flat, namely white noise, the dephasing rate $\Gamma_2 = 1/T_2$ can be expressed as a combination of the relaxation rate $\Gamma_1 = 1/T_1$ and pure dephasing rate Γ_ϕ

$$\frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_\phi}. \tag{2.33}$$

Extrinsic noise sources such as coupling the qubit to high-frequency control and readout lines cause fluctuations in the amplitude of the $|0\rangle$ and $|1\rangle$ eigenstates, characterized by the spectral density $S(f)$. The relaxation rate Γ_1 is directly related to the real part of the admittance $ReY\omega_{01}$ shunting the qubit JJ [97], therefore dissipation through the leads can be suppressed by operating in the dispersive regime and engineering high-Q coupling. On the other hand, transverse decoherence is caused by contributions from both T_1 and pure dephasing T_ϕ due to intrinsic noise in I_c, flux and/or charge causing adiabatic variations of ω_{01} [97–99], the origins of which are still not fully understood.

The transmon and a derivative of the flux qubit called *fluxonium* [100] are circuit-based adaptations for reducing the qubit sensitivity to offset charge noise and increasing anharmonicity by operating in $E_J/E_c \gg 1$ regime. In the limit of highly suppressed noise channels from the control lines, the application of amorphous dielectric materials in qubit fabrication and as insulation for device wiring gives rise to a large density of low-energy TLS due to microscopic defects, constituting a dominant source of dissipation and $1/f$ noise [97, 101]. According to the generalized tunnelling model, TLS can be visualized as excitations in symmetric double well potentials, with one type with similar energy distribution to that of a qubit resulting in coherent interaction and the other type with $E \sim k_B T$ energy scale resulting in non-coherent interactions [102]. Local rearrangement of atoms may switch the system between the two minima by tunnelling through an activation barrier. The occurrence of TLS defects in amorphous materials, which host spurious -OH bonds on the dielectric substrate and due to formation of native oxides on the surface of superconducting films significantly affects the intrinsic quality factor of distributed-element superconducting resonators [103, 104].

An important area that is emerging due to recent works on the role of metal-air interfaces in tantalum and niobium is on investigating the optimal film deposition conditions. NbTiN films are also susceptible towards formation of surface oxidation species such as NbO, Nb_2O_5 and TiO_2 [105], the role of these complex oxide species on dielectric losses is unclear as prior works on understanding the loss channels in oxides of Nb-based coplanar waveguide (CPW) resonator have shown

mixed results. One group claims a seven-fold improvement in resonator Q_i by removal of Nb oxides at the M-A interface using HF treatment [106]. In contrast, another group claim that that the M-A interface largely contributes towards power-independent non-TLS losses such as residual resistance, surface losses due to film roughness and/or magnetic flux trapping [104]. Depending on the localization of the TLS defects, fabrication efforts are focussed on minimizing dielectric loss channels between the metal-substrate (M-S), substrate-air (S-A), metal-air (M-A) and metal-metal (M-M) interfaces [107] (See Fig. 2.6). Finally, another important source of qubit decoherence which has gained impetus in the light of high coherence times achieved in superconducting qubits is the generation of non-equilibrium quasiparticles [108] due to impact of high-energy cosmic rays or ionizing radiation [109–111].

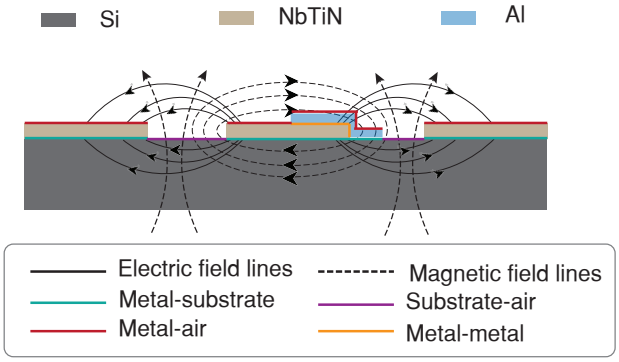


Figure 2.6: Cross-section view of a superconducting coplanar waveguide (CPW) showing the electric and magnetic field distribution. The four material interfaces hosting TLS and non-TLS defects are highlighted throughout the cross-section, the M-S interface comprises the region between the Si substrate and NbTiN metallization layer as well as the Al of JJs, the S-A and M-A interfaces correspond to free surfaces of Si, NbTiN and Al interacting with the environment and the M-M interface is the region where NbTiN and Al layers make galvanic contact, such as the contact pads of JJ electrodes and airbridges.

2.3. BUILDING BLOCKS OF QUANTUM LOGIC

In order to realize useful applications with a quantum computer, it is necessary to engineer interactions with multiple qubits by means of superposition and entanglement [112]. The practical implementation of a scalable quantum computer must fulfil *DiVincenzo's criteria*, which outline the need for well-defined qubits, the ability to initialize the qubit register to a known value, decoherence times longer than gate operation times, quantum gate operations and a means of measuring the qubit output [113]. Superconducting qubit-based processors are frontrunners for scalable

quantum computing due the ease of coupling multiple qubits, the ability to lithographically fabricate devices, incremental improvements in qubit quality and the compatibility with microwave signals. The implementation of multiple high-fidelity single and two-qubit gates forms the basis of quantum logic operations. However qubit operations are susceptible to multiple sources of error such as decoherence, miscalibration of the control and measurement electronics, crosstalk between components and leakage to non-computational subspace [114]. Overcoming these intrinsic limitations require the incorporation of QEC protocols.

2.3.1. SINGLE-QUBIT GATES

Quantum gates are unitary transformations acting on a state vector

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\varphi}\sin\left(\frac{\theta}{2}\right)|1\rangle,$$

where $|0\rangle$ and $|1\rangle$ are quantum analogues of the classical 0 and 1 bits. Unlike classic gates, quantum gates are reversible following principles of energy conservation in a closed quantum system. The superposition state in a single qubit can be represented in an intuitive manner on the surface of a unit sphere, namely *Bloch sphere*. The north and south poles of the Bloch sphere, shown in the blue and red circles shown in Fig. 2.7 correspond to the standard basis vectors $|0\rangle$ and $|1\rangle$ [115]. The pure states are represented at the surface of the sphere whereas mixed states are represented at the interior of the sphere [116]. The spherical coordinate φ is the relative phase with value between $[0, 2\pi]$ and θ is the measurement probability of the basis states with value between $[0, \pi]$ [117]. Single-qubit gates are visualized as rotations of the state vector along the x, y or z plane of the Bloch sphere. The Pauli gates represent rotations of the state vector multiplied by the Pauli spin matrices $\sigma_x = \left(\begin{smallmatrix} 0 & 1 \\ 1 & 0 \end{smallmatrix}\right)$, $\sigma_y = \left(\begin{smallmatrix} 0 & -i \\ i & 0 \end{smallmatrix}\right)$ and $\sigma_z = \left(\begin{smallmatrix} 1 & 0 \\ 0 & -1 \end{smallmatrix}\right)$ [118]. The Pauli X gate is referred to as the bit-flip gate, which flips $|0\rangle$ to $|1\rangle$ and vice versa, equivalent to the classical NOT gate. Pauli Z gate is otherwise referred to as phase-flip gate since it acts only on φ and Pauli Y is a bit and phase flip gate [118]. The Hadamard gate is a fundamental single-qubit gate which transforms the qubit state between the x and z axis away from the poles to create superposition [118].

The XY gates are executed by resonantly driving the qubit by varying the duration, amplitude and phase of the microwave pulse resulting in rotation of the state vector by π radians. The Z gate is implemented either by physically modifying the phase in the Bloch sphere by dynamically detuning the qubit frequency away from the drive field or virtually by applying a phase offset to the microwave pulse in successive X and Y gates [119]. Two well-characterized sources of error in single-qubit gate operations are the unintentional *leakage* of the qubit to higher energy state $|2\rangle$ and beyond due to the weak anharmonicity of transmons and phase errors caused by virtual excitations to $|2\rangle$ giving rise to AC Stark shift between the computational states [120]. Both errors are mitigated by derivative removal by adiabatic gate (DRAG) pulses which apply pulse-shaping and dynamic frequency tuning protocols to the coherent drive [8, 121] is routinely achieved. In the absence of the

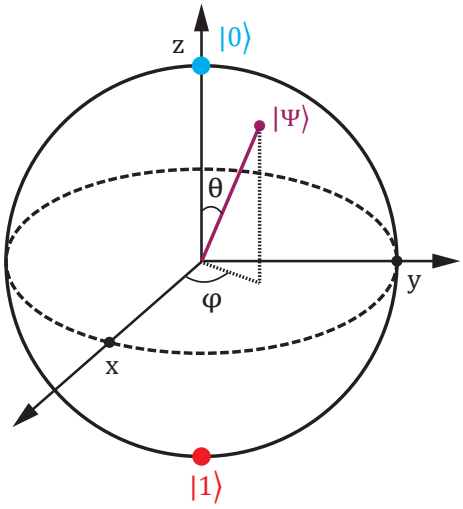


Figure 2.7: Bloch sphere representation of the superposition state of qubits.

frequency tuning component of DRAG pulses, phase errors are alternatively suppressed using virtual Z gates. The duration of single-qubit gates achieved ranges between 13–20 ns with gate fidelity $F_{1q} \geq 0.999$ [122, 123]. In multi-qubit architectures, microwave crosstalk between drive lines and neighbouring qubits operating at similar frequency is a significant problem [124]. Crosstalk between components in a superconducting quantum processor can be mitigated either by optimizing design and hardware choices or by hardware-agnostic software approaches [125].

2.3.2. TWO-QUBIT GATES

The basis of quantum algorithms lies in generating entanglement between multiple qubits through universal gate sets. Two-qubit gates are executed through various schemes which can be broadly categorized as either requiring frequency tunable qubits or by means of all-microwave control using fixed-frequency transmons [126]. The iSWAP and conditional phase (CPHASE) along with its subset, controlled-Z (CZ) gates represent the first category while cross resonance (CR), bSWAP, microwave-activated CPHASE (MAP) and resonator induced phase (RIP) gates belong to the second. To perform a CPHASE gate between a control qubit q_c and target qubit q_t, the qubit frequencies are adjusted such that the combined state of the qubits $|11\rangle$ is moved towards the $|11\rangle \leftrightarrow |02\rangle$ avoided crossing by adiabatic [120, 122, 127] or non-adiabatic [128, 129] flux pulsing. This causes q_t to acquire a state-dependent phase shift of π radians generating an entangled state $|\psi_{ct}\rangle$ [122, 130]. The flux tunable gates allow higher error margin for allocating qubit frequencies during device fabrication at the cost of increased flux noise-induced dephasing when tuning the qubit away from its sweet spot. Cross resonance gates, such as the controlled-not (CNOT) gate, are executed by driving q_c at the frequency of q_t, gener-

ating entanglement by ZX interaction [131, 132]. The advantages of this approach lie in the minimization of measurement overhead and additional noise channels during gate operation. However high-fidelity CR gates have stringent fabrication requirements to consistently allocate qubit frequencies, as interacting qubits with the wrong detuning exhibit frequency collisions [133].

Two-qubit gate fidelity is the most comprehensive measure of qubit quality and overall device yield, calculated from *randomized benchmarking* of long sequences of quantum gate operations [134]. Nearly half of the total error accrued in CPHASE gates is due to decoherence while the remainder is more or less evenly split between coherent sources of error from control electronics and state leakage [122]. In architectures with direct or bus-mediated capacitive coupling of qubits [36], the qubit-qubit coupling J cannot be actively tuned and instead relies on frequency detuning between the qubits or executing dynamical decoupling schemes. CPHASE gates in the dispersive regime are sensitive to coherent and correlated errors in the form of ZZ crosstalk in the limit of a finite detuning between $|11\rangle$ and $|02\rangle$ states [35].

2.3.3. Quantum error correction

Unlike classical computing which employs repetition codes for redundantly storing information to correct errors, quantum computing requires encoding the information in an entangled state of qubits. The most promising approach for implementing QEC protocols in superconducting qubits is using surface codes, a subset of topological codes [135, 136]. It is realized as 2D square lattice of *data* or code qubits and *ancilla* or measurement qubits that constitutes a repeatable unit cell. It encodes a logical qubit in multiple physical qubits determined by the code distance and layout of the unit cell [25]. In superconducting circuits, noise due to decoherence can be approximated as bit flips (X errors), phase flips (Z errors) or both, corresponding to the Pauli operators. Parity measurements, also called stabilizer measurements are performed on ancilla qubits along the X or Z basis to determine the parity of the neighbouring data qubits. A bit-flip (phase-flip) on a data qubit changes the eigenvalue of adjacent Z (X) stabilizers. To extract the *error syndrome*, a given stabilizer is measured by projective measurement of the ancilla qubit, with outcomes ± 1. The corresponding sets of stabilizer operators with mutually-commuting weights of two or four in the surface code are denoted as $\hat{S}^{Xi} = \prod_{j=1}^{2(4)} \hat{X}_j$ and $\hat{S}^{Zi} = \prod_{j=1}^{2(4)} \hat{Z}_j$. These operators are constructed by multiplying two or four Pauli operators ($\hat{X}$ or $\hat{Z}$) associated with the data qubits located at the vertices of a specific data-qubit plaquette. The measurement outcomes $s_{Ai} = \pm 1$ of individual stabilizers $\hat{S}_{Ai}$ are determined by observing changes in the auxiliary qubit state between consecutive cycles. These outcomes signify even or odd parity, respectively [13]. Both bit and phase-flip errors must be simultaneously detected and corrected with minimal perturbation to the entangled state for robust error correction. By increasing the number of physical qubits and therefore code distance, more errors can be corrected per QEC cycle [13]. The surface code distance can be increased simply by copy-pasting the defined unit cell. This strategy is also mirrored in the design and fabrication of the SQP in order to decrease complexity of chip design and fabrication, as shown

by a schematic of a 2D surface code lattice in Fig. 3.3. A crucial measure for assessing the success of QEC implementations is the quantum memory break-even point [137, 138]. This occurs when the lifespan of a logical qubit surpasses that of the most durable individual physical element within the system. Attaining the break-even point signifies that the incorporation of extra physical elements and operations in a QEC process does not result in more deterioration than the safeguarding they provide. Therefore, achieving the break-even point is a vital prerequisite for deploying fault-tolerant gates and error-resilient quantum computing.

3

ANATOMY OF SUPERCONDUCTING QUANTUM PROCESSORS

This chapter gives a comprehensive overview of the design principles of microwave-based coplanar waveguide transmission lines and circuit quantum electrodynamics used to control and readout the qubit state. The design of the quantum hardware and layout is based on a scalable surface code fabric called QuSurf for quantum error correction. To facilitate device scaling as well as rapid prototyping of hardware performance, we fabricate SQPs with through-silicon via and planar interconnects respectively. The second half of the chapter details our material choices, nanofabrication tools and techniques, packaging methods, cryogenic equipment and room-temperature control used to fabricate and characterize both SQP variants.

3.1. CONTROL AND MEASUREMENT OF SUPERCONDUCTING QUBITS

Microwave engineering has largely driven advances in the practical implementation of superconducting qubits for quantum computing applications. The energetic scale of superconductors is determined by the magnitude of the energy gap, for example the superconducting gap of aluminium is $\Delta(T) = 3.4 \times 10^{-4}$ eV [139]. From the Planck-Einstein relation $E = hf$, one can infer the gap frequency $f_c = 2\Delta/h$ ranging from 20 GHz for low-T_c superconductors up to THz range for high-T_c cuprate superconductors, which coincides with the range of microwave radiation [56].

The operational frequency range of transmon qubits typically falls between $4 - -8$ GHz for several key reasons. Firstly, the qubit frequencies must remain below the energy of the superconducting gap of aluminium, the standard material used for JJs whose upper limit is $\sim$ 80 GHz. Additionally, the cost and availability of microwave instrumentation and components become prohibitive in the 15-80 GHz range, leading to a preference for more accessible frequency regimes, particularly those below 12 GHz. Furthermore, to minimize unwanted thermal populations in the qubits, they are operated at temperatures significantly lower than the T_c of the superconductor. For instance, a 4.0-GHz qubit has an energy level approximately ten times that of an ambient qubit environment at 20 mK, a common base temperature for dilution refrigerators. Lastly, qubits with frequencies below 4.0 GHz require noise protection measures to mitigate susceptibility to thermal noise, rendering standard transmons less viable for such applications and necessitating the exploration of alternatives like fluxonium.

The interaction of atoms with discrete photon modes confined in highly reflective cavities describes the study of *cavity quantum electrodynamics*, enabling precise observation of quantum mechanics of coupled systems, engineering of quantum states and and studying quantum decoherence [140]. The same principle is applied by coupling superconducting artificial atoms to one-dimensional (1D) microwave cavities fabricated by means of on-chip simple distributed or lumped-element circuits, termed *circuit quantum electrodynamics* (cQED) [141]. Analogous to a tank circuit, a microwave cavity of length l acts as a bandpass filter due to the formation of standing waves at resonant frequencies, described by the relations $l = n\lambda_n/2$ and $f_n = nv_p/\lambda_n$, where v_p is the phase velocity of the microwave and λ_n is the resonator wavelength at the n^{th} harmonic $(n \in 1, 2, 3, \ldots)$. For a planar transmission line, v_p depends on the inductance $\mathcal{L}$ and capacitance $\mathcal{C}$ per unit length such that $v_p = 1/\sqrt{\mathcal{L}\mathcal{C}}$.

Another important feature of microwave cavities is the extremely low intrinsic loss described by the quality factor Q at resonant frequencies, in the order of 10^6 for underdamped resonators. Microwave interactions with superconducting qubits can be broadly categorized into three functions namely, resonant driving at the qubit transition frequency $\omega_{01}/2\pi$, two-qubit interactions and readout of the qubit state. Classical control of qubits is achieved using coplanar waveguide transmission lines (TL). There are two types of transmission lines, non-resonant elements which interface cQED components with the external electronics such as feedlines, drive and

flux-bias lines and resonant lines which mediate on-chip interaction namely readout resonators, Purcell filters and coupling buses.

3.1.1. COPLANAR WAVEGUIDE RESONATORS

A coplanar waveguide (CPW) is made of a thin metallic film deposited on a dielectric material with two ground electrodes running adjacent and parallel to the strip on the same plane [142]. The transverse electromagnetic (TEM) mode carried by a CPW is distributed between the dielectric substrate and in vacuum, therefore it supports a so-called *quasi-TEM* mode at non-zero frequencies. In the quasi-TEM mode, both electric and magnetic fields have perpendicular and parallel components to the direction of propagation of radiation, however the contribution of the longitudinal component is significantly smaller due to the dielectric inhomogeneity of the medium. Microwave TL resonators are harmonic LC oscillators which can be designed using lumped-element LC circuits, 2D CPW or 3D cavities, operating at a fundamental frequency ranging 5–15 GHz [143]. Unlike qubits, the energy level spacings in a harmonic oscillator are degenerate due to the linear inductance and capacitance of the circuit. CPW resonators are predominantly employed in present-day superconducting circuits due to a number of advantageous features such as the ease of design parameters, small lateral dimensions resulting in large electric field of the zero-point energy $E_{\mathrm{zpf}} \sim 0.2\ \mathrm{V/m}$ resulting in strong coupling to qubits and relatively long lifetimes of microwave photons ranging from 30–100 µs [141, 144]. The first demonstration of cQED between a CPB and a single photon used on-chip CPW resonators to mediate strong coupling [145].

CPW PROPERTIES AND RELATIONS

The CPW resonator is a distributed-element device consisting of a narrow centre conductor of width $w_{\mathrm{r}} \approx 8\text{–}12\ \mu\mathrm{m}$ separated from semi-infinite ground planes on either side by a gap $s_{\mathrm{r}} \approx 3\text{–}6\ \mu\mathrm{m}$ coupled to input-output transmission lines, as shown in Fig. 3.1. In the simple lumped-element approach, the resonator mode frequency ω_{r} and impedance Z_{r} are characterized by inductance L_{r} and capacitance C_{r} such that $\omega_{\mathrm{r}} = 1/\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}$ and $Z_{\mathrm{r}} = \sqrt{L_{\mathrm{r}}/C_{\mathrm{r}}}$. The characteristic impedance of a TL resonator $Z_0 = \sqrt{\mathcal{L}/\mathcal{C}}$. It is usually designed to be 50–150 Ω, limited by the upper bound of the vacuum impedance $Z_{\mathrm{vac}} = \sqrt{\mu_0/\varepsilon_0} = 377\ \Omega$, where μ_0 and ε_0 is the vacuum permeability and permittivity respectively. The CPW Z_0 depends on the relative dielectric constant ε_{r} and the ratio of $w_{\mathrm{r}}/s_{\mathrm{r}}$. The estimated v_{p} and Z_0 from approximating the CPW to be completely immersed in a dielectric medium with effective dielectric constant $\varepsilon_{\mathrm{r}} = (\varepsilon_{\mathrm{r}}+1)/2$ [142] is

$$v_{\mathrm{p}} = \sqrt{\left(\frac{2}{\varepsilon_{\mathrm{r}}+1}\right)}c, \tag{3.1}$$

$$Z_0 = \frac{1}{C_{\mathrm{r}}v_{\mathrm{p}}}. \tag{3.2}$$

The $\mathcal{L}$ of a superconducting resonator is a sum of temperature independent geometric inductance $\mathcal{L}_g$ and temperature dependent *kinetic inductance* $\mathcal{L}_k$ per unit length. Kinetic inductance (L_k), unique to superconductors, is associated with the inertial mass of Cooper pairs, which scales with $\lambda_L^2(T)$. Therefore with decreasing film thickness t, the magnitude of L_k becomes larger than L_g [146].

The geometrical contributions to $\mathcal{L}_g$ and $\mathcal{C}$ are calculated using conformal mapping techniques [144, 146] using the formulae

$$\mathcal{L}_g = \frac{\mu_0}{4}\frac{K(k')}{K(k)}, \tag{3.3}$$

$$\mathcal{C} = 4\varepsilon_0\varepsilon_r\frac{K(k')}{K(k)}, \tag{3.4}$$

where $K(k)$ is the elliptic integral of the first kind defined as

$$K(k) = \int_0^{\pi/2} \frac{d\theta}{1-k\sin^2\theta},$$

where the integral is taken over a quarter of the period of an elliptic function, with k taking the values

$$k = \frac{w_r}{w_r+2s_r}, k' = \sqrt{1-k^2}.$$

The $\mathcal{L}_k$ is related to the geometrical parameters of CPW as

$$\mathcal{L}_k = \mu_0\frac{\lambda_L^2}{tw_r}g(s_r,w_r,t), \tag{3.5}$$

where $g(s_r,w_r,t)$ is a geometrical factor given as

$$g(s_r,w_r,t) = \frac{1}{2k^2K(k)^2}\left\{-\ln\frac{t}{4w_r} - \frac{w_r}{w_r+2s_r}\ln\frac{t}{4(w_r+2s_r)} + \frac{2(w_r+s_r)}{w_r+2s_r}\ln\frac{s_r}{w_r+s_r}\right\}.$$

As per BCS theory, $\lambda_L(0)$ of a superconducting film in the local and dirty limits is related to T_c and normal-state film resistivity ρ ($\Omega-$cm) as

$$\lambda_L(0) = 1.05\times10^{-3}\sqrt{\frac{\rho(T_c)}{T_c}}, \tag{3.6}$$

an approximation which we employ extensively to analytically calculate our superconducting film properties [146]. An overview of the real-world values of the above-mentioned CPW parameters which we use in our SQPs is described in [147]. The L_k expressed in Eq. 3.5 using the London formalism is only valid under the conditions that the operating temperature of the superconductor is well below Tc of the film. In our case, with the effective device temperature of 50 mK when mounted to the mixing chamber of the dilution fridge, the London approach can be justified. Secondly,

this approach also assumes that the operating frequencies of the coplanar waveguides is substantially lower than the superconducting gap expressed $\hbar\omega_r \leq 2\Delta$. Our operating frequencies are in the range of 4–8 GHz, whereas the superconducting gap of NbTiN corresponds to photon energies of about 0.5 THz, again satisfying the criteria for London formalism. The limitation arises when it comes to quasiparticle dynamics, which the London formalism does not take into account. The Mattis-Bardeen formalism, on the other hand incorporates both real and imaginary parts to the complex conductivity expressed as $\sigma(\omega) = \sigma_1(\omega) - i\sigma_2(\omega)$, which takes into account the effect of quasiparticle excitations. The L_k can also be expressed using the Mattis-Bardeen approach as

$$L_k = \frac{1}{\mu_0 \omega \sigma_2(\omega)}.$$

$\lambda/2$ AND $\lambda/4$ RESONATORS

Depending on the termination of the TL resonator, voltage nodes and anti-nodes are formed which determines the length of the resonator as seen by the input impedance Z_{in}. This is extremely useful for designing microwave stubs which are connected at one end to a TL while the other end is either open-ended or short-circuited. From transmission-theory line [148], the voltage reflection coefficient from a distance looking into an impedance termination Z_L is

$$\Gamma(l) = e^{-i2\beta l}\frac{Z_L - Z_0}{Z_L + Z_0},$$

where $\beta = \omega/v_p$ is the phase constant of the TL [144]. For the case of an open-end TL referred to as $\lambda/2$ resonator, $Z_L \to \infty$ while Z_{in} varies periodically with the resonator length as $\lambda/2$ as per standing wave theory. The input impedance and the length of $\lambda/2$ resonator at the fundamental mode f_r is

$$Z_{in}(l) = -iZ_0 \cot(\beta l), \tag{3.7}$$

$$l = \frac{v_p}{2f_r}. \tag{3.8}$$

Similarly, for the short-circuited TL referred to as $\lambda/4$ resonator for which $Z_L = 0$

$$Z_{in}(l) = iZ_0 \tan(\beta l), \tag{3.9}$$

$$l = \frac{v_p}{4f_r}. \tag{3.10}$$

Using a weakly-coupled resonator, with either open-ended or short-circuited TL it is possible to directly extract v_p from experimentally determined parameters using Eqs. 3.8 and 3.10, useful for targeting resonator frequencies as a function of material properties of the superconducting film.

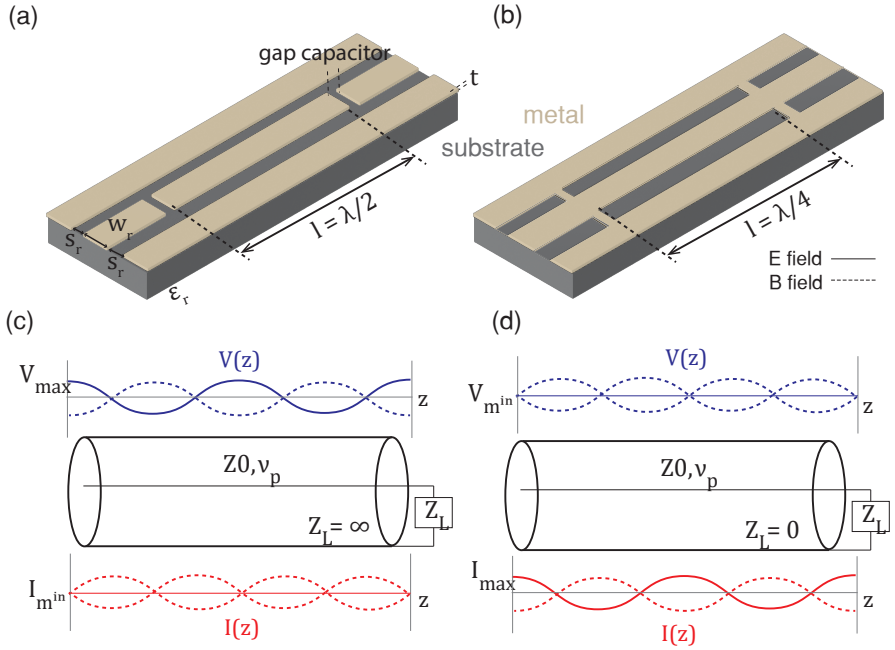


Figure 3.1: The CPW resonator geometry is defined by a centre conductor of width w_r separated by gap s_r from the ground plane, relative permittivity of the substrate ε_r and the thickness of the metal film t, applicable to both schematics. The solid and dashed lines show the distribution of electric and magnetic fields in the CPW resonator. Characteristics of a coplanar waveguide (CPW) transmission line resonator terminated with (a, c) open-ended load impedance designed using a gap capacitor(b, d) short-circuited load impedance.

Q FACTOR

A crucial property of microwave resonators is its internal or intrinsic quality factor Q_i, which is a measure of power loss in the system due to conductive, radiative and dielectric losses. For superconducting CPW resonators operating at the single-photon limit, dielectric losses constitute the dominant loss channel quantified by the *loss tangent* $\tan\delta_{int}$ [149, 150]. For a resonator fabricated using multiple dielectric materials, the internal quality factor is

$$\frac{1}{Q_i} = \sum_{i=1}^{N} p_{ei} \tan\delta_{inti}, \tag{3.11}$$

where p_{ei} is the electric energy filling factor and $\tan\delta_{inti}$ is the loss tangent for the ith dielectric [151]. For an unloaded resonator, the internal quality factor Q_i is related to C_r and resistance R_r of the LCR circuit as per Eq. 2.27. On coupling to input and

output TL also called *feedline*, by a capacitance C_κ, it experiences resistive loading R_L which modifies the effective quality factor Q_L of the parallel circuit. The Norton equivalent expression for the loaded quality factor Q_L is

$$\frac{1}{Q_L} = \frac{1}{Q_i} + \frac{1}{Q_e}, \tag{3.12}$$

where $Q_e = \frac{C_r}{Z_0 \omega_r C_\kappa^2}$ represents the strength of coupling between the resonator and TL [152]. The rate of photon decay κ_r from the resonator through the ports which also corresponds to the *resonator linewidth*, leads to a lowering of Q_L given by the relation $\kappa_r = \omega_r / Q_L$ [141].The loss tangent of intrinsic silicon at cryogenic temperatures below 100 mK is 2.7×10^{-6}, an order of magnitude lower than the value predicted at 1 K. Capacitive coupling of resonators to TL is achieved either using interdigitated finger capacitors as in the case of readout-Purcell filter resonator pairs or via side-coupling in the so-called *hanger* resonator configuration (See Section 6.4). C_κ is adjusted by modifying either the length of the 'elbow coupler' segment of the side-coupled resonator or the gap between the resonator and TL (w_g) [153]. Both approaches allow for coupling multiple resonators to a common feedline. The f_r and Q_i of resonators are characterized by its scattering parameters (S-parameters), mainly from S_{21} transmission spectrum by sweeping the frequency of the input microwave signal using a vector network analyser (VNA). Resonators are in the undercoupled regime when $Q_e \geq Q_i$, resulting in Q_L being dominated by intrinsic losses such as dielectric losses [144, 154]. This regime has important applications in investigating the contributions of material quality and fabrication processes towards TLS and non-TLS losses in resonators [103, 104, 155–157].

3.1.2. CIRCUIT QUANTUM ELECTRODYNAMICS

In most state-of-the-art superconducting quantum circuits, there are at least three control knobs mediated by microwave TL in order to perform single and two-qubit operations. With cQED, establishing strong coupling between the resonator and qubit either inductively or capacitively is a built-in feature of the system due to the large electric dipole moment of the transmon and the large zero-point electric field in CPW resonator. The primary criterion for interfacing qubits with the external control electronics is to balance the signal-to-noise (SNR) ratio of measurements with the fragile coherent state of the qubit. This is achieved by multiple interventions ranging from optimizing the chip design parameters using microwave simulations, heavily attenuating and/or filtering the thermal noise from I/O signals to the chip at cryogenic temperature and performing measurements with custom low-noise, high-speed pulse generation electronics. The generalized Jaynes-Cummings Hamiltonian describes the light-matter interaction in cavity QED which applies similarly to cQED

$$H = \underbrace{\hbar\omega_r \left(\hat{a}^\dagger \hat{a} + \frac{1}{2}\right)}_{\text{resonator}} + \underbrace{\frac{\hbar\omega_{01}}{2}\sigma_z}_{\text{qubit}} + \underbrace{\hbar g(\hat{a}\sigma_+ + \hat{a}^\dagger \sigma_-)}_{\text{resonator-qubit}}, \tag{3.13}$$

where $\hat{a}^\dagger(\hat{a})$ are the creation (annihilation) operators of the resonator photons $n = a^\dagger a$, $\sigma_z = \left(\begin{smallmatrix} 1 & 0 \\ 0 & -1 \end{smallmatrix}\right)$ is the Pauli-Z operator, g is the resonator-qubit coupling strength and σ_+, σ_- are the qubit excitation and de-excitation operators [158]. The interaction described by the Jaynes-Cummings Hamiltonian is a form of *transverse coupling*, specifically involving transitions between different energy levels.

The generic form of two coupled quantum systems take the form $H = H_1 + H_2 + H_{\text{int}}$, where H_{int} is the interaction Hamiltonian coupling the variables of both systems. Capacitive coupling is predominantly employed in most 2D SQP layouts, achieved by placing a capacitor between the voltage nodes of the resonators, qubit-qubit or qubit-resonator pair. The generalized interaction Hamiltonian is $H_{\text{int}} = C_g V_1 V_2$, where C_g is the coupling capacitance and $V_1(V_2)$ is the voltage operator of the corresponding nodes of the quantum systems [126].

3

MICROWAVE DRIVE LINE

Drive lines are used to control the qubit state by applying a persistent microwave tone equal to ω_{01}, required for single-qubit gates. In this regime, coherent exchange of a single photon between the transmon and the drive line at a rate g/π causes *Rabi oscillations* between the $|0\rangle$ and $|1\rangle$ states [145]. Drive lines must be under-coupled to qubits to operate at the single-photon limit to limit the rate of qubit relaxation due to thermal noise. The drive quality factor Q_{d} must be above 10^6 [159]. Furthermore, it must operate in a relatively broad bandwidth of $4-8$ GHz corresponding to the frequency range of transmons and resonators.

FLUX-BIAS LINE

Flux-bias lines (FBL) are short-circuited TL which enable coupling of an external magnetic flux to the dc SQUID loop of transmons for in-situ tuning of the E_J [6]. The qubit frequency is externally controlled by applying a current bias, which mitigates the need for stringent targeting of the qubit frequency during device fabrication. The flux-bias line is crucial for realizing two-qubit conditional-phase (CZ) gates by flux pulsing the qubit frequencies towards resonance [6, 36, 122, 160]. For design considerations, the mutual inductance coupling the transmon to the flux bias line must be weak ($\sim$ pH) in order to minimize qubit frequency fluctuations due to flux noise and the operating bandwidth is from d.c. up to 1 GHz [161].

QUBIT READOUT

Readout resonators (RR) are used to measure the state of the qubit after performing gate operations. The coupling scheme between RR and qubits is in the *dispersive regime* in order to suppress spontaneous relaxation of the qubit state, known as the *Purcell effect*. The resonator and qubit frequencies are detuned such that $\Delta_{\text{r}-01} = |\omega_{\text{r}} - \omega_{01}| \gg g$. The resulting dispersive shift of ω_{r} by a factor $\chi = g^2/\Delta_{\text{r}-01}$ gives the dressed resonator frequency $\tilde{\omega}_{\text{r}}$ depending on whether the qubit is in the ground $(\tilde{\omega}_{\text{r}} = \omega_{\text{r}} - \chi)$ or excited state $\tilde{\omega}_{\text{r}} = (\omega_{\text{r}} + \chi)$. This forms the basis for *quantum non-demolition* (QND) measurementof the qubit state in superconducting qubits [162, 163]. Conversely, the qubit experiences a back action during dispersive readout due

to quantum fluctuations of the photon number n in the resonator, causing AC Stark shift of the qubit frequency $\tilde{\omega_{01}} = \omega_{01} + {g^2}/{\Delta_{r-01}} n\sigma_z$, which can lead to qubit dephasing. The QND-ness of the readout measurement is therefore additionally dependent on the number of photons in the resonator field, such that $n < n_c = \Delta^2_{r-01}/4g^2$ where n_c is the critical photon limit which sets an upper bound for the dispersive regime [141, 163, 164].

Overcoming these limitations require designing RR with large detuning Δ_{r-01}, high coupling quality Q_c and small κ_r, but it is counter-productive to the measurement fidelity due to the attenuation of signal photons [165]. One way to perform high-fidelity readout and reset of the qubit state while preserving strong coupling is by modifying the readout resonator with the addition of a bandpass filter, called Purcell filter (PF) between the RR and feed line [166–168]. The resonator linewidth κ_r is ideally designed to be $\sim 2\chi$, such that it is over-coupled to the feed line. The RR quality factor Q_r is in the order of $\sim 10^4$ [141]. When the detuning between an RR-qubit pair is lower than the designed value, the Purcell decay rate is increased as described by the relation $\Gamma_{\text{Purcell}} = \kappa_r g^2/\Delta^2_{r-01}$ [141]. A similar condition applies to readout and PF resonator pairs, with an effective linewidth

$$\kappa_r = \frac{1}{2}\left(\kappa_p \pm \text{Re}\left\{\sqrt{-16J^2 + (\kappa_p - 2i\Delta_{rp})^2}\right\}\right), \tag{3.14}$$

where κ_p is the PF linewidth, J is the coupling strength and Δ_{rp} is the detuning between the RR and PF [167, 169].

QUBIT-QUBIT COUPLING

A relatively simple and scalable route for transverse coupling between spatially distant qubits is mediated by a high-Q $\lambda/2$ resonator connected at each end by a qubit [6, 141, 170–172]. The interaction of multiple two-level systems is described by the Tavis-Cummings Hamiltonian, which assumes that all the participating two-level systems possess identical ω_{01} and g [173, 174]. When two qubits with transition frequencies $\omega_i/2\pi$ and $\omega_j/2\pi$ are detuned from the cavity bus frequency such that $|\Delta_{i,j-r}| = |\omega_{i,j} - \omega_r| \gg g_{i,j}$, the resonator is dispersively shifted by both qubits. The transverse coupling strength of the qubits arises from virtual exchange of photons with the microwave cavity, described by $J = g_i g_j (1/\Delta_{i-r} + 1/\Delta_{j-r})$ under the condition that the qubits are degenerate. In principle, by tuning the qubit frequencies away from each other such that $|\omega_i - \omega_j| \gg J$, the interaction can be switched off. However, in practical multi-qubit systems a finite dispersive coupling (ζ) persists even when the detuning between the idling frequency of qubits satisfies the aforementioned condition. This is a form of static ZZ crosstalk which causes qubit dephasing if ζ is comparable to the decoherence rate (Γ_2), impacting two-qubit gate fidelity up to 0.4% [35, 175]. For the case of a qubit participating in an adiabatic controlled-phase gate Q_i and a non-interacting spectator qubit Q_j physically coupled to Q_i, ζ_i (ζ_j) induce an energy shift of the $|1\rangle$ ($|2\rangle$) of the gate qubit depending on

the state of the spectator qubit, described by

$$\zeta_1 = 2J^2\left(\frac{1}{\Delta_{ji}+\alpha_j}-\frac{1}{\Delta_{ji}-\alpha_i}\right),$$
$$\zeta_2 = J^2\left(-\frac{1}{\Delta_{ji}}+\frac{2}{\Delta_{ji}-\alpha_i}+\frac{3}{\Delta_{ji}-2\alpha_i}-\frac{4}{\Delta_{ji}-\alpha_i+\alpha_j}\right),$$

where Δ_{ji} is the detuning between Q_i and Q_j and α_i, α_j are the respective qubit anharmonicities. A finite detuning $\delta = (E_{|11\rangle} - E_{|02\rangle})/\hbar$ causes a deviation of the *conditional phase* Φ_c from the ideal value of π, such that $\Phi_c = \pi\left(1+\delta/2\sqrt{2}J\right)$ [35].

3.2. SCALABLE QUANTUM PROCESSORS

The scalability of SQPs at the hardware level is in itself a multi-layered challenge. The imperative lies in ensuring high-fidelity and low-crosstalk operations while simultaneously redesigning the hardware architecture. Solutions for scaling above 1000 physical qubits broadly falls into three layers: integrating 3D features in chip design and fabrication, resolving electromagnetic modes in microwave packaging and engineering cryogenic setups for circumventing limitations imposed by fridge cooling power and differential thermal contraction of various components [176]. This motivates the active development of 3D integration strategies such as flip-chip [177–179] to avoid overcrowding of circuit elements and vertical routing of input and output lines [180–182] to circumvent the scaling limitations associated with lateral wire-bonding.

3.2.1. QUSURF ARCHITECTURE

The fabrication of SQPs described in this thesis is based on the *QuSurf* full-stack architecture [36].[1] Our transmon is embedded with a symmetric SQUID loop connected to a floating[2] star-shaped shunt capacitor pads flanking either end, hence the moniker *Starmon*. The designed $E_J/E_c \sim 40$ and anharmonicity is $\alpha \sim -290$ MHz. Each Starmon is coupled to a dedicated drive line, flux-bias line and readout resonator. The unit cell of this architecture is a plaquette of four data and four ancilla qubits. The modularity of the quantum plane is also extended to the classical control electronics via spatial multiplexing for simplifying measurement overhead. The qubits are allocated into three frequency groups for single-qubit operations. The data qubits are designed to operate at f_{01} $Q_L = 4.9$ GHz and $Q_H = 6.7$ GHz and ancilla qubits (both X and Z-type) at $Q_M = 6.0$ GHz. The typical dimensions of the CPW centre width and gap is $w_r = 12\ \mu$m and $s_r = 4\ \mu$m respectively, with $Z_0 = 50\ \Omega$. The frequency of readout resonators is restricted within a narrow range of 7.0–8.0 GHz and resonator-qubit detuning Δ_{r-01} ranges between $1-2$ GHz due to the Purcell effect limitation between resonator and qubits below 7.0 GHz and the cut-off frequency of Josephson parametric travelling wave amplifiers (JTWPA) beyond 8.0 GHz.

[1] Developed by TU Delft, ETH Zurich, Netherlands Organization for Applied Scientific Research (TNO) and Zurich Instruments for the IARPA LogiQ program.

[2] No galvanic connection to ground

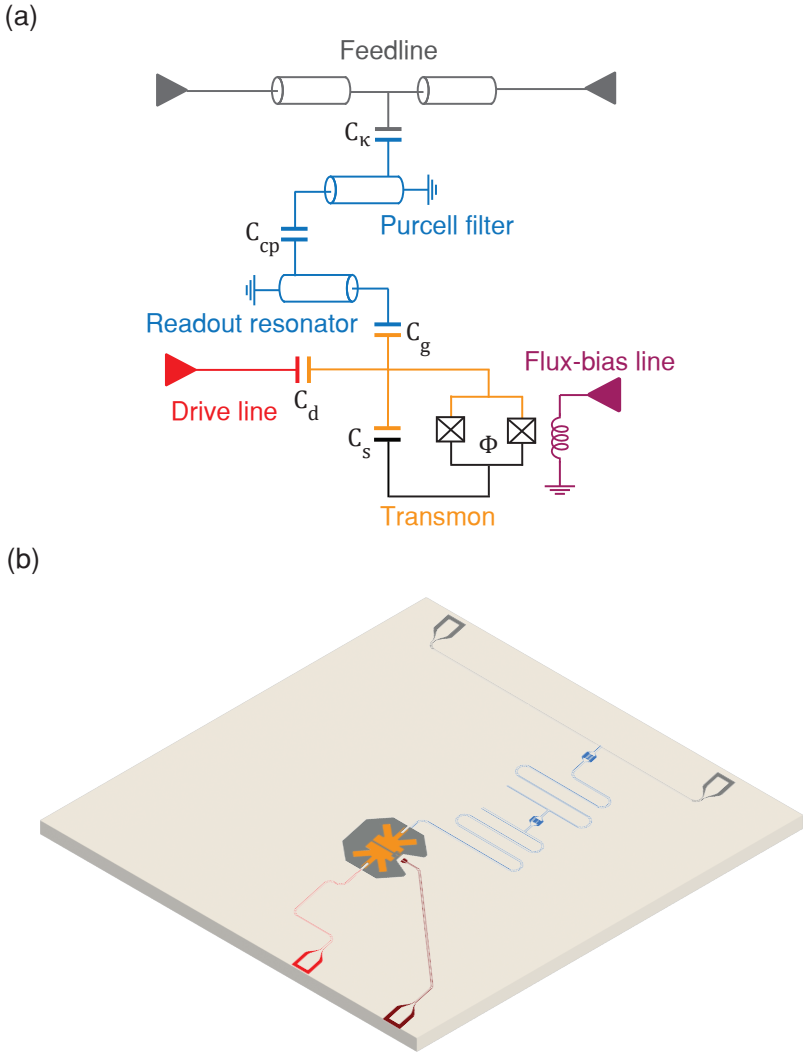


Figure 3.2: (a) Circuit schematic of a transmon qubit coupled to a drive line with capacitance C_{d}, flux-bias line and readout resonator with capacitance C_{g}. The readout resonator is capacitively coupled to a Purcell filter described by the term C_{cp} while the Purcell filter is coupled to the feedline by the term C_{k} (b) Design of a superconducting qubit device with a 'Starmon' qubit corresponding to the circuit.

The two diagonal branches on each capacitor pad of the Starmon is connected to a bus resonator for maximal nearest-neighbour interaction. A sequence of eight detuning sequences between data and ancilla qubits is required for flux-controlled CZ_f

gates performed at frequencies $f_{\mathrm{HM}}^{\mathrm{int}}$ ($\mathrm{Q_H}$-$\mathrm{Q_M}$) and $f_{\mathrm{ML}}^{\mathrm{int}}$ ($\mathrm{Q_M}$-$\mathrm{Q_L}$). Ancilla readout is performed at $f_{\mathrm{M}}^{\mathrm{park}}$ to minimize unwanted interactions with neighbouring qubits. Our surface code architecture allows for tunability of individual qubit parameters and nearest-neighbour coupling compared to the heavy hexagon code with fixed frequency qubits [183]. However, it provides limited control over qubit-qubit interactions compared to tunable coupler architectures [12, 184]. A compact form of the surface code with four data and three ancilla qubits called *Surface-7* served as a workhorse for assessing fabrication and performance metrics. Average two-qubit gate fidelity $F_{2q} = 0.995$ is reported from our Surface-7 devices [123]. A critical milestone of demonstrating repeated QEC has been achieved using a distance-3 surface code with 17 qubits based on this architecture [13]. To achieve the break-even point in quantum memory, the goal is to scale up quantum hardware up to *Surface-49*, a distance-5 circuit with 25 data qubits with state-of-the-art coherence and QEC cycle times [137].

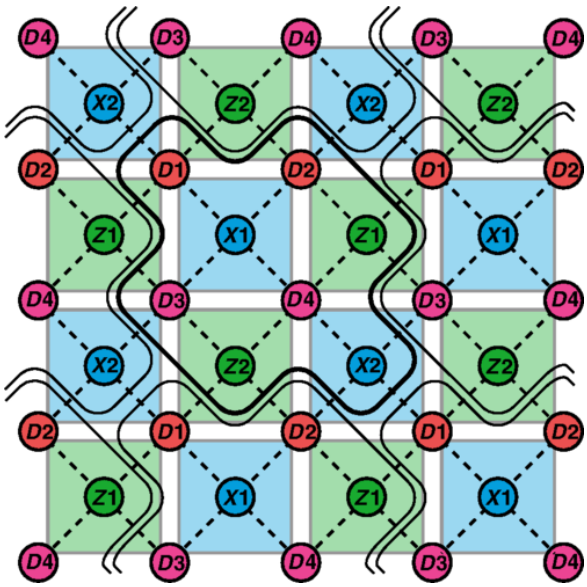


Figure 3.3: Schematic representation of the QuSurf architecture described in Section 3.2.1, with $\mathrm{Q_H}$and $\mathrm{Q_L}$represented by red and pink circles respectively. The ancilla qubits are represented by blue and green circles respectively, centred in green and blue plaquettes for X and Z type stabilizer measurements respectively. Nearest-neighbour qubit interactions are shown by dashed lines. The contour at the centre indicates the surface code unit cell. Reprinted with permission from Versluis *et al.* (2017) [36]. Copyright 2023 by the American Physical Society.

3.2.2. 3D INTERCONNECTS

Owing to the large dimensions of superconducting microwave components (> 200 µm), the chip form factor increases almost linearly on doubling the qubit count. Interconnect crowding is an imminent problem even in 50-qubit devices which are laterally routed by means of wirebonding to traces on a printed circuit board (PCB). Planar and extensible multilayer routing of control signals is appealing for scalability, as demonstrated in RSFQ circuits [185]. However, this method introduces interlayer dielectrics such as SiO_2 between multiple wiring layers, which adversely impacts qubit coherence. In order to facilitate uniform distribution of qubit arrays on the device plane, routing of control lines by exploiting the z direction using 3D interconnects such as superconducting through-silicon vias (TSVs) [36, 38, 39, 186, 187], indium ball grid arrays (BGAs) [178, 188, 189], direct out-of-plane wiring [182, 190], pogo pins [181] and the *quantum socket* [180, 191] have been developed. These approaches can be integrated either monolithically by directly connecting to the qubit chip or modularly to a PCB via an interposer. Flip-chip integration using indium bumps is becoming a preferred technique for alleviating on-chip crowding, as it allows separation of qubit and control/readout plane which are galvanically connected by indium bumps [12, 177–179, 192, 193]. Silicon interposer chips with superconducting TSVs are used to deliver signals vertically between the qubit chip and the lossy multilayer chip or PCB and suppress spurious slotline and substrate modes [37, 194]. Additionally on-chip airbridges and microwave crossovers serve as a quasi-3D wiring interconnects to suppress slotline modes and enable routing of signals between intersecting TL [195]. A general criterion for suppressing spurious modes due to the chip and package is that the package fundamental mode is at least twice that of the maximum qubit f_{01}. The challenges that need to be overcome for large-scale 3D integration are

- Small footprint including grounding features and diffusion barriers.
- Compatibility with all other materials, processes and temperatures used in the fabrication process.
- High and reliable yield in each manufacturing run, particularly when used for signal delivery.
- Possess high critical current > 10 mA for flux-tuning qubits.
- Minimally affect qubit coherence and yield of other fragile and critical components such as JJs and airbridges.
- Microwave and dc characterization must be verifiable for quality control.
- Impedance matching between the interconnect and measurement electronics, usually designed for 50 Ω.
- Resilience to shear stress and differential thermal expansion of multi-stack SQPs ranging from 10 mK to 300 K.

3.2.3. PLANAR VS. VERTICAL I/O FABRICATION

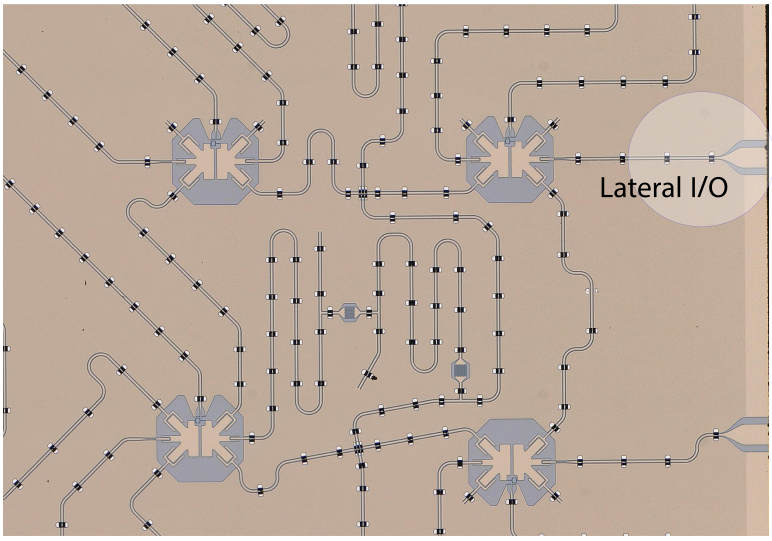
Owing to the complexity of scaling SQPs, our fabrication efforts are split between planar and vertical I/O (VIO) architectures [36]. The fabrication flow is relatively conserved across both device architectures except the steps involving TSV integration in the VIO platform. Another common feature in both platforms is the usage of subminiature push-on (SMP) connectors[3] in the PCB to connect to the fridge wiring.

In the **planar** approach, the chip is connected to the PCB by wirebonding and offers rapid prototyping with a lead time of 1-2 weeks. Device fabrication is carried out at the die-level with typical die sizes of 20×20 mm^2, which reduces writing time using e-beam lithography and allows for better process control. The planar layout allows integration of JJs with any geometry, explained further in Section 3.3.5. While lateral wirebonding hinders equidistant placement of on-chip components, it offers flexibility in chip design when iterating over the target parameters such as f_r, E_c, couplings and other modifications to the circuit elements. In the **VIO** approach, the qubit plane is covered with TiN-coated TSVs conformally deposited using atomic layer deposition (ALD) which serve as interconnects to the PCB for signal delivery. TSVs are envisioned as a necessary step towards monolithic scaling of SQPs beyond 17 physical qubits. The steps involving TSV integration (See Section 3.3.3) are ideally done at wafer scale, as it a time and resource-intensive process. However, further steps post TSV integration are done at die-level by cleaving the dies from the wafer. The complexity of VIO device fabrication is significantly higher due to the incorporation of unfilled TSVs at the beginning of the process flow. As a result, most of the challenges lie in circumventing the non-uniform spinning of resists on the chip especially during JJ fabrication. Further details on JJ types used in this work are discussed in Section 3.3.5. VIO architecture allows uniform distribution of components with shorter connection length, an essential ingredient for scalability. Furthermore, 3D interconnects generally have lower inductance and are amenable to precise impedance matching requirements by design. The chip is attached to a multilayer PCB which can accommodate higher component density by means of thermal compression bonding using electroplated indium. The caveats with this approach are increased fabrication complexity, lead times exceeding one month and additional overhead due to iteration of PCB layout along with chip design.

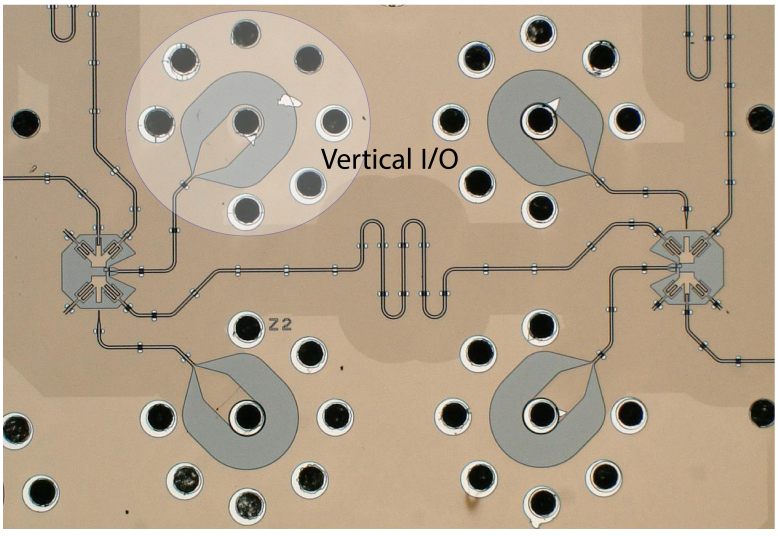
3.3. FABRICATION PROCESS

Superconducting quantum processors resemble monolithic microwave integrated circuits which are fabricated using conventional thin film technology and nanofabrication tools from the semiconductor industry. A generalized fabrication process applicable to planar or 2D SQP is briefly outlined here, followed by a detailed description of the process parameters used in this research. For chip design, our group uses a home-built software package called PyQIP based on Python programming language, developed in collaboration with TNO (See Appendix A.2). The choice of substrate materials is based on the need to maximally suppress dielectric loss

[3] Supplier: Rosenberger non-magnetic connectors, operating range: dc-40 GHz.



(a) Optical image of a planar SQP.



(b) Optical image of a vertical I/O SQP.

Figure 3.4: The two chip architectures.

through the medium. Crystalline materials characterized by low loss tangent at extremely low operating powers such as sapphire or intrinsic silicon serve as ideal substrates. The versatility and well-understood chemistry of silicon makes it an

appealing material for developing low-loss SQPs. The active microwave components such as the transmon capacitor pads and CPW TL are patterned first. The choice of superconducting film for the base metallization layer is somewhat arbitrary, with a preference for elemental and non-toxic superconductors with T_c ranging between $1–10$ K such as aluminium (Al), niobium (Nb) and recently tantalum (Ta). However, compound superconductors made of transition metal nitrides such as niobium nitride (NbN), niobium titanium nitride (NbTiN) and titanium nitride (TiN) are also viable candidates. Film properties such as T_c and kinetic inductance L_k influence the phase velocity v_p of CPW resonators, so careful choice of the base layer is necessary from the purview of scalability. The devices are patterned using photo (UV) or electron-beam lithography depending on the smallest feature size. Except the TSV lithography step, all patterns in our process are written using electron beam (e-beam) lithography with Raith EBPG 5000+ and 5200 systems, which feature 100 kV write mode with 3 apertures sizes at 200, 300 and 400 μm delivering $\geq$5-nm resolution. Conversion of graphic design system II (GDSII) layouts to the native e-beam .gpf format is done using BEAMER lithography software from GenISys GmbH (See Appendix A.3). In order to define the resonator and qubit capacitance, the deposited thin film can be removed by additive or subtractive patterning methods. The integration of Al/AlO_x/Al JJ to the qubits is either done concomitantly during the base layer fabrication or in a separate lithographic step. The JJ electrodes sandwiching a thin AlO_x tunnel barrier can be fabricated either in-situ using *multi-angle evaporation* or as separate deposition steps. Additionally passive components such as microwave crossovers can be integrated for multilayer wiring by means of lithographically-patterned airbridges or on-chip wire bonds. Finally the device is connected to a custom PCB, by means of wirebonding (planar) or indium-based thermocompression bonding (TCB) and packaged for cryogenic measurements.

3.3.1. SUBSTRATE PREPARATION

The substrate used in our planar fabrication process is float-zone (FZ) single-side polished high-resistivity silicon (Ø100 mm, $\rho \geq 10$ kΩ-cm and thickness 525 ± 10 μm) with (100) crystal orientation.[4] The VIO fab process uses double-side polished wafers with other specifications being relatively similar.[5] The choice of (100) orientation is based on the mechanical properties of the wafer that allows for ease and directionality of cleaving. The wafers are first subjected to successive degreasing steps with acetone and isopropanol (IPA) and dried using compressed nitrogen (N_2) gas. Optionally, the wafers can also be subjected to different cleaning processes for stripping organic contaminants. For visible gross contaminants, treating wafers with piranha solution boiled up to 90 °C is recommended. This step can be skipped for pristine wafers fresh out of the supplier's packaging. In case of presence of visible particulate matter on the wafer surface, it is necessary to incorporate megasonically-assisted Standard Clean-1 (SC-1) and Standard Clean-2 (SC-2)

[4] Supplier: Topsil GlobalWafers A/S
[5] Supplier: Siegert Wafer GmbH

wafer-cleaning steps (also known as RCA-1 and RCA-2) [196].

Several manufacturing processes using silicon substrates incorporate the removal of surface oxide contaminants using an aqueous solution of hydrofluoric acid (HF) [197]. The significance of this step prior to metallization with a superconducting film is underscored by the detrimental impact of spurious oxides between the metal-substrate interface (MA) to qubit coherence times. This process should leave behind a chemically inert, hydrogen-terminated surface (Si−H). However, prior studies on Si(111) surface treatments with aqueous HF revealed a locally well-ordered surface that is microscopically rough, characterized by preferential adsorption of trihydrides in Si rest-atom sites and coupled mono- and dihydrides at adatoms [198]. Varying the pH of HF solution drastically alters the uniformity of H-termination in Si(111) and (100) surfaces [199]. The etching of Si(111) using buffered oxide etchant (BOE) also called buffered HF, with a native pH~ 5 is a widely adopted industrial practice since it leaves the surface largely covered with monohydride with a low density of defect sites [200]. More recent studies on Si(100) wafers treated with BOE solutions of pH 5–7 produce surfaces with Si{110} faceted hillocks, whereas pH 7.8–10 solutions produce atomically-smooth surfaces [201].

Our substrate-etching process is done by immersing the wafer in buffered HF 7:1 for 120 s without additional modification to the solution pH followed by subsequent rinsing and drying in deionized (DI) H_2O and N_2 gas [103]. Our post HF-etch process is hexamethyldisilazane (HMDS) vapour priming at 150 °C, which strongly binds to residual oxygen on the Si wafer creating an additional hydrophobic layer. The role of BOE 7:1 dip + HMDS priming in removal of native oxides from the substrate-metal (S-M) interface was verified in the work by Bruno *et al.* by X-ray photoelectron spectroscopy (XPS) analysis of a bare silicon substrate, as shown in Fig. 3.5. The regrowth of SiO_x post-HF etching is markedly slow even on exposure to ambient air conditions, showing a logarithmic behaviour [202]. Whether a few-Å regrown native SiOx contributes significantly to TLS losses through the substrate-air (SA) interface is still a debate within the field. Some research groups [103, 104, 203] including ours employ additional post-processing steps after the initial HF etch in order to improve resonator Q_i. As a best practice, the cleaned wafer is transferred to the loadlock of a thin film deposition system for base layer metallization within 15 min.

3.3.2. BASE LAYER METALLIZATION

Our SQPs are fabricated using NbTiN as the superconducting film deposited using reactive DC magnetron sputtering. It is a type-II superconductor with qualities such as excellent mechanical hardness, high T_c (10–15 K), resistance to oxidation with applications in SIS mixers [204], superconducting nanowire single-photon detectors (SNSPDs) [205], microwave kinetic inductance detectors (MKIDs) [206] and superconducting circuits. The nitridation of NbTi alloy is achieved by injecting a small quantity of N_2 gas during sputtering. Sputtering is a physical vapour deposition (PVD) technique which enables precise eroding of target materials (in this case, the NbTi alloy) onto a substrate due to bombardment by a noble gas plasma such

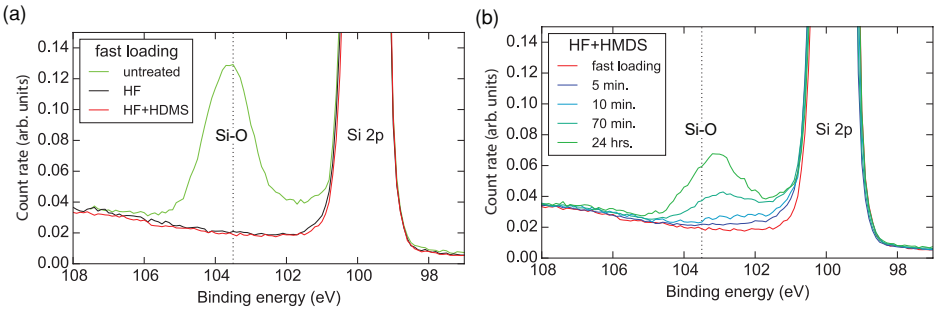


Figure 3.5: (a) The XPS spectrum features a prominent Si−O peak at 103:5±0:3 eV for the untreated Si substrate, which is significantly suppressed for substrates both treated with HF as well as the HF + HMDS combination. (b) The ability of the HF etch and HMDS priming process to retard regrowth of SiO_x is temporary, evidenced by the reappearance of the Si−O peak on the XPS spectrum after exposure to ambient conditions for 24 hours. Reprinted from Bruno *et al.* (2015) [103], with the permission of AIP Publishing.

as argon (Ar). On applying an RF voltage, the magnetron sputter source generates and confines the plasma within the vicinity of the target material placed at the cathode, ejecting atoms into the vacuum environment with sufficient kinetic energy to reach the substrate placed at the anode. The advantages of sputtering are the ability to deposit any material, including alloys regardless of its melting temperature while retaining identical composition in the film as the source material and the flexibility to position the source at any distance or orientation in the chamber. While it yields high-purity films with strong adhesion to the substrate, the thickness uniformity of the deposited film is affected by many process, material and geometric parameters [207, 208].

Metallized wafers used in this work are deposited with NbTiN from two different sputtering systems namely SuperAJA ATC 1800 and Nordiko-2000.[6] There are many differences in the operation parameters between the two sputtering systems, outlined in Table 3.1. The average normal-state resistivity of the NbTiN film is $\rho(T) = 100\ \mu\Omega\text{-cm}$ using both systems, which is just within the limit of highly-disordered superconductors [210]. Details of the extracted film resistivity of wafers used in this work deposited using the SuperAJA system are shown in the Appendix A.1[7]. The measured residual resistance ratio ($\mathrm{RRR}_{300\ \mathrm{K}/20\ \mathrm{K}}$) of NbTiN is between 0.9–1.1.

For our sputtering process using both systems, geometric constraints like substrate-target distance, target size, shape and profile of the erosion track give rise to a radial film profile with the film thickness decreasing from centre to edge. Given a nominal film thickness of $200\ \mathrm{nm}$ on a 100-mm wafer, the relative decrease in thickness is

[6] Further details about film optimization using Nordiko can be found in [208, 209]

[7] Majority of the wafers used in this work are deposited with NbTiN using SuperAJA, with at least three wafers deposited using Nordiko

observed to be $\sim 15\%$ from centre to edge. As shown in [209], $\rho(T)$ and λ_L increase from centre to edge, thereby increasing L_k towards the edge. The radial thickness gradient of NbTiN films from the SuperAJA film is measured from etched features positioned within 70×70 mm perimeter of a 100-mm wafer using atomic force microscopy, as shown in Fig. 3.6 Minimizing contributions from L_k is desirable in order to achieve control over resonator frequency targeting at the wafer scale.

Process parameter	SuperAJA	Nordiko
Target size (mm)	Ø76.2	Ø100
Nb:Ti composition (wt%)	66.9:33.1	81.9:18.1
Max T_c K	14	15
Substrate-target distance (mm)	133	80
Pressure (mTorr)	2.3	6
Ar flow (sccm)	50	100
N_2 flow (sccm)	3.5	5
Power (W)	250	400
Deposition rate (nm/s)	0.35–0.44	1.25–1.31
Film stress @200 nm (MPa)	-135	-418
Substrate rotation	Yes	No

Table 3.1: Process parameter variations between SuperAJA and Nordiko dc reactive magnetron sputter deposition systems. The parameters for Nordiko NbTiN films are referred from [208, 209].

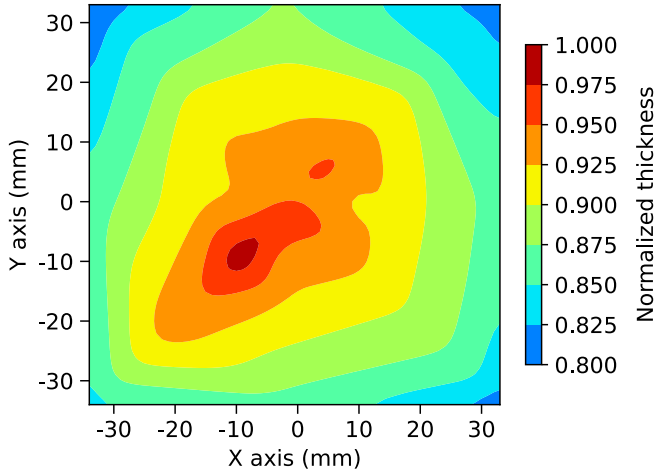


Figure 3.6: Contour plot of max-normalized thickness of NbTiN film deposited using SuperAJA system. Over 60 data points are acquired using atomic force microscopy (AFM) across a 70×70 mm^2 array of etched patterns.

3.3.3. VIO PREFAB

The integration of superconducting TSVs is a wafer-scale front end-of-line (EOL) process following NbTiN deposition which serves the twin purposes of routing sig-

nals between the chip and PCB (signal TSVs) and shunting ground planes in order to push spurious substrate modes above the operating frequency range (grounding TSVs). VIO prefab involves four sub-blocks of fabrication steps as follows,

- TSV pattern transfer using either contact or direct-write UV lithography.
- Deep reactive-ion etching (DRIE) of exposed Si using Bosch process.
- Conformal deposition of TSV sidewalls with TiN by plasma-enhanced atomic layer deposition (PE-ALD)
- Backside patterning of TiN layer to define TSV coax-like structures and under-bump metallization for TCB.

Prior to the DRIE and ALD steps the NbTiN base layer is protected with a 600-nm layer of sputtered SiO_2. The photolithography step is is done by covering both the wafer front and backside using negative working Dupont MX5050^{TM} dry roll-on resist. To ensure adhesion of the dry resist, the wafer surface is pretreated with vapour-phase HMDS and heated between 85–100 °C on a hotplate while performing a pressurized lamination. After UV exposure, the transparent polyester coversheet on MX5050 dry resist is removed and developed in aqueous-alkaline K_2CO_3 based solution, such as mr-D4000/75 developer from Microresist Technology GmBH. All the etching steps including DRIE Bosch process are performed using PlasmaPro 100 Estrelas system from Oxford Instruments, which also features cryogenic-DRIE capabilities. The parameters optimized to ensure smooth vertical sidewalls are the wafer chuck temperature (varied between 10 and −10 °C), RF power, and the duration of the SF_6/C_4F_8 plasma(s). After etching through the wafer, the photoresist is stripped using Baker PRS-3000™ at $90°C$ multiple times to completely remove residues. A ~ 100 nm layer of ALD TiN is deposited along the TSV sidewalls using tetrakis(dimethylamino)titanium (TDMAT) precursor at 270 °C with a deposition rate of 0.80 Å/cycle using a Veeco Fiji G2 system. The wafers are placed in the ALD chamber with the frontside placed downward on a 150-mm carrier wafer.

TSV-based coax-like structures allow for facile realization of impedance matching in RF/microwave-based circuits [211]. Our TSV coax structure comprises of a centre signal TSV surrounded by seven grounding TSVs with a total footprint of $1.2\ \text{mm}^2$, compatible with UT-047 coax cables [212]. The characteristic impedance of our TSV coax is related to the via dimension and distance between the signal and grounding vias by the equation

$$Z_0 = 138 \log_{10}\left(\frac{D_e}{D_v} \times \frac{1}{\sqrt{\varepsilon_r}}\right),$$

where $D_v = 160\ \mu\text{m}$ is the via diameter and $D_e = 1$ mm is distance between the edge of the signal via and the inner edge of the grounding vias as shown in Fig. 3.7(b). It is defined after the JJ deposition step by backside patterning using dry-resist UV lithography and standard reactive-ion etching (RIE) using SF_6/O_2 mixture to isolate the signal TSVs from the ALD TiN ground (See 3.3.4 for details). The etched region is cleaned with a gentle in-situ Ar ion milling prior to deposition of a Ti/Pt/Au

$(10/40/300\ \mathrm{nm})$ stack using a Temescal FC-2000 ebeam evaporator which serves as the underbump metallization layer for TCB with electroplated indium on the PCB [213].

The film properties are characterized by I-V measurements of two TSVs in series connected in a 4-wire configuration, performed in a 3He fridge with base temperature at 300 mK. By varying ALD recipe parameters such as the process temperature, number of deposition cycles and adjustments to the plasma purge time, we obtain the best values for $I_c = 11.5\ \mathrm{mA}$, $T_c = 3.7\ \mathrm{K}$ at the wafer surface and $1.4\ \mathrm{K}$ in the vias. In one device (VIO W33b G, refer to Fig. 4.8(a)), we demonstrate flux-biasing of qubits by applying currents $\geq 2\ \mathrm{mA}$ at 20 mK without causing any increase in the fridge temperature.

The measured Q_i is $\sim 5 \times 10^5$ from all-resonator devices subjected to the VIO fabrication processes. Among the six VIO Surface-7 characterized, two devices show full yield of qubits, with an average $T_1 = 7\ \mu\mathrm{s}$ measured from 31/42 qubits. This is lower compared to planar devices, suggesting that our VIO fabrication process is not yet optimized for high-coherence qubits. A persistent issue encountered during the TSV photolithography and DRIE steps are the lack of reproducibility in complete etch-through of the wafer and control of the sidewall roughness due to scalloping [214]. Another crucial aspect in optimization of the TiN film deposited along via sidewalls is to ensure conformality, prevent buildup of contaminants and particle deposition and establish ohmic contact with the NbTiN base layer across the chip. This is particularly relevant for routing DC current as any localized defects and film discontinuities can lead to the TSVs going normal and cause heating of the fridge. Additionally, connectorizing the fully fabricated VIO device to the PCB is prone to failures due to non-uniform contact between the backplane and the electroplated In (See Section 3.3.7). Due to the significantly higher complexity of VIO fabrication combined with suboptimal device yield and performance, further efforts in this direction are on hold.

3.3.4. BASE LAYER PATTERNING

The second (third) block in our planar (VIO) fabrication process comprises base layer patterning, in which the qubit capacitor pads, transmission lines, launchers, couplers, pattern markers and the *holey ground*[8] are written on the metallized substrates using electron-beam lithography using a dose range $300\text{–}385\ \mu\mathrm{Ccm}^{-2}$ with beam step size (BSS) $20\ \mathrm{nm}$. The e-beam resist of choice is 9% poly(α-methylstyrene-*co*-α-chloromethacrylate), abbreviated as CSAR 62[9] dispensed in anisole as the carrier solvent. It is a positive tone resist developed as an alternative to ZEP520A characterized by properties such as high processing speed, $\geq$ 6-nm resolution, high contrast and plasma etch stability [215, 216]. Post exposure, the sample is developed in pentyl acetate (also known as amyl acetate) at 20 °C for 60 s, followed by a 5 s dip in xylene which acts as a development stopper, rinsed for 60 s rinse in

[8] Small etched squares of dimensions $500 \times 500\ \mathrm{nm}^2$ fabricated throughout the chip plane which act as vortex traps for stray magnetic fields.

[9] Commercially sold as AR-P 6200 series of resists.

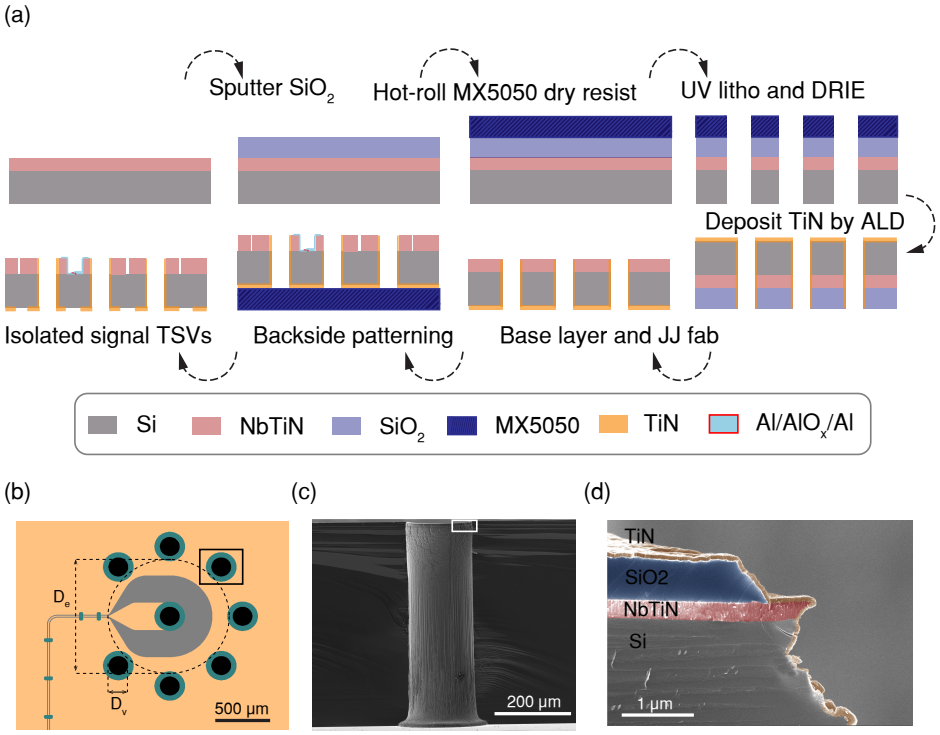


Figure 3.7: (a) Schematic of process flow for TSV integration post NbTiN metallization. (b) Coloured computer-aided design (CAD) layout of a TSV coax structure consisting of a centre signal via surrounded by grounding TSVs. The centre via is isolated by backside patterning to selectively remove TiN. (c) SEM micrograph of a single TSV obtained by cleaving a sample. (d) Zoom-in of the white box showing a false-coloured image of the TSV sidewalls metallized with ALD TiN, making galvanic contact with NbTiN base layer still protected with the sacrificial SiO_2 mask (Image courtesy: Dr. Alessandro Bruno).

IPA and finally dried using compressed N_2. The metal layer is patterned by physical/chemical removal using mask-based dry and wet etching techniques. For VIO devices, the alignment of the base layer with respect to the pre-fabricated TSVs is crucial, which must have a placement accuracy of $< 50\ \mu m$. This is done by means of a manual search for DRIE markers at the e-beam system and then overlaying the base layer pattern.

Dry etching is performed using RIE. RIE uses RF-generated plasma to etch NbTiN with higher selectivity than the protective resist or mask layer by fine-tuning the plasma conditions to create a highly directional etch profile. RIE is well suited to simultaneously etch a variety of materials, both dielectrics such as Si, SiO_2, Si_3N_4

as well as refractory metals such as Nb, Ta, Mo, Re and W. A typical configuration of the RIE system consists of a low-pressure (< 10^{-4} mbar) planar parallel plate reactor, where the sample to be etched is placed on the cathode capacitively coupled to the RF generator. The higher mobility of electrons compared to the ionized gas molecules on applying an oscillating electric field results in a build-up of a self-bias voltage at the target electrode, causing the ions to acquire a partial positive charge to physically bombard the sample. Reactive plasma species generated from halogenated gases such as CF_4, Cl_2, BCl_3, SF_6 to name a few diffuse into the surface of the sample and form volatile by-products, thereby chemically removing material. Oxygen is added to fluorinated gases in order to increase ion concentration and suppress formation of non-volatile fluoropolymers which tend to deposit along the process chamber walls. Etching at low pressures increases the mean free path of the ions, which results in anisotropic, i.e. directional etch profile, minimizes device contamination and microloading[10] [217]. The systems used for RIE are Z-400 by Leybold Heraeus GmbH (F3) and Etchlab 200 by Sentech Instruments (F1), with nearly similar process parameters. The open regions are etched using a mixture of SF_6 and O_2 at low process pressure ranging between $5–10\ \mu\text{bar}$ and RF power of $50\ \text{W}$ in both systems. The etch duration is determined by end-point detection using laser interferometry integrated with the system.

Depending on the device generation, the etching is completed either fully by means of RIE or split between dry and wet etching where RIE is terminated prematurely until about $\sim$10 nm of NbTiN is left on the open regions (See Fig. 3.8(a)). The remnant metal is then removed with a higher selectivity by wet etching using RCA-1 solution heated to 35 °C, with an etch rate of $\sim$2 nm/min. It is worth mentioning that a finite quantity of Si, ranging from $2–3\ \text{nm}$ is also removed by RCA-1 solution [218]. An inorganic masking layer is necessary for this process as RCA-1 solution attacks the CSAR resist. We investigated three different inorganic masks namely 100-nm thick sputtered SiO_2/Si_3N_4 and spin-on dielectrics such as 100-nm thick hydrogen silsesquioxane (HSQ) solution in methyl isobutyl ketone (MIBK) is deposited on the sample prior to spinning e-beam resist. Devices coated with the inorganic mask are subjected to HMDS vapour priming to facilitate good adhesion of resist.

After completion of dry etching and prior to wet etch, the resist layer is removed by a hot solvent strip at 80 °C, usually with N-methylpyrrolidone (NMP). The wet etch is terminated upon optical and 2-probe electrical inspection of the sample, confirming complete removal of NbTiN from the open regions. From multiple trial and errors, we observe that either HSQ or Si_3N_4 inorganic mask is more resilient to SC-1 solution, whereas sputtered SiO_2 is observed to succumb to cavitation defects. It is to be noted that wet etching is isotropic leading to undercutting and therefore roughening of the NbTiN sidewalls shown in Fig. 3.8(d,e). The duration of wet etch must be tightly controlled and monitored, ideally not exceeding 6 min. The etch profile becomes non-uniform when scaling from die level to a 100-mm wafer due to the centre to edge thickness variation of the sputtered NbTiN film. Given an active patterning

[10] Etch-rate dependence on feature size, also known as RIE lag effect or aspect ratio dependent etching (ARDE)

region of 70×70 mm^2, dies fabricated in the outer 35×35 mm^2 region of the wafer are prone to increased sidewall roughening compared to dies located towards the wafer centre inspite of using either HSQ or Si_3N_4 masks.

3.3.5. JOSEPHSON JUNCTION FABRICATION

Josephson junctions constitute the smallest feature of SQPs, with dimension ranging from $80 - 250$ nm in transmon qubits, necessitating e-beam lithography for pattern transfer. Current state-of-art fabrication techniques for JJs still involve employing multi-angle shadow evaporation with in-situ thermal oxidation to form the a self-limiting AlO_x tunnel barrier, either with or without a suspended resist bridge acting as a shadow mask. By varying the deposition angle (θ) as well as the azimuth (ϕ), it is possible to fabricate several useful alterations of the resist pattern without needing to break vacuum; an essential requirement for fabricating high-quality tunnel junctions. Our approach for fabricating the Al/AlO_x/Al sandwich involves first depositing a thin Al bottom electrode of nominal width W_b and thickness T_b at a tilt θ and azimuth ϕ_1. Then a thin AlO_x tunnel barrier is grown over the bottom electrode, usually by means of RT thermal oxidation. The thickness and uniformity of the thermally-grown tunnel barrier can be controlled by multiple knobs in the oxidation process such as O_2 partial pressure, ambient temperature, duration of oxidation [219, 220] and static vs. dynamic oxidation [221, 222] to name a few. Then a top electrode of nominal width and thickness W_t and T_t at a tilt θ and azimuth ϕ_2. Both electrodes are designed to make galvanic contact with the NbTiN base layer by means of openings in the SQUID loop called *junction bays*. Other variations of shadow evaporation tilt and azimuth angles can be found in [223–225].

The Niemeyer-Dolan technique [226], well-established for fabricating sub-μm JJs relies on creating overlapping electrodes using a suspended resist bridge offset from the substrate which acts as a shadowing mechanism, also referred to as 'i-type' junctions in this work, shown in Fig. 3.9(b). Inherent median deviation of ($\pm$ 1%) in the thickness of spun resist on planar wafers translates to a spread in the effective JJ overlap area (A'_overlap) and consequently the target qubit frequency (f_q) of about 80 MHz at the die level [227]. Bridgeless junctions work on the principle of $W = H \tan\theta$, where W is the pattern width and H is the thickness of the imaging resist (top resist) and θ is the deposition angle relative to normal incidence, rendering the JJ A'_overlap less sensitive to resist height variations (See Chapter 5 for further details).

Foreseeing that true scalability of our quantum hardware integrated with TSVs cannot be achieved with *Dolan-bridge junctions*, we investigate JJ deposition geometries specifically tailored to mitigate the effect of resist height variations on reproducibility of effective electrode dimensions ($W'_\mathrm{b}, W'_\mathrm{t}$). The first variant called bridgeless 'o-type' junctions are patterned with electrodes running parallel to each other as shown in Fig. 3.9(d), whereas the second variant, *Manhattan-style* or 'x-type' junctions are patterned with electrodes running orthogonally as in Fig. 3.9(e) [228]. The o-type JJ variant was retired mid-way, due to its sensitivity to the effective height of the etched Si-N sidewall and lack of control over the separation distance between the NbTiN bays.

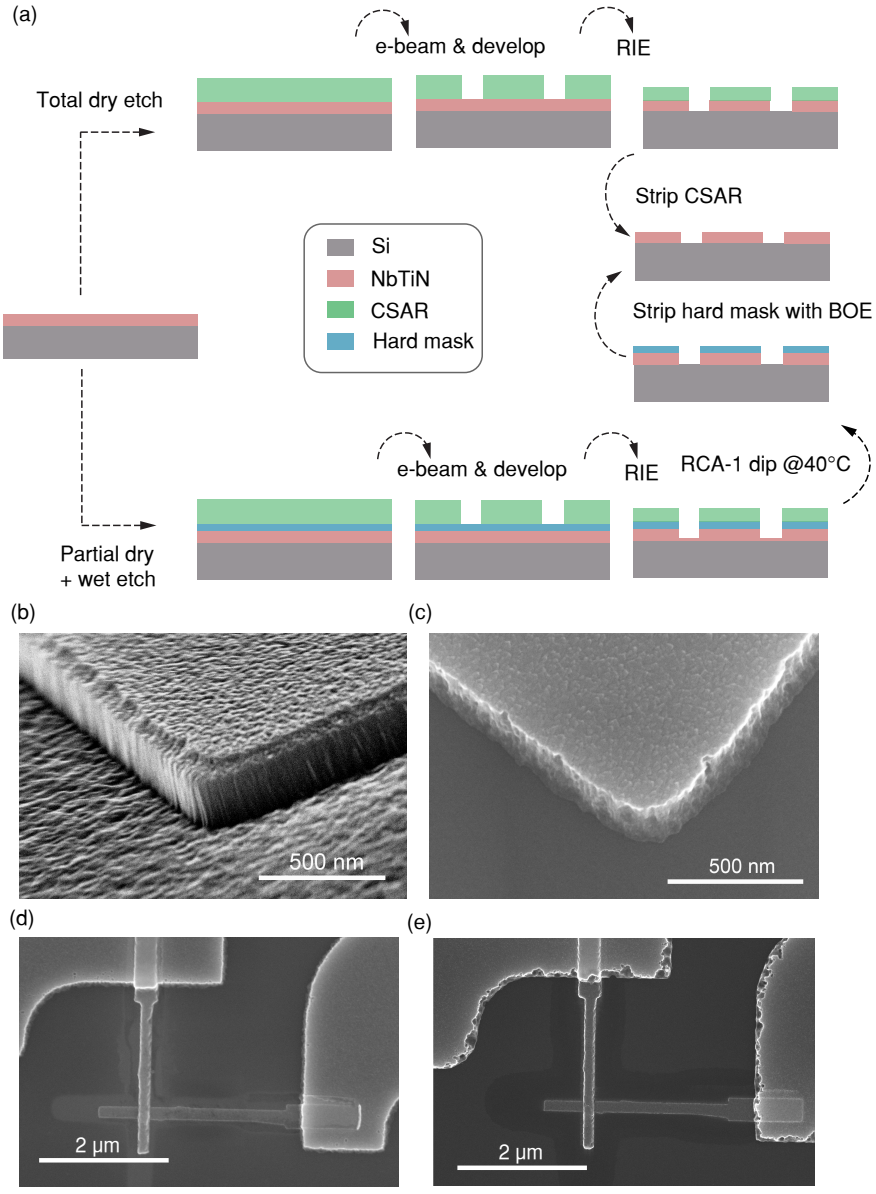


Figure 3.8: (a) Schematic of base layer patterning differentiating complete dry etch and partial dry + wet etching of NbTiN. SEM images of NbTiN film sidewall profile and Si roughness after (b) complete dry etching (c) partial dry + wet etching. Comparison of NbTiN sidewall profile using sputtered SiO_2 hard mask after wet etch duration of (d) 5 minutes (e) > 10 minutes.

For the fabrication of JJs, a bilayer resist stack comprising a bottom high dose sensitivity support layer and a top low dose sensitivity imaging layer is employed to facilitate high-resolution pattern transfer and clean lift-off of Al. Compared to the conventional bilayer resist stack employing methyl methacrylate (MMA)[11] monomer (support layer) and poly(methylmethacrylate) (PMMA) (imaging layer) we use a bilayer with poly(dimethylglutarimide) (PMGI) [12] as the support layer with PMMA imaging layer due to the large undercut formed using PMGI [229] and excellent tolerance of the stack when treated with HF solutions. All the JJ geometries are fabricated using a bilayer PMGI/PMMA resist stack as described in Ref. [227]. Each resist layer is baked for 5 min at $175°C$. The JJs are patterned by e-beam lithography using a dose 1850 μCcm^{-2} and BSS 4 nm. We do not implement proximity effect correction for JJs, this results in a proximity-induced broadening of the patterns. The PMMA layer is first developed by a 1:3 MIBK and IPA solution for 60 s, rinsed with additional IPA and dried with N_2 gas. The wafer is rinsed in deionized (DI) H_2O for 20 s both before and after development of the PMGI layer with Microposit MF™-321 developer. The JJ patterns are subjected to O_2 plasma descumming by RIE at 10 μbar and 20 W for 50 s followed by oxide strip using 7:1 BOE solution for 30 s. The wafers are then immediately transferred to the process chamber of the Al evaporator ensuing pumping in the load lock to 2×10^{-7} mbar. The oxidation process parameters are preserved across the junction styles, using static oxidation with 6N purity O_2 at oxidation pressure 1.3 mbar and oxidation time 11 min to minimize the number of process variables. Following the deposition of the top electrode, terminal *capping oxidation* is performed using the same oxidation conditions unless otherwise specified, adding a passivation layer around the junctions. The differences in the deposition parameters among the three JJ variants is summarized in Table 3.2.

During the first half of this research, JJ deposition is conducted using a manual home-built multi-angle evaporator called the Al-MBE. It is a modified molecular-beam epitaxy (MBE) system retrofitted with valves separating the upper process chamber and the lower crucible chamber in order to isolate the latter during RT thermal oxidation. The sample holder can be customized to mount a sample with maximum dimensions of 70×70 mm. The samples are mounted into the load lock at a 90° angle with a loading arm The sample xyz stages are motorized to adjust sample height, azimuthal rotation and deposition tilt which are controlled by a LabVIEW GUI. However, the opening and closing of the valves connecting the process chamber to either the load lock or the lower chamber are all operated manually. This introduces an element of human error particularly during the in-situ oxidation step. During the later half of this work, the induction of a Plassys MEB 550S automated multi-angle evaporation system bolstered our efforts towards wafer-scale fabrication of JJs.

[11] Methyl ester of methacrylic acid (MAA)
[12] Also known as Lift-off resists (LOR), PMGI-based resists are originally formulated for UV lithography.

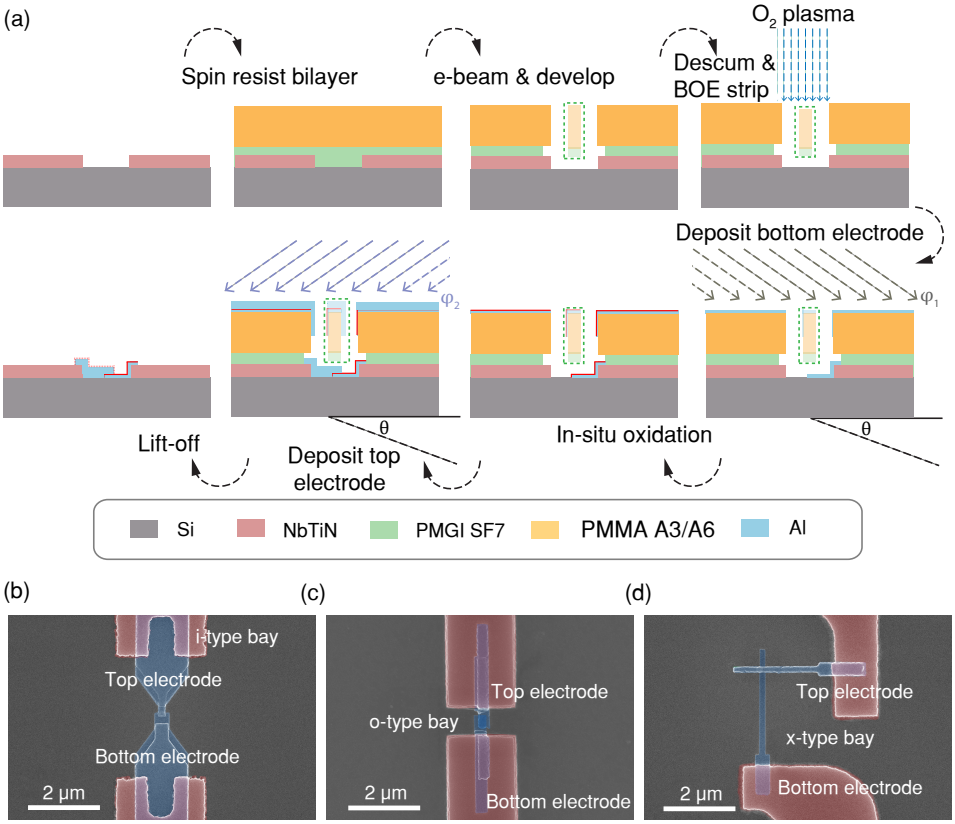


Figure 3.9: (a) Schematic of fabrication steps common to all JJ variants. The suspended resist bridge highlighted by the green box is relevant for Dolan-bridge (i-type) junctions. The capping oxidation layer is indicated by the dotted red lines in the final lifted-off JJ schematic. False-coloured SEM micrographs of (b) Dolan-bridge (i-type) JJ (c) bridgeless o-type JJ (d) bridgeless Manhattan-style (x-type) JJ.

3.3.6. AIRBRIDGES & CROSSOVERS

A notable disadvantage of CPW geometry is the excitation of coupled slotline modes due to discontinuities and/or asymmetry in the TL, such as shunt stubs and right-angle bends respectively. Airbridges equalize the voltage on the two ground planes of CPW lines at the discontinuity, which must be placed periodically along the length of the TL as the ratio of the slotline-like mode to the CPW mode increases as a function of distance from an initially placed airbridge [230]. Superconducting microwave circuits commonly employ arched Type A airbridges, which consists of a free standing metal strip connecting the ground planes on either side of the CPW

Parameter/JJ type	i-type	o-type	x-type
Shadow construct	Resist bridge	Bridgeless	Bridgeless
PMGI thickness (nm)	400	400	200
PMMA thickness (nm)	A3, 200	A3, 200	A6, 600
Deposition angles (°)	$\theta = 35$ $\phi_1 = 0$ $\phi_2 = 180$	$\theta = 15$ $\phi_1 = 0$ $\phi_2 = 180$	$\theta = 35$ $\phi_1 = 0$ $\phi_2 = 90$
Electrode thickness (nm)	$T_b = 30$, $T_t = 60$	$T_b = 50$ $T_t = 110$	$T_b = 35$ $T_t = 75$
Sweep electrode	W_t	W_t & W_b	W_b

Table 3.2: Comparison of deposition parameters for the three JJ variants

centre conductor [231]. It can be described by an equivalent T network with two half-series inductances and a shunt capacitance. The airbridge inductance per unit length is related as $L_{AB} = K_p L_0$ for an airbridge of length l_{AB}, where K_p is a correction factor. With a typical length of 30–100 μm, the shunt inductance of airbridges is significantly lower than on-chip wirebonds [195]. The shunt capacitance per unit length exerts the dominant effect as airbridges act like a parallel-plate capacitor between the centre conductor and ground, related as $C_{AB} = \frac{\varepsilon_0 w_r}{h_{AB}}$ where h_{AB} is the height clearance of the airbridge [232]. The CPW Z_0 is modified in Eq. 3.1 with the addition of C_{AB} to C_r. The typical airbridge dimensions of our device layout are $h_{AB} = 6\ \mu$m and $l_{AB} = 70\ \mu$m which gives $C_{AB} = 22$ pF/m. Increasing the density of airbridges along a resonator therefore decreases the resonator Q_i and lowers the $f_{r,meas}$, ideally design considerations must take into account to limit the coverage of resonators by airbridges.

Crossovers are microwave striplines that allow two isolated CPW lines to cross each other, increasing flexibility of chip design while lowering its footprint. It is an indispensable feature for device scaling in the planar architecture due to the limited degrees of freedom in lateral routing of signal lines, evident from the large number of crossovers implemented in planar Surface-17 layout (See Table 4.1. This brings into focus another design and material constraint due to the inherent fragility of these structures. We have observed an instance of heating of the fridge due to defective crossovers bridging FBL on a Surface-17 device Inari v1 (See Fig. **??**). Subsequent design generations assign a priority for TL which can be routed using crossovers, with feedlines and drive lines having maximum priority followed by bus resonator and lastly FBL.

The airbridge and crossover fabrication is the final lithographic step in both planar and VIO architectures because of the mechanical fragility of the structures. The arched 3-D profile of airbridges is achieved by means of resist reflow of a 6-μm thick layer of PMGI SF15 after the first e-beam step to open galvanic contact pads on the CPW ground planes across the centre conductor. The airbridge connecting the pads is patterned in the second e-beam step employing a PMMA bilayer, followed by a BOE dip to partially remove oxides from the NbTiN surface and deposition of 400 nm Al using an e-beam evaporator. After Al deposition, the die is coated with

a protective layer of photoresist and cleaved into two separate chips using DAD 3220 dicing saw from DISCO Corporation. This is followed by careful lift-off of the residual Al in multiple baths of NMP at 90 °C and rinsing with IPA while the devices are placed facing up. The fabrication of airbridges post JJ deposition causes a drift in the JJ G due to the resist baking and reflow steps. This is an important source of deviations in qubit frequency targeting, which is studied in more detail in Chapter 6.

3.3.7. Device packaging

Superconducting qubits require customized packaging solutions which simultaneously provide shielding of the SQP from external decoherence channels, connectivity to the fridge cabling, suppression of spurious frequency modes and adequate thermalization to the mixing chamber stage of the fridge. The packaging approach varies between the planar and VIO device architectures, described separately below. Certain attributes regarding the microwave package are common to both approaches, which typically consist of a gold-plated copper thermalization base and lid and a single or multi-layer PCB soldered with non-magnetic SMP connectors for connecting to coaxial fridge cables with SubMiniature version A (SMA) connectors as shown in Fig. 3.11(b). Outside the cold finger, a colour code is used to associate each SMA cable to the correct CPW line in the chip package. Careful design of the microwave package is necessary to avoid introducing spurious TEM modes. Spurious modes can originate either from the package and/or the device substrate [233]. Box modes can arise from metallized cavities formed above and below the chip due to the lid and the PCB cavity respectively where the frequency decreases with increasing dimensions [176]. Chip-based modes arise due to the higher ε_r of silicon. With increasing device form factor, the lowest frequency of the first eigenmode interferes with the operating range [233]. Other design and material considerations for packaging of SQPs are ensuring impedance matching at 50 Ω between the signal trace and surrounding ground of the PCB and the SMP connector in order to minimize signal reflections within the package and avoiding magnetic materials as it can adversely interfere with the flux-tunable qubits respectively.

The package is affixed to a cold finger made of gold-plated copper mounted at the mixing chamber stage[13]. Semi-rigid stainless steel fridge cables are inserted at the base of the cold finger and connected to the package. The cold finger is then enclosed by multiple layers of shielding cans namely two Cryophy nickel-iron soft alloy magnetic shields to protect the devices from external magnetic fields, a superconducting Al shield and an innermost infra-red shield made of gold-plated copper with the inner walls coated with radiation-absorbing substances such as a mixture of Stycast 2850FT epoxy resin and silicon carbide granules. Microwave drive lines require nearly ∼60 dB of attenuation incorporating both off-the-shelf cryogenic attenuators and home-made Eccosorb filters[14]. Flux-bias lines are filtered using low-

[13] coldest part of the dilution fridge

[14] See Laird, “Eccosorb®MF datasheet,” https://www.laird.com/sites/default/files/2021-07/RFP-DS-MF061721.pdf

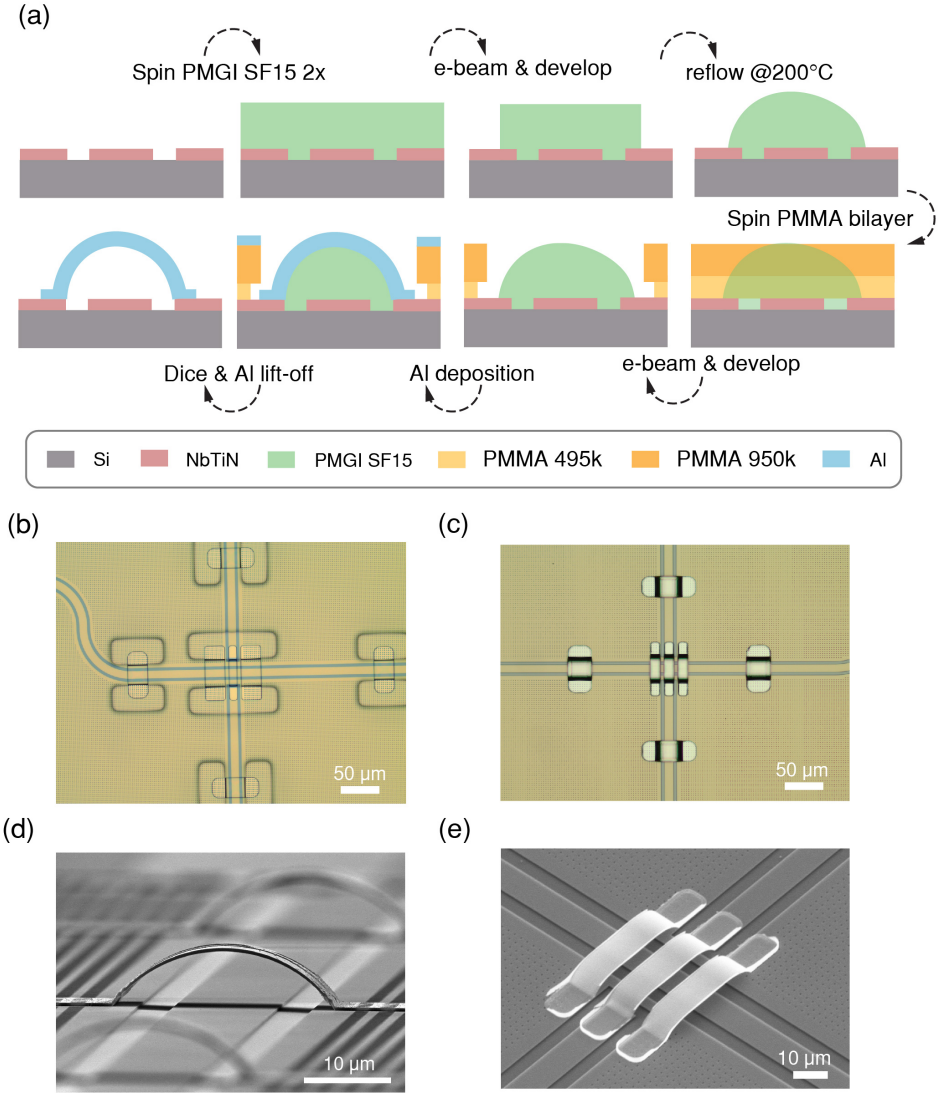


Figure 3.10: (a) Schematic of airbridge fabrication steps. (b) Optical image of the developed airbridge pattern on PMMA/MMA stack overlapping the contact pads exposed on the bottom PMGI layer after e-beam lithography. (c) Optical image of airbridge patterns after deposition of $400\ \mathrm{nm}$ Al, dicing and lift-off. (d) Tilted SEM micrograph of multiple airbridges fabricated across a CPW transmission line. (e) SEM micrograph of a crossover. SEM image credit: Dr. Alessandro Bruno

pass filters with a cut off frequency of 2 GHz. Additionally, the readin attenuation and readout chain amplification need to be addressed. Microwave amplification

performed by JTWPAs is crucial to improve the SNR of readout signals by at least 20 dB and can be integrated into the readout chain for improved signal detection, conferring advantages such as low added noise, high gain and wide bandwidth [234]. Finally, high electron mobility transistors (HEMT) are included in the 4 K stage of the readout signal amplification chain to minimize the addition of thermal noise to the weak qubit signal. A schematic of the fridge wiring for characterization of Surface-7 devices is added to the Appendix A, Fig. A.13. The dilution fridges used for characterizing the devices described in this work are built by Bluefors and Leiden Cryogenics. Details on improvements in shielding and cabling used in dilution fridges for superconducting qubits are described in [161, 235–238].

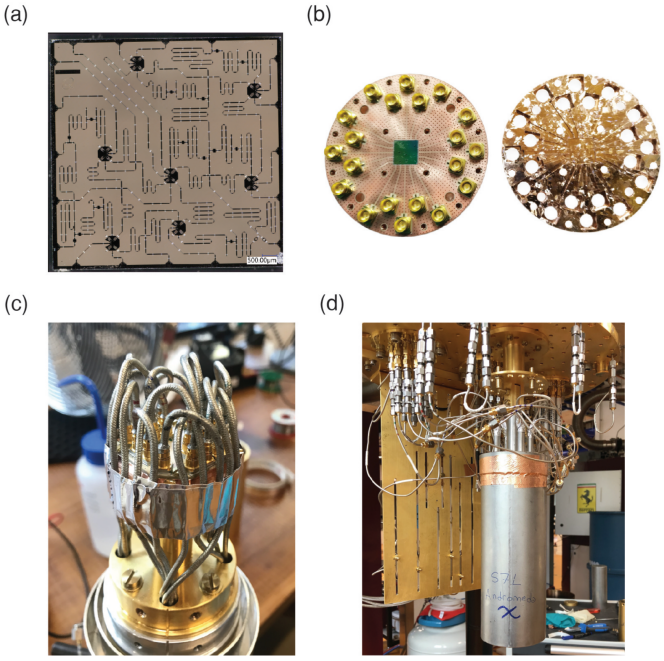


Figure 3.11: Packaging and cryogenic assembly of a planar Surface-7 v1 device. (a,b) The fabricated chip is wirebonded to a PCB and mounted on a copper base plate and covered by the shim, constituting the chip package. (c) The chip package is then mounted onto a cold finger and fridge cables are connected. (d) After connecting the cables, the cold finger is enclosed by shielding cans. Image credit: DiCarlo lab

PLANAR DEVICES

The PCB for mounting planar devices consists of a single high-conductivity copper layer with copper striplines embedded in the dielectric layer, made of Arlon AR1000 [15], shown in Fig. 3.11(a, b). The striplines are electromagnetically isolated from each other by rows of stitching vias drilled through the PCB substrate. The signal traces terminate at a copper-lined cavity positioned at the centre of the PCB with a depth of 1 mm which houses the chip. In case of Surface-7 and 17 devices, the cavity is cut out prior to wirebonding in order to eliminate spurious box modes from the package. Prior to soldering SMP connectors to a planar PCB using lead-

[15] Now part of Rogers Corporation.

free solder paste[16], it is subjected to pre-cleaning steps described in Appendix A. In contrast to the advantages of the lateral I/O method described in Section 3.2.3, there are two notable shortcomings to this approach. The first problem arises from impedance mismatch between the device ports and the PCB traces due to variable length of the Al wirebonds. This can lead to higher insertion loss and deteriorate signal integrity, which affects gate and readout fidelities [233]. The inductance of a 1 mm wire bond made of 25 µm pure Al wire roughly corresponds to 1 nH, which has a reactance X of 50 Ω at 10 GHz. Therefore, it is necessary to keep the wirebond length as short as possible [239]. All the planar SQPs presented in this work are wirebonded manually. This introduces variability in the length of signal wirebonds when trying to fit at least 2 bonds within the 120 µm wide CPW launcher. A high density of grounding wirebonds are added between launchpads to reduce crosstalk between signal wirebonds. Secondly, the PCB dimension nearly doubles in form factor with increasing qubit count, shown in Table 4.1. This is an inherent limitation on the scalability of monolithic planar SQPs, which again motivates the need for VIO architecture.

3

VIO DEVICES

VIO devices are mounted on a 6-layer PCB stackup with alternating layers of copper and FR-4 dielectric substrate. To establish ohmic contact between the VIO device backplane and the PCB (See Subsection 3.3.3) by TCB, a thick layer of indium is deposited on the PCB by means of electroplating using commercially procured indium sulfamate solution. The PCB is mounted at the cathode using a custom-made plating jig which exposes only the region where the die is attached while a strip of In with 99.99% purity is mounted at the anode, a schematic of this setup is shown in Fig. 3.12. The nominal electroplating parameters for depositing $\sim 34\ \mu\mathrm{m}$ of In are a deposition rate of 0.27 µm/min and a current density of 20 A/ft^2 with constant stirring of the plating bath. TCB does not require any adhesives or flux to attach the die to the package, instead it requires high temperature corresponding to the melting point of In and compressive force ranging from 50-100 g per bump to be applied on the die thereby forming a metallic bond with the PCB. This results in very clean low-resistance bonds devoid of flux or other chemical residues which can aggravate the quality of the device interfaces. To perform TCB, the electroplated PCB is cleaned with a dilute solution of hydrochloric acid immediately prior to bonding the device to remove indium oxides and placed on a hot plate. Precise alignment of the back-patterned signal and ground vias on the chip to the corresponding In-coated microbumps on the PCB for the bonding process is done by placing both the chip and the PCB on a custom copper microwave package. A large copper block is placed as a weight over the package and covered with a bell jar purged with pure N_2 gas. The hot plate is ramped over a period of 8-10 min up to 185 °C followed by a steady state heating at the setpoint for 2 min. This causes In to reflow and form metallic contacts with the backside-patterned underbump metallization of the die. It is necessary to ramp down the temperature of the hot plate equally slowly in order to

[16] Solder datasheet https://www.farnell.com/datasheets/2003737.pdf

prevent cracking of the metallic bonds due to sudden temperature fluctuation. The advantages of this approach is the ease in scalability of the bonding process and equidistant placement of I/O ports across the device. This allows for development of a copy-paste chip design template with increasing qubit count.

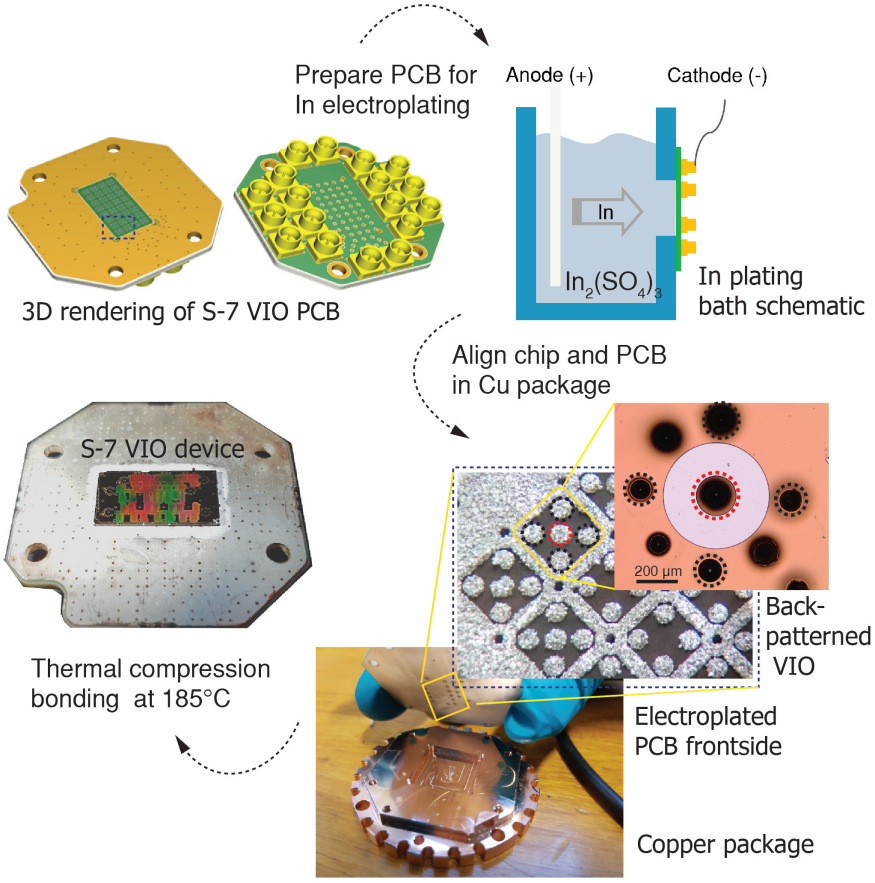


Figure 3.12: Schematic of process flow for thermal compression bonding (TCB) for VIO devices. The dotted red and black circles on the backside pattern of the VIO device align over the corresponding circles on the electroplated PCB. Image credits: Duije Deurloo for 3D rendering of S-7 VIO PCB, Dr. Alessandro Bruno for electroplating bath schematic, Cu package, electroplated PCB and S-7 VIO bonded to PCB.

3.3.8. MEASUREMENT ELECTRONICS

Scaling at the hardware level is only one part of the multi-pronged endeavour towards harnessing practical applications with quantum computing; it must be accompanied by robust scaling of cryogenic systems and control electronics. The

QuSurf architecture encompasses both custom-made and off-the-shelf room temperature electronics stack as shown in Fig. 3.13, described in [240–242]. The QuTech Central Controller (CC) acts as the interface between the end programmer and the lower-level electronics whose function is to determine and coordinate operations with precise timing using codewords. The lower-level control electronics include high-density arbitrary waveform generators (HDAWG) from Zurich Instruments used to generate both the pulse envelopes modulated through a Rohde & Schwarz microwave source for single-qubit gates and flux-pulses for CZ gates. Prior to induction of the HDAWG in the measurement rack, microwave pulses for single-qubit control were generated using the QuTech arbitrary waveform generators (QWG). Microwave operations using the HDAWG requires additional analog equipment for selective and real-time broadcasting of the control pulses, while tailoring the waveforms to individual qubits by means of a frequency reuse scheme. This is carried out using a home-built system called the vector switch matrix (VSM) with 8 input and 32 output channels. The Zurich Instruments Ultra-High Frequency Quantum Analyzer (UHFQA) combines the functionalities of an AWG and a digitizer featuring two input and output signals for baseband operation of quadrature signals (I/Q). It is capable of parallel readout of up to 10 superconducting qubits covering a frequency span of ± 600 MHz. The AWG produces the envelopes of microwave readout pulses injected to a feedline. The digitizer performs demodulation and weighted integration of the feedline output signal (post amplification and frequency down-conversion) and thresholds, producing a one-bit outcome for each qubit measured. Surface-7 devices make use of two UHFQAs, one per feedline.

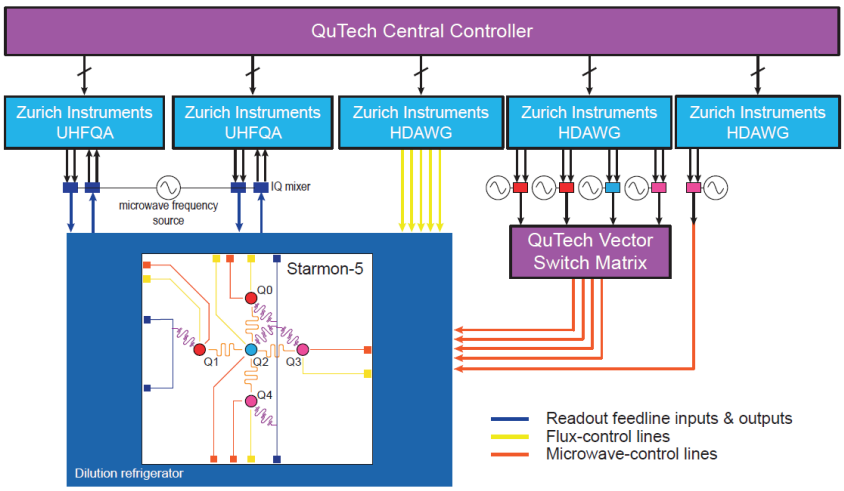


Figure 3.13: Schematic of key RT electronic instruments used for control of Surface-7 device. In this case, the wiring is shown for five qubits. Reprinted with permission from [243].

4

FABRICATION YIELD METRICS

This chapter is dedicated to quantifying the yield metrics relevant for superconducting qubits while increasing complexity and component density. The impact of fabrication processes on yield is broadly categorized into three metrics namely physical die yield, frequency targeting of resonant components and qubit quality characterized by relaxation (T_1) and coherence time (T_2). We introduce a customized solution to quantify physical yield by implementing automated image analysis and metrology of our chips to improve our understanding of factors which contribute fabrication uncertainty. The different factors which impact qubit frequency targeting are identified and detailed using both planar and VIO Surface-7 devices. We identify multiple fabrication-induced irregularities which impact both qubit frequency targeting as well as qubit coherence times from data acquired via room-temperature conductance as well as cryogenically characterized frequency and time domain measurements. Among the variables that impact qubit frequency targeting, we identify an important source of fabrication-induced variation evident at wafer-scale, particularly to bridgeless x-type (Manhattan-style) junctions. This results in a systematic decrease of the actual JJ overlap area and thereby conductance from wafer center to edge, which we qualitatively capture using a geometric model of spatially-dependent resist shadowing during junction electrode evaporation. Lastly, the chapter details the limitations in reproducing qubit relaxation and coherence times between different device iterations. [1].

[1] Parts of this chapter are published in [227]

Sources of systematic and random defects identified from our SQP fabrication processes are elaborated and quantified in this chapter. Quantum information encoded by superconducting qubits is prone to errors due to limitations posed by T_1 and T_2 of the physical qubits, measurement-induced errors such as residual photon population in resonators, leakage of quantum state out of the computational subspace from $|0\rangle$ and $|1\rangle$ and impact of non-equilibrium quasiparticles. In order to suppress errors below the break-even point of solid-state quantum memory, it is imperative to perform repeated QEC to detect both bit-flip (X) and phase-flip (Z) errors. A higher code distance (d), which requires scaling the number of physical qubits thereby increasing the circuit depth allows for correcting a proportionately greater number of errors [13, 244]. At the hardware level, the challenge lies in producing defect-free physical qubits while ensuring consistent reproducibility between batches and addressing hurdles in scalability. Yield models like critical dimension (CD) metrology, prevalent in semiconductor fabrication, have limited applicability for superconducting qubits due to the micron-sized critical dimensions, except for JJs. Fabrication yield metrics in SQPs encompass parameters like pattern transfer fidelity, minimizing defect accumulation at each manufacturing step, matching design specifications of resonator and qubit frequencies and materials and process quality control to enhance qubit and resonator quality. The goal of this work, which extends to the research community at large, is to identify bottlenecks in these parameters which limit the usefulness of multi-qubit devices to perform error detection ($d = 2$) or correction ($d \geq 3$). Assessing the yield in SQPs has become increasingly important due to the continual advancement in the number of physical qubits being realized [12, 245]. IBM currently leads among superconducting quantum hardware platforms, notably launching their 433-qubit "Osprey" processor (IBM, 2022) with accessibility to 413 qubits.

The QuSurf surface code architecture described in Section 3.2.1 is the guideline for design and fabrication of multi-qubit devices described in this chapter. Scaling upto 17 qubits, what we call Surface-17 allows for parallelized X and Z stabilizer measurements using CZ gates with a circuit depth nine [2] [36]. Parallelization of the stabilizer measurements is crucial for minimizing the duration of each error correction cycle in the backdrop of the range of coherence times achieved so far with transmons [137]. The fundamental sub-unit of the surface code is a 2-qubit device comprising of Q_L/ Q_H and a Q_M coupled to each other by a bus resonator. The smallest implementation for error detection is the planar Surface-7 comprising 4 data and 3 ancilla qubits [24], with the full-chip image shown in Fig. 4.1. For demonstration of error correction, we are continuing to work on iterating over the design and fabrication of Surface-17 devices which possesses full chip yield, qubit frequencies sufficiently detuned between nearest neighbours as well as from respective readout resonators (RR), with optimal coupling strengths between qubits and control lines and with average T_1 and T_2 exceeding 30 µs. A summary of the different planar and VIO SQP generations using the processes described in Chapter 3 that have been designed, fabricated and characterized by our research group

[2] In the context of QuSurf surface code, the circuit depth refers to the number of operations per QEC cycle on each ancilla qubit.

during the course of this work is presented in Table 4.1. In this chapter, the yield analysis is mainly based on three design iterations (v1, v2, v3) of Surface-7 devices fabricated by me. Out of a total 25 fabricated devices, 10 have undergone comprehensive cryogenic characterization, serving as benchmarks for assessing physical die yield, resonant element frequency targeting and qubit coherence times for our fabrication processes.

Characteristics	2-qubit	3-qubit	Surface-7	Surface-17
Interconnect	Planar	Planar	Planar VIO	Planar VIO
Fab timeline	2017	2018	2019 2018-19	2020-21 2018-19
# feedlines	1	1	2 2	3 3
Readout resonator design	$\lambda/2$	$\lambda/4$ with PF	$\lambda/4$ with PF $\lambda/2$	$\lambda/4$ with PF $\lambda/2$
Bus frequency (GHz)	8-9	8-9	25-29 8-9	25-29 8-9
# bus resonators	1	2	8 8	24 24
JJ geometry	o-type	o-type	i-type o-type	x-type x-type
# airbridges/crossovers	77/-	152/-	574/3 391/2	2222/20 1051/6
# I/O ports	6	8	18 18	40 40
Chip form factor (mm^2)	7 x 2	7 x 5	8 x 8 14 x 14	13 x 13 22 x 22
PCB form factor (mm^2)	$\pi(30/2)^2$	$\pi(30/2)^2$	$\pi(55/2)^2$ 35 x 35	$\pi(88/2)^2$ 40 x 40
# devices measured	2	3	11 6	13 1

Table 4.1: Overview of the chip design parameters and statistics of different generations of SQPs fabricated during this research. The entries in black (cyan) correspond to planar (VIO) architectures. Note that different JJ geometries are implemented in different device generations. PF stands for Purcell filter in the row describing the design of the readout resonator.

4.1. PHYSICAL DIE YIELD

The physical die yield measures the proportion of operational chip components following device fabrication compared to the intended count. In the context of a Planar Surface-7 device comprising 645 chip elements including airbridges, a subset of 55

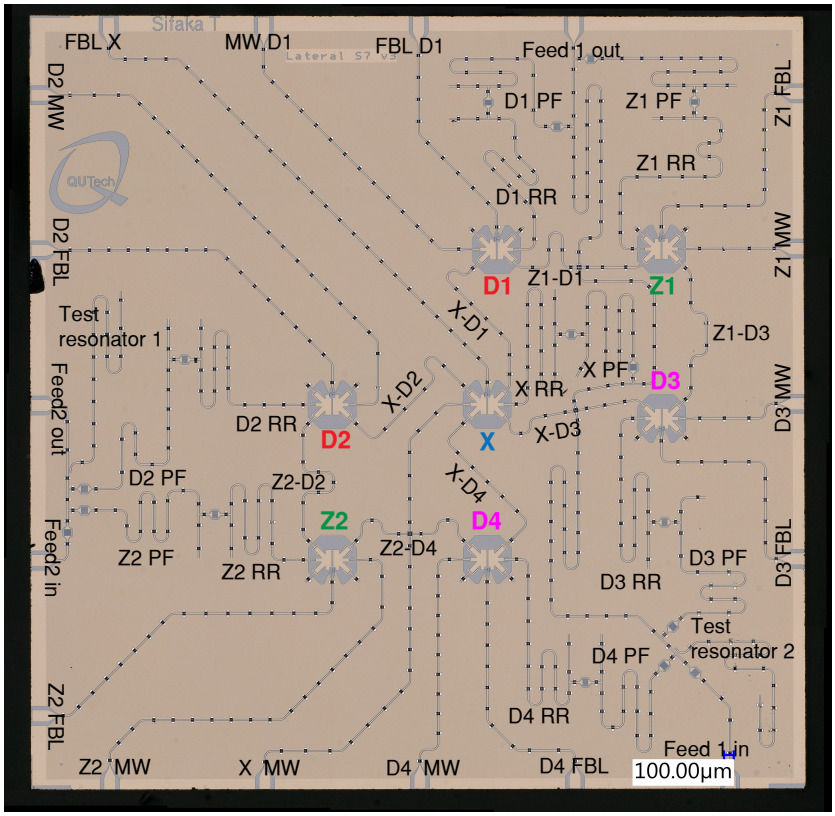


Figure 4.1: Stitched optical image of a planar Surface-7 device, with layout corresponding to generation v2/v3. The coloured labels indicate the seven qubits with red indicating $Q_H = 6.7$ GHz, purple for $Q_L = 4.9$ GHz, green for Z ancilla qubits and blue for X ancilla qubit at $Q_M = 6.0$ GHz. The control lines are indicated by black labels, with Q_M–Q_H/$Q_L$labels indicating bus resonators. RR here refer to readout resonators, PF to Purcell filters, FBL for flux-bias lines, MW for microwave drive lines and Feed1/Feed2 for the input and output ports of the primary/secondary feedline.

elements determine overall die yield. These include qubit capacitor pads (7), control transmisson lines (TL) including feedlines and readout resonators (RR) (23), buses (8), JJs (14), and crossovers (3). Packaging-related defects such as broken wirebonds, faulty connectors or detaching of fridge cables from the package are not factored into this calculation. A summary of the die yield of characterized planar Surface-7 devices, b,ased on the metrics described below is shown in Table 4.2.

Physical defects on the base layer tend to be either random or due to human errors. Several factors contribute, such as stitching errors introduced in the layout during e-beam patterning (See Appendix A.3), damage to the coated e-beam res-

ist after development, incomplete or overetching of the NbTiN film, collapse of Al airbridges on TL, among other potential causes. The addition of TSVs adversely impacts physical yield as the occurrence of these random defects are amplified further due to height variations of spun resist. However, we have still been able to fabricate Surface-7 VIO generation devices with full yield of qubits and control lines, as indicated in Table 4.2. Control TL yield is calculated from RT-measured resistances of the control lines via the corresponding PCB ports. An exception applies for gauging the number of working readout-Purcell filter resonator pairs, based on the number of double-resonance dips observed from transmission (S_{21}) measurements using VNA scans of the feedlines after cooldown. Buses are excluded from the calculation of die yield as they are not directly characterized in every device. Defects on feedlines leading to opens or shorts can render upto 5 readout resonators unusable[3], thereby having the most detrimental impact on device functionality. Careful inspection of the device at every fabrication and packaging step is enforced to minimize the chances of cooling down devices with less than 80% yield loss.

The nature of defects at the JJ step tend to be more complex as both systemic and random sources of error affect JJ yield. JJ yield losses occur due to either shorts, opens or half-open JJs for the case of transmons with SQUID loops. Abnormalities during fabrication process which can lead to either fully open JJs or with lower than expected conductance values are shown in Fig. 4.12. The calculation of qubit yield considers defects on both the capacitor pads and junctions. Defects introduced during the fabrication of airbridges/crossovers represent another catastrophic source of yield loss, given that two out of three crossovers route the primary feedline in all Surface-7 layouts. The most common issues encountered in this step are misalignment of the contact pad and/or airbridge patterns, insufficient development of the patterns, trapped bubbles in the thick PMGI resist layer post spinning that may locally affect the pattern fidelity and cracking of the bilayer resist stack prior to Al deposition (See chapter SI Fig. 4.13). Crossover yield is documented by optical inspection of the structures after dicing and lift-off.

4.1.1. `pyclq`: IMAGE ANALYSIS SUITE FOR SQP METROLOGY

Image-recognition based metrology, falling within the scope of non-destructive testing is widely used in the semiconductor industry for physical defect detection, measuring CD and overlay metrology concerning the alignment accuracy of multiple layers or patterns [246]. Additionally, optical inspection of the chip and/or PCB is now largely done by automated optical inspection (AOI) for detecting catastrophic failure and for quality control. Such tools would equally benefit scalable SQPs, as it becomes difficult to detect defects by employing only manual optical inspection. The challenges faced during the transition from die-level to wafer-scale fabrication of Surface-7 and 17 devices drives the need for a customized AOI solution for SQPs to automate the analysis of physical yield. `pyclq` is a home-built Python programming language-based image analysis suite using the package **openCV** which consists of three modules, each tailored towards inspection of JJs, airbridges and base

[3]Five (two) qubits are read out via the primary (secondary) feedline in a Surface-7 device.

Device ID	Control TL yield (%)	Qubit yield (%)	Crossover yield (%)	Total yield (%) yield (%)
W29 E3 VIO	100	100	100	100
W33b G VIO	100	100	100	100
Blossom X-v1	100	100	100	100
Blossom Y-v1	91.3	100	100	96.8 [b]
Andromeda X-v1	100	100	100	100
Berenike δ-v2	100	100	100	100
Chimera-v2	100	100	100	100
Kratos σ-v2	100	100	100	100
Kratos π-v2	100	100	100	100
Sifaka B-v3	69.5	100	100	88.8 [c]
Snowleopard B-v3	95.2	85.7	100	93.6 [d]
Vaquita B-v3	82.6	100	100	94.2 [e]
Vaquita T-v3 (Starmon-5)	95.6	85.7	100	93.8 [f]

[a] Surface-7 VIO generation
[b] 2 missing RR.
[c] No RR scanned.
[d] 1 qubit dead due to shorted JJ and 1 missing RR.
[e] 4 RR not scanned.
[f] Defective transmon capacitor and 1 missing RR.

Table 4.2: Summary of physical die yields of one VIO and planar Surface-7 devices. Qubit yield is assessed from the number of non-defective qubits measured at RT. Control TL yield is calculated based on RT-measured resistances measured between pin-to-ground of each signal trace, except for RR as explained in the main text. Crossover yield is determined by optical inspection. The total yield is calculated as the percent average of the individual yield metrics.

layer[4] respectively [247]. It is designed for analysis of both stand-alone images acquired using any optical microscope as well as real-time image feed obtained using a camera with a charge-coupled device (CCD) sensor integrated into our home-built automated probe station setup (APS-TASQ), described in further detail in Section 6.3.3. Feature detection and measuring a region of interest (ROI) is done using image-processing techniques namely *thresholding* and *segmentation*. Comparing the similarity between the optical image of the chip and the CAD layout is done by *template matching*.

[4] `pyclq:base` was not experimentally tested within the timespan of this research, it is an ongoing project

4.1.2. pyclq:JJ

pyclq:JJ module is developed to specifically extract the dimensions of Manhattan-style junctions namely the actual widths of the top and bottom electrodes $(W'_{\mathrm{b}}, W'_{\mathrm{t}})$ and the actual transverse overlap area (A'_{overlap}). A data flow diagram of the source code is shown in Fig. 4.2. The SEM micrographs are acquired using only the Hitachi Regulus 8230 in order to keep the image pixel size constant for consistent results. The function **cv2.THRESH_BINARY** converts the 8-bit grayscale image source (src) into a binary image, where the pixels are either 0 or 255 according to the formulae:

$$\text{cv2.kmeans} = \begin{cases} \text{maxValue}, & \text{if src}(x,y) > \text{thresh} \\ 0, & \text{otherwise} \end{cases}$$

where dst(x,y) is the pixel value at coordinates (x,y) in the output binary image, src(x,y) is the pixel value at coordinates (x,y) in the input grayscale image, maxValue is the maximum pixel value assigned to pixels that are above the threshold and thresh is the threshold value.

We employ the basic thresholding method which requires a manual input of either a single threshold value or a range, therefore pixels with values above the threshold become white (255) and below it become black (0). The average pixel value of the image is first read from the SEM micrograph metadata, then multiplied by a set range of thresholds between 1.0 and 2.0 to detect the edge. The top electrode is filled first to reduce pixel noise before detecting the edges of the bottom electrode. By summing the pixels row (column) wise above the threshold, the centre row (column) corresponding to the edge is obtained. The actual width W'_{t} (W'_{b}) is calculated from the mean of the non-zero distance between the edges for each threshold. The defined range of thresholds is used to filter the image and obtain the best edge. A'_{overlap} is obtained by summing the pixels between the outer row edges of W'_{t} over the inner column edges of W'_{b} [227]. The most reliable way to use the software is by the GUI inspection method, where the ROI is defined by a square expandable cursor. The software also allows for batch processing of multiple source files with common thresholding parameters, with overlap area highlighted in the destination file along with a summary of the measurements. The accuracy of pyclq:JJ is compared with A'_{overlap} extracted using ImageJ, where the ROI is defined manually. Generally, the former performs well as long as the image quality is sharp without excessive noise in the background. The edge detection is observed to be less accurate for the case of extremely small junctions $W_{\mathrm{t}}, W_{\mathrm{b}} < 80$ nm, resulting in overestimation of A'_{overlap}. We have tested the validity of the results from the software using hundreds of SEM micrographs of Manhattan-style JJs. All the datapoints in Fig. 5.12(d–f) are extracted using pyclq:JJ.

4.1.3. pyclq:AB

pyclq:AB is a software module developed to detect faulty or broken airbridges by all-optical metrology. Direct template matching from the CAD layout to the source image is not possible as airbridges are 3D structures. The program is deployed

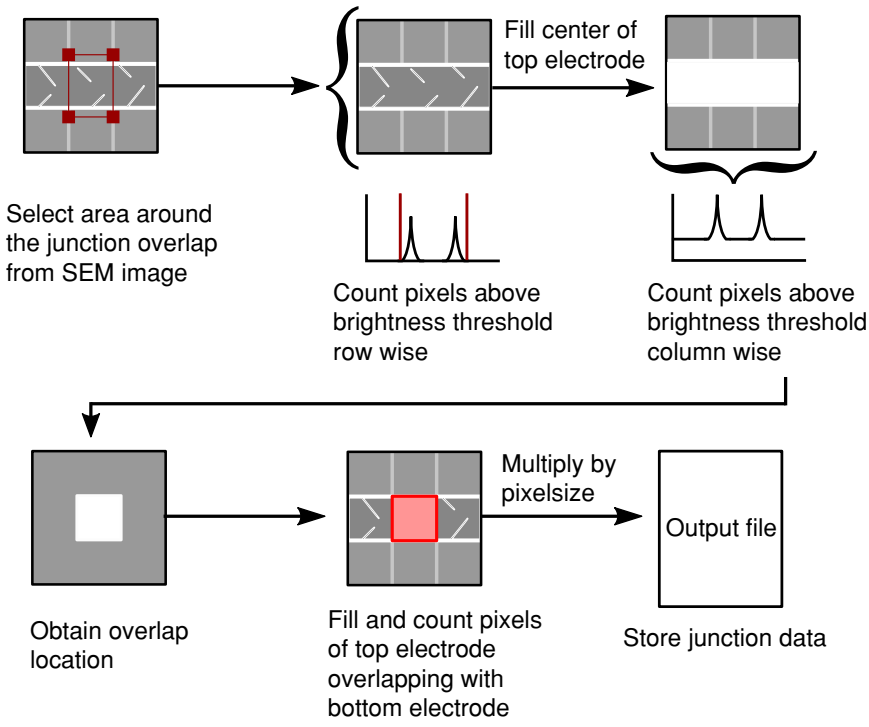


Figure 4.2: Process flow for `pyclq:JJ` for analysing SEM images of Manhattan-style (x-type) JJs. Reprinted from Muthusubramanian *et al.* (2024) [227] under Creative Commons CC BY 4.0 license.

on the APS-TASQ setup where the image acquisition is done in real-time. The coordinates of all airbridge locations and orientations are input into the code as a **.csv** file, in this case, we demonstrate proof-of-concept with a Planar Surface-17 v2 and v3 layouts. The camera exposure settings are adjusted to limit glare and shape deformation of the Al airbridges. Every airbridge is validated by centring it under the field of view of the $10\times$ microscope objective mounted on our setup. The source image in this case is a grayscale 8-bit image (similar to pyclq:JJ), which is partitioned into clusters based on their similarity using the K-means clustering algorithm for unsupervised machine learning. The clustering is based on the differences in light reflection from the airbridge curvature.

The function **cv2.kmeans** is applied twice as shown in the schematic Fig. 4.3, first to subtract the airbridge from the background and second to separate the different brightness components within the airbridge. Using the different clusters, a binary validation can be made with a path over the bridge. The centres of the clusters which pass this validation are averaged in order to define thresholds. This averaged bridge is compared to all the bridges using a template matching algorithm for a final

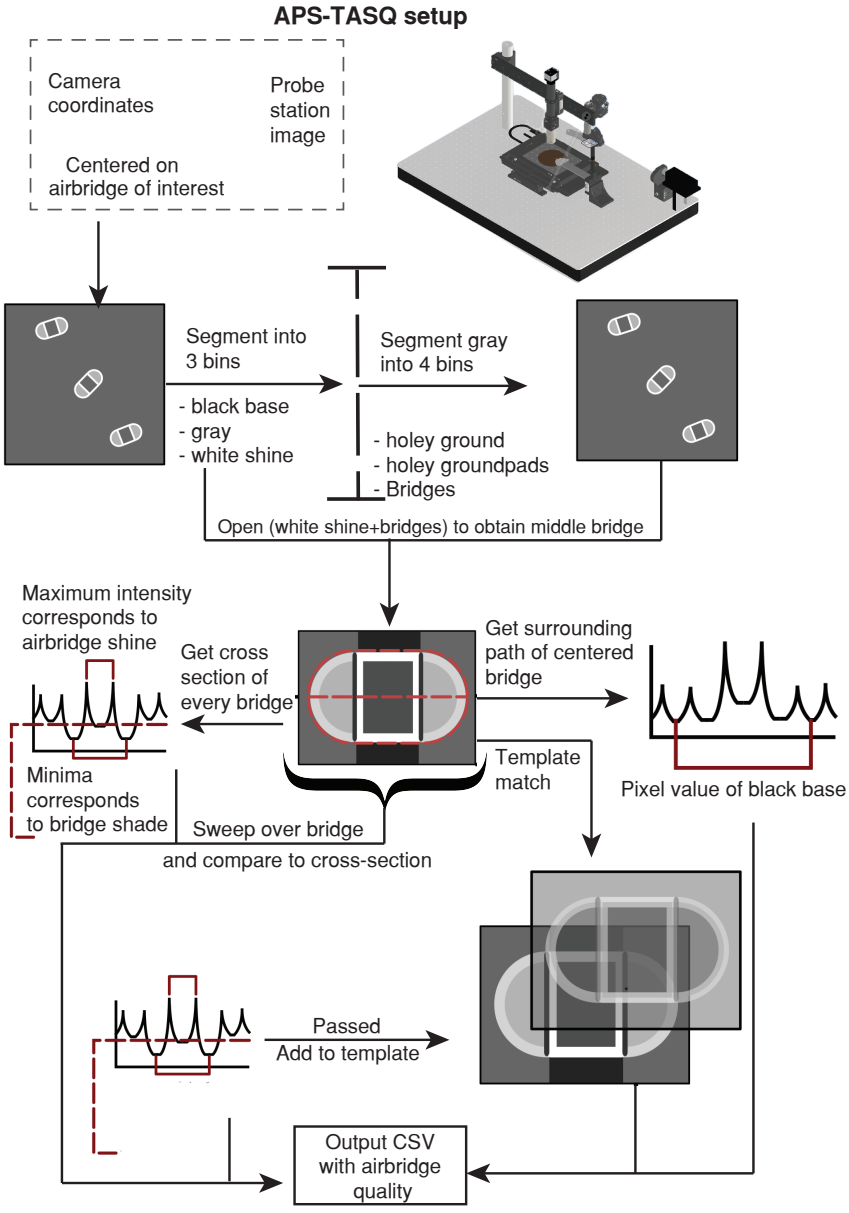


Figure 4.3: Process flow for `pyclq:AB` module. Reprinted from Veen (2021) [247].

validation, using the function **cv2.matchTemplate**. The similarity to the averaged airbridge is performed by template matching using a normalized cross correlation,

described in the chapter supplementary information (SI) in Subsection 4.5.3.

The physical airbridge yield of two Surface-17 devices with identical layouts are compared using `pyclq:AB`, as shown in Fig. 4.4 and the results are validated by manual inspection of select airbridges marked as good or bad depending on the value of confidence interval calculated using the formula Eq. 4.8 (See chapter SI 4.5.3). Due to a smaller number of on-chip crossovers, it is omitted from the analysis. The results of the optical metrology clearly indicate that the device in Fig. 4.4(d) has more defective airbridges, thereby serving as a excellent demonstration of an AOI proof-of-concept tailored for quantum hardware.

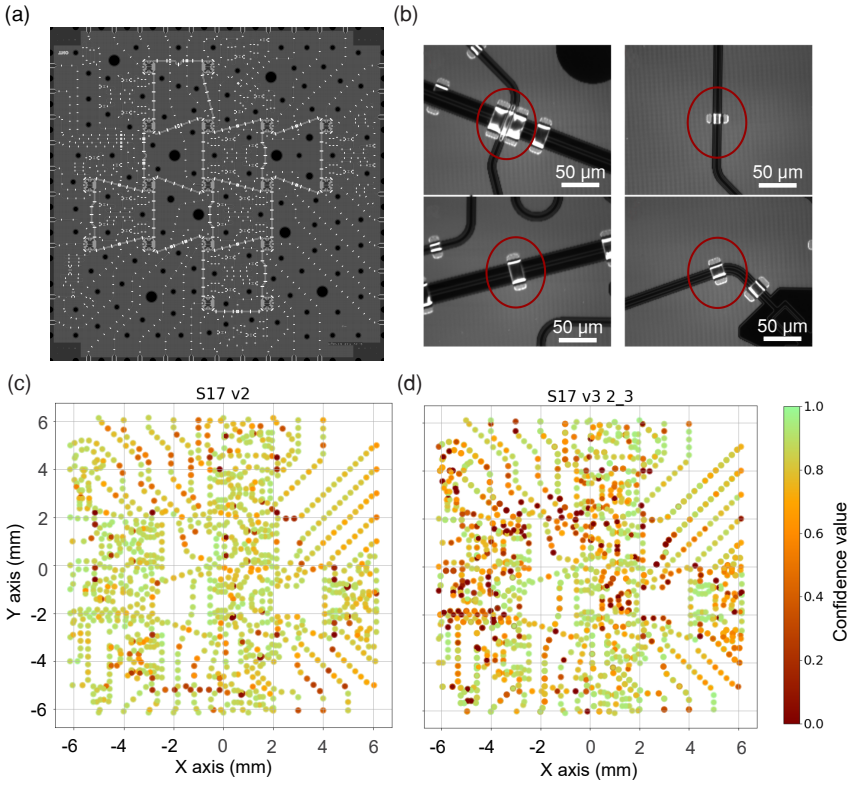


Figure 4.4: (a) Grayscale CAD layout of Surface-17 device showing all the base layer and airbridge elements. (b) Optical grayscale images acquired with the CCD camera of the APS-TASQ setup using a 10X magnification zoom lens. (c,d) Optical metrology of airbridges using `pyclq:AB` comparing (c) a Surface-17 v2 device with 113/1197 bridges marked as bad or doubtful (d) a Surface-17 v3 device with 545/1549 defective airbridges. Each point corresponds to an airbridge location which is optically inspected in real-time using the APS-TASQ setup. The confidence value for each airbridge is computed from results of the template matching algorithm. Reprinted from Veen (2021) [247].

4.2. FREQUENCY TARGETING OF QUBITS

Frequency targeting in multi-qubit SQPs is critical from many functional standpoints. Distinguishability in frequencies of nearest-neighbour qubits is necessary to avoid crosstalk, both from classical electromagnetic and residual quantum couplings. An important source of classical crosstalk is between microwave drive lines of adjacent qubits with a detuning $\Delta_{ji} = \omega_j - \omega_i$. When Δ_{ji} decreases, off-resonant driving results in bit-flip errors due to AC Stark shift of the qubit frequency [248].

A direct consequence of mistargeting of qubit frequencies is the deviation in detuning between qubit pairs. The designed detunings in our architecture are Q_H–Q_M= 700 MHz and Q_M–Q_L= 1000 MHz to minimize undesirable interactions between gate and spectator qubits while performing CZ gates. In the instances where Δ_{ji} is lesser than the designed value between a target and spectator qubit, it can give rise to static ZZ crosstalk due to cross-Kerr interaction [175, 249] during flux-pulsing operations. This leads to 5× increase in gate errors limiting its parallelization in SQPs [35, 250] with always-on transverse qubit coupling. The residual ZZ coupling is measured from the frequency difference $\Delta\omega_i^{(j)}$ between Ramsey oscillations of neighbouring qubits i and j in state $|1\rangle$ and $|0\rangle$ respectively [251]. A detailed characterization of frequency shifts experienced by the gate qubits due to the spectator qubit being in the excited state $|1\rangle$ using the device *Chimera v2* is described in [24]. Minimizing ZZ crosstalk is achieved in each design iteration by increasing the frequency detuning and/or decreasing qubit coupling strength $J_1/2\pi$ between the q_i and q_j.

Lastly, maintaining the targeted detuning (Δ_{r-01}) between qubit-resonator pairs is essential to operate in the dispersive regime. Frequency targeting of resonators is relatively straightforward, which requires the input ν_p extracted from high Q_e *witness resonators* fabricated in each chip. Deviations in RR frequency between the designed ($f_{\mathrm{r,des}}$) and measured ($f_{\mathrm{r,meas}}$) values occur mainly due to the radial thickness variation and from the L_k fraction of the film. Deviations beyond 20 MHz between RR-PF resonator pairs result in poor hybridization which is detrimental for readout fidelity [252]. The magnitude of the challenge becomes evident on scaling upto Surface-N, where coupling 20 qubits per feedline requires a frequency separation of 25 MHz at sampling rate 1 GSa/s. This limitation is imposed by the 3-GHz bandwidth of the signal amplification chain, which relies on a TWPA [234]. The evolution from 2-qubit to 17-qubit devices has deepened our understanding of factors contributing to deviations from intended device specifications. The sources of error in qubit frequency targeting due to fabrication are identified as follows:

4.2.1. TUNNEL BARRIER INHOMOGENEITY AND INSTABILITY

Non-uniformity in the thickness of the 1–2 nm-thick thermally grown AlO_x tunnel barrier due to randomness in crystal orientation of the grains and local increase in tunnel barrier thickness between grain boundary grooves of the lower Al electrode [49, 253, 254] pose fundamental constraints to achieving a high degree of control and reproducibility of junction conductance. In Ref. [49], it is shown that irrespective of the RT oxidation time and pressure conditions, the standard devi-

ation (**SD!**) of the tunnel barrier thickness does not decrease below 0.3 nm at the intra-sample level, thereby concentrating the active tunnelling region to less than 10% of the junction area. To illustrate the impact of tunnel barrier inhomogeneity, a die is fabricated containing 84 i-type JJ pair test structures with NbTiN metallization layer and nominally identical designed electrode widths swept from 70–154 nm. The RT conductance is characterized in the 2-wire configuration and the predicted qubit frequency ($f_{\mathrm{q,pred}}$) is plotted as a function of the designed sweeping electrode width of i-type JJ pairs as shown in Fig. 4.5. The spread is quantified by the coefficient of variation (CV) as depicted in the insets of Fig. 4.5(a) which is limited to $\sim 3.4\%$ and (b) at around $\sim 1.7\%$ respectively. It is inferred that the spread in conductance at the intra-die level is most likely attributed to localized variations in tunnel barrier thickness. Furthermore, the composition of the AlO_x layer is also susceptible to process and environmental variations due to its reactivity with heat, moisture and other atmospheric contaminants. This leads to temporal drifts in JJ conductance (Refer to Chapter 6).

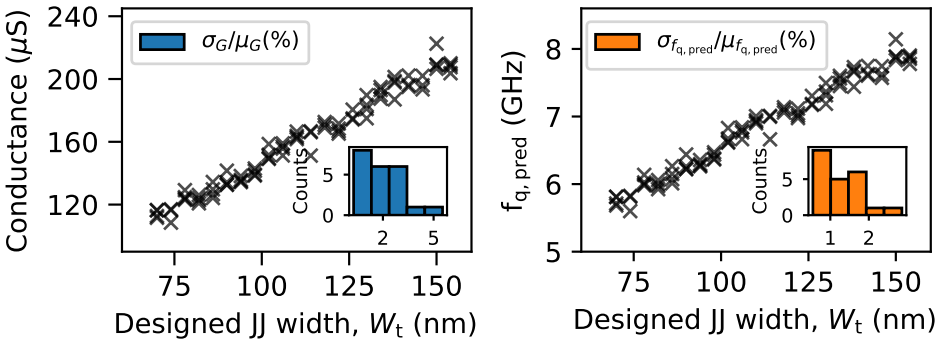


Figure 4.5: Statistics from i-type (Dolan-bridge) JJs fabricated on a 5×2 mm^2 area with four nominally identical repeats of junction width sweeps by varying the designed top electrode width (W_{t}) with a step size 4 nm. (a) Plot of conductance vs. W_{t}, with a histogram of the coefficient of variation CV $= \sigma_G/\mu_G(\%)$ plotted in the inset. (b) Plot of corresponding predicted qubit frequency ($f_{\mathrm{q,pred}}$) vs. W_{t} calculated from Eq. 2.13 using $E_{\mathrm{c}}/h = 285$ MHz and $M = 140$ GHz/mS, with a histogram of the coefficient of variation CV $= \sigma_{f_{\mathrm{q,pred}}}/\mu_{f_{\mathrm{q,pred}}}(\%)$ plotted in the inset.

4.2.2. VARIATIONS IN JJ OVERLAP AREA

Increasing the number of physical qubits also entails increasing the chip form factor, therefore ensuring spatial repeatability of qubit frequencies at the intra-die level is an important criterion for qubit frequency targeting. The dimensions of JJ top and bottom electrodes and the overlap area are sensitive to a multitude of fabrication subtleties which impede sub-50 MHz targeting precision. The JJ I_{c} is directly proportional to the overlap area of the top and bottom Al electrodes. It is well-known

that the overlap area of i-type junctions are sensitive to resist-height variations, which are quantified by acquiring statistics of i-type JJs fabricated on TSV-integrated wafers in Subsections 5.4.4 and 5.4.4. x-type (Manhattan-style) junctions are believed to obviate this limitation due to its relatively lower sensitivity to resist-height variations. However, this advantage is offset by the *resist-shadowing effect* [227, 255], which becomes evident on scaling the JJ fabrication from die-level to wafer-scale (Refer to Subsections 5.4.2 and 5.4.3). The mechanism of resist-shadowing resulting in a systematic centre-to-edge variation in the overlap area of x-type junctions is described in detail below.

GEOMETRIC RESIST-SHADOWING MODEL

The essence of the geometric model is a spatial dependence of junction electrode widths arising from oblique incidence of the Al flux during evaporation. Specifically, the width of vertical electrodes (both electrodes for i-type JJs, bottom electrode for x-type JJs) depends on the x coordinate, while that of horizontal electrodes (top electrode for x-type) depends on the y coordinate. Key parameters of the model are the thickness of the top resist $H = 600$ nm (which acts as the shadow mask), the wafer tilt $\theta = 35^\circ$ during Al evaporations, and the physical configuration of the Plassys MEB550S e-beam evaporator. These last parameters include the distance $D' = 650$ mm between the crucible at $\vec{C}$ and the pivot point $\vec{O}'$ of the sample holder, and the distance $R = 62.5$ mm between $\vec{O}'$ and centre $\vec{O}$ of the exposed wafer surface (see schematic in Fig. 4.6(a)). This results in a distance $D = D'\cos(\theta) - R$ between $\vec{C}$ and the plane defined by this surface [256]. In a Cartesian coordinate system with origin at $\vec{O}$ and $\vec{r} = (x, y, 0)$ lying on this plane, $\vec{C} = (0, D'\sin(\theta), D)$. Evaporation under these conditions deposits electrodes extending along the y axis. An electrode of this orientation with x coordinate has actual width

$$W'(x) \approx W + \delta W_{\text{offset}} - |x|\frac{H}{D}, \tag{4.1}$$

where δW_{offset} is a constant widening from over-exposure and development of the e-beam resist, as we do not calibrate the JJ patterns for proximity effect. Eq. 4.1 is valid for $D >> |x|$ which is the case in the Plassys evaporator as $D \approx 470$ mm. Including these modifications to the width of both electrodes, the actual overlap area becomes

$$A'_{\text{overlap}}(\vec{r}) = W'_{\text{b}}(x)W'_{\text{t}}(y). \tag{4.2}$$

Fig. 4.6(b) shows the spatial dependence of A'_{overlap} for x-type JJs with $W_{\text{b}} = W_{\text{t}} = 200$ nm and $\delta W_{\text{offset}} = 25$ nm on a 100-mm diameter wafer.

We can further expand the model by approximating the contribution of sidewalls to A'_{overlap}. The spatially-dependent actual bottom electrode thickness is

$$T'_{\text{b}}(\vec{r}) = T_{\text{b}}\frac{(D'-R)^2 D}{|\vec{r}-\vec{C}|^3}, \tag{4.3}$$

where $T_{\text{b}} = 35$ nm is the calibrated thickness at $\vec{O}$ under normal incidence $(\theta = 0)$.

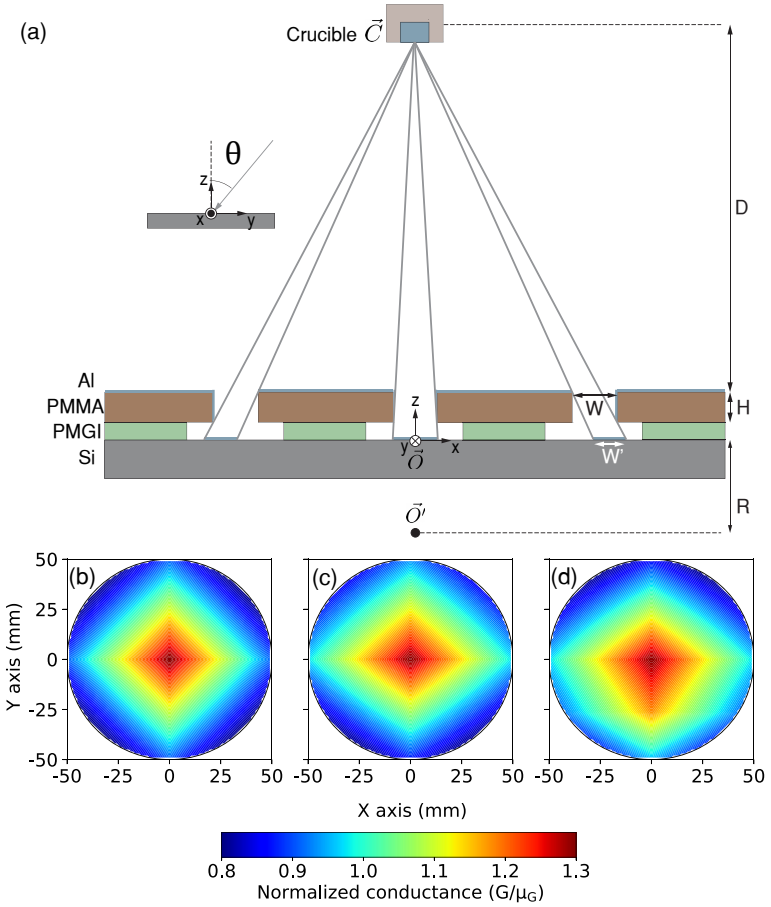


Figure 4.6: (a) Schematic of e-beam Al evaporation setup (not drawn to scale). Please see text for further details and parameter values. The illustration shows the decrease in junction electrode width from centre to edge of wafer arising from the spatially-dependent shadowing effect. (b) Wafer-scale mean-normalized conductance computed from actual junction overlap area A'_{overlap} as per equation 4.2, for Manhattan JJs with $W_{\text{t}} = W_{\text{b}} = 200$ nm and $\delta W_{\text{offset}} = 25$ nm. (c) Same as (b) but adding the overlap contribution from sidewalls as per equation 4.4. (d) Same as (c) but adding effects of the first evaporation (of the bottom electrode) on the second evaporation (of the top electrode) (equations 4.5 to 4.7).

Approximating the sidewalls as vertical,

$$A'_{\text{overlap}}(\vec{r}) = \left(W'_{\text{b}}(x) + 2T'_{\text{b}}(\vec{r})\right) W'_{\text{t}}(y), \tag{4.4}$$

The modified spatial dependence is shown in Fig. 4.6(c). Note that we do not model the effect of shadowing by the bottom electrode during evaporation of the

top electrode, which most likely reduces the overlap at the eastern sidewall (evident in Fig. 5.19).

Finally, we can model some predictable effects of the first evaporation (for the bottom electrode) on the top electrode. The first evaporation deposits an Al layer above the top resist, effectively increasing its height by $\delta H(\vec{r})$ (also given by the right-hand side of equation 4.3). More importantly, it also deposits a lip on the southern resist edge for the top electrode (see Fig. 4.15), with width W_{lip} and height H_{lip}:

$$W_{\text{lip}}(\vec{r}) = -T_{\text{b}} \frac{(D'-R)^2 (D'\sin(\theta)-y)}{|\vec{r}-\vec{C}|^3}, \tag{4.5}$$

$$H_{\text{lip}}(\vec{r}) = \frac{DW_{\text{t}}}{D'\sin(\theta)-y}. \tag{4.6}$$

The shadowing effect of these features makes

$$W'_{\text{t}}(\vec{r}) \approx W_{\text{t}} + \delta W_{\text{offset}} - \begin{cases} W_{\text{lip}}(\vec{r}) + H'(\vec{r})\frac{|y|}{D}, & \text{for } y \geq 0, \\ \max\left(H'(\vec{r})\frac{|y|}{D}, W_{\text{lip}}(\vec{r}) + H'_{\text{lip}}(\vec{r})\frac{|y|}{D}\right), & \text{for } y < 0, \end{cases} \tag{4.7}$$

where $H'(\vec{r}) = H + \delta H(\vec{r})$ and $H'_{\text{lip}}(\vec{r}) = H_{\text{lip}}(\vec{r}) + \delta H(\vec{r})$. Including all modelled effects leads to $A'_{\text{overlap}}(\vec{r})$ as shown in Fig. 4.6(d). Additionally, the behaviour of the other spatially-dependent variables in the geometric model are modelled in Fig. 4.16.

Experimental evidence for the resist-shadowing effect from wafer-scale depositions of x-type JJs is done by acquiring SEM images of JJs across the wafer, which indeed exhibits a systematic centre-to-edge decrease in W'_{b} and W'_{t} (Refer to Fig. 5.12). The implications of the resist-shadowing effect is wide-ranging, as it directly impacts the scalability at the level of Surface-17 devices. Mitigative measures have already been implemented during the course of this work, by pre-compensating the designed JJ widths (W_{b}) of x-type JJs following the trends of the geometric model. Indeed, one of the wafer-scale fabrication attempts with JJ widths pre-compensated for the resist-shadowing effect yielded devices (*Aurora v2*. *Aurelius v2* and *Jason v2*) with the lowest spread in qubit-qubit detuning, shown in Fig. 4.10.

4.2.3. RT MEASUREMENT ERRORS

An advantageous feature of transmon qubits is the ability to design and predict the operating frequencies in a purely analytical fashion from room-temperature measurements of the junction conductance using the Ambegaokar-Baratoff relation [257]. The G values are usually designed in the range $50-200\ \mu\text{S}$, which corresponds to our f_{q} specifications. This range is relatively convenient to measure with conventional I-V characterization. However, JJs are known to be sensitive to tunnel barrier breakdown even at low current bias values of $1\ \mu\text{A}$. We instead use a home-built transimpedance amplifier based on an inverting operational amplifier (op-amp) with a feedback resistor with $10^5\ \Omega$ gain (See Appendix A.4 for the circuit). This circuit produces a constant offset of $4\ \mu\text{S}$, even in the absence of a device under test. Most of the data presented in this work are acquired using a 2-wire method using $10\text{-}\mu\text{m}$

point diameter tungsten needles [5] mounted to probe manipulator arms of a manual probe station housed in VLL. In a 2-wire configuration, the external cabling resistance constitutes a fixed offset in the total G, which can be ignored if sufficiently small and if the resistance of the device under test (DUT) is at least an order of magnitude higher. The advantage of 4-wire over 2-wire method is the elimination of resistive contributions from the external cabling of the setup, with the caveat of requiring an additional pair of probe needles . Some of the measurements described in this work have been acquired using a 4-wire configuration using a home-built automated probe station (APS-TASQ). To quantify series resistance from the probe contact and external cabling denoted by R_c, we compared 2- and 4-wire G measurements taken with the APS, finding a best-fit value of $\sim 19\ \Omega$ (See Appendix A.4). When manually probing JJs, the user needs illumination in order to view the sample under the microscope. This introduces a parallel conductance channel from the Si substrate proportional to the magnitude of the incident intensity due to the photoelectric effect. This leads to overestimating $f_{q,pred}$ by at least 2% as in Fig. 4.7, particularly if the illumination source shares the same grounding as the rest of the probe station.

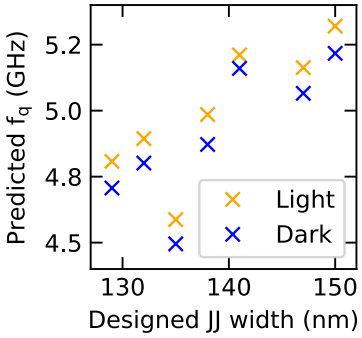


Figure 4.7: Comparison of effect of illumination on predicted frequency $f_{q,pred}$ as a function of designed JJ width of o-type junctions calculated as in Fig. 4.5

4.2.4. ERRORS IN RT-PREDICTED FREQUENCY

The Ambegaokar-Baratoff relation (Eq. 2.13) establishes a quantitative relationship between I_c and G_n. This is vital for calculating the transmon sweet spot frequency using Eq. 2.32. The E_c term is input as a design variable calculated by summing the total capacitive network of the transmon, usually with an electromagnetic solver. The constant M is therefore the only unknown variable when determining the conductance corresponding to the desired range of predicted qubit frequency ($f_{q,pred}$) by sweeping the JJ $A_{overlap}$. We start with a prior value of M based on E_J extracted from spectroscopy data. The values of initial-guess E_c and M for calculating $f_{q,pred}$ is varied for every device generation (See Table 4.3). We then compare the extent of agreement between the initial and measured values by performing a least-squares fit between the cryogenically characterized qubit frequencies ($f_{q,meas}$) and

[5] Model: 7B-5 tungsten probe needles from The Micromanipulator Company

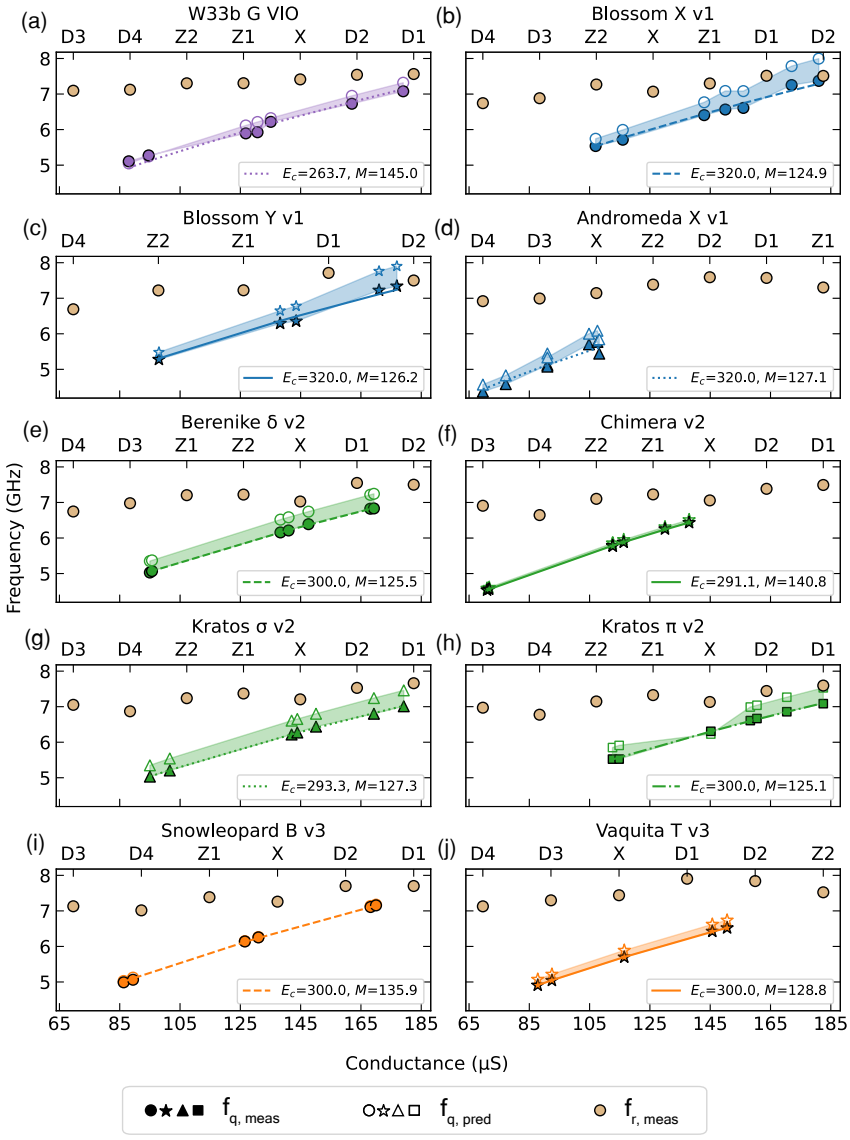


Figure 4.8: Plots of cryogenically characterized Surface-7 devices with predicted ($f_{\mathrm{q,pred}}$) and measured ($f_{\mathrm{q,meas}}$) qubit frequency vs. RT-measured G on the lower x axis and measured resonator frequency ($f_{\mathrm{r,meas}}$) vs. qubit identifier on the upper x axis. The non-linear least squares fits are extracted from $f_{\mathrm{q,meas}}$ vs. G using Eq. 2.32 using the bounds $M = 120 \leq x \leq 145$ GHz/mS and E_{c} (a) $0.23 \leq y \leq 0.28$ GHz, (b–d) $0.23 \leq y \leq 0.32$ GHz, (e–j) $0.23 \leq y \leq 0.3$ GHz. Data courtesy from DiCarlo lab.

the RT-measured G plotted in the lower x axis as shown in the subpanels of Fig. 4.8. Except W33b-G VIO which is fabricated with the VIO recipe and incorporates x-type JJs (Fig. 4.8(a)) , the JJ geometry (i-type) and fabrication processes are conserved across all the planar Surface-7 devices except for the base layer etching technique, which is switched to partial dry + wet etch from v2 generation onwards (Fig. 4.8(e)–(j)). This dataset presents an intriguing case study, where only the devices *Chimera v2* and *Snowleopard B v3* show excellent agreement between the input and extracted M value and consequently $f_{\mathrm{q,pred}}$ and $f_{\mathrm{q,meas}}$. In order to understand how wet etching qualitatively impacts the fabrication process and the substrate-air interface, the areal surface roughness (S_{a}) of the Si substrate at EOL is quantified by AFM scans from either the same device that is cooled down or from a sibling device fabricated in the same die (See chapter SI 4.5.5). It is curious to note that the measured Si roughness is also the lowest in the *Chimera v2* and *Snowleopard B v3*, followed closely by *Vaquita T v3*. Notably, for the devices *Berenike* δ *v2* (dry etch, $S_{\mathrm{a}} \sim 2$ nm) and *Chimera v2* (dry + wet etch, $S_{\mathrm{a}} \sim 0.3$ nm) the JJ deposition steps are performed simultaneously and the initial guess E_{c} and M are identical. However, the extracted superconducting gap constant from $f_{\mathrm{q,meas}}$ of *Berenike* δ *v2* is significantly lower than the input value at $M = 125$ GHz/mS, whereas in *Chimera v2*, the extracted $M = 141$ GHz/mS perfectly matches the input M value.

These observations may suggest a link between the substrate surface roughness which in turn affects the tunnel barrier transparency and thereby I_{c} [258]. A recent work highlights contributions from higher Josephson harmonics due to tunnelling through the inhomogeneous AlO_x layer, which increases susceptibility to charge dispersion thereby decreasing the effective E_J as calculated from the standard transmon model [254]. Further investigation is necessary to establish a clear relationship between Si surface roughness and the tunnel barrier homogeneity and its role in formation of high-transparency channels that affect the Josephson current-phase relation [259].

4.2.5. INCONSISTENT QUBIT PAIR DETUNING

Even if $f_{\mathrm{q,meas}}$ falls outside the target qubit frequency by ± 200 MHz, the chip can still be viable if the qubit pair detunings Δ_{ji} correspond to the target detunings $\Delta_{ji,\mathrm{target}}$. This is a necessary criterion to minimize residual ZZ crosstalk between qubits in the Qusurf architecture due to the always-on coupling of bus resonators (See Subsection 3.1.2). A Surface-7 device has 8 bus resonators between the ancilla and data qubit pairs X-D1, X-D2, X-D3, X-D4, Z1-D1, Z1-D3. Z2-D2 and Z2-D4 (See Fig. 4.1). To visualize the spread in the detuning between the qubit pairs, the difference between the target detuning $\Delta_{ij,\mathrm{target}}$ and the detuning from $f_{\mathrm{q,pred}}$ ($\Delta_{ij,\mathrm{pred}}$) and from $f_{\mathrm{q,meas}}$ ($\Delta_{ij,\mathrm{meas}}$) are calculated for the characterized Surface-7 devices and plotted in Fig. 4.9. Negative deviations observed in the plot do not aggravate static ZZ-crosstalk, as it implies that $\Delta_{ij,\mathrm{pred}}$ or $\Delta_{ij,\mathrm{meas}}$ is larger than the target value, which is observed in the case for all qubit-qubit detunings in *Snowleopard B v3*. In *Chimera v2*, 4 of the 8 detunings are lesser than $\Delta_{ij,\mathrm{target}}$ which causes phase shifts in the target qubit when the spectator qubit is in the $|1\rangle$ state.

The same analysis is extended over to a subset of planar Surface-17 devices

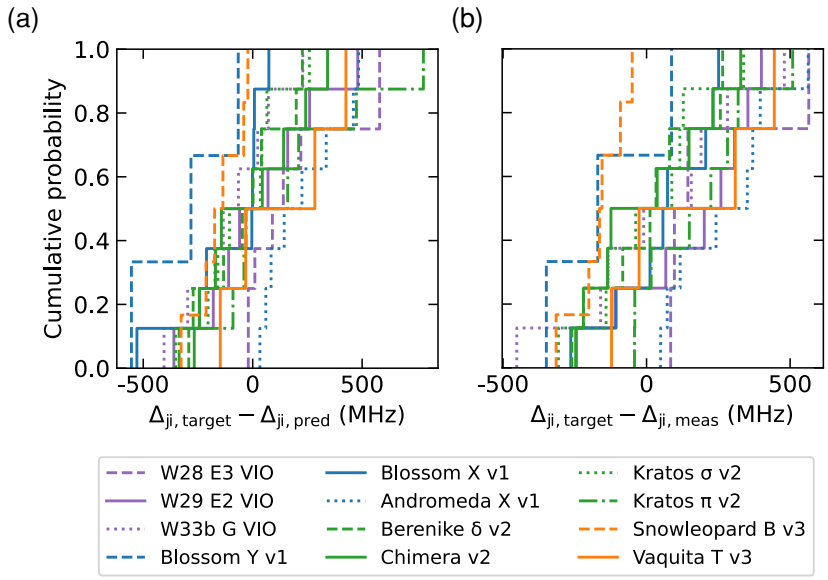


Figure 4.9: Cumulative probability distribution of the difference in qubit-qubit detuning from target and (a) $f_{\mathrm{q,pred}}$ (b) $f_{\mathrm{q,meas}}$ from planar and VIO Surface-7 devices. Data courtesy from DiCarlo lab.

which share similar design layout as that of Surface-7 devices, which are all integrated with x-type JJs. In Fig. 4.10, the SD of the deviation in detuning between target and $f_{\mathrm{q,pred}}$ is plotted, where devices upto generation v2 are fabricated on a full wafer, while the remainder are fabricated at die level. The A_{overlap} for each frequency group is sequentially increased for each die from centre-to-edge of the wafer to pre-compensate for the narrowing of electrodes due to the resist-shadowing effect (See Chapter 5). A single chip from either fabrication routes, *Aurora v2* at wafer scale and *Hyperion v4* at die level show a detuning spread ≤ 100 MHz. Comparatively, the detuning spread is lower in Surface-17 devices than Surface-7, with over 10 devices falling within 150 MHz margin.

4.3. QUBIT COHERENCE

This section elaborates further on how each fabrication process has been tested and validated vis-à-vis qubit coherence improvements. Based on density-matrix simulation on quantum memory, the aim is to target $T_1 \geq 30\ \mu$s so that the ratio of physical to logical error rates surpasses the break-even point of quantum memory in a distance-3 logical Surface-17 [137]. Quantifying improvements to qubit coherence by optimizing materials and fabrication strategies is perhaps the most challenging aspect of this research, due to the intrinsic disposition of nanofabrication techniques to many parameter fluctuations. Qubit coherence is known to be impacted

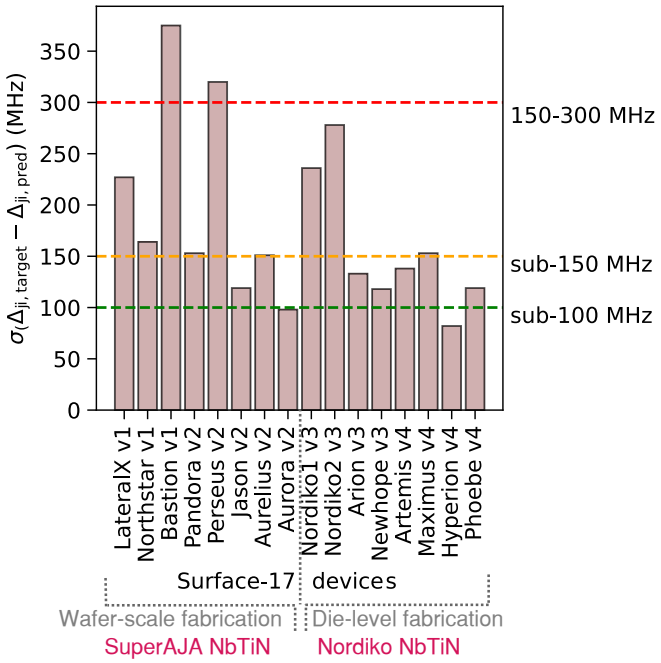


Figure 4.10: Bar plot of residual standard deviation (RSD) of qubit pair detunings Δ_{ji} calculated from $f_{\text{q,pred}}$. The devices up to *Perseus v2* are fabricated at wafer-scale without pre-compensating the JJ widths. The devices *Jason v2*, *Aurelius v2* and *Aurora v2* are fabricated from a single wafer pre-compensated for the resist-shadowing effect. Data courtesy from DiCarlo lab.

by multiple factors, notably flux noise [260], radiative loss [261], thermal and non-equilibrium quasiparticles [109, 111, 262–264]. In spite of the sensitivity of qubit coherence to environmental fluctuations, several research groups have demonstrated remarkable progress in prolonging qubit relaxation times above $100\ \mu s$ timescale [106, 265, 266], albeit with simpler fixed-frequency qubits devices without nearest-neighbour couplings. At the fabrication level, the focus remains on mitigating dielectric losses for improving qubit T_1 by engineering pristine interfaces between the materials, schematically depicted in Fig. 2.6. Addressing improvements to T_1 in our SQPs has been frustrated by the inability to identify concrete and reproducible parameters in fabrication which can then be improved upon; an Achilles' heel in our progress towards demonstrating QEC. I discern certain factors unique to our materials and fabrication processes which may be limiting our qubit quality, with the caveat that it needs to be validated by experimental evidence and theoretical models.

Metal-substrate interface

The M-S interface constitutes the largest interface in 2D transmons between the dielectric substrate and the deposited superconducting metallization layer. As described in Section 3.3.2, the pre-treatment of a bare Si wafer with HF and HMDS prior to sputtering NbTiN is directed towards removal of spurious native oxides which give rise to TLS defects contributing to qubit relaxation in the quantum regime [97]. This step is observed to be universally important irrespective of the metal

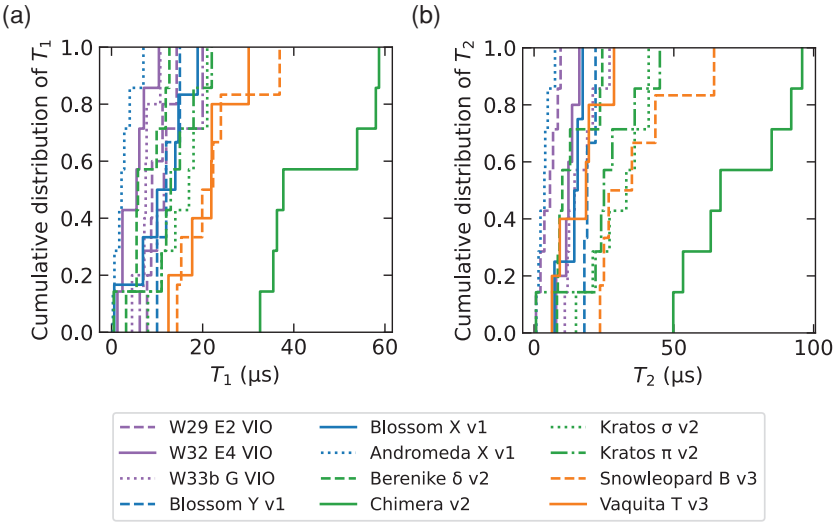


Figure 4.11: Cumulative distribution of (a) T_1 and (b) T_2 of characterized Surface-7 planar and VIO devices measured at the qubit sweet spot frequencies. Data courtesy from DiCarlo lab.

layer used for deposition. However, sapphire substrates do not benefit from HF treatment owing to its non-reactivity to strong acids and alkalis. In fact, state-of-the-art qubit relaxation times have been reported from devices fabricated on sapphire due to its low losses ($\tan\delta_{\text{int}} = 1.5 \times 10^{-8}$ at 9 GHz) [267]. On the other hand, low-temperature measurements of loss tangent of resonators fabricated on hi-res FZ Si is $\tan\delta_{\text{int}} = 2.7 \times 10^{-6}$ [268], indicating that Si substrates are not optimal for realizing low-loss qubits.

Aside from the superconducting metal layer, the interface between the substrate and the Al/AlO$_x$/Al stack of junctions is also another important M-S interface that warrants further investigation. The trend of the cumulative distribution of T_1 and T_2 of multiple planar and VIO Surface-7 devices in Fig. 4.11 indicate that devices subjected to dry + wet etch processing exhibit higher qubit quality. This once again brings into focus the role of Si roughness on tunnel barrier inhomogeneity, which is unfortunately not clearly established in this work as previously described in Subsection 4.2.4. We have only acquired comparative AFM scans of the Si substrate from the planar Surface-7 devices to extract the S_a without also measuring the roughness of the Al bottom electrode. Prior literature on substrate surface engineering of Si/superconductor interfaces show that the power-dependent losses of CPW resonators is greatly increased on the roughest surfaces [269]. Unfortunately, the Q_i measured from witness resonators of Surface-7 devices listed in Table 4.3 does not show any clear trend with the substrate S_a except for *Chimera v2*.

SUBSTRATE/METAL-AIR INTERFACES

The dry + wet etching process incorporates a post-etch HF step to remove inorganic sacrificial layer, which serves as an in-built measure to mitigate spurious oxides at the S-A interface. This hypothesis is based on prior work with TiN resonator showing a noticeable decrease in loss tangent of the S-A region after a post-fab HF treatment, compared to the control resonators [203]. The M-A interface is perhaps the least understood in our materials composition, given that we do not observe significant differences in Q_i between NbTiN resonator fabricated with either SuperAJA or Nordiko films. In a broad sense, we obtain more consistent results with films deposited using the Nordiko system, this maybe attributed to the superior deposition parameters and tool configuration. The highest Q_i measured from witness resonators integrated in planar SQPs in the single photon regime is 1.2×10^6 (Surface-17 *Nordiko-2 v3*), with average values around $\sim 5 \times 10^5$. This is at least a factor two smaller than previously reported Q_i from other nitride-based superconductors such as TiN [270, 271]. Recent work on superconducting microwave resonator with RF-magnetron sputtered epitaxial TiN films deposited on c-cut sapphire substrates have shown $Q_i = 3.3 \times 10^6$ in the single-photon regime [272]. This work lays emphasis on the deposition conditions and the resultant transport properties of the films.

METAL-METAL INTERFACE

Lastly, there are two metal-metal interfaces (M-M), one between the JJ electrodes and base layer and the other between the Al airbridge contact pads and base layer. For the case of the JJ-base layer interface, formation of spurious or stray junctions due to the exposure of NbTiN bay to high O_2 partial pressure during thermal in-situ tunnel barrier formation before depositing the JJ top electrode is a potential source of dielectric loss [273]. The dimensions of the JJ electrode contact pad, which is $5\times$ smaller for x-type JJs in comparison to i-type JJs, can also potentially aggravate the resistance between the Al/AlO_x/Al- NbTiN joint below the T_c of Al. Additionally, spurious junctions can also be formed in uniaxial JJ geometries such as i-type JJs where deposition on one electrode (bottom electrode) results in unintended deposition on the opposing electrode (top electrode) and vice versa. This cross-contamination is due to the alignment of both electrodes along a single axis, the proximity of the electrodes and the low deposition tilt $\theta_{\text{i-type}} = 15°$. Spurious junction-like structures formed in series with the intended junction constitutes another dissipative channel. IBM's qubits incorporates a modified version of the Dolan-bridge junction where the electrodes are defined orthogonally or 'tip-to-tip', which eliminates the introduction of spurious junctions [6].

4.4. DISCUSSION

In this chapter, we have introduced the key metrics relevant for fabrication of transmon-based SQPs, namely the physical yield of components, the targeting of resonators and qubits according to design specifications and qubit coherence. Both our planar

[6] Based on discussion with IBM research staff

and VIO fabrication processes are proven to be robust as evidenced by the $\geq 80\%$ physical yield from planar and VIO Surface-7 devices. To complement our scaling efforts towards wafer-scale fabrication of Surface-17 devices, we developed a home-built AOI called `pyclq:JJ` tailored for analysing the critical dimensions of Josephson junctions from SEM micrographs, specifically x-type JJs due to their simple geometry. The success of all-optical metrology for automating the inspection of airbridges will certainly aid future efforts in wafer-scale fabrication of SQPs.

In spite of fabricating multiple Surface-7 devices under nominally identical fabrication conditions described in Chapter 4, both the compounded yield of SQPs factoring in all the yield metrics and the batch-to-batch reproducibility of the devices fall short of the target values. We uncover an important source of spatial variation in the effective overlap area of junctions due to the geometric limitations of multi-angle evaporation of JJs without a resist bridge as the shadowing mechanism. This observation has far-reaching implications; firstly bridgeless junctions are intrinsically unsuitable for wafer-scale fabrication and require pre-compensation of the designed patterns to nullify the resist-shadowing effect. Secondly, it calls into focus the need to engineer the resist stack height H depending on the range of patterned JJ widths W and the desired tolerance for centre-to-edge variation in conductance.

Moving onto the comparison of cryogenic vs. RT measurements of qubit frequencies in Surface-7 devices, the device *Chimera v2* checks the boxes in terms of 100% die yield and above-average coherence times. However, the suboptimal design choices in the fabrication of JJs resulted in decreased detunings of all qubit pairs associated with qubit D2, which leads to a sizeable ZZ interaction. The increased surface roughness observed in other dies fabricated on Si(100) substrates could be attributed to the poor resilience of sputtered SiO_2 inorganic mask when treated in RCA-1 solution compared to HSQ. We observe the formation of triangular pitted defects from the AFM scans on Si(111) substrates after treatment with RCA-1 solution (AFM scans not shown in this work), as a result of which further iterations using this substrate was discontinued.

4.5. FABRICATION YIELD METRICS: SUPPLEMENTARY INFORMATION

4.5.1. JJ FAILURE MODES

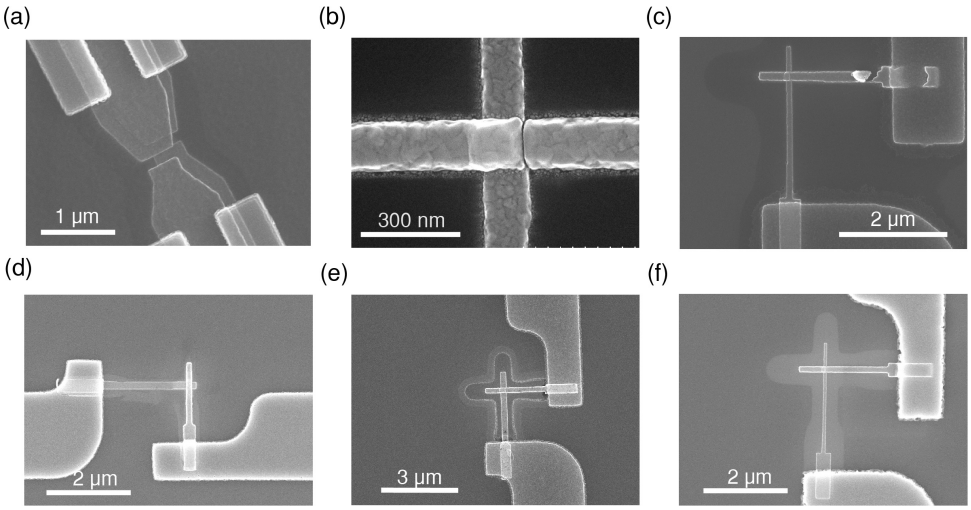


Figure 4.12: Possible failure modes in fabrication of JJs which lead to half-open or fully open junctions (a) In i-type JJs, the primary cause of open junctions are due to non-overlap of the electrodes, this may occur due to reduced thickness of the botto resist. (b) Zoom-in of an x-type junction reveals a crack on the top electrode as it intersects the bottom electrode, which in this instance lead to an open junction. The appearance of this crack does not always lead to failure. (c) Random breaks along the electrode arm, in this case an x-type JJ can also cause open junctions. (d) In the instance of non-symmetric overlap between the top and bottom electrodes, a significant decrease in conductance has been observed. (e) This is an instance where the JJ failure is attributed to build-up of resist contaminants observed as dark spots near the JJ contact pads. The device was developed nearly two weeks after e-beam patterning which likely led to the build-up of contaminants. (f) This is a random instance of JJ failure which is most likely caused by insufficient plasma descumming, evident from the whitish halo surrounding the junction.

4.5.2. AIRBRIDGE FAILURE MODES

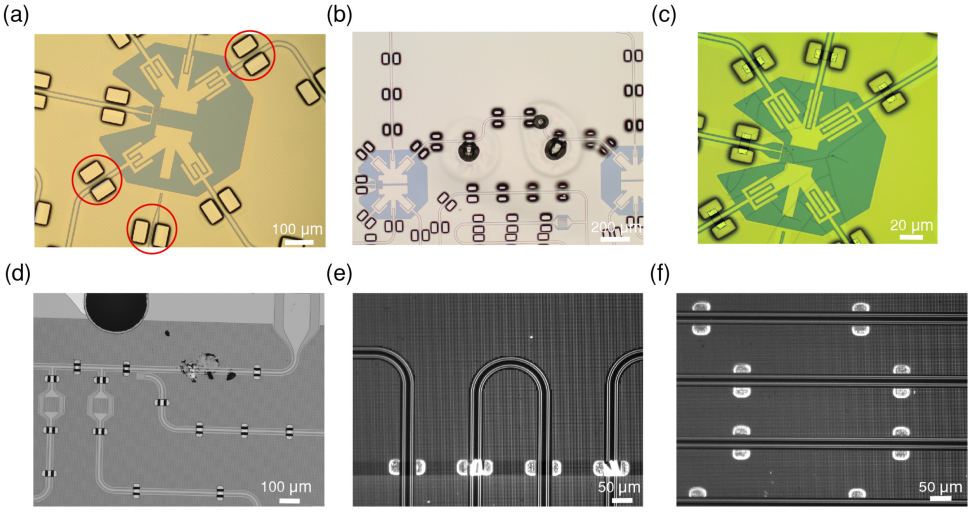


Figure 4.13: Different factors which have been identified to contribute to defective airbridges are (a) Misalignment of the PMGI contact pads highlighted by red circles, increasing the risk of shorting multiple transmission lines if proceeding with PMMA airbridge fabrication. (b) Introduction of bubbles in the thick PMGI resist which distorts the patterns. (c) Formation of cracks on spinning PMMA/MMA resist stack after reflowing at 200 °C. Examples of defective airbridges leading to (d) shorting of a TL (e) Partial deformation of the 3D structure (f) Total break of the 3D structures.

4.5.3. PYCLQ:AB ADDITIONAL INFORMATION

The calculation of confidence interval for airbridge quality is done using the method **cv2.TM_CCOEFF_NORMED** [7].

$$R(x,y) = \frac{\sum_{x',y'} \left(T'\left(x',y'\right) \cdot I'\left(x+x',y+y'\right)\right)}{\sqrt{\sum_{x',y'} T'\left(x',y'\right)^2 \cdot \sum_{x',y'} I'\left(x+x',y+y'\right)^2}} \tag{4.8}$$

where,

$$T'\left(x',y'\right) = T\left(x',y'\right) - 1/(w \cdot h) \cdot \sum_{x'',y''} T\left(x'',y''\right)$$

$$I'\left(x+x',y+y'\right) = I\left(x+x',y+y'\right) - 1/(w \cdot h) \cdot \sum_{x'',y''} I\left(x+x'',y+y''\right)$$

w and h are the width and height of the template, x', y' and x'', y'' are the relative

[7] OpenCV Object detection documentation: https://docs.opencv.org/4.x/df/dfbgroup__imgproc__object.html

locations of the pixels from the template on the image. x', y' are independent from x'', y''. T' and I' are normalized at every location to reduce the effect of variations in illumination of the chip in the APS-TASQ setup from run-to-run. Additionally, it highlights breaks or deformities in each individual airbridge due to the differences in optical contrast. Usually the source image consists of multiple airbridges, the averaged airbridge template slides over a patch of the source image. This results in a grayscale image, where the pixels which correspond best to the location of the template shows the highest confidence value, as shown in Fig. 4.14.

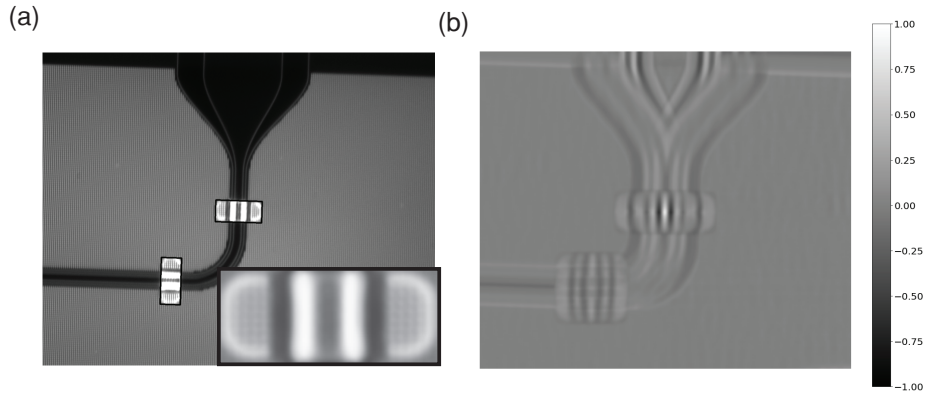


Figure 4.14: Example of a template matching instance from a source image containing two airbridges. (a) The APS-TASQ setup is centred on the horizontal airbridge in this case. The horizontal airbridge is template matched with a higher confidence value in (b) due to the addition of the orientation in the input airbridge coordinate file.

4.5.4. Resist-shadowing model additional data

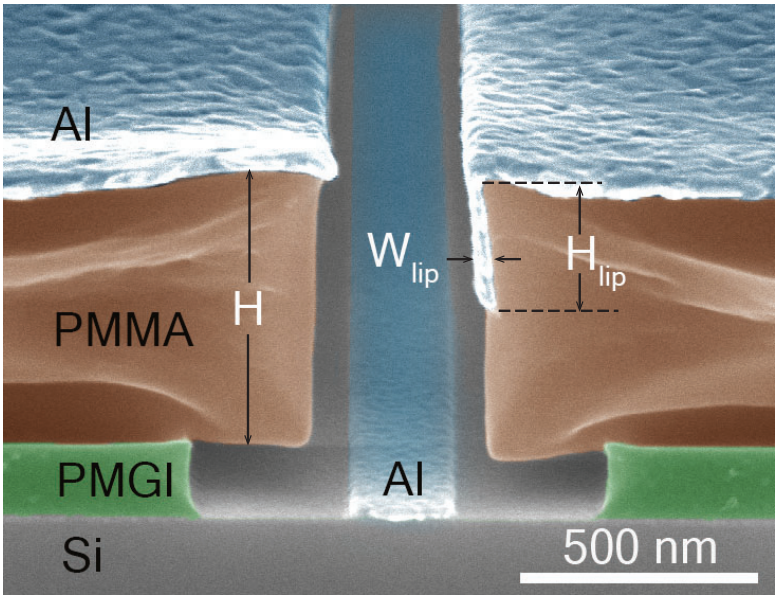


Figure 4.15: Cross-sectional SEM image of the resist stack of Manhattan JJs, with added false colour to highlight different materials. The cut shown corresponds to the horizontal electrode of a Manhattan JJ near wafer centre. The wafer is cleaved after deposition and lift-off of $20\ \mathrm{nm}$ of Al for both bottom and top electrodes at $\theta = 35°$. The Al thickness is intentionally reduced to minimize buckling of the resist stack. This image is taken at $76°$ tilt, using low beam current $(10\ \mathrm{A})$ and accelerating voltage $(5\ \mathrm{kV})$ to minimize distortion of the resist stack. The large undercut for the PMGI layer is created by the higher dissolution rate of PMGI during development using MF-321, which is based on tetramethyl ammonium hydroxide.

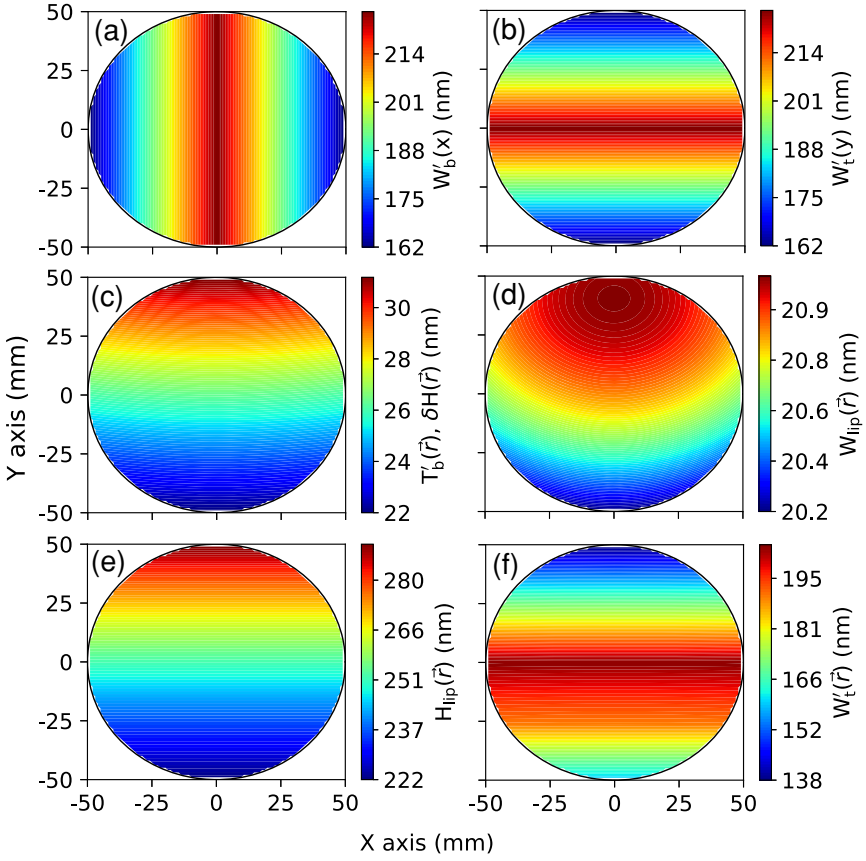


Figure 4.16: Contour plots of spatially dependent variables of the geometric model. (a) Actual bottom electrode width $W'_b(x)$ as per equation 4.2. (b) Actual top electrode width $W'_t(y)$ as per equation 4.2. (c) Actual bottom electrode thickness $T'_b(\vec{r})$ as per equation 4.3. (d) Lip thickness $W_{lip}(\vec{r})$ as per equation 4.5 (see Fig. 4.15 for reference). (e) Lip height $H_{lip}(\vec{r})$ as per equation 4.6 (see Fig. 4.15 for reference). (f) Actual top electrode width $W'_t(\vec{r})$ as per equation 4.7.

4.5.5. Dry vs. wet etch S_a comparison

AFM measurements of Si surfaces performed using Bruker AFM Dimension FastScan system with Scanasyst-Air AFM probes[8] either post end of fabrication or after cryogenic characterization to extract S_a. See Table 4.3 for all the S_a measurements.

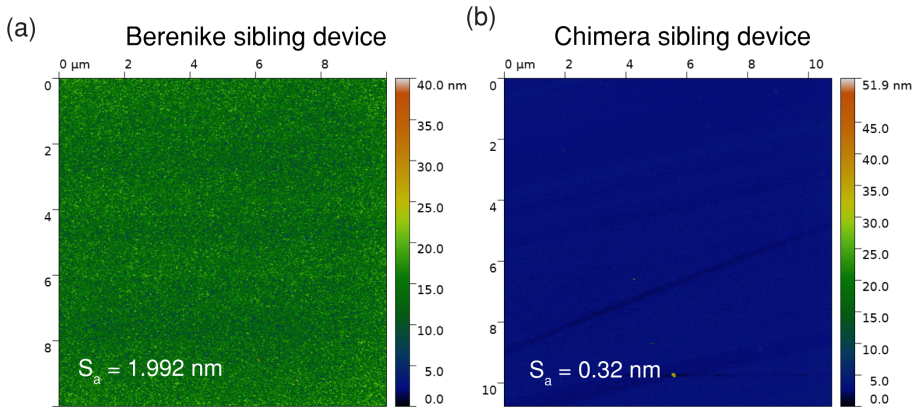


Figure 4.17: AFM scans from sibling devices of (a) *Berenike δ v2* which is patterned by full dry etch. (b) *Chimera v2* which is the first Surface-7 device patterned using partial dry + wet etch, with the lowest S_a of all Surface-7 devices computed from the entire scan region.

4.5.6. Extended fabrication information for Surface-7 devices

Table 4.3 summarizes additional relevant fabrication details for the characterized Surface-7 devices. The column **Fabrication timeline** lists the date of fabrication end-of-line (EOl) and CD-1 refers to the date of first cooldown of the device. The **Film details** column specifies the NbTiN film ID and film resistivity (ρ) calculated from 4-wire sheet resistance and thickness of the deposited film. The column **Etch method** details the base layer etching method, composition of inorganic mask used for wet etching along with the measured S_a from AFM measurements. The input E_c and M used for calculating $f_{q,pred}$ in Fig. 4.8 are listed in columns 5 and 6. In column 7, the Q_i of witness resonators (Hanger H1 (H2) on Feedline 1 (2)), with designed $Q_e = 10^5$ are characterized in the single photon regime ($n_{ph} \sim 1$).

[8] Refer to https://www.brukerafmprobes.com/p-3726-scanasyst-air.aspx for tip specifications.

Device	Fabrication timeline	Film details	Etch method	E_c, init (MHz)	M init (GHz/mS)	$Q_\mathrm{i} \times 10^3$
W33b VIO	···	WDS33 Si(100), ρ= 111.5 µΩ cm	Dry etch, S_a = ···	$Q_L = Q_M = Q_L = 280$	144	···
Blossom X v1	EOL: May 28 2019, CD-1: June 7 2019	WS4 Si(100), ρ= 106.9 µΩ cm	Dry etch, S_a = 1.67 nm	$Q_L = 305$; $Q_M^1 = 313$; $Q_M^2 = 327$; $Q_H = 343$	140	H2=430
Blossom Y v1	EOL: May 28 2019, CD-1: June 7 2019	WS4 Si(100)	Dry etch, S_a = ···	$Q_L = 305$; $Q_M^1 = 313$; $Q_M^2 = 327$; $Q_H = 343$	140	···
Andromeda X v1	EOL: May 20 2019, CD-1: June 19 2019	WS3 Si(100), ρ= 80.7 µΩ cm	Dry etch, S_a = ···	$Q_L = 305$; $Q_M^1 = 313$; $Q_M^2 = 327$; $Q_H = 343$	140	H1=38
Chimera v2	EOL: July 14 2019, CD-1: July 16 2019	WS4 Si(100)	Wet etch HSQ mask, S_a = 0.32 nm	$Q_L = Q_M = Q_H = 300$	140	H2=1100
Berenike δ v2	EOL: July 15, 2019, CD-1: July 16 2019	WS3 Si(100)	Dry etch, S_a = 2.0 nm	$Q_L = Q_M = Q_H = 300$	140	···
Kratos σ v2	EOL: Aug 2 2019, CD-1:Aug 6 2019	WDS-1 Si(111), ρ= 93.3 µΩ cm	Wet etch SiO_2 mask, S_a = ···	$Q_L = Q_M = Q_H = 300$	140	H1=528, H2=368
Kratos π v2	EOL: Aug 2 2019, CD-1: Aug 6 2019	WDS-1 Si(111)	Wet etch SiO_2 mask, S_a = ···	$Q_L = Q_M = Q_H = 300$	140	H2 $\sim$ 300
Snowleopard B v3	EOL: Oct 14 2019, CD-1: Oct 17 2019	WS6 Si(100), ρ= 94.6 µΩ cm	Wet etch SiO_2 mask, S_a = 0.57 nm	$Q_L = Q_M = Q_H = 300$	137	H2 $\sim$ 344
Sifaka B v3	EOL: Oct 14 2019, CD-1: Oct 17 2019	WS6 Si(100)	Wet etch SiO_2 mask, S_a = 0.7 nm	$Q_L = Q_M = Q_H = 300$	137	···
Vaquita T v3 (Starmon-5)	EOL: Nov 25 2019, CD-1: Jan 9 2020	WS6 Si(100)	Wet etch SiO_2 mask, S_a=0.59 nm	$Q_L = Q_M = Q_H = 300$	137	···

Table 4.3: Additional fabrication details of Surface-7 devices.

5

WAFER-SCALE UNIFORMITY OF JOSEPHSON JUNCTIONS

In this chapter we investigate die-level and wafer-scale uniformity of i-type (Dolan-bridge) and bridgeless x-type (Manhattan-style) Josephson junctions, using multiple wafers with and without through-silicon vias (TSVs). The spread in JJ conductance is quantified at both die- and wafer-level by the coefficient of variation (CV) of conductance and residual standard deviation (RSD) of the predicted qubit frequency $f_{\mathrm{q,pred}}$. From multi-wafer studies, it is observed that i-type junctions fabricated on planar substrates have the highest yield and lowest room-temperature conductance spread, with a die-level RSD of $\sim 80\,\mathrm{MHz}$. In TSV-integrated substrates, x-type junctions outperforms i-type JJs both in terms of yield and conductance spread, however the lowest die-level RSD $\sim 250\,\mathrm{MHz}$ achievable is not compatible with the 50-MHz margin desired in real-world SQPs. To further validate the resist-shadowing effect, we acquire SEM micrographs of x-type JJs fabricated on wafers with different metallization layers namely bare Si, NbTiN and TiN. We uncover another contribution to spatial dependence in JJ conductance variations due to a net contact resistance between the Al/NbTiN interface which also increases from centre-to-edge due to the thickness non-uniformity of our sputtered NbTiN films on 100 mm wafers with both SuperAJA and Nordiko sputtering tools. [1].

[1] Parts of this chapter are published in [227]

5.1. IN SEARCH OF THE PERFECT JUNCTION

An important limitation to qubit frequency targeting is variability in the fabrication of Al/AlO_x/Al JJs, which most commonly relies on double-angle shadow evaporation with intermediate in-situ oxidation (Described in Subsection 4.2.2). The JJ fabrication variables affecting the E_J are the overlap area between the two Al electrodes and the tunnel barrier thickness. The two most popular JJ fabrication variants differ only in the shadowing mechanism: Dolan-bridge [226] use a suspended resist bridge whereas Manhattan-style or x-type [228] junctions do not. Since Dolan-bridge JJs are more sensitive to resist-height variation by design, bridgeless Manhattan JJs are a pragmatic choice at the outset, particularly on substrates with TSVs that compromise the uniformity of spin-coated resist. The work by Kreikebaum et al. [221] demonstrating wafer-scale relative standard deviation (RSD) of critical current $< 3.5\%$ using single JJs and asymmetric SQUID fabricated on high-resistivity Si wafers is a emphatic affirmation for transitioning towards Manhattan-style junctions. However, merits of continuing with Dolan-bridge junctions, which is more established in the field is highlighted by the work of Foroozani et al. [274] showcasing the ability to pattern junctions solely using 193 nm photolithography. This work showcases a path towards scalability of fabrication of Josephson junctions at the 300-mm wafer level. In this work, we perform a systematic experimental investigation comparing the uniformity of Dolan-bridge and Manhattan-style JJs, henceforth referred to as i-type and x-type respectively, at both die- and wafer-scale on 100-mm bare Si wafers, metallized wafers and finally on metallized TSV-integrated wafers. We benchmark uniformity using RT conductance measurements, extracting the coefficient of variation (CV) of RT-measured G and residual standard deviation (RSD) of predicted transmon frequency. A wafer-center-to-edge variation is observed particularly in x-type junctions, which we attribute to a geometric shadowing effect during electrode evaporation. Scanning electron microscopy (SEM) of many junctions supports the resist-shadowing geometric model, and further points to remnant spatial dependence possibly due to contact resistance between the JJs and the metal bays as a result of the non-ideal interface between the Al electrodes and the oxidized wiring layer. Our findings indicate that for our current fabrication processes, i-type perform best for planar substrates, while the opposite holds for TSV-integrated substrates. We identify several paths for further required improvement.

5.1.1. FIRST EVIDENCE OF RESIST-SHADOWING EFFECT

The near-doubling of die size when scaling from the 7-qubit Surface-7 to 17-qubit Surface-17 SQP (See Chapter 4) begins to limit optimal usage of 100 mm NbTiN-metallized wafers due to the non-uniformity of the film thickness (Refer to Subsection 3.3.2). The transition from die-level to wafer-scale fabrication of JJs began after installation of the automated wafer-scale multi-angle evaporator (Plassys MEB 550S) around early 2020. The first trial of wafer-scale fabrication is carried out on a $70 \times 70\ \mathrm{mm}^2$ NbTiN-metallized TSV-integrated wafer patterned with eight Surface-17

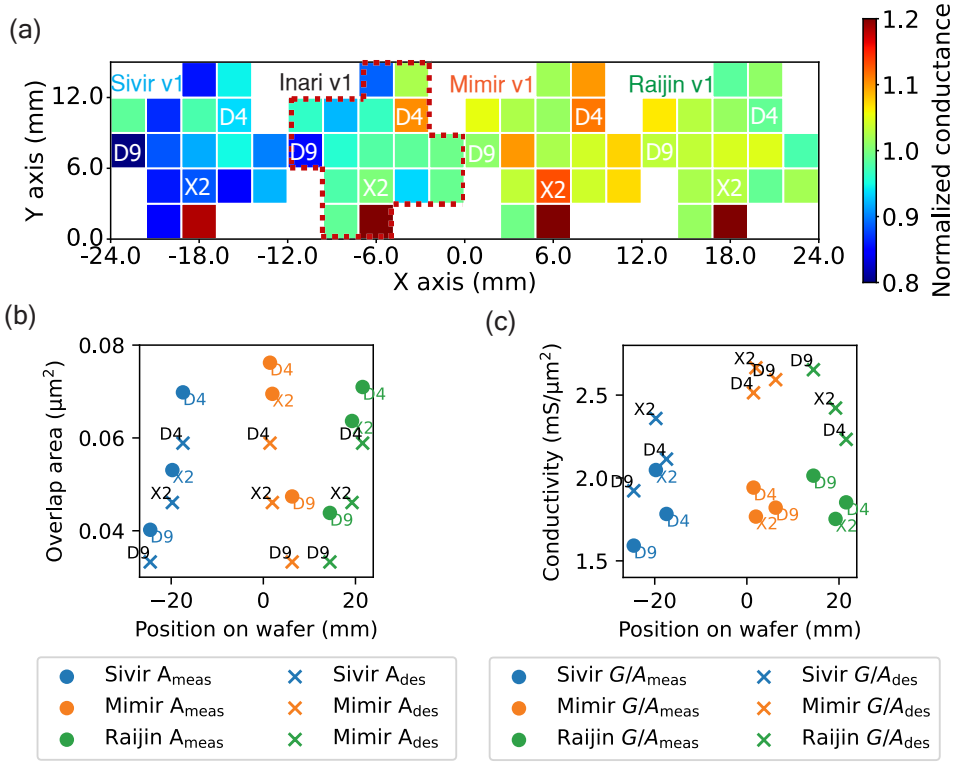


Figure 5.1: (a) Normalized heatmap of RT-predicted G of four Surface-17 repeats with x-type JJ pairs fabricated on a 70×70 mm^2 TSV-integrated wafer. Qubit D3 at the bottom right of all the device repeats was wrongly assigned the designed JJ width of Q_H. SEM micrographs of x-type JJ pairs in qubits D9, X2 and D4 from dies Sivir v1, Mimir v1 and Raijin v1 are acquired.(b) Plot of summed measured and designed overlap areas extracted from the labelled qubits in (a) as a function of relative position of the qubit from the wafer centre. (c) Plot of area-normalized conductivity calculated from summed measured and designed overlap area as a function of relative qubit position.

repeats incorporating grounding TSVs but are connectorized by lateral wirebonding. A layout of this wafer is shown in Fig. 5.6, fabricated using the VIO process flow excluding the backside patterning steps. Due to defects on the base layer, only 4 Surface-17 repeats are patterned with JJs. The nominal widths of the bottom electrode patterned for each frequency group are Q_L= 104 nm, Q_M= 144 nm and Q_H= 184 nm, with a fixed top electrode width 160 nm. The RT G is acquired after JJ deposition, shown as a normalized conductance (G/μ_G) heatmap in Fig. **??**(a) according to the procedure described in Section 5.3. Except for a design error in qubit D3 of the layout resulting in a significantly higher G/μ_G, we obtain 100% physical

yield of JJs. A closer look at the distribution of normalized conductance however, shows a centre-to-edge dependence. To investigate the cause, SEM micrographs of 3 qubits from each repeat namely, D9, X2 and D4 are acquired. The device Inari v1, marked by red dotted lines is cryogenically characterized, therefore no SEM images of JJs are acquired from this device. The measured overlap area plotted in Fig. 5.1(b) is the sum of overlap areas extracted from each JJ in the SQUID loop using ImageJ.[2]. The designed overlap area is calculated as $2W_bW_t$ (Note: this only applies to x-type JJs). Additionally the JJ conductivity is calculated by normalizing conductance with the summed designed and measured overlap area shown in Fig. 5.1(c). It can be observed that the measured overlap area for all the three qubits is highest at the wafer centre. The conductivity calculated from measured overlap area consequently is lower than the value calculated from designed area for all imaged junctions. This dataset, although limited in terms of statistics, is key to formulating further wafer-scale experiments to understand the systematic centre-to-edge variation in electrode dimensions and conductivity elaborated in Section 5.5.

5.2. WAFERSCALE FABRICATION: DESIGN OF EXPERIMENTS

The initial observation of a centre-to-edge variation in RT-measured G from the first wafer-scale JJ deposition described above requires further scrutiny, as we started off with a rather complex wafer layout with many fabrication variables. We investigate the uniformity and reproducibility of i-type and x-type JJs through a multi-wafer study using 100-mm diameter high-resistivity Si wafers. For each junction type, the experiments are performed both at die- and wafer-level. Due to run-to-run variations generally encountered with fabrication of JJs, we sequentially increase the complexity of the wafer-scale tests described as follows:

- Simplify JJ fabrication with a one-step ebeam lithography for writing junctions directly coupled to a contact pad on **bare Si wafers**.
- Pattern **single JJs** with a fixed designed JJ overlap (A_{overlap}) in an upright square lattice throughout the bare Si wafer.
- Transition to **metallized wafers** patterned with a square lattice of test structures for symmetric JJ pairs with a fixed A_{overlap}.
- Design A_{overlap} sweeps of JJ pairs in a **copy-paste lattice** across the metallized wafer.
- Converge to wafer-scale fab with multiple A_{overlap} sweeps of JJ pairs on **TSV-integrated wafers**.

[2]This exercise prompted the development of `pyclq-JJ` module to automate image analysis for extracting JJ overlap area described in Subsection 4.1.2

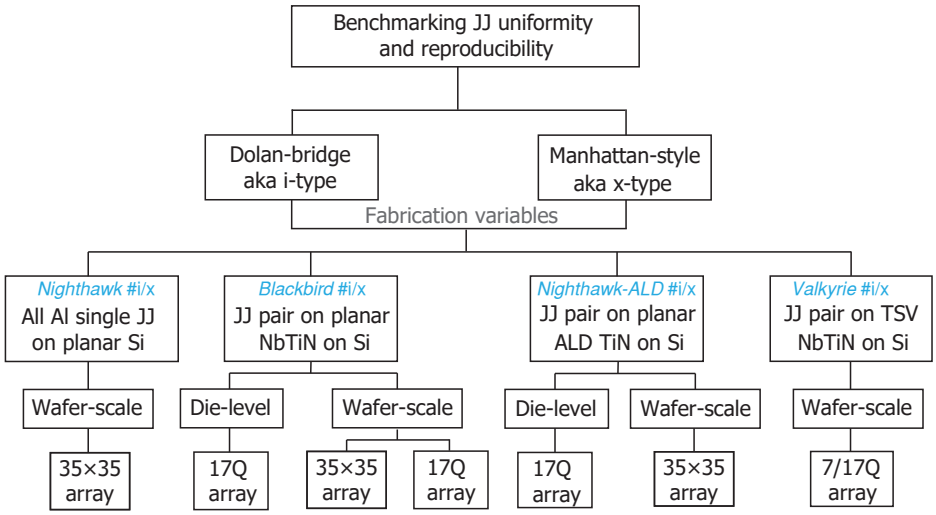


Figure 5.2: Schematic of design of experiments developed for comparing i-type (Dolan-bridge) and x-type (Manhattan-style) JJs by RT G measurements. Wafer-scale experiments are performed on planar bare Si, NbTiN- and TiN-metallized and on NbTiN-metallized TSV-integrated wafers employing both 35×35 array and 17Q array layouts. Die-level experiments are carried out using only the 17Q array layout by cleaving the wafer into 13×13 mm^2 dies prior to JJ deposition.

Depending on the mix of variables, the wafers are distinguished by a unique name series with the experimental iteration number and the JJ type (i/x). Bare Si wafers with single JJs are labelled as *Nighthawk* (# i/x), metallized wafers are labelled as *Blackbird* (# i/x) and TSV-integrated wafers are labelled as *Valkyrie* (# i/x). An exception applies to one set of wafers metallized with TiN deposited by ALD, which are labelled as *Nighthawk-ALD* (# i/x), explained later in this section. A schematic overview of the experimental variables which are tested to disentangle the various contributions towards the spread in RT G measurements is shown in Fig. 5.2.

WAFERSCALE FABRICATION: MATERIALS AND METHODS

Bare Si wafers are directly used after cleaning with acetone and IPA for patterning single junctions along with contact pads in a single e-beam lithography step as shown in Fig. 5.4, which are henceforth called 'All Al' junctions. We fabricate a total of 12 wafers with all Al JJs. Three wafers metallized with 200 nm NbTiN are used for this experiment, using either SuperAJA or the Nordiko system to deposit the film as per the procedure described in Subsection 3.3.2). The film sheet resistance measured using the 4-point method is in the range $0.95 - 1.15\ \Omega/\square$ and the decrease in film thickness from centre to edge is ~ 25 nm for films from both systems. Two TiN wafers of film thickness ~ 160 nm are deposited by ALD using 1900 cycles of TDMAT

precursor at $300^{\circ}\mathrm{C}$ using the Veeco Fiji V2 system. The measured sheet resistance of ALD TiN film is in the range of $1.21 - 1.36\ \Omega/\square$. Note that the JJ test structures on the metallized wafers incorporate symmetric JJ test pairs in a SQUID loop, which mimic the two-junction transmon used in our standard SQPs as shown in Fig. 5.3. The base layer is defined for all metallized wafers by partial dry + wet etching using HSQ as the inorganic mask which is cured by a post-spin bake at 300 °C. For the *Valkyrie* sample series, we skip the TSV sidewall metallization step with TiN. Post TSV integration, the wafers are cleaved at the edges resulting in a $70 \times 70\ \mathrm{mm}^2$ square wafer. To facilitate uniform dispensing of e-beam resist, a custom chuck made of stainless steel is used to hold the square TSV-integrated wafer in place during spinning, in place of standard vacuum chucking. The precise alignment of the base layer with respect to the TSV locations on the wafer is important in order to ensure 100% yield of the JJ test structures. This is done at the e-beam lithography system using predefined markers from the DRIE step. The JJ fabrication recipes for i-type and x-type junctions are kept constant across all the substrates and layouts, as described in Section 3.3.5, unless otherwise specified. All the JJ depositions are terminated with a capping oxidation step.

5

WAFERSCALE FABRICATION: PLANAR AND TSV WAFER LAYOUTS

The 35×35 **array** is a wafer-scale layout which is a simple square lattice containing either 1225 or 4900 $(4 \times 35 \times 35)$ JJ test structures spanning $70 \times 70\ \mathrm{mm}^2$, shown in Fig. 5.4(a). In the *Nighthawk* series, the bare Si wafers are patterned with single JJs, which are written in a single e-beam writing step along with the $100 \times 100\ \mu\mathrm{m}^2$ Al probing pads, as in Fig. 5.4(b,c). All the junctions are designed with a single nominal JJ $W_\mathrm{b} = W_\mathrm{t} = 200\ \mathrm{nm}$ for x-type JJs, whereas for i-type JJs, the top electrode length is $150\ \mathrm{nm}$ and $W_\mathrm{t} = 200\ \mathrm{nm}$. A disadvantage of this pattern is the spurious deposition of Al on both probing pads, however we neglect any contributions from it. A total of eight wafers with x-type JJs and one with i-type JJs are fabricated in the *Nighthawk* series. The same JJ design principle is applied for the metallized 35×35 array wafers, with one wafer for each JJ variant fabricated on NbTiN-metallized substrates (*Blackbird 4x* & *Blackbird 5i*) and a single ALD TiN-coated wafer with x-type junctions (*Nighthawk-ALD 3x*). The purpose of the TiN-metallized wafers is to dissect the impact of the non-uniformity of sputtered NbTiN films on JJ conductance by replacing NbTiN with a conformal base layer deposited using ALD, with $\sim \pm 5\ \mathrm{nm}$ variations in film thickness from centre to edge of the wafer acquired from AFM measurements.

In the **Planar 17Q array** layout, a 13×13 mm die-level layout mimicking Surface-17 [36, 252, 275] is copy-pasted into two 2×4 arrays, the top (bottom) array with i-type (x-type) test structures. One wafer *Blackbird 2* with both JJ test pads is made, shown in Fig. 5.5(c). At the location of each transmon of the SQP, we place a sub-array of 4×4 test structures. Within each sub-array (Fig. 5.5(a,b)), the designed single-junction overlap area (A_overlap) is finely stepped within one of three ranges, labelled low (l), mid (m) and high (h), mimicking the choice of three qubit-frequency groups in our SQPs [24, 36, 252, 275]. For i-type JJs, we change A_overlap by varying the width W_t of the top electrode and keeping the width of the bottom electrode

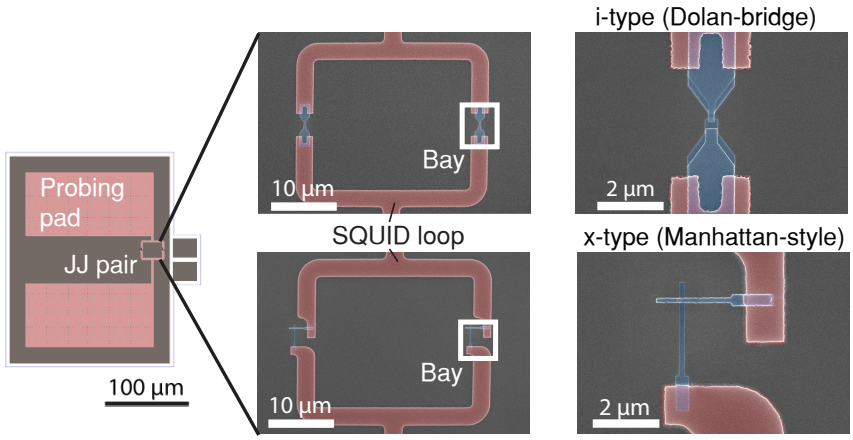


Figure 5.3: Coloured CAD layout and SEM images at two length scales of the test structures used to investigate uniformity of i-type versus x-type JJ pairs on NbTiN metallized planar and TSV-integrated wafers as well as ALD TiN metallized planar wafers. Two junctions in each structure (blue) complete a loop with a pre-fabricated metal base (red) which connect to probing pads for measuring the parallel conductance of the junction pair.

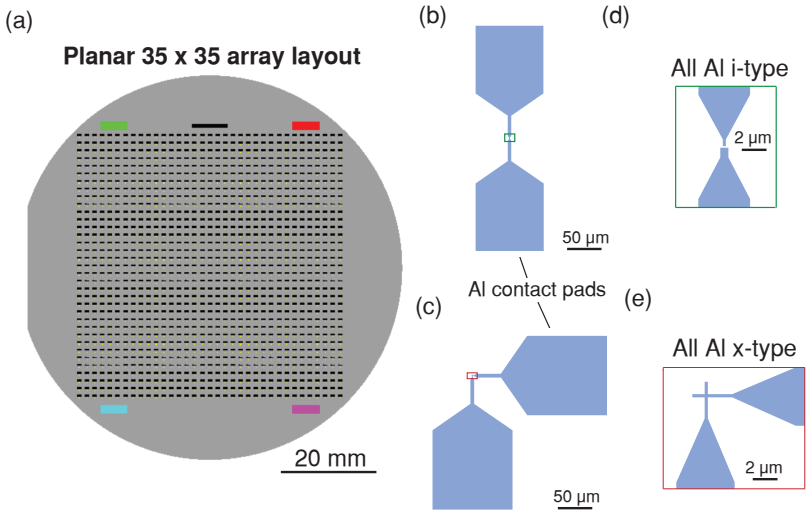


Figure 5.4: (a) Wafer-scale layout of the 35×35 array, common for both planar Si and metallized wafers. Coloured CAD layout of (b) all Al i-type and (c) all Al x-type JJs. (d, e) Zoom-in of the all Al JJ variants.

$W_b = 3W_t$. For x-type structures, we instead vary W_b and fix $W_t = 160$ nm. In total, the wafer contains 2176 test structures of each JJ variant. We first fabricate only the x-type JJs on the bottom half of the wafer and perform all conductance measurements on them. We subsequently fabricate and measure all i-type JJs on the top half of the wafer. **Die-level samples** are made with identical fabrication steps to the wafer-scale equivalent, the only difference is that the repeats are diced prior to depositing junctions. Each planar 17Q die has a unique identifier with the wafer series name (in this case, *Blackbird*), JJ type and an additional positional identifier with the columns marked 1-4 from left to right of the wafer centre and rows marked as either **c** denoting centre and **e** from top to bottom of the wafer as shown in Fig. 5.5(c). We fabricate a total of 8 die-level samples using the Planar 17Q layout for each JJ variant from a NbTiN/Si wafer *Blackbird 1* and an ALD TiN/Si *Nighthawk-ALD 2*[3].

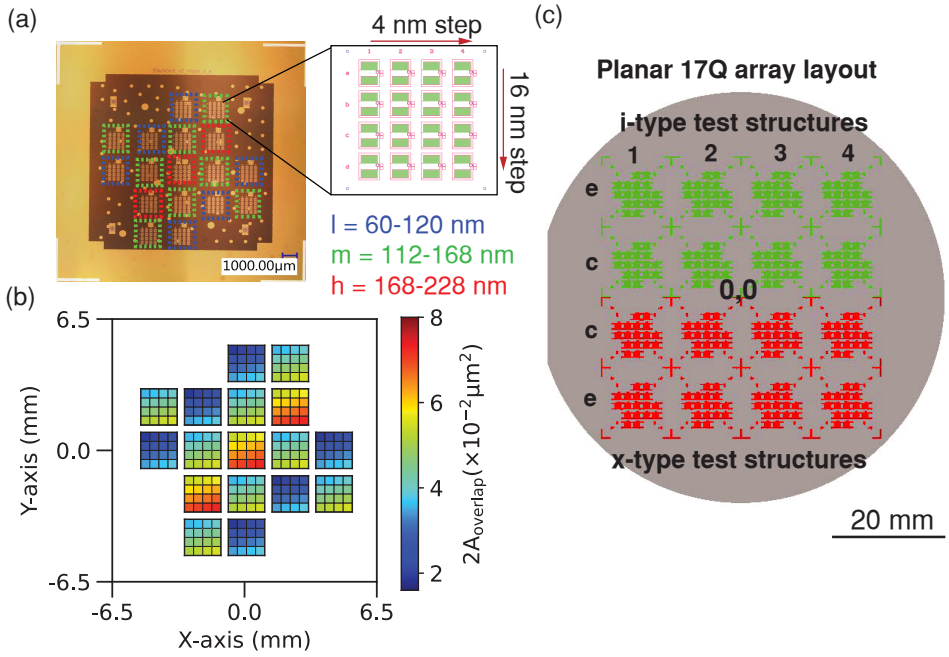


Figure 5.5: (a) Optical image of Planar 17Q array layout, mimicking a Surface-17 device in terms of placement of the 4×4 subset of JJ test structures, shown by the inset. (b) Equivalent heatmap of designed overlap area (A_{overlap}), where the JJ width in each array is swept in one of three ranges labelled l, m and h. (c) Wafer-scale layout of the Planar 17Q array, with i-type test pads at the top half and x-type test pads at the bottom half.

[3]These test devices are used for experiments detailed in Section 6.5

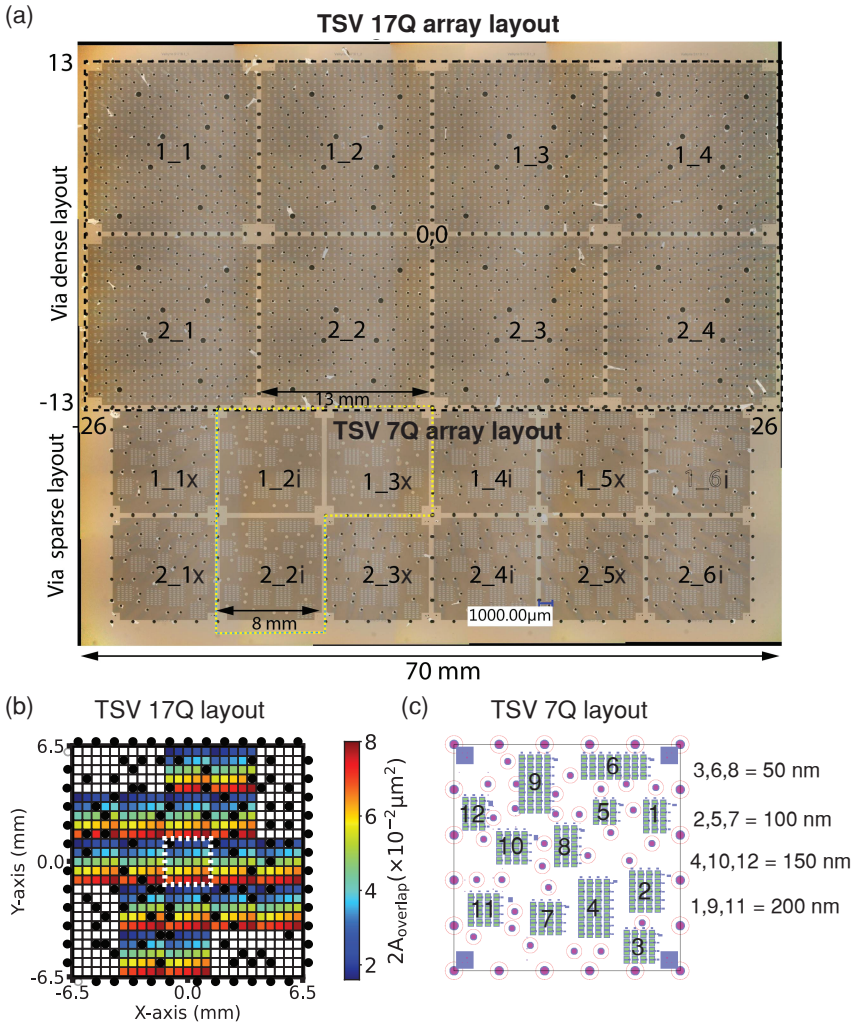


Figure 5.6: (a) Stitched optical image of the 70×70 mm^2 NbTiN -metallized TSV-integrated wafer used for TSV 17Q (top) and 7Q (bottom) array layout for i-type and x-type JJs. The 7Q repeats highlighted by a yellow dotted line are devoid of TSVs. (b) Heatmap of A_{overlap} in a die-level TSV 17Q (via dense) layout arranged as 17 5×5 sub-arrays of junction test structures, indicated by the white dotted line. The dots correspond to via positions in the layout. (c) Coloured CAD snapshot of the TSV 7Q (via sparse) layout. Each numbered array is patterned with a single nominal JJ width.

For the **TSV 17Q array layout**, a separate wafer containing test structures of only one JJ variant is fabricated (*Valkyrie 2x, Valkyrie 3i*). In each wafer, the die-level

layout (copy-pasted into one 2×4 array) has TSVs placed at the same locations as a variant of Surface-17 with TSVs (Fig. 5.6). The density ($\sim 1.7\%$ area coverage) and position of TSVs in the via dense layout is chosen to push the lowest-frequency spurious modes of the SQP in its sample holder to $\gtrsim 15$ GHz (as per finite-element simulation). At the location of each transmon in the SQP, we place a 5×5 sub-array of test structures. In this case, all sub-arrays are identical. Importantly, test structures overlapping with TSVs, although fabricated, are ignored and not included in conductance measurements. This yields at most 378 viable test structures per die and thus 3024 per wafer. The **TSV 7Q array** has the same form factor as a Surface-7 device, containing 12 JJ test pad islands, similar to the planar 17Q layout with fixed designed JJ widths in each island (Fig. 5.6(c)). The odd-numbered columns are patterned with x-type test pads whereas the even-numbered ones contain i-type pads. Additionally, we omit vias in the photolithography mask on three dies highlighted by the yellow dotted line for side-by-side comparison of the JJ conductance on dies with and without TSVs.

5

5.3. RT CONDUCTANCE MEASUREMENTS AND ANALYSIS

All G measurements are acquired by the 2-point method using a home-built transimpedance amplifier. A low input voltage $(10\ \mathrm{mV})$ is applied across the junctions to minimize the possibility of causing failure to open or short circuit. Measurements on all planar wafers are performed using a manual probe station, with one exception noted below. During manual measurements, the intensity from a light-emitting diode source is set to the lowest possible visibility $(< 500\,\mathrm{lx})$ to minimize the parallel conductance contribution from the Si substrate to $\sim 5\ \mu\mathrm{S}$. Measurements on the TSV 17Q wafers as well as on the Planar 35×35 TiN wafer are performed using a home-built automated probe station. The measured series resistance contribution from external cabling is $< 10\ \Omega$. The series resistance of NbTiN probing pads was found to vary from $200\ \Omega$ at wafer center to $330\ \Omega$ at wafer edge by fabricating test structures with bays short-circuited directly in the base layer in *Blackbird 2*. This variation is attributed to the radial dependence of the thickness of the sputtered NbTiN films (resistivity $\rho = 100\ \mu\Omega\text{-cm}$).

Based on the junction geometries and expected variations in fabrication, as well as measured variations in series resistance of the wiring, the expected conductance range of both JJ types is $40 - 350\ \mu\mathrm{S}$. Values $< 20\ \mu\mathrm{S}$ and $> 500\ \mu\mathrm{S}$ are filtered out as they mostly correspond to open and shorted junctions respectively. To systematically detect and filter out data containing an open junction in a pair, a two-part linear regression analysis of conductance versus A_{overlap} is implemented within each die in the planar and TSV 17Q wafers. Values below 70% of the initial best fit are filtered out, the number of half-open JJs filtered are shown in Fig. 5.14 and 5.15. For the planar 35×35 array wafers containing nominally identical test structures throughout, conductance values below 70% of the mean are filtered out. The yield loss due to opens and shorts in each dataset is explained in the results section.

To quantify non-uniformity at both die and wafer scale, we use the conductance CV as a function of A_{overlap} and the RSD of predicted qubit frequency, denoted by σ_f.

For the sake of clarity, we specify whether the RSD is calculated at die-level or wafer-scale in plots and tables. Die-(wafer-) level conductance CV is calculated using all the test structures with identical A_{overlap} across the die (wafer) when calculating the mean conductance (μ_G) and standard deviation of conductance (σ_G). For the 35×35 layouts with nominally identical A_{overlap}, all the test structures are used to compute CV. For the 17Q planar and TSV layouts, the CV is compared as a function of A_{overlap}.

The spatial variation of junction conductance is visualized using heatmaps of conductance normalized by μ_G of all test structures with identical A_{overlap}. The predicted transmon qubit transition frequency (f_{01}) is calculated from G using Eq. 2.32 where $E_c/h = 270\ \text{MHz}$ and $M = 134\ \text{GHz/mS}$. For the case of 17Q planar and TSV layouts, die-level RSD is calculated from the residuals of the second fit. Wafer-level RSD is calculated similarly, but the residuals are obtained by performing a single fit on the combined filtered G data from all dies.

To test the geometric resist-shadowing model, SEM images of JJs from different coordinates on all Planar 35×35 wafers are acquired at $10^5\times$ magnification. SEM imaging is only performed after conductance measurements are completed. The actual deposited junction widths (W_b', W_t') and overlap area (A'_{overlap}) are extracted using our home-made image analysis software `pyclq` with the work flow described in Fig. 4.2. The presence of other sources of spatial non-uniformity is evidenced from the spatial dependence of effective JJ conductivity calculated as $G/\Sigma A'_{\text{overlap}}$.

5.4. WAFER-SCALE FABRICATION: RESULTS AND OBSERVATIONS

In practice, the path towards wafer-scale fabrication requires standardization of each process step and parameter to ensure batch-to-batch reproducibility, with a mutual benefit of improving the nanofabrication engineer's adeptness. Some of the common practices for all wafers are outlined below, with exceptions for each substrate or layout separately explained in each section. The wafers are loaded on dedicated 100-mm e-beam sample holders, available on both Raith EBPG 5000+ and 5200 systems. *Valkyrie* samples are loaded on either 3" mask plates or on 200-mm substrate holders. The wafers are developed by immersion and gentle agitation using borosilicate crystallizer beakers and dried using a wafer spinner. Plasma descumming using the Sentech Etchlab 200 system is done by placing the wafer at 0° azimuth with respect to the patterned features at the centre of the direct load, unless otherwise specified. This is followed by BOE strip using flat-bottom polytetrafluoroethylene (PTFE) beakers and tweezers. The wafer is thoroughly rinsed in DI H_2O and aligned on the sample holder of the Plassys evaporator. Using an alignment reference at the centre left of the holder, the wafer is mounted at 0°(180°) with respect to the holder for i-type (x-type) JJs. Rotational offsets of the wafer with respect to the sample holder are corrected by manual adjustment under an optical microscope, using the flat side of the sample holder as the reference. The sample holder is loaded upside down into the load lock using a dedicated holder mounting tool. The recipes are programmed for fully automatic execution of the deposition process, initiated after the process chamber is pumped down to the target pressure

range, usually between $2\text{–}4 \times 10^{-8}$ mbar. Prior to depositing Al, 20 nm of titanium is deposited to lower the process chamber pressure. The samples are lifted off in hot NMP bath by placing them upright using borosilicate envelopes, with intermittent gentle aspiration using glass pipettes. The measurements are acquired within 48 hours post deposition using the manual probe station or APS-TASQ setup.

5.4.1. SINGLE JJ STATISTICS ON BARE SI WAFERS

We firstly compare x-type and i-type JJs on planar bare Si wafers using the 35×35 array layout using the baseline JJ fabrication recipes (wafer IDs: *Nighthawk 2x* and *Nighthawk 1i*). The wafers are directly spun with the corresponding JJ resist stack and are aligned using 4-inch holders of Raith EBPG at the position relative to the holder's centre [4] using the the 4-inch wafer holder of Raith EBPG 5000+ system. The Al probing pads and JJ arms are written separately as a coarse and fine pattern with BSS = 60 nm and 10 nm respectively, resulting in a total writing time of ~ 3 hours 40 min. Except *Nighthawk 6x* (Refer to Fig.5.20), all the wafers are characterized using the manual probe station. From the all Al i-type wafer shown in Fig. 5.7(a), a G/μ_G gradient is discernible from left to right of the wafer, the cause of this behaviour in all Al i-type JJs is not examined in detail in this work, as only one wafer of this kind is studied. The corresponding histogram (Fig. 5.7(c)), shows a normal distribution of the conductance values, with the lowest σ_G of all the planar wafer-scale datasets. An analysis of the filtered outliers reveals 4 shorted and 2 open junctions, while the remainder are filtered as the G is lower than 70% of μ_G.

Moving on to x-type JJs on bare Si, the centre-to-edge variation of G/μ_G becomes evident (Fig. 5.7(b)), consequently the σ_G is 57% higher than the i-type equivalent. This indicates that the cause of this behaviour is likely due to the resist shadowing effect described in Subsection 4.2.2 which results in a systematic variation of the effective JJ overlap area (A'_{overlap}). We also acquire 32 SEM micrographs of JJs across *Nighthawk 2x* wafer in order to validate the resist-shadowing model, described in Section 5.5. In order to rule out other fabrication-induced sources of the centre-to-edge variation, we performed experiments by varying the O_2 descumming recipe, described in chapter SI 5.7.2. The computed $\text{CV} = 6.8\%$ from *Nighthawk 2x*, our best dataset from planar x-type JJs, is 2 times higher than the values reported for state-of-the-art wafer-scale spread of 3.5%. [221]. Barring the omitted rows of JJs in this dataset, analysis of filtered data reveals no shorted junctions and 29 open junctions, showing significantly higher yield loss than its i-type counterpart. However, the *Nighthawk 2x* wafer shows the highest yield among all x-type full-wafer datasets.

5.4.2. PLANAR 35 × 35 WAFER-SCALE STATISTICS

This set of experiments add a single layer of complexity, introduced by metallization of the Si wafer with sputtered NbTiN. The e-beam lithography step for JJ patterns is done by aligning it with respect to the pre-fabricated JJ test structures using marker

[4] Alignment reference 1|C|F|O: C; (<X,Y> [um]): 0,0

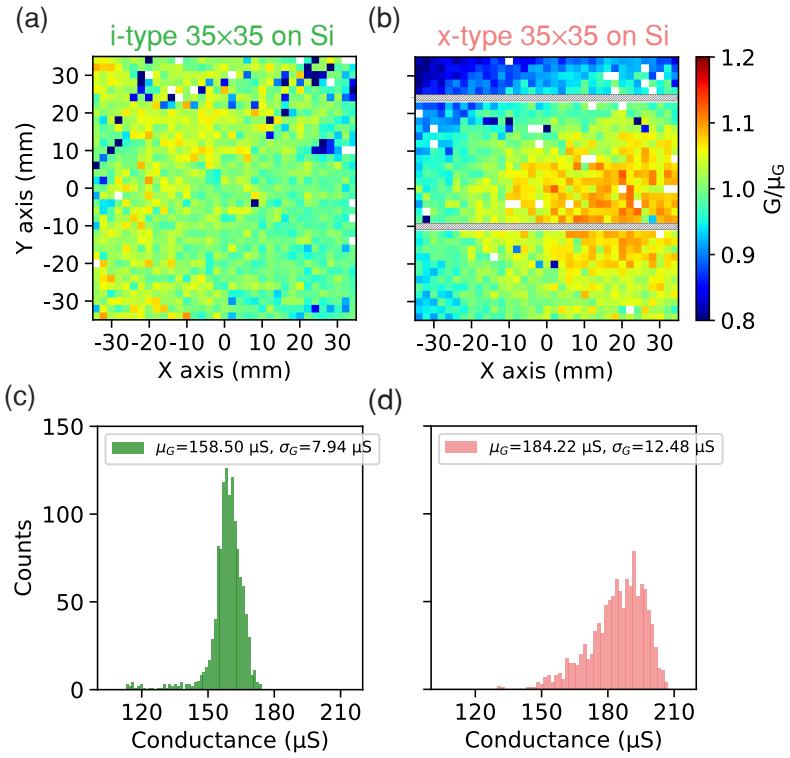


Figure 5.7: Normalized conductance heatmaps of (a) i-type single JJs on planar Si (wafer ID: *Nighthawk 1i*) (b) x-type single JJs on planar Si (wafer ID: *Nighthawk 2x*). Two rows are accidentally omitted during measurements, indicated by the hatched rows. (c,d) Conductance histograms of the corresponding wafers.

search [5]. Four sets of pattern markers are placed at each quadrant of the wafer in addition to the global markers located at the periphery of the array in order to ensure the JJ patterns do not drift across the wafer during writing. The only dataset obtained with i-type junctions on NbTiN shows an unexpected conductance gradient extending along the diagonal from top left to bottom right of the wafer (Fig. 5.8(a)). Upon SEM inspection, we find that that most of the JJs along the top left quadrant of the wafer are significantly shifted away from the bay without any difference in the JJ overlap area in spite of our marker search routine. This may partially explain the higher σ_G in this wafer (Fig. 5.8(c)) The centre-to-edge variation appears more prominent in the metallized version of the wafer as seen from Fig. 5.8(b). The spread is consequently nearly a factor 3x higher than i-type JJs on NbTiN-metallized wafer. The number of defective junctions due to shorts or opens are very low, with the *Blackbird 4x* wafer exhibiting 4 open and 1 shorted JJ pair and *Blackbird 5i*

[5]Using negative $20 \times 20\ \mu\mathrm{m}^2$ markers 'RN20'

showing only 2 shorts and 1 open JJ, showing an effective yield of 99% (See Table 5.1).

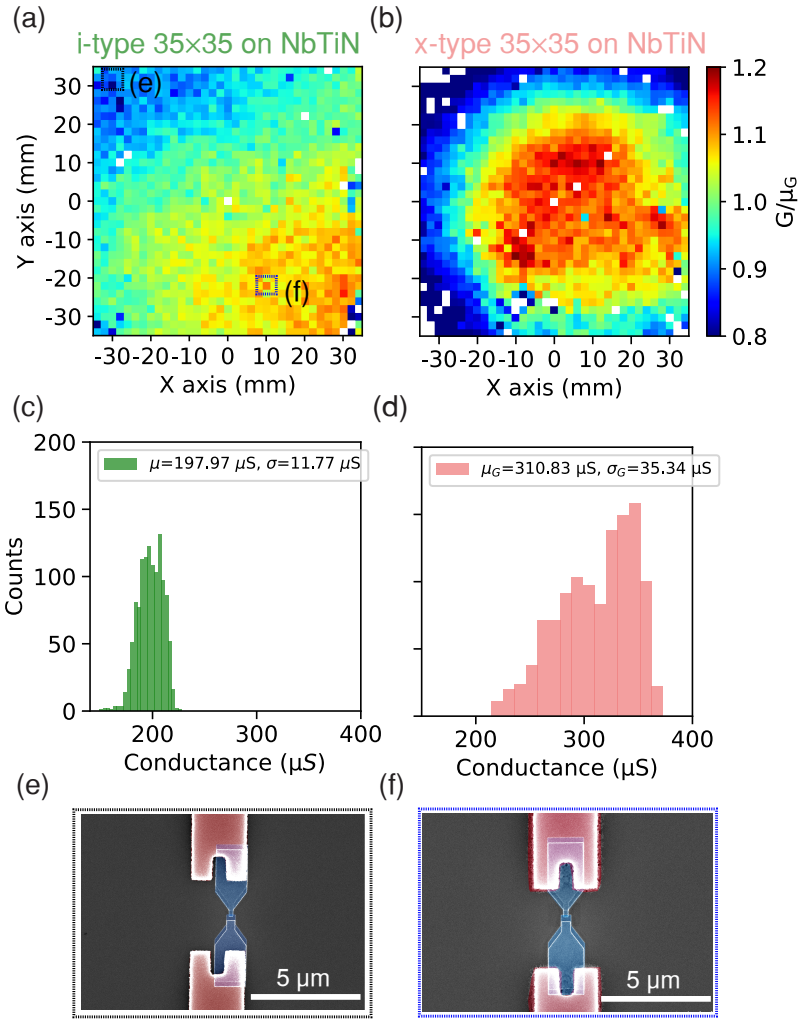


Figure 5.8: Normalized conductance heatmaps in the 35×35 layout on planar NbTiN-metallized wafers of (a) i-type JJ pairs (wafer ID: *Blackbird* 5i) (b) x-type JJ pairs (wafer ID: *Blackbird 4x*). (c,d) Conductance histograms of the corresponding wafers. SEM micrographs of i-type JJs are taken from the wafer at two locations indicated by the boxes. (e) Dislocation of the JJ by ~ 700 nm at the top left corner of the wafer from the centre of the bay. (f) Correct placement of the junction with respect to the bay.

5.4.3. PLANAR 17Q WAFER-SCALE STATISTICS

The objective of this experiment is to simulate wafer-scale fabrication of planar Surface-17 devices and apply both die-level and wafer-scale statistics to discern the sources of variation in junction G. We introduce two variables in this dataset, namely the NbTiN metallization layer and a sweep of A_{overlap} using multiple repeats of both i-type and x-type JJs. We note that the sequence of electrode deposition for i-type JJs was accidentally reversed during deposition in this dataset. A significant sidewall contribution to the conductance may explain the $\sim 70\ \mu\text{S}$ intercept observed in Fig. 5.14. A zoomed-out view (Fig. 5.9(a)) of this dataset shows that the spatial variation of normalized conductance for i-type JJs is significantly lower than for x-type JJs. For the latter, there is a clear systematic decrease from centre to edge, making it unsurprising that the wafer-scale conductance CV is higher for x-type over all A_{overlap}. The general decrease observed in the conductance CV with increasing A_{overlap} is in line with previous works [106, 224]. At die level, the spread of i-type JJs is also lowest, with $\sim 100\ \text{MHz}$ RSD uniform across the wafer. For x-type JJs, the RSD increases away from wafer centre, indicating that the spatial variation is relevant even at die level. The die-level CV for this dataset is plotted in Fig. 5.16 in the chapter SI. i-type JJ show nearly identical distribution in CV across all the dies. On the other hand, the CV distribution as a function of A_{overlap} of x-type JJs from dies positioned at the centre columns (Column 2 and 3) are identical to that of i-type JJs, except for the die located at $x, |y| = -8.3, 25.7$ (ID: *Blackbird 2x 2e*). This is due to the transition of resist shadowing effect between the centre and edge dies, which coincides roughly along the diagonal from the top left to the bottom right of this die. The yield of i-type planar 17Q dataset is the highest across all the waferscale datasets, with a net yield of 99.2%. The breakdown of outliers contributed by shorted and open junctions is 11 and 0 respectively. On the other hand, the planar 17Q x-type dataset exhibits the lowest yield among all x-type wafers with over 70 shorts and 7 open junctions. Multiple SEM images of the failed junctions, particularly along the wafer edges indicate that the NbTiN bays are over-etched, as shown previously in Fig. 3.8, however this observation does not present any clear evidence for the disproportionate number of shorts. We also perform die-level experiments with this layout only with x-type junctions to uncover another source of centre-to-edge distribution of G/μ_G due to the net contact resistance between the JJ Al/NbTiN interfaces, described further in Section 5.7.4.

5.4.4. TSV 17Q WAFER-SCALE STATISTICS

The objective of this experiment is to quantify and compare the magnitude of conductance spread in both i- and x-type JJs fabricated on TSV-integrated substrates using the identical resist stack and post patterning steps as used for planar substrates. It is an important factor in determining the suitability of the VIO architecture for increasing the number physical qubits. A total of 3024 test structures are fabricated per JJ variant for the TSV 17Q dataset. From Fig. 5.10, we can again discern an underlying centre-to-edge dependence for x-type JJs. However, this trend is masked by a significant increase in disorder. The disorder is much stronger for i-

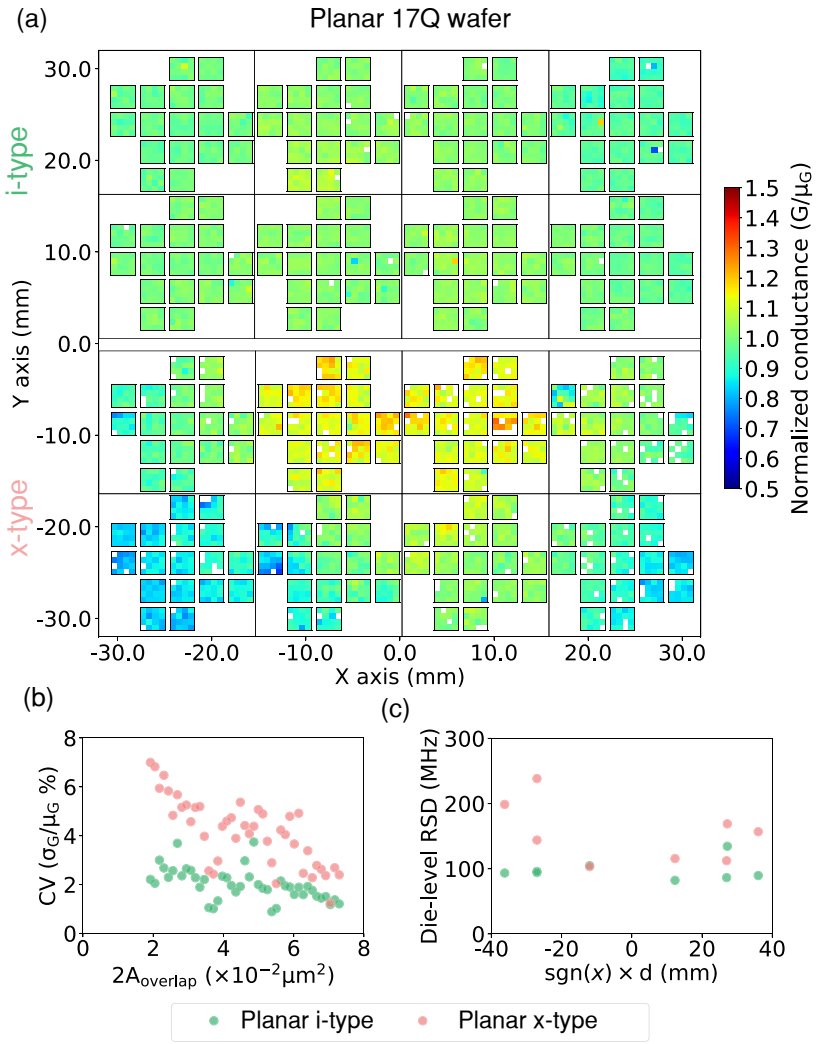


Figure 5.9: (a) Wafer-scale mean-normalized conductance heatmap of i-type (top) and x-type (bottom) JJ test structures on the Planar 17Q wafer. The origin $(0,0)$ indicates wafer centre. Blank cells correspond to test structures identified as defective by the filtering. For this dataset, both JJ types are fabricated on a single wafer. (b) Wafer-scale conductance CV for both junction types as a function of A_{overlap}. (c) Die-level RSD of predicted qubit frequency as a function of distance (d) between die and wafer centres.

type JJs, evident both at wafer scale and die level. Interestingly, the CV for i-type does not display any clear dependence on A_{overlap}, suggesting that resist-height

variations dominate the spread. This observation re-establishes Measurements of resist-height variations caused by TSVs and evidence of the impact of such variations on junction electrode and overlap geometries are shown in Fig. 5.11. Understandably, i-type JJs on TSV wafers are equally susceptible to both shorts and opens with nearly 60 shorted and 69 open junctions due to the sheer randomness of the resist height variations. x-type JJs on TSV 17Q wafer fares slightly better with 66 shorted and 25 open junctions.

Note that the CV and RSD for i-type are calculated both with and without applying regression filters. This is necessary because the high disorder makes the regression filter unable to reject only defective junctions. Even with the artificial improvement of the CV and RSD in i-type JJs that may arise from removing non-defective junctions, a strong conclusion holds: with TSVs, x-type JJs systematically outperform i-type JJs. Nonetheless, with ≥ 250 MHz RSD at die level, even x-type JJs fall very short of frequency targeting objectives in the presence of TSVs. However, there is room for optimism as this investigation is best interpreted as a worst-case scenario for actual TSV-integrated SQPs. In our test, we place many junction pairs per transmon location of Surface-17. Therefore, in a real Surface-17, transmon JJ pairs would on average be $500\ \mu$m away from TSVs. Furthermore, the footprint of TSVs could be further optimized following [37].

5.4.5. RESIST HEIGHT VARIATION ON TSV WAFERS

The integration of TSVs on the wafer prior to junction fabrication creates discontinuities during centrifugal spinning of e-beam resist, resulting in a localized thinning of resist in the immediate periphery of vias. Fig. 5.11(a) shows an optical microscope image of a TSV wafer, with the same layout as the TSV 17Q wafers used in the experiment, taken after spinning the bilayer resist stack for i-type JJs. The visual appearance of the resist-height variation for a wafer spun with the resist stack for x-type JJs is similar (not shown). The resist thickness variations caused by TSVs appear as multiple birefringent bands around the vias, resembling the shape of 'comet tails'. The length of the comet tail is shortest for vias located at wafer centre. With increasing radial distance of the TSVs, the tails gradually elongate facing away from the wafer centre. The width of the comet tails is dependent on the via diameter.

We use contact profilometry lines scans to quantify the height variation of a single resist close to the larger-sized vias ($400\ \mu$m diameter), located near the edge of the wafer. A layer of PMMA A6 (950) with nominal thickness of 600 nm is spun on the TSV wafer for this experiment. Fig. 5.11(b) shows the locations along the comet tails where profilometry scans are acquired with the numbers indicating the measured depth, with each scan spanning $850\ \mu$m across the comet tail. Lines scans performed on four TSVs all appear as symmetric U-shaped curves, as shown in Fig. 5.11(c). The resist thickness decreases by 360 ± 22 nm from the nominal value at a distance of $250\ \mu$m away from the TSV. We repeat the procedure after instead spinning a single layer of PMGI SF7 of the nominal thickness 400 nm used for i-type JJs. In this case, the line scans span $700\ \mu$m across the comet tails. The

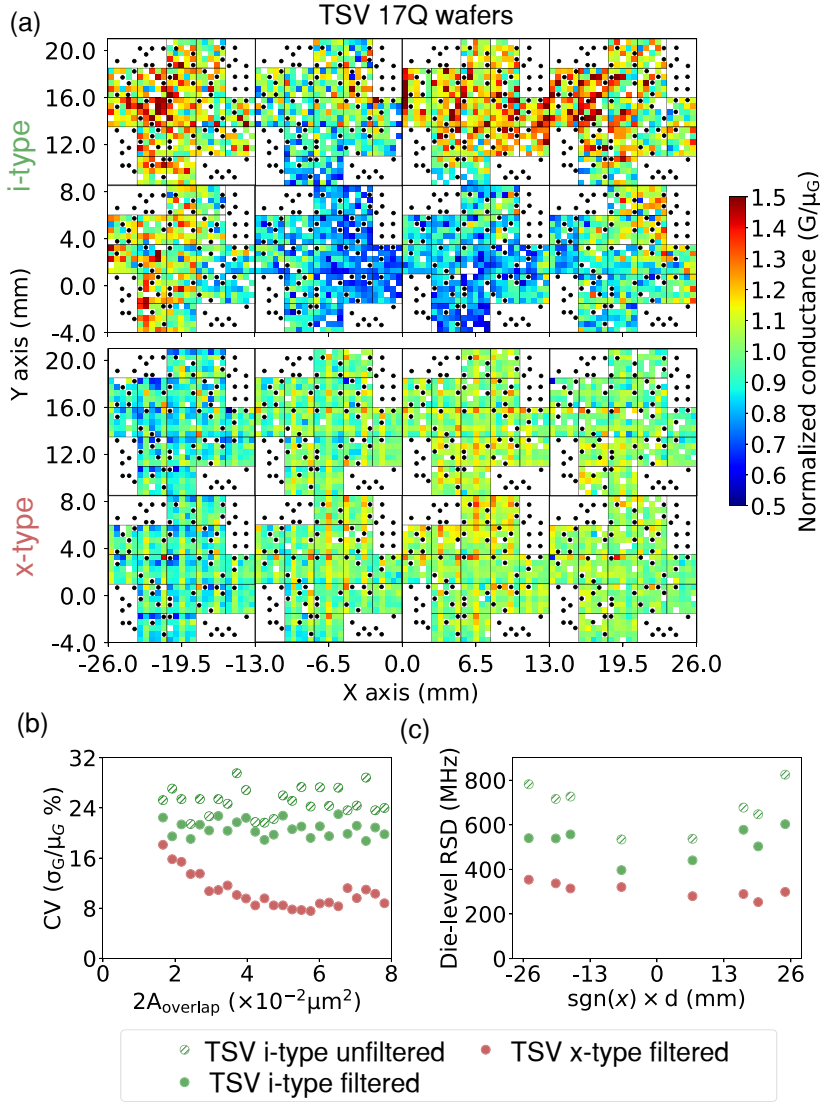


Figure 5.10: (a) Wafer-scale mean-normalized conductance heatmap of i-type (top) and x-type (bottom) JJ test structures on TSV-integrated 17Q wafers. For this dataset, two separate wafers are fabricated, one for each JJ type. The origin $(0,0)$ indicates wafer centre. Blank cells correspond to defective junctions removed by filtering outliers at die level. Cells marked with black circles indicate TSV locations. (b) Wafer-scale CV for unfiltered (nf) and regression-filtered (f) i-type JJ pairs and for filtered x-type JJ pairs as a function of A_{overlap}. (c) Die-level RSD of predicted qubit frequency as a function of distance (d) between die and wafer centres.

resist profiles on three TSVs appear as irregular V-shaped curves, with an average decrease of 127 ± 33 nm at a distance ~ 250 μm away from the TSVs.

To understand the impact of these local resist-height variations, we acquire SEM micrographs of a few JJs located within 200 μm of the smaller-sized vias (160 μm diameter) in both TSV 17Q i- and x-type wafers. We observe two key features, exemplified in Figs. 5.11(d, e). First, i-type JJs show a significant reduction in their overlap area, which arises from thinning of the bottom resist reducing the length of the overlap region along the electrode axis. Second, x-type JJs show spurious deposition of Al near the contact between each electrode and the NbTiN bays. This spurious deposition arises from thinning of the top resist, which prevents it from fully masking the Al metal flux during evaporation of the other electrode.

5.5. CONTACT RESISTANCE BETWEEN AL/NBTIN INTERFACE

The geometric model (See Subsection 4.2.2) predicts that junction conductivity computed from designed overlap area ($G/\Sigma A_{\text{overlap}}$) will show a centre-to-edge decrease as it ignores the positional dependence of the contact area. Experimental results for the three Planar 35×35 wafers clearly show this trend (Figs. 5.12(g–i)). Due to the inaccuracy of approximating A'_{overlap} using top-view SEM images, a slight centre-to-edge increase could even be observed. Conductivity computed as $G/\Sigma A'_{\text{overlap}}$ is very uniform for the all-Al wafer, but not for the wafers with NbTiN and TiN probing pads. In these, the conductivity is very similar (~ 4 mS$/\mu$m^2) at wafer centre, but decreases noticeably away from it. These observations suggest that series resistance from the contact region (nominally 32.4×10^{-2} μm^2) between Al electrodes and the NbTiN or TiN bays is small at wafer center but increases significantly away from centre. While the contact region area is also impacted by the geometric shadowing effect, fractionally the effect is much less significant than for the JJ overlap areas, and cannot explain the observation.

Using circuit analysis, we can calculate the contact resistance per junction required to match the observed reduction in conductivity computed from A'_{overlap} at wafer edge. There are three sets of series resistances in a 2-terminal measurement configuration for each junction in a SQUID loop, namely the joint resistance at the interface of Al electrodes and the base layer. The joint resistance between the bottom (top) Al electrode and base layer is given by R (R') as the in-situ oxidation step contributes towards a higher joint resistance. The resistance of the measuring pads is denoted by R_{pad}, which is measured to vary from 200 Ω at wafer centre to 330 Ω at wafer edge for NbTiN (unknown for TiN) from the wafer *Blackbird 2*. Lastly the contact resistance of the probe and external cabling is R_{c}. The true junction conductance is $g = \sigma A'_{\text{overlap}}$, where σ is the apparent conductivity at the wafer centre at ~ 4 mS$/\mu$m^2. We find $R + R' \sim 2.3$ kΩ for NbTiN pads and ~ 900 Ω for TiN pads.

Further evidence of this effect can be gleaned from the observed wafer-scale CV for the Planar 35×35 wafers (see Table 5.1) and from die-level studies conducted using the planar 17Q layout with x-type junctions shown in the chapter SI (See Fig. 5.22). In the absence of any geometric shadowing and spatially-dependent contact resistance, one would expect the CV for the Al wafer to be $\sim \sqrt{2}$ larger

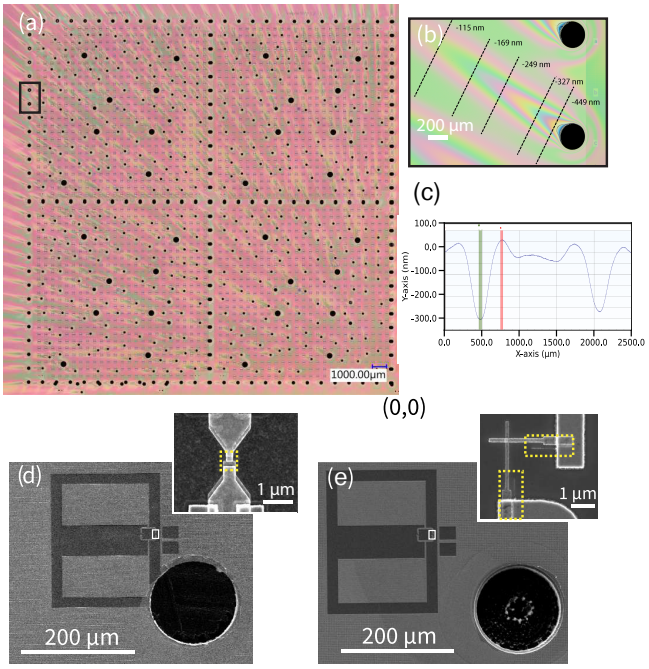


Figure 5.11: (a) Optical micrograph of a wafer with identical TSV layout as the TSV 17Q wafers, taken after spinning the x-type JJ resist stack. Wafer centre is at the bottom-right corner of the image. (b) Optical image of a single TSV from the same wafer, indicated by the black box in (a), taken after spinning layer of PMMA A6 (950K) with the nominal thickness $600\ \mathrm{nm}$ used for x-type JJs. The black dotted line indicates the location and direction of profilometry line scan performed as described in Section 5.4.4. (c) Snapshot of a profilometry line scan performed on the PMMA AG (950K) resist stack spanning the length of two adjacent TSVs, with dips corresponding to the resist profile approximately 200 µm away from the TSVs. (d) SEM micrograph of a i-type JJ test structure in close proximity to a via in the TSV 17Q i-type wafer. Inset: A zoom-in on one of the junctions reveals a reduction of the length of the overlap region along the electrode axis. (e) SEM micrograph of an x-type JJ test structure in close proximity to a via in the TSV 17Q x-type wafer. Inset: A zoom-in on the junction electrodes shows spurious deposition of Al near the contact between electrodes and the NbTiN bays.

because it contains single-JJ test structures while the NbTiN and TiN wafers contain JJ pairs. Geometric shadowing would tend to make the CV similar for all wafers. Instead, the NbTiN and TiN wafers show highest CV.

A new JJ variant with $W_\mathrm{b} = W_\mathrm{t} = 200\ \mathrm{nm}$ and $1.5 \times 1.5\ \mu\mathrm{m}^2$ contact pads, named 'xl-type' contact pads is designed with enlarged bays as shown in Fig. 5.13(a,b) and

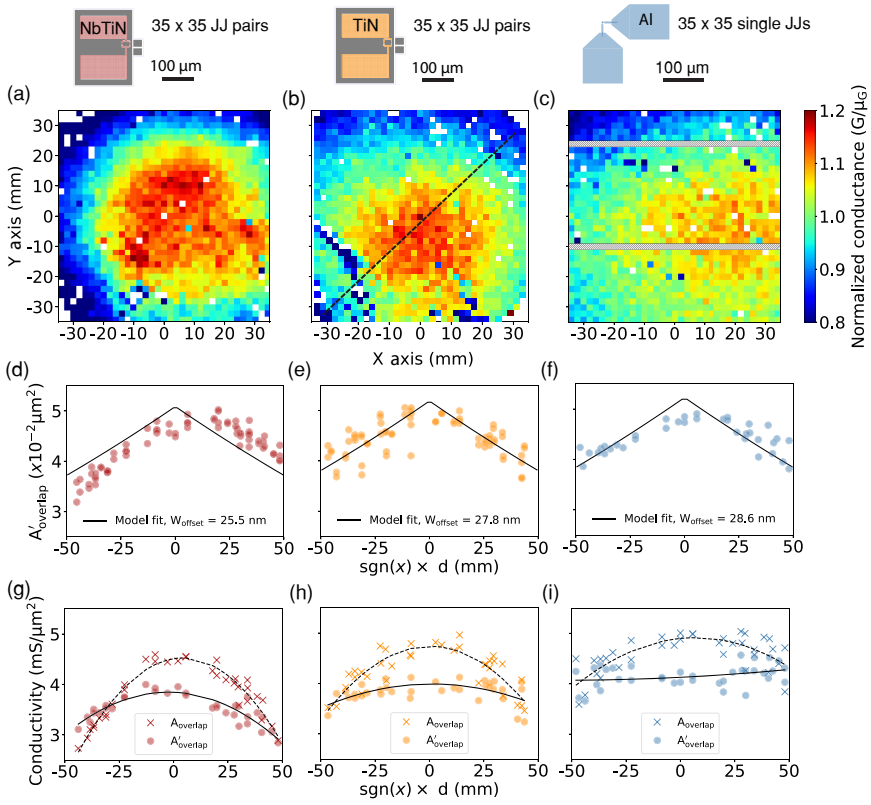


Figure 5.12: Wafer-scale mean-normalized conductance heatmap of 35×35 array of x-type JJ test structures fabricated on three planar wafers with the variants indicated by the top schematics. (a,b) Symmetric junction pairs with (a) Same as Fig. 5.8(b). (b) ALD TiN on Si wafer (*Nighthawk-ALD 3x*). The black dotted line indicates the diagonal along which the JJ pairs are imaged for Fig. 5.19. (c) Same as Fig. 5.7(b). (d–f) Distribution of actual JJ overlap area A'_{overlap} as a function of junction radial position (d). Here, A'_{overlap} is extracted from top-view SEM images. Note that A'_{overlap} does not include the sidewall overlap as this contribution cannot be extracted from these images. The black curves are the best fits of the simplest geometric model (equation 4.2 with single free parameter δW_{offset}). (g–i) Effective junction conductivity (computed from designed and actual overlap areas) as a function of d. The dashed (solid) curves are quadratic fits of A_{overlap} (A'_{overlap}).

deposited on a 35×35 layout NbTiN-metallized wafer with 4900 test structures using the standard JJ recipe (ID: *Blackbird 1xl*). The resulting normalized conductance heatmap is fascinating, as the centre-to-edge variation is now more pronounced compared to the conventional x-type geometry.

The normalized heatmap obtained from the enlarged xl-type JJ contact pads

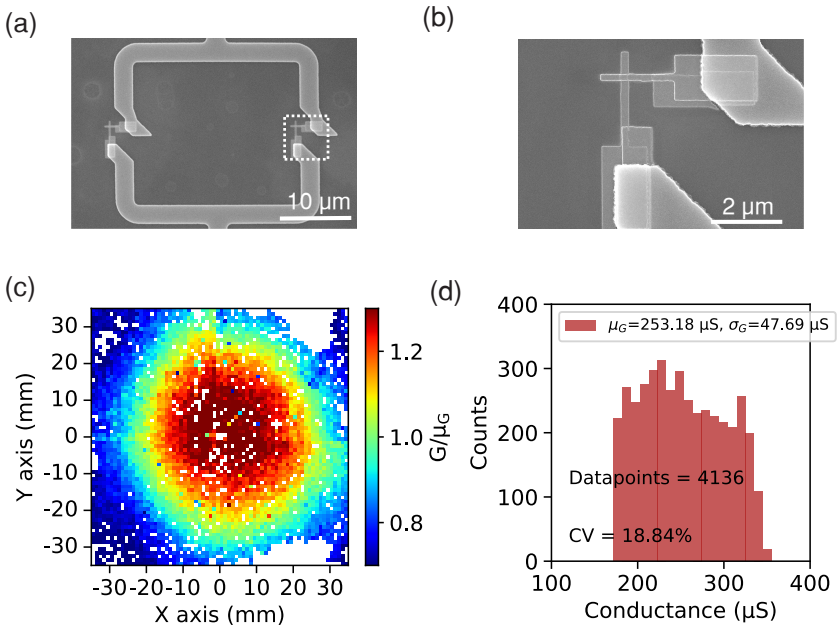


Figure 5.13: (a, b) SEM micrographs of a modified Manhattan-style junction 'xl-type' with enlarged contact pads and reshaped bays.(c) Normalized heatmap acquired from 4900 datapoints, the absence of many datapoints at the top and bottom right of the wafer is due to defective etching of the test pads. (d) Histogram of the dataset, showing the largest σ_G recorded from all planar wafer variants.

(Fig. 5.13(c)) seems initially counter-intuitive, as one might assume that increasing the contact area of the pads is likely to flatten out the overall variation in conductance. It is possible that merely increasing the overlap dimensions without needing to add a separate bandaging step is sufficient to overcome contact resistance differences across the wafer, resulting in the resist shadowing effect being the dominant contributor to the spatial variation in conductance. What does not add up here is that the planar TiN ALD wafer does not show such a prominent gradient. The conformal film should give rise to a relatively uniform contact resistance across the wafer, thereby negating this competing source of the radial distribution. There are still a few open questions concerning this problem.

It remains important for future research to directly measure the magnitude and spatial dependence of this contact resistance, and to reduce both using bandaging layers [224, 276].

Junction type	Substrate	Yield (%)	CV wafer scale (%)	RSD wafer scale (MHz)	RSD die level (MHz)
i-type	Planar 17Q NbTiN	2160/2176 = 99.2 17Q yield = 87.2	0.8-3.7	140	98
	TSV 17Q NbTiN	2958/3024 = 97.8 17Q yield = 68.5 [a] 2770/3024 = 91.6 17Q yield = 22.5 [b]	21.6-29.5 18.5-22.5	800 666	681 [a] 520 [b]
	Planar 35×35 NbTiN	1214/1225 = 99.1 17Q yield = 85.7	6	231	80
	Planar 35×35 Al	1208/1225 = 98.6 17Q yield = 78.6	5	176	113
x-type	Planar 17Q NbTiN	2006/2176 = 92.2 17Q yield = 25.1	1.2–7	317	155
	TSV 17Q NbTiN	2867/3024 = 94.8 17Q yield = 40.3	7.5–18	342	306
	Planar $35times35$ NbTiN	1176/1225 = 96.0 17Q yield = 50	11.3	549	182
	Planar 35×35 TiN	1161/1225 = 94.8 17Q yield = 40.3	8.9	446	172
	Planar 35×35 Al	1121/1155 = 97.0 [c] 17Q yield = 59.5	6.8	251	119

[a] Without regression filtering.
[b] With regression filtering.
[c] Two rows were accidentally omitted during data acquisition.

Table 5.1: Summary of metrics obtained for i- and x-type JJ test structures on all wafers used throughout this study. The 17Q yield reported is that calculated for a Surface-17 SQP using the per-junction-pair yield of the Planar and TSV 17Q wafers. We note that the yield of actual planar Surface-17 SQPs with x-type JJs is roughly 50%, higher than that calculated from the Planar 17Q wafer. The die-level RSD is the average across the eight dies in the 17Q wafers. For the 35×35 Planar wafers, the die-level RSD is calculated from the average of sixteen 6×6 arrays of test structures within the inner $50\times50\,\mathrm{mm}^2$ area of the wafers.

5.6. Discussion

Both from the purview of reproducibility and JJ yield on planar wafers, i-type junctions are definitively superior to x-type junctions fabricated in this study. This indicates the need to further optimize the resist stack and oxidation parameters for x-type JJs in order to flatten out the wafer-scale variations further. The CV of junction conductance for both JJ types is observed to increase systematically as a function of increasing fabrication complexity of the substrates. To understand wafer-scale distribution of surface roughness due to dry + wet etching, the S_a of Si substrate of

Blackbird 4x is mapped from different regions of the wafer post JJ deposition and characterization using AFM. It ranges from $S_a = 0.715$ nm at the centre to 1.89 nm towards the wafer edge. This is also to be expected given the radial gradient of the NbTiN film and the ability of RCA-1 solution to etch Si. To qualitatively discern whether surface roughness affects wafer-scale variability, we compare the CV computed only from the bottom half of the planar i-type wafers on bare Si (Fig. 5.4(a)) and on NbTiN (Fig. 5.8(a)) in order to avoid the top dislocated junctions in *Blackbird 5i*. The bare Si sample shows CV = 3.2% obtained from 625 datapoints at the lower half compared to 5.35% from 621 points for the metallized wafer. This may indicate that surface roughness of the etched Si regions is an important contributor to wafer-scale spread of JJs.

Comparing the statistics of x-type JJs fabricated on planar and TSV 17Q layout substrates show that the wafer-scale RSD is relatively constant across both substrates ($\sim 330 \pm 10$ MHz), however the average die-level RSD of the 17Q TSV substrate is double that of the planar counterpart. The sensitivity of A_{overlap} to resist height variations is

$$\frac{\delta A_{\text{overlap}}}{A_{\text{overlap}}} \approx \frac{|x|}{D}\frac{\delta H}{W_b} + \frac{|y|}{D}\frac{\delta H}{W_t}.$$

Plugging in values for $|x| = |y| = 1$ mm, $W_b = W_t = 160$ nm and $\delta H \sim 360$ nm obtained from profilometry measurements, we get $\delta A_{\text{overlap}}/A_{\text{overlap}} \sim 0.01$.

This is an approximate solution, as measurements of localized resist height variations alone are not sufficient to fully quantify how TSVs contribute to resist height variations across the wafer. For example, we do not clearly understand why the TSV 17Q i-type wafer shows a centre-to-edge increase in conductance observed from the normalized heatmap in Fig. 5.10(a). We would expect that, with the increasing length of the comet tails going from wafer centre to edge, the normalized conductance pattern would show the opposite trend.

Concerning the effect of variation in sidewall overlap area predicted by the geometric model, (See Subsection 4.2.2) it would be worthwhile to experimentally equalize T_b' across the wafer by breaking the deposition of the bottom electrode into two steps with an intermittent change in tilt θ in the opposite direction [225]. The lowest wafer-scale CV for x-type JJs reported by Kreikebaum *et al.* [221] is from a planar bare Si substrate with single junctions using a top resist stack $H_t \approx 150$ nm. Our attempts to fabricate x-type JJs using a bottom-heavy resist stack (described in subsection 5.7.3) did not lead to conclusive results. Further efforts are necessary to verify if decreasing the thickness of the top resist stack would flatten out the wafer-scale variation in A'_{overlap}. This experiment should ideally be repeated by increasing the aspect ratio of the electrodes to eliminate the sidewall deposition of lifted-off Al.

Finally, the existence of a large contact resistance between the Al/NbTiN joint arising from the formation of oxides due to the in-situ oxidation process for growing the tunnel barrier coupled with the non-uniform thickness distribution of sputtered films, underscores the need to modify multiple aspects of x-type JJ design as well as deposition sequence. This is equally valid in i-type junctions, revealed by the SEM image of a junction shifted away from the centre of the bay, effectively halving the contact area in the north-west quadrant (Fig. 5.8(a)). This is the principal

cause of the large centre-to-edge distribution in G/μ_G in the experiment described in subsection 5.7.4.

5.7. WAFER-SCALE UNIFORMITY OF JOSEPHSON JUNCTIONS: SUPPLEMENTARY INFORMATION

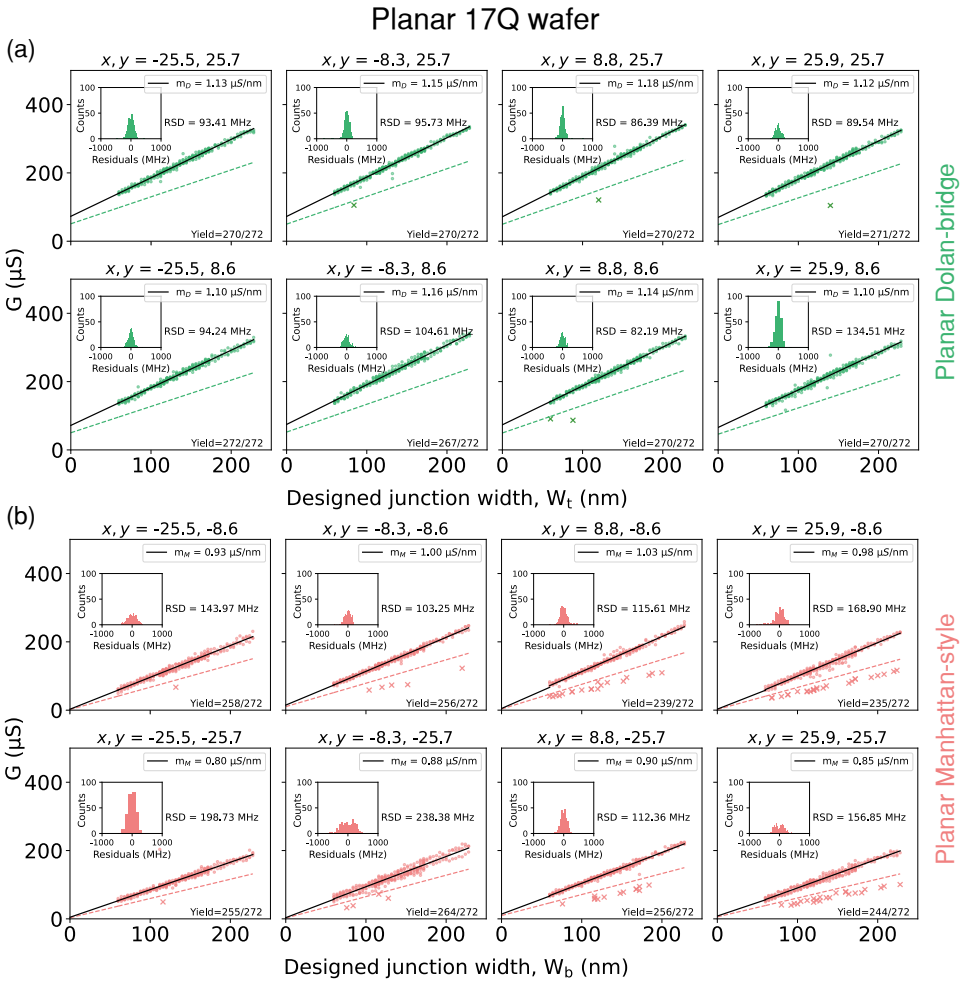


Figure 5.14: Die-level linear regression analysis of conductance as function of designed junction width of the variable electrode of (a) i-type and (b) x-type JJ pairs on the Planar 17Q wafer. Coordinates shown at the top of each panel indicate die center (relative to wafer centre). The dotted coloured lines correspond to the best fit of the initial regression. The crosses below the dotted coloured line are interpreted as half-open junctions. The filtered data are then fit again with a second regression. Insets: The residuals from the second regression fit are plotted in units of predicted qubit frequency. The frequency RSDs obtained from these histograms are plotted in Fig. 5.9(c).

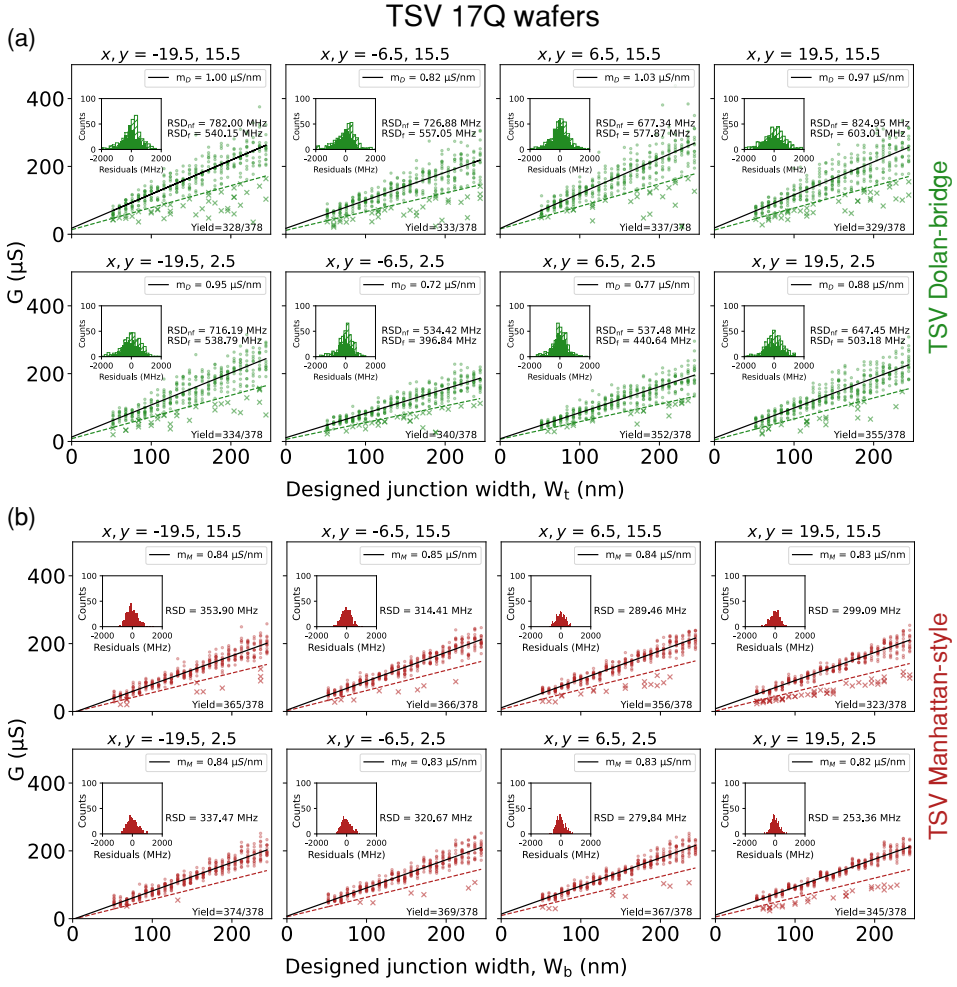


Figure 5.15: Die-level linear regression analysis of conductance as a function of designed width of the variable electrode of (a) i-type and (b) x-type JJ pairs on the TSV 17Q wafer. Coordinates shown at the top of each panel indicate die center (relative to wafer centre). The outliers are filtered using the method described in Section 5.3. Due to the large spread in conductance in the TSV i-type data, the initial regression filter does not clearly discriminate half-open junctions. The die-level RSD, is therefore calculated from unfiltered $(\mathrm{RSD_{nf}})$ as well as filtered $(\mathrm{RSD_f})$ conductance data, plotted in Fig. 5.10(c).

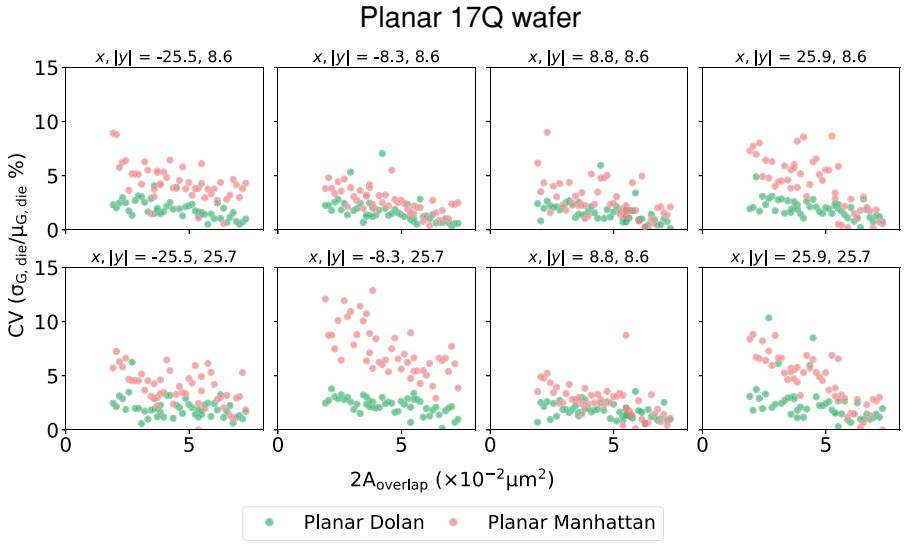


Figure 5.16: Die-level conductance CV as a function of the designed overlap area for i-type (green) and x-type (red) JJ pairs fabricated on the Planar 17Q wafer. Coordinates shown at the top of each panel indicate die center (relative to wafer centre).

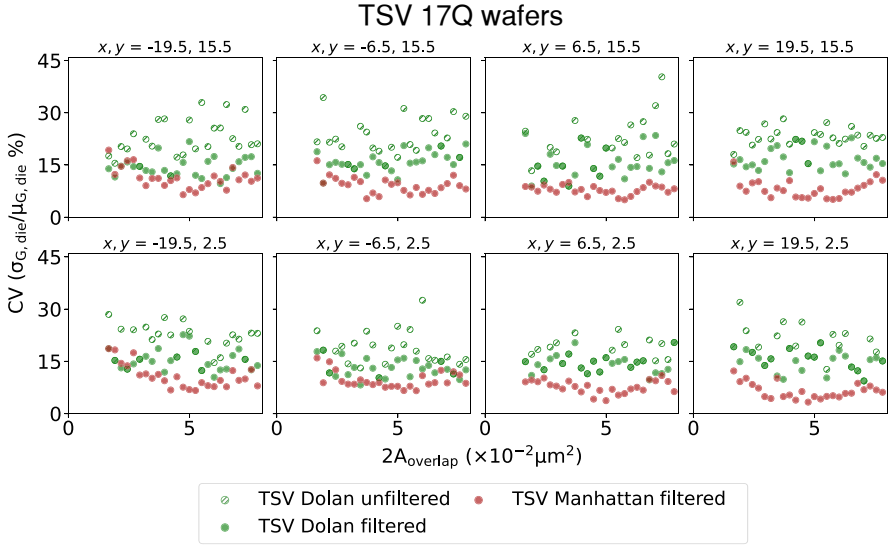


Figure 5.17: Die-level conductance CV as a function of the designed overlap area for unfiltered (hatched) and filtered (green) i-type and for x-type (red) JJ pairs fabricated on the TSV 17Q wafer. Coordinates shown at the top of each panel indicate die center (relative to wafer centre).

5.7.1. TSV 7Q wafer-scale statistics

The TSV 7Q layout, described in Fig. 5.6(c) consists of alternating dies with i-type and x-type JJ test structures with 3 planar repeats sandwiched between the TSV-sparse layouts. Each island is patterned with nominally identical junctions. We first deposit x-type JJs and measure G followed by deposition of i-type JJs. The objective of this experiment is to compare the role of resist height variations at the intra-wafer level and the difference in the magnitude of conductance between nominally identical junctions fabricated on a planar die and a TSV-integrated die. From Fig. 5.11(a), the planar dies 1_2 i, 2_2 i and 1_3 x are largely devoid of the resist comet tails. The μ_G and σ_G are plotted for $W_\mathrm{b} = W_\mathrm{t} = 50, 100, 150, 200$ nm for each die. The results reveal interesting behaviour in variation of G as a function of the orientation of the comet tails, which is the causative factor for on-chip resist height fluctuations. In case of x-type JJs, as expected, there is no discernible difference in the conductance distribution between the 5 TSV containing dies and the singular planar die (1_3 x). Turning over to the i-type JJ dataset, the highest μ_G is observed for the designed JJ widths among the planar dies (1_2 i and 2_2 i) whereas G is nearly halved in three of the TSV dies (2_4 i, 1_6 i and 2_6 i). Why is the die 1_4 i not affected similar to the TSV counterparts? On taking a closer look at the comet tails, it is evident that the comet tails are shortest at the centre of the wafer (this repeat constitutes the lower half of the *Valkyrie* wafer) and therefore the conductance value is similar to that observed in the planar i-type dies.

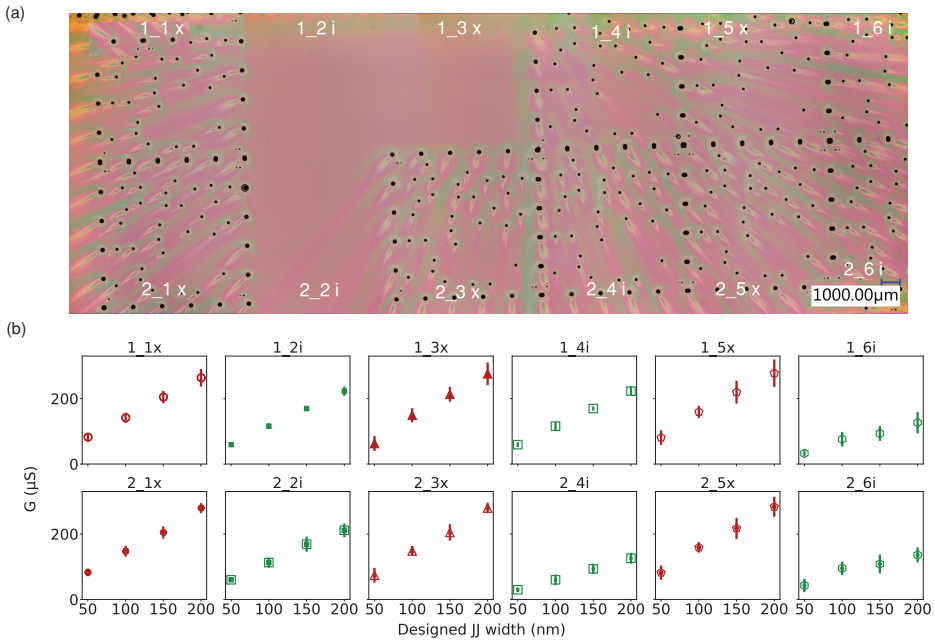


Figure 5.18: (a) Stitched optical image of a TSV 7Q layout coated with e-beam resist stack used for x-type JJs. (b) Error bar plot of conductance vs. designed junction width of each TSV 7Q die.

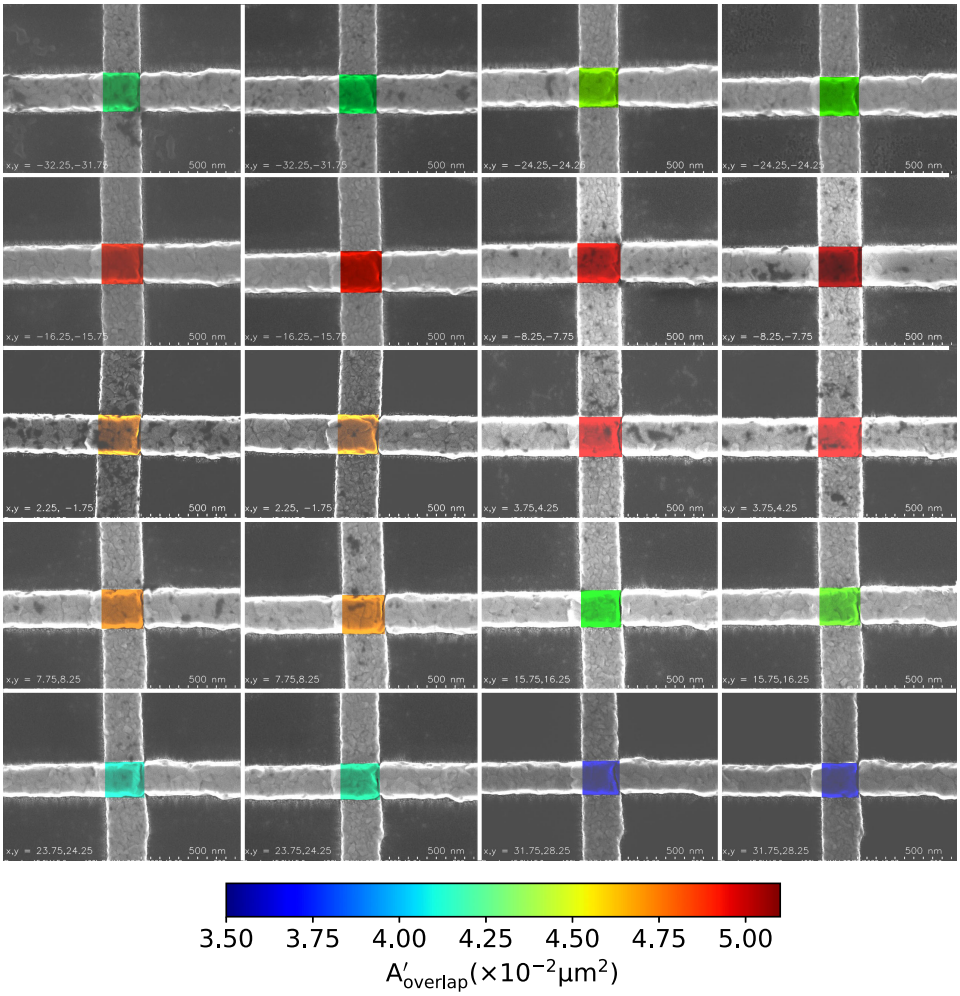


Figure 5.19: Compilation of a subset of SEM micrographs used to extract actual electrode widths and junction overlap areas for several of the x-type junction pairs fabricated on the planar 35×35 TiN wafer (Fig. 5.12(b)). The images are acquired from test pads positioned diagonally across this wafer shown by the black dotted line. Images of junctions for a JJ pair are placed side by side. Each image is labelled with the coordinates of the JJ pair relative to wafer centre.

5.7.2. VARIATION OF O_2 PLASMA TREATMENT

We also investigate if varying the O_2 plasma descumming recipe can affect the centre-to-edge variation in overlap area using all-Al single x-type JJs fabricated on planar Si substrates. Referring back from Subsection 3.3.5, O_2 plasma descumming is performed using RIE in order to clean resist residues from the developed JJ patterns. In Ref. [221], it is reported that splitting the plasma ashing step by rotating the wafer 4x and 16x result in a more radially symmetric I_c gradient across the wafer using a high pressure (~ 500 mbar) isotropic etch process. We fabricate a total of 6 wafers with variations in the plasma treatment described in Fig. 5.20. The significance of the descumming step in improving wafer yield is highlighted by the large non-radial spread in G/μ_G of *Nighthawk 1x*, which is not subjected to any descumming. The large number of defective JJs observed in *Nighthawk 4x* is likely due to wafer handling issue in spite of using the standard descumming protocol. Among the plasma ashing variants, we do not observe any improvement in wafer-scale spread nor in the symmetry of the radial conductance gradient. We test an alternative plasma etching system, a PVA Tepla 300 using the following parameters: O_2 flow rate = 200 sccm, RF power = 100 W, intensity = 76, process pressure $\approx$ 0.6 mbar and etch time = 120 s. The centre-to-edge gradient appears to be smeared by patches of insufficiently descummed JJ patterns, further optimization in this direction is therefore discontinued.

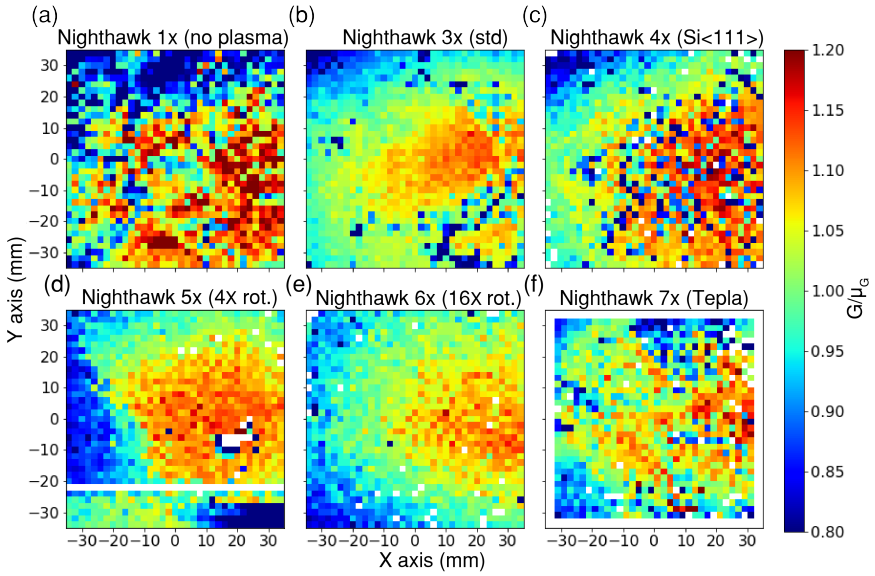


Figure 5.20: Mean normalized conductance heatmaps of x-type JJs on planar Si with 35×35 layout used to test the influence of plasma descumming on wafer-scale uniformity. The computed CV (σ_G/μ_G) is (a) 14.3% (b) 7.3% (c) 9% (d) 9.4% (e) 6.7% (f) 8.3%. Reprinted from Duivestein (2021) [255].

5.7.3. Resist-stack engineering for X-type junctions

Referring back to the geometric model in Section 4.2.2, the height of the top (imaging) resist H is the only fabrication parameter that can be modified if we intend to flatten the spread in x-type JJs. The RSD of G from our wafers are twice as high as the values reported from [221], what comes to attention here is that the authors of this work use a *bottom heavy* resist stack (500/150 nm) as opposed to our *top heavy* composition (200/600 nm). A new experiment is undertaken tempted by this hypothesis, wherein the height of the individual resists in the bilayer stack is reversed, such that it is *bottom heavy*, as opposed to the conventional recipe. In place of a $200\ \mathrm{nm}$ PMGI SF7 bottom resist, I substitute with a $600\ \mathrm{nm}$ MMA(8.5)/MAA (EL11) layer which yields a more controllable undercut profile. The top resist layer is thinned from a $600\ \mathrm{nm}$ to $250\ \mathrm{nm}$ using PMMA A3 (950K). This resist bilayer is developed only in MIBK:IPA (1:3) solution for 60 s. The deposition tilt is increased to 45° to compensate for the reduced height of the top resist. Two wafer-scale tests on planar Si are performed under these adjusted parameters, with the best dataset illustrated in Fig. 5.21(c,d). A conductance gradient is still observed, although it is now offset towards the north-west of the wafer. Unfortunately, it is challenging to draw definitive conclusions on potential causes, as the other dataset still exhibits a center-to-edge gradient (not presented here). The lack of a clear centre-to-edge gradient using our top-heavy resist stack is puzzling, a possible reasons which can be attributed to this observation is the presence of lifted-off Al metal deposited along sidewalls of the electrodes, which may affect the junction conductance. The next iteration of this experiment must be performed by increasing the length of the top and bottom electrodes from $2.8\ \mu\mathrm{m}$ to at least $10\ \mu\mathrm{m}$ between the overlap region and the contact pads. Additionally, the JJ yield is lower at 85% compared to the standard process, with most of the filtered data corresponding to open junctions. Analysing SEM images of defective junctions revealed dark regions corresponding to organic residues. Tests to identify the source of this contamination show that the MMA/MAA bottom resist layer is not stable when treated with BOE solution, leaving residues on the junction pattern prior to deposition. Further optimization of the modified recipe is required, with a focus on replacing the stripping of native oxides after plasma descumming using argon ion-milling instead of BOE solution.

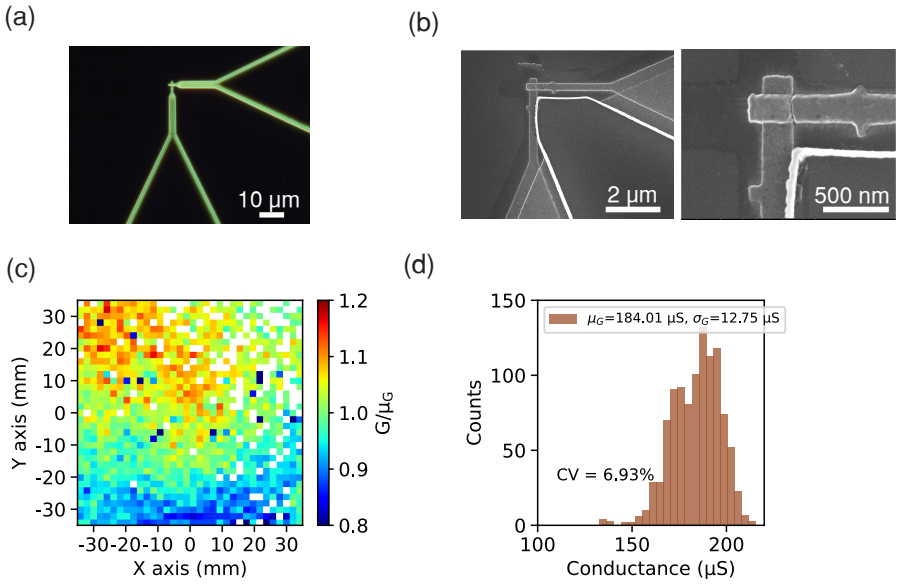


Figure 5.21: (a) Optical dark field image of the developed PMMA/MMA modified resist stack. (b) SEM micrographs of the x-type junctions with $W_\mathrm{b} = W_\mathrm{t} = 200$ nm. The bright lines connected to one end of the JJ electrodes are Al deposited along the walls of the resist undercut profile. (c) Heatmap of G/μ_G of x-type JJs with $W_\mathrm{t} = W_\mathrm{b} = 200$ nm in 35×35 layout on planar Si(100) substrate using the *bottom heavy* PMMA/MMA resist stack. (d) Histogram of the dataset , with identical values of μ_G and σ_G as in Fig. 5.7(d).

5.7.4. Contact resistance: die-level statistics

In addition to the waferscale studies aimed at extracting the order of magnitude of contact resistance between the Al/AlO_x/Al-NbTiN joint in x-type JJs, we also performed an experiment by dicing a wafer (*Blackbird 1*) with Planar 17Q array layout and depositing each x-type die individually in a random order over a span of one working week. Each die is placed at the centre of the Plassys holder and evaporated under nominally identical conditions, with the only variable here being the position of each die with respect to the wafer. We then analyse the 8 individual datasets in a manner similar to Fig. 5.9. A similar centre-to-edge variation as the geometric model, however significantly pronounced again appears as observed in Fig. 5.22(a). This is purely a manifestation of the JJ-base layer contact resistance. The apparent conductivity from the measured overlap area (A'_{overlap}) extracted by imaging at least three JJ pairs from each die varies from $\sim 3.5\ \text{mS}/\mu\text{m}^2$ for the centre dies *2c, 3c, 2e* to $\sim 2.2\ \text{mS}/\mu\text{m}^2$ for the remaining edge dies. It is unlikely that variations in tunnel barrier formation between successive depositions can lead to such a systematic spatial variation.

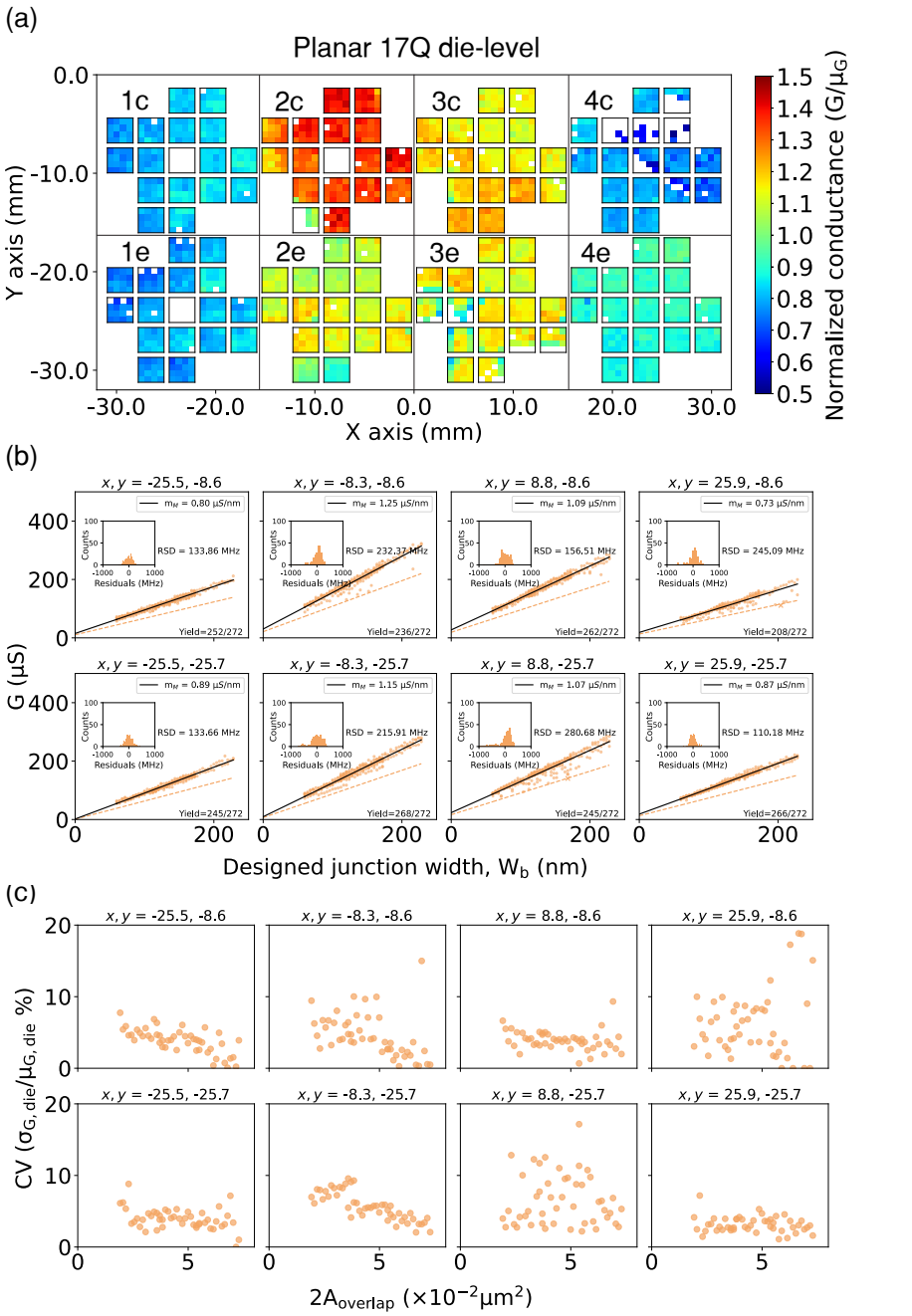


Figure 5.22: (a) Normalized conductance heatmap of 8 dies patterned with the planar 17Q layout. (b) Die-level linear regression analysis of conductance as a function of designed width of the variable electrode of x-type junctions in die-level planar 17Q layout. (c) Die-level conductance CV as a function of the designed overlap area.

6

POST-FABRICATION FREQUENCY TARGETING

This chapter delves into the chemical mechanism of ageing observed in Al/AlO_x/Al Josephson junctions. Various environmental and experimental factors which induce junction ageing are identified through RT conductance statistics with test structures as well as through cryogenic measurements. It discusses post-fabrication tuning strategies which can be applied at the hardware level to locally or globally mitigate inaccuracies in qubit frequency targeting using laser annealing and rapid thermal annealing respectively. With laser annealing, we demonstrate the ability to monotonically trim qubit frequencies on wirebonded SQPs after initial characterization of the devices in a dilution fridge. The work here demonstrates a targeting precision $\sim 24\ \mathrm{MHz}$ for annealed qubits, thereby creating avenues for post-fabrication fine-tuning of qubit-pair and resonator-qubit detunings. Experiments with rapid thermal annealing (RTA) highlights that the magnitude and directionality of ageing is a temporally-driven process owing to the reactivity of the AlO_x tunnel barrier towards its environment. A thorough understanding of all the identified RTA process variables enables us to to engineer on-demand ageing or anti-ageing of junctions.

6.1. ALO_x TUNNEL BARRIER

Aluminium oxide (AlO_x) is a well-characterized dielectric and passivation layer which can be deposited by multiple thin-film techniques such as sputtering, CVD and ALD or thermally grown from Al metal due to its high reactivity with O_2. It is the most widely adopted tunnel barrier to date in superconducting circuits due to the reliable in-situ thermal oxidation of Al at RT when JJs are fabricated using multi-angle evaporation. Non-uniformity in the thickness of the tunnel barrier grown using thermal oxidation is a known problem, which leads to inhomogeneity of the tunnel current across the barrier. As explained previously in Subsection 4.2.1, the conductance per unit area is much smaller in reality, about 10% of the total AlO_x barrier in comparison to the assumptions made in chapter 5 [49]. The structural properties of the Al/AlO_x layer system are sensitive to oxidation parameters such as O_2 pressure, duration and process temperature [277, 278]. Additionally, the deposition parameters of the Al bottom electrode influence the grain size and homogeneity of the entire Al/AlO_x/Al stack, as it is observed that the thickness of AlO_x increases locally along the grooves of the Al grain boundaries [253]. Therefore, growing epitaxial Al films which inherently possess large grain size is key to minimizing tunnel barrier fluctuations for fabricating reliable and scalable SQPs. Inspite of the nearly 25.5% lattice mismatch between Al and Si, epitaxial growth of Al is reported with Al(111) surfaces grown on clean pretreated Si(111) substrate at deposition temperature $200\ ^\circ\mathrm{C}$ and rate $1.0\ \mathrm{nm/s}$ [279].

The typical oxidation parameters of O_2 pressure (0.1-1 mbar) and duration (3-30 min) at RT used in JJ fabrication yield thin amorphous layers of α-Al_2O_3 with thickness ranging ~ 1.5–$2.0\ \mathrm{nm}$. The atomic structure of ultra-thin AlO_x is influenced to a greater extent by interfacial interaction with the bottom and top Al electrodes compared to bulk oxides. The origin of oxygen vacancies and relocalization of Al and O are related to the reduced coordination of O atoms at the Al/AlO_x/Al interface leading to oxygen deficiency [280]. Defects arising from O_2 vacancies and dangling bonds, as shown in Fig. 6.1, due to absorption of -OH groups give rise to TLS in the tunnel barrier, which is a well-known limiting factor for improving decoherence in SQPs [101]. TLSs are sources of low-energy excitations which can couple to oscillating electric fields in superconducting circuits via their electric dipole moment, a hallmark property of glasses [281]. This also contributes towards fluctuations in conductance of JJs in addition to geometric variations in the junction overlap area.

Another implication of this interfacial disorder is the time evolution of junction conductance and capacitance due to *ageing* on prolonged storage at ambient atmosphere and temperature, repeated thermal cycling and annealing at temperatures between 200–$450\ ^\circ\mathrm{C}$ [282–284]. The junction conductance continually decreases logarithmically as a function of time and ambient pressure, with the rate mechanism saturating at $10^{-2}\ \mathrm{mbar}$ for Al/AlO_x/Al junctions [285]. This phenomenon is associated with either diffusion of O_2 between the tunnel barrier and Al electrodes or due to the change in the chemical composition of the barrier by absorption or desorption of other atoms and molecules besides O_2, with the latter process assumed to play a dominant role in junction ageing [286]. The presence of resist residues in the junction pattern post development is also detrimental to tunnel barrier quality,

which motivates the inclusion of O_2 plasma descumming and HF dip pre-cleaning steps prior to JJ deposition [286, 287].

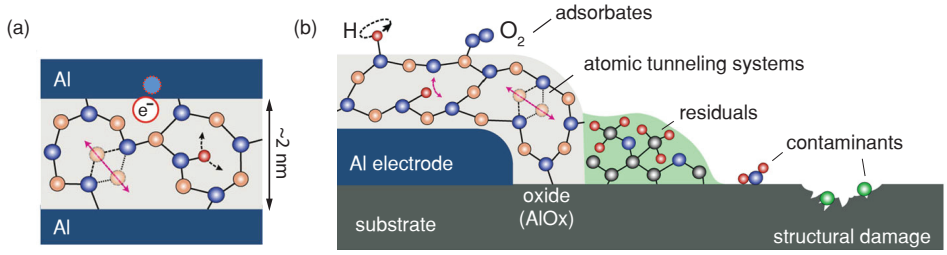


Figure 6.1: (a) Ball-and-stick illustration of AlO_x tunnel barrier sandwiched between Al leads, highlighting various defects arising due to atomic tunnelling systems (red arrow), hydrogen impurities (dashed black arrows),and trapped electrons (red circles) that contribute to TLS formation. (b) Sketch indicating surface defects such as structural damage on the substrate, residues from fabrication processes such as resist (indicated in green) and atmospheric contaminants such as molecular oxygen and hydrogen, which are a likely source of $1/f$ noise. Reprinted from Lisenfeld *et al.* (2019) [281] under Creative Commons BY License managed by Springer Nature.

6.1.1. JUNCTION AGEING

Junction ageing is referred to the temporal evolution of the AlO_x tunnel barrier during device storage at ambient conditions. Aside from A_{overlap}, the junction G is also influenced by the localized defect density of the tunnel barrier. In the absence of a fabrication-based solution to arrest the reactivity of the AlO_x layer during storage or due to end-of-line fabrication steps such as airbridge integration, interim efforts are necessary to understand its impact on qubit frequency targeting. Depending on the prior state of the tunnel barrier the global conductance post AB annealing can either decrease (increase), termed as ageing (anti-ageing) within this context. Many factors in the fabrication parameters of JJs significantly affect the magnitude and directionality of both ageing as well as on-demand annealing processes. In order to establish a correlation between the tunnel barrier hygiene and the annealing processes, it is necessary to intuitively understand how deviations in each step of the fabrication flow affect the junctions in the first place. The outcomes of ageing and on-demand annealing are observed to be correlated to the following fabrication and environmental parameters, identified from statistics of nearly 10^5 junctions fabricated over hundreds of deposition rounds using the nominally fixed JJ parameters described in chapter 3:

- JJ geometry
- Capping oxidation layer
- Ambient conditions and duration of device storage

- High-temperature fabrication steps such as airbridge resist reflow.

The junction can be terminated with an oxide layer post deposition of the Al top electrode to passivate the JJs. However this is a temporary measure, as the capping oxide layer itself degrades over time which strongly depends on the conditions in which the device containing the JJs is stored. On incorporating a capping layer, it can be expected that JJs become less sensitive to ageing in either direction [273]. However the capping layer only serves to retard junction ageing, not completely halt it. It is temporally inevitable to halt ageing unless the devices are stored in high vacuum conditions. All devices used for experiments described in this work are stored either in vacuum desiccators pumped down to 10^{-3} mbar or in atmospheric pressure N_2 desiccators. Therefore JJ ageing during storage must be taken into account to gain a better understanding of predicting the outcome of on-demand annealing strategies.

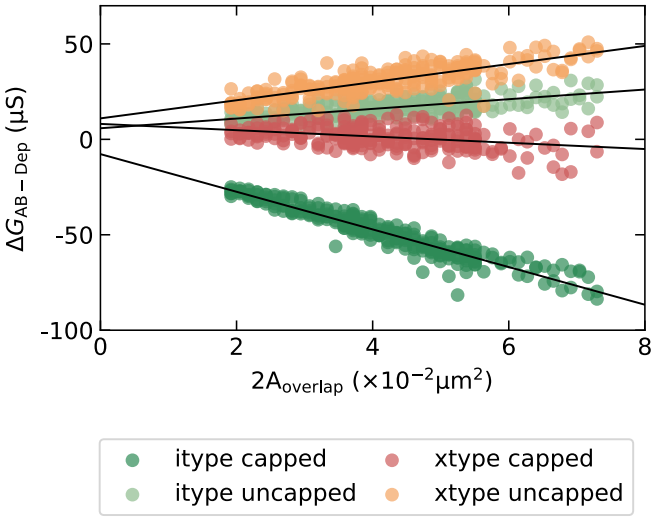


Figure 6.2: Change in RT conductance (ΔG) post AB anneal at $200\ ^\circ C$ and deposition in i-type (Dolan-bridge) and x-type (Manhattan-style) JJs deposited on dies coated with 200 nm sputtered NbTiN. The black lines indicate linear regression fits, with coefficients for each dataset listed in Table 6.1.

JJ type	Passivation	Storage (days)	ΔG fit ($\mu S/\mu m^2$)	R^2
i-type	Capped	5	-986.3	0.914
	Uncapped	< 1	253.5	0.424
x-type	Capped	< 1	-164.6	0.132
	Uncapped	< 1	474.5	0.638

Table 6.1: Table of AB anneal variables corresponding to Fig. 6.2 along with the regression fit parameters. Storage indicates the time the device was parked between the two measurements.

The airbridge integration steps post JJ deposition is essentially an annealing process in itself where the JJs are covered with a layer of resist and heated up to

200 °C to reflow the resist. This step introduces tremendous uncertainty with regards to qubit frequency targeting as the global conductance trend is observed to shift in either direction or even in some instances show non-uniform ageing behaviour within the device from run to run. Additionally a correlation between the state of junction passivation and conductance shift post AB annealing is observed from Fig. 6.2. Uncapped junctions of either variant are prone to anti-ageing post airbridge anneal step whereas capped junctions tend to age. This is because the G of capped junctions post deposition is systematically higher than that of uncapped junctions in both geometric variants (For additional data, see chapter SOM Fig. 6.19). This observation is not backed up by sufficient understanding of the tunnel barrier mechanism which leads to this behaviour. A reasonable hypothesis can be the rapid hydroxylation of the exposed regions of the AlO_x by ambient water vapour. It is likely that environmentally-induced ageing (EIA) of JJs is a leading cause for temporal decrease in the tunnel barrier transparency, even when fabrication is performed in a controlled cleanroom environment with typical relative humidity (RH) levels between 50–60%. We cannot further assert the validity of this statement in the absence of data relating to the rate kinetics of the hydroxylation process in ambient conditions, however *ab-initio* simulations of reaction of H_2O molecules on Al(111) surface estimate dissociation into OH^- occurring in the order of picoseconds [288]. Predicting the outcome of the magnitude and directionality of the conductance shift is further compounded by lag times between the deposition and airbridge steps. The longer storage period for capped i-type junctions in Fig. 6.2 maybe a contributing factor for the large ΔG shift. Therefore a systematic documentation of the storage duration between the deposition and airbridge (AB) annealing steps is carried out in most of our fabrication runs.

6.1.2. THERMAL ANNEALING OF ALO_x

Thermal annealing of Al/AlO_x/Al JJs was used in early works to stabilize the oxide barrier properties by artificially accelerating the relaxation of the glassy state to its energy minimum, with complete stabilization reported to occur at annealing temperature of $400\ ^\circ\mathrm{C}$ either in air, vacuum or an inert gas such as N_2 [287, 289]. Studies on comparing the effect of rapid thermal annealing treatment on thermally-grown vs. plasma-grown AlO_x tunnel barriers show that the conductance of thermal oxide barriers decline sharply at process temperature $\geq 300\ ^\circ\mathrm{C}$ while that of plasma-grown barriers start changing $\geq 450\ ^\circ\mathrm{C}$ [282]. The junction properties post thermal annealing are improved due to the dehydration of -OH groups which present undesirable resonances in tunnelling conductance spectra ($\mathrm{d}I/\mathrm{d}V$), which result in increase in junction R_N and E_c , thereby increasing barrier height [287]. However annealing Al/AlO_x/Al single-electron transistors in the presence of forming gas (FG) at $1.0\ \mathrm{mbar}$ pressure revealed two different regimes with regard to the change in resistance as a function of the temperature [290]. Annealing at $200\ ^\circ\mathrm{C}$ in the presence of FG revealed nearly 30–40% systematic increase in conductance without affecting the tunnel contact behaviour which saturated post 30 min. At $400\ ^\circ\mathrm{C}$ FG annealing, the conductance was nearly halved post 15 min independent of the initial measured value. This observation can be interpreted as follows: at a moderate an-

nealing temperature, dehydroxylation of Al hydroxides such as gibbsite $\gamma-\mathrm{Al(OH)_3}$, boehmite $\gamma-\mathrm{AlO(OH)}$ and possibly other polymorphs start occurring above $145\ ^\circ\mathrm{C}$ [291, 292]. The tunnel barrier morphology is likely altered due to formation of spikes at sites where -OH groups are removed without significant change in C_J, effectively decreasing the barrier thickness and tunnelling resistance [290]. At higher temperature however, a clear decrease of C_J is observed which is attributed to increase in barrier thickness due to thermally activated diffusion of unbound O_2 from interstitial lattice sites or from the dissociated hydroxides. It has also been shown that thermal annealing of Al/AlO_x/Al junctions at $400\ ^\circ\mathrm{C}$ reduces characteristic $1/f$ noise by an order of magnitude due to lowered density of states of TLS [293]. The disadvantages posed by the amorphous tunnel barrier can be overcome by incorporating thermal annealing as a fabrication tool. Two annealing techniques are investigated in this work which confer the ability to tune the junction conductance on-demand post device fabrication, namely *laser annealing* (LA) at atmospheric conditions and *rapid thermal annealing* (RTA) in N_2 and FG environments for investigating the possibility of post-fabrication bidirectional tuning of JJ conductance. Combining both techniques could pave the way for a robust, scalable and iterative frequency targeting approach which significantly reduces fabrication overhead.

6.2. LASER ANNEALING

Laser annealing (LA) of JJs has emerged as a facile and innovative tool for targeting qubit frequencies with less than 1% dispersion in JJ conductance in $1\ \mathrm{cm}^2$ chips, a feat that has eluded state-of-the-art microfabrication techniques. The operating principle of LA is based on locally heating the substrate below the fabricated JJs thereby decreasing barrier transparency due to a combination of physical and chemical modifications to the AlO_x layer. From the perspective of a fabrication engineer, this method offers twin benefits of significantly reducing the need for multiple RT statistics to identify the precise JJ parameters corresponding to the target f_q and improving throughput of viable devices from a fabrication round for cryogenic characterization. It was first demonstrated on individual Nb/Al-AlO_x/Nb JJs for localized trimming of junction conductance using Ar^+ laser at wavelength $\lambda = 514.5\ \mathrm{nm}$ [294]. Almost a decade later, we showed the first proof-of-concept of LA as an effective tool to circumvent fabrication-limited qubit frequency targeting precision using tunable transmons [295]. Since then, the scalability of this technique to mitigate frequency collisions in CR-gate architecture by narrowing the as-fabricated frequency targeting precision from $132.3\ \mathrm{MHz}$ to $\sim 14\ \mathrm{MHz}$ post LA was demonstrated by IBM [133, 296]. The extensibility of LA to wafer-scale frequency targeting has also been demonstrated, the limiting factor envisaged in this case is the ageing of junctions post on-demand annealing [297]. However, as stated before, annealed JJs tend to be more resilient towards ageing compared to as-deposited junctions. In conjunction with post-fabrication trimming of resonator frequency using shorted airbridges, we have shown that LA on flux-tunable transmons improves the average readout fidelity on a Surface-17 device up to 98.9% [252]. However, a drawback of this technique as shown so far is that qubit frequency can only be monotonically

lowered.

6.2.1. OPTICS FOR LASER ANNEALING

Localized thermal annealing of JJs is achieved by designing the optical path of a high-power laser spot directed towards the device. The requirements for a laser annealing setup are determined by certain crucial parameters such as the dimensions of the JJs used, material choice of the device substrate such as sapphire (Al_2O_3) or Si and the desired range and precision of tunability of JJ conductance. Additional considerations include laser safety, setup design ergonomics and levels of automation. Continuous wave (CW) lasers are preferable for this application over pulsed lasers in order to have higher control over trimming JJ conductance. The choice of laser wavelength (λ) depends on the absorption coefficient of the substrate for efficient conversion of incident photons to heat. The relatively broad absorptance of Si between $1.1-4.0$ eV $(300-800$ nm) [298] allows for a wide selection of commercial diode-pumped solid-state (DPSS) lasers to be used for LA applications. A lower wavelength laser ranging between $375-532$ nm is therefore optimal for increasing the surface temperature of Si. Performing LA on SQPs fabricated on sapphire is more challenging as it is transparent from 150 to 6000 nm [299].

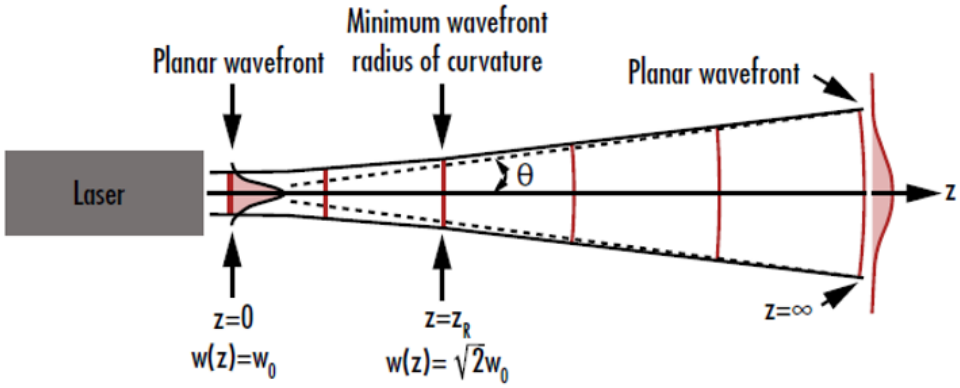


Figure 6.3: Schematic of curvature of the wavefront of a Gaussian beam emitted by a laser source. It is near-zero when it is both very close and very far away from the beam waist w_0. Reprinted with permission from Edmund Optics [300]

Achieving a high precision below 30 MHz and large range of post-fabrication tuning of qubit frequency up to 300 MHz will require at least a Class 3B ($5-500$ mW) or 4 (>500 mW) laser with the laser beam focused to a spot size ranging between $2-50$ μm at the target device. The ideal propagation of a laser beam has a Gaussian beam profile, defined by its beam waist or radius (w_0, unit μm), Rayleigh range ($z_R = \pi w_0^2/\lambda$, unit μm) and beam divergence ($\Theta_0 = \lambda/\pi w_0$, unit mrad). These parameters are typically specified by the manufacturer of a laser source along with the central wavelength (λ), range of output power P_L and transverse mode of the laser. The beam width ($w(z)$) as it exits the laser emitter is the diameter of the beam along

its propagation or optical axis (z axis) where the intensity drops to $1/e^2$ times the maximum value, related to the w_0 and z as

$$w(z) = w_0\sqrt{1+\left(\frac{z}{z_\mathrm{R}}\right)^2}.$$

The minimum value of $w(z)$ is W_0 at the beam waist ($z=0$), reaches $\sqrt{2}w_0$ at $z=\pm z_\mathrm{R}$ known as the depth-of-focus and increases linearly with z [301]. The optical intensity is the power per unit area of a laser which is a function of the axial and radial positions z and $d=\sqrt{x^2+y^2}$ respectively

$$I(z,d) = I_0\left[\frac{w_0}{w(z)}\right]^2 \exp\left[-\frac{2d^2}{w^2(z)}\right],$$

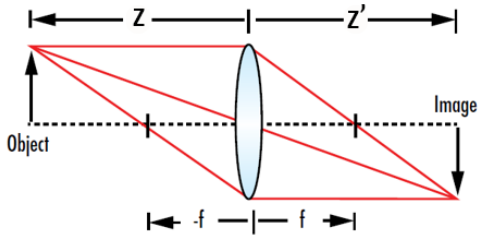
where I_0 is the maximum value of intensity at $z=0$. For a CW laser, it is related to the laser optical power as

$$P_\mathrm{L} = \frac{\pi w_0^2}{2}(1-\eta_\mathrm{L})I_0, \tag{6.1}$$

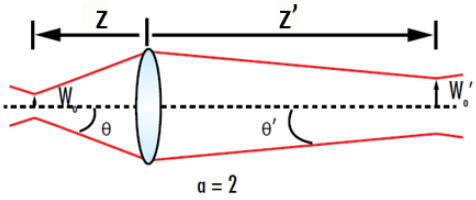
where η_L is the total power loss factor due to absorption, scattering, reflectivity and/or transmission of the laser power due to optical components such as steering mirrors, beam splitters or dichroic mirrors and focusing lenses.

A standardized measure of the laser beam quality, termed the M^2 factor, compares the deviation of a real laser beam with that of a diffraction-limited Gaussian beam. It signifies the limit to which a laser beam can be focussed and the optical intensity that can be achieved, related to the divergence angle as $\Theta = M^2\lambda/\pi w_0$ [302]. If the M^2 factor for a laser source is not provided by the manufacturer, it can be experimentally determined by measuring the beam diameter at various positions within and beyond $2z_\mathrm{R}$ of the focal point using a beam profiling camera. All single transverse electric mode (TEM_{00}) diode laser beams are considered quasi-Gaussian with $M^2 < 1.5$. However, high-power laser beams contain multiple TE modes due to the larger width of the diode active layer and therefore cannot be as tightly focussed compared to TEM_{00} beams. Therefore striking a balance between the total output laser power and achievable beam spot size is an important consideration for targeting the desired range of conductance change ($\Delta\mathrm{G}$).

Finally, choosing the right optics for constructing a simple and cost-effective LA setup from a dizzying variety of optical components is challenging from the perspective of a fabrication engineer inexperienced in optical physics. The primary consideration in this regard is to optimize the number and quality of optical components to manipulate the laser beam towards the device with the desired intensity and beam radius in order to minimize the net losses to P_L. An infinity-corrected microscope objective lens is one of the most widely used optics for laser-focusing applications as it allows for additional optical components such as beam expanders, beam shapers and laser filters to be placed into the optical path. In the paraxial approximation, the final radius of a collimated laser beam focused using a converging lens (plano-convex or double-convex lens) of focal length f and numerical aperture (NA) is $w_0' = \Theta f$, since the product of a ray angle and image size is constant,



(a) Schematic describing the thin lens equation. Reprinted with permission from Edmund Optics [300]



(b) Schematic of Gaussian beam propagation using the thin lens approximation to calculate the location z' of the output beam waist when the distance between the object and the lens z and the focal length f are known. In this case, the object refers to the input laser beam waist w_0. Reprinted with permission from Edmund Optics [300]

known as the optical invariant [303]. However converging lenses introduce inherent spherical aberrations when focusing the beam, leading to blurring. Hence an aspheric lens must be added to the optical path prior to the imaging lens, which improves aberration correction and enables designing high light throughput in low $f/\#$ [1] systems while simultaneously maintaining good image quality [304]. It can also be used as a collimating lens for laser sources with a large Θ such as fibre-coupled lasers and pigtailed laser diodes. The dioptric or optical power of a single lens (P_o), a measure of the focusing power as a function of the curvature of a lens, is equal to the reciprocal of the focal length $P_o = 1/f$. For a system of two convex lenses such as a collimating lens and a focusing lens of focal length f_1 and f_2 respectively, the dioptric power then is simply the sum of the reciprocal of the focal lengths $P_o = 1/f_1 + 1/f_2$. Using the thin lens approximation for a Gaussian beam [305], the distance between the image, i.e., the focused laser spot and the lens, is related to z_R:

$$\begin{aligned} \frac{1}{z'} &= \frac{1}{z} + \frac{1}{f} \\ &= \frac{1}{z + \frac{z_R^2}{z+f}} + \frac{1}{f}. \end{aligned} \tag{6.2}$$

The magnification m of a lens, which is the ratio between the height of the image and the height of the object can be expressed in terms of f and z_R as

$$m = \frac{w_0'}{w_0} = \frac{1}{\sqrt{\left(1 - \frac{z}{f}\right)^2 + \left(\frac{z_R}{f}\right)^2}}. \tag{6.3}$$

Under conditions where $z \ll z_R$ and $z \gg z_R$, Eq. 6.2 and 6.3 reduce to $z' \approx f$ for both cases while $m = f/z_R$ for the former condition and $m = f/|z|$ respectively.

[1] Pronounced F-number, it is the ratio of the focal length of the lens to the effective aperture diameter.

6.3. EXPERIMENTAL SETUP AND RESULTS

To induce $\Delta G \geq 50\,\mathrm{MHz}$ in JJs fabricated on high-resistivity Si substrates, the annealing temperature must be above 160 °C. Therefore the uncertainty in designing a LA setup lies in determining the required energy density $E_L = I\tau$, where τ is the irradiation time. Prior work on LA showed that Nb-based JJs fabricated on Si substrate irradiated for 30 s with a laser intensity of $I = 200 - 220\ \mathrm{mW/cm^2}$ resulted in a 40% decrease in junction critical current I_c, which corresponds to a temperature range of 160–170 °C [306]. Using this value as a baseline, we iterated experiments using three different configurations of optics listed chronologically.

6.3.1. GREEN LASER SETUP

This is the first iteration of LA experiments performed using a free-space single longitudinal mode $\lambda = 532\ \mathrm{nm}$ diode laser source with $P_{L,max} = 100\ \mathrm{mW}$.[2] The optical path as shown in Fig. 6.5(a) consists of the laser source, steering mirrors and optional optic fibre output enclosed in a dark box to minimize stray reflections. The beam is passed through a cube-mounted pellicle beamsplitter (45:55 R:T). The transmitted beam passes through an infinity optical system consisting of a tube lens and a 50X objective lens. The reflected beam is captured by the CCD camera to monitor the beam position with respect to the device. The DUT is attached to a custom PCB and mounted on a cryostat with an XY motorized stage. The smallest beam diameter achieved with this setup is $2w_0' \sim 8\ \mu\mathrm{m}$ with a final output power $P_L = 40\ \mathrm{mW}$ delivered at the device. Since the SQUID loop dimensions exceed that of the laser spot, each JJ is individually laser-annealed for a nominal τ. JJs are characterized by RT conductance measurements using a manual probe station pre- and post-LA not integrated with the optical apparatus. Two datasets of test JJs with bridgeless o-type junctions obtained from this setup show the effect on ΔG on varying junction dimensions and τ. From Fig. 6.5(b), it is observed that $\Delta G\%$ is relatively constant on sweeping the designed electrode widths with a fixed $\tau = 5\ \mathrm{min}$ for each JJ, with the mean $\mu_{\Delta G} = -8.2\%$ and standard deviation $\sigma_{\Delta G} = 0.7\%$. Sweeping τ from $3 - 20\ \mathrm{min}$ results in larger $|\Delta G|$, enabling frequency trimming (Δf_q) in the range of $30 - 400\ \mathrm{MHz}$. Fig. 6.5(c) shows a sweep of τ on JJs subjected to simulated AB annealing, where ΔG_{LA-AB} shows a power-law dependence.

6.3.2. VIOLET LASER SETUP

This is our first home-built LA setup in collaboration with TNO, Delft using a multi transverse mode $\lambda = 405\ \mathrm{nm}$ Ø5.6 mm transistor-outline-can (TO-can) laser diode (Nichia NDVl7116) with $P_{L,max} = 600\ \mathrm{mW}$, shown in Fig. 6.6(a). The diode is connected to an external dc power supply unit, with operating range of $3 - 6\ \mathrm{V}$ forward voltage and $150 - 600\ \mathrm{mA}$ current for diode activation. The diode is additionally enclosed in a passive Al heat sink and mounted with a 5-mm collimating lens[3] in front

[2] Optical table setup access provided by Zwiller Lab, Quantum Transport group, TU Delft.
[3] Details of the lens not specified by manufacturer

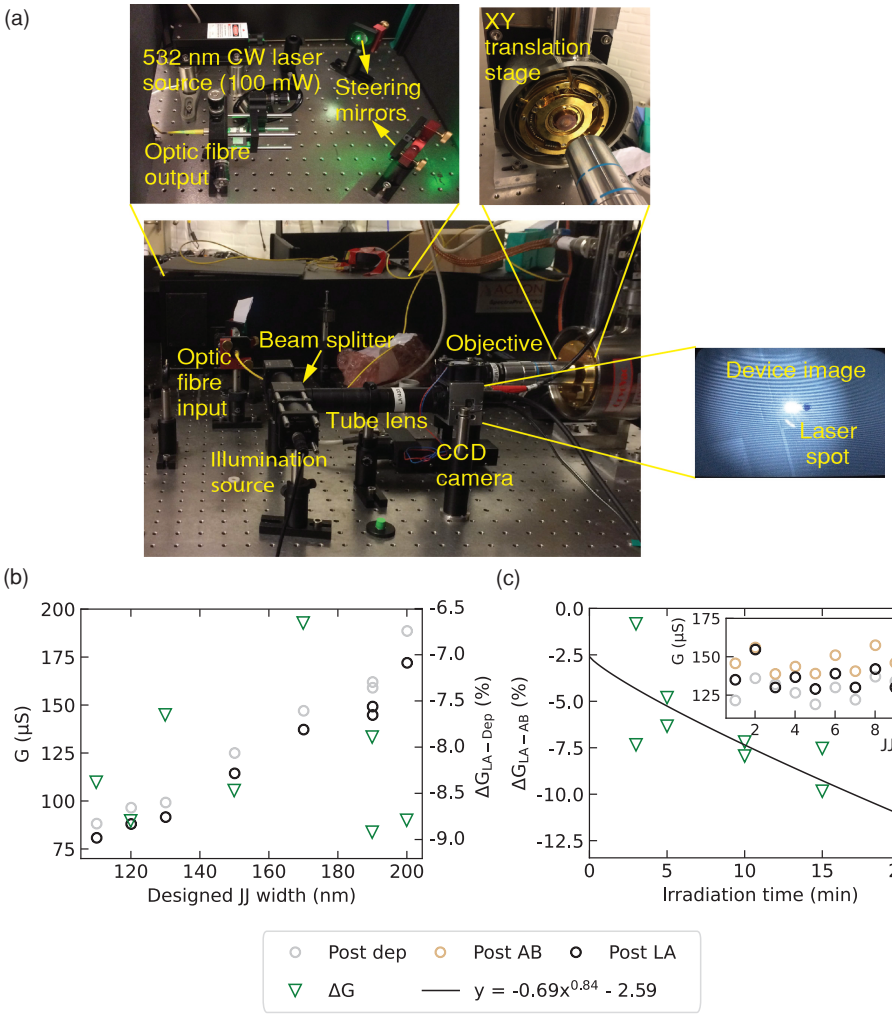


Figure 6.5: (a) Images of the 532-nm Green Laser Setup optical table. Post-fabrication trimming of conductance in o-type JJs RT conductance measurements. (b) Dual-axis plot of conductance (ΔG) (left y axis) and % change in (right y axis) of JJs laser-annealed immediately post deposition for $\tau = 5$ min vs. JJ width. (c) ΔG % between laser annealing (LA) and airbridge (AB) annealing of JJs of nominal widths 150 and 160 nm vs. irradiation time τ. The data is fitted with a power-law distribution shown by the black line. Inset: JJ conductance values acquired sequentially post JJ deposition (grey), post-AB annealing (beige) and post-LA (black).

of the emitter and is cooled by a mini brushless ventilator during operation. The laser optical path is arranged compactly in this prototype on a 90 x 60 cm breadboard with

two Al-coated steering mirrors (Thorlabs PF10-03-G01 Ø25.4 mm) to manipulate the beam towards a vertically mounted beam-focusing assembly held in position by a Ø1.5" dynamically damped post. The incoming beam is deflected towards the device by a rectangular long-pass dichroic mirror with a cut-on wavelength at 425 nm (Thorlabs DMLP425R) mounted at a 45° angle of incidence using a cage cube. It is necessary to ensure the laser beam is centred at the dichroic mirror in order to minimize stray reflections. A 10X long working distance infinity-corrected objective lens (Mitutoyo 10X EO M Plan Apo) is mounted below the cage cube facing the sample stage. A tube lens (Edmund Optics MT-4 accessory tube lens) is positioned above the cube to focus the image on a CCD camera (Thorlabs DCU224M, monochrome) mounted at the top of the column using a camera extension tube (Edmund Optics C-mount camera 152.5 mm extension tube).[4]

This configuration limits degrees of freedom in orientations of the optics, which is advantageous in terms of reducing the effort to align the laser spot and variability in final P_{L} and ω_0' during every usage. The total contribution to the laser power losses due to absorption by the steering mirrors, dichroic mirror and objective lens is $\eta_{\mathrm{L}} = (1 - R_{\mathrm{M}}^2 \times R_{\mathrm{D}} \times T_{\mathrm{O}})$, where $R_{\mathrm{M}} > 90\%$, $R_{\mathrm{D}} > 95\%$ are the average reflectance values of the Al mirror and dichroic mirror respectively and $T_{\mathrm{lens}} \sim 80\%$ is the transmission at 405 nm, giving a total predicted $\eta_{\mathrm{L}} \sim 38\%$. The sample stage used in this setup is a manual XYZ stage with 5 mm translation in each axis. The sample is fixed below the objective by taping it to a bare PCB for thermal isolation from the stage. The vertical assembly along with the beam manipulation components are enclosed in all directions by metallic laser safety barriers. The JJs are characterized by RT conductance measurements using a manual probe station pre- and post-LA not integrated with the optical apparatus. The incident P_{L} on the device is controlled by manually changing the current applied to the diode, which is placed outside of the optical path. The smallest beam diameter achieved with this setup is $2w_0' \sim 5\ \mu\mathrm{m}$ with output power $P_{\mathrm{L}} = 350\ \mathrm{mW}$ delivered at the device. The laser intensity I is varied by changing $2w_0'$ while keeping the output laser power constant at $350\ \mathrm{mW}$, as shown in Fig. 6.6(b) by either irradiating both JJs in the SQUID loop simultaneously using a large spot size $2w_0' \approx 30\ \mu\mathrm{m}$ or individually with a small spot size of $2w_0' \approx 10\ \mu\mathrm{m}$. The laser intensity obtained from the large spot ($\approx\leq 50\ \mathrm{mW/cm^2}$) constitutes a lower bound for annealing i-type junctions as ΔG is negligible irrespective of the irradiation time τ. On the other hand, the magnitude of ΔG for the $\approx 10\ \mu\mathrm{m}$ spot shows a power-law dependence with τ. This setup therefore allows for a significantly larger tuning of ΔG corresponding to over $1.5\ \mathrm{GHz}$ trimming of f_{q}. However large deviations in ΔG (highest $\sigma_{\Delta G} = 10.7\%$) with the small spot size is observed, which is likely explained by mechanical instabilities arising from the lack of features such as motorized stage, vacuum chuck for mounting the sample and insufficient vibration isolation of the optical table. With smaller spot sizes the resolution of the objective further limits accuracy of the laser spot positioning over the junctions. Lastly, this setup is not equipped with beam shaping optics to produce a circular flat top Gaussian profile [5]

[4] Connecting multiple optical components together also require special adapters, details of which are omitted here.

[5] Flat top laser beams have a constant irradiance profile throughout the cross section of the spot, at the

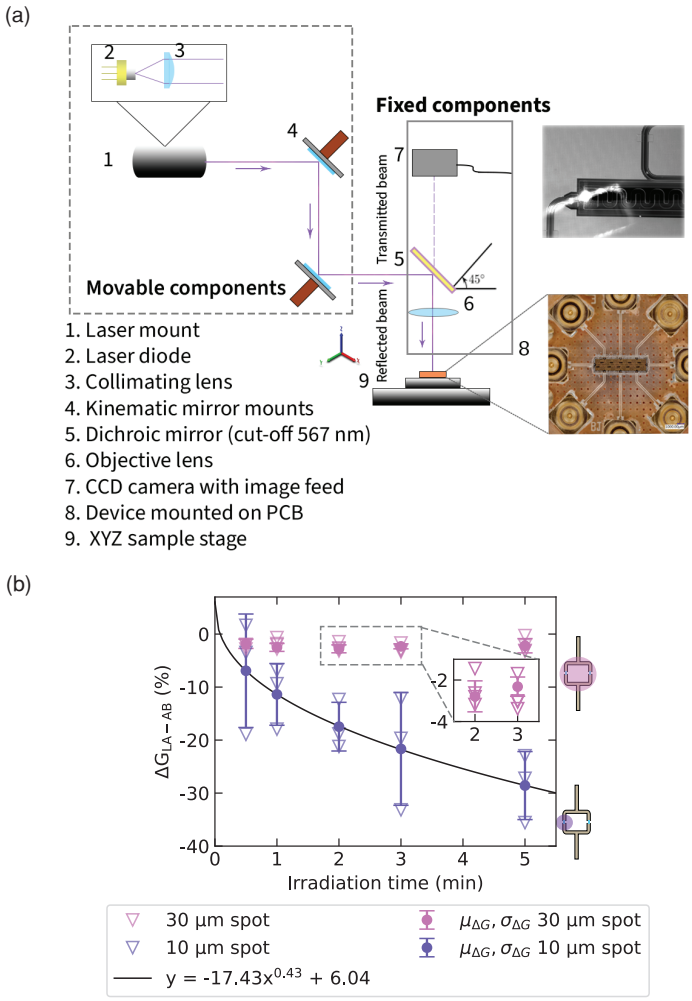


Figure 6.6: (a) Schematic of the Violet Laser Setup. (b) Post-fabrication trimming of junction conductance in i-type JJ pairs using the 405-nm Violet Laser Setup. The laser power is constant at $P_{\mathrm{L}} = 350\ \mathrm{mW}$, instead the intensity I is varied by defocusing the laser spot size as shown by the schematic. With the $30\ \mu\mathrm{m}$ spot size, both JJs in the SQUID loop are irradiated simultaneously, whereas each JJ is irradiated separately for the dataset obtained using the $10\ \mu\mathrm{m}$ spot.

ideally required for narrowing $\Delta\mathrm{G}$ spread.

cost of higher optical system complexity.

6.3.3. APS-TASQ SETUP

The Automated Probe Station for Thermal Annealing of Superconducting Qubits (APS-TASQ) is an upgraded version of the Violet Laser Setup retaining the same dimensions and optical path. It is equipped with a Class 4 multi transverse mode laser with $\lambda = 405 \pm 6$ nm diode laser with $P_{\mathrm{L,max}} = 1000$ mW (CNI Lasers MDL-III-405). The dedicated power supply unit included with the laser source operates at currents ranging between $50 - 80$ mA, with the diode activation threshold at ~ 300 mA. The final focused spot size obtained using this laser source is $2w_0' \approx 45\ \mu$m, which allows only for simultaneous irradiation of both junctions in the SQUID loop. The most significant improvement in this iteration of the experimental setup is the ability to tailor the LA of JJs by means of closed-loop feedback of 4-point RT conductance measurements integrated with the optical apparatus. This is achieved by consecutive cycles of measurementand laser annealing of each junction pair in order to controllably shift RT conductance to a predefined target value. It is not possible to measure the JJ while it is being irradiated due to the risk of inducing pinhole defects in the tunnel barrier [307]. The algorithm implemented in the active feedback control assumes that the irradiation time τ as the only control parameter which results in a monotonic decrease in junction G from the initial value G_{init}. On defining a target conductance G_{target} and a nominal maximum irradiation time τ_{max}, the normalized tuning behaviour is expressed as

$$y(\tau \rightarrow \tau_{\mathrm{max}}) = (G_{\mathrm{target}} - G_{\mathrm{init}})/G_{\mathrm{init}}. \tag{6.4}$$

When $G_{\mathrm{target}} < G_{\mathrm{init}}$, $y(\tau) \geq$G$_{\mathrm{target}}$ or $y(\tau_{\mathrm{max}}) <$G$_{\mathrm{target}}$, the automated measurement protocol ceases to anneal the JJs. In order to predict τ_{max} for $G_{\mathrm{init}} \rightarrow G_{\mathrm{target}}$, a fit function defined as a power-law distribution is defined

$$f_{a,b}\tau : a\tau^{1/b}, \tag{6.5}$$

where a and b may slightly vary between junction pairs due to tunnel barrier inhomogeneities. This is addressed by employing an iterative method for optimizing these parameters, which acts an as unsupervised training protocol for closed-loop laser annealing, thereby significantly improving the targeting precision [308].

Fig. 6.7 illustrates the additional hardware integrated this setup to facilitate wafer-scale automated probing and improvement in LA accuracy. We add a Ø1" optical beam shutter (Thorlabs SH1/M1) to the laser path with a dedicated benchtop controller (Thorlabs SC10) with 10 ms shutter closing time. The beam shutter is used to automate the exposure time of the laser beam, thereby eliminating the need to manually change the current on the PSU, which contributes to errors arising from fluctuations in P_{L} while cyclically annealing junctions. The manual XYZ stage is replaced by a motorized XY scanning stage (Thorlabs MLS203-1) with a 250-mm translation distance and a position accuracy of < 3 µm. To facilitate compact arrangement of the setup, the probing apparatus consists of four impedance-controlled flat-tip tungsten ceramic-blade needles with 19 µm tip diameter (FormFactor SP-DCQ-04-58) mounted on a probe card in a collinear configuration. The probe card is affixed to a 3-D printed plastic cantilever with an 8° bend at the front-

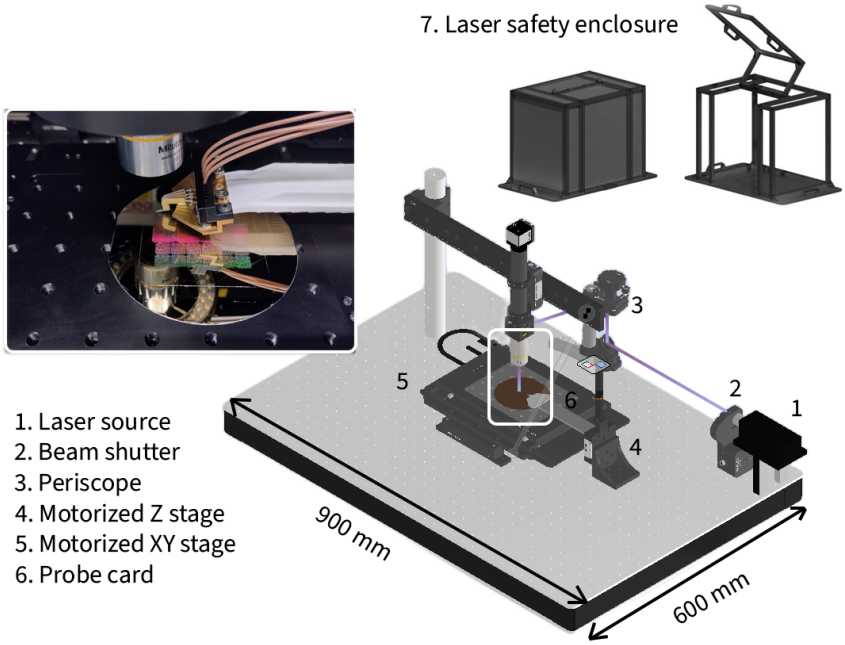


Figure 6.7: 3D drawing of the APS-TASQ setup components. The violet line traces the optical path of the laser source towards the DUT.

facing end to facilitate landing the probe needles on a variety of chip layouts, including planar octobox, Surface-7 and Surface-17 SQPs mounted on connectorized PCBs with at least 1 mm clearance between the probe card and the SMP connectors. The plastic cantilever is mounted on a motorized Z stage (Thorlabs MT1-Z8) with a 12 mm travel range. Two technical issues with this component concerning the velocity ripple at operational speeds above 2.6 mm/s and loss of motion due to backlash are addressed by operating the motor at speeds below 2.3 mm/s and by setting a landing depth at least 200–300 µm lower than the initial calibrated height of a NbTiN-metallized sample. These measures ensure uniform contact between the probe needles and the wafer surface, under the assumption that the specified landing depth is within the elastic deformation limit of the needles [6]. The safety features of the APS-TASQ setup include a robust laser enclosure using off-the-shelf 25-mm construction rails and slotted corner cubes from Thorlabs, with an opening hatch integrated in front of the frame mounted on hinges at the top of the enclosure. The frames of the enclosure are fitted with black hardboard-based laser safety panels (Thorlabs TB-4) which minimize exposure of the DUT to ambient light as well as absorbing stray reflections from the laser source. The opening hatch is connected to a magnetic interlock which acts as a safety feature by disconnecting

[6]The elastic deformation limit of the needles depends on the material being probed

the power supply connected to the laser PSU when opened in the middle of the annealing operation. This is necessary to improve the safety of the APS-TASQ setup from a Class 4 to Class 1 category. Details about the software control and design of the user interface are described in the chapter SOM 6.7.1. The success of the APS-TASQ setup is demonstrated by the deployment of closed-loop feedback between RT G measurements and automated laser irradiation on connectorized Surface-17 devices, demonstrated in Fig. 6.8. Due to feedback control of the target conductance, a targeting precision $\sigma_f \sim$ 14 MHz has been demonstrated from RT measurements [308].

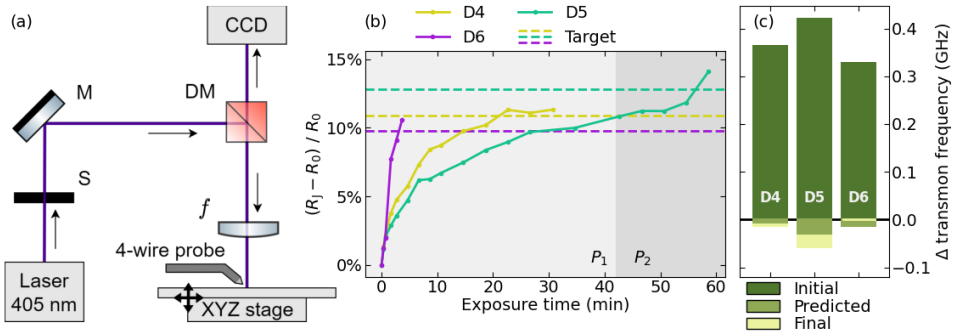


Figure 6.8: Demonstration of closed-loop laser annealing of junctions embedded in Surface-17 devices. (a) Alternative schematic of the optical configuration of the laser setup, shown earlier in Fig. 6.6(a). (b) The relative change in 4-wire resistance between the final vale R_J and initial value $R0$ for three Q_H transmons (D4, D5 and D6) is plotted as a function of incident laser power and exposure time, with the target resistance range indicated by horizontal lines. The incident laser power is maintained at $P1 = 170$ mW ($P2 = 200$ mW) in the light (dark) grey window. (c) The deviation of qubit frequency from target, σ_f is the highest post initial cooldown shown in dark green, post laser annealing the Δf_q from RT-predicted values and second cooldown is significantly diminished. Figure reprinted from Valles *et al.* (2023) [252] under Creative Commons CC BY license managed by AIP Publishing.

6.4. TARGETING PRECISION OF LASER ANNEALING

We perform laser annealing experiments using the Violet Laser Setup to quantify the frequency targeting precision between an expected f_q (in this case the predicted value $f_{q,pred}$) and the measured f_q (in this case the measured value $f_{q,meas}$) denoted $\sigma_f = \sqrt{\Sigma\left(f_{q,meas} - f_{q,pred}\right)^2 / N}$. Using a device comprising multiple independent, flux-tunable transmons, we show proof-of-concept experiments combining cryogenic characterization namely resonator and qubit spectroscopy and time-domain measurements prior to and post LA. We implement a device design with relatively simple and compact qubits, nicknamed *Zapmon* consisting of interdigitated capa-

citor pads shunting a SQUID loop with symmetric i-type JJs. The device layout incorporates dedicated flux-bias lines for six out of ten qubits as shown in Fig. 6.9 and Table 6.2. The initial target f_q are estimated based on input $E_c = 285$ MHz and $M = 140$ GHz/mS. All readout resonators are capacitively coupled to the feedline in the hanger configuration with $Q_e = 7000$ and fixed coupler gap $w_g = 4$ μm. Additionally a witness resonator with a designed frequency $f_{r,des} = 8.0$ GHz, $Q_e = 10^6$ and $w_g = 12$ μm is added to extract ν_p. At the designed $\kappa/2\pi = 1$ MHz, $\Delta_{r-01} = 1.0$ GHz and coupling strength $g = 25$ MHz gives $T_1^{\text{Purcell}} \approx 254$ μs and $n_c \approx 400$.

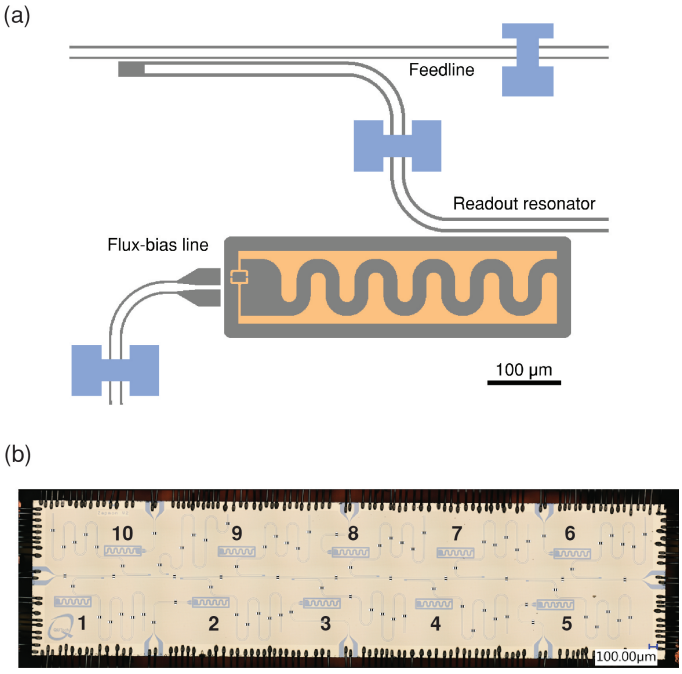


Figure 6.9: (a) CAD drawing of Zapmon qubit with i-type JJs and interdigitated capacitor pads. The $\lambda/4$ readout resonator are capacitively coupled to both the feedline and qubit. (b) Full chip image of a Zapmon device consisting of 10 qubits, of which five possess dedicated flux-bias lines.

Qubit	1	2	3	4	5	6	7	8	9	10
$f_{q,des}$ (GHz)	6.0	6.1	6.2	6.3	6.4	6.5	6.6	6.7	6.8	6.9
FBL	–	✓	✓	–	✓	✓	–	✓	–	✓
$f_{r,des}$ (GHz)	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	7.8	7.9
W_t (nm)	80	84	88	92	96	100	104	108	112	116

Table 6.2: Design and fabrication parameters of the 10-qubit Zapmon layout preserved across the three measured devices.

The devices are fabricated using the standard planar fabrication process described in Chapter 3. Two dies each containing six repeats of the 8×2 mm^2 Zapmon device are fabricated. For each device, the RT conductance measurements are recorded after wirebonding and immediately prior to the 1^{st} cooldown. Each device is mounted on a gold-plated copper cold finger and shielded as described in section 3.3.7. A total of three full-yield Zapmon devices (device **A**, **B** and **C**) are characterized for this experiment[7]. The RR frequencies are identified within a scanning range of $6.9 - 8.1$ GHz using a Rohde & Schwarz vector network VNA. The $f_{\mathrm{r,meas}}$ are observed to be evenly spaced, however the frequencies are globally shifted by $f_{\mathrm{r,meas}} - f_{\mathrm{r,des}} \approx 100$ MHz. The internal quality factor is extracted from the weakly-coupled test resonator in device following the procedure described in [103] is $Q_{\mathrm{i}} \geq 5 \times 10^5$ in devices **A** and **C**. From measurements of the readout resonator power shifts, 28 out of 30 qubits are identified. To measure qubit frequencies, a variable frequency spectroscopy tone f_{spec} is sent through the feedline followed immediately by the readout tone. At $f_{\mathrm{spec}} = f_{01}$, the steady-state population of the $|1\rangle$ state is a Lorentzian visible as a peak in the readout. The lower bound of full width at half maximum of the peak is limited by T_2 which increases with the spectroscopy power P_{spec}. The response of qubits to dedicated FBL are measured to determine sweetspot f_{q} closest to zero current in order to minimize thermal load on the device from over 60 measurements of resonator-flux line sweeps and qubit spectroscopy as a function of varying the current in FBL. Even qubits without dedicated FBL are observed to be frequency tunable by nearest-neighbour lines over 100 MHz. To estimate the values of anharmonicity and thereby experimentally determine E_{c} and E_J from Eq. 2.29, either high power spectroscopy above $P_{\mathrm{spec}} > 0$ dB to induce 02 transition (device **A**) or two-tone spectroscopy (devices **B** & **C**) is performed. Finally we perform time-domain experiments to measure qubit T_1 and T_2.

The $f_{\mathrm{q,pred}}$ values prior to 1^{st} cooldown are calculated using initial designed parameters of $E_{\mathrm{c}}/h = 285$ MHz and $M = 140$ GHz/mS. Immediately after warming up the fridge, RT conductance measurements are obtained before irradiating each qubit with nominal laser parameters described in Table 6.3. The chip is then allowed to cool off with a settling time of 5 min after annealing and prior to RT-probing the qubit. The w_0' used for annealing 5 qubits in Device A is larger than the SQUID loop dimensions, allowing for both JJs to be irradiated simultaneously. Since smaller spot sizes are used in 2 qubits in device **A** and for all qubits in devices **B** and **C**, each JJ is irradiated separately, each for 2 min. The samples remain mounted on the thermalization plate during LA, in order to minimize handling of the sample prior to the 2^{nd} cooldown. The same measurement procedure is repeated as in 1^{st} cooldown, however this time $f_{\mathrm{q,pred}}$ is calculated from the E_{c} and E_J extracted from the qubit anharmonicity measured in the 1^{st} cooldown.

A summary of the measured parameters is presented in Table 6.3. Several interesting observations can be gleaned from these results. Firstly, the inverse dependence of laser I on f_{q} is clearly observed from Fig. 6.10(a), with device **A** (**C**) showing the lowest (highest) Δf_{q} among the annealed qubits. We indeed observe that LA is a spatially confined process as there is minimal deviation of f_{q} among

[7] Measurements performed by Luc Janssen and Filip Malinowski, DiCarlo lab, QuTech.

Parameter	Device A	Device B	Device C
# qubits initial	10/10	8/10	10/10
σ_f 1^{st} cooldown (MHz)	28.4	43.6	40.1
# qubits LA	7/10	6/10	5/10
P_{L} (mW)	345	350	360
$\pi w_0'^2$ ($\times 10^{-6}$cm^2)	14.8 1.2	1.2 –	0.4 –
I (mW/cm^2)	23.6 297.8	297.8 –	823.5 –
ΔG [L] (μS)	4.7 ± 3 -10.5 ± 3.5	-11.4 ± 1.4 –	-25.7 ± 13.7 –
Δf_{q} [L] (MHz)	-81.2 ± 29.7 -244.0 ± 32.5	-281.8 ± 25.9 –	-766.0 ± 332.2 –
σ_f [L] 2^{nd} cooldown (MHz)	69.0	23.7	221.7
σ_f [C] 2^{nd} cooldown (MHz)	29.0	25.3	7.6

Table 6.3: Summary of LA statistics from each Zapmon device. # initial and # LA are the number of qubits cryogenically characterized in the 1^{st} cooldown and 2^{nd} cooldown respectively. The laser-annealed junctions, labelled [L] (See chapter SI 6.7) are irradiated for a duration of $\tau = 2$ min by varying I using three different spot sizes. The areas of the spot are calculated from images acquired with the CCD camera using ImageJ. In device **A**, two qubits are annealed using a smaller spot size, with each JJ in the SQUID loop irradiated separately. The frequency targeting precision σ_f is the standard deviation of difference between $f_{\mathrm{q,meas}}$ and $f_{\mathrm{q,pred}}$, calculated for both 1^{st} and 2^{nd} cooldowns. The σ_f in 2^{nd} cooldown is calculated separately for control [C] and annealed [L] qubits. The Δf_{q} (ΔG) are the mean and standard deviation of the difference in $f_{\mathrm{q,meas}}$ (G) post and prior to LA.

control qubits between successive cooldowns. The $f_{\mathrm{q,meas}}$ from 1^{st} cooldown show relatively good agreement with $f_{\mathrm{q,pred}}$ with a cumulative $\sigma_f = 14$ MHz across all the devices, as shown by the square data points in Fig. 6.10(b). The σ_f in 2^{nd} cooldown, which serves as a gauge of the accuracy and precision of the annealing process is significantly higher in all the devices in 2^{nd} cooldown for several reasons. The standard deviation of ΔG and consequently Δf_{q} is the highest in device **C**, which is likely due to the limitation in resolution of the microscope to accurately align the smallest laser spot on the JJ and poor isolation of the Violet Laser setup from mechanical vibrations leading to drifting of the laser spot during the annealing process. The higher σ_f of device **A** likely originates from errors during RT measurements due to contact resistance between the probe needles and the narrow Zapmon capacitor pads. This may also explain the lower $f_{\mathrm{q,pred}}$ compared to $f_{\mathrm{q,meas}}$ in qubits 2, 7 and 9 measured in the 2^{nd} cooldown. Device **B** shows the lowest σ_f among the annealed qubits, 50% lower than the desired targeting precision of 50 MHz. Certain anomalies are observed in device **C**, notably the ≥ 200 MHz deviation between $f_{\mathrm{q,pred}}$ and $f_{\mathrm{q,meas}}$ in qubits 5 and 7 and the large relative change in E_{c} and M in qubit 7 post

LA. This maybe either due to human error or insufficient settling time for the device, resulting in the measurement of a higher G while the JJs are still hot. We clarify that the loss of qubit yield in device **C** is not caused by the high laser P_{L}, as two qubits were shorted during probing prior to annealing. The effect of LA on qubit T_1 and T_2, plotted in Fig. 6.11 is uncertain with some qubits being adversely impacted, while qubit 9 in device **A** and 5 & 7 in device **C** show substantial improvement in T_1 in the 2^{nd} cooldown. These qubits also show the largest relative change in anharmonicity between 1^{st} and 2^{nd} cooldowns, aside from qubit 9 in device **C**.

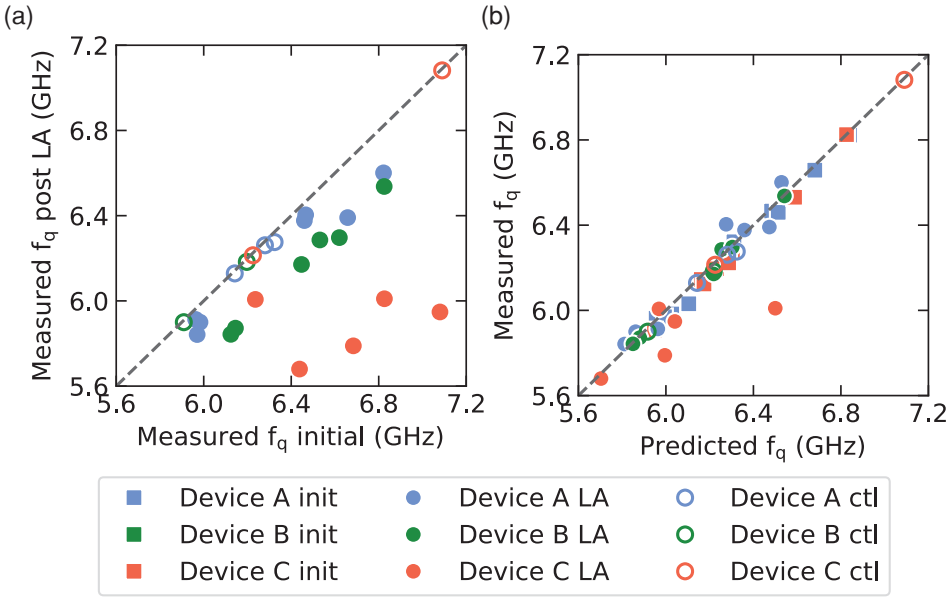


Figure 6.10: (a) Comparison of measured f_{q} of the three Zapmon devices before and post LA. The hollow circles are control (ctl) qubits which are not subjected to LA. The devices are annealed using different intensities with a constant irradiation time of 2 min per JJ as described in Table 6.3. (b) Comparison of measured and predicted f_{q} of the Zapmon devices from the initial characterization (init) and post LA.

6.5. RAPID THERMAL ANNEALING

This section details the experiments performed to investigate the experimental parameters necessary to effect on-demand anti-ageing of JJs using rapid thermal annealing [309]. This process is routinely employed in the semiconductor industry to instantaneously heat materials to temperatures over $1000\ ^{\circ}\mathrm{C}$ followed by a relatively slower cooling period to minimize cracking or dislocations due to thermal shock. Unlike furnace annealing which is used to heat large batches of samples

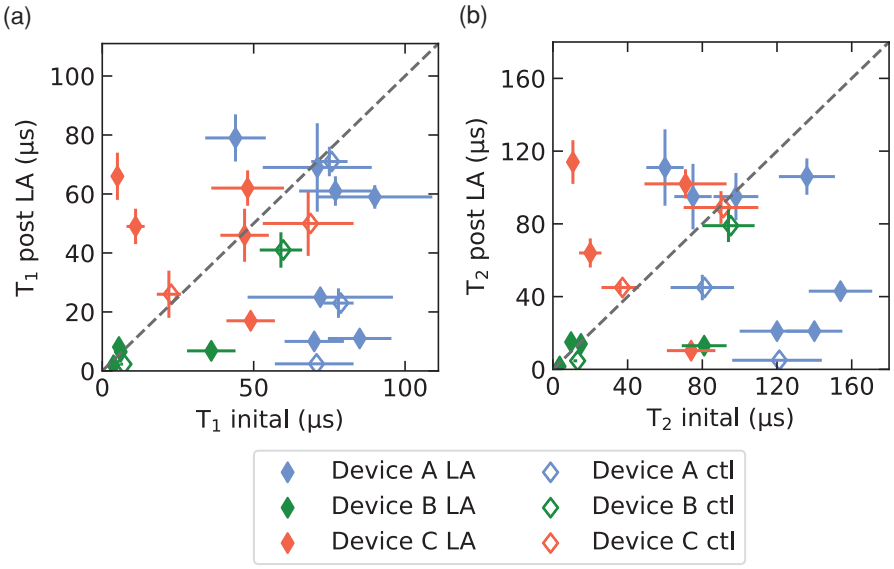


Figure 6.11: Plots of (a) T_1 (b) T_2 of Zapmon devices measured from before and post LA.

over a longer time period usually between 120–240 min, RTA is usually confined to processing individual samples in the order of 2–10 min. RTA differs from laser annealing in two ways; the entire device is heated resulting in global shifts in G and the annealing can be carried out in an inert gaseous environment, a necessary criterion to demonstrate JJ anti-ageing. The variables explored in our RTA experiments are the junction geometry, capping oxidation, ambient gas conditions and annealing temperature (T_{RTA}) as shown in Fig. 6.12(a). We explore the parameter space with a heuristic approach, therefore combinations of experimental variables which likely do not lead to JJ anti-ageing based on the initial datasets are omitted. Additionally we also evaluate the effect of RTA on two temporally aged devices subjected to different storage periods.

The equipment used for RTA is a Solaris 100 Rapid Thermal Processor capable of processing Ø100 mm wafers at a temperature range from RT–1250 °C shown in Fig. 6.12(b) [310]. The heating uniformity of a wafer is controlled by an upper and lower array of 13 tungsten halogen lamps with customized three-zone temperature control for ensuring $\pm\,2\,^{\circ}\mathrm{C}$ deviation. The repeatability of T_{RTA} is enabled by use of state-of-the-art thermocouple signal conditioning using the SOLARIS software, which allows users to create calibration curves for different wafer types and backside emmissivity by adjusting the parameters of the proportional-integral-derivative (PID) controller. The recipes developed for our experiments are optimized by adjusting the Ramp Exit Modifier (REM) value during the Ramp step and Intensity

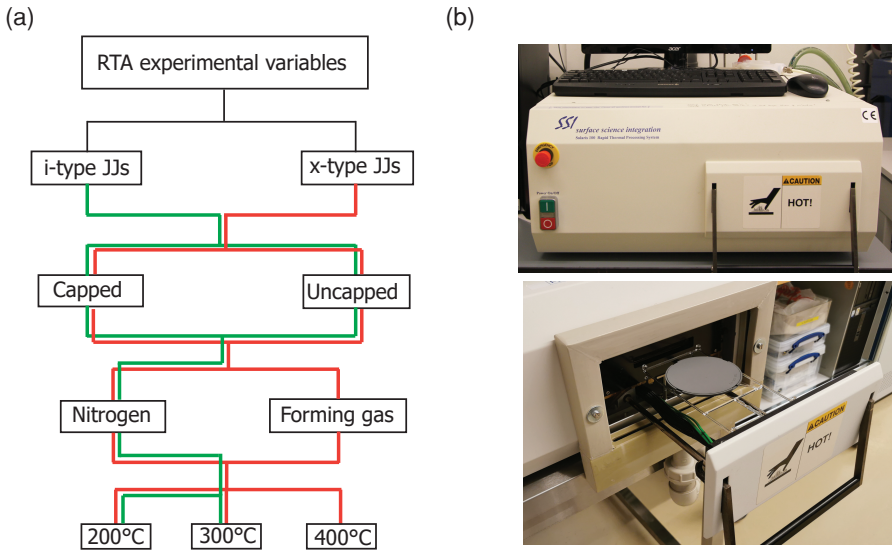


Figure 6.12: (a) Parameter space explored in the rapid thermal annealing experiments with JJs. The green (red) lines indicate process variables specific for i-type (x-type) junctions. (b) Images of the Solaris 100 RTP equipment used for this experiment.

during the steady-state temperature hold step in order to minimize instances of temperature overshooting or undershooting during each run. An example of the RTA annealing cycle showing the magnitude and duration of all the process parameters is shown in Fig. 6.20. All recipes are designed involving five steps namely an initial purge step for 5 min, ramp up at $100\ ^{\circ}\mathrm{C/s}$, hold and ramp down to RT. The annealing hold time and gas flow rate is maintained at 2 min and 8 sccm respectively for all temperatureand inlet gas variables. The temperature overshoot is observed to be limited to $\leq 20\ ^{\circ}\mathrm{C}$ for all the recipes.

We fabricate a wafer by depositing 160-nm thick TiN metallization layer using ALD ($R_s = 1.21\Omega/\square$) and pattern Surface-17 JJ island test structures with 8 dies containing i-type junction bays on the upper half of the wafer and 8 dies with x-type bays on the lower half, as described in Chapter 5.2. The dies are labelled 'e' or 'c' depending on its position with respect to the wafer centre and from 1–4 spanning from left to right of the wafer. After base layer patterning, the wafer is diced and further fabrication steps namely JJ deposition and RTA steps are carried out at die-level. The choice of switching away from NbTiN in this case is to avoid variations in the inter-die contact resistance between the JJ electrodes and the base layer, described previously in Subsection 5.7.4. The feedback cycle of the experiment is structured such that JJ deposition, acquisition of RT conductance using either the 2-point (manual probe station) or 4-point (APS-TASQ) method after JJ deposition, the

RTA process and the final RT measurement is completed within 48 hours for each device. We ensure that all the G measurements for each sample are acquired with the same probe station. We obtain statistics from over 14 successive deposition and annealing datasets, shown in Table 6.4. The storage time between the RT measurements are indicated to systematically track the directionality of JJ ageing with respect to the variable parameters. Some of the dies are recycled for multiple depositions by stripping the Al/AlO_x/Al JJs, performed by wet etching Al using a dilute solution of TMAH, namely MF™-321 developer. No significant deterioration of JJ reproducibility or yield is observed in the recycled dies. Firstly we compare the reproducibility of ΔG post deposition between the capped and uncapped datasets of i-type and x-type junctions. Then we compare ΔG post RTA between capped and uncapped samples from each variant at the nominal T_{RTA}. We note that most of our datasets are acquired at 200 and 300 °C. We then perform linear regression as well as Pearson correlation between A_{overlap} as the independent variable and ΔG as the dependent variable and extract the residual standard deviation (RSD) of ΔG. The slope of the linear regression is used as the criterion to compare the magnitude and direction of the relative change in G across the datasets.

ID	JJ type	Capping	Storage (days)	T_{RTA} (°C)	Gas	ΔG fit (μS/μm^2)	r	RSD (μS/μm^2)
[1] 1e	i-type	✓	3	200	N_2	-948.77	-0.85	7.93
[2] 2e	i-type	✓	<1	300	N_2	-947.50	-0.83	8.46
[3] 3e	i-type	✗	1	200	N_2	-379.49	-0.89	2.57
[4] 4e	i-type	✗	1	300	N_2	-907.18	-0.90	5.93
[5] 4e	x-type	✓	<1	200	N_2	-84.82	-0.14	7.96
[6] 3e	x-type	✓	<1	300	N_2	-914.64	-0.79	9.57
[7] 1e	x-type	✗	<2	200	N_2	153.26	0.43	4.22
[8] 2e	x-type	✗	<2	300	N_2	-1232.72	-0.92	6.97
[9] 4e	x-type	✓	<1	200	FG	0.02	0.307	5.17
[10] 3e*	x-type	✗	<2	200	FG	648.01	0.896	4.32
[11] 2e*	x-type	✗	1	200	FG	623.59	0.861	4.64
[12] 4c*	x-type	✗	1	300	FG	1032.3	0.974	3.14
[13] 3e*	x-type	✗	2	300	FG	-300.56	-0.424	8.74
[14] 4e*	x-type	✗	<1	400	FG	-1311.08	-0.893	8.55

Table 6.4: Summary of RTA experiments performed on devices fabricated from *Nighthawk-ALD 2* (NH-ALD 2) wafer coated with 160 nm ALD TiN. The device entries indicated with * are shown in Fig. 6.13. The column Storage indicates the lag time between RT G measurements acquired post deposition and RTA respectively, r is the Pearson's correlation coefficient and RSD is the residual standard deviation calculated between A_{overlap} and ΔG.

The most important result which we reproduce from prior literature is the temperature dependence of G, which decreases when subjected to annealing above $T_{\mathrm{RTA}} > 200$ °C for almost all devices. The second observation, which has not been demonstrated in prior literature to the best of our knowledge, is the significance of the capping layer in determining the directionality of ΔG. Among all experimental

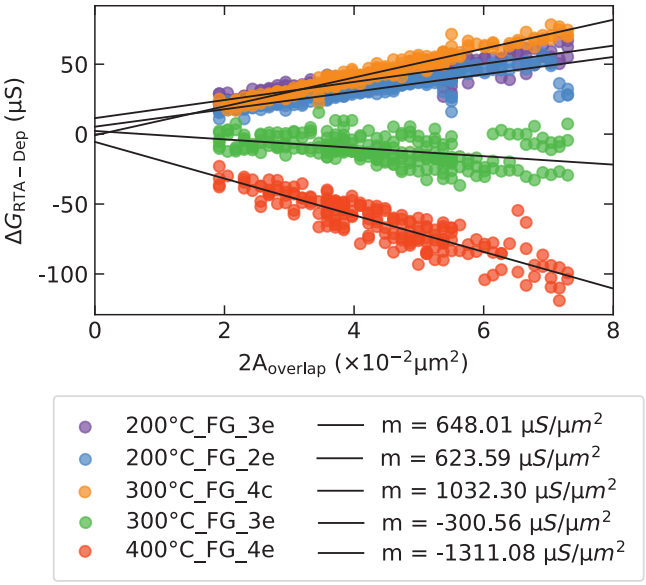


Figure 6.13: Plot of ΔG measured post RTA and post deposition vs. $A_{overlap}$ of uncapped x-type JJs in FG environment at different T_{RTA}. The coefficients of the linear fits shown by black lines indicate the magnitude and direction of annealing between the different experimental parameters.

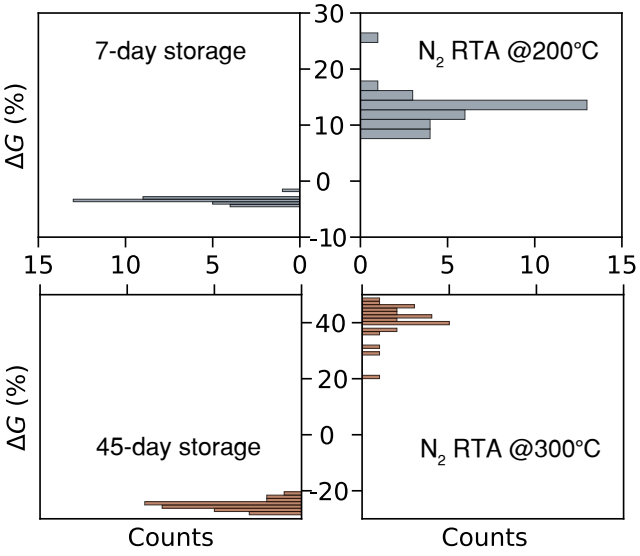


Figure 6.14: Histogram of relative change in ΔG of two x-type JJ devices stored in a N_2 desiccator for 7 and 45 days and subjected to RTA in N_2 gas after the storage period. In both devices, G decreases after storage and increases after RTA.

combinations, significant anti-ageing is consistently observed in uncapped x-type JJs subjected to RTA annealing in FG, indicated by the positive coefficients in Fig. 6.13. While both datasets of RTA at 200 °C show anti-ageing of similar magnitude, one instance of RTA at 300 °C shows the highest anti-ageing among all datasets at

$m = 1032\ \mu\mathrm{S}/\mu\mathrm{m}^2$.[8] Expanding on the results obtained from other datasets, entry [7] corresponding to a single dataset of uncapped x-type JJs annealed at $200\ ^\circ\mathrm{C}$ in N_2 gas also shows anti-ageing, albeit with a smaller slope compared to FG. The only outlier among capped datasets is entry [9], subjected to RTA in FG at $200\ ^\circ\mathrm{C}$, showing a nearly zero slope. All i-type junction datasets show a monotonic decrease in G across the parameter space, suggesting a strong dependence of the annealing behaviour on the JJ geometry.

We additionally perform experiments with two capped x-type devices to understand the effect of long-term storage on the tunnel barrier hygiene. The relative change in ΔG is calculated from the RT G values of 32 JJs with nominal $W_\mathrm{b} = 112$–$228\ \mathrm{nm}$ (JJ islands X1 and D6) measured immediately post deposition, after storage in a N_2 desiccator for a period of 7 and 45 days respectively and after RTA. The typical RH of the desiccator is about 30–40% at $20\ ^\circ\mathrm{C}$. The results from the relative change in temporal ageing study shown in Fig. 6.14 indicate that the capping oxidation layer is also sensitive to hydroxylation due to interaction with residual water vapour. The effect of EIA is observed to decrease G with increasing storage period, with $\mu_{G,\ \mathrm{stor-dep}} = -3.5\%$ and -25.2% for the 7 and 45-day stored devices respectively. The RTA treatment in N_2 gas at 200 (7-day device) and $300\ ^\circ\mathrm{C}$ (45-day device) not only reverses the effect of EIA with $\mu_{G,\ \mathrm{RTA-stor}} = 12.6\%$ and 41.5%, it also increases G above as-deposited values by $\mu_{G,\ \mathrm{RTA-dep}} = 8.8\%$ and 6.1% respectively.

6.6. Discussion

In this chapter, we compared the role of capping oxidation and environmental variables between i- and x-type JJs which lead to temporal variations in junction conductance. Ageing continues to remain an important problem that will require customized solutions, such as an ultra-high vacuum package allowing for vacuum loading [311]. The two different annealing approaches, namely LA and RTA are undertaken in order to discern environmentally-induced ageing (EIA) effects from fabrication-induced processes such as simulated annealed for resist reflow used in airbridge fabrication. A common feature for both annealing techniques is that the ageing behaviour is always relative to the temporal degradation or reinforcement of the tunnel barrier from its initial pristine state immediately post JJ deposition. Laser annealing performed at ambient environment induces ageing of junctions irrespective of the addition/omission of the capping layer. The susceptibility of junctions to LA shows a power-law dependence on the exposure time and intensity I of the laser beam. We observe that the sensitivity towards both ageing and on-demand annealing processes is dependent on the junction geometry and the area of AlO_x interface that is exposed to the environment. Both bridgeless JJ variants namely o-type and x-type are highly susceptible to ageing as well as annealing in comparison to i-type junctions. The anti-ageing observed at $200\ ^\circ\mathrm{C}$ with uncapped x-type JJs is likely to have similar origins for both simulated AB annealing as well as RTA at $200\ ^\circ\mathrm{C}$.

[8] We clarify that some discrepancies are observed in the RT conductance data post deposition for device entry [12], likely due to improper landing of the APS-TASQ probe needles on the test pads.

This maybe attributed to the high aspect-ratio of the electrodes in the bridgeless variants, however we did not investigate this in further detail. It would be interesting to investigate the ageing behaviour as a function of the area of the tunnel barrier exposed along the seams of the Al electrodes, visualized in Fig. 6.15. The tunnel barrier seams would be shielded to a greater extent if the narrower electrode (W_t in this case) is buried under broader taper as shown in Fig. 6.15(c). From these observations, we further categorize laser and rapid thermal annealing as an *oxygen-rich* and *oxygen-deficient* annealing process respectively. Junctions subjected to AB annealing are also observed to be resilient towards anti-ageing and require an effective on-demand annealing temperature higher than $200\ ^{\circ}\mathrm{C}$ to further trim JJ conductance.

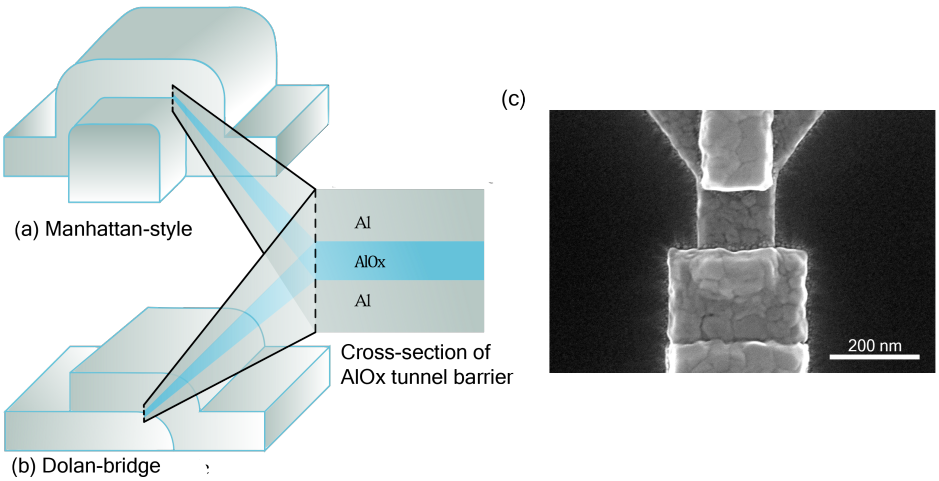


Figure 6.15: Schematic of cross-section of (a) Manhattan-style and (b) Dolan-bridge JJs showing the seams of the AlO_x tunnel barrier which are interacting with the immediate environment. Image courtesy: H. M. Veen (c) SEM micrograph of a Dolan-bridge JJ with the deposition azimuth angles swapped between the bottom and top electrode.

6.7. Post-fabrication frequency targeting: Supplementary Information

6.7.1. APS-TASQ user interface

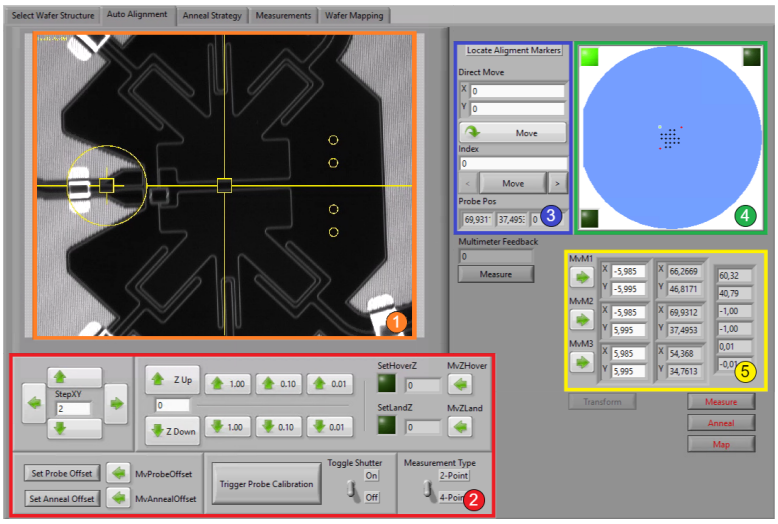


Figure 6.16: Screenshot of the APS-TASQ user interface panel developed using LabVIEW. **1** shows the camera feed used for device alignment. The XY- and Z-stage manual controls with user-defined step sizes are shown in **2**. Fast navigation to specific XY-stage coordinates is performed with **3**. Schematic of customizable device layout showing transmon or test JJ pad positions shown in **4**. Front-end option to specify device marker locations with respect to device coordinate space and corresponding transformation to the XY-stage coordinates shown in **5**. Reprinted from van der Meer (2021) [308].

For automated probing, sub-micron precision in alignment is essential for landing on the desired regions of the device and for positioning the laser spot exactly on the SQUID loop. The sample to be measured is essentially a 2D surface with each point represented by x and y vector. The device is aligned with respect to the XY stage via live video feed from the CCD camera by locating the 20 µm square markers at the periphery of the device and defining a transformation matrix from an input of at least three marker coordinates. Details on the protocol used to store and access device coordinates, positions of SQUID loops and capacitor pads between the LabVIEW GUI and Python back-end are described in further detail in [308]. The alignment settings are specified in this GUI panel, which gives a complete overview of all the measurement variables. Subpanel **1** of the panel screenshot shows the dark-field optical feedback of a Starmon qubit positioned below the objective. The grid overlay on the camera image indicates the centre of the screen, the four circles to the right shows the landing position of the probe needles and the circle with a

bull's eye indicates the position of the laser beam spot for LA. Prior to launching a measurement and annealing round on the APS-TASQ, the user performs XY and Z adjustments of all the above-mentioned positions on the device through sub-panel **2** of the panel. The Z-stage calibration involves recording the landing and hovering positions along with the overhead offset for neutralizing backlash of the probe needles mounted to the Z-stage. During laser annealing, the SQUID loop must be positioned away from the probe needles by a safe distance margin, this is adjusted using the probe and anneal offset buttons at the bottom left of the panel. For conveniently operating the GUI, the screen is made interactive through click-and-drag functionality with a mouse. For debugging purposes, this section also features a toggle for the beam-shutter and for switching between 2 and 4-point measurement. Subpanel **3** is used to directly position the XY stage under and away from the optics. Section **4** is is a schematic representation of the device layout, which can be either pre-loaded through the Python back-end for device protocols or created on the fly under the 'Select Wafer Structure' panel. A cartoon is then created of either a 4 inch wafer, a square die with the input device dimensions with black dots indicating the layout of the JJ test structures. After aligning each marker to the centre square of the grid overlay, confirmed by clicking on the green squares in subpanel **4**, the device-level coordinates are updated in subpanel **5** to recalculate the solution vector with respect to the XY stage coordinates. In case the placement of the sample is partially outside the reach of the probe handle, the omitted JJ test coordinates turn red on the device cartoon. After performing all the precursory alignments, the measurements or laser annealing protocols can be initialized under the 'Measurements' or 'Anneal Strategy' tabs respectively. The data is read and written using a custom class for serializing complex class objects using the `pickle` module through the Python back-end.

6.7.2. SUMMARY OF ZAPMON DEVICES

In Tables 6.6, 6.8 and 6.10 [C] and [L] refer to control and annealed qubits respectively. The values after $\pm$ are standard deviations. In Device B, Qubit 10 is recovered in CD-2 after removing a broken AB on its readout resonator.

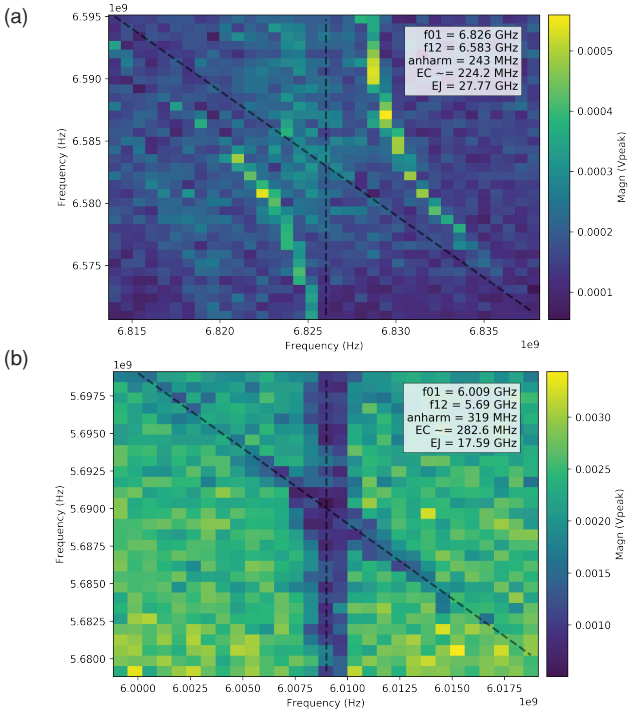


Figure 6.17: Comparison of two-tone spectroscopy of qubit 7 in Device C from (a) CD-1 and (b) CD-2. The tone intersecting the vertical dashed line corresponds to the f_{01} transition whereas the tone along the diagonal corresponds to the f_{02} transition, which is the sum of the 01 and 12 source frequencies. The difference between 12 and 01 tones yields the anharmonicity, which can be used to calculate E_c and E_J from Eq. 2.29. Reprinted from Janssen (2019) [312]

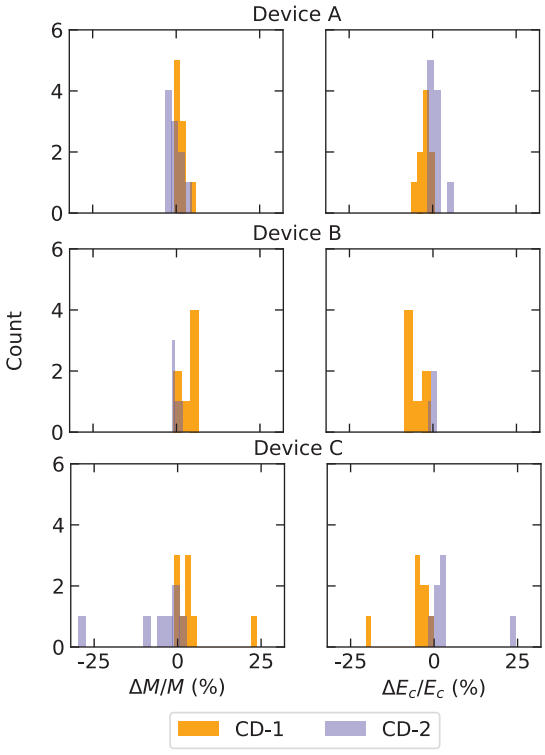


Figure 6.18: Comparison of fractional change in M and E_c between CD-1 and CD-2. The large deviations observed in Device C correspond to qubit 7 and 9.

Table 6.5: Device A cooldown-1

Qubit	$f_{r,meas}$ (GHz)	$f_{q,pred}$ (GHz)	$f_{q,meas}$ (GHz)	T_1 (μs)	T_2^* (μs)	T_2 (μs)	α (MHz)	E_c (MHz)	E_J (GHz)
1	7.116	5.955	5.963	90 ± 19	37 ± 6	136 ± 15	-325	287.0	17.1
2	7.219	6.026	5.983	72 ± 25	24 ± 5	154 ± 17	-315	279.4	17.6
3	7.320	5.993	5.970	85 ± 11	25 ± 5	140 ± 15	-321	284.0	17.3
4	7.423	6.171	6.14	71 ± 5	41 ± 3	90 ± 7	-308	274.8	18.8
5	7.530	6.304	6.278	78 ± 5	60 ± 10	80 ± 17	-314	280.2	19.3
6	7.636	6.311	6.322	70 ± 13	82 ± 10	120 ± 24	-316	282.0	19.4
7	7.739	6.483	6.466	77 ± 12	30 ± 5	98 ± 12	-306	274.8	20.8
8	7.836	6.513	6.460	71 ± 18	57 ± 10	75 ± 10	-314	281.2	20.3
9	7.937	6.839	6.822	44 ± 10	76 ± 10	60 ± 10	294	266.6	23.6
10	8.033	6.680	6.658	70 ± 10	100 ± 10	120 ± 10	-312	280.5	21.5

Table 6.6: Device A cooldown-2

Qubit	$f_{r,meas}$ (GHz)	$f_{q,pred}$ (GHz)	$f_{q,meas}$ (GHz)	T_1 (μs)	T_2^* (μs)	T_2 (μs)	α (MHz)	E_c (MHz)	E_J (GHz)
1[L]	7.116	5.963	5.913	57 ± 4	37 ± 6	106 ± 10	-328	289.0	16.7
2[L]	7.219	5.861	5.900	24 ± 2	14 ± 0.7	43 ± 5	-316	279.7	17.2
3[L]	7.320	5.811	5.842	10 ± 2	14 ± 1	21 ± 2	-316	279.4	16.8
4[C]	7.425	6.140	6.129	71 ± 5	41 ± 3	90 ± 7	-316	281.0	18.4
5[C]	7.530	6.278	6.261	23 ± 5	35 ± 6	45 ± 7	-310	277.0	19.4
6[C]	7.636	6.322	6.276	2.4 ± 0.3	3.4 ± 0.8	5.0 ± 0.6	-316	281.8	19.2
7[L]	7.739	6.275	6.404	61 ± 5	30 ± 5	95 ± 13	-308	276.1	20.3
8[L]	7.836	6.359	6.377	69 ± 15	36 ± 6	95 ± 18	-316	282.3	19.7
9[L]	7.936	6.528	6.601	79 ± 8	120 ± 8	111 ± 21	-316	283.4	21.0
10[L]	8.034	6.473	6.391	9.8 ± 1	13.7 ± 0.7	21 ± 1	-308	276.0	20.2

Table 6.7: Device B cooldown-1

Qubit	$f_{r,meas}$ (GHz)	$f_{q,pred}$ (GHz)	$f_{q,meas}$ (GHz)	T_1 (μs)	T_2^* (μs)	T_2 (μs)	α (MHz)	E_c (MHz)	E_J (GHz)
1	7.112	6.104	6.031	45 ± 8	35 ± 12	86 ± 24	-317	281.2	17.8
2	7.210	5.948	5.907	59 ± 7	44 ± 18	94 ± 14	-321	283.6	17.0
3	7.305	6.161	6.145	5.5 ± 0.7	3.2 ± 0.2	10 ± 1	-311	277.2	18.7
4	7.406	6.174	6.124	3.7 ± 0.2	1.24 ± 0.04	3.6 ± 0.4	-295	264.4	19.4
5	7.530	6.304	6.272	13 ± 1	22 ± 3	25 ± 5	-304	272.3	19.7
6	6.447	–	–	–	–	–	–	–	–
7	7.715	6.588	6.531	6.1 ± 0.4	11.8 ± 0.7	15 ± 2	-288	260.6	22.2
8	7.815	6.23	6.195	6.4 ± 0.4	8.7 ± 0.3	12 ± 1	-298	266.8	19.2
9	7.920	6.825	6.825	3.6 ± 8	49 ± 12	89 ± 12	-295	267.4	23.6
10	–	6.620	–	–	–	–	–	–	–

Table 6.8: Device B cooldown-2

Qubit	$f_{r,meas}$ (GHz)	$f_{q,pred}$ (GHz)	$f_{q,meas}$ (GHz)	T_1 (μs)	T_2^* (μs)	T_2 (μs)	α (MHz)	E_c (MHz)	E_J (GHz)
1	7.112	–	–	–	–	–	–	–	–
2[C]	7.210	5.914	5.900	41 ± 6	29 ± 12	79 ± 9	-320	282.7	17.0
3[L]	7.305	5.880	5.872	8.1 ± 0.4	13.4 ± 0.9	15 ± 1	-317	280.3	17.0
4[L]	7.406	5.849	5.843	1.9 ± 0.1	0.9 ± 0.1	1.6 ± 0.1	-301	-267.7	17.5
5	7.513	–	–	–	–	–	–	–	–
6[L]	7.614	6.218	6.171	10.7 ± 0.6	13 ± 2	21 ± 1	-311	277.3	18.8
7[L]	7.715	6.254	6.286	6.5 ± 0.8	11 ± 1	14 ± 1	-292	262.3	20.5
8[C]	7.815	6.216	6.183	2.3 ± 0.2	4.1 ± 0.2	4.7 ± 0.4	-298	266.7	19.6
9[L]	7.920	6.541	6.537	6.8 ± 0.3	6.7 ± 0.8	13 ± 1	-292	263.7	22.0
10[L]	8.028	6.304	6.297	45 ± 10	40 ± 13	80 ± 20	-309	276.7	19.6

Table 6.9: Device C cooldown-1

Qubit	$f_{r,meas}$ (GHz)	$f_{q,pred}$ (GHz)	$f_{q,meas}$ (GHz)	T_1 (μs)	T_2^* (μs)	T_2 (μs)	α (MHz)	E_c (MHz)	E_J (GHz)
1	7.123	6.287	6.223	68 ± 15	27 ± 4	90 ± 20	-317	281.8	18.9
2	7.226	6.327	6.301	74 ± 12	39 ± 5	97 ± 17	-314	280.3	19.4
3	7.326	6.262	6.236	49 ± 8	50 ± 10	74 ± 13	-320	284.7	18.7
4	7.431	6.495	6.438	48 ± 12	55 ± 15	71 ± 22	-306	274.3	20.6
5	7.538	6.680	6.684	5.0 ± 0.5	9.9 ± 0.9	10.7 ± 0.7	-306	275.8	22.0
6	7.643	6.883	6.833	41 ± 8	35 ± 10	60 ± 9	-298	269.9	23.4
7	7.747	6.823	6.826	11 ± 3	5 ± 1	20 ± 6	-246	226.8	27.5
8	7.842	6.856	6.804	52 ± 6	61 ± 10	80 ± 15	-307	277.1	22.7
9	7.943	7.109	7.080	47 ± 8	32 ± 3	21 ± 4	-299	271.8	24.9
10	8.041	7.125	7.088	22 ± 4	22 ± 7	36 ± 10	-297	270.1	25.1

Table 6.10: Device C cooldown-2

Qubit	$f_{r,meas}$ (GHz)	$f_{q,pred}$ (GHz)	$f_{q,meas}$ (GHz)	T_1 (μs)	T_2^* (μs)	T_2 (μs)	α (MHz)	E_c (MHz)	E_J (GHz)
1[C]	7.123	6.223	6.214	50 ± 11	25 ± 5	89 ± 9	-317	282.2	18.8
2	7.226	–	–	–	–	–	–	–	–
3[L]	7.326	5.968	6.007	17 ± 1.1	7.1 ± 0.6	10.3 ± 0.5	-315	279.5	17.7
4[L]	7.431	5.703	5.680	62 ± 6	22 ± 5	102 ± 8	-321	282.1	15.8
5[L]	7.538	5.995	5.789	66 ± 8	23 ± 3	114 ± 12	-321	282.8	16.4
6	7.643	–	–	–	–	–	–	–	–
7[L]	7.747	6.499	6.010	49 ± 6	24 ± 2	64 ± 8	-319	282.7	17.6
8	7.842	–	–	–	–	–	–	–	–
9[L]	7.943	6.041	5.948	46 ± 9	–	–	-316	280.0	17.4
10[C]	8.041	7.088	7.082	26 ± 8	34 ± 10	45 ± 10	-297	270.0	25.1

6.7.3. ADDITIONAL DATA RTA EXPERIMENTS

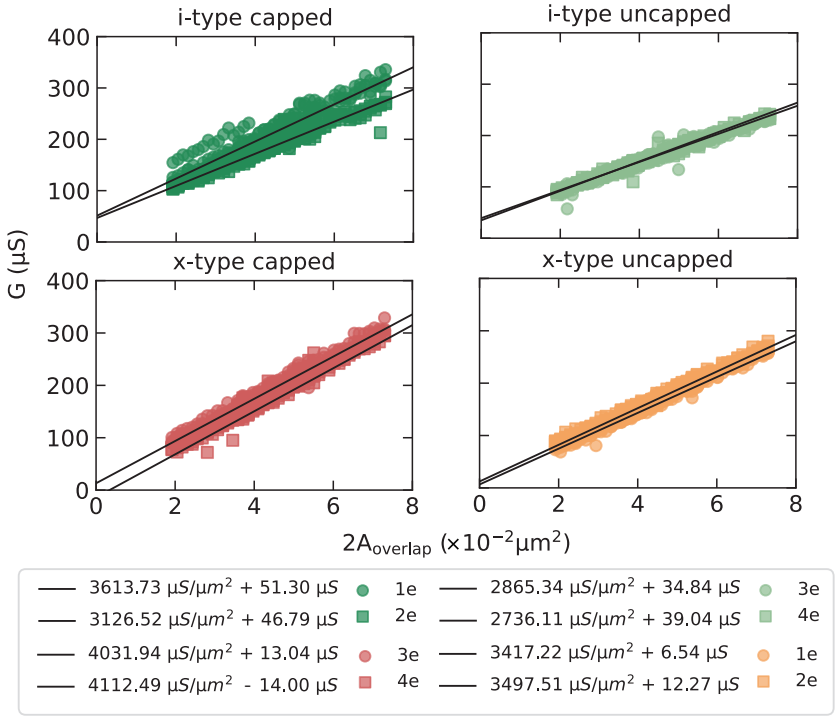


Figure 6.19: Comparison of G between capped and uncapped i-type and x-type JJs immediately post deposition. The black lines are regression fits, outliers such as half-open junctions are filtered as per the procedure discussed in Chapter 5. The conductance of uncapped variants is systematically lower as inferred from the slope of the fits.

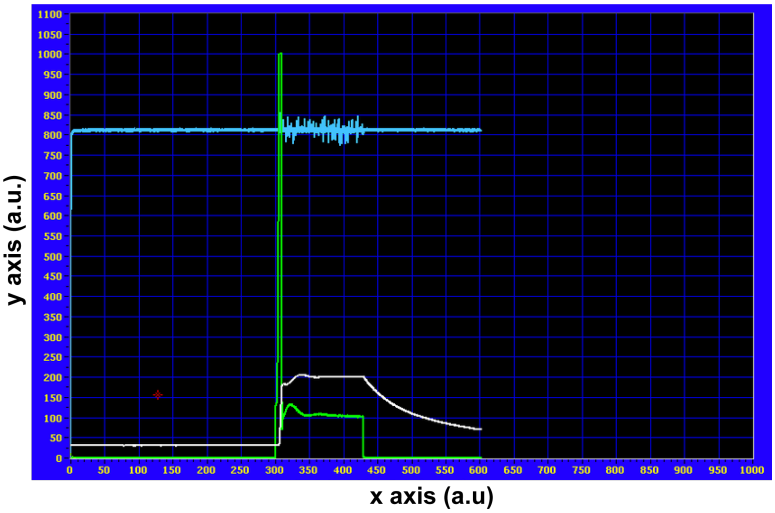


Figure 6.20: Snapshot of the RTA annealing recipe at $200^{\circ}C$ using FG. The white line corresponds to the temperature of the process, the green line corresponds to the PID power and the light blue line indicates the gas flow rate.

7

CONCLUSIONS AND OUTLOOK

Qubit frequency targeting, situated as a subset of challenges within the broader context of scalable SQPs, has been the focal point of investigation in this research. Throughout our study, we have explored scientific and engineering approaches aimed at understanding the fundamental factors influencing the reproducibility of fabrication processes and predictability of transmon frequency from RT measurements, specifically focusing on JJs based on shadow-evaporation. Our initial efforts were directed towards systematically increasing the qubit count from two-qubit devices upto 17-qubit devices either employing lateral wirebonding (planar approach) or through-silicon via (TSV)-based signal delivery (VIO approach) using the fabrication processes detailed in Chapter 3. The overall fabrication yield, described by physical yield, qubit frequency targeting and qubit coherence of Surface-7/17 planar and VIO devices were verified by RT and cryogenic characterization, described in Chapter 4.

The success of this work is attributed to the ability to investigate the cause and effect of failure modes in JJs through RT conductance measurements, SEM images as well as predicting the qubit frequency ($f_{\mathrm{q,pred}}$) with reasonable accuracy using the Ambegaokar-Baratoff relation. Qubit coherence, on the other hand is a far more complex and multi-pronged challenge to tackle that requires a complete overhaul with regard to the choice of materials in our fabrication processes. Furthermore, we observe a pronounced effect on frequency targeting when scaling from die-level to wafer-scale fabrication, evident from a centre-to-edge variation in the measured overlap area (A'_{overlap}) of x-type (Manhattan-style) JJs. This motivated a multi-wafer study, described in Chapter 5 to systematically quantify wafer-scale and die-level variations of Dolan-bridge and Manhattan-style junctions in both planar and TSV-integrated wafers, employing metrics such as the coefficient of variation (CV) of conductance (σ_G/μ_G) and the relative standard deviation (RSD) of $f_{\mathrm{q,pred}}$ which are inversely proportional to the targeting precision. The die- and wafer-scale CV of Dolan-bridge JJs from our work are on par with state-of-the-art values reported in prior literature, summarized in Table 7.1. Our suboptimal results for Manhattan JJs are likely due to a stronger resist-shadowing effect owing to the top-heavy resist stack ($H_{\mathrm{t}} = 600$ nm) and contributions from contact resistance on metallized sub-

strates.

We independently reported the first observation of a centre-to-edge distribution in the overlap area of Manhattan-style JJs owing to the shadowing effect of the resist walls during multi-angled deposition of the electrodes. Experiments with Manhattan-style (x-type) JJs renew our understanding of the interplay between the shadowing geometry and the spatial variation of the evaporated metal flux deposited from a point source. The magnitude of the resist-shadowing effect on the JJ overlap area is captured by SEM characterization of over 100 junctions (See Fig. 5.12), showing a $\sim 35\%$ decrease in A'_{overlap} from centre to edge of the wafer.

To the best of our knowledge, we present the largest statistical data to date quantifying the spread in JJ conductance and qubit frequency targeting precision in the presence of TSVs. The results from Fig. 5.10 unveiled a nuanced picture regarding the suitability of resist-bridge vs. bridgeless JJ variants for scalable SQPs described in further detail in Section 5.6.

We obtain a minimum die-level frequency RSD of $80\ \mathrm{MHz}$ from planar NbTiN-metallized 35×35 layout Dolan-bridge junctions (See Table 5.1). This is higher imprecision than the desired margin of $\sigma_f = 50\ \mathrm{MHz}$, which is slightly relaxed for flux-tunable qubits in comparison to a fixed-frequency qubit architecture which requires $16\ \mathrm{MHz}$ [133]. We seek recourse in post-fabrication tuning of qubit frequency using localized laser annealing, described in Chapter 6. Although demonstrating the proof-of-concept of a consistent decrease in f_{q} with increasing laser power P_{L} was straightforward, the difficulty lay in creating a closed-loop feedback system linking laser annealing parameters with the desired junction conductance, aiming to minimize the disparity between target ($f_{\mathrm{q,des}}$) and measured ($f_{\mathrm{q,meas}}$) values post-laser annealing compared to the initial as-fabricated values. With incremental improvements in the design and functionality of the APS-TASQ setup, LA has become a routine procedure for trimming f_{q} in the range 30–$300\ \mathrm{MHz}$.

7

7.0.1. Mapping sources of variation to qubit frequency

From various experiments described in this thesis, I categorize the factors which can impact JJ fabrication and thereby qubit frequency targeting, described succinctly in Fig. 7.1. On modifying certain 'Controlled input factors' such as the die size and base patterning processes described in Chapter 5, we observed sources of variations to the A'_{overlap} of both Dolan-bridge and Manhattan JJs. The geometric resist-shadowing effect is a unique feature observed only in bridgeless Manhattan JJs which results in variation of both transverse and sidewall overlap areas. Junction ageing, on the other hand is a property of the AlO_x tunnel barrier which is influenced by the addition of a final capping/passivation layer determined by the input factor 'JJ deposition and oxidation parameters'. From Chapter 6, we observe that Manhattan JJs are more susceptible to both ageing and anti-ageing behaviour, whereas Dolan-bridge junctions are predisposed towards ageing.

The 'Unaccounted sources of variations' are factors which are identified in this work which are not quantified directly. In Subsection 4.2.4, I speculate the role of surface roughness of the Si substrate on calculating $f_{\mathrm{q,pred}}$. This is because of the discrepancy in the extracted M from $f_{\mathrm{q,meas}}$ and G shown in Fig. 4.8 in spite of

the fabrication processes of all planar Surface-7 devices being nominally identical, with a deliberate exception of the base layer etching step. The junction harmonics model [254] predicts a lower effective E_J due to the existence of high-transmission channels within the Al/AlO_x/Al tunnel barrier caused by the presence of contaminants, defects or random crystallographic orientations of the bottom Al electrode [279]. Although it is known from prior literature that the AlO_x tunnel barrier grown by room-temperature thermal oxidation is inherently inhomogeneous, it remains to be investigated whether increasing surface roughness of the substrate influences the microscopic structure of the tunnel barrier.

The formation of a sizeable contact resistance at the interface of the junction electrodes and NbTiN base layer is a crucial finding of this work, which is quantified indirectly by computing the JJ conductivity from the effective overlap area A'_{overlap} of Manhattan JJs. This contributes to a parallel centre-to-edge decrease in the effective RT G values, particularly evident in Manhattan JJs due to the small JJ contact pads and possibly due to the formation of physical breaks on the top electrode due to the higher deposition tilt angle (See Fig. 4.12(b)). However, the impact of contact resistance on qubit frequency targeting has not been quantified in this work. Lastly, we have sporadically observed drifts in fabrication processes due to fluctuations in cleanroom temperature and humidity conditions normally maintained at 20 °C and 50% relative humidity (RH) respectively, which affect batch to batch reproducibility of G as a function of A_{overlap}. This has been a recurring issue due to heatwaves in the summer months, increasing RH levels above 70%.

As shown earlier in Subsection 4.2.3, the factors categorized as 'Noise sources' affect the acquisition of RT G measurements using our home-built transimpedance amplifier. In the 2-wire configuration, external cabling resistance R_{c} introduces a small but finite inaccuracy to G. The series resistance of probing pads R_{pad} cannot be isolated from the effective resistance of the JJs, which too is a relatively negligible value compared to the measurement range between 4–14 $\mathrm{k\Omega}$. In order to minimize parasitic conductance contributions due to the illumination source, we limit the light intensity to 500 lx such that the substrate conductance is $\sim 1\ \mu\mathrm{S}$. Inconsistencies in the input values of E_{c} and $\Delta(0)$ affect the calculation of $f_{\mathrm{q,pred}}$ using the Ambegaokar-Baratoff relation. These values are monitored from measurements of f_{01} and anharmonicity at their flux sweetspot.

Prior works	Material	JJ type	JJ area (μm^2)	Wafer-scale CV%	Die-level CV%
Lotkhov et al. 2006 [313]	Al/AlO_x/Al	Dolan-bridge	0.125 – 0.25	10 – 20	···
Bumble et al. 2009 [314]	Nb/Al-AlO_x/Nb	Trilayer	0.33	···	2 – 4
Pop et al. 2012 [286]	Al	Dolan-bridge	0.02 – 0.2	···	3.5
Tolpygo et al. 2014 [315]	Nb/Al-AlO_x-Al/Nb	Planarized	0.03 – 1.8	0.8 – 8	···
Kreikebaum et al. 2020 [221]	Al/AlO_x/Al	Manhattan	0.042	3.5	1.8
Osman et al. 2021 [224]	Al/AlO_x/Al	Manhattan	0.01 – 0.16	2.5 – 6.3	1.2 – 2.9
Hertzberg et al. 2021 [133]	Al/AlO_x/Al	Dolan-bridge	0.01	···	4.6
Verjauw et al. 2022 [106]	Al/AlO_x/Al	Overlap	0.03 – 0.07	···	2 – 5.5
Takahashi et al. 2022 [225]	Al/AlO_x/Al	Manhattan	0.05	3.4	1.9
Muthusubramanian et al. 2024[227]	Al/AlO_x/Al	Dolan-bridge	0.02 – 0.07	1 – 4	0.5 – 4
Muthusubramanian et al. 2024 [227]	Al/AlO_x/Al	Manhattan	0.02 – 0.07	2 – 8	1.4 – 6

Table 7.1: Comparison of wafer-scale and die-level JJ variation statistics between prior literature and the results described in this thesis, indicated by the bold text.

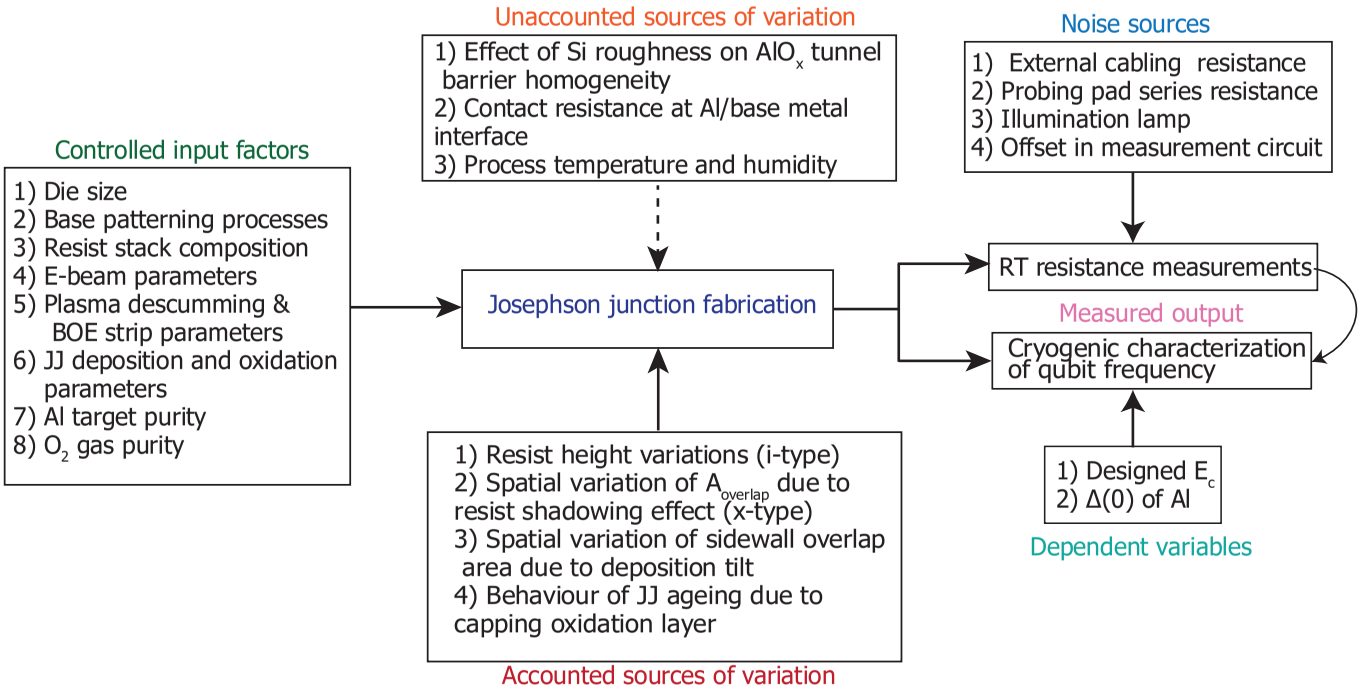


Figure 7.1: Flow chart of the different factors categorized as controlled inputs, identified causes, potentially unknown sources and measurement-induced errors which impact the fabrication and characterization of Josephson junctions.

7.0.2. Limitations of this work

In this section, I address the shortfalls of this work, organized according to the order of the chapters. In Chapter 3, we characterized the centre-to-edge variation in thickness profile of a 200 nm-thick NbTiN film deposited via DC magnetron sputtering. This irregularity influences various facets of fabrication and chip design, including unevenness in etching the substrate layer, fluctuations in kinetic inductance and subsequent phase velocity across the wafer, resulting in discrepancies in resonance frequencies between readout and Purcell filter resonators [252], and fluctuations in contact resistance between the Al/NbTiN interface of JJs.

Based on the results from wafer-scale fabrication of junctions on TSV-integrated substrates detailed in Chapter 5, we identify several paths for improvement for future efforts on VIO fabrication. The current aspect ratio of the TSVs is relatively large at approximately 3:1, other works employing ALD TiN as the TSV metallization layer have shown significantly smaller aspect ratios of 8:1 [39]. Reducing the TSV footprint is necessary to minimize the impact of resist height variations when patterning the base layer and crucially Josephson junctions. However, the footprint of our VIO is in fact limited by the pitch of the SMA connectors and not necessarily by any fabrication limitations. Optimizing this bottleneck requires the development of custom scalable SQP-specific solutions for microwave connectors, or rather using TSV-integrated devices as interposers for allowing stackable three-dimensional scaling [194].

In hindsight, it would have been very useful to perform additional test experiments to probe the spatial dependence of the metal/JJ interface resistance R (R') corresponding to the bottom (top) electrode, described in Chapter 5. This could be done with two sets of test structures. In one set, the oxidation step would be eliminated in the fabrication of the Manhattan JJs, effectively making shorted junctions and making joints of type R . In the other set, the oxidation step would be performed before the evaporation of both electrodes instead, again making shorted JJs but now making joints of type R' . A detailed study of the Al/NbTiN and/or Al/TiN joint resistance and its spatial dependence (with and without bandaging) remains very interesting for future research.

In the short term, this contact resistance can be addressed by either increasing the contact area of the JJ electrodes or by incorporating a bandaging layer which establishes galvanic contact between the JJ electrodes and the base layer [224] or as an additional overlay metal layer larger than the JJ contact pad [273, 276]. To test this idea, our team fabricated Surface-17 devices (*Hyperion v4, Phoebe v4*) with JJs carrying the large contact pads, with the former showing the lowest spread in qubit-qubit detuning calculated from $f_{\mathrm{q,pred}}$ values (Fig. 4.10). However, sufficient time-domain characterization is not performed on this device, therefore this question remains to be investigated further.

In Chapter 6, we did not perform time- and frequency-domain characterization of an SQP subjected to the effect of junction anti-ageing using forming gas at $200\,^{\circ}\mathrm{C}$. It is known that exposure of superconductors to hydrogen results in *hydrogen poisoning*, which can introduce impurities and defects in the crystal lattice of superconductors resulting in variability in junction I_c [316]. All our laser annealing experiments

were performed under atmospheric conditions, it would be interesting to perform localized annealing of JJs in an inert gaseous atmosphere such as argon or nitrogen to test if it would result in ageing or anti-ageing.

7.1. OUTLOOK FOR FUTURE SQPS

It is a truly exciting time to be involved in R&D efforts in superconducting qubits at this juncture, with innovation being driven by both large and small-scale commercialization ventures and academia alike. Current SQPs operate as standalone hardware where all quantum operations are performed on-chip in a single dilution refrigerator. A noteworthy experiment to link two dilution fridges by a 4.9 m-long WR-90 Al rectangular waveguide and generate entanglement on two spatially-separated qubits is described in [317]. Further scope for improving near-term monolithic SQPs would require addressing limitations imposed by fixed qubit-qubit couplings, interconnect crowding caused by lateral wirebonding and increasing baseline qubit coherence above $50\ \mu$s, discussed in further detail below.

MITIGATING ZZ-CROSSTALK

One of the shortfalls of a fixed bus architecture for qubit-qubit coupling is the always-on ZZ coupling between nearest neighbour qubits, which introduces errors in two-qubit gate fidelity and exacerbates dephasing of the target qubits [35]. Our current protocol for net-zero (NZ) or sudden net-zero (SNZ) CZ gates involves flux-pulsing one of the participant qubits by atleast 500 MHz below its flux-insensitive point, which causes dephasing due to flux noise [123, 127]. Although this can be countered by carefully applying echo sequences to reverse the accumulated phase errors, it contributes to significant measurement overhead when scaling to multiple qubit pairs. Tunable coupling allows for a large on/off ratio between two-qubit interactions (J_1), thereby altogether eliminating static ZZ crosstalk [318] and further relaxing the margins for qubit frequency targeting. Hardware-based approaches include flux-tunable couplers [12, 175, 319], multipath couplers [320, 321] and hybrid superconducting qubits [322, 323]. Hardware-efficient approaches without requiring additional circuit complexity include off-resonant driving of qubits [324, 325] and dynamical decoupling [250, 326]. It must be kept in mind that the tuning range and precision can also be limited by the hardware and control choices, therefore the need for reproducible qubit frequency grouping within the chip will still remain relevant.

FLIP-CHIP APPROACH FOR SCALABILITY

One of the objectives of this work was to determine the viability of vertical I/O architecture to scale over 50 physical qubits in terms of overcoming fabrication complexities to meet baseline requirements for qubit frequency targeting precision and quality. As stated previously, there is certainly room for optimization to decrease the footprint of TSVs which may flatten out resist height variations to some extent. However, in the light of rapid strides made by IBM by switching to multi-level wiring

architecture using flip-chip approach [1], it is worth considering the merits of a modular SQP from the purview of fabrication overhead. Separating the resonator and qubit planes would increase the fabrication throughput and minimize downtime. A separate interposer device, comprising only TSVs can enable signal fan-out from the resonator/control plane, as demonstrated in [37, 176]. However, the addition of multiple layers galvanically connected only by small indium bump bonds in the flip-chip approach would delay the rate of quasiparticle recombination, as reported from a study on correlated errors in Google Sycamore processor due to high-energy cosmic radiation [111]. Future efforts would need to optimize thermalization of the flip-chip package and add islands of phonon absorbers made of either a low T_c superconductor or normal metal such as copper on the backside of the resonator and qubit layers to assist the down-conversion of cosmic rays [328–330]. It would also benefit continuing to use NbTiN as the superconducting base layer for flip-chip as the recombination time is significantly faster in a high T_c superconductor.

Cracking the coherence problem

Inherently superconducting qubits are imperfect artificial atoms; the limitation of this platform lies in the shorter decoherence times compared to other physical QC modalities such as trapped ions or NV centres. Research is still ongoing to better understand materials and tailor conventional lithographic processes towards realizing pristine interfaces, high Q_i eventually translating to improvement in qubit T_1 and T_2. Several improvements in the fabrication processes, choice of superconducting films with exotic metal oxide properties such as niobium (Nb), tantalum (Ta) and dielectric materials with high quality factor such as sapphire and intrinsic silicon have dramatically increased T_1 in planar transmon-based circuits upto $500\ \mu s$ [265, 266, 331].

There are multiple ideas to test regarding our current limitations in achieving higher qubit T_1 and T_2. To better understand the limitations of our NbTiN films in terms of Q_i, we can optimize our sputtering recipes to favour epitaxial film growth, yielding low-resistivity films [332] and by systematically investigating the relationship between resonator Q_i and material properties such as film microstructure (using suitable crystal structure visualization techniques such as Annular Dark-Field (ADF) imaging or electron backscatter diffraction (EBSD)), film stress and stoichiometry. From a nanofabrication standpoint, finding the right knobs for optimizing sputtering recipes for alloys (Nb:Ti in this case) is a challenge in itself due to the need to monitor long-term control of the film composition deposited on the substrate and understanding the impact of the parameters and geometry of the deposition system on the film quality [332, 333].

There is certainly scope for further improvement in our film deposition parameters in order to demonstrate better and reproducible qubit coherences, however elemental superconductors such as Nb or Ta have gained more traction recently due to the results from [265, 266, 334]. Ideally switching to an elemental superconductor for future iterations of SQPs should also be accompanied by improving the

[1] Debuted in the 127-qubit Eagle processor [327]

wafer-scale uniformity of the film thickness and reproducibility of the material's sheet resistance.

Subtractive patterning of the base layer tends to increase the roughness of the surface, as described in Chapter 4. This is a known factor which is expected to contribute to a larger spread in wafer-scale conductance of metallized substrates. This may also have a profound implication on qubit coherence. It would be interesting for future research to study the effect of Si substrate roughness on the formation of defects or high-transmission channels in the AlO_x tunnel barrier supported by two-tone spectroscopy measurements of the transition frequencies f_{0j} of the transmon upto $j = 6$ [254]

The transition from i-type JJs in Surface-7 to x-type JJs in Surface-17 was not sufficiently backed by experimental data regarding the reproducibility of qubit relaxation times. From multiple iterations of Surface-17 devices, which have only been fabricated with x-type junctions, none has demonstrated an average $T_1 \geq 30\ \mu s$ (Data not shown in this work). An ideal experiment to determine the impact of JJ geometry on dielectric losses is to fabricate both types of junctions on two identically processed devices, where one device is deposited with i-type JJs first followed by x-type and the other device with the JJ steps done vice versa.

TRANSITIONING OUT OF ACADEMIC CLEANROOM

The present obstacles facing the production of quantum computing hardware involve shifting from a limited, primarily academic approach to one that is commercially viable and the lack of a scalability model that in some way, can mirror the progression of semiconductor integrated circuits. For example, the non-availability of sputter deposition tools which can ensure uniformity of superconducting films deposited on 100-mm wafers in Kavli Nanolab, Delft is currently a major bottleneck towards reliable wafer-scale fabrication. Shared usage of equipment for dry etching and other sensitive processes can contaminate SQPs due to redeposition of non-volatile metal fluorides. Investing in a dedicated cleanroom facility for processing elemental superconductors within the private sector could go a long way towards structuring incremental R&D in this field. The fabrication of JJs by multi-angle evaporation employing in-situ oxidation is challenging to scale up, as demonstrated by the multi-wafer analysis of junction uniformity in this work. In order to transition to a production facility, the superconducting qubit community would eventually need to wean away from shadow evaporation and instead focus on optimizing trilayer [315] or overlap junctions [106, 335] for increased qubit coherence. Cryogenic characterization of JJs would become feasible on reverting to Nb/Al-AlO_x/Nb junctions, which could significantly decreases errors in estimating qubit frequencies [336]. The development of nascent customized AOI solutions such as our home-built `pyclq` software and the APS-TASQ setup are local innovations based on ideas borrowed from the semiconductor industry.

A

APPENDIX

A.1. NBTIN FILM MONITORING

The wafers used in this study (WS3, WS4, WS5, WS6, *Blackbird 4x (planar* 35×35 *layout)*, *Valkyrie 2x* (TSV 17Q layout)) are plotted alongside the data from the monitoring log. The calculated resistivity values of wafers WS5, WS6 and the Blackbird and Valkyrie wafers are identical.

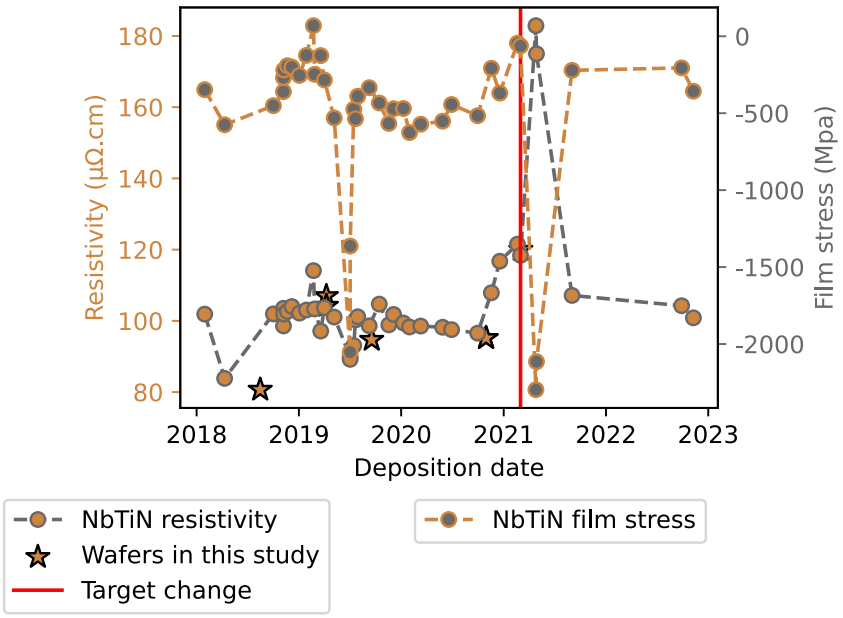


Figure A.1: NbTiN deposition log using the SuperAJA system. Each wafer is deposited with 100 nm of NbTiN for acquiring 4-wire resistance and compressive stress measurements. The red line indicates the date of change of NbTi target. Data courtesy: Ivan Kulesh and Dr. Marta Pita-Vidal, Kouwenhoven lab, QuTech

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A.2. PYQIP FOR CHIP DESIGN

PyQIP is our home-built Python-based scripts for CAD design using the package **gdspy** customized for our SQPs [147]. It also enables export of the generated CAD layout to CST Studio Suite[1], our preferred choice for 3D EM simulation and analysis. It is modular by design which allows for design and development of SQPs either with hanger RR or with RR-PF pairs, with or without VIOs and with different transmon designs such as Starmon or the Yalemon. The Chip class is the heart of all modules in PyQIP as every structure added to the layout goes through this class. The different layers which needs to be added to a SQP is defined as a dictionary `layerdict` in the class Chip Element. CPW parameters are either hard-coded, simulated using EM software or analytically calculated from formulae described in Section 3.1.1. While every element can be placed in the layout by means of a location expressed in Cartesian coordinates, the routing of CPW requires additional input in the form of an array of points and angles to route the CPW. Depending the chosen PCB layout, for example octobox, Surface 7 or Surface 17, the anchor points for CPW routing is between a qubit and a launcher at the outer perimeter of the layout. The launcher class is imported from `pyqip.Core.TSIO` and is predefined as a dictionary with the corresponding coordinates and orientation in the PCB module, imported as `pyqip.PCBs.PCB`. The airbridge module is called through the Chip module as `chip.set_airbridge_module`, allowing the user to customize airbridge placement for every CPW in a layout. There are four defined modules namely 'Length', 'Recommended', 'Traditional' and 'Intersection'. The 'Length' module is most flexible, allowing for placement of airbridges at any location on a specified CPW using the dictionary `lengths`. The transmon qubit designs *Starmon* and *Yalemon* are defined in in the Qubits module `pyqip.Qubits.Qubit` and are drawn by specifying several parameters common to each individual qubit type, defining a cell and adding elementary shapes to it such as `gdspy.Rectangle()` and `gdspy.Round()` and conjoining the polygon shapes together using Boolean operations defined as `gdspy.boolean(operand1, operand2,operation, precision=0.01, max_points=200, layer=0, datatype=0)`. The predefined Boolean operations available in gdspy library are `('or','and', 'xor','not')`. The SQUID loop requires additional parameters such as the JJ type (o, i and x-type) and the corresponding bay style are defined separately under the class 'Qubit Utilities'.

A.3. E-BEAM PATTERN CONVERSION AND WRITING

The conversion of GDSII files to Raith e-beam lithography tool compatible **.gpf** layout is done using BEAMER software. It supports advanced features such as optimal fracturing of complex curved layouts, flexible control of field and shot placement, writing order and compensation of tooling artifacts such as proximity error correction. It is also possible to assign multiple doses to a single layer using feature dose

[1] Renamed now as SIMULIA

assignment (FDA). All the fabrication blocks except VIO pre-fab are done using e-beam lithography. In this work, we have used various holders from the EBPG 5000+ and 5200 systems which can accommodate 2 to 8-inch samples[2]. Except for the dedicated 4-inch wafer holders, height and rotational alignment are performed on the holder tables prior to loading the holder for writing. The tolerances for variation in sample tilt is $\pm 3\ \mu\mathrm{m}$, above which the Raith EBL system aborts the job writing. The device xy coordinates are acquired with respect the Faraday cup[3] devices mounted on 2-inch and 3-inch holders. Below are screenshots of the BEAMER flow along with the output for each pattern, namely the base layer, JJs and airbridges. We follow the conventional best practices for selection of important parameters such as a the beam step size (BSS) such that BSS = $\sqrt{2}\times$ Beam spot size. The selection of BSS is further dependent on the smallest feature size of the pattern being written and the desired resolution of increment in pattern size, crucial for designing reliable JJ width sweeps. Additionally, the writing time and dose are optimized based on the relationship

$$\text{Dose } (\mu\text{C/cm}^2) \times \text{Area } (\text{cm}^2) = \text{Writing time } (\text{s}) \times \text{Beam Current } (\text{nA}).$$

Here the Area refers to the region illuminated by the e-beam and not the entire write field [337]. The mainfield dimensions define the area that can be exposed in a single shot. Efficient use of the mainfield helps in optimizing throughput and reducing the overall exposure time. The largest mainfield size in BEAMER is $1.04 \times 1.04\ \text{mm}^2$. The subfield dimensions are important to ensure proper stitching and overlap between adjacent subfields in order to create a continuous pattern without defects. Stitch errors arise due to deviation in the alignment of the pattern between consecutive writing fields when the tool is performing multiple stage movements [338]. Additionally, in multi-shot exposures, the subfields must be precisely aligned and overlapped to create a seamless pattern. Misconfigurations or errors in defining subfield dimensions, overlaps, or gaps can lead to stitching errors. Other causes for stitching can also arise from imperfections in the electron optics system such as lens aberrations or distortions and inaccuracies in the scaling or calibration of deflectors which steer the e-beam [339]. The CPWs are the longest features in our layout spanning multiple writing fields. This gives rise to the possibility of stitching errors (described briefly in Chapter 4), which essentially shorts the entire CPW and is a major source of losses in physical die yield. A simple solution we identified to prevent this issue from recurring is to change the field settings from 'Fixed' to 'Floating' in the process EXPORT under the 'Advanced' tab (See Fig. A.5 for comparison). This allows BEAMER to optimize the position and number of fields for the layout, reducing the number of stage movements. This still does not fully eliminate the problem of extending across multiple fields, however we have observed a significant reduction in the number of instances of such field stitch errors. For JJs which

[2] A good tutorial of e-beam holders with a description of the components can be found in https://www.epfl.ch/research/facilities/cmi/equipment/ebeam-lithography/raith-ebpg5000/ebeam-holders/

[3] Metal conductive cup positioned at the centre top of each e-beam holder designed to measure beam current in vacuum.

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comprise the smallest features in our layout, we use the smallest mainfield dimensions $160 \times 160\ \mu\mathrm{m}^2$ with subfield dimensions $4.525 \times 4.525\ \mu\mathrm{m}^2$ in order to ensure uniform exposure of the pattern. The airbridge patterns are rendered similarly to that of the base layer. In order to execute the pattern writing, we use the software CJOB, developed by Raith which is a graphical user interface to tailor the exposures on the sample. It is similar to the drag and drop graphical interface of BEAMER to define multiple exposures on a sample. An example of the CJOB user interface is shown in Fig. A.6. The most important feature of CJOB which is used extensively in this work is marker-search based pattern alignment, described in multiple sections in Chapter 5. A snapshot of the base layer exposure showing the marker search menu is also shown in Fig. A.6. For alignment of the base layer pattern on a TSV-integrated substrate, we manually verify the location of each DRIE marker, which are roughly $30\ \mu\mathrm{m}$ diameter circles and translate the coordinates with respect to the origin 'O' instead of the Faraday cup.

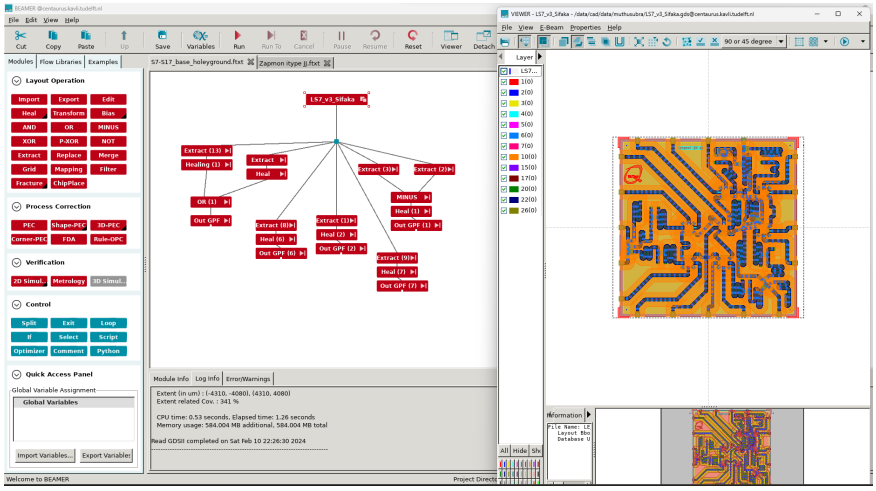

Figure A.2: Our BEAMER process flow to the left of the image. The process flow, created separately in BEAMER with file extension **.ftxt**, can be used and modified repetitively for multiple GDSII files. In this snapshot, the input GDSII file of a planar Surface-7 device is imported into the software.

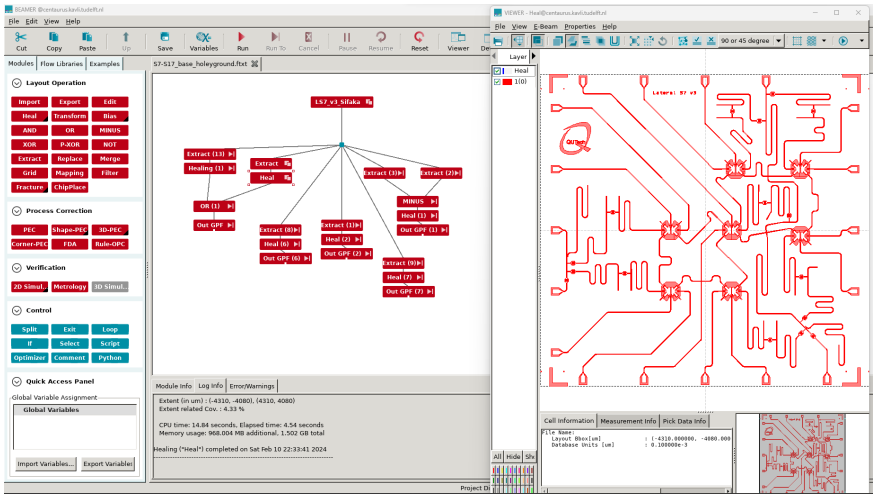

Figure A.3: The base layer comprising the launchers, CPW and qubits is extracted along with markers, using BSS = 40 nm

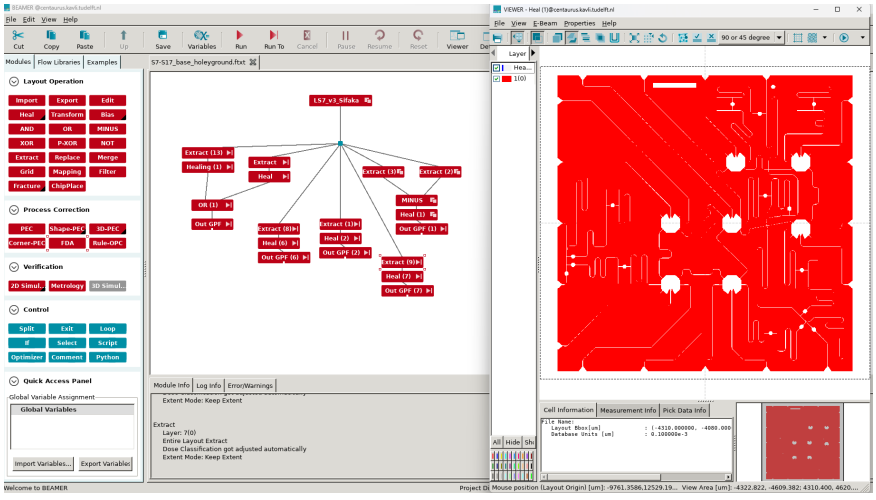

Figure A.4: The holeyground is patterned separately from the base layer with a BSS = 100 nm to minimize the writing time. The extraction of this layer involves subtracting 'Layer 3' corresponding to the holey ground layer from 'Layer 4' corresponding to the holey ground masking layer. This prevents the holey ground from being patterned all over the CPW and qubit features.

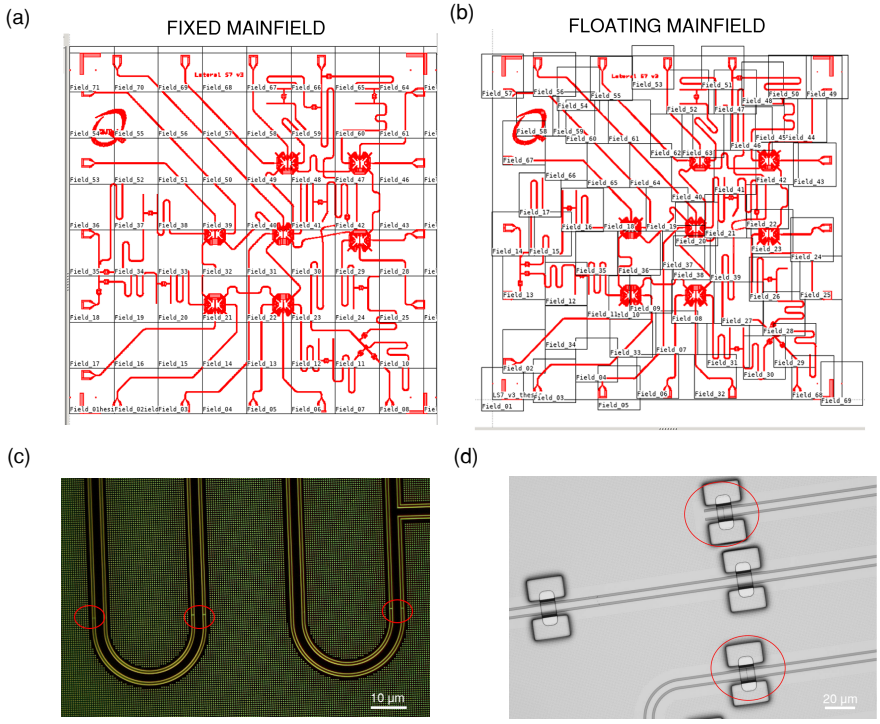

Figure A.5: Comparison of (a) Fixed and (b) Floating mainfield settings on the exported .gpf file of the base layer. Examples of stitching error induced defects, highlighted by red circles on (c) CPWs (d) airbridges.

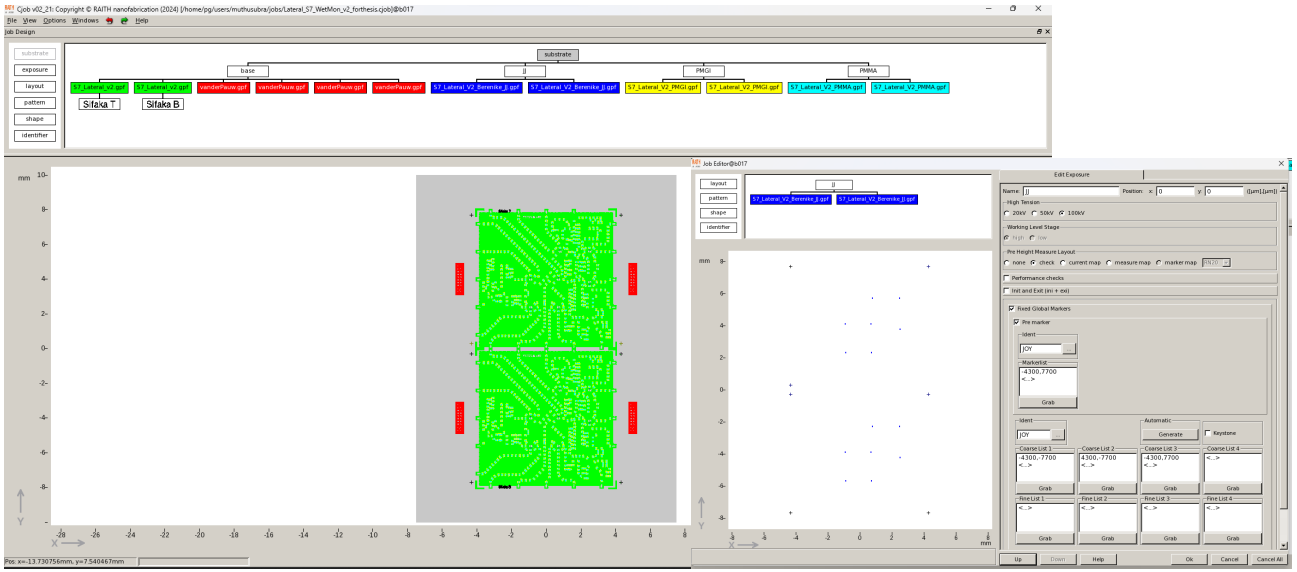

Figure A.6: Screenshot of the CJOB software with pattern writing preparation for a 15×20 mm Surface-7 device. Each exposure block comprising multiple ***.gpf** patterns can be individually exported as a ***.job** file for e-beam lithography. For each planar SQP device, we have four e-beam exposure steps, namely base layer, JJs and the two airbridge patterning steps for the airbridge scaffold and the bridge.

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A.4. JUNCTION MEASUREMENT BOX

To measure the resistance of either single Josephson junctions or nominally symmetric pairs embedded in a SQUID loop, the samples are probed at RT by the 2-point method using a manual probe station and using both 2- and 4-wire configurations using the APS-TASQ setup (described in Section 6.3.3). The primary difference between 2 and 4-wire conductance measurements is that the 2-point method is sensitive to voltage drop across the leads and cabling on applying a bias current, thereby resulting in a lower measurement accuracy. This is particularly problematic when the resistance of the DUT is in the range of $\sim 10^2\ \Omega$, as typical lead resistance ranges from $10\ \mathrm{m\Omega}$ to $10\ \Omega$. Our JJs have a typical resistance value ranging from 4–$14\ \mathrm{k\Omega}$, thereby justifying our reason for acquiring a majority of the RT measurement results shown in this work using the 2-point method. However, we do not employ the I-V sweep approach to characterize JJs due to the risk of electrical breakdown of the tunnel barrier on applying a bias current. Therefore we use a voltage source $V_\mathrm{s} = 10\ \mathrm{mV}$ giving rise to a current $I_\mathrm{s} = 1\ \mu\mathrm{A}$ applied through the junction. The circuit comprises of an inverting operational amplifier connected to a feedback resistor R_f, which has three ranges: $1\ \mathrm{k\Omega}$, $100\ \mathrm{k\Omega}$ and $10\ \mathrm{M\Omega}$ such that it forms a closed feedback loop. Normally, we operate with $R_f = 100\ \mathrm{k\Omega}$. The junction resistance R_JJ as shown in the schematic is calculated as:

$$1/G = R_\mathrm{JJ} = \frac{V_\mathrm{s}}{I_\mathrm{s}}. \tag{A.1}$$

The circuit schematic shown in Fig. A.7 represents a SQUID loop with an effective resistance R_JJ connected to the probing pads indicated by the orange squares which is connected to a *differential amplifier*. The measurement circuit consists of an inverting op-amp with a feedback resistor R_f where the potential difference between the (+) and (−) pins is $0\mathrm{V}$ forming a virtual short. In the 2-wire configuration as represented by box ①, a source voltage V_s is applied across the SQUID, with the drain electrode connected to the inverting terminal (−) of the op-amp while the (+) terminal is grounded to the circuit casing. In the linear regime, the ratio between R_f connected between the output voltage V_out and (−) terminal and R_JJ determines the amplification of V_s, with the closed loop gain expressed by the formula

$$V_\mathrm{out} = -I_\mathrm{s} R_\mathrm{f}, \tag{A.2}$$

$$\mathrm{Gain} = \frac{V_\mathrm{out}}{V_\mathrm{s}} = -\frac{R_\mathrm{f}}{R_\mathrm{JJ}}. \tag{A.3}$$

V_out is then measured using a Keithley 2000 multimeter. The shortcoming of the 2-wire configuration is that it does not eliminate the voltage drop between the probe needles and the DUT due to contact resistance, denoted as R_c. The actual JJ resistance R'_JJ is now rewritten as $R'_\mathrm{JJ} = R_\mathrm{JJ} - 2R_\mathrm{c}$. This also modifies the junction current such that $I'_\mathrm{s} = V_\mathrm{s}/R'_\mathrm{JJ}$. Substituting in Eq. A.3

$$V'_\mathrm{out} = -I'_\mathrm{s} R_\mathrm{f} \tag{A.4}$$

$$R'_\mathrm{JJ} = -\frac{V_\mathrm{s}}{V'_\mathrm{out}} R_\mathrm{f}. \tag{A.5}$$

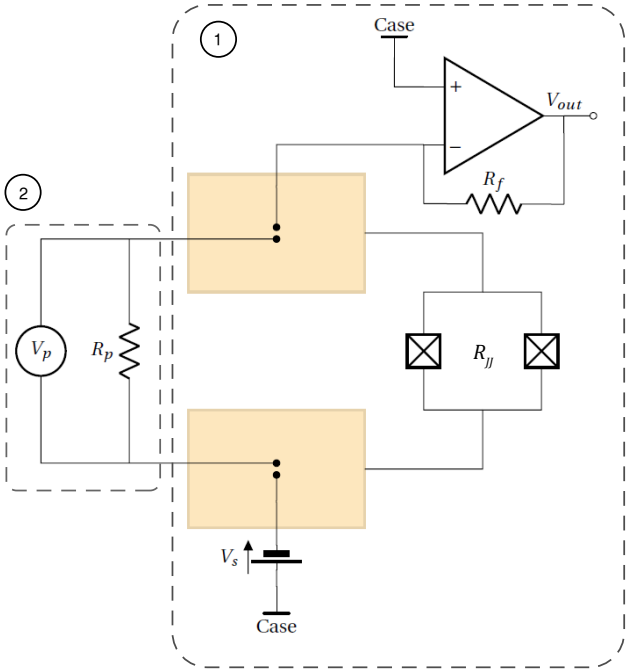

Figure A.7: Schematic of the junction measurement box circuit used for RT characterization of JJ pairs, with effective resistance R_{JJ}. Box ① is the 2-wire configuration of the setup with an input comprising of an inverting op-amp with feedback resistor. To eliminate the series contact resistance of the probe needles, a high-impedance differential amplifier is connected to the measurement circuit as represented by box ②. Reprinted from van der Zalm, (2022) [309].

In the 4-wire configuration shown in box ②, an additional pair of probe needles with nominally identical contact resistance R_c[4] and a high-impedance differential amplifier with an input resistance $R_p = 10\ \mathrm{M\Omega}$ connected in parallel to R_{JJ}, in order to prevent build-up in potential difference due to V_p when the two circuits are isolated. Since $R_p \geq R_{JJ}$, the voltage from the high-impedance amplifier is $V_p \approx I_s' R_{JJ}'$. Substituting in Eq. A.5

$$R_{JJ}' \approx \frac{V_p}{I_s'} = -\frac{V_p}{V_{out}'} R_f. \tag{A.6}$$

To quantify the role of probe contact resistance R_c (See Section **??**), we compare the difference in conductance between 2 and 4-wire configurations from a full-wafer

[4] In the APS-TASQ setup, the Form Factor DC-Q probe comes with four probe needles sharing a common ground plane where the outer needles measure the voltage drop due to R_c.

dataset using the APS-TASQ setup. The 2-wire conductance (G_{2w}) is related to R_c and 4-wire conductance (G_{4w}) as

$$G_{2w} = \frac{G_{4w}}{1 + R_c G_{4w}}. \tag{A.7}$$

We compare 2 and 4-wire G measurements acquired from the 35×35 layout planar TiN/Si wafer (*Nighthawk-ALD 3x*) and from NbTiN/Si wafer with enlarged JJ contact pads (Refer to Fig. 5.13) as shown in Fig. A.8. Ideally the difference between G_{4w} and G_{2w} should be minimal if the needles are centred within the probing pads and the motorized Z-stage is properly calibrated to land the needles uniformly throughout the wafer, as in the case of Fig. A.8(a,c). For the case of the dataset from *Blackbird 1xl* wafer, the sensitivity of the 2-point G values to a voltage drop across R_c is evident from the deviation of G from the diagonal, shown in Fig. A.8(b,d).

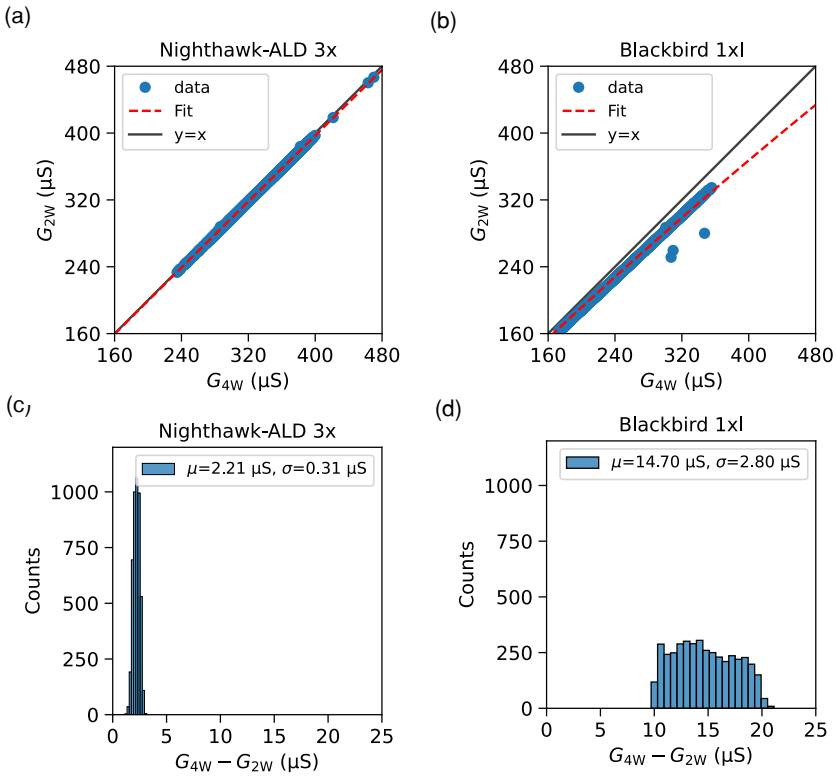

Figure A.8: Comparison of 2 and 4-wire measurements using the full-wafer datasets. The fits are plotted using Eq. A.7 (a) *Nighthawk-ALD 3x* containing 4631 datapoints of JJ test pairs post filtering of defective junctions, with $R_c \approx 19\ \Omega$ from the fit. (b) *Blackbird 1xl* containing 4120 datapoints of JJ test pairs post filtering, with $R_c \approx 223\ \Omega$ obtained from the fit (c, d) Histogram of $G_{4w} - G_{2w}$, where the μ and σ indicate the mean and SD. Note: Outliers above $30\ \mu S$ are filtered out in (d).

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A.5. MULTI-ANGLE EVAPORATOR OPERATIONS

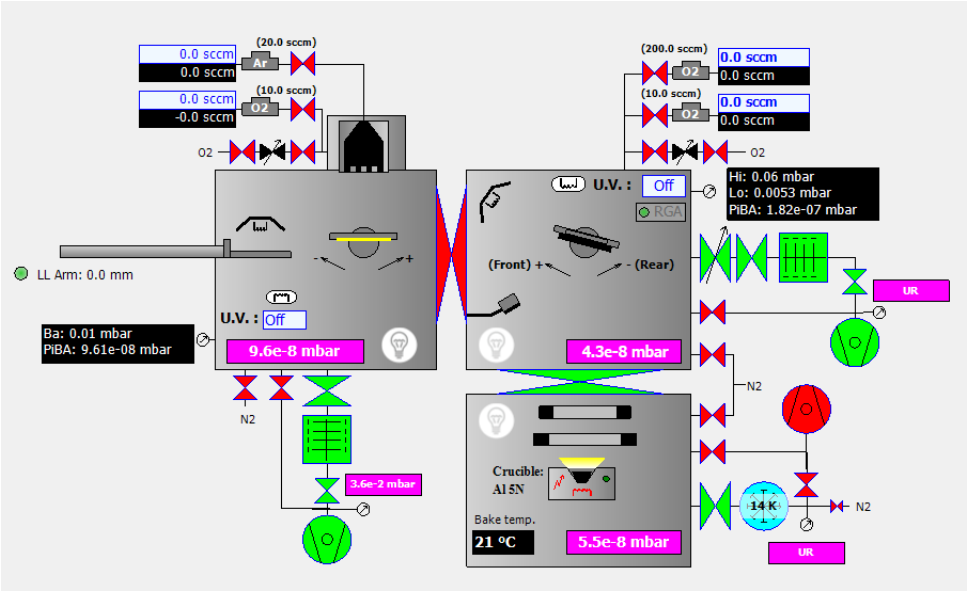

Figure A.9: Process conditions in the Plassys MEB 550S multi-angle e-beam evaporator during the deposition of the first electrode. In the schematic, the shutter connecting the process chamber and the lower chamber is green, indicating it is open.

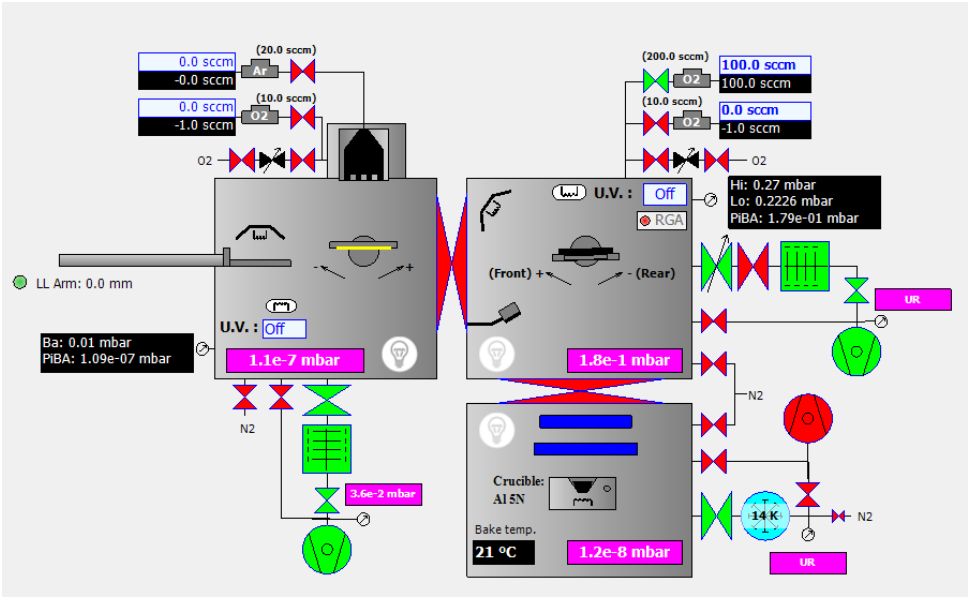

Figure A.10: Process conditions during the in-situ oxidation step with 6N purity O_2 using a partial pressure of 1.3 mbar. In the schematic, the shutter connecting the process chamber and the lower chamber is red, indicating it is closed.

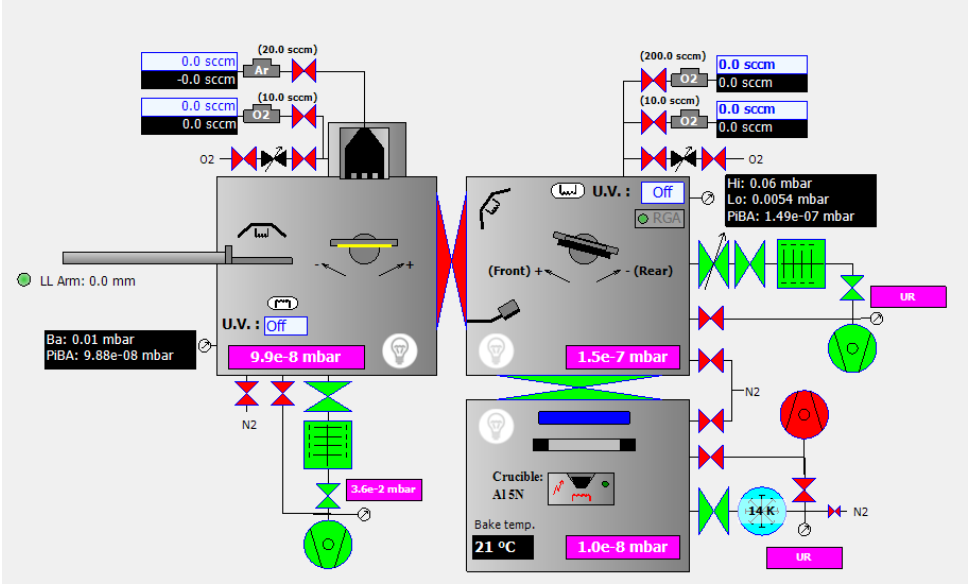

Figure A.11: Process conditions during the second Al deposition step. The process chamber pressure is half an order of magnitude higher after pumping out the chamber of residual O_2 gas.

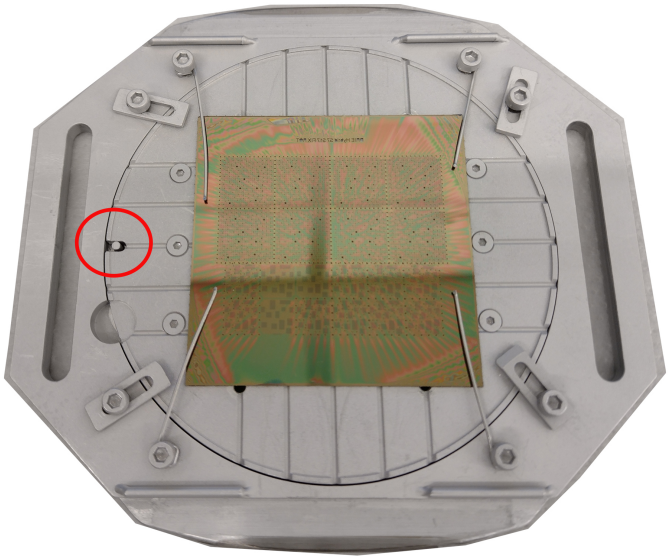

Figure A.12: Snapshot of the Plassys evaporator holder with *Valkyrie 3i* wafer. The alignment reference, marked in red to the left of the holder is used to preset the rotation of the sample with respect to the holder. For samples with Dolan-bridge junctions, as in this picture the sample is mounted at 0° rotation with respect to the holder, for Manhattan JJs the sample is mounted 180° with respect to the holder.

A.6. FRIDGE WIRING DIAGRAM

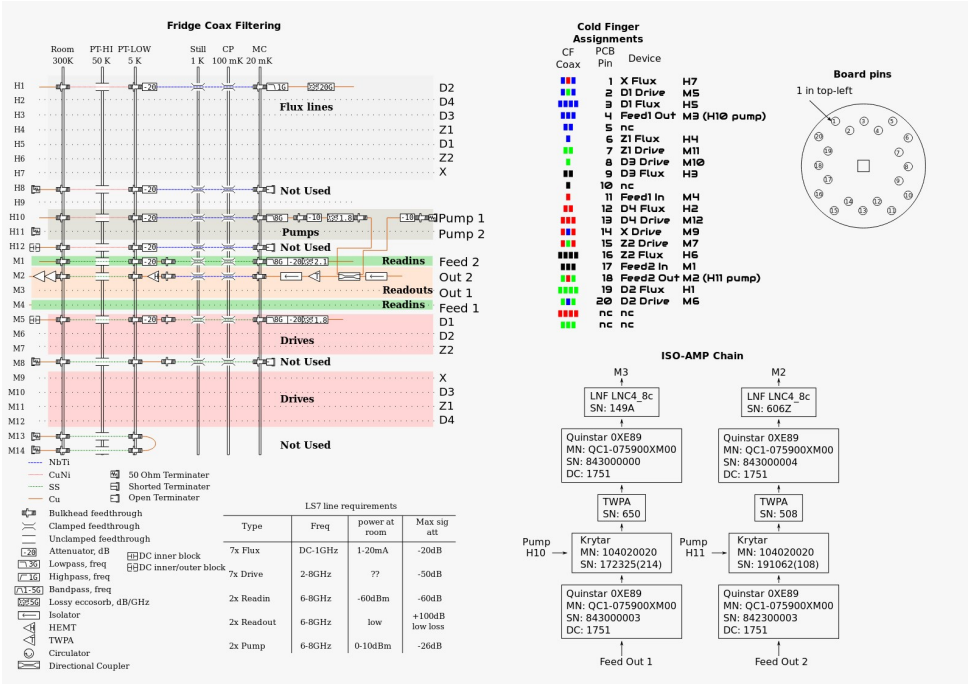

Figure A.13: Fridge wiring diagram for a Surface-7 device. Image credit: Dr. Matthew Sarsby, DiCarlo Lab.

ACKNOWLEDGEMENTS

Words fail to capture the journey of the past ten years that has brought me to this juncture in life. What began as, perhaps a whim to transition from chemical engineering to applied physics has profoundly reshaped my psyche and outlook on life. It has been, in essence, a gruelling, disorienting, and, most importantly, humbling experience; one that has allowed me to forge deep, meaningful connections and bonds with the people I acknowledge here. This, in many ways, makes this the most significant chapter of my thesis.

Achyutha, you gave me the wings to make that daring jump across the Atlantic as I was winding up in Baltimore, where you were helping me move out of my apartment while I was writing my Masters thesis. Ten years later, you're still here with me, helping me pack up from our loving home in Den Haag. In the years between, despite the distance — whether between the Netherlands and India or the Netherlands and the USA, the months-long lockdowns of the COVID-19 pandemic, our health scares, emotional upheavals, and financial uncertainties, you held onto me and my sanity and pumped in strength when I was losing it. We have almost made it, I dream and hope that our journey continues on towards the next chapter of our lives.

I am extremely lucky to have been blessed with parents like *Lakshmi amma* and *Srikanthan appa*, whose unwavering support kept my fire alive through countless moments of doubt and delay. Amma, your daily phone calls at 13:00 CET were a source of comfort and strength, energizing me throughout these years. I have strived to live by your wise words, translated from Tamil: *"There is nothing a woman cannot achieve if she sets her mind to it"* Appa, you have been my rock, always helping me focus on the most important challenges of the day and guiding me with calm wisdom. I am greatly thankful to *Dr. Shanti Neelakesi*, a good friend of Amma for her help and expertise with drafting a Tamil version of my PhD summary.

While love might have been the clarion call for my move to Netherlands, what set my sights on Delft is the world-class academic cleanroom hosted by the *Kavli Institute of Nanoscience* (whose logo I am proud to showcase on the back thesis cover). Therefore my first note of thanks goes to the training and administrative staff of Kavli Nanolab, for fostering an open and productive atmosphere to learn nanofabrication processes from the ground up. I am proud to be a part of this hard-working and passionate community of fellow *fabbers*, from whom I have learnt a lot and have been privileged to give back. I wish to specially thank *David Thoen* for supervising the Nordiko 2000 sputtering tool and the Leybold Heraeus F3 RIE system for depositing and etching NbTiN. The discussions I had with you on the details of sputtering a superconducting alloy gave me many insights, which have contributed towards writing this thesis.

A special person from this community, who was the first friend I made a decade ago coming to TU Delft is *Alessandro Bruno*. I still vividly remember our first meeting at a FOM Veldhoven conference after-party, egregiously conversing beyond physics-related topics. Our joint birthday bashes many years ago were a raging hit and still fondly reminisced; to have 75 people under one roof being fed, watered and entertained was honestly quite the logistical feat. Since then, our friendship has only deepened, leading to multiple fruitful collaborations, with the laser annealing project being a standout among many. I am eternally grateful for your mentorship, particularly in teaching me the intricacies of fabricating superconducting qubits, and for your infectious enthusiasm, which sparked my passion for this field of research. You will always have a friend in me, just as I know I will always have one in you.

It is a profound honour to be able to write this PhD dissertation on a core topic of practical quantum computing, especially coming from a non-physics background. This achievement is a testament to the exemplary supervision of my PhD promotor, *Leonardo DiCarlo*. Leo, you have taught me invaluable lessons in life with your uncompromising commitment to excellence in research, personal discipline, ethical reasoning and strategic thinking. The topic of my PhD thesis is inspired by your clear directive, *"Nands, you need to fix the E_J problem!"* and boy am I glad that I embraced this challenge! Through this, I discovered a deep passion for Josephson junctions, and as I began recognizing patterns in the failure modes of the devices we fabricated, this work became a personal obsession. Formulating these observations into an elegant geometric model is thanks to your acuity and prowess on the shadow evaporation process used for junctions. I admire your keen ability to identify the essential problems and to steer our research toward innovative solutions. Beyond technical knowledge, you instilled in me the importance of rigour and creativity in scientific thought, and the value of perseverance when tackling complex problems. Last, but not the least, I am a big fan of your oratorical skills, I would never want to miss an opportunity to hear you give a seminar talk. I am eternally thankful to you for offering me this once-in-a-lifetime opportunity to perform world-class research in this exciting and rapidly advancing field of quantum physics. You not only shaped my career but also helped me grow as a scientist and a person. Your mentorship will remain an enduring influence on both my professional and personal journey.

Team spirit has always been a defining feature of working in the DiCarlo lab, and rightfully so thanks to the big-hearted colleagues I had the fortune to work with. For a brief period during the pandemic, the DiCarlo lab's OG nanofabrication team was formed which included *Ale, Christos Zachariadis, Matvey Finkel* and myself. The spurt in productivity was palpable, we collectively migrated towards wafer-scale fabrication and developed the APS-TASQ setup specifically tailored for this transition. *Christos*, your relentless dedication and speed in fabricating multiple Surface-17 devices were truly awe-inspiring. Thanks to your deftness and expertise with the Bosch process, we were able to produce perfect, defect-free TSV substrates for our wafer-scale JJ paper. Your humility, wicked sense of humour and military-like discipline are qualities I deeply admire, and I'm honoured to have you by my side as my paranymph at the defense ceremony.

Matvey, we have known each other for a very long time as well, first as colleagues in Quantum Nanoscience department and now in QuTech. When Ale moved to QuantWare, you became my go-to person for advice and critical feedback. I cherished our in-depth discussions and even our occasional heated debates over the various fabrication challenges we faced. You pushed me to tackle junction ageing systematically, and though I had less than eight months left in my PhD, it became my favourite project, delving into material science and chemistry, areas which are my forte. I will always remain indebted to you for helping me with acquiring additional data for our wafer-scale JJ paper after my PhD tenure had ended, without your contributions, we would not have been able to publish it with such confidence. I also thank you for helping me prepare for my defence with mock sessions.

When Leo suggested it was time for me to mentor Master's and Bachelor's students, I initially felt skeptical, and perhaps a bit fearful, about whether I could successfully guide students to complete their projects, especially in the midst of the COVID-19 pandemic. But once I got to start working with and for each one of you, *Pim Duivestein, Sean van der Meer, Martijn Veen* and *Joost van der Zalm*, a fierce sense of responsibility and determination supplanted all the doubts, and I could only see one outcome: success. The four of you are collectively the pillars on which my PhD dissertation is built.

Pim, you led from the front on performing the wafer-scale fabrication of junctions and giving me that much-needed extra pair of hands to literally manually measure thousands of junctions. *Sean*, you followed suit immediately with setting-up the APS-TASQ setup and automated laser annealing protocols, helping us automate full-wafer measurements. Your mastery with Python programming helped us set up an incredible, ergonomic custom-built tool on a very tight financial as well as time budget. I expect nothing less from you in terms of your ambition to also finish your PhD in DiCarlo lab with the same level of aplomb and finesse.

Martijn, I absolutely had a blast co-developing `pyclq` with you, I think everyone around us underestimated how seamlessly the software suite worked. That look of bewildered excitement on Leo when you did a live demo of the airbridge defect detection was priceless. Besides our fruitful collaboration, I found a fellow kindred spirit in you with a love for plants, critters and a passion for the arts. You inspired me to organize our quaint painting parties where we simply let our creative juices flow between the palette and paper along with the company of our beloved Sean, *Rebecca Gharibaan* and *Bas van Asten*.

Joost, I am thankful and lucky for the level of trust we built in our working relationship while navigating the path to success in the junction ageing project. Despite the numerous delays in the cleanroom and my motorcycle accident, I was grateful that you remained calm and stayed committed to the systematic approach that underpinned the success of this project. Our partnership is not over yet; I have promised myself that I will work toward publishing the results with each of my students, and I will do my best to do the same with our bidirectional junction annealing work.

I am grateful to *Andreas Fognini*, *Ronan Gourgues* and *Jin Chang* during their tenure at Zwiller lab for providing access to their laser setup and helping me with optimizing the experiments for consistent results. I am extremely thankful to *Tessel*

van der Laan, who during her tenure at QuTech guided me towards *Ronald Hagen* from TNO for building the laser annealing setup. Thanks to Ronald's expertise, the laser optical path was built quickly and efficiently which remains functional to this date in the upgraded APS-TASQ setup.

Thijs Stavenga, we started roughly at the same time in the group but somehow we didn't really get started with conversing until the geometric model conundrum. I was surprised and delighted by your alacrity, veiled by your subdued personality. This was the turning point for me, when I started talking more often to you. During the thesis writing stage, you became my confidant, helping me in subtle yet significant ways to improve how I presented my data. You are a rare person, and I hope our paths continue to cross in the future.

Christian Dickel, we have known each other for a long time even before I joined DiCarlo lab. I remember your mischievous antics at the joint MED-QT *uitjes* back in the days, its hard to ignore you I must say! You are the one who embraced and brought me in the company of fellow QT folks (later renamed to QuTech), I truly felt I belonged among you guys. Your Wednesday evening *Delftse da da jams* were a sensation, I remember *Nathan Langford's* haunting rendition of Bill Withers' *Ain't no sunshine* on the keyboard and *James Kroll's* crazy guitar skills coming to life during these sessions. You are incredibly multi-talented yourself, on one side improvizing your violin skills while blaring a full-throated Rage Against the Machine song. I mean, who can forget you belting out *'Killing in the name of'* during your post-PhD defence party?! During the year and a half we overlapped in the DiCarlo lab, I struggled to adapt to its fast-paced dynamics, and I took many cues from you, especially on how to present myself and avoid sounding too high-pitched when giving counterarguments. Your PhD thesis remains a staple on my reading list, and I'm so thankful you put in the time and effort to write such an elaborate introduction chapter, which helped me connect the dots between the various concepts related to superconducting qubits. I'm also grateful that you took on the role of an older sibling, continuing to talk to me whenever I got stuck writing my thesis. The icing on the cake was our discussion about the role of surface roughness on junction harmonics, based on your recent publication with IBM. This was the missing link I needed to make sense of the data I had gathered from my Surface-7 devices. I will definitely stay in touch with you and *Jasmin*, a visit to your place is long overdue. I hope I keep my promise once my PhD is finally complete.

Ramiro Sagastizabal, you have been an incredible compadre, always ready to help me understand and interpret measurements from our devices. Throughout my work and even while writing this thesis, I frequently referred to your sketches and notes, which explained the various formulas connecting qubit design with measurement parameters. The 3-qubit device you created along with *Xavieret Bonet* for the variational quantum eigensolver (VQE) project was the very first chip I worked on in the DiCarlo lab. I was over the moon when you got to first work with the Surface-7 *Chimera* device for your project on generating thermofield double states. Having you and Ale at my wedding in India was a truly cherished moment that I hold dear to this day. I'm excited at the prospect of working with you again in Barcelona.

Dave Michalak, you completely shattered the stereotypes I had about industry-

based scientists working for large U.S. multinational corporations. Your humility, ability to handle tense situations with ease, keen discernment of what to say and when, and your foresight in designing experiments for scalability are traits I deeply admire. Years ago, your suggestion to devise a 6-port resistance measurement to individually characterize the resistances of the junction electrode contact region and the overlap area opened my eyes to the significant impact of contact resistance on room-temperature conductances of Josephson junctions. I am grateful to have had the opportunity to work alongside you and to have learned from one of the best.

Stefano Poletto, I am extremely thankful to you for walking me through the baby steps of chip design and teaching the basic principles of microwave engineering, including design of coplanar-waveguide resonators. I was very happy we connected again during March Meetings in Boston and Chicago. *Florian Luthi*, I remember your comforting presence right behind me in the common office area on the B-wing second floor. You've helped me multiple times when I was trying to debug my scripts or when I was trying to find some relevant papers and also watered my plants when I was away on holidays. Thank you for your good-will and I hope we get to bump into each other sometime in the future. *Nadia Haidar*, although we only briefly overlapped, I fondly remember our fun conversations and your inputs on simulating earlier versions of Surface-7 devices. I deeply respect your work, I was enthralled to learn that you have started your own research group at EWI. I wish you all the very best and I hope to keep in touch with you. *Brian Tarasinksi*, thank you for spending long late nights waiting for me to bring the freshly wirebonded chips to cool down in the fridges. Thanks to your brilliance, I got to learn more about the Bluefors XLD dilution fridges. *Pagani* remains my favourite fridge because of the fond memories I shared with you. I vividly remember the laidback barbecues organized by you and *Viacheslav Ostroukh* in Leiden, I was thrilled to be accepted by theoretical physics community!

I wish to extend my gratitude to *Filip Malinowski* and *Luc Janssen* for the detailed characterization of the Zapmon devices used for the proof-of-concept laser annealing experiments. *Luc*, your bachelors thesis was instrumental in understanding the limitations of the Violet laser setup and enabling us to move on to the APS-TASQ setup. *Niels Bultink, Adriaan Rol,* and *Tom O'Brien*, thank you for giving me the opportunity to fabricate devices for your experiments. *Adriaan*, as you so eloquently put it in your own acknowledgements, thank you for being a constant presence in my life for nearly nine years. Whether I sought your advice on tricky matters of the mind or heart, you always helped me untangle my thoughts, separating emotions from reason to make clear-headed decisions.

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Hany Ali, *Jorge Marques* and *Miguel Moreira*, the three of you are a force to reckon with in the world of qubit measurements and it is no wonder that you collectively pushed the envelope on advancing quantum error correction and quantum neural networks respectively. Thanks to your insights, I became very interested in learning and understanding more about connecting the dots between QEC and the failure modes in device fabrication. *Hany*, I especially thank you for your generosity with Egyptian seafood and the Iftar party festivities at your home along with *Juwahar*. *Santiago Valles*, I was amazed by your level of dedication and independence during your Masters project. Your sincerity towards science drew me to help you in any way I could while you were trying to draw some finite conclusions out of a rather difficult project. I wish you the very best of success in finishing your PhD thesis and your future scientific endeavours.

Ruggero DiCarlo, I might have come across as a bit direct during your interview with the group, I still wonder what triggered that response from me. But just weeks later, I realized that I had developed an almost instant fraternal bond with you when I learned about your struggles to find a place to stay in the Netherlands. Without hesitation, I opened my home to you, even though my own future in the country was uncertain at the time. You have a rare, endearing ability to show empathy far beyond your years. I think of you as my younger brother, and I am incredibly thankful for the help you gave me when I was moving out of my home in Den Haag. It felt poetic when we reminisced about the good times spent there. I bid a tearful goodbye now, but I promise I will be there for your PhD defense, no matter where I am.

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when you came to Delft almost a decade ago. I have enjoyed your companionship on many occasions over the years, your chill and soft-spoken demeanour outside of work has soothed me whenever I didn't have a good outing in the cleanroom. I hope our friendship stays sealed and cemented as the years pass. *Raymond Schouten* and *Raymond Vermeulen*, not many experimental PhD students at QuTech could find their way with acquiring data without your help with configuring and debugging measurement electronics. *R. Schouten*, I especially thank you for your time for sitting and explaining to me about op-amps and about the junction measurement box which we used for measuring RT junction conductance. *Charlotte van Hees*, thank you for the wonderful initiative of launching the QuTech Female Scientist Lunches, I think it really helped the female members of QuTech come out of their shells and interact more openly with their peers. I sincerely thank the QuTech management assistant staff *Marja Plas*, *Jenny Boks-Zondervan* and *Romina Bisetti* for your help with documentation, keeping my TIM hours in sync with my project code, help with placing orders, laptop purchase and repair and finally with my PhD thesis printing.

The last phase, probably the toughest phase I experienced during this journey was during the dissertation writing period. I couldn't have balanced a full-time job along with the rigour of writing the dissertation without the help of my precious colleagues *Mathilde Lemang, Merve Tamer Dorian Oser, Lars Friesem, Kiki Schuurman* and *Burcin Ulgen*. Thank you for empathizing with my pain and for giving me the space to attend to thesis as well as my family needs. You came in at the very last phase of my life here, but I am glad you did, thank you *Polina Vabishchevich* I hope we get to spend more time together in another part of the world.

From my previous life in TU Delft at Quantum Nanoscience, a few good friends did stick along with me as I decided to give another shot at doing a PhD. First and foremost in that list are *Nikos Papadopoulous* and *Andrea Mitrovska*, I cannot remember the number of times I have leaned on your shoulder during times of difficulty. You guys are family to us, I will truly miss *Adam* and *Ria*. Everytime I have come to spend time with you, I have felt at home. I am so happy that our meeting in Delft has led to such as fulfilling friendship with both of you. *Ignacio Olavarria*, no matter the time zone difference, I am so glad that I have an incredibly caring and genuine friend in you. I thank you for all the wishes and the encouragement over the years. *Venketash Seshan*, you were one of the influential voices which convinced me to give another go at fulfilling my dreams. Thank you for that gentle nudge. *Martijn Cohen* and *Ranko Toskovic*, I know it has been long overdue since I threw my own PhD party. I toast one for our friendship which has endured and kept us endeared to each other all these years.

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EDUCATION

2001–2007 Secondary school
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Promotors: Prof. dr. L. DiCarlo and Prof. dr. ir. L. Kuipers

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Glossary

absorption coefficient Reciprocal of the depth of penetration of radiation into a bulk solid at which the intensity of the incident radiation is attenuated by the solid to 1/e of its initial value at a distance $\lambda/4\pi k$ from the surface boundary where k is the extinction coefficient. Source: www.reading.ac.uk/infrared/technical-library/substrate-optical-theory-introduction/absorption-andextinction-coefficient-theory. 126

AC Stark shift Also known as Autler-Townes effect. It is the alternating current equivalent of the Stark effect The Stark effect in the context of microwave superconducting circuits refers to the shift in energy levels of the qubit states due to an external electric field.. 22

BOE Buffered oxide etchants are blends of 49% hydrofluoric acid (HF) and 40% ammonium fluoride (NH_4F) buffer in various predetermined ratios. The buffering helps maintain a relatively constant etch rate by stabilizing the pH of the solution. An example of a commercial preparation of BOE consists of 7:1 volume ratio of H_2O and HF : NH_4F is 12.5 : 87.5 wt.%. Source: General Chemical Technical data: BOE® Buffered Oxide Etchants. 40

Bosch process A strongly anisotropic etching process of silicon which involve cyclical etching using SF_6 as the etching gas and C_4F_8 as the sidewall passivation gas. Source: https://www.samcointl.com/opto/basics-bosch-process-silicon-deep-rie/. 42

Brownian motion The random motion of particles suspended in a fluid at thermal equilibrium due to collisions with other molecules.. 16

Clifford gate Clifford gates are elements of the Clifford group that encompass a set of quantum operations that map the set of n-fold Pauli group products into itself. The simplest Clifford group in multiqubit quantum computation is generated by a restricted set of unitary Clifford gates - the Hadamard $\pi/4$-phase and controlled-X gates. Source:[344]. 4

coherence length ξ_0 The superconducting coherence length is a measure of the size of the Cooper pair. It describes the distance of propagation of fluctuations in the Ginzburg-Landau order parameter. It strongly depends on the energy gap and temperature. Source: [345]. 11

conformal mapping A conformal mapping is an angle preserving transformation also known as biholomorphic map. Important in complex analysis with applications in several areas of physics and engineering. Source: https://mathworld.wolfram.com/ConformalMapping.html. 27

Coulomb blockade The obstruction of charging and discharging in a nanoscale system to a single-electron limit due to repulsion between electrons in the island and the leads.. 15

cross-Kerr It is a second-order effect arising from the non-linearity that is induced in a resonator by the higher energy levels of a dispersively coupled qubit. Cross-Kerr interaction can be realized by coupling two qubits of different frequencies via a resonator or vice versa. . 66

elliptic function Class of mathematical functions in complex analysis that are doubly periodic such that $f(z)$ is analytic and has no singularities except for poles in the finite part of the complex plane. Elliptic functions with a single pole of order 2 with complex residue 0 are called Weierstrass elliptic functions. Elliptic functions with two simple poles having residues a_0 and $-a_0$ are called Jacobi elliptic functions. Source: https://mathworld.wolfram.com/EllipticFunction.html. 28

emmissivity It is the ratio of thermal energy radiated from a material's surface to that emitted by a blackbody at a given temperature wavelength and standardized viewing conditions. Source: [346]. 139

epitaxial It is the process of crystal growth or deposition of thin film that is well-oriented in its crystallographic axis to that of the substrate or the seed layer. This promotes uniform film growth in terms of thickness and composition and minimizes introduction of crystal defects and dislocations.. 77

forming gas A mixture of H_2 and N_2 of varying mole fractions between 5–20% H_2 by volume obtained from dissociation of ammonia.. 125

gauge-invariant An electrodynamic property by which scalar and vector potentials describing a physical system remain constant under local transformations. Source: https://en.wikipedia.org/wiki/Gauge_theory. 9

Gaussian beam A light beam whose electric field profile in a plane perpendicular to the beam axis can be described with a Gaussian function with a corresponding intensity profile. Source: https://www.rp-photonics.com/gaussian_beams.html. 127

Johnson noise The noise arising from thermal agitation of charge carriers in a electrical conductor at equilibrium which gives rise to random fluctuations in the voltage across its terminals. It is a white noise as the power spectral density is independent of the frequency spectrum. Source: https://en.wikipedia.org/wiki/Johnson–Nyquist_noise. 14

Kirchhoff's law Two equalities that describe the conservation of charge and energy in lumped element model of electrical circuits. It comprises the junction law (also known as current law) and closed loop law (also known as voltage law). Source: https://en.wikipedia.org/wiki/Kirchhoff's_circuit_laws. 14

leakage It refers to the undesired population of states outside the computational subspace. Superconducting qubits operate in a two-level quantum system where the computational basis states $|0\rangle$ and $|1\rangle$ represent the logical 0 and 1 states.. 5

London penetration depth λ_L The London penetration depth is the distance inside the surface of a superconductor at which the magnetic field reduces to e^{-1} times its value at the surface. The value depends strongly on temperature and becomes much larger as $T \to T_c$. Source: [139]. 11

no-cloning theorem The no-cloning theorem claims that a quantum device cannot be constructed to generate an exact copy of an arbitrary quantum state $|\Psi\rangle$ namely to perform the following mapping $|\Psi\rangle \otimes |0\rangle \to |\Psi\rangle \otimes |\Psi\rangle$. It fundamentally reinforces the Heisenberg uncertainty principle in quantum mechanics. Source: [347].. 3

Norton equivalent A theorem in circuit analysis which states that any linear circuit containing several energy sources and resistances can be replaced by a single current source in parallel with a single resistor. Source: [348]. 29

paraxial approximation An approximation to the full equations of optics that is valid in the limit of small angles from the optical axis. Source: https://scienceworld.wolfram.com/physics/ParaxialApproximation.html. 128

piranha solution A strong oxidizing agent which is a mixture of 3:1 sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). The generation of oxygen free radicals from the reaction causes the dissolution of elemental carbon.. 39

proximity effect correction It refers to the minimization of unintentional broadening of an e-beam resist pattern due to forward and back scattered primary electrons. It depends on density and atomic weight of the substrate and resist as well as the energy of the primary electrons. The energy distribution of the scattered electrons is approximated as the weighted sum of several Gaussian distributions constituting the proximity function. Source: GenISys BEAMER User Manual. 48

quadrature signals (I/Q) Quadrature signals, also known as I/Q signals are a pair of sinusoid signals that have the same frequency and a relative phase shift of 90°. They form the basis of complex RF signal modulation and demodulation, both in hardware and in software, as well as in complex signal analysis. Source: https://www.tek.com/en/blog/quadrature-iq-signals-explained . 56

resist reflow Thermal heating of resist above its glass transition temperature (T_g) post development.. 51

Standard Clean-1 (SC-1) A silicon wafer cleaning process using a hot, alkaline solution of 30% hydrogen peroxide (H_2O_2) and 28% ammonium hydroxide (NH_4OH) in DI H_2O in 1:1:5 ratio, otherwise known as APM mixture. Part of the 'RCA Standard Clean' recipes developed by Radio Corporation America for removal of particulate and organic contaminants. Source: [196]. 39

Standard Clean-2 (SC-2) A silicon wafer cleaning process using a hot, acidic solution of 37% hydrochloric acid HCl and 30% H_2O_2 in DI H_2O in 1:1:6 ratio, otherwise known as HPM mixture. Part of the 'RCA Standard Clean' recipes developed by Radio Corporation America for removal of metal ion contaminants introduced after SC-1 cleaning. Source: [196]. 39

transpilation Process of translating quantum circuits or algorithms through a series of transformations to make them compatible for specific quantum hardware characteristics. Popular tools for transpilation in quantum computing include Qiskit's transpiler module. Source: https://docs.quantum.ibm.com/api/qiskit/transpiler. 2

zero-point energy The fluctuations in the lowest-possible energy state of a quantum mechanical system at absolute zero temperature due to manifestation of the Heisenberg uncertainty principle is referred to as the zero-point energy. Vacuum fluctuations lead to the existence of zero-point energy in empty space as per quantum field theory. Source: [349]. 27

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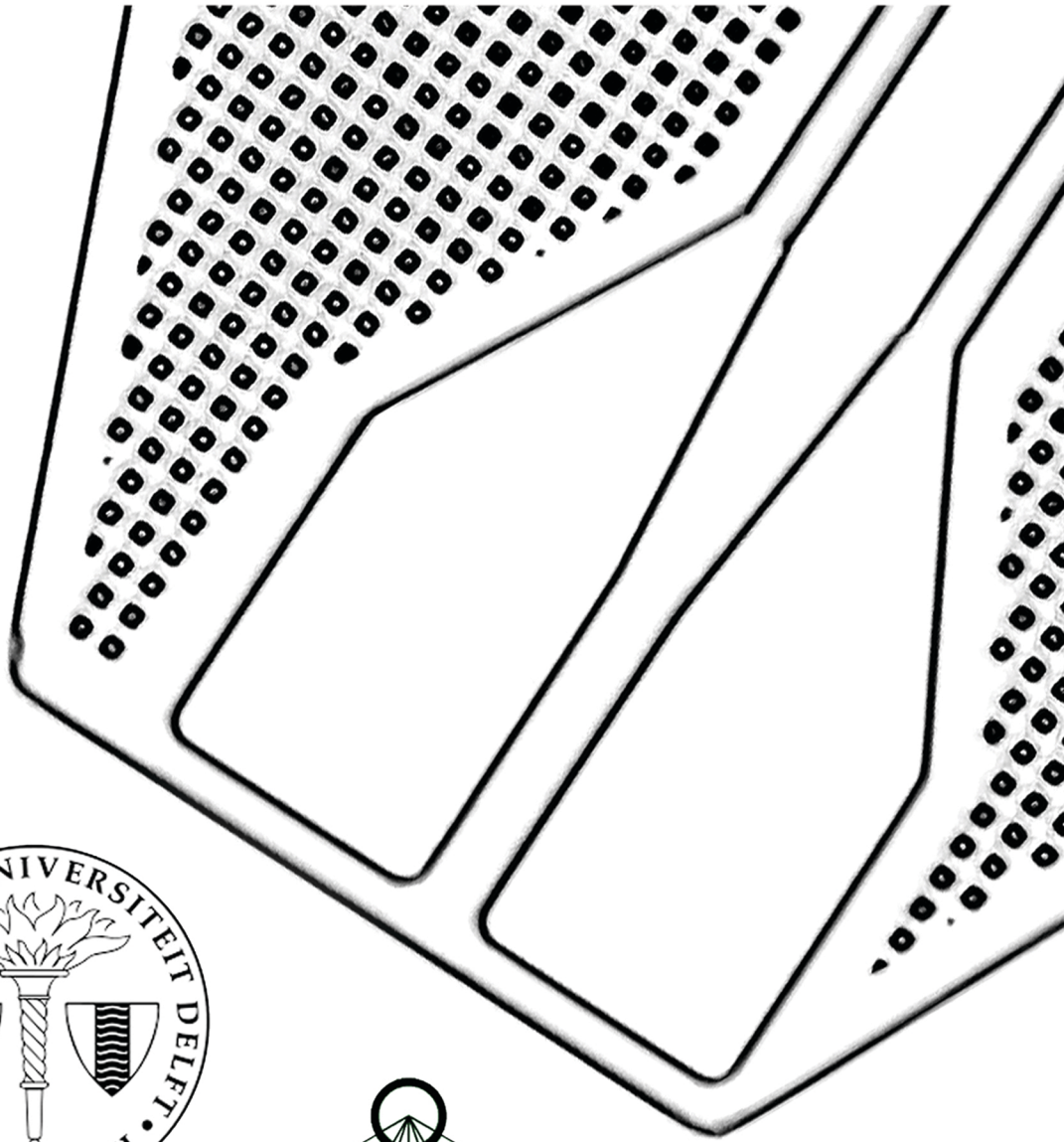

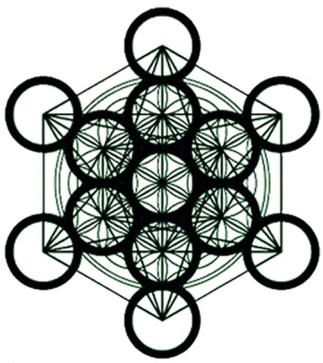

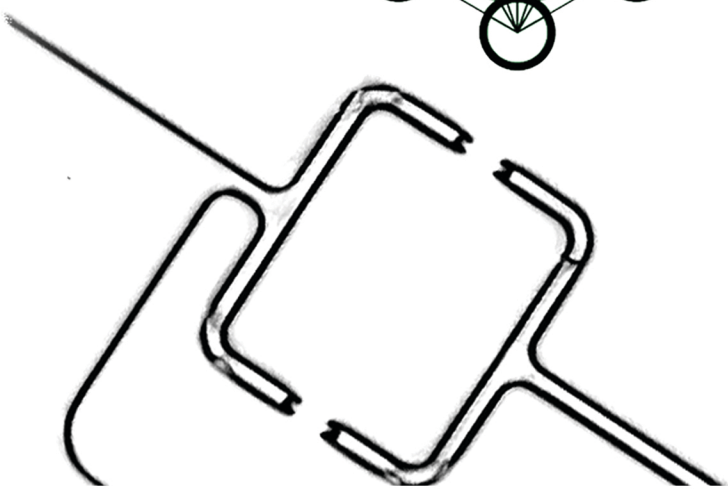

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