Silicon Micromachining of High Aspect Ratio, High-Density Through-Wafer Electrical Interconnects for 3-D Multichip Packaging

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***Abstract*—This paper presents a novel silicon micromachining method, which combines tetra methyl ammonium hydroxide (TMAH) etching and deep-reactive ion etching (DRIE) along with bottom-up copper electroplating, to fabricate high-density and high-aspect ratio through-wafer electrical interconnects (TWEIs) for three-dimensional multichip packaging. The silicon wafer was locally etched with TMAH from the backside until the desired membrane thickness was reached, and then DRIE was performed on the membrane until the holes were etched through. TMAH etching preserved large areas of the wafers at the original thickness, thus, ensuring relatively strong mechanical strength and manipulability. DRIE made it possible to realize high-aspect ratio holes with minimized wafer area consumption. A new bottom-up copper electroplating technique was developed to fill the high-aspect ratio through-wafer holes. This method can avoid seams and voids while achieving attractive electrical features. Through-wafer holes, as small as 5 μm in diameter, have been realized by using the combination of TMAH and DRIE, and have been completely and uniformly filled by using bottom-up copper electroplating.**

***Index Terms*—Copper electroplating, deep-reactive ion etching (DRIE), interconnect, packaging, through-wafer, tetra methyl ammonium hydroxide (TMAH).**

I. Introduction

To SATISFY the increasing needs for functionality and performance, integrated circuits (ICs) use more and more transistors, which require more electrical interconnects occupying more chip space despite the continuous reductions in feature size. This leads to inefficient use of silicon and high cost. Furthermore, with the increase of chip size and the complexity of interconnects, long global interconnects induce large signal propagation (*RC*) delay that can offset the speed increase of ICs benefits from the reduction in feature size [1].

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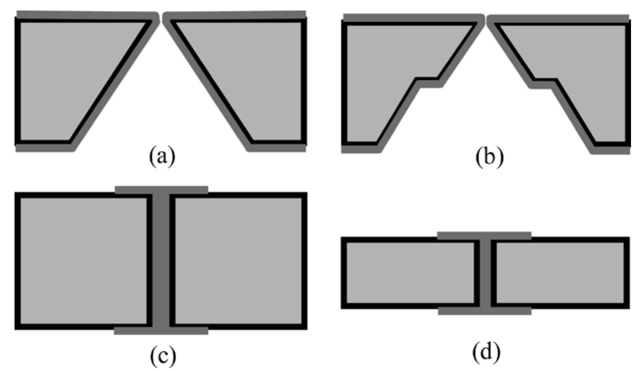


Fig. 1. Schematic configurations of TWEIs. (a) Wet anisotropic-etched whole-thickness wafers by KOH. (b) Two-level anisotropic wet-etched whole-thickness wafers. (c) Electrochemical- or DRIE-etched whole-thickness wafers. (d) DRIE-etched wafers after CMP thinning.

Three-dimensional (3-D) multilayered packaging offers a promising solution for building more sophisticated chips. Three-dimensional packaging provide not only benefits including low cost and small size, but also the performance and functionality not possible in two-dimensional (2-D) circuits. For instance, the visual cortex of the human brain is so powerful a computing structure that a conventional CMOS system with an equivalent ability would occupy approximately 1 m^3 of volume and dissipate a few kilowatts of power [2]. In 3-D packaging, devices on different substrates can be connected with vertical through-wafer electrical interconnects (TWEIs), which reduce the number of long global interconnects, the complexity of chip design, the interconnect-occupied area, and the *RC* delay [1]. Another advantage of TWEIs is the more efficient use of silicon by placing passive components on the backside of wafers and connecting them to the frontside with TWEIs [3]. Three-dimensional configuration is also a powerful tool to address challenges such as cost and packaging in microelectromechanical systems (MEMS) [4], [5]. Therefore, TWEIs will play an important role in 3-D packaging and integration.

Several methods based on silicon micromachining have been developed to fabricate TWEIs (see Fig. 1). Basically, three processes are involved in the fabrication process, i.e., etching through-wafer vias (TWVs), depositing insulation layers onto the wall of TWVs, and filling or depositing the holes with electrical conductive materials. The most commonly used method, developed in the early years of TWEI fabrication, employs

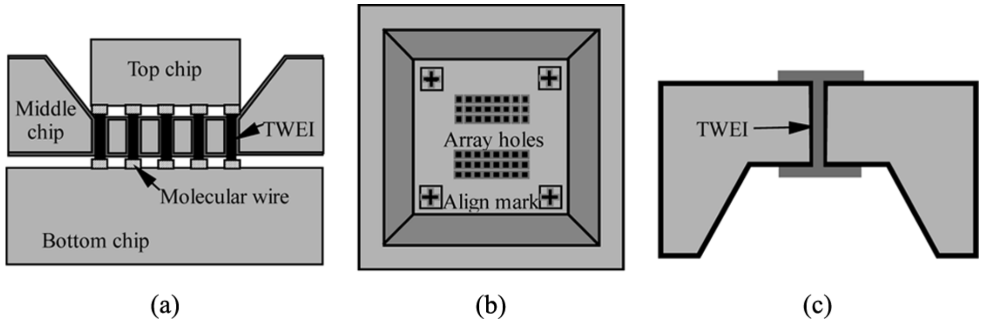


Fig. 2. Schematic illustrations of TWEI for 3-D multichip packaging. (a) Schematic illustration of the 3-D packaging structure. (b) Top view of the middle chip with TWEIs. (c) Schematic of the cross section of the high aspect ratio TWEI.

KOH to etch TWVs and metal deposition to realize conductive interconnects [6]–[10]. This method can be applied to thick silicon wafers, but KOH etching results in slant cavities and large footprints that make it impossible to achieve high-density configurations. In addition, the capacitance between the ground and the metal on the cavity sidewalls prevents it from being used in high-frequency applications. Deep-reactive ion etching (DRIE) is another option for TWV fabrication [5], [11]–[20]. DRIE is capable of etching vertical high-aspect ratio holes; however, the maximum available aspect ratio of DRIE limits the diameter of TWVs etched on whole-thickness standard 4-in wafers larger than 20 μm. Chemical mechanical polishing (CMP) facilitates DRIE etching of small TWVs by thinning wafers [14]–[16], and TWVs with diameters as small as 10 μm have been obtained by DRIE etching silicon wafers from both sides. Wafer thinning, however, decreases the mechanical strength of wafers and causes the problem of poor manipulability during manufacturing. Although photo-assisted electrochemical etching [21]–[24] has been proposed to etch high aspect ratio TWVs (>100), it can be applied only to n-type wafers, and there are great difficulties in depositing barrier layers onto the sidewalls of such deep holes and filling the holes with conductive materials.

For electrically connecting the TWVs, gold [6], [7] and aluminum [3], [8] thin films have been deposited and patterned into the KOH-etched holes. Currently, copper electrochemical deposition techniques are utilized increasingly in fabrication of interconnects [25] because of the compatibility of copper with conventional multilayer interconnection in large-scale integration, the high conductivity, and the low cost of physical or chemical vapor depositions. Electrochemical deposition of copper into holes and trenches lined with copper seed layer and diffusion barrier has demonstrated good via-filling capability and low resistivity (less than 2×10^{-3} Ωcm) [5], [11]–[16]. Heavily doped poly-silicon [17]–[20] has also been used to fill TWVs due to its IC compatibility, though its electrical features are not as good as metals.

As the feature size of IC shrinks, it is desirable to achieve small TWVs ($<$ 10 μm) to implement high-density TWEIs but without deteriorating wafer manipulability remarkably. This paper presents such a fabrication method, based on DRIE and tetra methyl ammonium hydroxide (TMAH) etching, to realize high-density and high-aspect ratio TWEIs on whole-thickness 4-in wafers for 3-D multichip packaging.

II. Packaging and Fabrication Scheme

A 3-D multichip packaging system, based on three levels of chips stacked one on another as shown in Fig. 2(a), was developed to realize complex structures with high-density 3-D connects such as artificial visual cortex [2], [27]. The top chip and the bottom chip were connected to the middle chip by self-assembled molecular wires, and the devices on the front- and backsides of the middle chip were through-wafer connected by high density TWEIs, see Fig. 2(b). Therefore, TWEIs on the middle chip with bumps on both the front- and the backsides were needed to implement the 3-D packaging.

In order to develop a process applicable to thick wafers, both TMAH etching and DRIE were employed to etch TWVs. Silicon wafers were locally etched from the backside using TMAH until the desired membrane thickness was reached, and then DRIE etching was performed on the membrane to etch TWVs. The TWVs were then filled with copper to form electrical conductive plugs and bumps by the newly developed bottom-up electroplating technique, as shown in Fig. 2(c).

The process benefited from the combination of TMAH etching and DRIE. TMAH etching maintained large parts of the wafers at their original thickness, which ensured their relatively strong mechanical strength and manipulability, while DRIE made it possible to realize high density and high-aspect ratio holes with minimal wafer area consumption. The TMAH-etched cavities on the backside of the wafers were preferred because they prevented the devices on the backside, e.g., bumps or passive inductors, from being damaged by transportation or manipulation during fabrication.

III. Fabrication Process

Fabrication started from standard one-side polished 4-in $\langle 100 \rangle$ p-type silicon wafers with resistivity of 2–5 Ωcm and nominal thickness of 525 μm. Fig. 3 is a schematic flow chart of the fabrication process, which involves etching TWVs and filling the TWVs with copper. TWVs with different configurations and dimensions, such as square and circular holes with diameters from 5 to 50 μm, were designed to demonstrate the feasibility of the process and to characterize the electrical features of TWEIs.

A. Etch of TWVs

The reference alignment marks for all the following processes, including backside to frontside alignment, were first

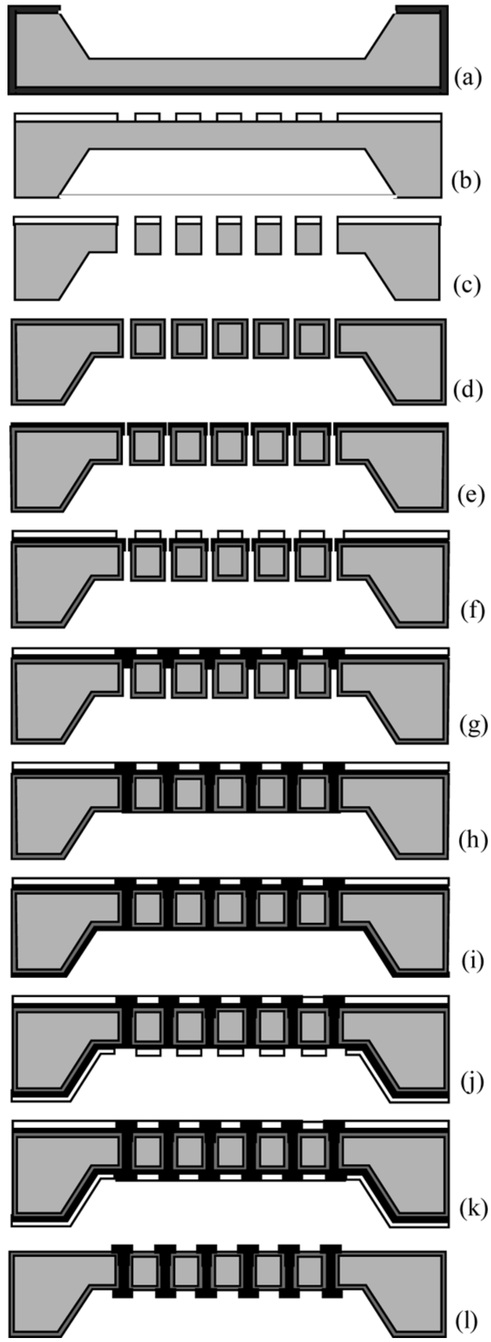


Fig. 3. Fabrication process for TWEIs. (a) Deposition of silicon nitride by LPCVD as the protection layer, patterning and RIE etching the silicon nitride, and TMAH etching of silicon to locally thin the wafer. (b) Deposition of silicon oxide on the frontside by PECVD as the protection layer for DRIE, patterning and etching the silicon oxide. (c) Time-multiplexed DRIE etching of high-aspect ratio through-membrane holes. (d) Conformal deposition of silicon nitride film as the barrier layer. (e) Deposition of adhesion layer and copper seed layer on the frontside. (f) Electroplating and patterning thick photoresist. (g) Frontside copper electroplating to seal the holes. (h) Bottom-up copper electroplating to fill the through-wafer holes. (i) Deposition of adhesion layer and copper seed layer on the backside. (j) Electroplating and patterning photoresist on the backside. (k) Copper electroplating on the backside to pattern the metal structures. (l) Removal of the photoresist, the copper seed layer, and the adhesion layer.

patterned on the frontside of the wafer and etched by RIE with depth of 1 μm. The silicon wafers were locally etched by TMAH anisotropic wet etching from the backside until the desired membrane thickness was reached. In the experiments, 50–150 μm thick silicon membranes were used. For the purpose of IC compatibility, TMAH was preferred to KOH because TMAH hardly etches metals used in IC metallization. The etching rate of 22% TMAH at 80°C is about 40 μm/h, so the etching time was from about 9.5 h for a 150-μm membrane and 12 h for a 50-μm membrane. Low-pressure chemical vapor deposition (LPCVD) silicon nitride was used as the protection layer in TMAH etching. Because the time for TMAH etching was very long, a special chuck was used to protect the frontside metal from being attacked by TMAH.

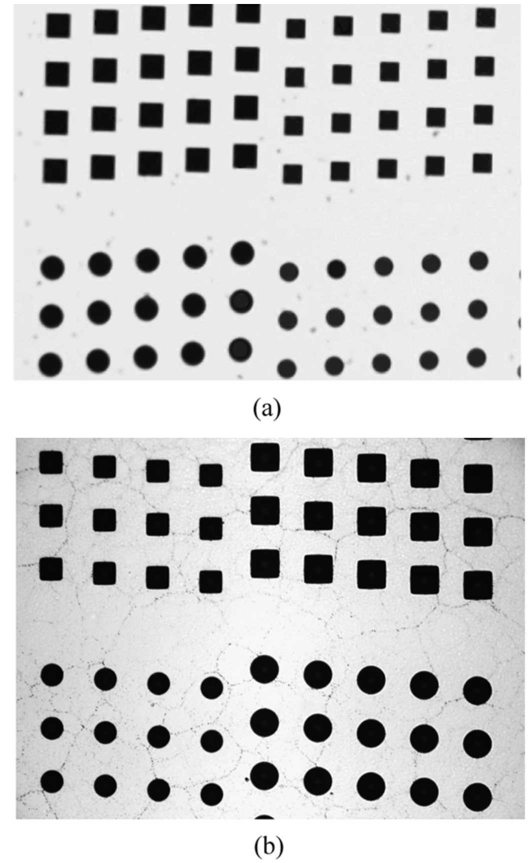


Fig. 4. Optical photographs of TWVs. (a) Frontside. (b) Backside.

DRIE was employed to etch high-aspect ratio circular and square holes through the membrane, with diameters of 5–50 μm. Due to the limited aspect-ratio of DRIE-etched holes, membranes thicker than 200 μm should be etched from both the frontside and the backside, so that the aspect-ratio can be reduced to half of that etched from only one side. This makes the DRIE easier for small holes, and can save fabrication time. Due to the "RIE lag," i.e., high-aspect ratio holes are etched much more slowly than lower ones, TWVs should have the same dimension on the same wafer to facilitate the etching process. Fortunately, since there was no silicon nitride or silicon dioxide below the holes and the DRIE aimed at etching through, the etching can be performed long enough to etch all holes through, without the "notching effect." Fig. 4 shows the optical photos of circular and square TWVs.

B. Copper Electroplating for Sealing TWVs

Silicon nitride thin films with thickness of 300 nm, deposited by PECVD on both sides of the substrate and inside of the TWVs, were used as the barrier layers to insulate the silicon substrate from the conductive material that filled in the TWVs. Then a 20-nm Ta/TiN was sputtered on the substrate as the adhesion layer; this strengthened the adhesion of copper to the barrier layer. A 300-nm-thick Cu seed layer was subsequently sputtered on the frontside of the substrate. This process has the convenient characteristic that the copper can also be sputtered into the inner wall of the TWVs at the vicinity of the opening due to the limited aspect-ratio of sputtering, see Fig. 3(e). This was the key factor that determined the result of next step- sealing the holes with copper electroplating. A thick layer of negative photoresist (ED 2100) was then electroplated on the frontside of the substrates [26], followed by patterning.

Then, copper was deposited on the frontside of the substrate using a pulse-reverse copper electroplating machine (MECO, Drunen, Holland). The copper plating bath contained copper sulfate ($CuSO_4 \cdot 5H_2O$) and sulfuric acid (H_2SO_4), as well as several organic additives including polyethylene glycol (PEG) and hydrochloric acid (HCl). Typical cupric ion concentrations in commercial use range from 10–100 g/L. High copper concentrations are useful when a rapid deposition is required, such as in this experiment to achieve the desired thickness. Lower copper concentrations can provide a uniformly increased charge transfer resistance at all points on the wafer surface, and can improve the Cu quality, such as the uniformity of its profile. The copper sulfate concentration must be adequate to avoid depletion of the cupric ion inside the high-aspect ratio holes and to get high deposition rates. In this experiment, the concentration of the plating bath and the current density were, respectively, 100 g/L and 30 mA/cm^2.

As a result of the sputtered copper seed layer inside TWVs, the electroplated copper grew not only on the frontside of the substrate, but also on the inner wall of the TWVs, along the radial direction. Because the electric field around the opening of TWVs was strengthened due to the sharp shape, Cu deposition around the openings was faster than that on other flat areas, as shown in Fig. 5. Therefore, the electroplated copper approached the center of the TWVs at the openings. This led to a partial block of the openings of the TWVs, which was very desirable for the next step, the bottom-up electroplating. After a period of electroplating, the holes were completely blocked on the frontside.

Fig. 6(a) is an optical photo of the TWVs after 2 h of Cu electroplating. It is evident that about half of each opening was covered by Cu. It can also be seen that the fraction of uncovered area of the small holes was smaller than that of the larger holes, indicating that smaller holes can be sealed faster than larger ones. Fig. 6(b) shows that, after 4 h of Cu electroplating, the openings of all holes were completely sealed by Cu. It was found from the experiments that square holes, in which the electroplated copper grew from the four edges and formed crescent-like shapes, were sealed faster than circular holes, in which copper grew uniformly toward the centers. However, the electroplating in square holes induced higher protrusions from the wafer plane, which could cause difficulties in subsequent processes, such as in contact-mode lithography.

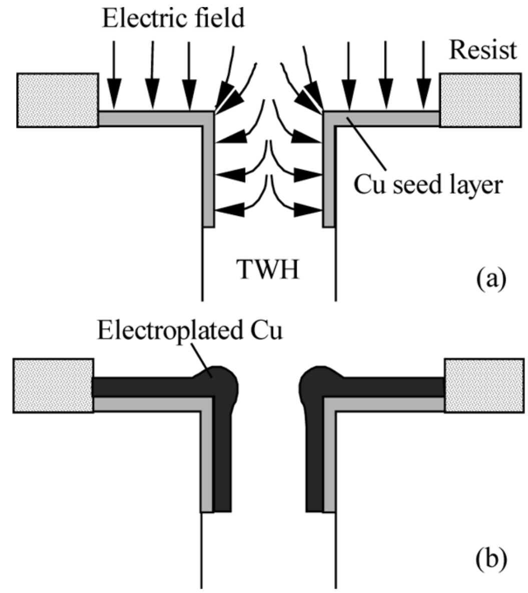
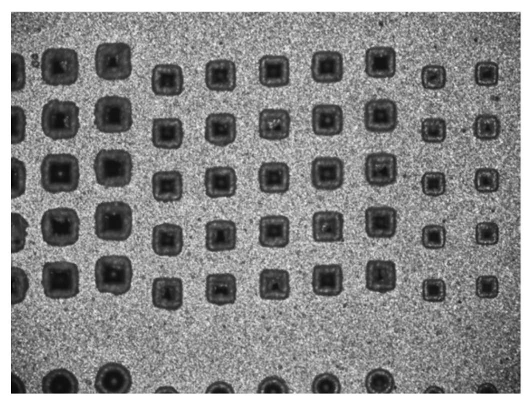
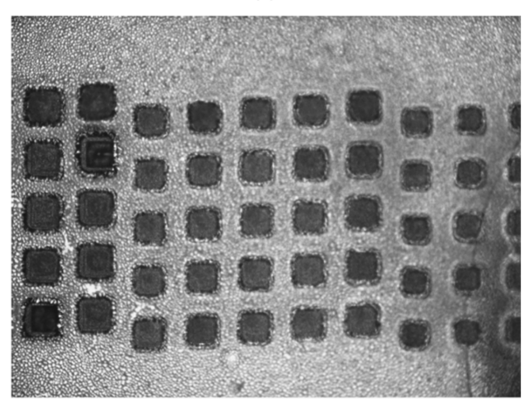


Fig. 5. Schematic illustration of the principle of sealing the TWH with Cu electroplating. (a) Distribution of the electric field. (b) Formation of the electroplated Cu.



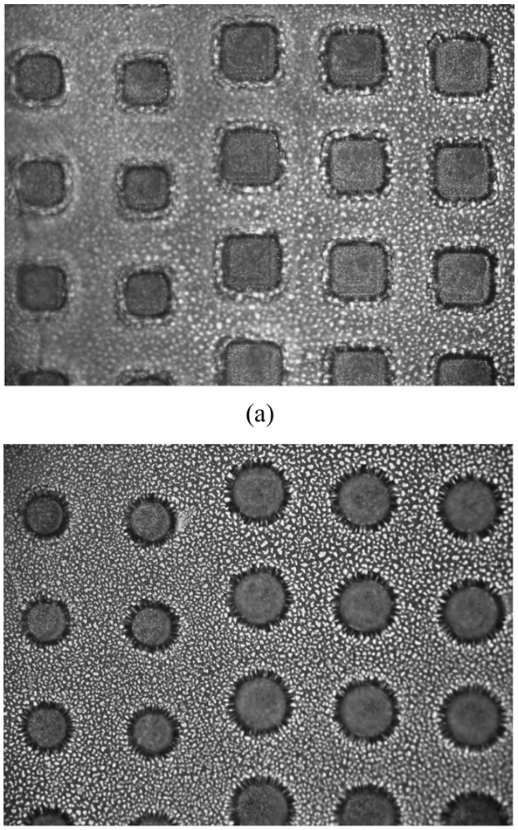
(a)



(b)

Fig. 6. Copper electroplating for frontside TWH sealing. (a) After 2-h copper electroplating, holes are partially sealed. (b) After 4-h copper electroplating, holes are completely sealed.

The sealing rate can be improved by increasing the copper concentration in the plating bath and the current density, as more



(a)

(b)

Fig. 7. Optical photographs of TWEIs at backside were completely filled with copper after bottom-up electroplating. (a) Square. (b) Circular.

reaction species are available and can be easily supplied. In this experiment, since the copper seed layer and, thus, the copper electroplating happened not far from the top of the TWVs, the copper concentration did not evidently influence the outside to inside ratio of the deposition rate.

The electroplating rate also increased with current density, even at lower copper concentrations. This resulted in rapid sealing of the holes for normal conformal electroplating. Hence, the current density for sealing the holes should be increased within a proper range, but compromise had to be made between the deposition rate and the electrical characteristics of electroplated Cu as fast deposition yields large grain size [25]. Therefore, although pulse-reversed electroplating reduced the copper growth rate along the horizontal directions, it was still preferred due to the excellent quality that it produced.

C. Bottom-Up Copper Electroplating

After frontside copper electroplating, the openings of the TWVs were blocked completely. Then the wafers were flipped over and bottom-up Cu electroplating was performed to fill the TWVs. The Cu films covering the front side openings were used as the seed layer for bottom-up copper electroplating. Since there was no Cu seed layer on the inner wall of the TWVs, the Cu deposited by bottom-up electroplating grew from the Cu film only along the height of TWVs. As a result, the TWVs were completely filled with no voids or seams. When the Cu plugs reached the bottom of the TMAH-etched cavities, electroplating was stopped.

The concentration of the cupric ion and the current density in the bottom-up electroplating were, 100 g/L and 20 mA/cm^2, respectively. In this instance, it took about 150 min to fill TWVs of 90 μm deep. TWVs with diameters of 5–50 μm were completely filled with copper, without forming any voids and seams, as shown in Fig. 7. These results demonstrate that bottom-up electroplating is the most appropriate method for filling high aspect-ratio (or deep) holes.

Due to the high aspect-ratio of the TWVs, the mass transfer inside the blind holes was slow during the bottom-up copper electroplating, resulting in higher deposition rate for holes with small aspect-ratio. Consequently, smaller holes were filled more slowly than larger ones, a phenomenon known as "electroplating lag." This can cause undesirable, uneven deposition. While electroplating lag could not be eliminated, it can be reduced by continuous and uniform stirring of the bath. This is very crucial to bottom-up electroplating to get uniform deposition rate.

A second important consideration during bottom-up electroplating is to maintain adequate concentration of copper sulfate to avoid depletion of cupric ions within deep holes at high deposition rate (large current density). This was achieved by using lower current density in bottom-up electroplating than that used in sealing TWVs. Continuous and uniform stirring was also helpful.

D. Backside Patterning

In order to fabricate bumps and passive devices at the bottom of the TMAH-etched cavities, one additional mask and several steps were required after bottom-up electroplating.

A layer of 20-nm-thick Ta/TiN and a 300-nm-thick copper film were sputtered sequentially on the backside as the adhesion layer and the seed layer, respectively. Immediately after the seed layer, a photoresist (ED 2100) layer with thickness of 10 μm was electroplated onto the backside, followed by pattern transfer of bumps or passive components onto the bottom of the cavities. A double-side contact aligner (EV-420) was used because the patterns on the backside should be aligned to those on the frontside. As during both the TMAH etching and DRIE, the reference alignment marks on the frontside of the silicon substrate were covered by LPCVD silicon nitride or silicon oxide, they were well protected for double-side alignment. The alignment marks aligned from the backside to the reference on the frontside should be mirrored when fabricating masks. After development, photoresist molds were formed and then Cu electroplating was performed on the backside. Once the desired thickness of the Cu layer was obtained, electroplating was stopped, and the photoresist as well as the Cu seed layer and the Ti/TiN adhesion layer were removed by using, respectively, oxygen plasma and etchant.

Because the photoresist layer to be exposed was on the bottom of the TMAH-etched cavities, a deep gap, from 375 to 475 μm, existed between the mask and the photoresist layer. This gap caused serious problems in the process.

The first problem was how to coat the bottom of the cavities with a uniform photoresist layer. The uniformity of the photoresist layers is crucial to the lithography process to get better resolution, which determined the density of TWEIs.

However, using conventional spin-coating method, photoresist accumulates at the bottom edges of the deep cavities, resulting in a nonuniform photoresist layer. This presents great difficulty in archiving good resolution in lithography. In addition, nonuniform photoresist layers can create the so called "ghost image" when the incident light beam to the smooth slant sidewalls of the cavities is reflected to the bottom or the opposite sidewalls, resulting in unexpected exposure. To solve this problem, photoresist electroplating was used instead of conventional spin-coating to obtain uniform 10-μm photoresist layer [26]. Preliminary experiments showed that the nonuniformity in 10-μm photoresist was less than 10%, much better than that of spin-coating.

Because of the deep cavities and the exceptionally thick photoresist layer, higher exposure energy was needed to expose the photoresist on the bottom of the cavities. In the experiments, exposure energies from 350 to 375 mJ/cm^2 were used. To some extent, the exposure time and the energy were tailored according to the specificity of the patterns, e.g., long and narrow lines required a little longer exposure time and higher energy.

Another consideration was loss of resolution. Resolution deteriorates when diffraction occurs at feature edges on the mask in the proximity mode. Due to the deep gap between the mask and the photoresist layer, the dimensions of patterned structures can differ from the original values at the layout. Preliminary experiments showed that the deep gap deformed the shape of small patterned structures, e.g., rounding of the corners. This loss of resolution has to be taken into account when designing structures in deep cavities. Once the photoresist coating process is optimized for uniformity and reproducibility, tailoring of the dimensions of the patterns during mask design can partially compensate for loss of resolution [6].

In spite of current limitations, the process developed was capable of realizing bumps for 5-μm holes and passive components on the bottom of the cavities, such as backside integrated spiral inductors. The patterning results indicated that for the cavities 400 to 475 μm deep, photoresist layers with thickness of 10 to 16 μm were well patterned for the desired structures, and features as small as 8 μm was implemented.

IV. Results and Discussion

Based on these developed processes, high-aspect ratio TWEIs with diameters of 5–50 μm and space distances of 50 μm have been realized. Fig. 8 shows the scanning electron microscope (SEM) photograph of an independent copper-filled TWEI. It can be seen that the TWV is completely filled by bottom-up electroplated copper without voids or seams. This demonstrates the capability of bottom-up electroplating in filling high-aspect ratio holes. The scallops along the hole induced by DRIE cannot be recognized, but it is evident that DRIE made a varying diameter. Measurements on resistance structures were carried out and the resistance of TWEI was extracted. The average resistivity of the electroplated Cu inside TWEIs was 2.5×10^{-5} Ωcm. Compared with the resistivity of doped polysilicon (greater than 1×10^{-2} Ωcm [18]), these Cu-filled TWEIs had an extremely low resistivity. This is very attractive for applications that require high-density interconnects and low resistivity.

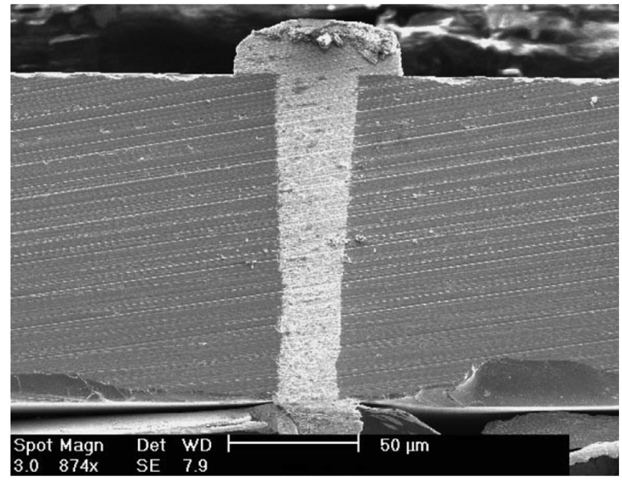


Fig. 8. SEM photograph of the cross section of a TWEI.

Fig. 9(a) shows a TWEI array. This array has been applied to the packaging of a three-chip stacked artificial visual cortex [2], [27]. As the achievable structure from the backside patterning was 8 μm, it can be expected that, from the fabrication point of view, TWVs can be placed even closer together, and, therefore, higher density is possible. However, the mechanical strength is a critical issue in wafers with through-wafer holes. Because the full wafer thickness is maintained for a considerable fraction of the wafer by using local TMAH etching, the mechanical strength of such a micromachined wafer is similar to that of a solid wafer [3]. The presence of via-holes has only a limited impact on the wafer stiffness, but can lead to significant stress when vias are placed closely together [28]. Therefore, the density of TWHs is limited by not only the fabrication capability but also the mechanical stress. Experiments show that the interval distance can be as small as 20 μm without the problems of mechanical stability or manufacturability, and the wafers used in this experiments did not fail due to mechanical problems.

Another application of TWEIs is the integration of backside spiral inductors, which is shown in Fig. 9(b). The inductors had two turns, and the outer dimensions were 226 by 226 μm. The inductor was integrated at the bottom of a 445-μm-deep cavity and contacts were brought to the frontside via two TWEIs. Two types of integrated passive inductors, with and without back ground plane, were fabricated on the bottom of the cavities on the backside to demonstrate the feasibility of the integration of passive components on the backside. Compared with planar spiral inductors in conventional silicon processes, which occupy a typical area of about 200 by 200 μm and are placed side by side with active devices, backside integration is quite attractive as it can substantially save chip area.

Due to "electroplating lag," smaller holes were filled much more slowly than larger ones. So, when 5-μm holes were completely filled, Cu caps like "mushroom" appeared at the openings of lager holes, as shown in Fig. 9(c). During the Cu electroplating for sealing the holes, smaller holes were blocked much faster than larger ones, whereas in bottom-up electroplating for filling the holes, the larger ones were filled much faster than smaller ones. Although these inconsistencies in electroplating rate could be reduced to some extent, they

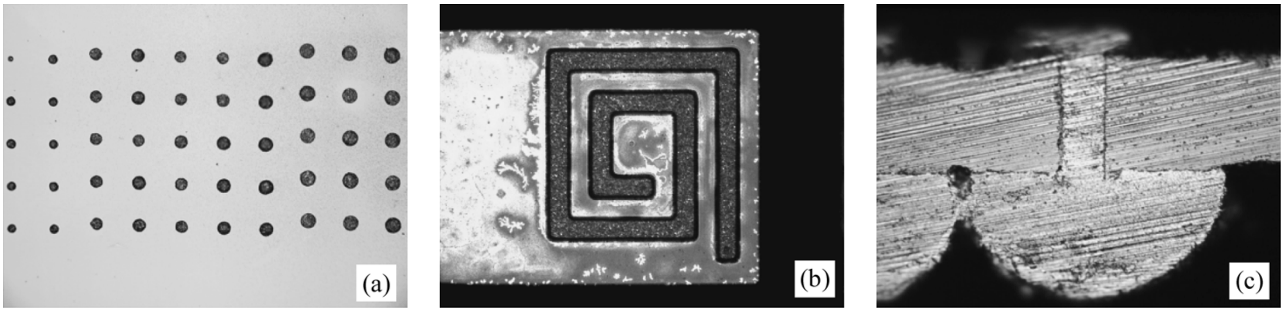


Fig. 9. Through-wafer electrical interconnects. (a) Contact pads. The diameter is 5 μm for the smallest holes and 15 μm for the largest ones. (b) Passive inductor on the bottom of the TMAH-etched cavity. The inductor is connected to the frontside with TWEI. (c) Cross section of TWEI. The diameter is 30 μm and the thickness of the membrane is 80 μm. Because of the "electroplating lag", when the smallest holes (5 μm) was completely filled, a "mushroom" appeared at the contact pads of larger holes.

suggest that the TWVs of the same dimension would facilitate the electroplating process.

Although TMAH etching was successful, the use of the special chuck for frontside protection was quite complicated, and the long etching time limited throughput. In addition, due to the temperature limitation of metal in post-CMOS processes, protection films of silicon nitride or silicon dioxide can only be deposited by PECVD, which is possible for thin-film deposition under 400 °C. However, pinholes in PECVD-deposited silicon nitride films can result in serious wafer damage in long TMAH etching process. In this experiment, two-step deposition was adopted to solve this problem, and satisfactory results were obtained.

V. Conclusion

High-density and high-aspect ratio TWEIs have been fabricated on whole-thickness wafers and applied to 3-D multichip packaging and backside inductor integration. This demonstrates the feasibility of the silicon micromachining process to fabricate high-density and high-aspect ratio TWVs and the capability of the newly developed bottom-up copper electroplating to fill them. The success of this technique attributes to the combination of TMAH wet etching and DRIE, as well as the bottom-up electroplating. TMAH etching thins the wafer without significantly decreasing its mechanical strength and manipulability by locally etching the wafer. DRIE realizes high-aspect ratio and high-density TWVs with small diameters on the membranes. Bottom-up copper electroplating fills the high-aspect ratio TWVs without forming voids and seams. TWVs with diameters as small as 5 μm have been fabricated and completely filled with copper. Compared with doped polysilicon or patterned aluminum, the resistance of copper is much smaller. Thus, this silicon micromachining process along with bottom-up electroplating is a promising tool to fabricate TWEIs and realized 3-D packaging.

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