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M.Sc. Thesis

A Low-Noise Transimpedance Amplifier for Ultrasound Imaging with 40dB Continuous-Time Gain Compensation

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The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled **"A Low-Noise Transimpedance Amplifier for Ultrasound Imaging with 40dB Continuous-Time Gain Compensation"** by **Qian Wang M.Sc.** in partial fulfillment of the requirements for the degree of **Master of Science**.

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Abstract

This work presents a low-noise amplifier (LNA) for miniature 3D ultrasound probes. Time gain compensation (TGC) is required to provide continuously variable gain and compensate for the attenuated echo signal, resulting in decreased output dynamic range (DR). As TGC is embedded in the LNA, a power-hungry LNA is no longer needed to handle the full dynamic range of attenuated echo signals. Compared to the prior art where TGC is applied after the LNA, this structure reduces die area and power consumption greatly.

The LNA with built-in TGC functionality is comprised of a transimpedance amplifier (TIA) with an exponentially increasing feedback resistive network. Since a transducer with a relatively high impedance is targeted, a TIA is utilized to interface with the transducer and sense the signal current. TGC is implemented in a continuous fashion by tunable resistors so as to alleviate imaging artifacts associated with gain-switching moments. The resistive feedback network is achieved by triode transistors with exponentially decreasing gate voltages. Three parallel branches of triode transistors are varied simultaneously to obtain a 40dB gain range. Each branch consists of two back-to-back triodes to mitigate non-linearity related to the body effect.

The variable-gain loop amplifier employing a current-reuse topology enables constant closed-loop bandwidth in an energy-efficient way. The first stage is a fixed-gain stage with dynamic biasing to save power at the lowest gain setting. The next two stages are variable-gain stages with variable resistive loads. The load resistor is implemented in the same fashion as the TIA's feedback resistor to achieve intrinsic gain matching. The last stage is a buffer to provide low output impedance for stability.

The LNA has been designed in 0.18 μm CMOS technology and occupies an estimated die area of 0.0339 mm^2. The effective gain range is 40 dB with ± 1 dB gain error. The LNA's noise floor at the highest gain is below 1.15 $pA/\sqrt{Hz}$ and its harmonic distortion is better than -40 dB. During 100 μs receive period, the total power consumption is 6 mW from a ± 0.9 V supply. The LNA featuring a small area and high power efficiency is a promising circuit for miniature 3D ultrasound probes.

Acknowledgements

The last two years in the Netherlands have been an important phase in my life. At TU Delft I gained knowledge as well as a love for life. I learned to seize the moment and enjoy happiness instead of being anxious about the unknown future. I learned to make trade-offs and make the most of my resources. Most importantly, this experience led to a greater interest in designing analog circuits.

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Contents

1 Introduction

The past decade has seen the rapid development of ultrasound imaging devices in medical imaging, such as intracardiac echocardiography (ICE), intravascular ultrasound (IVUS), and transesophageal echocardiography (TEE) probes. A growing trend in real-time 3D imaging has led to a proliferation of the application of 2D matrix transducer arrays, which overcome the limitation of traditional 1D transducer arrays. Application-specific integrated circuits (ASICs) play a crucial role in the development of ultrasound devices. By close integration with the transducer arrays, the ASIC locally amplifies the received echo signals and further converts them into digitized signals to be processed by imaging systems.

As the first key blocks in the receive chain of such ASICs, the analog front end (AFE) obtains echo signals from the transducer and locally amplifies the signal before applying a time-varying gain to compensate for the signal attenuation in the medium. Each AFE channel typically contains a low-noise amplifier (LNA) and a time-gain compensation (TGC) amplifier. Since there could be hundreds of channels in an in-probe ASIC, an optimized AFE is necessary aiming at an efficient and cost-effective design.

This work presents the design of power- and area-efficient LNA with built-in TGC functionality. By combining LNA and TGC in a single structure, area and power efficiency are optimized.

1.1 Background

According to recent data from the World Health Organization (WHO), one of the most common causes of death among the elderly is cardiovascular disease, which takes up to 23.5% of the total death in 2020 [1]. An important cause of cardiovascular disease is atherosclerosis, created by plaques in the arteries. Thus, a safe, accurate diagnostic system is called for in order to prevent cardiovascular disease. Ultrasound imaging has emerged as a powerful imaging technique for visualization and diagnosis of cardiovascular disease [2]. Compared with computed tomography (CT) or magnetic resonance imaging (MRI), echocardiography is impeccably safe, cost-effective, and has real-time imaging characteristics [3].

Conventional ultrasound probes are quite bulky, as each transducer element is connected to a coaxial cable before connecting to channels on an exterior imaging system. Traditional 1D transducers are utilized to reconstruct 2D cross-sectional images. How-

ever, conventional brightness-mode 2D ultrasound imaging shows certain limitations. Since 2D images are performed in a single position or single plane, multiple images from different planes are necessary for anatomy and pathology purposes [4]. This could be time-consuming and inaccurate, which increases the chance of misdiagnosis.

There's a clinical need for real-time 3D imaging, which facilitates a more accurate diagnosis of abnormal anatomies. In order to generate 3D images, 2D matrix transducer arrays are utilized. In order to avoid grating lobes, the element pitch should be kept quite small while the aperture should be large for high resolution, leading to thousands of transducer elements [5]. However, the one-to-one correspondence between transducer, cable and channel limits the transceiver channel to atmost 256 [6]. This problem constrains the prevalence of 2D transducer arrays.

To bridge the gap between a large number of transducer elements and the limited number of channels, ASICs are integrated in the probes to interface between the transducer and the imaging system. By means of multiplexing [7] or sub-array beamforming [8], channel count reduction could be realized by employing ASIC. The ASIC performs local amplification on echo signals to improve SNR and implements impedance matching especially when connecting small, high-impedance transducer elements to long cables [4][6]. Besides, the ASIC also enables full digitization of echo signals. As the AFE and ADC are embedded within the ASIC, the data acquisition moves from the external imaging system into the ASIC, which motivates the portability of the imaging system. This is a primitive step for 3D miniaturized probes since the traditional imaging system with AFE and ADC is replaced by smart devices [6]. Additionally, the improvement on ASICs boosts the miniaturized 3D probes because the per-element circuitry is small enough to be mounted directly in the probe tip, even in a pitch-matched fashion [8, 9].

1.2 Ultrasound Imaging System

As Fig.1.1 shows, a major building block of an ultrasound system are the transceiver circuits, which dominate the signal performance and thus the power consumption. Therefore, transceiver circuits should be carefully designed.

The transceiver circuits consist of a signal transmit path and a receive path. For signal transmission, the high voltage (HV) pulses are timed by a TX beamformer, which generates a spatial distribution of acoustic waves to be converged at a focal point. HV pulser is an essential block for triggering TX transducer elements. HV pulses are indispensable when an attenuated echo signal needs to be detected. Since propagation delay is proportional to depth, the signal attenuation is quite strong for an echo signal from a deepest point [5]. Thus, large enough pressure needs to be generated by the TX transducer elements in order to provide detectable amplitude even from a deepest point. Therefore, the amplitude of these pulses can reach more than 100V [6]. These pulses are connected to the transducer via a T/R switch, which protects the signal receive path from high voltage pulses.

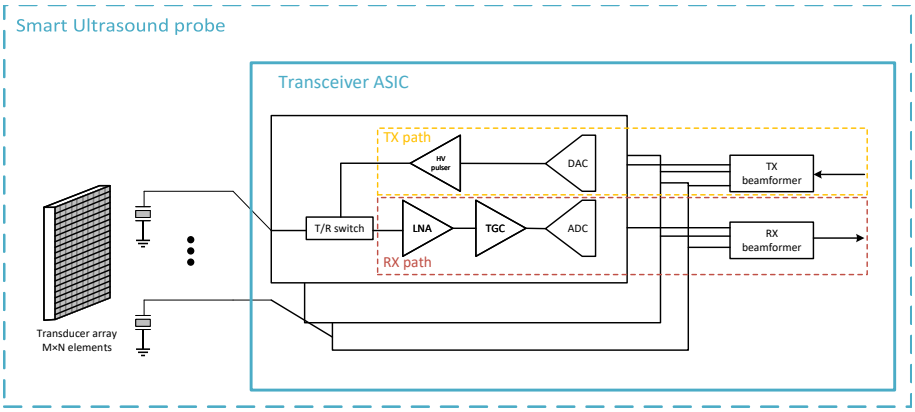


Figure 1.1: Block diagram of the transceiver ASIC in smart ultrasound probe

During the receive phase, an echo signal is captured by a transducer element and amplified by an LNA. As propagation delay increases with time and depth, the signals that arrive last encounter more attenuation than signals that arrive first. To compensate for the signal loss, a TGC amplifier is introduced, providing a linear-in-dB gain that increases with time. It also benefits the overall dynamic range. Then the echo signals are digitized by an ADC and fed into an RX beamformer, which adds the signals in a delay-and-sum fashion. Lastly, RX data from the RX beamformer are further processed to reconstruct an image.

For a smart ultrasound imaging system, many design parameters could be altered for an optimized design at a given SNR. For specific transducer characteristics and a fixed beamforming scheme, the signal amplitude depends on the amplitude of the HV pulses while the noise floor is limited by the noise of the transducer element [6]. Often there's a trade-off between RX power consumption and TX power consumption [6]. In the case of an ideal noise-free receive circuit, the minimum amplitude of the HV pulses is determined by the SNR performance. But in reality, SNR is degraded by the noise figure (NF) of the receive circuits. There are two ways of improving SNR. The first way is to increase the amplitude of the TX pulses to improve signal amplitude. The other method is to improve the NF by suppressing noise from the RX circuits at the expense of RX power consumption. Since the TX pulses only turn on for a short period, TX power consumption is not our top concern.

This work focuses on the design of the RX path, aiming at low-area and low-power AFE design. As seen in Fig.1.2 the AFE is optimized by replacing conventional LNA and TGC with a single LNA architecture with built-in TGC function.

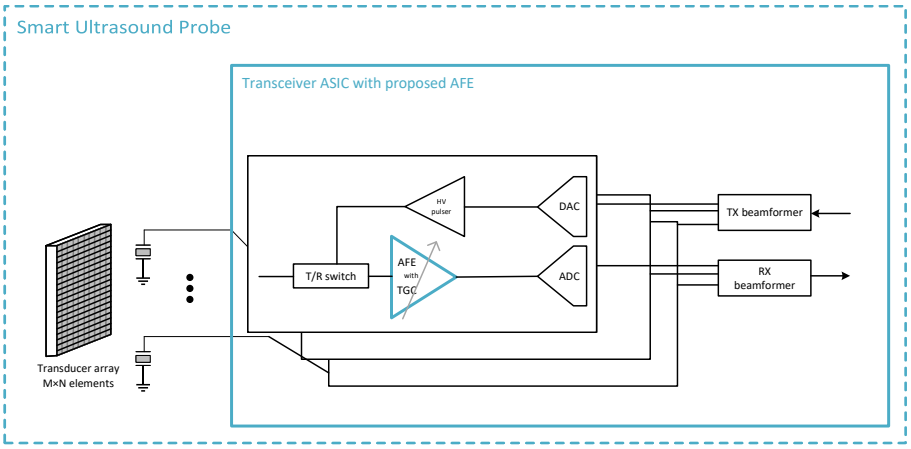


Figure 1.2: Block diagram of a transceiver ASIC with the proposed AFE

1.3 Time-Gain Compensation

The ultrasound waves suffer from signal attenuation when traveling within an attenuating medium like the human body. Then the attenuated echo signals are scattered back and received by the transducer elements after a certain time span, and the traveling time is proportional to the travel distance. Therefore, the echo signals scattered from deep tissue arrive later than those coming from nearby organs and experience more attenuation. The signal attenuation in the medium can be determined using equation (1.1) [10], where α is the attenuation coefficient, ℓ is the traveling length and f is the frequency of the ultrasound waves.

$$\text{Attenuation} = \alpha \left[\frac{\text{dB}}{\text{MHz} \cdot \text{cm}} \right] \cdot \ell[\text{cm}] \cdot \text{f}[\text{MHz}] \tag{1.1}$$

Equation (1.1) demonstrates that the signal attenuation is linearly proportional to the travel distance and the ultrasound frequency. At higher frequencies, the ultrasound waves provide better resolution but face less penetration and greater attenuation. This situation emphasizes the importance of the TGC amplifier.

To mitigate the attenuation and maintain a constant amplitude envelope, the TGC amplifier provides an exponentially-increasing gain over time. Thus, the TGC amplifier reduces the dynamic range that needs to be processed by the remainder of the signal path and benefits power consumption.

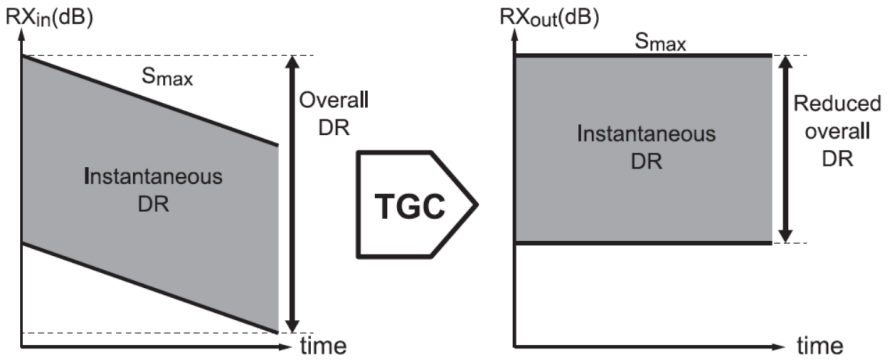


Figure 1.3: (a) Dynamic range over time (b) Dynamic range after ideal time-gain compensation[11]

1.4 Motivation

In conventional ultrasound imaging systems, the receive path comprises a separate LNA and TGC, which is not preferred for several reasons. Firstly, power-hungry LNAs are essential for handling the overall DR of the attenuated signal while satisfying noise performance. Such fixed-gain LNAs require additional power for the output stage to achieve linearity at large inputs or demand extra power to suppress the noise of the next stage when the LNA's gain is limited. Besides, the separation of LNA and TGC implies an extra cost of power and die area.

The inefficiency in terms of area and power calls for a better AFE design. Fig.1.2 shows the proposed architecture with combined LNA and TGC. In this architecture, both power consumption and die area could be saved. Since TGC is a built-in function, the LNA only handles the instantaneous DR at its output while facing the same noise requirements, which relaxes the requirements of the LNA, leading to increased power efficiency. It's also expected that the combined structure saves die area.

Previous studies[8, 11, 12, 13, 14] also explored the combined AFE structure. In [8], programmable gain amplifiers with discrete gain steps are used but limited by the artifacts related to gain-switching moments. Commercial AFE structures with continuous gain control are insensitive to gain-switching artifacts, but they are too large and power-inefficient [15]. In [11] a variable-gain LNA with continuous TGC is presented, using a capacitive feedback network and current steering network to provide continuous TGC. But the die area is considerably large due to the large capacitive network. Moreover, the linear interpolation between exponentially-spaced gain steps leads to non-negligible gain error. [13] describes a pitched-matched AFE consisting of two interpolating variable-gain stages. A novel complementary current steering network (CCSN) is used as an interpolator to achieve a pseudo-exponential trajectory, resulting in the lowest reported gain error. The hardware-sharing scheme achieves 4X smaller die area compared to[11]. But the feedback network still occupies quite some area because of capacitive arrays. And the current steering biasing network (CCSN) is shared among

multiple channels, which could lead to correlated noise.

To further reduce per-channel area, [12] proposes an LNA with a resistive feedback network to provide continuous gain control. By employing triode transistors as a resistive feedback network, the estimated die area is 6X smaller than [11]. On top of that, the exponential voltage generator is a tiny structure comprising a Mosfet-C network. This independent structure is provided for each branch of the resistive feedback network, so there is no correlated noise from different channels of LNA. A major drawback of the design presented in [12] is that the output only has limited driving capability. The stability issues remain to be solved when driving a large load capacitor. The dB-linear gain error is >2X larger than [13] and the power consumption is 6X larger than [13].

Therefore, the need for a pitch-matched AFE design with high power efficiency and small gain error is highly motivated. The aim of this work is to present such a power-efficient AFE design with the smallest area and acceptable linear-in-dB gain error.

1.5 Design Specification

The proposed LNA-TGC will be implemented in TSMC 0.18 μm MS technology with $\pm$0.9 V supply. The design specifications are listed in table 1.1. In order to deliver a promising solution for miniature 3D probes, area and power are two top concerns. In [11] the die area is 0.12 mm^2 with 5.2 mW power consumption. The goal is to design an LNA with built-in TGC functionality in a comparatively small area. Therefore the design trade-offs are mainly made considering minimized area and power.

In order to compare performances with the state-of-the-art, the same capacitive micromachined transducer (CMUT) from [11] is targeted in this work. The adopted transducer has a bandwidth of 5$\sim$10 MHz and a center frequency of 7.5 MHz. It can be viewed as a resonator modeled by a capacitor, resistor and inductor. The CMUT model further comprises a signal-current source and a shunt capacitor of 18 pF at 7.5 MHz. The noise contribution of the LNA-TGC should not exceed that of the CMUT at the highest gain as the dominant noise source is the transducer. Therefore, the input-referred noise target is set to 1 pA/$\sqrt{Hz}$ at 7.5 MHz. For the LNA-TGC design, the noise specification only targets the high end where the SNR requirement is more stringent. At the lowest gain, the echo signal is the largest and the tolerated noise level can be increased without any SNR degradation.

Furthermore, total harmonic distortion (THD) is taken into account as linearity issues are important in this design.

Table 1.1: Target Performance Specs

Input center frequency	7.5 MHz
Bandwidth	5-10 MHz
Peak input amplitude	0.5 μA-50 μA
Input referred noise density	1 pA/$\sqrt{Hz}$ at 7.5 MHz
SNR	44 dB
Gain range	40 dB
Gain error	$\pm$0.5 dB
THD	<-40 dB
Receive time period	100 μs

1.6 Thesis Structure

This thesis presents a variable-gain low-noise amplifier with continuous TGC function that mitigates the switching artifacts related to discrete gain steps. The presented amplifier architecture has a low-power design and compact size that better adapts to the requirements of miniaturized ultrasound probes. This thesis is organized as follows. Chapter 1 has summarized the research overview of the ultrasound imaging system and proposed the motivation and aim of this work, and the design specification. Chapter 2 reviews the existing LNA designs with built-in TGC functions, analyzes their strengths and weaknesses, and highlights the research gap. Chapter 3 demonstrates the proposed LNA architecture. Chapter 4 focuses on the circuit implementation of the proposed LNA architecture, while chapter 5 illustrates the performance and results of this design. At last, chapter 6 compares this work performance with the state-of-the-art and draws conclusions.

2 Prior Art

A considerable amount of studies have explored various approaches to perform amplification with TGC function. These studies can be divided into two categories based on the implementation of the gain control: Programmable gain amplifiers (PGA) with discrete gain steps and Variable gain amplifiers (VGA) with continuous gain [6]. In either approach, the amplifiers realize a dB-linear gain over time with digital code or analog control voltage. The exponentially increasing gain profile compensates for the incoming attenuated echo signal and delivers a constant output amplitude envelope. However, amplifiers with an ideally dB-linear gain do not exist in the real world. The gain profile always shows certain gain inaccuracy or limited gain range in view of area and power limitations. Assuming a fixed gain range and noise target, designing an amplifier with improved gain accuracy and reduced die area and power is our top concern.

The following sections examine various architectures to realize the TGC function. As the advantages and disadvantages of certain architectures are compared, the research gap is clarified and the architecture of this work is motivated.

2.1 Discrete TGC Implementations

Employing a PGA with discrete gain steps is a viable approach to approximate exponentially varying gain. The most attractive advantage is that the gain steps are controlled by simple digital circuits and can be accurately defined. The gain profile is set by switching on sequential gain steps and the gain range is extended by increasing the number of gain steps. However, amplifiers with discrete gain steps suffer from artifacts associated with gain-switching moments. When switching between two adjacent steps, the switching transient can cause artifacts in the ultrasound images [11]. As the switching is proportional to image depth, using larger gain steps can lead to noticeable artifacts at an image depth corresponding to the switching transient. Such adverse effects could be alleviated by smaller gain steps, but this means more gain steps are required for a fixed gain range, which results in increased complexity circuitry with substantial die area.

PGAs also suffer from image artifacts associated with improper TGC. In B-mode imaging, the image brightness shows variation due to the mismatching of the gain compensation and the attenuation. Since PGAs with discrete gain steps often have 3X larger gain error compared to their counterparts with continuous TGC [11], the image artifacts

pose a challenge for achieving dB-linear gain with PGA.

There are various architectures to attain discrete gain steps. They are globally divided into three categories: resistive feedback network, capacitive feedback network and current steering network.

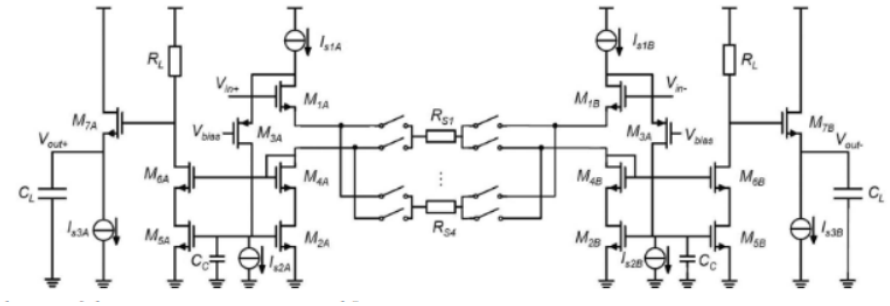


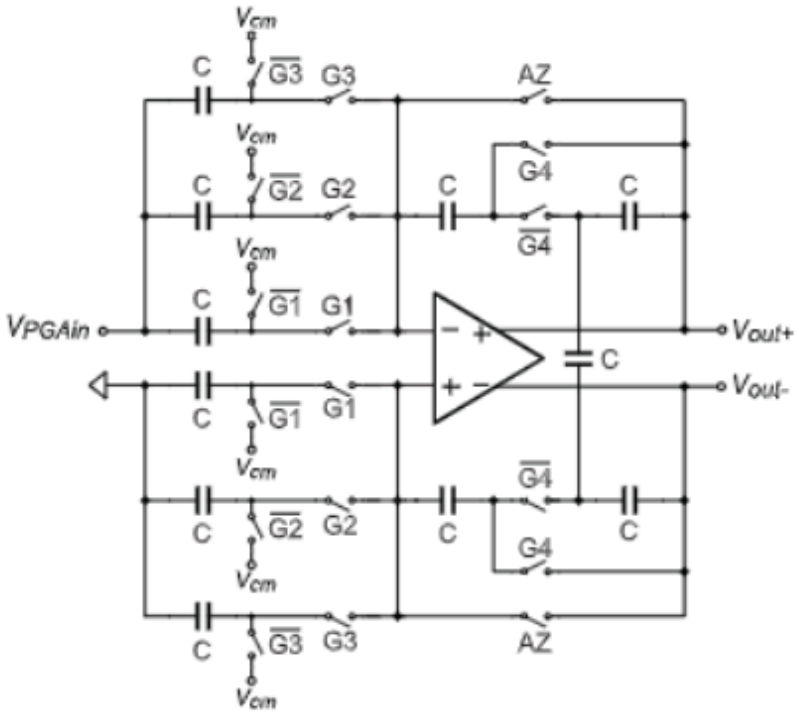
Figure 2.1: Open-loop PGA with programmable resistive network [16]

Programmable resistive feedback networks often utilize impedance ratios as gains to minimize PVT effects. Both open-loop [16][8]and closed-loop topologies [18] [19]can be found in existing studies. Fig.2.1 shows an open-loop PGA which aims to obtain high BW while maintaining low power consumption. It consists of a differential pair of common source amplifiers with tunable source-degeneration resistor R_S, which approximates as linearized transconductance, and a load resistor R_L, which converts current into an output voltage. As R_S is tuned and R_L is constant, the amplifier gain is defined by $\frac{R_L}{R_S}$. Differential topology is exploited to improve immunity to interference.

As Fig.2.2 depicts, the programmable capacitive feedback network is another choice of PGA [17, 20, 21]. An inherent advantage of capacitors is noise-free, but capacitors are quite expensive and occupy a large area, which is not applicable for miniature ultrasound probes.

The current steering network is another technique for discrete gain setting [22, 23]. Instead of varying impedance ratios, the gain is set by the current ratio that flows into feedback branches as shown in Fig.2.3. The current ratio is controlled by the current division network (CDN). The adopted current steering topology is accurate and insensitive to PVT variations, however, it is not applicable to high-frequency operational amplifiers because of the large output current demand by operational amplifiers [23].

Although discrete gain steps suffer from image artifacts, it appears to be helpful to look into various architectures of PGAs. All three methods can be converted into continuous gain settings with the external analog control signal.



	G1	G2	G3	G4
6 dB	0	1	1	1
12 dB	0	1	0	0
18 dB	0	1	1	0
24 dB	1	1	1	0

Figure 2.2: Fully differential PGA with capacitive feedback network and gain control code map [17]

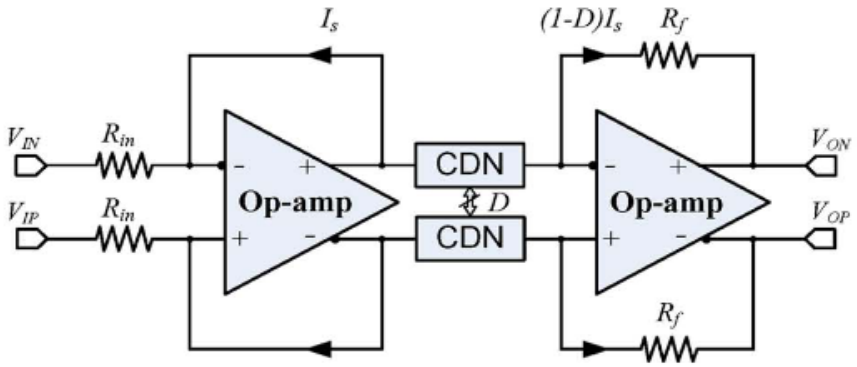


Figure 2.3: PGA architecture with the CDN [23]

2.2 Continuous TGC Implementations

To alleviate the handicap of amplifiers with discrete gain steps, VGA with a continuous gain is a better approach to achieving a smooth curve. The amplifier comprises a gain control circuit to which analog control voltage is applied. The control voltage is ramped linearly over time to obtain the desired gain range, avoiding imaging problems associated with switching transient.

Generally, the gain implementations are split into three main subgroups:

1. Amplifiers with purely exponential function [12, 24, 25]: They rely on the inherent characteristics of BJTs or MOSFETs in the sub-threshold region to obtain a exponential function. But they are sensitive to PVT variations.

2. Amplifiers with pseudo exponential gain [26, 27, 28]: They are designed based on the chosen approximated exponential equation. Multiple mathematical approximations could realize pseudo exponential functionality with respective gain range and gain error.

3. Amplifiers with interpolation between discrete gain steps [11, 13, 29, 30, 31]: They are similar to PGA with discrete gain steps but the gain is switched continuously by means of a current steering network.

In the following subsections, all three methods and their typologies are illustrated and their strengths and weaknesses are compared. Based on the state-of-the-art, the performance of the representative architectures will be compared in section 2.3.

2.2.1 Purely Exponential Functionality

Building a dB-linear gain profile is the most critical issue in the VGA design. One approach for designing a CMOS-based VGA with dB linear gain is realized by bipolar transistors (BJT) [24] or MOS devices [25]. The inherent exponential characteristics of devices can easily be adopted for the design of dB-linear gain. In [24] exponential gain control is achieved by bipolar devices. Although bipolar devices proved to be effective for a wide gain range, it is not cost-effective standard CMOS technology, restraining its use. Another choice is to use MOS devices in the triode region to obtain exponential gain with the help of the exponential control generation circuit.

In pursuit of accurate dB-linear characteristics across a wide range, a simple and robust 'cell-based' method is presented for VGA design [25]. The biggest advantage of cell-based VGA is that the number of cascaded unit cells can be chosen corresponding to system requirements, without consuming too much power. Fig.2.4 demonstrates the schematic of the unit cell with gain compensation, comprising both nMOS and pMOS transistors as active loads. The exponential gain profile is obtained by tuning the bulk control voltage of the pMOS and no extra circuitry like exponential generators is required. The voltage gain is simply the transconductance ratio of input pairs and load

transistors. Since the current through $M_{5,6}$ is constant and $V_{OV3,4} + \Delta V_{OV3,4}$ is much bigger than nV_T, the voltage gain can be approximated as follows:

$$A_v = \frac{g_{m5,6}}{g_{m1,2} + g_{m3,4}} = \frac{g_{m5,6}}{g_{m1,2} + g_{m3,4} + \Delta g_{m1,2} + \Delta g_{m3,4}} = \frac{g_{m5,6}}{g_{m1,2} + g_{m3,4} - \frac{2\Delta I_{Ds3,4}}{nV_T}} \tag{2.1}$$

The threshold voltage with body effect is calculated as follows. Since $M_{1,2}$ is biased in sub-threshold region, the $\Delta V_{gs1,2}$ is omitted and $\Delta I_{DS3,4}$ only depends on $\Delta V_{TH3,4}$. After calculation $\Delta I_{DS3,4}$ is linear proportional to $\Delta V_{SB3,4}$, indicating a variable bulk voltage could induce a change in current.

As long as the nMOS transistor loads are large enough and biased in the sub-threshold region, an accurate dB-linear curve is obtained by adjusting the pMOS bulk voltage.

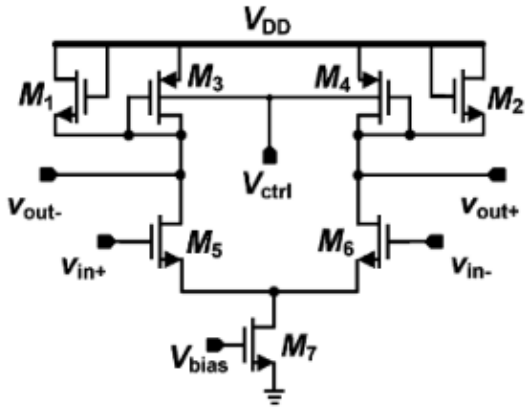


Figure 2.4: Schematic of the unit cell with tunable pMOS bulk voltage [25]

However, there's a price to pay for cascading gain stages to achieve a wide gain range. The cascading stages introduce multiple secondary poles and reduce the signal bandwidth. Besides, the open-loop structures are sensitive to PVT variations.

2.2.2 Pseudo Exponential Functionality

Pseudo-exponential functionality is another method for attaining a dB-linear gain. It possesses the merit of immunity to PVT variations due to the independence of inherent properties of MOS devices (or BJT devices). The gain over a certain range can be approximated by circuitry that mimics various kinds of mathematical expressions such as the Taylor series or Duong's approximation.

One of the most common method is Taylor series approximation $e^x = (\frac{1+x}{1-x})^2$. Fig.2.5 shows two types of VGA employing this approximation, where the transconductance ratio or resistor ratio is tuned to resemble an exponential curve. Fig.2.5 (a) shows an open-loop amplifier whose gain is controlled by input and output bias current. However,

using this method the gain range is limited to 12 dB [26, 27, 28]. Although cascading multiple stages can extend the gain range, it leads to large gain error, high power consumption and large chip area. Fig.2.5 (b) illustrates another VGA with a closed-loop structure, MOS transistors in the sub-threshold region are adopted in the feedback network as tunable resistors. To approximate the gain curve, the resistance R_{m1} and R_{m2} vary in opposite directions by controlling the gate voltage in opposite directions. This topology eliminates the non-linearity related to the amplifier, but non-linearity related to MOS transistors itself becomes a significant source of error. Moreover, the gain range is subject to the limited control voltage range, especially in low supply voltage design. As a consequence, MOS nonlinearity, and limited gain range remains to be the major disadvantages.

In summary, the major advantage of pseudo exponential functionality is that the adverse effects of PVT variations are suppressed due to matched devices. While the disadvantage is that the gain range is quite limited.

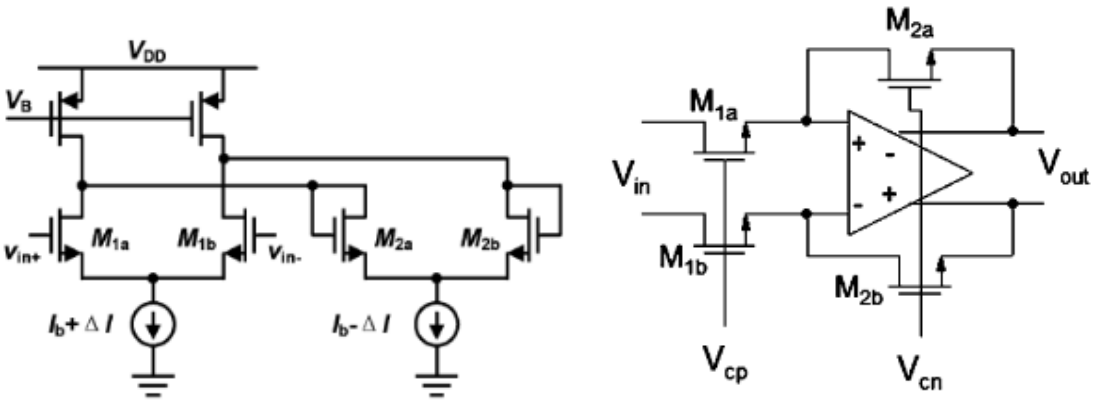


Figure 2.5: (a) VGA with tunable Transconductance ratio (b) Feedback tuning VGA [29]

2.2.3 Interpolation

Interpolation is the third approach to produce dB-linear gain, which is employed in LNA-TGC structure extensively [11, 13]. A TGC amplifier with interpolation between discrete gain steps has a feedback network to provide gain steps and a smooth transition between these gain steps [31, 32]. In [31] a resistive ladder attenuator network is employed to provide fixed attenuation gain for each step and multiple input stages with controllable biasing are switched gradually ensuring a smooth curve.

Interpolation can also be achieved by smoothly altering the resistance values in the resistive feedback network [29]. The multiple-ramp controlled switches allow for a high linearity trim mechanism. By introducing switch-controlled parallel resistors, the nonlinear region in resistance changing is reduced by turning multiple switches simultaneously. The price of this smooth transition is additional voltage-ramp circuitry,

resulting in increased area and power.

Another topology of interpolation involves current steering by means of differential pair. By shifting the gate voltage of the differential pair, the fraction of output current that is steered into the input could be changed, and thus the current gain is continuously varied [30].

A similar topology of interpolation by current steering is also adopted in [11] in a current-amplifier-based TIA. Fig.2.6 illustrates the circuit diagram in which the current steering network (CSN) directs the amplified current into feedback nodes through a series of pMOS transistors. The feedback current steers from tap to tap by pulling down the corresponding gate voltage $V_{GP,n}$. And 5-tap capacitive ladder network is proposed for 40 dB wide gain range. Each gain step consists of ladder capacitor C_A, C_B and $C_T$to provide a current gain of $\alpha = 1 + \frac{C_T}{C_A}$. As this current mechanism requires a large capacitive network, this proposed topology occupies a per-channel die area of 0.12 mm^2 and is comparatively large for pitch-matched AFE with 2D transducers.

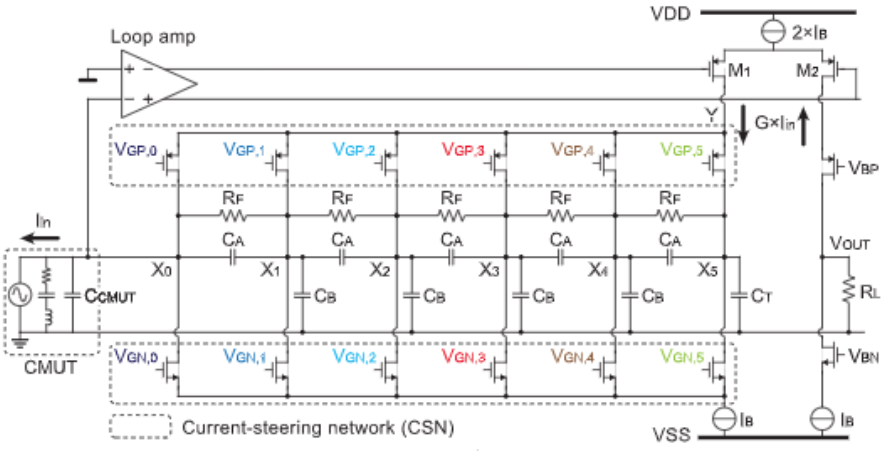


Figure 2.6: Linear interpolation by current steering network[11]

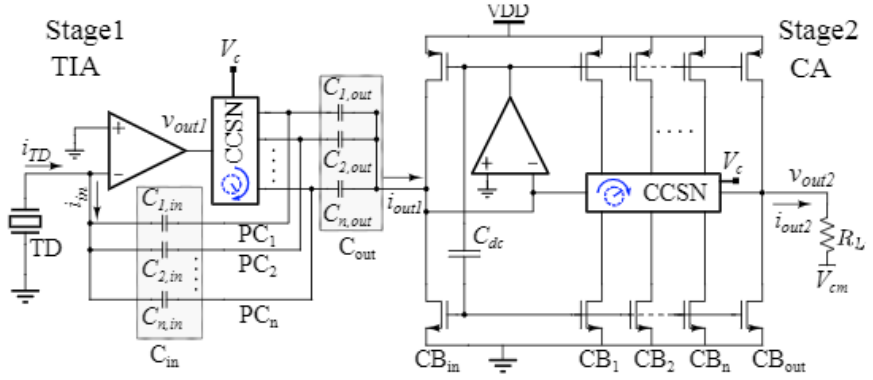


Figure 2.7: Two stage AFE with Complementary Current Steering Network [13]

As depicted in Fig.2.7 a two-stage interpolating VGA is adopted for a more compact area of AFE and improved dB-linear gain accuracy [13]. The first stage is TIA with a feedback capacitive array followed by a output capacitive array to keep a current i_{out1} and the ratio of $\frac{i_{out1}}{i_{TD}}$ is set by capacitive arrays C_{in} and C_{out}. The second stage of VGA is a current amplifier in which the gain is defined by current mirror ratios between input and output. The gain steps in each stage follow $\frac{1+x}{1-x}$ trajectory approximating a $(\frac{1+x}{1-x})^2$ curve that estimates the desired exponential gain curve. The CCSN of each stage performs interpolation between adjacent two taps such that the interpolation also follows a pseudo exponential trajectory, contributing to a great reduction in dB-linear gain error. The additional merit of this design is the hardware-sharing scheme, which enables high area and power efficiency by sharing hardware like voltage regulators.

2.2.4 Exponential Functionality of Triode Device

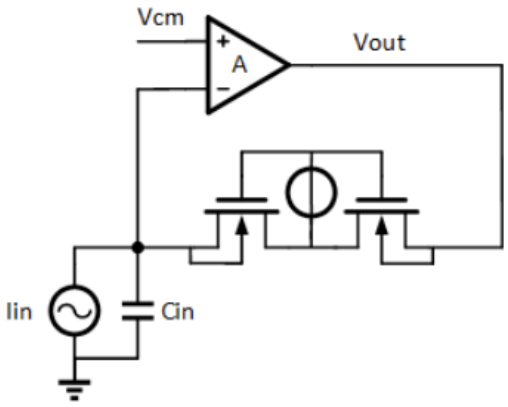


Figure 2.8: Schematic of the TIA with a pseudo resistor [12]

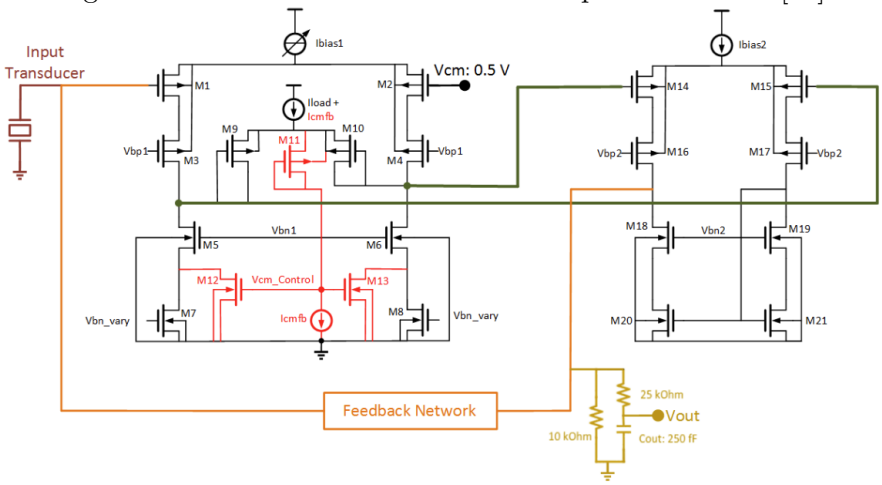


Figure 2.9: schematic of the loop amplifier[12]

In contrast to the previous topologies, continuous TGCs can be realized by triode

devices. A variable-gain low-noise transimpedance amplifier is demonstrated in [12], and the simplified schematic is shown in Fig.2.8. The basic concept is to use triode devices as the feedback impedance. Since the source-drain resistance of the triode device is inversely proportional to the gate-source voltage, an exponentially decaying control voltage is applied to obtain an exponentially increasing impedance. Multiple triode devices can be implemented in parallel for a wide gain range. Unlike the interpolation scheme, no current steering network is required. In this case, all resistive branches are connected initially to provide the smallest feedback impedance. Gradually some branches are turned off by lowering control voltages and disconnected from the feedback network. As the control voltage decreases, the largest feedback impedance is obtained at the end of receiving period. There are no explicit switches in the branches because of the inherent property of parallel impedance.

Using MOS devices causes non-linearity and noise issues. The MOS non-linearity is caused by the body effect. By means of the dual transistors, the even-order harmonics are greatly improved. The noise issues are negligible when the impedance value is large.

The exponential voltage generator comprises a precharged capacitor and a big resistor. To save area, a pseudo resistor is made by a transistor in the saturation region. The principle is that a constant current is drawn from the pseudo resistor to discharge the capacitor. Thus the voltage of a discharging capacitor mimics the decaying exponential control voltage. This simple generator only contributes thermal noise which is quite small. And each LNA channel has individual exponential voltage generators, so there's no correlated noise introduced by the control voltage generation circuit.

Fig.2.9 shows a simplified schematic of the loop amplifier. The load capacitor introduces a second pole at the output. Since the loop amplifier is a two-stage OTA, the output impedance is large, leading to a current division between feedback resistance and the output impedance at high gain. The first stage needs to have a 20 dB variable gain to compensate for the decreasing loopgain at high gain. When the feedback resistance increases to a level where the partial current is absorbed by the load, the gain of the first stage boosts to maintain a constant unity gain frequency. Since the output impedance of the OTA is quite large, a resistive broadening technique is applied to drive an output load from a stability perspective.

In a word, this topology effectively reduces the circuit complexity and saves area by employing the pseudo resistive feedback network. But the load-driving capability is limited even with the resistive-broadening technique. The output impedance of the loop amplifier should be inherently low for stability reasons. Moreover, having a varying bias current source in the first stage can be problematic. The variable bias current source is designed linearly dependent on the feedback resistance and copied to the main amplifier with current mirrors. This implies that the current noise of the variable bias generator is directly copied and amplified to the main amplifier. Even if the original current noise is small, the multiplied current noise could have a significant contribution to the input noise. A low-pass filter is employed to mitigate the problem. However, the varying input transconductance and the varying feedback resistance are not intrinsically matching.

Ideally, the two variables should change in the same manner to achieve a constant UGBW, but with the operating points changing as I_b increases, the ratio deviates from expectation. Consequently, UGBW moves as a function of gain, leading to instability issues.

2.3 Research Gap

In most cases of sections 2.1 and 2.2, the TGC amplifier is followed by the LNA. This poses challenges for both TGC and LNA. Firstly, it implies that LNA is obliged to handle the full DR at its own output at the expense of additional power. Secondly, TGC amplifiers have a limited capacity to suppress noise as it depends on the LNA to attain the needed NF.

Designing LNA and TGC in a combined fashion appears appealing for two reasons. The first merit is associated with better power efficiency. Combining TGC and LNA in a single feedback loop prevents energy from being wasted on the LNA output handling the full DR. Besides, LNAs have a loose noise target at the lowest gain. Power is only consumed to suppress noise at the highest gain, where the noise requirement is most stringent [11]. The second advantage is the die area. In miniature 3D imaging probes, high area efficiency is strongly advocated for pitch-matched integration. Realizing Combined LNA-TGC with the smallest die area is our priority under competitive noise performance and wide gain range.

Table 2.1: Comparison with the Prior Art

	Target specification	[11]	[12]	[13]	[14]
Process	0.18 μm CMOS	0.18μm HV BCDMOS	0.18 μm CMOS	0.18μm HV BCDMOS	0.18μm HV CMOS
Topology	TIA	TIA	TIA	TIA	TIA
TGC type	purely exponential	ITP	Purely expoential	ITP	DT
−3-dB(MHz)	10	7.1	20	17.5	10
Max gain(dBΩ)	106	107	100	102	116
Gain range(dB)	40	33	40	36	12
Gain error(dB)	±1.5	±1	±1.4	±0.4	±3
TD Capacitance (pF)	18	15	18	1	2
Input referred noise density ($pA/\sqrt{Hz}$)	1@7.5MHz	1.7@5MHz	1.12@7.5MHz	1.31@10MHz	0.41@5MHz
Power consumption(mW)	**	5.2	5.5	0.8	1.4
Area/ch.(mm^2)	**	0.12	0.013	0.025	0.028
$NEF[mP \cdot \sqrt{(mW/Hz)}]$	**	0.78	0.8	**	2.7

[1] $NEF = P_{n,in} \cdot \sqrt{POWER_{tot}}$[14], $P_{n,in}$is the input-referred acoustic pressure noise spectral density averaged in passband

Compared with the prior art, the merits and drawbacks of the introduced work are presented in table 2.1. Both [11]and [13] adopt a capacitive feedback network to realize gain steps and current steering as interpolation schemes. The capacitive feedback network can accurately define the gain and hardly contributes noise, unlike the resistive feedback network. It is also immune to PVT variations or non-linearity problems related to non-linear devices. However, the price to pay is the die area. The larger capacitive ladder network in [11] makes it unsuitable for pitch-matched layouts. Although the area per channel LNA is much reduced in [13], there is still room for improvement. The interpolation requires a current steering network and current steering biasing network to generate a series of gate voltages for continuous gain control. These networks consume area as well. In summary, the interpolation with the capacitive feedback network is not the best scheme for continuous TGC from the perspective of the die area. Besides, the

current steering biasing network also adds noise to the input and leads to correlated noise if it is shared among different LNA channels.

An exponential scheme with triode devices, in contrast, seems fit for an area-efficient design. Due to the inherent characteristics of triode MOS devices, triode MOSFETs are ideally tunable resistors when applied varying gate voltages[12]. Compared to a TIA with capacitive feedback, this approach can reach a minimal die area. But it comes with inherent non-linearity of MOS devices and thermal noise contribution, which requires careful design. One intriguing merit is that the control voltage generator only includes a pseudo-R-C network, a tiny structure compared to the current steering biasing network. Each individual tunable resistor has its own control voltage generator, thus avoiding correlated noise from different LNA channels. Overall this scheme can reduce the gain control circuit's complexity and save area.

However, the loop amplifier has low driving capability due to the OTA structure and requires a resistive-broadening technique for stability. A better frequency compensation strategy could solve this problem. Another critical issue is the gain control mechanism in the main amplifier. It is hard to have varying input transconductance and feedback resistance tracking each other. And imperfect gain matching leads to a slowly moving UGBW. The variable bias current source generator also introduces input-referred noise which is reduced by a low-pass filter.

In view of all three schemes, a purely exponential scheme is more appealing in terms of area. In response to all the difficulties related to the TIA with the pseudo-resistive network, an improved architecture with resistive feedback is called for.

3 Architecture

This chapter aims to design a suitable architecture for the proposed LNA-TGC. It begins with an analysis of the transducer. The feedback network topology is adopted from [12], aiming for linear-in-dB variable gain while consuming minimal die area. The architectural design is made regarding driving capability, constant closed-loop bandwidth and power efficiency. The goal is to deliver a feasible TIA architecture with a pseudo resistive feedback network to achieve high area efficiency and competitive performance.

3.1 Transducer

Transducer characteristics determine the topologies of the LNA. Different types of LNAs interface with transducers with different source impedance. Thus, a tailored analysis of the target transducer's impedance profile is necessary in order to choose an optimal topology of the LNA.

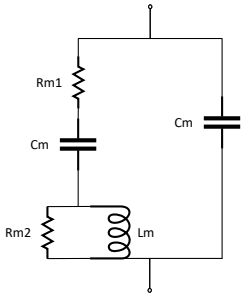
In order to explore the loading effect of the transducer, it's critical to choose a model which fits its electrical properties. As shown in Fig.3.1, the transducer comprises a static capacitive branch and a motional RLC branch. The operating frequency is determined by the resonant branch. Since the same CMUT transducer is adopted from [11, 12], the center frequency is set at 7.5 MHz with a bandwidth of 5-10 MHz. Given the model parameters of the adopted CMUT, we can intuitively analyze which branch dominates at resonant frequency:

$$(1) R_{m2} + \frac{1}{2\pi f \cdot C_m} > \frac{1}{2\pi C_p} \tag{3.1}$$

$$(2) R_{m2} + \frac{1}{2\pi f \cdot C_m} < \frac{1}{2\pi C_p} \tag{3.2}$$

With simple approximation, some parameters are neglected and the result shows that the dominant branch is the capacitive branch. The computed input impedance around the center frequency is 1.2 kΩ. This impedance value is considered relatively high and requires an amplifier with low input impedance. Therefore, the input source is modeled as a current source to minimize the input signal distortion.

For simplification, the CMUT transducer is modeled as an input current source and a shunt capacitor of 18 pF. First, the resonant branch is negligible as the impedance



Component	Value
Rm1	1.1mΩ
Rm2	16.9kΩ
Lm	3.1mH
Cm	2,38pF
Cp	17,62pF

Figure 3.1: The equivalent Van-Dyke model for CMUT transducers

of the transducer is determined by the capacitive branch in the bandwidth of interest. Second, the simplified diagram is more clear to read.

3.2 Transimpedance Amplifier

Due to the relatively high input impedance, the LNA structure should be embodied as a TIA or a CA. As the following blocks require a voltage input, there should be a current to voltage conversion in the LNA. Therefore, a TIA is chosen to be the LNA topology.

As depicted in Fig.3.2, the proposed TIA is a closed-loop structure with resistive feedback. The merit is that TIA and TGC function can be designed separately and simplifies the design. The feedback path focuses on the gain range and the feedforward path handles noise, bandwidth and distortion. The closed loop TIA also keeps the transimpedance gain approximately equivalent to the feedback impedance if the loop amplifier has a large gain. Therefore, the overall transimpedance gain is achieved by exponentially varying feedback impedance.

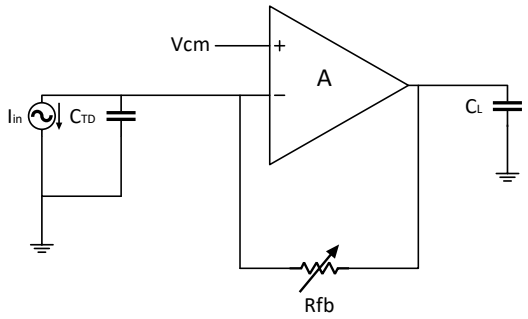


Figure 3.2: the schematic of the TIA with the output load

The design of LNA includes three steps. First, the exponentially increasing resistive feedback network is designed based on design specifications. Then the loop amplifier is created. Finally, the overall TIA architecture is evaluated in terms of stability, noise, distortion and gain requirements.

3.3 Feedback Network

The general scheme of the resistive feedback network is based on [12]. As discussed in section 2.3, a capacitive feedback network occupies a larger die area compared to a pseudo resistive network. The interpolation involves current steering, resulting in a large biasing ladder network at the expense of area. From the perspective of area efficiency, a resistive network composed of MOS devices is more appealing.

3.3.1 Pseudo Resistor

The fundamental element of the feedback network is a tunable resistor, which is designed with MOS transistors in the triode region. In order to obtain a tunable resistor, the MOS device is operated in the triode region:

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2) \tag{3.3}$$

Due to the quadratic terms of drain-source voltage, the device should operate in the deep triode region to mitigate the second-order distortion introduced by the drain-source voltage. If the second-order distortion is negligible then the drain current can be readdressed as:

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_T)V_{DS}) \tag{3.4}$$

In this case, a tunable resistor is created if the overdrive voltage is an exponentially decaying voltage source:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}((V_{GS} - V_T)} \tag{3.5}$$

The deep triode condition is expressed as $V_{DS} < 2(V_{GS} - V_T)$ which should be maintained during the full receive period. This implies that the minimum overdrive voltage should be two times larger than the limited output swing.

To further improve the linearity of the triode devices, the feedback resistor is embodied as two back-to-back triode devices connected in series with their bulks connected to outer nodes [12]. This topology is utilized to limit the distortion associated with the body effect and improve the linearity of the feedback network. Since the input source is a purely AC current source, the current flowing through the feedback changes direction

every half cycle, leading to drain and source switching positions every half cycle. The threshold voltage is a function of the source-bulk voltage:

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \tag{3.6}$$

The threshold voltage affected by V_{SB} no longer remains constant and MOS resistance will be distorted. Two triode devices with bulks connected to opposite sides are designed to cancel out first-order terms of the body effect. Aiming at saving area and reducing distortion, the configuration in Fig.3.3 is chosen, due to its well-balanced nature.

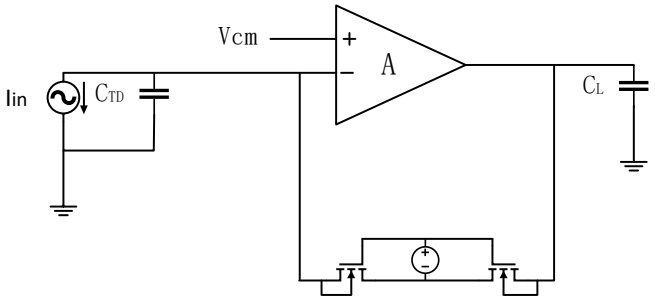


Figure 3.3: the TIA with parallel tunable resistors configuration

The varying feedback resistance value is determined based on two factors. First, the thermal noise contributed by the feedback resistors should be insignificant to leave more noise budget for the loop amplifier. Based on calculations, the minimal resistance is 100 kΩ at the high end of the gain range. Second, the maximal resistance is subject to maximal signal swing. The signal swing cannot be too large to leave enough voltage headroom at the output. It is restricted by the gain range as well. The minimal overdrive voltage is determined by maximal swing, and doubling the signal swing leads to 6 dB gain range degradation. Regarding the trade-offs, the resistance is set to 200 kΩ at the high end, leading to a 100 mV swing. With a 100 mV swing, there's enough headroom to keep the output stage in saturation.

Apart from MOS linearity, another crucial issue is to obtain the gain range. The overall 40 dB gain range is obtained with an output amplitude of 100 mV. According to the design specifications in section 1.5, the input current amplitude decreases from 50 μA to 0.5 μA, leading to a resistance range from 2 kΩ to 200 kΩ.

To compute the gain range, the V_{cm} level must be chosen such that all transistors in the loop amplifier are in saturation. To allow for voltage headrooms for the current-reuse amplifier, V_{cm} is chosen around mid-supply. The proposed LNA is implemented in ±0.9 V supply, so the V_{cm} is chosen at 0 V.

The gain range of a single branch is set by overdrive-voltage ratios. The minimal overdrive voltage is two times larger than the maximal source-drain voltage in the deep triode condition. With a 100 mV swing, the maximal source-drain voltage is also 100 mV, resulting in a minimal overdrive voltage of 200 mV. The maximal overdrive voltage

depends on the maximal gate voltage. The gate voltages can be chosen at the supply rail or 2V higher than the lowest potential terminal since they are 2V transistors.

The maximal gate voltages are either 0.9V (positive supply) or 1.9V ($2V + V_{cm} - V_{out_amplitude}$). The output amplitude is $V_{cm} + V_{signal} = 0.1V$. Since in the triode region the MOS resistance is inversely proportional to the overdrive voltage, the overdrive voltage range reflects the resistance range. The gain range of a single resistor branch is computed with a positive supply, assuming a threshold voltage of 550mV:

$$\frac{V_{OV_{max}}}{V_{OV_{min}}} = \frac{0.9V - 0.1V - 0.55V}{0.2V} = \frac{0.25V}{0.2V} = 1.94dB \tag{3.7}$$

The gain range of a single resistor branch can also be computed with the highest potential voltage, assuming a threshold voltage of 550mV:

$$\frac{V_{OV_{max}}}{V_{OV_{min}}} = \frac{1.9V - 0.1V - 0.55V}{0.2V} = \frac{1.25V}{0.2V} = 15.9dB \tag{3.8}$$

Since a single branch could only achieve a 15.9 dB gain range in the best-case scenario, a strategy for extending the gain range is desired. Using parallel branches can meet the requirements while maintaining the source-drain voltage. Three parallel branches are required for extending the gain range. By operating each branch at its individual interval, the overall gain range can be obtained. As shown in Fig.3.4, the feedback network adopts three branches to cover the required 40 dB, with sufficient gain overlap to smoothen out the transitions.

Assuming an exponentially decreasing control voltage source, the resistance of each branch is exponentially increased as a function of time. By sizing the triode transistors differently and applying various decreasing rates of control voltages, the overall parallel resistance is nearly an exponentially increasing curve. At the lowest gain, all three branches are connected to deal with the maximal input amplitude and a 2 kΩ resistance is obtained. While at the highest gain, only one branch still turns on to amplify the smallest input signal, resulting in a 200 kΩ resistance. The linearity does not degrade significantly since all the branches handle the 40 dB input change compared to a T-network topology [12].

A gradual gain-switching mechanism is desired for operating each branch (or multiple branches) at the proper interval. A way of implementing this is to add a source follower to each branch[12]. The schematic using source followers as switches is shown in Fig.3.5. By turning down the bias current the source follower is effectively disconnected from the branch and the respective branch is turned off. With a current steering scheme, the transition can be quite smooth. The advantage is that the range of each branch can be equivalent and each branch is individually optimized. While the drawbacks are straightforward. Firstly, the added bias current sources increase the input-referred noise. Secondly, multiple gate control voltages are required to steer the current between different source followers. Thirdly, the source followers degrade linearity and add complexity, not to mention the additional power consumption.

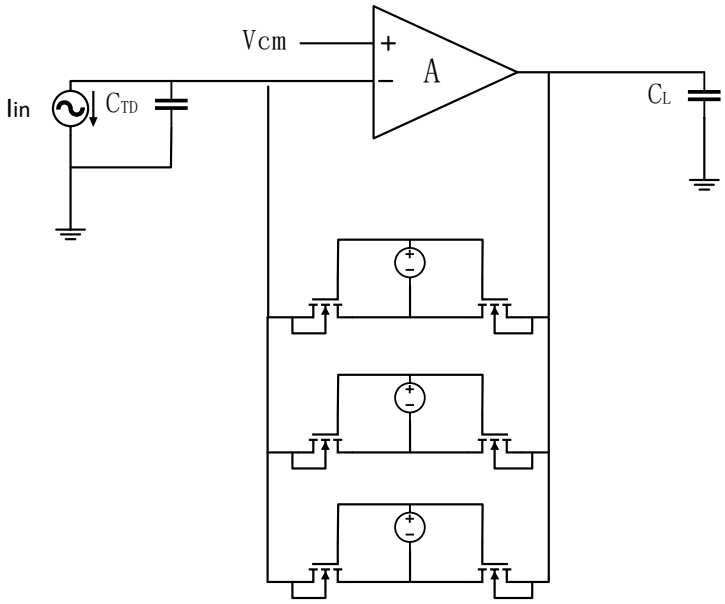


Figure 3.4: the TIA with parallel tunable resistors configuration

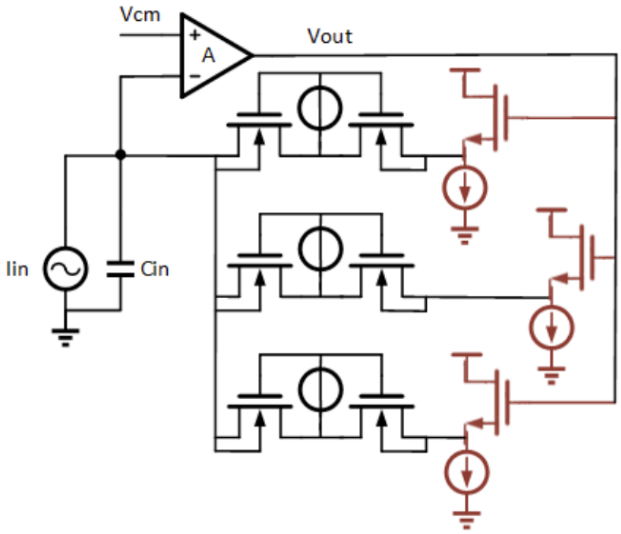


Figure 3.5: the TIA with explicit switches scheme [12]

An appropriate switching mechanism does not require an explicit switch. In this case, impedance steering needs no switches and the resistance itself will decide which branch dominates at their interval. Thanks to the nature of parallel resistance, the overall resistance is dominated by the smallest branch, while any other branch with relatively large resistance is considered inactive or disconnected. Each individual branch switching can be achieved by continuing to increase the resistance by decreasing the gate voltages, far exceeding its own gain range. Even when the gate voltage is reduced below the threshold voltage, the particular branch is still considered turned off. The smallest-resistance gain curve is switched smoothly if the control voltages of each branch

decrease at different rates.

3.3.2 Control Voltage Generation

To deliver an exponentially decaying control voltage, a MOSFET-C network is presented in Fig.3.6. With a precharged capacitor with a resistor, the voltage drop on the capacitor mimics an exponentially decaying voltage.

Since the discharge resistor is quite large (in the order of $M\Omega$), using real resistors seems unrealistic in terms of area and cost. The pseudo resistor is substituted with a MOS device in the saturation region. By keeping the overdrive voltage of the saturation device constant the drain current almost stays constant neglecting channel-length modulation. In other words, a constant current is flowing from the precharged capacitor.

However, this linear discharge method leads to some gain error since the overall resistance is not purely an exponential function. This gain error is a systematic error that can be further processed by digital post filters.

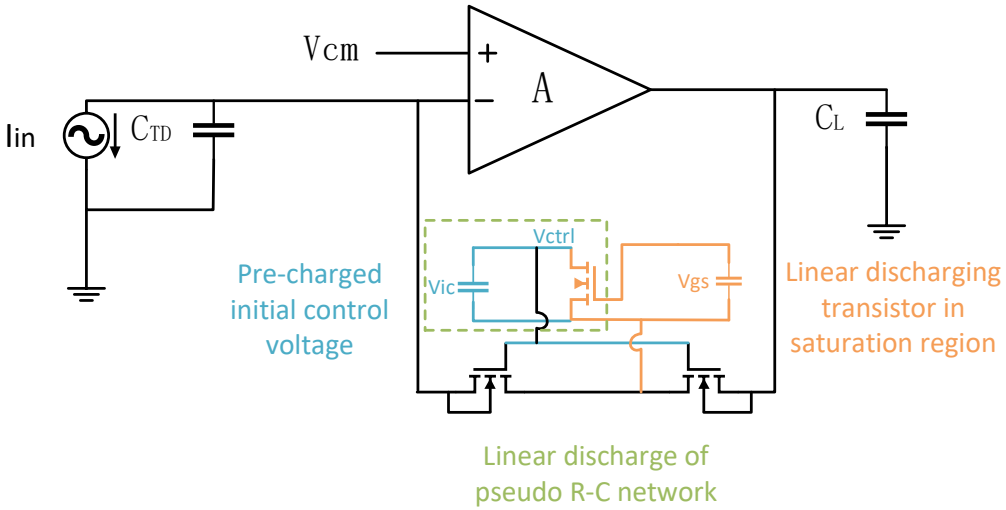


Figure 3.6: Control voltage generation circuit

3.3.3 Overall Feedback Architecture

The overall feedback network is depicted in Fig.3.7. It comprises three branches of dual transistor configuration and a control voltage generation circuit for each branch. Each dual transistors have different W/L ratios. Together with the control voltage generator, each dual transistor dominates at its own interval, leading to a dB-linear impedance profile.

Fig.3.8 (a) depicts different control voltages for three branches. For simplicity, all

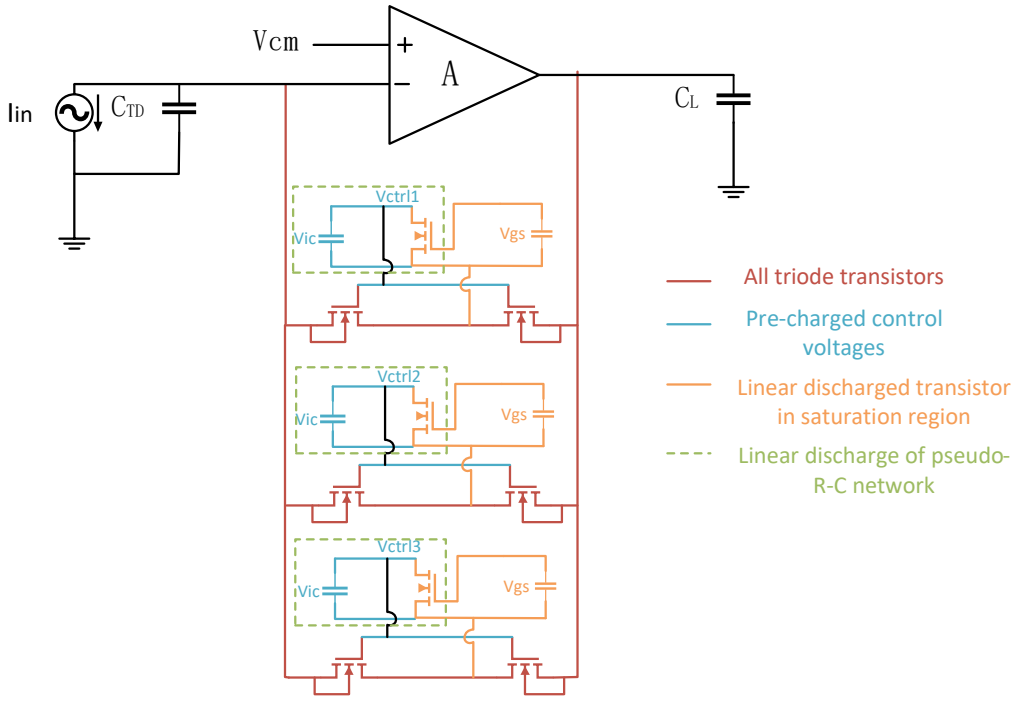


Figure 3.7: TIA with the overall feedback network

precharged capacitors have the same initial voltage and are released simultaneously. Choosing a single release moment allows reusing the existing control signals of the T/R switch [12]. In addition, multiple releasing moments will give rise to abrupt resistance change, causing transient artifacts.

Fig.3.8 (b) shows the ideal impedance profile and the impedance profile with the proposed feedback network. The figure shows some deviation with respect to a linear-in-dB curve. This is due to the artifacts at each gain-switching moment. This can be adjusted by discharging the current. By trimming the discharging current, the discharging rate of each branch is adjusted, leading to a smoother gain curve. The impedance deviation with respect to the ideal dB-linear curve is ± 1 dB in the 40 dB range using an ideal loop amp.

This feedback architecture has several advantages. First, it occupies less area than a capacitive feedback network. Two types of capacitors are used in the control voltage generator. First, the capacitor which sets the initial control voltage is chosen at 2.5 pF to convey an accurate discharge current. Trade-offs are made between minimizing die area and maintaining an accurate discharge current. Second, a 1 pF capacitor is used to keep the constant gate-source voltage of the discharging transistor. To mitigate the effect of the leaking current, a larger capacitor can be selected at the cost of more area. Therefore, a 2.5 pF discharging capacitor and a 1pF precharged capacitor are used in a single control voltage generator. For a three-branch feedback network, an overall capacitance of 10.5 pF is needed.

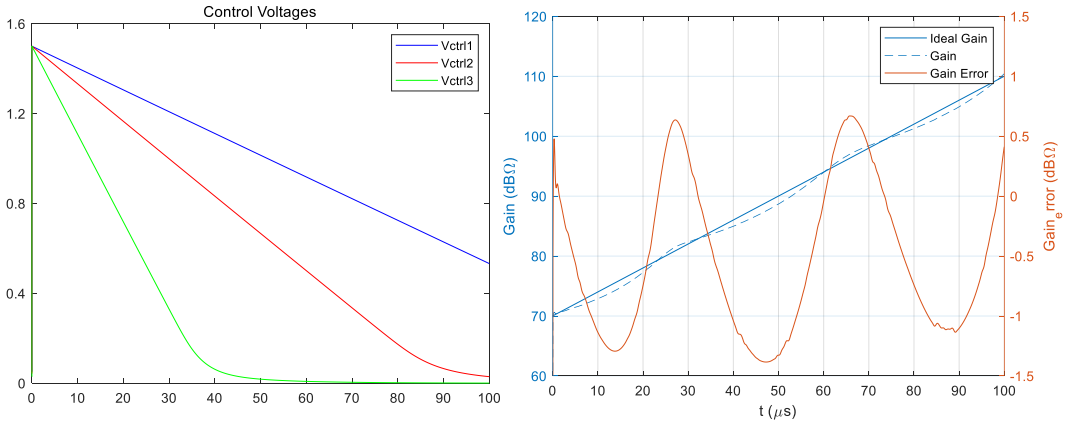


Figure 3.8: (a) Different control signals for three branches (b) The impedance deviation w.r.t. a linear-in-dB line

Second, the exponential control generator is a simple R-C network designed for each branch. Each individual circuit only contributes thermal noise from the pseudo resistor, which is quite small. Since the control generator is not shared among multiple LNA channels, the correlated noise is omitted.

3.4 Noise Analysis

In order to detect the smallest echo signal at the highest gain, the noise contribution of TIA cannot exceed the noise from the CMUT transducer. The two main noise sources are the feedback network and the loop amplifier. Since the loop amplifier consumes most of the power to achieve the noise target, a stringent noise budget for the loop amplifier implies large power consumption. Therefore, 90% of the total noise budget is for the loop amplifier, and 10% is left for the feedback network.

Since the pseudo-MOS transistor is regarded as noisy like a normal resistor, the minimal resistance value at the highest gain is about 100 kΩ:

$$i_n = \sqrt{\frac{4kT}{R}} \tag{3.9}$$

However, other factors must be considered as well. The resistance value influences the performance metrics of the loop amplifier. The feedback resistance together with the input 18 pF transducer forms a dominant pole. Assuming a low output impedance, the loopgain is calculated as follows:

$$Loopgain = \frac{A_v}{1 + sC_{TD}R_{fb}} \tag{3.10}$$

Where A_v is the DC gain of the loop amplifier. The loop amplifier needs at least 20 dB gain for accurate amplification. At the lowest gain, if the feedback impedance is 1

$k\Omega$, the input pole would be $s = \frac{1}{R_{fb}C_{TD}} = 8.8MHz$, and the unity gain frequency is 88 MHz. This is power-inefficient as more power is used to maintain an unnecessarily large bandwidth. It also causes instability due to secondary poles.

To vary the dominate input pole within a reasonable frequency range for a proper UGBW, the feedback resistance is set to 200 kΩ, resulting in a 100 mV output swing. The input-referred current noise density of the feedback resistor is :

$$i_{n,fb} = \sqrt{\frac{4kT}{R_{fb}}} = 0.29pA/\sqrt{Hz} \tag{3.11}$$

Another dominant noise source is the loop amplifier. Excluding the noise from the feedback resistor, the noise budget for the loop amplifier is 0.96 $pA/\sqrt{Hz}$. Since the input impedance of the transducer is 1.2 kΩ, the loop amplifier's input voltage noise density should stay below 1.15 $nV/\sqrt{Hz}$ to maintain an input-referred current noise of 1 $pA/\sqrt{Hz}$. This noise specification only targets the highest gain where the input signal is smallest and the SNR is most stringent. At the lowest gain, the input signal increases by 40 dB, resulting in an input-referred voltage noise target of 120 $nV/\sqrt{Hz}$, which is far simpler to obtain. Realizing this noise target in a power-efficient way is one of the most crucial goals in loop amplifier implementations, and will be further discussed in section 4.1.

4 Circuit Implementation

The previous chapter has discussed the architectural design of the proposed TGC-LNA, including the feedback network. In this chapter, the loop amplifier in the feedforward path will be implemented, aiming at obtaining noise specs while maintaining low power usage. The design choices are motivated by different trade-offs, including noise, power, gain control, linearity and stability.

The schematic of the loop amplifier and its bias network is shown in Fig.4.9.

4.1 Loop amplifier

As the main amplifier needs to achieve a good noise figure and realize accurate gain variation, the architectural design of the loop amplifier is critical. It impacts the overall performance of the TIA. As mentioned in chapter 3, the closed-loop topology allows for a separate design of TGC functionality and the LNA. The LNA determines the noise performance while the TGC plays a significant role in the transimpedance gain variation. But the TGC's variable gain will have a large impact on the loop amplifier's stability and gain control. Therefore, the varying feedback resistance should be taken into consideration when designing the loop amplifier.

As stated in section 2.2.4, the loop amplifier needs load-driving capability as well as a variable gain to maintain a constant unity-gain bandwidth. This indicates that a single-stage loop amplifier will not fulfill the requirements. Hence, the design calls for a multi-stage loop amplifier where different stages are optimized for respective specifications based on low power usage.

In the following sections, the building blocks and their design parameters are motivated. The design trade-offs are presented in all aspects.

4.1.1 Stability

The design of the loop amplifier starts with a detailed analysis of its frequency response. The loop entails a 40 dB-varying feedback resistor, an 18 pF transducer capacitor and a 1 pF load capacitor, indicating a two-pole system. It's critical to inspect the loop stability otherwise the op-amp goes unstable easily.

Fig.4.1 illustrates the simplified structure of the TIA. The R_{out} is merely the output impedance of the loop amplifier, implying a pole at the output. The varying R_{fb} along with the C_{TD} will create an input pole moving two decades within the bandwidth. As shown in Fig.3.2, a simplified model for the TIA is presented for frequency response analysis. Regardless of the interior design, the loop amplifier is modeled with a voltage gain of A. After breaking the loop at the input node, the loopgain is calculated as the amplifier gain multiplied by the feedback factor from the output to the input. The loopgain function is listed below:

$$\begin{aligned} \frac{AV_x - V_{out}}{R_{out}} &= V_{out} \cdot sC_L + V_i \cdot sC_{TD} \\ \frac{V_{out} - V_i}{R_{fb}} = V_i \cdot sC_{TD} &\Rightarrow V_{out} = V_i \cdot (1 + s \cdot C_{TD}R_{fb}) \\ \Rightarrow \frac{V_i}{V_x} &= \frac{A}{(1 + sC_{TD}R_{fb})(1 + sC_LR_{out}) + sC_{TD}R_{out}} \end{aligned} \tag{4.1}$$

And the poles are calculated as:

$$s^2 \cdot C_{TD}R_{fb}C_LR_{out} + s \cdot (C_{TD}R_{fb} + C_LR_{out} + C_{TD}R_{out}) + 1 = 0 \tag{4.2}$$

$$s_1 = \frac{1}{C_{TD}(R_{fb} + R_{out})}, \quad s_2 = \frac{1}{C_L(R_{fb} \| R_{out})}$$

where the R_{fb} is the feedback resistance and the R_{out} is the output impedance.

$$\text{when } R_{out} = 500\Omega, \quad Rfb = 2\text{k}\Omega, \quad f1 = 3.5\text{MHz}, \quad f2 = 400\text{MHz}$$

$$\text{when } R_{out} = 500\Omega, \quad Rfb = 200\text{k}\Omega, \quad f1 = 44\text{kHz}, \quad f2 = 318\text{MHz}$$

Here the two poles f_1, f_2 are approximated since f_2 is $>$ 100X higher than f_1.

For loop stability the desired R_{out} should be much smaller than R_{fb}. If R_{out} is comparable to R_{fb}, the output pole will play a significant role in the bandwidth of interest, which may lead to insufficient phase margin as the R_{fb} increases as a function of time. When R_{out} is much higher than R_{fb}, the input pole always exists at the low frequency. The input pole solely depends on R_{fb}, resulting in a 40-dB moving pole. This will definitely cause stability problems at the highest gain. The only choice is to set a much lower resistance value for R_{out} from the loop stability perspective. The additional merit of this design choice is the UGBW, which will be elaborated on later.

As covered in section 3.4, the feedback resistance ranges from $2k\Omega$ to $200k\Omega$. The output impedance should be as small as possible, but a small output impedance requires more power consumption. From this point of view, the output impedance is set at 500Ω, 4X smaller than the feedback resistance. Given the feedback resistance range of $2k\Omega$ to $200k\Omega$, the dominant input pole shifts from 35 MHz to 44 kHz while the output pole always lies in the high frequency and hardly deteriorates the stability. This imposes another problem associated with the UGBW.

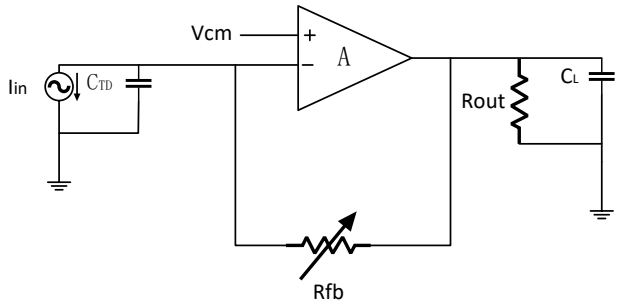


Figure 4.1: The TIA structure, including the output resistance and load capacitor

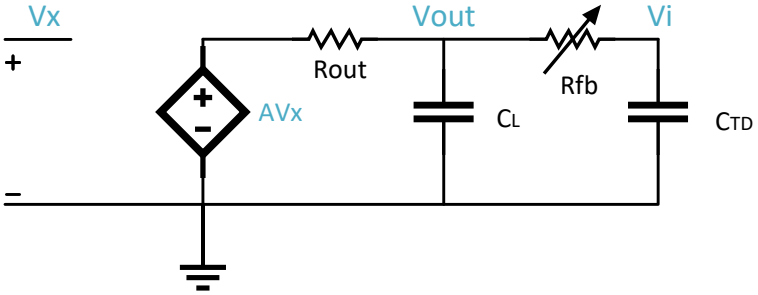


Figure 4.2: Simplified model of the frequency response

Assuming a fixed amplifier gain, a varying unity gain bandwidth (UGBW) will be observed due to the shifting dominant pole. The UGBW decreases as the feedback resistance increases, resulting in a 40 dB moving UGBW. This will give rise to several issues. First, the loop amplifier has the smallest bandwidth at the highest gain. For a specific UGBW requirement, increasing the UGBW to meet the target is inefficient because excessive power is wasted to maintain a larger UGBW at the smallest gain. The UGBW is optimized at a fixed frequency for high power efficiency at the low end.

The second issue for a moving UGBW is instability due to secondary poles. Ideally, at the low end, there exists only one pole in the bandwidth as the output pole is pushed to higher frequencies. But the loop amplifier needs multiple stages to obtain noise, gain and stability requirements. These stages provide output poles that may deteriorate the phase margin, especially at the smallest gain. Avoiding the situation by increasing the bandwidth of each stage will result in additional power consumption, which is detrimental. To allow for a stable amplifier, the phase margin is kept large. As a result, a fixed UGBW is called for.

Comparing the two subfigures of Fig.4.3, it is obvious that the DC gain of the loop amplifier must be altered as a function of gain for a fixed UGBW. As the dominant pole shifts to low frequencies the DC gain is increased and vice versa. The dominant pole is $s_1 = \frac{1}{C_{TD}(R_{fb}+R_{out})}$, the output impedance should be extremely low to allow for an accurate variation in the dominant pole. As the feedback resistance increases by 40 dB, the amplifier gain should also shift by 40 dB in the same fashion to realize a

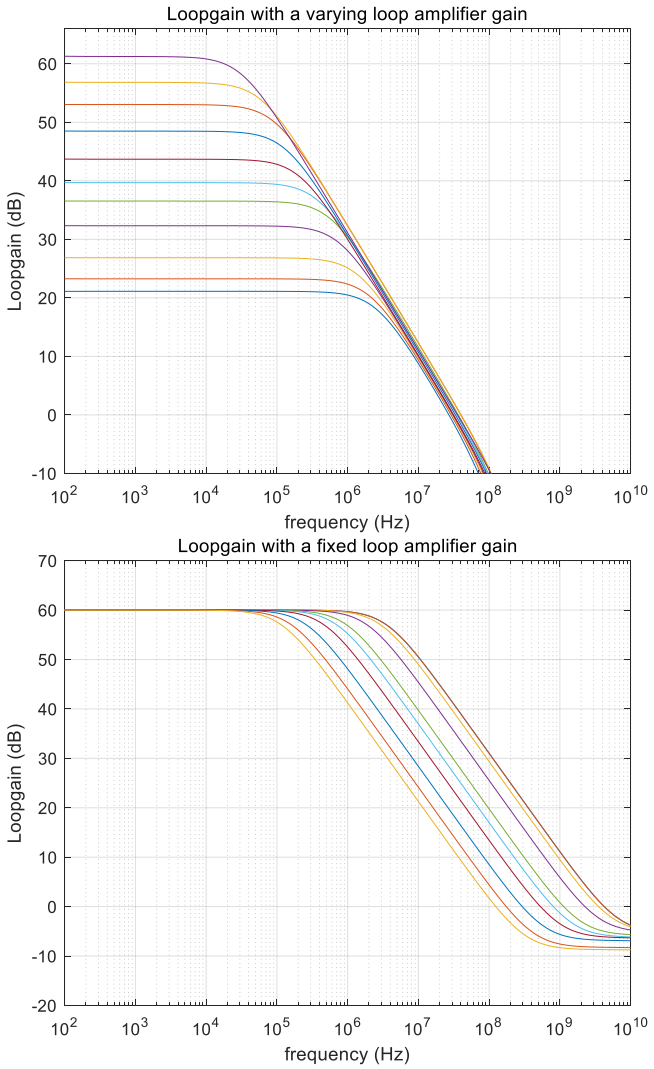


Figure 4.3: Different loopgain over whole gain range, with a fixed amplifier gain and a varying amplifier gain

gain-independent UGBW:

$$Loopgain = \frac{A}{1 + s \cdot (R_{fb} + R_{out}) \cdot C_{TD}} \tag{4.3}$$

Where A and R_{fb} are a function of gain.

Any unmatched gain control will lead to a time-varying UGBW. To alter the DC gain the loop amplifier must have variable-gain stages. This will be further implemented in section 4.1.2.

The unity gain frequency should be chosen in terms of sufficient DC gain and proper phase shift. A small UGBW means an insufficient DC gain and results in a signal swing at the input. To make the closed-loop gain accurate the DC gain should be at least 20

dB. A large UGBW is also unwanted because excessive phase shift is viewed at unity gain frequency. This causes an oscillating system.

In summary, specific design requirements are clarified based on stability issues. First, the loop amplifier entails a buffer as the last stage to provide low output impedance. Second, the gain of the loop amplifier is made variable to maintain a gain-independent UGBW and have high power efficiency. Third, each stage of the loop amplifier should push its output pole as far as possible, so that the loop stability is not significantly degraded.

4.1.2 Variable-gain stages

To obtain a gain-independent UGBW, a 40 dB variable-gain loop amplifier is required. As discussed in section 4.1.1, the DC gain of the loop amplifier should be at least 20 dB to allow for an accurate feedback gain. Thus, the gain range of the loop amplifier is 20-60 dB with an exponentially increasing function which resembles the feedback resistance.

There are two approaches to achieving variable gain, varying transconductance or varying the load. The simplified circuits are shown in Fig.4.4. Each method has its own merits and drawbacks. Varying the transconductance enables high power efficiency while maintaining high bandwidth. Because of the linear dependency between input transconductance and the bias current, the bias current is an increasing exponential function, leading to decreased average power consumption compared to the constant power consumed by the variable load topology. This imposes a varying noise floor. However, a varying noise floor does not degrade SNR performance as long as the gain difference is larger than the variation in the noise floor. In this case, the gain range is 40 dB, meaning the variation of the noise density shall not exceed 40 dB. As the input gm also increases by 40 dB the input-referred noise density grows by 20 dB, indicating no compromised SNR performance.

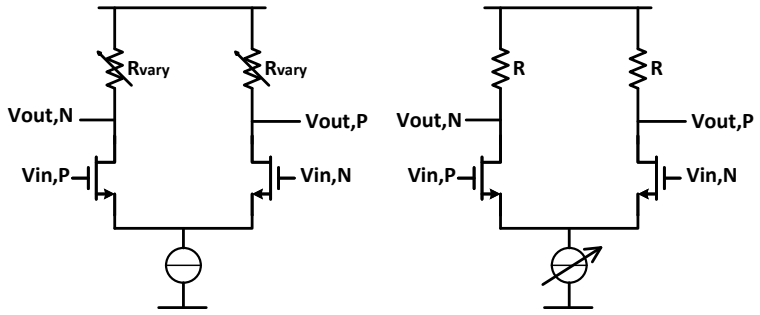


Figure 4.4: Two circuits to implement variable-gain, without CMFB

However, varying gm is an unreliable method in practice. As depicted in Fig.4.5, [12] introduces an active loop configuration to keep the linear relation between the bias

current source and the feedback resistance. The active loop uses a loop amplifier to keep the linear relation accurate.

There are mainly two concerns, noise and the mismatch between variable gm and variable feedback resistance. Normally the gm is controlled by a variable current source. First, the bias current source generator contains certain current noise density, which is copied directly into the main amplifier and amplified by the current mirrors. Extra actions must be taken to decrease the noise generated from the bias current source. A low pass filter can be implemented to filter out the in-band noise, as shown in Fig.4.5.

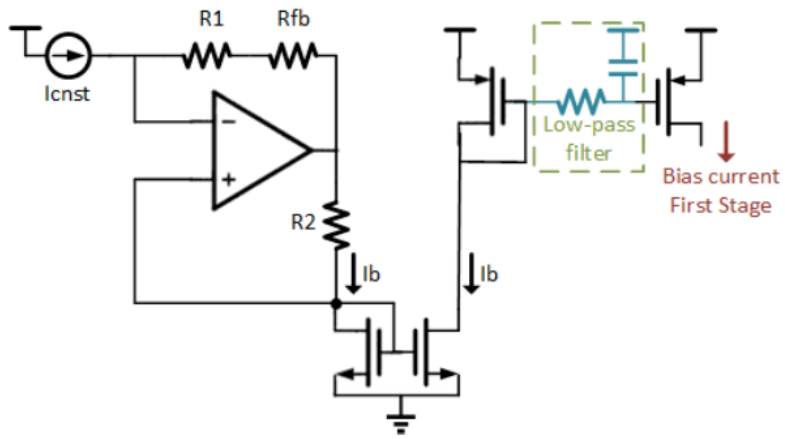


Figure 4.5: Variable bias current source linearly dependent on the feedback resistance, with a low-pass filter [12]

Another drawback is the inherent gain mismatch between the bias source and the feedback resistance. The bias current is expected to have a linear relation with the feedback resistance, resulting in an exponential current source. But the input gm no longer has a linear dependency on the 40 dB varying bias source as the operating points of the input transistors do not perform well. Even if the input gm shows a 40 dB variation, it is not recommended since the two gain control mechanisms are not tracking each other. Each mechanism generates some gain error and the ratio between gm and feedback resistance exhibits a larger variation. This leads to a moving UGBW.

The difficulties of the variable gm implementation motivated the variable load solution. The shortcoming of the variable load is the lower bandwidth while maintaining a constant power consumption. Firstly, the power consumption is not decreased as gm is constant, which is power inefficient compared to the variable gm solution. Secondly, the variable load introduces a moving output pole which shifts two decades in the band of interest. Together with the 40 dB moving input pole, the phase shifts significantly at the highest gain and causes instability of the loop amplifier.

However, the gain of the variable load can be split evenly into two stages. With each

stage providing a 20 dB variable gain, the output pole associated with the variable load only shifts by one decade. Assuming a UGBW of 25 MHz and an open-loop bandwidth of 100 MHz, the phase shift of one secondary pole is 15 °, so two secondary poles ensure 60 °phase margin. Therefore, a low, varying bandwidth due to the variable load does not create instability.

In summary, both downsides of the variable load are addressable through appropriate design choices. While the irresistible advantage is the intrinsic gain matching between the variable load and the feedback resistance. By adopting the dual triode transistors with the Mosfet-C network, a tunable resistor can be built. This way the two gain control mechanisms are identical and track each other.

4.1.3 Architecture

A suitable architecture is a foundation for designing the loop amplifier. There are multiple choices for LNAs such as noise cancellation amplifiers[33, 34], current reuse amplifiers[11], or telescopic amplifiers[12]. The working principles and performance of different architectures are illustrated and compared. Among all performance metrics, noise and power performance are prioritized.

Fig.4.6 shows the structure of a traditional noise-canceling amplifier. This amplifier achieves good noise performance and input impedance matching with two signal paths. First, M_{1P} is the common source amplifier with a resistive shunt feedback loop. It amplifies the signal (also the noise) while keeping input impedance matching. The input impedance is inversely proportional to g_{m1P}. M_{3P} is a source follower to convey the input signal. Second, M_{2P} is a common source amplifier that not only amplifies the signal but also provides an auxiliary path for noise cancellation. By setting proper transconductance for three PMOS devices, the noise from the main path and the auxiliary path will cancel each other. Thus, a low noise figure is obtained.

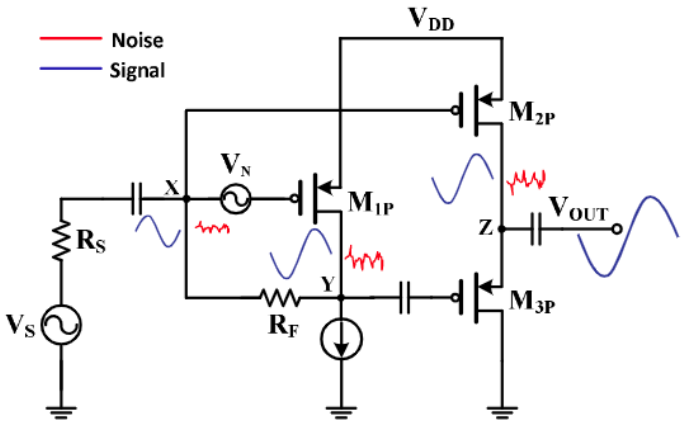


Figure 4.6: A schematic of a shunt-feedback feedforward noise canceling amplifier [33]

[33] adopts this noise canceling technique in combination with a complementary CMOS amplifier topology and designed an LNA with low NF and high linearity. Based on this wideband complementary noise and distortion canceling LNA, a current reuse topology is further carried out for low-power design.

However, despite of all the merits of the noise-canceling amplifier, it fails to meet the requirement of variable gain. For a fixed UGBW, the design aims to achieve a variable gain of 40 dB. Obviously, the g_{m1P} cannot be varied for input impedance matching. The shunt-feedback resistor R_F can be varied. But the amplification factor of the noise from node X to node Y is also varied as a function of R_F. Assuming a constant transconductance of the auxiliary amplifier, the noise canceling technique no longer applies. In order to cancel noise, the g_{m2P} (or g_{m3P}) must be made variable. This poses a leaking output current and strong signal distortion due to unmatched transconductance.

In a word, the noise canceling technique is not compatible with variable-gain loop amplifiers.

Fig.4.7 shows a current reuse amplifier structure adopted in [11]. The input pairs consist of both NMOS and PMOS pairs, which doubles the input transconductance g_{m1}. Besides, the cascade transistors are employed to increase the output impedance and mitigate the effect of large gate-drain capacitance. As a result, the voltage gain is increased and the input-referred noise is reduced.

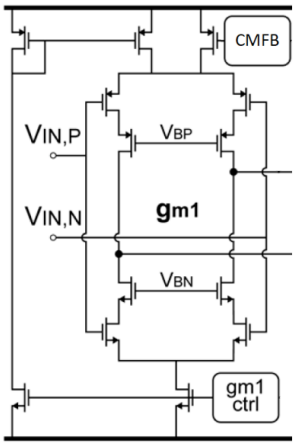


Figure 4.7: A schematic of a current reuse amplifier (without load) [11]

Applying this current reuse structure, the power efficiency is increased. From the perspective of the noise, the input-referred noise voltage density is decreased by a factor of $\sqrt{2}$. Compared to the traditional telescopic amplifier used in [12], the same target can be realized in higher power efficiency, which is crucial in this design.

Input voltage is another factor that restricts the amplifier structure. The current reuse amplifier demands a mid-supply input level to leave voltage headrooms for the cascades. In contrast, a telescopic amplifier can have a relatively low or high input level based on

the input transistor type. The common mode voltage is chosen at mid-supply (0 V), in combination with the symmetrical supplies, the current reuse structure outperforms other structures.

Therefore, the current reuse structure serves as the basic structure of the loop amplifier. The load of each sub-amplifier is freely chosen based on its functionality.

The four stages of the loop amplifier are shown in Fig.4.8. The first stage is a current reuse input stage with diode-connected loads. The gain of the first stage is constant at $\frac{g_{m1}}{g_{m1L}}$. In order to save power, a ramp voltage generator is applied to deliver an increasing tail current. The input transconductance is largest only at the high end of the gain range, where the noise target is the lowest. While at the low end of the gain range, a higher input noise level is tolerated, so the input transconductance is reduced, resulting in less power dissipation.

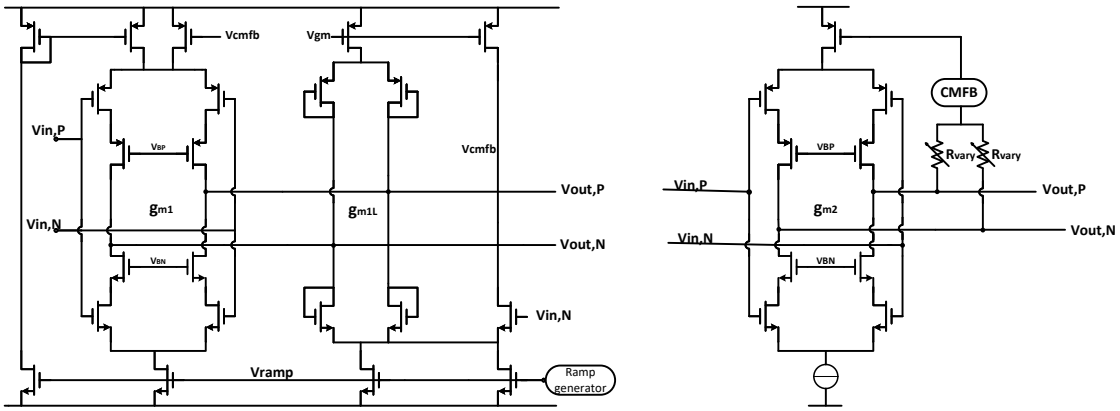
As discussed in section 4.1.2, the intermediate two stages are constant input stages with variable resistance loads. For simplicity, the second and third stages have identical structures. As shown in Fig.4.8(b), each stage has a current reuse input stage with a variable load resistor, realizing a 20 dB varying gain. The cascading of two stages achieves a 40 dB variable gain. The variable load resistors will be explained in section 4.3.

The output stage requires a low output impedance, therefore a buffer is provided in Fig.4.8(c). Since ultrasound signals are single-ended, the LNAs are bounded by single-ended structures. As the preceding stages adopt a fully differential structure to suppress the even-order distortion, the output stage needs a differential to single-ended structure. The proposed buffer is a combination of a source follower and a common source amplifier. The input capacitors decouple ac signal swing from the input voltage level. Thus, the biasing condition is set by diode-connected transistors at the TX phase. This ensures that the output is biased at mid-supply. The input capacitance is chosen at 2 pF to minimize the leaking current.

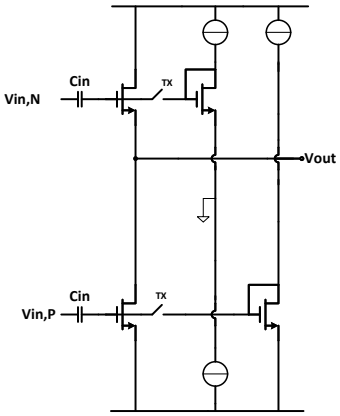
The gain of all four stages are separately designed to realize all design performance at the cost of minimal power consumption.

As the loop amplifier needs to achieve a 20-60 dB gain range in line with the feedback resistance, the gain of each stage must be carefully allocated. As stated in section 4.1.2, each variable-gain stage provides 20 dB gain variation by varying loads. The rest 20 dB constant gain is divided by all stages except the buffer. In principle, the first stage should have a 20 dB voltage gain for optimizing noise. Unfortunately, it cannot be realized due to the gm loads. Since the gain of the loop amplifier is only 20 dB, a 10 mV signal swing appears at the input, resulting in an amplified swing at the first stage output. The output swing of the first stage is limited to 50 mV. The first stage's voltage gain cannot exceed 14 dB.

Since the second and third stages have an overall 6 dB gain, the noise of these two stages will also affect the input noise voltage, implying a larger bias current for the first stage.



(a) The first stage with dynamic biasing (b) The intermediate stage with variable loads



(c) The buffer stage, differential to single-ended amplifier

Figure 4.8: Each stage of the proposed loop amplifier

To mitigate this effect, the second stage is designed to have more transconductance than that of the third stage. Because the thermal noise contribution of the second stage has a larger impact on the input noise level than that of the third stage.

Apart from noise optimization, bandwidth is another key factor to consider. The variable gain stages introduce two poles that move 20 dB within the bandwidth. Hence, the varying resistor value should be small enough to keep phase shift to a minimum. The varying resistances are different since the third stage pole sees less parasitic capacitance. Due to the higher resistance of the third stage load, the third stage requires less input gm. This concurs with the opinion that the second stage should have a larger gm.

4.1.4 Noise Optimization

As stated in section 3.4, the noise target of the loop amplifier is different at the high/low end of the gain range. At the highest gain, the input signal is quite small, thus a lowest noise target is aimed for minimal SNR degradation. In contrast, the input has the largest amplitude at the low end, so a large input noise level is acceptable. Given the noise specification of 1 $pA/\sqrt{Hz}$, the noise budget for the loop amplifier is $0.96pA/\sqrt{Hz}$ at the highest gain, excluding the noise contribution of a 200 $k\Omega$ feedback resistor. The converted input-referred noise voltage density is $1.15nV/\sqrt{Hz}$. While the noise target at the lowest gain is $120nV/\sqrt{Hz}$, which is far more achievable.

Considering the voltage gain of each stage, the noise contribution of the loop amplifier is mainly determined by the first stage, and partially dependent on the second stage. As shown in Fig.4.8(a)(b), the input-referred noise is mainly attributed to input pairs and the loads. Due to the small gain from the gate of cascode transistors to the output, the cascodes contribute little noise compared to the input devices. The current sources only contribute noise to the common mode, thus its differential noise is neglected.

There are mainly two kinds of noise contributed by the transistors: thermal noise and flicker noise. The thermal noise is calculated as follows[35] :

$$V_{n,thermal} = \sqrt{\frac{4kT\gamma}{g_m}} \tag{4.4}$$

Where k is the Boltzman constant, T is the kelvin temperature and γ is a process coefficient approximated 2/3 for long channel transistors. The determining factor is the transconductance g_m. To reduce thermal noise the transconductance must be increased.

Another noise source is the flicker noise, which is represented as[35]:

$$V_{n,1/f} = \sqrt{\frac{K}{C_{ox}WL \cdot f}} \tag{4.5}$$

Where K is a process-dependent constant, C_{ox} is the gate oxide capacitance and f is the frequency. The flicker noise is inversely proportional to $W \cdot L$, indicating the area is increased to reduce flicker noise. Therefore it is unsurprising to observe devices occupying a large area in low-noise applications. But it's worth noting that the increasing WL also increases gate capacitance, resulting in more parasitic capacitance. This may cause stability problems in secondary poles.

In summary, the noise of the first-stage and second-stage amplifiers is mainly optimized by the input pair and the diode-connected load. In order to achieve the maximum g_{m1} and g_{m1L}, the W/L ratio is tweaked to a large value for high power efficiency. Meanwhile, the flicker noise is also reduced by increasing the area. When the transistor is adjusted in weak inversion, the g_m/I_d is constant. At the higher gain, the bias current I_d must be increased to suppress the thermal noise. While at the lower gain, a large

noise level is targeted, so the I_d can be reduced, allowing for noise optimization in a power-efficient manner.

4.1.5 Nonlinearity

Multiple reasons can contribute to the non-linearity. The nonlinearity can originate from the output variation due to large swings or the small signal gain variation with the input level. Nonlinearity can be reduced by differential circuits as differential circuits produce no even harmonics. For this reason, the first three stages are fully-differential structures.

All the stages suffer from small signal gain variation, which is more pronounced in the third stage and the buffer. The third stage and the buffer have the largest output swing of 100 mV. This may reveal the non-linear behavior of the transistors, leading to odd-order harmonic distortions. Therefore, extra actions should be taken to mitigate the non-linear behavior of the transistors.

As for the buffer stage, the differential to single-ended structure is a dominant source of even-order harmonics. As shown in Fig.4.8(c) the signal path is different for positive input and negative input. To minimize the even harmonics, the transconductance of the input transistors should be as close as possible. Due to the input current, the drain current of the top NMOS device in the buffer shows a 50 μA deviation compared to the bottom NMOS device at the lowest gain. This unmatched transconductance leads to imbalanced gain for differential input. Again, solutions are needed.

The nonlinearity of the body effect is another source of even-order distortion. This appears in the feedback network as well as the buffer. For the feedback network, the dual configuration is used to cancel out even harmonics and only odd harmonics remain. With regard to the buffer, the body effect of the top NMOS will play a role in distortion if it's connected to the bulk of its bias transistor. This helps to save area in layout design. But the resulting distortion can not be ignored. Thus, the bulk of top NMOS is connected to its source, eliminating the body effect.

The nonlinearity caused by large signal swings can be resolved by extending the linear region of the transistors. By reducing the W/L ratio, the overdrive voltage of the input transistors is increased and thus the linear region is expanded. However, the bias current of the third stage is a bit improved to avoid voltage gain drop. For the buffer stage, as long as the low output impedance is obtained, the W/L ratio can be reduced.

Regarding the nonlinearity of the imbalance structure, the transconductance of the input transistors should be matched by increasing the DC current. Since the buffer and its bias network form two current mirrors, the DC current is copied from the bias network. The solution is to increase the current of the bias network. However, the price to pay is power consumption. If the constraint of the THD is not even harmonics, there's no reason to consume extra power.

4.1.6 Overall loop amplifier

The overall loop amplifier is shown in Fig.4.9. For simplicity, the input transducer, the load capacitor and the feedback network are not shown. The ramp voltage generator and the circuit implementations of the variable load resistor will be introduced in the next two sections.

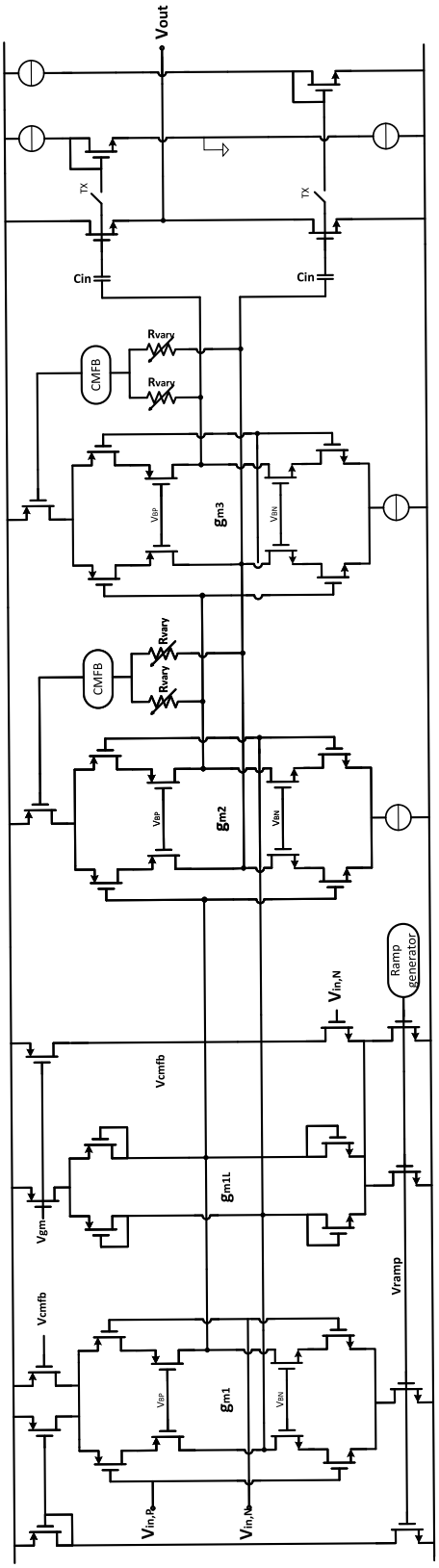


Figure 4.9: A schematic of the loop amplifier

4.2 Ramp voltage generator

The gain of the first stage amplifier is designed as a transconductance ratio. By varying the input transconductance and the load transconductance in the same manner, different input noise target is achieved. Thus, a ramp voltage to deliver a variable bias current is imperative.

In [11] a gm-control circuit is applied with an external ramp voltage V_{TGC} to deliver an exponentially varying bias current. Fig.4.10 shows the transistor-level circuit diagram. The $V_{ref,i}$, generated by means of a resistive ladder network, are compared with a ramp-down voltage V_{TGC}. When the V_{TGC} decreases to a certain level, the tail currents from the constant current sources are steered into the varying bias source.

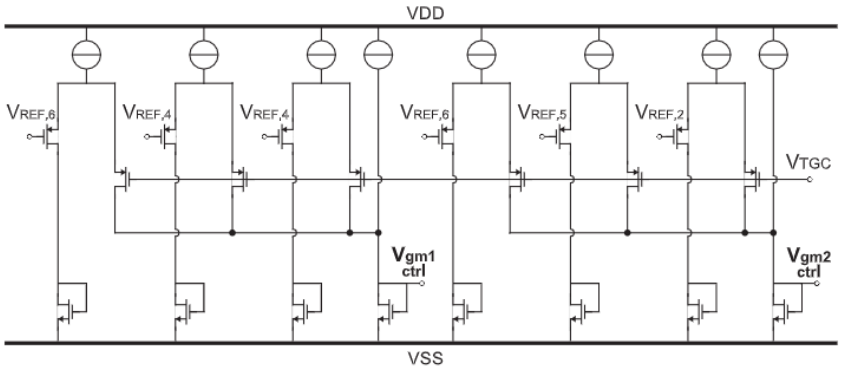


Figure 4.10: Circuit diagram of transconductance control circuit

This topology is not preferred for the following reasons. First, it requires extra circuits to generate ramp voltage and reference voltages. Second, the tail current sources are not fully utilized by the variable bias source, implying low power efficiency. Last but not least, when increasing transconductance is all that is needed, this circuit provides exponentially increasing transconductance, meaning an overdesign.

Therefore, a ramp voltage generator is designed to create an increasing transconductance for the first stage. As shown in Fig.4.11, the circuit consists of a pre-charged capacitor C_1 and a linear discharge MOSFET-C network. The two diode-connected loads are biased at different levels to provide initial voltages for C_1 and V_{ramp}, respectively. At the TX phase, all three switches are connected as C_1 and C_2 are pre-charged to inital voltage levels. At the RX phase, the voltage on C_1 remains while the voltage drop on C_2 is reduced as a constant current is drawn into the transistor in the saturation region. By setting proper bias points and discharge current, the voltage range of V_{ramp} is controllable. The simulated ramp voltage is shown in Fig.4.12.

This topology has several advantages. First, the circuit is simple as no external circuit is required. Second, the power efficiency of this circuit is quite high as the power consumption for the bias network is low.

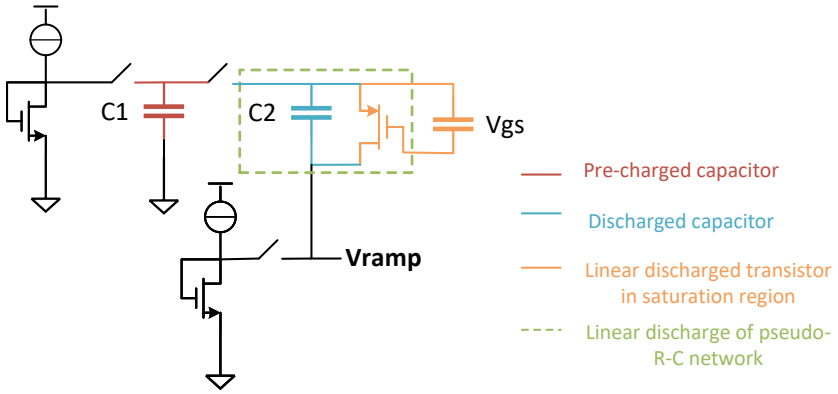


Figure 4.11: Circuit diagram of the ramp voltage generator

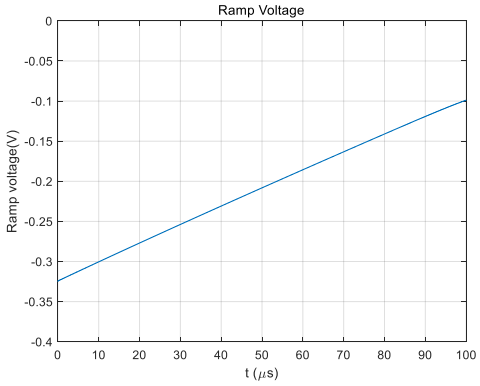


Figure 4.12: The ramp voltage as a function of time

4.3 Variable load resistance

The variable load resistors are utilized in the intermediate two stages, with each providing 20 dB gain. For intrinsic gain matching between the gain of the loop amplifier and the feedback resistance, the same topology is chosen to design varying load resistance.

As seen in Fig.4.13, the load resistor consists of three parallel branches of dual triode devices and the corresponding control voltage generator. Two branches are sufficient for achieving the 20 dB gain range. But three branches are chosen for more perfect gain matching. As shown in Fig.3.8, at gain switching moments the real gain curve shows the largest deviation from the ideal dB-linear curve. Such a pattern should also be seen in the gain of the load resistance. Therefore, three branches are utilized.

For simplicity, the control voltage generator are identical to that of the feedback network. The 2.5 pF discharging capacitor, 1 pF precharged capacitor as well as the same discharge transistor are adopted. To customize the discharge current, the precharged gate-source voltage is selected individually.

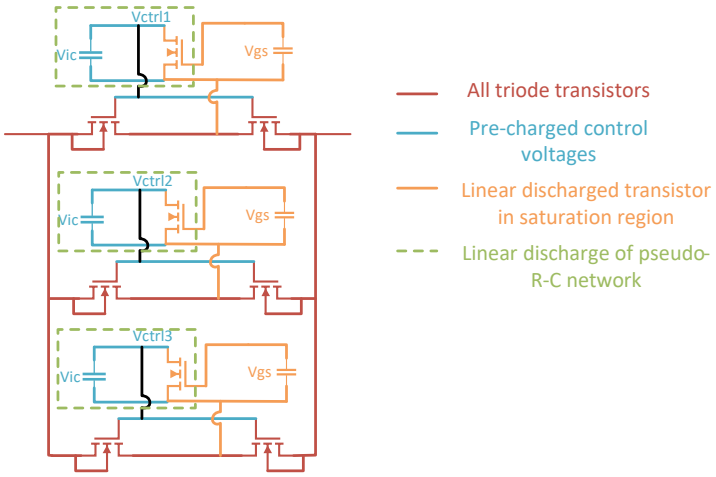


Figure 4.13: A schematic of the variable load resistor

The load resistance values should be carefully chosen among the trade-off between power and bandwidth. As stated in section 4.1.3, the second stage requires higher transconductance than the third stage to achieve the noise target. Besides, the phase margin is mainly affected by the output pole of the second stage. Therefore, the load resistor in the second stage is designed lower at 2.5 $k\Omega$. While for the third stage the power can be saved by decreasing the tail current, implying a larger load resistance. The third stage load is set at 10 $k\Omega$ at the highest gain.

5 Performance

Given the overall circuit implementation of the proposed TIA, the validation of its operation is required. In this chapter, the simulated results of all metrics are illustrated and evaluated by comparing them to the design specifications listed in table 1.1.

5.1 AC response

To verify the validity of this amplifier ac closed-loop simulation is carried out. Fig.5.1 shows the closed-loop gain of the proposed TIA. Since the transimpedance gain shifts over time, it is necessary to inspect the gain at each time interval. Over the receiving period of 100 μs, the closed-loop DC gain varies from 66 to 106 dBΩ, meaning the overall 40 dB gain range is obtained.

To meet the gain range requirement within the bandwidth of interest, the closed-loop bandwidth is at least larger than the bandwidth of interest. Since the transducer operates with 5-10 MHz, the -3 dB bandwidth should be larger than 10 MHz. It can be observed that the -3 dB bandwidth is larger than 10 MHz. The closed-loop gain does not show any degradation over the bandwidth of interest.

From Fig.5.2 the closed-loop bandwidth is around 50 MHz, which is much larger than the band of interest. The -3 dB shows minor variation as a function of gain. This is expected due to the gain mismatch between the dominant pole and loopgain. But this variation does not comprise the closed-loop gain, therefore, the gain range target is satisfied in the closed-loop configuration.

The closed-loop bandwidth variation is owing to the non-negligible output impedance. Since a zero at the closed-loop curve is regarded as a pole in the loopgain curve, we can see that the closed-loop has a zero at $\frac{1}{C_{TD}(R_{fb}+R_L)}$. At the lowest gain, the output impedance is not insignificant compared to the feedback resistor, so the variation of the zero is less than 40 dB. This mismatch leads to a varying closed-loop bandwidth.

5.2 Stability

A gain-independent unity gain bandwidth is crucial for the stability of the loop. The loop amplifier is designed to have a varying gain that matches the varying dominant

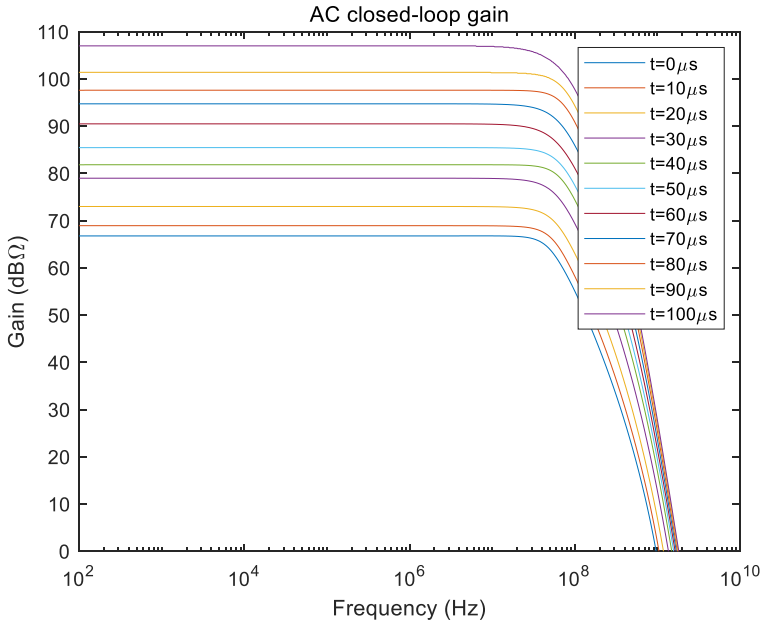


Figure 5.1: The closed-loop gain at different gain settings

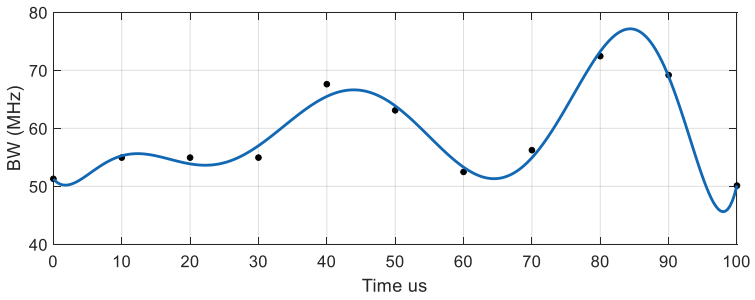


Figure 5.2: -3dB bandwidth as a function of gain

pole to deliver a constant UGBW. From Fig.5.3, it can be concluded that the UGBW is almost constant as the dominant pole shifts as a function of gain. Since the variable gain in the loop amplifier is achieved by varying load resistance, at higher gain settings the phase margin shows variation due to the secondary poles.

The phase margin and unity-gain bandwidth at different gains are shown in Fig.5.4. The phase margin degrades a little at the higher gain as expected, but it stays above 60 degrees. Therefore, the stability of this loop is ensured.

The UGBW varies from 29 MHz to 42 MHz over the whole receive period, deviating from an ideally constant UGBW. This can be attributed to the fact that the dominant pole varies less than 40 dB. Given the dominant pole equation $s = \frac{1}{(R_{fb}+R_{out})C_{TD}}$ and the R_{out} resistance of 500 Ω, it can be computed that the dominant pole shifts by 38 dB while the loopgain varies by 40 dB. The solution is to decrease the R_{out} at the

expense of more power consumption. From the perspective of high power efficiency, this solution is not accepted.

Another source comes from the gain mismatch between the R_{vary} and R_{fb}. Since they both employed the same structure (shown in Fig.4.13) the gain mismatch is minimized. Regardless of the R_{out}, the UGBW is considered a gain-independent UGBW.

The gain margin and the gain margin frequency are shown in Fig.5.4. At different gain settings, the gain margin stays below -14 dB, once again verifying the LNA's stability.

Comparing the unity gain frequency and the closed-loop bandwidth, it's surprising to find that the closed-loop bandwidth is larger than the unity gain bandwidth. The decompensated op-amp accounts for this effect. When the open loop gain is unity gain, the opamp becomes unstable due to the input pole and output pole. The opamp is only stable at a higher closed-loop gain, where the opamp open-loop gain drops to 0 dB before the second pole. The unity gain frequency is the crossover point of the open-loop gain and the closed-loop curve. But due to the existence of the second pole, the role-off rate is greater than 20 dB/dec, resulting in smaller unity gain frequency compared to the gain-bandwidth product. Therefore, the closed-loop bandwidth is always larger than the unity gain bandwidth.

Another factor is the finite gain of the opamp.Ideally, when the output impedance is omitted, the dominate pole of the loopgain is $\frac{1}{R_{fb}C_{TD}}$ and the unity frequency is $\frac{A}{R_{fb}C_{TD}}$. While the closed-loop bandwidth is $\frac{1+A}{R_{fb}C_{TD}}$, leading to 10% higher bandwidth at 20 dB loopgain.

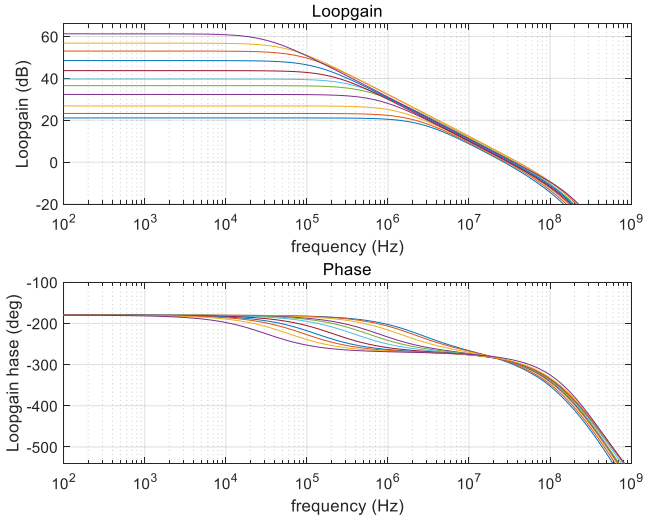


Figure 5.3: Loopgain and Loopgain phase at different gain

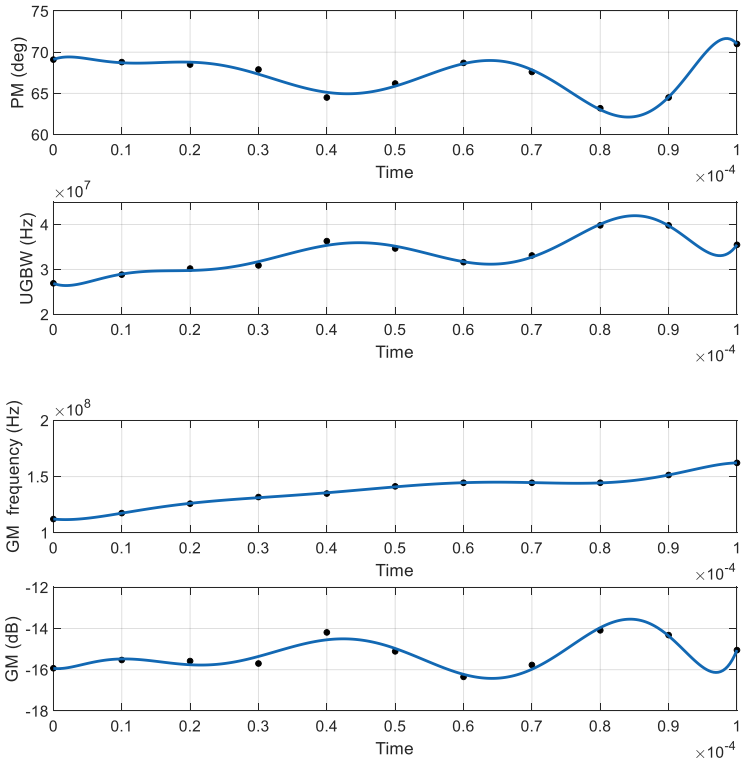


Figure 5.4: Phase margin and gain margin

5.3 Transient response

To assess the transient response of the LNA, the transient performance in the whole receive period should be looked into. To verify the time gain compensation functionality, the simulation should test the output amplitude given a dB-linear decaying current source as input. The input current is a 7.5 MHz sinusoidal signal with amplitude varying from 50 μA to 0.5 μA. The output should deliver a constant envelope of 100 mV, while in Fig.5.5 the output amplitude varies between 85-112 mV.

From the result of Fig.5.5, the following two conclusions can be drawn. First, for 40 dB input dynamic range, the output remains constant and the overall DR equals the instantaneous DR. This validates the time gain compensation. However, the output amplitude shows certain variations, deviating from an ideal constant envelope. This is due to the gain error in the feedback network. Firstly, the gain deviates from the ideal gain curve at the gain-switching moments because of the parallel structure. Secondly, the control voltage generator does not deliver a dB-linear voltage. As shown in Fig.3.8, the control voltage is linearly discharged because a Mosfet in the saturation region is used as a resistor. The gain deviation could be minimized with real resistors, but it results in large area consumption.

Another observation is the recurring output amplitude variation. The output voltage shows three variations at the gain switching moments, which corresponds to the three branches in the feedback network. Since each branch dominates the gain in its individual time interval, the switching between two branches would cause certain gain error. This can be minimized by employing more branches.

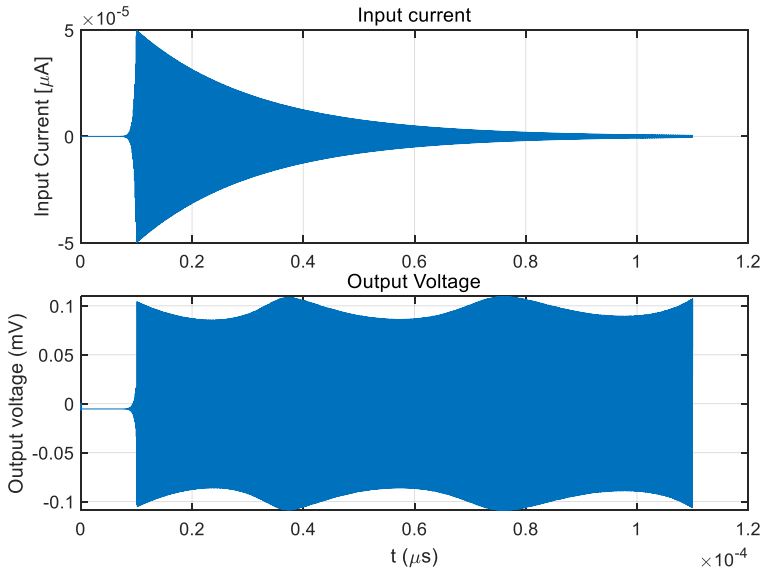


Figure 5.5: Transcient response of the input and output

5.4 Gain error and Nonlinearity

To evaluate the accuracy of this time gain compensation, the gain error is computed by comparing the transimpedance gain of the TIA with the ideal gain curve. In Fig.5.6 such a comparison is made and the computed gain error is ±1 dB. This gain error is acceptable as it could be corrected by digital post-processing.

In view of the dynamic range, the overall DR should be reduced by 40 dB with an ideal time gain compensation. But with this LNA, the overall DR is only reduced by 38 dB. The dynamic range reduction is 2 dB less than ideal, but it is still sufficient for the following ADC to handle the signal without SNR degradation.

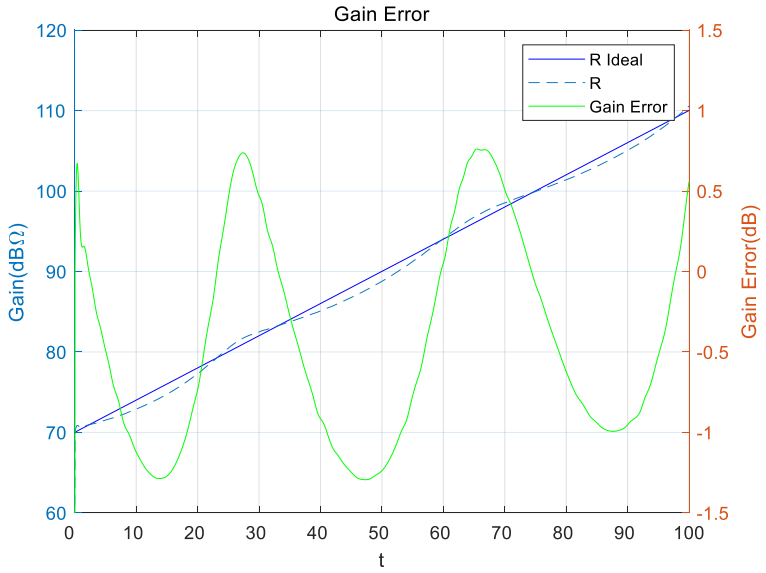


Figure 5.6: Gain error

Except for the gain error, the linearity of this LNA is a key factor that influences the overall performance. Even if all other performance metrics meet the requirements, the amplifier does not work properly without acceptable signal distortion. The linearity requirement is that the THD stays below -40 dB.

Fig.5.7 demonstrates the output spectrum of different gain settings. The HD1 is the fundamental, representing the 100 mV output voltage. It can be observed that the limiting factor of THD is HD2 and HD3. HD2 results from the imbalance structure of the buffer stage, which could be minimized by increasing the input transconductance. HD3 is mainly caused by the insufficient linear region of the input transistors. The detailed measures are introduced in section 4.1.5.

The total harmonic distortion is shown in Fig.5.8. The THD stays below -40 dB during the whole receive period, which meets the linearity requirements.

It can be concluded that the THD is the worst at the lowest gain. At the lowest gain,

the loopgain is also the lowest, thus the AC ground is no longer virtue AC ground, but with an input signal swing. The signal swing is amplified and an even larger swing appears at later stages. Thus, the operating regions of the later stages do not cover for the larger swing, leading to the non-linear characteristics of the Mosfets. While the THD behaves better at the higher end of the gain range due to the increased loopgain.

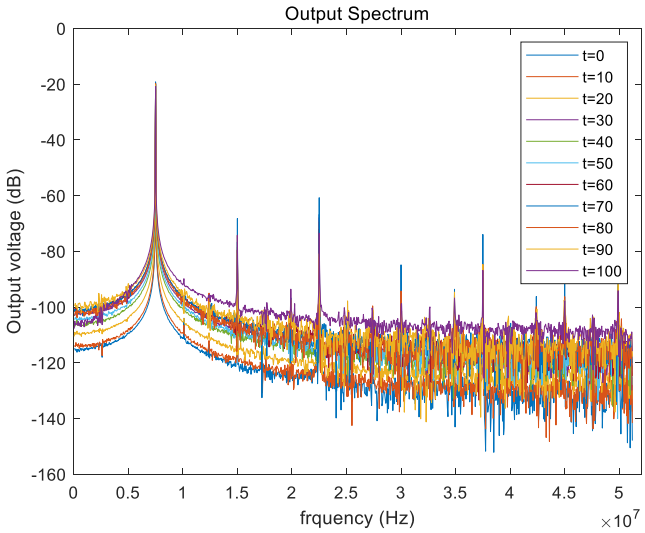


Figure 5.7: Harmonic Distortion

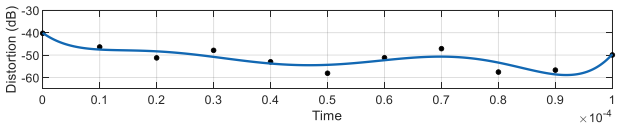


Figure 5.8: The total harmonic distortion as a function of gain

5.5 Noise performance

Apart from the time gain compensation function, low noise is another critical target of this design. The noise target is 1 $pA/\sqrt{Hz}$ at 7.5 MHz for the highest gain setting. The simulated input-referred current density is 1.15 $pA/\sqrt{Hz}$ at 7.5 MHz for the highest gain setting, which almost meets the noise target.

Fig.5.9 shows the input and output referred noise density. It can be observed that the input-referred noise current density is higher at the lower end of the gain range. This does not degrade SNR performance since the signal is inversely proportional to the feedback resistance and the input-referred noise is inversely proportional to the square

root of the feedback resistance. Thus, the SNR increases as the gain reach the low end.

Fig.5.10 shows the SNR performance of the proposed LNA. The input current is the ideal decaying current and the current noise density is computed by integrating the simulated input-referred noise over the bandwidth. The simulated SNR at the lowest gain is 42.8 dB. The SNR of the input transducer is 44 dB at the highest gain. The two SNR is comparable to each other, suggesting the noise power of the LNA is similar to the noise power of the transducer. When computing both noise of the transducer and the LNA, the overall SNR is 40.3 dB. The SNR degradation is 3.7 dB due to the employment of LNA. This result is reasonable since the noise target will cause 3 dB SNR degradation.

The noise performance could be further improved by increasing the bias current of the first stage, resulting in more power consumption.

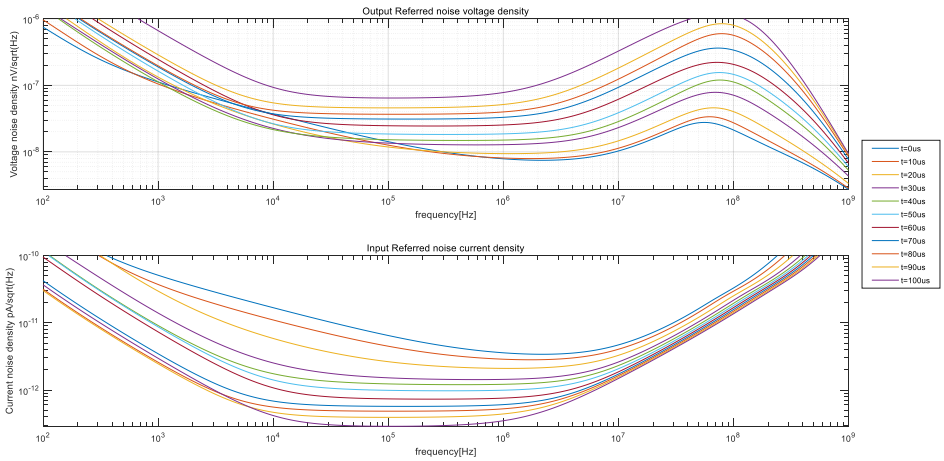


Figure 5.9: Output and input referred noise density

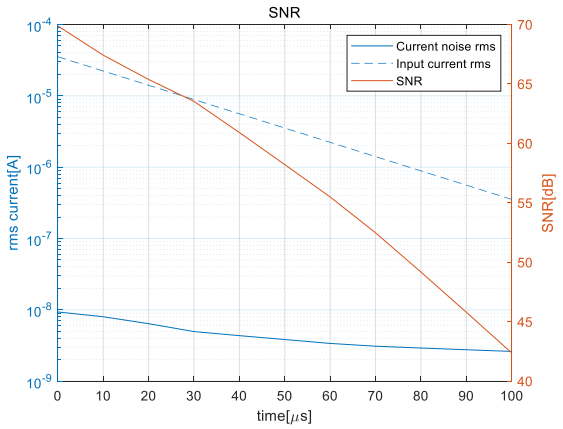


Figure 5.10: The SNR of the proposed LNA

5.6 Power

The proposed LNA meets all performance specifications. But power consumption plays an important role in assessing the noise efficiency of this design, which should not be overlooked. The instantaneous and average power consumption is shown in Fig.5.11, and the average power consumption is computed by integrating the instantaneous power consumption before averaging it in the whole receive period.

It can be seen that the instantaneous power consumption is increasing linearly as a function of time. The result is consistent with what is expected as the first stage bias current is increased in a linear manner. Besides, the instantaneous power consumption shows a sinusoidal behavior. The sinusoidal drain-source current in the buffer stage accounts for this behavior.

The computed average power consumption is 6 mW, which is a bit higher than the 5.2 mW presented in [11]. But it is comparable to the 5.5 mW in [12], with the advantage of a 1 pF load-driving capability.

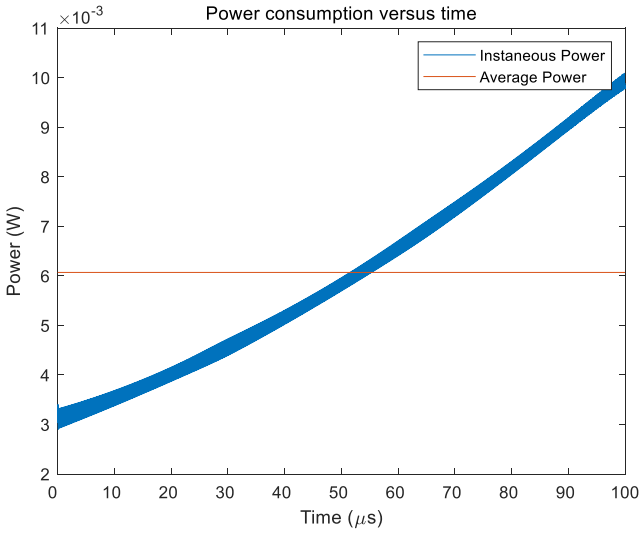


Figure 5.11: The power consumption of the proposed LNA in the whole receive period

Fig.5.12 shows the power dissipation percentage of the LNA. The loop amplifier is the dominant power consumer. While the power consumption of the biasing network for the feedback resistor and the load resistor is considered negligible since the voltage sources are only used to precharge the capacitors.

The first stage consumes most of the power as expected, so as to achieve the noise target at the highest gain. The second stage consumes the second most of the power such that the second stage has a lower noise contribution compared to the first stage. The power of the third stage is dissipated to suppress the non-linearity due to the large signal swing at the lowest gain setting. At last, the buffer requires power to drive the

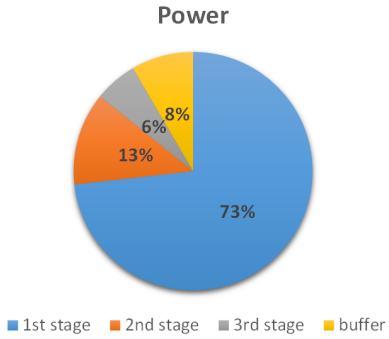


Figure 5.12: The power dissipation of the LNA

load capacitor.

When comparing the power consumption with [12], it is crucial to compare the power efficiency in terms of the low noise performance. [12] and this design share the same noise target, thus the power dissipated in the first stage can be compared. The varying bias current in [12] shifts from 1 mA to 6 mA in the whole receive period, while in Fig.5.13 the bias current of this design is almost halved, implying the power efficiency of the first stage is almost doubled. The current reuse topology accounts for this high power efficiency.

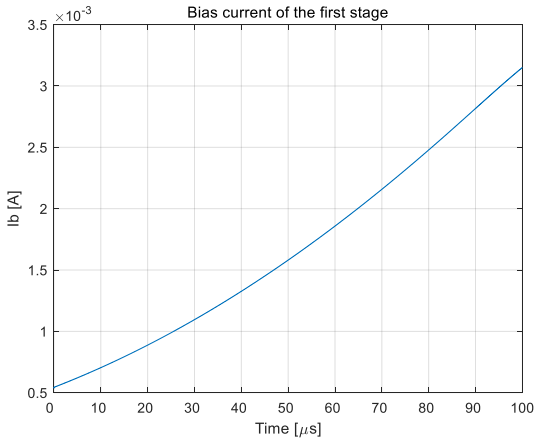


Figure 5.13: The first stage bias current of this design

5.7 Area

The area estimation is made regarding the transistor dimensions and overall capacitance used in a single LNA channel. The bias network is also included.

Based on the auto layout, the channel area required for the transistors is about 30000

μm^2. This includes the channel area and the area used for source and drains connections, but interconnection is excluded. Assuming a 30% margin of error, the per channel area is about 33000 μm^2.

As illustrated in section 3.3.3 the overall capacitance of 10.5 pF is required for a three-branch feedback network. The variable load resistor adopts the same structure so the capacitance is also 10.5 pF. Including the 2 pF input capacitance of the buffer, the overall capacitance is 56.5 pF. Given that 1 pF MIM capacitance occupies 500 μm^2, the total area consumed by capacitors is 28250 μm^2. Assuming a 20 % budget for shielding the capacitors and interconnect, the estimated area is 33900 μm^2 in terms of the MIM capacitors.

The total area depends on the placement of the transistors and capacitors. The first approach is to place them adjacent to each other, resulting in an area of 66900 μm^2. The other method is to stack the MIM capacitors on top of the transistors to reuse the die area. In this way, the total area is reduced to 33900 μm^2, which is dominated by the MIM capacitors. In terms of minimal area, the second approach is favored.

Compared to [11], the LNA per channel area is greatly reduced due to the resistive feedback network. But the area is more than 2X higher than [12] as a consequence of variable load resistive network.

6 Conclusion

In this chapter, the performance metrics of this design are summarized and compared with the prior art. The results shed light on the improvement methods and future works.

6.1 Conclusion

This thesis has presented a low noise transimpedance amplifier with a time gain compensating function. The proposed LNA obtains 40 dB gain range with ± 1 dB gain error during the 100 μs receive period. The LNA achieves a noise target of 1.15 $pA/\sqrt{Hz}$ and suppresses the THD below -40 dB. Based on 0.18μm CMOS technology, the LNA occupies an estimated area of 0.0339 μm^2 and consumes 6 mW power from a $\pm 0.9V$ supply.

The realization of the LNA and the TGC function is by means of a closed-loop structure. This allows for an individual design for the feedforward and feedback paths. The feedback path is a resistive network consisting of parallel back-to-back triode transistors. As the control voltages decreases at different rates, each branch in the resistive network dominates in part of the gain range. A capacitor linear discharge network is applied to mimic the exponential control voltage. This small circuit contributes little noise and prevents correlated noise among different channels.

The feedforward path comprises a four-stage loop amplifier, optimized for noise requirements in a power-efficient manner. Many trade-offs are made between stability, noise, power, driving capacity and fixed UGBW. The loop amplifier adopts a current reuse topology and adaptive biasing for the first stage to increase power efficiency. Compared to [12], when targeting the same noise level, the power efficiency is doubled. For driving capability, the loop amplifier designed a buffer as the output stage. The output impedance is so low that the DC gain of the loop amplifier also needs to vary by 40 dB to obtain a fixed UGBW. This is realized by intrinsic gain matching between the variable internal resistors of the loop amplifier and the feedback resistor. Compared to [12], the UGBW shows limited variation. The gain error within the 40 dB gain range is also reduced to ± 1 dB, meaning the dynamic range reduction rises to 38 dB.

As shown in Table 6.1, the performance metrics are listed with comparison to the prior art. As the same transducer is used in [11, 12], this design can be compared in the same dimension. Compared to [11], the die area is reduced by 3X and a lower noise target is

met at the cost of a bit higher power consumption. Comparing with [12] the gain error is minimized and the UGBW variation is reduced at the cost of almost 3X larger area. Similar noise performance is obtained with competitive power consumption while the driving capability is improved.

Table 6.1: Performance comparison with the Prior Art

	Performance specification	[11]	[12]	[13]	[14]
Process	0.18 μm CMOS	0.18μm HV BCDMOS	0.18 μm CMOS	0.18μm HV BCDMOS	0.18μm HV CMOS
Topology	TIA	TIA	TIA	TIA	TIA
TGC type	purely exponential	ITP	Purely expoential	ITP	DT
−3-dB(MHz)	50	7.1	20	17.5	10
Max gain(dBΩ)	106	107	100	102	116
Gain range(dB)	40	33	40	36	12
Gain error(dB)	±1	±1	±1.4	±0.4	±3
TD Capacitance (pF)	18	15	18	1	2
Input referred noise density ($pA/\sqrt{Hz}$)	1.15@7.5MHz	1.7@5MHz	1.12@7.5MHz	1.31@10MHz	0.41@5MHz
Power consumption(mW)	6	5.2	5.5	0.8	1.4
Area/ch.(mm^2)	0.0339	0.12	0.013	0.025	0.028
NEF[1]$mP \cdot \sqrt{(mW/Hz)}$	0.84	0.78	0.8	**	2.7

[1] $NEF = P_{n,in} \cdot \sqrt{POWER_{tot}}$[14], $P_{n,in}$is the input-referred acoustic pressure noise spectral density averaged in passband

6.2 Future Works

This design has been verified by means of circuit simulations. The layout and post-layout simulation are still required for a prototype. Before manufacturing the prototype, corner simulations are of vital importance. The loop needs to satisfy the target specification over the PVT variations. At the moment the exponential voltage generator is biased by constant voltage sources, implying the system is sensitive to gain variation. A bias circuitry remains to be designed for the control voltage generator.

There is still room for improvement on this design. First, the gain error could be optimized by adding more branches to the network. As stated earlier, the gain error reaches its maximum at the gain-switching moments. More branches could smoothen out the gain curve and reduce the gain error. But it leads to the inevitable increased die area.

The second optimization targets for distortion issues. The worst THD happens at the largest signal swing. A linearization technique is required to reduce the dependence of circuit's gain upon input levels. Source degeneration and a local feedback network can be applied to the third stage to improve the linearity.

In terms of area estimation, the capacitors in the RC discharge network could be further reduced if the mismatch due to the charge injection is acceptable. Even if there are certain errors caused by the inaccurate discharge current or leaking current, it does not lead to SNR degradation so long as the gain error is tolerable. Besides, the area of the discharge networks in the loop amplifiers can be reduced compared to that in the feedback network. Because a slow varying UGBW does not compromise the performance.

In terms of power consumption, the power efficiency of the first stage could be further improved. The variable bias current of the first stage is linearly increased, but it could be an exponential curve or a parabola function with fixed instantaneous transconduc-

tance at the highest gain. Thus, power consumption can be minimized even further.

Bibliography

[1] "Cardiovascular diseases," No. I00-I99, 2020. World Health Organization Database.

[2] J. J. Kastelein and E. de Groot, "Ultrasound imaging techniques for the evaluation of cardiovascular therapies," *European heart journal*, vol. 29, no. 7, pp. 849–858, 2008.

[3] K. K. Shung, *Diagnostic ultrasound: Imaging and blood flow measurements*. CRC press, 2005.

[4] M. Shabanimotlagh, *Ultrasound Matrix Transducers for High Frame Rate 3D Medical Imaging*. PhD thesis, Delft University of Technology, 2018.

[5] T. L. Szabo, "Chapter 1 - introduction," in *Diagnostic Ultrasound Imaging: Inside Out (Second Edition)* (T. L. Szabo, ed.), pp. 1–37, Boston: Academic Press, second edition ed., 2014.

[6] C. Chen and M. A. P. Pertijs, "Integrated transceivers for emerging medical ultrasound imaging devices: A review," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 104–114, 10 2021.

[7] G. Jung, C. Tekes, M. W. Rashid, T. M. Carpenter, D. Cowell, S. Freear, F. L. Degertekin, and M. Ghovanloo, "A reduced-wire ICE catheter ASIC with TX beamforming and RX time-division multiplexing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 6, pp. 1246–1255, 2018.

[8] C. Chen, Z. Chen, D. Bera, S. B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z. Y. Chang, J. Ponte, C. Prins, H. J. Vos, J. G. Bosch, M. D. Verweij, N. D. Jong, and M. A. Pertijs, "A front-end ASIC with receive sub-array beamforming integrated with a 32 $\times$ 32 PZT matrix transducer for 3-D transesophageal echocardiography," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 994–1006, 4 2017.

[9] D. Wildes, W. Lee, B. Haider, S. Cogan, K. Sundaresan, D. M. Mills, C. Yetter, P. H. Hart, C. R. Haun, M. Concepcion, J. Kirkhorn, and M. Bitoun, "4-D ICE: A 2-D array transducer with integrated ASIC in a 10-fr catheter for real-time 3-D intracardiac echocardiography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 12, pp. 2159–2173, 2016.

[10] M. O. Culjat, D. Goldenberg, P. Tewari, and R. S. Singh, "A review of tissue substitutes for ultrasound imaging," *Ultrasound in medicine & biology*, vol. 36, no. 6, pp. 861–873, 2010.

[11] E. Kang, M. Tan, J. S. An, Z. Y. Chang, P. Vince, N. Sénégond, T. Mateo, C. Meynier, and M. A. Pertijs, "A variable-gain low-noise transimpedance amplifier

for miniature ultrasound probes," *IEEE Journal of Solid-State Circuits*, vol. 55, pp. 3157–3168, 12 2020.

[12] J. Tams, "A combined time-gain compensation low-noise amplifier for ultrasound imaging applications," Msc thesis, Delft University of Technology, 11 2020.

[13] P. Guo, Z. Y. Chang, E. Noothout, H. J. Vos, J. G. Bosch, N. D. Jong, M. D. Verweij, and M. A. Pertijs, "A pitch-matched analog front-end with continuous time-gain compensation for high-density ultrasound transducer arrays," pp. 163–166, Institute of Electrical and Electronics Engineers Inc., 9 2021.

[14] K. Chen, H.-S. Lee, and C. G. Sodini, "A column-row-parallel ASIC architecture for 3D wearable / portable medical ultrasonic imaging," in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 1–2, 2014.

[15] *"VCA 2617"*, Aug, 2005. Texas Instrument Dallas TX USA Datasheet.

[16] Z. Yu, S. Blaak, Z. Y. Chang, J. Yao, J. G. Bosch, C. Prins, C. T. Lancee, N. D. Jong, M. A. Pertijs, and G. C. Meijer, "Front-end receiver electronics for a matrix transducer for 3-D transesophageal echocardiography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 59, pp. 1500–1512, 2012.

[17] C. Chen, Z. Chen, D. Bera, E. Noothout, Z.-Y. Chang, M. Tan, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, "A pitch-matched front-end ASIC with integrated subarray beamforming adc for miniature 3-D ultrasound probes," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3050–3064, 2018.

[18] Y. Wang, M. Koen, and D. Ma, "Low-noise CMOS tgc amplifier with adaptive gain control for ultrasound imaging receivers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 1, pp. 26–30, 2011.

[19] C. Chen, S. B. Raghunathan, Z. Yu, M. Shabanimotlagh, Z. Chen, Z.-y. Chang, S. Blaak, C. Prins, J. Ponte, E. Noothout, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, "A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 1, pp. 47–59, 2016.

[20] M. Tan, C. Chen, Z. Chen, J. Janjic, V. Daeichin, Z. Y. Chang, E. Noothout, G. V. Soest, M. D. Verweij, N. D. Jong, and M. A. Pertijs, "A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 2284–2297, 8 2018.

[21] M.-C. Chen, A. Peña Perez, S.-R. Kothapalli, P. Cathelin, A. Cathelin, S. S. Gambhir, and B. Murmann, "A pixel pitch-matched ultrasound receiver for 3-D photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, 2017.

[22] H. Elwan, A. Tekin, and K. Pedrotti, "A differential-ramp based 65 dB-linear VGA technique in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2503–2514, 2009.

[23] H. H. Nguyen, H. N. Nguyen, J. S. Lee, and S. G. Lee, "A binary-weighted switching and reconfiguration-based programmable gain amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, pp. 699–703, 2009.

[24] X. Song, Z. H. Lu, and X. P. Yu, "An accurate dB-linear CMOS VGA based on double duplicate biasing technique," *IEEE Solid-State Circuits Letters*, vol. 1, pp. 98–101, 4 2018.

[25] H. Liu, X. Zhu, C. C. Boon, and X. He, "Cell-based variable-gain amplifiers with accurate dB-linear characteristic in 0.18 μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 586–596, 2 2015.

[26] Q. H. Duong, Q. Le, C. W. Kim, and S. G. Lee, "A 95-dB linear low-power variable gain amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, pp. 1648–1657, 2006.

[27] Q.-H. Duong and S.-G. Lee, "86 dB 1.4 mW 1.8 V 0.07 mm^2 single-stage variable gain amplifier in 0.18 μm CMOS," *Electronics Letters*, vol. 43, no. 1, pp. 19–21, 2007.

[28] H. D. Lee, K. A. Lee, and S. Hong, "A wideband CMOS variable gain amplifier with an exponential gain control," vol. 55, pp. 1363–1373, Institute of Electrical and Electronics Engineers Inc., 2007.

[29] H. Elwan, A. Tekin, and K. Pedrotti, "A differential-ramp based 65 dB-linear VGA technique in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2503–2514, 9 2009.

[30] B. R. Veillette, "Variable gain current amplifier with a feedback loop including a differential pair," Sept. 28 2004. US Patent 6,798,291.

[31] E. Brunner, "An ultra-low noise linear-in-dB variable gain amplifier for medical ultrasound applications," in *Proceedings of WESCON'95*, pp. 650–, 1995.

[32] B. Gilbert, "A low-noise wideband variable-gain amplifier using an interpolated ladder attenuator," in *1991 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pp. 280–281, 1991.

[33] Y. Tang, Y. Feng, Q. Fan, C. Fang, J. Zou, and J. Chen, "A wideband complementary noise and distortion canceling LNA for high-frequency ultrasound imaging applications," pp. 1–4, Institute of Electrical and Electronics Engineers Inc., 6 2018.

[34] Y. Tang, Y. Feng, Q. Fan, R. Zhang, and J. Chen, "A current reuse wideband LNA with complementary noise and distortion cancellation for ultrasound imaging applications," pp. 171–174, Institute of Electrical and Electronics Engineers Inc., 1 2019.

[35] B. Razavi, *Design of Analog CMOS Integrated Circuits.* Electrical Engineering Series, McGraw-Hill, 2001.

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