# A SOLID-STATE TRANSFORMER FOR INTERCONNECTION BETWEEN THE MEDIUM- AND THE LOW-VOLTAGE GRID

DESIGN, CONTROL AND BEHAVIOR ANALYSIS

DELFT UNIVERSITY OF TECHNOLOGY ELECTRICAL ENGINEERING, MATHEMATICS AND COMPUTER SCIENCE ELECTRICAL POWER PROCESSING

> MASTER OF SCIENCE THESIS REPORT ANIEL SHRI



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**Challenge the future** 

## A SOLID-STATE TRANSFORMER FOR INTERCONNECTION BETWEEN THE MEDIUM- AND THE LOW-VOLTAGE GRID

Design, Control and Behavior Analysis

By

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### ABSTRACT

In recent years the complexity of the grid systems has grown due to the increased penetration of renewable energy and distributed generation sources. The increased complexity requires new methods to quickly manage the changing sources and loads. This research focuses on one of such technologies, called the Solid State Transformer (SST).

A SST uses power electronic devices and a high-frequency transformer to achieve isolation and voltage conversion from one level to another. Several SST topologies have been proposed by different research groups, without a clear consensus on which is most suited for grid applications. To ensure a proper choice of topology, a separate literature review is presented in this thesis. The final choice of topology is extremely modular and can be expanded to any voltage and power level.

A first order design is made based on this topology for quantitative research. In order to reduce computation times during simulations, the SST circuit is reduced to an averaged model. After development of the averaged model, the controller for the different parts of the SST is designed. The averaged model of the SST along with its controller is then placed in several grid scenarios to investigate its behavior. These simulations show satisfactory behavior of the SST under both normal operation and disturbances.

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## LIST OF SYMBOLS

Symbol	Description		
$\overline{x}$	Average value of x		
<i>x</i>	Small-signal value of x		
C <sub>3P4L</sub>	DC-link capacitor for the 3P4L converter		
C <sub>CHB</sub>	CHB DC-link filter		
C <sub>DAB1</sub>	DAB capacitor on the side of the CHB		
C <sub>DAB1</sub> Sum of C <sub>CHB</sub> and C <sub>DAB1s</sub>			
C <sub>DAB2s</sub> DAB capacitor on the 3P4L converter side			
C <sub>f-3P4L</sub> 3P4L filter capacitor			
d Average switching function, also defined as the duty cycle			
D <sub>DAB</sub> (Quiescent) duty cycle of the DAB			
d <sub>DAB</sub>	DAB duty cycle		
d <sub>k-3P4L</sub>	3P4L duty cycle for phase-leg k		
d <sub>kj-CHB</sub> Duty cycle in the j <sup>th</sup> module of the CHB in of the k <sup>th</sup> phase			
f frequency			
f <sub>CHB</sub>	CHB switching frequency		
<b>f</b> <sub>CHB</sub> -effective	Effective CHB switching frequency		
f <sub>DAB</sub>	DAB switching frequency		
f <sub>DAB</sub>	DAB switching frequency		
f <sub>grid</sub>	Grid frequency		
G <sub>id-boost-DAB</sub>	DAB control-to-output-current for boost mode		
G <sub>id-buck-DAB</sub>	DAB control-to-output-current for buck mode		
G <sub>idd-3P4L</sub>	3P4L converter control-to-output-current transfer function for the d-frame		
G <sub>idd-CHB</sub>	CHB control-to-output-current transfer function for the d-frame		
G <sub>idq-3P4L</sub>	<u>3P4L converter control-to-output-current transfer function for the q-frame</u>		
G <sub>idq-CHB</sub>	CHB control-to-output-current transfer function for the q-frame		
G <sub>idz-3P4L</sub>	3P4L converter control-to-output-current transfer function for the z-frame		
G <sub>vd-3P4L</sub>	LV-side grid-voltage-to-duty-cycle transfer function		
G <sub>vi-boost-DAB</sub>	DAB output-current-to-DC-ink-voltage for buck mode		
G <sub>vi-buck-DAB</sub>	2DAB output-current to DC link voltage transfor function		
G <sub>vid-3P4L</sub>	CHR output current to DC link voltage transfer function		
G <sub>vid-CHB</sub>	PL-companyator for the DAB boost mode current-loop		
H	PI-compensator for the DAB buck mode current-loop		
H. L. C. C. L.	PI-compensator for the d-frame single module CHB current-loop		
H.11 cr.	PL-compensator for the 3P/L converter da frame current loop		
	PI-compensator for the a-frame single module CHB current-loop		
	PI-compensator for the 3P4L converter z-frame current loop		
	PI-compensator for the 3P4L converter in standalone mode		
Hyi boost DAP	PI-compensator for the DAB boost mode voltage -loop		
Hyi buck DAR	PI-compensator for the DAB buck mode voltage-loop		
Hvid 2D4I	PI-compensator for the 3P4L converter voltage loop		
Hvid-CHB-1N	PI-compensator for a single module CHB voltage-loop		
	DAB DC-current on the side of the CHB		
i <sub>DAB2</sub>	DAB DC-current on the side of the 3P4L converter		
i <sub>DC1</sub>	Total current flowing between the CHB and the DAB array		
i <sub>DC2</sub>	Total current on DC-side of 3P4L converter		
i <sub>DC-3P4L</sub>	3P4L DC-side current		
ірс-снв	DC-side current of a CHB H-bridge		

Symbol	Description			
i <sub>k-3P4L</sub>	AC current through $L_{fl-3P4L}$ for k=a, b, c or the current through the neutral			
	inductor $L_{fN-3P4L}$ for k = N			
$\mathbf{i}_{k-MV}$	Current through phase k on the MV-side			
I <sub>ph-MV</sub>	Current through the MV-side filter			
I <sub>ph-MV1</sub>	IV1 Fundamental current of I <sub>ph-MV</sub>			
K <sub>i</sub>	Integral factor of the PI-controller			
K <sub>p</sub>	Proportional factor of the PI-controller			
L <sub>CHB</sub>	CHB filter inductor			
L <sub>DAB</sub>	Transformer leakage inductance			
L <sub>DAB</sub>	Primary referred, total leakage inductance of the transformer			
L <sub>DAB1</sub>	Leakage inductance of the primary winding			
L <sub>DAB2</sub>	Leakage inductance of the secondary winding			
L <sub>f1-3P4L</sub>	3P4L filter inductor on converter side			
L <sub>f2-3P4L</sub>	3P4L filter inductor on grid/load side			
N <sub>m</sub>	Number of H-Bridges in each phase of the CHB			
n <sub>Tr</sub>	Transformer turns-ratio			
n <sub>Tr</sub>	Transformer turns-ratio			
Р	Active power			
P <sub>DAB</sub>	Power transferred through the DAB			
P <sub>DAB1</sub>	Power of the DAB on the CHB side			
P <sub>DAB2</sub>	Power of the DAB on the 3P4L converter side			
P <sub>DAB</sub> -rated	Rated power of the DAB			
Prated	Rated active power			
Q	Reactive power			
S	Apparent power			
S <sub>bb</sub>	Buck-boost selection switch			
S <sub>max</sub>	Maximum apparent power			
S <sub>sa</sub>	Standalone selection switch			
V <sub>abc-cf-3P4L</sub>	Voltage across the filter capacitor on the AC-side of the 3P4L converter			
V <sub>CHB</sub>	AC-side voltage of the CHB			
V <sub>DAB1</sub>	DC-voltage between the CHB and the DAB			
V <sub>DAB2</sub>	DC-voltage of the DAB on the side of the 3P4L converter			
V <sub>in</sub>	Input voltage			
v <sub>k-3P4</sub>	3P4L Voltage of phase-leg k with respect to the ground			
Vout	Output voltage			
V <sub>ph-LV</sub>	Phase-voltage of the LV-grid			
V <sub>ph-MV</sub>	Phase-to-neutral MV grid voltage			
X*	Set or desired value of x			
x"	Parameter referred to the secondary side of the transformer			
Xd	d-frame component of x <sub>abc</sub>			
Xq	q-frame component of x <sub>abc</sub>			
Xz	z-frame component of x <sub>abc</sub>			
θ	Angular displacement; equal to $\int 2\pi f dt$			
φ	Angle between apparent power and rated power			
ω <sub>g</sub>	Angular grid frequency, equal to $2\pi \mathrm{f}_{\mathrm{grid}}$			

## LIST OF ABBREVIATIONS

Acronym	Description		
1¢3W	Single-Phase Three-Wire		
2L-VSC	SC Two-Level Voltage Source Inverter		
3D-SVPWM 3D Space Vector Puls Width Modulation			
3L-ANPC	three Active NPC		
3P4L Three-phase Four-Leg			
5L-ANPC	five level Active NPC		
5L-HNPC	five level H-bridge NPC		
AC	Alternating Current		
СНВ	Cascade H-Bridge		
CPWM	Continuous Pulse Width Modulation		
DAB	Dual Active Bridge		
DC	Direct Current		
DPWM	Discontinuous Pulse Width		
FC	Flying Capacitor		
HF	High Frequency		
IEEE	Institute of Electrical and Electronics Engineers		
IGBT	Isolated-Gate Bipolar Transistor		
LF	Low Frequency		
LFT	Line Frequency Transformer		
LS-PWM	Level Shifted PWM		
LV	Low Voltage		
MMC	Modular Multilevel Converter		
MV	Medium Voltage		
NPC	Neutral Point Clamped		
PCC	Point of Common Coupling		
PCC	Point of Common Coupling		
PI	Proportional Integral		
PLL	Phase-Locked Loop		
PS	Phase Shift		
PS-PWM	Phase Shifted PWM		
PV	Photovoltaic		
RMS	Root Mean Square		
SST	Solid State Transformer		
SVM	Space Vector Modulation		
TDD	Total Demand Distortion		
THD	Total Harmonic Distortion		
TTC	Transistor Clamped Converter		
ZVS	Zero Voltage Switching		

## Chapter 1 INTRODUCTION

In recent years, the complexity of the electrical grid has grown due to the increased use of renewable energy and other distributed generation sources. To cope with this complexity, new technologies are required for better control and a more reliable operation of the grid. One of such technologies is the solid-state transformer (SST). The SST technology is quite new and therefore the knowledge on the behavior of these systems in the grid is rather limited. In order to gain more insight into the workings of this device, this research will focus on developing a mathematical model along with a control scheme which can be used for simulating the SST and its behavior in the grid.

## 1.1 Background Information

In the present power grids, energy is generated in large power stations and transmitted over high voltage lines. This energy is then delivered to consumers via medium and low-voltage lines. In these grid layouts, the power flow goes only in one direction: from central power stations to consumers[1]. In recent years, many European countries have started to liberalize their electricity market. This liberalization brought with it an increased penetration of renewable energy and other distributed generation sources in the grid. These developments cause the network layout and operation to become much more complex. In order to better manage future grids, sometimes also called smart grids, new technologies are required that allow better control, an increased number of power inputs and bi-directional power flow.

A key enabler for smart grids is the solid-state transformer. The SST offers ways to control the routing of electricity and provides flexible methods for interfacing distributed generation with the grid. The solid-state transformer also allows for control of the power flow, which is needed to ensure a stable and secure operation of the grid. However, this comes at the cost of a more complex and expensive system.

A typical SST consists of an AC/DC rectifier, a DC/DC converter with high-frequency transformer and a DC/AC inverter. One of the functions of a SST is similar to that of a traditional line frequency transformer (LFT), namely increasing or decreasing the voltage. Additional features of the SST not found in LFS are[2]:

- Reduced size and weight
- Instantaneous voltage regulation
- Fault isolation
- Power factor correction
- Control of active and reactive power flow
- Fault current management on low-voltage and high voltage side
- Active power filtering of harmonic content on the input

- Good voltage regulating capabilities
- The output can have a different frequency and number of phases than the input
- Possibility of a DC input or output
- Voltage dip and sag ride though capability (with enough energy storage)

In recent years, the costs of power electronics has decreased, and more reliable, low loss, high power, high frequency power electronics have become available. The cheaper price and the fact that the solid-state transformer can replace certain grid components along with the conventional transformer, makes the solid-state transformer potentially economically feasible[3].

This economically feasibility combined with the many advantages of the solid-state transformer made engineers at TNO pursue further research into the development and application of these devices in the grid.

## **1.2 From Problem to Focus**

There is limited information available on grid behavior of the SST due to its novel technology. Simulation software allows investigation of the SST's performance without having to build a prototype first. Situations such as load changes or power failure can be simulated by creating the circuit model in SPICE software. These simulations have one major drawback, namely the long computation times. This is caused by the following reasons[4]:

- 1. Due to the complexity of the control algorithms and switching elements, the simulation waveforms require long computational times to generate.
- 2. When the system contains transient times that are a magnitude larger than the sampling time, the simulation time needs to be increased in order to analyze steady state operation. An increase of the simulation time automatically increases the computation time.
- 3. The overall computation time for obtaining simulation waveforms at steady-state can drastically increase with the increased number of switching elements and control loops.

In order to reduce the computation times, the switching model can be replaced with an averaged signal model. Averaged signal models offer several advantages over switching models such as[5]:

- 1. Faster simulation times that can reduce the simulation times by a factor of 100 or more.
- 2. The analysis of the input and output relationship without being obscured by the switching ripple.
- 3. The averages signal models can be linearized to design a feedback controller.

In order to create the averaged signal model, a clear understanding of the operation of the SST is required.

## **1.3 Problem Statement**

Using the information from the previous section, the problem statement can be defined as: *"Much of the dynamic behavio of SSTs in the medium- and low-voltage grid is not yet known."* 

## 1.4 Research Objective

The research objective that follows from the problem statement is:

"Design a mathematical model and controller for the SST to investigate its dynamic behavior under different grid conditions"

## **1.5 Research Questions**

Several questions are defined in order to help come to the research objective. Sub-questions are also defined to support the main questions. The questions on which this research will focus are:

- 1. What is the current state of art of the solid-state transformer technology?
  - 1.1. What solid-state transformer architectures are available?
  - 1.2. What topologies are available to construct a SST?
    - 1.2.1. What modulation techniques are available for those topologies?
- 2. What models are needed in order to simulate the behavior of the SST?
  - 2.1. Which models are needed for faster simulations?
  - 2.2. Which models are needed for controller design?
- 3. Which control scheme is best suited for the chosen model and topology?
- 4. Which situations can the SST encounter in the grid?
  - 4.1. How does the SST behave in those situations?

## **1.6 Case Specification**

For a quantitative analysis of the SST, certain parameters for this research are predefined. These parameters and their values are presented in Table 1.1. Although this research is done with the specified values in mind, the equations and models are kept flexible enough for applications at any rated value.

Parameter Name	Symbol	Value
Rated Power	P <sub>rated</sub>	1 MW
Medium-Voltage (line-to-line)	V <sub>MV</sub>	10 kV
Low voltage (line-to-line)	$V_{LV}$	400 V
Grid Frequency	$\mathbf{f}_{\mathrm{grid}}$	50 Hz

Table 1.1: SST specifications

## **1.7 Research Approach**

This research is broken down in several steps, each focusing on a different aspect of the SST. Figure 1.1 shows a global overview of the different stages of this research that lead to answering the problem statement. The steps from literature study to conclusions and recommendations are:

- 1. Literature study
- 2. First order design
- 3. Derivation of mathematical models
- 4. Controller design
- 5. Grid simulations
- 6. Conclusions and recommendations



Figure 1.1: Research approach

Each stage of the research approach along with its results is documented in a separate chapter in this thesis report. The chapter on literature study is done in order to identify the present status of solid-state transformer technology. The different methods of constructing a SST are evaluated and a suitable topology is chosen. Along with the choice of topologies for the SST, a study is done to select the appropriate modulation technique for those topologies. These topologies and modulation schemes are applied to a given case in the next chapter. A first order design is then developed where the appropriate voltages, currents and passive components are calculated. The chapter on modeling of the SST focuses on developing two types of models. The first type is used in order to achieve faster simulation results, while the second type of model is later used for development on the controller. The chapter on controller design expands on the construction of the different controllers that will be used for the SST. After completion of the controllers, the model of the SST, along with its controller is used to simulate different scenarios. These scenarios range from operation under rated conditions to short-circuit situations. The results of these simulations will finally be used to draw conclusions and give recommendations for future research.

There are several topologies, modulation schemes, modeling methods and control approaches that can be used to achieve the research goal. To limit the scope of this thesis, at each step of this research the possible options are presented and a suitable candidate is chosen. The chosen candidate is then used in subsequent parts of this thesis. For instance, when a topology is chosen in chapter 2, only the modulation schemes for that topology are presented. Modulation schemes for the other topologies are left out, because they don't attribute to the rest of this research.

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## Chapter 2

# LITERATURE REVIEW OF SST CONCEPTS, TOPOLOGIES AND MODULATION SCHEMES

In recent years, the interest in SST technology has increased. Several research groups are investigating the applicability of the SST for different purposes. This has led to different SST architectures and topologies. This chapter provides an overview of the available architectures and chooses the one most suited for grid applications. After this selection, a choice of topologies and modulation methods for each of the stages in the SST is made.

## 2.1 Solid State Transformer Concepts

The traditional Line Frequency Transformer (LFT) has been used since the introduction of AC systems for voltage conversion and isolation. The widespread use of this device has resulted in a cheap, efficient, reliable and mature technology and any increase in performance are marginal and come at great cost[1]. Despite its global use, the LFT suffers from several disadvantages. Some of these are:

- Bulky size and heavy weight
- Transformer oil can be harmful when exposed to the environment
- Core saturation produces harmonics, which results in large inrush currents
- Unwanted characteristics on the input side, such as voltage dips, are represented in output waveform
- Harmonics in the output current has an influence on the input. Depending on the transformer connection, the harmonics can propagate to the network or lead to an increase of primary winding losses.
- Relative high losses at their average operation load. Transformers are usually designed with their maximum efficiency at near to full load, while transformers in a distribution environment have an average operation load of 30%.
- All LFTs suffer from non-perfect voltage regulation. The voltage regulation capability of a transformer is inversely proportional to its rating. At distribution level, the transformers are generally small and voltage regulation is not very good.



The Solid State Transformer (SST) provides an alternative to the LFT. It uses power electronics devices and a high-frequency transformer to achieve voltage conversion and

isolation. It should be noted that the SST is not a 1:1 replacement of the LFT, but rather a multi-functional device, where one of its functions is transforming one AC level to another. Other functions and benefits of the SST which are absent in the LFT are [2][3]:

- High controllability due to the use of power electronics.
- Reduced size and weight because of its high-frequency transformer. The transformer size is inverse proportional to its frequency; hence a higher frequency results in a smaller transformer.
- Unity power factor because the AC/DC stage acts as a power correction device. Unity power factor will usually increase the available active power by 20%.
- Not being affected by voltage swell or sag as there is a DC link in the solid state transformer.
- Capability to maintain output power for a few cycles due to the energy stored in the DC link capacitor.
- Function as circuit breaker. Once the power electronics used in the solid state transformer are turned off, the flow of electricity will stop and the circuit is interrupted.
- Fast fault detection and protection.

#### 2.1.1 General applications of the SST

A SST can be used instead of the conventional LFT in any electrical system, but because of its additional advantages and functions, the application of the SST in certain areas is much more attractive. Examples of these applications are[4][5][6]:

#### 1. Locomotives and other traction systems (Figure 2.2)

The transformer used in current locomotive vehicles is 16.7Hz and is  $\pm$ 15% of the total weight of the locomotive. The SST can provide a significant weight reduction. Additionally, the SST is also able to improve the efficiency, reduce EMC, harmonics and acoustic emissions[7].

#### 2. Offshore energy generation (Figure 2.3)

Offshore generation, whether from wind, tidal or any other source, can benefit from the reduction in weight and size. This reduction leads to smaller and thus cheaper offshore platforms. Another advantage is that the SST can achieve unity power factor, thus increasing the efficiency in power transmission.

#### 3. Smart Grids (Figure 2.4)

In future power systems, the usage of renewable generation is expected to increase, and will require an energy management scheme that is fundamentally different from the classic methods. For fast and efficient management of the changes in different loads and sources, the SST can be used to dynamically adjust the energy distribution in the grid. The function of the SST as described in this scenario is similar to that of a router, but instead of managing data, the SST will manage the flow of energy. For this reason, the SST is sometimes also called an energy router[8]

This research will limit its focus on the application of the SST for (smart) grids.



#### 2.1.2 Applications of the SST in the grid

The following application scenarios of the SST are possible [9]:

#### 1. Application between generation source and load or distribution grid (Figure 2.5.a+b)

In this scenario, the SST can enable constant voltage and frequency at its output if the input voltage and frequency are variable. The SST can also allow the energy transport between source and load or grid to occur at unity power factor. This results in better utilization of the transmission lines and increased flow of active power. Another function, which the SST can provide, is to improve system damping during the transient state.

#### 2. Application between two distribution grids (Figure 2.5.c)

One of the features of the SST is that it does not require both grids to have the same voltage level, frequency or to operate synchronously. The SST can be used to control the active power flow between both grids. It can also be used as a reactive power compensator for both grids. A special application in Figure 2.5.c is when considering the commercial side of power systems. During periods when energy in grid 2 is cheaper than in grid 1, the operator of grid 1 can reduce its own generation and buy the energy from grid 2[10].

#### 3. Connection between the MV- and LV-grid (Figure 2.5d)

In contrast to the LFT, the SST can accurately control the amount of active power flowing from the MV- to the LV-grid. This is useful if the LV-side also has generation sources such

as PV-panels. The SST can limit the amount of energy that flows back and forward through certain parts of the grid, to avoid overload of transmission lines with limited current carrying capacity.

#### 4. Connection between MV-grid and loads (Figure 2.5e)

LV-loads are often unbalanced which can lead to harmonics disturbances in the voltage and asymmetrical voltages. A neutral wire is added in order to eliminate these disturbances and achieve a more symmetrical voltage. When the imbalance is large or consists of many non-linear loads, the addition of a neutral wire might not nullify the disturbances completely. In this case, the SST can help by generating a voltage that hardly suffers from unbalanced and non-linear loads.

#### 5. Application as interface for distributed generation and smart grids (Figure 2.5.d)

Distributed energy sources, such as photovoltaic arrays and wind turbines, provide a variety of electric sources. These sources often have a varying voltage or frequency or can even be a DC voltage. The SST is flexible enough to allow connection of these sources to the traditional grid.

Different applications of the SST lead to different requirements; therefore, this research will limit its scope to the applications in Figure 2.5d and Figure 2.5e.



Figure 2.5: Schematic overview of the SST applications

#### 2.1.3 Barriers for Widespread Usage

Despite the many advantages and applications for the SST, it still faces some challenges, which keeps it from universal acceptance. These are mostly a result of the novelty of the SST technology and are expected to be resolved as the SST matures. The current disadvantages of the SST compared to the LFT are shown in Figure 2.6. They can be summarized as[1]:

• The LFT costs less compared to the SST. This statement applies to the first generation of SSTs, but with the decreasing price in semiconductors and control circuitry, the

price of the SST will also decrease. The increasing price of resources, such as copper and ferrites, to build the LFT will also have a positive effect on SST adoption.

- The complex nature of the SST results in a system that is unlikely to be as reliable as the LFT. However, a modular design of the SST allows for isolation and bypassing of faults. As with all systems, the reliability of the SST is expected to increase as the technology matures.
- The efficiency of the SST is hard to compare with the LFT. It is not yet clear what the efficiency of a mature SST will be, since the values in literature vary between 90% and 98.1% (compared to the LFT, which is > 97.3%). Although the total efficiency of the LFT is better than the SST, features as harmonic reduction and unity power factor can result in the SST having better performance than the LFT.



Despite its drawbacks, the increased functionality of a distribution grid with a SST makes this concept economically viable in the near future.

#### 2.1.4 Current research on the SST

First mention of the SST dates back to research done in 1980 by James Brooks[11]. Due to hardware limitations, the SST was not a practical solution during that time. New developments have made the SST an interesting research topic again, resulting in different architectures and topologies. Based on the goal of the different research groups, the SST architectures that have been developed in the last 10 years can be categorized as [5]:

SST architectures based on their topologies:

- 1. A cyclo converter based SST for low-voltage, low-power application patented by EATON[12]
- 2. Van der Merwe proposed an architecture using a multilevel AC-DC converter and a DC-DC converter with passive rectifiers. This topology was developed for unidirectional power flow and can be extended to a bidirectional system by replacing the passive rectifier with active systems[1].
- 3. Steimel et al. developed an architecture with a soft switching DC-DC converter stage[13].
- 4. Researchers at ETH Zurich are working on a matrix converter with the code name MAGACube[5].
- 5. The FREEDM project is investigating a SST based on a single-phase system with modularity in mind[14].

SST architectures based on their application:

- Akagi (2005/2007) proposed two SST architectures. A fully phase modular topology 1. for MV motor drives. The other architecture consists of back-to-back connections of static compensators (STATCOMs) for grid applications.
- The UNIFLEX project is working on a three-port SST, where 2 ports are used for 2. interconnection between 3.3kV grids and the third one is for LV grid connection[15].
- ABB is currently investigating the application of SSTs for traction application. They 3. were able to increase both efficiency and power density [16][7].

SST architectures with focus on switching devices

- 1. Das et al. is working on a solid state power station using SiC devices[17].
- EPRI in USA developed a 20kVA SST prototype named Intelligent Universal 2. Transformer (IUT). This system uses SGTOs instead of IGBTs or MOSFETS along with a resonant DC/DC converter to reduce switching losses[18].

Different research teams have used different architectures and topologies for the SST. Since it is difficult to decide beforehand which is most suited for this research, a dedicated study is done to determine the optimal topologies for this research.

### 2.2 Schematic overview

By definition, the SST consists of one or more power electronics converters and an integrated high-frequency transformer. There are several SST architectures, but based on the topologies, they can be classified in four categories [19]:

- 1. Single-stage with no DC link (Figure 2.7.a)
- 2. Two-stage with a DC link on the secondary side (Figure 2.7.b)
- 3. Two-stage with a DC link on the primary side (Figure 2.7.c)
- 4. Three-stage with a DC link on both the primary and secondary side (Figure 2.7.d)



Figure 2.7: Possible SST architectures[19][20]

Of the four possible classifications, the three-stage architecture, with two DCs (Figure 2.7.d), is the most feasible because of its high flexibility and control performance. The DC links decouple the MV- from the LV-side, allowing for independent reactive power control and input voltage sag ride-though. This topology also allows better control of voltages and currents on both primary and secondary side[19][21][22]. It consists of an AC-DC conversion stage at the MV-side, a DC-DC conversion stage with high-frequency transformer for isolation and a DC-AC conversion stage at the LV-side.

## 2.3 AC-DC Conversion Stage

The AC-DC conversion stage of the SST has a MV, AC-side and a DC-side. There are two options available for operating at such high voltages[23]:

- 1. Two-level converters using cutting-edge high voltage power semiconductors
- 2. Multilevel converters using mature power semiconductors



Figure 2.8: SST schematic with AC-DC Conversion Stage highlighted

The use of high power semiconductor in combination with classic Two-Level Voltage Source Converter (2L-VSC) topologies has the advantage of using well-known circuit structures and control methods. However, the newer power semiconductors are more expensive and their higher power rating introduces other power-requirements and the need of HV filters.[24] The scalability of 2L-VSCs is also an issue, since the voltage handling capabilities are restricted by the power semiconductor ratings.

The new converter topologies, also known as multilevel converters use well-known, inexpensive power electronics. Multilevel topologies are scalable to any desired voltage rating, but result in a more complex circuit with several challenges for implementation and control. Nevertheless, this complexity also enables more control degrees of freedom that can be used to boost the power quality and efficiency. These properties have made the multilevel converters very attractive for further development and implementation[23] [24], and are the reason why a multilevel topology will be used in the AC-DC stage of the SST.

#### 2.3.1 Topologies

Multilevel Converters have become a big success because of their higher power ratings, lower common-mode voltages, reduced harmonic content, near sinusoidal currents, no or small input and output filter, increased efficiency, possible fault tolerant operation[24].

Multilevel converters contain an array of power semiconductor devices and capacitive voltage sources, which are used to produce a multistep voltage waveform. This stepped waveform is generated by switching the power semiconductors in such a way that the capacitive voltage sources are added to the desired voltage. The number of levels of a converter is defined as the number of constant voltage values that can be generated between the output terminal and the neutral. In order to be classified as a multilevel converter, each phase of the converter has to generate at least three different voltage levels. This is illustrated in Figure 2.9.

The first multilevel converters that were introduced were the Cascade H-Bridge (CHB), the Neutral Point Clamped (NPC) and the Flying Capacitor (FC) topology. These three topologies are the most studied and have found their way into several commercial applications. Of the other available topologies, the ones that have found practical applications are the five level H-bridge NPC (5L-HNPC), the three Active NPC (3L-ANPC), the five level Active NPC (5L-ANPC) the Transistor Clamped Converter (TTC) , and the Modular Multilevel Converter (MMC, also called M<sup>2</sup>LC or M2C) [25][26][27].



#### 2.3.1.1 Neutral Point Clamped or Diode-Clamped Converters

The Neutral Point Clamped (NPC) or Diode-Clamped Converter (DCC) consists of several traditional two-level VSIs, with some small modifications, connected one over the other[24]. A three level NPC is shown in Figure 2.10. The negative point of the upper converter is connected to the positive point to form the new phase output, while the original outputs are joined together through two clamping diodes to form the neutral point N, dividing the DC-link voltage  $V_{DC}$  in two. Due to this division, each power device has to block only half the total converter voltage, therefore the power rating of the converter can be doubled using the same semiconductor technology used in traditional VSIs. Since the neutral point enables a zero voltage level, the phase-leg in Figure 2.10 is able to generate three voltage levels.



Figure 2.10: Three-level NPC power circuit

Although the NPC is theoretically expandable to any number of output voltage levels, in practice this number is limited to five[28][29]. At higher output voltage levels, capacitor voltage balance problems begin to arise. Another problem experienced is that while the switches only have to handle the operating voltage, the clamping diodes must be able to withstand several times the operating voltage. This requires several diodes to be connected in series and results in higher conduction losses. The series connected diodes also produce reverse recovery currents, causing an increase in switching losses.

The main advantages of the NPC are [30][31]:

- All phases share the same DC bus and which reduces the capacitor requirements.
- The capacitors can be pre-charged as a group.
- The efficiency of the converter is high when the devices are switched at fundamental frequency.
- The reactive power flow can be controlled.
- The control method is simple for back-to-back converters.

The main disadvantages of the NPC are:

- The real power flow is difficult to control for the individual converter because the intermediate DC levels can lead to an overcharge or discharge of capacitors without precise monitoring and control.
- The number of clamping diodes increases with the square of the number of voltage levels, which might not be practical for systems with a high number of levels.
- The current flowing through the switches differs because certain switches conduct for a longer period than others do. When this is not taken into account during the design phase, it can lead to over- or under sizing of switching devices.
- The uneven current flow also causes uneven losses, which result in unsymmetrical temperature distribution. This affects the cooling system design and limits the maximum power rating, output current and switching frequency of the converter for a specific semiconductor technology[25].

#### 2.3.1.2 Flying Capacitor Converters

The Flying Capacitor (FC) Converter is very similar to the NPC, with the main difference is that the clamping diodes are replaced by flying capacitors. In the FC topology, the load cannot be directly connected to the neutral. Instead, the load is connected to the positive or negative bar, through the flying capacitor with opposite polarity with respect to the DC-link, in order to obtain a zero voltage level. Another important difference with the NPC topology is that the FC has a modular structure and can easily be extended to achieve more voltage levels and higher power rates.

The main advantages of the FC are [30][31]:

- The large number of capacitors allows the converter to ride through short outages and deep voltage sags.
- Both real and reactive power can be controlled.
- Provides switch combination redundancy for balancing different voltage levels.

The main disadvantages of the FC are:

- High converter levels require a large amount of storage capacitors. Systems with high converter levels are more bulky, expensive and more difficult to package.
- High switching frequencies are required in order to keep the capacitors balanced, whether self-balancing or a complex control-assisted modulation method is used. These high switching frequencies are not feasible for high power applications.
- The required pre-charging of the capacitors to the same voltage level at start-up is complex.
- Switch utilization and efficiency are poor for real power transmission.



#### 2.3.1.3 Cascade H-Bridge Converters

The Cascade H-Bridge (CHB) Converter consists of a cascaded connection of several single phase H-Bridge inverters. Each H-Bridge is connected to an isolated DC source and represents two voltage source phase legs; whose line-to-line voltage equals that H-Bridge's output. A single H-Bridge is therefore able to generate three different output voltages. In order to obtain the zero level voltage, the phase outputs can be connected to the positive or negative nodes of the inverter. The output voltages of two or more cascaded connected H-Bridges can be combined to form different output voltage levels, this increases the total converter output voltage and power rating.

The isolated DC sources required by this topology can be supplied by an array of photovoltaic modules. Another option is to use the rectified output of a transformer with multiple secondary windings.

The main advantages of the CHB are [30][31]:

- The CHB can generate more output voltage levels than the NPC and the FC. This
  enables the CHB to have lower device switching frequencies for the same output
  voltage waveform. Lower devices switching frequencies allow for air cooling and
  higher fundamental output frequency without derating and without the use of an
  output filter [25].
- The topology allows for modularized layout and easy packaging, because each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors.
- Bulky and lossy snubber circuits can be avoided, since soft-switching is possible with this topology.
- Automatically balance of the capacitor voltages, since the average charge of each DC capacitor over one line cycle equals zero.
- When the transformer is equipped with appropriate displacements in the windings, it can result in input-current harmonics reduction[26].

The major disadvantages of the CHB are:

- Each H-bridge requires an isolated voltage source.
- The maximum DC-link voltage of each H-bridge is limited by the voltage rating of its components. Because of this limitation, the CHB is unable to generate a high voltage DC-link.

A variant of the CHB with asymmetric voltage sources has also been proposed. The basic idea of this topology is to take advantage of the different power rates of the converter cells. The high power cells can be switched at a lower frequency, therefore reducing switching losses, making higher power handling capabilities possible. The disadvantage of this topology is that the use of different power levels eliminates the input current low order harmonic cancellation effect of the CHB. It also requires different power semiconductors and different thermal design, resulting in a topology that is no longer modular. Another disadvantage is that for some asymmetric voltage ratios or modulation indexes, the circulating current among the power cells can cause the current in the low power cells to flow in opposite direction with respect to the main current. This requires complex measurements in order to keep the capacitors at desired voltage ratio under these conditions. Despite the advantages of this topology, the mentioned disadvantages have kept it from commercial implementation[32].

#### 2.3.1.4 H-bridge NPC

The Five-Level H-bridge NPC (HNPC) consists of an H-bridge connections of three-level NPCs (3L-NPC) [25][33][34]. As with a normal H-Bridge, the HNPC requires isolated DC sources for

each H-bridge. A transformer with dedicated secondary three-phase windings is used to supply the required DC sources.

The main advantage of the HNPC is:

• The complex transformer is able to effectively cancel low-order harmonics

The disadvantages of the 5L-HNPC are:

- The topology requires a rather complex modulation scheme
- The control method should be able to balance the DC bus capacitor voltage and the switching loss among the inverter arms
- This topology is less modular than the CHB topology

#### 2.3.1.5 Three-Level Active NPC

The Three-Level Active NPC (3L-ANPC) was created to address the problems faced in the 3L-NPC. By replacing the clamping diodes with clamping switches, the current can be forced to go through the upper or lower clamping path. This can be used to control the power loss distribution and enables much higher power rates than the normal 3L-NPC.

Although control of the power loss distribution is better in the 3L-ANPC, it still suffers from the other drawbacks of the conventional NPC[35].

#### 2.3.1.6 Five-Level Active NPC

A variation of the 3L-ANPC is the five-level NPC (5L-ANPC) and is formed by a series connection of two 3L-ANPC with a FC power cell connected between the ANPC switching devices[25].

The main advantages of the 5L-ANPC are:

- The use of FCs enables modularity; this is not possible with the classic NPC topology
- Higher voltage levels can be achieved by adding FCs, without the need to add seriesconnected diodes

The main disadvantages of the 5L-ANPC are:

- The control and circuit structure of the 5L-ANPC are complex.
- The control scheme needs to be able to handle the FC control and voltage initialization, and the NPC DC-link capacitor voltage.
- Increasing the number of FCs only increases the number of output voltage levels, not the power rating. This is still limited by the ANPC part of the circuit.

#### 2.3.1.7 Transistor-Clamped Converter

The Transistor-Clamped Converter (TCC) or Neutral Point Piloted (NPP) is very similar to the NPC, but instead of clamping diodes, bidirectional switches are used. This allows for a controllable path for the currents and enables better control of the power loss distribution[25][36][37].

The advantages of the TCC are:

- The TCC requires only half the amount of switches compared to the NPC and FC.
- The switches only have to handle half the voltage compared to the NPC. This allows for double the switching frequency and a better output waveform for the same current.

- Simple control of the gates, because only one power transistor is switched at a time. This results in a direct relation between the transistor which has to be turned on, and the output voltage.
- Modular design[38].

The main disadvantages of the TCC are:

- A voltage balancing strategy is required.
- Large number of transistors required

#### 2.3.1.8 Modular Multilevel Converter

The Modular Multilevel Converter (MMC, also known as M<sup>2</sup>LC or M2C) topology was introduced in the early 2000s and received a lot of attention from industry and academics alike. The MMC is formed by connecting several identical modules, consisting of an AC/DC converter and a floating capacitor, in series to obtain a single or three-phase output voltage[25][39]. The module switches are used to connect or bypass their respective capacitor to the total array of capacitors in the converter leg in order to generate the multilevel waveform.

The main advantages of the MMC are[25][39][40]:

- The topology is highly modular, flexible, and scalable, making a range from mediumto high-voltage levels possible.
- It has low harmonic content and low filter requirements.
- The MMC does not require separate DC sources, eliminating the need for a special transformer.
- Each module provides its own capacitor and therefore there is no need for high-voltage DC-link capacitors.
- An increase of levels enables a decrease in module switching frequency without compromising the power quality.

The main disadvantage of the MMC is:

• A complex control is required to pre-charge the capacitors and balance the average value of the voltage across each submodule capacitor[41].

#### 2.3.1.9 Modularity

A lot of emphasis has been placed on modularity of certain topologies. A modular system is a system consisting of similar building blocks. Since these blocks are identical, they effectively reduce manufacturing costs and allow for easy scaling and service of the system. They can also be used to provide optional degrees of redundancy, by implementing a control that can bypass defective modules[42]. The modularity of a CHB is shown in Figure 2.13.



#### 2.3.1.10 Discussion

In order to choose between the different topologies, certain aspects of the topologies are listed in Table 2.1.

	Control	Voltage Balance Control	Modular	Major Disadvantages
NPC	Simple	Unattainable	No	Voltage balance issues for systems with more than 3 levels
FC	Complex	Complex	Yes	Higher output levels require a large amount of capacitors
СНВ	Simple	Simple	Yes	High voltage DC-link not achievable
HNPC	Complex	Complex	limited	Complex control and modulation
3L-ANPC	Complex	Complex	No	Number of clamping diodes increase with square of output levels
5L-ANPC	Complex	Complex	Yes	Complex circuit and control
TTC	Simple	Complex	Yes	Large number of transistors required
MMC	Complex	Complex	Yes	Complex control

Table 2.1: Comparison of multilevel topologies

The data presented in Table 2.1, shows that the CHB has a simple control, simple voltage balance control and a modular structure. The fact that the CHB is unable to achieve a high voltage DC-link is not a limitation for this research, since it only focuses on interconnection between two AC-voltages. Thus, when looking at the advantages of the CHB, it becomes clear that this is the most suited topology for the AC-DC conversion stage of the SST.

#### 2.3.2 Modulation

Multilevel converters require multilevel modulation methods. These methods have received a lot of attention over the last years from researchers. The main reasons for the increased interest are[23]:

- The challenge to apply traditional modulation techniques to multilevel converters
- The inherit complexities of multilevel converters due to the increased amount of power semiconductor devices
- The possibility to take advantage of the extra degrees of freedom provided by the additional switching states provided by multilevel topologies

These reasons lead to the development of several modulation methods, each with their own unique features and drawbacks, depending on the application. Depending on the domain in which the modulation technique operates, two categories can be distinguished. These are:

- Voltage based algorithms.
- Space vector based algorithms

#### Voltage Level Based Algorithms

Voltage Level Based Algorithms operate in the time domain. Among the several voltage level based modulation techniques, the PWM methods are the most often used. The reasons for this high adoption are high performance, simplicity, fixed switching frequency and easy digital and analog implementation[43].

#### Space Vector Based Algorithms

Space Vector based algorithms are techniques where the reference voltage is represented by a reference vector. Instead of using a phase reference in the time domain, these methods use the reference vector to compute the switching times and states. Space vector algorithms have redundant vectors, which can generate the same phase-to-neutral voltage. This feature can be

used to improve inverter properties by using the redundant vector to fulfill other objectives, such as[44]:

- Reducing the common-mode DC output voltage
- Reducing the effect of overmodulation of output currents
- Improving the voltage spectrum
- Minimizing the switching frequency
- Controlling the DC-link voltage when floating cells are used

Although several space vector based algorithms are available, they are not the dominant modulation technique used in the industry. The reason for this is that carrier based PWM only requires a reference signal, carrier signals, and a simple comparator to for the gating signals. Space vector based algorithms on the other hand, require at least three stages: a stage to select the vectors for modulation, a stage to compute the duty cycle and a stage where the sequence for the vectors is generated. This means that the space vector algorithms have higher hardware requirements than the PWM techniques

There are several multilevel modulation techniques available, but not all are applicable for the CHB. The most common multilevel modulation methods for the CHB methods is given in **Error! Reference source not found.** Figure 2.14[45][46].



Figure 2.14: Classification of the most common multilevel modulation techniques

#### 2.3.2.1 Phase Shifted PWM

The Phase Shifted PWM (PS-PWM) is a multicarrier-based sinusoidal PWM developed for the control of multi-cell converters like the CHB. Each cell is assigned with two carriers and is modulated independently using the same reference signal. A phase shift across all the carriers is introduced in order to generate the stepped multilevel waveform[26][45]. The cell switching frequency of an n level converter is n times lower than the converter output frequency. A lower cell switching frequency means that the power electronic devices switch at a lower frequency resulting in fewer losses. PS-PWM causes the power to be evenly distributed among the cells across the entire modulation index. This allows reduction in input current harmonics for the CHB.

#### 2.3.2.2 Level Shifted PWM

Another multicarrier-based sinusoidal PWM is obtained by arranging the carriers in shifts. This modulation technique, where each carrier represents a possible output voltage level of the converter, is known as the Level Shifted PWM (LS-PWM)[23]. The LS-PWM method has better harmonic cancelation properties than the PS-PWM, but these are very small differences which are filtered by the load[25]. This method results in uneven power

distribution among the different cells leading to input current distortion in CHB circuits. Depending on the consecutive arrangement of carriers, the LS-PWM can be classified as:

- Phase Disposition PWM (PD-PWM), where all carriers are arranged on in vertical shifts with respect to each other.
- Phase Opposition Disposition PWM (POD-PWM), where the positive carriers are • arranged in phase with each other and in opposite phase with the negative carriers.
- Alternate Phase Opposition Disposition PWM (APOD-PWM), where each consecutive carrier is in opposite phase with its predecessor.

An example of each method is given in Figure 2.16.



Redundant switching states Figure 2.19: Single Phase Modulation (1DM) control region for a five level single-phase DCC[48]

2E Output voltages

-2E

#### 2.3.2.3 2D Space Vector Modulation

The 2D Space Vector Modulation (2D-SVM) works by transferring the three phase voltages of the converter to the  $\alpha$ - $\beta$  plane. The 2D-SVM determines the nearest vector to the reference vector to generate the switching sequence and their duty cycles. The 2D-SVM uses simple calculations, and can be used for any three-phase balanced system.

#### 2.3.2.4 3D Space Vector Modulation

The 3D Space Vector Modulation (3D-SVM) is a generalization of the 2D-SVM for unbalanced networks. When the system is in an unbalanced situation, or if a zero sequence or triple harmonics are present in the system, the state vectors are no longer located in the  $\alpha$ - $\beta$  plane. In order to calculate the state vectors under these conditions, the  $\alpha$ - $\beta$  plane is extended into the third dimension with a  $\gamma$  axis. The 3D-SVM is useful for compensating the zero sequence in active power filters, in systems with or without neutral unbalanced loads or triple harmonics and for balancing DC-link capacitor voltages. This method is applicable as a modulation technique for all applications that provide a 3D vector control.

#### 2.3.2.5 Single Phase Modulation

2.3.2.6 Discussion

A rather new modulation technique is the Single Phase Modulation (1DM). The 1DM uses a simple algorithm to determine the switching sequence and corresponding times. It does this by generating the reference phase voltage as an average of the nearest phase-voltage levels. The computational costs of the 1DM are low, independent of the number of levels and its performance is equivalent to that of 2D-SVM and 3D-SVM. The 1DM is independent of the chosen topology, but requires post processing to select one stage between the possible redundant states[47]. The control region of a 1DM is given in Figure 2.19Error! Reference source not found.. If for example the generated reference phase voltage is 1.7E, the 1DM strategy uses states {21, 20} or {10, 20}.

#### Hardware Remarks Algorithm Requirements Minimal Each cell is assigned with a pair of carriers, **PS-PWM** Simple allowing for easy control **LS-PWM** Simple Minimal Slightly better harmonic cancelation Only applicable for balanced 3 phase networks 2D-SVM Complex Extensive **3D-SVM** Complex Suitable for balanced and unbalanced 3 phase Extensive networks with or without neutral Independent of topology and number of phases 1DM Simple Extensive

A summary of available modulation methods is listed in Table 2.2.

Table 2.2: Summary of modulation methods

After going over the information presented in Table 2.2, it becomes clear that PS-PWM is the most suited modulation method for the CHB. The technique's simple algorithm, minimal hardware requirements and natural applicability to the CHB topology make it a good candidate. PS-PWM is also the only real commercial modulation method in CHBs[25].

## 2.4 DC-DC Conversion Stage

The second stage of the SST is a DC-DC conversion stage. Its schematic in Figure 2.20 shows that this stage can be divided in three parts:

- A DC-AC converter at the input
- A high-frequency (HF) transformer in the middle
- An AC-DC converter at the output

The HF transformer is required to achieve electric isolation. It also allows large voltage and current ratios between input and output. The usage of a HF transformer in the SST is the main reason for size reduction in comparison with the LFT. Figure 2.21 shows the magnitude of difference between a LFT and a HF transformer. To properly utilize this advantage, the topology for the DC-DC conversion stage should be as compact as possible without sacrificing the overall efficiency.

The DC-DC converter will receive its input from the AC-DC conversion stage. Since the AC-DC stage is responsible for delivering a constant output voltage, the input voltage of the DC-DC converter is not expected to vary much.



Figure 2.21: Comparison between a LFT and a high-frequency transformer[49]

### 2.4.1 Topologies

There are several classic isolated DC-DC converters available such as the isolated flyback, forward and Cúk converter. These topologies have the advantage of a simple circuit and low number of switches. However, the isolated flyback and forward converter suffer from ineffective transformer and switch utilization. The Cúk converter suffers from hard switching; uneven distributed switch stresses and requires two blocking capacitors with large current handling capacity and two inductors. These drawbacks make the isolated flyback, forward and Cúk unsuited topology for the DC-DC converters.

The possible candidate topologies for the DC-DC converter of the SST are[50]:

- Single-phase Dual Active Bridge converter
- Three-phase Dual Active Bridge converter
- Bidirectional Isolated Full Bridge converter
- Bidirectional Isolated Current Doubler converter
- Bidirectional Isolated Push-Pull converter
- LLC converter

#### 2.4.1.1 Single-phase Dual Active Bridge converter

The Single-phase Dual Active Bridge (DAB) converter consists of a full bridge circuit on the primary and the secondary side, with a HF transformer in between. The DAB utilizes the leakage inductance of the transformer to provide energy storage and to modify the shape of the current waveform. The major advantages of the DAB are the low number of passive components, evenly shared currents in the switches and soft switching properties. The drawback is that, depending on the modulation scheme and operating voltage, large RMS currents can flow through the DC capacitors, especially on the secondary side.

#### 2.4.1.2 Three-phase Dual Active Bridge converter

The Three-phase Dual Active Bridge consists of three half bridges on both the primary and secondary side. It requires three inductors for energy storage and three HF transformers; although a single three-phase, HF transformer can be used instead. It achieves good overall efficiency and requires lower ratings for the transformer, switches and inductors compared to the DAB. This topology also has smaller RMS capacitor currents and component ratings than the DAB. A disadvantage of this topology is the number of power semiconductor devices needed: it requires 12 switches. Other disadvantages are the high conduction and switching losses when operated within wide power and voltage ranges.



#### 2.4.1.3 Bidirectional Isolated Full Bridge converter

The Bidirectional Isolated Full Bridge converter contains a full bridge with a capacitive filter (voltage sourced) on the primary side and a full bridge with inductive filter (current sourced) on the secondary side. This topology allows high switching frequency, which results in a high power density. However, additional volume is required for the inductor on the secondary side. Another disadvantage is the requirement of a snubber circuit to avoid voltage spikes during switching. These spikes occur because the switches on the secondary side repeatedly connect the inductor on the secondary side to the stray inductance of the transformer.



2.4.1.4 Bidirectional Isolated Current Doubler converter

A variation of the bidirectional isolated full bridge converter is the Bidirectional Isolated Current Doubler converter. This topology replaces the two upper switches of the full bridge on secondary side with inductors. These inductors enable high current handling capabilities and a reduction in conduction losses. A drawback is that this topology requires a transformer with larger power rating. It also requires two large inductors for the secondary side.

#### 2.4.1.5 Bidirectional Isolated Push-Pull converter

The Bidirectional Isolated Push-Pull converter is another variation of the bidirectional isolated full bridge converter. It has a center-tapped transformer with two windings on the secondary side and one output inductor. The output inductor operates at double the switching frequency of the semiconductor, which results in half the inductance requirement

of bidirectional isolated current doubler topology. Since each winding only conducts during half the switching period, the transformer is ineffectively utilized and requires a higher power rating.



#### 2.4.1.6 LLC converter

The LLC is a resonant DC-DC converter. Resonant converters generate nearly sinusoidal transformer currents. This results in low switching losses, which allows higher switching frequencies and higher power densities. The LLC converter has a capacitor in series with the transformer leakage inductance, which blocks DC and prevents saturation of the HF transformer. Both primary and secondary sides of the transformer are connected to a full bridge circuit. The main disadvantage is that the actual switching frequency varies strongly with the supplied voltage and load. This even leads to an uncontrollable situation in the case of no load, since that situation requires infinite switching.

#### 2.4.1.7 Discussion

In order to select a suitable DC-DC converter for the SST, a comparison between the available topologies is presented in this section.

	Advantages	Disadvantages
Single-phase Dual	-Fewest passive components	-Large RMS DC capacitor
Active Bridge	-Good efficiency	currents may occur
converter		
Three-phase Dual	-Smaller RMS current than DAB	-Requires large number of
Active Bridge	-Lower component ratings	switches and inductors
converter	-No need for extra inductors	-Higher losses
<b>Bidirectional Isolated</b>	-High switching frequency and	-Requires extra inductor
Full Bridge converter	power density	-Requires snubber circuit
<b>Bidirectional Isolated</b>	-High current handling and	-Requires two extra inductors
Current Doubler	lower conduction losses	-Limited operating voltage
topology	-Fewer switches required	
<b>Bidirectional Isolated</b>	-High current handling with	- Ineffective use of complex
Push-Pull topology	reduced inductor requirements	transformer
	-Fewer switches required	
LLC converter	-Higher switching frequency	-Large inductor and capacitor
	and power density	required
	-Good efficiency	-Uncontrollable at no load

Table 2.3: Comparison between DC-DC converter topologies

Table 2.3 shows that the Single-phase Dual Active Bridge (DAB) achieves good efficiency while keeping the number of passive components low. This allows for a simple and compact circuit. For this reason the will be used for the DC-DC conversion stage of the SST.

#### 2.4.2 Modulation

The main modulation methods that are applied for the DAB are[51]:

- Phase Shift Modulation
- Trapezoidal Modulation
- Triangular Modulation

Each of these methods has a certain operating range of input voltage, output voltage and load in which the system results in the lowest losses. As stated before, the DC-DC conversion stage is expected to receive a constant input voltage from the AC-DC stage. At the same time, it is expected of the DC-DC conversion stage to deliver a constant output voltage to the DC-AC conversion stage. This means that the DAB will operate at a constant input-output voltage ratio. The only operating parameter which changes is the system load.

#### 2.4.2.1 Phase Shift Modulation

The Phase Shift Modulation, also known as the Rectangular Modulation works by switching the primary and the secondary side at a duty cycle of 50%. The power transfer between both sides can be controlled by adjusting the angle between the primary and secondary switching waveform. This modulation method offers the following advantages[52][51]:

- Low control complexity
- Lowest RMS circuit current compared to the other two modulation methods
- Highest power transfer possible
- Symmetrical share of the losses on all switches
- Zero voltage switching (ZVS) during turn-on of the switches

The disadvantages of this modulation method are[52]:

- Eight commutations have to be preformed
- Negative current on the DC side reduces power transfer, this results in a lower efficiency
- High losses are cause by reactive power when no active power is transferred
- Turn-off of switches happens under non-zero-voltage conditions, which result in switching losses



### 2.4.2.2 Trapezoidal Modulation

The Trapezoidal Modulation method is able to reduce the turn-off switching losses by adding a blanking time to the primary switching voltage. This causes half the number of switches (four switches) to switch-off under zero-voltage conditions. However, adding this blanking time requires a higher RMS current in order to transfer the same amount of power, which results in higher conduction losses. The advantages of this method are[52][51]:

- Lower switching losses
- Usable for a larger voltage range

The disadvantages are:

- Higher conduction losses
- Unsymmetrical losses if the primary voltage differs from the secondary voltage
- Complicated modulation and control algorithm
- Unable to operate under no-load conditions

#### 2.4.2.3 Triangular Modulation

A special case of trapezoidal modulation is the Triangular Modulation method. This method uses the blanking time or the phase shift to cause one edge of the primary switching voltage to overlap with the secondary. This results in a triangular transformer current, with only two switches turning off under non-zero-voltage conditions. This allows further reduction of the turn-off losses, however, the conduction losses increase due to a larger current peak. The advantages of this method are:

- Lowest switching losses compared to the other two methods
- Very suitable when the primary and secondary voltage ratios are different from the transformer turns-ratio

The disadvantages are:

- The switching losses always occur in the same two switches
- Inefficient use of the period for power transfer
- Complicated modulation and control algorithm
- Highest RMS current compared to the other two methods

#### 2.4.2.4 Discussion

A brief comparison of three modulation methods is presented in Table 2.4.

	Major Advantage	Major Disadvantage
Phase Shift Modulation	Simple control and algorithm	Higher losses at low power levels
Trapezoidal Modulation	High voltage range	Unable to operate under no-load
<b>Triangular Modulation</b>	Low switching losses	High RMS currents
Inangular Modulation	LOW SWITCHING IOSSES	

Table 2.4: Major advantages and disadvantages of the DAB modulation methods

Table 2.4 shows that the phase shift modulation is simple to implement. Its lower RMS currents result in lower component ratings. These advantages outweigh the higher turn-off losses faced with this method. For these reasons, the phase shift modulation is the most suited method for the DAB.

## 2.5 DC-AC Conversion Stage

The third stage of the SST is an AC-DC circuit that converts the DC output from the DC-DC stage into an AC voltage (Figure 2.31). Since this stage is at low voltage, it is more feasible to use a Two-Level Voltage Source Inverter (2L-VSC) than a multilevel inverter. The reasons for this are the cheaper, simpler circuit and the use of a more mature technology.



Figure 2.31: SST schematic with DC-AC Conversion Stage highlighted

#### 2.5.1 Topologies

The DC-AC conversion stage of the SST should be capable of producing a three-phase line-toline and line-to-neutral voltage. This stage will either be connected to a low-voltage distribution grid on will work in standalone mode. In both cases, it should be capable of handling asymmetrical loads, since distribution grids are inherently asymmetrical [53]. They should also allow bidirectional power flow, to accommodate the integration of distributed generation. Based on the required functions, the possible DC-AC topologies are:

• Three Half-Bridges Converters in parallel

- Three Full-Bridges Converters in parallel
- Three Single-Phase Three-Wire Converters in parallel
- Conventional Three-Phase Converter
- Three-Phase Four-Leg Converter

#### 2.5.1.1 Half-Bridge Converters

The Half-Bridge Converter is the basic block of the voltage source DC-AC converters. It is build up out of two bidirectional switches. Each switch consists of a controllable power semiconductor device and an antiparallel diode[54]. An example of a three-phase converter built from half-bridges is shown in Figure 2.32.

#### 2.5.1.2 Full-Bridge Converters

Each phase of the Full-Bridge (also called H-Bridge) Converters consist of two half-bridge converters, as shown in Figure 2.33. An advantage with the Full-Bridge Converter is that it requires a lower DC-link voltage than the other topologies[55]. As with the half-bridge, three full-bridge converters are needed to generate a three-phase output.



#### 2.5.1.3 Single-Phase Three-Wire Converters

The Single-Phase Three-Wire ( $1\phi 3W$ ) Converter uses a combination of three half-bridges and LC output filters to generate two line-to-line and line-to-neutral voltages[56]. From its schematic in Figure 2.34, it becomes clear that this topology requires a lot more components that the previous topologies. However, the addition of the extra switching leg makes this topology capable of handling unbalanced loads. Like the previous single-phase converters, the  $1\phi 3W$  also requires a separate converter cell for each output phase.
# 2.5.1.4 Conventional Three-Phase Converter

The Conventional Three-Phase Converter consists of three parallel-connected half-bridge converters. Each half-bridge (also called phase-leg) generates an output voltage, which is shifted with 120° with respect to its predecessor[57]. This topology does not require a separate DC source for each phase, which is an advantage, compared to the single-phase topologies.

# 2.5.1.5 Three-phase Four-Leg Converter

One problem faced with the conventional three-phase converter is the unequal voltage sharing between the capacitors. This requires large DC-link capacitors or an extra voltage balancing control scheme. The Three-phase Four-Leg (3P4L) Converter overcomes this problem by adding another switching leg. The addition of the fourth leg allows control over the neutral current, which results in a lower DC-link voltage and lower RMS capacitor current. A drawback is that this topology requires a much more complicated control scheme[58].

# 2.5.1.6 Discussion

A short comparison is presented in this section in order to select the best suited topology.

	Switches	Main advantage	Main disadvantage
Half-Bridge	6	Low number of switches	Voltage unbalance
Full-Bridge	12	Lowest DC-link voltage	issues[58]
1 <b>\$</b> 3W	18	Can handle unbalanced loads	Large number of switches
3 phase converter	6	Simple circuit and control	DC-link unbalance
3P4L	8	Can handle unbalanced loads	Complex control

 Table 2.5: Main advantages and disadvantages of the different DC-AC topologies

Table 2.5 shows that the three-phase four-leg converter is capable of handling unbalanced loads while keeping the number of switches to a minimum. This makes the 3P-4L converter the most suited DC-AC topology for the SST.

# 2.5.2 Modulation

The modulation methods available for the 3P4L converter were originally developed for the conventional three-phase converter. The three major modulation methods available for the 3P4L converter are:

- 3D Space Vector Modulation
- Continuous Pulse Width Modulation
- Discontinuous Pulse Width Modulation

# 2.5.2.1 3D Space Vector Pulse Width Modulation

The 3D Space Vector Pulse Width Modulation (3D-SVPWM) is an extension of the 2D space vector modulation. The 3D-SVPWM method generates an output voltage vector based on a combination of the phase-to-neutral and zero vector in abc or in the  $\alpha\beta\gamma$  coordinates. The selection of the output vector allows a good compromise between switching losses and harmonic content. However, this method is requires complex calculations and therefore requires a lot of computation power[59].

#### 2.5.2.2 Continuous Pulse Width Modulation

The Continuous Pulse Width Modulation (CPWM) is an adaptation of the CPWM for three-leg inverters. The PWM signals are generated by comparing the phase-voltages and the neutral phase-voltage to a triangular carrier waveform. The simple algorithm of the CPWM allows for easy implementation with very low hardware requirements[59][60]. However, compared with other modulation methods, CPWM may result in higher switching losses[61]. The implementation of CPWM in Figure 2.39 shows that this method only requires the conventional abc duty cycle in order to generate the IGBT gate signals.

#### 2.5.2.3 Discontinuous Pulse Width Modulation

The Discontinuous Pulse Width Modulation (DPWM) uses discontinuous waves. During each carrier cycle one phase ceases modulation and its associated phase is clamped to the positive or negative DC value[62]. This enables the generation of an output with low switching losses and low distortion at high line-voltages. However, most DPWM methods require the phase angle of the output voltage or current, thus resulting in a more computational intense system[62][63].



 $\overbrace{[0,\infty]}^{\text{tr}}$ 

#### 2.5.2.4 Discussion

Three modulation methods have been presented for the 3P-4L converter. In order to select the best modulation method for this converter, a short discussion will follow in this section.

	Implementation	Switching losses
<b>3D-SVPWM</b>	Complex	Modest
CPWM	Easy	Modest
DPWM	Complex	Low

Table 2.6: Comparison between modulation methods for the 3P-4L converter

The 3D-SVPWM and DPWM are difficult to implement because of their high computation requirements. The CPWM on the other hand, has very low hardware requirements and an easy algorithm (Figure 2.39), which makes it very suitable to use for the 3P4L converter.

# 2.6 Summary

The usage of renewable and distributed energy generation is expected to increase in the future. To quickly and efficiently manage the changing sources and loads, the SST can be used to dynamically adjust the energy distribution in the grid. In preparation of this scenario, many research groups have developed and investigated different architectures and topologies for the SST. Since there is no consensus over which is the most suited for grid applications, an independent review is presented in this chapter. The chosen SST structure of the SST consists of an AC-DC, DC-DC and DC-AC stage for optimal control of the power, voltages and currents. The available topologies and modulation methods for each stage are investigated in order to choose a suitable candidate. The chosen topologies and modulation methods are:

- CHB topology for the AC-DC stage because of its modular structure and ability to handle voltages higher than commercial IGBTs
- PS-PWM as a modulation method for the CHB because of its simplicity
- DAB topology for the DC-DC conversion stage because of its efficiency and compactness
- Phase shift modulation for the DAB for its simplicity
- 3P4L converter for the DC-AC stage because of its ability to handle unbalanced loads while keeping the numbers of IGBTs to a minimum
- CPWM for the 3P4L converter because of its easy implementation

The following chapters will apply the chosen topologies and modulation methods to a case study for further investigation of the SST.

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# Chapter 3 FIRST ORDER DESIGN OF THE SST

To investigate how the SST behaves under certain conditions, a model of the SST needs to be constructed first. Creating this model requires the values of several parameters, such as switching frequencies and ratings of passive components. This model is normally achieved through a detailed design process. However, since this research is only interested in the dynamic behavior of, a first order design of the SST is sufficient. The first order design offers a rough estimate of the parameter values, and does not take factors such as losses and design optimization into account.

The main purpose of this chapter is to determine the essential parameter values required for a first order design of the SST. The first section gives an overview of the requirements, specifications and assumptions made while designing the SST; followed by a short description on distortion and filters. Analysis for parameter selection of the Cascaded H-Bridge, the Dual-Active Bridge and the Three-Phase Four-Leg Converter are given in subsequent sections. The converter equations are then applied to a specific case and the SST waveforms are validated through simulations. Finally, the overall circuit of the SST is presented and its modularity is discussed.

# 3.1 System Requirements, Specifications and Assumptions

The calculations for the first order design are based on specifications given for a case study. Parameters that are not specified or can't directly be calculated from specified values will be chosen based on the requirements and assumptions.

# 3.1.1 Requirements

The main requirement is that the SST should operate at a medium voltage level on one side and at a low voltage on the other side. Furthermore, the SST should be capable of operating in the presence and absence of a low-voltage grid. These modes of operation are known as grid connected and standalone mode respectively and are shown in Figure 3.1.

Other requirements for this research are:

- Fast dynamic response
- Power transfer possible in all four quadrants
- IEEE compliant harmonic content
- The calculated parameters should allow practical implementation and scalability of the SST



Figure 3.1: Required modes of operation. (a) Grid connected. (b) Standalone mode

#### 3.1.2 Specifications

The minimal parameters that need to be specified for the SST are:

- Rated Power P<sub>rated</sub>
- Line-to-Line Medium Voltage V<sub>MV</sub>
- Line-to-Line Low Voltage  $V_{LV}$
- Grid Frequency f<sub>grid</sub>

Another specification of importance is the voltage rating of available power electronic switches. These ratings determine the restrictions for voltage levels and will also determine the number of H-Bridges in the CHB.

# 3.1.3 Assumptions

As stated in the introduction of this chapter, the first order design makes some assumptions. These assumptions allow for simple calculation and approximation of the parameter values. Unless specified otherwise, the assumptions made are:

- The components are lossless
- The switches turn on and off instantaneously
- The passive components operate within a linear region and phenomenon such as saturation are avoided

Another assumption made is about the maximum power transfer. The requirements state that the SST should be capable of power transfer in all four quadrants. In other words, the SST should be capable of active and reactive power flow. When only the rated active power is given in the SST specifications, the assumption is made that at unity power flow the rated active power equals the maximum apparent power. In other words:

$$S_{max} = P_{rated}$$
; for  $cos(\varphi) = 1$  (3.1)

Where S<sub>max</sub> is the maximum apparent power through the SST

 $cos(\phi)$  is the angle between the active power and apparent power vector

Rewriting (3.1) for any value of S and  $cos(\phi)$  yields:

$$|S| = \sqrt{P^2 + Q^2} \le |P_{rated}| \tag{3.2}$$

Where S, P and Q are respectively the apparent, active and reactive power through the SST The desired operation area of the SST is shown in the red shaded area of Figure 3.2.



# 3.2 Waveform distortions and filters

# 3.2.1 Waveform distortions

The switching action of the power electronics in the SST cause its operation to be accompanied by distorted voltages and currents. This distortion causes power losses, heating in electrical equipment, oscillations in rotating machines, power cables and capacitors[1].

The total distortion caused by a waveform is called the Total Harmonic Distortion (THD) and defined as the ratio between the RMS value of all the harmonics to the RMS value of the fundamental harmonic[1]. Another term that can be used as a measurement for harmonic distortion is the Total Demand Distortion (TDD). The calculation of the TDD is the same as the THD; however, the value of TDD is determined under full load conditions, whereas the THD can be calculated under any condition. Since the current varies with the load, the TDD can be used to give a clear definition of the current distortion in a system.

The IEEE recommendations for distortion levels are defined in the IEEE 519-1992 standard[1] and are the levels for which the SST will be designed. The recommended limits for the voltage and currents are presented in Table 3.1[1]. Since the short circuit current at the PCC is unknown, the ratio of short circuit- and load current is assumed to be smaller than 20. This ensures compatibility of the SST with any value of  $I_{SC}$ . The distortion limit enforced for the SST will also be set to 80% of the IEEE values; this allows the SST to operate at a safe level below the IEEE limits.

$I_{SC}$ / $I_{L}$	<b>h</b> < 11	$11 \le h \le 17$	$17 \le h \le 23$	$23 \le h \le 35$	35≤h	TDD
< 20	4	2	1	0.6	0.3	5
20 < 50	7	3.5	2.5	1	0.5	8
50 < 100	10	4.5	4	1.5	0.7	12
100 < 1000	12	5.5	5	2	1	15
> 1000	15	7	6	2.5	1.4	20

Table 3.1: IEEE Standards for Current Distortion Limits for odd harmonics in percent of IL. Evenharmonics are limited to 25% of the odd harmonic limit[1].

Where  $I_{SC}$  is the maximum short circuit current at the point of common coupling (PCC)  $I_L$  is the maximum demand load (at fundamental frequency) at PCC h is the harmonic order

# 3.2.2 Grid Filters

The SST is connected to the high- and low-voltage grid through a filter. These filters have two functions. Their first function is to allow control of active and reactive power control between the SST and the grid. The second function is to reduce the harmonic distortion generated by the SST[2].

The three most common types of filters are [3]:

• L-filter

The L-filter shown in Figure 3.3(a) is the most basic filter, providing a damping of -20 dB over the whole range. In order to sufficiently attenuate the harmonic content, this filter must be used for a converter operating at a high switching frequency.

• LC-filter

The LC-filter in Figure 3.3(b) uses a shunt capacitor to achieve an attenuation of -40 dB. The LC-filter is suited for configurations where the load impedance across the capacitor is relatively high and above the switching frequency.

• LCL-filter

The LCL-filter shown in Figure 3.3(c) provides an attenuation of -60 db for frequencies larger than the resonance frequency of the filter. This filter achieves reduced levels of harmonic distortion with lower switching frequencies and with smaller passive elements. On the other hand, the LCL-filter can cause dynamic and steady state current distortion due to resonance.



Figure 3.3: Types of filters (a) L-filter (b) LC-filter (c) LCL-filter

The SST requires two filters:

- 1. One to couple the CHB to the MV-grid
- 2. One to couple the 3P4L converter to the LV-grid or load

# Filter for the CHB

A simple L-filter can be used for to couple the CHB to the MV-grid. There are two main reasons why the filter type can be used for this purpose:

- 1. The structure of the CHB and its modulation scheme result in a high effective switching frequency as the number of H-Bridges increase. An increase of H-Bridges also creates a more sinusoidal waveform. These two properties result in reduced harmonic distortion and require smaller filters[4]. The high effective switching frequency ensures proper filtering operation, while its small size requirement ensures a low voltage drop the filter inductor.
- 2. A high-voltage capacitor is rather expensive. In order to reduce costs, a filter with a capacitor is to be avoided whenever possible

# Filter for the 3P4L converter

The 3P4L converter has a high power and low-voltage rating. The

The 3P4L converter has a high power and low-voltage rating. This results in a high current flow through the 3P4L converter. At high current levels the switching frequency is often kept at a low value in order to limit the switching losses. A simple L-type filter would not be sufficient to reduce the harmonic distortions and meet grid standards. Moreover, lower switching frequencies require higher filter inductances. These increase costs more and also result in poor dynamic behavior[5].

L- and LC-type filters are useful when the system is connected to a fixed grid impedance. The LV-side of the SST is required to operate at both grid connected and standalone mode and therefore observes different impedance in each mode. Designing a L- or LC-type filter for a

specific operation mode leads to insufficient harmonic attenuation at the other mode[6]. The LCL-type filter does not suffer from this drawback and is therefore suited for the 3P4L converter.

The LCL-type filter reduces harmonic distortion over the whole spectrum and provides - 60dB filtering for frequencies above its resonance frequency. It also results in much smaller filter component values, resulting in a lower voltage drop compared to the L-type filter. This is another advantage of using the LCL-filter for the 3P4L converter.

As mentioned before, an LCL-type filter may cause current distortion due to resonance. Damping is required in order to avoid these distortions. There are two types of damping[7]:

1. Passive damping

Passive damping uses additional L, C or R elements in series or parallel with the filter capacitor. Passive damping results in lower system efficiency, because of the losses introduced by the damping elements. Passive damping also reduces the filter effectiveness, because it is very difficult to apply damping to only those frequencies where resonance can occur.

2. Active damping

Active damping consists of modifying the controller structure by adding an additional branch to the existing control scheme. Active damping does not produce losses, but are more sensitive to parameter uncertainties.

To keep the system losses to a minimum, an active damping scheme will be used for the 3P4L converter.

# 3.2.3 DC-link Capacitance

The SST contains two DC-links, one between the Cascaded H-Bridge and Dual-Active Bridge and another one between the Dual-Active Bridge and the Three-Phase Four-Leg converter (Figure 3.4).



The rectified voltage from the CHB to the DAB through DC-link(1) is not a constant voltage and neither is the voltage through DC-link(2). Filter capacitors are used in order to achieve a smooth DC-voltage at the DC-links. An infinite large capacitance would yield a DC-voltage with a constant value[8]. Since only a finite value of the capacitance is possible in practice, the DC-link is allowed to have a small voltage ripple. In practice, the peak-to-peak ripple in the DC-link is limited to 10%[9]. For The minimum capacitance for rectified sinusoidal waveforms, such as those from the CHB and 3P4L converter, can be calculated using[8]:

$$C_{min-sin} = \frac{P}{2 * \pi * f * V_{DC} * \Delta V}$$
(3.3)

Where  $C_{\min-\sin}$  is the minimum capacitance value for a DC-voltage with sinusoidal ripple

f is the sinusoidal frequency

P is the power through the DC-link

VDC is the DC-link voltage

 $\Delta V$  is the peak-to-peak DC-link ripple voltage

Additional capacitors are needed on both sides of the DAB for smoothing the voltage waveforms generated as a result of its switching actions. The proposed value for the minimum capacitance for the DAB according to [10] equals:

$$C_{min-DAB} = \frac{50 * P}{V_{DC}^2 * f_{sw}}$$
(3.4)

Where P is the power through the DC-link

 $C_{min-DAB}$  is the minimum DC-link capacitance for the DAB  $V_{DC}$  is the DC-link voltage  $f_{sw}$  is the switching frequency

# 3.3 Cascade H-Bridge

The Cascaded H-Bridge is used to convert the AC input voltage to a rectified DC voltage. It consists of an input filter, several H-Bridges in cascade and an output filter capacitance for each H-Bridge (Figure 3.5). Furthermore, each H-Bridge is connected to a control circuit, which switches the IGBTs on or off in order to get the desired waveform. The parameters that are required to create a model of the CHB are:

- Number of H-Bridges
- DC-link voltage
- Filter capacitor
- Grid filter
- Switching frequency

#### 3.3.1 Power Control

In order to analyze the power transfer between the grid and the CHB, a single-phase representation of the relationship between grid and CHB can be derived by considering only the fundamental harmonics. This replaces the CHB circuit with a single AC-voltage source as shown in Figure 3.6. The vector relationship of the parameters in Figure 3.6 is shown in Figure 3.7.

The equations of the power flow between the MV-grid and the CHB can be derived using vector analysis of Figure 3.7. The resulting equations are:

$$P = 3 * V_{ph-MV} * I_{ph-MV1} * cos(\varphi)$$
  
= 3 \* V<sub>ph-MV</sub> \*  $\frac{V_{CHB1} * sin(\delta)}{2 * \pi * f_{grid} * L_{CHB}}$  (3.5)  
$$Q = 3 * V_{ph-MV} * I_{ph-MV1} * sin(\varphi)$$
  
= 3 \* V<sub>ph-MV</sub> \*  $\frac{V_{ph-MV} - V_{CHB1} * cos(\delta)}{2 * \pi * f_{grid} * L_{CHB}}$  (3.6)

Where P is the active power flowing between the MV-grid and the CHB

Q is the reactive power flowing between the MV-grid and the CHB



Figure 3.5: One of three identical phases in an n-modules Cascaded H-Bridge

Where  $V_{ph-MV}$  is the phase-to-neutral MV grid voltage  $I_{ph-MV}$  is the current through the inductor  $V_{CHB}$  is the voltage on the AC side of the CHB  $V_{DAB1}$  is the voltage over DC-link(1)  $L_{CHB}$  is the filter inductor  $S_x$  is an IGBT switch  $C_{CHB}$  is the DC-link capacitor



Where  $V_{CHB1}$  is the fundamental voltage over the CHB  $I_{ph-MV1}$  is the fundamental current through the inductor



Figure 3.7: Vector relationship between voltages and current (a) Arbitrary current (b) Power flow from CHB to MV-grid at unity power factor (c) Power flow from MV-grid to CHB at unity power factor

Where  $\varphi$  is the angle between the MV-grid voltage- and current  $\delta$  is the angle between the MV-grid voltage and the CHB voltage

The value of  $V_{ph-MV}$  and  $f_{grid}$  is fixed by the MV-grid, while the load determines the value of current  $I_{ph-MV}$ . In order to adjust the amount of active and reactive power flow, the angle  $\phi$  needs to be altered. This can be done by adjusting the voltage  $V_{CHB1}$  or  $\delta$ . By adjusting the angle  $\delta$  and the modulation index (3.7) of the CHB, the active and reactive power flow between the grid and the CHB can be adjusted.

$$m_{a-CHB} = \frac{\sqrt{2} * V_{CHB1}}{N_m * V_{DAB1}}$$
(3.7)

Where  $m_{a-CHB}$  is the modulation index of the CHB  $N_m$  is the number of parallel H-Bridges

# 3.3.2 DC-link voltage and Number of H-Bridges

The CHB consists of cascaded connected H-Bridges. An increase of H-Bridges leads to a better waveform[4], however, the addition of each H-Bridge requires an extra DAB converter with HF transformer. This increases the overall system volume, complexity and cost. For this reason, the number of H-Bridges should be kept to a minimum.

The DC-link voltage is restricted by two values:

1. The lower limit is set by the DC-link voltage ripple

The voltage ripple is limited to 10%. Assuming the voltage drop over the inductor is zero, the peak AC-voltage over each H-Bridge should be a maximum of 95% of the DC-link voltage. The AC-voltage should be kept below 95% in order to avoid overlap of the DC-ripple and the AC-voltage.

2. The upper limit is set by the voltage rating of available IGBT switches

The voltage across the DC-link cannot be larger than the rated value of the IGBT. In practice a safety margin of 20% is taken into account, limiting the upper value of the DC-link voltage to 80% of the rated IGBT voltage.

A drawing of the limitations set for the DC-link voltage is shown in Figure 3.8.



Figure 3.8: Limitations for the DC-link voltage (a) Lower Limit (b) Upper Limit

Where V<sub>peak-IGBT</sub> is the peak voltage over the IGBT

V<sub>rated-IGBT</sub> is the rated IGBT value

 $V_{peak-ph-MV}$  is the peak voltage of  $V_{ph-MV}$ 

Margin in V<sub>DAB1</sub> is the margin between the maximum and minimum DC-link voltage

As stated before, the maximum DC-link voltage is limited by the rated IGBT voltage, and can be calculated using:

$$V_{DAB1-max} = \frac{80}{105} \% * V_{rated-IGBT}$$
(3.8)

The peak-phase voltage and the number of modules limit the minimum DC-link voltage. This voltage can be calculated using:

$$V_{DAB1-min} = \frac{100}{95} \% * \frac{\sqrt{2} * V_{ph-MV}}{N_m}$$
(3.9)

And the number of modules can be calculated using:

$$N_m = \operatorname{ceil}\left(\frac{100 * \sqrt{2} * V_{ph-MV}}{95 * V_{DAB1-max}}\right)$$
(3.10)

Where ceil is the function that rounds the value between the brackets upwards to the next highest integer.

Figure 3.8 shows that there is a margin between  $V_{DAB-min}$  and  $V_{DAB-max}$ . This margin can be used to choose the DC-link voltage in such a way that an optimal winding ratio for the transformer of the Dual-Active Bridge can be achieved.

#### 3.3.3 Filter Capacitor

The value of the capacitance, needed for a smooth DC-link voltage, can be calculated using equation (3.3). Assuming the power is evenly distributed among the three phases and several H-Bridges, the equation for the rectified power per phase, per H-Bridge becomes:

$$P = \frac{1}{3} * \frac{P_{rated}}{N_m} \tag{3.11}$$

Setting the voltage ripple to 10% and using equation (3.11) into (3.3), gives the equation for  $C_{CHB}$ :

$$C_{CHB} = \frac{\frac{1}{3} * \frac{P_{rated}}{N_m}}{2 * \pi * f_{grid} * (0.1 * V_{DAB1}) * V_{DAB1}} = \frac{P_{rated}}{0.6 * N_m * \pi * f_{grid} * V_{DAB1}^2}$$
(3.12)

#### 3.3.4 Carrier frequency and filter inductor

The values of the carrier frequency  $f_{CHB}$  and filter inductor  $L_{CHB}$  are determined based by the harmonic distortion caused by the CHB. A higher carrier frequency results in lower harmonic distortion, but also increases the switching losses. A higher inductance  $L_{CHB}$  reduces the harmonic distortion, but at the same time increases the inductor size, cost and the voltage drop over that inductor.

In order to get an idea of where the highest switching distortion occurs, the structure and modulation scheme of the CHB needs to be taken into account. The CHB is modulated using a Phase-Shifted PWM (PS-PWM) scheme. Each H-Bridge is assigned two carrier signals with a frequency of  $f_{CHB}$ . Due to the nature of the PS-PWM scheme, the effective switching frequency of the CHB is:

$$f_{CHB-effective} = 2 * N_m * f_{CHB}$$
(3.13)

Where  $f_{\text{CHB-effective}}$  is the CHB effective switching frequency  $f_{\text{CHB}}$  is the carrier frequency

The stringent levels for the harmonic distortion set by the IEEE is imposed for frequencies above the 35<sup>th</sup> harmonic, which is at 1750Hz for a grid frequency of 50Hz. According to equation (3.13), a switching frequency of 900Hz will produce distortions above the 35<sup>th</sup> harmonic.

Since the recommended distortion level for every harmonic above the  $35^{th}$  is the same, it is useful to analyze the individual distortion levels for these harmonics first. When a combination of  $f_{CHB}$  and  $L_{CHB}$  is found that reduces the distortion for harmonics above the  $35^{th}$  to the desired levels, the next step is to determine if that combination of  $f_{CHB}$  and  $L_{CHB}$  also reduces the individual distortion below the  $35^{th}$  harmonic. Finally, the THD should be determined. If the THD is also below the desired levels, that combination of inductance and frequency is suited for the CHB. A flowchart of the process is shown in Figure 3.9.

It is clear that several combinations of  $f_{CHB}$  and  $L_{CHB}$  may result in IEEE compliant distortion levels. In such cases the designer has to choose a suitable combination based on other factors such as size and weight of the inductor, voltage drop and switching losses.



Figure 3.9: Selection of filter inductor  $L_{CHB}$  and carrier frequency  $f_{CHB}$ 

# 3.4 Dual-Active Bridge

The Dual-Active Bridge is used to achieve galvanic isolation between the high- and lowvoltage side of the SST. It consists of a DC/AC-AC/DC converter with a high-frequency transformer in between. An n-module DAB circuit is shown in Figure 3.10. The number of DAB modules is equal to the number of H-Bridges in the CHB. Each DAB module is connected to a single H-Bridge from the CHB. The outputs of the DABs are all connected to a DC-bus. The parameters required to create a DAB model are:

- Transformer turns-ratio n<sub>Tr</sub>
- Switching frequency  $f_{DAB}$
- Leakage inductance L<sub>DAB</sub>
- Filter capacitors C<sub>DAB1s</sub> and C<sub>DAB2</sub>

#### 3.4.1 Power Control

The DAB uses the Phase Shift method to control the flow of power between the high and lowvoltage side of the transformer. The equivalent circuit of the transformer is shown in Figure 3.11[11]. For analytical purposes, the small series resistances and large parallel branches can be neglected. This allows for summation of both leakage inductances as presented in equation (3.14) and results in a simplified circuit as shown in Figure 3.12[12].



Figure 3.10: N-module Dual-Active Bridge



Figure 3.11: Transformer equivalent circuit

(3.14)

Where  $V_{ac-DAB1}$  is the primary transformer side voltage  $V_{ac-DAB2}$  is the secondary transformer side voltage  $R_{DAB1}$  is the resistance of the primary winding  $R_{DAB2}$  is the resistance of the secondary winding  $L_M$  is the magnetizing inductance of the transformer  $R_c$  is the magnetic core resistance  $L_{DAB1}$  is the leakage inductance of the primary winding  $L_{DAB2}$  is the leakage inductance of the secondary winding



Figure 3.12: Simplified circuit of the DAB transformer

Where  $I_{L-DAB}$  is the current through the inductor  $L_{DAB}$ 

L<sub>DAB</sub> is the primary referred leakage inductance of the transformer [13]

The Phase Shift modulation scheme works by adjusting the phase shift between the voltage  $V_{ac-DAB1}$  and  $V_{ac-DAB2}$  as shown in Figure 3.13. When the losses are neglected, the transferred power through the DAB equals[14]:

$$P_{DAB} = \frac{n_{Tr} * V_{DAB1} * V_{DAB2}}{2 * f_{DAB} * L_{DAB}} * D_{DAB} (1 - D_{DAB})$$
(3.15)

Where P<sub>DAB</sub> is the power transferred through the DAB

 $f_{DAB}$  is the DAB switching frequency

 $D_{\text{DAB}}$  is the duty cycle or phase-shift of the DAB

 $V_{\text{DAB1}}$  is the voltage of the DAB on the CHB-side

 $V_{\text{DAB2}}$  is the voltage of the DAB on the 3P4L converter side

The duty cycle is based on half the switching period and is calculated using[14]:

$$D_{DAB} = \frac{t_{on-DAB}}{\frac{T_{s-DAB}}{2}}$$

$$= 2 * t_{on-DAB} * f_{DAB}$$
(3.16)

Where  $t_{on-DAB}$  is the time-delay before the low-voltage H-Bridge is switched on  $T_{s-DAB}$  is the switching period of the DAB



Figure 3.13: Input and output transformer voltages of the DAB

Assuming the power through the SST is evenly distributed among the several DAB modules, the rated power per DAB module is:

$$P_{DAB-rated} = \frac{1}{3} * \frac{1}{N_m} * P_{rated}$$
(3.17)

Where P<sub>DAB-rated</sub> is the rated power of the DAB

N<sub>m</sub> is the number of H-Bridges in the CHB

#### 3.4.2 Soft switching operation

One of the main reasons the DAB topology was chosen, was because of its soft switching capabilities. Soft switching means that the IGBT switches turn-on and off at either zero voltage or at zero current. This results in neglectable switching losses and allowing high switching frequencies and small transformer dimensions. In order to take advantage of the soft switching properties of the SST, the operating range of the DAB has to be in a certain region. In order to identify that region, the parameter DC-conversion ratio is introduced. This parameter is also called the normalized output voltage and is defined as[13]:

$$DC - ratio = \frac{n_{Tr} * V_{DAB2}}{V_{DAB1}}$$
(3.18)

As shown in Figure 3.14 and Figure 3.15, the variation of d causes the DAB to go from the soft switching to the hard switching region. The hard switching region is to be avoided, because the switching operation in that region does not occur at zero voltage- or current. This introduces unwanted switching losses.



For Figure 3.14 and Figure 3.15 and [13]:

$$I_{DAB2(pu)} = \frac{I_{DAB2}}{V_{DAB1} * n_{Tr} * 2 * \pi * f_{DAB} * L_{DAB}}$$
(3.19)  
$$P = \frac{d(pu)}{(3.20)}$$

$$R = \frac{u(pu)}{I_{DAB2(pu)}}$$

In order to avoid the hard switching region, the DC-conversion ratio d should ideally be equal to one. This gives a full range of soft switching operation, as can be seen in Figure 3.14 and

Figure 3.15. This can be achieved by keeping the voltage on both sides of the DAB as constant as possible.

#### 3.4.3 Transformer turns-ratio

The transformer of the DAB provides the required isolation and voltage matching between the high- and low-voltage sides of the DAB. Its leakage inductance is used as an instantaneous energy storage device[15]. The turns-ratio of the transformer is defined as  $n_{Tr}$  and gives the relationship between the high- and low-voltage as[11]:

$$n_{Tr} = \frac{V_{DAB1}}{V_{DAB2}} \tag{3.21}$$

The values of  $V_{DAB1}$  and  $V_{DAB2}$  are determined by the requirements of respectively the CHB and the 3P4L converter. The value of  $n_{Tr}$  depends on the ratio of these two voltages and can have any arbitrary value. However, for design purposes, it is often preferred to have a transformer turns-ratio with a small numerator and denominator. In other words, it is more preferred to have an  $n_{Tr}$  of 2/3 than on of 245/994. Assuming there is a number Gp, where Gp is defined as:

$$Gp = \frac{V_{DAB1}}{GCD(V_{DAB1}, V_{DAB2})} * \frac{V_{DAB2}}{GCD(V_{DAB1}, V_{DAB2})} \text{ for } \begin{cases} V_{DAB1-min} \le V_{DAB1} \le V_{DAB1-max} \\ V_{DAB1} * V_{DAB2} \end{cases}$$

$$= \frac{V_{DAB1} * V_{DAB2}}{\left(GCD(V_{DAB1}, V_{DAB2})\right)^{2}} \text{ for } \begin{cases} V_{DAB1-min} \le V_{DAB1} \le V_{DAB1-max} \\ V_{DAB2-min} \le V_{DAB2} \le V_{DAB2-max} \end{cases}$$
(3.22)

Where GCD is the Greatest Common Divisor

 $V_{DAB1-min}$  and  $V_{DAB2-min}$  are the minimal value of respectively  $V_{DAB1}$  and  $V_{DAB2}$ 

 $V_{DAB1-max}$  and  $V_{DAB2-max}$  are the maximum value of respectively  $V_{DAB1}$  and  $V_{DAB2}$ 

The optimal transformer turns-ratio occurs at the minimal value of fp. If this minimum value of Gp is known, the optimum transformer turns-ratio can be calculated using

$$n_{Tr} = \frac{V_{DAB1@Gp-min}}{V_{DAB2@Gp-min}}$$
(3.23)

Where  $V_{DAB1@fp-min}$  is the voltage  $V_{DAB1}$  at the minimum value of Gp

V<sub>DAB2@fp-min</sub> is the voltage V<sub>DAB2</sub> at the minimum value of Gp

#### 3.4.4 Switching Frequency

The choice of switching frequency for the DAB requires a detailed design. An optimal switching frequency can be chosen based on the transformer characteristics, switching devices and desired efficiency. Since a detailed design is out of the scope of this research, the results from a previous research are used to determine the switching frequency. Most publications use a switching frequency of 20kHz. This frequency is used for power ratings from 1kW to 1MW [16][17][18][19][20][21][22][23]. This frequency is high enough to prevent the transformer and external inductors from generating acoustic noise[23].

Since a frequency of 20kHz is applicable for a large range of power ratings, this frequency will be used as the switching frequency of the DAB.

#### 3.4.5 Leakage Inductance

The leakage inductance required for operating the DAB can be calculated using (3.15):

$$L_{DAB} = \frac{n_{Tr} * V_{DAB1} * V_{DAB2}}{2 * f_{DAB} * P_{DAB}} * D_{DAB} (1 - D_{DAB})$$
(3.24)

The maximum power transfer through the DAB occurs for  $D_{DAB} = 0.5$ . In this case (3.24) becomes:

$$L_{DAB} = \frac{n_{Tr} * V_{DAB1} * V_{DAB2}}{2 * f_{DAB} * P_{DAB}} * \frac{1}{4}$$

$$= \frac{n_{Tr} * V_{DAB1} * V_{DAB2}}{8 * f_{DAB} * P_{DAB-rated}}$$
(3.25)

If all but  $P_{DAB}$  in (3.25) are fixed, the inductance  $L_{DAB_max}$  is inverse proportional to the maximum transferable power through the DAB. For sufficient bandwidth of the duty cycle  $D_{DAB}$ , the value of  $L_{DAB}$  is restricted to a maximum of 80% of the maximum value of  $L_{DAB}$ , which equals to:

$$L_{DAB\_max} = 80\% * \frac{n_{Tr} * V_{DAB1} * V_{DAB2}}{8 * f_{DAB} * P_{DAB-rated}}$$

$$= \frac{n_{Tr} * V_{DAB1} * V_{DAB2}}{10 * f_{DAB} * P_{DAB-rated}}$$
(3.26)

Where  $L_{DAB-max}$  is the maximum leakage inductance of the DAB transformer  $P_{DAB-rated}$  is the rated DAB power

#### 3.4.6 Filter capacitor

The DAB has two filter capacitors: one at DC-link(1) and the other at DC-link(2). Their values can be calculated with equation (3.4). The value of the capacitor on the CHB side is:

$$C_{DAB1s} = \frac{50 * P_{DAB-rated}}{V_{DAB1}^2 * f_{DAB}}$$
(3.27)

The DC capacitor  $C_{DAB1s}$  is used to smooth out the voltage ripple caused by the switching action of the DAB. This capacitor is in parallel with the capacitor  $C_{CHB}$ , which is used to smooth out the voltage ripple caused by the CHB switching action. The voltage ripple over  $C_{CHB}$  operates at a much lower frequency than that over  $C_{DAB1s}$ . In practice a low-frequency capacitor is used for  $C_{CHB}$ , while a high-frequency capacitor is used for  $C_{DAB1s}$ . However, for analytical purposes,  $C_{CHB}$  and  $C_{DAB1s}$  can be added to simplify analysis. The total capacitance between each H-bridge and DAB equals:

$$C_{DAB1} = C_{CHB} + C_{DAB1s} \tag{3.28}$$

The filter capacitance required for DAB on the side of the 3P4L converter equals:

$$C_{DAB2} = \frac{50 * P_{DAB-rated}}{V_{DAB2}^2 * f_{DAB}}$$
(3.29)

#### 3.5 Three-Phase Four-Leg Converter

The DC-AC stage of the SST has a 3P4L converter that takes the DC voltage from the DAB and converts it into an AC voltage. On the AC-side, the 3P4L converter can be connected either to a LV-grid while operating in grid connected mode, or to a load while operating in standalone mode. The 3P4L converter consists of four half bridges: one per phase and one for the neutral (Figure 3.16). The following parameters are required to create a model of the 3P4L converter:

- DC-link voltage
- Filter capacitor
- Switching frequency and grid filter values



Figure 3.16: Circuit overview of the 3P4L converter

#### 3.5.1 Power Control

By taking only the fundamental output voltage of the 3P4L converter, a single-phase representation can be made for both modes of operation. These representations are shown in Figure 3.17 and can be used to analyze the power flow between the 3P4L converter and its output.



Figure 3.17: Single-line circuits of the 3P4L converter in (a) Grid connected operation (b) Standalone operation

Where V<sub>3P4L1</sub> is the fundamental harmonic phase voltage of the 3P4L converter

 $L_{f1\mathchar`embed{split}}L_{f2\mathchar`embed{split}}L_{f2\mathchar`embed{split}}L_{f1\mathchar`embed{split}}L_{f1\mathchar`embed{split}}L_{f1\mathchar`embed{split}}$  are the passive filter elements

i<sub>1</sub> is the phase current on the output of the 3P4L converter

i2 is the phase current at the grid-side or through the load

V<sub>ph-LV</sub> is the phase-voltage of the grid

 $Z_{load}$  is the load connected to the 3P4L converter when operating in standalone mode

#### Grid connected

Mesh analysis of operation in grid connected mode shown in Figure 3.17(a) gives two equations:

$$-V_{3P4L1} + i_1 * \left( X_{Lf1} + X_{Cf} + X_{LfN} \right) - i_2 * X_{Cf} = 0$$
(3.30)

$$V_{ph-LV} - i_1 * X_{cf} + i_2 * (X_{Lf2} + X_{Cf}) = 0$$
(3.31)

Where  $X_{Lf1} = j * 2\pi f_{grid} * L_{f1-3P4L}$   $X_{Lf2} = j * 2\pi f_{grid} * L_{f2-3P4L}$   $X_{LfN} = j * 2\pi f_{grid} * L_{fN-3P4L}$   $X_{Cf} = \frac{1}{j*2\pi f_{grid}*C_{f-3P4L}}$  $\mathbf{f}_{grid}$  is the grid frequency The voltage V<sub>ph-LV</sub> is fixed by the low-voltage grid and the current i<sub>2</sub> is determined by the load:

$$i_2 = \frac{P}{3 * V_{ph-LV} * \cos(\varphi)}$$
(3.32)

Where P is the load on the output of the SST

 $\phi$  is the angle between the grid voltage  $V_{\text{ph-LV}}$  and current  $i_2$ 

Rewriting (3.30) and (3.31) as function of the current  $i_2$  results in:

$$V_{3P4L1} = \left(\frac{V_{ph-LV} + i_2 * (X_{Lf2} + X_{Cf})}{X_{Cf}}\right) * (X_{Lf2} + X_{LfN} + X_{Cf}) - i_2 * X_{Cf3}$$
(3.33)

The converter voltage  $V_{3P4L1}$  is a complex value that consists of an amplitude and an angle. The power that the SST has to supply to the LV-grid determines the amplitude and angle of this converter voltage.

#### Standalone mode

The same analysis can also be done for standalone operating mode. This leads to the following mesh equations for Figure 3.17(b):

$$-V_{3P4L1} + i_1 * (X_{Lf1} + X_{LfN} + X_{Cf}) - i_2 * X_{Cf} = 0$$
(3.34)

$$-i_1 * X_{Cf} + i_2 * (X_{Cf} + X_{Lf2} - Z_{load}) = 0$$
(3.35)

When operating at standalone mode, the SST is required to provide the same voltage as when operating in grid connected mode. Hence, the voltage over the load impedance  $Z_{load}$  equals the grid voltage  $V_{ph-LV}$ . The current through the impedance can be calculated using these two variables:

$$i_2 = \frac{V_{ph-LV}}{Z_{load}} \tag{3.36}$$

Rewriting (3.34) and (3.35) for the converter voltage V<sub>3P4L1</sub> results in:

$$W_{3P4L1} = \left(\frac{i_2 * \left(X_{Cf} + X_{Lf2} + Z_{load}\right)}{X_{Cf}}\right) * \left(X_{Lf1} + X_{LfN} + X_{Cf}\right) - i_2 * X_{Cf}$$
(3.37)

Equation (3.37) gives the expression for the converter voltage  $V_{3P4L1}$  that is required when impedance  $Z_{load}$  is connected to the output of the SST.

#### 3.5.2 DC-link voltage

The relationship between the DC-link voltage and the fundamental AC-output voltage of a 3P4L converter is[24]:

$$V_{DAB2} \ge \sqrt{3} * \sqrt{2} * V_{3P4L1}$$

$$\ge \sqrt{6} * V_{3P4L1}$$
(3.38)

The capacitor in the LCL-filter of the 3P4L converter causes a voltage drop. This voltage drop should be less than 10% of the grid voltage[25]. A margin of 5% below the DC-link voltage is reserved for the DC-link capacitor ripple. Considering the both margins, the minimum DC-link voltage is:

$$95\% * V_{DAB2-min} = \sqrt{6} * 110\% * V_{ph-LV}$$

$$V_{DAB2-min} = \sqrt{6} * \frac{1.1}{0.95} * V_{ph-LV}$$
(3.39)

Where  $V_{DAB2-min}$  is the minimum required DC-link voltage  $V_{DAB2}$ 

#### 3.5.3 DC-link Capacitor

The DC-link capacitor can be calculated using equation (3.3) can be applied to calculate the second filter capacitor in DC-link(2). Setting the voltage ripple to 10% gives:

$$C_{3P4L} = \frac{P_{rated}}{2\pi f_{arid} * 0.1 * V_{DAB2}^2}$$
(3.40)

#### 3.5.4 Switching Frequency and Grid Filter Values

The switching frequency and filter values are related to each other. Increasing the switching frequency reduces the filter requirements, but also increases the switching losses. Likewise, increasing the filter values, reduces the required switching frequency, but increases the voltage drop over the filter.

An LCL-type filter couples the 3P4L converter to the low-voltage grid or load. This filter should pass the following criteria [1][26][27][28]:

- i. The Total Harmonic Distortion (THD) should comply to the IEEE 1547 norms
- ii. To keep the capacitor  $C_{f\cdot 3P4L}$  to an acceptable size, its value should be less than 5% of the base impedance.
- iii. The voltage drop over the filter should be less than 10% of the grid voltage
- iv. The resonance frequencies should be between ten times the grid frequency  $f_{grid}$  and half the switching frequency  $f_{3P4L}$ . The resonance frequencies should be in this range to avoid resonance problems at the lower and higher parts of the harmonic spectrum

#### Switching frequency

The 3P4L converter operates at low-voltage and has high currents flowing though the converter at rated power. In order to limit the switching losses, the recommended switching frequency is to be kept below 5kHz[7].



Figure 3.18: LCL-filter in (a) abc-domain (b) αβ -domain (c) γ -domain

#### **Grid Filter Values**

The equivalent of the LCL-filter in the abc- and the  $\alpha\beta\gamma$ -frame is shown in Figure 3.18. The LCL-filter causes resonance at  $f_{res-\alpha\beta}$  in  $\alpha\beta$ -frame and at  $f_{res-\gamma}$  in the  $\gamma$ -frame [29]. The difference in resonance frequency is caused by the inductor in the neutral connection, used to filter EMI [30]. From a control point of view, it is desired that both resonance frequencies stay below <sup>1</sup>/<sub>4</sub> of the switching frequency in order to have sufficient bandwidth for the placement of PI controller values. The resonance frequencies  $f_{res-\alpha\beta}$  and  $f_{res-\gamma}$  are equal to[29][31]:

$$f_{res-\alpha\beta} = \frac{1}{2\pi} \sqrt{\frac{L_{f1-3P4L} + L_{f2-3P4L}}{L_{f1-3P4L}L_{f2-3P4L}C_{f-3P4L}}}$$
(3.41)

$$f_{res-\gamma} = \frac{1}{2\pi} \sqrt{\frac{L_{f1-3P4L} + L_{f2-3P4L} + 3L_{fN-3P4L}}{3L_{f2-3P4L}L_{fN-3P4L}C_{f-3P4L} + L_{f1-3P4L}L_{f2-3P4L}C_{f-3P4L}}}$$
(3.42)

In order to achieve the smallest value for  $C_{f\cdot 3P4L}$ ,  $L_{f1\cdot 3P4L}$  should be equal to that of  $L_{f2\cdot 3P4L}$  [32]. Using this property and expressing the LCL-filter parameters in terms of the base impedance  $Z_{base}$ , results in:

$$L_{f1-3P4L} = L_{f2-3P4L} = y\left(\frac{Z_{base}}{2\pi f_{grid}}\right)$$
 (3.43)

$$C_{f-3P4L} = x \left( \frac{1}{2\pi f_{grid} Z_{base}} \right)$$
(3.44)

$$Z_{base} = \frac{V_{ph-LV}^2}{P_{rated}}$$
(3.45)

Specifying  $f_{res-\gamma}$  as a factor of  $f_{res-\alpha\beta}$  and combining equations (3.41)-(3.44) gives the relationships:

$$f_{res-\alpha\beta} = f_{grid} \sqrt{\frac{2}{xy}}$$
(3.46)

$$f_{res-\gamma} = w * f_{res-\alpha\beta} \tag{3.47}$$

$$L_{fN-3P4L} = \frac{2 * L_{f1-3P4L} - (2\pi * f_{res-\gamma})^2 * L_{f1-3P4L}^2 * C_{f-3P4L}}{3 * (2\pi * f_{res-\gamma})^2 * L_{f1-3P4L} * C_{f-3P4L} - 3}$$
(3.48)

To reduce the system dimensions and costs, it is preferred to have low values for the LCLparameters. According to equations (3.46) and (3.47), the LCL-filter parameters are small when  $f_{res \cdot \alpha\beta}$  is large and  $f_{res \cdot \gamma}$  is almost equal to  $f_{res \cdot \alpha\beta}$ . Reduction in the LCL-parameters results in less harmonic filtering, therefore there is an optimal range where harmonic reduction is satisfactory and the LCL-values are minimal.

The proposed algorithm in Figure 3.19 can be used to find suitable values for the LCL-filter. After the switching frequency  $f_{3P3L}$  is chosen, the initial values of  $f_{res-\alpha\beta}$ , x and w are selected so that the filter parameters are minimal. If the first iteration does not yield in suitable results, the values of  $f_{res-\alpha\beta}$ , x and w can be adjusted until the voltage drop and harmonic distortion are within desired limits. If after a certain number of iterations the limits for  $f_{res-\alpha\beta}$ , x and w are reached, the only option left is to increase the switching frequency  $f_{3P4L}$  and start the procedure over.



Figure 3.19: Algorithm to select LCL-parameters

# 3.6 Design Results

The equations presented in the previous subsections are used in this subsection to create a first-order design of an SST for given specifications. These specifications are listed in section 3.6.1 and the associated values of the CHB, DAB and 3P4L converter are given in the subsequent subsections.

# 3.6.1 Solid State Transformer specifications

The specifications, for which the rest of the SST parameters are designed, were presented in Chapter 1 and are shown again in Table 3.2.

Parameter Name	Symbol	Value
Rated Power	P <sub>rated</sub>	1 MW
Medium-Voltage (line-to-line)	V <sub>MV</sub>	10 kV
Low-Voltage (line-to-line)	V <sub>LV</sub>	400 V
Grid Frequency	$\mathbf{f}_{\mathrm{grid}}$	50 Hz

Table 3.2: SST specifications

# 3.6.2 Cascaded H-Bridge

The calculated values for the CHB parameters are shown in Table 3.3. The available IGBT switches for this project were specified with a voltage rating of 800, 1200 and 1700V. A high number of H-Bridges increases complexity of the system. For this reason, a low number of H-Bridges is desired. The selected number of H-Bridges, along with the voltage range for  $V_{DAB1}$  is shown in the highlighted row of Table 3.4. The final DC-link voltage  $V_{DAB1}$  is chosen from Table 3.6. The value of the filter inductor and carrier frequency is determined with the flowchart in Figure 3.9. A graphical representation of the results gained with this flowchart is shown in Figure 3.20 and Figure 3.21. Finally, the voltage waveform is shown in Figure 3.22

and the current waveform along with its harmonic distortion is illustrated in Figure 3.23 and Figure 3.24.

Parameter Name	Symbol	Value	Equation / Figure / Table
Number of H-Bridges	N <sub>m</sub>	7	Equation (3.10); Table 3.4
DC-link voltage	V <sub>DAB1</sub>	1260 V	Table 3.6
Capacitance*	C <sub>CHB</sub>	<b>960</b> μF	Equation (3.12)
Carrier Frequency	$\mathbf{f}_{CHB}$	1050 Hz	Figure 3.9, Figure 3.20,
Inductor Value*	L <sub>CHB</sub>	10 mH	Figure 3.21, Figure 3.24

Table 3.3: CHB parameter values

\* minimum value

IGBT rated voltage (Vrated-IGBT)	Number of H-Bridges	VDAB1-min (V)	VDAB1-max (V)
800	15	573.0	609.5
1200	10	859.5	914.3
1700	7	1227.8	1295.2

Table 3.4: IGBT switches with achievable number modules and voltages







#### 3.6.3 Dual-Active Bridge

The parameter values for the DAB are shown in Table 3.5. The rated power for each DAB module is calculated using equation (3.17) under the assumption that the power through the SST is divided equally amongst the DAB modules.

According to equation (3.22), the minimum value of Gp is 28 for the given range of  $V_{DAB1}$  in Table 3.4 and for  $V_{DAB2-min} < V_{DAB2} < 110\% V_{DAB2-min}$  (equation (3.39)). The possible combinations for  $V_{DAB1}$  and  $V_{DAB2}$  for Gp < 50 are shown in Table 3.6. The value of 1260V puts  $V_{DAB1}$  in the middle of its extremes. For this reason the value for  $V_{DAB2}$  and  $n_{Tr}$  associated with  $V_{DAB1} = 1260V$  are chosen.

The maximum leakage inductance is calculated based on (3.26). Finally, the required filter capacitances are calculated with equation (3.26). The resulting waveforms of the DAB are shown in Figure 3.26 and Figure 3.27.

Parameter Name	Symbol	Value	Equation / Figure / Table
DAB Power	P <sub>DAB</sub>	47.6 kW	Equation (3.17)
Transformer turns-ratio	n <sub>Tr</sub>	4/7	Table 3.6
Switching frequency	<b>f</b> <sub>DAB</sub>	20 kHz	-
Leakage inductance**	L <sub>DAB</sub>	<b>170</b> μF	Equation (3.26), Figure 3.25
Filter capacitor DC-link(1)*	C <sub>DAB1</sub>	75 μF	Equation (3.27)
Filter capacitor DC-link(2)*	C <sub>DAB2</sub>	<b>230</b> μF	Equation (3.29)

Table 3.5: Parameter values for the DAB

\* minimum value

\*\* maximum value

$V_{DAB1}(V)$	$\mathbf{V}_{\mathrm{DAB2}}\left(\mathbf{V}\right)$	Gp	n <sub>Tr</sub>
1232	704	28	4/7
1233	685	45	5/9
1236	721	84	7/12
1239	708	28	4/7
1242	690	45	5/9
1246	712	28	4/7
1248	728	84	7/12
1251	695	45	5/9
1253	716	28	4/7
1260	700	45	5/9
1260	720	28	4/7
1260	735	84	7/12
1265	690	66	6/11
1267	724	28	4/7
1269	705	45	5/9
1274	686	91	7/13
1274	728	28	4/7
1276	696	66	6/11
1278	710	45	5/9
1281	732	28	4/7
1287	693	91	7/13
1287	702	66	6/11
1287	715	45	5/9

Table 3.6: Voltages and transformer turns-ratio minimum value of fp









Figure 3.27: DAB currents at rated power

#### 3.6.4 Three-Phase Four-Leg Converter

The parameters required for the 3P4L converter are shown in Table 3.7. The relationship between the voltage drop, resonance frequencies and switching harmonic distortion from the algorithm in Figure 3.19 is shown in Figure 3.28-Figure 3.31. To keep the voltage drop to a minimum, the value of x is chosen at 4%. As Figure 3.34 and Figure 3.35 show, the reduction in harmonic distortion cause by the LCL-filter is more than sufficient.

Parameter Name	Symbol	Value	Equation / Figure / Table
DC-link voltage	V <sub>DAB2</sub>	720 V	Table 3.6
DC-link(2) capacitor*	C <sub>3P4L</sub>	61.4 mF	Equation (3.40)
x	x	4%	Equation (3.44)
W	w	95%	Equation (3.47)
<i>α</i> β-frame resonance frequency	<b>f</b> <sub>res-αβ</sub>	875 Hz	Equation (3.46)
γ-frame resonance frequency	$\mathbf{f}_{res-\gamma}$	831.2 Hz	Equation (3.47)
Filter inductor	L <sub>f1-3P4L</sub>	83 μΗ	Figure 3.19, Figure 3.28 -
Filter inductor	L <sub>f2-3P4L</sub>	83 μΗ	Figure 3.31
	L <sub>fN-3P4L</sub>	6.7 μΗ	
Filter capacitor	C <sub>f-3P4L</sub>	800 μF	

Table 3.7: Parameters for the 3P4L converter









# 3.7 Overall circuit of the SST

According to Table 3.3, the CHB needs 7 H-Bridges per phase for operating at line-to-line voltage of 10kV. A DAB is connected at the DC-side of each H-Bridge, which equals a total of 21 DABs in the whole SST. The DABs are connected in parallel at  $V_{DAB2}$  and subsequently connected to a 3P4L converter. An overview of this circuit is shown in Figure 3.36.

Although the circuit in Figure 3.36 with 260 IGBTs seems complex, several elements keep repeating. This is the modular nature of the chosen SST topology. There are 21 H-Bridge and DAB couples, along with one 3P4L converter. The chosen topology is scalable for any voltage level on the CHB side. A higher or lower MV-side voltage simply requires an increase or decrease of H-Bridge and DAB modules. The rated power of the SST is also scalable. The power on the MV-side is equally distributed between the different modules. An increase of modules or simply an increase of power handling capabilities of the modules leads to an overall higher power rating in the MV-side. Since the voltage on the LV-side is fixed, an increase in power results in an increase in current rating. In order to handle the higher currents on the LV-side, additional 3P4L converters can be connected in parallel. This distributes the current over the several 3P4L converters, resulting in a lower current rating per converter. The modularity of the SST is shown in Figure 3.37.

The three-stage SST architecture used in this thesis is also used by many other research groups. However, most groups have chosen either a conventional three-phase or a single-phase topology for the DC-AC stage with simple L- or LC-filter [33][34][35][36][37][38]. The architecture as shown in Figure 3.36 and Figure 3.37 with the 3P4L converter in combination with the LCL-filter has not been used.

# 3.8 Summary

The equations and procedures to make a first order design of the SST are presented in this chapter. Practical considerations such as safety margins have been taken into account. This is done, while keeping the equations in a general form for applicability at any specified voltage, current or power level.

A cases study is used in order to determine the different parameters of the CHB, DAB and the 3P4L converter. Simulations show that all three converters perform satisfactory. The harmonic content is kept below IEEE standards while keeping the switching frequency as low as possible.

The final circuit shows the modular nature of the chosen topologies. Although the values are calculated for a specific case, the topology allows expansion to any voltage level and any power rating. The proposed architecture also contains a novel part in its usage of the 3P4L converter in combination with the LCL-filter.



Figure 3.36: Circuit overview of the SST



Figure 3.37: Modular structure of the SST

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# Chapter 4

# MATHEMATICAL MODELS FOR SIMULATION AND CONTROLLER DESIGN

The next step after developing the converter circuit is to design the converter controller and analyze its performance. Simulation software is often used to determine the behavior of a converter and its controller before the hardware model is built. Although software allows rapid prototyping, power electronic circuits often suffer from long simulation times. The reasons for this are[1]:

- The non-linear nature of converter topologies and control circuits require long computational times to generate the simulation waveforms.
- If the converter circuit has a long start-up period, the operation time of the simulated circuit will be quite long in order be able to show its operation at steady-state.
- Addition of a diode, switch or control circuit operating at high frequencies adds additional computational time. As a result, circuits with a large number of switches require a long computational time to generate the switching waveform.

In order to avoid such long simulation times, the complex converter circuit can be replaced with an averaged model. This model approximates the original system by averaging the effect of the fast switching circuit and preserving the low frequency behavior of the converter[2][3]. An example of a current waveform with switching ripple and its average is shown in Figure 4.1.





Although averaged models are useful to study global dynamic behavior of the converter[3], they cannot be used to directly derive the transfer functions required for controller design. The averaged model has to be linearized around a quiescent operation point, in which the harmonics of the modulation or excitation frequency are neglected. Such a linearized model is called a small-signal model[2]. The small-signal model of a diode is shown in Figure 4.2.



There are several ways to average a converter circuit, the methods applied to the SST are[2]:

#### 1. Averaged switch modeling

The idea behind averaged switch modeling is to replace a switch network with its averaged switch network in order to obtain a complete averaged circuit of the converter. The switch network consists of one or more switch and diode pairs, while the averaged switch consists of a controlled voltage and current source. Averaged switch modeling is simple, intuitive and the same model is applicable to many different converter configurations.

#### 2. Mathematical averaging

When the behavior of certain parts within the converter is not required in order analyze the system's waveforms, that part can be replaced with its mathematical equivalent. This is especially useful when the irrelevant parts operate at higher frequencies or contain non-linear elements.

#### 3. State-space averaging

State-space averaging is done by obtaining the differential equations that describe a system. The derivatives of the so-called state variables are expressed as linear combinations of the system's independent inputs and state variables themselves. The advantage of state-space averaging is that the small-signal model is easily obtained from the state-space equations.

This chapter covers the derivation of the averaged model, the small-signal model and the transfer functions for the several parts of the SST. The first section does this for the CHB, the second for the DAB and finally, the third for the 3P4L converter.

#### 4.1 Models for the Cascaded H-Bridge

#### 4.1.1 Averaged Model

In order to derive the averaged model of the CHB, the switching function is averaged over one period and eventually replaced with and averaged switch model. This averaging removes the high-frequency components of the switching waveform, leaving only the fundamental frequency. The average operator can be expressed as [2][4][5]:

$$d = \overline{S}(t) = \frac{1}{T_s} \int_t^{t+T_s} S(\tau) d\tau$$
(4.1)

Where T<sub>s</sub> is the fundamental period

 $S(\tau)$  is the switching function d and  $\bar{S}(\tau)$  are the average switching function, also defined as the duty cycle The value of the voltage  $v_{\text{CHB}}$  and current  $i_{\text{DC-CHB}}$  generated by the single-phase, single-module CHB converter in Figure 4.3 is:



Figure 4.3: Single-phase, single-module CHB converter circuit

Applying the averaging operator (4.1) to (4.2) and (4.3) gives:

$$\overline{v}_{DAB1} = \left(\frac{1}{T_s} \int_t^{t+T_s} S(\tau) d\tau\right) * v_{DAB1} \Leftrightarrow \overline{v}_{DAB1} = d * v_{DAB1}$$

$$\overline{i}_{DC-CHB} = \left(\frac{1}{T_s} \int_t^{t+T_s} S(\tau) d\tau\right) * i_{MV} \Leftrightarrow \overline{i}_{DC-CHB} = d * i_{MV}$$

$$(4.4)$$

Equations (4.4) and (4.5) show that the H-Bridge in Figure 4.3 can be replaced with a controlled voltage source on the AC side and a controlled current source on the DC side of the circuit. All other components remain unchanged. The averaged model of Figure 4.3 is shown in Figure 4.4. Because this model only contains continuous elements, the complexity of the circuit decreases and simulations can be done in the continuous mode. This reduces the required simulation time, but also increases insight into the operation of the converter circuit.



Figure 4.4: Averaged model of a single-phase, single-module CHB converter

The same averaging operator can be applied to the three-phase N-module CHB in Figure 4.5. The voltage and current equations for a three-phase CHB converter circuit are:

$$v_{k-CHB} = \sum_{j=1}^{N_m} S_{kj} * v_{kj-DAB1}$$
(4.6)

$$i_{kj-DC-CHB} = S_{kj} * i_{k-MV}$$
 for  $j = 1 ... N_m$  (4.7)

Where k is phase a, b or c

 $N_{\rm m}$  is the number of H-bridge modules

 $v_{k-CHB}$  is the AC voltage generated by phase k of the CHB  $v_{kj-DAB1}$  is the voltage on the DC side of a H-bridge module  $i_{k-MV}$  is the AC current in phase k  $S_{ki}$  is the switching function for the j<sup>th</sup> H-bridge module in phase k

The average switch equations for Figure 4.6 derived from (4.6) and (4.7) are:

$$\overline{v}_{k-CHB} = \sum_{j=1}^{N_m} d_{CHB-kj} * v_{kj-DAB1}$$
(4.8)

$$\overline{i}_{kj-DC-CHB} = d_{CHB-kj} * i_{k-MV} \text{ for } j = 1 \dots N_m$$
(4.9)

Where  $\overline{v}_{k-CHB}$  and  $\overline{i}_{kj-DC-CHB}$ ,  $d_{kj-CHB}$  are the average values of  $v_{k-CHB}$  and  $i_{kj-DC}$  and  $S_{kj}$ 





The averaged model in Figure 4.6 is still too complicated for controller design and can be simplified based on the following assumptions:

1. The DC-link voltages of the H-bridge modules are equal, in other words:

$$v_{DAB1} = v_{aj-DAB1} = v_{bj-DAB1} = v_{cj-DAB1}$$
 for  $j = 1 \dots N_m$  (4.10)

Where  $v_{DAB1}$  is the average voltage on the DC side of each H-bridge module

2. Each H-bridge module has the same load; therefore the current going through all phases is the same.

$$R_L = R_{L-aj} = R_{L-bj} = R_{L-cj} \text{ for } j = 1 \dots N_m$$
(4.11)

$$i_{MV}| = |i_{a-MV}| = |i_{b-MV}| = |i_{c-MV}|$$
(4.12)

Where R<sub>L</sub> DC load of each H-bridge module

 $|i_{\mbox{\scriptsize MV}}|$  is the amplitude of the AC phase current

3. Since each DC-link voltage is assumed to be equal, all duty cycles in the same phase can also be assumed to be equal. This also allows the controlled voltage sources to be replaced with on controlled voltage source that is  $N_m$  times the value of a single controlled voltage source in Figure 4.6.

$$d_{k-CHB} = d_{k1-CHB} = d_{k2-CHB} = \dots = d_{kNm-CHB}$$
 for  $k = a, b, c$  (4.13)

$$\overline{v}_{k-CHB} = N_m d_{k-CHB} v_{DAB1} \text{ for } k = a, b, c$$
(4.14)

Based on these assumptions, the averaged model in Figure 4.6 can be simplified to that of Figure 4.7.



Figure 4.7: Simplified avared model of an N-module CHB

#### 4.1.2 Small-Signal Model and Transfer Functions

The small-signal model is used to derive the transfer functions that are required to tune the CHB controller. The equations for the small-signal model can be derived from the averaged model in Figure 4.7. The KVL equations for the AC and DC side of the CHB are:

$$N_{m}v_{DAB1} \begin{bmatrix} d_{a-CHB} \\ d_{b-CHB} \\ d_{c-CHB} \end{bmatrix} + L_{CHB} \frac{d}{dt} \begin{bmatrix} i_{a-MV} \\ i_{b-MV} \\ i_{c-MV} \end{bmatrix} + R_{CHB} \begin{bmatrix} i_{a-MV} \\ i_{b-MV} \\ i_{c-MV} \end{bmatrix} - \begin{bmatrix} v_{a-ph-MV} \\ v_{b-ph-MV} \\ v_{c-ph-MV} \end{bmatrix} = 0$$
(4.15)

$$\begin{bmatrix} d_{aj-CHB} & d_{bj-CHB} & d_{cj-CHB} \end{bmatrix} \begin{bmatrix} l_{a-MV} \\ i_{b-MV} \\ i_{c-MV} \end{bmatrix} - 3C_{DAB1} \frac{d}{dt} v_{DAB1} - \frac{3}{R_L} v_{DAB1} = 0$$
(4.16)

Where  $j = 1 \dots N_m$ 

Since the controller will be constructed using PI compensators, equations (4.15) and (4.16) have to be rewritten in the dq-domain using the Park transformation[6]. The resulting equations in the dq-frame are:

$$N_{m}v_{DAB1} \begin{bmatrix} d_{d-CHB} \\ d_{q-CHB} \end{bmatrix} + L_{CHB} \frac{d}{dt} \begin{bmatrix} i_{d-MV} \\ i_{q-MV} \end{bmatrix} - \begin{bmatrix} 0 & L_{CHB}\omega_g \\ -L_{CHB}\omega_g & 0 \end{bmatrix} \begin{bmatrix} i_{d-MV} \\ i_{q-MV} \end{bmatrix} + R_{CHB} \begin{bmatrix} i_{d-MV} \\ i_{q-MV} \end{bmatrix} - \begin{bmatrix} v_{d-ph-MV} \\ v_{q-ph-MV} \end{bmatrix} = 0$$

$$(4.17)$$

$$\begin{bmatrix} d_{dj-CHB} & d_{qj-CHB} \end{bmatrix} \begin{bmatrix} i_{d-MV} \\ i_{q-MV} \end{bmatrix} - 3C_{DAB1} \frac{d}{dt} v_{DAB1} - \frac{R_L}{3} v_{DAB1} = 0$$
(4.18)

Where  $\omega_g = 2\pi * f_{grid}$ 

f<sub>grid</sub> is the grid frequency

Equations (4.17) and (4.18) are time varying signals and need to be linearized around a quiescent operating point in order to construct the small-signal model. This is done by giving the time varying variable x a quiescent value of X plus a superimposed small perturbation  $\hat{x}$ . In other words, the variable x is rewritten with[2]:

$$x = X + \hat{x} \tag{4.19}$$

Applying (4.19) to equations (4.17) and (4.18) gives:

$$N_{m}(V_{DAB1} + \hat{v}_{DAB1}) \begin{bmatrix} D_{d-CHB} + \hat{d}_{d-CHB} \\ D_{q-CHB} + \hat{d}_{q-CHB} \end{bmatrix} + L_{CHB} \frac{d}{dt} \begin{bmatrix} I_{d-MV} + \hat{i}_{d-MV} \\ I_{q-MV} + \hat{i}_{q-MV} \end{bmatrix} \\ - \begin{bmatrix} 0 & L_{CHB} \omega_g \\ -L_{CHB} \omega_g & 0 \end{bmatrix} \begin{bmatrix} I_{d-MV} + \hat{i}_{d-MV} \\ I_{q-MV} + \hat{i}_{q-MV} \end{bmatrix} + R_{CHB} \begin{bmatrix} I_{d-MV} + \hat{i}_{d-MV} \\ I_{q-MV} + \hat{i}_{q-MV} \end{bmatrix} \\ - \begin{bmatrix} V_{d-ph-MV} + \hat{v}_{d-ph-MV} \\ V_{q-ph-MV} + \hat{v}_{q-ph-MV} \end{bmatrix} = 0 \\ \begin{bmatrix} D_{d-CHB} + \hat{d}_{d-CHB} & D_{q-CHB} + \hat{d}_{q-CHB} \end{bmatrix} \begin{bmatrix} I_{d-MV} + \hat{i}_{d-MV} \\ I_{q-MV} + \hat{i}_{q-MV} \end{bmatrix} - 3C_{DAB1} \frac{d}{dt} (V_{DAB1} + \hat{v}_{DAB1}) \\ - \frac{R_L}{3} (V_{DAB1} + \hat{v}_{DAB1}) = 0 \end{bmatrix}$$

$$(4.21)$$

Taking only the DC terms of equation (4.20) into account and rewriting it, gives the quiescent value of the duty cycle for a given current. This equation will later be used for the decoupling between the dq-frame, and as a feed-forward controller.

$$\begin{bmatrix} D_{d-CHB} \\ D_{q-CHB} \end{bmatrix} = -\frac{R_{CHB} - \begin{bmatrix} 0 & L_{CHB}\omega_g \\ -L_{CHB}\omega_g & 0 \end{bmatrix} \begin{bmatrix} I_{d-MV} \\ I_{q-MV} \end{bmatrix} + \begin{bmatrix} V_{d-ph-MV} \\ V_{q-ph-MV} \end{bmatrix}}{N_m * V_{DAB1}}$$
(4.22)

The first order AC terms of equations (4.20) and (4.21) form the small-signal model. Neglecting the second order terms and rewriting the equations (4.20) and (4.21) line-by-line in the Laplace domain gives:

$$N_{m}V_{DAB1}\hat{d}_{d-CHB} + N_{m}\hat{v}_{DAB1}D_{d-CHB} + (sL_{CHB} + R_{CHB})\hat{\iota}_{d-MV} - L_{CHB}\omega_{g}\hat{\iota}_{q-MV} - \hat{v}_{d-ph-MV} = 0$$
(4.23)

$$N_{m}V_{DAB1}\hat{d}_{q-CHB} + N_{m}\hat{v}_{DAB1}D_{q-CHB} + (sL_{CHB} + R_{CHB})\hat{i}_{q-MV} - L_{CHB}\omega_{g}\hat{i}_{d-MV} - \hat{v}_{q-ph-MV} = 0$$
(4.24)

$$D_{d-CHB}\hat{i}_{d-MV} + \hat{d}_{d-CHB}I_{d-MV} + D_{q-CHB}\hat{i}_{q-MV} + \hat{d}_{q-CHB}I_{q-MV} - \left(3C_{DAB1} + \frac{R_L}{3}\right)\hat{v}_{DAB1}$$
(4.25)  
= 0

Where s is the Laplace operator

The relevant transfer functions required to construct the controller are the control-to-outputcurrent and the output-current-to-DC-link-voltage transfer functions. These transfer functions can be constructed from equations (4.23) - (4.25) by setting all other AC variations to zero and keeping only the variables that are of interest.

The control-to-output-current transfer function for the D-frame is:

$$G_{idd-CHB} \begin{vmatrix} \hat{d}_{q-CHB}=0 \\ \hat{v}_{DAB1}=0 \\ \hat{v}_{d-ph-MV}=0 \\ \hat{v}_{q-ph-MV}=0 \end{vmatrix}$$

$$(4.26)$$

Applying the conditions specified in (4.26) to equation (4.23) gives:

$$N_m d_{d-CHB} V_{DAB1} + (sL_{CHB} + R_{CHB}) \hat{\iota}_{d-MV} - L_{CHB} \omega_g \hat{\iota}_{q-MV} = 0$$
(4.27)

To get rid of the variable  $\hat{i}_{q-MV}$  in equation (4.27), the same conditions stated in (4.26) can be applied to (4.24), resulting in:

$$\hat{\iota}_{q-MV} = \frac{-L_{CHB}\omega_g \hat{\iota}_{d-MV}}{sL_{CHB} + R_{CHB}}$$
(4.28)

From (4.26), (4.27) and (4.28) the control-to-output-current transfer function for the d-frame is:

$$G_{idd-CHB} = \frac{\hat{\iota}_{d-MV}}{\hat{d}_{d-CHB}} = -\frac{N_m V_{DAB1} (sL_{CHB} + R_{CHB})}{(sL_{CHB} + R_{CHB})^2 + \omega_g^2 L_{CHB}^2}$$
(4.29)

The analysis for the control-to-output-current transfer function in the Q-frame is the same as in the D-frame and has the same final equation:

$$G_{idq-CHB} \begin{cases} \hat{d}_{d-CHB=0} &= \frac{\hat{l}_{q-MV}}{\hat{d}_{q-CHB}} = -\frac{N_m V_{DAB1} (sL_{CHB} + R_{CHB})}{(sL_{CHB} + R_{CHB})^2 + \omega_g^2 L_{CHB}^2} \\ \hat{v}_{d-ph-MV=0} & \hat{v}_{q-ph-MV=0} \end{cases}$$
(4.30)

The final transfer function of interest is the output-current-to-DC-link-voltage transfer function. This transfer function can be derived from (4.25) by removing the load  $R_L$  and setting the AC variation of the duty cycle and grid voltage in the dq-frame to zero.

$$G_{vid-CHB} \begin{vmatrix} \hat{a}_{d-CHB}=0 \\ \hat{a}_{q-CHB}=0 \\ \hat{v}_{d-ph-MV}=0 \\ \hat{v}_{q-ph-MV}=0 \end{vmatrix}$$

$$(4.31)$$

For the conditions given in (4.31), equation (4.25) gives:

$$D_{d-CHB}\hat{\iota}_{d-MV} + D_{q-CHB}\hat{\iota}_{q-MV} - 3sC_{DAB1}\hat{\nu}_{DAB1} = 0$$
(4.32)

The value of  $\hat{i}_{q-MV}$  from (4.23) with the conditions in (4.31) equals:

$$\hat{\imath}_{q-MV} = -\frac{L_{CHB}\omega_g}{sL_{CHB} + R_{CHB}}\hat{\imath}_{d-MV} - \frac{N_m D_{q-CHB}}{sL_{CHB} + R_{CHB}}\hat{\imath}_{DAB1}$$
(4.33)

Using (4.31), (4.32) and (4.33) to construct the output-current-to-DC-link-voltage transfer function results in:

$$G_{vid-CHB} = \frac{\hat{v}_{DAB1}}{\hat{\iota}_{d-MV}} = \frac{D_{d-CHB}(sL_{CHB} + R_{CHB}) - D_{q-CHB}L_{CHB}\omega_g}{N_m D_{q-CHB}^2 + 3sC_{DAB1}(sL_{CHB} + R_{CHB})}$$
(4.34)

#### 4.2 Models for the Dual-Active Bridge

#### 4.2.1 Averaged Model

The converter circuit for a DAB is shown in Figure 4.8. The power electronic switches operate at a high frequency in the kHz range, resulting in transformer with small dimensions. For dynamic simulations, especially on system level, the transformer currents and voltages are less important compared to other SST waveforms. Simulating multi-kHz waveforms would also require a long computational time.



Figure 4.8: Dual-Active Bridge converter circuit

To speed up simulations, only the DAB input and output voltages are taken into account to derive a mathematical averaged model. The relationship between these parameters can be determined by the power balance. Assuming the DAB is lossless, the relationship between the input and output power is:

$$P_{DAB1} = P_{DAB2} \Leftrightarrow v_{DAB1} i_{DAB1} = v_{DAB2} i_{DAB2}$$
(4.35)

Where P<sub>DAB1</sub> is the power of the DAB on the CHB side

 $P_{DAB2}$  is the power of the DAB on the 3P4L converter side

The power supplied to the DAB is[7]:

$$P_{DAB1} = \frac{n_{Tr} v_{DAB1} v_{DAB2}}{2 f_{DAB} L_{DAB}} d_{DAB} (1 - d_{DAB})$$
(4.36)

Where d<sub>DAB</sub> is the DAB duty cycle

The current flowing on the output side of the DAB can be derived from the relationships stated in equation (4.35) and (4.36):

$$i_{DAB2} = \frac{n_{Tr} v_{DAB1}}{2f_{DAB} L_{DAB}} d_{DAB} (1 - d_{DAB})$$
(4.37)

Likewise, the input current calculated from equations (4.35) and (4.36) is:

$$i_{DAB1} = \frac{n_{Tr} v_{DAB2}}{2f_{DAB} L_{DAB}} d_{DAB} (1 - d_{DAB})$$
(4.38)

The current values in (4.37) and (4.38) are linked to the opposite side of the transformer by means of the voltage value. This allows construction of an averaged model using these two equations, as shown in Figure 4.9.



4.2.2 Small-Signal Models and Transfer Functions

The averaged model of the DAB presented in Figure 4.9 does not contain enough parameters to construct a small-signal model. Another way to derive the small-signal model of the DAB is with the help of state-space averaging. A typical state-space description of a converter is expressed as linear combination independent inputs and the physical state of its energy storage elements, such as capacitor voltages and inductor currents. To construct the state-space averaged model, the state-space description of each switching interval is derived and multiplied with the duty cycle for that interval[2].





#### 4.2.2.1 DAB operating in buck mode

The transformer voltage waveforms for Figure 4.8 are shown in Figure 4.10. When the DAB is operating in buck mode, the power flows from the high-voltage input to the low-voltage output. The equivalent DAB circuit for buck mode during  $t_0$  with the parameters transferred to the secondary side of the transformer is shown in Figure 4.11. For the period  $t_1$ , the DAB circuit is shown in Figure 4.12.



Figure 4.11: DAB circuit for period t<sub>0</sub> in buck mode



Where  $L_{DAB}$ " =  $L_{DAB}/n_{Tr}^{2}$  $R_{DAB}$ " =  $R_{DAB}/n_{Tr}^{2}$ 

To simplify circuit analysis, Figure 4.11 and Figure 4.12 can be reduced to the circuits shown in Figure 4.13 and Figure 4.14. The voltage waveforms in the transformer are symmetrical; hence analysis of only one half of the waveform is necessary.



The circuit equations for Figure 4.13 are:

$$-\frac{v_{DAB1}}{n_{Tr}} + L_{DAB}^{\prime\prime} \frac{d}{dt} i_{DAB2} + R_{DAB}^{\prime\prime} i_{DAB2} - v_{DAB2} = 0$$
(4.39)

$$C_{DAB2} \frac{d}{dt} v_{DAB2} + \frac{v_{DAB2}}{R_{L2}} + i_{DAB2} = 0$$
(4.40)

And the circuit equations for Figure 4.14 are:

$$-\frac{v_{DAB1}}{n_{Tr}} + L_{DAB}'' \frac{d}{dt} i_{DAB2} + R_{DAB} i_{DAB2} + v_{DAB2} = 0$$
(4.41)

$$C_{DAB2} \frac{d}{dt} v_{DAB2} + \frac{v_{DAB2}}{R_{L2}} - i_{DAB2} = 0$$
(4.42)

The energy storage elements in Figure 4.13 and Figure 4.14 are the transformer leakage inductance  $L_{DAB}$  and the capacitor  $C_{DAB2}$ . The state-space variables are therefore the current  $i_{DAB2}$  through the inductance  $L_{DAB}$  and the capacitor voltage  $v_{DAB2}$  over  $C_{DAB2}$ . Rewriting equations (4.39) - (4.42) as state-space equations gives:

$$\frac{d}{dt}x = A_{1}x + B_{1}u \Leftrightarrow \frac{d}{dt} \begin{bmatrix} i_{DAB2} \\ v_{DAB2} \end{bmatrix} = \begin{bmatrix} -\frac{R'_{DAB}}{L'_{DAB}} & \frac{1}{L'_{DAB}} \\ -\frac{1}{C_{DAB2}} & -\frac{1}{R_{L2}C_{DAB2}} \end{bmatrix} \begin{bmatrix} i_{DAB2} \\ v_{DAB2} \end{bmatrix} + \begin{bmatrix} \frac{1}{n_{Tr}L'_{DAB}} \\ 0 \end{bmatrix} v_{DAB1}$$
(4.43)

$$\frac{d}{dt}x = A_2 x + B_2 u \Leftrightarrow \frac{d}{dt} \begin{bmatrix} i_{DAB2} \\ v_{DAB2} \end{bmatrix} = \begin{bmatrix} -\frac{R_{DAB}^{''}}{L_{DAB}^{''}} & -\frac{1}{L_{DAB}^{''}} \\ \frac{1}{C_{DAB2}} & -\frac{1}{R_{L2}C_{DAB2}} \end{bmatrix} \begin{bmatrix} i_{DAB2} \\ v_{DAB2} \end{bmatrix} + \begin{bmatrix} \frac{1}{n_{Tr}L_{DAB}^{''}} \\ 0 \end{bmatrix} v_{DAB1}$$
(4.44)

Equation (4.43) is the state-space equation for Figure 4.13, while (4.44) is the state-space equation for Figure 4.14. The small-signal model for the DAB operating in buck mode can be constructed by substituting these two equations in the general form[2]:

$$s\hat{x} = A\hat{x} + B\hat{u} + \{(A_1 - A_2)X + (B_1 - B_2)U\}\hat{d}$$
(4.45)

Where  $\hat{x}$  is the small AC variation of the state-space variables

 $\hat{u}$  is the small AC variation of the independent variables

 $\hat{d}$  is the small AC variation of the duty cycle

X is the quiescent value of the state-space variables

U is the quiescent value of the independent variables

 $A_1$ ,  $A_2$ ,  $B_1$  and  $B_2$  are the matrixes from equations (4.43) and (4.44)

The matrix A and B in (4.45) are equal to[2]:

$$A = D_{DAB}A_{1} + (1 - D_{DAB})A_{2} \Leftrightarrow A = \begin{bmatrix} -\frac{R_{DAB}^{"}}{L_{DAB}^{"}} & \frac{2D_{DAB} - 1}{L_{DAB}^{"}} \\ -\frac{2D_{DAB} + 1}{C_{DAB2}} & -\frac{1}{R_{L2}C_{DAB2}} \end{bmatrix}$$
(4.46)

$$B = D_{DAB}B_1 + (1 - D_{DAB})B_2 \Leftrightarrow B = \begin{bmatrix} \frac{1}{n_{Tr}L''_{DAB}} \\ 0 \end{bmatrix}$$
(4.47)

Where  $D_{DAB}$  is the quiescent value of the duty cycle

Using equations (4.43) - (4.47) to derive the small-signal model for the DAB operating in buck mode results in:

$$s \begin{bmatrix} \hat{\iota}_{DAB2} \\ \hat{\upsilon}_{DAB2} \end{bmatrix} = \begin{bmatrix} -\frac{R''_{DAB}}{L''_{DAB}} & \frac{2D_{DAB} - 1}{L''_{DAB}} \\ -\frac{2D_{DAB} + 1}{C_{DAB2}} & -\frac{1}{R_{L2}C_{DAB2}} \end{bmatrix} \begin{bmatrix} \hat{\iota}_{DAB2} \\ \hat{\upsilon}_{DAB2} \end{bmatrix} + \begin{bmatrix} \frac{1}{n_{Tr}L''_{DAB}} \\ 0 \end{bmatrix} \hat{\upsilon}_{DAB1} + \begin{bmatrix} \frac{2V_{DAB2}}{L''_{DAB}} \\ -\frac{2I_{DAB2}}{C_{DAB2}} \end{bmatrix} \hat{d}_{DAB}$$
(4.48)

Rewriting equation (4.48) into line-by-line equations for the transfer functions gives:

$$s\hat{\imath}_{DAB2} = -\frac{R_{DAB}^{\prime\prime}}{L_{DAB}^{\prime\prime}}\hat{\imath}_{DAB2} + \frac{2D_{DAB}-1}{L_{DAB}^{\prime\prime}}\hat{v}_{DAB2} + \frac{1}{n_{Tr}L_{DAB}^{\prime\prime}}\hat{v}_{DAB1} + \frac{2V_{DAB2}}{L_{DAB}^{\prime\prime}}\hat{d}_{DAB}$$
(4.49)

$$s\hat{v}_{DAB2} = -\frac{2D_{DAB} + 1}{C_{DAB2}}\hat{\iota}_{DAB2} - \frac{1}{R_{L2}C_{DAB2}}\hat{v}_{DAB2} - \frac{2I_{DAB2}}{C_{DAB2}}\hat{d}_{DAB}$$
(4.50)

The two transfer functions required to tune the DAB controller are the control-to-outputcurrent and the output-current-to-DC-link-voltage transfer functions. The control-to-outputcurrent transfer function derived from (4.49) is:

$$G_{id-buck-DAB}\Big|_{\substack{\hat{v}_{DAB2}=0\\\hat{v}_{DAB1}=0}} = \frac{\hat{\iota}_{DAB2}}{\hat{d}_{DAB}} = \frac{2V_{DAB2}}{sL''_{DAB} + R''_{DAB}} = \frac{2V_{DAB2}}{n_{Tr}^{-2}(sL_{DAB} + R_{DAB})}$$
(4.51)

The output-current-to-DC-link-voltage transfer function derived from equation (4.50) is:

$$G_{vi-buck-DAB}\Big|_{\substack{\hat{v}_{DAB1}=0\\\hat{a}_{DAB}=0}} = \frac{\hat{v}_{DAB2}}{\hat{v}_{DAB2}} = \frac{R_{L2}(-2D_{DAB}+1)}{sR_{L2}C_{DAB2}+1}$$
(4.52)

#### 4.2.2.2 DAB operating in boost mode

The equivalent DAB converter circuits for the DAB operating in boost mode for  $t_0$  and  $t_1$  are shown in Figure 4.15 and Figure 4.16. These are exactly the same as Figure 4.11 and Figure 4.12, with the main difference that all parameters are referenced to the primary side of the

transformer. This means that the transfer functions for the DAB operating in boost mode can be written as those in buck mode with parameters from the primary side. Based on equation (4.51) the control-to-output-current transfer function becomes:

$$G_{id-boost-DAB}\Big|_{\substack{\hat{v}_{DAB2}=0\\\hat{v}_{DAB1}=0}} = \frac{\hat{t}_{DAB1}}{\hat{d}_{DAB}} = \frac{2V_{DAB1}}{sL_{DAB} + R_{DAB}}$$
(4.53)

And based on equation (4.52) the output-current-to-DC-link-voltage transfer function becomes:

$$G_{\nu i-boost-DAB}\Big|_{\substack{\hat{v}_{DAB2}=0\\\hat{d}_{DAB}=0}} = \frac{\hat{v}_{DAB1}}{\hat{v}_{DAB1}} = \frac{R_{L1}(-2D_{DAB}+1)}{sR_{L1}C_{DAB1}+1}$$
(4.54)



Figure 4.16: DAB circuit for period t<sub>1</sub> in boost mode

#### 4.3 Models for the Three-phase Four-Leg Converter

#### 4.3.1 Averaged Model

A 3P4L converter is responsible for power transfer between the DAB and the LV grid. The electrical circuit for this converter is shown in Figure 4.17



The AC voltage generated by a phase-leg of the 3P4L converter is equal to:

$$v_{k-3P4L} = S_{k-3P4L} v_{DAB2} \tag{4.55}$$

Where  $v_{k-3P4}$  is the voltage of phase-leg k with respect to the ground  $S_{k-3P4L}$  is the switching function of phase-leg k k is phase-leg a, b, c or the neural leg N

The current  $i_{DC-3P4L}$  flowing on the DC side as a result of the AC currents equals:

 $i_{DC-3P4L} = S_{a-3P4L}i_{a-3P4L} + S_{b-3P4L}i_{b-3P4L} + S_{c-3P4L}i_{c-3P4L} + S_{N-3P4L}i_{N-3P4L}$ (4.56) Where  $i_{k\cdot 3P4L}$  is the AC current through  $L_{f1\cdot 3P4L}$  for k=a, b, c or the current through the neutral inductor  $L_{fN\cdot 3P4L}$  for k = N

Applying the averaging function from equation (4.1) to (4.55) and (4.56) gives the average value for the DC current and AC voltage generated by the 3P4L converter, namely:

$$\overline{v}_{k-3P4L} = d_{k-3P4L} v_{DAB2}$$
(4.57)

 $i_{DC-3P4L} = d_{a-3P4L}i_{a-3P4L} + d_{b-3P4L}i_{b-3P4L} + d_{c-3P4L}i_{c-3P4L} + d_{N-3P4L}i_{N-3P4L}$ (4.58) Where k is phase-leg a, b, c or the neutral N

 $d_{k-3P4L}$  is the average value or the switching function  $S_{k-3P4L}$ , also called the duty cycle  $\overline{v}_{k-3P4L}$  is the average AC voltage generated by each phase-leg of the 3P4L converter  $\overline{i}_{DC-3P4L}$  is the average current on the DC side of the 3P4L converter

Equations (4.57) and (4.58) are used to construct the averaged model of the 3P4L converter shown in Figure 4.18. It should be noted that when the 3P4L converter is connected to a symmetrical load, the current  $i_{N-3P4L}$  through the neutral wire will be zero.



Figure 4.18: Averaged model of a 3P4L converter

# 4.3.2 Small-Signal Model and Transfer Functions for Operation in Grid Connected Mode

The averaged model in Figure 4.18 can be used to derive the small-signal model of the 3P4L operating in grid connected mode. To make the analysis easier, certain simplifications can be applied to the model in Figure 4.18. These are:

1. The four duty cycles are generated from a three-phase duty cycle by the modulation algorithm. This means that the controller only needs to generate three duty cycles as shown in equation (4.59) [8].

$$d_{kN-3P4L} = d_{k-3P4L} - d_{N-3P4L}$$
 for  $k = a, b, c$  (4.59)

2. For tuning the controller compensators, the influence of the capacitors  $C_{f-3P4L}$  is negligible[9][10].

These simplifications reduce the averaged model in Figure 4.18 to that of Figure 4.19. The phase inductors and resistors have been combined, using equation (4.60), to reduce the number of components.



Figure 4.19: Simplified averaged model of a 3P4L converter

Circuit analysis of Figure 4.19 gives the following equations:

$$-v_{DAB2} \begin{bmatrix} d_{aN-3P4L} \\ d_{bN-3P4L} \\ d_{cN-3P4L} \end{bmatrix} + R_{f-3P4L} \begin{bmatrix} i_{a-3P4L} \\ i_{b-3P4L} \\ i_{c-3P4L} \end{bmatrix} + L_{f-3P4L} \frac{d}{dt} \begin{bmatrix} i_{a-3P4L} \\ i_{b-3P4L} \\ i_{c-3P4L} \end{bmatrix} + \begin{bmatrix} v_{aN-LV} \\ v_{bN-LV} \\ v_{N-LV} \end{bmatrix} - L_{fN-3PfL} \frac{d}{dt} \begin{bmatrix} i_{N-3P4L} \\ i_{N-3P4L} \\ i_{N-3P4L} \end{bmatrix} - R_{fN-3P4L} \begin{bmatrix} i_{N-3P4L} \\ i_{N-3P4L} \\ i_{N-3P4L} \end{bmatrix} = 0$$

$$d \qquad (4.61)$$

 $C_{3P4L}\frac{d}{dt}v_{DAB2} + d_{aN-3P4L}i_{a-3P4L} + d_{bN-3P4L}i_{b-3P4L} + d_{cN-3P4L}i_{c-3P4L} - i_{N-3P4L} = 0$ (4.62)

Loads in the low-voltage distribution grid are typically unbalanced and thus have a current flowing though the neutral. In order to control this current, an extra compensator is needed for the zero-reference frame. This requires the full dqz-transformation of equations (4.61) and (4.62) from the ABC frame.

$$-v_{DAB2} \begin{bmatrix} d_{d-3P4L} \\ d_{q-3P4L} \\ d_{z-3P4L} \end{bmatrix} + R_{f-3P4L} \begin{bmatrix} i_{d-3P4L} \\ i_{q-3P4L} \\ i_{z-3P4L} \end{bmatrix} + L_{f-3P4L} \frac{d}{dt} \begin{bmatrix} i_{d-3P4L} \\ i_{q-3P4L} \\ i_{z-3P4L} \end{bmatrix} \\ + L_{f-3P4L} \begin{bmatrix} 0 & -\omega_g & 0 \\ \omega_g & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{d-3P4L} \\ i_{q-3P4L} \\ i_{z-3P4L} \end{bmatrix} + \begin{bmatrix} v_{d-LV} \\ v_{q-LV} \\ v_{z-LV} \end{bmatrix} - L_{fN-3P4L} \frac{d}{dt} \begin{bmatrix} 0 \\ 0 \\ 3i_{z-3P4L} \end{bmatrix} \begin{bmatrix} 4.63 \\ 0 \\ 3i_{z-3P4L} \end{bmatrix} \\ - R_{fN-3P4L} \begin{bmatrix} 0 \\ 0 \\ i_{z-3P4L} \end{bmatrix} = 0$$

$$C_{3P4L}\frac{d}{dt}v_{DAB2} + d_{d-3P4L}i_{d-3P4L} + d_{q-3P4L}i_{q-3P4L} + d_{z-3P4L}i_{z-3P4L} - 3i_{z-3P4L} = 0$$
(4.64)

Applying equation (4.19) to (4.63) and (4.64) to derive the small-signal model for the 3P4L converter results in:

$$-\hat{v}_{DAB2}D_{d-3P4L} - V_{DAB2}\hat{d}_{d-3P4L} + sL_{f-3P4L}\hat{\iota}_{d-3P4L} - \omega_g L_{f-3P4L}\hat{\iota}_{q-3P4L} + R_{f-3P4L}\hat{\iota}_{d-3P4L} + \hat{v}_{d-LV} = 0$$
(4.65)

$$-\hat{v}_{DAB2}D_{q-3P4L} - V_{DAB2}\hat{d}_{q-3P4L} + sL_{f-3P4L}\hat{i}_{q-3P4L} + \omega_g L_{f-3P4L}\hat{i}_{d-3P4L} + R_{f-3P4L}\hat{i}_{q-3P4L} + \hat{v}_{q-LV} = 0$$
(4.66)

$$-\hat{v}_{DAB2}D_{z-3P4L} - V_{DAB2}\hat{d}_{z-3P4L} + sL_{f-3P4L}\hat{i}_{z-3P4L} + R_{f-3P4L}\hat{i}_{z-3P4L} + \hat{v}_{z-LV} - 3sL_{fN-3P4L}\hat{i}_{z-3P4L} - 3R_{fN-3P4L}\hat{i}_{z-3P4L} = 0$$
(4.67)

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$$sC_{3P4L}\hat{v}_{DAB2} + \hat{d}_{d-3P4L}I_{d-3P4L} + \hat{d}_{q-3P4L}I_{q-3P4L} + \hat{d}_{z-3P4L}I_{z-3P4L} + D_{d-3P4L}\hat{i}_{d-3P4L} + D_{q-3P4L}\hat{i}_{q-3P4L} + D_{0-3P4L}\hat{i}_{0-3P4L} - 3\hat{i}_{z-3P4L} = 0$$
(4.68)

Where X is the quiescent value of variable x

 $\hat{x}$  is a small variation of x

The transfer functions that will be used to tune the controller of the 3P4L operating in grid connected mode are the control-to-output-current and the output-current-to-DC-link-voltage. These can be derived from equations (4.65), (4.66), (4.67) and (4.68).

The control-to-output-current transfer function for the d-frame is:

$$G_{idd-3P4L} \Big|_{\substack{\hat{d}_{qz-3P4L}=0\\ \hat{v}_{DAB2}=0\\ \hat{v}_{dqz-LV}=0}} = \frac{\hat{\iota}_{d-3P4L}}{\hat{d}_{d-3P4L}}$$
(4.69)

Where  $\hat{d}_{qz-3P4L} = \hat{d}_{q-3P4L} = \hat{d}_{z-3P4L}$ and  $\hat{v}_{dqz-LV} = \hat{v}_{d-LV} = \hat{v}_{q-LV} = \hat{v}_{z-LV}$ 

Applying the conditions specified in (4.69) to (4.65) and (4.66) gives:

$$-V_{DAB2}\hat{d}_{d-3P4L} + sL_{f-3P4L}\hat{i}_{d-3P4L} - \omega_g L_{f-3P4L}\hat{i}_{q-3P4L} + R_{f-3P4L}\hat{i}_{d-3P4L} = 0$$
(4.70)

$$\hat{\iota}_{q-3P4L} = -\frac{\omega_g L_{f-3P4L} \iota_{d-3P4L}}{s L_{f-3P4L} + R_{f-3P4L}}$$
(4.71)

Combining equations (4.69), (4.70) and (4.71) results in the control-to-output-current transfer function for the d-frame:

$$G_{idd-3P4L} = \frac{\hat{\iota}_{d-3P4L}}{\hat{d}_{d-3P4L}} = \frac{V_{DAB2} \left( sL_{f-3P4L} + R_{f-3P4L} \right)}{\left( sL_{f-3P4L} + R_{f-3P4L} \right)^2 + \omega_g^2 L_{f-3P4L}^2}$$
(4.72)

The control-to-output-current transfer function for the Q-frame can be derived the same was as that for the q-frame and equals:

$$G_{idq-3P4L} \Big|_{\substack{\hat{d}_{dz-3P4L}=0\\\hat{v}_{DAB2}=0\\\hat{v}_{dqz-LV}=0}} = \frac{\hat{\iota}_{q-3P4L}}{\hat{d}_{q-3P4L}} = \frac{V_{DAB2} \left( sL_{f-3P4L} + R_{f-3P4L} \right)}{\left( sL_{f-3P4L} + R_{f-3P4L} \right)^2 + \omega_g^2 L_{f-3P4L}^2}$$
(4.73)

Where  $\hat{d}_{dz-3P4L} = \hat{d}_{d-3P4L} = \hat{d}_{z-3P4L}$ 

The control-to-output-current transfer function for the z-frame follows from equation (4.67):

$$G_{idz-3P4L} \Big|_{\substack{\hat{d}_{dq}-3P4L=0\\ \hat{v}_{DAB2}=0\\ \hat{v}_{dqz-LV}=0}} = \frac{\hat{l}_{z-3P4L}}{\hat{d}_{z-3P4L}} = \frac{V_{DAB2}}{s(L_{f-3P4L}-3L_{fN-3P4L}) + R_{f-3P4L} - 3R_{fN-3P4L}}$$
(4.74)

The output-current-to-DC-link-voltage transfer function is defined as follows:

$$G_{vid-3P4L} \Big|_{\substack{\hat{d}_{dqz-3P4L}=0\\\hat{v}_{dqz-LV}=0}} = \frac{\hat{v}_{DAB2}}{\hat{\iota}_{d-3P4L}}$$
(4.75)

Where  $\hat{d}_{qz-3P4L}$  is  $\hat{d}_{d-3P4L}$ ,  $\hat{d}_{q-3P4L}$  and  $\hat{d}_{0-3P4L}$ 

Applying the conditions in (4.75) to (4.66) and (4.68) gives:

 $sC_{3P4L}\hat{v}_{DAB2} + D_{d-3P4L}\hat{i}_{d-3P4L} + D_{q-3P4L}\hat{i}_{q-3P4L} + (D_{z-3P4L} - 3)\hat{i}_{z-3P4L} = 0$ (4.76)

$$\hat{\iota}_{q-3P4L} = \frac{\hat{\nu}_{DAB2} D_{q-3P4L} - \omega_g L_{f-3P4L} \hat{\iota}_{d-3P4L}}{s L_{f-3P4L} + R_{f-3P4L}}$$
(4.77)

There is no coupling between the D-frame and z-frame, thus  $\hat{i}_{z-3P4L}$  in (4.76) is zero. Taking this into account and using equations (4.76) and (4.77) results in the output-current-to-DC-link-voltage transfer function:

$$G_{vid-3P4L} = \frac{\hat{v}_{DAB2}}{\hat{\iota}_{d-3P4L}} = \frac{\omega_g L_{f-3P4L} D_{q-3P4L} - D_{d-3P4L} (sL_{f-3P4L} + R_{f-3P4L})}{sC_{3P4L} (sL_{f-3P4L} + R_{f-3P4L}) + D_{q-3P3L}^2}$$
(4.78)

Finally, the grid-voltage-to-duty-cycle transfer function can be derived by keeping only the variations of interest to non-zero, resulting in:

$$G_{vdd-3P4L}\Big|_{\substack{\hat{i}_{dqz-3P4L}=0\\\hat{v}_{DAB2}=0\\\hat{v}_{qz-LV}=0}}^{\hat{i}_{dqz-3P4L}=0} = \frac{\hat{v}_{d-LV}}{\hat{d}_{d-3P4L}} = V_{DAB2}$$
(4.79)

$$G_{vdq-3P4L}\Big|_{\substack{\hat{v}_{dqz-3P4L}=0\\\hat{v}_{DAB2}=0\\\hat{v}_{dz-LV}}}^{\hat{v}_{dqz-3P4L}=0} = \frac{\hat{v}_{q-LV}}{\hat{d}_{q-3P4L}} = V_{DAB2}$$
(4.80)

$$G_{vdz-3P4L} \Big|_{\substack{\hat{v}_{dqz-3P4L}=0\\\hat{v}_{DAB2}=0\\\hat{v}_{dq-LV}=0}}^{\hat{v}_{dqz-3P4L}=0} = \frac{\hat{v}_{z-LV}}{\hat{d}_{z-3P4L}} = V_{DAB2}$$
(4.81)

Where  $\hat{v}_{qz-LV} = \hat{v}_{q-LV} = \hat{v}_{z-3P4L} = 0$  $\hat{v}_{dz-LV} = \hat{v}_{d-LV} = \hat{v}_{z-3P4L} = 0$  $\hat{v}_{dq-LV} = \hat{v}_{d-LV} = \hat{v}_{q-3P4L} = 0$ 

#### 4.3.3 Small-Signal Model and Transfer Functions for Operation in Standalone Mode

When the low-voltage side of the SST is no longer connected to a utility grid, but rather operating in standalone mode, the 3P4L converter is responsible for keeping the load voltage at a constant value. Low-voltage grids typically have unbalanced loads that appear as oscillations when the signal is transformed to the dq-frame. These can cause unsatisfactory operation of the controller when PI compensators are used [11].

In order to remove these oscillations, the abc-signal is first decomposed to symmetrical components before converting it to the dq-frame. The sequence decomposition is a modified form of the conventional method, and is especially suited for real-time control in unbalanced situations[12]. Decoupling (4.61) in symmetrical components and then transforming the resulting signals to the dq-frame gives equation (4.83).

Comparing equations (4.63) and (4.83) reveal that these two equations are similar and therefore the small-signal model derived for (4.63) is also applicable for (4.83). Thus, the transfer functions for the 3P4L converter in symmetrical components equals:

$$G_{vddp-3P4L} = G_{vdqp-3P4L} = G_{vddn-3P4L} = G_{vdqn-3P4L} = G_{vddn-3P4L} = G_{vdqh-3P4L} = G_{vdqh-3P4L} = G_{vdqh-3P4L} = G_{vd-3P4L} = \frac{\hat{v}_{LV}}{\hat{d}_{3P4L}} = V_{DAB2}$$
(4.82)

$$-v_{DAB2}\begin{bmatrix} d_{dp-3P4L} \\ d_{qp-3P4L} \\ d_{dn-3P4L} \\ d_{qn-3P4L} \\ d_{qn-3P4L} \\ d_{qh-3P4L} \end{bmatrix} + R_{f-3P4L}\begin{bmatrix} i_{dp-3P4L} \\ i_{qn-3P4L} \\ i_{dn-3P4L} \end{bmatrix} + L_{f-3P4L} \frac{d}{dt} \begin{bmatrix} i_{dp-3P4L} \\ i_{qn-3P4L} \\ i_{qn-3$$

Where  $x_{dp}$  is the d-component of the positive sequence

 $x_{qp}$  is the q-component of the positive sequence  $x_{dn}$  is the d-component of the negative sequence  $x_{qn}$  is the q-component of the negative sequence  $x_{dh}$  is the d-component of the homopolar sequence  $x_{qh}$  is the q-component of the homopolar sequence

## 4.4 Comparison between the Switching and Averaged Models

This section shows a comparison between the different waveforms of the converter circuit models and the averaged models. The blue waveform in the graphs is a signal from the converter circuit, while the red waveform is from its averaged model. The converter circuits are simulated using a discrete solver with a sampling time of 1000 times the switching frequency. A lower sampling time reduces computation times, but can also lead to aliasing issues and is therefore not recommended. The averaged models are simulated with the variable-step solver ode23tb with a relative tolerance of 0.1ms, which are the recommended settings[13]. The specifications of the computer on which the benchmarks were done, are shown in Table 4.1.

Description	Value
OS	Windows 7 SP1 64 bit
Processor	Intel Core i5 M480 @ 2.7 GHz
RAM	4 GB

Table 4.1: Computer specifications

#### 4.4.1 Cascaded H-Bridge

The waveforms of the CHB converter circuit are compared to those of the averaged model in Figure 4.20-Figure 4.22. The blue waveforms are obtained from the converter circuit with switches and diodes, while the red waveforms are from the averaged circuit. Both waveforms overlap and their RMS or mean value are almost equal. The small difference is most likely caused due to sampling and averaging the switching circuit in Simulink. Since both waveforms match, it can be concluded that the averaged circuit is a valid representation of its switching counterpart. The computation times of both models, listed in Table 4.2, show that the averaged model is almost 100 times faster than the switching model, and therefore more suited for simulating the global behavior of the CHB.



Description	Value
Simulation time	100 ms
Computational time for converter circuit	22.885 seconds
Computational time for averaged model	0.249 seconds
Reduction in computation time	91.9 x faster

Table 4.2: Benchmark results for the CHB models

#### 4.4.2 Dual-Active Bridge

The averaged model of the DAB replaces the H-bridges and transformer circuit with an averaged model consisting only of two controlled current sources. In order to compare the behavior of the averaged model with the switching model, a sinusoidal signal is superimposed on both  $V_{DAB1}$  and  $V_{DAB2}$ . The superimposed signal on  $V_{DAB1}$  and  $V_{DAB2}$  oscillate at respectively 1/5 and 1/12 times the DAB switching frequency, both at 5% of their carrier signal. The resulting current waveforms of the averaged circuit only have a neglectable difference in amplitude compared to switching circuit's waveforms. This difference is most likely a result of non-ideal nature of the transformer in the switching circuit. The computational time of both circuits is listed in Table 4.3. Operating at approximately 150 times faster, the

computational gains of the averaged model are very beneficial for simulating the DAB at longer time intervals.



Figure 4.23: DAB voltages with a voltage ripple of 5%, v<sub>DAB1</sub>(-) oscillating at <sup>1</sup>/<sub>12</sub>\*f<sub>DAB</sub> and v<sub>DAB2</sub>(-) oscillating at <sup>1</sup>/<sub>5</sub>\*f<sub>DAB</sub>



Description	Value
Simulation time	100 ms
Computational time for converter circuit	33.22 seconds
Computational time for averaged model	0.219 seconds
Reduction in computation time	151.7 x faster

Table 4.3: Benchmark results for the DAB models

#### 4.4.3 Three-Phase Four-Leg Converter

The 3P4L converter contains a LCL-filter, which can cause oscillations. If there is hardly any damping in the circuit, the 3P4L converter needs a longer time to reach its steady-state operation point. An example of this behavior is shown in Figure 4.25-Figure 4.33, where after 40ms the oscillations still appear in the waveforms. A comparison is made between the required computation time for a simulation of 100ms and 1 second. The results in Table 4.4 and Table 4.5 show that the averaged model is faster for both cases. Because of the large oscillations in the first voltage periods, the computational gain is only 32 times. After these first cycles, the converter reaches its steady-state and the computation time of the averaged model reduces by a factor of 126. In addition to the gain in computation time, the averaged model also gives more insight into the low frequency behavior of the oscillations. This effect can clearly be seen in Figure 4.33.

Just like with the CHB AC-side waveforms, the RMS values of the 3P4L converter are calculated and compared. The RMS value of the switching waveform is slightly higher. This deviation is the result of the discrete averaging blocks in Simulink.





Description	Value
Simulation time	100 ms
Computational time for converter circuit	14.758 seconds
Computational time for averaged model	0.453 seconds
Reduction in computation time	32.6x faster

Table 4.4: Benchmark results for the 3P4L converter at a simulation time of 100 ms

Description	Value
Simulation time	1 second
Computational time for converter circuit	143.770 seconds
Computational time for averaged model	1.139 seconds
Reduction in computation time	126x faster

Table 4.5: Benchmark results for the 3P4L converter at a simulation time of 1 second

#### 4.5 Summary

The mathematical models of the CHB, DAB and 3P4L converter are presented in this chapter. The first type of model presented for each is the averaged model. The averaged models are able to simulate the converter behavior much faster than their switching circuit model. The reduction of computational times achieved with the averaged models is often a factor of 100 or more. Another model presented in this chapter is the small-signal model. These models are used to construct the transfer functions that will be used in the next chapter for controller design.

#### 4.6 References

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# Chapter 5 CONTROLLER DESIGN

This chapter presents the control strategies used in order to keep the SST operating at a desired set point. The three modes in which the SST can operate, shown in Figure 5.1 - Figure 5.3, are:

- 1. Boost mode, where the active power flows from the LV to the MV grid
- 2. Buck mode, where the active power flows from the MV to the LV grid
- 3. Standalone mode, where the utility voltage of the LV grid is absent and only loads are connected to the LV side of the SST



Figure 5.3: SST operating in standalone mode

Depending on the mode in which the SST operates, each converter has the specific task to keep an AC current, an AC voltage or a DC voltage at a constant level. The control objectives for the converters in each operating mode are shown in Table 5.1.

	СНВ	DAB	3P4L
Boost mode	i <sub>MV</sub>	V <sub>DAB1</sub>	V <sub>DAB2</sub>
Buck mode	V <sub>DAB1</sub>	V <sub>DAB2</sub>	$\mathbf{i}_{\mathrm{LV}}$
Standalone mode	V <sub>DAB1</sub>	V <sub>DAB2</sub>	$\mathbf{v}_{\mathrm{LV}}$

Table 5.1: Control objectives for each converter with their corresponding operating mode

According to Table 5.1, the CHB and DAB only have 2 possible control objectives, while the 3P4L converter has 3 of those. This makes sense, since the only difference between the operation in buck mode and standalone mode is that in standalone mode the voltage on the LV side is no longer supplied by the utility but the SST. The controllers for the three converters are a combination of feed-forward and feedback controllers. The feed-forward controller is often based on circuit equations and is used to improve dynamic behavior. The feedback controller actively measures the control parameter and is therefore able to adjust the duty cycle to obtain the desired steady state value with high accuracy. The feedback controllers are implemented using PI compensators because of their simplicity and easy implementation[1].

In addition to the controllers for the 3 converters, 2 extra controllers are needed for correct operation of the SST. These are:

- 1. The phase-locked loop (PLL) to determine the grid frequency and its angular frequency
- 2. The logic controller, which determines the operation mode for the SST

The first part of this chapter presents the PLL, since that used in the controllers that follow. Then the controllers for the three converters are constructed, and finally the design for the logic controller is presented.

#### 5.1 Phase-Locked Loop

Conventional PI compensators have the drawback of introducing a steady-state error when operating in the abc-frame. In order to control AC waveforms with PI compensators, those waveforms need to be transformed to the dqz-frame[2][3]. The transformation from the abc-to the dqz-frame requires information about the grid voltage. More specifically, the transformation requires the value of the phase angle  $\theta_{g}$ . One of the most widespread approaches to extracting the phase angle is the use of a phase-locked loop (PLL).



Figure 5.4: Phase-locked loop

The bock diagram of the conventional PLL is shown in Figure 5.4. The voltage is first transformed from its natural abc-frame to the stationary  $\alpha\beta$ -frame with the Clarke transformation. The voltage is then transformed from the  $\alpha\beta$ -frame to the dq-frame using an initial estimate of the angular frequency  $\omega_0$ . The value of  $\omega_0$  is set to  $2\pi$  times the grid

frequency, which is equal to  $100\pi$  for 50Hz. The q-component resulting from the dq transformation is a measured for the error signal and is regulated to zero using the PI compensator. When the PLL generates a phase angle that is equal to that of the input, the error becomes zero.

In addition to the phase angle, the PLL in Figure 5.4 is also able to extract two other values, namely the grid frequency and the amplitude of the grid voltage. These parameters can later be used in other parts of the SST control.

The SimPowerSystems package used in MATLAB/Simulink to simulate the different circuits, includes a PLL, however tests have shown that this PLL delivers unsatisfactory results. The built-in PLL includes an averaging block to remove ripples in the voltage. This averaging block has a buffer that stores the value of the voltage waveform for a certain amount of time. The drawback of using this buffer is that under transient behavior, the simulation step size is reduced and Simulink needs to dynamically adjust the buffer size. This process results in unacceptably long computational times and therefore the PLL in Figure 5.4 is used instead of the build-in version.

#### 5.1.1 Simulation Results

To validate the performance of the PLL in Figure 5.4, the frequency of the waveform in Figure 5.5 is measured. The value of the PI compensator is[4]:

$$H_{PLL} = 1.43 + \frac{221}{s} \tag{5.1}$$

Figure 5.6 shows that the output of the PLL follows the input disturbance of the waveform. Figure 5.7 and Figure 5.8 confirm that there is a relation between the harmonics present in the waveform and the PLL frequency output. This relationship can be useful for detecting faults in the grid and to determine when to change from grid connected to standalone mode.



## 5.2 Controllers for the Cascaded H-Bridge

The CHB consists of  $N_m$  H-bridges per phase, and each H-bridge has to be controlled in such a way that the sum of the individual bridge voltages equals the required AC-side voltage. In order to simplify analysis of the CHB, the control system for a single level CHB is first constructed. That control system is then modified for a multi-level CHB and is finally outfitted with a voltage balance and feed-forward control.

#### 5.2.1 Single level Cascaded H-Bridge

The single-level CHB shown in Figure 5.9 has the same two modes of operation as the multilevel CHB. These are:

- 1. Boost mode, where energy flows from the DC-side to the MV-side
- 2. Buck mode, where energy flows from the MV-side to the DC-side



#### 5.2.1.1 Single-level CHB operating in boost mode

When the CHB is operating in boost mode, the voltage  $V_{DAB1}$  is controlled by the DAB converters and therefore is assumed to be constant in this mode. The current flows in the direction of the MV grid and is kept at the desired value using the control scheme displayed in Figure 5.10. The current through the filter inductor  $L_{CHB}$  is measured in each phase, and transformed to the dq-frame. That value is than compared with the desired dq-value, shown with an asterisk, and the error is fed to a PI-compensator. If the PI-values are properly chosen, a small error is sufficient to produce the desired current value[5][6].



The voltage  $V_{d-MV}$  in Figure 5.10 is determined using the PLL in Figure 5.4. The saturation block prevents the current from becoming too large during a voltage drop, since its value is calculated using:

$$i_{d-MV}^* = \frac{2}{3} * \frac{P^*}{V_{d-MV}}$$
(5.2)

The values of the PI-controllers are determined using the open-loop transfer function, which consists of the small-signal transfer function of the system and the sampling delay. The PI-compensator, together with the open-loop transfer function, forms the closed-loop transfer function. The closed-loop transfer function is written as:

$$T_{cl} = H_{PI} * T_{sm} * G_{ss} \tag{5.3}$$

Where  $T_{cl}$  is the closed-loop transfer function

H<sub>PI</sub> is the PI-compensator transfer function

T<sub>sm</sub> is the delay caused by sampling action of the microcontroller or DSP

#### G<sub>ss</sub> is the small-signal transfer function

The sampling delay is caused by limitation in modern microcontrollers and DSPs. These devices, which are often used to implement the control scheme, do not allow the sampling frequency to become too high. In a typical case, sampling is allowed twice per modulation period. This delay has to be taken into account when constructing the closed-loop transfer function. The sampling delay can be approximated by[7]:

$$T_{sm} = e^{-s\frac{1}{2f_{sw}}}$$
(5.4)

Where f<sub>sw</sub> is the switching frequency

To ensure system stability, the closed-loop transfer function requires a positive phase margin and gain margin[8]. The gain margin is defined as the magnitude at which the phase crosses -180°, while the phase margin is determined at the cut-off frequency, and equals[5]:

phase margin = 
$$180^\circ + \angle T_{cl}(j2\pi f_{cut})$$
 (5.5)

Where T<sub>cl</sub> is the closed-loop transfer function

and  $f_{cut}$  is the cutoff frequency, the frequency where the magnitude crosses 0dB

Due to the sampling delay, the maximum cut-off frequency equals half the switching frequency. The controller bandwidth depends on the cut-off frequency and therefore has a maximum of half the switching frequency. To avoid interference of the integrator at the cut-

off frequency, the lag frequency in (5.6) should be much lower than the cut-off frequency  $f_{cut}$ . The general description of a PI-compensator is:

$$H_{PI}(s) = H_{\infty} \left( 1 + \frac{2\pi f_L}{s} \right)$$
(5.6)

Where  $H_{\infty}$  is the gain at  $s \rightarrow \infty$ 

f<sub>L</sub> is the lag frequency of the PI-compensator

A more common way of writing down the equation of a PI-compensator is:

$$H_{PI}(s) = K_p + \frac{K_i}{s}$$
(5.7)

Where K<sub>p</sub> is the proportional gain of the compensator and K<sub>i</sub> is the integral gain

The cut-off frequency is defined as the frequency where the magnitude of the loop gain is unity or 0 dB.

$$|T(j2\pi f_{cut})| = 0 \ dB = 1 \tag{5.8}$$

.

Where T is the open- or closed-loop transfer function

Using equations (5.3) and (5.8), the magnitude of the PI-compensator can be calculated as:

$$|H_{\infty}| = \left| \frac{1}{T_{sm}(j2\pi f_{cut}) * G_{ss}(j2\pi f_{cut}) * \left(1 + \frac{2\pi f_L}{s}\right)} \right|$$
(5.9)

Once the value of  $|H_{\infty}|$  is calculated, the complete PI-compensator can be constructed as:

$$H_{PI} = -sign(\angle T(j2\pi f_{cut})) * |H_{\infty}| * \left(1 + \frac{2\pi f_L}{s}\right)$$
(5.10)

The negative sign of the open-loop transfer function is required as correction factor for the absolute values used in equation (5.9).

The small-signal transfer functions for a single-level CHB, operating in boost mode, was derived in the previous chapter, and equals:

$$G_{idd-CHB} = \frac{\hat{\iota}_{d-MV}}{\hat{d}_{d-CHB}} = -\frac{N_m V_{DAB1} (sL_{CHB} + R_{CHB})}{(sL_{CHB} + R_{CHB})^2 + \omega_g^2 L_{CHB}^2}$$
(5.11)

$$G_{idq-CHB} = \frac{\hat{l}_{q-MV}}{\hat{d}_{q-CHB}} = -\frac{N_m V_{DAB1} (sL_{CHB} + R_{CHB})}{(sL_{CHB} + R_{CHB})^2 + \omega_g^2 L_{CHB}^2}$$
(5.12)

Where  $N_m = 1$ 

The sampling delay and closed-loop transfer functions for the single-level CHB currents equal:

$$T_{sm-CHB-1N} = e^{-s\frac{1}{2f_{CHB}}}$$
(5.13)

$$T_{idd-CHB-1N} = H_{idd-CHB-1N} * T_{sm-CHB-1N} * G_{idd-CHB}$$
(5.14)

$$T_{iqd-CHB-1N} = H_{idq-CHB-1N} * T_{sm-CHB-1N} * G_{idq-CHB}$$
(5.15)

The theoretical cut-off frequency is at half the switching frequency  $f_{c-CHB}$  per H-bridge, however due to the sampling delay the achievable cut-off frequency is much lower. A cut-off frequency of 225Hz results in a phase margin of 45.8° for both closed-loop current transfer functions. The differences between the open- and close-loop transfer functions are shown in

Figure 5.11 and Figure 5.12. Since the open loop transfer function for the d- and the q-frame are the same, their resulting closed-loop transfer function is also the same.

Parameter	Value
PI-compensator $H_{idd-CHB-1N}$ and $H_{idq-CHB-1N}$	$K_p = -0.0106, K_i = -1.5$
Cut-off frequency	225 Hz
Lag frequency	22.5 Hz
Phase margin	45.8°
Gain margin	7.51 dB





To verify the performance of the PI-compensators, the single-level CHB is connected the following loads:

- The system is unloaded until 200ms
- A reactive power flow starts to flow at 200ms
- In addition to the reactive power, the active power starts to flow from the CHB to the grid at 500ms

The behavior of the system is presented in Figure 5.13 - Figure 5.15 and shows that the operation of the PI-compensators is satisfactory. The change in value is almost instantaneous and there are no visible oscillations. When the value of the active power changes at 500ms, the value of the reactive power changes momentarily. This phenomenon is a result of the current coupling between the d- and the q-frame. To neutralize this effect, a feed-forward action will be used in the final form of the controller.

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#### 5.2.1.2 Single-level CHB operating in buck mode

When operating in buck mode, the power flows from the MV-grid to the CHB. In this mode, the CHB has to provide a constant  $V_{DAB1}$  voltage. The two most common feed-back methods to generate a constant voltage are shown in Figure 5.16. They are voltage-mode control and current-mode control[5][6][9].



Voltage-mode control is also called duty cycle control, because it adjusts the duty cycle directly as a response to changes in the output voltage. The voltage-mode control consists of a single control loop, has low hardware requirements and reacts fast to output voltage disturbances. When disturbances occur in the input voltage, the voltage-mode control reacts rather slowly. This is because these disturbances need to propagate from the input to the output voltage before they can be observed and corrected by the controller. In order to overcome this problem, a feed-forward loop is often added to the voltage-mode controller.

Current-mode control, also called current-programmed mode or current-injected mode, has two control loops: an inner current loop and an outer voltage loop. The name current-mode control comes from the fact that the current is directly controlled, while the voltage is controlled indirectly by the current loop. The output voltage is measured and compared to the desired value. The error between these two values is used to generate a reference current value, which is compared to the actual current value to finally generate a duty cycle. This results in a very robust wide-bandwidth output voltage control. However, this robustness comes at the cost of a more complex control system.

To control the DC voltage  $V_{DAB1}$ , the current-mode control is used because of its robustness and because it is already available in the boost part of the controller. Since the inner currentloop was already designed for the CHB operating in boost mode, only the outer voltage-loop needs to be added to create a current-mode control. The voltage-loop, shown in Figure 5.17, averages the sum of the  $V_{DAB1}$  DC-voltages and compares that to the desired value of  $V_{DAB1}$ . The error is compensated by a PI-controller and the output is fed to the inner current-loop of Figure 5.10.



Figure 5.17: Outer voltage-loop for single-level CHB

The transfer function for the voltage-loop, as derived in the previous chapter, is shown in equation (5.16). The current-loop serves as an intermediate step between the voltage-loop and the duty cycle, and therefore its closed-loop transfer function from equation (5.14) has to be added to that of the voltage-loop, as shown in (5.17). In order to avoid interference of the inner-loop due to the operation of the outer-loop, the cut-off frequency  $f_{cut}$  for the PI-compensator of the voltage-loop should be chosen approximately 1/10<sup>th</sup> of the current-loop cut-off frequency. Placing the cut-off frequency at 22.5 Hz results in a stable control loop with a phase margin of 50.5°, as shown in Figure 5.18.

$$G_{vid-CHB} = \frac{\hat{v}_{DAB1}}{\hat{\iota}_{d-MV}} = \frac{D_{d-CHB}(sL_{CHB} + R_{CHB}) - D_{q-CHB}L_{CHB}\omega_g}{N_m D_{q-CHB}^2 + 3sC_{DAB1}(sL_{CHB} + R_{CHB})}$$
(5.16)

Where N<sub>m</sub>=1

$$T_{vid-CHB-1N} = H_{vid-CHB-1N} * G_{vid-CHB} * \frac{T_{idd-CHB-1N}}{T_{idd-CHB-1N} + 1}$$
(5.17)

Value
$K_p = 0.526, K_i = 26$
22.7 Hz
7.9 Hz
50.5°
21.7 dB

#### Table 5.3: PI-compensator design parameters

To investigate the performance of the PI-compensator, the DC-side of the CHB is loaded with the rated power at 600ms. The AC-side behavior is shown in Figure 5.19 - Figure 5.23, while the DC-side is shown in Figure 5.20 - Figure 5.22. An increase in current on the DC-side results in a decrease in voltage  $V_{DAB1}$ . The controller detects this change in voltage and adjusts the duty ratio, so that the voltage can be restored to the rated value. The controller is able to achieve this in less than 0.1 sec with a drop in voltage of no more than 10%. There are small oscillations present on the current waveform, however, these are small compared to the rest of the waveform and do not pose a risk for loss of stability.



Figure 5.18: Compensated and uncompensated transfer functions for the voltage-loop



#### 5.2.2 Multilevel Cascaded H-Bridge

The single-level CHB can be expanded to create a multilevel CHB. And just like the single-level CHB, the multilevel CHB has 2 modes of operation:

- Boost mode
- Buck mode

#### 5.2.2.1 Multilevel CHB operating in boost mode

When the multilevel CHB is operating in boost mode, energy flows through the DC-side of the CHB to the AC-side. The DC-side voltage  $V_{DAB1}$  for each individual H-bridge is supplied by a separate DAB. In this mode, the control strategy of the DAB is to generate a constant DC-voltage  $V_{DAB1}$ . Because of this, it is assumed that the DC-voltage  $V_{DAB1}$  on each H-bridge is constant and at rated value.

The boost controller in Figure 5.10 only uses AC-side variables on its input. This allows the controller to be used for the multilevel CHB without changing its structure. The transfer functions displayed in (5.11) and (5.12) are reused to develop the PI-compensators. The only difference between the single-level CHB and the multilevel CHB is that the number of levels for this research is now 7. An addition of H-bridges in the CHB results in the change in sampling delay, and equation (5.13) changes to (5.18). Substituting  $N_m = 7$  in (5.11) - (5.12) and placing the cut-off frequency at 735Hz results in a stable closed loop (5.19), with a phase margin of 66.3°, as shown in Figure 5.24 and Figure 5.25.

$$T_{sm-CHB} = e^{-s\frac{1}{2N_m f_{CHB}}}$$
(5.18)

$$T_{idd-CHB} = H_{idd-CHB} * T_{sm-CHB} * G_{idd-CHB}$$
(5.19)

Where  $N_m = 7$ 

Value
$K_p = -0.00519, K_i = -2.39$
735 Hz
73.5 Hz
66.3°
13.9 dB

Table 5.4: PI-compensator design parameters







Figure 5.25: Compensated and uncompensated transfer functions for the q-frame current

The verification of the constructed controller for the multilevel CHB is done by checking its behavior for a step change in reactive power and then in active power. The following scenario is displayed in Figure 5.26 - Figure 5.28.

- A reactive power flow starts to flow at 400ms
- In addition to the reactive power, the active power starts to flow from the CHB to the grid at 700ms

The change in both active and reactive power in Figure 5.28 is almost instantaneously with very little overshoot. The voltage and current waveforms have a smooth shape, without any irregularities. Based on Figure 5.26 - Figure 5.28, it can be concluded that the controller performs optimal under rated conditions.



#### 5.2.2.2 Multilevel CHB operating in buck mode

When the CHB is operating in buck mode, the energy flows from the AC-side to the DC-side of the CHB. The AC-side voltage of the single-level CHB depends only on the DC-voltage and the duty cycle of a single H-bridge. When multiple H-bridges are cascaded, the AC-voltage depends on the sum of the DC-voltage of each H-bridge and their duty cycle. To account for the increase of H-bridges, a summation step is added and to the voltage-loop and the averaging factor is adjusted in Figure 5.17 to create Figure 5.29.

The transfer function for the voltage-loop in (5.16) is also valid for a multilevel CHB. The difference here is that  $N_m$  for the case study equals 7, instead of one for the case of a single-level CHB. Substituting  $N_m$  = 7 in (5.16) and choosing a cut-off frequency of 36.8 Hz results in a phase margin of 82.8°. This phase margin can be seen in Figure 5.30 and is more than enough for to stabilize the closed-loop in equation (5.20).

$$T_{vid-CHB} = H_{vid-CHB} * G_{vid-CHB} * \frac{T_{idd-CHB}}{T_{idd-CHB} + 1}$$
(5.20)





Parameter	Value
PI-compensator H <sub>idd-CHB</sub> and H <sub>idq-CHB</sub>	$K_p = 2.42, K_i = 112$
Cut-off frequency	36.8 Hz
Lag frequency	3.9 Hz
Phase margin	82.8°
Gain margin	33.9 dB





Figure 5.30: Compensated and uncompensated transfer functions for the voltage-loop

To validate the performance of the controller with the calculated PI-values, the DC-side load of the multilevel CHB is changed at 500ms from 0 to the rated value. Figure 5.31, Figure 5.33 and Figure 5.35 show that the change in power is almost instantaneously with very little overshoot. However, Figure 5.32, Figure 5.34 and Figure 5.36 show that although the average value of the voltage is at rated value, individual DC-voltages are not. This is a problem because of two reasons:

- 1. The switching scheme chosen for the DAB has the lowest losses when the input- and output voltages are at rated value.
- 2. Large differences in DC-voltages can lead to system instabilities.

Because of these reasons, additional measures have to be taken to ensure an equal voltage among the several H-bridges.


## 5.2.3 Voltage Balance

Under ideal conditions, the voltage  $V_{DAB1}$  is equal across each H-bridge. However, as Figure 5.34 and Figure 5.36 show, voltage levels across the individual H-bridges can differ, while the average voltage  $V_{DAB1}$  is at rated value. To overcome this problem, a voltage balancing scheme, developed at TNO, is added to each phase of the controller.

The principle operation of the voltage balance scheme can be explained using Figure 5.37. Without the balancing scheme, the voltage on the AC-side of the CHB equals:

$$V_{x-CHB} = d_{x-CHB} * (V_{x1-DAB1} + V_{x2-DAB1} + \dots + V_{xNm-DAB1})$$
(5.21)  
x is phase a b or c

Where x is phase a, b or c

Without the balancing scheme, the voltage vectors in Figure 5.37(a) can have any arbitrary value, as long as their sum is sufficient to generate  $V_{CHB}$  when multiplied by the duty cycle. The voltage balancing scheme multiplies the duty cycle of each H-bridge with a scalar, so that the attribution to  $V_{CHB}$  is equal. The product of the balancing scalars is unity, that is:

$$b_x = b_{x1} * b_{x2} * \dots * b_{xNm} = 1$$
(5.22)

Where x is phase a, b or c

When the balancing factor is added to equation (5.21), the AC-side voltage of the CHB becomes:

$$V_{x-CHB} = d_{x-CHB} * (b_{x1}V_{x1-DAB1} + b_{x2}V_{x2-DAB1} + \dots + b_{xNm}V_{xNm-DAB1})$$
(5.23)

Where x is phase a, b or c



Figure 5.37: Voltage vectors of phase a without- and with voltage balance scheme

The implementation of the voltage balance scheme is shown in Figure 5.38. The balancing factor is generated for each H-bridge by a PI-composer. This is then multiplied with the duty cycle for that specific phase. The input signal for the PI-composer is the difference between the individual H-bridge voltage and the average DC-voltage. The difference is first multiplied by the sign of the d-frame current to ensure that proper corrective action is caused by the balancing factor. It is important that the output of the PI-composers at startup equals 1; otherwise the CHB is unable to generate an AC-voltage, as is confirmed with equation (5.22). The parameters of the PI-compensators is imperially determined and shown in (5.24).

$$H_{vd-CHB} = 1 + \frac{1}{s}$$
(5.24)

To get an idea of the performance of the voltage balance scheme, the same situation as in section 5.2.2.2 is repeated and the results are presented in Figure 5.41 and Figure 5.44. A change in active power flow introduces a voltage difference between the different H-bridges. This difference is measured by the voltage balancing scheme and adjusts the balancing factor, so that the voltages over the H-bridges is equalized. The restoration of the voltage to its rated value takes less than 200ms and the difference between the individual volages is kept relatively small.





An additional advantage of the voltage balance scheme is that it also ensures equal voltage amongst the H-bridges in case of component mismatch. Due to tolerances specified by the manufacturer, not all the capacitances and switches will have the exact same properties. Figure 5.45 and Figure 5.46 show what can happen when the capacitor of the second H-bridge in phase a is 80% of the rated value. As can be expected, the controller without voltage balancing scheme is unable to ensure equal voltages between the different H-bridges and might eventually end in an unstable situation. However, when the voltage balancing scheme is added, the voltage in the H-bridge with the smaller capacitor shows little deviation from the average DC-side voltage.



### 5.2.4 Feed-forward controller

Disturbances in the system can be eliminated using feedback control. The mechanism of a feedback loop needs to sense an error before it can come into action. In certain situations it is possible to determine or measure the disturbances before it can influence the rest of the system. It is preferred to removes these disturbances before they influence the system. This can be achieved with a feed-forward controller[10].

An example of a feed-forward controller is shown in Figure 5.47. This control is based on the mathematical relationship between the input current and the steady-state duty cycle, as was derived in the previous chapter. The q-frame MV-side voltage is set to zero by the PLL, and therefore  $V_{q-ph-MV}$  in Figure 5.47 is also set to zero. The feed-forward controller is connected in parallel to the feedback controller and the calculated duty cycle of both controllers is combined.



Figure 5.47: Feed-forward control

Figure 5.48 shows the change in active and reactive power for a control system without feed-forward. The scenario depicted here is the same as in Figure 5.28. Figure 5.49 shows the behavior of a system with feed-forward control. The difference in behavior is best noticed when the active power changes. The system with feed-forward displays a much smaller dip than the one without feed-forward. The system without feed-forward also needs more time to return to its set value, as seen in Figure 5.50.



#### 5.2.5 Overall Control Architecture

Figure 5.51 gives an overall overview of the controller that is used to keep the parameters of the multilevel CHB at desired values. The voltage-loop, the current-loop, the feed-forward controller and the voltage balancing scheme are clearly visible. An important element in the controller is the S<sub>bb</sub> switch. This switch is controlled by the SST's logic controller, and its value specifies if the CHB is operating in buck- or boost-mode. Based on the position of this switch, the value of the d-frame current is calculated either using the voltage-loop or as a function of the desired active power and grid voltage. Since the PI-compensators need a DC-signal to operate properly, the AC-side voltage and current are first transformed to the dq-frame before they are used. The current-loop and the feed-forward controller both determine the value of the duty cycle using their own algorithm. The value of both duty cycles is added and transformed from the dq-frame back to the abc-frame. Finally, the duty cycle is fed to the voltage balance scheme, which then calculates the duty cycle for each individual H-bridge.



Figure 5.51: Overall overview of the multilevel CHB controller

# 5.3 Controllers for the Dual-Active Bridge

The Dual-Active Bridges are connected between the CHB and the 3P4L converter. The DAB provides isolation between the MV- and the LV-side and is responsible to for keeping either  $V_{DAB1}$  or  $V_{DAB2}$  at their rated value. The voltage which is controlled by the DAB is determined by the mode it is operating in. If the DAB is operating in buck mode, it is responsible for keeping  $V_{DAB2}$  at a constant value, and in boost mode it is responsible for  $V_{DAB1}$ .



Figure 5.52: Circuit overview of a Dual-Active Bridge

Figure 5.52 shows a circuit overview of the DAB. The ultimate goal of this circuit is to provide a constant voltage. In order to achieve this goal, a current-programmed controller will be used. A comparison between the DAB operating in buck and boost mode is made in Table 5.6. From a control point of view, both operation modes of the DAB are similar and their control strategy will therefore be presented side-by-side in the next parts of this chapter.

	Buck	Boost
Flow of energy	$V_{DAB1} \rightarrow V_{DAB2}$	$V_{DAB1} \leftarrow V_{DAB2}$
Current-loop control parameter	i <sub>DAB2</sub>	i <sub>DAB1</sub>
Voltage-loop control parameter	V <sub>DAB2</sub>	V <sub>DAB1</sub>
Externally controlled parameter	V <sub>DAB1</sub>	V <sub>DAB2</sub>

Table 5.6: Comparison between DAB operating in Buck and Boost mode

#### 5.3.1 Current-loop

The feedback control system for the DAB consists of an outer voltage-loop and an inner current-loop. In order to design the current-loop, the voltage on both sides of the DAB is assumed to be constant. This can be artificially achieved by replacing the capacitors in Figure 5.52 with two DC-voltage sources operating at  $V_{DAB1}$  and  $V_{DAB2}$ . The current-loop for the DAB operating in buck and in boost mode is shown in respectively Figure 5.53 and Figure 5.54.



According to equation (5.4), the sampling delay for the DAB in both buck and boost mode equals:

$$T_{sm-DAB} = e^{-s\frac{1}{2f_{DAB}}}$$
(5.25)

The transfer function of the DAB operating in buck mode is shown in (5.25). In order to construct a fast closed-loop response, the cut-off frequency for (5.27) is placed at 2500 Hz. This cut-off frequency at 2.5 kHz results in a phase margin of  $29^{\circ}$ .

$$G_{id-buck-DAB} = \frac{\hat{i}_{DAB2}}{\hat{d}_{DAB}} = \frac{2V_{DAB2}}{n_{Tr}^{-2}(sL_{DAB} + R_{DAB})}$$
(5.26)

$$T_{id-buck-DAB} = H_{id-buck-DAB} * T_{sm-DAB} * G_{id-buck-DAB}$$
(5.27)

The transfer function for the DAB in boost mode in (5.28) is comparable to the buck mode transfer function in (5.26). A cut-off frequency of 3 kHz for the closed-loop transfer function (5.29) results in a stable system with a phase margin of  $41.4^{\circ}$ .

$$G_{id-boost-DAB} = \frac{\hat{i}_{DAB1}}{\hat{d}_{DAB}} = \frac{2V_{DAB1}}{sL_{DAB} + R_{DAB}}$$
(5.28)

$$T_{id-boost-DAB} = H_{id-boost-DAB} * T_{sm-DAB} * G_{id-boost-DAB}$$
(5.29)

Parameter	Buck mode	Boost mode
PI-compensator	$\mathbf{H}_{id-buck-DAB}$	$\mathbf{H}_{id-boost-DAB}$
K <sub>p</sub> and K <sub>i</sub> values	$K_p = 0.000278, K_i = 3.5$	K <sub>p</sub> = 0.000695, K <sub>i</sub> = 5.24
Cut-off frequency	2500 Hz	3000 Hz
Lag frequency	2000 Hz	1200 Hz
Phase margin	29°	41.4°
Gain margin	12.6 dB	10.3 dB

Table 5.7: PI-compensator design parameters

The effectiveness of the calculated PI-values for buck- and boost mode operation is investigated and their results are presented in Figure 5.57-Figure 5.60. As mentioned earlier, both DC-voltages are fixed at their rated value, therefore the graphs In Figure 5.57 and Figure 5.58 are a constant line. At t = 30ms the current is increased to its rated value in buck mode, and to the negative of the rated value in boost mode. Figure 5.59 and Figure 5.60 show that both current loops respond quickly and are able to reach the desired value in less than 10ms.



#### 5.3.2 Voltage-loop

The outer-loop or voltage-loop for the DAB in buck and boost mode is shown in Figure 5.61 and Figure 5.62. This voltage-loop generates a reference current-value based on the difference between the measured and desired DC-voltage.





**Figure 5.61: DAB voltage-loop for buck mode** The transfer functions associated with the DAB in buck mode are shown in (5.30) and (5.31). A cut-off frequency at 200 Hz results in a closed-loop transfer function with a phase margin of 96.3°. This margin is more than enough for a stable control loop.

$$G_{vi-buck-DAB} = \frac{\hat{v}_{DAB2}}{\hat{\iota}_{DAB2}} = \frac{R_{L2}(-2D_{DAB}+1)}{sR_{L2}C_{DAB2}+1}$$
(5.30)

$$T_{vi-buck-DAB} = H_{vi-buck-DAB} * G_{vi-buck-DAB} * \frac{T_{id-buck-DAB}}{T_{id-buck-DAB} + 1}$$
(5.31)

The same design process is repeated for the boost mode transfer functions in (5.32) and (5.33). A cut-off frequency of 270 Hz results in a phase margin of 84.5°, which is also more than sufficient for a stable control loop.

$$G_{vi-boost-DAB} = \frac{\hat{v}_{DAB2}}{\hat{\iota}_{DAB2}} = \frac{R_{L1}(-2D_{DAB}+1)}{sR_{L1}C_{DAB1}+1}$$
(5.32)

$$T_{vi-boost-DAB} = H_{vi-boost-DAB} * G_{vi-boost-DAB} * \frac{T_{id-boost-DAB}}{T_{id-boost-DAB} + 1}$$
(5.33)

Parameter	Buck mode	Boost mode
PI-compensator	H <sub>vi-buck-DAB</sub>	H <sub>vi-boost-DAB</sub>
K <sub>p</sub> and K <sub>i</sub> values	$K_p = 0.669, K_i = 168$	$K_p = -1.8, K_i = -306$
Cut-off frequency	200 Hz	270 Hz
Lag frequency	40 Hz	27 Hz
Phase margin	96.3°	84.5°
Gain margin	18.2 dB	21.1 dB

 Table 5.8: PI-compensator design parameters









The same scenario as in 5.3.1 is repeated for a DAB with the complete feedback control, that is, a controller with both the voltage- and the current loop. For operation in buck mode, the voltage  $V_{DAB1}$  is fixed using a constant voltage supply, while the capacitor  $C_{DAB2}$  in Figure 5.52 restored and a variable load is placed parallel to it. In boost mode, the simulation elements are adjusted the other way around. The voltage  $V_{DAB2}$  is fixed using a constant DC-source,  $C_{DAB1}$  is restored and a variable load in connected parallel to it.

A change in the load to the rated value of  $i_{DAB2}$  results in a drop in voltage  $V_{DAB2}$ . The controller is fast to react and within 10ms the voltage and currents reach their steady-state value. Although there is an overshoot in the power, the controller is able to restrict this to an acceptable value of 20%.

The same scenario is repeated for boost mode, but the difference here is the negative flow in power. The boost mode controller is a bit slower than the buck mode controller and the voltage and currents need a bit more than 10ms to reach their steady state value. The boost mode controller shows less overshoot than with the buck mode controller.



#### 5.3.3 Feed-Forward Controller

In order to reduce the overshoot and to increase the overall robustness of the system, a feedforward is added in parallel to the feedback controller. Assuming the DAB is lossless, the equations for the power flow can be written as:

$$P_{DAB} = V_{DAB1} * i_{DAB1} = \frac{V_{DAB2}^2}{R_{L2}}$$
(5.34)

$$P_{DAB} = \frac{V_{DAB1}V_{DAB2}D_{DAB}(1 - D_{DAB})}{2n_{Tr}f_{DAB}L_{DAB}}$$
(5.35)

The duty cycle  $D_{DAB}$  in (5.35) can be solved by combining (5.33) and (5.34) to get:

$$D_{DAB} = \frac{1 - \sqrt{1 - \frac{8f_{DAB}L_{DAB}V_{DAB2}}{n_{Tr}R_{L2}V_{DAB2}}}}{2}$$
(5.36)

Equation (5.36) can be approximated by substituting the rated value for  $V_{DAB1}$  and  $V_{DAB2}$  and expanding the equation using a second order Taylor series[11]:

$$D_{DAB} = \frac{K_1}{4R_{L2}} \left( 1 + \frac{K_1}{4R_{L2}} \right)$$
(5.37)

where 
$$K_1 = \frac{8f_{DAB}L_{DAB}V_{DAB2}^*}{n_{Tr}V_{DAB1}^*}$$
 (5.38)

The load R<sub>L2</sub> can be estimated using the duty cycle from the feedback loop:

$$R_{L2} = \frac{2f_{DAB}L_{DAB}V_{DAB2}}{n_{Tr}V_{DAB1}d_{DAB}^*(1-d_{DAB}^*)}$$
(5.39)

Although equation (5.39) is derived for a DAB operating in buck mode, equations (5.37) - (5.39) only need the measured DC-voltages  $V_{DAB1}$  and  $V_{DAB2}$ , along with the feedback duty cycle in order to approximate the feed-forward duty cycle. This makes the feed-forward controller applicable for both buck and boost mode, as long as the feedback duty-cycle is calculated by the correct feedback loop. A schematic overview of the feed-forward controller is given in Figure 5.71.



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To compare the control system with and without feed-forward controller, the same scenario as in section 5.3.2 is repeated.

The results for the DAB in buck mode are shown in Figure 5.72, Figure 5.74 and Figure 5.76. The difference between the system with and without feed-forward control is clearly visible. The dip in voltage  $V_{DAB2}$  is less, the overshoot in the currents is also smaller and the oscillation has been eliminated. The attribution of the feed-forward control to the current and voltage waveform results in a power waveform that has almost zero overshoot.

The effect of the feed-forward controller on the waveforms for the DAB in boost mode is less than buck mode, as can be seen in Figure 5.73, Figure 5.75 and Figure 5.77. There is hardly any difference in the voltage  $V_{DAB1}$  between the system with and without feed-forward. On the

other hand, compared to the system without feed-forward, the currents in the system with feed-forward have a smaller overshoot. The net result is that the power waveform also has a smaller overshoot, making the effect of the feed-forward controller a welcome attribution to the overall control system.



### 5.3.4 Overall Control Layout

An overall overview of the DAB controller is shown in Figure 5.78. The controller consists of 2 current programmed controllers, one for operation in buck mode and another for operation in boost mode. There is a feed-forward controller parallel the feedback current programmed controllers. As with the multilevel CHB controller, the DAB also has a buck-boost selector switch. This switch is controlled by the logic controller and selects the proper feedback controller output, depending on the operation mode of the SST. The duty cycle selected by this switch is sent to the feed-forward controller where the feed-forward duty cycle is

calculated. The feedback and feed-forward duty cycle are finally added and used in the modulator to determine the gate output for the IGBT switches.

The overall controller for the DAB is kept as simple as possible, while at the same time trying to achieve a robust system. The reason for the simplicity is that each DAB is controlled independently from the rest of the system. The only input the DAB controller receives from the logic controller is the position of the buck-boost selector. This parameter tells the DAB whether to keep the  $V_{DAB1}$  or  $V_{DAB2}$  constant. The 21 DABs in the SST used for the case study each have their own controller. If the control system is kept simple enough, multiple controllers can be implemented using a single microprocessor. This reduces overall complexity and the total cost of the SST.



Figure 5.78: Overall DAB controller overview

# 5.3.5 Effect of the DC-ripple

While developing the controller for the CHB, the DC-side voltages revealed that although the average voltage  $V_{DAB1}$  is constant at steady state, the individual DC-voltages contain a ripple. This voltage ripple can be reduced by increasing the capacitance in  $C_{DAB1}$ , but due to practical constraints, the ripple is designed to have a peak-peak value of  $10\% V_{DAB1}$  at rated power. It is desired that this ripple does not propagate to the rest of the SST, because it is a source of disturbance, increases the stress on controllers and might lead to instabilities.

To verify if a voltage ripple on one side of the DAB propagates through to the other side, an AC-voltage is superimposed on  $V_{DAB1}$  for operation in buck mode. The AC-voltage has a peek-peek value of  $10\% V_{DAB1}$ . The same is repeated for operation in boost mode, but in this mode, a voltage ripple of  $10\% V_{DAB2}$  is superimposed on  $V_{DAB2}$ . The results are shown in Figure 5.79 - Figure 5.84. These images show that the operation of the controller is sufficient enough to negate the effects of the input voltage ripple, resulting in a constant output voltage.



# 5.4 Controllers for the Three-Phase Four-Leg converter

The Three-Phase Four-Leg converter connects the SST to the LV-grid. It converts the DC-voltage  $V_{DAB2}$  to an AC-voltage. By adjusting the amplitude and phase shift of that AC-voltage, it is possible to transfer energy back and forward between the LV-grid and the SST.

Figure 5.85 shows a circuit overview of the 3P4L converter. Unlike the CHB and the DAB, the 3P4L converter has 3 modes of operation instead of two. When the converter is connected to the grid, the 2 possible modes of operation are buck- and boost mode. When the LV-grid voltage is absent, the 3P4L converter switches to its standalone mode. In this mode, the 3P4L converter is responsible for generating a constant AC-voltage. A quick overview of the 3 modes along with the external and control parameters is given in Table 5.9.

	Buck	Boost	Standalone
Flow of energy	$V_{DAB2} \rightarrow V_{LV}$	$V_{DAB2} \leftarrow V_{LV}$	$V_{DAB2} \rightarrow V_{LV}$
Control parameter	$\mathbf{i}_{\mathrm{LV}}$	V <sub>DAB2</sub>	V <sub>LV</sub>
Externally controlled	$V_{DAB2}$ and $V_{LV}$	V <sub>LV</sub>	V <sub>DAB2</sub>

Table 5.9: The three operation modes of the 3P4L converter



#### 5.4.1 Buck mode controller

The buck mode controller allows the 3P4L converter to generate a desired AC-current. A schematic overview of this controller is shown in Figure 5.86. In contrast to the CHB controller, the AC-current in the 3P4L controller is transformed not only to the dq-frame, but also to the z-frame. The extra frame is added to account for unbalanced situations. The desired d-frame current is a function of the desired active power and the q-frame current is calculated based on the desired reactive power. Since the z-frame does not attribute to active power or reactive power flow, its desired value is always set to zero. PI-compensators calculate a duty cycle based on the error between the desired and the actual currents in the d-, q- and z-frame.



Figure 5.86: 3P4L controller for buck mode operation

As is the case with the CHB, the 3P4L current-loop also contains a coupling between the dand the q-frame. This causes a change in active power when the reactive power changes and the other way around. In order to reduce this effect, a decoupling factor is added to generated dq-frame duty cycle. The decoupling factor can be calculated with the help of the DC-voltage  $V_{DAB2}$  and the dq-currents and equals[12]:

d-frame: 
$$\frac{2\pi f_{grid} (L_{f1-3P4L} + L_{f2-3P4L})}{V_{DAB2}} * i_{d-LV} = -K_{dq} * i_{q-LV}$$
(5.40)

q-frame: 
$$\frac{-2\pi f_{grid} \left( L_{f1-3P4L} + L_{f2-3P4L} \right)}{V_{DAB2}} * i_{q-LV} = K_{dq} * i_{d-LV}$$
(5.41)

The sampling delay for the 3P4L converter is similar to that of the DAB and is shown in equation (5.42). The d-frame transfer function is the same as that of the q-frame. This allows for simultaneous construction of the PI-compensators. The sampling delay, along with the dq-frame transfer function (5.43) and the PI-compensator place the closed loop transfer function (5.44) at a phase margin of 75.3°.

$$T_{sm-3P4L} = e^{-s\frac{1}{2f_{3P4L}}}$$
(5.42)

$$G_{idd-3P4L} = G_{idq-3P4L} = G_{iddq-3P4L} = \frac{\hat{\iota}_{d-3P4L}}{\hat{d}_{d-3P4L}} = \frac{V_{DAB2}(sL_{f-3P4L} + R_{f-3P4L})}{\left(sL_{f-3P4L} + R_{f-3P4L}\right)^2 + \omega_g^2 L_{f-3P4L}^2}$$
(5.43)

$$T_{iddq-3P4L} = H_{iddq-3P4L} * T_{sm-3P4L} * G_{iddq-3P4L}$$
(5.44)

The z-frame PI-compensator is designed the same way as was done for the dq-frame. The z-frame transfer functions are shown in (5.45) and (5.46). The phase margin of the closed-loop transfer function is placed at a stable value of 66.1°.

$$G_{idz-3P4L} = \frac{\hat{l}_{z-3P4L}}{\hat{d}_{z-3P4L}} = \frac{V_{DAB2}}{s(L_{f-3P4L} - 3L_{fN-3P4L}) + R_{f-3P4L} - 3R_{fN-3P4L}}$$
(5.45)

$$T_{idz-3P4L} = H_{idz-3P4L} * T_{sm-3P4L} * G_{idz-3P4L}$$

Parameter	d- and q-frame	z-frame
PI-compensator	${ m H}_{ m iddq-3P4L}$	H <sub>idz-3P4L</sub>
K <sub>p</sub> and K <sub>i</sub> values	$K_p = 0.000335, K_i = 0.0368$	K <sub>p</sub> = 0.000687, K <sub>i</sub> = 0.151
Cut-off frequency	175 Hz	350 Hz
Lag frequency	17.5 Hz	35 Hz
Phase margin	75.3°	66.1 <sup>°</sup>
Gain margin	20.7 dB	13.9 dB

Table 5.10: PI-compensator design parameters



Figure 5.87: Compensated and uncompensated transfer functions for the dq-frame



Bode Diagram

Figure 5.88: Compensated and uncompensated transfer functions for the z-frame

(5.46)

The performance of the buck mode controller is tested by loading the 3P4L converter with 500kVA reactive power at 200ms. An active power flow of 1MW is added to the output at 300ms. The results are shown in Figure 5.89 - Figure 5.92. The change in both active and reactive power is processed almost instantaneously by the controller while keeping the overshoot at acceptable levels. There is a coupling between the d- and q-frame is visible in Figure 5.90 and Figure 5.91, but thanks to the decoupling factor, the effects are minimized.



#### 5.4.2 Boost mode controller

Boost mode control is achieved by adding a voltage-loop to the buck mode controller. This controller, shown in Figure 5.93, uses the difference between the desired and the actual DC-voltage  $V_{DAB2}$  to generate a reference d-frame current. This reference current is then used by the buck mode controller to generate a duty-cycle.



Figure 5.93: 3P4L boost mode controller

The transfer functions for the 3P4L boost mode controller are shown in equation (5.47) and (5.48). Due to the small cut-off frequency of the current loop, the voltage-loop cut-off frequency has to be placed at 26Hz in order to achieve acceptable controller behavior. The parameters of the PI-compensator for the voltage-loop are presented in Table 5.11.

$$G_{vid-3P4L} = \frac{\hat{v}_{DAB2}}{\hat{\iota}_{d-3P4L}} = \frac{\omega_g L_{f-3P4L} D_{q-3P4L} - D_{d-3P4L} (sL_{f-3P4L} + R_{f-3P4L})}{sC_{3P4L} (sL_{f-3P4L} + R_{f-3P4L}) + D_{q-3P3L}^2}$$
(5.47)

T	* $G$ aput * $T_{iddq-3P4L}$	( <b>F</b> 49)
1 vid-buck-DAB — $11$ vid-3P4L	$T_{iddq-3P4L} + 1$	(3.48)

Parameter	Value
PI-compensator H <sub>vid-3P4L</sub>	$K_p = -14.6, K_i = -1210$
Cut-off frequency	26.3 Hz
Lag frequency	13.1 Hz
Phase margin	118°
Gain margin	35.1 dB

Table 5.11: PI-compensator design parameters



Figure 5.94: Compensated and uncompensated transfer functions for the boost mode controller

The behavior of the currents, voltages and power when the 3P4L is loaded with its rated power is shown in Figure 5.95 - Figure 5.98. The transients last 50-100ms, after which the system returns to a steady state. During the change in load, the DC-side voltage reaches a dip of 13% its rated value. The amplitude of the voltage dip remains the same, regardless of the chosen values for the PI-compensator. If a value smaller than 13% is desired, the capacitance  $C_{3P4L}$  in Figure 5.85 can be increased. However, since the DC-voltage  $V_{DAB2}$  is an internal value and the dip does not cause instabilities, a value of 13% is acceptable.





#### 5.4.3 Standalone controller

In standalone mode, the SST is disconnected from the LV-grid and the 3P4L converter is responsible for generating a constant LV-side voltage. When the LV-side loads are unbalanced, the conventional abc-to-dqz transformation will contain an AC-ripple that oscillates at double the grid frequency. The PI-compensators need a DC-signal for optimal operation and an AC-ripple can lead to degradation of the controller performance. In order to remove the ripple, the method of sequence decomposition is applied to the measured AC-voltage before transforming it to the dq-frame[13]. The principle of transformation to the dq-frame in sequence components is shown in Figure 5.99, with the transformation matrices given in equation (5.49). Transforming back to the abc-domain from dq-frame sequence components is shown in Figure 5.100.

$$F_{p} = \frac{1}{3} \begin{bmatrix} 1 & a & a^{2} \\ a^{2} & 1 & a \\ a & a^{2} & 1 \end{bmatrix}, F_{n} = \frac{1}{3} \begin{bmatrix} 1 & a^{2} & a \\ a & 1 & a^{2} \\ a^{2} & a & 1 \end{bmatrix}, F_{h}^{*} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ a & a & a \\ a^{2} & a^{2} & a^{2} \end{bmatrix}$$
(5.49)

Where  $a = e^{j\frac{2\pi}{3}}$ 



Figure 5.99: abc-to-dq transformation in sequence components



Figure 5.100: dq-to-abc transformation from sequence components



Figure 5.101: 3P4L controller for operation in standalone mode

Because the transformations in Figure 5.99 and Figure 5.100 are computation intensive, a simple voltage mode controller, shown in Figure 5.101, is used to regulate the LV-side voltage[14]. The desired AC-voltage depends only on the value of the positive d-frame sequence. All other components are regarded as irregularities in the output voltage and need to be reduced to zero. The grid synchronizer block will be explained in the next part of this chapter.

The transfer functions for the 3P4L converter operating in standalone mode are shown in equations (5.50) and (5.51). Since the transfer function in (5.50) is the same for the dq-frame in all three sequence components, the same PI-compensator values can be used across the whole controller. The transfer function in (5.50) is a constant value. In order to achieve a proper working PI-compensator, the gain margin needs to be placed at infinite, which in turn places the lag frequency at 34Hz. The resulting PI-compensator parameters achieved from this gain margin an lag frequency are shown in Table 5.12.

$$G_{vddp-3P4L} = G_{vdqp-3P4L} = G_{vddn-3P4L} = G_{vdqn-3P4L} = G_{vddh-3P4L} = G_{vdqh-3P4L}$$
  
=  $G_{vd-3P4L} = \frac{\hat{v}_{LV}}{\hat{d}_{3P4L}} = V_{DAB2}$  (5.50)

$$T_{idz-3P4L} = H_{vd-3P4L} * T_{sm-3P4L} * G_{vd-3P4L}$$
(5.51)

Parameter	Value
PI-compensator H <sub>vd-3P4L</sub>	$K_p = 0.00138, K_i = 0.304$
Cut-off frequency	437.5 Hz
Lag frequency	34 Hz
Phase margin	153°
Gain margin	infinite

Table 5.12: PI-compensator design parameters



Figure 5.102: Compensated and uncompensated transfer functions for the standalone controller

The performance of the standalone controller is simulated by operating it at rated power. The results of the test are shown in Figure 5.103-Figure 5.105. These figures show that the desired value is reached within 20ms. They also show that the controller is also susceptible to the resonance caused by the LCL-filter. A method to reduce this resonance is presented in the next part of this section.



#### 5.4.4 Active damping

As shown in the previous section, the LCL-filter at the output of the 3P4L converter can cause resonance. Resonance is a source for harmonic distortion and can lead to converter instabilities. There are two ways to reduce the resonance from the waveforms. These are:

- 1. With the help of a resistor in series or parallel to the LCL-filter inductors or capacitors
- 2. Modifying the control scheme by adding an additional loop

The addition of a resistor leads to steady-state losses and is therefore not desired. The active damping scheme shown in Figure 5.106 will be used to reduce the resonance[14]. The optimal value for the damping factor is calculated using equations (5.52) - (5.54) and is shown in (5.55).

$$V_{abc-Cf-3P4L} \longrightarrow d/dt \longrightarrow K_{d-3P4L} d_{d-abc}$$

Figure 5.106: Active damping circuit

$$f_{res1} = \frac{1}{2\pi} \sqrt{\frac{L_{f1-3P4L} + L_{f2-3P4L}}{L_{f1-3P4L}L_{f-3P4L2}C_{-3P4Lf}}}$$
(5.52)

$$R_d = \frac{\sqrt{2}}{2\pi f_{res1} C_{f-3P4L}}$$
(5.53)

$$K_{d-3P4L} = \frac{R_d C_{f-3P4L}}{V_{DAB2}}$$
(5.54)

$$K_{d-3P4L} = 3.7 * 10^{-7} \tag{5.55}$$

A comparison between the 3P4L with and without damping is shown in Figure 5.107 - Figure 5.112. The load is reduced in half at 200ms and again restored to the rated value at 300ms. The waveforms for the situation without active damping contain a lot of resonance and the system is on the edge of stability. The currents and voltages have very high peaks, resulting in a peak power output of 7 times the rated value. It is clear that such a scenario can lead to hardware malfunction and should be avoided. On the other hand, when active damping is added to the controller, the system experiences minimal influence from the resonance caused by the LCL-filter. The voltage and current waveforms are within limits and the only ripple present on the power waveform is caused by the feedback controller.





#### 5.4.5 Feed-forward controller

To improve the controller performance, the feed-forward controller shown in Figure 5.113 is added in parallel to the feedback controller. The load current feed-forward transfer function equals [15]:

$$G_{id-ff-3P4L} = \frac{L_{f2-3P4L}}{V_{DAB2}} \left( \frac{d}{dt} i_{d-LV} - \omega i_{q-LV} \right)$$
(5.56)

$$G_{iq-ff-3P4L} = \frac{L_{f2-3P4L}}{V_{DAB2}} \left( \frac{d}{dt} i_{q-LV} + \omega i_{d-LV} \right)$$
(5.57)

$$G_{iz-ff-4P4L} = \frac{L_{f2-3P4L}}{V_{DAB2}} i_{z-LV}$$
(5.58)

The transfer functions in (5.56)-(5.58) require the derivative of the load current and a transformation to the dqz-domain. These operations can be avoided by noting that the derivative of the load current equals the voltage drop over the inductor  $L_{f2-3P4L}$ . This voltage drop equals the difference between the capacitor voltage  $V_{Cf-3P4L}$  and the grid voltage  $V_{LV}$ . Rewriting (5.56)-(5.58) in terms of voltages in the abc domain results in the single equation (5.59) with its schematic shown in Figure 5.113.



The DC-currents and active power waveforms for all 3 controllers is shown in Figure 5.114-Figure 5.119 for the case with and without feed-forward. The feed-forward controller has a positive effect on the 3P4L converter operating in boost mode. The difference between the waveforms for buck and standalone mode is that with feed-forward, the system reaches its steady-state position earlier than without feed-forward. However, the feed-forward controller causes an overshoot that is larger than the situation without feed-forward in both modes. It is suspected that the overshoot is a result of the stiff DC-voltage used for the simulations. When the 3P4L converter is connected to the rest of the SST the DC-voltage V<sub>DAB2</sub> will be less stiff. This is because  $V_{DAB2}$  is regulated by the DABs, and as Figure 5.72 shows, there is a small dip in the DC-voltage when the load changes. For this reason, the feed-forward controller can be used for all 3 modes of operation.



## 5.4.6 Overall control layout

The overall controller for the 3P4L converter is shown in Figure 5.120. There are 5 major control loops. Three of the control loops are used depending on the operation mode, and two always attribute to the final duty cycle. Just like with the overall controller for the CHB and the DAB, the 3P4L controller has a S<sub>bb</sub> switch that is used to selects how the reference d-frame current is calculated. If the converter is operating in buck mode, the reference current is a

simple mathematical function of the grid voltage and desired active power. However, if the converter is operating in boost mode, the reference current is generated by the boost mode voltage loop. Unlike the CHB and the DAB, the 3P4L converter has a second selection switch  $S_{SA}$ . If the converter is operating in standalone mode, the  $S_{SA}$  switch bypasses the current-loop and selects the output calculated by the standalone controller. The feed-forward controller increases the overall response, while the active damping circuit is used to reduce resonance in the output waveforms.



Figure 5.120: Overall controller of the 3P4L converter

# 5.5 Logic Controller

A schematic overview of the logic controller is shown in Figure 5.121. This controller operates independent from the CHB, the 3P4L and the several DAB controllers. The output of the logic controller sets the other controllers in buck, boost or standalone operation mode.

At each samping point, the logic controller determines if the utility voltage  $V_{util}$  and its frequency  $f_{util}$  are within tolerated values. If this is the case, the value of the buck-boost switch  $S_{bb}$  is simply determined by the value of the desired active power. A value of zero for  $S_{bb}$  corresponds to a power flow from the MV- to the LV-side, while a value of 1 corresponds to the opposite power flow.

When the utility voltage  $V_{util}$  or frequency  $f_{util}$  reach values outside of the acceptable range, the logic controller disconnects the SST from the LV-utility and changes its operating mode to standalone mode. Since standalone mode is the same as buck mode for the CHB and the DAB, the S<sub>bb</sub> variable is set to zero.

When the utility voltage  $V_{util}$  and frequency  $f_{util}$  return to acceptable values and the SST is still disconnected from the LV-utility grid, a timer starts up. This timer prevents the SST to close the connect switch immediately after the LV-utility voltage has returned. The return of the utility voltage is usually accompanied by transients caused by passive elements in the grid. Closing  $S_g$  immediately at the moment the voltage returns might lead to reconnection during such a transient period. After the utility voltage and frequency have been in the tolerable range for at least 2 periods, the controller assumes that the transients in the grid have damped out and the SST can reconnect to the LV-utility. Before the reconnection can occur, the voltage generated by the SST must first be synchronized with the utility voltage to avoid

large switching currents. After reconnection, the SST can return to either buck or boost mode, depending on the desired active power.



## Table 5.13: Overview of the SST

Symbol	Value = 0	Value = 1
S <sub>bb</sub>	Energy flow: MV →LV	Energy flow: MV 🗲 LV
S <sub>SA</sub>	V <sub>LV</sub> provided by utility	V <sub>LV</sub> generated by 3P4L converter
Sg	SST disconnected to LV-grid	SST connected to LV-grid
Table 514. Symbols used in Tigran 5121		

Table 5.14: Symbols used in Figure 5.121

## 5.5.1 Grid synchronization

When the 3P4L converter is operating in standalone mode, the utility grid voltage is unavailable and the PLL can no longer be used to extract its angular displacement  $\theta$ . Using

the voltage generated by the SST to extract  $\theta$  is not reliable, because the variable is no longer independent. Any distortions in the grid voltage or changes in the load can lead to a change in  $\theta$ , which in turn is used to generate a voltage causing  $\theta$  to drift from its desired value. To overcome this problem, a sawtooth generator is used to generate  $\theta$ . The generated signal has an amplitude of  $2\pi$  and a frequency equal to that of the grid frequency, expressed as (5.60).

$$\theta_{virtual} = 2\pi f_{grid} * t \tag{5.60}$$

$$v_{LV}(t) = V_{LV} * \sin(\theta_{LV})$$
(5.61)

$$v_{util}(t) = V_{util} * \sin(\theta_{util} + \delta)$$
(5.62)

The voltage generated using the virtual PLL is expressed using equation (5.61). The utility voltage can return at any given moment, and will often not be in phase with the SST voltage. To account for this phase difference, the utility voltage has an angle  $\delta$  in its expression (5.62). The phase difference between the utility voltage and SST voltage can cause large switching currents upon reconnection. In order to avoid this, a synchronization scheme is implemented.

$$\theta_{sync} = \begin{cases} \int_0^t 2\pi f_{sync} dt = 2\pi f_{sync} * t & \text{for } sync = 1 \\ 0 & \text{for } sync = 0 \end{cases}$$
(5.63)

$$\theta_{LV} = \begin{cases} \theta_{virtual} + \theta_{sync} = 2\pi (f_{grid} + f_{sync}) * t & \text{for } sync = 1\\ \theta_{virtual} & \text{for } sync = 0 \end{cases}$$
(5.64)

A schematic overview of this synchronization scheme is shown in Figure 5.123. When the sync command is set to 1 by the logic controller, the angular frequency is slightly increased. Because of this increment, the voltage generated by the SST takes less time to complete a period and the phase difference between the utility and the SST voltage changes. At a certain point the difference between the two voltages becomes (almost) zero. At this instance reconnection with the utility grid is possible without causing large switching currents.

An example of the synchronization process is shown in Figure 5.123. At 500ms the synchronization variable is set to 1. At this instance, the virtual PLL frequency is increased with  $\frac{1}{2}$ Hz. After ±175ms the phase difference between the two signals is minimal and reconnection is possible.





Figure 5.124: Overall controller overview of the SST

# 5.6 Overall Overview of the SST Controllers

An overall overview of the SST is given in Figure 5.124. The four controllers developed in this chapter are shown, along with the voltage balancing scheme of the CHB. This overview clearly shows that the controllers of the CHB, DAB and 3P4L are loosely connected. The only common connections these three controllers share are the output from the logic controller. The advantage of this structure is that the controllers don't need to be implemented on one big processing unit. Instead, cheap DSPs can be used to implement the individual controllers. Another advantage of this structure is that the modularity of the system is maintained by splitting up the complex task of controlling the SST in smaller sections.

The modularity can be expended by implementing the voltage balancing schemes on a separate DSP for each H-Bridge. Each voltage balancing scheme only needs the CHB duty cycle  $d_{CHB}$  as calculated by the CHB controller. Since the average DC-voltage  $V_{avg-DAB1}$  of all the H-bridges is already calculated by the CHB controller, this value can also be passed on to the DSPs for voltage balancing in order to reduce computation tasks. When the voltage balance controllers are implemented on a separate DSP, a synchronization signal  $S_{ynCHB}$  is needed between the different controllers to allow precise generation of the PS-PWM sawtooth signal.

Fortunately, the DSPs that are most commonly used in converters have the option of receiving an external synchronization signal[16].

# 5.7 Summary

The controllers for the different stages of the SST are presented in this chapter. The controllers of the CHB, DAB and the 3P4L converter all consist of at least a feedback and a feed-forward portion. Each converters stage has special issues which are solved by adding additional stages to the controllers. The issue of uneven DC-voltages in the CHB is solved by using a voltage balancing scheme in its controller. Another issue was the resonance caused by the LCL-filter on the LV-side of the SST. This is solved by adding an active damping scheme to the 3P4L controller.

The operating mode of the three controllers is determined by the logic controller. This controller is also responsible for disconnecting the SST from the utility grid when its voltage is outside of the tolerated range. When the utility voltage is restored, the logic controller ensures that the SST is reconnected to the grid when the utility and the SST voltage are in phase. A synchronization scheme is also available to ensure that the phase difference between the SST and utility voltage is reduced, in order to achieve minimal overcurrents during the reconnection with the grid.

The CHB, DAB and 3P4L controllers are able to regulate their stage of the SST without the need for mutual interaction. This results in independent systems that can be implemented in in separate DSPs instead of a single expensive computer. The use of separate DSPs allows preservation of the SST modularity despite its complex control scheme.

## 5.8 References

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# Chapter 6

# **SST** BEHAVIOR UNDER DIFFERENT GRID SITUATIONS

This chapter depicts the final model of the SST and its controllers operating under different scenarios. The first set of scenarios display the SST under rated conditions. The second set shows how the SST operates when irregular conditions, such as voltage dips and short circuits, occur at the MV side. Finally, the last sets of scenarios show how the SST operates when irregularities occur on the LV side. The several parameters that are inspected during the simulations are shown in Figure 6.1.



Figure 6.1: Overview of the SST and its parameters

# 6.1 SST operation under rated conditions

#### 6.1.1 Active power transfer in buck mode

The first scenario is on how the SST operates when the active power flow changes from zero to the rated value of 1 MW. The change of active power occurs at 300ms, long after the startup transients have subsided.



Figure 6.2: Active power flow



As soon as the command for the change in active power is given, the current on the LV starts to change. The change in LV current triggers an increase of active power in the LV side, but it also causes the voltage  $V_{DAB2}$  to drop. The controller of the DAB registers the voltage drop, and adjusts its phase shift to try and restore  $V_{DAB2}$ . The change in phase shift results in an increase in the power flow in the DAB, and at the same time, it causes the voltage  $V_{DAB1}$  to drop. In buck mode power transfer, the CHB controller is given the task to regulate the  $V_{DAB1}$ . To restore  $V_{DAB1}$  back to its desired value, the CHB controller adjusts the modulation index, which in turn increases the active power flow on the MV side.

#### 6.1.2 Active power transfer in boost mode

The conditions for boost mode power transfer are the same as those in buck mode. The only difference is that active power is given a reference value of -1 MW instead of 1 MW.





The command for the change in power is processed by the CHB. At t = 300 ms, the CHB controller adjusts its modulation index, resulting in a negative increase of active power. This results in a decrease in  $V_{DAB1}$ . The DAB controller compensates for this voltage drop by adjusting its phase shift, causing a negative increase of the power through the DAB, and also a voltage drop in  $V_{DAB2}$ . The 3P4L converter notices this drop and adjusts its modulation index to try and restore  $V_{DAB2}$ , resulting in an increase of current and negative increase of the active power.

The difference between buck mode and boost mode active power transfer is that in the first case, a change of active power at the LV side results in a change at the DAB, and finally in a change of active power at the MV side. With boost mode power transfer, the change occurs at the MV side and is followed by the DAB and finally the LV side.

## 6.1.3 Capacitive power at the MV side

In this scenario, the reactive power on the MV side is changed to take on the value of 1 MVAr, which is a purely inductive power flow.





The change of reactive power only affects the MV side. Since there is no active power flowing through the SST, the currents in the DAB remain unchanged, and there is no noticeable sign of activity on the LV side.

Because the behavior of the SST during a change capacitive power to 1 MVAr is similar to that of a change to and inductive value of -1 MVAr, the graphs of the latter situation is omitted.

## 6.1.4 Inductive power flow on the LV side

The change of reactive power on the LV side to a capacitive value of -1 MVAr shows similar results as the change of reactive power at the MV side, as can be seen in Figure 6.33 - Figure 6.41.





6.1.5 Capacitive power flow on the LV side

Figure 6.43 - Figure 6.51 show that changing the value of the reactive power on the LV side to an inductive value of 1 MVAr yields in undesired results.



The irregularities in Figure 6.43 - Figure 6.51 can be explained by comparing the available DC-link voltage  $V_{DAB2}$  with the required value. In order to do this, the circuit equations on the LV side of the SST are presented below.



Figure 6.52: Single phase equivalent circuit on the LV side

The circuit equations for Figure 6.52 are:

$$W_{converter} + i_1 * \left( R_{f1-3P4L} + X_{Lf1-3P4L} + X_{Cf-3P4L} \right) - i_2 * X_{Cf-3P4L} = 0$$
(6.1)

$$-V_{LV} - i_1 * X_{Cf-3P4L} + i_2 * \left( R_{f2-3P4L} + X_{Lf1-3P4L} + X_{Cf-3P4L} \right) = 0$$
(6.2)

For any combination of active and reactive power, the current i<sub>2</sub> equals:

$$i_{2} = conj\left(\frac{\tilde{S}}{\sqrt{3} * V_{LV}}\right) \Leftrightarrow conj\left(\frac{P_{LV} + j * Q_{LV}}{\sqrt{3} * V_{LV}}\right)$$
(6.3)

Where conj(x) represents the complex conjugate of the value of xand  $\tilde{S}$  is the complex power

Rewriting (6.1), (6.2) and (6.3) to calculate the converter voltage  $V_{converter}$  results in:

$$V_{converter} = \left(R_{f1-3P4L} + X_{Lf1-3P4L} + X_{Cf-3P4L}\right)$$

$$= \frac{\left(R_{f2-3P4L} + X_{Lf2-3P4L} + X_{Cf-3P4L}\right) * i_2 + \frac{V_{LV}}{\sqrt{3}}}{X_{Cf-3P4L}} - X_{Cf-3P4L} * i_2$$
(6.4)

The minimum DC-link voltage  $V_{DAB2}$  required to generate an arbitrary converter voltage  $V_{converter}$  is[1]:

$$V_{DAB2-min} = \sqrt{6} * V_{converter} \tag{6.5}$$

An apparent power S of 1 MVA can be the result of any combination of active and reactive power on the LV side. The minimum DC-link voltage  $V_{DAB2}$  for all possible combinations for S equals 1 MVA is plotted in Figure 6.54.



Figure 6.53: Minimum required DC-link voltage V<sub>DAB2</sub>. Plateau: V<sub>DAB2</sub>



sufficient  $V_{DAB2}$ , Red:  $V_{DAB2}$  to small
The red part of the plot in Figure 6.54 and the plateau in Figure 6.53 show that the chosen  $V_{DAB2}$  is not large enough to allow a purely reactive power flow of 1 MVAr on the LV side. Since  $V_{DAB2}$  is not large enough, the SST is unable to generate a pure three-phase sine on the LV side, and instead causes a neutral current to flow, as can be seen in Figure 6.48 and Figure 6.55. However, the plots do show that the chosen voltage  $V_{DAB2}$  is sufficient to allow the rated active power of 1 MW on the LV side, as stated in the specifications. Figure 6.57 - Figure 6.65 show that if the value of  $Q_{LV}$  is chosen so that the required  $V_{DAB2}$  is below the plateau in Figure 6.53, the generated waveforms have a similar shape as reactive power flow on the MV side. Figure 6.56 shows the voltage waveform for the  $V_{DAB2}$  is large enough, in this case under a  $Q_{LV}$  of 0.5 MVAr.



#### 6.2 SST operating under disturbances on MV side Some of the most common disturbances that can occur are:

- 1. Voltage dips on the MV-side while the SST is in buck mode
- 2. Voltage dips on the MV-side while the SST is operating in boost mode
- 3. Line-to-ground fault while the SST is in buck mode
- 4. Line-to-ground fault while the SST is operating in boost mode.

#### 6.2.1 Voltage dip on MV side while in buck mode

Figure 6.66 - Figure 6.89 shows the behavior of the SST in buck mode while a voltage dip occurs on the MV-side.



When the SST is operating in buck mode, the CHB's task is to ensure a constant DC-link voltage  $V_{DAB1}$ . When the voltage on the MV side drops, the CHB notices a change in  $V_{DAB1}$ , and adjusts its modulation index. This causes an increase in the MV side current. The increase in current on the MV side is just enough to compensate for the lowered voltage  $V_{MV}$ . Since the CHB is able to keep  $V_{DAB1}$  at an almost constant level, the DAB and the 3P4L converter hardly notice the changes on the MV side and are able to operate undisturbed.

#### 6.2.2 Voltage dip on MV side while in boost mode

Figure 6.78 - Figure 6.89 show the behavior of the SST for the same voltage dip on the MV-side as the previous scenario, but the difference here is that the power flow is in boost direction.



When the SST is operating in boost mode, the CHB is only responsible of controlling the desired MV-side AC current. The value of this current is a function of the desired power and grid voltage as shown in (6.6). Because the desired power remains the same, a drop in the voltage leads to an increase in the set point of the current. This increment results in an unchanged power flow, leaving the LV-side waveforms unaffected.

$$i_{d-MV}^* = \frac{2P_{desired}}{3V_{d-MV}}$$
(6.6)

The capability of the SST to operate relatively undisturbed during a voltage dip can be very advantageous in a grid with a lot of renewable energy generation. Not only is this behavior preferred, but in certain countries the grid codes require wind energy systems to ride though voltage dips without interruption[2].

#### 6.2.3 Line-to-ground fault on the MV side during buck mode operation

When an overhead transmission line touches the ground because of wind, ice or a falling tree limb, a line-to-ground fault can occur. Another type of fault that can occur is the line-to-line faults, as a result of two transmission lines coming in contact with each other. And finally there are three-phase faults that are caused when all three lines touch each other, or fall two the ground. Of the three types of faults occurring in the grid, the line-to-ground is the most common fault[3]. The behavior of the SST during such faults in buck mode is shown in Figure 6.91 - Figure 6.101.



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At the moment of line-to-ground fault, a power flow of 1 MW is thought through the SST from the MV- to the LV side. Figure 6.91 - Figure 6.101 show the waveforms after the short-circuit transients have subsided. The SST is operating in buck mode, and therefore the CHBs control strategy is to supply a constant DC voltage  $V_{DAB1}$  to the DAB. In order to generate a constant DC voltage from an unbalanced MV grid voltage, the CHB generates a MV current i- $_{MV}$  which has a strong third harmonic ripple as seen in Figure 6.114. The voltages and currents on the MV side cause a pulsating active power P and a very large reactive power Q, however, since  $V_{DAB1}$  is kept relatively constant, the waveforms on the LV side remain unaffected by the short circuit. In this case, physical limitations of the SST and its components determine whether or not the SST is able to sustain such a short circuit.

#### 6.2.4 Line-to-ground fault on the MV side during boost mode operation

The same line-to-ground fault is repeated, but this time with the SST operating in boost mode. The resulting waveforms are shown in Figure 6.102 - Figure 6.113.





In boost mode, the CHB tries to generate a constant current, but is unable to do so because of the unbalanced MV voltage. The current waveform generated by the CHB is much smaller than the one generated under buck operating mode and has a smaller harmonic ripple as can be seen in Figure 6.115. However, since the current  $i_{MV}$  isn't a perfect sine, nor does it compensate to create a constant voltage  $V_{DABI}$ , the ripple in the active power on the MV side propagates through the DAB and manifests on the LV-side waveforms.



## 6.3 SST operating under disturbances on LV-side

Just as with the MV-side, the LV-side can also experience several types of disturbances. The ones investigated are:

- 1. Disconnection from the grid to operate in standalone mode
- 2. Unbalanced loads in standalone mode
- 3. Voltage dips on the LV-side while operating in boost mode
- 4. Voltage dips on the LV-side while in buck mode
- 5. Line-to-ground faults

### 6.3.1 Disconnection from the grid to operate in standalone mode

The SST is designed to operate when the LV side is connected to a LV grid and in standalone mode. The SST is also designed to automatically switch between both modes of operation. When connected to a LV grid, the utility is responsible to supplying a constant grid voltage  $V_{LV}$ , while the SST is responsible for generating  $V_{LV}$  when operating in standalone mode.

In order to test this capability, the scenario depicted in Figure 6.116:

- 1. At t = 300 ms: the value of P goes to 1 MW.
- 2. At t = 600 ms: the LV side grid voltage drops to 0 V.
- 3. At t > 600 ms: the SST disconnects from the LV grid. Only a three-phase symmetrical load of 1  $\Omega$  remains.
- 4. At t = 700 ms: the LV utility voltage returns.
- 5. At t = 740 ms: after the SST registered at least 2 consecutive cycles of constant LV utility voltage, it starts with the synchronization process.
- 6. At t  $\approx$  801 ms: the LV side voltage generated by the SST and that of the utility are in phase and the SST can reconnect to the LV grid again.



Reconnecting to the grid can cause large transient voltages and currents if the utility grid voltage contains a phase shift with respect to the SST voltage. In order to ensure a smooth transition from grid connected to standalone mode, the controller contains a synchronization procedure. The initial waveform of the utility grid voltage can also contain ripples and turn-on transients from interaction with other parts of the grid. To avoid reconnection during such ripples, the synchronization starts after at least 2 consecutive, constant waveforms are measured in the utility grid voltage. As soon as the SST voltage is in phase with the utility grid voltage, reconnection occurs and the active and reactive power can be adjusted again to pre-disconnection values. Figure 6.122 shows that the synchronization method used for the SST allows for a relatively transient-free reconnection to the LV grid.



Should the utility grid voltage drop again before reconnection, the synchronization process simply stops and the SST monitors the utility grid voltage again for the next opportunity to reconnect. This is shown in Figure 6.129 - Figure 6.134.

#### 6.3.2 Operation in standalone mode with unbalanced loads

When operating in standalone mode, the main task of the SST is to provide a constant LV voltage  $V_{LV}$ , which is independent of the load. Since unbalanced loads are more common in the LV grid, the scenario in Figure 6.134 - Figure 6.146 show the behavior of the SST under unbalanced operation. The loads connected to the LV side of the SST are a single phase RC load of  $0.5 \Omega + 0.1$  F and a three phase symmetrical load of  $1 \Omega$ .







Figure 6.140 and Figure 6.143 show that despite the highly unbalanced load on the LV side, the LV voltage  $V_{3P4L}$  remains relatively constant as required.

#### 6.3.3 Voltage drip on LV side while operating in boost mode

Just like on the MV side, a voltage dip on the LV side is possible. However, for simulation purposes, any noticeable voltage dip would lead to the SST switching over from grid connected to standalone mode. In order to keep the SST operating in grid connected mode, the function for automatic disconnection is disabled. The behavior of the SST during a voltage dip on the LV side is simulated for operation in buck mode and shown in the graphs below.





Figure 6.147 - Figure 6.156 show the same voltage and current waveforms during a voltage dip while the SST is operating in boost mode. During the voltage drop, the 3P4L increases the LV current in order to supply a constant DC voltage  $V_{DAB2}$  to the DAB. Because of this, no effects of the LV side voltage dip is noticed on the MV side. This behavior is similar to a voltage dip on the MV side during buck operation, where the CHB increased the MV current in order to supply a constant  $V_{DAB1}$ 

#### 6.3.4 Voltage dips on the LV-side while in buck mode

Another scenario is shown in Figure 6.157 - Figure 6.166, where the LV voltage drops during operation in buck mode. In this mode, the 3P4L converter is set to supply a desired LV current. This current is a function of the desired power and voltage as shown in (6.7). Keeping the power constant, at a decrease in voltage, results in an increase in current. This behavior is displayed in Figure 6.163. This figure also shows that increasing the current may lead to very large values at lower voltage levels. In order to keep the current within a certain threshold, the value of equation (6.7) should be restricted.





#### 6.3.5 Line-to-ground fault on LV side

When a line-to-ground fault occurs in the LV grid, the SST would measure the resulting voltage dip and disconnect from the LV grid. However, it is possible that the fault occurs before the switch and the SST is unable to disconnect the fault from its terminals. In this case the SST would still disconnect from the LV grid and try to provide a three-phase sinusoidal voltage to its loads, including the fault. This scenario is depicted in Figure 6.167 - Figure 6.178.





Figure 6.167 - Figure 6.178 show the following:

- 1. The MV current has a third component that dominates the waveform, also shown in Figure 6.179.
- 2. The power through the DAB reaches an absolute value of twice the rated power.
- 3. The voltage  $V_{3P4L}$  is no longer a three-phase sinusoidal waveform.
- 4. The reactive power on the LV side reaches peaks of twice the rated value.

From these 4 points it is clear that the SST does not operate as required during a fault on the LV side. The reason behind this might be that the 3P4L controller is not fast enough to limit the short-circuit current. To protect the SST from the high currents, a circuit breaker can be placed at low-voltage terminals of the SST. Another option is to increase the bandwidth of the controller or to design a completely new control method for the 3P4L converter.



Figure 6.179: THD of i<sub>MV</sub> under line-to-ground fault on LV side

### 6.4 Summary

This chapter presented the behavior of the SST under different conditions. The following was observed from the results of the several scenarios:

- The SST is capable of bidirectional active power flow for the rated value of ±1 MW.
- When choosing the value of  $V_{DAB2}$ , both rated active and reactive power have to be taken into account. If the maximum reactive power is a positive inductive value,  $V_{DAB2}$  will be determined by the reactive power. Otherwise,  $V_{DAB2}$  will depend on the value of the rated active power.
- When the voltage drops on either the MV-side or the LV-side of the SST, the control algorithm is able to compensate for this voltage drop by increasing the current. This increment results in an unchanged power flow on the side of the voltage drop, and therefore the disturbance does not propagate through to the other side of the SST. This behavior occurs in both buck mode and boost mode.
- A different behavior is observed when a line-to-ground short circuit occurs at the MV side. In buck mode, the waveforms of the LV side remain unaffected. This is in contrast with the operation in boost mode, there the ripple caused by the short circuit does propagate through to the LV-side
- The grid synchronization method used for the SST is capable of almost transient-free reconnection to the LV grid.

- While operating in standalone mode, the SST is able to generate a constant LV voltage  $V_{LV}$  under balanced and unbalanced conditions.
- When a line-to-ground fault occurs on the LV side and the SST is unable to disconnect it, the SST is unable to operate as required. The large currents that flow during such a fault can damage the SST.

## 6.5 References

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# **CONCLUSIONS**

The goal of this research was to design a mathematical model and controller for the SST and to determine its behavior under different grid conditions. In order to achieve this goal, the research was divided in several chapters in order to focus on a certain part of the research.

A review of literature available on SSTs and related topics revealed the need for new technologies in grid systems. The increase of renewable and distribution sources, along with the liberation of the electricity market have caused the grid layout to become more complex. In order to quickly and efficiently manage the changing sources and loads, the SST can be used to dynamically adjust the energy distribution in the grid. Since many configurations of the SST have been proposed, without a clear consensus for which is the best, an independent review was done at the beginning of this research. Based on this review, the chosen architecture, topologies and modulation schemes are:

- A three stage SST architecture, consisting of an AC-DC, DC-DC and DC-AC stage, because of its high flexibility and control capabilities.
- A Cascaded H-Bridge multilevel converter with PS-PWM modulation for the AC-DC stage. This combination provides a modular structure, is able to handle higher voltages and has an easy to implement modulation technique.
- Dual-Active Bridges with Phase Shift modulation for the DC-DC stage. This topology is very compact, and when operating at a fixed voltage level with Phase Shift modulation, has a high efficiency.
- A Three-Phase Four-Leg DC-AC converter with CPWM. This topology is able to precisely handle both balanced an unbalanced loads while keeping the number of IGBTs low.. The CPWM modulation method is simple to implement and uses the conventional abc-frame duty cycle.

A case study was applied to the chosen topology. The resulting circuit shows that a SST based on this topology is extremely modular. In order to increase the voltage level on the MV-side of the SST, the number of levels in the CHB simply has to be increased. To increase the current handling capability of the DC-AC side, one or more 3P4L converters can be added in parallel. The proposed topology also includes a novelty because the combination 3P4L converter and LCL-filter has not been used in three stage SST architectures.

The circuit for the case study contained a total of 260 IGBT switches. In order to reduce the computation time of simulations, the circuit models of the SST have been converted to averaged models. Since the high frequency behavior of the converters is absent in the averaged models, a massive reduction in computational time is achieved. This reduction in computation time in most cases is a factor of 100 or more.

In order to properly regulate the currents, voltages and power flow of the SST, a controller has to be designed for each stage of the SST. The controllers developed for the SST are:

- Feedback controllers to keep a converter parameter at a desired value
- Feed-forward controllers in parallel with feedback controllers, these are optional but recommended as they greatly improve dynamic performance
- A voltage balancing scheme to ensure an equal DC-link voltage among the several Hbridges in the CHB
- A damping scheme to damp out oscillations caused by the LCL-filter on the AC-side of the 3P4L converter
- A synchronization scheme to avoid large currents during reconnection with the LVside utility
- A logic controller to determine the operation mode of the SST and to disconnect or reconnect the LV-side to the utility

When the controllers are loosely coupled, just as proposed in this research, they can be implemented on separate DSPs instead of one big processing unit. The use of separate DSPs preserves the modularity of the SST on both circuit and control level.

Investigation of the SST operation under different conditions shows the following:

- One of the parameters that limits the maximum capacitive power on the LV-side is the DC-link voltage  $V_{\text{DAB2}}$
- If a voltage dip occurs on one side of the SST, the controllers react by increasing the current value, thus keeping the power flow constant. Because the power flow is kept constant, the other side of the SST is unaffected by the voltage drop
- During a short circuit in buck mode on the MV-side, the SST is able to keep the DClink voltage constant. This prevents the short circuit to propagate through to the LVside. However, in boost mode the SST is unable to keep the DC-link voltage constant and the disturbance on the MV-side is noticed on the LV-side
- The grid synchronization scheme is able to prevent large overcurrents during reconnection of the LV-side and the utility
- The SST is able to generate a constant AC-voltage in standalone mode, regardless of the type of load on the LV-side
- Line-to-ground faults on the LV-side cause unacceptably large currents and need to be disconnected

The overall conclusion of this research can be summarized by stating that the topology presented here along with its controller, is shown to be capable of solving challenges faced with the increased complexity of grid systems.

# **Recommendations and Future Work**

This research proposed the topology and control method for a SST. Simulations of this SST show exceptional performance at both rated conditions and grid disturbances. However, due to time restraints, certain aspects of the SST have not been covered in this thesis.

#### 1. Controller optimization

The controllers used in this research are limited to PI and simple feed-forward controllers. In recent years other, more robust controllers have appeared in the field of power electronics. In order to achieve better performance, it is worth to investigate the application of these new controllers for the SST.

#### 2. Protection schemes

Chapter 6 shows that there are conditions, such as short-circuits, under which the SST in unable to sustain the desired voltage and currents. These conditions can lead to permanent damage of the SST and other grid components. In order to ensure a reliable operation, a protection scheme must be added to the SST. This can be a physical device, such as a circuit breaker, or it can be an algorithm that restores the currents to its safe operation point.

#### 3. Autonomous operation

The control scheme developed during this research still requires a grid operator to specify the active and reactive power that should flow through the SST. In autonomous mode, the value of the active and reactive power is automatically determined using respectively the frequency and voltage drop. When many SSTs are responsible for maintaining constant voltage and frequency in the same part of the grid, the action of one SST can be perceived by another as a disturbance. This scenario requires intercommunication between different SSTs, which is out of the scope of this research.

#### 4. Start-up procedure

This research did not take the start-up procedure of the SST into account. The capacitors were assumed to have an initial voltage level equal to their rated value, and inrush currents were ignored. In practice the capacitors have to be pre-charged before the converter can properly function. Additional measures are also taken into account to avoid large inrush currents when starting the converter. Since this research only focused on the behavior of the SST in operation mode, the development of a start-up sequence is left for future studies.

The scope of this thesis is limited to the mathematical modeling of the SST. There is much work to be done before the proposed architecture is ready for mass production. Much of this work involves the designing and building the SST. Below are some of the aspects that still require investigation:

#### 1. Efficiency calculation

One of the frequent asked questions is on the efficiency of the SST. Since the system was assumed to be losses during this research, no quantitative answer could be given to this question. In order to calculate the efficiency of the SST, a loss model has to be developed. These calculations can be verified through practical design and by building the SST.

### 2. Weight and size reduction

One of the advantages of the SST is its reduced size and weight. The amount of reduction possible with the SST can only be determined by optimizing the SST design for maximum power density.

#### 3. Reliability and availability

When integrating new components into the grid, utility operators often want to know the reliability and availability of that component. A risk analysis can be used to determine these two factors. Such an analysis requires real world data, which can only be acquired when the SST is put into operation under different conditions for a longer period of time.

#### 4. Cost estimation

Another unanswered question from this research is the cost of a commercial SST. Again, this is a question that can be answered with a practical design.

# **APPENDICES**

# A1. SST PROTOTYPE DESIGNED AT TNO

As mentioned in the introduction, researchers at TNO were in the process of developing an SST. The prototype build was a single phase model and consisted of a CHB with 3 H-bridge modules with a DAB connected to the DC-side of each H-bridge module. A DC-AC stage was not included in the model because a conventional three-phase inverter was deemed sufficient. The experimental setup of the SST is shown in Fig. 1.



Fig. 1: SST prototype as developed by TNO

### A2. THE CONVENTIONAL THREE-PHASE CONVERTER

One thing that should be noted is that the control schemes developed for the 3P4L converter are not exclusively developed for a converter with 4 switching legs. As shown in Chapter 5 - Figure 5.120, the output signal of the controller is an abc-signal. The modulator translates this signal to an abcN-signal that can be used for the 3P4L converter.

To compare the performance of the 3P4L converter with the conventional three-phase converter, the controller in Figure 5.120 is connected to the circuit in Fig. 2. With the exception of the neutral leg, both converters are identical.

The same non-linear load is connected to both the 3P4L and the conventional converter. The relevant results are plotted in Fig. 3-Fig. 8. The major difference between the 3P4L and the conventional converter is seen in the DC-current. The current on the DC-side is twice as large for the conventional converter. With the exception of a small dent in the AC-voltage of the 3P4L converter, the AC-voltages generated by this converter are closer to a perfect sine than those of the conventional converter. Another difference between the converter outputs is seen in the AC-current. Although phase B and C are loaded with a linear load, the non-linearity of phase A has a distorting effect on the other two phases at the conventional converter. This distortion is absent in the AC-current waveforms for the 3P4L converter.





### **A3. HARMONIC DISTORTION**

The switching actions in power electronics cause distorted voltages and currents. Although the distorted waveforms may appear complex, they can always be decomposed into multiple waveforms called harmonics. Harmonics are sinusoidal waves with a frequency of an integer multiple of the fundamental frequency. For example, for a fundamental frequency of 50Hz, the 2<sup>nd</sup>, 3<sup>th</sup> and 4<sup>th</sup> harmonic waves will be occur at 100Hz, 150Hz and 200Hz respectively. The decomposition of a square wave voltage into its harmonic components is shown in Figure 9.1[1].



Figure 9.1: Decomposition of a square wave voltage (a) square wave (b) harmonic equivalent

Any periodic function f(t) can be written as Fourier series, which is a sum of sinusoids[1]:

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n * \cos(n * \omega * t) + b_n * \sin(n * \omega * t)$$
(9.1)

Where  $\omega = 2 * \pi * f$ 

f is the fundamental frequency

Equation (9.1) can be rewritten as[1]:

$$f(t) = \sum_{n=0}^{\infty} c_n * \cos(n * \omega * t + \theta_n)$$
(9.2)

Where  $c_0 = a_0$  and  $\theta_0$ 

$$c_n = \sqrt{a_n^2 + b_n^2}$$
  
$$\theta_n = -\tan(\mathbf{b}_n / \mathbf{a}_n)$$

Each cosine term in (9.2) is called a Fourier component or a harmonic of the function f(t) with "n" harmonics.

- c<sub>n</sub> is the amplitude component
- $\theta_n$  is the component phase
- $c_0 = a_0$  is the DC component
- c<sub>1</sub> is the fundamental harmonic of the periodic function f(t)

The amount of distortion caused by the n<sup>th</sup> harmonic is defined as[2]:

distortion<sub>n</sub> = 
$$\frac{\sqrt{c_n^2}}{\sqrt{c_1^2}}$$
 (9.3)

Where c<sub>n</sub> is the amplitude of the nth harmonic and c<sub>1</sub> is the amplitude of the fundamental

The total distortion caused by a waveform is called the Total Harmonic Distortion (THD) and defined as the ratio between the RMS value of all the harmonics to the RMS value of the fundamental harmonic[3].

$$THD = \frac{\sqrt{c_2^2 + c_3^2 + c_4^2 + \dots + c_n^2}}{\sqrt{c_1^2}} * 100\% \Leftrightarrow THD = \frac{\sqrt{\sum_{n=2}^{\infty} c_n^2}}{\sqrt{c_1^2}} * 100\%$$
(9.4)

#### A4. ABC-TO-DQZ TRANSFORMATION

The abc-to-dqz transformation is a transformation of coordinates from the three-phase stationary system to the dqz reference coordinate system. The method of transforming from one frame to the other is shown in (9.5) - (9.8)[4]. This method is the amplitude invariant version, which means that when transforming from one frame to the other, the amplitude remains the same.

$$x_{dqz} = F_{dqz} x_{abc} \tag{9.5}$$

$$x_{abc} = F_{dqz}^{-1} x_{dqz} \tag{9.6}$$

$$F_{dqz} = \frac{2}{3} \begin{bmatrix} \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{4\pi}{3}\right) \\ \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}$$
(9.7)

$$F_{dqz}^{-1} = \frac{2}{3} \begin{bmatrix} \sin(\theta) & \cos(\theta) & 1/2\\ \sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) & 1/2\\ \sin\left(\theta - \frac{4\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) & 1/2 \end{bmatrix}$$
(9.8)

It should be noted that the abc-to-dqz transformation presented here is slightly different from the conventional form[5]. This method is the default version included in Simulink and is therefore used throughout the rest of the thesis[6].

When the three phases are balanced, the z-frame equals zero and the vectors can be represented as Fig. 9. An example of this transformation is shown in Fig. 10 - Fig. 13. The phase displacement is extracted from the reference signal using a PLL as presented in chapter 5. If the original signal is in phase with the reference signal, the resulting dq-variables only contain a d-coordinate. If a phase shift is added between the reference and the original signal, the resulting transformation yields a d- and a q-coordinate.



#### A5. SEQUENCE DECOMPOSITION FOR CONTROL PURPOSES

The conventional method of sequence decomposition results in three sequence components:

- The positive sequence, rotating counter-clockwise at twice the grid frequency
- The negative sequence, rotating clockwise at twice the grid frequency
- The homopolar sequence, shows up as a single sine at grid frequency

The positive sequence can be transformed to the dq-frame using the normal Park transformation, while the negative sequence can be transformed by feeding  $-\omega_g$  to the park transformation matrix instead of  $\omega_g$  shows that the vectors of the homopolar sequence are in phase with each other. In order to convert the homopolar sequence to the dq frame, the homopolar phase B and C are spatially shifted by respectively 120° and 240° with the help of a rotational matrix[7]. The transformation matrices for decomposing an abc-waveform into sequence components and back are presented in (9.9)-(9.15).

$$x_{abc-p} = F_p x_{abc} \tag{9.9}$$

$$x_{abc-n} = F_n x_{abc} \tag{9.10}$$

$$x_{abc-h} = F_h^* x_{abc} \tag{9.11}$$

$$F_p = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}$$
(9.12)

$$F_n = \frac{1}{3} \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix}$$
(9.13)

$$F_h^* = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ a & a & a \\ a^2 & a^2 & a^2 \end{bmatrix}$$
(9.14)

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} x_{a-p} + x_{a-n} + x_{a-h} \\ x_{b-p} + x_{b-n} + x_{b-h} \\ x_{c-p} + x_{c-n} + x_{c-h} \end{bmatrix}$$
(9.15)

An example of the sequence decomposition is shown in Fig. 15 - Fig. 22. The original waveform in Fig. 15 is first decoupled in sequence components before being transformed to the dq-frame. Since the sequence components are a three-phase balanced sine, the resulting dq-transformation is a constant DC signal. Compared to the conventional dqz-transformation in Fig. 16, this method is better suited for PI-compensators.





### A6. CONFERENCE PUBLICATION

A. Shri, M. Gerber, and J. Popovic, "Design and control of a Three-Phase Four-Leg inverter for Solid-State Transformer applications," in *EPE'13 ECCE Europe 15th Conference on Power Electronics and Applications*, 2013.

### **A7. CONFERENCE POSTER**

Conference:	15th European Conference on Power Electronics and Applications
Date:	3-5 September 2013, Lille (France)
Topic:	Power Electronics for the grid: Microgrid control
Title:	Design And Control Of A 3P4L Inverter For Solid-State Transformer
	Applications

### **A8. REFERENCES**

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# **DESIGN AND CONTROL OF A THREE-PHASE FOUR-LEG INVERTER FOR SOLID-STATE TRANSFORMER APPLICATIONS**

A Shri **J** Popovic MB Gerber **JA Ferreira** 

#### **Motivation** The DC/AC stage of SSTs is often required to

operate at low-voltage and high-power conditions

with both balanced and unbalanced loads. The

conventional three-phase converter with L- or LC-

**1.** Topology

filter was not designed for these conditions.

• Precise control of all 3 phases and neutral

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-174

-K‡

1. In  $\alpha\beta$ -frame 2. In γ-frame

Optimal design:

 $f_{res-\gamma} = w * f_{res-\alpha\beta}$ 

Calculate

Calculate L<sub>f1</sub>; L<sub>f2</sub>; L<sub>fN</sub>; C<sub>f</sub>

Determine Voltage drop ΔV & larmonic distortion HD<sub>sw</sub> at f<sub>3P4L</sub>

3P4L Converter with LCL-Filter

#### **Objectives**

- Provide a procedure for calculating the passive values of the LCL-filter
  - Create a control scheme with sufficient performance under both balanced and unbalanced loads
  - Propose a damping method to eliminate oscillations caused by the LCL-filter

#### **3. Control Scheme**

#### • Proposed combination of 3P4L converter with LCL-filter performs satisfactory under balanced and unbalanced loads.

• An iterative algorithm is presented to determine optimal LCL-values

Conclusions

- •The damping scheme is able to significantly reduce oscillations
- •The control scheme is able to generate a constant voltage under different conditions

