Non-intrusive Near-field Characterization of Microwave Circuits and Devices

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DOI
10.4233/uuid:b6866d16-9a29-4fac-9f73-42a5ad26fc0f

Publication date
2017

Document Version
Final published version

Citation (APA)
Hou, R. (2017). *Non-intrusive Near-field Characterization of Microwave Circuits and Devices*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:b6866d16-9a29-4fac-9f73-42a5ad26fc0f

Non-intrusive Near-field Characterization of Microwave Circuits and Devices

Non-intrusive Near-field Characterization of Microwave Circuits and Devices

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op dinsdag 24 januari 2017 om 10:00 uur

door

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ISBN 978-94-6295-592-9

An electronic version of this dissertation is available at
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All perception is a selection from a totality of possibilities and a limitation of what is possible in the future.

Werner K. Heisenberg

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1

Introduction

1.1. Motivation

Ever since the industrial revolution, technological development has brought to human kind unprecedented prosperity. In the last century, despite the two world wars, global population quadrupled from 1.5 billion to 6 billion whereas the gross world product increased 37 times from 1.1 trillion dollars to 41 trillion dollars (inflation corrected), according to statistics from the World Bank.

This growth is unfortunately accompanied by environmental impacts, such as pollution and climate change, casting doubts on the sustainability. The World Health Organization estimated that air pollution accounted for 7 million deaths (i.e. one in eight deaths) in 2012. Fourteen of the fifteen hottest years have been in the 21st century, reported in 2015 by the World Meteorological Organization. Environmental sustainability increasingly challenges the industrialization and economic development.

A potential solution to the environmental challenges is the information and communication technology (ICT). ICT significantly transforms business processes, improves resource allocation, transportation and facilitates global collaboration. Accounting for 2-3% global green-house gas emission, ICT boosts overall productivity by 40% among OECD countries, reported by the International Chamber of Commerce in 2010. Yet the use of ICT is still expanding in an unparalleled speed. Cisco Systems reported in 2012 that the internet traffic had increased nearly 100 times in the previous 10 years, from 356 petabytes per month in 2002 to 31,338 petabytes per month in 2012. Even more outstanding growth of 1000 times in the previous 7 years, from 0.9 petabytes per month in 2005 to 885 petabytes per month in 2012 was experienced by the mobile internet traffic.

Information explosion in mobile networks, fueled by an unlimited exponential growth of Moore's law in the semiconductor industry, casts new doubts to its

sustainability. According to Shannon's law, information rate in a communication channel is theoretically limited by the channel bandwidth and signal-to-noise ratio (SNR). Since in practical scenarios both frequency spectrum and electrical power are physically finite quantities that cannot increase exponentially over time, the efficient use of these resources comes into focus of research for new wireless communication systems.

The efficient use of frequency spectrum has been improved by the introduction of complex digital modulation schemes such as the Orthogonal Frequency Division Multiplexing (OFDM) as used in the 4th generation mobile networks. The enhancement of power efficiency of transmitters for wireless applications, or even more particularly, the improvement of the power efficiency of the large semiconductor transistors used in these wireless transmitters forms the driving motivation for this PhD study.

1.2. Background

Mobile networks use radio transmissions between their end-user equipment (UE), e.g. mobile phones, and their (macro-cell) radio base stations (RBS). Since RBSs need to provide high transmit powers, while functioning 24/7, their energy consumption typically dominates the CO_2 footprint of a mobile network. Within the RBS, the final stage power amplifier (PA) is used to boost the transmit signals from milli-Watts levels to hundreds of Watts. It is this final-stage PA that impacts the system efficiency the most.

Final stage PAs in a modern RBS are operating in high-efficiency classes, (e.g. class B, J or F). Furthermore, circuit-level techniques, such as Doherty or Chireix architectures, are often employed to enhance efficiency for complex modulated signals with large peak-to-average power ratios (PAPR). Final stage PAs are powered by large-periphery high-power transistors. Ultimately, it is the efficiency of these power transistors that determine the PA efficiency.

Today, RBS final-stage PAs are predominantly using laterally-diffused metal-oxide-semiconductor (LDMOS) field-effect-transistors (FET), mainly because their silicon substrates have low costs. The trend of RBS PAs towards higher frequencies and higher powers embraces another type of power devices, namely gallium nitride (GaN) high-electron-mobility-transistors (HEMT). These GaN HEMTs provide higher break-down voltages, higher current handling and higher thermal conductivity, yielding significantly better power density capabilities than silicon based LDMOS devices. These basic properties make GaN very attractive for future RBS PA applications.

For both LDMOS and GaN transistors, power can be scaled up by duplicating transistor fingers in "parallel" to form a transistor cell, and duplicating these cells in parallel to form a power transistor core, also referred to as a "die". Unfortunately, this power scaling is not linearly proportional to the aggregated gate width. In reality, duplicating transistor cells has a diminished return in power and a degradation in efficiency. Especially in RBS applications, where

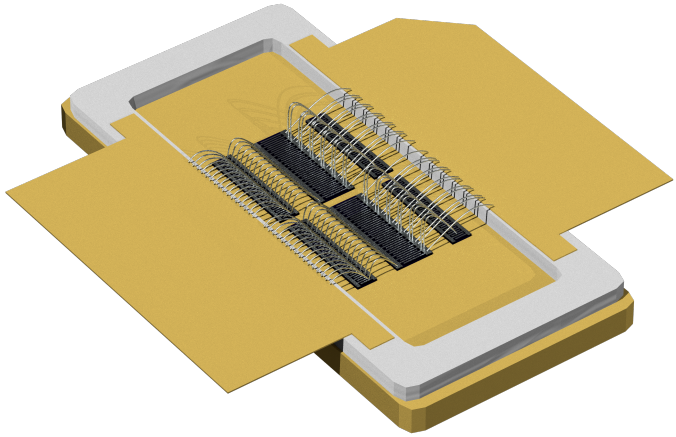

Figure 1.1: A packaged LDMOS power transistor device with its ceramic lid removed.

the amount of parallel fingers is large and aggregated power is high, efficiency degradation becomes an issue and the related energy waste works out to be significant.

These power scaling issues have been largely attributed to spatially distributed effects. More specifically, due to uneven temperature distribution across a transistor die and the uneven electromagnetic (EM) coupling between bondwires, identical transistor cells and fingers in "parallel" do not operate in identical conditions.

Although these distributed effects can be plausibly explained in theory and simulated from electrical-thermal-EM device models, they are, due to their multi-physics nature, very difficult to be uniquely quantified and verified in experiments.

Inside a modern high-power transistor package, there can be multiple semiconductor dies, with their transistors grouped in cells, whose input and output are connected by bondwires to the package leads or matching capacitors (see Fig. 1.1). Such a 3 dimensional complex circuit does not possess well-defined wave-ports for conventional microwave measurements. Even if such a packaged transistor can be disassembled, the measurement of individual components is inconclusive because the change in parasitics, like crosstalk between two adjacent bondwires or through the thermal conductivity of the transistor die, invalidates the EM and temperature distribution in real-life operation. An alternative method, capable of measuring in-circuit electrical parameters in-situ, yet does not influence its normal operation, is keenly in need.

1.3. Purpose of this Research

To aid the future development of more energy-efficient RF power devices that suffer less from "power scaling" degradation issues, the objective of this research work is:

"to develop novel measurement techniques for detailed high-power transistor characterization, which are:

1. performed in-situ, while the device under test is operating under its optimum or otherwise specified conditions;
2. non-intrusive mechanically and electrically;
3. capable for high-resolution inspection, so that bondwires, cells and even fingers of a transistor can be individually distinguished and characterized;
4. capable to measure in-circuit electrical parameters such as reflection coefficients and absolute voltage- and current-waveforms."

All these features need to be realized and satisfied simultaneously in order to be able to quantify distributed effects in power transistors in a clear and well-defined manner. First of all, an in-situ measurement approach is necessary since a power distribution only exist while the device is operating. Secondly, non-intrusiveness is essential since the perturbation of electrical contacts, magnetic coupling or thermal conductivity may alter power distributions across transistor fingers. Thirdly, high resolution for individual bondwires, cells and fingers is needed since uneven power distribution can be very localized. Last but not least, (absolute) voltages and currents in magnitude and phase at fundamental and harmonic frequencies are needed to fully characterize the distribution of loading conditions and power in such a complex RF-power device.

1.4. Scope of this Research

Non-intrusive measurement techniques are around for quite some time. A general survey of these techniques can be found in [1], where existing techniques are categorized based on their physical principles. More specifically, electron-beam methods are performed by a Scanning Electron Microscope (SEM). Photo-emissive probing is based on photoelectrons excited by a pulsed laser beam. Both techniques require a vacuum chamber with numerous feedthroughs. Electro-optical sampling is based on Pockels effect. It requires a piece of miniaturized electro-optical crystal, whose refraction index changes with the electric field. Electric force microscopy relies on Coulombic interaction. Coulomb force is detected typically at a distance of 50 nm, a demanding position accuracy. Capacitive probing is based on displacement current induction. It requires a highly sensitive pre-amplifier very close to the probe tip.

This research is focused on the capacitive probing technique for the sake of instrumentation simplicity. Costly and complex equipment such as vacuum

chambers, miniaturized electrooptical crystals, pulsed lasers and nanometer positioning instruments are, in such an approach, not necessary. Moreover, the focused application of high-power RF device characterization simplifies the electric probe approach even further. Due to the strong electric field in these applications and high capacitive coupling at microwave frequencies, the sensitivity of the electric probe is much better than low-frequency low-power attempts. A technique based on a passive electric probe without any tip amplification is therefore very attractive for its low-cost and simplicity.

1.5. Thesis Organization

The main body of this thesis focuses on the development of the contactless measurement technique intended for RF power devices characterization and evaluation.

In view of this, Chapter 2 gives the starting point. Here the microwave structure that we aim to contactlessly characterize, is considered as an inverse problem. Doing so, the electric-field information detected by a field probe can be directly linked to the in-situ reflection coefficient of interest. For this purpose, an EM model assisted near-field technique is proposed to solve the inverse problem. This ratio oriented contactless characterization technique, suited for the measurement of (distributed) reflection coefficients was validated using a passive bondwire structure.

Chapter 3 extends the proposed technique to include the absolute magnitude measurement of voltages and currents, by relating them to a calibrated output power measurement. To show the practical value of this (extended) contactless measurement technique, a 400-W Doherty PA board was characterized for its electrical interactions between main and peaking transistors. Doing so, for the first time, these interactions were quantified in an experimental manner. This interesting approach allows to monitor the most relevant mechanisms and detect problems in the Doherty efficiency enhancement in power back-off operations.

Chapter 4 extends the developed contactless in-situ measurement technique to absolute power and phase calibration over the harmonic frequencies in order to facilitate waveform reconstruction. Note that such a capability is very important in the characterization of power devices and in particular to GaN devices, whose electrical performance is strongly dependent on the applied harmonic terminations.

Within Chapter 5, we further improve the resolution of the proposed measurement technique in order to be able to distinguish the voltages and currents at individual bondwire terminals of a packaged high-power LDMOS transistor with its internal harmonic terminations.

Next, in Chapter 6, the distributed effects of a 100 W GaN HEMT are successfully characterized, using an improved probing technique to measure distributed in-circuit voltages directly on the device fingers. This later approach further in-

creases the reliability of the in-situ field probe approach into the level that broken device fingers can be detected in clear and unified manner. The strength of this technique is demonstrated by the characterization of the absolute currents and voltages of individual transistor cells and fingers at fundamental and the second harmonic frequencies.

Finally, Chapter 7 provides an intriguing spin-off application of the developed contactless measurement techniques. Here a miniaturized contact-less measurement setup is developed and implemented as a six-port reflectometer, which is integrated inside the package of a RF-power transistor. Note that such feature can provide load monitoring and load protection at the transistor level, which is very useful in applications that experience strongly varying load conditions like solid-state microwave heating systems.

Chapter 8 concludes the research in this thesis and provides to the most important conclusions and recommendations for future work.

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2

Contactless Measurement of In-circuit Reflection Coefficients

[1]This chapter introduces a new method for the contactless measurement of in-circuit reflection-coefficients (Γ_{insitu}). The proposed method relies on an electromagnetic (EM) model of a known passive structure (e.g. a bondwire array) that can be embedded in any unknown circuitry. By operating the circuit to be investigated normally and probing locally the EM field induced by the known structure inside this circuit, the in-circuit reflection coefficients at boundaries of this structure under the actual operating conditions can be directly obtained.

The proposed method is demonstrated on a single bondwire and verified by a set of independent measurements. The high potential of the proposed method for future applications is demonstrated by applying it to a bondwire array that mimics the output connections of a large-periphery high-power device.

2.1. Introduction

The accurate knowledge of the loading conditions seen by components embedded in a microwave circuit is crucial for troubleshooting as well as performance optimization. To motivate this, consider the drain connections inside the package of a typical high-power transistor, as shown in Fig. 2.1. A column of identical transistor cells are connected in parallel and wire-bonded to the drain lead. The in-circuit reflection coefficients ($\Gamma_{1,2,\cdots,N}$), seen by the individual transistor cells in large-signal operation, directly affect the gain, efficiency and

[1]Parts of this chapter have been published in Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International [1].

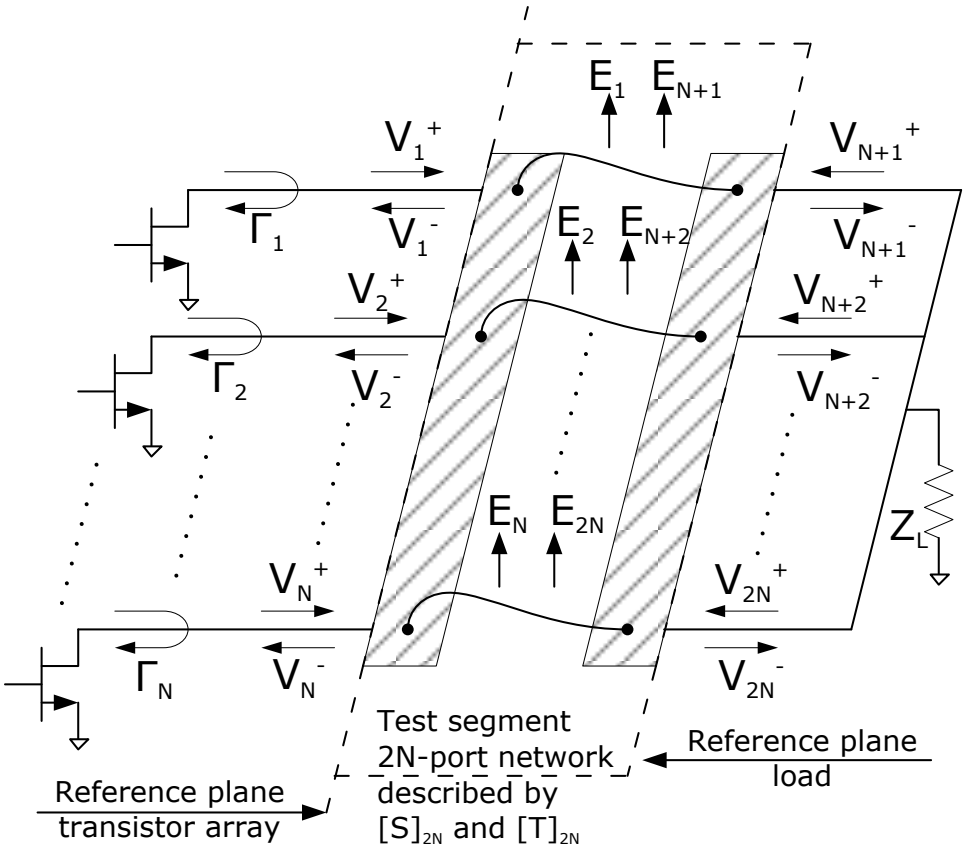

Figure 2.1: Application example of the proposed method: a packaged high power device with drain terminals connected by a strip and wire-bonded to the package lead. For such a structure it is advantageous to study, using a non-interfering measurement, the actual loading conditions ($\Gamma_{1,2,\ldots,N}$) and power distribution of the individual transistor cells.

output power of the transistor. The detailed knowledge of these reflection coefficients enables a refined optimization of high-power transistors based on a deep insight of their load conditions per transistor unit-cell.

Despite their importance, these individual loading conditions (Γ_{insitu}) are troublesome to measure until now. Any attempt to create a probing port disturbs the power distribution, parasitics and thermal effects. For this reason, a contactless measurement method, capable of measuring the actual reflection coefficients within a normally operating circuit is very appealing.

Previous works have demonstrated contactless S-parameter measurement by probing the magnetic [2] or electric [3] field above a uniform transmission line. Doing a similar measurement above an irregular sub-structure (e.g. a bondwire), would require calibration of the contactless system based on a

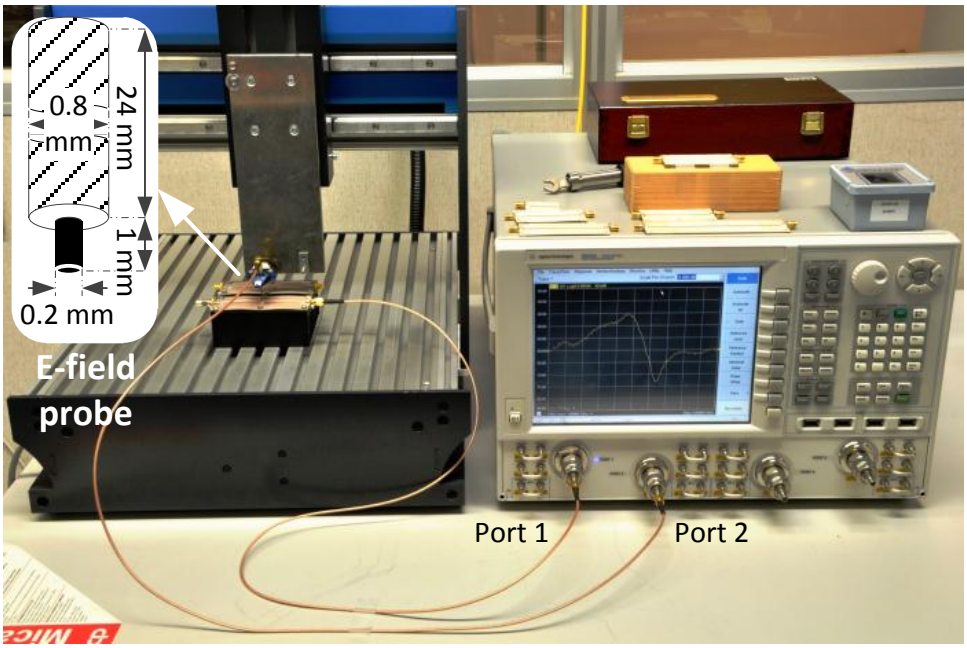

Figure 2.2: The field measurement setup consisting of a VNA, a numerically controlled 3D positioner and an E-field probe.

physical duplicate of the sub-structure [4, 5]. Some duplications, such as copying bondwires, if not assisted by the original manufacturer, can be inaccurate, expensive and time-consuming. Due to these difficulties, the measurement of *in-situ* reflection coefficients as shown in Fig. 2.1 has not yet been solved by existing techniques.

The proposed method relies on a numerical EM model of the bondwires embedded in a device-under-test (DUT), instead of a physical duplicate. In the next sections, we present the measurement principle, its procedure and compare measured results with reference data from a set of conventional techniques. Finally, we demonstrate the high potential of the proposed method to optimize high-power transistors by measuring Γ_{insitu} at terminals of multiple parallel bondwires.

2.2. Method Description

2.2.1. Measurement principle

As shown in Fig. 2.1, N bondwires can be modeled as a 2N-port network. At any port i, the scattered voltage V_i^- is a linear combination of all $2N$ incident

voltages, i.e.

$$V_i^- = \sum_{j=1}^{2N} S_{ij} V_j^+, \quad i = 1, 2, \cdots, 2N, \tag{2.1}$$

where S_{ij} is the well-known S-parameter from port j to i. Similarly, at any location k in space, the vertical component of the electric field E_k induced by the bondwires is also a linear combination of all incident voltages, expressed as

$$E_k = \sum_{j=1}^{2N} T_{kj} V_j^+, \quad k = 1, 2, \cdots, 2N, \tag{2.2}$$

where T_{kj} is the voltage to E-field transfer from port j to location k. Note that S- and T- parameters depend only on the 2N-port network. If its geometry and material composition are known, S_{ij} and T_{kj} are also known and can be numerically solved by a 3D EM simulator.

For any DUT containing the bondwire structure, it is possible to probe the vertical component of the E-field E_k at $2N$ locations above the bondwires (see Fig. 2.1). Note that during these measurements the DUT is operating in its normal condition. The measured field quantities form $2N$ equations, which allows us to solve the $2N$ unknown incident voltages V_j^+ from (2.2) and scattered voltages V_i^- from (2.1). Finally, as seen from Fig. 2.1, the in-circuit reflection coefficient Γ_l at port l can be readily derived as

$$\Gamma_l = \frac{V_l^-}{V_l^+}. \tag{2.3}$$

2.2.2. Measurement Procedure

The N bondwires embedded in the DUT are considered as the test segment. Vertical and oblique photographs of the bondwires are taken through a microscope in order to obtain their 3D geometry.

The resulting bondwire model is configured as a 2N-port network in a 3D EM-field simulator, i.e. Ansoft HFSS, to solve the S- and T-parameters. For each frequency of interest, a normalized incident voltage of $1\angle 0^\circ$ V excites port j, yielding a transfer $S_{ij} = V_i^-$ to port i and $T_{kj} = E_k$ to location k in space. In total, $2N \times 2N$ S-parameters for all port-port transfers and $2N \times 2N$ T-parameters for all port-location transfers are calculated at each frequency of interest.

After that, the actual field at the $2N$ locations are measured while the DUT operates in its normal condition. The measurement setup for our experiments is shown in Fig. 2.2. A vector network analyzer (VNA) excites the DUT through port 1 and senses the vertical components of the E-field above the test segment by a field probe at port 2. The field probe, made of a piece of semi-rigid coaxial cable, is mounted vertically on a numerically controlled 3D positioner.

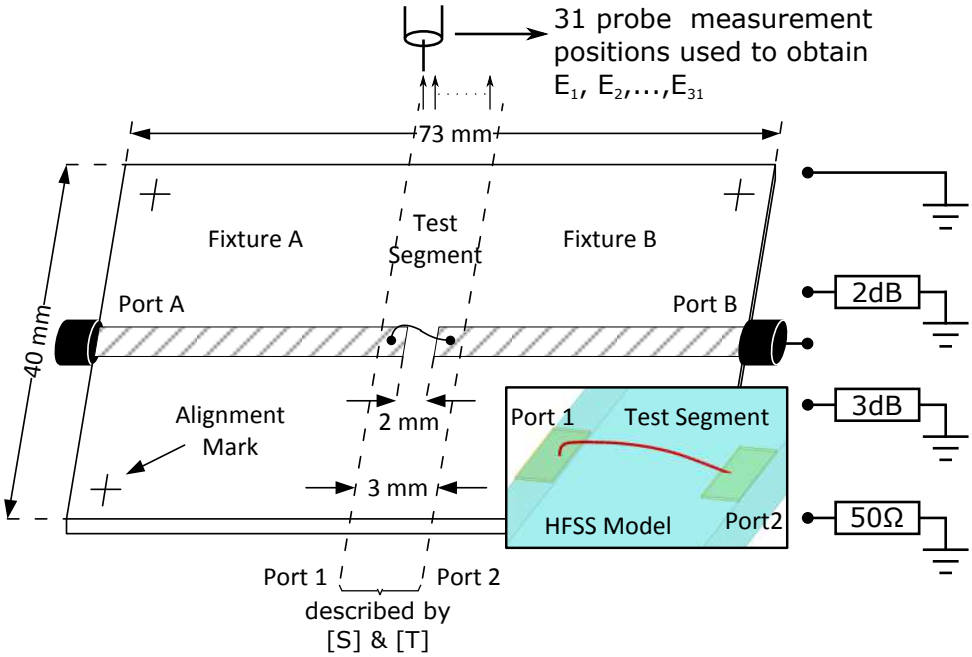

Figure 2.3: Simple test fixture with a single bondwire used for the verification of the proposed method; (inset) the HFSS model of the test segment. In the verification, 4 independent terminations are used, namely a short, 2-dB-attenuation + short, 3-dB-attenuation + short and a 50-ohm match.

The VNA measures the uncalibrated transmission parameter $S_{21,k}$ as E_k at probe position k. Note that the uncalibrated S_{21} is a relative indication of vertical E-field strength. Converting it to absolute field intensity is not required to compute reflection coefficients, since the unknown ratio between $S_{21,k}$ and E_k scales all port voltages, V_i^- and V_j^+, by the same amount, and eventually drops out of the computation of the reflection coefficients.

In the final step, $2N$ equations are formed from (2.2) and (2.1) to solve V_j^+ and V_i^- at all $2N$ ports, yielding the measured *in-situ* reflection coefficients at any ports using (2.3).

2.3. Measurement Validation

In order to validate the proposed method, the test structure, shown in Fig. 2.3, is manufactured. The test structure has 2 pieces of 35-mm long (each about half-wavelength at 3 GHz) 50 Ω microstrip built on a 30-mil thick Rogers 3003 substrate ($\epsilon_r = 3$). The microstrip has a 2 mm gap in the middle, which is bridged by a gold bondwire of 35 μm diameter. The bondwire, together with 0.5 mm long microstrip sections at each side of the gap (between virtual port 1 and 2 in Fig. 2.3) are considered as the test segment.

To obtain the essential information of the test segment, it is first modeled

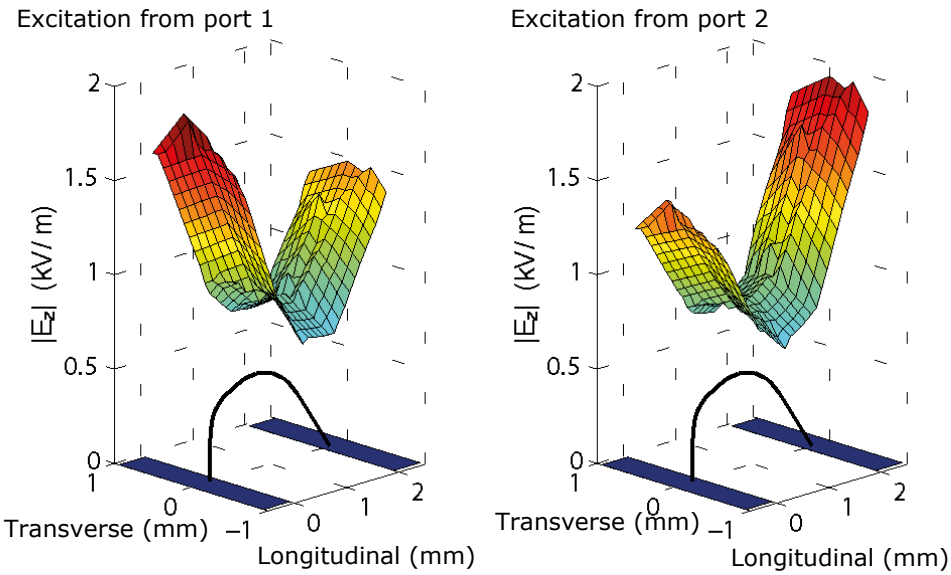

Figure 2.4: Forward problem solved by HFSS: the vertical E field 500 μm above the bondwire induced by the single bondwire under 1 Watt 3 GHz excitation from port 1 and 2.

in HFSS as a 2-port network (shown in Fig. 2.3). Solving for the S-parameters in (2.1), in this case a 2-by-2 complex matrix, is a standard procedure in HFSS whereas the solution for T-parameters in (2.2) requires further explanation. For each frequency of interest, we excite port 1 and 2 in sequence and solve for the corresponding electric field patterns. For instance, at 3 GHz, the induced electric field (vertical component) by the test segment 500 μm above the substrate is plotted in Fig. 2.4. Each E-field component in the figure (a complex quantity with a magnitude and a phase) corresponds to a T-parameter in (2.2).

Next, during the actual field measurement (Fig. 2.5), the VNA port 1 excites the test fixture at the left coaxial port, while the port the right is terminated by 4 different coaxial loads, namely, a match, a short, a short with 2dB and 3dB attenuators, to provide us with sufficient independent experimental data to verify our proposed procedure. For each loading condition and each frequency of interest, the vertical component of the induced E-field is sensed and fed back to the VNA by a semi-rigid coaxial probe (0.8 mm outer diameter, 1 mm center protrusion). The E-field probe is mounted on a 3-dimentional translation stage, which scans a 1-mm wide, 3-mm long horizontal area 0.5 mm above the bondwire in 0.1 mm steps. The S_{21} from the VNA as a relative measurement of vertical E-field strength is plotted in Fig. 2.6 for a specific loading condition at 3 GHz. Since the measured E-field is caused by a specific combination of incident wave excitations from the 2 ports, it must be a linear combination of the simulated field patterns in Fig. 2.4. The linear combination coefficients are

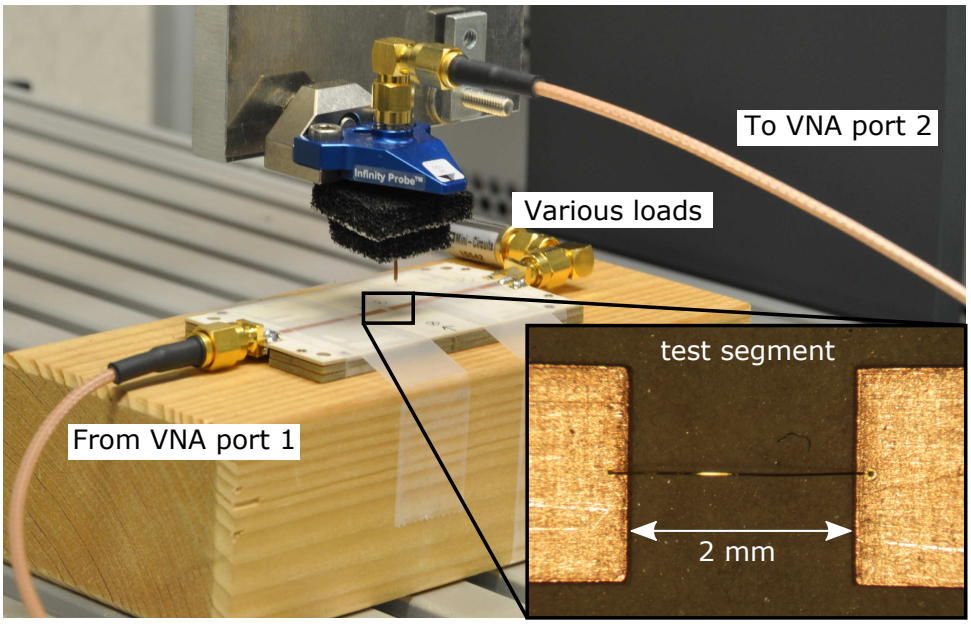

Figure 2.5: Single-bondwire test-fixture in the measurement setup. The test segment (inset) is a single bondwire bridgeing a 2-mm microstrip gap.

Table 2.1: Contactless measurement errors.

RMS errors at 2-4 GHz	short	short-2dB	short-3dB	match
complex error magnitude	0.162	0.043	0.038	0.048
magnitude error	0.050	0.033	0.029	0.035
phase error	9.1°	4.0°	9.4°	5.0°

the incident waves to be calculated in the next step.

The measured field at each of the 11x31 locations E_k (a complex quantity) is applied to (2.2), yielding in total 341 equations for 2 unknown incident voltages V_1^+ and V_2^+. This over-determined equation set is solved in the least-square sense. The result of which is then applied to (2.1) to solve for the scattered voltages V_1^- and V_2^-. Finally, reflection coefficients Γ_{insitu} at port 1 and 2 can be calculated from (2.3). The results of this deduction are plotted in Fig. 2.7 for port 1 and Fig. 2.8 for port 2.

As a comparison, reference data obtained using conventional measurement techniques are also shown in the figure. The conventional approach employs a direct short-open-load-thru (SOLT) calibrated VNA measurement at coaxial port A / B, followed by a thru-reflect-line (TRL) second-tier calibration to deembed/embed fixture-A / B and shift the reference plane to the virtual port 1 / 2 (Fig. 2.3).

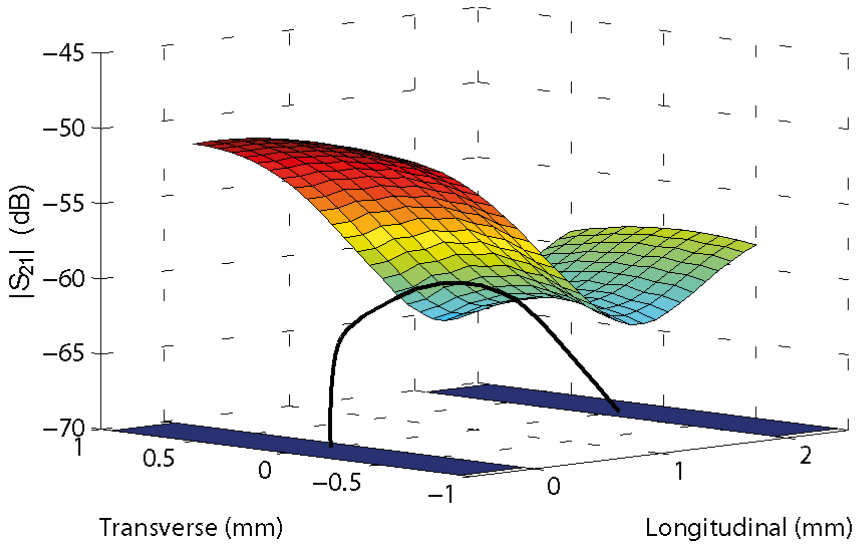

Figure 2.6: VNA measurement result: S_{21} magnitude at 3 GHz. The E-field probe scans a 1-mm wide, 3-mm long horizontal area 0.5 mm above the bondwire segment in 0.1 mm steps.

From Fig. 2.7, the applied coaxial loading conditions are not immediately clear due to the bondwire discontinuity. Most noticeably, in the case of a matched load, the reflection coefficient at bondwire terminal has a non-zero magnitude. Its phase is however flat over frequency, indicating a near-zero delay. It indicates the discontinuity immediately after port 1 (at the bondwire terminal) to be the major contributor for reflection. In the short+2/3 dB loading conditions, varying magnitude and group delay suggests that both the bondwire discontinuity and the coaxial loads contribute to the total reflection.

In the short coaxial loading condition, a clear discrepancy is observed near 2.7 GHz from Fig. 2.7. The field measurement yields a reflection coefficient magnitude larger than unity, which cannot be physically correct. This aggravated error occurs due to a large voltage standing wave ratio (VSWR) caused by the highly reflective coaxial load. At around 2.7 GHz, the 35 mm microstrip is half a wavelength long and a voltage standing wave dip falls right on top of the test segment. The E-field at this combination of frequency, location and loading condition is too weak to be measured reliably. Apart from this discrepancy, a general agreement between the contactless measurement and the TRL deembedded benchmark data can be observed. The root-mean-square errors for different loads are listed in Tab. 2.1.

Fig. 2.8 shows the reflection coefficients at the port 2 (load side, as shown in Fig. 2.3) of the test segment. At this port, 4 distinctive flat magnitude curves clearly indicate the 4 applied coaxial loading conditions. The 2 distinctive

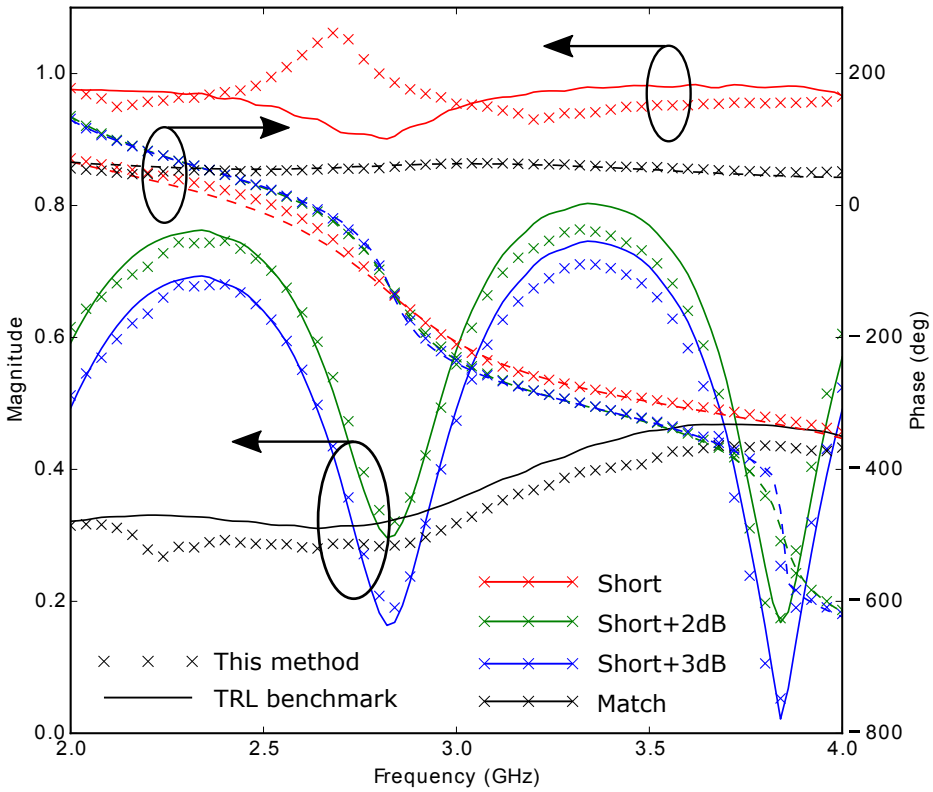

Figure 2.7: $|\Gamma|$ and $\angle\Gamma$, field measurement vs. TRL deembedded benchmark data, at virtual port 1, for 4 different coaxial loads, namely, match, short, short with 2dB and 3dB attenuators from 2 to 4 GHz.

phase slopes are due to the extra delay of the 2/3 dB attenuators. Again, a general agreement between the field measurement and TRL embedding is evident, except the voltage standing wave dip in the full-reflection case at 2.7 GHz.

2.4. Demonstration Above Multiple Bondwires

To demonstrate the high potential of the proposed method, we scan the vertical E field above a set of parallel bondwires and deduce the Γ_{insitu} at each bondwire terminal.

The test fixture is shown in Fig. 2.9, in which tapered lines on a 20-mil thick GML-1000 substrate ($\epsilon_r = 3.05$) extend the 50 Ω coaxial ports to two bondpads of 10 mm width and 1 mm length. A 2 mm gap between the bondpads is bridged by 33 gold bondwires in parallel, with 25 μm diameter, 3 mm horizontal length and 300 μm pitch. The bondwires with their pads are considered as the test segment, resembling the drain-lead connection in a large-periphery power

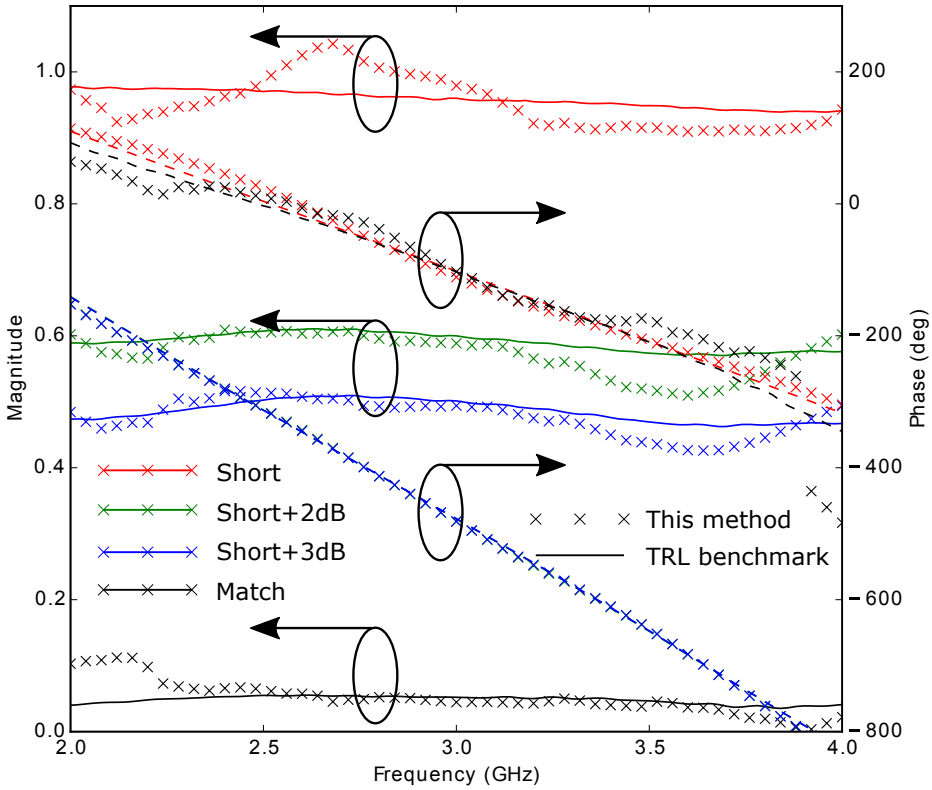

Figure 2.8: $|\Gamma|$ and $\angle\Gamma$, field measurement vs. TRL deembedded benchmark data, at virtual port 2, for 4 different coaxial loads, namely, match, short, short with 2dB and 3dB attenuators from 2 to 4 GHz.

device.

The test segment is modeled in HFSS as a 34 port network. 33 ports correspond to the 33 bondwire terminals at the source side, and the 34th port is at the load side bondpad. Each of the 34 ports is excited in turn by a 1 Watt power source while other ports are match-terminated. This procedure yields 34 field patterns comparable to Fig. 2.4. Each field pattern element is a T-parameter in (2.2).

During field scanning, the test fixture is driven by the RF source in the VNA at one coaxial port, and terminated by a 50 Ω load at the other port. The field probe scans in a 10 by 3 mm horizontal plane, 0.5 mm above the substrate. The measured vertical E-field is plotted in Fig. 2.10.

Using the previously described method, the Γ_{insitu} at each individual bondwire terminal can be obtained. For the ease of illustration, the results are converted to in-circuit load impedances, Z_{insitu}. The related magnitude and phase at each of the 33 bondwire terminals are plotted in Fig. 2.11.

In the figure, there are 5 curves representing the terminal impedances at

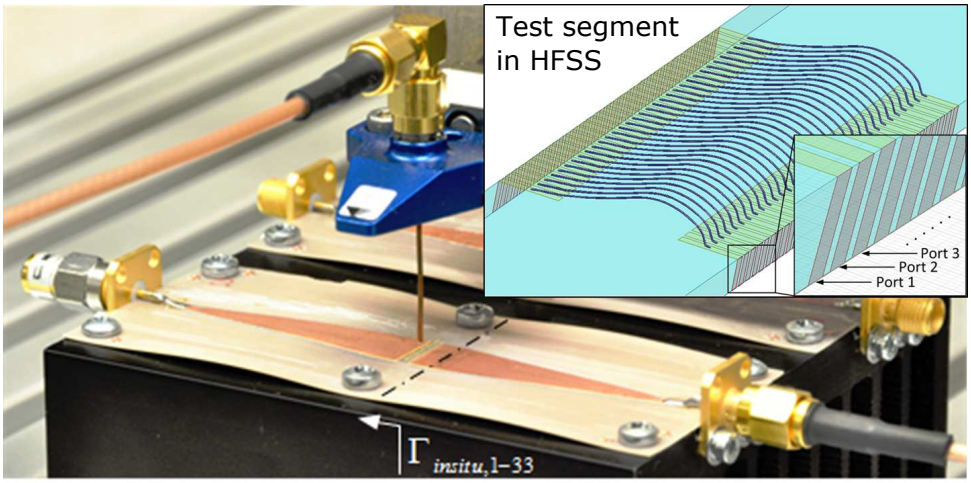

Figure 2.9: E-field measurement above the test fixture with 33 parallel bondwires.

1-5 GHz. The curves show that impedance magnitude increases with frequency while its phase is close to +90 degrees, indicating the expected inductive behavior. The impedance phase decreases slightly from +90 degrees at higher frequencies due to the gradually influential parasitic capacitance between the bondwires and ground plane. Furthermore, it can be observed from the figure that the impedance distribution is uneven across the bondwire array. Outer bondwires offer impedances that are lower than the inner ones. This phenomenon can be considered skin effect if we treat all bondwires as a single piece of metal; or proximity effect if we treat bondwires as separate metals. Fundamentally speaking, in either case, the magnetic coupling between bondwires causes the mutual inductances to be high for the inner wires and low for the outer wires.

Although the absolute accuracy of the data is still subject to field-probe calibration, the trend is clearly indicated. Were such a measurement to be performed above a similar test segment at the drain side of a large-periphery high-power device, a similar result would have indicated that not all transistor cells had been matched to their optimum loads. Moreover, such a measurement can pin-point problematic locations in detail and indicate the mismatch quantitatively, not only for the fundamental but also for the harmonic terminations, data of great value to the developers of power devices and subjects to be covered in following chapters.

2.5. Conclusion

A new contactless method is proposed to measure in-circuit reflection coefficients, Γ_{insitu}, while the circuit-under-test is in its normal operating condition.

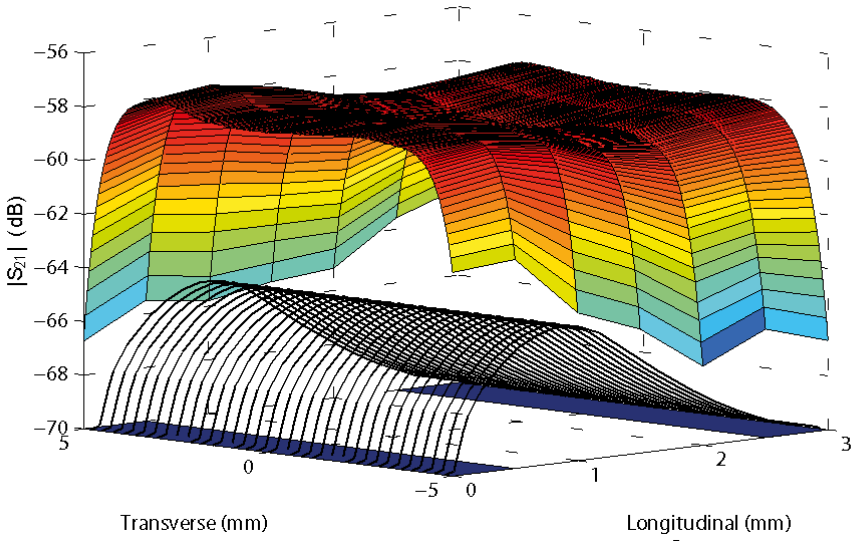

Figure 2.10: Measurement result: S_{21} magnitude from the VNA as a indication of relative strength of vertial E-field induced by the bondwire array under VNA excitation and a specific loading condition.

Relying on EM modeling and field probing, the method is capable to provide the Γ_{insitu} at bondwire terminals. The achieved results agree fairly with independent data obtained through conventional measurement techniques. Moreover, as a further demonstration of the proposed method, the Γ_{insitu} measurement of multiple parallel bondwires is shown.

> "The prospect of the proposed technique is far reaching, since future experiments will allow inspection of non-uniform fundamental (and harmonic) loading conditions in packaged high-power devices, as well as, the independent inspection of the time varying loading conditions as occurring in Doherty power amplifiers."[1]

In retrospect, when the original writing of this topic was drafted in 2011 and published in 2012, neither of the two envisioned applications was considered feasible. Yet they were attempted and successfully demonstrated, one after the other in the following years [6, 7], using variants of the proposed method. These endeavors are the subjects of the following chapters. Up to date, to the authors' best knowledge, these phenomena have never been visualized through conventional microwave measurement techniques.

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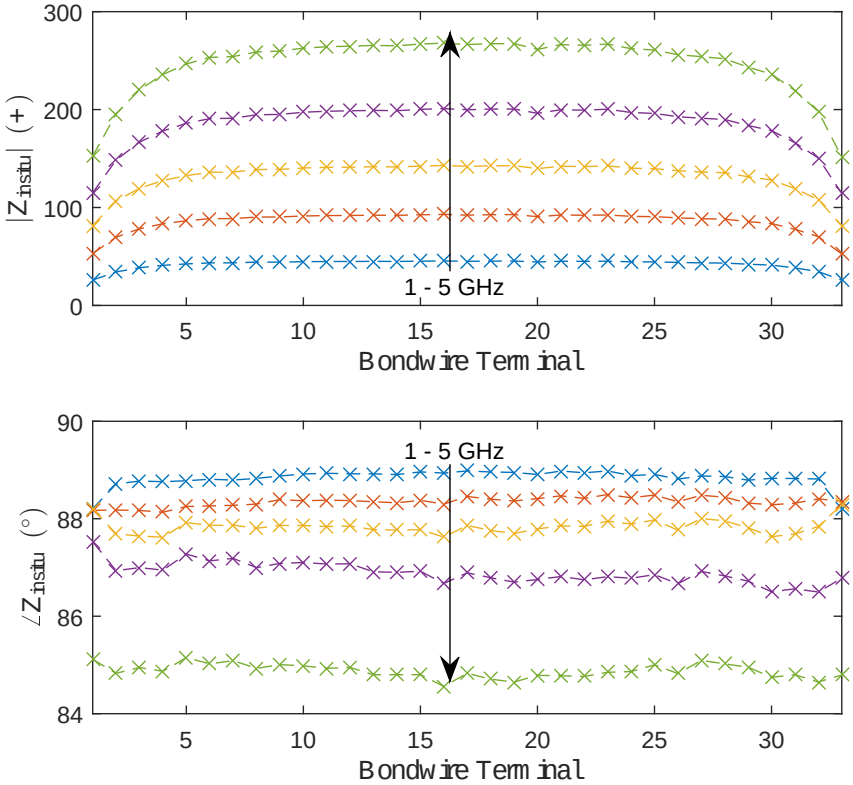

Figure 2.11: The magnitude and phase of in-circuit impedance, Z_{insitu} at frequency 1-5 GHz, looking into each of the 33 bondwire terminals.

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3

Non-intrusive Characterization of Active Device Interactions in High-efficiency Power Amplifiers

[1]In this chapter, the non-intrusive near-field technique of Chapter 2 is extended from ratio measurements, to the determination of absolute voltage and current magnitudes. This is done as follows, in addition to the use of the EM-based segment model that links the (probable) field information to the electrical quantities of interest, now a power calibration is performed on an externally accessible (output) connector. This extra step allows us (when output losses are low) to directly define the magnitude of the in-stitu voltages and currents.

The proposed technique has been applied in order to experimentally monitor the active device interactions in a 2.2-GHz 400-W LDMOS Doherty power amplifier (PA). Using this technique, the individual behaviors of interacting power devices in a high-efficiency PA, in terms of their inter-dependent drain voltages, currents, power, efficiency and loading impedance, have been experimentally quantified for the first time.

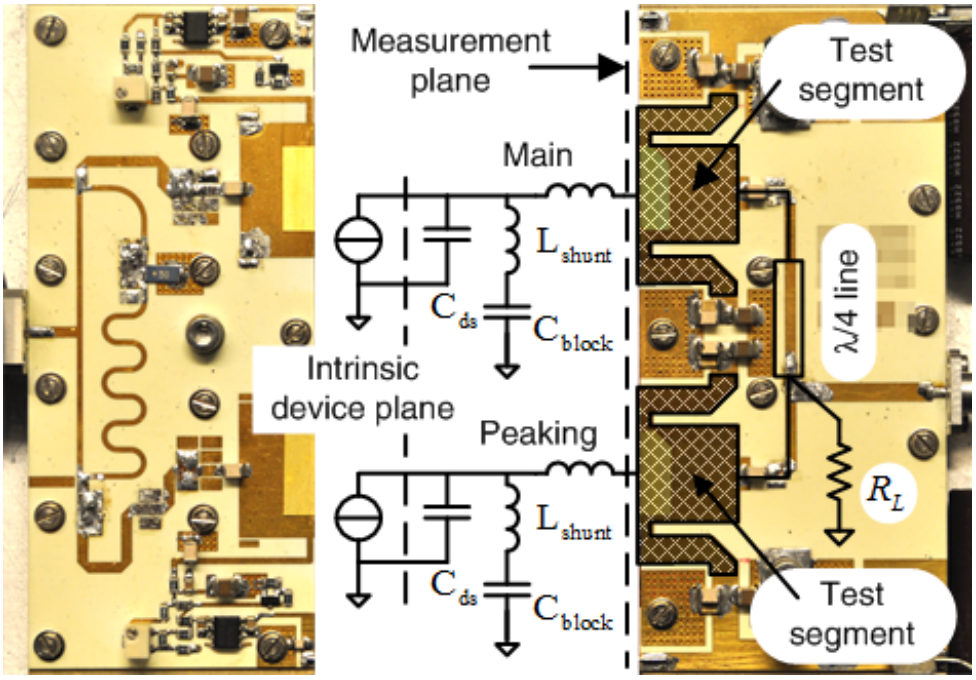


Figure 3.1: A 2.2-GHz 400-W LDMOS Doherty PA under test. It consists of two identical 200-W LDMOS devices, namely the main and peaking devices in Doherty terms.

3.1. Introduction

Modern RF power amplifiers, such as Doherty and outphasing PAs, enhance efficiency by means of active load modulation [2]. In such PAs (e.g. the Doherty PA in Fig. 3.1), multiple branch amplifiers modulate each other's loading impedance at different power levels. These varying loading conditions significantly change the behavior of the individual active devices and decisively affect the linearity, output power and efficiency of the PA. An experimental technique to accurately characterize such interaction of the physical devices, in terms of their inter-dependent output voltages and currents would provide detailed insight for PA design, troubleshooting and optimization.

Despite its importance, device interaction is a troublesome phenomenon to characterize. Conventional measurement techniques focus on the externally available parameters of the entire PA or individual non-interacting components, thus are unable to reveal the internal interactions between the active devices in a multi-branch PA. Insertion of voltage / current probes or directional couplers to measure internal amplifier conditions is a straightforward solution in most simulators, but is electrically and mechanically difficult, if not impossible

[1]Parts of this chapter have been published in Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International [1].

in practice.

New opportunities for PA measurement are promoted by recent advances in non-contacting near-field techniques [3–13]. Previous work has shown that the electric field induced by a microstrip can be accurately probed [3]. The probed field permits the deduction of S-parameters by the reconstruction of propagating waves [4]. The absolute power of the propagating waves on a microstrip is available through a non-contacting power calibration [8]. The relative power of propagating waves in irregular, multi-port and coupled interconnections is obtainable through a numerical electromagnetic solver [14].

This work applies a similar technique as in [14] to investigate the internal active-device interaction in the 2.2-GHz 400-W LDMOS Doherty PA shown in Fig. 3.1. The electric field induced by the drain-side interconnections is probed during a power sweep to reconstruct the in-circuit propagating waves. Instead of a power calibration as in [8], a low-loss power combiner in the PA is assumed and the PA output power is directly used to calibrate the absolute power waves. The interaction between the 2 LDMOS devices is characterized in terms of their inter-dependent voltages, currents, power, efficiency and loading impedance. Measurement results are de-embedded to the intrinsic device plane to facilitate a straightforward comparison to the theoretical Doherty PA behavior. To the authors' best knowledge, the in-circuit conditions of interacting devices are experimentally obtained and reported for the first time.

3.2. Doherty PA Description

The Doherty PA to be characterized for its internal devices interaction is shown in Fig. 3.1. The PA under test employs two identical 200-W laterally-defused metal-oxcide-semiconductor-field-effect-transistors (LDMOS). To interpret the internal Doherty conditions, each device output is considered as a current source with a shunt capacitance C_{ds}. The current source is connected through a shunt-L pre-matching network to the package lead. Outside the package, each drain lead is matched through a wide microstrip to the power combiner and biased through two symmetrical stubs. These planar interconnections are indicated in Fig. 3.1 as the test segments.

The details of the test segments are shown in Fig. 3.2. The power devices inject power into this test segment from the drive port. The power flowing to the load port is either delivered to the load or reflected by the load. The 2 side stubs serve both as DC biasing paths and as 2nd harmonic shorts (necessary for the Class-B operation). At the fundamental frequency, the biasing stubs have a length close to quarter-wavelength, effectively transforming the RF short-circuit terminations from the bias ports (see Fig. 3.2) to open-circuit conditions in the intrinsic current-generator plane (see Fig. 3.1).

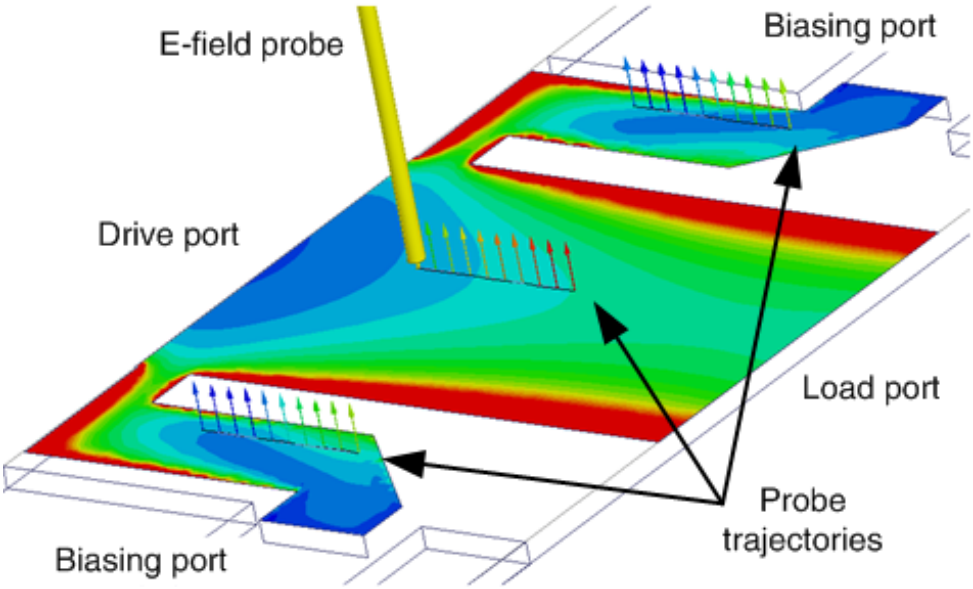


Figure 3.2: A section of the output matching network modeled in HFSS as the test segment. Simulation yields the vertical component of electric field 500 μm above the planar structure.

3.3. Characterization Procedure

3.3.1. Physical near-field measurement

The physical E-field measurement is performed in the setup shown in Fig. 3.3. The field probe is made of a 500-μm diameter semi-rigid coaxial cable with 300-μm center conductor protrusion. The probe is mounted on a 3D translation stage to scan the E-field 500 μm above the planar structure in 1-mm steps along 3 trajectories indicated in Fig. 3.2.

The Doherty PA underneath the probe is driven by a 2.14 GHz RF signal. This RF signal is modulated by 10-μs width, 1% duty-cycle pulses to avoid excessive power dissipation and self-heating effects. The transfer from the PA input to the field probe is measured by a vector network analyzer. This transfer is used as a relative measure of the E-field magnitude and phase.

3.3.2. Numerical deduction of incident and scattered waves

In order to deduce port conditions from the measured E-field, their transfer relationship need to be calculated. This step is performed in an electromagnetic field simulator, ANSYS HFSS. The 4-port test segment together with the coaxial field probe is modeled in HFSS, as shown in 3.2.

Inside the EM-field simulator, each of the 4 ports of the test segment is excited individually, yielding 4 respective field distributions, as shown in Fig 3.4

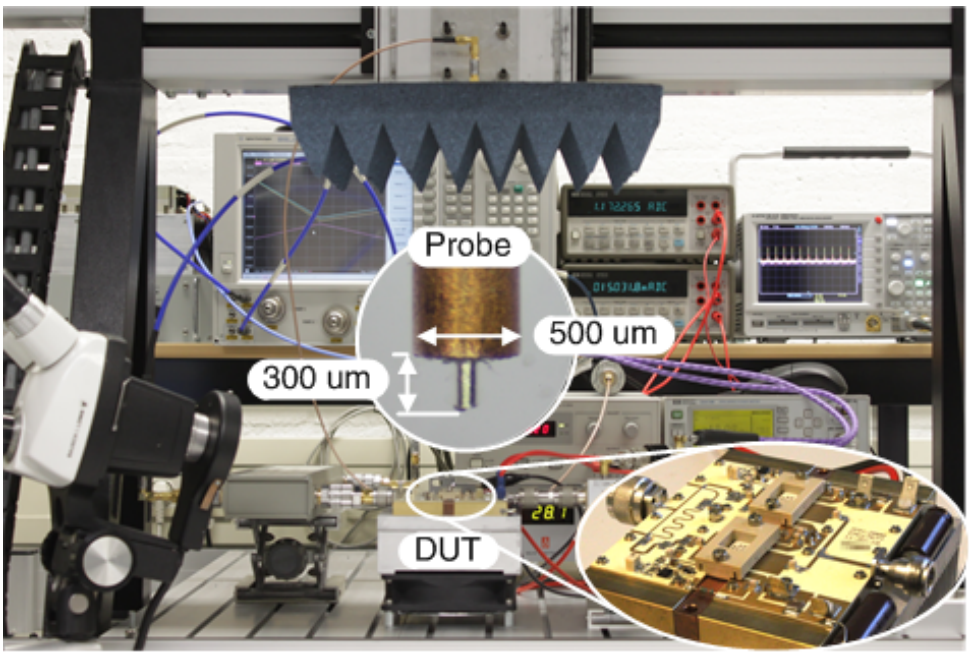


Figure 3.3: Field measurement setup.

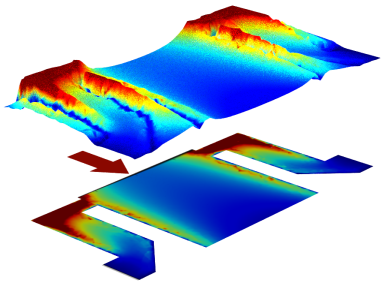
(a) - (d). In a physical measurement of an operating PA, power flows into the test segment through all 4 ports simultaneously. Therefore the physically measured E-field (Fig. 3.4 (e) must be a linear combination of the 4 simulated field distributions. The combination coefficients disclose the ratio of the actual port excitations in the operating PA.

Based on the physically measured E-field and the 4 previously obtained HFSS-simulated field distributions, the relative power waves at each port going in and out of the test segment are deduced, by the method shown in [14].

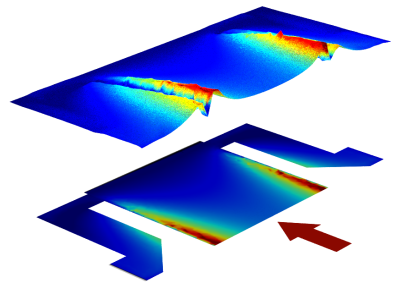
3.3.3. Deduction of port voltages and currents

Up to this stage, relative voltages and currents are readily available at the drive ports. Obtaining them as absolute quantities requires a power calibration. For this purpose, a power calibration is first performed at the output coaxial connector of the Doherty PA using a conventional power meter, then by assuming low-loss in the power combiner, the absolute power waves at the drive ports of the test segments are determined.

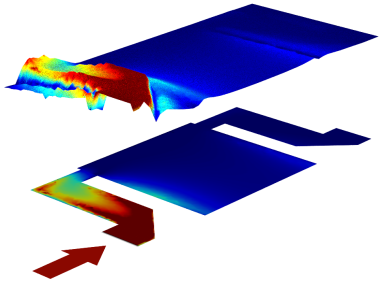
To facilitate a clear comparison of the measurement data to the well-known Doherty PA theory [2], an additional de-embedding of the package model is performed to transform the traveling waves from the measurement plane to the intrinsic device plane, as indicated in Fig. 3.1.



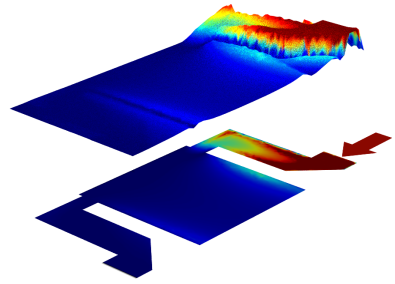
(a) Modal E-field from port 1 excitation.



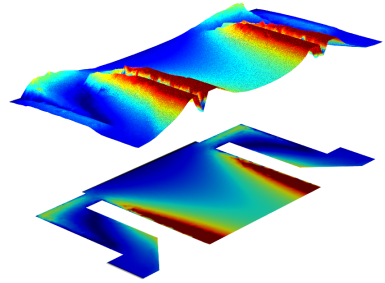
(b) Modal E-field from port 2 excitation.



(c) Modal E-field from port 3 excitation.



(d) Modal E-field from port 4 excitation.



(e) Total E-field above the output matching network.

Figure 3.4: HFSS simulation result: E-field superposition. The measured vertical E-field 500 μm above the planar output matching network in (e) is a superposition of 4 HFSS computed modal fields given in (a) - (d) that follow from single-port excitations.

3.4. Measurement Results

To fully demonstrate the high practical value of this characterization technique, the Doherty PA is measured under an optimal and an improper biasing conditions. In the improper biasing case, the gate of the peaking device is biased at a higher voltage (1227 mV instead of the optimal 452 mV), effectively detuning the peaking PA branch from Class-C to Class-AB. As shown in Fig. 3.5, this detuning degrades the drain efficiency. But the underlying cause is not

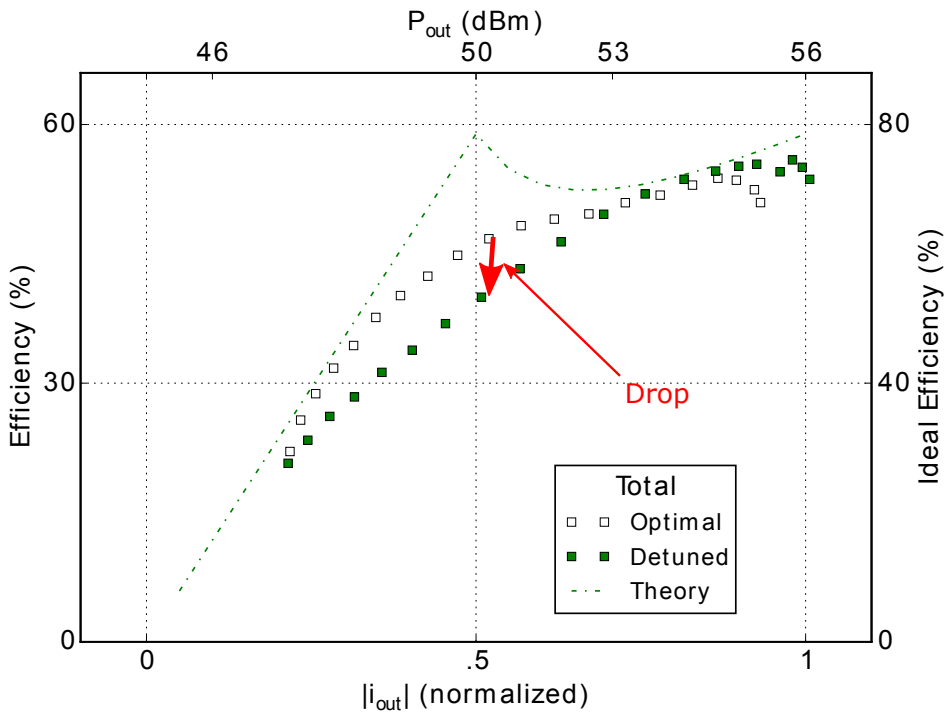


Figure 3.5: Troubleshooting demonstration: drain efficiency for the Doherty PA with normal and detuned bias conditions for the peaking-branch device is compared to the ideal theoretical behavior. The efficiency degradation is evident but the underlying cause is unclear.

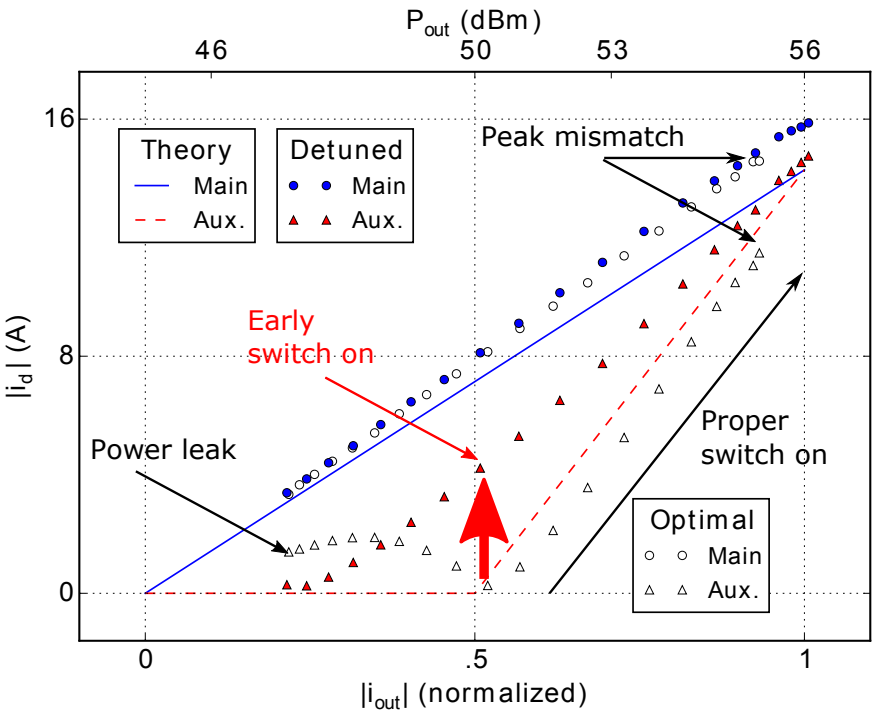


Figure 3.6: Drain currents for the main and peaking devices. Measurements of the Doherty PA with normal and detuned bias conditions for the peaking-branch device are compared to the ideal theoretical behavior.

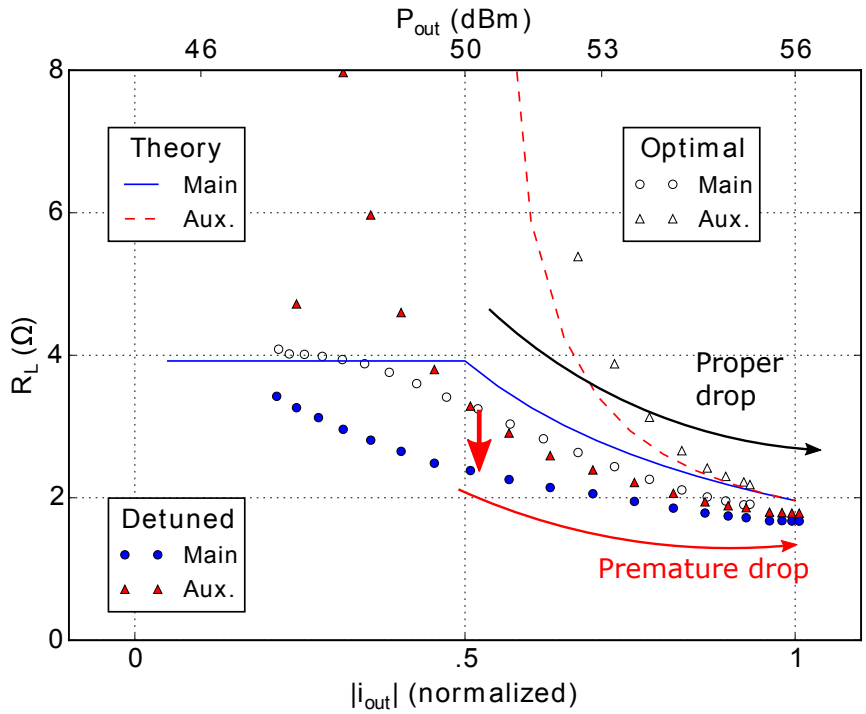


Figure 3.7: Load resistances seen by the main- and peaking-branch devices. Measurements of the Doherty PA with normal and detuned bias conditions for the peaking-branch device are compared to the ideal theoretical behavior.

observable from this overall performance. In the following section , we apply the proposed method to look into the in-circuit voltages and currents for the PA in both operating conditions, to study the internal active device interaction.

Since alternative experimental techniques are unavailable to obtain this kind of in-situ measurement data, the measurement results are directly compared to the ideal "textbook like" Doherty behavior. For this ideal Doherty we assume that its active devices behave as linear current sources operating in Class-B, with a clipping voltage of 28 V and maximum output power of 200 W to allow a straightforward comparison with our measurement data.

The drain currents vs. normalized input voltage for the main and peaking devices are plotted in Fig. 3.6. For an ideal symmetrical Doherty PA in a power sweep, the main current grows proportionally over the entire power range whereas the peaking current is zero in the low half-range and grows twice as fast in the high-half range. At peak input power, both devices deliver equal output power. In reality, even optimally tuned PAs have practical artifacts, as shown in Fig. 3.6. For example, at deep power back-off, well below 6 dB, output current leaks through the peaking device due to its finite output

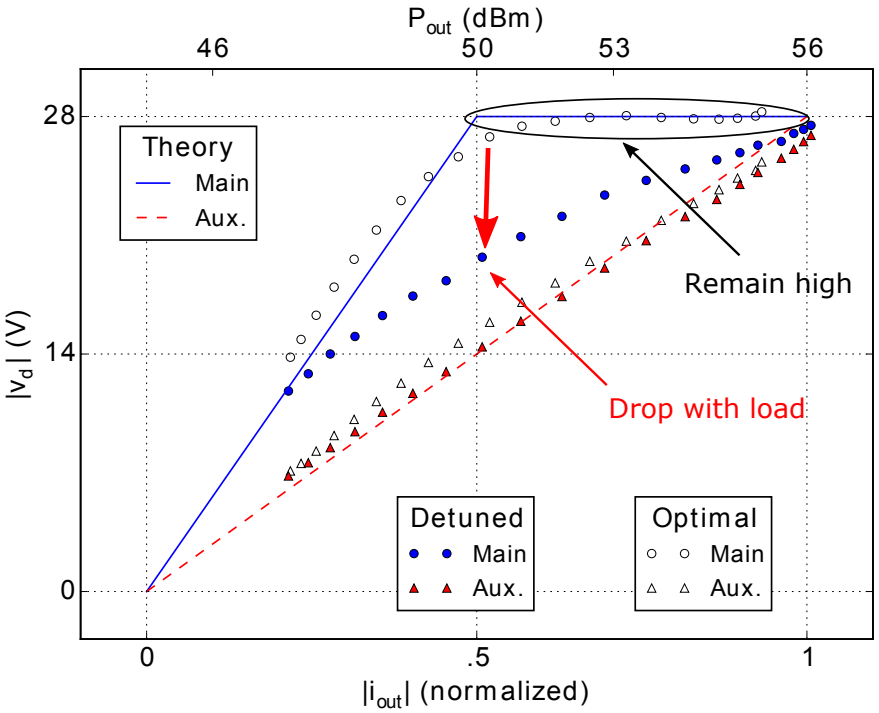


Figure 3.8: Drain voltages for the main- and peaking-branch devices. Measurements of the Doherty PA with normal and detuned bias conditions for the peaking-branch device are compared to the ideal theoretical behavior.

conductance. Furthermore, at peak output power, the peaking device fails to fully match current to the main device because of its Class-C operation. In the detuned case, the higher gate bias causes the peaking device to switch on earlier than it should. The peaking current deviates away from its theoretical reference. The consequence of this early switch-on will be further analyzed.

The purpose for the peaking device to switch on above 6 dB back-off is to modulate the loading condition of the main-branch device. As shown in Fig. 3.7, the load resistances for the main- and peaking-branch devices vary with input power. Ideally, the main device sees a passive load in the low power region. After the peaking device switches on, it reduces the apparent load resistance of the main-branch device. At peak output power, the main resistance is halved. It can be observed from Fig. 3.7 that this ideal behavior is reasonably well followed by the optimally tuned Doherty PA. But in the detuned case, due to the early peaking device switch on, the load-pulling effect happens too early, resulting a premature main resistance drop. The consequence of this early load-pulling will be further analyzed.

The purpose for the peaking device to load-pull the main is to maintain the

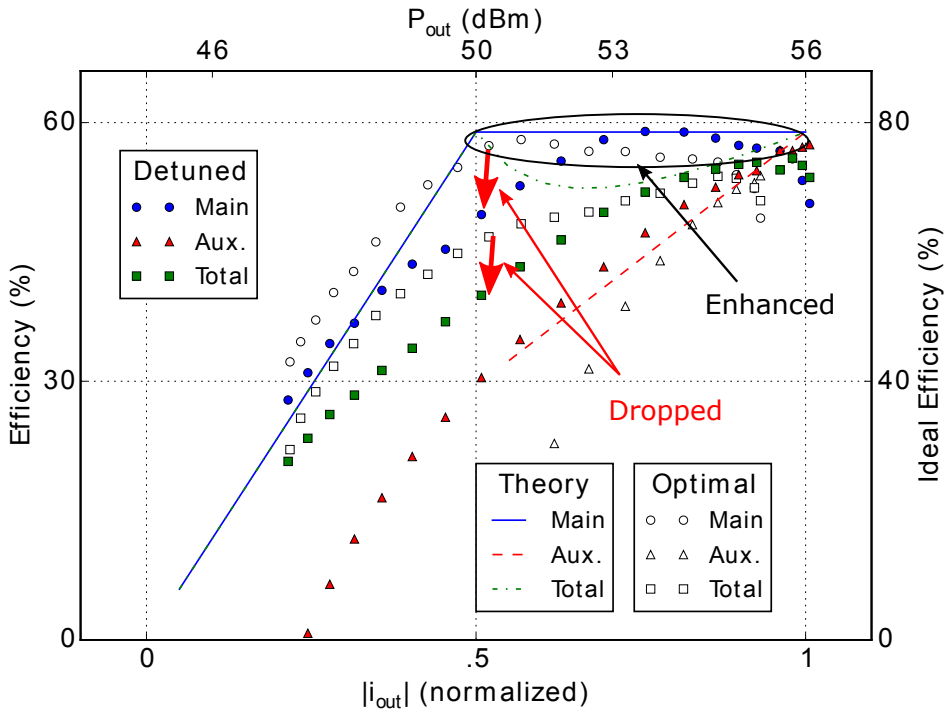


Figure 3.9: Drain efficiency for the main- and peaking-branch devices. Measurement of the Doherty PA with normal and detuned bias conditions for the peaking-branch device are compared to the ideal theoretical behavior.

drain voltage of the main device at its maximum voltage swing. As shown in Fig. 3.8, in the ideal case, the peaking device pulls down the main load resistance to counteract the increasing main current. The net effect is that the main voltage reaches its top level in the 6 dB back-off point and is maintained there. It can be observed from Fig. 3.8 that the optimally tuned PA follows the ideal Doherty behavior fairly well. But in the detuned case, due to the premature load-pulling downwards, drain voltage of the main device fails to reach its peak at 6-dB back-off point. The consequence of this drain voltage drop will be further analyzed.

The purpose to maintain a high drain voltage is to obtain a high efficiency. As shown in Fig. 3.9, in the ideal case, since the main voltage reaches its top level in the 6 dB back-off point, the main efficiency also reaches its top. This results the pronounced Doherty efficiency peak at the back-off point. It can be observed from Fig. 3.8 that the efficiency of the main device in the optimally tuned case indeed follows the ideal Doherty behavior. But in the detuned case, since the main voltage fails to peak at the back-off point, the main efficiency suffers as well. The aggregated results finally lead us to the total efficiency degradation as first observed from Fig. 3.5.

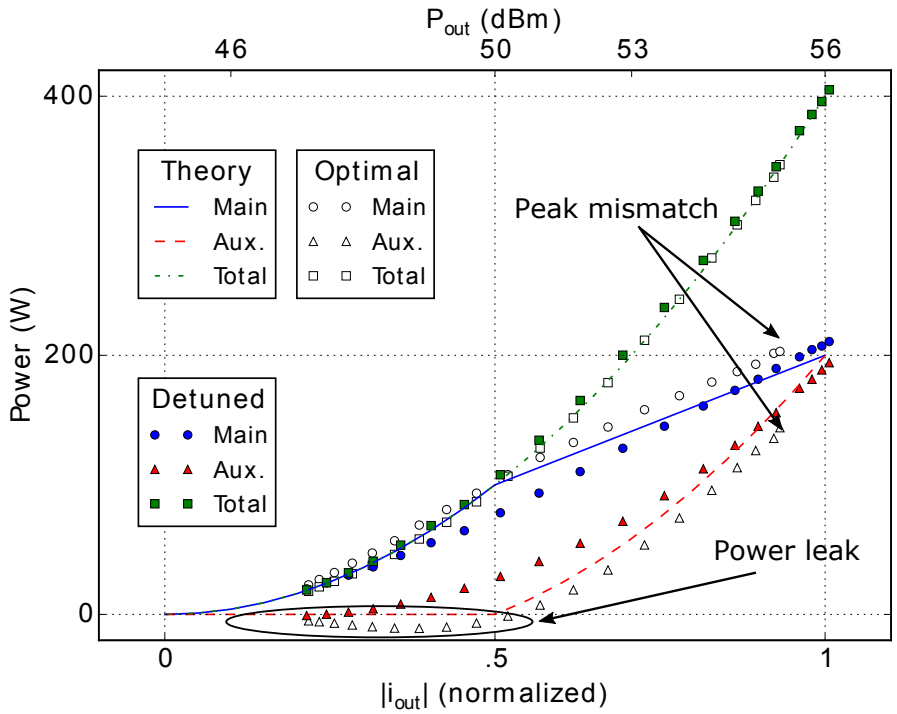


Figure 3.10: Output power for the main- and peaking-branch devices. Measurements of the Doherty PA with normal and detuned bias conditions for the peaking-branch device are compared to the ideal theoretical behavior.

For completeness, the output power from the main, peaking devices and the entire PA, is plotted in Fig. 3.10. A comparison of theory and reality again shows practical artefacts such as power leakage in the peaking device in low power levels due to finite off-state impedance and peak power mismatch due to Class C vs. AB operation.

As has been demonstrated in the analysis process, since the proposed near-field characterization method unveils internal circuit conditions without affecting the DUT under its normal operation, it enables us to inspect physical circuits in great details and experimentally quantify active-device interactions in a Doherty PA which have, before the publication of this work, only been seen in circuit simulators.

3.5. Conclusion

A non-intrusive near-field technique has been applied to obtain the in-situ circuit conditions of a 2.2-GHz 400-W Doherty PA. By measuring the local electric field induced by a known test segment, the traveling waves at the boundaries of

this test segment can be reconstructed. This technique enables the individual characterization of the interacting devices in a fully operational PA in terms of loading conditions, output voltage, current, power and efficiency at their intrinsic device planes. These experimentally obtained in-circuit conditions have been compared with the theoretical Doherty behavior, showing good agreement. A further characterization of deteriorating device interaction in a detuned Doherty PA demonstrates the high practical value of this technique for PA design, troubleshooting and optimization. According to the best knowledge of the authors, the interaction of active devices in a PA is experimentally characterized for the first time.

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4

Contactless Measurement of Absolute Voltage Waveforms by a Passive Electric-field Probe

[1]This chapter proposes an improved technique for accurate, contactless measurement of the absolute voltage waveforms of microwave circuits, employing a passive electric-field sensing probe. The proposed technique uses an electromagnetic model of the interaction between the probe and a device under test, to allow the extraction of the coupling capacitance variation versus frequency. Employing this information the measurement accuracy is improved, especially for higher (i.e., harmonic) frequencies, yielding enhanced waveform fidelity. The proposed method is validated on a microstrip line carrying waveforms with rich harmonic content. The accuracy of the proposed technique is benchmarked against a conventional thru-reflect-line (TRL) de-embedding approach by a nonlinear vector network analyzer (NVNA). Measurement results show that the root-mean square (RMS) error can be improved by 3 percentage points (from 8% to 5%) compared to the prior arts over the frequency range from 1 to 5 GHz.

4.1. Introduction

The accurate knowledge of in-situ voltage waveforms, is desirable for both troubleshooting and optimization of microwave circuits. Conventional microwave

[1]Parts of this chapter have been accepted for publication in the IEEE Microwave and Wireless Components Letters.

measurements can only access in-circuit voltages through well-defined terminals (i.e. connectors or probe landing pads) by means of de-embedding. If the circuit section between the accessible ports and the desired measurement location is not characterized, i.e., through break-out sections or second-tier calibration, conventional de-embedding techniques cannot be applied.

Over the years, various passive contactless techniques have been introduced to perform in-situ contactless measurements [1–14]. Using an electric-field probe, contactless techniques can provide, non-intrusively, voltage information at locations that are otherwise inaccessible [15–21]. However, absolute voltage measurements without galvanic contact are difficult in general, since the E-field probe operation strongly depends on the capacitive coupling between its tip and the device under test (DUT), which is set by the probe location. Furthermore, this coupling varies considerably with the local geometries of the DUTs and thus can only be calibrated in-situ.

Recently, an in-situ calibration technique was proposed in [21], which makes use of a low-frequency (e.g. 1 MHz) transfer measurement to characterize the in-situ coupling capacitances between the DUT and the active probe. Consequently, it effectively accounts for both the locational sensitivity and DUT dependency. However, [21] cannot account for frequency dependence of the DUT-probe coupling capacitance, causing increased inaccuracies for harmonic amplitudes at higher frequencies, which manifest themselves in time domain as waveform distortion.

In this contribution, in-situ waveform calibration is experimentally benchmarked against conventional TRL de-embedding techniques for the first time. In addition, numerical electromagnetic (EM) analysis is used to quantify and include the frequency dependent coupling capacitance between the E-field probe and a microstrip line segment (or any other DUT geometry). This computed frequency-varying capacitance is used to correct the low-frequency calibration method of [21] to further improve its accuracy at higher frequencies. As such, a non-intrusive measurement of in-circuit absolute voltage waveforms with high accuracy is proposed. The method is experimentally validated by contactless measurement of voltage waveforms with rich harmonic content from 1 to 5 GHz at a specific in-circuit location. The accuracy of the proposed technique is benchmarked against NVNA measurements employing conventional single-line (quarter wavelength at 3 GHz) TRL de-embedding.

The E-field probe measurement principle including frequency dependent capacitive coupling, is given in Section 4.2. Numerical EM analysis of probe-DUT coupling and the capacitance extraction procedure are detailed in Section 4.3. Measurement validation of the proposed approach is given in Section 4.4.

4.2. Principle of E-field Probe Measurement

To simplify the derivations, without loss of generality, this work considers the coupling of the E-field probe to a section of microstrip transmission line (Fig.

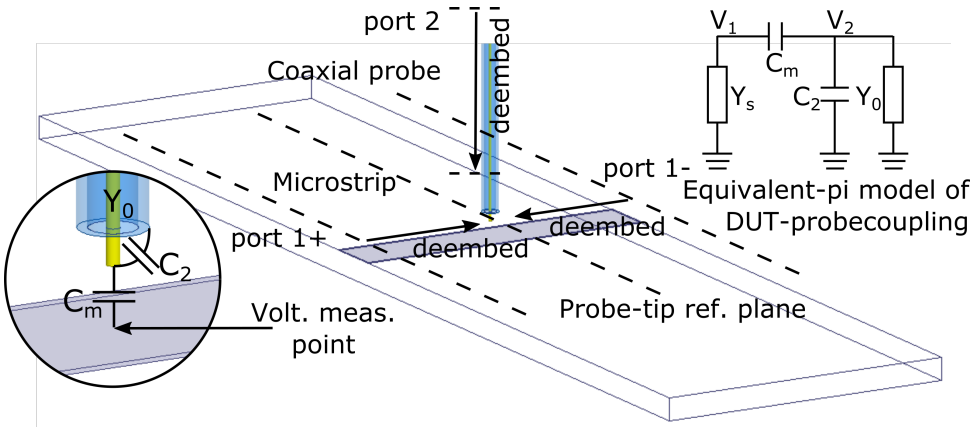


Figure 4.1: Capacitive coupling between an electric-field probe and a microstrip line is modeled in HFSS. Inset (lower left): electrostatic model of the probe-tip-to-DUT coupling. Inset (upper right): equivalent-pi circuit model of DUT-probe coupling.

4.1). The microstrip line has a dominant quasi-TEM propagation mode with fixed source and load terminations yielding a uniquely defined voltage at any specific location along the line. The microstrip segment of interest at such a location (Fig. 4.1), which satisfies the lumped assumption and bears a uniquely defined voltage, is considered as the DUT. The energized DUT induces an electric field, which can be sensed by the E-field probe without galvanic contact. The probe is made from an open-ended coaxial cable with center conductor protrusion. The probe tip, DUT and their distance are all considered to be electrically small compared to the wavelength at the frequency of interest. Under these assumptions, the DUT-probe coupling is predominantly capacitive. Therefore, the voltage transfer from the DUT to the "differential" probe output (i.e. the difference between the inner- and outer-conductor of the probe, referred to the microstrip ground) can be expressed by the lumped coupling capacitances as

$$\frac{V_2}{V_1} = \frac{j\omega C_m}{j\omega C_m + j\omega C_2 + Y_0}, \tag{4.1}$$

where V_1, V_2, C_2, C_m and Y_0 are the DUT voltage, probe output voltage, probe-tip fringe capacitance, DUT-probe mutual capacitance, and the characteristic admittance of the coaxial probe, respectively. For an active E-field probe [18–21], Y_0 can be neglected due to the high input impedance of a buffer amplifier located directly at the probe, simplifying (4.1) to,

$$\frac{V_2}{V_1} = \frac{C_m}{C_m + C_2}, \tag{4.2}$$

where C_2 is dominated by the input capacitance of the voltage amplifier. For a passive probe [15–17], the C_m and C_2 of a few fF at GHz frequencies are

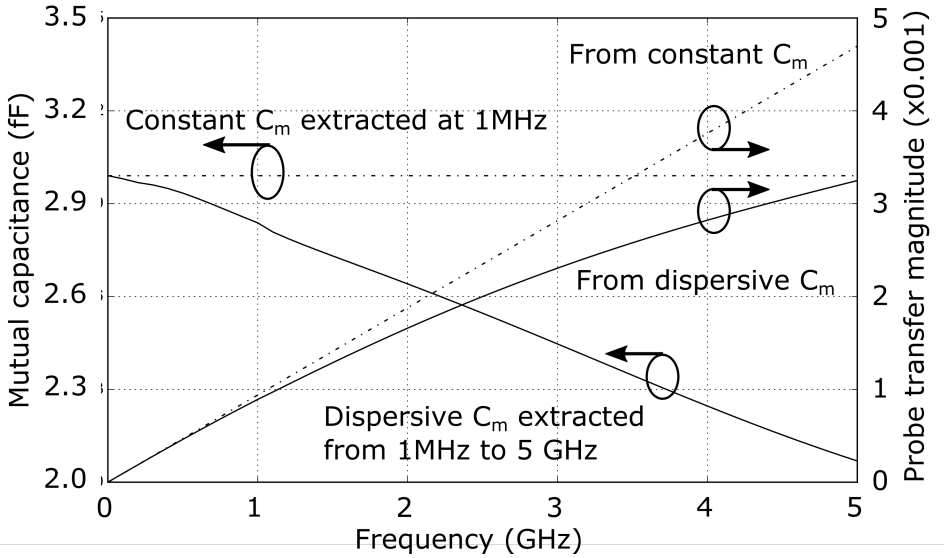


Figure 4.2: Mutual capacitance C_m and DUT-probe voltage transfer magnitude vs. frequency extracted from HFSS. The C_m extracted at 1 MHz (assuming constant) differs significantly from those extracted from an EM model at each frequencies from 1 MHz to 5 GHz (dispersive in frequency).

negligible to Y_0, simplifying (4.1) to,

$$\frac{V_2}{V_1} = \frac{j\omega C_m}{Y_0}. \tag{4.3}$$

If the frequency dependency of the capacitances is neglected, the voltage transfers in either (4.2) or (4.3) can be characterized by a low frequency signal and extrapolated to higher frequencies as proposed in [21]. However, in reality, the DUT-probe coupling capacitance C_m decrease at high frequencies, because increased metal reactance effectively divides lumped capacitances into distributed ones. This effect can be quantified and visualized by using full-wave EM analysis.

4.3. Numerical EM Analysis of Probe-DUT Coupling

The probe-microstrip coupling is modeled in an EM simulator, Ansys HFSS (Fig. 4.1). In this figure, a 50 Ω microstrip line is constructed from a 10-mm-long, 1.88-mm-wide, 35-um-thick copper trace on a 0.76-mm-thick Rogers 3003 substrate (ϵ_r=3). The electric probe is made from a 50-mm-long, 0.5-mm-diameter semi-rigid coaxial cable with 300 μm center conductor protrusion. The probe tip is positioned 500 μm above the metal surface. The choice of such a probe

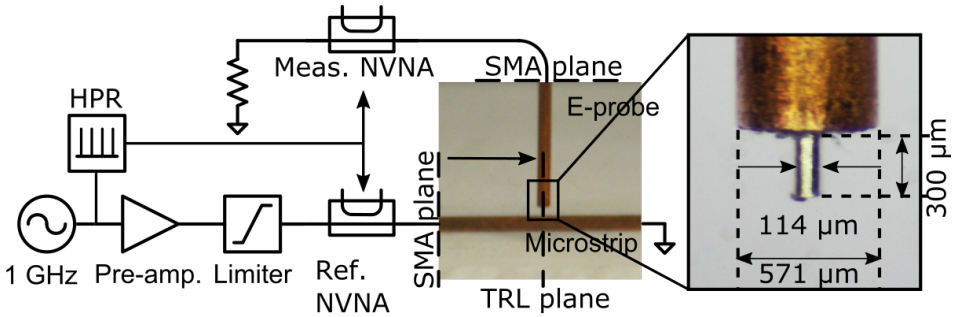


Figure 4.3: Contactless voltage waveform measurement setup. Inset: E-field probe dimensions.

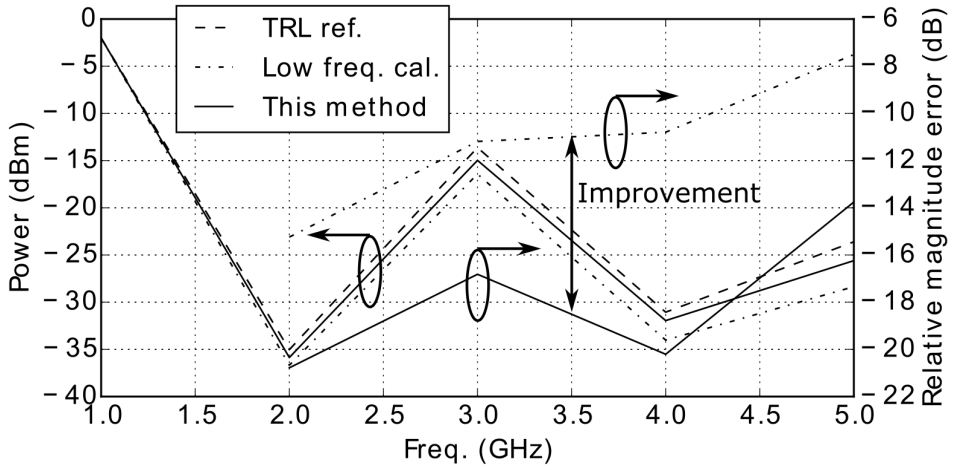
to DUT distance is often a trade-off among signal-to-noise ratio (SNR), spatial resolution and intrusiveness. For a more quantitative analysis, the coupling capacitances in (4.1) are extracted from the 3-port s-parameter of the model in Fig. 4.1. First, the coaxial cable (probe) and the left/right microstrip sections (to the probe ref. plane of Fig. 4.1) are de-embedded. The 3-port de-embedded s-parameters are then reduced to a 2-port model by considering only the common mode of the 2 microstrip ports. After that, an S- to Y-parameter conversion yields the capacitances of the equivalent-pi model in Fig. 4.1 (lower-left and upper right insets).

The probe-DUT coupling capacitance, C_m, extracted at low (1 MHz) and high (1-5 GHz) frequencies are plotted in Fig. 4.2, highlighting the evident frequency dependence of the coupling capacitance. The inaccuracy from a low-frequency extraction, still small at 1 GHz, rapidly increases with frequency. Once quantified, this knowledge can be leveraged to improve the accuracy of waveform measurements.

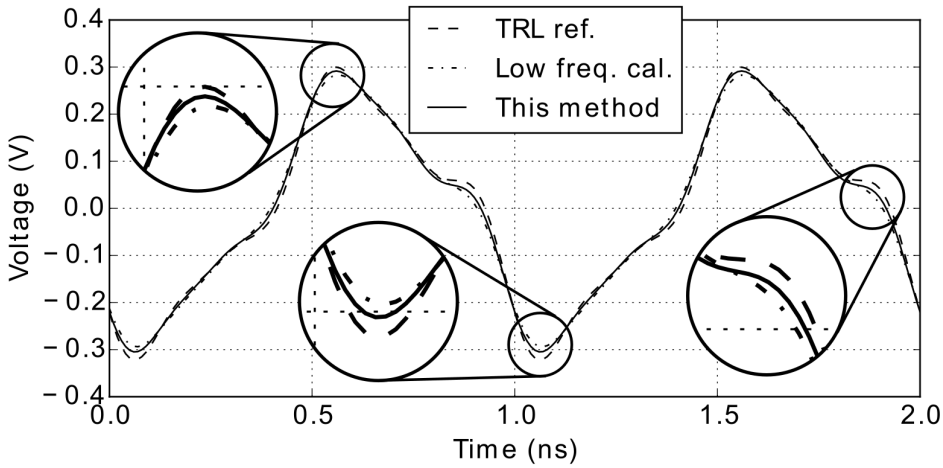
4.4. Measurement Results

To validate the proposed method for the accurate measurement of absolute voltage waveforms in-situ at RF frequencies, we use the measurement setup as shown in Fig. 4.3. The driving 1 GHz sinusoidal signal is pre-amplified and passed through a power limiter (Mini-circuits VLM-73-1W-S+) to create a waveform with rich harmonic content. The distorted signal propagates through the 50 ohm microstrip line and is reflected by a short termination. These two directional waves interfere, yielding different voltage waveforms along the microstrip line. The EM-modeled E-field probe is positioned at a fixed position by a 3D translation stage 500 μm above the center of the microstrip line. Its horizontal position along the line is defined at a TRL calibrated reference plane.

The output voltage from the E-field probe is measured by a non-linear vector network analyzer (NVNA) with a harmonic phase reference (HPR). The NVNA is first calibrated at the SMA connector planes (in Fig. 4.3) for s-parameters,



(a)



(b)

Figure 4.4: Measurement validation in frequency domain (a) and time domain (b): Contactless measurements with low-frequency calibration and further EM-model assisted correction are compared with the reference signal from a conventional connectorized NVNA measurement + TRL de-embedding.

absolute power and absolute (harmonic) phase from 1 to 5 GHz. Then, an in-situ calibration [21] is performed for the measurement NVNA at 1 GHz (instead of 1 MHz for better SNR from the HPR), whereas the reference NVNA performs a conventional waveform measurement at the TRL plane (in Fig. 4.3), using TRL de-embedding. TRL provides an independent reference and accuracy benchmark due to the better reproducibility as a conductive measurement. The capacitive loading effect of the E-field probe (a few fF) to the 50 Ω microstrip line is neglected at GHz frequencies.

Results from both the contactless and the conventional measurement are plotted in Fig. 4.4 (a) and (b) in frequency- and time-domain, respectively. Clear agreement between the contactless techniques and the reference measurement can be observed. As such, the in-situ calibration method [21] is experimentally validated. Furthermore, Fig. 4.4 (a) shows that the in-situ calibration at 1 GHz yields increasing magnitude errors at higher frequencies. These errors are reduced by the improved technique introduced in this work, i.e. to use the frequency dependent capacitance extracted from the EM model to correct the relative voltage transfers, as shown in Fig. 4.2. The corrected waveform is zoomed in in Fig. 4.4 (b), where the accuracy improvement is evident. A more quantitative analysis of the waveform accuracy in Fig. 4.4 (b) indicates that the root-mean-square (RMS) error of a low-frequency calibration is improved by about 3 percentage points (from 8.53% to 5.36%) by accounting for the probe-DUT coupling dispersion, as proposed in this work. To the authors' best knowledge, calibrated contactless measurement of absolute voltage waveforms has been experimentally validated at GHz frequencies for the first time.

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5

Non-intrusive Near-field Characterization of Distributed Effects in Large-periphery LDMOS RF Power Transistors

[1]This chapter demonstrates the EM-model-assisted non-intrusive near-field technique applied to 100 W and 200 W 0.1-μm gate-length LDMOS transistors with in-package matching networks. The absolute voltages and currents are found by making use of the additional power calibration step described in Chapter 3. Using this technique the voltage and current magnitudes of the individual drain bondwire terminals in operating LDMOS devices were experimentally quantified for the first time.

5.1. Introduction

Modern base-station transmitters are predominantly powered by laterally-diffused-metal-oxide-semiconductor (LDMOS) transistors. As shown in Fig. 5.1, an LDMOS device is made of identical transistor cells connected in parallel. Power capacity scales up by increasing the number of cells, yielding large peripheries. When the physical/electrical size becomes a significant portion of a wavelength, identical cells no longer operate under equal conditions. Distributed effects,

[1]Parts of this chapter have been published in Microwave Symposium Digest (IMS), 2015 IEEE MTT-S International [1].

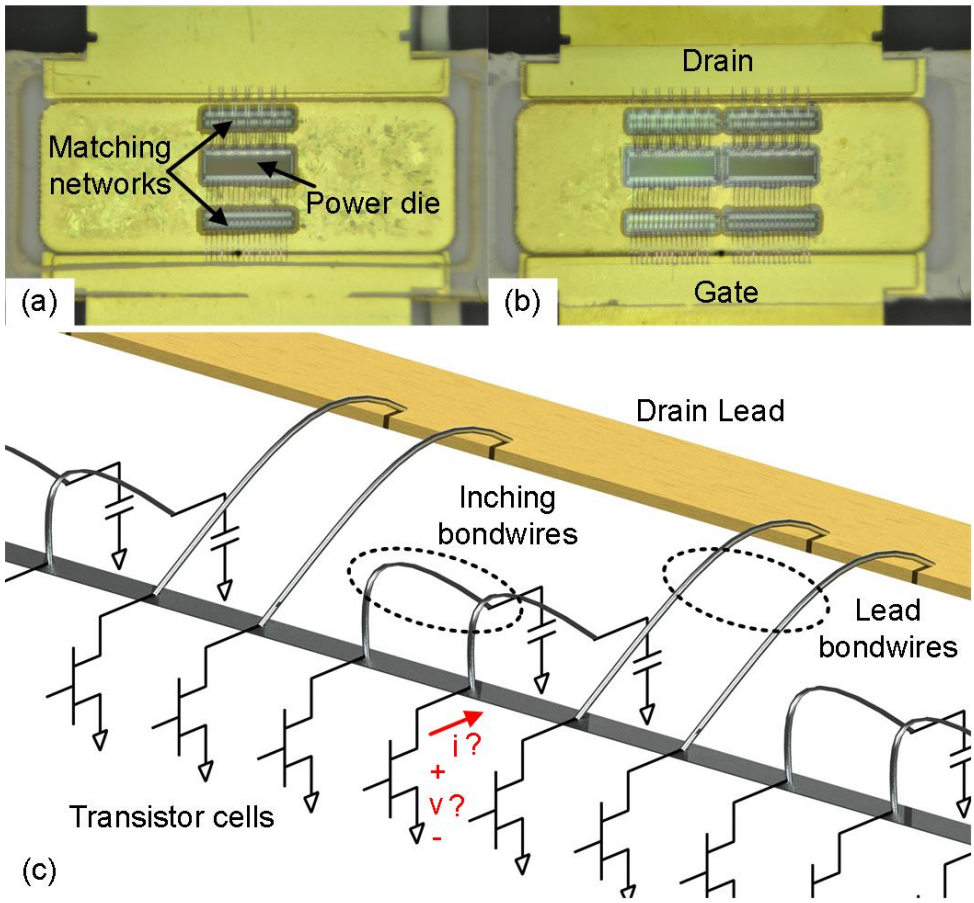

Figure 5.1: Packaged 2.14-GHz 100 W (a) and 200 W (b) LDMOS transistors with internal matching networks to be characterized for their distributed effects. The goal of the characterization is to deduce distributed voltages and currents at individual drain bondwire terminals (c).

such as temperature variations and non-uniform electromagnetic (EM) couplings between bonding wires, lead to an unequal cell performance, degrading gain, power and efficiency. Even worse, unbalanced cells interact, risking odd-mode oscillations and device failure.

Although important for cellular infrastructure performance and reliability, distributed effects in LDMOS devices are difficult to characterize. Nonlinear semiconductor cells interact with each other through electronic, thermal and EM phenomena. Moreover, such interaction has to be measured in-situ without physical intrusion. Because of this difficulty, experimental inspection of distributed effects is up to date mainly done by temperature measurements, e.g. thermal imaging (Fig. 5.2), which is unfortunately not quantitative in the electrical sense. So far, quantitative studies of distributed effects are performed

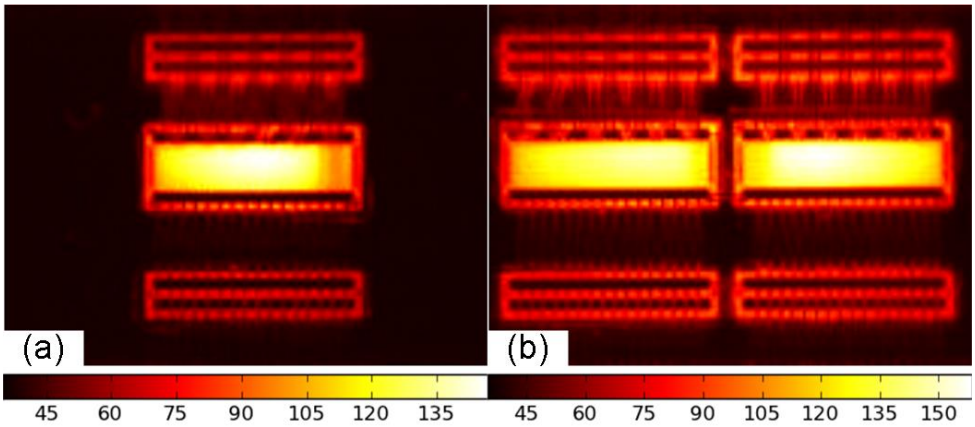

Figure 5.2: Thermographs of the 100-W (a) and 200-W (b) devices at peak power CW operations. Temperature scales are in Celsius. Uneven temperature across transistor dies is evident but electrical consequences to the unit cells are not quantified.

Device	max. power	max. PAE
100 W	50.4 dBm	71.8%
200 W	52.8 dBm	67.1%

Table 5.1: Peak power and peak efficiency measured by fundamental load-pull. Power scaling leads to a degradation of efficiency and power density.

only in multi-physics simulations [2].

In this chapter, we apply the hybrid EM modeling + near-field measurement technique introduced in Chapter 3 to characterize the distributed effects in power devices. Similar as thermography used in prior arts, the measurement of the EM field can be both non-intrusive and in-situ [3–13]. Furthermore, the signal-to-noise-ratio (SNR) limitation of EM measurement is greatly alleviated in this high-power and high-frequency application. Due to these high potentials, applying near-field techniques to study power devices has been actively pursued in recent years [14–18]. The experiment discribed in this chapter advances the state-of-art by combining an EM model of bondwires, measured near-field and calibrated power for LDMOS characterization. Actual voltages and currents at individual drain bondwire terminals of operating LDMOS devices are experimentally quantified for the first time.

5.2. Measurement Description

5.2.1. Devices Under Test

Fig. 5.1 shows the packaged 100 W and 200 W LDMOS transistors (with their ceramic caps removed) made specifically for cellular base station applications from 2110 MHz to 2170 MHz. The transistors consist of 28 V power dies with 0.1

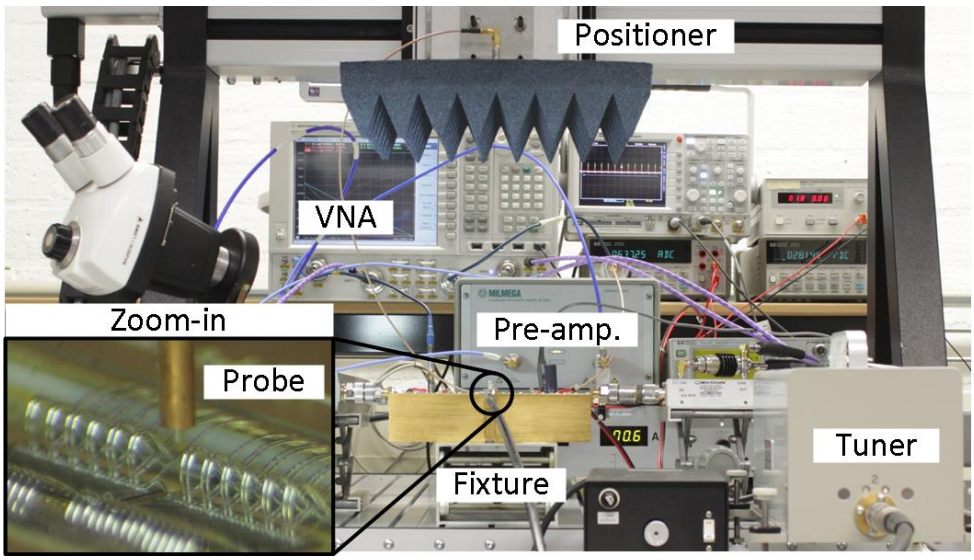

Figure 5.3: Near-field measurement setup used in these LDMOS near-field experiments.

μm gate length and 110 mm total gate width. The dies are 50 μm thin, eutectically attached to metal flanges. High-Q input and output matching networks are also package integrated. In particular, the drain-to-source capacitance is resonated out by parallel inching bondwires at the fundamental frequency (Fig. 5.1 (c)). For each die at the drain side, 24 aluminum bondwires each 50 μm in diameter with 130 μm pitch are grouped in interleaved pairs, forming the 2.5-mm long lead- and 1.1 mm long inching-connections.

Although the 200 W device duplicates exactly the 100 W die and wire bonding manifold, it delivers neither twice the output power nor the same efficiency. The maximum available power and maximum power-added-efficiency (PAE) from the 2 devices are measured by a fundamental load-pull and listed in Table 5.1. Ideal 2x duplication of the 100 W device would yield 53.4 dBm P_{out} and 71.8% PAE, whereas in reality, the actual 200 W device performs below expectation by 0.6 dB in power and 4.7% in PAE.

The conventional method to troubleshoot power transistors is thermography. The infrared images for the 100-W and 200-W devices in peak power CW operation are shown in Fig. 5.2. It can be observed from the the images that the temperature distribution across the power dies is uneven. The center of a power die is hotter than its two edges, likely due to finite thermal conductance. The power dies in this technology are only 50 μm thick exactly for the sake of reducing thermal conductances across the dies. Furthermore, thermal images show that the max die temperature for the 200 W device ($158.5°C$) is 12 degrees higher than that of the 100 W device ($146.7°C$). The heat center also shifts from the center of the die to the inter edges. Rising temperature

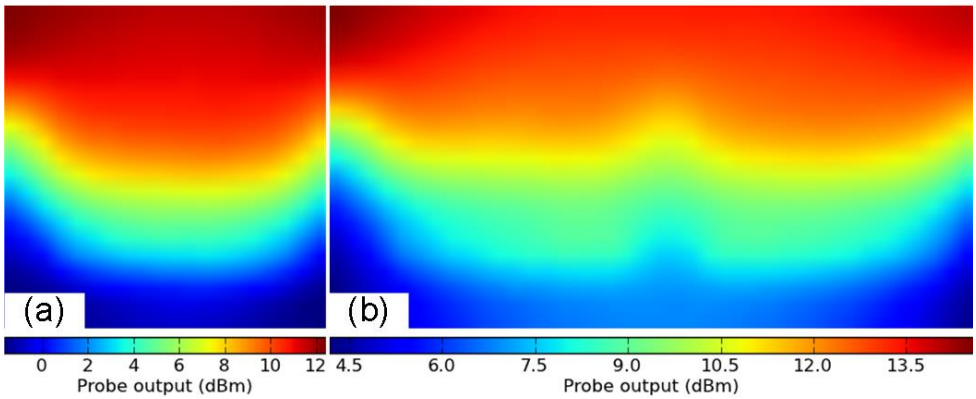

Figure 5.4: Vertically polarized E-field measured 500 μm above drain bondwires of 100-W (a) and 200-W (b) devices at peak power operations.

could explain a reduced power density and efficiency due to reduced electron mobility.

A remarkable advantage of thermography is its low intrusiveness, assuming the emissivity spray does not perturb the device operation significantly. But the foregoing analysis, being qualitative, also exposes the limitation of thermography. The rest of this section explores another non-intrusive method to quantitatively measure internal device operation by observing the microwave region of the electromagnetic spectrum.

5.2.2. Measurement Setup

The electric near-field measurement setup used for these experiments is shown in Fig. 5.3. The DUTs are bolt mounted on a wideband test fixture that provides a 7x impedance up-conversion from device leads to 50 ohm APC7 connectors. This test-fixture is connected to a passive mechanical tuner at the output which provides the optimum fundamental loading condition for maximum efficiency. The devices are biased at 28V drain voltage and 600 mA quiescent current per die, driven to peak power and water cooled. The RF excitation of 2.14 GHz is generated by a vector network analyzer (VNA) and pulsed at 1 kHz repetition rate and 10% duty cycles. The vertical component of the electric field is measured by a 0.5-mm diameter open-ended semi-rigid coaxial cable with a 300 μm center tip protrusion. The probe tip scans 0.5 mm above the drain bondwire manifold in 200 μm steps along and 50 μm steps across the wires.

The field scan result is shown in Fig. 5.4. Since the bondwire arrays are elevated from the power dies, they induce a stronger E-field than the power dies. The die peripheries are observable. But compared with thermal images from Fig. 5.2, the E-field images have are significantly inferior in terms of raw

resolution. The winning edge for E-field imaging is a quantitative relationship from the measured field to the in-circuit electrical quantities, i.e. voltages and currents, within the operating device.

5.2.3. Deduction of absolute V and I from relative E-field

In HFSS, the drain bondwire array for each die is modeled as a 25 port network (Fig. 5.1(c)). 24 ports are on the bondwire terminals at the power die side; and 1 port on the output lead side.

To construct the relationship between port voltages / currents and electric near-field, each port is individually excited while all others are match terminated. This process yields 25 field patterns. The excitation combinations are iterated until the simulated E-field matches the measured one in the least-square sense [16, 18]. In this way, the voltages and currents at wire terminals in the physical measurement are obtained.

Since the E-field probing is relative, the derived voltages and currents differ from their physical values by a scaling factor. This unknown linear scaling factor is deduced by a power calibration. In detail, calibrated power is measured at the APC7 fixture connector. The output fixture tapper is deembedded to determine the actual output power at device package plane. With this knowledge, all near-field determined distributed voltages and currents are proportionally scaled up or down, such that their resulting output power equals the one found by the power calibration.

5.3. Measurement Results

5.3.1. 100-W Si LDMOS

For the 100 W LDMOS transistor, the current and voltage distributions at the 24 output bondwire terminals are plotted in Fig. 5.5 and 5.6 at various power levels. It can be clearly observed from Fig. 5.5 that two different types of bondwire pairs (lead and inching connections) interleave. The inching wire pairs carry 3 times more current than their neighboring lead-wire pairs. Further comparison of the current phases in Fig. 5.5 to the corresponding voltage phases in Fig. 5.6 shows that the at the lead-wire terminals, voltages and currents are in phase, indicating real output power. In clear contrast, at inching wires terminals, the current phase lags 90 degrees from the voltage phase, indicating a pure inductive loading.

These observations are comparable to a medium-Q parallel LCR resonator. In such a circuit, the inductive current compared with resistor current would also have Q times magnitude and 90 degrees phase lag. From this analogy, the intended resonance between the inching wires and C_{ds} is evident. From the observed Q of around 3, it is even possible to estimate the intrinsic bandwidth of these internally shunt-L matched LDMOS devices. In the extreme case, a load modulation of 10:1 (e.g. in an asymmetrical Doherty PA back-off level) would yield a Q-factor of 30. The shunt-L matching could still sustain 70 MHz

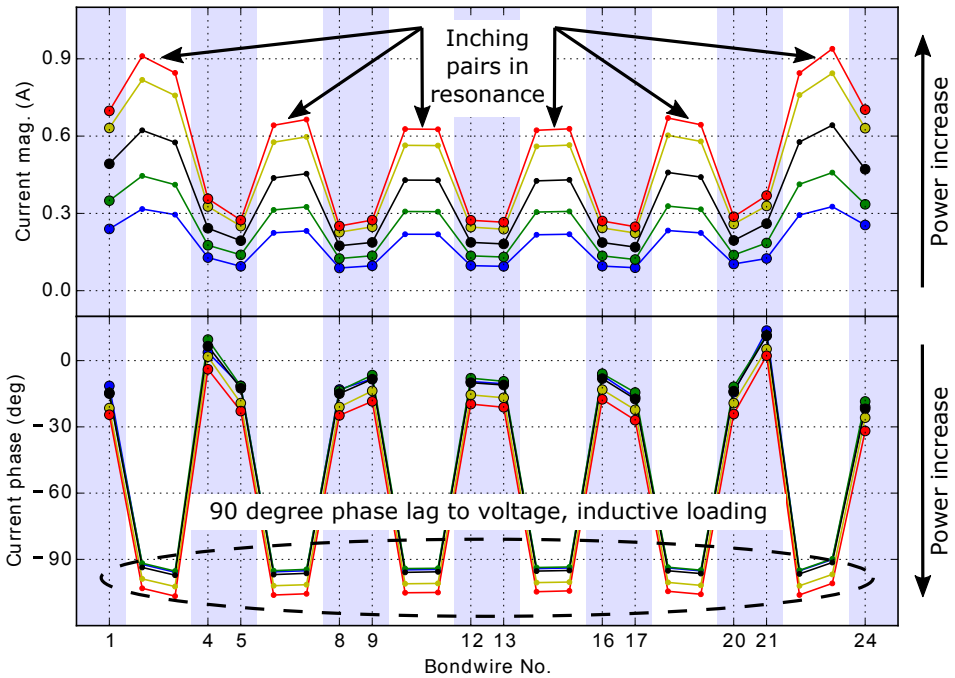

Figure 5.5: Magnitude and phase of the currents at the drain bondwire terminals of the 100W LDMOS power transistor at various output power levels: 10, 7, 4, 1 dB backoff and 2 dB compression.

bandwidth to cover the entire UMTS band 1 (2110-2170 MHz).

Another physical effect noticeable in Fig. 5.5 is the current crowding at the two edges. It is tempting to simply attribute such current crowing as skin effect / proximity effect, from a pure electromagnetic point of view. But in retrospect, from Fig. 5.2, elevated temperature at a die center also reduces output current at the center compared to the die edges (due to lower electron mobility). Therefore, the measured current crowding should better be explained as a combined effect from electromagnetic and thermal perspectives.

It can be observed from Fig. 5.6 that the voltage distribution across the bondwire array is quite flat. Such flatness is understandable since all bondpads at the power die are connected. Fig. 5.6 also shows that voltage phase decreases with an increase of power. Although this AM-PM non-linearity is not a distributed effect, it is still worth a brief explanation. It is well known that Si LDMOS transistors have categorically lagging AM-PM non-linearity. But against common belief, such negative AM-PM is not caused by the voltage knee (triode region) clipping. Knee clipping does cause an AM-PM distortion that is positive/negative with a capacitive/inductive loading condition, as frequently encountered with Gallium Nitride (GaN) high-electron-mobility transistors (HEMT) [19]. But Si LDMOS has predominantly negative AM-PM distortions, under both

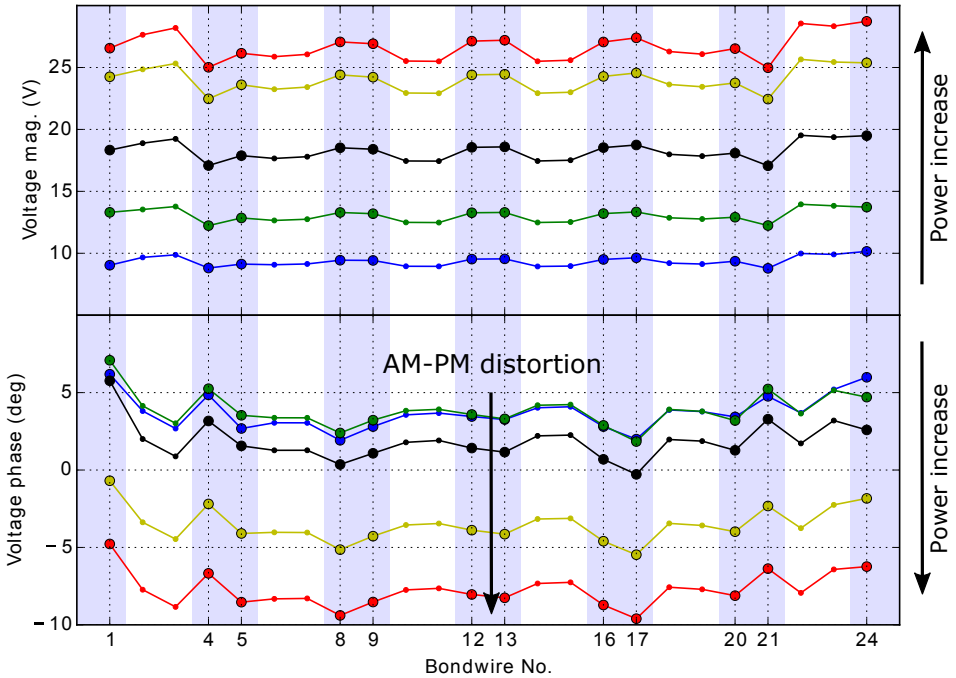

Figure 5.6: Magnitude and phase of the voltages at drain bondwire terminals of the 100W LDMOS power transistor at various output power levels: 10, 7, 4, 1 dB backoff and 2 dB compression.

inductive and capacitive loading conditions. The AM-PM distortion in Si LDMOS is most likely dominated by the non-linear C_{ds} [20]. A power increase leads to a larger voltage swing, a larger C_{ds}, hence a larger current flowing through C_{ds} which leads the drain voltage by 90 degrees. Since the drain voltage in a sound design is close to -180 degree from the intrinsic drain current (I_{ds}), the C_{ds} current will be -90 degrees from I_{ds}. The total drain current, being a vector summation of I_{ds} and C_{ds} current will lag in phase with a increase of C_{ds}.

The output power distribution across the 24 bondwire terminals is plotted in Fig. 5.7. It can be observed that the power distribution is uneven. Outer bondwires carry almost twice power per wire compared to the inner ones. The similarity of Fig. 5.7 to Fig. 5.5 suggests that the power distribution is caused by the current crowding as detailed before. Another effect observed from Fig. 5.7 is the negative power flow into the inching bondwires. Since passive resonant tanks do not generate power, the power inflow has to be supported by parasitic backwave coupling from the output bondwires to the inching bondwires.

As illustrated in Fig. 5.7, the power flow within a large-periphery LDMOS with in-package matching network is complicated. Quantifying this complicated power flow in-situ demonstrates the usefulness of the proposed technique.

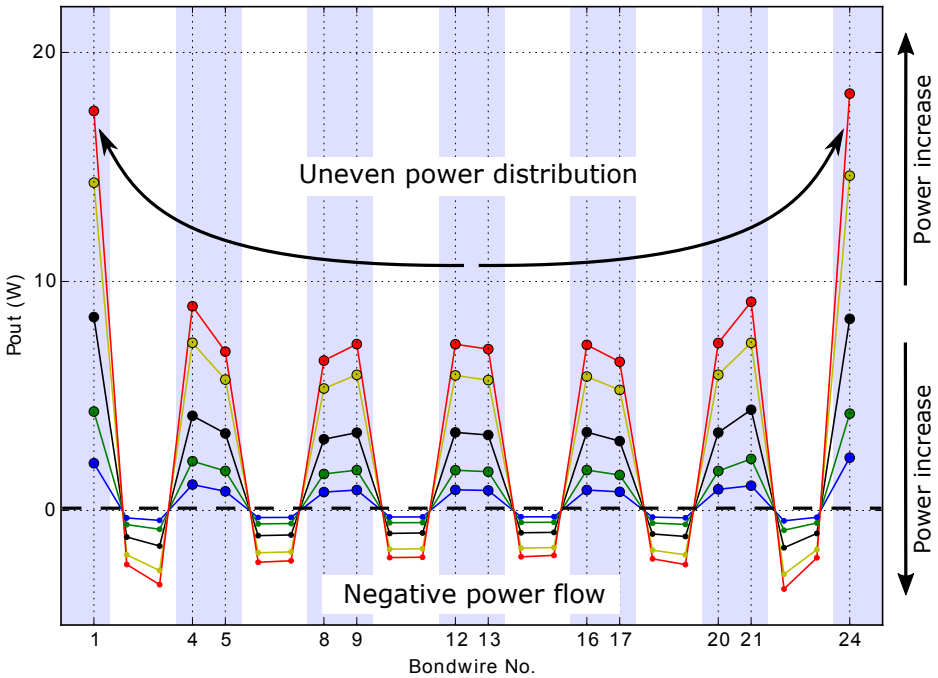

Figure 5.7: Output power into drain bondwire terminals of the 100W LDMOS power transistor at various output power levels: 10, 7, 4, 1 dB backoff and 2 dB compression.

5.3.2. 200-W Si LDMOS

For the 200 W LDMOS transistor, the current, voltage and output power distributions at the 48 output bondwire terminals are plotted in Fig. 5.8, 5.9 and 5.10 at various power levels. Aforementioned phenomena, namely bondwire pairs, inching resonance, current crowding, AM-PM, uneven power and backwave coupling are all visible in the 200 W devices as well. Compared with the 100 W device, the current valley is shifted from the center of the power die to a spot more close to the inner edge. This center shift is in agreement with the hot-spots shift in the infrared image (Fig. 5.2). Furthermore, the current crowding effect is more prominent in the 200 W device, which correlates to the reduced average power density and PAE of this device.

5.3.3. Error analysis

Error analysis of the internal device conditions is not straightforward since quantities at the individual wire terminals are not accessible by conventional techniques. The only possible validation is at the lead-side of the bondwire array, where the effective loading impedance (voltage to current ratio) can be independently verified by conventional fixture deembedding. As shown in Table 5.2, the near-field characterized voltage and current have a ratio error at the device

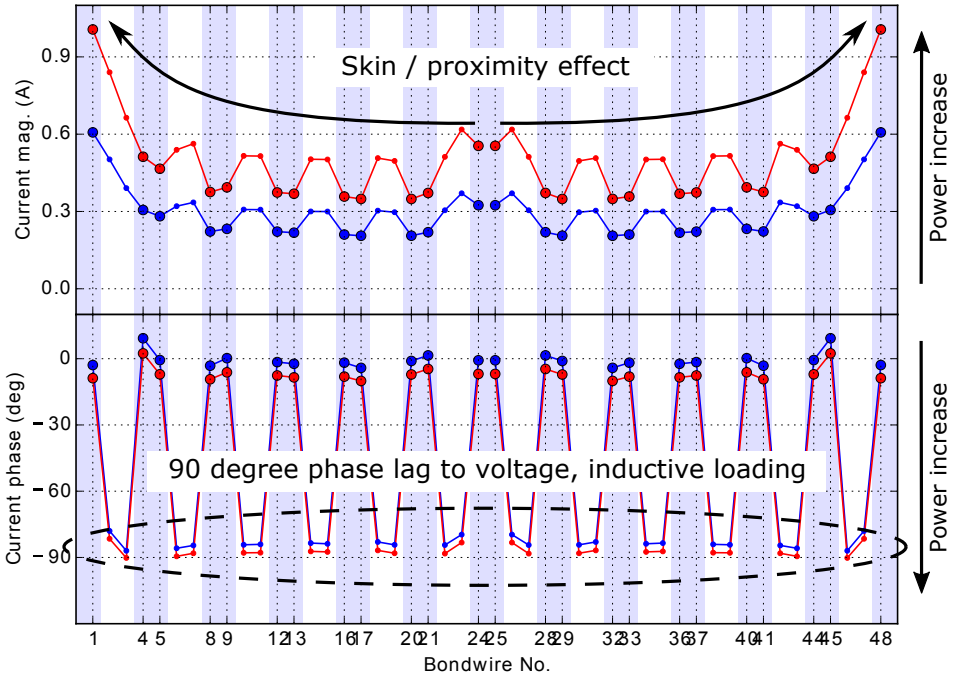

Figure 5.8: Magnitude and phase of the outbound current at drain bondwire terminals of the 200W LDMOS power transistor at peak and 6 dB power backoff.

Device	This method	Conventional de-embedding	Error
100-W	$0.831\angle -162°$	$0.777\angle -158°$	$0.0546\angle -4.11°$
200-W	$0.947\angle -169°$	$0.925\angle -170°$	$0.0223\angle 1.43°$

Table 5.2: Error analysis: Package plane reflection coefficients.

plane of 5% in full-scale magnitude and $4°$ in phase. This can serve both as a sanity check and an error estimation.

5.4. Conclusion

An EM-model-assisted, non-intrusive near-field technique is demonstrated to characterize distributed effects in packaged LDMOS transistors. It enables in-situ measurement of voltages and currents at individual drain-bondwire terminals, yielding deep insight and detailed knowledge for device troubleshooting and optimization. These in-circuit in-situ parameters, which until now are only accessible from simulators, have been experimentally quantified for the first time.

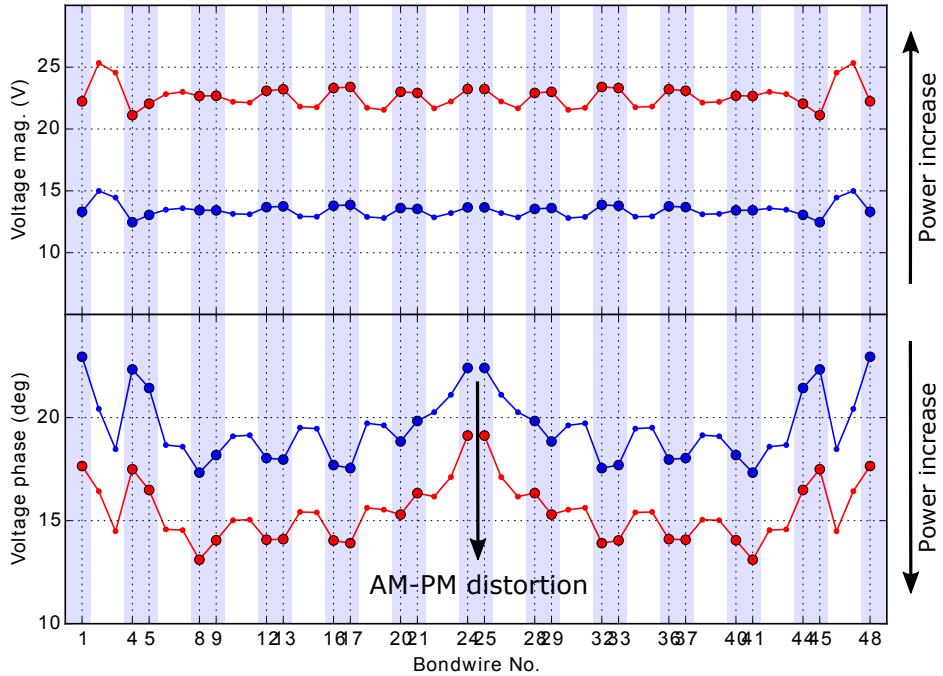

Figure 5.9: Magnitude and phase of the voltages at drain bondwire terminals of the 200W LDMOS power transistor at peak and 6 dB power backoff.

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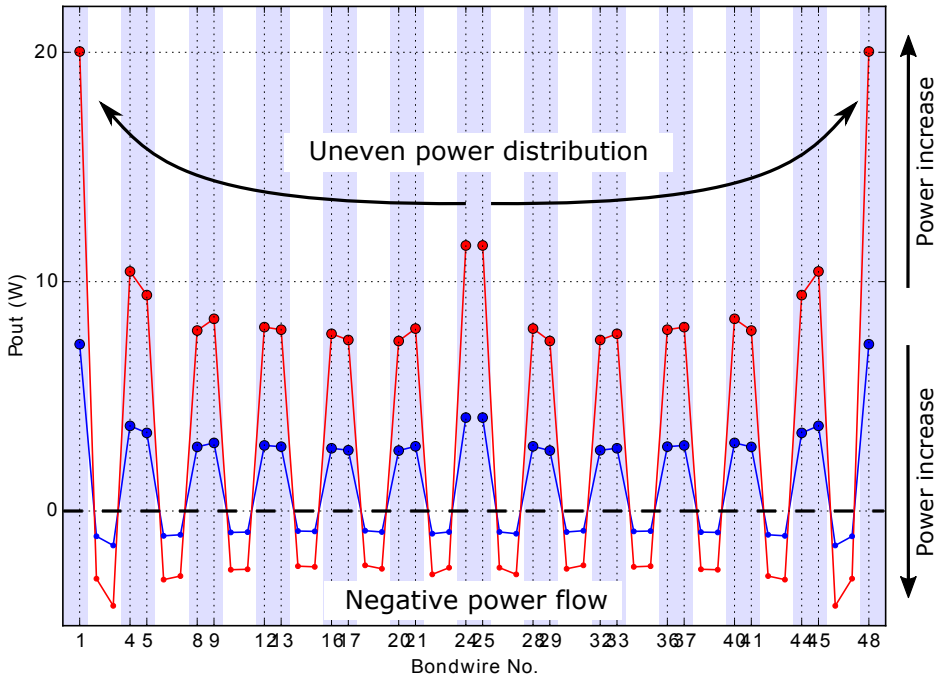

Figure 5.10: Output power into drain bondwire terminals of the 200W LDMOS power transistor at peak and 6 dB power backoff.

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6

Non-intrusive Near-field Characterization of Spatially Distributed Effects in Large-periphery High-power GaN HEMTs

[1]This work introduces an improved non-intrusive near-field technique for in-situ characterization of distributed effects in GaN high-power transistors. Compared with previous passive probing approaches which sense electric fields induced by drain bondwires, the proposed method employs the position-signal difference method to measure E-field induced by transistor fingers. This allows a more robust and detailed identification of the in-circuit electrical quantities, such as voltages, currents, loading impedance and output power, spatially distributed over individual transistor cells and fingers. The electric field has been measured directly at the fingers of a 100W GaN power transistor at fundamental and second harmonic frequencies, while the device operates under realistic loading conditions. The experimentally determined in-circuit quantities are compared to their counterparts from an independently developed distributed in-house model of the same device for validation. The practical value of the proposed method is further demonstrated by uniquely identifying device damage at the finger level (enforced by laser cutting).

[1]Parts of this chapter have been accepted for publication in the IEEE Transactions on Microwave Theory and Techniques.

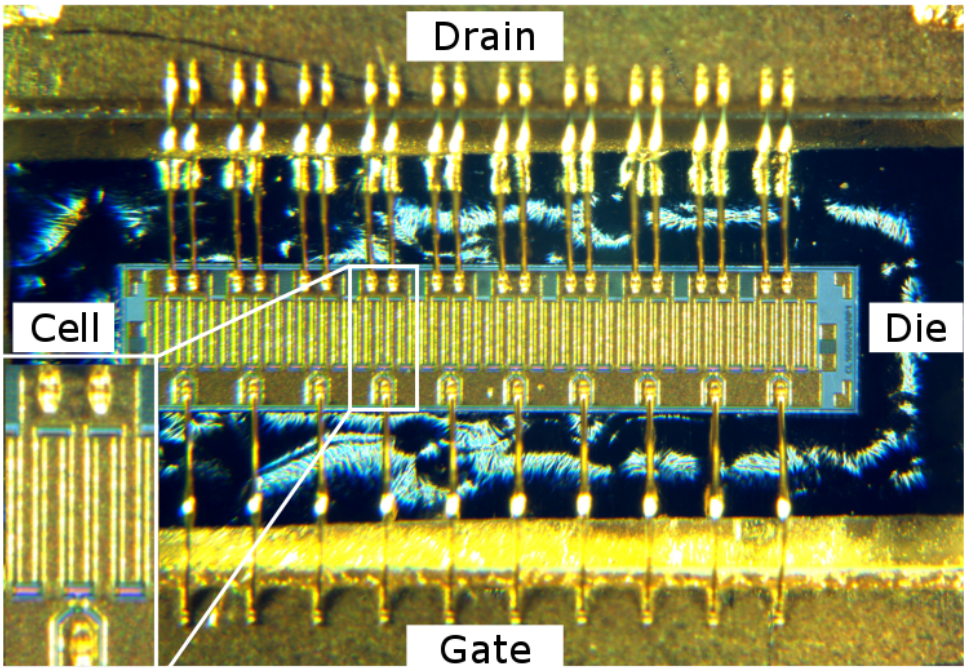


Figure 6.1: Device under test: A packaged Ampleon 100W RF Power GaN HEMT with its ceramic cap removed. The transistor die consists of 10 identical cells in parallel to be characterized for their distributed effects.

6.1. Introduction

Persistent growth of wireless data traffic relentlessly pushes communication networks towards higher frequencies and signal bandwidths, while still requiring high efficiency and output power. The efficiency and output power demands are the highest for the infrastructural transmitters, or more specifically, on their final stage radio-frequency (RF) power amplifiers (PA). Although conventionally powered by laterally-diffused-metal-oxide-semiconductor (LDMOS) transistors, these demanding applications are increasingly adopting gallium nitride (GaN) high-electron-mobility transistors (HEMT) to profit from their high power density, thermal conductivity and efficiency potential [1].

To meet the demand for high power amplification, GaN transistors, like their LDMOS counterparts, are composed out of a large number of identical transistor cells placed in parallel, (as shown in Fig. 6.1), yielding a large periphery transverse to the power propagation direction. When this aggregated periphery becomes thermally and electrically large, identical transistor cells no longer operate under equal (electrical and thermal) conditions. For example, cells at the center of a transistor die experience higher temperature compared to the cells at the edges of this die, due to the finite thermal conductance of the sub-

strate [2]. Furthermore, center cells tend to experience more inductive loading than the outer ones, due to the magnetic mutual coupling of the parallel bondwires at the drain side [3]. Consequently, the distributions of voltage, current and power across the transistor cells are not uniform [2–5]. These distributed effects may strongly affect transistor performance with respect to gain, power and efficiency. Even worse, unequally operated cells may further load-pull each other, causing odd-mode device oscillations.

Although important for cellular infrastructure performance and reliability, the analysis of distributed effects in GaN devices remains a challenging research topic. Previously, distributed voltages and currents of individual cells and fingers in gallium arsenide (GaAs) HEMT [2], HBT [6] and silicon LDMOS [5] devices have been successively quantified by the use of distributed and multi-physics models and simulations. When applying this technique to GaN devices, we encounter increased complexity and uncertainty, due to trapping phenomena, less mature material preparation and processing [7]. As such, transistor-cell performance spread is higher than what can be expected for silicon based technologies. As a result, the multi-physics modeling of high-power GaN HEMTs tends to be more difficult and less well understood than for GaAs and silicon devices. The simplified approach of using the prior art of a multi-physics model to study distributed effects in GaN devices calls for a careful measurement validation.

So far, the validation of power transistor models is often limited to the external device conditions at the package reference planes. Since there are many different internal device distributions that can all yield similar external conditions at the package leads, underlying physical phenomena can be completely masked or erroneously interpreted, while still agreeing to external validation. Due to this reason, imaging techniques, including thermography and passive field probing, were proposed in previous work [5] to validate distributed models in fine resolution and detail.

Thermography [8] observes the infrared (IR) radiation of the device which is directly related to the surface temperature and localized power dissipation across the transistor cells. It has the advantage to be in-situ, which is necessary to characterize spatially distributed effects since they manifest themselves only in an operating device. However, thermography alone cannot directly validate a distributed electrical model in terms of localized voltages and currents.

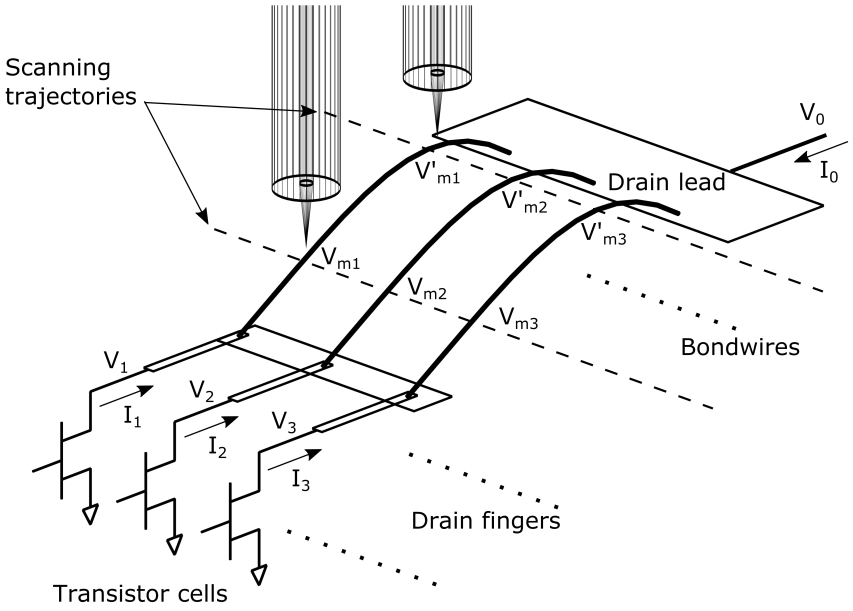
The alternative technique, passive field probing, has been used as an inspection technique in microwave circuit diagnosis for decades [9–13]. These techniques, due to a lack of galvanic contact, typically aim to probe the electric or magnetic field as relative quantities, which are naturally suited for imaging [14–17], as well as to measure ratio quantities such as reflection coefficients and S-parameters [18–25]. Making use of near-field probes for troubleshooting / understanding PA devices in more detail was first envisioned in [26, 27] and has been developed in the recent years [28–33].

Similar with thermography, passive field probing is also capable to characterize distributed effects in an operating device in-situ [33]. More importantly, in contrast with thermography, the electric / magnetic field has a direct relationship to the in-circuit voltages / currents. Therefore, passive field probing has the potential to validate a distributed transistor model directly in terms of its electrical quantities.

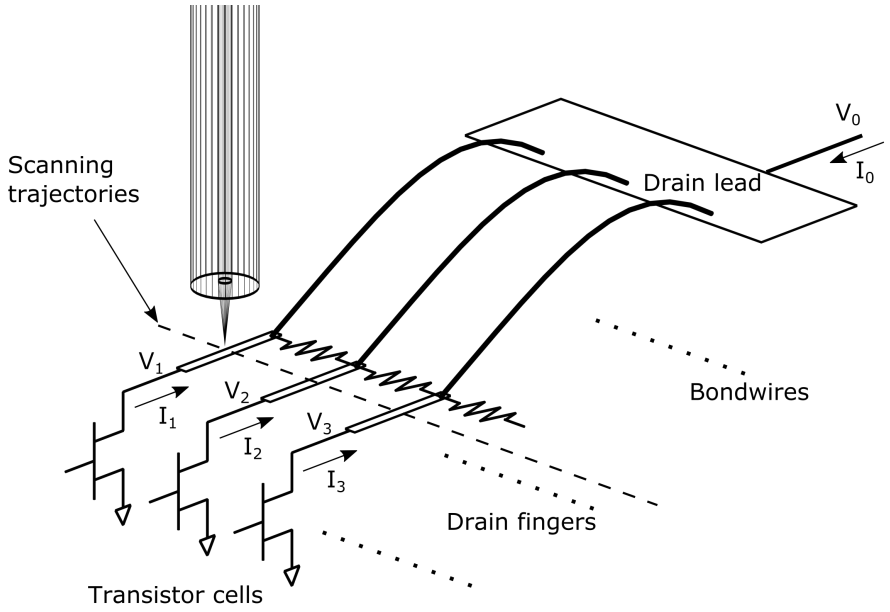
However, such a comparison of distributed model simulation vs. passive field probing measurement has never been reported up to date, probably due to its many difficulties. First of all, packaged transistors are very compact, requiring a miniaturized probe and accurate positioning to achieve sufficient resolution. Secondly, any variation of probe-DUT distance changes their coupling factor, causing measurement uncertainties. These difficulties need to be addressed to enable distributed model validation by means of field probing.

Up-to-date, passive field probing techniques for power device characterization [28–31, 33] have been focused on the E-field induced by the drain bondwire array (Fig. 6.2 (a)). In this work, the E-field is directly probed above the drain fingers of a GaN device instead of its connecting drain bondwires (as shown in Fig. 6.2 (b)). This change of probing location enables us to develop and apply a novel principle to deembed the output bondwire array in a reliable and accurate manner, employing a technique for near-field scanning microwave microscopy (NSMM) named the position-signal difference (PSD) method [34]. As such, the proposed technique improves the prior arts of non-intrusive characterization techniques [28–31, 33] in the following aspects. First and foremost, semiconductor dies have high surface flatness with superior geometric uniformity which cannot be achieved by bondwires, resulting in a much more constant probe-DUT coupling. Furthermore, this improved tolerance permits the probe tip to be lowered to close proximity (10-20μm) above the top metal layer, yielding a very localized coupling to individual drain fingers with high resolution. These improvements enable the in-situ characterization of finger voltages and cell currents distributed in a GaN high-power transistor. Consequently, for the first time, the experimentally quantified voltages and currents at individual fingers and cells are used to validate an independently developed multi-physics distributed model of the same device.

This paper is organized as follows. Section 6.2 describes the GaN device under test. Section 6.3 introduces the in-house developed multi-physics model for this investigation and presents its conventional validation aiming at reproducing RF quantities evaluated at the package reference planes. Section 6.4 explains the underlying principles of the proposed characterization method. Section 6.5 presents the probe construction and properties. Section 6.6 gives the realized measurement setup. Section 6.7 presents the measurement results yielding the deduced voltages and currents distributed at fingers in an operating 100W GaN transistor, which are compared to the results of the in-house developed multi-physics model of the same device. We further demonstrate the practical



(a) LDMOS



(b) GaN

Figure 6.2: (a) Previous bondwire-based near-field scanning technique senses electric field above each bondwires at least at 2 locations to determine the voltage and current for the corresponding cell. (b) Modified ”above die” near-field scanning technique not only mitigates the measurement error induced by bondwire irregularities but also improves the spatial resolution.

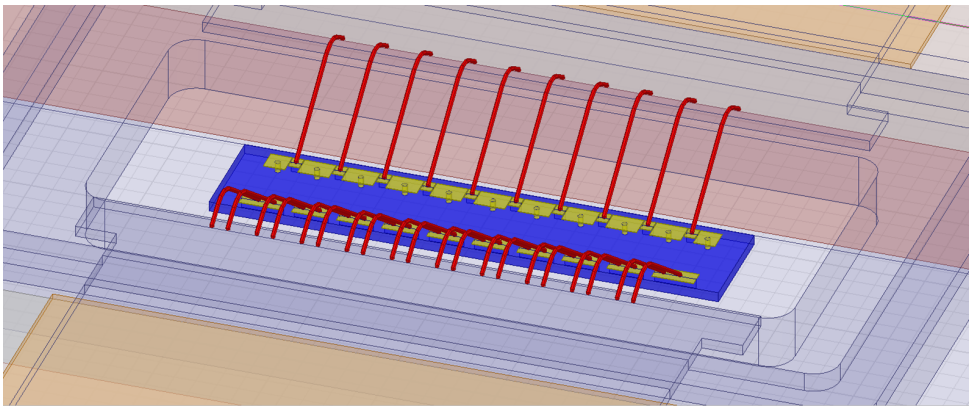


Figure 6.3: Illustration of the three-dimensional structure simulated with HFSS. It comprises the die substrate with bonding pads, gate and drain bond-wires, package and micro strip lines.

value of the proposed technique by in-situ identification of single-finger damage enforced by laser cutting. We conclude in Section 6.8.

6.2. Description of the Device under Test

The device under test is a commercially available general-purpose RF Power GaN HEMT with 100 W rated output power and DC to 3.5 GHz operating frequency provided by Ampleon Netherlands. The device is sealed in a SOT467C flanged ceramic-air package with AuSn die attach.

A photo showing the inside of the package is given in Fig. 6.1. In the center lies a 0.5 μm gate length, GaN on silicon-carbide (SiC) HEMT. The die consists of 10 cells in "parallel". Each cell has 2.4-mm gate width separated into 6 fingers spaced 70 μm apart. At the top metal layer, the drain and source metal fingers are 400 μm long and approximately 60 μm wide. For stability reasons, the drain nodes of the cells are connected by on-die resistors.

The die is connected to the package leads by 38-μm diameter Au bondwires. The gate manifold has 10 bondwires of 1.6-mm horizontal length and 420-μm pitch. The drain manifold has 10 pairs of bondwires of 1.3-mm horizontal length, 150-μm pitch within a pair and 270-μm pitch between pairs.

6.3. Multi-physics Device Model and Simulation

Simulations are performed with an in-house distributed model independently developed at Ampleon. The model consists of an electro-thermal model for the power transistor supplemented by an S-parameter matrix which describes the electromagnetic (EM) effects associated with the packaging structure and bond-wire sets.

Such S-parameter matrix is generated by finite element EM simulations with

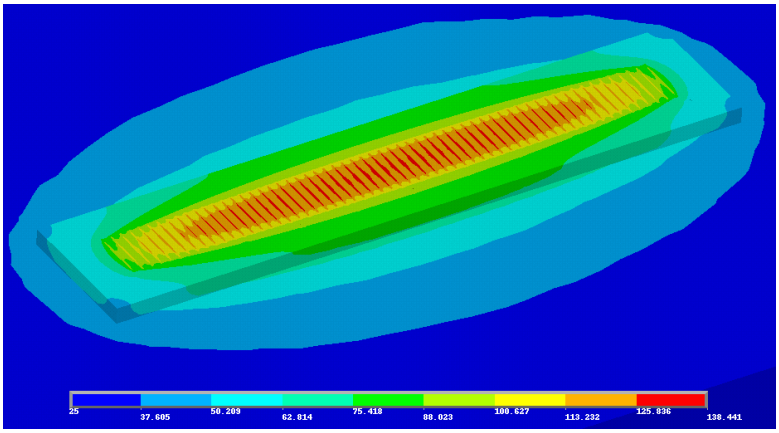


Figure 6.4: Simulated temperature distribution for the entire packaged die corresponding to a uniform power dissipation of 4 W/mm. The bottom of the package flange is held at a constant temperature, while all other surfaces are assumed to be adiabatic. The heat sources run parallel to the gate fingers and are located at the heterojunction interface.

ANSYS HFSS of the three-dimensional structure showed in Fig. 6.3. The structure comprises a substrate with bonding pads, gate and drain bond-wires, the package and a section of a micro-strip line at both the input and output sides. Lumped ports are used as terminations at the bond pads, while a wave port is defined at the beginning of each micro-strip line as excitation.

The power transistor is modelled as a linear array of 10 identical unit cells connected in parallel by a gate bus. The inductive coupling between fingers belonging to different cells is described according to [35]. The thermal resistance matrix of the entire packaged power transistor is obtained by means of finite element ANSYS thermal simulations, previously calibrated against IR measurements. Fig. 6.4 shows the temperature distribution typically observed for the packaged power transistor. Cells in the center portion of the die experience higher temperatures due to the non-uniform spread of the heat. To derive the elements of the thermal matrix, the superposition procedure originally proposed in [6] is used. Specifically, each unit cell j is excited to an appropriate dissipating power P_j sequentially and the resulting temperature increase over the whole die is simulated. The matrix elements are then defined using $R_{ij} = (T_i - T_0)/P_j$ where $P_{i \neq j} = 0$ and temperature T_i for each unit cell is calculated by averaging the peak temperatures of the 6 internal fingers. In this way, the thermal behavior of each unit cell is characterized depending on its location along the array. The thermal resistance matrix of the power transistor has the form of a 10-port impedance matrix, with each port being connected to the thermal node of an instance of the electro-thermal transistor model.

The unit cell electro-thermal transistor model is extracted from DC and RF on-wafer measurements. Harmonic-balance (large-signal) simulations with

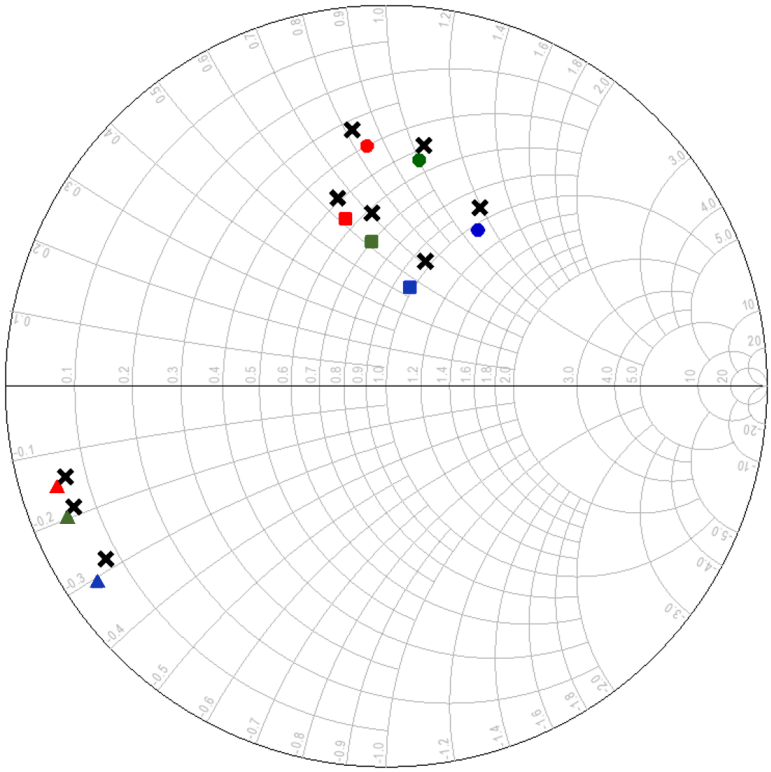
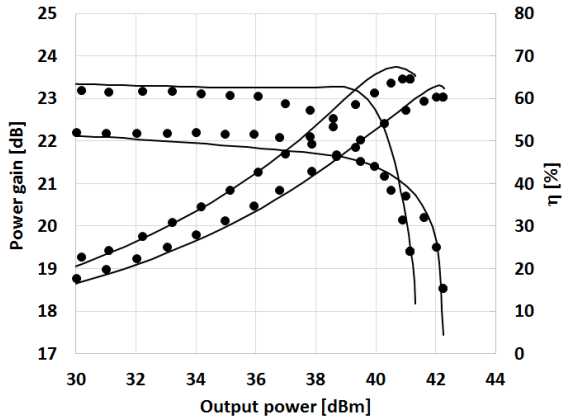


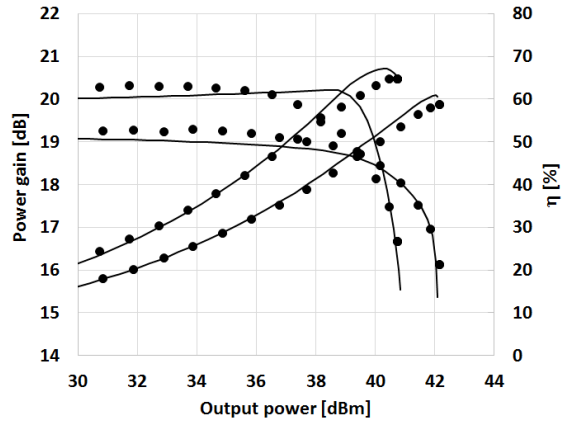
Figure 6.5: On-wafer measured (colored symbols) and simulated (crosses) load impedances for maximum drain efficiency (circles) and maximum output power (squares) and input impedances (triangles) for a single unit cell (2.4 mm die) at 2 (blue), 3 (green) and 4 (red) GHz.

Keysight ADS of the unit cell compare favorably against active load-pull data from 2 to 4 GHz. Specifically, Fig. 6.5 displays measured and simulated load impedances for maximum drain efficiency and maximum output power for a single unit cell at 2, 3 and 4 GHz, whereas Fig. 6.6 shows simulations and measurements of gain and efficiency versus power for the corresponding loads. These results validate the unit cell core model. Subsequently, large-signal simulations of the packaged transistor model have been carried out to verify the correctness of the entire structure. By way of example, the measured and simulated gain and efficiency as a function of the output power at 2.14 GHz are shown in Fig. 6.7. For both measurement and simulation, the load is matched for maximum efficiency. The agreement between the measured and simulated data is acceptable. Since the quantities of Fig. 6.7 are evaluated at the package leads, such comparison generally validates the structure as a two-port network for loads in the high efficiency region.

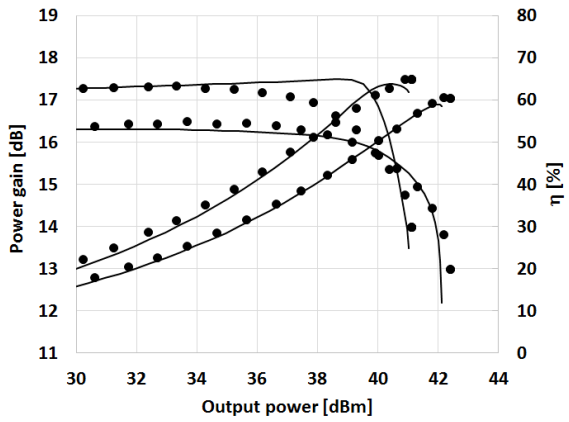
To ascertain the predictive capability of the entire distributed model in terms of the internal voltage and current distributions, additional harmonic-balance



(a) At 2 GHz.



(b) At 3 GHz.



(c) At 4 GHz.

Figure 6.6: On wafer measured (circles) and simulated (lines) power sweeps showing gain and drain efficiency at maximum efficiency and maximum output power loads for a single unit cell (2.4 mm die) at 2, 3, and 4 GHz. Load-pull measurements carried out in pulsed conditions (50 μs pulse width, 5% duty cycle) with second harmonic load not optimized (50 V supply voltage, 30 mA quiescent current).

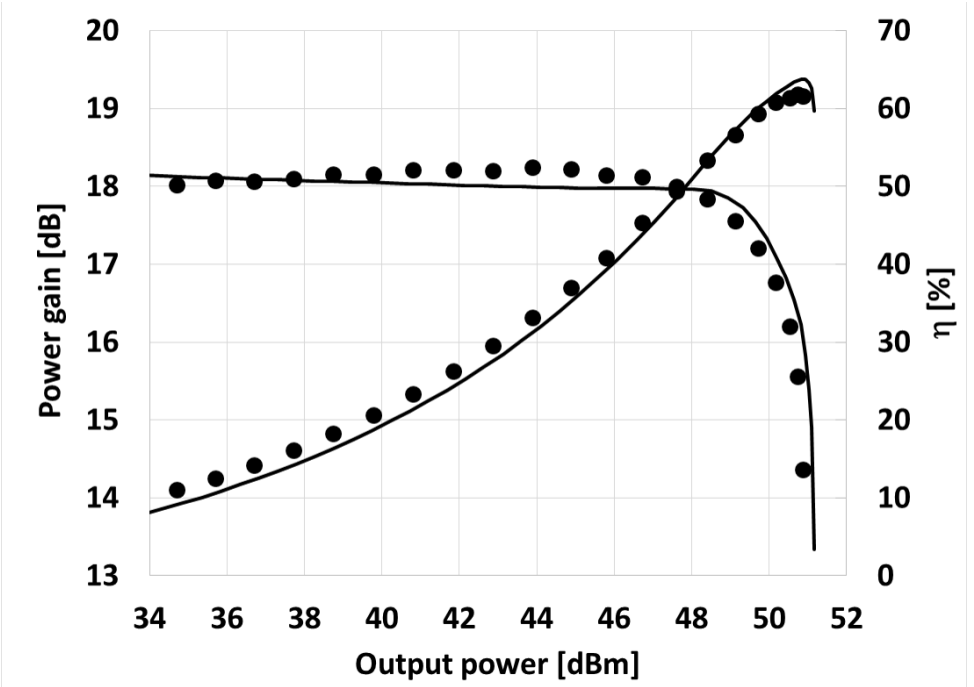


Figure 6.7: Measured (circles) and simulated (lines) power sweeps for the entire packaged power transistor showing gain and drain efficiency at maximum efficiency conditions. The measured maximum efficiency load is 3.9+1.4j Ω while the simulated maximum efficiency load was found to be 3.1+1.0j Ω. Load-pull measurements carried out at 2.14 GHz in pulsed conditions (50 μs pulse width, 10% duty cycle) with second harmonic load not optimized (50 V supply voltage, 300 mA quiescent current).

simulations have been carried out under the same conditions, including biasing, flange temperature and harmonic loading impedances as adopted for the validation measurements of Section 6.7.

6.4. Principle of Deembedding the Output Bondwire Network

The determination of in-circuit voltages and currents on the transistor die from near-field and package-plane microwave measurement requires the deembedding of the output bondwire network. For a general description of this deembedding procedure, the output network of the DUT is simplified as a composition of the drain lead, the bondwire array, and the on-die interconnect to the N drain fingers with resistive connections, as shown in Fig. 6.2 (b). The details of the actual DUT, that every unit cell comprises 3 drain fingers which are shorted by the corresponding drain pad, are not considered here. They are treated as a specific application of the principle and detailed in Section 6.7.

Conventionally, the overall DUT output network can be deembedded as a 2-

port. Consequently, all the active fingers are considered to be lumped together. In other words, the conditions

$$\begin{aligned} i_{tot} &= i_1 + i_2 + \cdots + i_N \\ v_{tot} &= v_1 = v_2 = \cdots = v_N, \end{aligned} \tag{6.1}$$

are implicitly assumed. Under this assumption, the 2-port bondwire array network enforces an I-V relationship by a 2-by-2 admittance matrix

$$\begin{bmatrix} i_0 \\ i_{tot} \end{bmatrix} = \begin{bmatrix} y_{0,0} & y_{0,tot} \\ y_{tot,0} & y_{tot,tot} \end{bmatrix} \begin{bmatrix} v_0 \\ v_{tot} \end{bmatrix}. \tag{6.2}$$

This admittance matrix $[Y]_{2\times 2}$ is solely and completely determined by the passive bondwire array network. In other words, it is a constant matrix that does not vary with operating conditions. The constant values in $[Y]_{2\times 2}$ can either be measured from a physical duplicate in a deembedding fixture or numerically extracted from an EM model. In an operating device, since the exact voltage and current waveforms at the drain lead (i_0 and v_0) are accessible by conventional techniques such as LSNA or NVNA, the lumped voltage and current waveforms for the transistor die (i_{tot} and v_{tot}) can be deduced by (6.2). This 2-port deembedding method works fine for small periphery devices.

For high-power devices (large-periphery) operating at high frequency (short wavelength), such as the GaN DUT, the lumped assumption in (6.1) may not be valid any more. In order to quantify the distributed effects, voltages and currents at the individual fingers ($v_1, v_2, \cdots, v_N$ and $i_1, i_2, \cdots, i_N$) need to be considered as independent quantities. Consequently, the bondwire array segment has to be modeled in more detail as an $N+1$-port network as shown in Fig. 6.2 (b), i.e.

$$\begin{bmatrix} i_0 \\ i_1 \\ \vdots \\ i_N \end{bmatrix} = \begin{bmatrix} y_{0,0} & y_{0,1} & \cdots & y_{0,N} \\ y_{1,0} & y_{1,1} & \cdots & y_{1,N} \\ \vdots & \vdots & \ddots & \vdots \\ y_{N,0} & y_{N,1} & \cdots & y_{N,N} \end{bmatrix} \begin{bmatrix} v_0 \\ v_1 \\ \vdots \\ v_N \end{bmatrix}. \tag{6.3}$$

Similar as in the two-port approach of above, the admittance matrix $[Y]$ of the passive bondwire array, being constant, can either be determined by a multiport measurement of a physical duplicate or numerically extracted from an EM model; and the output port conditions i_0 and v_0 can be measured by LSNA or NVNA. However, deembedding the distributed bondwire-array from 1 port to N ports is no longer feasible due to the under-determined equations in (6.3). Extra N quantities have to be determined. E.g. distributed currents ($i_1, i_2, \cdots, i_N$) can be solved from (6.3) if we know the distributed voltages ($v_1, v_2, \cdots, v_N$).

The voltages at individual fingers are not directly accessible by conventional microwave techniques. But each of the energized fingers does induce an electric

field around it. Due to passiveness, the superposition principle yields

$$\begin{bmatrix} E_1 \\ E_2 \\ \vdots \\ E_N \end{bmatrix} = \begin{bmatrix} t_{1,1} & t_{1,2} & \cdots & t_{1,N} \\ t_{2,1} & t_{2,2} & \cdots & t_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ t_{N,1} & t_{N,2} & \cdots & t_{N,N} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix}, \tag{6.4}$$

where t_{ij} denotes the contribution from finger voltage v_j to E-field E_i. These E-field components can be measured by a passive probe. If the measurement is performed in close proximity with sufficient resolution, the measured E-field components can be so dominated by the localized voltage on a single finger that the influences from other finger voltages become negligible. In this case, the $[T]$ matrix becomes diagonal. Moreover, if the localized E-field can be taken in consistent manners for each finger, thanks to the surface flatness of the semiconductor die, then all the diagonal elements of the transfer matrix can be assumed equal, i.e.

$$\begin{bmatrix} E_1 \\ E_2 \\ \vdots \\ E_N \end{bmatrix} = t \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix}. \tag{6.5}$$

If we could measure the N E-field components with localization and consistency properties as defined in (6.5), the proportional factor t can be derived from first row of (6.3) as

$$t = \frac{y_{0,1}E_1 + y_{0,2}E_2 + \cdots + y_{0,N}E_N}{i_0 - y_{0,0}v_0}. \tag{6.6}$$

It should be noted from (6.6) that the measurement of $E_{1,2,\ldots,N}$ does not need to yield absolute magnitude and phase. Relative magnitude and phase of $E_{1,2,\ldots,N}$ among the N spatial locations are sufficient since the proportional factor t can absorb any magnitude and phase scaling between the relative field measurement of $E_{1,2,\ldots,N}$ and the absolute waveform measurement of v_0 and i_0. Therefore, the transfer function of the E-field probe, and the absolute distance between the probe and the DUT do not need to be calibrated.

After the deduction of factor t from (6.6), all the finger voltages can be derived from (6.5) and all finger currents from (6.3). As such, distributed voltages and currents at the individual fingers ($v_1, v_2, \cdots, v_N$ and $i_1, i_2, \cdots, i_N$) can be deduced from the acquisition of output quantities v_0, i_0, near-field $E_{1,2,\ldots,N}$ and the Y-parameters $[Y]$ of the passive bondwire array.

Since the output quantities v_0, i_0 and the near-field $E_{1,2,\ldots,N}$ vary with the device operating conditions (bias, input, load impedance, temperature, etc.), obtaining them clearly requires in-situ measurement. On the other hand, since the Y-parameters $[Y]$ of the passive bondwire array are constants, they can either be determined off-line by a multi-port measurement of a physical duplicate or numerically extracted from an EM model. Determination of the Y-parameters

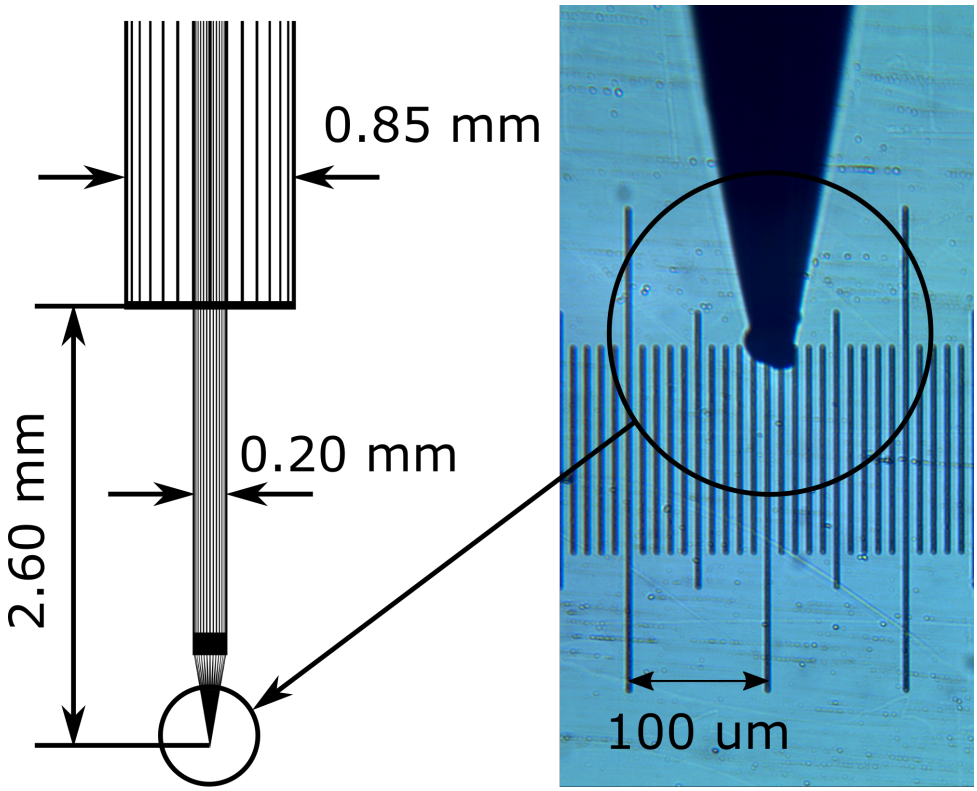


Figure 6.8: E-field probe illustration. Probe tip wears out due to repeated landing for vertical alignment.

by measurement would be tedious but is not theoretically impossible. In practice though, it is much more convenient to extract them from an EM model of the passive output network, which is the approach adopted for this work.

6.5. E-field Probe Considerations

6.5.1. Probe Description

The E-field probe is a 50-Ω semi-rigid coaxial cable with a sharp 2.6-mm-long center tip, as shown in Fig. 6.8. The outer conductor is made of copper with an outer diameter of 0.85 mm. The center conductor is made of tungsten with a diameter of 0.20 mm. The probe tip (shown in the photo in Fig. 6.8) had a 10-μm diameter but has been worn out to 30 μm due to repeated landing for vertical alignment.

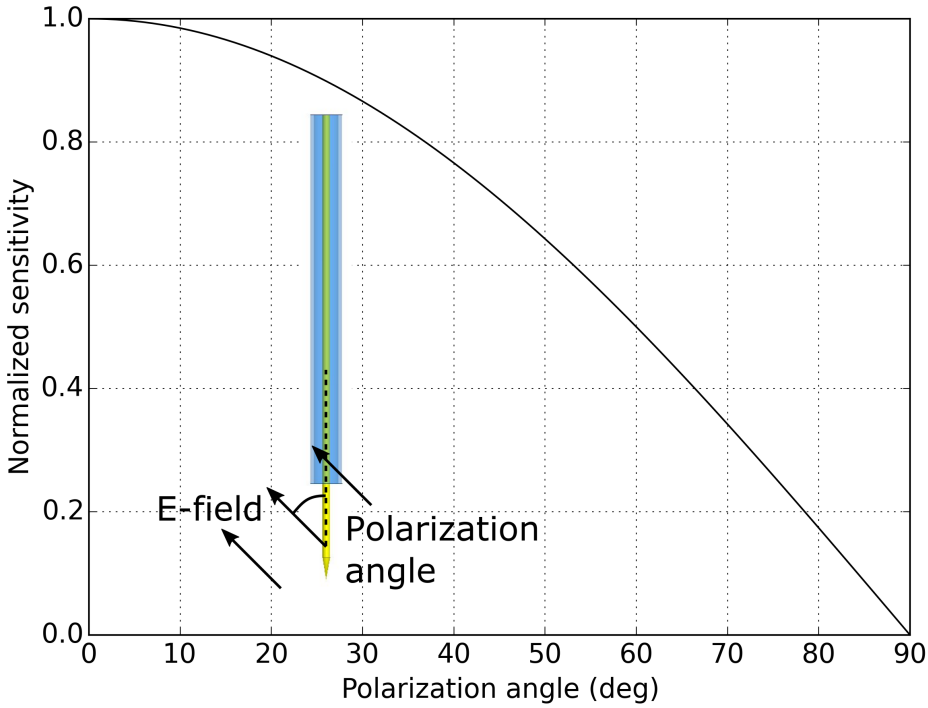


Figure 6.9: HFSS simulation of probe sensitivity to polarized E-field: The E-field probe is excited by an incident propagating plane wave of 4 GHz in free space. The probe axis is at the same plane as the E-field vector and the propagation direction of the plane wave. The normalized probe response to the excitation is plotted against the angle between the probe axis and the E-field vector.

6.5.2. Probe Properties

Polarization

Since the E-field probe shown in Fig. 6.8 is axially symmetric, it is only sensitive to the E-field polarized in its axial direction. To verify this, a 3D EM simulation is performed in HFSS where the probe structure is driven by an incident plane-wave excitation in free space with different polarization. The simulation result is plotted in Fig. 6.9.

As can be observed, the sensitivity of the probe is the strongest when the E-field is polarized in the same direction as the probe axis, but zero when the E-field vector is perpendicular to the probe axis. Therefore, the probe, when vertically mounted, is only sensitive to the vertical component of the E-field.

Such ideal polarized sensitivity relies on a perfectly axial symmetry. In reality, engineering tolerance of probe construction and mounting orientation limit the achievable rejection of E-field components in the radial directions.

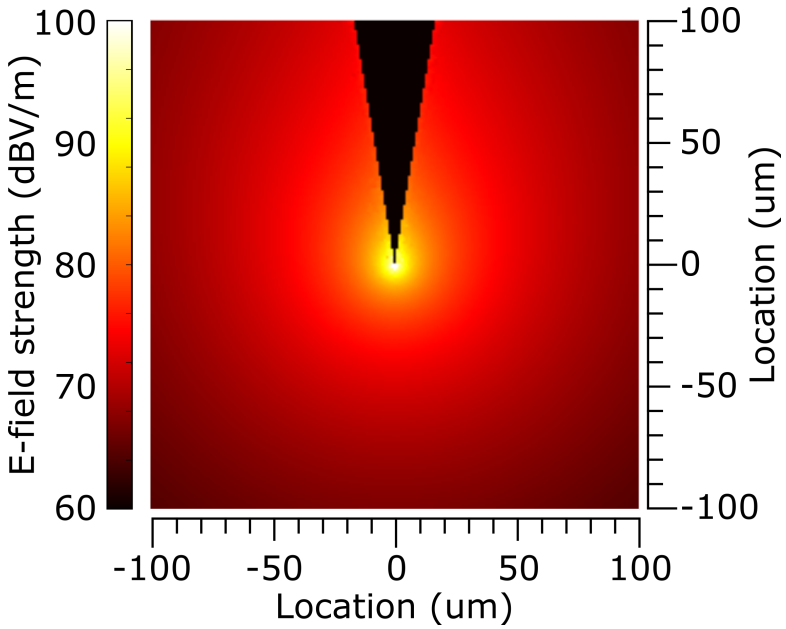


Figure 6.10: HFSS simulation of probe radiation pattern: The E-field probe is excited by an incident wave of 1-V magnitude at 2 GHz from the coaxial port. The strength of the vertical component of the induced E-field is plotted.

Resolution

To visualize the spatial resolution of the E-field probe, the radiation pattern of the probe is simulated in HFSS and plotted in Fig. 6.10. It should be identical to the receiving pattern of the probe due to antenna reciprocity. From Fig. 6.10, it is observed that the probe is most sensitive to the E-field in the proximity of its tip. Therefore, reducing the probe-DUT distance enhances both sensitivity and resolution.

A more quantitative analysis is shown in Fig. 6.11, where several horizontal slices of Fig. 6.10 are taken at different heights (10, 30 and 50 μm) below the probe tip. It is observed in Fig. 6.11 that the curves flatten out with an increase of probe-DUT distance, indicating a degradation of spatial resolution. But a differential readout at 10 and 50 μm (also shown in Fig. 6.11) actually enhances the spatial resolution even beyond that at the closest distance of 10 μm. This technique is originally proposed in [34] as the position-signal-difference (PSD) method. In this work, the PSD method is advantageously employed to achieve finger-level resolution without disturbing the operating DUT.

Intrusion

The probe tip being a piece of metal enforces a very different boundary condition from that of air. Hence it inevitably influences the electric field distribution

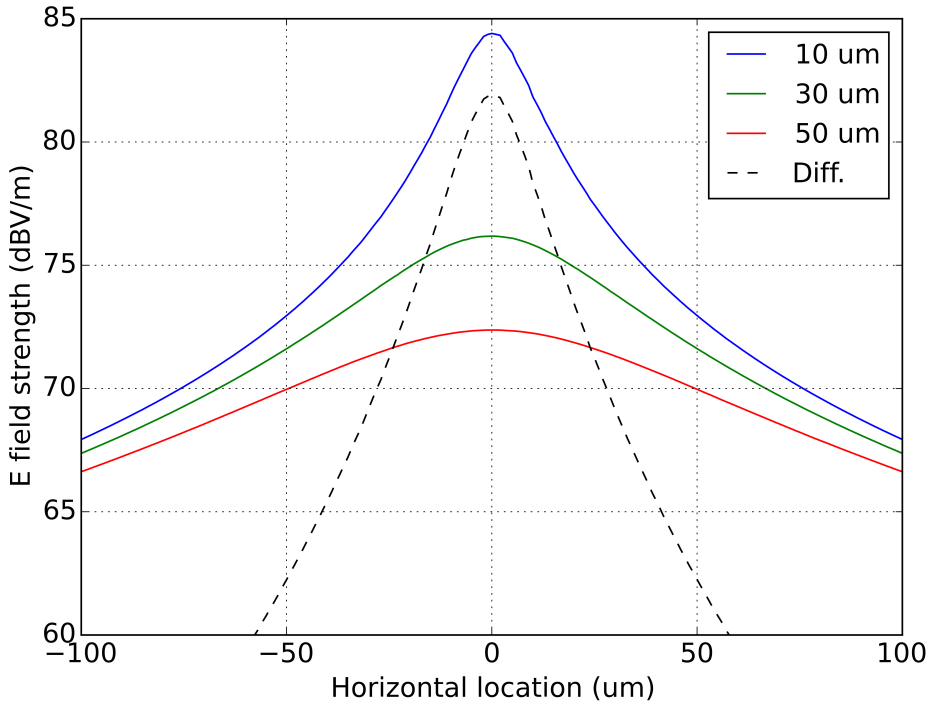


Figure 6.11: HFSS simulation: spatial resolution of the probe with probe-tip-to-DUT distance of 10, 30 and 50 μm. The difference between the 10 and 50 μm readout improves the resolution.

induced by the DUT. When such an influence occurs in the reactive near-field, as is generally the case, the presence of the probe exerts a perturbation on the DUT, potentially altering in-circuit quantities to be measured.

To demonstrate this effect, the influence of the E-field probe to the E-field induced by a microstrip line is plotted in Fig. 6.12 (a) and (b). The extra E-field induced between the line and the probe varies proportionally with the line voltage pin-pointed by the probe tip, which is necessary for the voltage sensing. But this said E-field also stores electric energy as a capacitance, which has a loading effect to the microstrip line.

Due to this reason, for non-intrusive measurement, the extra capacitance induced by the probe needs to be reduced to a negligible level to the DUT by keeping a certain probe-DUT distance. In other words, in order not to disturb the DUT, the mutual impedance between the probe and the DUT should be much greater than the self-impedance of the DUT, as will be further addressed in Section 6.7.

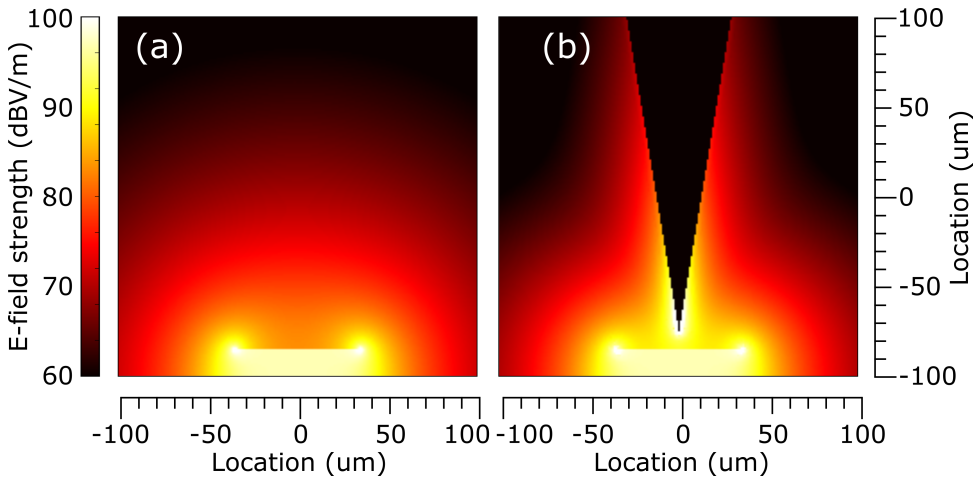


Figure 6.12: HFSS simulation of probe intrusive effect: A 50-Ω 70-μm microstrip line suspended in air. The line is excited by an incident wave of 4 GHz and 1-V magnitude at one end and match terminated at the other end. The E-field strength at a cross section of the line, without and with the E-field probe 10 μm above the line, is plotted in (a) and (b), respectively.

6.6. Measurement Setup

The block diagram for the electric-field measurement setup is shown in Fig. 6.13. The bottom part is conventional for a power transistor load-pull system. An RF test signal is generated by a pulse modulated source (RF src.1), pre-amplified by a driving PA and monitored by the input bi-directional coupler (as a_1 and b_1). The DUT is mounted on a test fixture which transforms the input and output impedance (from 50 Ω APC7 connectors to 12.6 Ω at device package planes), biases the gate and drain, and dissipates the heat by water cooling. At the output side, a mechanical tuner sets the fundamental loading condition of the DUT, which is monitored by the output bi-directional coupler (as a_2 and b_2). This configuration puts the DUT under its nominal operating conditions with controlled biasing, loading impedance and temperature.

Above the conventional setup, the coaxial probe detailed in Fig. 6.8 senses the vertical component of the electric field induced by the operating DUT. The probe output is coupled out by a third bi-directional coupler as b_3 in the figure. All the coupled waves (a_1, b_1, a_2, b_2 and b_3) are coherently measured by a VNA (Agilent 4-port PNA-X N5242A). In order to reconstruct the voltage waveform from measured harmonics, the VNA also coherently measures a harmonic phase reference (Agilent U9391C) b_4, driven by another RF source (RF src.0) which is synchronized (10-MHz phase locked) to the test signal generator (RF src.1).

The E-field probe is positioned by a computer controlled motorized 3-dimentional linear translation stage. The vertical alignment of the probe to the DUT is indicated by a DC volt meter when the probe tip contacts the top-layer metal of the biased DUT. The horizontal probe-DUT alignment is based on an NSMM image

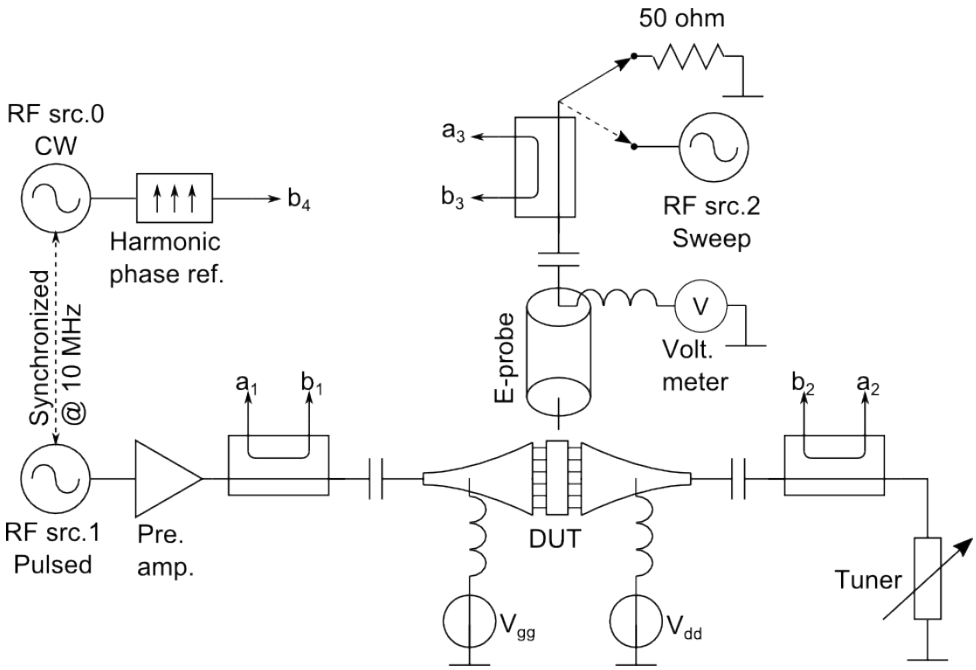


Figure 6.13: Block diagram: measurement setup.

taken by the same setup while the DUT is powered off. To take such an image, a third RF source (RF src.2) injects power (frequency swept) into the field probe to illuminate the (unbiased) DUT. The reflection coefficient from the probe tip is monitored by the probe coupler (b_3/a_3) and registered with locations to form the image.

The details of the measurement setup are shown in Fig. 6.14. The DUT (with its ceramic cap removed) is bolt-mounted on the test fixture. The mount leaves a 10-by-10 mm window so that the field probe can access the transistor die.

The positioning accuracy is paramount for the proposed technique to work. As shown in Fig. 6.14, a laser pointer mounted in parallel to the E-field probe, together with an oblique-looking long-focal-distance microscope, are used for rough probe positioning. After this, a fine positioning based on NSMM imaging and probe contact has to be performed. The top metal layer of the DUT semiconductor die has an inter-digit pitch of only 70 μm. Probe horizontal position uncertainty should be smaller than this to achieve finger level resolution. Furthermore, in the measurement process, the probe tip is placed 15 μm above the top-layer metal surface of the die. This choice of height is a trade-off between resolution and intrusiveness, as will be detailed later. A vertical positioning error introduces a voltage measurement error and should thus be minimized. The 3D translation stage used in this experiment has a rated positioning accuracy

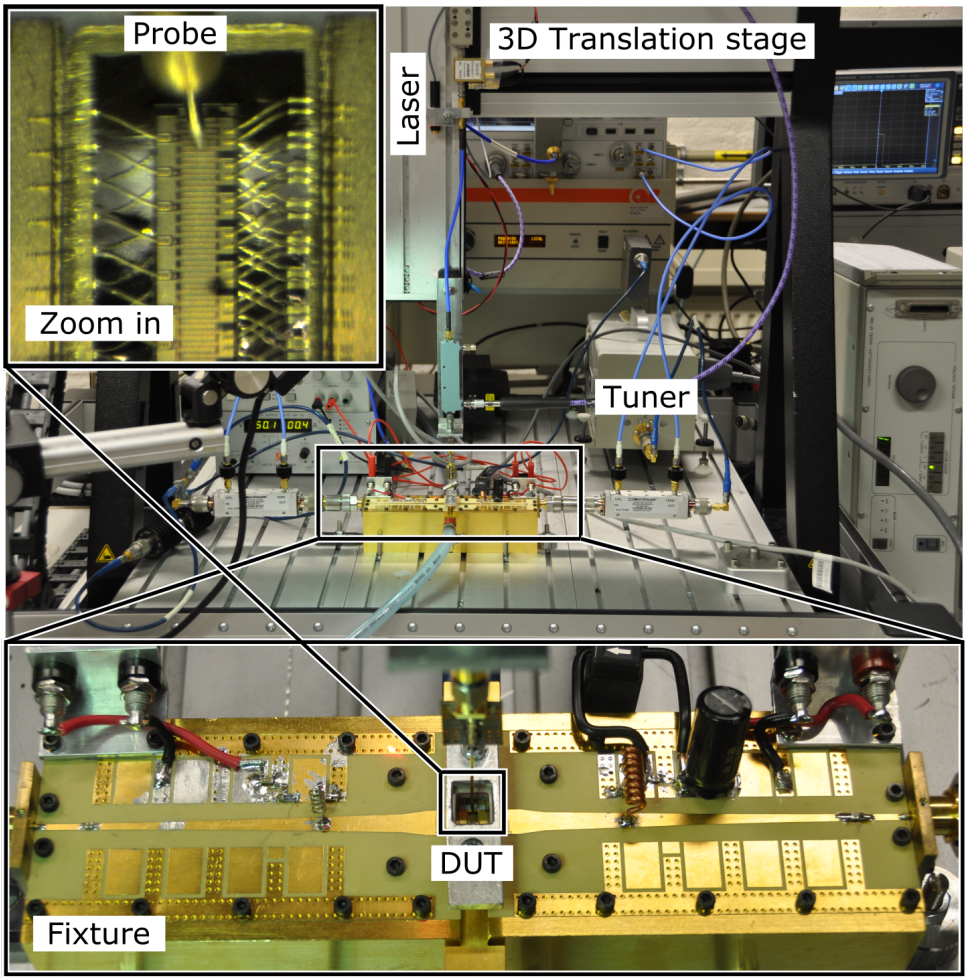


Figure 6.14: Measurement setup in reality.

of 1 μm. Its vertical positions are further checked by a laser interferometer to be repeatable within 0.1 μm.

In high power measurement of this kind, thermal expansion of the fixture chuck may cause significant vertical positioning error. For example, CW excitation of the DUT (under max. efficiency loading condition) to its 100 W rated power for 15 minutes causes a thermal expansion of the fixture up to 50 μm above its height in room temperature, despite continuous water cooling. This growth easily consumes the 15 μm probe-DUT distance and causes a mechanical contact. Such a contact during a probe scan may short-circuit the top-layer metal gaps between drain and source and destroy the DUT instantly. For instrument safety, an extra DC block and 10 dB attenuation are always applied

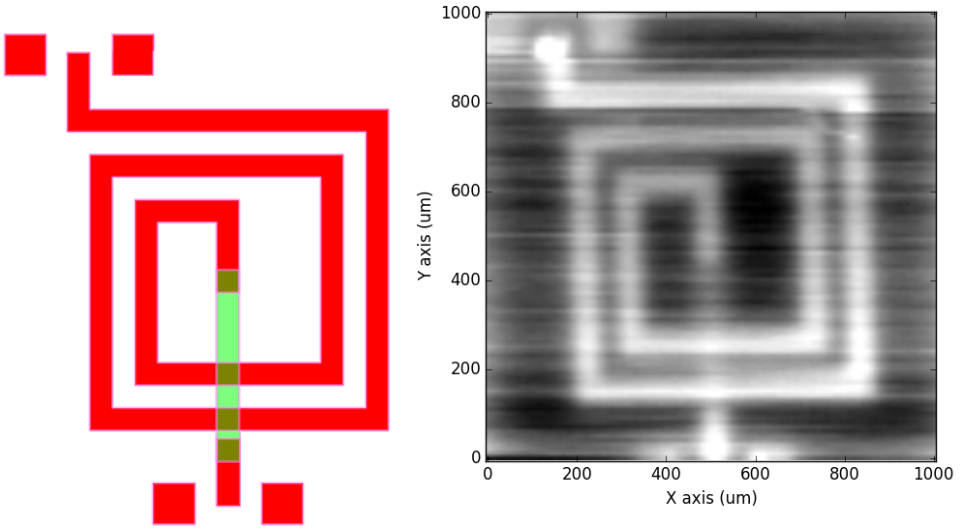


Figure 6.15: NSMM resolution: a spiral inductor layout (a) vs. its NSMM image (b).

between the field probe and the VNA despite their negative impact on sensitivity. For device safety, low duty-cycle pulsed RF together with water cooling reduce the thermal expansion effectively.

6.7. Measurement Results

6.7.1. NSMM Resolution

In order to prevent damage in case of a probe-DUT contact, their fine alignment is performed while the DUT is powered off and illuminated by the E-field probe, as an NSMM imaging process. The horizontal resolution of the proposed NSMM imaging setup is shown in Fig. 6.15. Fig. 6.15 (a) shows the layout of a 2.5-turn spiral inductor with 50-μm traces and 50-μm trace spacing. The spiral inductor is fabricated on the top 2 Aluminum layers on a silicon wafer and scanned by the proposed NSMM setup.

The VNA measures the reflection coefficient of the probe from 100 MHz to 5 GHz in 100 MHz steps. The probe scans a 1000-by-1000 μm area 20 μm above the top metal layer in 10 μm steps. The phase of the measured reflection coefficient, averaged in frequency, is plotted in a gray scale shown in Fig. 6.15 (b). It can be observed that the 50 μm traces are clearly identifiable. The ratio of resolution (around 10 μm) to the shortest wavelength (at 5 GHz) is around $R/\lambda \approx 1.7 \times 10^{-4}$. Since this resolution is sufficient to distinguish the 70 μm

inter-digit pitch found on the top metal layer of the GaN transistor under test, the proposed NSMM setup is viable for fine horizontal alignment of the DUT for finger level resolution.

6.7.2. Probe Intrusion

Minimizing the probe-DUT distance improves resolution, but the probe intrusion needs to be carefully checked to prevent the probe from disturbing the DUT from its normal operation.

In order to find a minimum non-intrusive probe-DUT distance, the E-field probe scans at different heights along a 6.5-mm long coplanar waveguide (CPW) on a Cascade CSR-3 impedance standard substrate (ISS). The CPW is excited by a ground-signal-ground contact probe at one end, and is open ended at the other end. A network analyzer simultaneously measures the S_{11} (the impedance seen by the contact probe) and the S_{21} (the transfer from the contact probe to the E-field probe). The measurement results are shown in Fig. 6.16. It can be observed from the figure that the probe intrusion is not only a matter of height but also horizontal location dependent. Specifically, the impedance of the open-ended CPW line (S_{11}) is significantly perturbed when the E-field probe is 10 μm above the open termination.

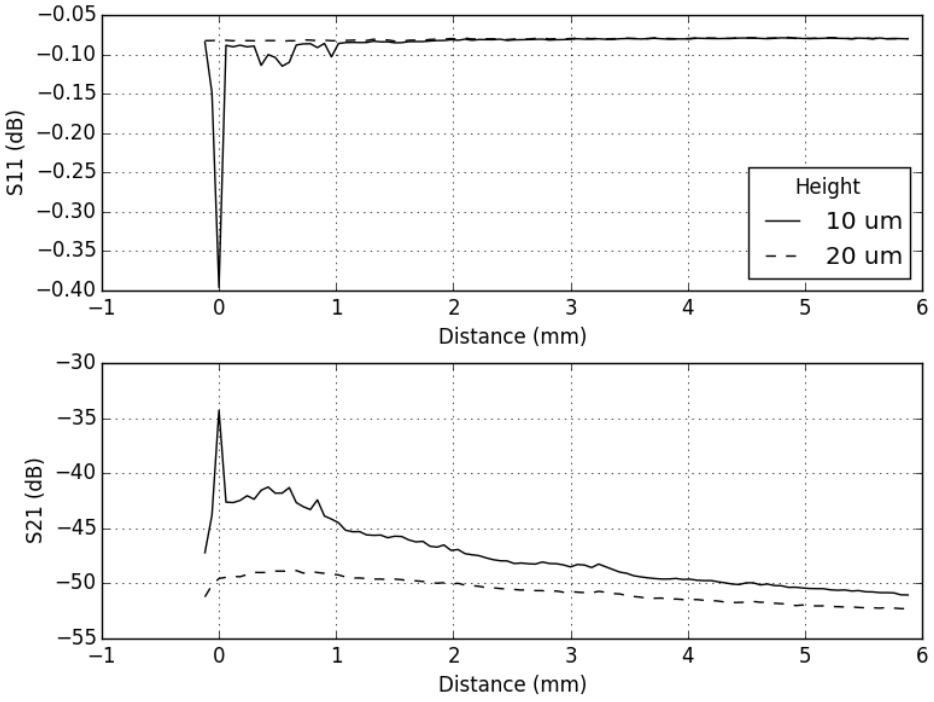
This result can be understood as the source loading effect of a voltage measurement. The E-field probe can be considered as a high-impedance voltage probe in parallel to the DUT for voltage measurement. If the DUT also has a high impedance that is comparable to the probe impedance, the voltage probe would load the DUT. In the experiment in Fig. 6.16, increasing the vertical probe-DUT distance increases the impedance of the E-field probe, whereas increasing the horizontal probe-DUT distance reduces the impedance of the DUT. Either way reduces the probe intrusion.

This result is further used to estimate the probe intrusion to the GaN device. The intrinsic transistors on the die are ideally speaking current sources, i.e. they have high drain-to-source impedances. But under the normal operating condition, the intrinsic transistors are matched to a loading condition dictated by their voltage and current capabilities. As will be shown later, the impedance at each transistor finger (at 2 GHz fundamental) is about 300 Ω. The same impedance exists on the CPW line about 3.6 mm from the open termination. As shown in Fig. 6.16 (a), even at 10 μm height, probe intrusion is not observable at this impedance level.

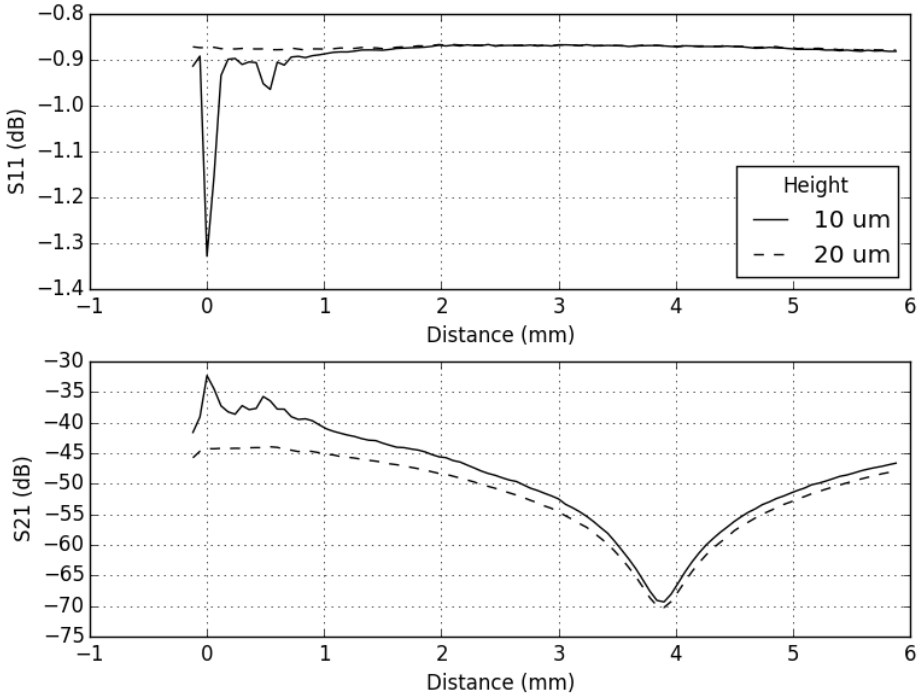
6.7.3. Distributed Effects in GaN DUT

E-field measurement

The GaN device is biased at 330 mA quiescent drain current and 50 V drain voltage. It is driven to compression by a 1-kHz-rate, 10%-duty-cycle pulse-modulated RF signal at 2 GHz. Its fundamental loading impedance is tuned to 4.2+2.2j Ω at the device package plane, close to the maximum efficiency



(a) At 2 GHz.



(b) At 8 GHz.

Figure 6.16: E-field probe scanning along an open-ended CPW line at various locations. The S_{11} monitored by a contact probe and the S_{21} measured as the contact probe to E-field probe transfer are plotted versus the horizontal distance between the E-field probe and the open termination.

Table 6.1: Operating conditions and loading impedances at fundamental and 2nd harmonic for the simulation and measurement of distributed effects.

Biasing drain voltage	50 V	
Quiescent drain current	330 mA	
Flange temperature	20 Celsius	
Frequency	2 GHz (fund.)	4 GHz (HM2)
Load impedance (Ω)	4.2+2.2j	11.3+19.8j

operation. The 2nd harmonic loading condition 11.3+19.8j Ω is only monitored but not controlled. During the whole measurement, the DUT is water-cooled constantly to 20 Celsius heat-sink temperature. These operating conditions are summarized in Table 6.1.

The E-field probe tip keeps a 15-μm height above the top metal layer and scans across the energized power die in 10-μm horizontal steps. The raw output from the E-field probe (measured by the VNA) is shown in Fig. 6.17. It can be observed that the measured electric field has interleaved peaks and valleys 70 μm apart, corresponding to the interleaved drain and source fingers on the power die. However, a more dominant curvature (high in the middle and low at the two edges) prevent a straightforward voltage interpretation. The curvature indicates stronger E-field in the middle of the power die since the probe in a middle location couples to more fingers. This coupling variation can be compensated by a baseline reading, i.e. a second scan 65 μm above the top metal layer. As shown in Fig. 6.17, the finger details are missing in this probe altitude but the curvature from uneven coupling remains. The difference of the electric field at the two heights suppresses the non-dominant probe coupling (off diagonal elements in (6.4)) and enhances the finger resolution, as explained in Fig. 6.11 in Section 6.5. From the differential readout curve in Fig. 6.17, in total 30 peaks are clearly observed, indicating 30 drain finger locations.

Post-processing for in-circuit voltages and currents

The peaks of the differential measurement are taken as the relative E-fields $E_{1,2,\ldots,N}$ in (6.6). The output voltage v_0 and current i_0 are measured conventionally by an NVNA at the fixture connector and deembedded to the package reference plane. Once the Y-parameters $[Y]$ are known, all these quantities are substituted into (6.6) to solve for the proportional factor t, which is consequently substituted into (6.5) to calculate the absolute finger voltages. After that, the current can be directly solved from (6.3). The specific DUT used in this experiment has every 3 fingers shorted at the drain to form a unit cell (see Fig. 6.1). This arrangement would yield an ill-posed Y-matrix. In other words, every 3-row group, i.e. row

$$3n+1, 3n+2, 3n+3, (n = 0, 1, \cdots, 9), \tag{6.7}$$

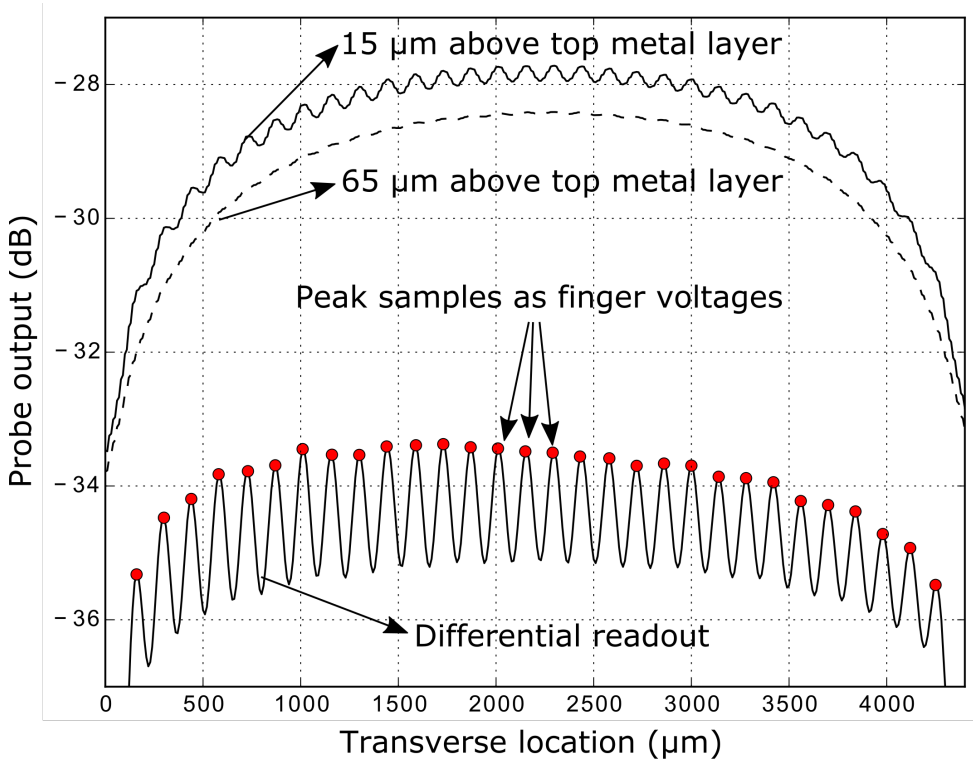
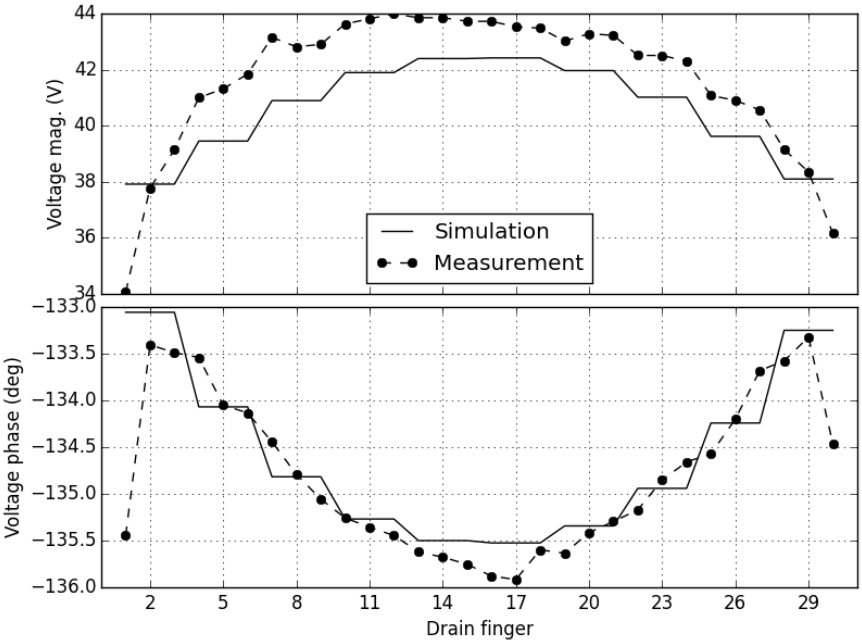


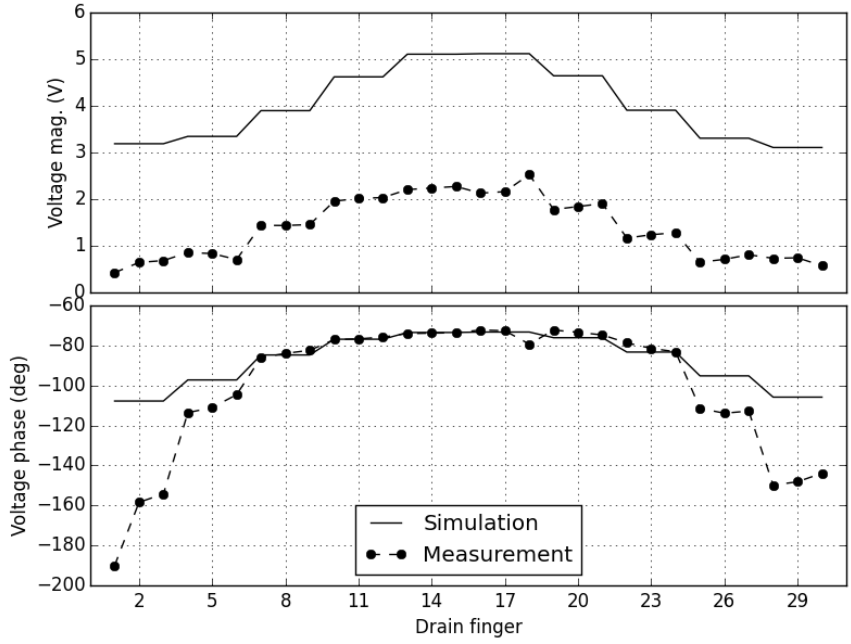
Figure 6.17: Electric probe output at 15 and 65 μm above the top metal layer, scanned across the power die in 10-μm steps. Their difference enhances the resolution of interleaved drain and source fingers. The peaks of the differential output are taken as the finger voltages.

in the Y-matrix in (6.3) yields 3 almost linearly dependent equations. In order to solve the ill-posed problem, we further assume an even current distribution across every 3 fingers in a cell, effectively averaging the currents for every 3 rows in (6.7) to reach the end results. A set of 10 current values is then derived from the Y-matrix computed by the 3D EM simulation of the structure depicted in Fig. 6.3. Doing so, each finger current shown below is actually one-third of the current flowing through the corresponding bondwires from its located cell. To gain more insight, the voltage and current products and ratios are also calculated, yielding RF output power and loading impedances across fingers.

From the post-processing, the deduced distributions of voltage, current, loading impedance and RF output power across fingers are plotted in Fig. 6.18, 6.19, and 6.20 and 6.21, respectively. Each figure has two subfigures ((a) and (b)) for the fundamental frequency (2 GHz) and the 2nd harmonic (4 GHz), respectively. Within each subfigure, complex quantities, i.e. voltages, currents and impedances are plotted in their RMS magnitude and phase. All post-processed measurement results are compared with their corresponding

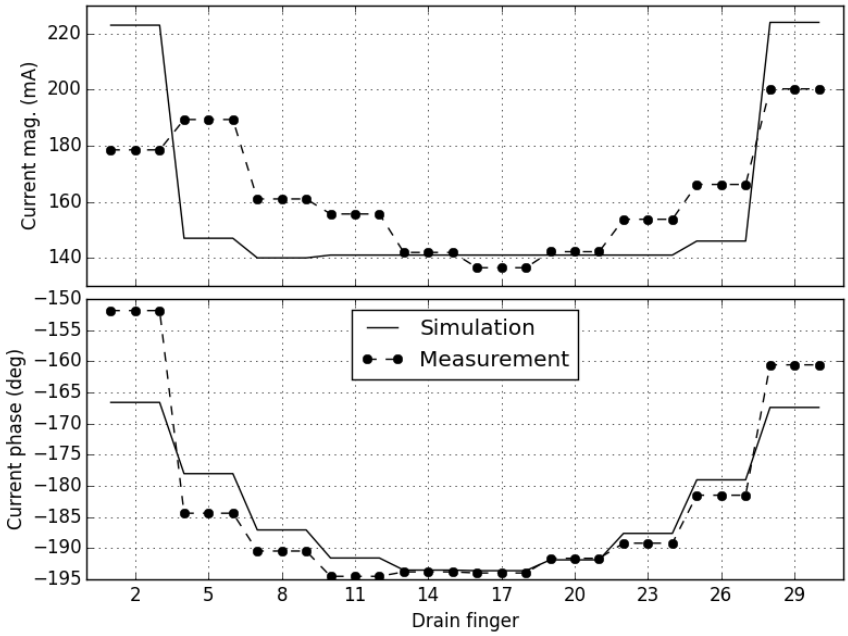


(a) At 2 GHz (fundamental)

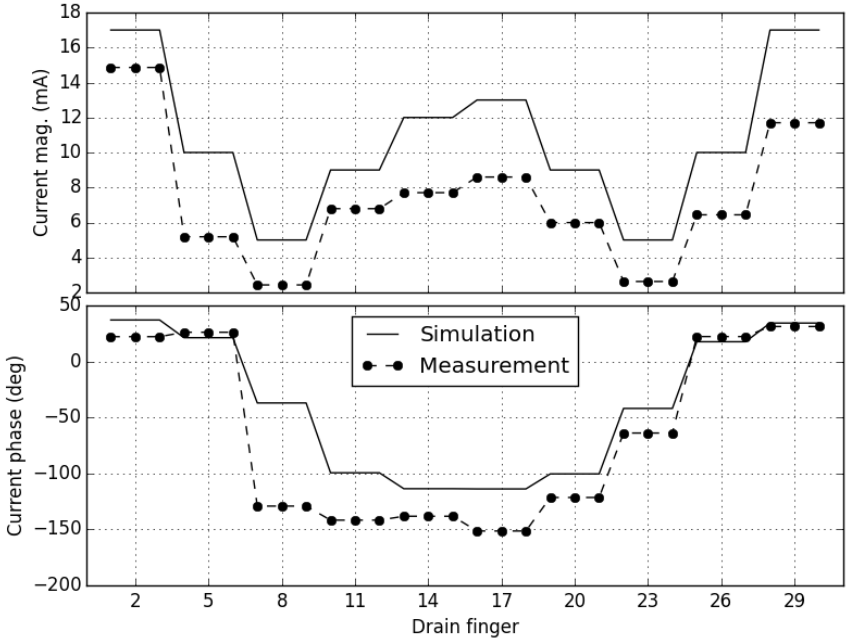


(b) At 4 GHz (2nd harmonic)

Figure 6.18: Voltage distribution across fingers plotted in magnitude (RMS) and phase. Measurement is compared with the simulation result of the independently developed distributed device model.

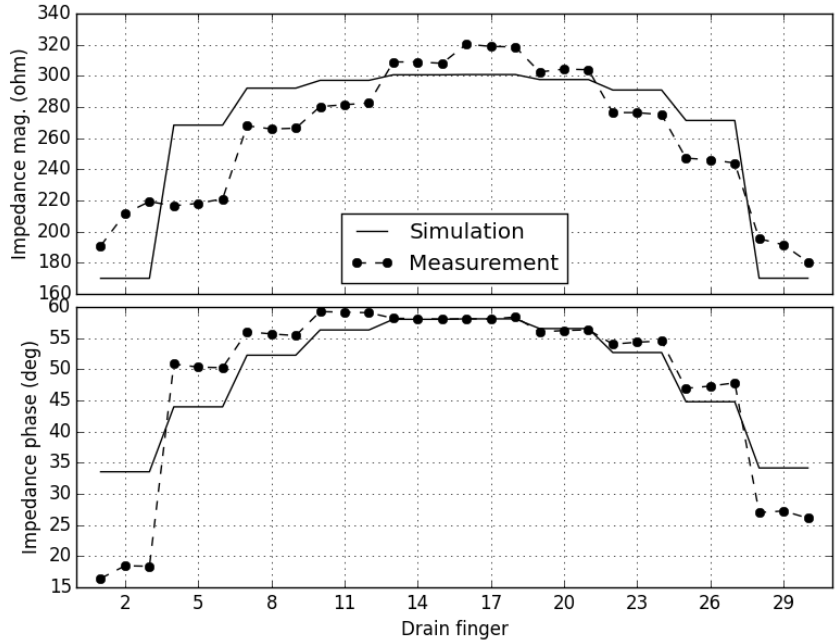


(a) At 2 GHz (fundamental)

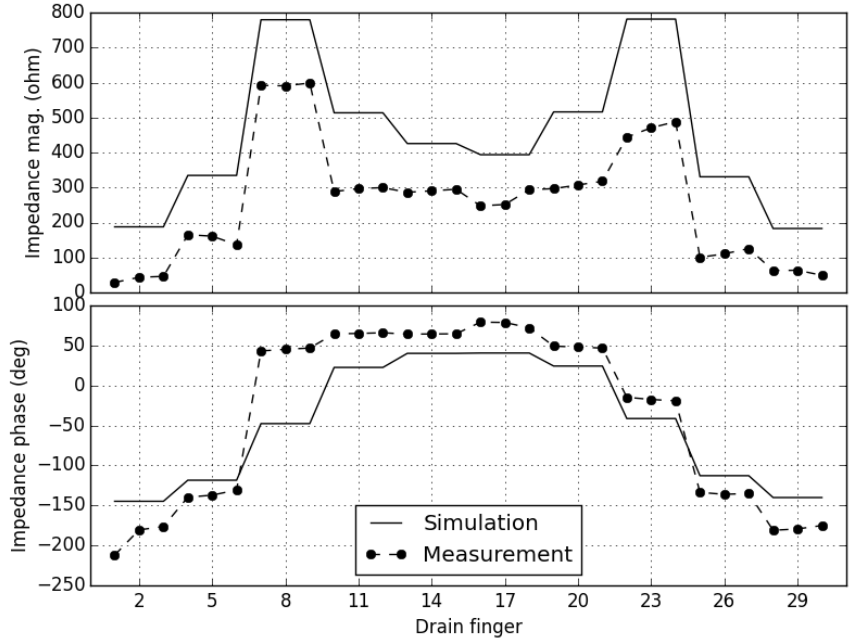


(b) At 4 GHz (2nd harmonic)

Figure 6.19: Current distribution across fingers plotted in magnitude (RMS) and phase. Measurement is compared with the simulation result of the independently developed distributed device model.

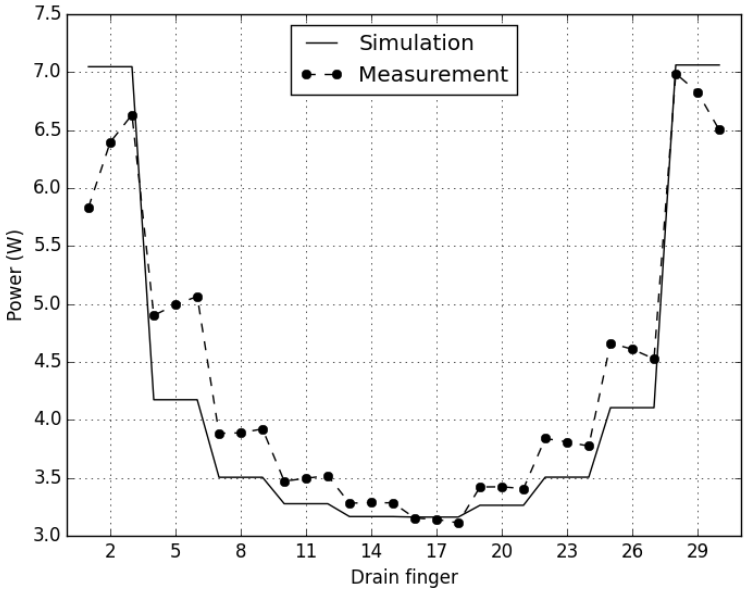


(a) At 2 GHz (fundamental)

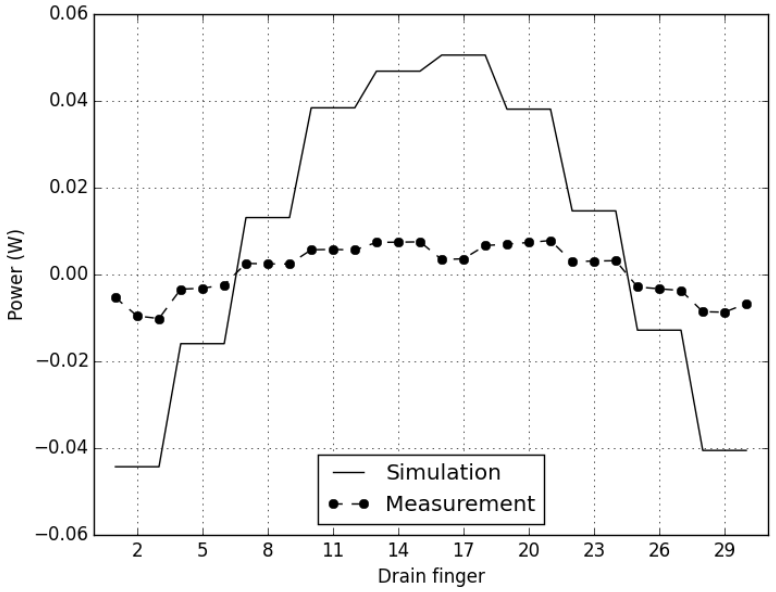


(b) At 4 GHz (2nd harmonic)

Figure 6.20: Loading impedance distribution across fingers plotted in magnitude and phase. Measurement is compared with the simulation result of the independently developed distributed device model.



(a) At 2 GHz (fundamental)



(b) At 4 GHz (2nd harmonic)

Figure 6.21: RF output power distribution across fingers. Measurement is compared with the simulation result of the independently developed distributed device model.

simulation results, obtained in the way described in Section 6.3.

Fig. 6.18 shows that the voltage magnitude and phase distributions are uneven along the array of cells and represents an experimental verification of the non-uniform distribution of voltage across fingers. The agreement between simulation and measurement is evident at fundamental (Fig. 6.18 (a)) for both the voltage magnitude and phase distribution. However, at the 2nd harmonic, (Fig. 6.18 (b)), the simulation clearly overestimates the measured voltage.

From Fig. 6.19 (a), we observe that the outer cells outputs to the drain lead more current than the middle ones at the fundamental frequency. This current crowding at the edges can be attributed, at least partially, to the skin / proximity effect caused by mutually coupled bondwires. At the 2nd harmonic frequency, (Fig. 6.19 (b)), a distinctive 'W' shape current magnitude distribution is predicted by the model and verified by the measurement. A general agreement between simulation and measurement can be observed for both magnitude and phase at both the fundamental and the 2nd harmonic.

In Fig. 6.20, simulation agrees with measurement for both loading-impedance magnitude and phase at both frequencies, although the agreement is again better at the fundamental frequency (Fig. 6.20 (a)). At the 2nd harmonic, (Fig. 6.20 (b)), a distinctive 'M' shape impedance magnitude distribution is observed, a likely consequence of the current distribution from Fig. 6.19 (b).

The RF output power distribution at fundamental (shown in Fig. 6.21 (a)) has a distinctive 'U' shape, which should be a direct consequence of the uneven current distribution. This finding agrees with results reported in [3]. The agreement between simulation and measurement at fundamental is good. At the 2nd harmonic (shown in Fig. 6.21 (b)), the simulation grossly overestimates the power, a likely consequence of the voltage discrepancy already observed.

It is worth noticing that, because of the way each finger current is calculated, the quantity in Fig. 6.21 represents the RF power propagating through the bond-wires towards the drain lead. Due to the lower effective inductances seen by the outer cells, yielding somewhat lower loading impedances, it is expected that these outer cells provide to the lead more output power than the center ones. Furthermore, since the loading conditions vary over the device, also the individual efficiencies of the cells will vary. Correspondingly, the simulation indicates that the outer cells can release their dissipated energy most effectively, since they are less surrounded by heat generating neighboring cells. This impacts the temperature distribution the most, yielding the rather typical bell shaped temperature profile. It is this ambiguous relationship between temperature- and RF power-distribution, that demonstrates the advantage of the proposed electrically direct characterization approach over conventional thermography based approaches.

Error analysis

Overall, the agreements between simulations and measurements at the fundamental frequency, as shown in Fig. 6.18-6.21 (a), have validated the distributed

multi-physics model detailed in Section 6.3 with respect to its predictability to distributed effects. However, the disagreements still present between measurement and simulation traces require a more in-depth discussion which is summarized in the following points:

1. The discrepancies (mostly in magnitude) at the second harmonic frequency (Fig. 6.18-6.21 (b)) indicate that the model in general shows more 2nd order distortion than the actual measurement based data. In checking the root cause of this phenomena, first the linearity of the VNA mixer down-conversion itself has been verified and found to be sufficient for the conducted experiments. Secondly, when considering the distributed device model behavior in more detail, it was found that the simulation model also tends to predict a more abrupt (fundamental) gain compression versus power than the actual measurement data (Fig. 6.6). Since the 2nd harmonic generation by a transistor measured around its compression point tends to increase with the abruptness of this compression, an over prediction of this 2nd harmonic by this transistor model can be indeed somewhat expected. This suggests that there are still some improvements to make in accurately describing the non-linear effects within the transistor model. Since these non-linear effects strongly depend on their (distributed) fundamental and harmonic loading conditions, such an activity can, in our view, strongly benefit from the proposed characterization work in this paper, which allows a straightforward comparison at the individual cell level of a (large) power device.

2. The measured voltage variations shown in Fig. 6.18 (a) within every 3-finger cell group, especially for the two fringe fingers at the sides, are unlikely a physical effect, considering every 3 fingers in a cell are short-circuited by a bond-pad. Whereas some of these minor variations may be attributed to random probe-DUT distance variations caused by mechanical instabilities, the largest variations at the two fringe fingers at the sides are clearly systematic errors. Since all the other fingers have both a left- and a right-hand neighboring finger except the two fringe ones, the systematic errors suggest that the E-field probe still has certain amount of residue coupling to neighboring fingers. A possible improvement is to further enhance the spatial resolution of the probe, by means of e.g. a sharper probe tip or a shorter probe-DUT distance.

3. Considering that the DUT is fabricated to be symmetrical with strict engineering tolerances, any minor asymmetry observed in Fig. 6.18-6.21 is more likely caused by measurement inaccuracy rather than a physical reality. Likely causes of this error are the imperfect planarization of the probe w.r.t. the DUT (note that there is also a slight asymmetry in Fig. 6.17) or an uneven thermal expansion of the fixture as explained in the end of Section 6.6, which makes the probe-DUT distance and their coupling to

vary along the die. In light of this, more sophisticated probe height control, such as closed-loop systems, or in-situ calibration techniques [30] are attractive future work directions.

6.7.4. Finger Damage Detection

Near-field measurement not only enables the validation of distributed device models, but also detects device defects (e.g. parasitic bipolar snap-back) in reality that cannot be predicted by any simulation model. For a demonstration of the potential of the proposed technique in defect detection, an intentional finger damage is made by laser cutting. As shown in Fig. 6.22 (a), the laser cuts on the top metal layer the 3rd drain finger of the 5th cell from the left. In effect, 800 μm wide gate periphery or 3% of the device capability is disabled.

The device is put to the same testing conditions as before. A near-field probe scan yields the result in Fig. 6.22 (b). The 30 drain fingers can be identified from the differential probe output. The finger damage is clearly identified.

6.8. Conclusion

This work presents an improved non-intrusive near-field probing technique for the characterization of distributed effects in a high-power GaN HEMT. This technique applies the NSMM PSD method to measure directly the E-field induced by energized transistor fingers. The flat semiconductor surface further permits close probe-DUT proximity. Consequently, more constant probe-DUT coupling as well as more localized field data can be obtained. The proposed technique experimentally quantifies voltages at individual fingers 70 μm apart within an operating GaN HEMT. The obtained voltage and current distributions validate an independently developed multi-physics distributed device model of the same device. The added value of having direct measurement insight in the finger voltage distribution without any pre-assumptions on the active device itself has been further demonstrated by identifying a device defect at the finger level, which is enforced by laser cutting.

Acknowledgment

The authors would like to acknowledge their colleagues in Ampleon Netherlands: Michel de Langen for designing the bondwire calibration kits and Rik Jos for many inspiring discussions.

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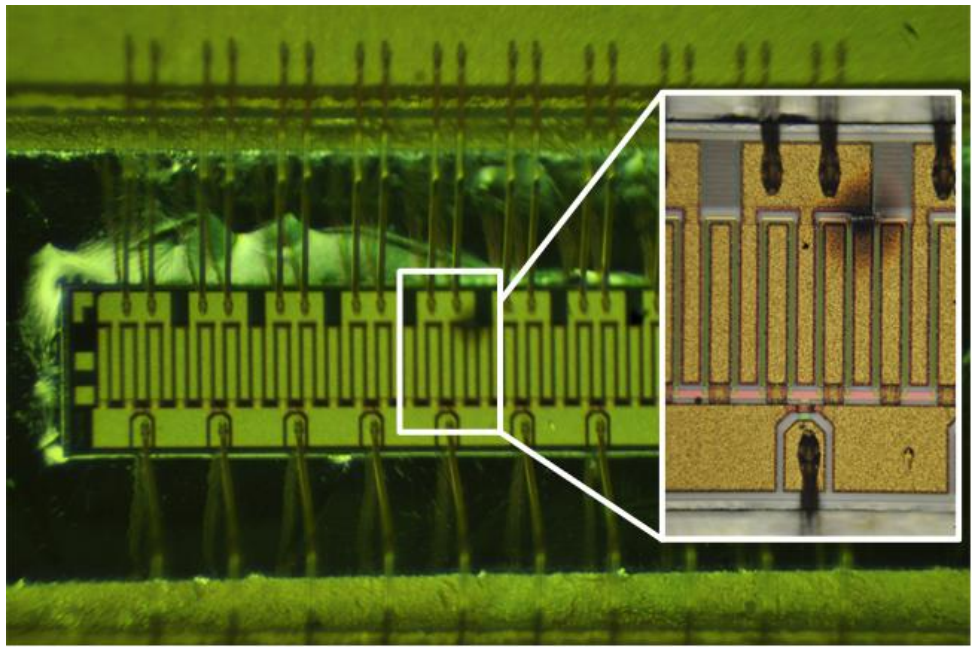
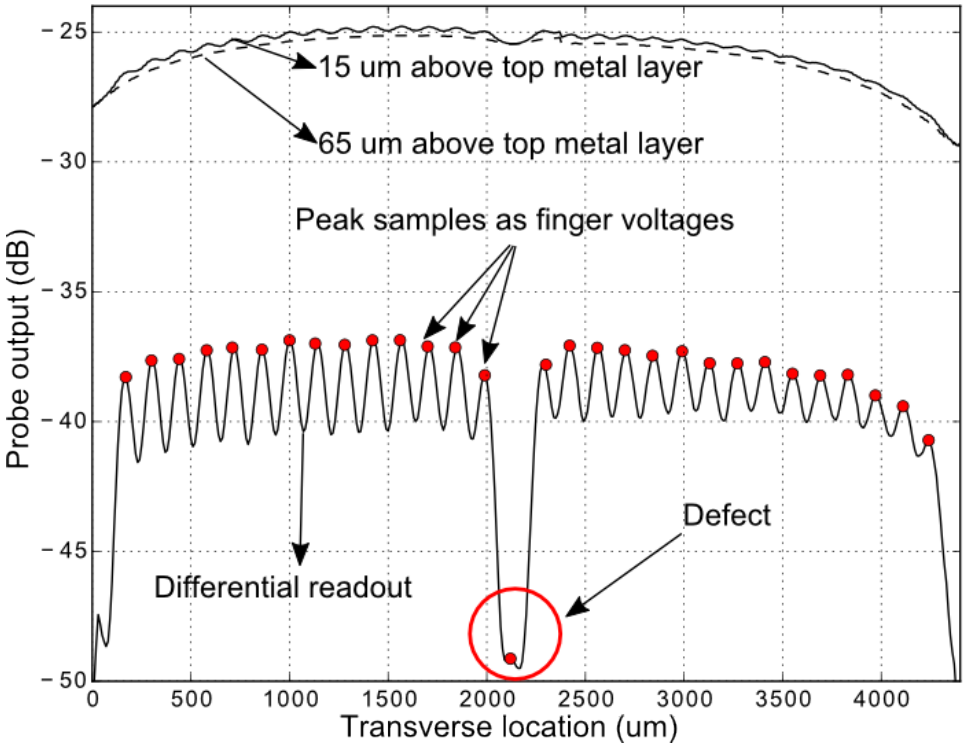


(a)



(b)

Figure 6.22: Artificial finger damage: the 3rd drain finger of the 5th cell from the left is cut by laser. Microscope image (a) is compared to the near-field measurement result (b). Defect is clearly identified.

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7

A Package-Integratable Six-Port Reflectometer for Power Devices

[1]High frequency power devices require specific loading conditions to provide maximum output power, operate efficiently and avoid self-destruction. In applications with unknown or time varying loading conditions it is therefore desirable to monitor, in-situ, the loading conditions offered to the PA. This work proposes an ultra-compact six-port package-integratable reflectometer. The resulting structure is implemented on a 9.4- by 4-mm substrate that can fit into an SOT1110A package. The performance of the realized hardware is validated by an active load-pull system, which synthesizes impedances covering the entire Smith chart.

7.1. Introduction

High-power RF devices can only be energy efficient and failure free in a restricted range of loading conditions. In communication applications like base stations, these loading conditions are generally identified by load-pull measurements first and later implemented by impedance matching networks. However, in emerging applications like solid-state RF heating (e.g. microwave ovens), loading conditions can be totally unknown or vastly varying. If undetected, these varying loading conditions may degrade gain, output power and efficiency of the power devices, and possibly cause instability, device degradation, or more

[1]Parts of this chapter have been published in Microwave Symposium Digest (IMS), 2014 IEEE MTT-S International [1]. This work has been carried out in the context of the TUDelft master project of Razvan Venter, who was mentored by the author of this thesis, Rui Hou, together with Koen Buisman.

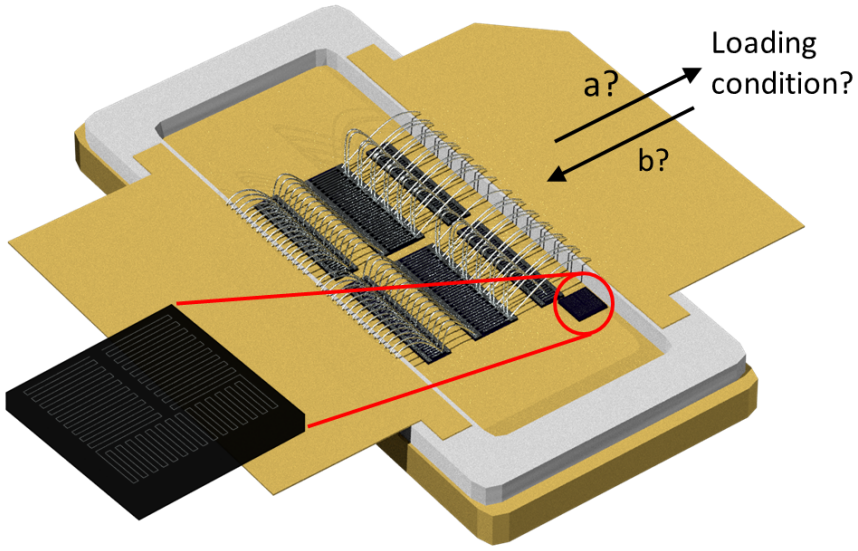


Figure 7.1: Application example: a compact reflectometer integrated in a ceramic-air power transistor package. The goal is to monitor the instantaneous loading condition of power transistors in real-time.

severely, immediate failure due to voltage or thermal breakdown. Therefore, measuring the in-situ reflection coefficients seen by the power device (e.g. by inserting directional couplers) is crucial to promote device integrity and system performance in these emerging applications.

Conventional vector measurement at the coupler's arms requires mixers and local oscillators, which can be complex and costly to integrate in the device. In addition, they require knowledge on the actual operating frequency and might cause spectral pollution due to leakage of the down-conversion LO signal. On the other hand, simpler and cheaper methods like a directional coupler with power meters typically ignore the phase information and introduce inaccuracies due to finite coupler directivity.

This work is based on the six-port reflectometer technique [2]. When optimally implemented, this technique can provide very compact, accurate, low-cost and low-complexity power device mismatch-detection. Such attributes make this technique ideal for application in high volume consumer products like solid-state microwave ovens. To achieve this, the six-port network in this work is designed as a novel half-wavelength ring, which is weakly coupled to the bondwires connecting the power-transistor die with the (drain) package-lead, as shown in Fig. 7.1. This provides a straightforward and affordable monitoring of the output loading conditions right at the package boundary. Validation of

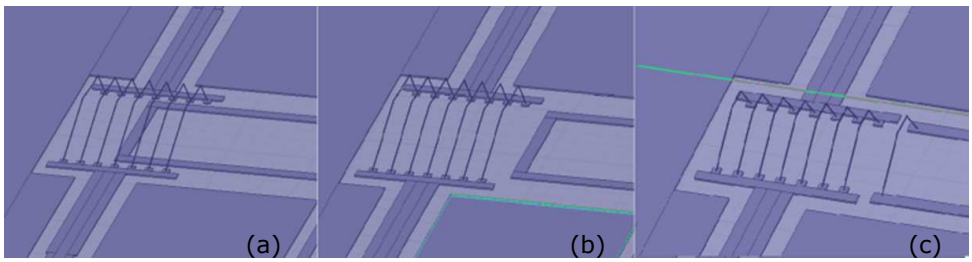


Figure 7.2: Bondwire coupling structures to be studied. Microstrip placed (a) underneath and (b) besides to the bondwire array. (c) Extra bondwire placed next to the bondwire array.

Structure type	Directivity	Coupling
Loop under bondwire (HFSS)	12 dB	-25 dB
Loop beside bondwire (HFSS)	15 dB	-30 dB
(Measurement)	13.9 dB	-29 dB
Loop as an extra bondwire (HFSS)	10 dB	-20 dB

Table 7.1: Simulation and measurement results for the 3 candidate coupling structures at 2.45 GHz.

the proposed method is performed using an active load-pull system.

7.2. Design and Implementation

Distinguishing from the abundant six-port literature [3], the proposed design targets power devices and aims for very low-insertion losses, thus weak coupling (e.g. -30 dB). Furthermore, package integration with a power device implies a very short distance compared to the wavelength, from drain terminal (port 1) to the package lead (port 2), to couple out the monitoring signals. Because of these constrains, all the 6x6 S-parameters should preferably be near 0 in magnitude, except S_{21} and S_{12}, which should be very close to 1 in magnitude and close to zero in phase. Due to these special requirements, the proposed six-port implementation consists of two parts, namely a low-loss directional coupler (to minimize power loss and maximize directivity in the short through path) and an interferometer (to separate incident and reflected power waves from their interfered standing-wave pattern by amplitude-only detection at the appropriate locations on a transmission line structure).

7.2.1. Bondwire based directional coupler

Conventional LDMOS power transistors make use of an array of parallel bondwires to connect their drains at the power bar to the package lead (Fig. 7.1). In view of the aimed load detection, these bondwires can be conveniently used as the through path of a directional coupler. The objective here is to separate the incident and reflected power waves propagating along the bondwires with high directivity without affecting the drain efficiency of the power device (low

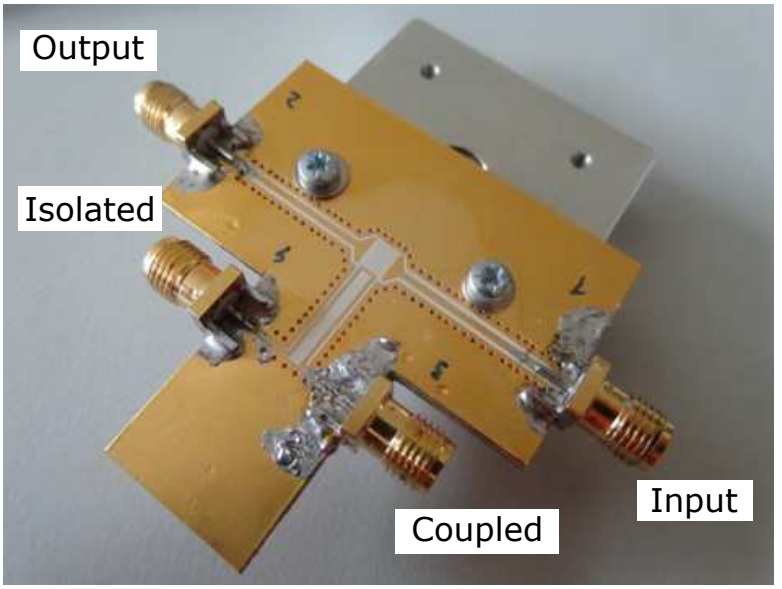


Figure 7.3: Implementation of bondwire coupling structure from Fig. 7.2 (b).

coupling). To explore the design space of the bondwire based coupler, several implementation options (Fig. 7.2) have been studied:

- a short microstrip directly under the bondwire array
- a short microstrip to the side of the bondwire array
- an extra bondwire to the side of the bondwire array

An electromagnetic simulator, Ansys HFSS, is used to calculate the directivity and coupling factors of the various topologies. Physical prototypes have been assembled to verify the HFSS simulations on 2.54 mm thick Rogers 3006 substrates. The simulation results are listed in Table 7.1. It can be concluded from Table 7.1 that a short microstrip line placed next to the bondwire array (Fig. 7.2 (b)) yields in this set of experiments the highest directivity and the lowest coupling factor.

A hardware prototype of the optimal coupling structure is implemented and presented in Fig. 7.3. The measurement result is also listed in Table 7.1. The bondwire coupler prototype demonstrates 13.9 dB directivity and -29 dB coupling factor, only 1 dB away from HFSS simulation.

7.2.2. Interferometer

Incident and reflected waves on a transmission line interfere and yield a standing wave. Measuring these standing-wave voltages at a few locations along the

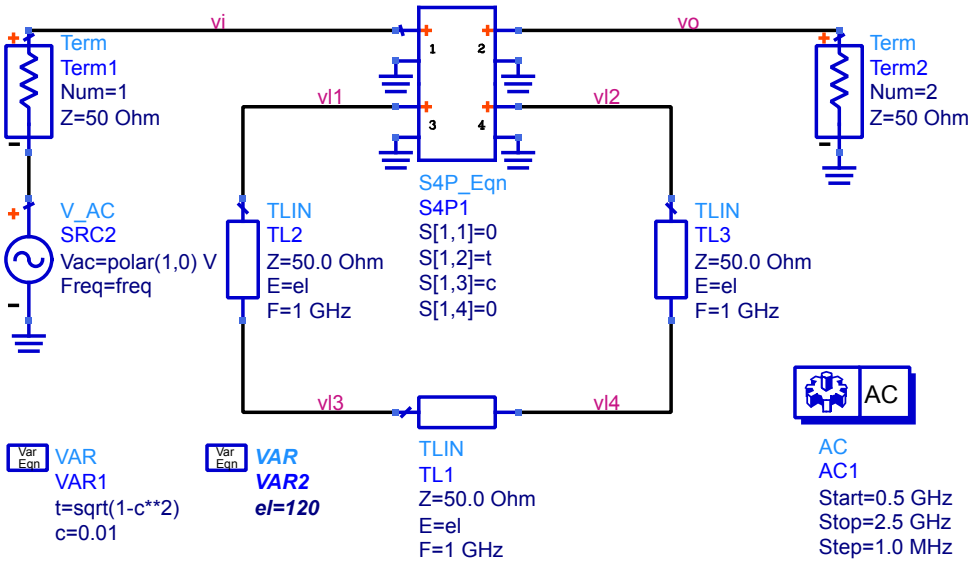


Figure 7.4: An ideal 40 dB bidirectional coupler with its 2 coupling arms closed in a loop.

transmission line can provide not only their relative magnitude but also their relative phase and thus the reflection coefficient in its vector form. The main advantage of this method is the requirement of only amplitude (envelope) detectors. In this work, we use this well known principle. However, its direct application on the through path (e.g. measuring 2.45 GHz waves on 2 mm long bondwires) would cover only a small fraction of the wavelength and as a consequence, yields an ill-posed problem. To avoid this difficulty and reach high detection accuracy, we choose to use bondwires only as a coupling mechanism and make use of an electrically larger loop, connecting the coupler arms to uphold the wave interference pattern as shown in Fig. 7.4.

In Fig. 7.4, an ideal bidirectional coupler with 40 dB coupling and infinite directivity feeds the coupled waves in opposite directions into a transmission line loop. The loop is 360 deg at 1 GHz. Voltage at 4 locations are plotted. From the simulation result, Fig. 7.5, it can be observed that when the loop is a integer wavelength long (at 1, 2 GHz, etc.), coupled waves constructively interfere with the circulating waves. In contrast, when the loop is half a wavelength long (at 0.5, 1.5, 2.5 GHz, etc.), the interference is destructive. This behavior is sometimes used in the implementation of pass- and stop-bands for microwave coupled-loop filters.

For comparison, in a half-wavelength transmission line terminated by a fully reflective load, waves interfere in *opposite* directions, yielding a standing wave. Cancellation happens only at *discrete* locations. In contrast, in a loop interferometer with half a wavelength, circulating waves interfere in the *same* direction. This cancellation happens at *every* location in the loop. The destructive inter-

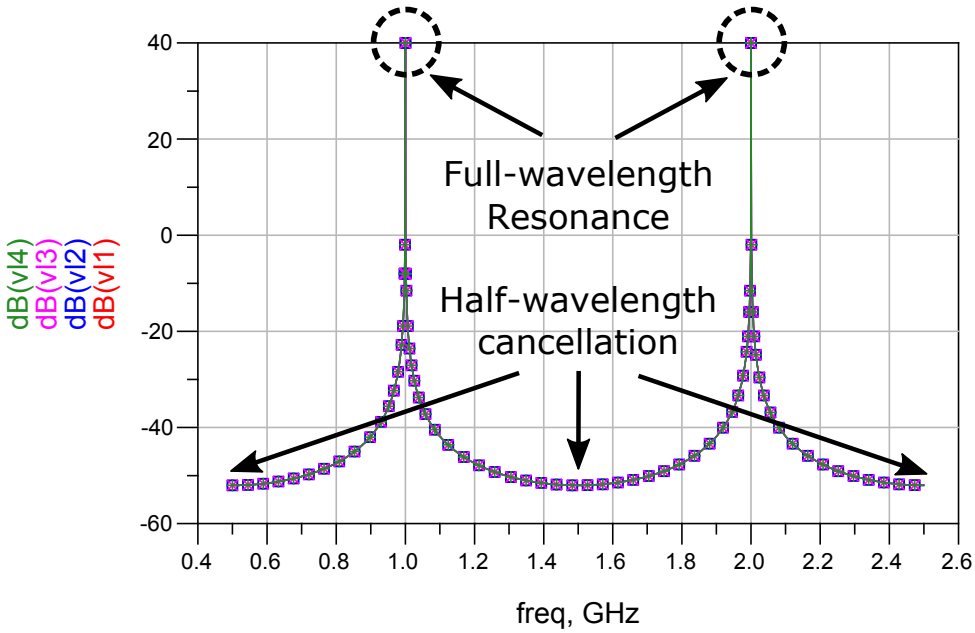


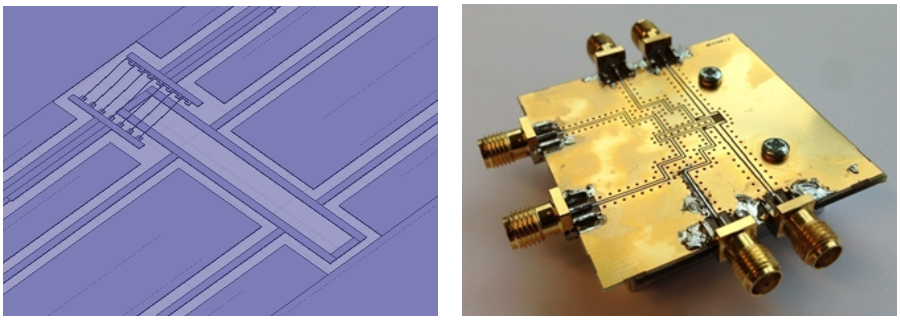
Figure 7.5: ADS simulation result showing loop resonance at integer wavelengths.

ference however do not yield a complete cancellation because a small portion of the wave, after traveling along the whole loop, gets coupled back to the main line. Thus coupling factor and loop loss also determines the quality factor of the loop resonator.

Resonant loop interferometer

When a closed loop is made a full wavelength long (or an integer multiple of wavelengths), traveling waves inside the closed loop can interfere constructively. Power will flow from the main thru path into the closed loop via the bidirectional coupler. As long as the input power is larger than the output power, energy accumulates in the loop, yielding resonance and accordingly enhanced voltages and currents for detection.

A resonant loop is beneficial to applications aiming for high sensitivity, but less suitable to the proposed application for the following reasons. First of all, in PA applications, an output signal with rich harmonic contents is quite common. In this scenario, if the loop is designed to have exactly a wavelength at the operating frequency of the PA, all its harmonics would also be in resonance and be amplified accordingly, yielding potentially a significant system error. Secondly, a high Q factor would boost the PA signal to an unnecessarily large level, potentially overdriving the power detectors in the detection loop out of their square-law operations. Thirdly, a high-Q resonance will make the signal level sensitive to frequency, demanding a receiver to have high dynamic range and



(a) (b)

Figure 7.6: HFSS simulation and hardware implementation of the half-wavelength non-resonant loop interferometer.

frequency range. Last but not least, in our application, the ISM 2.45 GHz band yields a full wavelength loop size that is difficult to integrate.

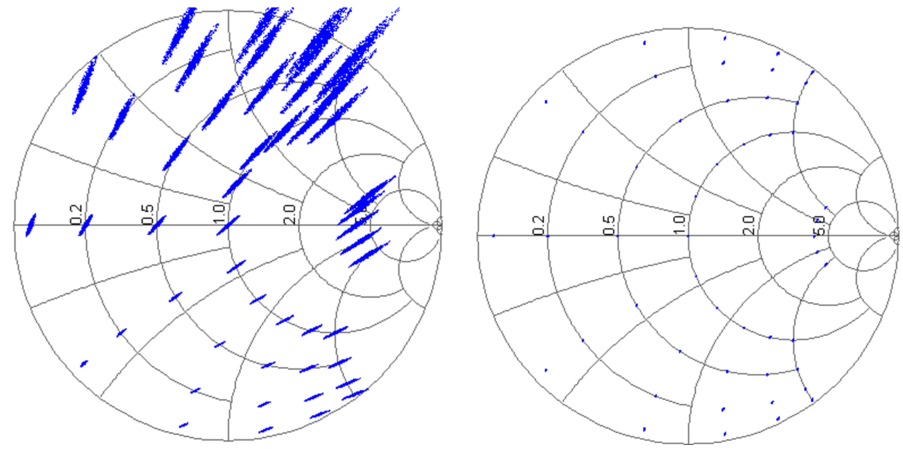
Non-resonant loop interferometer

If the resonance requirement is relaxed, loop size no longer need to be an exact integer of a wavelength, but only a fraction of a wavelength determined by detector separations. The lack of a clear resonance removes any voltage enhancement, but signal strength is less of an issue in high-power transistors. In the case of an optimal detector separation of 45° (as will be explained later), a 4-detector loop only need to be $\frac{3}{8}\lambda$ long. Compared to a full-wavelength loop, it would save more than 50% of the chip circumference.

Due to these foregoing considerations, a non-resonant $\lambda/2$ loop is used in the prototype design as shown in Fig. 7.6. By choosing a half-wavelength loop, a sufficient coverage of the standing-wave interference pattern (which is $\lambda/2$ periodic) is guaranteed, while being sufficiently compact to be compatible with package integration. The combined bondwire coupler and half-wavelength loop yields the low-loss ultra-compact six-port design, presented as an HFSS simulation model in Fig. 7.6 (a) and as the physical implementation in Fig. 7.6 (b).

Detector separation

In the proposed $\lambda/2$ loop detection approach, the distance between each two consecutive tapping positions is optimized to 45° at the design frequency, so that the impact of noise on the detection is reduced to a minimum. In order to verify this, Monte Carlo simulations are performed. First 1000 noisy data samples are created assuming a 50 dB detector signal to noise ratio (SNR) and applied to a non-optimal structure with only 10° of phase shift between the loop detection ports (Fig. 7.7(a)). Next the same experiment is repeated with the intended structure with the optimum 45° phase shift between the test ports



(a) (b)

Figure 7.7: Monte Carlo analysis: the impact of noise on the reflection coefficient detection for different loading points across the Smith Chart. Power detectors are 10° (a) and 45° (b) apart.

(Fig. 7.7(b)). It can be easily noted that the later (proposed implementation) reduces the impact of the noise.

7.2.3. Power detectors

Diode selection

For the sake of simplicity, compactness and low-cost, square-law diode detectors as shown in Fig. 7.8 are used for the 4 loop detection ports. For good sensitivity, low-barrier Schottky diodes with a large saturation current are frequently used as square-law detectors. The reason is explained in the following derivation.

The I-V relation of a diode

$$i = I_s\left(e^{\frac{v}{nV_T}} - 1\right)$$

can be expanded as a Taylor series at zero-bias

$$i = I_s\left[\frac{v}{nV_T} + \frac{\left(\frac{v}{nV_T}\right)^2}{2!} + \frac{\left(\frac{v}{nV_T}\right)^3}{3!} + \ldots\right], \tag{7.1}$$

where I_s is the saturation current, n the emission coefficient and $V_T = kT/q$ the thermal voltage.

The first term of 7.1 yield the small-signal resistance

$$R_D = \frac{nV_T}{I_s}. \tag{7.2}$$

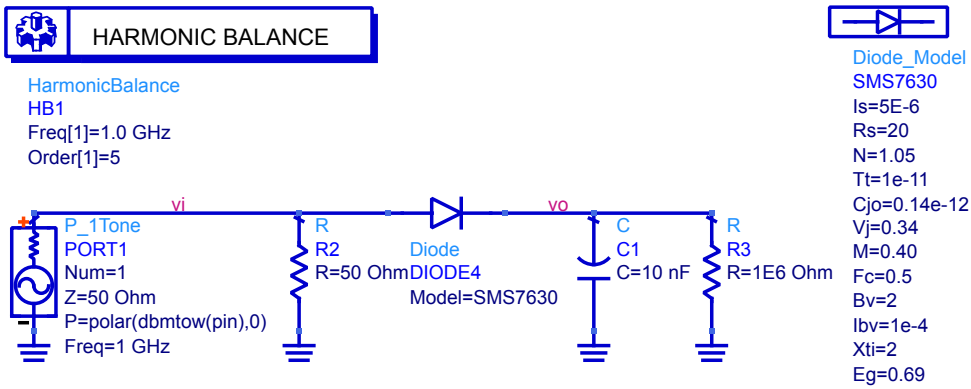


Figure 7.8: Square law detector schematic in ADS together with diode model for Skyworks SMS7830.

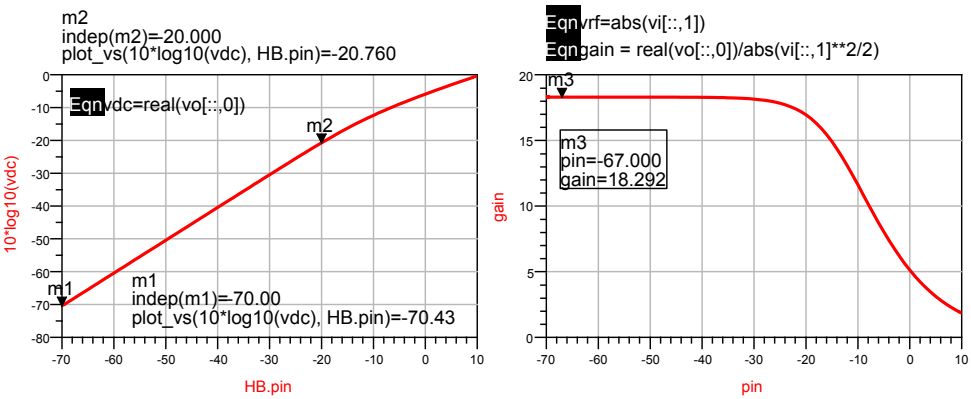


Figure 7.9: ADS simulation result: RF to DC conversion.

This resistance is temperature dependent. Furthermore, it is both the input resistance for an RF signal and the output resistance for the converted DC signal. For the sake of input matching, R_D should be high enough (>>50Ω) in order not to load the 50Ω parallel matching resistor. However, for the sake of power conversion, R_D should be low enough (<<Mohm) in order not to be overloaded by a practical DC readout. This trade-off is inherent for any passive converters.

Due to the consideration above, Skyworks SMS7630 diodes ($I_s = 5\mu A$) are selected for the square-law detectors. The small-signal resistance from 7.2 is around $5.5k\Omega$ at room temperature. The diode model and the detector schematic are plotted in Fig. 7.8.

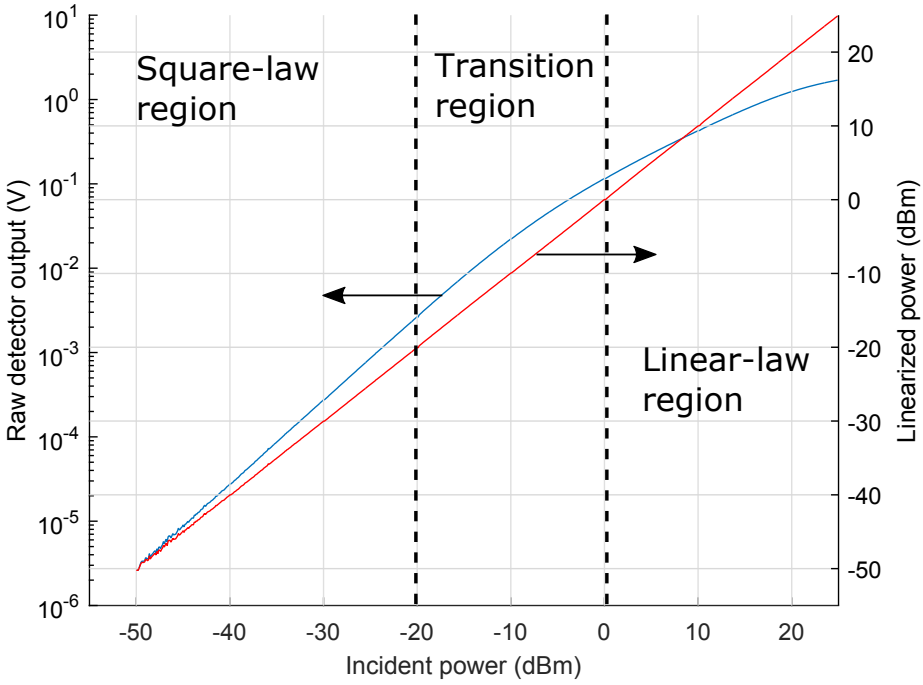


Figure 7.10: Measurement result: power detector output before and after linearization.

Functional simulation

The second-order term of 7.1 is the lowest order non-linearity to convert RF energy into DC. The conversion from RF to DC is

$$I_{DC} = \frac{I_s}{2\,(nV_T)^2} v_{rf}^2, \tag{7.3}$$

$$V_{DC} = I_{DC} R_D = \frac{v_{rf}^2}{2nV_T}. \tag{7.4}$$

It shows that the output DC voltage is proportional to the square of RF excitation, explaining the name square-law detector. The agreement between 7.4 and the diode model is verified by a harmonic balance simulation as shown in Fig. 7.9. Within the linear region of the detector (input power < -30 dBm), the simulated DC voltage is indeed proportional to RF power with a factor $1/2nV_T = 18.3$ at room temperature.

Measurement result

The aforementioned square-law power detector of Fig. 7.8 is fabricated and measured in an incident power sweep from -50 to +25 dBm, as shown in Fig.

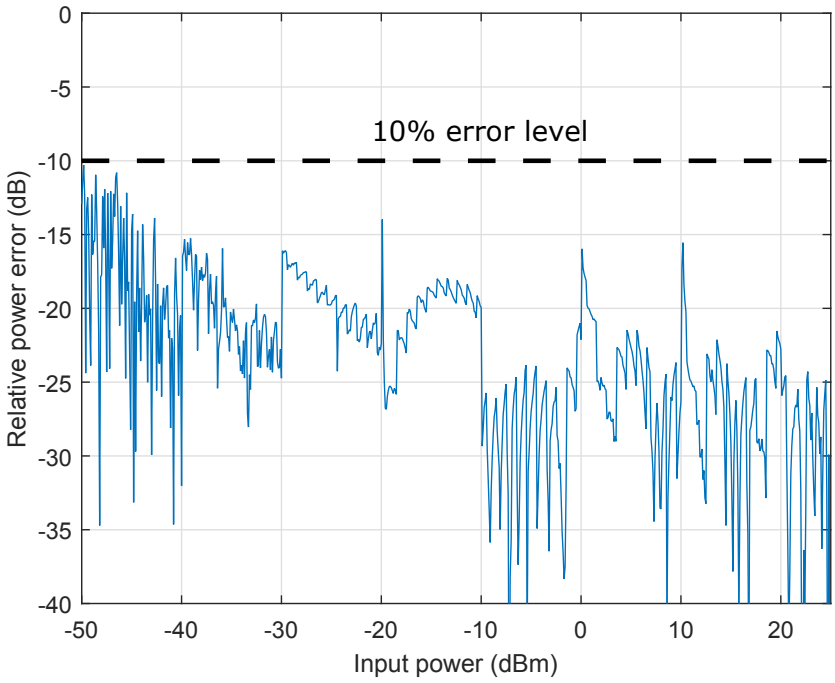
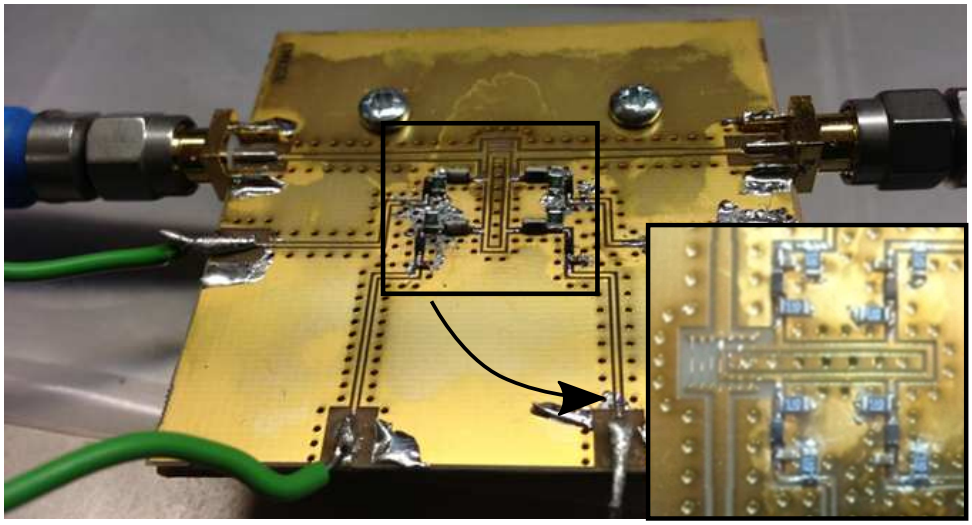


Figure 7.11: Power detector measurement error after linearization.

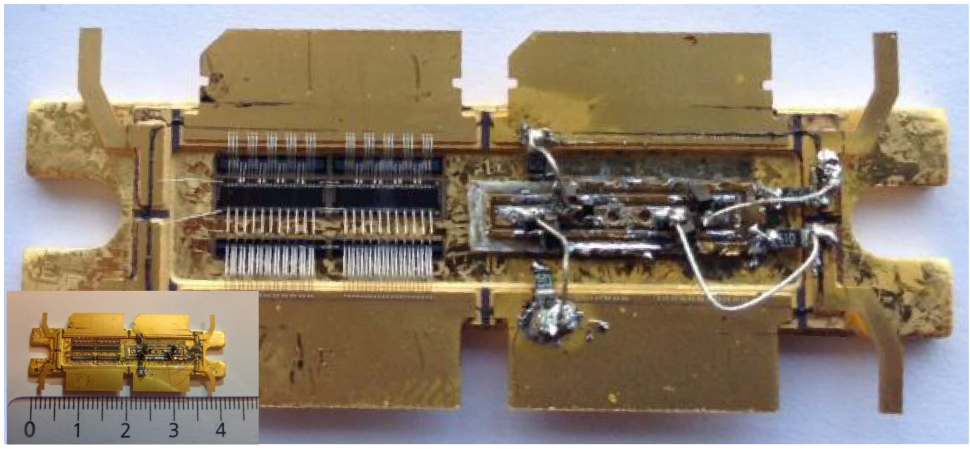
7.10. The intrinsic device non-linearity is clearly observed. In the low power region (when the incident power is below -20 dBm), the detector works as a square-law detector. In the high power region (Pin > 0 dBm), it becomes an envelope detector. Due to the necessity to operate the device beyond its square-law region (Pin > -20 dBm), the diode detector output need to be linearized [4]. The logarithmic curve of the raw detector voltage is fitted by a 12th order polynomial function. The curve-fitting result is then inverted to correct raw detector voltage outputs into linearized power reading. The linearized detector output is also shown in Fig. 7.10. Linearization error, referred to a calibrated power meter (Hewlett Packard E4419A) is plotted in Fig. 7.11. It could be observed that a total dynamic range of 75 dB is achieved by the linearized power detector with the worst-case relative root-mean-square (RMS) error below -10 dB (10%).

7.2.4. Prototype Implementation

The complete six-port reflectometer prototype, including the aforementioned bondwire coupler, ring interferometer and square-law detectors, is shown in Fig. 7.12 (a). This prototype is designed for the industrial, scientific and medical



(a)



(b)

Figure 7.12: Prototype implementation of the six-port reflectometer for testing (a) and package fitting (b), including the bondwire coupler, ring interferometer and the square-law power detectors.

(ISM) band centered at 2.45 GHz. The size of the functional part is only 9.4 by 4 mm (37.6 mm2), which is compact enough to fit into an SOT1110A power transistor package, as shown in Fig. 7.12 (b).

In this implementation, an additional resistive voltage divider (50:1) is inserted at each of the 4 detector ports. The benefits are 3 folds. It scales the signal to the square-law region of the diode, minimizes the power-dependent return loss from the diode and introduces dissipation to the 180° loop to avoid unlimited destructive interference.

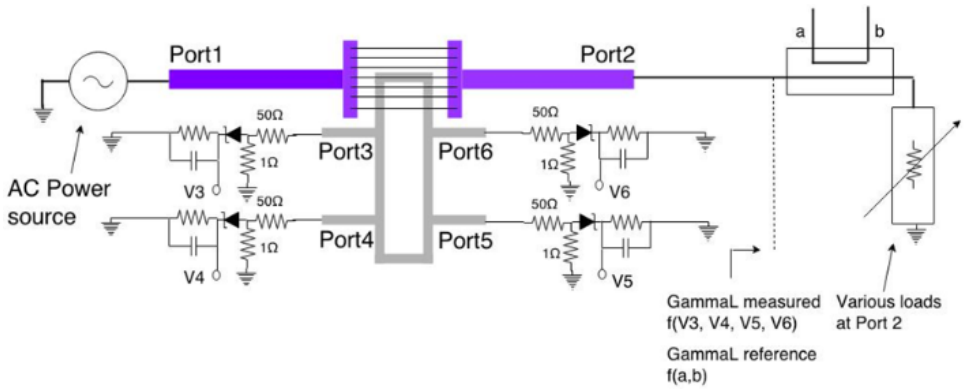


Figure 7.13: Measurement setup to validate the proposed six-port reflectometer. An active load-pull system is used both to synthesize loading conditions covering a Smith chart and to measure the provided reflection coefficients as references.

7.3. Experimental Results

The prototype shown in Fig. 7.12 (a) is validated in a measurement setup illustrated in Fig. 7.13. In this experiment, power is injected from connector port 1, passing through the bondwire array and flowing out of connector port 2. An active load-pull system generates various loading conditions at port 2 and reflect power back through the bondwire array. A tiny (-30 dB) portion of the incident and reflected power flowing through the bondwire array is coupled into the $\lambda/2$ interferometer loop in the counter-clockwise and clockwise directions, respectively. The circulating waves interfere inside the loop, creating a standing wave pattern. The 4 power detectors sense the standing wave in 4 fixed locations $\lambda/8$ apart, and convert the power into 4 DC voltages. The DC voltages are measured by a 4-way low-noise readout circuit.

The calibration of the compact reflectometer is performed in two different ways, treating the proposed design either as a conventional six-port measurement device or using an application specific calibration for microwave power amplifiers. The measurement results under these two calibration methods are reported accordingly.

7.3.1. Conventional Six-port calibration

Six-to-four port reduction

The proposed design can be used as a generic six-port reflectometer. The systematic error of the six-port interferometer is attributed to the 11 error terms and calibrated by 9 unknown loads (preferably evenly distributed close to the edge of the smith chart) and a standard short-open-load (SOL) calibration [5]. In total, 95 loads uniformly covering the whole Smith chart are synthesized by an active load-pull system and applied at port 2 of the six-port circuit. The DC voltages at the 4 detection ports (ports 3-6) are monitored by a 4-way low-noise

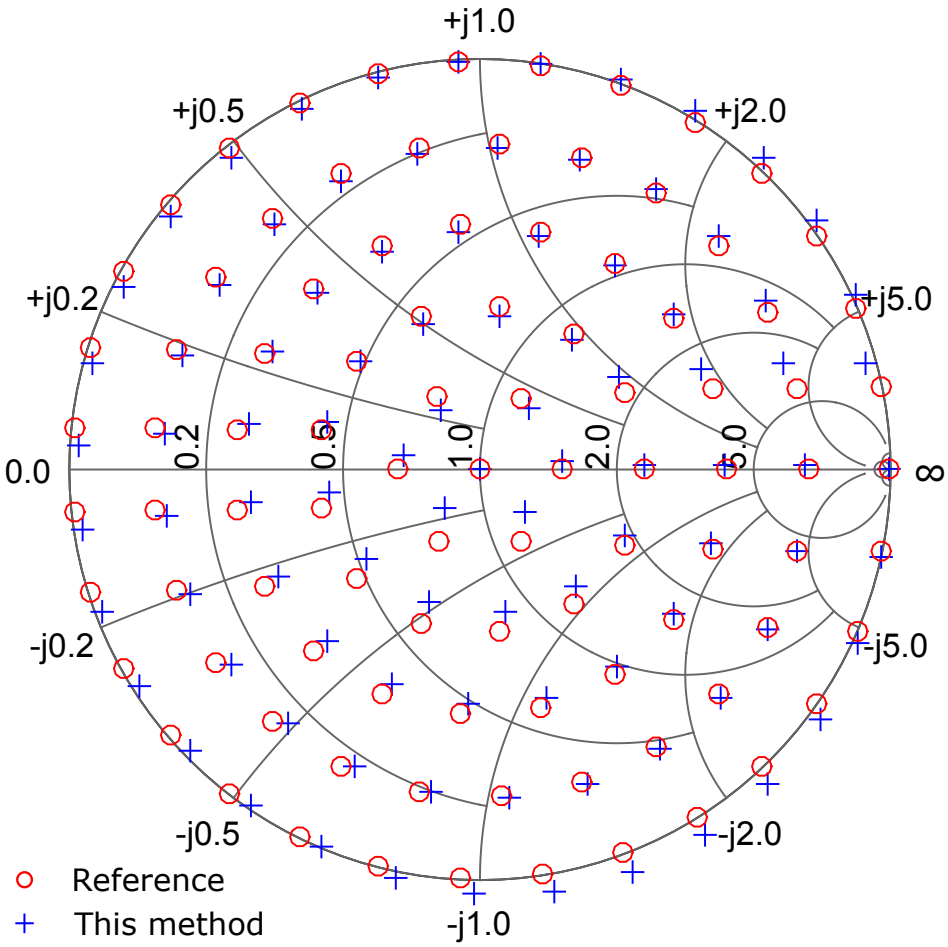


Figure 7.14: Measured reflection coefficients from the proposed six-port reflectometer using a standard six-port calibration method vs. references from the calibrated active load-pull setup.

readout circuit.

Calibrated result

The reflection coefficients calculated from the measured DC voltages are plotted in Fig. 7.14. Independent measurement results from the calibrated load-pull setup are also plotted as a reference. General agreement between the two is clearly observed. The measurement error in dB full-scale is plotted in Fig. 7.15, with a worst case below -20 dBFS.

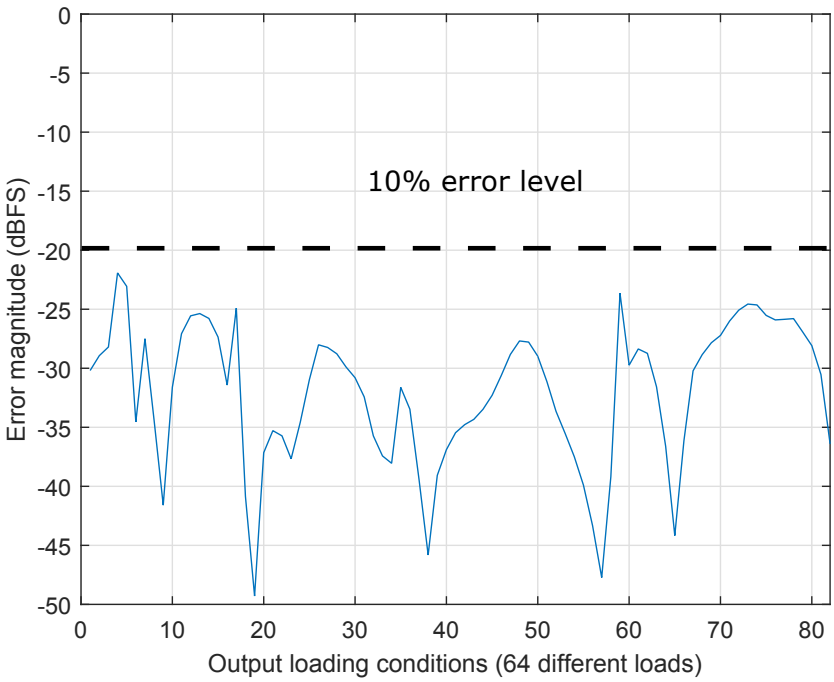


Figure 7.15: Error of measured reflection coefficients compared to reference values, in dB-full-scale. The x-axis represents the different test loads applied to port 2.

7.3.2. Application specific calibration

Power devices are commonly characterized in a load-pull setup. When the proposed compact reflectometer is integrated with such power transistors, the routine load-pull measurement permits a simpler calibration.

Since a load-pull setup provides calibrated loading conditions to the PA under test, these loading conditions, together with the six-port detector outputs can be framed into a look-up table. The six-port calibration and correction procedure in this case is simplified into a table construction and look up procedure. Consequently, the measurement accuracy in this case is determined by the repeatability of the reflectometer and the look-up table grid density.

To demonstrate this simplification, 347 evenly distributed loading conditions on the Smith chart is generated by the active load-pull system. For each loading condition, the six-port reflectometer outputs 4 detector values. This process yields a 347 by 4 look-up table.

After the creation of the lookup table grid, the reflectometer measures any loading conditions generated by the active load-pull system. For each unknown loading, the reflectometer measures 4 detector values. A table look-up is performed by searching for a table entry with matching 4 detector values (in the

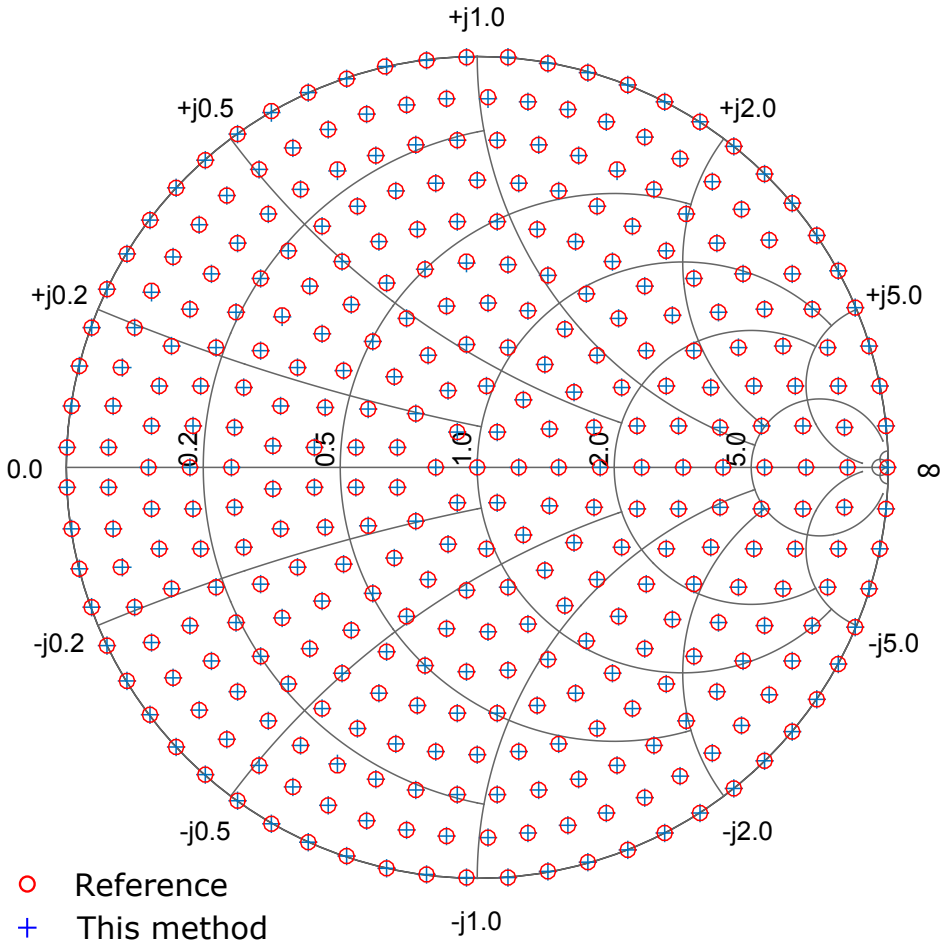


Figure 7.16: Measured reflection coefficients from the proposed six-port reflectometer using a lookup table vs. references from the calibrated active load-pull setup.

least square sense). The table look-up results are shown in Fig. 7.16, compared with reference readings from the load-pull system. Excellent agreement between the six-port reflectometer and the calibrated load-pull system can be observed. In this case, since the unknown loadings are the same as the known loadings for the look-up table construction, excellent agreement indicates repeatability of both the load-pull setup and the reflectometer under test.

7.4. Conclusion

A package integratable six-port reflectometer for power devices has been presented. It uses the bondwires connection between the drain of the power bar

and the package to couple a small amount of output power to a detection loop with little efficiency degradation. The latter loop is sampled by diode detectors at four different locations placed $\lambda/8$ apart. This well-chosen distance minimizes the impact of noise. The realized reflectometer has been designed for the 2.4-2.5 GHz ISM band and has a size of only 9.4 by 4 $\mathrm{m}m^2$. Future work aims for further size reduction by implementing the $\lambda/8$ delay lines with on-chip lumped components, integrated detection diodes and DC readout circuitry. The proposed approach could ultimately enable fully integrated in-package RF power systems capable to monitor their load conditions in low-cost high-volume RF heating applications such as solid-state microwave ovens.

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8

Conclusion

8.1. Summary of Results

In this work, a non-intrusive near-field measurement technique is extensively developed and explored for the in-situ characterization, optimization and troubleshooting of power amplifiers and power devices. The proposed technique employs a passive electric-field sensing probe to measure the electric near-field while the DUTs are operating in their normal conditions. Further assisted by an electromagnetic model of the passive structures within the DUTs, the proposed technique is capable to deduce the in-circuit parameters such as voltages, currents, power and impedances.

Even for the measurement of only an in-circuit voltage, the use of an electromagnetic model is found to be beneficial since the frequency variation of coupling capacitance between the probe and DUT can be accounted for. Employing this information the measurement accuracy is improved, especially for higher (i.e., harmonic) frequencies, yielding enhanced waveform fidelity. The proposed method is validated on a microstrip line carrying waveforms with rich harmonic content. The accuracy of the proposed technique is benchmarked against a conventional thru-reflect-line (TRL) de-embedding approach by a nonlinear vector network analyzer (NVNA). Measurement results show that the root-mean square (RMS) error can be improved by 3 percentage points (from 8% to 5%) compared to the prior arts over the frequency range from 1 to 5 GHz.

The capability of the proposed technique is first demonstrated by the individual characterization of the interacting devices in a fully operational 2.2-GHz 400-W Doherty PA in terms of loading conditions, output voltage, current, power and efficiency at their intrinsic device planes. These experimentally obtained in-circuit conditions have been compared with the theoretical Doherty behavior, showing good agreement. A further characterization of deteriorating device interaction in a detuned Doherty PA demonstrates the high practical value of

this technique for PA design, troubleshooting and optimization. According to the best knowledge of the authors, the interaction of active devices in a PA is experimentally characterized for the first time.

In a much smaller scale within high-power transistor packages, the proposed method is used to detect uneven performance of transistor cells, also known as spatially distributed effects, by characterizing in-circuit parameters at the bondwire terminals. In a first attempt, a passive bondwire structure is used to benchmark the measurement accuracy. The achieved results agree fairly with independent data obtained through conventional measurement techniques. Then, distributed effects in packaged 100-W and 200-W LDMOS transistors with internal matching networks are successfully characterized by the proposed technique in terms of in-situ voltages and currents at individual drain-bondwire terminals, yielding deep insight and detailed knowledge for device troubleshooting and optimization. These in-circuit in-situ parameters, which until now are only accessible from simulators, have been experimentally quantified for the first time.

The proposed technique is further improved for the characterization of distributed effects in a high-power GaN HEMT. The improvement applies the NSMM PSD method to measure directly the E-field induced by energized transistor fingers. The flat semiconductor surface further permits close probe-DUT proximity. Consequently, more constant probe-DUT coupling as well as more localized field data can be obtained. The proposed technique experimentally quantifies voltages at individual fingers 70 $\mu\mathrm{m}$ apart within an operating GaN HEMT. The obtained voltage and current distributions validate an independently developed multi-physics distributed device model of the same device. The added value of having direct measurement insight in the finger voltage distribution without any pre-assumptions on the active device itself has been further demonstrated by identifying a device defect at the finger level, which is enforced by laser cutting.

Besides being a measurement method, the near-field technique presented in this work can also be used as a monitoring device integrated into a packaged power transistor. This point is demonstrated by a package integratable six-port reflectometer for power transistors. It uses the bondwires connection between the drain of the power bar and the package to couple a small amount of output power to a detection loop with little efficiency degradation. The latter loop is sampled by diode detectors at four different locations placed $\lambda/8$ apart. This well-chosen distance minimizes the impact of noise. The realized reflectometer has been designed for the 2.4-2.5 GHz ISM band and has a size of only 9.4 by 4 $\mathrm{m}m^2$. Future work aims for further size reduction by implementing the $\lambda/8$ delay lines with on-chip lumped components, integrated detection diodes and DC readout circuitry. The proposed approach could ultimately enable fully integrated in-package RF power systems capable to monitor their load conditions in low-cost high-volume RF heating applications such as solid-state microwave ovens.

8.2. Future Work

The potential of the proposed technique is far reaching. Probe design and manufacturing can be improved for higher resolution and sensitivity. A contactless calibration technique would be very appealing for measurement accuracy improvement. Probe locationing and positioning equipments could be improved to reduce model-measurement discrepancy. Other coupling mechanisms such as magnetic probes and wave probes are useful complements to directly measure current and power waves, respectively. Ultimately, to promoted the near-field technique for microwave metrology, an extensive error analysis is recommended.

With the possibility of in-situ access of the internal localized voltages and currents at fundamental and harmonic frequencies, now it is time to use these techniques to our advantage and indeed to start optimizing power devices and amplifiers for their efficiency and linearity performance, a route that can provide significant benefits in device and amplifier performance and will help to reduce the energy consumption of wireless networks and RF solid-state heating applications in the future.

Summary

In this work, a near-field measurement technique is extensively developed and explored for the characterization, optimization and troubleshooting of power amplifiers and power devices. Similar as far-field imaging, near-field scanning is capable of passively observing circuits under test in-situ and without intrusion. These unique advantages enable the the near-field technique for the live observation of unperturbed dynamic processes such as active device interactions in a Doherty PA.

However, unlike far-field imaging, whose resolution is limited by diffraction, near-field scanning can achieve super resolution due to evanescent-wave coupling. This enhanced resolution permits the near-field technique to distinguish individual transistor bondwires, cells and fingers (with tens of micrometers dimensions) at RF and microwave frequencies (several GHz) rather than optical frequencies (tens of THz).

Imaging microwave circuits at their operating frequencies has an unparalleled potential, since a unique link exists between the observable electromagnetic near-field and inaccessible in-circuit electrical parameters such as voltages and currents. The major contribution of this research is to establish this link by numerical EM modeling and to experimentally prove its feasibility.

High resolution, passively observed in-situ field images can then be used to deduce otherwise inaccessible circuit parameters such as voltages and currents in great spatial details. This EM-model assisted near-field measurement technique is experimentally demonstrated to have successfully characterized distributed voltages and currents at bondwire terminals of LDMOS FETs and at cells and fingers of GaN HEMTs.

Near-field scanning microwave microscopes take relative images in most published works. This research has proposed that calibrated near-field images have physically meaningful intensity and contrast. These absolute-intensity images can be used to deduce in-circuit voltages and traveling waves in their absolute waveforms. This absolute near-field measurement technique is validated by a set of conventional measurements from a calibrated non-linear vector network analyzer and TRL deembedding.

An alternative near-field measurement application to high-power transistors is demonstrated as a simple, cheap, compact and accurate reflectometer based on the six-port principle.

Samenvatting

In dit proefschrift wordt een nabije-veld meettechniek ontwikkeld en uitgebreid onderzocht voor de karakterisatie, optimalisatie en het oplossen van problemen van eindversterkers en vermogens-transistoren. Net als verre-veld beeldvorming kan nabije-veld beeldvorming passief schakelingen in-situ voor testdoeleinden waarnemen, zonder deze te beïnvloeden. Deze unieke voordelen maken het mogelijk een nabije-veld techniek te gebruiken voor rechtstreekse observatie van dynamische processen, zonder deze te beïnvloeden, zoals actieve interactie tussen transistoren in een Doherty vermogensversterker. Echter, in tegenstelling tot verre-veld beeldvorming, waarvan de resolutie wordt beperkt door diffractie, kan nabije-veld beeldvorming superresolutie waarnemingen realiseren door de koppeling met evanescente velden. Deze verbeterde resolutie met de nabije-veld techniek, maakt het mogelijk om individuele transistor bond-draden, cellen en vingers (met afmetingen van tientallen micrometers) te onderscheiden bij RF en micro-golf frequenties (meerdere GHz) in plaats van bij optische frequenties (tientallen THz). Beeldvorming van micro-golf schakelingen op hun operationele frequentie heeft een ongekende potentie, omdat er een unieke link bestaat tussen het waarneembare elektromagnetische nabije-veld en de ontoegankelijke elektrische parameters van de schakeling zoals spanningen en stromen. De belangrijkste bijdrage van dit onderzoek is om deze link met gebruik van numerieke EM modellen vast te stellen en experimenteel de haalbaarheid te bewijzen. Hoge resolutie, passief waargenomen in-situ veld beelden kunnen vervolgens worden gebruikt om ontoegankelijke parameters van schakelingen zoals spanningen en stromen uit de ruimtelijke gegevens af te leiden. Deze EM-model geassisteerde nabije-veld techniek is experimenteel aangetoond door met succes de spannings- en stroom-verdeling in bond-draden van LDMOS FETs en in de cellen en vingers van GaN HEMTs te karakteriseren. Nabije-veld micro-golf microscopie maakt gebruikt van relatieve beelden in de meeste gepubliceerde werken. Dit proefschrift stelt voor dat gekalibreerde nabije-veld beelden fysisch zinvolle amplitude en contrast informatie bevatten. Van deze absolute amplitude beelden kunnen derhalve de absolute golfvormen van de spanningen en de lopende golven in de schakeling worden afgeleid. Deze absolute nabije-veld techniek is gevalideerd door een reeks van conventionele metingen met gebruik van een gekalibreerde niet-lineaire vector network analyzer en TRL deembedding. Een alternatieve nabije-veld meettoepassing voor hoog-vermogenstransistoren op basis van het zes-poorten principe wordt aangetoond en gerealiseerd als een eenvoudige, goedkope, compacte en nauwkeurige reflectiemeter.

Acknowledgements

The work presented in this thesis could not have been done without the help and influence of many individuals.

Firstly, I would like to express my gratitude to my promotor Prof. dr. ing. Leo C. N. de Vreede and my co-promotor Dr. Marco Spirito for their relentless and insightful guidance.

I am deeply grateful to Fred van Rijs, John Gajadharsing, Klaus Werner, Michel de Langen, Thomas Roedle, Martino Lorenzini, Rob Heeres, Rik Jos, Steven Theeuwen, Jawad Qureshi, Ji Zhao, Edmund Neo, Vittorio Cuoco, Bob Ostovarpour and Jingchu He from NXP Semiconductors for their professional and timely support.

I would like to thank Bert-Jan Kooij, Koen Buisman, Cong Huang, David Calvillo-Cortes, Marco Pelk, Michele Squillante, Mauro Marchetti, Ajay Kumar Manjanna, Morteza Alavi, Haiying Cao and Razvan Venter for the many inspiring discussions and contributions to the work presented in this thesis.

I am very grateful to Atef Akhnoukh, Wil Straver, Ali Kaichouhi, Antoon Frehe, Vladimir Jovanovic, Loek van Schie, Wim Tiwon and of course Marion de Vlieger for their help and support technically and otherwise.

I would like to thank Prof. dr. John Long and Prof. dr. Bogdan Staszewski for their recommendation of me to Leo.

I really appreciate Michiel Grashuis and Hans Konig from Brightsight who helped me generously and professionally in an urgent request of laser cutting.

It is my great pleasure to have worked with Nitz Saputra, Wanghua Wu, Yi Zhao, Senad Hiseni, Mina Danesh, Duan Zhao, Ruimin Yang, Yiongjia Li, Xiongchuan Huang, Feifei Huo, Jingwen Fan, Akshay Visweswaran, Seyed Ahmadi Mehr, Gennaro Gentile, Luca Galatro, Zhirui Zong, Zhebin Hu, Ying Wu, Xun Luo, Huizhen Qian, Hao Gao, Jianing Wang, Gerasimos Vlachogiannakis, Satoshi Malotaux, Arturo Santaniello, Yue Chen and Yiyu Shen.

I am grateful to NXP Semiconductors for the financial sponsorship and technical collaboration, to Anteverta B.V. for their powerful active harmonic load-pull system, to Brightsight B.V. for their generous technical help in an emergency.

Last but not least, I am deeply thankful to my family for their constant encouragement and to my wife for the love.

Curriculum Vitæ

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