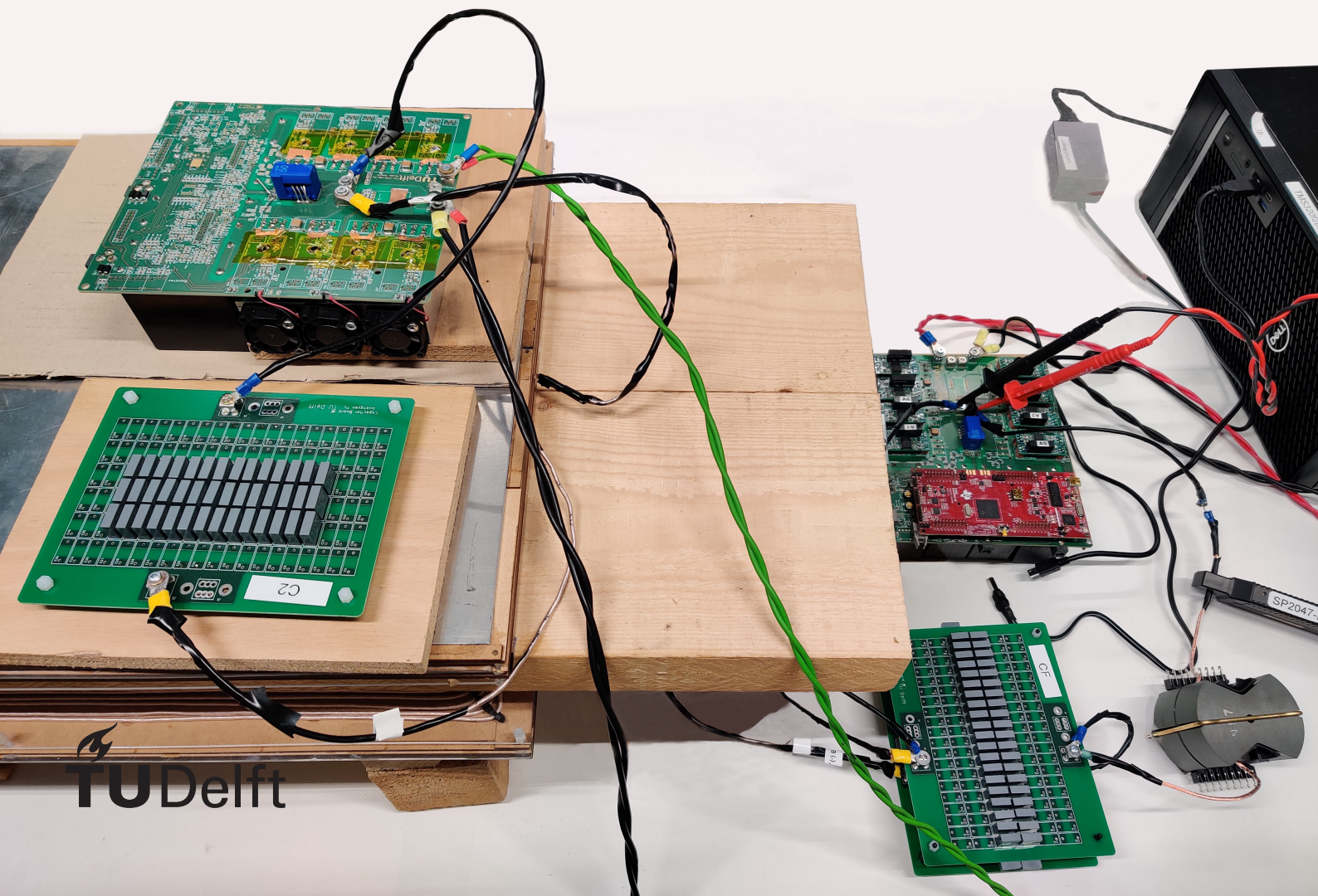


Benchmark of Different Compensations for Wireless Power Transfer with DC/DC Converters Included

Pengcheng Ye



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by

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Preface

This document is Pengcheng Ye's master thesis, which contains the outcome of my graduation project from November 2021 to August 2022.

I would like to thank my thesis advisor Prof.dr. Pavol Bauer and daily supervisor Dr. Jianning Dong for their time and guidance. Thanks to Francesca Grazian for helping me complete the experimental verification despite her busy schedule. I also want to express my gratitude to Guangyao Yu, who gave me patient guidance and help throughout the whole process of my graduation project. It is his enthusiasm for academics that motivated me to overcome the various challenges I encountered during this thesis.

I want to thank my friends and family for their company and encouragement, which is especially valuable at this particular time of the Covid-19 pandemic. Thanks to my sister Yunting Huang for her company and help in my thesis. Finally, I would like to thank my girlfriend Yue Gao for her love and unconditional support throughout my study process.

Pengcheng Ye
Delft, August 2022

Abstract

The compensation network in wireless power transfer (WPT) system has many functions, including increasing efficiency, providing constant voltage/current output, reducing volt-ampere rating, etc. With the popularity of wireless charging for electric vehicles, more and more compensation topologies with distinctive characteristics are proposed. Therefore, a comprehensive comparison among various compensation topologies under rated operating condition is necessary for the selection of compensation topology for WPT. In this thesis, eight compensation topologies are selected for benchmark and compared in terms of efficiency, component voltage/current stress, design freedom, misalignment behaviour, etc. under the rated operating condition set based on SAE J2954 [1] standard. Given the analytical comparison results, the S-S compensation and LCC-S compensation are selected for further analysis and experimental verification.

In the practical design process of the compensation, the voltage/current stress on each component and the implementation of zero voltage switching (ZVS) on switches are two critical issues to be considered. For the calculation of components' peak voltage/current, the fundamental-frequency analysis is the most widely used calculation method, which is inaccurate in some inductors' voltage peak calculation. Therefore, a new resonant inductor voltage peak calculation method is proposed in this thesis, which is proved to be more accurate in both simulation and experiments in S-S and LCC-S compensations. For the implementation of ZVS, few studies have given the calculation method of switching current due to its complexity. In this thesis, a new switching current calculation method for LCC-S compensation is proposed and compared with the existing calculation method. A tuning method for ZVS implementation based on this calculation method is also proposed. Results from simulation and experiments under various operating conditions are provided to verify the accuracy of the newly proposed switching current calculation method. In the experiments, the LCC-S compensation and S-S compensation are compared under different power and input voltages. Experimental results show that the efficiency of LCC-S compensation is higher at low power, because of the lower conduction loss on MOSFETs. However, the efficiency of S-S compensation is higher at high power due to less losses on compensation components.

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1

Introduction

This chapter first introduces the development of wireless power transmission, existing applications and application prospects and other background knowledge. Besides, the general topology of wireless charging for electric vehicles, and the role of compensation networks play in it are introduced.

This chapter illustrates the importance of compensation networks and the diversity of topologies. Some existing studies on different compensation topologies are also given and analyzed. Based on these existing studies, research objectives can be proposed to achieve a more comprehensive comparison of different compensation topologies.

The structure of this study is given at the end of this chapter.

1.1. Background

The history of wireless power transmission can date back to the late 1800s, when Nikola Tesla wanted to build a world-wide wireless transmission system [2]. Until now, wireless power transfer (WPT) system has been used for a great variety of applications and has brought many possibilities for energy transfer.

In [3], the applications of WPT technology are divided into two main categories, far-field transmission and near-field transmission. An example of a far-field WPT technology application is low-power sensor networks. Far-field WPT technology also makes it possible to transfer solar energy from space to earth or remove the heavy fuel of spacecraft by transferring power wirelessly.

Compared with far-field WPT, the near-field WPT can achieve higher efficiency and is more commonly used in daily life. Some common near-field WPT applications are wireless charging of some daily low-power electronic devices such as electric toothbrushes and cell phones. With the improvement of WPT technology, wireless charging of high-power devices such as electric vehicles (EV) is becoming an important application of WPT technology, which is also the main application studied in this thesis.

Electric vehicles are gaining popularity due to their ability to reduce greenhouse gas emissions, while the application of WPT in electric vehicles can help increase driving range, reduce battery size and improve charging convenience [4].

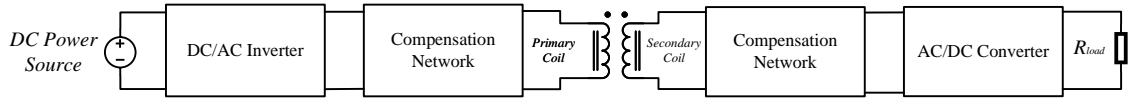


Figure 1.1: WPT Schematic

Figure 1.1 presents a typical schematic of a WPT system for charging electric vehicles, where DC power source can be a DC grid or an AC grid connected to a rectifier. The DC voltage is first converted to a high-frequency AC voltage through the DC/AC inverter. Then, this high-frequency AC voltage source is transmitted from the primary coil through an air gap to the secondary coil. Finally, the ac power is rectified to DC power by AC/DC converter on the secondary side to charge the battery of the electric vehicle. Due to the large distance between the primary and secondary coils in this energy transfer process, the primary and secondary coils are usually loosely coupled, and the leakage inductance on both sides are relatively large. Therefore, the compensation network is added to compensate the leakage inductance and reduce the voltage-ampere rating of the WPT system [5]. Besides, the compensation network can provide constant voltage/current output and achieve high efficiency of the WPT system [6].

Compensation network is critical in the WPT system, so a great number of compensation topologies have been proposed and studied in recent years [7]. The focus of this thesis is to investigate and compare various compensation topologies under the rated operation conditions defined by SAE J2954 [8].

1.2. Problem definition

Currently, there is a very wide range of topologies available for compensation networks, and different topologies have varied features and functions. Therefore, it is necessary to study and compare different topologies.

In [7], the various compensation topologies are split into several basic resonant network blocks composed of passive components to analyze the principles of achieving constant voltage/current and zero phase angle (ZPA). However, the unique characteristics of different topologies are not well illustrated and compared.

The study in [9] provides a comprehensive comparison of different topologies, taking into account a variety of factors including efficiency, compensation components sensitivity, wireless transmission distance, control strategy, etc. However, it only focuses on the conventional two-element compensation topologies, and little work has been done on high order compensation topologies.

Some studies like [10] and [11] give a comparison between the features of conventional topology and high order composite topology, but only two topologies are taken into account, which is not so comprehensive.

In this thesis, the conventional compensation topologies and high order compensation topologies as well as some newly proposed novel high order compensation topologies are considered comprehensively, and the characteristic analyses of different topologies are given to provide guidance for compensation topology selection under SAE standard. After the topologies comparison, two optimal topologies are selected for experimental verification.

There are two important issues to focus on during the compensation topology design process: components voltage/current stresses and ZVS implementation. In terms of components stresses, most studies adopt fundamental-frequency analyses to calculate the voltage/current stresses, however, this method is not accurate in some cases. The simulation and experimental analyses in this thesis demonstrate that the results of this calculation method are significantly smaller when it is applied to the resonant inductor voltage stress calculation. Therefore, a new resonant inductor voltage stress calculation method is proposed in this thesis, which is verified experimentally, and proven to be quite accurate.

In terms of ZVS implementation, few studies have analyzed the implementation of ZVS in detail in the LCC-S topology, since the calculation of the switching current is very difficult. In [12], a switching current calculation method and the corresponding tuning method for LCC-LCC compensation topology is proposed, which is applied by [13] in LCC-S compensation. This calculation method only roughly takes into account the influence of the high-order harmonics from the input voltage, but in fact the influencing factors of the switching current are more complicated. A new switching current calculation method is proposed in this thesis, which is verified by simulation and experiments to accurately calculate the switching current values under various operating conditions. Based on this calculation method, a tuning method for ZVS implementation in LCC-S compensation is also proposed.

1.3. Research objectives and structure

The purpose of this study is to analyze and compare different compensation topologies, and the following factors are focused in the analyses and comparison process:

- Efficiency

Efficiency is a critical factor in WPT system. High efficiency can help reduce energy consumption.

- Voltage stress

Damage or breakdown could happen when voltages on compensation components are too large. Appropriate voltage stress is also a consideration when designing compensation components. The voltage stress should be reduced as much as possible.

- Current stress

Conducting high currents on the compensation components increases the losses on the components and thus reduces the efficiency. In addition, excessive current stress could damage the components, so current stress is also an important factor to be considered when designing a compensation component.

- Misalignment behaviour

When there is a vertical or lateral misalignment during EVs wireless charging, the coupling coefficient between primary and secondary coils will change, which normally becomes smaller than the aligned condition. In this case, the voltage and current stresses of the components as well as the efficiency of the system will change. The voltage and current stress in some compensation topologies could become very high causing damage of components.

- Design freedom

Some topologies have little or no control over the output by adjusting the compensation components parameters, due to their simple compensation structures or limitations in compensation methods. Therefore, for WPT adopting low-design-freedom compensation topology, the output voltage/current can not be supplied as designed when the input voltage changes. However, for WPT adopting high-design-freedom compensation topology, adjusting compensation components values can allow the setup operating at the new input voltage.

- Cost

Different compensation topologies require different numbers of compensation components and different component values, so the cost of the compensation network varies. The lower-cost compensation topology should be selected when other requirements are satisfied.

The structure of this research is organized as 1.2.

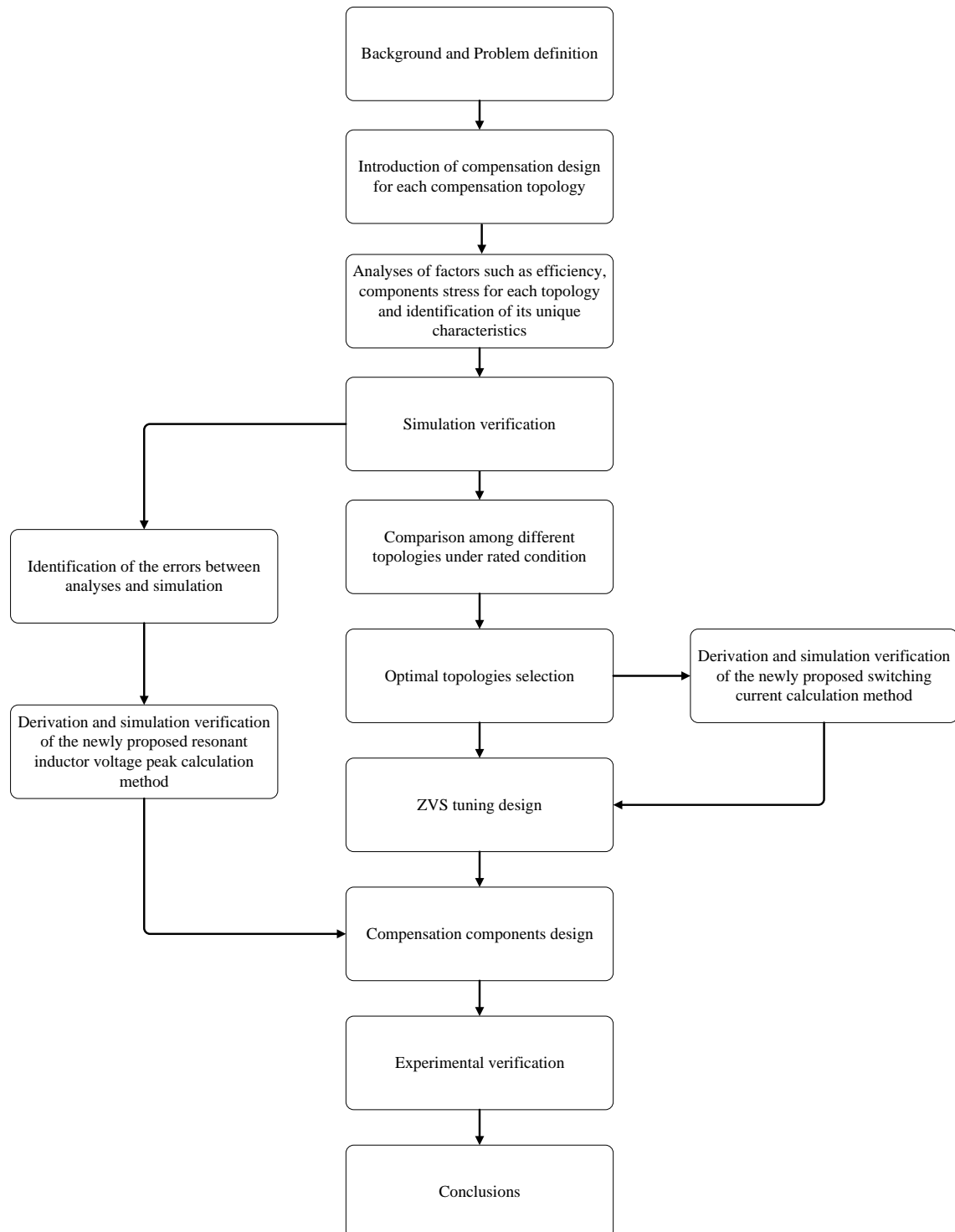


Figure 1.2: Thesis structure

2

Analyses and comparison of different topologies

Compensation networks for wireless power transfer now have many kinds of topologies, and each has distinctive characteristics. Herein, all compensation topologies are divided into three main types: conventional two-element compensation topologies, high-order composite compensation topologies and novel high-order composite compensation topologies. These three types of topologies will be introduced and analyzed in sections 2.2, 2.3 and 2.4, respectively.

The computation of voltage and current stress on each component and efficiency for each topology are introduced in sections 2.2, 2.3 and 2.4, and summarized for topologies comparison in section 2.5. Simulation models based on circuit simulator PLECS are used to verify the analyses.

To make a fair comparison of the various topologies, the rated working condition of the wireless power transfer system based on SAE standard is defined in section 2.1. In section 2.5, all topologies are compared in many aspects, and a summary table is given at the end of the section.

2.1. Rated working condition

The general schematic of the WPT system is shown in figure 1.1. Here, some specific parameter values will be defined according to the SAE standard [1]. The DC charging voltage V_{DC} is 400 V and the battery side voltage V_{Bat} is the same as V_{DC} . However, for S-S topology, due to the limit of design freedom, the charging voltage needs to be decreased to meet the output voltage requirement, thus there is an extra front-end buck converter to decrease the DC voltage.

The DC voltage source is connected to a full bridge inverter to generate AC source V_s for the system. Normally only fundamental frequency component is considered during the analysis, thus the AC source can be calculated by: $V_s = \frac{2\sqrt{2}}{\pi} V_{DC}$. The switching frequency f of the full bridge inverter is 85 kHz and the angular frequency ω is $2\pi f$.

It is assumed that the primary-side inductance L_1 and the secondary-side inductance L_2 are fixed. The rated coupling coefficient k between the primary and secondary coils is 0.2 and the mutual inductance M can be calculated by: $M = k \cdot \sqrt{L_1 L_2}$.

The rated output power P_o is 4 kW, therefore, the battery side current I_{Bat} can be calculated by: $I_{Bat} = \frac{P_o}{V_{Bat}}$ and the battery side equivalent resistor R_{load} can be calculated by: $R_{load} = \frac{V_{Bat}}{I_{Bat}}$.

For non-ideal analysis, the quality factors Q_{L_1} and Q_{L_2} of the primary coil L_1 and the secondary coil L_2 are selected as 500 [14], and defined in table 2.1.

All compensation topologies are compared under the rated working condition specified above, and table 2.1 summarizes all parameter values.

V_{DC}	400 V
f	85 kHz
ω	$2\pi f$
L_1	200 μ H
L_2	220 μ H
M	41.95 μ H
k	0.2
P_o	4 kW
V_{Bat}	400 V
I_{Bat}	10 A
R_{load}	40 Ω
Q_{L_1}	500
Q_{L_2}	500

Table 2.1: Rated working condition parameter values

2.2. Conventional two-element compensation topologies

The conventional two-element compensation topologies include S-S, S-P, P-S and P-P topologies where "S" refers to the series connection of the compensation capacitor and the coil while "P" refers to the parallel connection of the compensation capacitor and the coil. Among these four topologies, the S-S compensation topology is the most widely used because the compensation capacitor is independent of the load and the mutual inductance, which makes compensation design simpler and more reliable under misalignment. Based on the considerations above, only S-S topology is analyzed here.

2.2.1. S-S topology

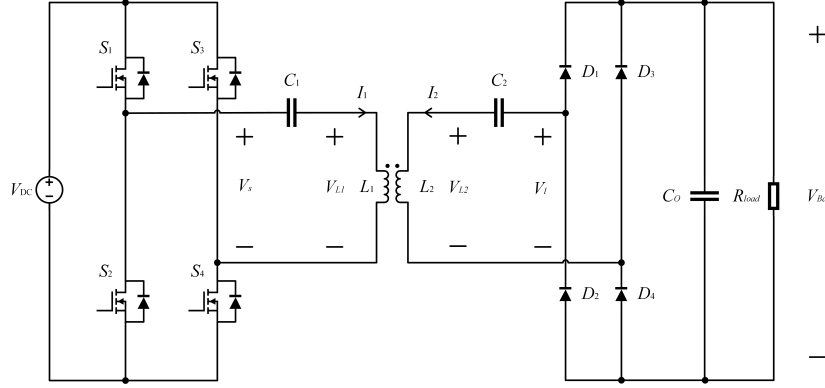


Figure 2.1: S-S Compensation Topology

In S-S topology which features constant current output, the primary compensation capacitor C_1 and the secondary compensation capacitor C_2 are designed to resonate with L_1 and L_2 individually, which are calculated based on (2.1) and (2.2), and $C_1 = 17.53 \text{ nF}$, $C_2 = 15.94 \text{ nF}$.

At the primary side, since L_1 is compensated by C_1 , there is $\dot{V}_s = j\omega M \dot{I}_2$. Substitute $I_{Bat} = \frac{2\sqrt{2}}{\pi} I_2$, output current can be calculated as $I_{Bat} = \frac{2\sqrt{2}}{\pi} \frac{V_s}{\omega M}$. From this equation it can be seen that the output current is only decided by the input voltage and the mutual inductance, thus the design freedom of S-S topology is quite low. According to the rated condition, $I_{Bat} = 10 \text{ A}$, therefore, the input voltage needs to be adjusted to $V_s = \frac{\pi}{2\sqrt{2}} \omega M I_{Bat}$, and $V_{DC} = \frac{\pi}{2\sqrt{2}} V_s = 276.42 \text{ V}$.

$$j\omega L_1 + \frac{1}{j\omega C_1} = 0 \quad (2.1)$$

$$j\omega L_2 + \frac{1}{j\omega C_2} = 0 \quad (2.2)$$

For convenience of deriving voltage and current in the circuit, only fundamental frequency component is considered, and the original topology is simplified as figure 2.2. V_s and V_l are the fundamental frequency component of V_{DC} and V_{Bat} , and can be calculated by: $V_s = \frac{2\sqrt{2}}{\pi} V_{DC}$ and $V_l = \frac{2\sqrt{2}}{\pi} V_{Bat}$. R_{ac} is the equivalent resistance of R_{load} referred to the front side of the rectifier. Since the output power is unchanged after conversion, there is: $P_o = \frac{V_{Bat}^2}{R_{load}} = \frac{V_l^2}{R_{ac}}$. Based on these, the expression of R_{ac} can be derived as (2.3).

$$R_{ac} = \frac{8}{\pi^2} R_{load} \quad (2.3)$$

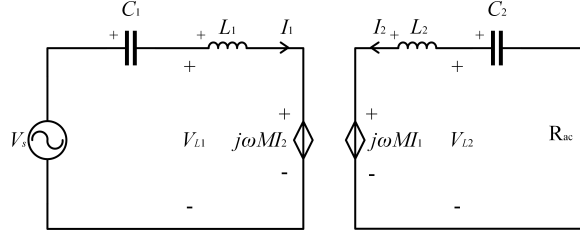


Figure 2.2: S-S Compensation Schematic

When the WPT system is fully compensated, (2.4) can be derived by applying Kirchhoff's Voltage Law (KVL) on both primary and secondary circuit. For calculation simplicity, the secondary side impedance is referred to the primary side as an equivalent impedance Z_{ref} which is calculated by:

$Z_{ref} = \frac{j\omega M I_2}{I_1}$, and can be further derived as (2.5) when (2.4) is substituted.

$$\begin{cases} j\omega M \dot{I}_2 = \dot{V}_s \\ j\omega M \dot{I}_1 = -\dot{I}_2 \cdot R_{ac} \end{cases} \quad (2.4)$$

$$Z_{ref} = \frac{\omega^2 M^2}{R_{ac}} \quad (2.5)$$

The primary coil's current I_1 and the secondary coil's current I_2 can be solved in (2.6). Based on I_1 and I_2 , the voltage stresses of the compensation capacitors can be obtained in (2.7), and the voltage stresses of L_1 and L_2 can be given by (2.8).

$$\begin{cases} \dot{I}_1 = \frac{\dot{V}_s}{Z_{ref}} = \frac{\dot{V}_s R_{ac}}{\omega^2 M^2} \\ \dot{I}_2 = -\frac{j\omega M \dot{I}_1}{R_{ac}} = -j \frac{\dot{V}_s}{\omega M} \end{cases} \quad (2.6)$$

$$\begin{cases} \dot{V}_{C1} = \dot{I}_1 \cdot \frac{1}{j\omega C_1} \\ \dot{V}_{C2} = -\dot{I}_2 \cdot \frac{1}{j\omega C_2} \end{cases} \quad (2.7)$$

$$\begin{cases} \dot{V}_{L1} = j\omega M \dot{I}_2 + j\omega L_1 \dot{I}_1 \\ \dot{V}_{L2} = j\omega M \dot{I}_1 + j\omega L_2 \dot{I}_2 \end{cases} \quad (2.8)$$

For efficiency calculation, since the serial resistance of compensation components are much smaller than the coil resistance, only the losses from the coils are considered with specified quality factors Q_{L1} and Q_{L2} in section 2.1. To obtain the efficiency of S-S compensation topology, non-ideal analyses is applied. In non-ideal condition, the resistance of L_1 and L_2 are given by (2.9). The non-ideal S-S compensation schematic is shown in figure 2.3.

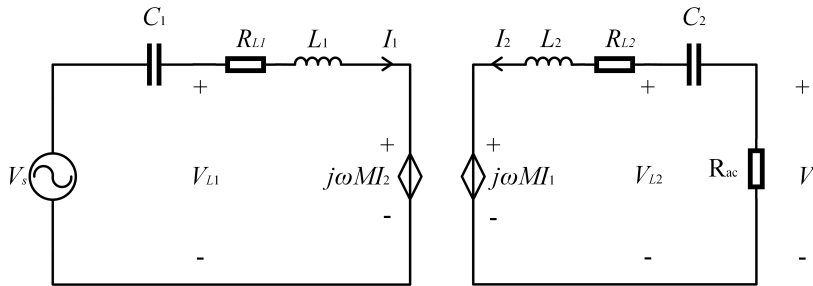


Figure 2.3: Non-ideal S-S Compensation Schematic

$$\begin{cases} R_{L1} = \frac{\omega L_1}{Q_{L1}} \\ R_{L2} = \frac{\omega L_2}{Q_{L2}} \end{cases} \quad (2.9)$$

The primary side efficiency η_1 can be calculated by $\eta_1 = \frac{Z'_{ref}}{Z'_{ref} + R_{L1}}$ and the secondary side efficiency η_2 can be calculated by $\eta_2 = \frac{R_{ac}}{R_{ac} + R_{L2}}$. Here, Z_{ref} in ideal analyses is adjusted to $Z'_{ref} = \frac{\omega^2 M^2}{R_{ac} + R_{L2}}$, because R_{L2} is also included in analyses. The total efficiency of the S-S compensation topology is $\eta = \eta_1 \cdot \eta_2$. Combining the expression of Z'_{ref} and (2.9), η can be derived as (2.10).

$$\eta = \frac{k^2 Q_{L1} Q_{L2}}{k^2 Q_{L1} (Q_L + Q_{L2}) + \frac{Q_L}{Q_{L2}} + \frac{Q_{L2}}{Q_L} + 2} \quad (2.10)$$

Where Q_L is the loaded quality factor and $Q_L = \frac{\omega L_2}{R_{ac}}$, k is the coupling coefficient between primary and secondary coils. By checking the denominator of (2.10), when (2.11) is satisfied, the highest efficiency will be achieved.

$$Q_L (k^2 Q_{L1} + \frac{1}{Q_{L2}}) = \frac{Q_{L2}}{Q_L} \quad (2.11)$$

The optimal Q_L is given by (2.12).

$$Q_{L_{opt}} = \sqrt{\frac{Q_{L2}^2}{k^2 Q_{L1} Q_{L2} + 1}}. \quad (2.12)$$

In some articles, the efficiency equation (2.10) is expressed in terms of resistance as (2.13), and the optimal load in this case is given by (2.14) [3].

$$\eta = \frac{\omega^2 M^2 R_{ac}}{\omega^2 M^2 (R_{L2} + R_{ac}) + R_{L1} \cdot (R_{L2} + R_{ac})^2} \quad (2.13)$$

$$R_{L_{opt}} = \sqrt{\frac{\omega^2 M^2 R_{L2}}{R_{L1}} + R_{L2}^2} \quad (2.14)$$

Simulation verification of S-S topology

The S-S compensation topology simulation model is made using PLECS and is shown in figure 2.4. In table 2.2, the simulation results are compared with the calculation results based on the analyses given above.

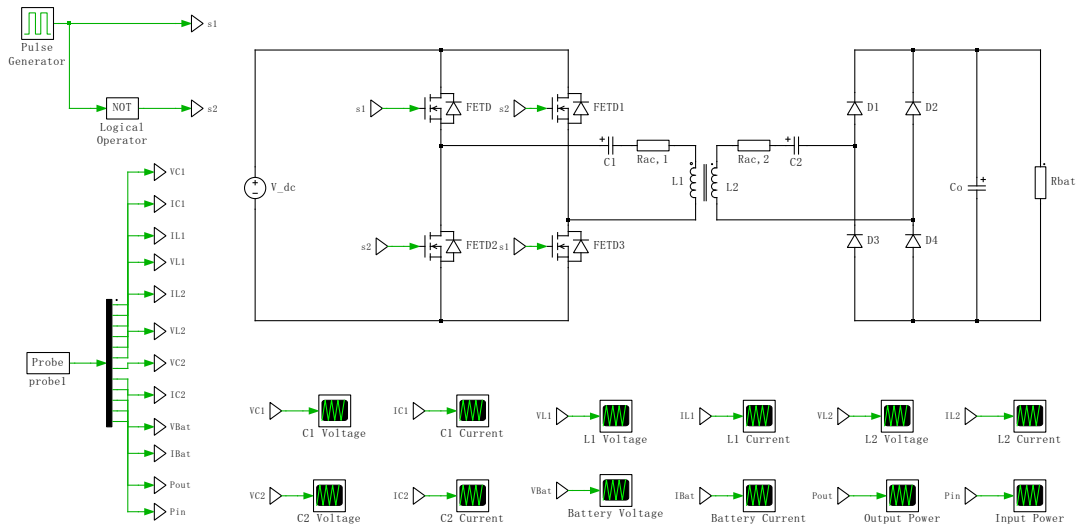


Figure 2.4: S-S Simulation model

	V_{C_1} (V)	V_{L_1} (V)	V_{L_2} (V)	V_{C_2} (V)	I_{C_1} (A)
Simulation Results	2425.25	2700.8	2243.2	1843.54	22.42
Calculation Results	2428	2453.3	1914.6	1845.6	22.73
	I_{L_1} (A)	I_{L_2} (A)	I_{C_2} (A)	Efficiency	
Simulation Results	22.42	15.48	15.48	0.979	
Calculation Results	22.73	15.71	15.71	0.979	

Table 2.2: S-S Simulation and Calculation Comparison

As can be seen from the table, when only fundamental frequency is considered, the calculated currents on all components and voltages on C_1 and C_2 are very close to the simulation results. However, there are some deviations in the calculated voltages on L_1 and L_2 . Therefore, a new calculation method needs to be applied, which is called resonant inductor voltage peak calculation method, and will be introduced in section 3.1.1.

When resistances of the primary and secondary coils are considered, the simulated voltage and current stresses are close to the ones in ideal model. Therefore, when calculating voltage and current stresses, the resistances can be neglected.

2.3. High-order composite compensation topologies

Compared to conventional two-element compensation topologies, the high-order composite compensation topologies introduce more compensation components which increase the design freedom, and different high-order composite compensation has its own superior characteristics. Among these compensation topologies, the LCC-S, LCC-LCC and S-LCC topologies are more widely used, and will be discussed in this section.

2.3.1. LCC-S topology

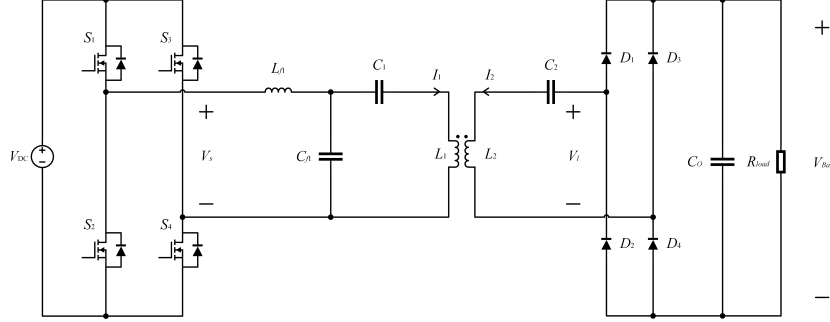


Figure 2.5: LCC-S Topology

LCC-S Compensation topology can provide constant voltage output. At primary side, L_{f1} is designed to resonate with C_{f1} to create constant current I_1 , which then produces a constant voltage through a current controlled voltage source at the secondary side. Since C_2 is designed to resonate with L_2 , the load-side voltage V_l is the same as the secondary-side voltage produced by I_1 . Therefore, the battery-side output voltage can be kept constant.

The LCC-S compensation topology can also be simplified in the same way as the S-S compensation. The simplified schematic is shown in figure 2.6.

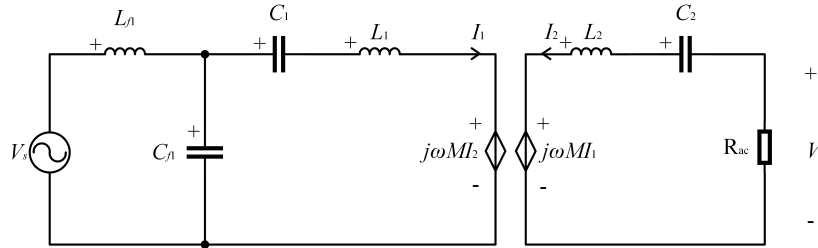


Figure 2.6: LCC-S Schematic

The secondary side of LCC-S compensation topology is the same as S-S compensation, thus Z_{ref} can still be calculated using (2.5). For the primary side, L_{f1} , C_{f1} , C_1 and L_1 form a T-type circuit which is then connected to Z_{ref} . This T-type circuit is shown in figure 2.7. To achieve input zero phase angle (ZPA), the input impedance of this T-type circuit is analyzed.

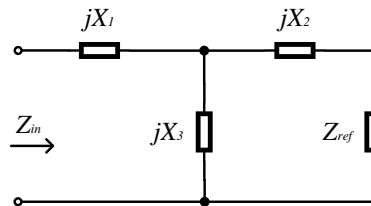


Figure 2.7: T Type Circuit

Z_{in} can be expressed by (2.15). Since L_{f1} resonates with C_{f1} , there is: $jX_1 + jX_3 = 0$. Therefore, to achieve $\text{Im}(Z_{in}) = 0$, $X_2 + X_3$ must be 0, which means $X_1 = X_2$. In the original circuit, there is: $\frac{1}{j\omega C_1} + j\omega L_1 = j\omega L_{f1}$, and Z_{in} can thus be simplified as $Z_{in} = \frac{\omega^2 L_{f1}^2}{Z_{ref}}$.

$$Z_{in} = jX_1 + (jX_2 + Z_{ref}) \parallel jX_3 = \frac{Z_{ref} \cdot X_3^2}{Z_{ref}^2 + (X_2 + X_3)^2} + j \frac{(X_2 + X_3)(X_1 X_3 + X_1 X_2 + X_2 X_3) + Z_{ref}^2 (X_1 + X_3)}{Z_{ref} + (X_2 + X_3)^2} \quad (2.15)$$

Applying Norton's theorem, current \dot{I}_1 can be calculated by (2.16) and the secondary-side current \dot{I}_2 can then be calculated by (2.17). The output voltage V_{Bat} can be calculated by $V_{Bat} = \frac{\pi}{2\sqrt{2}} I_2 \cdot R_{ac}$. Substituting (2.17) and $V_s = \frac{2\sqrt{2}}{\pi} V_{DC}$, V_{Bat} can also be derived as (2.18). From (2.18), it is known that the battery side voltage V_{Bat} can be controlled by controlling the ratio of M to L_{f1} , therefore the design freedom of this topology is higher than S-S topology. Here, L_{f1} is designed to equal M to meet the output voltage requirement. Table 2.3 concludes the designed parameters of all compensation components of LCC-S topology.

$$\dot{I}_1 = \frac{\dot{V}_s}{j\omega L_{f1}} \quad (2.16)$$

$$\dot{I}_2 = -\frac{j\omega M \dot{I}_1}{R_{ac}} = -\frac{M}{L_{f1}} \frac{\dot{V}_s}{R_{ac}} \quad (2.17)$$

$$V_{Bat} = \frac{M}{L_{f1}} V_{DC} \quad (2.18)$$

L_{f1}	41.95 μH
C_{f1}	83.57 nF
C_1	22.18 nF
C_2	15.94 nF

Table 2.3: LCC-S Compensation Parameters

For primary side, L_{f1} and C_{f1} form a resonant filter connected after V_s . These three components can be considered as a sinusoidal current source with value of I_1 , which is calculated by (2.16). Thus, the voltages and currents on C_1 , L_1 and C_{f1} can be calculated by (2.19). For L_{f1} , the current $\dot{I}_{L_{f1}}$ can be calculated by $\dot{I}_{L_{f1}} = \frac{\dot{V}_s}{Z_{in}}$, and the voltage is $\dot{V}_{L_{f1}} = j\omega L_{f1} \cdot \dot{I}_{L_{f1}}$. For the secondary side, since the current \dot{I}_2 can be obtained in (2.17), the voltages and currents on L_2 and C_2 can be calculated by (2.20).

$$\left\{ \begin{array}{l} \dot{V}_{C_1} = \dot{I}_1 \cdot \frac{1}{j\omega C_1} \\ \dot{I}_{C_1} = \dot{I}_1 \\ \dot{V}_{L_1} = \dot{I}_1 \cdot (j\omega L_1 + Z_{ref}) \\ \dot{I}_{L_1} = \dot{I}_1 \\ \dot{V}_{C_{f1}} = \dot{I}_1 \cdot (j\omega L_1 + \frac{1}{j\omega C_1} + Z_{ref}) = \dot{I}_1 \cdot (j\omega L_{f1} + Z_{ref}) \\ \dot{I}_{C_{f1}} = \dot{V}_{C_{f1}} \cdot j\omega C_{f1} \end{array} \right. \quad (2.19)$$

$$\left\{ \begin{array}{l} \dot{I}_{L_2} = -\dot{I}_2 \\ \dot{V}_{L_2} = j\omega M \dot{I}_1 + j\omega L_2 \dot{I}_2 \\ \dot{I}_{C_2} = -\dot{I}_2 \\ \dot{V}_{C_2} = -\dot{I}_2 \cdot \frac{1}{j\omega C_2} \end{array} \right. \quad (2.20)$$

For non-ideal analyses, the equivalent schematic is shown in figure 2.8. Since the primary and secondary coils of LCC-S topology are the same as S-S topology, the coil resistance are also the same. The efficiency can be obtained by analyzing on two circuits through which the current I_1 and I_2 flow separately and the expression is the same as (2.10).

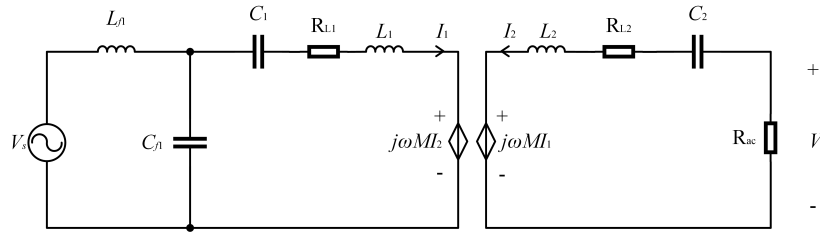
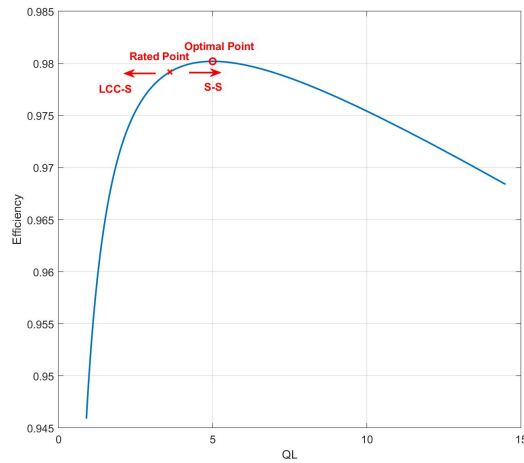


Figure 2.8: Non-ideal LCC-S Schematic

Substitute the parameters from table 2.1 into the optimal load expression (2.12), $Q_{L_{opt}} = 5$. Q_L under rated condition can be calculated by: $Q_L = \frac{\omega L_2}{R_{ac}} = 3.62$. Thus, Q_L under rated condition is close to the optimal Q_L . The efficiencies of S-S and LCC-S under rated condition are the same, due to the same Q_L , but they are different when power is reduced. With power reduction, the equivalent resistance R_{ac} in LCC-S topology increases due to constant output voltage, and Q_L thus decreases. However, the equivalent resistance R_{ac} in S-S topology decreases with power reduction due to the constant output current, and Q_L thus increases. Therefore, when power is reduced based on the rated condition, the efficiency of S-S topology will first rise to the optimal point, and then drop. However, the efficiency of LCC-S topology will keep decreasing, as in figure 2.9.

Figure 2.9: Efficiency- Q_L

Simulation verification of LCC-S topology

The simulation model of LCC-S topology is shown in figure 2.10

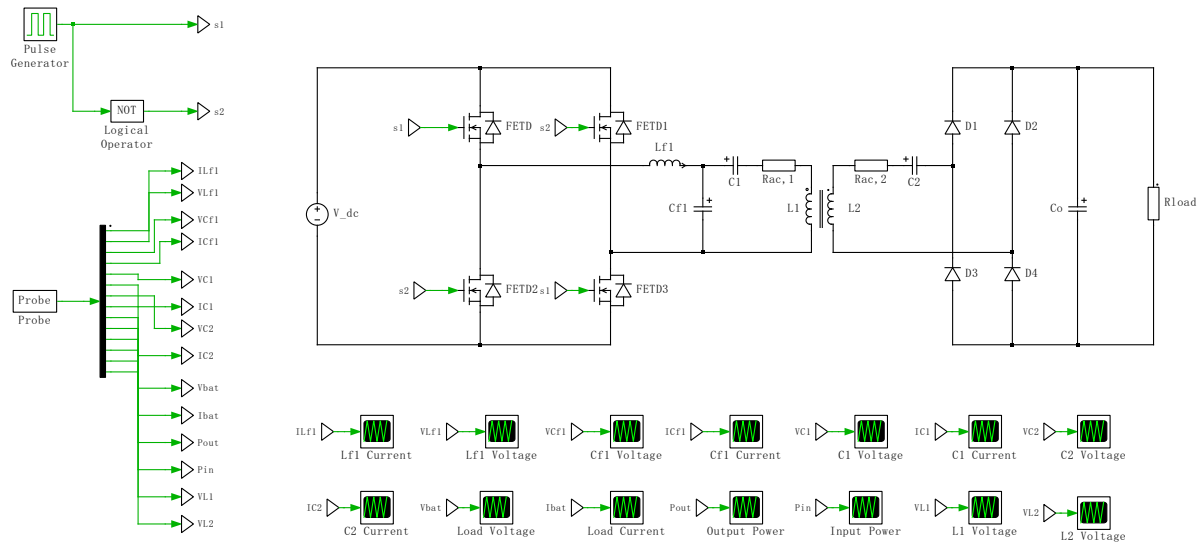


Figure 2.10: LCC-S Simulation model

Simulation Results	$V_{L_{f1}}$ (V)	$V_{C_{f1}}$ (V)	V_{C_1} (V)	V_{L_1} (V)	V_{L_2} (V)	V_{C_2} (V)	$I_{L_{f1}}$ (A)
Calculation Results	754.29	598.48	1923.8	2451.69	2229.52	1832.38	16.4
Simulation Results	351.95	619.07	1918.7	2453.3	1914.6	1845.6	15.71
Simulation Results	$I_{C_{f1}}$ (A)	I_{C_1} (A)	I_{L_1} (A)	I_{L_2} (A)	I_{C_2} (A)	Efficiency	
Calculation Results	28.95	22.4	22.4	15.77	15.77	0.979	
	27.63	22.73	22.73	15.71	15.71	0.979	

Table 2.4: LCC-S Simulation and Calculation Comparison

From table 2.4 it can be seen that only the voltage peaks on L_{f1} and L_2 are inaccurate from the simulation results, while other parameters calculations are quite accurate.

As in the S-S compensation topology, the high order harmonics can cause an increase on the voltage peaks of the resonant inductors. The introduced resonant inductor voltage peak calculation method in section 3.1.2 can eliminate this calculation error on voltage peaks of resonant inductors.

2.3.2. LCC-LCC topology

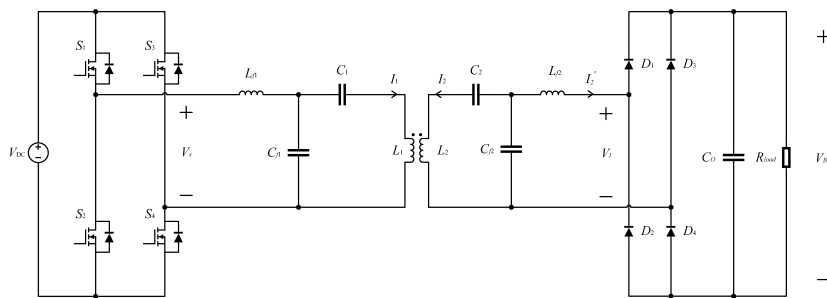


Figure 2.11: LCC-LCC Topology

The LCC-LCC topology which features constant current output is shown in figure 2.11. Compensation inductor L_{f1} is designed to resonate with C_{f1} to provide constant primary coil current $\dot{I}_1 = \frac{\dot{V}_s}{j\omega L_{f1}}$, which then produces a constant current controlled voltage source $j\omega M \dot{I}_1$ at the secondary side. C_{f2} is designed to resonate with the equivalent electrical parameter of $j\omega L_2 + \frac{1}{j\omega C_2}$ to provide a constant current $\dot{I}'_2 = \frac{j\omega M \dot{I}_1}{j\omega L_2 + \frac{1}{j\omega C_2}}$ on L_{f2} . As analyzed in section 2.3.1, in a T type circuit to achieve ZPA,

$\frac{1}{j\omega C_1} + j\omega L_1 = j\omega L_{f1}$ and $j\omega L_2 + \frac{1}{j\omega C_2} = j\omega L_{f2}$ should be satisfied. Considering the rms value of battery-side current $I_{Bat} = \frac{2\sqrt{2}}{\pi} I'_2$, the expression of I_{Bat} regarding V_s is given by (2.21), which can be applied on controlling output current. Since the primary and secondary side circuits are almost symmetrical, for simplicity, $L_{f1} = L_{f2}$ [12]. Compensation inductors L_{f1} and L_{f2} can be calculated by (2.22).

$$I_{Bat} = \frac{2\sqrt{2}}{\pi} \frac{V_s M}{\omega L_{f1} L_{f2}} \quad (2.21)$$

$$L_{f1} = L_{f2} = \sqrt{\frac{2\sqrt{2}}{\pi} \frac{V_s M}{\omega I_{Bat}}}. \quad (2.22)$$

The designed compensation parameters are in table 2.5 .

L_{f1}	50.47 μH
C_{f1}	69.47 nF
C_1	23.45 nF
C_2	20.68 nF
C_{f2}	69.47 nF
L_{f2}	50.47 μH

Table 2.5: LCC-LCC Compensation Parameters

To analyze the voltage and current on each component, the simplified LCC-LCC schematic is shown in figure 2.12. The current and voltage on C_1 can be calculated by (2.23). The generated secondary current controlled voltage source is $j\omega M \dot{I}_1 = \frac{M}{L_{f1}} \dot{V}_s$, thus the current and voltage on L_{f2} can be calculated by (2.24). The battery-side load resistance R_{load} can be converted to R_{ac} as mentioned before. To obtain the secondary coil current I_2 , R_{ac} is further converted as Z_{sec} at the left side of the LCC compensation as mentioned in section 2.3.1, and the input impedance Z_{sec} of the secondary circuit is given by $Z_{sec} = \frac{\omega^2 L_{f2}^2}{R_{ac}}$. Therefore, the current and voltage on C_2 can be calculated by (2.25). Using current I_2 and I'_2 , the voltage and current stresses on L_2 and C_{f2} can be calculated by (2.26) and (2.27).

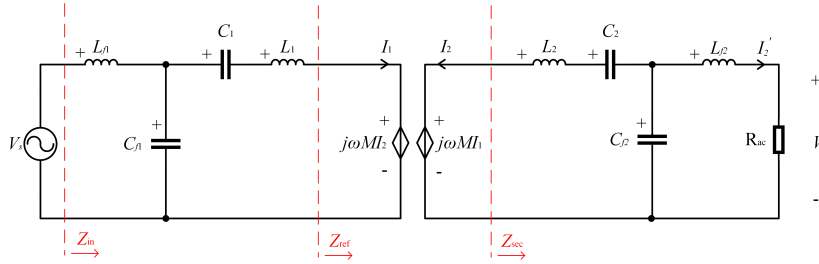


Figure 2.12: LCC-LCC Schematic

$$\begin{cases} I_1 = \frac{\dot{V}_s}{j\omega L_{f1}} \\ \dot{V}_{C_1} = I_1 \cdot \frac{1}{j\omega C_1} \end{cases} \quad (2.23)$$

$$\begin{cases} I'_2 = \frac{\frac{M}{L_{f1}} \dot{V}_s}{j\omega L_2 + \frac{1}{j\omega C_2}} = \frac{\dot{V}_s M}{j\omega L_{f1} L_{f2}} \\ \dot{V}_{L_{f2}} = I'_2 \cdot j\omega L_{f2} = \frac{M}{L_{f1}} \dot{V}_s \end{cases} \quad (2.24)$$

$$\begin{cases} I_{C_2} = -I_2 = -\frac{M \dot{V}_s}{L_{f1} Z_{sec}} \\ \dot{V}_{C_2} = I_{C_2} \cdot \frac{1}{j\omega C_2} \end{cases} \quad (2.25)$$

$$\begin{cases} I_{L_2} = -I_2 = -\frac{M\dot{V}_s}{L_{f1}Z_{sec}} \\ \dot{V}_{L_2} = j\omega M\dot{I}_1 + j\omega L_2\dot{I}_2 \end{cases} \quad (2.26)$$

$$\begin{cases} \dot{V}_{C_{f2}} = \dot{I}_2' (j\omega L_{f2} + R_{ac}) \\ \dot{I}_{C_{f2}} = \dot{V}_{C_{f2}} \cdot j\omega C_{f2} \end{cases} \quad (2.27)$$

The secondary impedance Z_{sec} can be referred to the primary side using (2.5), which is $Z_{sec} = \frac{\omega^2 L_{f2}^2}{R_{ac}}$ and Z_{ref} in LCC-LCC topology is $Z_{ref} = \frac{\omega^2 M^2}{Z_{sec}} = \frac{M^2}{L_{f2}^2} R_{ac}$. Z_{ref} can be further converted to the left side of the primary-side LCC compensation and this equivalent impedance is $Z_{in} = \frac{\omega^2 L_{f1}^2}{Z_{ref}} = \frac{\omega^2 L_{f1}^2 L_{f2}^2}{M^2 R_{ac}}$. Therefore, the input current \dot{I}_{in} is $\dot{I}_{in} = \frac{\dot{V}_s}{Z_{in}}$ and the primary-side components stresses can be solved as follows.

$$\begin{cases} \dot{I}_{L_{f1}} = \dot{I}_{in} \\ \dot{V}_{L_{f1}} = \dot{I}_{L_{f1}} \cdot j\omega L_{f1} \end{cases} \quad (2.28)$$

$$\begin{cases} \dot{V}_{C_{f1}} = \dot{I}_1 \cdot \left(\frac{1}{j\omega C_1} + j\omega L_1 + Z_{ref} \right) \\ \dot{I}_{C_{f1}} = \dot{V}_{C_{f1}} \cdot j\omega C_{f1} \end{cases} \quad (2.29)$$

$$\begin{cases} \dot{I}_{L_1} = \dot{I}_1 \\ \dot{V}_{L_1} = \dot{I}_1 \cdot (j\omega L_1 + Z_{ref}) \end{cases} \quad (2.30)$$

To calculate the efficiency of LCC-LCC compensation, the non-ideal schematic is shown in figure 2.13. When R_{ac} is converted to the secondary-side LCC compensation network as Z_{sec} , this schematic is the same as LCC-S topology. Thus, after substituting R_{ac} with Z_{sec} , the efficiency of LCC-LCC can be calculated in the same way as SS and LCC-S. The Q'_L of LCC-LCC topology under rated condition is $Q'_L = \frac{\omega L_2}{Z_{sec}} = \frac{L_2 R_{ac}}{\omega L_{f2}^2} = 5.24$. The Q'_L of LCC-LCC compensation is closer to the optimal point than the ones of SS and LCC-S, thus the efficiency is also larger, which is 0.98.

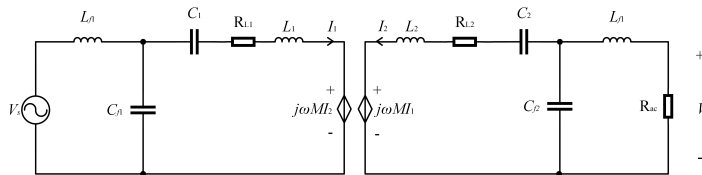


Figure 2.13: Non-ideal LCC-LCC Schematic

Simulation verification of LCC-LCC topology

A double-sided LCC topology simulation is made in PLECS to verify the analyses above. The simulation is shown in figure 2.14.

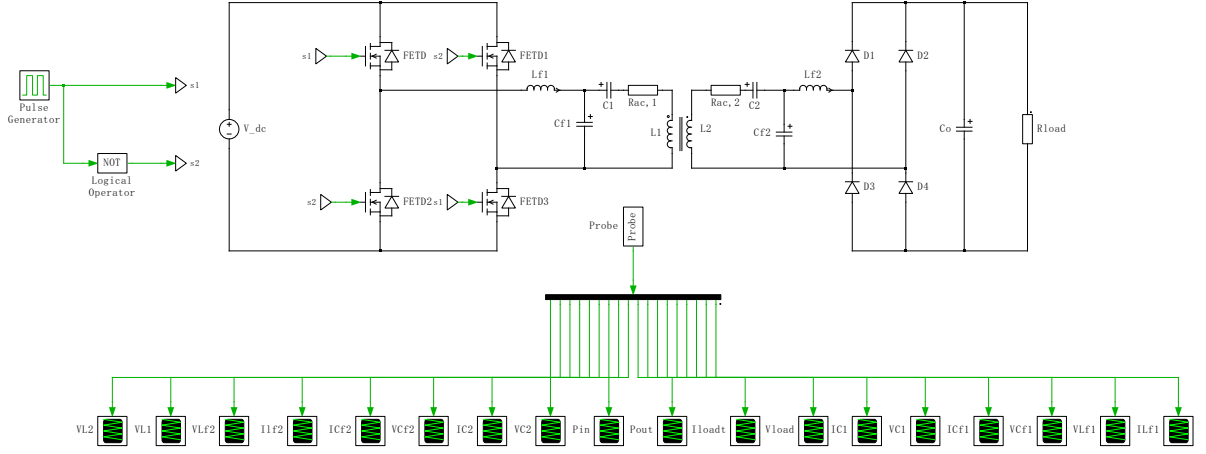


Figure 2.14: LCC-LCC Simulation model

Simulation Results	$V_{L_{f1}}$ (V)	$V_{C_{f1}}$ (V)	V_{C_1} (V)	V_{L_1} (V)	V_{L_2} (V)	V_{C_2} (V)	$V_{C_{f2}}$ (V)
Calculation Results	787.98	739.43	1510.87	2188.97	2302.02	1639.84	733.23
Simulation Results	423.38	662.29	1509.00	2062.30	2260.20	1710.90	662.30
Simulation Results	$V_{L_{f2}}$ (V)	$I_{L_{f1}}$ (A)	$I_{C_{f1}}$ (A)	I_{C_1} (A)	I_{L_1} (A)	I_{L_2} (A)	I_{C_2} (A)
Calculation Results	788.20	16.63	28.77	18.79	18.79	18.00	18.00
Simulation Results	909.30	15.71	24.57	18.90	18.90	18.90	18.90
Simulation results	$I_{C_{f2}}$ (A)	$I_{L_{f2}}$ (A)	Efficiency				
Calculation results	28.64	17.22	0.98				
	24.57	15.71	0.98				

Table 2.6: LCC-LCC Simulation and Calculation Comparison

From table 2.6, it can be seen that high order harmonics have a larger impact on the fundamental analysis method in LCC-LCC topology, and the calculation errors on all components appear to increase a little. In particular, for voltage stresses, the calculation errors on peak voltage on the filter inductors L_{f1} and L_{f2} are still the largest. As for current stresses, the calculation errors on C_{f1} and C_{f2} are relatively large.

2.3.3. S-LCC topology

In S-LCC topology, C_1 is designed to resonate with L_1 , thus $\dot{V}_s = j\omega M \dot{I}_2$, then \dot{I}_2 can be calculated by (2.31). The secondary-side coil can therefore be regarded as a constant AC current source with value of I_2 . L_{f2} resonates with C_{f2} to produce a constant output voltage V_l , which can be calculated by applying Thevenin's theorem: $V_l = I_2 \cdot \frac{1}{\omega C_{f2}}$. Since $I_2 = \frac{V_s}{\omega M}$ and $\omega L_{f2} = \frac{1}{\omega C_{f2}}$, the expression of V_l is given by (2.32). Substitute $V_s = \frac{2\sqrt{2}}{\pi} V_{DC}$ and $V_l = \frac{2\sqrt{2}}{\pi} V_{Bat}$ in (2.32), there is $V_{Bat} = \frac{L_{f2}}{M} V_{DC}$, which can be applied on controlling the output voltage. Since $V_{Bat} = V_{DC}$, L_{f2} is designed as $L_{f2} = M$. To achieve ZPA, there is $j\omega L_2 + \frac{1}{j\omega C_2} = j\omega L_{f2}$. Based on these, the compensation parameters are summarized in table 2.7.

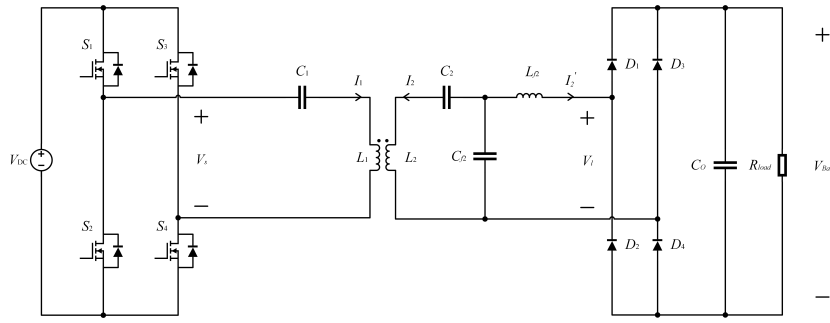


Figure 2.15: S-LCC Topology

$$\dot{I}_2 = \frac{\dot{V}_s}{j\omega M} \quad (2.31)$$

$$V_l = \frac{L_{f2}}{M} V_s \quad (2.32)$$

C_1	17.53 nF
C_2	19.69 nF
C_{f2}	83.57 nF
L_{f2}	41.95 μ H

Table 2.7: S-LCC Compensation Parameters

The topology is simplified as figure 2.16. For the secondary side, since current I_2 is constant and can be calculated using (2.31), the voltage and current on C_2 can be calculated by (2.33). Current I_2' can be calculated by $I_2' = \frac{\dot{V}_l}{R_{ac}} = \frac{\dot{V}_s L_{f2}}{R_{ac} M}$, where R_{ac} can be calculated by (2.3). R_{ac} can be converted at the input of the T-type circuit as mentioned in section 2.3.1, the new equivalent impedance Z_{sec} is $Z_{sec} = \frac{\omega^2 L_{f2}^2}{R_{ac}}$. Z_{sec} can be then converted to the primary side as Z_{ref} , which can be calculated by $Z_{ref} = \frac{\omega^2 M^2}{Z_{sec}} = \frac{M^2}{L_{f2}^2} R_{ac}$. Therefore, the primary-side current I_1 can be calculated as $I_1 = \frac{\dot{V}_s}{Z_{ref}}$. Based on these, the voltage and current on L_2 , C_{f2} and L_{f2} can be calculated by (2.34), (2.35) and (2.36).

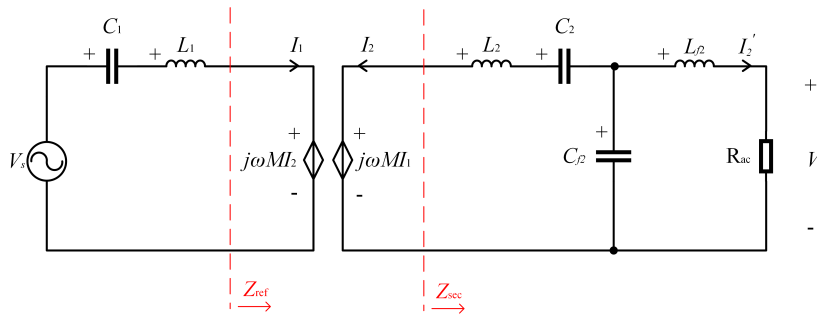


Figure 2.16: S-LCC Schematic

$$\begin{cases} \dot{I}_{C_2} = -\dot{I}_2 \\ \dot{V}_{C_2} = -\dot{I}_2 \cdot \frac{1}{j\omega C_2} \end{cases} \quad (2.33)$$

$$\begin{cases} \dot{I}_{L_2} = -\dot{I}_2 = -\frac{\dot{V}_s}{j\omega M} \\ \dot{V}_{L_2} = \dot{I}_2 \cdot j\omega L_2 + j\omega M \dot{I}_1 \end{cases} \quad (2.34)$$

$$\begin{cases} \dot{V}_{C_{f2}} = \dot{I}'_2 \cdot (j\omega L_{f2} + R_{ac}) \\ \dot{I}_{C_{f2}} = \dot{V}_{C_{f2}} \cdot j\omega C_{f2} \end{cases} \quad (2.35)$$

$$\begin{cases} \dot{V}_{L_{f2}} = \dot{I}'_2 \cdot j\omega L_{f2} \\ \dot{I}_{L_{f2}} = \dot{I}'_2 \end{cases} \quad (2.36)$$

The current and voltage on primary-side components are calculated as follows:

$$\begin{cases} \dot{I}_{C_1} = \dot{I}_1 \\ \dot{V}_{C_1} = \dot{I}_1 \cdot \frac{1}{j\omega C_1} \end{cases} \quad (2.37)$$

$$\begin{cases} \dot{I}_{L_1} = \dot{I}_1 \\ \dot{V}_{L_1} = \dot{I}_1 \cdot (j\omega L_1 + Z_{ref}) \end{cases} \quad (2.38)$$

For efficiency calculation, the S-LCC topology can be calculated in the same way as LCC-LCC. R_{ac} is first converted as Z_{sec} , then Q'_L can be calculated as $Q'_L = \frac{\omega L_2}{Z_{sec}} = \frac{L_2 R_{ac}}{\omega L_{f2}^2} = 7.59$, which is at the right side of the optimal load, and the corresponding efficiency is 0.978. Since the output voltage of S-LCC topology is constant, when output power decreases, R_{ac} increases and Q'_L increases. From figure 2.9 it can be found that the efficiency will therefore drop continuously.

Simulation verification of S-LCC topology

The simulation of S-LCC topology is shown in 2.17.

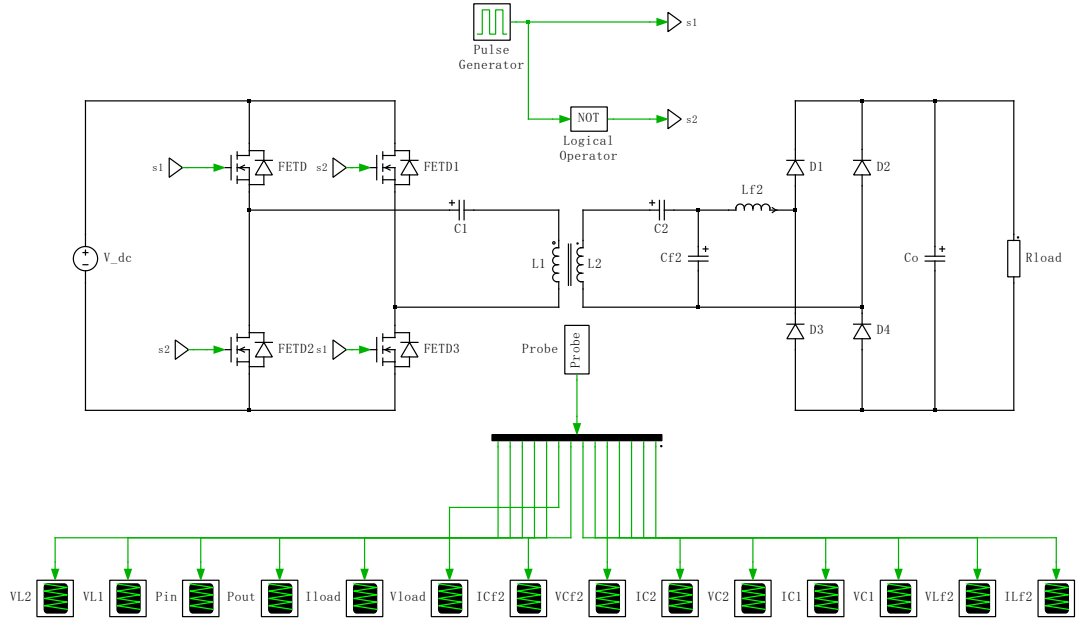


Figure 2.17: S-LCC Simulation model

	V_{C_1} (V)	V_{L_1} (V)	V_{L_2} (V)	V_{C_2} (V)	$V_{C_{f2}}$ (V)	$V_{L_{f2}}$ (V)	I_{C_1} (A)
Simulation Results	1806.98	2207.00	2842.07	2167.00	731.47	750.56	16.31
Calculation Results	1677.60	1753.20	2693.90	2161.60	619.00	351.91	15.71
	I_{L_1} (A)	I_{L_2} (A)	I_{C_2} (A)	$I_{C_{f2}}$ (A)	$I_{L_{f2}}$ (A)	Efficiency	
Simulation Results	16.31	22.40	22.40	34.00	18.77	0.978	
Calculation Results	15.71	22.73	22.73	27.63	15.71	0.979	

Table 2.8: S-LCC Simulation and Calculation Comparison

As can be seen from the table 2.8, for voltage stresses, the maximum calculation error still occurs on the resonant inductors L_1 and L_{f2} . For current stresses, due to the high-order harmonic current existing on these two components, the current peaks on C_{f2} and L_{f2} obtained from analysis are not so accurate.

2.4. Novel high-order composite compensation topologies

In addition to the widely used high order composite compensation topologies introduced in section 2.3, some novel high-order composite compensation topologies have been proposed. These topologies aim to solve some shortcomings in the conventional two-element topologies or high-order composite topologies. However, while addressing these shortcomings, some new problems have also arisen.

In this section, several novel high-order composite topologies are introduced, their unique features are analyzed and some of their problems under rated conditions are illustrated.

2.4.1. LC-S topology

The LC-S topology is proposed in [15]. Compared to the S-S compensation topology, the LC-S topology offers increased design freedom while maintaining the advantage that the resonant frequency is independent of the load and mutual inductance. In addition, it needs fewer compensation components than the high-order composite compensation topologies in section 2.3, resulting in lower cost and compensation components power loss, and smaller system size.

Figure 2.18 shows the LC-S topology compensation which features constant current output. To analyse its compensation method, the analytical circuit is shown in figure 2.19, where C_{f1} is split into C'_{f1} and C''_{f1} . C'_{f1} resonates with L_{f1} to provide a constant current $\frac{\dot{V}_s}{j\omega L_{f1}}$, which is then converted to constant voltage by the CL resonant tank. Therefore, this LC compensation produces a constant output voltage $\frac{\dot{V}_s}{j\omega L_{f1}} \cdot \frac{1}{j\omega C''_{f1}}$. Substitute $C''_{f1} = \frac{1}{\omega^2 L_1}$, the original expression can also be written as $-\frac{L_1}{L_{f1}} \dot{V}_s$, therefore there is (2.39), which can be used to control output current.

The rms value of I_2 is: $I_2 = \frac{\pi}{2\sqrt{2}} I_{Bat}$, the compensation parameter L_{f1} can be designed as $L_{f1} = \frac{V_s L_1}{\omega M I_2}$. Based on the compensation method mentioned above, C_{f1} can be designed using (2.40). C_2 is designed for realizing ZPA. According to [15], C_2 is designed by (2.41). All the compensation parameters are summarized in table 2.9.

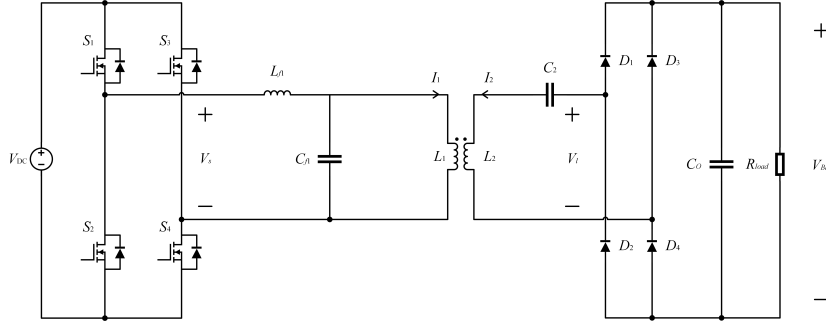


Figure 2.18: LC-S Topology

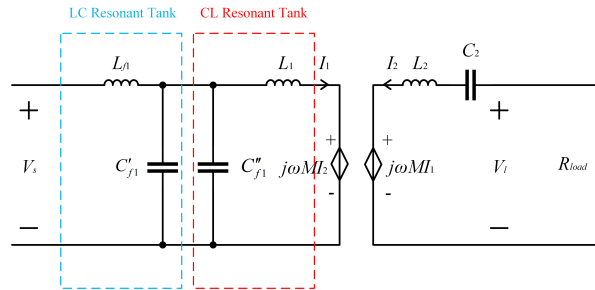


Figure 2.19: Analytical Circuit of LC-S Topology

$$\dot{I}_2 = -\frac{L_1}{j\omega M L_{f1}} \dot{V}_s \quad (2.39)$$

L_{f1}	289.42 μH
C_{f1}	29.64 nF
C_2	17.67 nF

Table 2.9: LC-S Compensation Parameters

$$\begin{cases} \frac{1}{j\omega C''_{f1}} + j\omega L_1 = 0 \\ \frac{1}{j\omega C'_{f1}} + j\omega L_{f1} = 0 \\ C_{f1} = C'_{f1} + C''_{f1} \end{cases} \quad (2.40)$$

$$C_2 = \frac{L_1 C'_{f1}}{\omega^2 (L_2 L_1 C'_{f1} - M^2 C_{f1})} \quad (2.41)$$

The simplified schematic is shown in figure 2.20, where Z_{sec} is the equivalent secondary-side impedance, Z_{ref} is Z_{sec} referred to the primary side, Z_C stands for the equivalent impedance of L_1 , Z_{ref} and C_{f1} , and Z_{in} is the input impedance of the circuit. These impedance are given in (2.42).

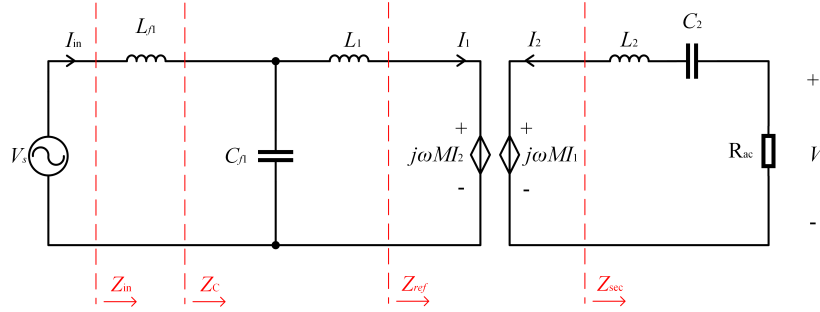


Figure 2.20: LC-S Schematic

$$\begin{cases} Z_{sec} = R_{ac} + \frac{1}{j\omega C_2} + j\omega L_2 \\ Z_{ref} = \frac{\omega^2 M^2}{Z_{sec}} \\ Z_C = (j\omega L_1 + Z_{ref}) \parallel \frac{1}{j\omega C_{f1}} \\ Z_{in} = j\omega L_{f1} + Z_C \end{cases} \quad (2.42)$$

As mentioned before, the output of the CL resonant tank is a constant voltage $-\frac{L_1}{L_{f1}} \dot{V}_s$, current i_1 can thus be calculated as (2.43). Current i_{in} can be calculated by $i_{in} = \frac{\dot{V}_s}{Z_{in}}$. The stress on each component can be obtained with these currents, as shown in (2.44).

$$i_1 = -\frac{L_1 \dot{V}_s}{L_{f1} Z_{ref}} \quad (2.43)$$

$$\begin{cases} i_{L_{f1}} = i_{in} \\ \dot{V}_{L_{f1}} = i_{in} \cdot j\omega L_{f1} \\ \dot{V}_{C_{f1}} = i_1 \cdot (j\omega L_1 + Z_{ref}) \\ \dot{V}_{C_{f1}} = \dot{V}_{C_{f1}} \cdot j\omega C_{f1} \\ i_{L_1} = i_1 \\ \dot{V}_{L_1} = \dot{V}_{C_{f1}} \\ i_{L_2} = -i_2 \\ \dot{V}_{L_2} = j\omega M \dot{i}_1 + j\omega L_2 \cdot \dot{i}_2 \\ \dot{V}_{C_2} = -\dot{i}_2 \\ \dot{V}_{C_2} = -\dot{i}_2 \cdot \frac{1}{j\omega C_2} \end{cases} \quad (2.44)$$

For efficiency calculation, the non-ideal schematic is shown in figure 2.21, where R_{L_1} and R_{L_2} are calculated by (2.9), $Z'_{sec} = R_{L_2} + R_{ac} + j\omega L_2 + \frac{1}{j\omega C_2}$ and $Z'_{ref} = \frac{\omega^2 M^2}{Z'_{sec}}$. Thus, the efficiency of the primary circuit is given by $\eta_1 = \frac{\text{Re}(Z'_{ref})}{\text{Re}(Z'_{ref}) + R_{L_1}}$ and the efficiency of the secondary circuit is given by $\eta_2 = \frac{R_{ac}}{R_{ac} + R_{L_2}}$. The total efficiency is $\eta = \eta_1 \cdot \eta_2 = 0.977$, which is very close to the topologies mentioned before.

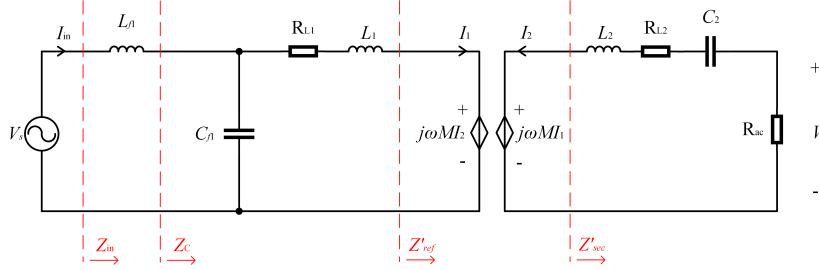


Figure 2.21: Non-ideal LC-S Schematic

Simulation verification of LC-S topology

The simulation model of LC-S compensation topology is shown in figure 2.22.

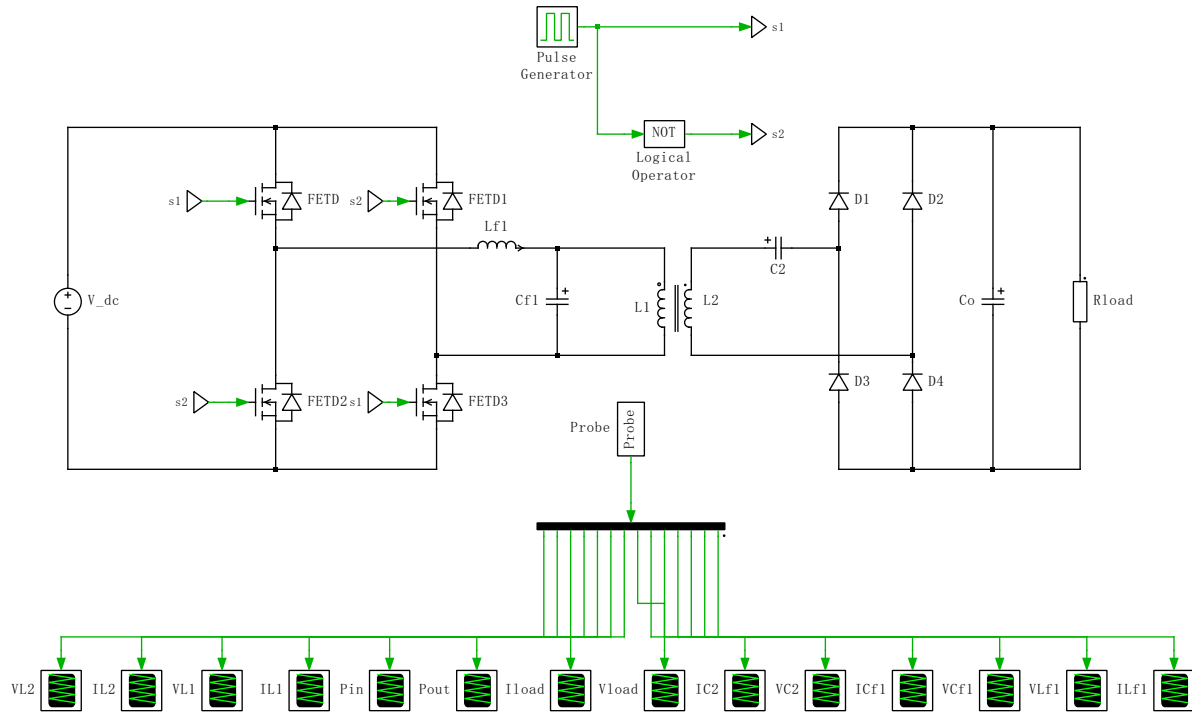


Figure 2.22: LC-S Simulation model

	$V_{L_{f1}}$ (V)	$V_{C_{f1}}$ (V)	V_{L_1} (V)	V_{L_2} (V)	V_{C_2} (V)	$I_{L_{f1}}$ (A)
Simulation Results	2818.20	2503.42	2503.42	2059.93	1660.90	15.65
Calculation Results	2428.00	2480.80	2480.80	1741.10	1665.00	15.71
	$I_{C_{f1}}$ (A)	I_{L_1} (A)	I_{L_2} (A)	I_{C_2} (A)	Efficiency	
Simulation Results	39.86	24.40	15.82	15.82	0.977	
Calculation Results	39.28	24.12	15.71	15.71	0.978	

Table 2.10: LC-S Simulation and Calculation Comparison

In table 2.10, the largest calculation errors are on the voltage peaks of resonant inductors L_{f1} and

L_2 . Other simulation results are close to the calculation results obtained from the analysis above.

2.4.2. S/SP topology

In [16], a novel S/SP compensation topology is proposed. Compared to the S-S topology, the S/SP topology features with better output controllability, and still maintains relatively high system efficiency.

The S/SP topology is shown in figure 2.23. To analyze its compensation method, the T type model is adopted, which is shown in figure 2.24, where L_{1s} is the primary leakage inductance calculated by $L_{1s} = L_1 - M$, and L_{2s} is the secondary leakage inductance calculated by $L_{2s} = L_2 - M$. Compensation capacitor C_1 resonates with L_{1s} , C_2 resonates with L_{2s} , and C_{f2} resonates with M ensuring ZPA realization of the circuit. Thus, $V_l = V_s$, and the output voltage is independent of the load.

All the compensation components values are included in table 2.11. From the analysis above, it is clear that the compensation design is dependent on the mutual inductance M , thus when misalignment happens, this topology does not work properly. Besides, the output voltage is directly controlled by the input, losing the design freedom on the output control.

C_1	22.18 nF
C_2	19.69 nF
C_{f2}	83.57 nF

Table 2.11: S/SP Compensation Parameters

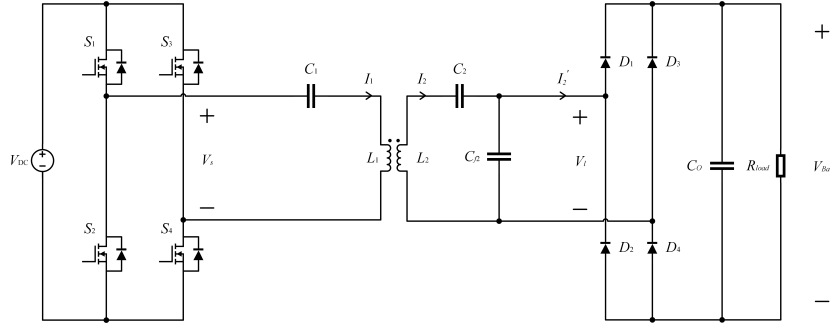


Figure 2.23: S/SP Topology

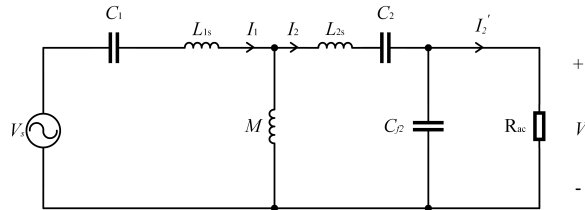


Figure 2.24: S/SP Schematic

2.4.3. LC-CL Topology

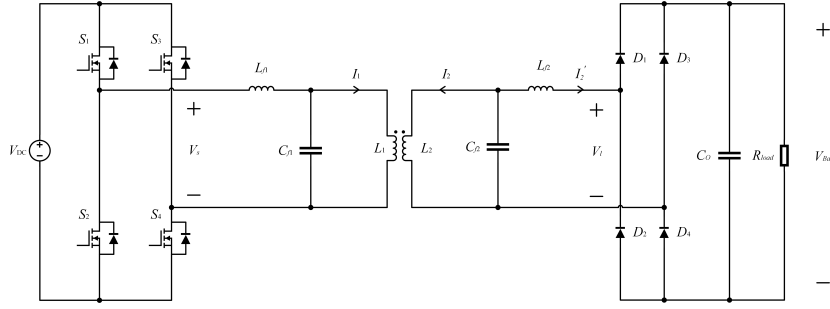


Figure 2.25: LC-CL Topology

A novel LC-CL topology is proposed in [17], which looks the same as LCL-LCL, but with a different tuning method. This topology offers better constant current output characteristic than S-S topology, while also providing more design freedom. The topology of LC-CL is shown in figure 2.25, and its analytical circuit is shown in figure 2.26, where C_{f1} is split into C'_{f1} and C''_{f1} , and L_{1s} , L_{2s} are the leakage inductance of the coils as mentioned in section 2.4.2. C'_{f1} resonates with L_{f1} to generate a constant current, and then this constant current is transferred to a constant voltage with the CL resonant tank. Finally, the constant voltage is transferred into constant current output with the LC resonant tank at the secondary side, which can be calculated by $I'_2 = j \frac{\dot{V}_s L_{1s}}{\omega L_{f1} L_{2s}}$, with which the output current can be

controlled. Since $I_{Bat} = \frac{2\sqrt{2}}{\pi} I'_2$, parameter L_{f1} can be designed as $L_{f1} = \frac{2\sqrt{2}}{\pi} \frac{V_s L_{1s}}{I_{Bat} \omega L_{2s}}$ to meet the output current requirement. Based on the compensation method introduced above, the compensation capacitors are given by 2.45.

In [17], an efficiency-based optimisation algorithm is also proposed, which can find an optimal L_{f2} to achieve the highest efficiency. The algorithm iteratively finds the L_{f2} value that maximizes the efficiency of the system by calculating the ESR of each component in the range of L_{f2} varying from 0 to L_{f2up} , where L_{f2up} can result in ZPA. In this article, L_{f2} is directly set to be the value that implements ZPA, which is calculated by $L_{f2} = \frac{L_{2s}^2 L_{1s} M + L_{2s} L_{1s}^2 M + L_{2s}^2 L_{1s}^2 + L_{2s}^2 L_{f1} M}{M L_{1s}^2}$. All the compensation components parameters are included in table 2.12.

$$\begin{cases} C'_{f1} = \frac{1}{\omega^2 L_{f1}} \\ C''_{f1} = \frac{1}{\omega^2 L_{1s}} \\ C_{f1} = C'_{f1} + C''_{f1} \\ C_{f2} = \frac{1}{\omega^2 L_{2s}} \end{cases} \quad (2.45)$$

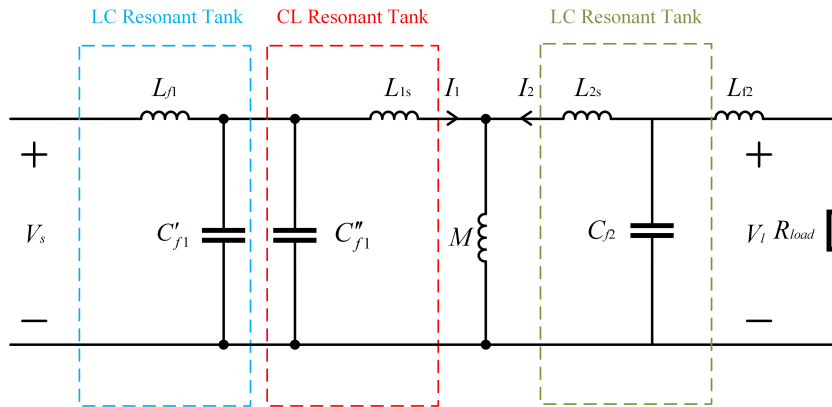


Figure 2.26: Analytical Circuit of LC-CL Topology

L_{f1}	C_{f1}	C_{f2}	L_{f2}
53.88 μH	87.24 nF	19.69 nF	1200 μH

Table 2.12: LC-CL Compensation Parameters

As can be seen from the table, L_{f2} in this topology is too large, and all the components parameters are dependent on M , thus same problem in section 2.4.2 will happen under misalignment.

2.4.4. LCL-S Topology

The LCL-S topology is shown in figure 2.27 [18]. The compensation principle of LCL-S topology is the same as LCC-S topology, however, the compensation capacitor C_1 is replaced by L_{f2} . Since L_{f1} resonates with C_{f1} , the current I_1 is calculated by $I_1 = \frac{\dot{V}_s}{j\omega L_{f1}}$ and the generated current controlled voltage source at the secondary side is $j\omega M I_1 = \frac{M \dot{V}_s}{L_{f1}}$. Thus, the output voltage is deduced as $V_{Bat} = \frac{\pi}{2\sqrt{2}} \frac{M V_s}{L_{f1}} = \frac{M V_{DC}}{L_{f1}}$. As mentioned in section 2.3.1, to achieve ZPA, there is $L_{f1} = L_{f2} + L_1$. Therefore, L_{f1} is larger than L_1 and much larger than M . The output voltage is much smaller than the input voltage, which is not acceptable for rated condition.

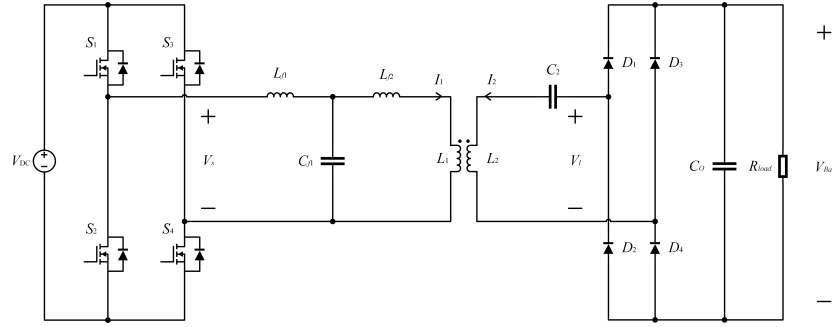


Figure 2.27: LCL-S Topology

2.5. Compensation topologies comparison

Based on the topologies analyses in the above sections, this section compares all the topologies from components stresses, efficiency and misalignment behaviour under rated condition. As analyzed in sections 2.4.2 and 2.4.3, both S/SP and LC-CL topologies compensation methods are associated with mutual inductance in achieving ZPA, which cannot maintain ZPA under misalignment, and the compensation design is relatively complex, so these two topologies are not considered for comparisons in this section. The LCL-S topology is also not considered because the design freedom is too low to meet the WPT system rated condition requirements.

A table summarizing all the comparison results is given at the end of this section.

2.5.1. Components stress comparison

The voltage and current stress on each component of different topologies are obtained and shown in Figure 2.28. The voltage and current peaks are used here given the need to consider breakdown in the design.

For voltage stress, the voltages on each component of all topologies are close to each other, with the voltage across L_2 of S-LCC being relatively high.

For current stress, the current on C_{f1} in LC-S is too high. Therefore, the LC-S topology is not suitable for the specified rated condition.

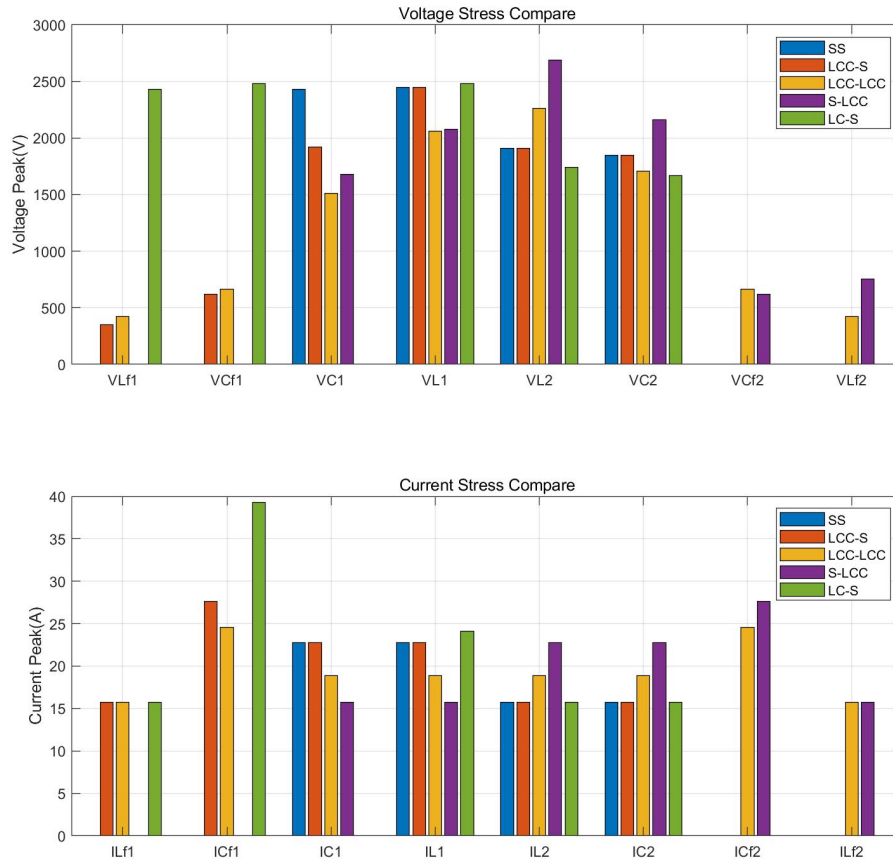


Figure 2.28: Voltage and Current Stress Comparison

2.5.2. Misalignment behaviour comparison

- Misalignment under constant output power and input voltage

When the primary-side and secondary-side coils are horizontally misaligned, the mutual inductance will decrease. Assuming a constant output power with a fixed input voltage source, figure 2.29 and 2.30 reflect the variation of the voltage and current stress on each component in different topologies under misalignment.

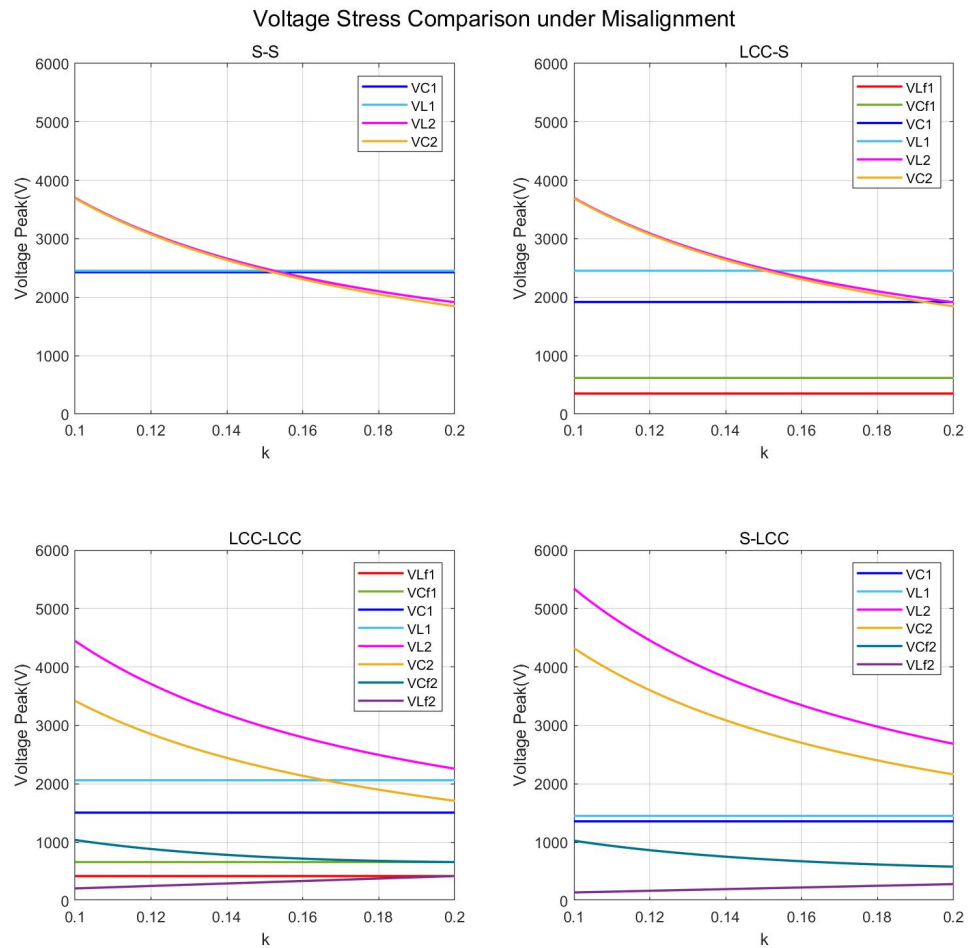


Figure 2.29: Voltage Stress Comparison under Misalignment

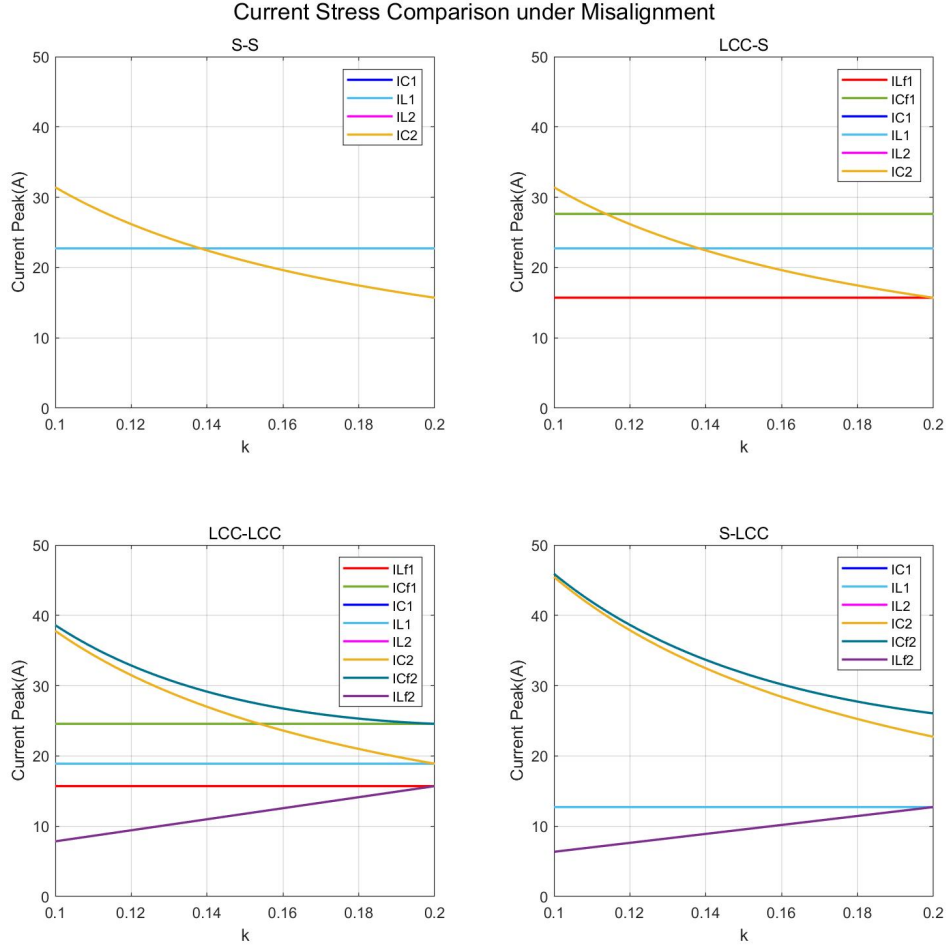


Figure 2.30: Current Stress Comparison under Misalignment

From the plots, it can be seen that L_2 and C_2 in LCC-LCC and S-LCC have higher voltage stresses. As for current stresses, the currents on C_{f2} , L_2 and C_2 of LCC-LCC topology and S-LCC topology are larger under misalignment.

In LCC-LCC topology, the output current can be calculated by (2.21). Therefore, R_{ac} under misalignment can be written as $R_{ac} = \frac{8}{\pi^2} \frac{P}{I_{Bat}^2} = \frac{P \omega^2 L_{f1}^2 L_{f2}^2}{V_s^2 M^2}$. Substituting the expression of R_{ac} into the expression of Z_{sec} , and then using (2.26), the expression of current I_{L2} can be deduced as (2.46). Current I_{L2} is inversely proportional to M , thus the current and voltage on L_2 and C_2 are very large under misalignment. In S-LCC topology, the current and voltage on L_2 and C_2 are obtained in (2.34) and (2.33), which are also inversely proportional to M and increased a lot under misalignment.

$$I_{L2} = \frac{PL_{f1}}{V_s M} \quad (2.46)$$

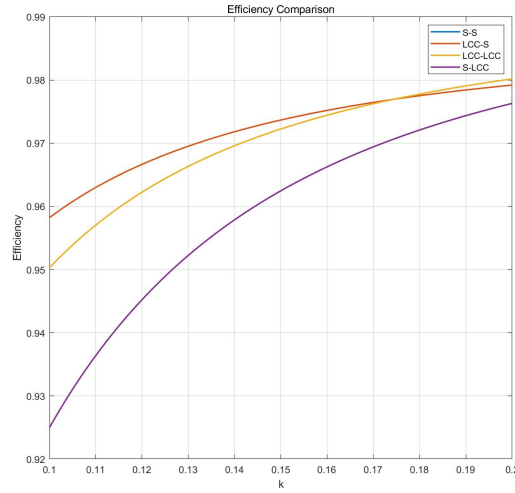


Figure 2.31: Efficiency Comparison under Misalignment

Under misalignment, the efficiency variations for different topologies is shown in figure 2.31, which are calculated based on the analyses in previous sections. The efficiency of S-S is the same as LCC-S, due to the same calculation method and the same R_{ac} under misalignment. From the figure, it can be seen that the efficiency of S-LCC is lower compared with other topologies under misalignment.

- Misalignment under constant output power and output voltage

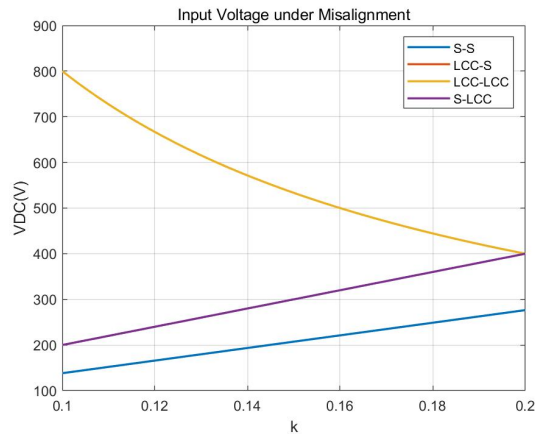


Figure 2.32: Input Voltage under Misalignment

If the output voltage and power are both fixed, the input voltage needs to be adjusted under misalignment. Figure 2.32 shows how input voltages are adjusted under misalignment for different compensation topologies. Both LCC-LCC and LCC-S topologies require the input voltage to increase inversely as the mutual inductance decreases, and their curves overlap. This is because both topologies have an LCC topology on the primary side, which is equivalent to a current source proportional to the input voltage V_{DC} , and generates a voltage source on the secondary coil proportional to the mutual inductance, so the input voltage needs to increase inversely as the mutual inductance decreases to keep the output voltage constant.

In this case, the voltage/current stress on each component and efficiency of different compensation topologies are shown in figure 2.33, 2.34 and 2.35. As can be seen from the figures, when the output voltage and power are constant and the system is under misalignment, the voltage/current peaks of LCC-S and S-S are higher, and the efficiency of these two topologies are lower (S-S efficiency curve overlap with LCC-S efficiency curve).

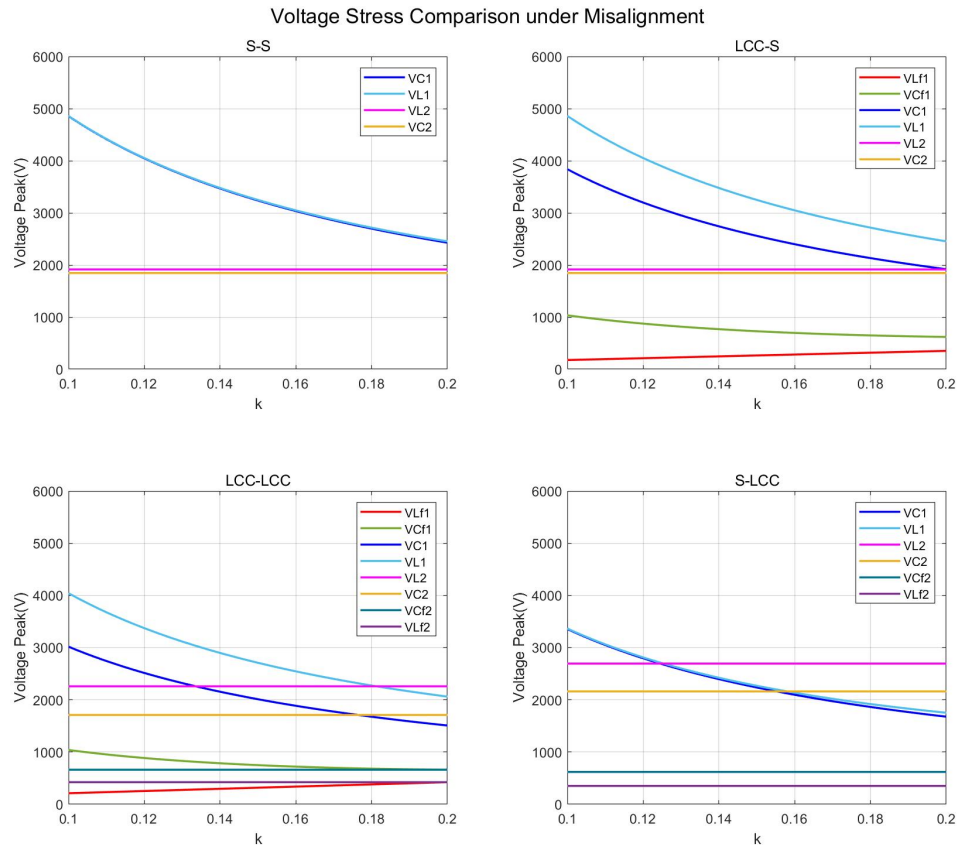


Figure 2.33: Voltage Stress Comparison under Misalignment with Constant Output Voltage

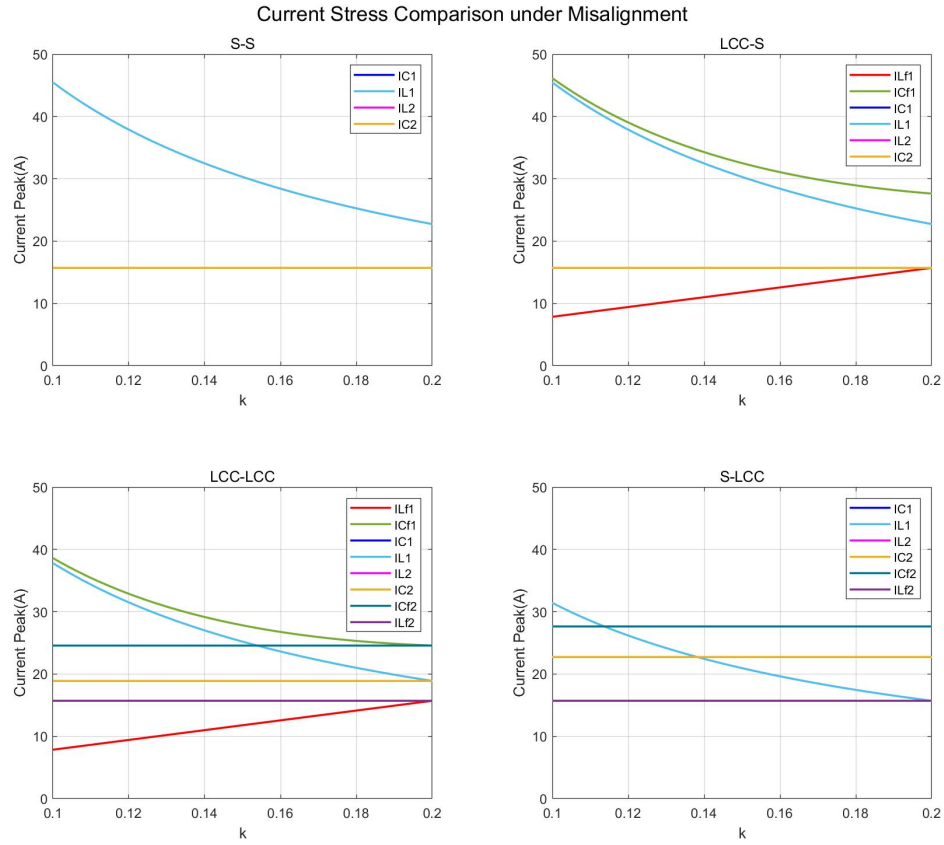


Figure 2.34: Current Stress Comparison under Misalignment with Constant Output Voltage

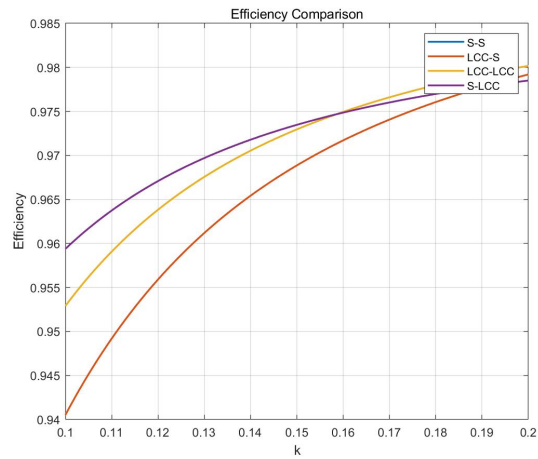


Figure 2.35: Efficiency Comparison under Misalignment with Constant Output Voltage

2.5.3. Topologies comparison conclusion

All the comparison results are summarized in figure 2.36. Here the highest values of the voltage and current peaks on each component of different compensation topologies are taken to represent the component voltage/current stress behaviour.

The S-S topology excels in most aspects, however, it has poor design freedom, which means the

output is only determined by the input voltage and mutual inductance, and an extra front-end DC-DC converter is therefore necessary. The LCC-S topology has two additional compensation components compared to the S-S topology, but the problem of low design freedom is solved, and it has the same superior performance as the S-S topology in almost all aspects. Other topologies are relatively worse compared to these two topologies.


	SS	LCC-S	LCC-LCC	S-LCC	LC-S	S-SP	LC-CL	LCL-S	
Efficiency	0.979	0.979	0.979	0.978	0.977	0.9593	0.8		 <div>Good</div> <div>Moderate</div> <div>Bad</div>
Component Voltage Stress	2700 V (VL1)	2451.69 V (VL1)	2302.14 V (VL2)	2841.91 V (VL2)	2818.48 V (VL1)	3877.04 V (VL2)	10082.6 V (VC2)		
Component Current Stress	22.57 A (IC1)	28.9 A (IC1)	28.78 A (IC1)	34 A (IC2)	39.86 A (IC1)	36.34 A (IC2, IC3)	105.81 A (IC2)		
Design Freedom									
Cost									
Misalignment Behavior (Constant V_{in} , P_{out})									
Misalignment Behavior (Constant V_{out} , P_{out})									

Figure 2.36: Conclusion Table

3

Resonant inductor voltage peak calculation method and implementation of ZVS

In the previous chapter, the LCC-S and S-S compensation topologies are proved to have relatively better performance, however, the analysis results on voltage peaks of resonant inductors are not accurate from the simulation results, as shown in section 2.2.1 and 2.3.1. Therefore, a new resonant inductor voltage peak calculation method is proposed and applied in section 3.1 to obtain more accurate voltage stresses in S-S and LCC-S topology, which is conducive to the breakdown design of inductors.

Section 3.2 and 3.3 provide two possible methods to achieve ZVS, including compensation components tuning and switching frequency adjustment. Besides, a new switching current calculation method is proposed to help ZVS implementation design.

3.1. Resonant inductor voltage peak calculation method and simulation verification

3.1.1. Resonant inductor voltage peak calculation method applied in S-S topology

The simulation and calculation results of voltage/current stresses on each component in S-S topology are presented in table 2.2. As can be seen from the table, the voltage peaks on the resonant inductors L_1 and L_2 are not accurate under fundamental frequency analysis. The simulated voltages of L_1 and L_2 are shown in figure 3.1.

As can be seen in the figure, there is an abrupt voltage change on the simulated inductor voltages. This is due to the harmonics in the output of the H-bridge inverter. When calculating the circuit voltages and currents, only the fundamental frequency component is taken into account, however, the waveform of these voltage stresses are not sinusoidal but the superposition of sinusoidal wave and square wave. Therefore, a more accurate method of calculating voltage peaks is introduced here.

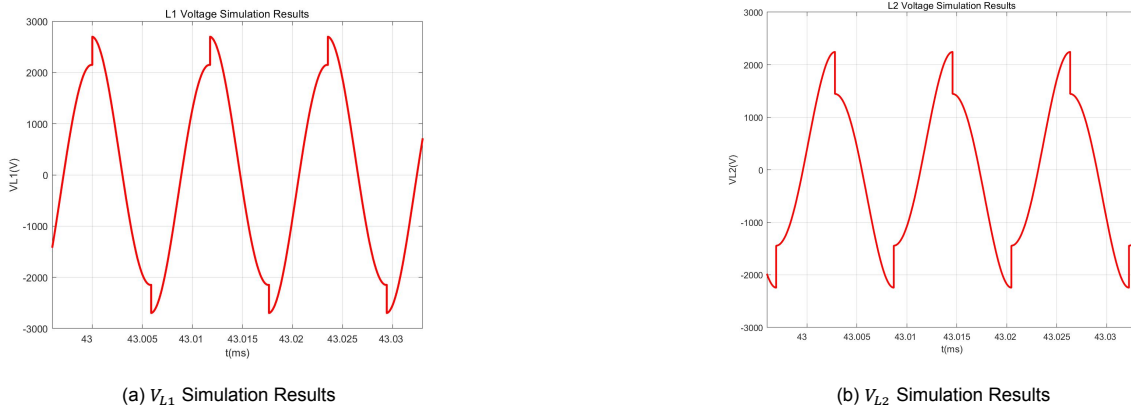


Figure 3.1: L1 and L2 Voltage Simulation

Applying KVL, the voltage on L_1 can also be written as $V_{L1} = V_{ss} - V_{C1}$, where V_{ss} is the output voltage of the DC-AC inverter. V_{ss} is a square-wave voltage with the amplitude of V_{DC} and the fundamental component of V_{ss} is V_s . The high-order frequency harmonic current only produce a small voltage across the capacitor, so the voltage V_{C1} can be approximated as a sinusoidal wave.

Since Z_{ref} is purely resistive and L_1 resonates with C_1 , current \hat{I}_1 is in phase with voltage source V_s . According to (2.7), \hat{V}_{C1} lags V_s 90° in phase, thus the voltage peak on L_1 can be obtained in (3.1), where \hat{V}_{C1} is the peak voltage of C_1 and can be calculated by $\hat{V}_{C1} = \sqrt{2}V_{C1}$.

$$\hat{V}_{L1} = V_{DC} + \hat{V}_{C1} \quad (3.1)$$

The voltage on L_2 can be analyzed in the same way and equation (3.2) can be derived, where \hat{V}_{C2} is the peak voltage of C_2 and can be calculated by $\hat{V}_{C2} = \sqrt{2}V_{C2}$.

$$\hat{V}_{L2} = V_{Bat} + \hat{V}_{C2} \quad (3.2)$$

Figure 3.2 exhibits the results of different calculation methods compared with simulation. It shows that fundamental frequency analysis can obtain accurate voltage peak values of C_1 and C_2 , due to the almost non-distortion of the sinusoidal voltages and currents under the studied load. However, for L_1 and L_2 , there is a large error which can be avoided by applying resonant inductor voltage peak calculation method.

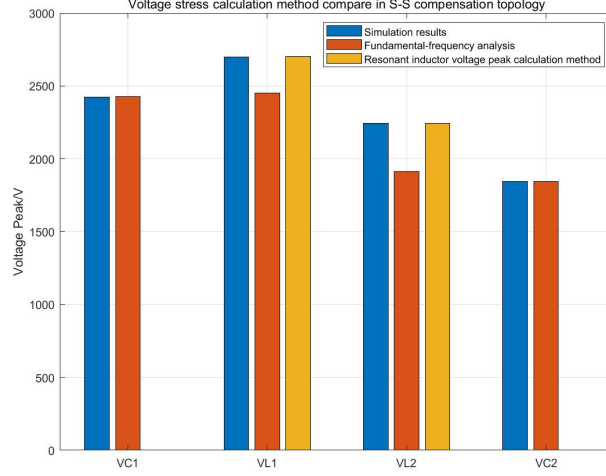
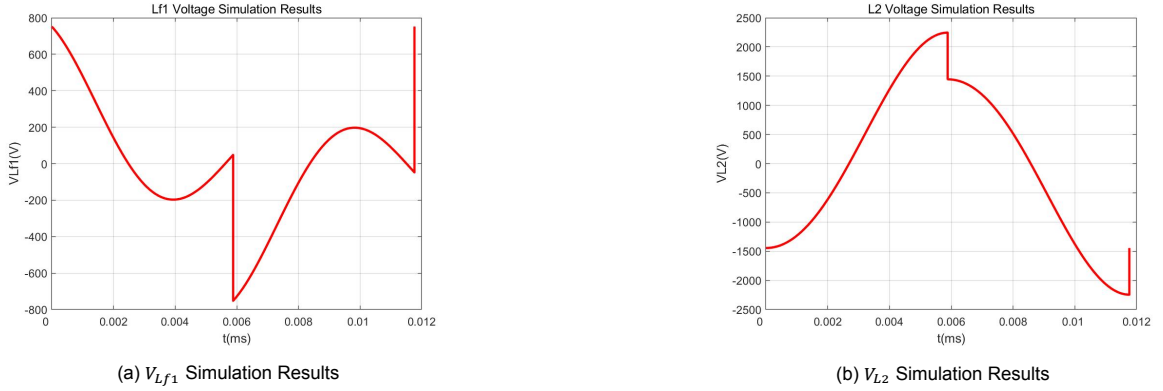


Figure 3.2: S-S Voltage Stress Calculation Method Compare

3.1.2. Resonant inductor voltage peak calculation method applied in LCC-S topology

Table 2.4 shows the simulation and calculation results of voltage and current stress on components of LCC-S topology.

Similar to the S-S topology, in fundamental frequency analysis, the calculated voltage peaks on the filter inductors L_{f1} and L_2 in the LCC-S are inaccurate from the simulation. The simulated results are shown in figure 3.3, in which the high-order harmonics' effect can be clearly seen. Therefore, the proposed new resonant inductor voltage peak calculation method is applied here.

Figure 3.3: L_{f1} and L_2 Voltage Simulation

Applying KVL, voltage on L_{f1} can be expressed as $V_{Lf1} = V_{ss} - V_{Cf1}$. Here, V_{ss} , which is a square wave with amplitude of V_{DC} , is the output of the primary inverter. The fundamental-frequency component of V_{ss} is V_s . To obtain the peak value of V_{Lf1} , only the positive half of the period need to be analyzed. Thus, the time-domain expression of V_{Lf1} is: $v_{Lf1} = V_{DC} - \hat{V}_{Cf1} \sin(\omega t + \alpha)$ ($0 \leq \omega t \leq \pi$), where α is the phase angle of \hat{V}_{Cf1} . Since \hat{V}_{Cf1} can also be written as $\hat{V}_{Cf1} = \hat{I}_1 \cdot (j\omega L_{f1} + Z_{ref}) = \hat{V}_s (1 + \frac{Z_{ref}}{j\omega L_{f1}})$, the range of α is: $-\frac{\pi}{2} < \alpha < 0$. When $\omega t = 0$, v_{Lf1} has the peak value, which is calculated by (3.3). Since the secondary side of LCC-S is the same as S-S, the voltage peak on L_2 can still be calculated using (3.2).

$$\hat{V}_{Lf1} = V_{DC} - \hat{V}_{Cf1} \sin(\alpha) = V_{DC} - \sqrt{2} \text{Im}(\hat{V}_{Cf1}) = V_{DC} + \sqrt{2} \frac{V_s}{\omega L_{f1}} \cdot Z_{ref} \quad (3.3)$$

The calculated results applying resonant inductor voltage peak calculation method compared with fundamental-frequency analysis and simulation are shown in figure 3.4. The resonant inductor voltage peak calculation method still provides more accurate results for the voltage peaks on the resonant inductors in LCC-S topology.

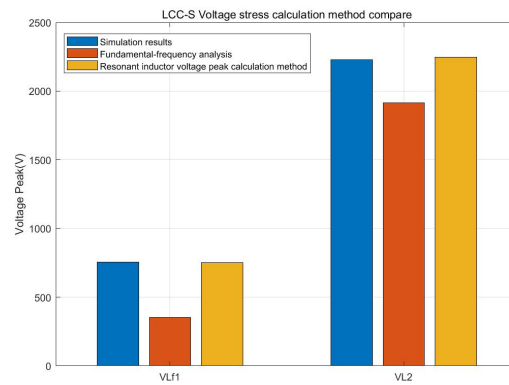


Figure 3.4: LCC-S Voltage Stress Calculation Compare

3.2. Components sensitivity analysis

3.2.1. S-S Components sensitivity analysis

To achieve zero voltage switching (ZVS), the input current needs to lag the input voltage by a certain angle, one feasible way to achieve this is to slightly change the compensation components parameters. Here, all compensation components are modified by a factor of 0.9-1.1, and their effects on the output current value and the phase angle of the input current are analyzed.

- Modification on C_1

The modified compensation capacitor C_1 is nC_1 , where n (0.9 – 1.1) is the modification factor. When only C_1 is modified and C_2 keeps the same value, the secondary side is the same as the original S-S topology, thus Z_{ref} is still calculated by (2.5). However, since the primary side is not fully compensated, the new primary-side current I'_1 is calculated by $I'_1 = \frac{\dot{V}_s}{\frac{1}{j\omega n C_1} + j\omega L_1 + Z_{ref}}$. Substitute the compensation design equation $\frac{1}{j\omega C_1} + j\omega L_1 = 0$, current I'_1 can be derived as $\frac{\dot{V}_s}{(1-\frac{1}{n})j\omega L_1 + Z_{ref}}$, and the secondary-side voltage can be calculated by $\dot{V}'_l = j\omega M I'_1 = \frac{\dot{V}_s j\omega M}{(1-\frac{1}{n})j\omega L_1 + Z_{ref}}$. The new secondary current I'_2 after modification of C_1 can be calculated as $I'_2 = -\frac{\dot{V}'_l}{R_{ac}} = -\frac{\dot{V}_s j\omega M}{(1-\frac{1}{n})j\omega L_1 R_{ac} + \omega^2 M^2}$. Using (2.6), the output current deviation d_i can be calculated by (3.4).

$$d_i = \frac{I'_{Bat}}{I_{Bat}} = \frac{I'_2}{I_2} = \frac{1}{\sqrt{\left(\frac{n-1}{n} \cdot \frac{L_1 R_{ac}}{\omega M^2}\right)^2 + 1}} \quad (3.4)$$

The input impedance $Z'_{in} = \frac{1}{j\omega n C_1} + j\omega L_1 + Z_{ref} = (1 - \frac{1}{n})j\omega L_1 + Z_{ref}$, thus the input current angle can be calculated by (3.5).

$$\theta_{in} = -\arctan\left(\frac{n-1}{n} \frac{L_1 R_{ac}}{\omega M^2}\right) \quad (3.5)$$

- Modification on C_2

When modification is on C_2 , the modified compensation capacitor is nC_2 . The primary-side capacitor is still fully compensated, thus there is $\dot{V}_s = j\omega M I'_2$, where I'_2 is the secondary current after modification. Therefore, the new secondary current I'_2 is the same as I_2 in the original S-S circuit, and $d_i = \frac{I'_2}{I_2} =$

1. Since the secondary compensation is not fully compensated, the new $Z'_{ref} = \frac{\omega^2 M^2}{\frac{1}{j\omega n C_2} + j\omega L_2 + R_{ac}} = \frac{\omega^2 M^2}{(1-\frac{1}{n})j\omega L_2 + R_{ac}}$, and $Z'_{in} = Z'_{ref}$. Thus, the input current angle can be calculated by (3.6).

$$\theta_{in} = \arctan\left(\frac{n-1}{n} \frac{\omega L_2}{R_{ac}}\right) \quad (3.6)$$

- Compensation components tuning method

The simulation and calculation results are shown in figure 3.5. As analyzed above, modification on C_2 doesn't influence the output current, and can change the input current phase angle. Therefore, it is possible to achieve ZVS without affecting the output by decreasing the parameter of C_2 .

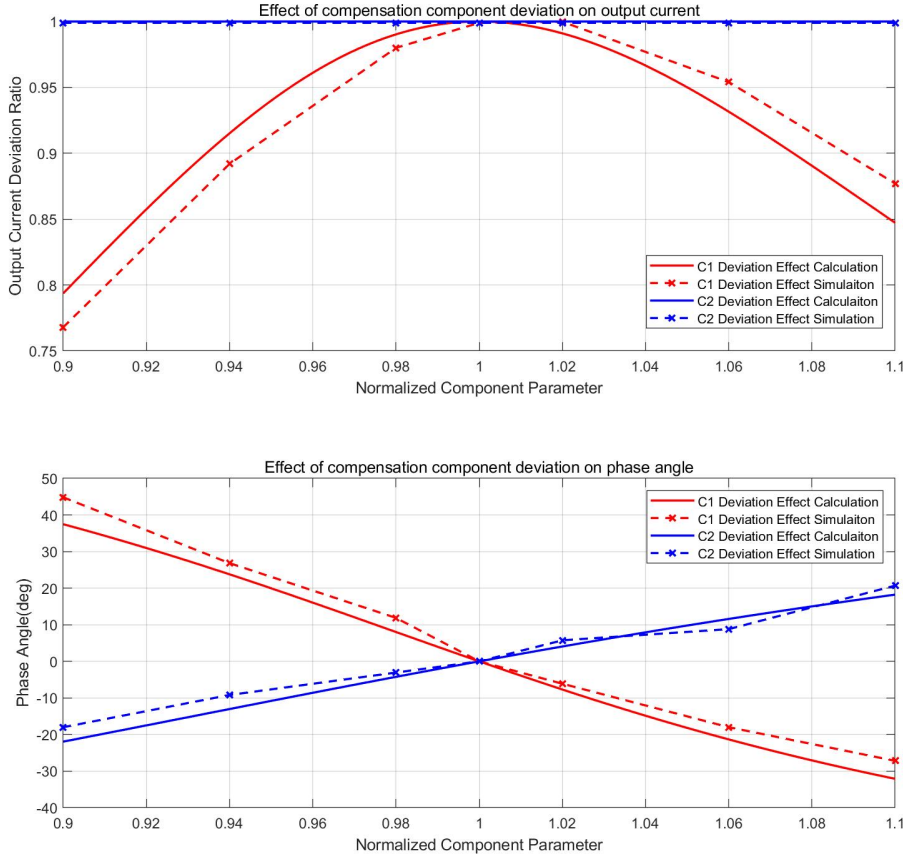


Figure 3.5: S-S Component Sensitivity Analysis

3.2.2. LCC-S Components Sensitivity Analysis

In order to achieve ZVS without affecting the output, each compensation component will be modified by a factor of n (0.9-1.1), and then analyzed for its effect on the input current phase angle and output voltage.

- Modification on L_{f1}

When L_{f1} is modified to nL_{f1} , the equivalent input impedance Z_{in} mentioned in section 2.3.1 needs to be modified to $Z'_{in} = \frac{L_{f1}^2 R_{ac}}{M^2} + (n-1)j\omega L_{f1}$. The input current on L_{f1} is $\dot{I}'_{L_{f1}} = \frac{\dot{V}_s}{Z'_{in}}$. Therefore, the primary coil current \dot{I}'_1 can be calculated by $\dot{I}'_1 = \dot{I}'_{L_{f1}} \cdot \frac{\frac{1}{j\omega C_{f1}}}{\frac{1}{j\omega C_{f1}} + \frac{1}{j\omega C_1} + j\omega L_1 + Z_{ref}} = -j \frac{\dot{V}_s}{\omega L_{f1} + j \frac{(n-1)\omega^2 M^2}{R_{ac}}}$, and the load side voltage can be calculated by $\dot{V}'_l = j\omega M \dot{I}'_1 = \frac{\dot{V}_s \omega M}{\omega L_{f1} + j \frac{(n-1)\omega^2 M^2}{R_{ac}}}$. Based on the calculations above, the output voltage deviation ratio and input current phase angle are deduced as (3.7) and (3.8).

$$d_v = \frac{\dot{V}'_{Bat}}{\dot{V}_{Bat}} = \left| \frac{\dot{V}'_l}{\dot{V}_l} \right| = \frac{1}{\sqrt{1 + \left[\frac{(n-1)\omega M^2}{R_{ac} L_{f1}} \right]^2}} \quad (3.7)$$

$$\theta_{in} = -\arctan \frac{(n-1)\omega M^2}{L_{f1} R_{ac}} \quad (3.8)$$

- Modification on C_{f1}

When C_{f1} is modified as nC_{f1} , input equivalent impedance is $Z'_{in} = (Z_{ref} + j\omega L_1 + \frac{1}{j\omega C_1}) \parallel \frac{1}{j\omega n C_{f1}} + j\omega L_{f1} = \frac{j(n-1)\omega^2 M^2 L_{f1} + (2-n)\omega L_{f1}^2 R_{ac}}{n\omega M^2 + j(n-1)L_{f1} R_{ac}}$, and input current is $I'_{in} = \frac{\dot{V}_s}{Z'_{in}}$. The load voltage can be deduced as $\dot{V}'_l = \frac{\dot{V}_s}{j \frac{\omega M}{R_{ac}}(n-1) + \frac{2-n}{\omega^2 C_{f1} M}}$ using the same way above. The output voltage deviation ratio and input current phase angle are given by (3.9) and (3.10).

$$d_v = \frac{1}{\sqrt{\frac{\omega^2 M^2}{R_{ac}^2}(n-1)^2 + (2-n)^2}} \quad (3.9)$$

$$\theta_{in} = -\text{Angle}(Z'_{in}) \quad (3.10)$$

- Modification on C_1

When modification is on C_1 , the input impedance is $Z'_{in} = (Z_{ref} + j\omega L_1 + \frac{1}{j\omega n C_1}) \parallel \frac{1}{j\omega C_{f1}} + j\omega L_{f1} = \frac{\frac{1-n}{n} \frac{1}{j\omega C_1} + Z_{ref}}{\omega^2 L_{f1}^2}$, thus the input current angle is calculated by (3.11). Since L_{f1} resonates with C_{f1} , current I_1 is only decided by L_{f1} , thus I_1 is unchanged, and load voltage V_l is also unchanged. The output voltage deviation ratio is $d_v = 1$.

$$\theta_{in} = \arctan\left(\frac{n-1}{n} \frac{1}{\omega C_1 Z_{ref}}\right) \quad (3.11)$$

- Modification on C_2

When deviation is on C_2 , the equivalent secondary side impedance Z_{ref} needs to be changed to $Z'_{ref} = \frac{\omega^2 M^2}{\frac{1}{j\omega n C_2} + j\omega L_2 + R_{ac}}$, thus the input impedance is $Z'_{in} = \frac{\omega^2 L_{f1}^2}{Z'_{ref}} = \frac{L_{f1}^2}{M^2} (\frac{1-n}{j\omega n C_2} + R_{ac})$. The input current angle is calculated by (3.12). The primary coil current I_1 is unchanged and can be calculated using (2.16). The secondary side current I'_2 is changed to $I'_2 = \frac{j\omega M I_1}{\frac{1}{j\omega n C_2} + j\omega L_2 + R_{ac}}$. Substitute $\dot{V}'_l = I'_2 R_{ac}$, the output voltage deviation ratio can be deduced as (3.13).

$$\theta_{in} = \arctan\left(\frac{1-n}{n} \frac{1}{\omega C_2 R_{ac}}\right) \quad (3.12)$$

$$d_v = \frac{1}{\sqrt{\left(\frac{n-1}{n} \frac{\omega L_2}{R_{ac}}\right)^2 + 1}} \quad (3.13)$$

- Compensation components tuning method

The simulation and calculation results are shown in figure 3.6. Modification on C_1 and L_{f1} have little influence on output voltage, however, modification on C_1 cause larger influence on input current phase angle. Therefore, adjusting C_1 is more suitable for implementing ZVS.

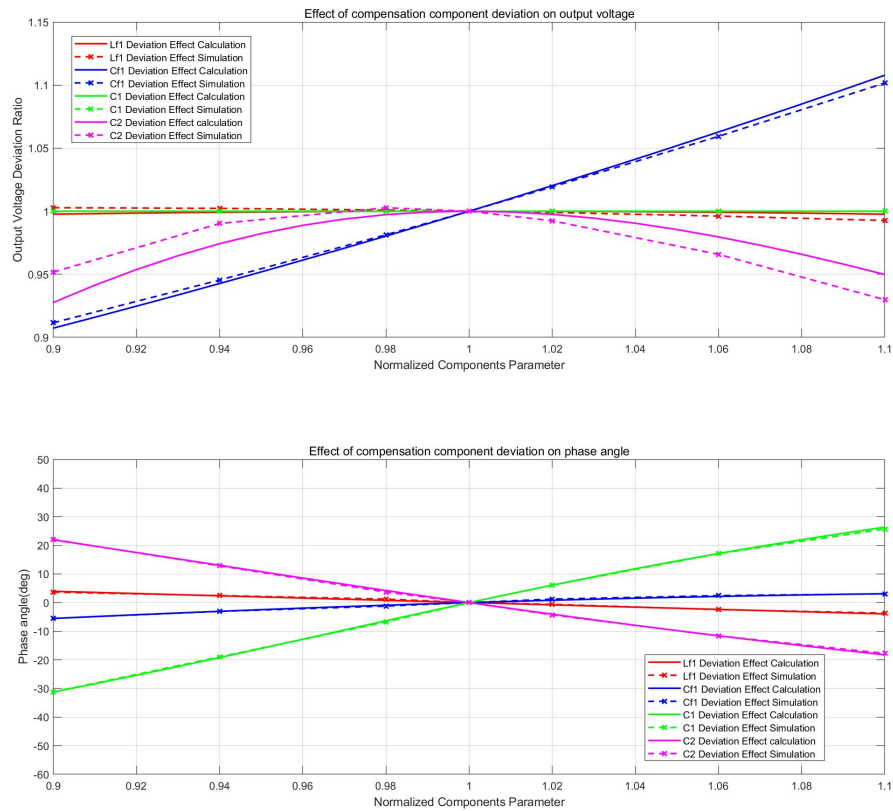


Figure 3.6: LCC-S Component Sensitivity

3.3. Frequency variation analysis

Apart from tuning the values of the compensation components, a slight change in input voltage frequency to operate the resonant converter in a detuned state by a slight change on the switching frequency is another feasible solution for implementing ZVS.

In this section, the input voltage frequency will be varied in the range of 80-90 kHz, and its effect on the output voltage/current and the phase angle of the input current will be calculated and analyzed.

3.3.1. S-S Frequency variation analysis

When the system is not working at resonant frequency, the compensation can not fully compensate, $Z_{ref} = \frac{\omega^2 M^2}{j\omega L_2 + \frac{1}{j\omega C_2} + R_{ac}}$, and $Z_{in} = Z_{ref} + j\omega L_1 + \frac{1}{j\omega C_1}$. Using the same way mentioned before, the output current I'_{Bat} and phase angle θ_{in} can be calculated. The calculation results are shown in figure 3.7.

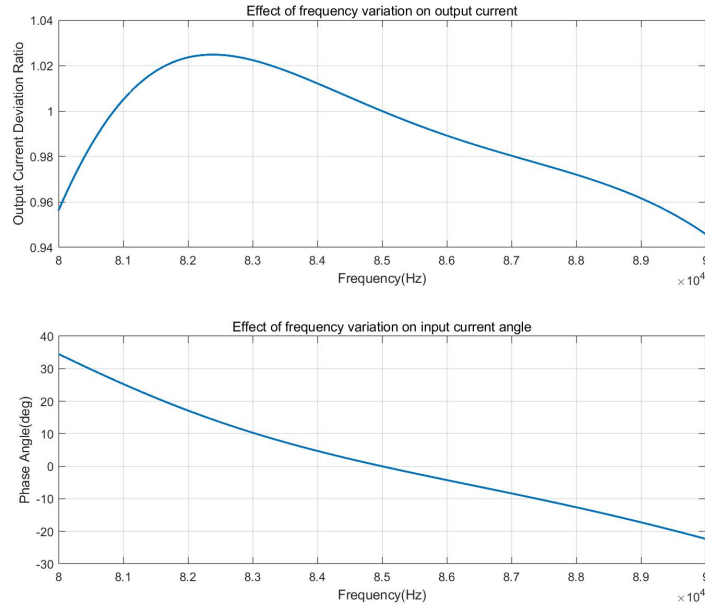


Figure 3.7: S-S Frequency Variation Influence

As can be seen from the figure, changing the input voltage frequency still causes the input current phase angle to lag, however, it slightly reduces the output current.

3.3.2. LCC-S frequency variation analysis

When the system operating frequency varies from 80 kHz to 90 kHz, the compensation network can not fully compensate. In this case, $Z_{ref} = \frac{\omega^2 M^2}{j\omega L_2 + \frac{1}{j\omega C_2} + R_{ac}}$, and $Z_{in} = (Z_{ref} + j\omega L_1 + \frac{1}{j\omega C_1}) \parallel \frac{1}{j\omega C_{f1}} + j\omega L_{f1}$. The output voltage and input current angle can be calculated as mentioned before, and the calculation results are shown in figure 3.8.

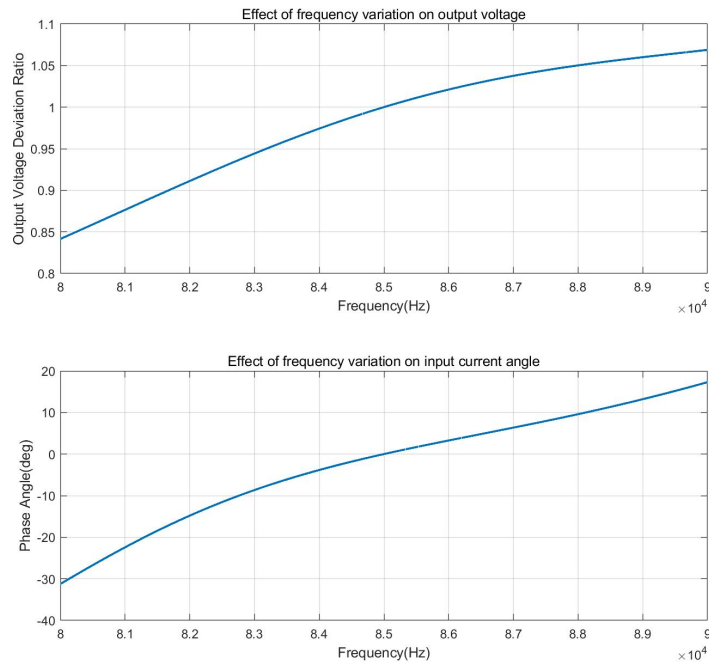


Figure 3.8: LCC-S Frequency Variation Influence

Similar to the S-S topology, changing the input voltage frequency can lag the input current phase angle, however, the output voltage is reduced even more in the LCC-S topology.

3.4. Switching current calculation method in LCC-S compensation topology and its tuning method

To achieve ZVS during switching, the switching current must lag the voltage, and this switching current must be large enough to completely charge or discharge the parasitic capacitors of the switches within dead time. However, when the switching current is too large, the losses on MOSFETs will also be increased. Therefore, the tuning of the switching current needs trade-offs, and the calculation method of switching current is especially important in this case.

Currently, there are few studies on the calculation method of switching current. In [12], a switching current calculation method in double-sided LCC compensation topology is proposed, and some researches apply this method in LCC-S compensation topology [13]. However, this calculation method does not consider the secondary-side harmonics and the influence of parasitic capacitors of the back-end converter. Therefore, a new switching current calculation method is proposed here, and the tuning method based on this calculation method will also be introduced.

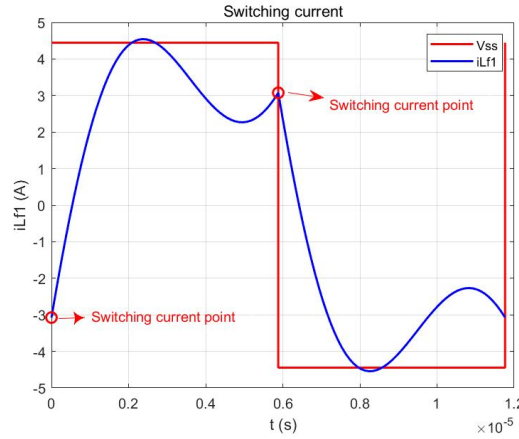


Figure 3.9: Switching current point in simulation

3.4.1. Switching current calculation method when fully compensated

When the LCC-S compensation topology is fully compensated, in fundamental analysis, the input impedance Z_{in} is completely resistive. Current $\dot{I}_{Lf1-1st}$ (the fundamental-frequency component of current \dot{I}_{Lf1}) is in phase with the input voltage \dot{V}_s , and $i_{Lf1-1st} = 0$ when $t = 0$ or $\frac{T}{2}$. Therefore, the switching current is only caused by the high-order frequency component of this topology in this case. In this section, the calculation method of switching current caused by high-order frequency will be introduced.

Applying KVL on the primary side of the LCC-S topology, there is (3.14), where V_{ss} is a square-wave voltage with amplitude of V_{DC} .

$$L_{f1} \frac{di_{Lf1}}{dt} + v_{C1} + L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} = V_{ss} \quad (3.14)$$

Integrating the high-order frequency components of both sides of equation (3.14) from 0 to $\frac{T}{2}$, equation (3.15) can be derived. Here, $2i_{s_kh} = i_{Lf1_kh}(t = \frac{T}{2}) - i_{Lf1_kh}(t = 0)$, and i_{s_kh} is the high-order frequency components of switching current. v_{C1_kh} , i_{1_kh} , i_{2_kh} and V_{ss_kh} represent the high-order frequency components of v_{C1} , i_1 , i_2 and V_{ss} respectively.

$$L_{f1} \cdot 2i_{s_kh} + \int_0^{\frac{T}{2}} v_{C1_kh} dt + L_1 \cdot \left[i_{1_kh}(t = \frac{T}{2}) - i_{1_kh}(t = 0) \right] + M \cdot \left[i_{2_kh}(t = \frac{T}{2}) - i_{2_kh}(t = 0) \right] = \int_0^{\frac{T}{2}} V_{ss_kh} dt \quad (3.15)$$

Applying KVL in the two circuits on the primary side and the circuit on the secondary side, equation (3.16) for high-order harmonics can be obtained, where \dot{I}_{1_khs} , \dot{I}_{Lf1_khs} and \dot{I}_{2_khs} are the phasors of the high-order harmonic currents, $k_{hs} = 2q + 1$ ($q = 1, 2, 3, \dots$) represents the order of harmonics.

$$\begin{cases} jk_hst\omega L_{f1} \cdot \dot{I}_{Lf1_k_hst} + \frac{1}{jk_hst\omega C_{f1}} \cdot (\dot{I}_{Lf1_k_hst} - \dot{I}_{1_k_hst}) = \frac{2\sqrt{2}V_{DC}}{k_hst\pi} \\ \dot{I}_{1_k_hst} \cdot \left(\frac{1}{jk_hst\omega C_{f1}} + \frac{1}{jk_hst\omega C_1} + jk_hst\omega L_1 \right) - \dot{I}_{Lf1_k_hst} \cdot \frac{1}{jk_hst\omega C_{f1}} + \dot{I}_{2_k_hst} \cdot jk_hst\omega M = 0 \\ \dot{I}_{1_k_hst} \cdot jk_hst\omega M + \dot{I}_{2_k_hst} \cdot (jk_hst\omega L_2 + \frac{1}{jk_hst\omega C_2}) = \frac{2\sqrt{2}V_{Bat}}{k_hst\pi} \end{cases} \quad (3.16)$$

By solving the first equation of (3.16) and substitute $C_{f1} = \frac{1}{\omega^2 L_{f1}}$, $\dot{I}_{Lf1_k_hst}$ can be expressed by $\dot{I}_{Lf1_k_hst} = (\dot{I}_{1_k_hst} + j \frac{2\sqrt{2}\omega C_{f1}}{\pi} V_{DC}) \cdot \frac{1}{1-k_hst}$. Substitute the expression of $\dot{I}_{Lf1_k_hst}$ and $C_1 = \frac{1}{\omega^2(L_1-L_{f1})}$ into the second equation of (3.16), there is (3.17). Since $\frac{1}{k_hst(k_hst-1)}\omega L_{f1}$ is relatively small compared with $\frac{k_hst-1}{k_hst}\omega L_1$, this term can be neglected. Finally, substitute the expression of $\dot{I}_{2_k_hst}$ and $C_2 = \frac{1}{\omega^2 L_2}$ into the third equation of (3.16), $\dot{I}_{1_k_hst}$ can be solved as (3.18). When $t = \frac{T}{2}$, $\dot{I}_{1_k_hst}$ reaches its peak. Therefore, $L_1 \cdot \left[\dot{I}_{1_k_hst}(t = \frac{T}{2}) - \dot{I}_{1_k_hst}(t = 0) \right]$ can be calculated by (3.19), where $I_{1k_h} = \sum_{q=1}^{\infty} \frac{2\sqrt{2}(2q+1)^2 M(V_{Bat} + \frac{L_2 V_{DC}}{(2q+1)^2 M})}{(2q+1)^4 \omega M^2 \pi - [(2q+1)^2 - 1]^2 \omega L_1 L_2 \pi} \approx (\frac{\pi^2}{8} - 1) \frac{2\sqrt{2} M V_{Bat}}{\omega \pi (M^2 - L_1 L_2)} + (\frac{\pi^4}{96} - 1) \frac{2\sqrt{2} L_2 V_{DC}}{\omega \pi (M^2 - L_1 L_2)}$ is the sum of RMS values of high-order harmonic currents in I_1 .

$$\dot{I}_{2_k_hst} = -j \frac{2\sqrt{2}V_{DC}}{k_hst^2 (1 - k_hst) \omega M \pi} - \left[\frac{k_hst - 1}{k_hst} \omega L_1 - \frac{1}{k_hst (k_hst - 1)} \omega L_{f1} \right] \cdot \frac{1}{k_hst \omega M} \cdot \dot{I}_{1_k_hst} \quad (3.17)$$

$$\dot{I}_{1_k_hst} = -j \frac{2\sqrt{2}k_hst M (V_{Bat} + \frac{L_2 V_{DC}}{k_hst M})}{k_hst^4 \omega M^2 \pi - (k_hst - 1)^2 \omega L_1 L_2 \pi} \quad (3.18)$$

$$L_1 \cdot \left[\dot{I}_{1_k_hst}(t = \frac{T}{2}) - \dot{I}_{1_k_hst}(t = 0) \right] = L_1 \cdot 2\sqrt{2} I_{1k_h} \quad (3.19)$$

For the voltage $v_{C1_k_hst}$, the time-domain expression is given by (3.20). Therefore, the integral of $v_{C1_k_hst}$ from 0 to $\frac{T}{2}$ has a coefficient $\frac{1}{k_hst}$, which makes it relatively small compared with $L_1 \cdot 2\sqrt{2} I_{1k_h}$ and can be neglected.

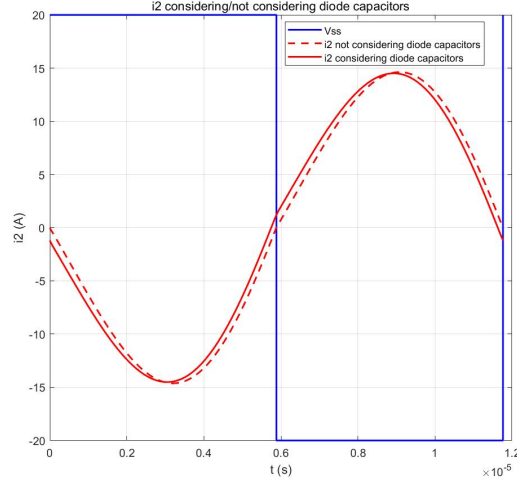
$$v_{C1_k_hst} = \sqrt{2} I_{1_k_hst} \cdot \frac{1}{k_hst \cdot \omega C_1} \sin(k_hst \cdot \omega t - \pi) \quad (3.20)$$

For current i_2 , when diodes of back-end rectifier are ideal, i_2 is 0 when $t = 0$ or $\frac{T}{2}$, as shown in figure 3.10. However, when diode parasitic capacitors are considered, there is a current charging or discharging the parasitic capacitors of the diodes during the voltage transition. Since this charging process is short, assuming that the current is charging the diode parasitic capacitors linearly with the slope of i_2 when $t = 0$ or $\frac{T}{2}$. Since the front-end voltage V_{ss} is in the same phase as the input voltage of the back-end diode bridge V_l , V_l is 0 when $t = 0$ or $\frac{T}{2}$. When V_l drops from V_{Bat} to 0, there is (3.21), where C_u is the parasitic capacitor of each diode and t_c is the time required for V_l to drop from V_{Bat} to 0. Therefore, the value of i_2 when $t = \frac{T}{2}$ can be given by (3.22), and $M \cdot \left[i_{2_k_hst}(t = \frac{T}{2}) - i_{2_k_hst}(t = 0) \right]$ can be written as (3.23).

$$\frac{\sqrt{2}\omega I_2 t_c^2}{2C_u} = V_{Bat} \quad (3.21)$$

$$i_{2o} = t_c \cdot \sqrt{2}\omega I_2 \quad (3.22)$$

$$M \cdot \left[i_{2_k_hst}(t = \frac{T}{2}) - i_{2_k_hst}(t = 0) \right] = 2i_{2o} \cdot M \quad (3.23)$$

Figure 3.10: i_2 considering/not considering diode capacitors

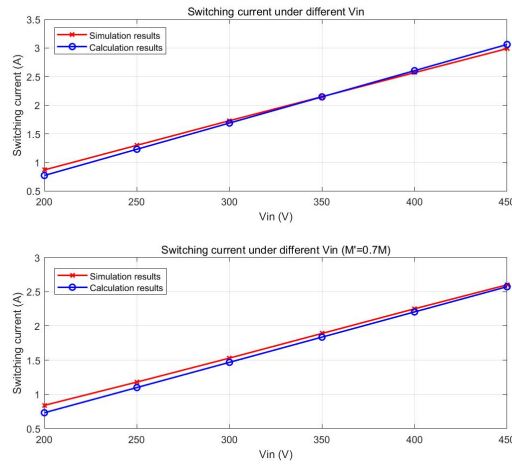
When fundamental-frequency component is not considered, the integration of V_{ss_kh} can be written as (3.24).

$$\int_0^{\frac{T}{2}} V_{ss_kh} dt = V_{DC} \frac{T}{2} - \frac{2\sqrt{2}V_s}{\omega} \quad (3.24)$$

Substitute (3.19), (3.23) and (3.24) in (3.15), the high-order frequency component of switching current i_{s_kh} can be given by (3.25).

$$i_{s_kh} = \frac{\pi V_{DC} - 2\sqrt{2}V_s - 2\omega M i_{2o} - 2\sqrt{2}\omega L_1 I_{1kh}}{2\omega L_{f1}} \quad (3.25)$$

To verify the switching current calculation method, a fully compensated LCC-S model is built in PLECS. The simulation results and calculation results comparison are shown in figure 3.11 and 3.12.

Figure 3.11: Switching current under different V_{in}

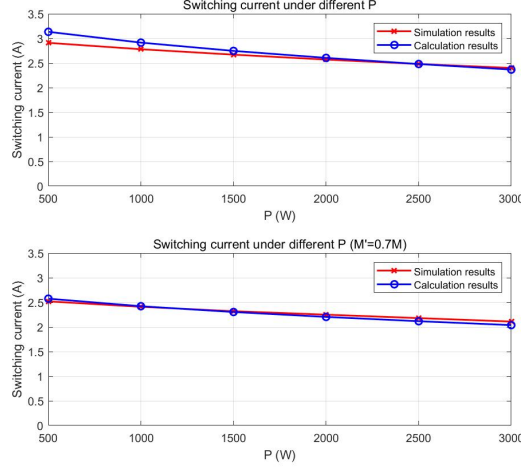


Figure 3.12: Switching current under different P

In figure 3.11, the input voltage varies from 200 V to 450 V, while the power is fixed at 2000 W. In figure 3.12, the power varies from 500 W to 3000 W, while the input voltage is fixed at 400 V. Misalignment (mutual inductance decreases to 0.7 M) under these conditions are also considered. Based on these two figures, it can be seen that this high-order frequency component switching current calculation method is pretty accurate. It can also be seen that the switching current drops with increasing power or decreasing mutual inductance, and increases with increasing input voltage.

The simulation parameters values are shown in table 3.1.

L_1 (μH)	L_2 (μH)	M (μH)	L_{f1} (μH)	C_{f1} (nF)
339	226.5	106	100.5	34.89
C_1 (nF)	C_2 (nF)	C_u (pF)		
14.7	15.48	300		

Table 3.1: Circuit parameters in simulation when system is fully compensated

3.4.2. Switching current calculation method considering components sensitivity

Section 3.4 gives the switching current calculation method when the LCC-S compensation topology is fully compensated. However, in reality, deviations in components values due to manufacturing or other issues can make the system not fully compensated. Furthermore, compensation topology that is not fully compensated can sometimes be used to achieve ZVS. Therefore, it is very important to conduct a components sensitivity analysis of the switching current.

When the compensation topology is not fully compensated, the fundamental-frequency component of current I_{in} is not in phase with V_s , as analysed in section 3.2.2. Therefore, I_{in_1st} is not 0 when $t = 0$ or $\frac{T}{2}$. This switching current caused by fundamental-frequency component is designated as i_{s_1st} , and should be added to equation (3.25) when compensation topology is not fully compensated. Here, it is assumed that the components sensitivity has little influence on i_{s_kh} [13], which can be verified with simulation or solving the equation (3.16) considering the components sensitivity.

Based on the analysis in section 2.3.1, the following equivalent impedance can be given in (3.26).

$$\begin{cases} Z_{sec} = j\omega L_2 + \frac{1}{j\omega C_2} + R_{ac} \\ Z_{ref} = \frac{\omega^2 M^2}{Z_{sec}} = \frac{\omega^2 M^2}{j\omega L_2 + \frac{1}{j\omega C_2} + R_{ac}} \\ Z_{in} = \frac{1}{j\omega C_{f1}} \parallel (Z_{ref} + j\omega L_1 + \frac{1}{j\omega C_1}) + j\omega L_{f1} \\ = \frac{-\omega^4 M^2 C_1 C_2 + (1 - \omega^2 C_1 L_1) \cdot (1 + j\omega C_2 R_{ac} - \omega^2 C_2 L_2)}{-j\omega^5 M^2 C_1 C_2 C_{f1} + (j\omega C_{f1} + j\omega C_1 - j\omega^3 C_1 C_{f1} L_1) \cdot (1 + j\omega C_2 R_{ac} - \omega^2 C_2 L_2)} + j\omega L_{f1} \end{cases} \quad (3.26)$$

When the system is not fully compensated, the compensation capacitors can be expressed as (3.27), where n_f , n_1 and n_2 are the modification factors of C_{f1} , C_1 and C_2 respectively, which can represent the degree of system detuning.

$$\begin{cases} C_{f1} = n_f \cdot \frac{1}{\omega^2 L_{f1}} \\ C_1 = n_1 \cdot \frac{1}{\omega^2 (L_1 - L_{f1})} \\ C_2 = n_2 \cdot \frac{1}{\omega^2 L_2} \end{cases} \quad (3.27)$$

Substitute (3.27) in (3.26), the equivalent input impedance considering components sensitivity can be expressed by (3.28).

$$Z'_{in} = \frac{-n_1 n_2 \omega^4 M^2 C_1 C_2 + (1 - n_1 \omega^2 C_1 L_1) \cdot (1 + j n_2 \omega C_2 R_{ac} - n_2 \omega^2 C_2 L_2)}{-j n_1 n_2 n_f \omega^5 M^2 C_1 C_2 C_{f1} + (j n_f \omega C_{f1} + j n_1 \omega C_1 - j n_1 n_f \omega^3 C_1 C_{f1} L_1) \cdot (1 + j n_2 \omega C_2 R_{ac} - n_2 \omega^2 C_2 L_2)} + j \omega L_{f1} \quad (3.28)$$

Based on (3.28), the switching current value when $t = \frac{T}{2}$ can be give by (3.29), where θ_{in} which can be calculated by (3.10) is the angle of input current. Therefore, the switching current calculation method considering components sensitivity can be expressed as (3.30).

$$i_{s_1st} = - \left| \frac{\sqrt{2} V_s}{Z'_{in}} \right| \cdot \sin \theta_{in} \quad (3.29)$$

$$i_s = i_{s_1st} + i_{s_kh} = - \left| \frac{\sqrt{2} V_s}{Z'_{in}} \right| \cdot \sin \theta_{in} + \frac{\pi V_{DC} - 2\sqrt{2} V_s - 2\omega M i_{2o} - 2\sqrt{2} \omega L_1 I_{1kh}}{2\omega L_{f1}} \quad (3.30)$$

3.4.3. Tuning method based on the proposed switching current calculation method

As analysed in section 3.2.2, tuning C_1 is the best choice to implement ZVS. Assuming that n_f , n_2 equal to 1, the switching current expression regarding to n_1 can be given by (3.31), where i'_s is the switching current value after tuning.

$$i'_s = \frac{\pi V_{DC} - 2\sqrt{2} V_s \left(\frac{n_1 - 1}{n_1} \frac{L_1}{L_{f1}} + \frac{1}{n_1} \right) - 2\omega M i_{2o} - 2\sqrt{2} \omega L_1 I_{1kh}}{2\omega L_{f1}} \quad (3.31)$$

The minimal switching current required for ZVS can be calculated by (3.32) [19], where C_{oss} is the parasitic capacitor of each diode, and t_{dead} is the dead time of the MOSFETs inverter.

$$i_{s,required} = \frac{2V_{DC} C_{oss}}{t_{dead}} \quad (3.32)$$

Based on the minimal switching current requirement, the modification factor n_1 can be given by (3.33).

$$n_1 = \frac{L_1 - L_{f1}}{L_{f1}} \cdot \frac{2\sqrt{2} V_s}{2\omega L_{f1} i'_s + 2\sqrt{2} \omega L_1 I_{1kh} + 2\omega M i_{2o} - \pi V_{DC} + 2\sqrt{2} V_s \frac{L_1}{L_{f1}}} \quad (3.33)$$

3.4.4. Simulation verification of switching current calculation method

To verify the switching current calculation method and its tuning method, a LCC-S compensation topology model is built in PLECS, which is shown in figure 3.13.

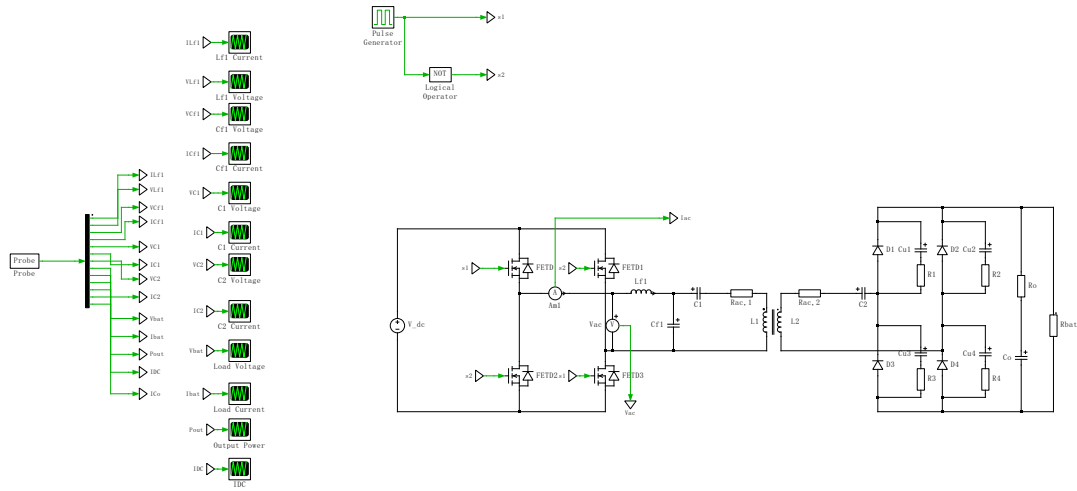


Figure 3.13: Simulated LCC-S compensation topology

Assuming that the tuning modification factor $n_1 = 0.95$, the calculation and simulation results of the switching current are shown in figures 3.14 and 3.15.

As comparison, a switching current calculation method proposed in [13] is also given in (3.34), and is shown in figures 3.14 and 3.14, as well. The first term in (3.34) represents the high-order harmonics from the input voltage V_{ss} , and the second term represents the influence of components sensitivity in fundamental frequency, as analysed before. Therefore, when considering the influence of high-order harmonics, this calculation method didn't consider the influence from the diodes parasitic capacitors, and the high-order harmonics of back-end voltage V_L .

$$i_s = \frac{\sqrt{2}}{4} \frac{V_s}{\omega L_{f1}} - \left| \frac{\sqrt{2}V_s}{Z'_{in}} \right| \cdot \sin \theta_{in} \quad (3.34)$$

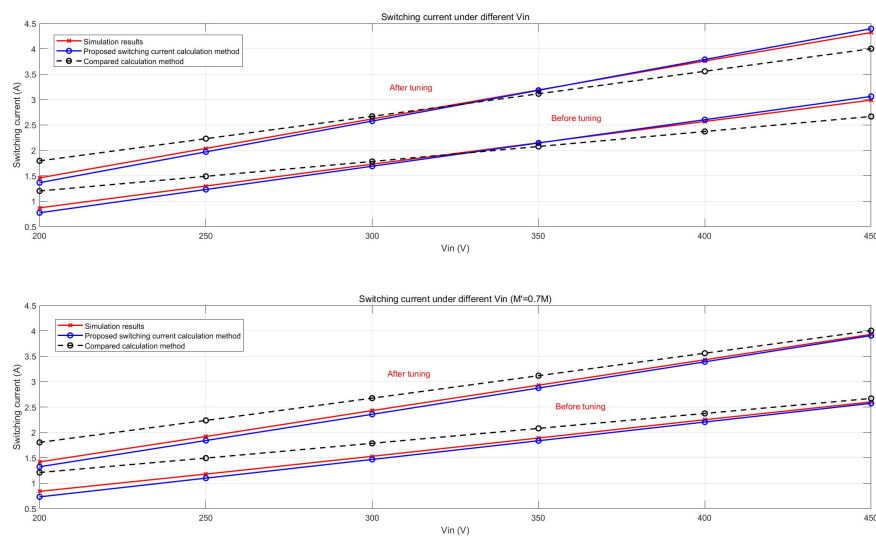


Figure 3.14: Switching current under different V_{in} after tuning

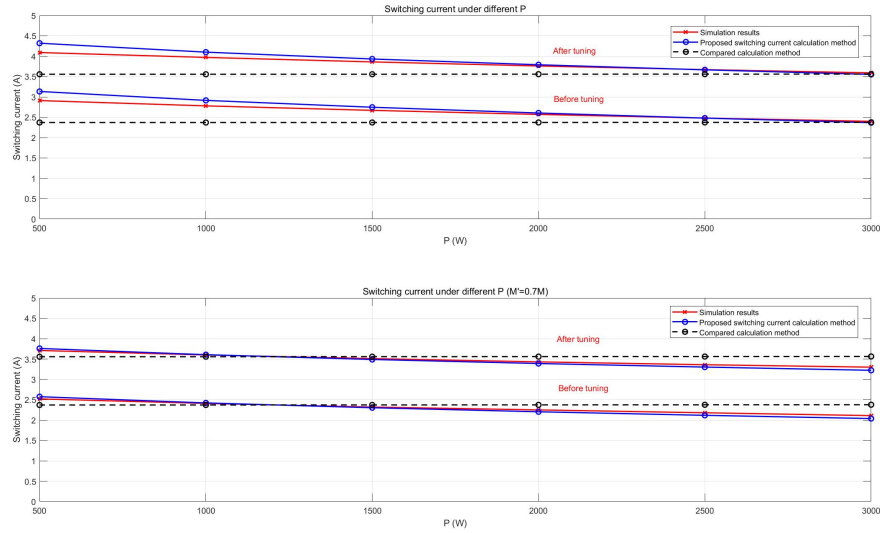


Figure 3.15: Switching current under different P after tuning

As can be seen from these figures, the switching current after tuning increases, and the proposed switching current calculation method matches well with the simulation results. However, since the compared switching current calculation method didn't consider the influence from the back-end, it is almost constant under different mutual inductance, which does not fit the simulation results.

4

Experimental verification

In this chapter, a series of experiments are conducted to verify the conclusions given in previous chapters.

Section 4.1 introduces the design procedure of the LCC-S compensation, and the power loss on each component (including compensation inductor, compensation capacitors, MOSFETs, diodes, primary and secondary coils etc.) is analyzed. The actual measured values of all the components are given in section 4.2.

Section 4.3 gives a comparison of the efficiency of LCC-S compensation and S-S compensation under various operating conditions. After the comparison, the conclusion gives a more suitable operating scenario for both topologies.

Section 4.4 verifies the resonant inductor voltage peak calculation method proposed in section 3.1 on both LCC-S and S-S compensation topology.

Section 4.5 provides experimental verification of the switching current calculation method proposed in section 3.4. A comprehensive experimental verification is given considering different input voltages, different input power and misalignment. Besides that, two capacitors of different capacitance values of C_1 are used in all operating conditions to verify the effect of the tuning method on switching current.

4.1. Experimental parameters and design

Circuit parameters in the experiment are presented in table 4.1, where the calculation and design method of the compensation components parameters are given in section 2.3.1. Note that the coil parameters are different from the analysis in the previous sections, these coil parameters are from the existing prototype in the lab.

Design	L_1 (μH)	L_2 (μH)	M (μH)	L_{f1} (μH)	C_{f1} (nF)
	338	224.7	93.9	93.9	37.34
Design	C_1 (nF)	C_2 (nF)	V_{DC} (V)	V_{Bat} (V)	P_{out} (kW)
	14.36	15.67	400	400	3

Table 4.1: Designed circuit parameters in experiment

When designing inductors, capacitors and calculating power loss on each component, the voltage/current stresses on each component need to be considered. The following table gives the voltage/current stress values for each component.

RMS voltage stress (V)	L_{f1}	C_{f1}	C_1
Peak voltage stress (V)	417.76	551.56	936.18
RMS current stress (A)	990.81	780.02	1324
Peak current stress (A)	8.33	11.00	7.18
	11.78	15.55	10.16
RMS voltage stress (V)	L_1	L_2	C_2
Peak voltage stress (V)	1362.00	1058.40	995.25
RMS current stress (A)	1926.10	1807.50	1407.5
Peak current stress (A)	7.18	8.33	8.33
	10.16	11.78	11.78

Table 4.2: Voltage/current stress on each component

4.1.1. Compensation inductor design and its power loss calculation

The selected core of the compensation inductor L_{f1} is PM/74/59, and the chosen core material is N87. Based on its datasheet, the design-related parameters are summarized in table 4.3.

μ_r	A_e (mm^2)	l_e (mm)	V_e (mm^3)
1290	790	128	101000

Table 4.3: Design-related core parameters

In this table, μ_r is the relative permeability of this core material. A_e and l_e are the effective magnetic cross section and effective magnetic path length of the core, respectively. V_e is the effective magnetic volume.

Dimensions of the PM/74/59 core is shown in figure 4.1. To reduce the loss caused by the multi-layer coils, the inductor is wound with only one layer. Considering the height of the core, the number of turns of the coil N is set to be 14.

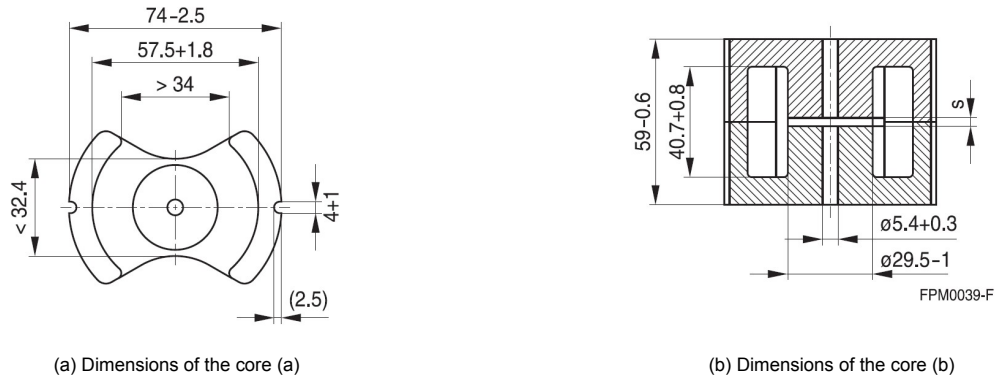


Figure 4.1: Dimensions of the core

The design procedure of the compensation inductor and related formulae can be referred to the paper [20]. The maximum flux density can be calculated by (4.1), and the air-gap length is calculated by (4.2).

As can be seen from the equation (4.1), the maximum flux density B_{\max} can be reduced by increasing the number of turns of the coil, which can reduce the core loss. Therefore, it is necessary to increase the number of turns of the coil as much as possible within one layer.

The specification of used Litz wire is $600 \times 71 \mu\text{m}$, and the diameter of it is $d = 2.5 \text{ mm}$. The required height of the core is given by $H = Nd + l_g = 37 \text{ mm}$, which is smaller but close to the actual height of the core.

$$B_{\max} = \frac{L_{f1} \hat{I}_{Lf1}}{A_e N} = 0.1 \text{ T} \quad (4.1)$$

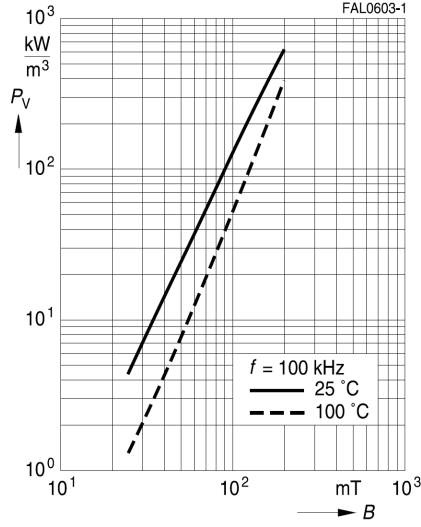
$$l_g = \frac{N^2 A_e \mu_0}{L_{f1}} - \frac{l_e}{\mu_r} = 2 \text{ mm} \quad (4.2)$$

Power loss calculation

1. Core loss According to [20], the core loss can be calculated by the Steinmetz equation (4.3), where k , α and β are the Steinmetz coefficients and can be obtained by curve fitting the loss curve of the core material. \hat{B} is the maximum flux density which is already calculated by (4.1).

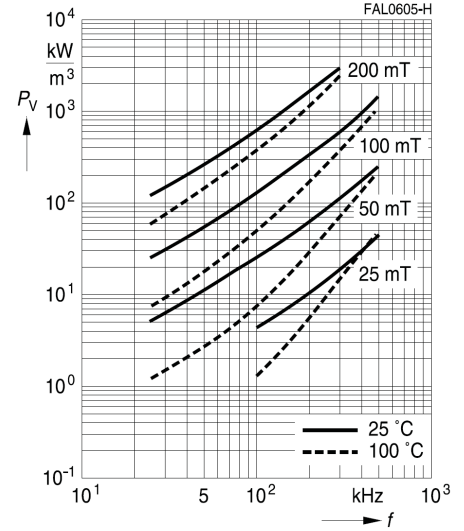
$$P_{core} = k f^\alpha \hat{B}^\beta V_e \quad (4.3)$$

Relative core losses
versus AC field flux density
(measured on R34 toroids)



(a) Relative core loss versus B

Relative core losses
versus frequency
(measured on R34 toroids)



(b) Relative core loss versus f

Figure 4.2: Core loss curves

From datasheet of N87 material, figure 4.2 presents the core loss curves. Assuming the wireless power transfer system is operating under 100 °C, curve fitting of the loss curves gives the Steinmetz coefficients: $\alpha = 1.3589$, $\beta = 2.91$ and $k = 77.6635$. Applying the Steinmetz equation, core loss under rated condition is calculated to be 4.04 W.

2. Winding loss

From figure 4.1, it can be seen that the diameter of the core is 29.5 mm. Thus, the length of one turn is $l_t = 29.5\pi$ mm. The resistance of the wire is calculated by (4.4), where S is the copper area of the Litz wire. The winding loss of the inductor under rated condition is given by (4.5).

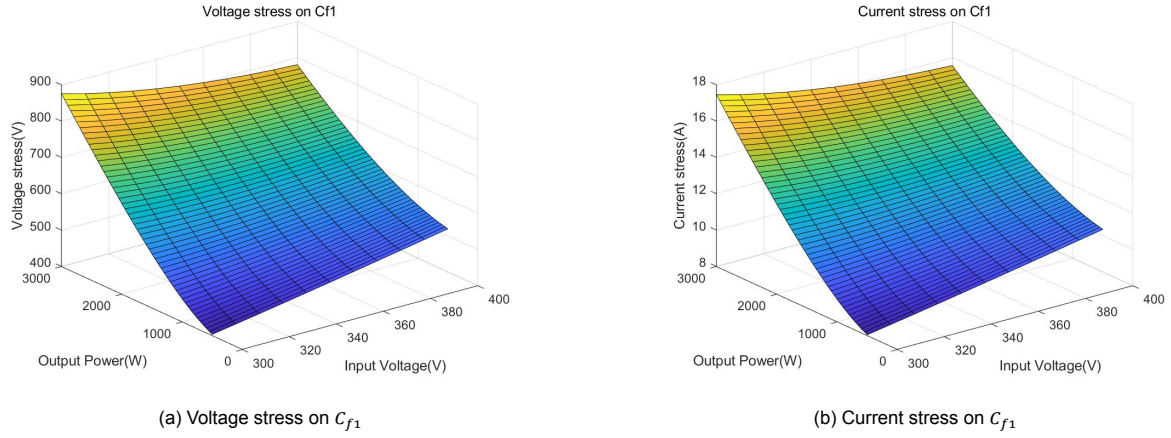
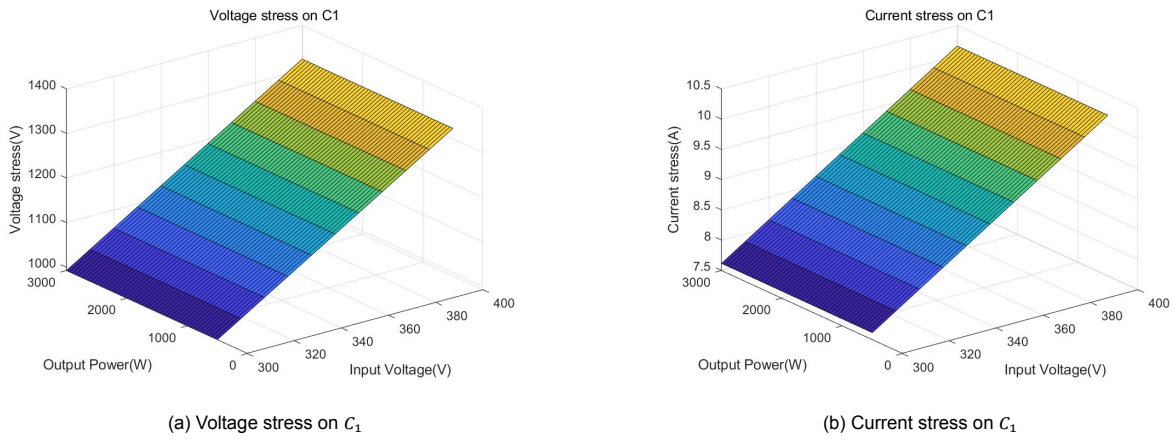
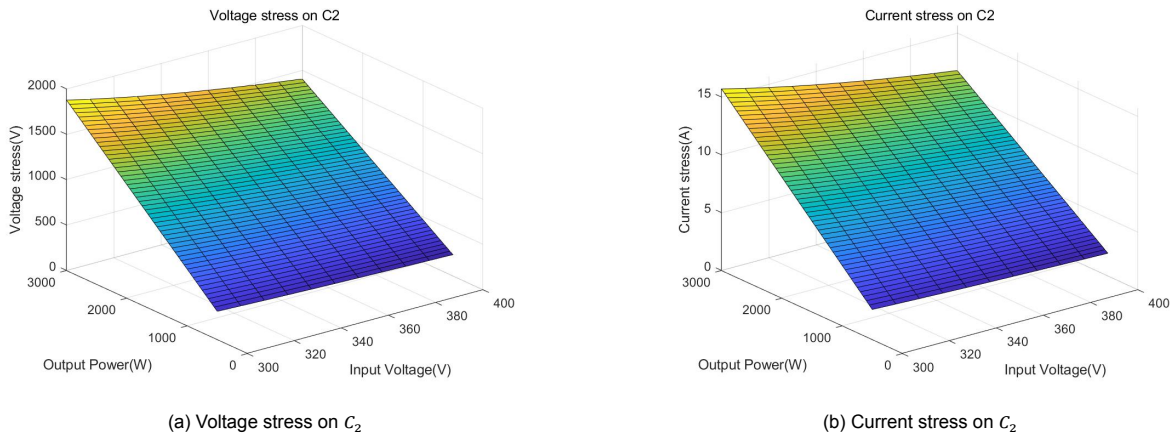
$$R_{DC} = \frac{\rho l_w}{S} = \frac{1.72 \times 10^{-8} \times 1.2975}{600 \times \pi \times \left(\frac{71 \times 10^{-6}}{2}\right)^2} = 9.4 \text{ m}\Omega \quad (4.4)$$

$$P_W = I_{Lf1rms}^2 R_{DC} = 0.65 \text{ W} \quad (4.5)$$

4.1.2. Compensation capacitors design and power loss calculation

Before the capacitor design, the voltage and current stress on each compensation capacitor need to be calculated. For safety reason, the voltage and current peak on each component is used here.

Assuming the input voltage range is 300 V – 400 V and the output power range is 500 W – 3000 W, the voltage and current stress on each compensation capacitor within the range can be calculated based on section 2.3.1 and presented by figures 4.3, 4.4 and 4.5.

Figure 4.3: Voltage and current stresses on C_{f1} Figure 4.4: Voltage and current stresses on C_1 Figure 4.5: Voltage and current stresses on C_2

From the figures above, it can be seen that the largest voltage and current on C_{f1} are 875.47 V and 17.46 A when V_{DC} is 300 V and P_{out} is 3000 W.

The voltage and current on C_1 is only decided by V_{DC} . When V_{DC} is 400 V, the voltage and current stress applied to C_1 is the largest, which are 1323.95 V and 10.16 A, respectively.

The voltage and current on C_2 is proportional to P_{out} , and inversely proportional to V_{DC} . Therefore, when V_{DC} is 300 V and P_{out} is 3000 W, the voltage and current stress on C_2 is the largest, which are 1876.66 V and 15.71 A respectively.

Compensation capacitor design

For compensation capacitors, a 6.8 nF (650 V_{rms}) capacitor (KEMET R76TF16805050J) is used as the unit capacitor. From datasheet, the resistance of each unit capacitor is $R_s = 93.62 \text{ m}\Omega$. The maximum voltage of one unit capacitor is 650 V, and the maximum current of one unit capacitor is 1.8 A.

- C_{f1} is required to be 37.34 nF and is designed as $6.8 \text{ nF} \cdot 2 \times 11 = 37.4 \text{ nF}$. The voltage on each unit capacitor is $\frac{875.47 \text{ V}}{2} = 437.74 \text{ V}$, which is smaller than 650 V. The current on each unit capacitor is $\frac{17.46 \text{ A}}{11} = 1.59 \text{ A}$, which is smaller than 1.8 A.
- C_1 is required to be 14.36 nF and is designed as $6.8 \text{ nF} \cdot 4 \times 8 = 13.6 \text{ nF}$. The voltage on each unit capacitor is $\frac{1323.95 \text{ V}}{4} = 330.99 \text{ V}$, which is smaller than 650 V. The current on each unit capacitor is $\frac{10.16 \text{ A}}{8} = 1.27 \text{ A}$, which is smaller than 1.8 A.
- C_2 is required to be 15.67 nF and is designed as $6.8 \text{ nF} \cdot 4 \times 9 = 15.3 \text{ nF}$. The voltage on each unit capacitor is $\frac{1876.66 \text{ V}}{4} = 469.17 \text{ V}$, which is smaller than 650 V. The current on each unit capacitor is $\frac{15.71 \text{ A}}{9} = 1.75 \text{ A}$, which is smaller than 1.8 A.

Capacitors power loss calculation

Based on the capacitor design above, the equivalent resistance of each capacitor can be calculated. Using the rms current value on each capacitor given in table 4.2, the power loss of capacitors under rated condition can be derived.

- Power loss on C_{f1}

$$R_{C_{f1}} = \frac{2}{11} R_s = 0.017 \Omega$$

$$P_{C_{f1}} = I_{C_{f1}rms}^2 R_{C_{f1}} = 2.06 \text{ W}$$
- Power loss on C_1

$$R_{C_1} = \frac{4}{8} R_s = 0.0468 \Omega$$

$$P_{C_1} = I_{C_1rms}^2 R_{C_1} = 2.41 \text{ W}$$
- Power loss on C_2

$$R_{C_2} = \frac{4}{9} R_s = 0.0416 \Omega$$

$$P_{C_2} = I_{C_2rms}^2 R_{C_2} = 2.89 \text{ W}$$
- Total capacitors losses
$$P_{Ct} = P_{C_{f1}} + P_{C_1} + P_{C_2} = 7.36 \text{ W}$$

4.1.3. Power electronic component and coil losses

This section will introduce the calculation of energy losses from the primary inverter, secondary rectifier and transmission coils in the wireless power transfer system.

MOSFETs losses

Four MOSFETs (1200V SiC MOSFETs C2M0040120D) form an inverter after the DC voltage source V_{DC} at the primary side. From data sheet, the switching off energy $E_{off} = 15 \mu\text{J}$ and the on resistance is $R_{ds,on} = 50 \text{ m}\Omega$.

Each switch is conducted for only half a cycle, therefore, the rms current on each switch is calculated by $I_{switchrms} = \frac{I_{Lfrms}}{\sqrt{2}} = 5.89 \text{ A}$.

- Conduction loss $P_{switch_conduction} = 4 \times I_{switchrms}^2 R_{ds,on} = 6.94 \text{ W}$

- Switching loss $P_{switch_switching} = 4 \times f \cdot E_{off} = 5.1 \text{ W}$
- Total MOSFETs losses $P_{switch_total} = P_{switch_conduction} + P_{switch_switching} = 12.04 \text{ W}$

Diodes losses

Four diodes (1200V Sic diodes C4D20120D) form a passive rectifier before the DC battery load at the secondary side. From datasheet, the forward voltage of diode is $V_F = 0.8 \text{ V}$ and the resistance of the diode is $r = 75 \text{ m}\Omega$.

Similar to the switch at the front-end, each diode at the back-end only conducts for half a cycle. Therefore, the rms current on each diode is calculated by $I_{Frms} = \frac{I_{C2rms}}{\sqrt{2}} = 5.89 \text{ A}$. The average current on each diode is calculated by $I_{Fav} = \frac{\hat{I}_{C2}}{\pi} = 3.75 \text{ A}$, where \hat{I}_{C2} is the peak current on C_2 .

The power losses on diodes are given by (4.6).

$$P_{diode} = 4 \times \left[V_F \cdot I_{Fav} + r \cdot \left(\frac{I_{Frms}}{2} \right)^2 \right] = 14.6 \text{ W} \quad (4.6)$$

Primary coil and secondary coil losses

The resistance of the primary and secondary coil are $R_{L1} = 650 \text{ m}\Omega$ and $R_{L2} = 440 \text{ m}\Omega$, respectively. Using the rms current values on L_1 and L_2 in table 4.2, the power losses can be derived as follows:

- Power loss on L_1
 $P_{L1} = I_{L1rms}^2 R_{L1} = 33.52 \text{ W}$
- Power loss on L_2
 $P_{L2} = I_{L2rms}^2 R_{L2} = 30.53 \text{ W}$

4.1.4. Efficiency and percentage of each category of power loss

Based on the calculation of various power losses in the above sections, the wireless power transfer system efficiency and the percentage of each power losses source can be drawn as 4.6 and 4.7.

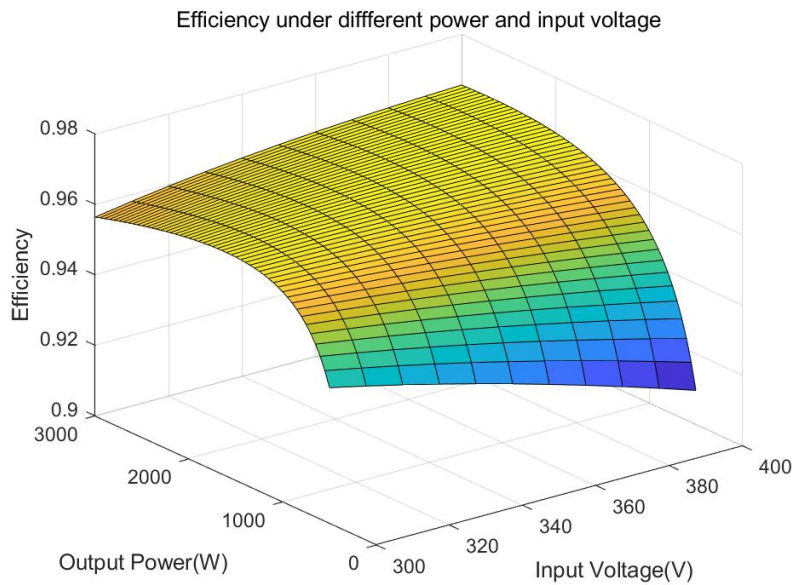


Figure 4.6: Efficiency under different input voltage and output power

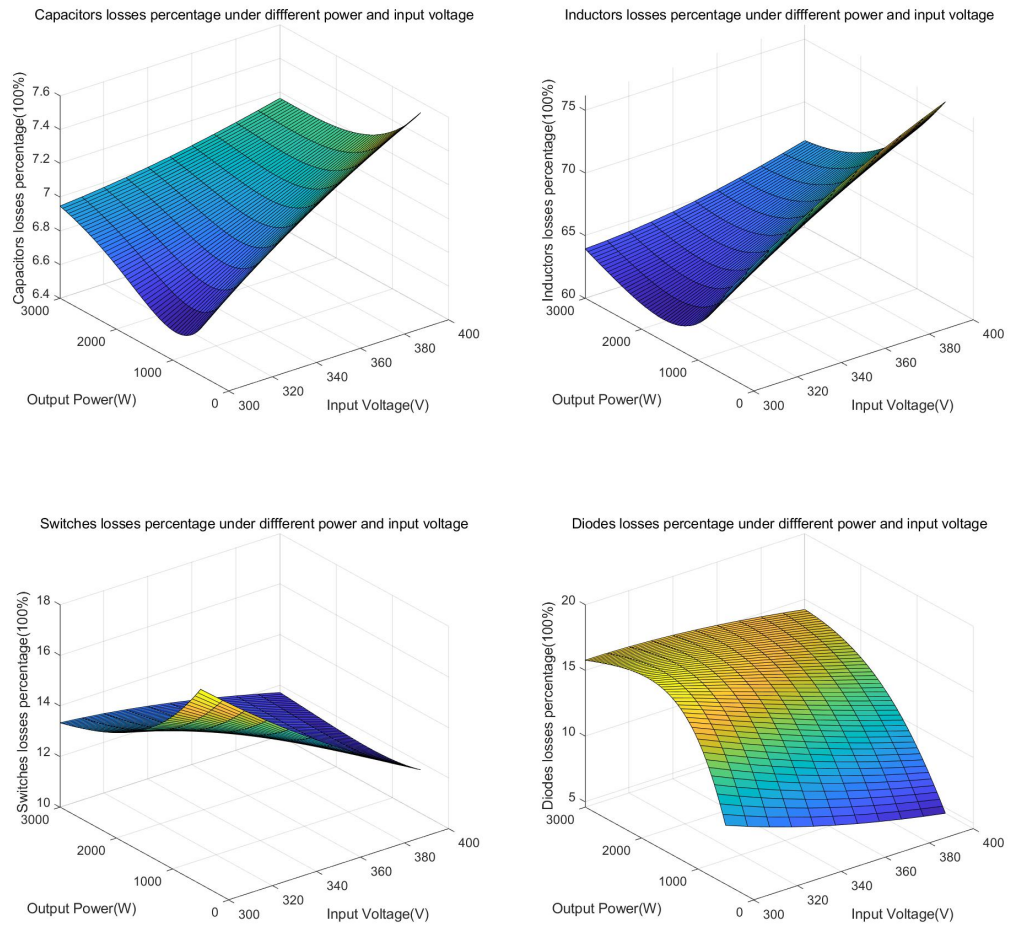


Figure 4.7: Percentage of each power loss under different input voltage and output power

As can be seen from the figure 4.6, the efficiency of the system in the defined rated condition is almost the largest within the range of operating conditions, which is 96.58%. The minimum system efficiency occurs when the system is operating at 400V input voltage and 500W output power. In this case, the system efficiency is 90.96%, which is also acceptable.

In figure 4.7, all power losses are divided into four categories:

- Capacitors losses: Including the losses on capacitors C_{f1} , C_1 and C_2 .
- Inductors losses: Including the losses on compensation inductor L_{f1} and transmission coils L_1 and L_2 .
- Switches losses: Including power losses on four MOSFETs at the front end.
- Diodes losses: Including the power losses on four diodes at the back end.

The percentage of each category of power loss is presented in figure 4.7. As can be seen from the figure, the percentage of inductors power losses is the largest, accounting for about 70% of the total power losses. This is because the resistances of the primary and secondary coils are much larger than the resistances of other components.

Diodes losses percentage is the second largest under high output power because of the high secondary current in this case.

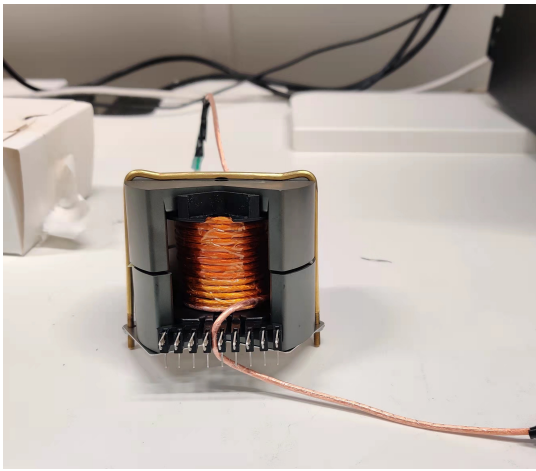
In summary, the most important things to increase the efficiency under high power output is to reduce the power losses on the transmission coils and the back-end diodes.

4.2. Experimental components parameters measurements

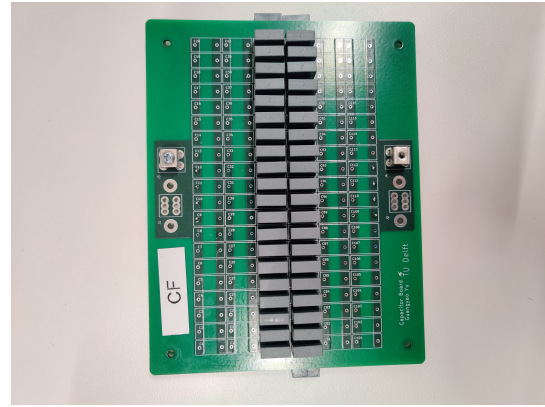
The compensation components measurements under different frequency are shown in table 4.4 and 4.5. In the experiments, $f = 85 \text{ kHz}$.

f (kHz)	20 kHz	40 kHz	60 kHz	80 kHz	85 kHz	100 kHz	120 kHz	140 kHz	160 kHz
$L_{f1} (\mu H)$	100.60	100.50	100.57	100.55	100.50	100.50	100.58	100.60	100.60
$C_{f1} (nF)$	35.84	35.84	35.84	35.85	35.86	35.87	35.88	35.89	35.9
$C_1 (nF)$	14.42	14.43	14.44	14.46	14.46	14.48	14.51	14.56	14.6
Tuned $C_1 (nF)$	13.90	13.90	13.90	13.91	13.92	13.92	13.93	13.94	13.96
$C_2 (nF)$	15.54	15.54	15.54	15.54	15.54	15.54	15.53	15.53	15.53

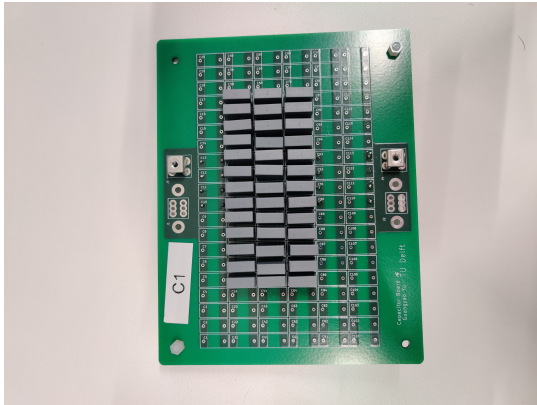
Table 4.4: Measured values of LCC-S compensation components in the experiments



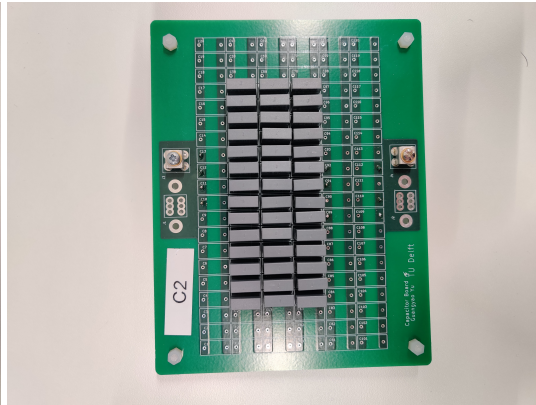
(a) L_{f1}



(b) C_{f1}



(c) C_1



(d) C_2

Figure 4.8: Pictures of compensation components in LCC-S compensation topology

f (kHz)	20kHz	40 kHz	60 kHz	80 kHz	85 kHz	100 kHz	120 kHz	140 kHz	160 kHz
$C_1 (nF)$	10.92	10.92	10.93	10.93	10.93	10.94	10.95	10.96	10.97
$C_2 (nF)$	14.42	14.43	14.43	14.44	14.44	14.44	14.46	14.47	14.48

Table 4.5: Measured values of S-S compensation components in the experiments

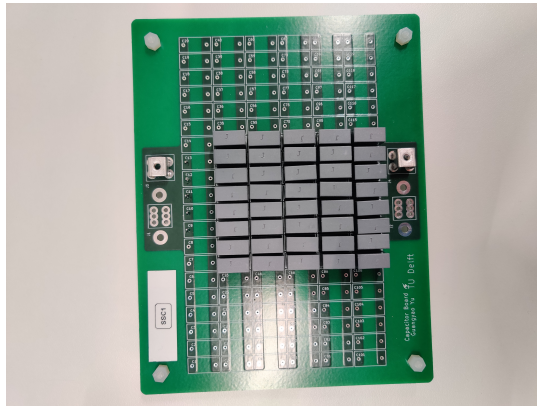
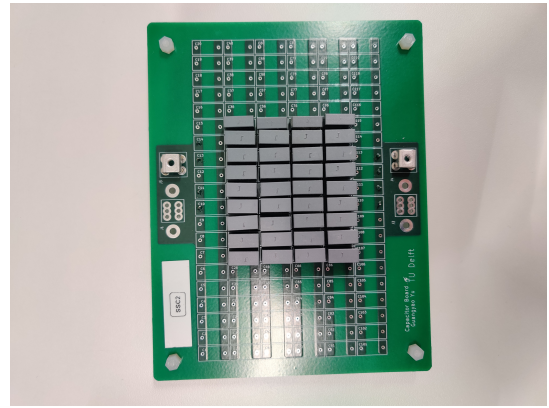
(a) C_1 (b) C_2

Figure 4.9: Pictures of compensation components in S-S compensation topology

The measurements of transmission coils parameters are shown in table 4.6. All these values are measured under 85 kHz. In this case, since the secondary coil is not flat, the left, middle and right distances between the primary coil and the secondary coil are listed in table 4.7.

L_1 (μH)	L_2 (μH)	M (μH)	R_{L_1} ($m\Omega$)	R_{L_2} ($m\Omega$)
339.0	226.5	106.0	640.0	400.8

Table 4.6: Transmission coils parameters measurements

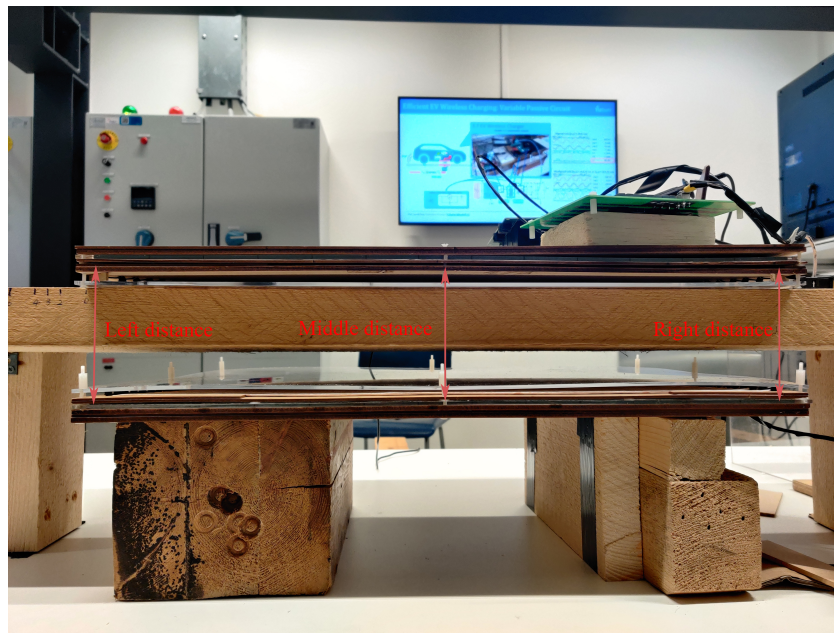


Figure 4.10: Primary and secondary coils

Left distance (cm)	Middle distance (cm)	Right distance (cm)
10.3	10.1	10.1

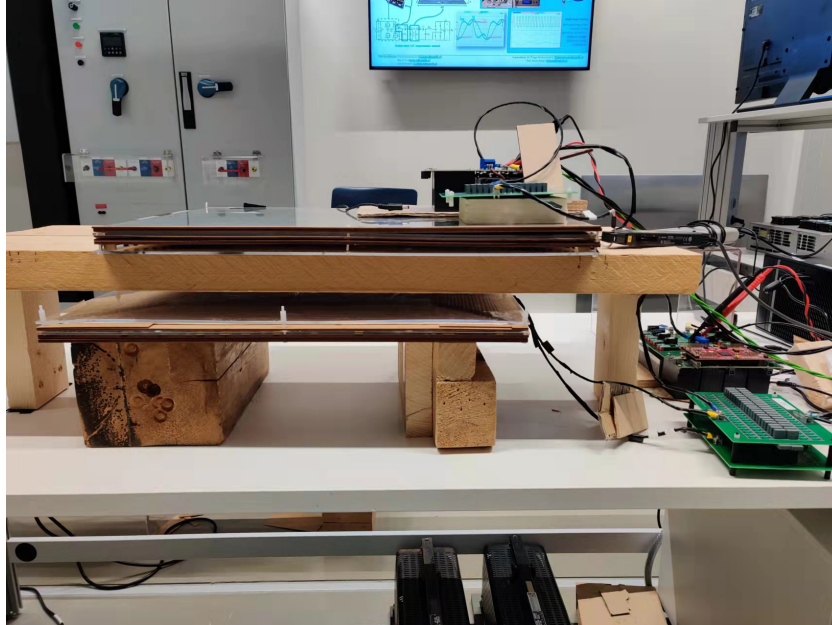
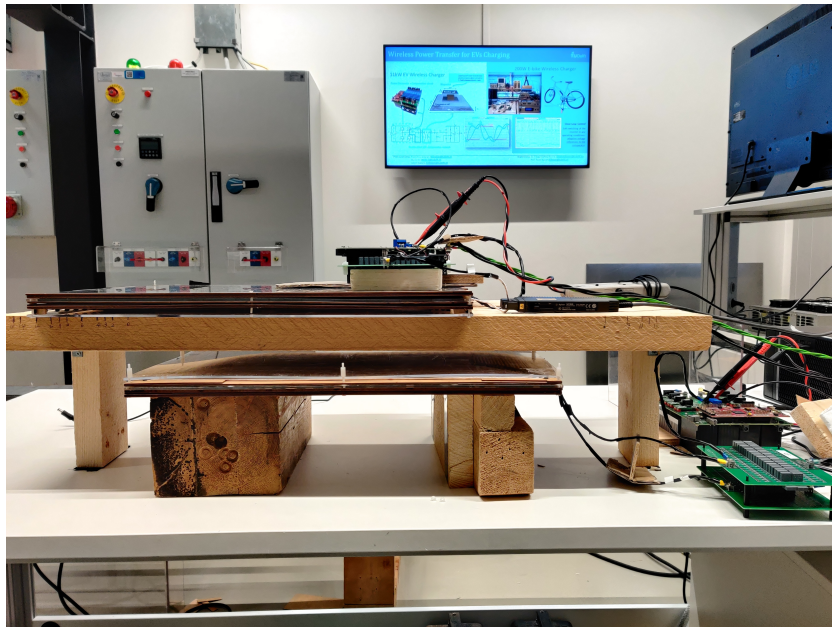
Table 4.7: Transmission coils distances

To test the properties of the system operating under misalignment, a lateral misalignment is introduced between the primary and secondary coils, and the variations of mutual inductance M are shown in table 4.8.

Lateral misalignment (cm)	6	7	8
Mutual inductance (μH)	97.75	94.95	91.65
Lateral misalignment (cm)	11	12	13
Mutual inductance (μH)	81.85	79.40	76.95

Table 4.8: Mutual inductance under lateral misalignment

In the experiment, the lateral misalignment is set to be 8 cm and 13 cm individually, as shown in figures 4.11 and 4.12. The mutual inductance are $91.65 \mu H$ and $76.95 \mu H$, respectively.

Figure 4.11: Lateral misalignment (8 cm) $M = 91.65 \mu H$ Figure 4.12: Lateral misalignment (13 cm) $M = 76.95 \mu H$

4.3. S-S and LCC-S efficiency comparison

To compare the efficiency of the S-S and LCC-S compensation more fairly, the output voltage of these two compensation topologies are fixed at 370 V and 425 V, respectively. The input power is increased from 500 W to 3000 W. The efficiency under these conditions are shown in figure 4.13 and 4.14.

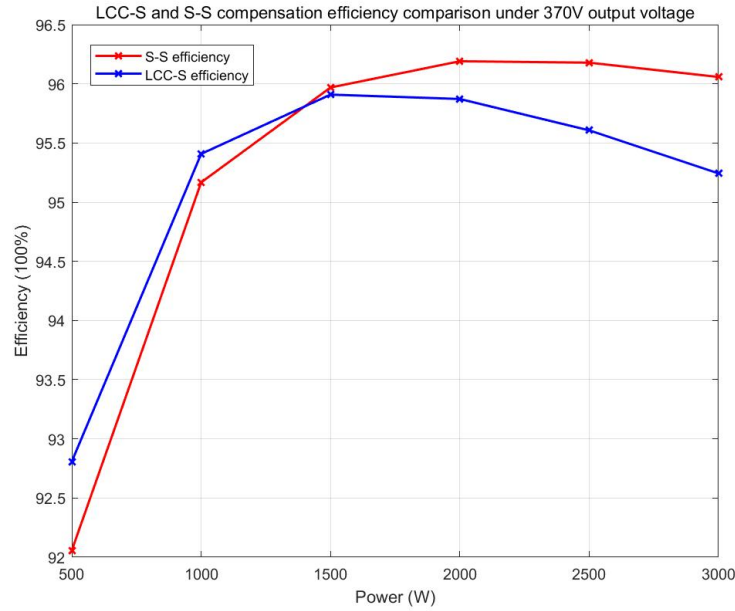


Figure 4.13: LCC-S and S-S compensation efficiency comparison under 370 V output voltage

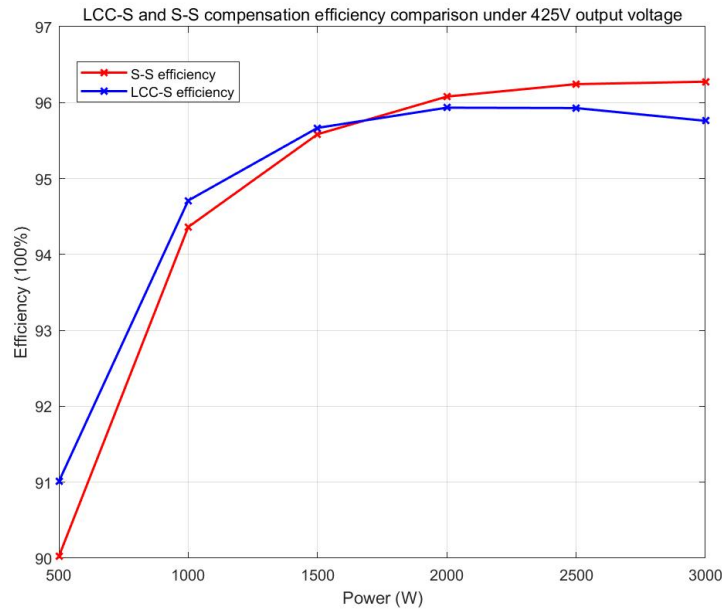


Figure 4.14: LCC-S and S-S compensation efficiency comparison under 425 V output voltage

When output voltage and power are the same, R_{Bat} and R_{ac} of these two compensation topologies are the same. Therefore, as analysed in section 2.2.1 and 2.3.1, the efficiency of these two topologies should be the same. However, the losses on the compensation components are not considered in

the analyses in section 2.2.1 and 2.3.1. Since there are more compensation components in LCC-S topology, the losses on compensation components of LCC-S topology are higher. Therefore, the efficiency of S-S compensation is higher.

When the system is operating at low power, V_{in} of LCC-S compensation is constant. However, V_{in} of S-S compensation will reduce to a small value, and a high input current is required, as shown in figure 4.15. This high input current causes high conduction loss on the front-end MOSFETs. Therefore, the efficiency of S-S compensation could be lower than LCC-S compensation under low input power.

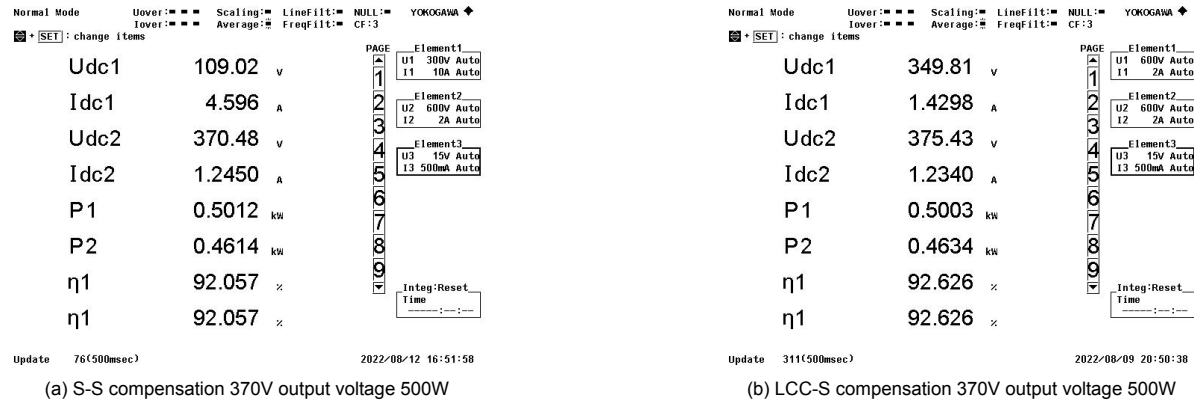


Figure 4.15: Efficiency of S-S and LCC-S compensation with fixed output voltage at 500 W

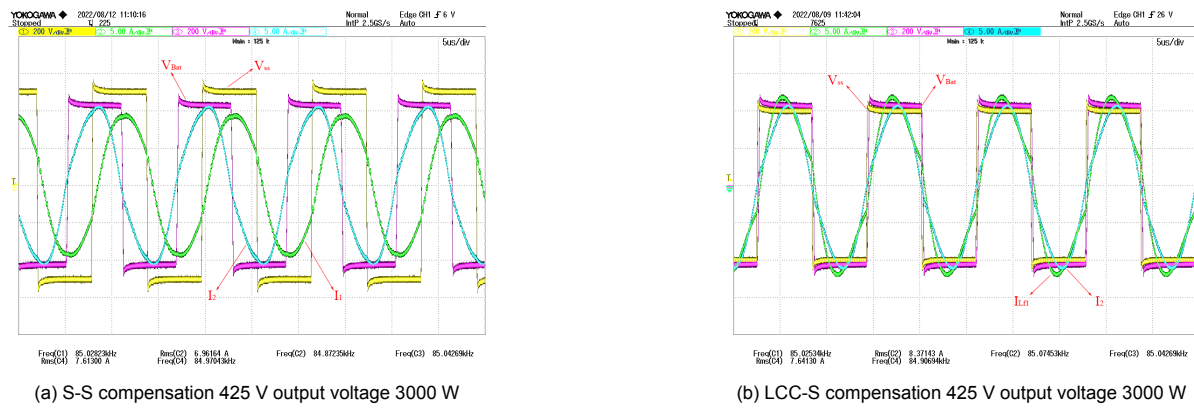


Figure 4.16: S-S and LCC-S compensation with fixed output voltage at 3000 W

Based on the analyses above, it can be concluded that when the output voltage is fixed, S-S compensation performs better than LCC-S in terms of efficiency at high power due to fewer compensation components. However, at low power, the efficiency of S-S compensation is lower than LCC-S compensation due to the higher conduction losses on MOSFETs.

In addition, LCC-S is better than S-S in terms of safety. Since S-S compensation has current-source characteristics, when the load side is open, the voltage at two ends of the open circuit is theoretically infinite, which may cause damage to the load-side equipment. As for the LCC-S topology, it has voltage-source characteristic, and when the load side is open, it won't influence the load-side equipment. However, since the output of S-S compensated WPT system features a CC output, it can be directly connected to batteries, while for LCC-S compensation, a back-end DC/DC converter is needed to regulate the charging current and voltage.

4.4. Resonant inductor voltage peak calculation method verification

To verify the resonant inductor voltage peak calculation method, the S-S compensation and LCC-S compensation are used.

In the experiment for LCC-S compensation, N2791A High-Voltage differential probe is used to measure the voltage, and it can measure up to 700 V voltage. Therefore, to avoid over-range, the voltage stresses tests are conducted under 500 W.

Figure 4.17 shows the voltage stresses in the experiment under 250 V input voltage and 500 W input power in LCC-S compensation. The waveforms of $V_{L_{f1}}$ and V_{L_1} are similar to the simulated voltages shown in figure 3.3, which are the superposition of the fundamental-waveform and the square-waveform. Therefore, the fundamental analysis can not give a precise voltage peak of $V_{L_{f1}}$ and V_{L_1} . When under different input voltages, the waveforms of these voltages are also similar.

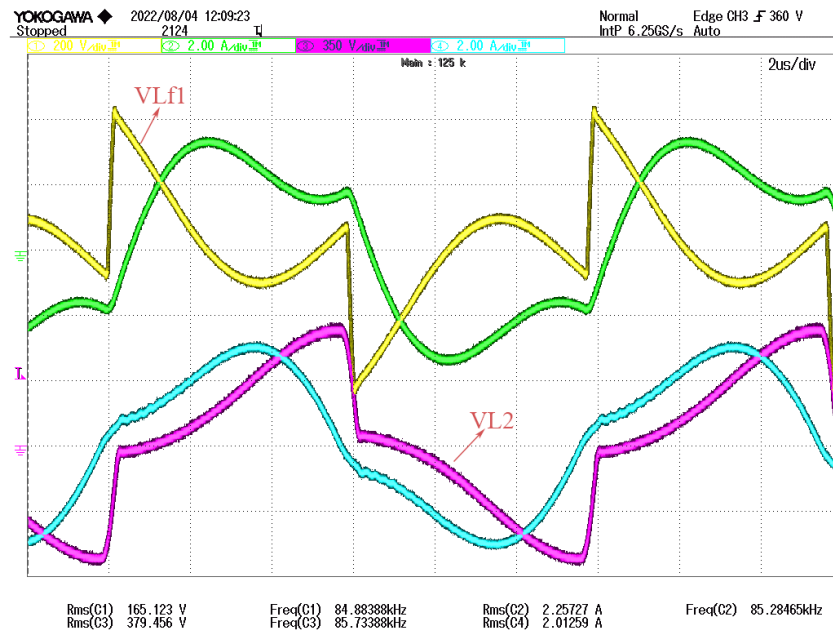


Figure 4.17: Voltage stresses under 250 V input voltage and 500 W input power in LCC-S compensation

The measured voltage peaks and the resonant inductor voltage peak calculation method results and the results of fundamental analysis are shown in figure 4.18. As can be seen from the figure, the resonant inductor voltage peak calculation method can calculate the peak-voltages on the resonant inductors much more accurately.

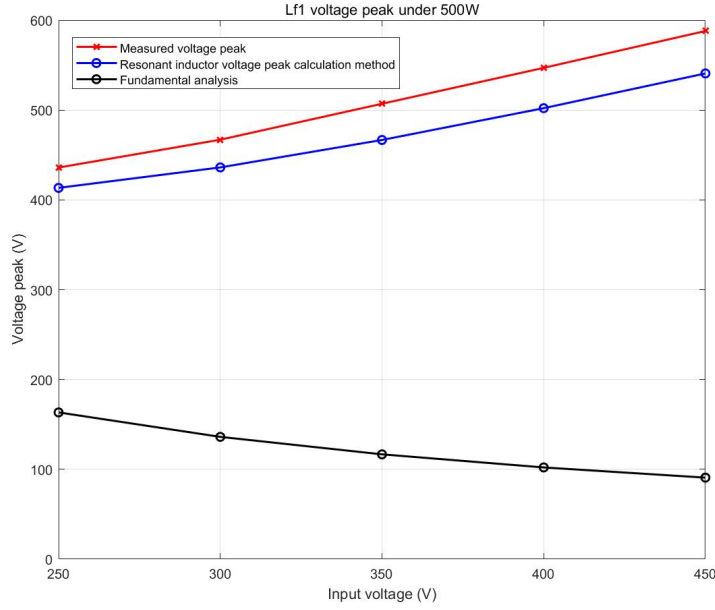
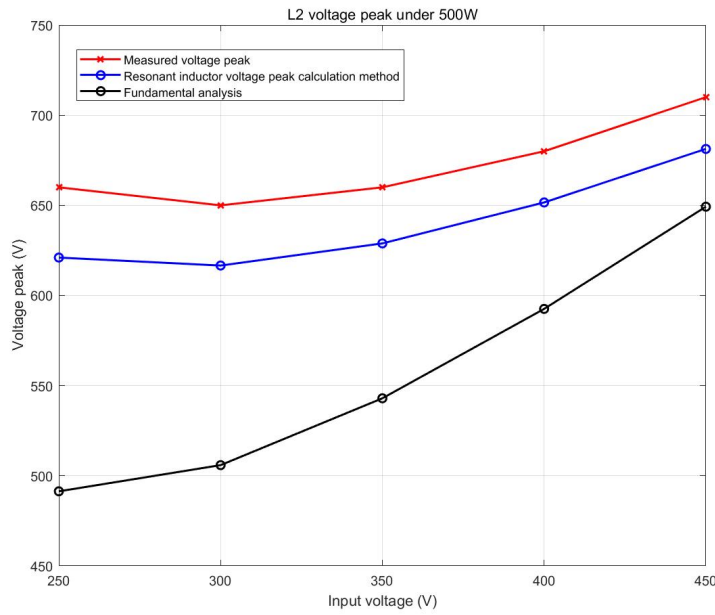
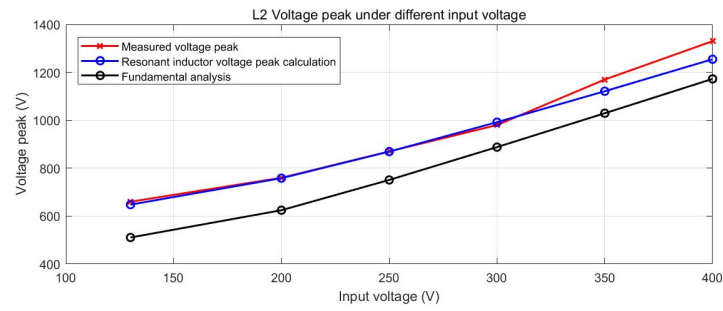
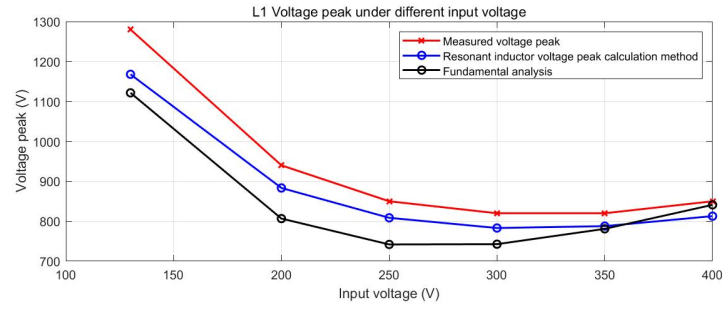
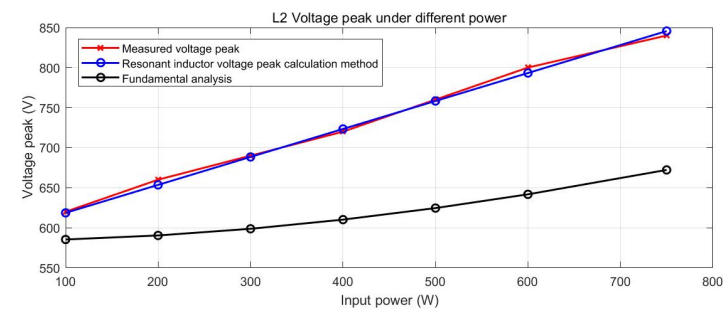
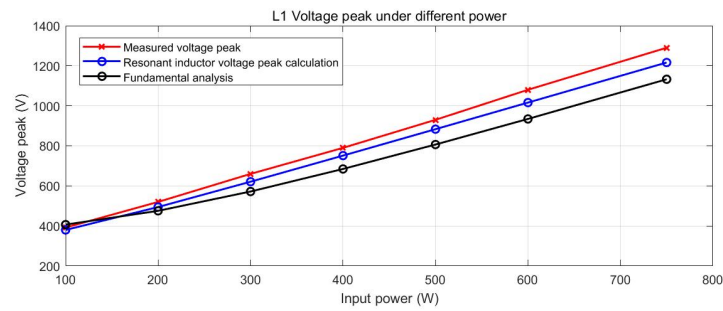
(a) Voltage peaks on L_{f1} in LCC-S compensation(b) Voltage peaks on L_2 in LCC-S compensation

Figure 4.18: Comparison of resonant inductor voltage peak calculation method and fundamental analysis with experimental results for LCC-S compensation

For S-S compensation, the voltage peaks on L_1 and L_2 are measured to verify the resonant inductor voltage peak calculation method. The experiments are conducted under different voltages and different power. The input power is fixed at 500 W when tested under different voltages, and the input voltage is fixed at 200 V when tested under different power. As can be seen from figure 4.19, the voltage stresses on the coils are the superposition of sinusoidal wave and square wave, as analyzed in section 3.1.1. The test results are shown in figure 4.19.

(a) Inductors voltage stresses under different V_{in} in SS compensation

(b) Inductors voltage stresses under different power in S-S compensation

Figure 4.19: Comparison of resonant inductor voltage peak calculation method and fundamental analysis with experimental results for S-S compensation

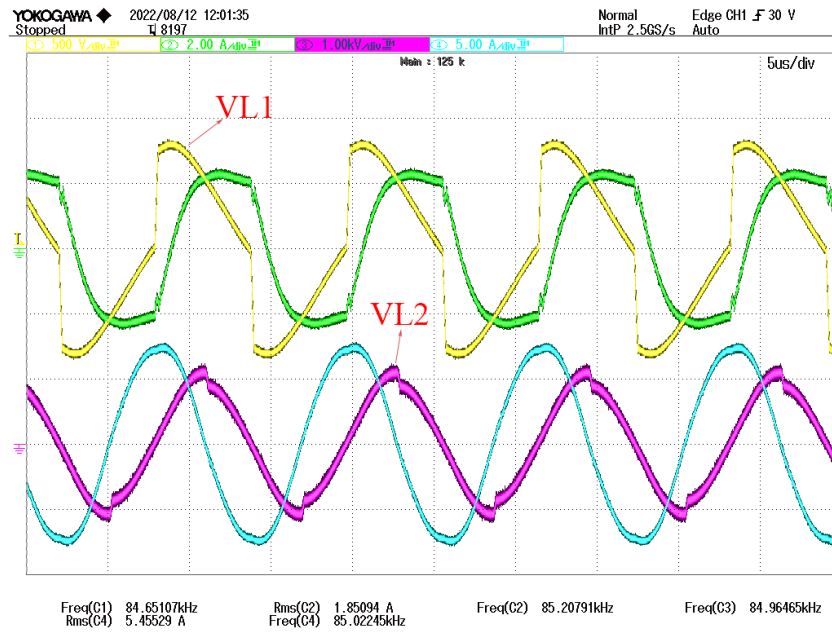


Figure 4.20: Voltage stresses under 350 V input voltage and 500 W input power in S-S compensation

Based on the above experimental verification, the resonant inductor voltage peak calculation method proposed in this article outperforms the fundamental analysis method in various cases in S-S and LCC-S topologies. Therefore, this calculation method can play an important role in breakdown voltage design for resonant inductors.

4.5. Switching current calculation method verification

To verify the switching current calculation method, the LCC-S compensation topology is experimented with different voltages, different power and different mutual inductances. In addition, two capacitors C_1 are used for experiments separately (as shown in table 4.4). The tuned C_1 with a smaller capacitor value is used to verify the effect of the tuning method on the switching current. Based on the measured components values in tables 4.4, 4.6, and 4.8, the tuning modification factor of each component can be obtained by applying the equation (3.27), and summarized in table 4.9. Substitute these modification factors in the switching current calculation method, the switching current under each condition can be obtained.

n_1	0.9789
$n_{1,tuned}$	0.9449
n_f	1.0302
n_2	1

Table 4.9: Modification factors in experiments

Figure 4.21 shows the switching current point under 400 V input voltage and 1000 W input power, which is the same working condition as shown in figure 3.9 in section 3.4. It can be seen that the waveform of the current is similar to the simulated one, and the switching current values are also close.

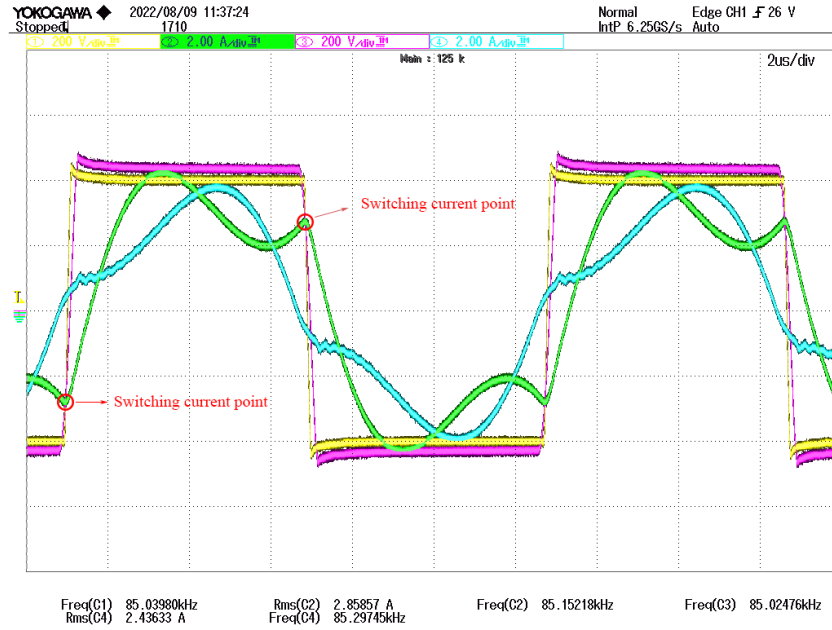
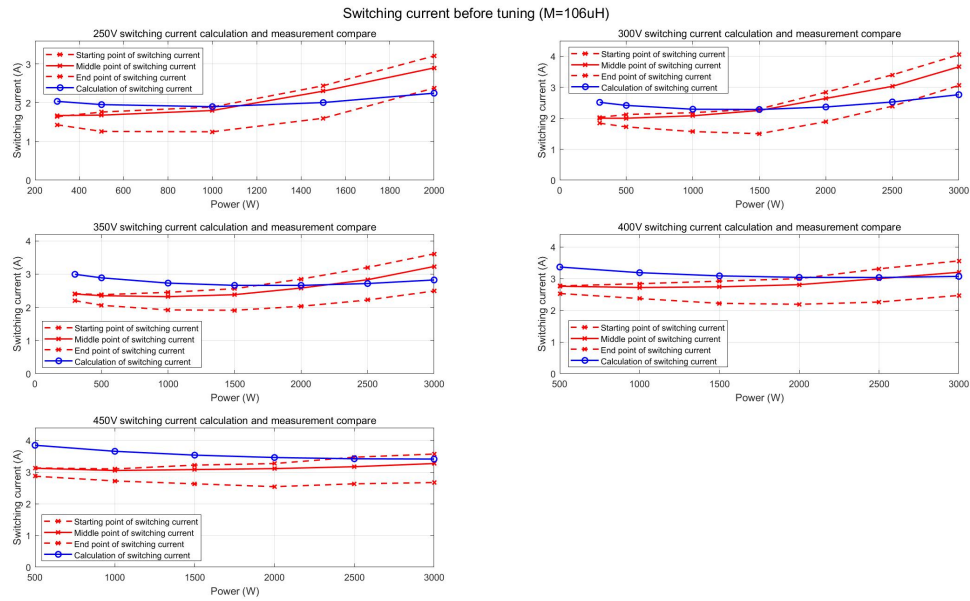
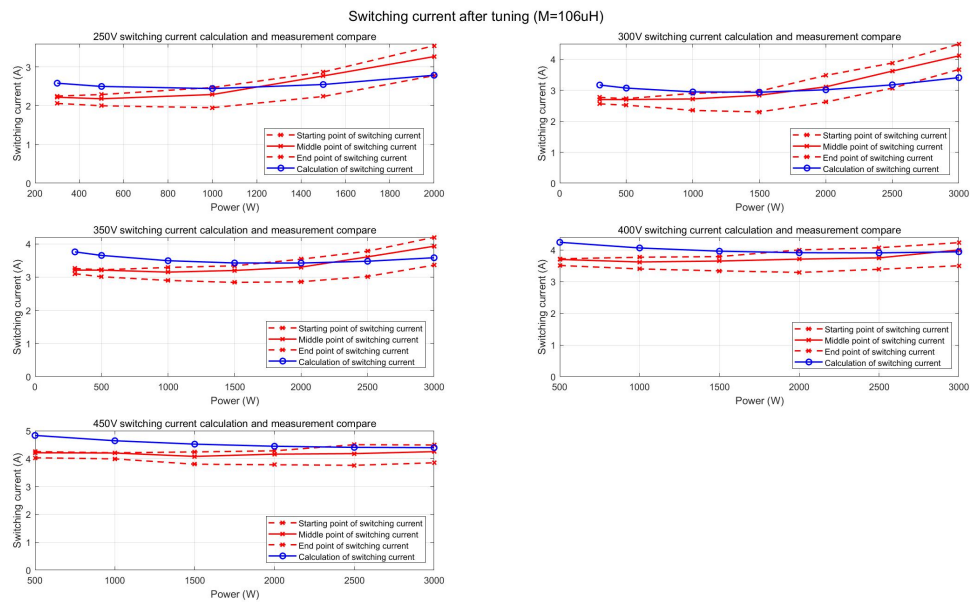
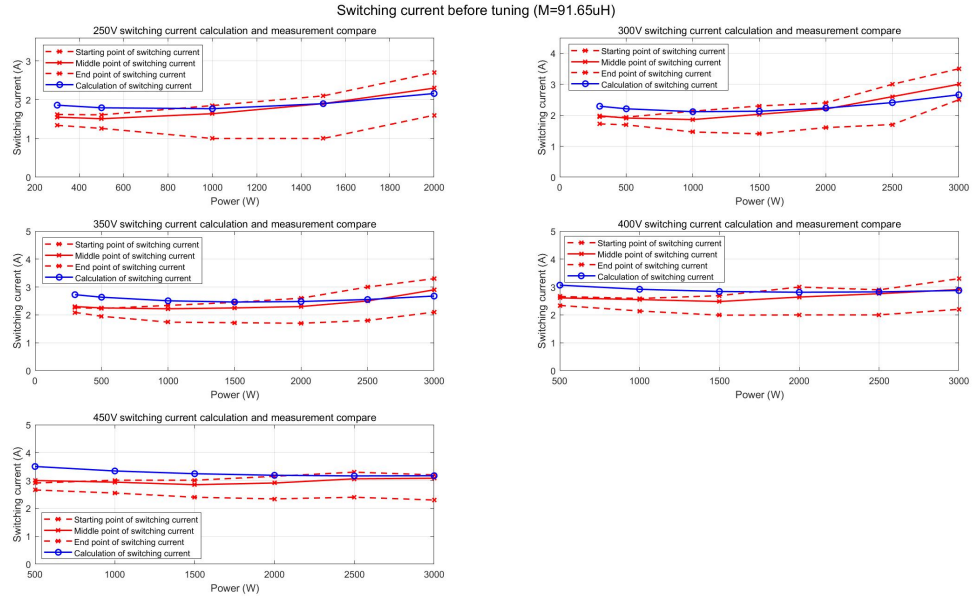
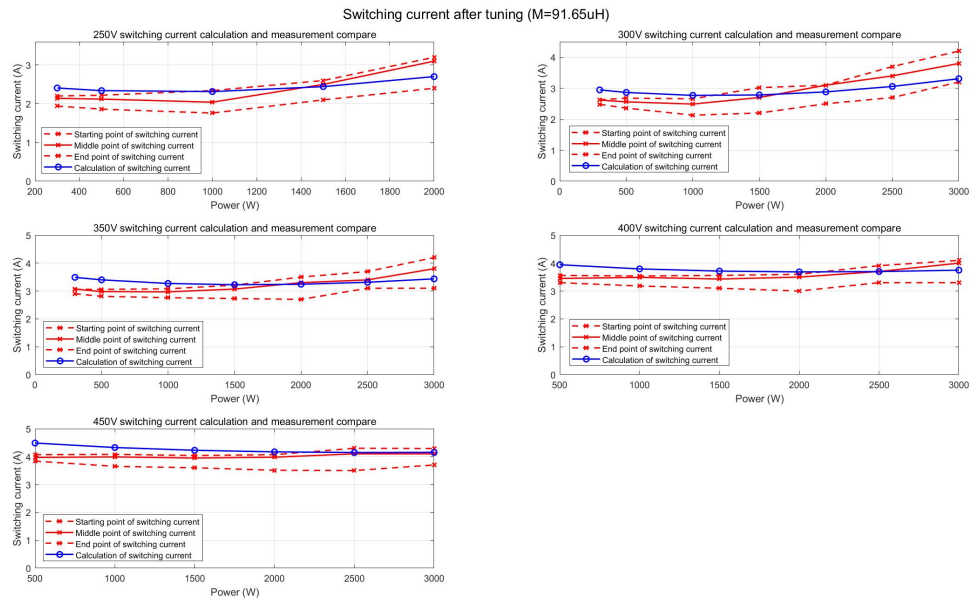
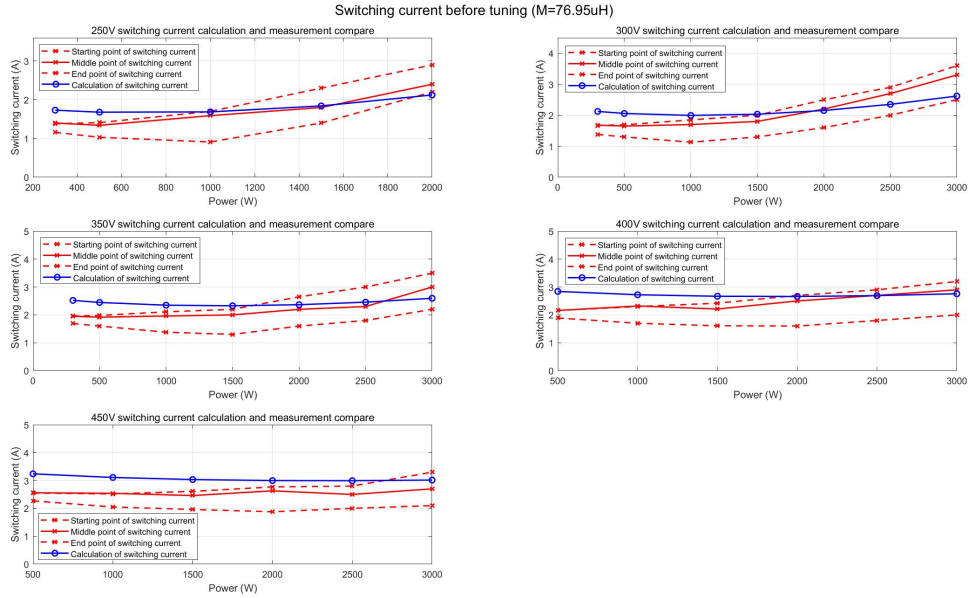
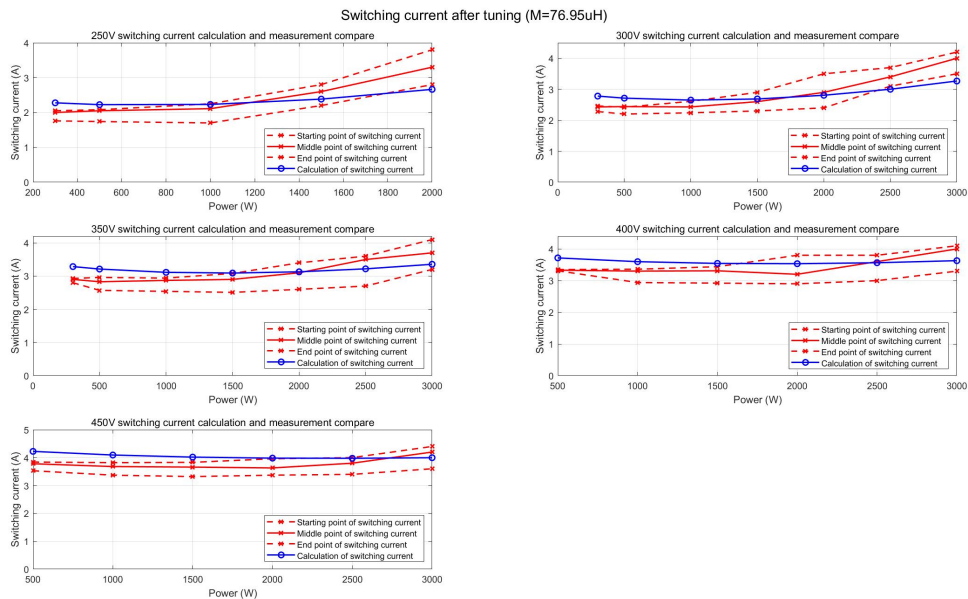


Figure 4.21: Switching current point in experiment at 400 V input voltage and 1 kW input power.

It can be seen from figure 4.21 that although the front-end MOSFETs switching time is very short (around 100-200 ns), the switching current is not a fixed value during this process due to the fast switching current change. Therefore, the current value when V_{ss} crossing 0 (which is also the zero-phase point in the previous analyses) is chosen to represent the switching current value, and shown in the test results figures 4.23-4.27 as solid lines with cross. The switching current values at the beginning and the end of switching are also presented in the test results figures as dotted lines with cross.

Figure 4.22: Switching current before tuning ($M=106\mu\text{H}$)Figure 4.23: Switching current after tuning ($M=106\mu\text{H}$)

Figure 4.24: Switching current before tuning ($M=91.65\mu\text{H}$)Figure 4.25: Switching current after tuning ($M=91.65\mu\text{H}$)

Figure 4.26: Switching current before tuning ($M=76.95\mu\text{H}$)Figure 4.27: Switching current after tuning ($M=76.95\mu\text{H}$)

From these test result plots, it can be seen that the switching current calculation method proposed in this article can calculate the switching current values under all kinds of operating conditions. In addition, the experiments also verify that tuning the value of capacitor C_1 can increase the switching current value and successfully predict the switching current value after tuning with the switching current calculation method. It is also experimentally demonstrated that under misalignment, the switching current values generally decrease in all operating conditions, making the implementation of ZVS more difficult.

The efficiency data for these tests are shown in figure 4.28. In practice, although the switching current needs to be large enough to satisfy the ZVS implementation, excessive switching current can also cause increased losses on MOSFETs, (in fact, the efficiency after tuning capacitor C_1 are generally

slightly lower than before the tuning, since the set up used in experiments is easy to achieve ZVS, and has already achieved ZVS before tuning). Therefore, the design of switching current requires cautious consideration. The switching current calculation method proposed in this article can be of great use in switching current design.

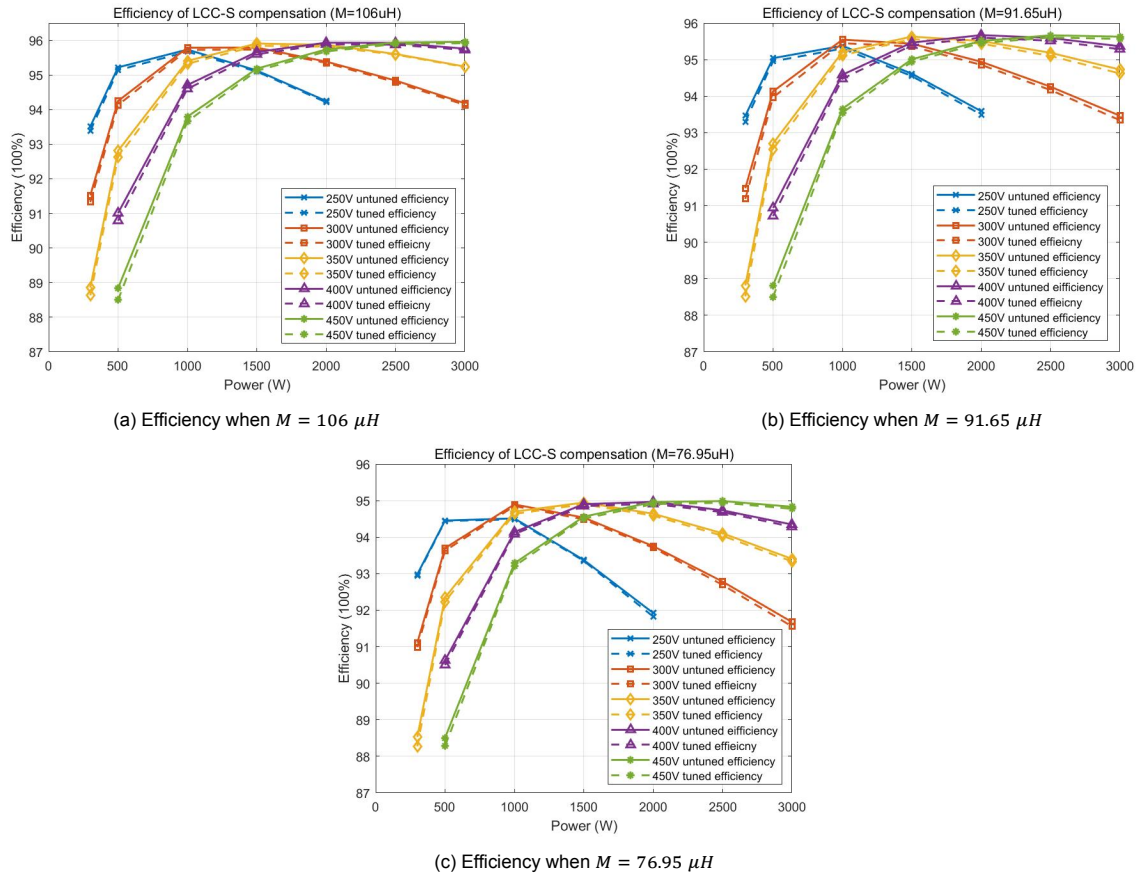


Figure 4.28: Efficiency of LCC-S under aligned and misaligned conditions

Conclusion

In this thesis, a benchmark of different compensation topologies is given, based on which two optimal compensation topologies are selected for further study. In the design process of compensation, two critical issues, components stress and implementation of ZVS, are studied in depth in this thesis. Regarding these two issues, a new resonant inductor voltage stress calculation method and a new switching current calculation method are proposed and experimentally verified, respectively. The conclusions of this thesis can be basically summarized as follows:

- **Conclusion for benchmark of different compensation topologies**

This thesis gives a benchmark of 8 different compensation topologies under the rated condition based on SAE standard. All these compensation topologies are comprehensively compared in terms of efficiency, components voltage/current stress, design freedom, misalignment behaviour, cost, etc.

In the simulation and calculation analyses in chapter 2, the LCC-S and S-S topologies outperform other compensation topologies in most aspects. Therefore, in chapter 4, a further experimental analyses of these two topologies are performed. After conducting the experimental analyses, the following more specific conclusions on these two compensation topologies can be drawn:

1. Although the efficiency expressions for S-S and LCC-S compensation are the same for a given output voltage and power (when only the primary and secondary coils impedance are considered), in practice, S-S compensation is more efficient in the high power case due to more power losses on compensation components in LCC-S compensation topology. However, in the low power case, due to a higher input current, the conduction losses on switches are higher in S-S compensation, which makes LCC-S compensation more efficient.
2. Due to the CC characteristic of S-S compensation topology, when the load is open or the load current is 0, the voltage across the load is theoretically infinite, easily causing damage to the equipment at the load. However, the LCC-S compensation which features CV does not have this problem.

Therefore, the choice of compensation topology for these two types needs to be considered in terms of operating conditions, design freedom requirement and safety issues, etc.

- **Conclusion for resonant inductor voltage peak calculation method**

In this article, the study of resonant inductor voltages in S-S and LCC-S compensation topologies is given to explain the formation of voltage waveform on resonant inductors. Based on that, a resonant inductor voltage peak calculation method is proposed. Experimental validation proves that this calculation method is more accurate than the traditional fundamental-frequency analysis in all operating conditions.

- **Conclusion for switching current calculation method**

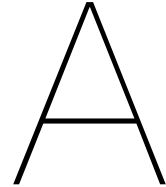
In this thesis, the effects of high-order harmonics of the front-end and back-end voltages, the parasitic capacitance of the back-end rectifier diodes and components sensitivity on the switching current are analyzed and calculated. Experiments verifies that the switching current calculation method proposed in this article can give an accurate value of the switching current under various operating conditions.

Based on the analyses and experimental results, it can be concluded that the implementation of ZVS becomes more difficult under misalignment. However, a high value of the switching current could lead to an increase on losses on MOSFETs and thus to a decrease in efficiency. Therefore, the design of the switching current needs to be taken into caution.

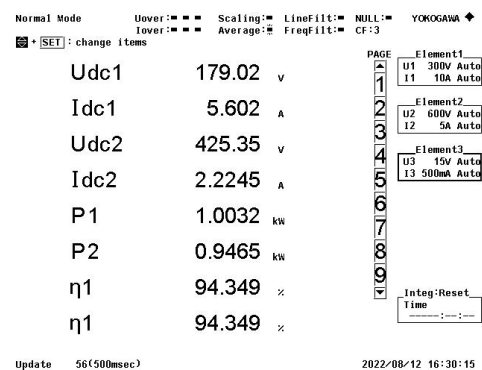
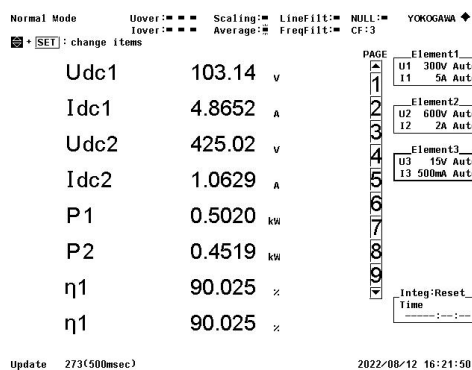
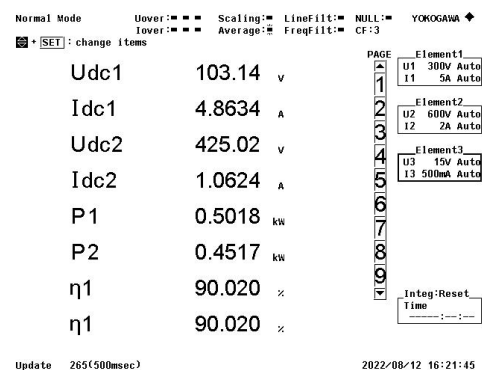
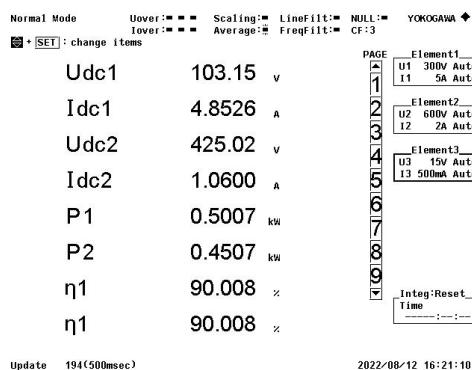
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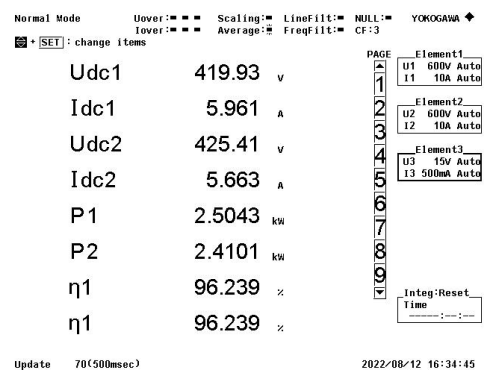
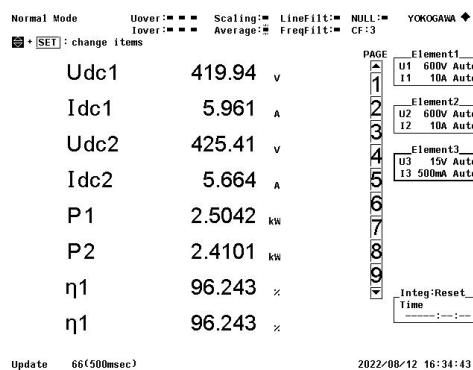
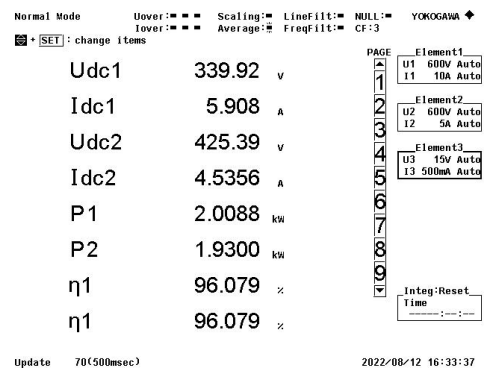
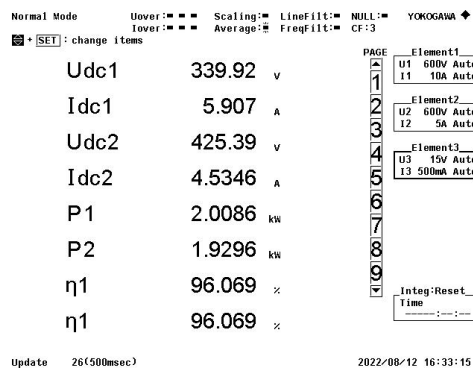
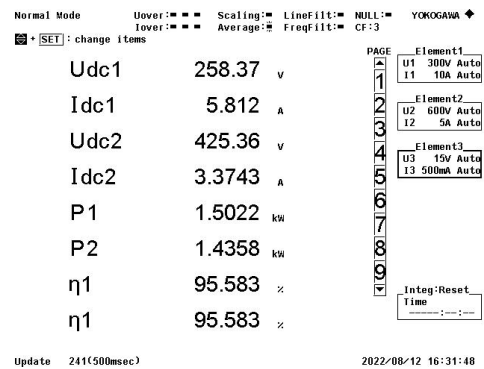
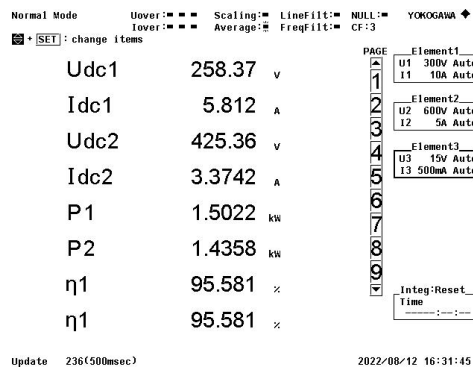
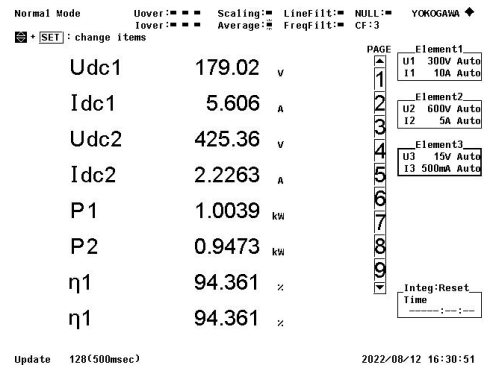
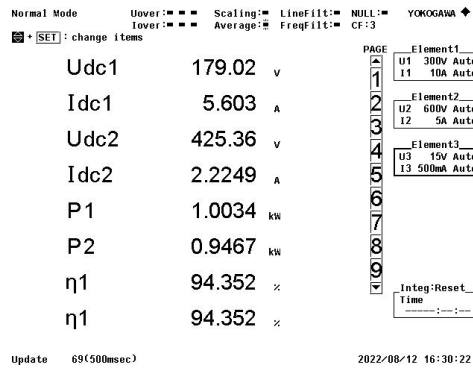
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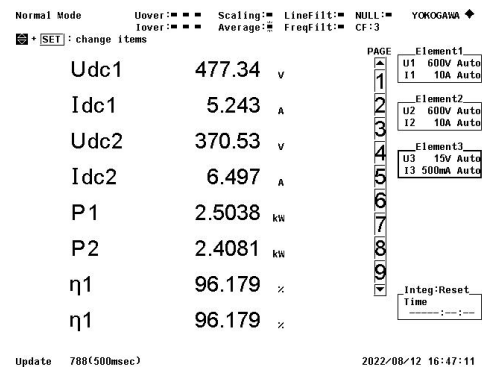
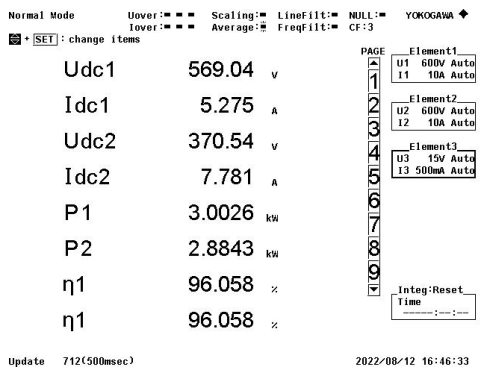
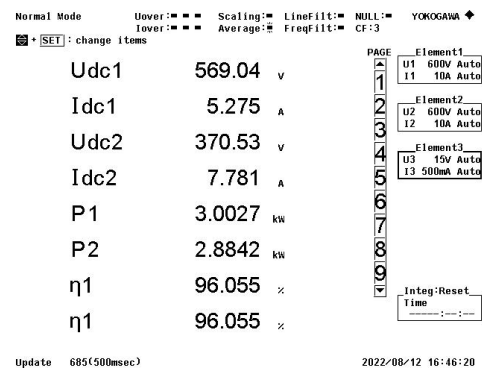
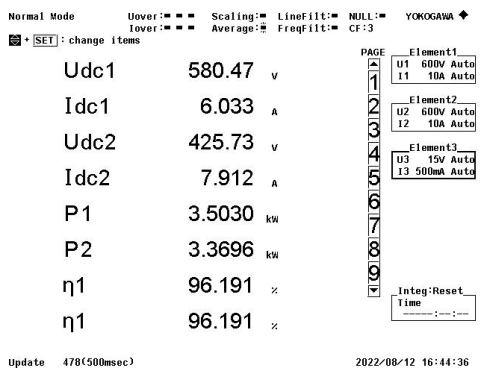
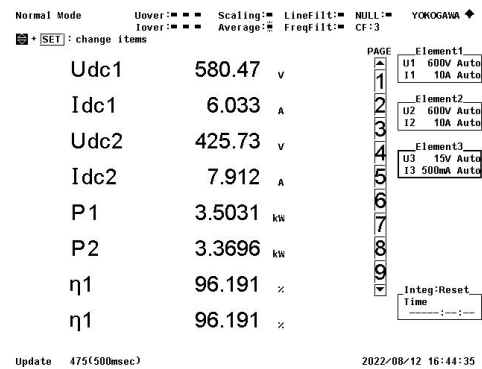
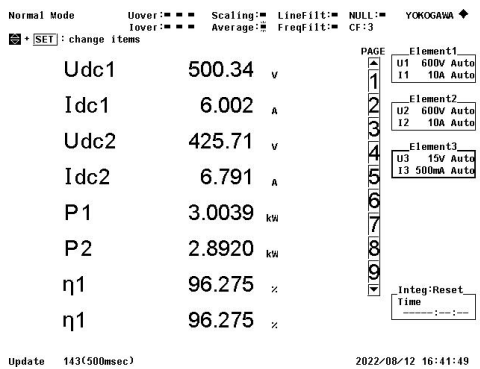
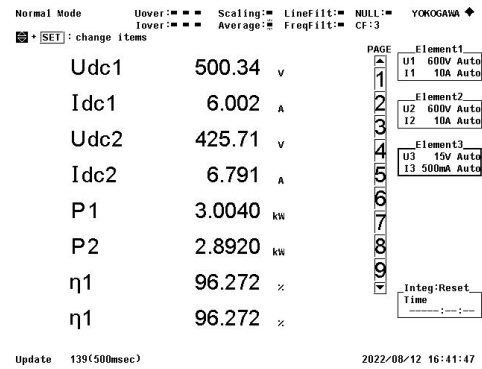
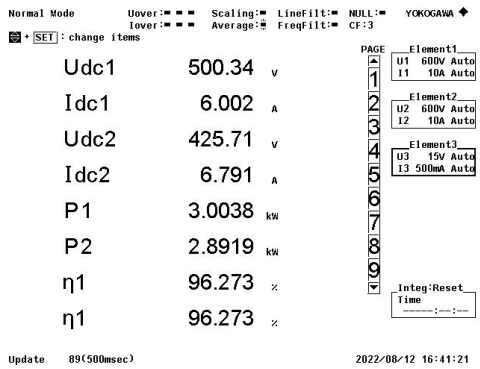
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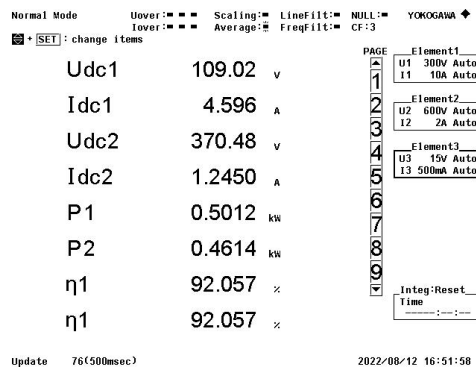
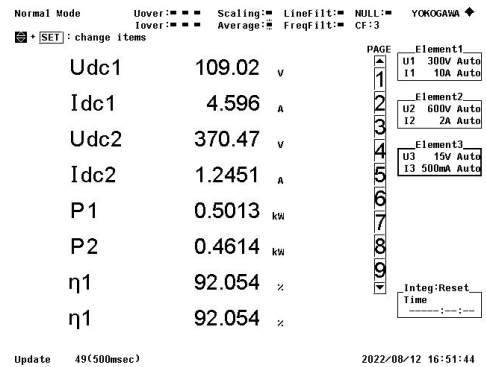
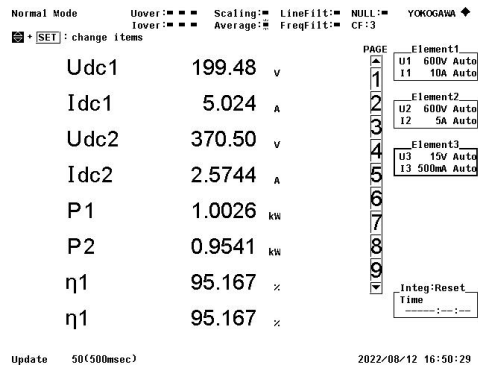
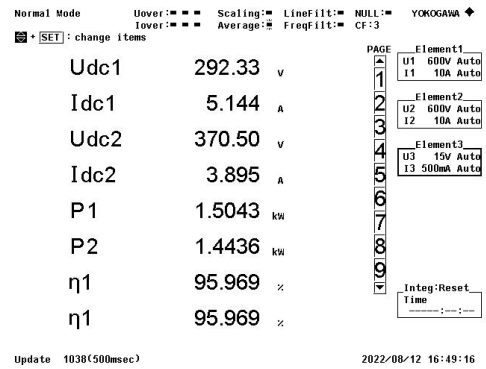
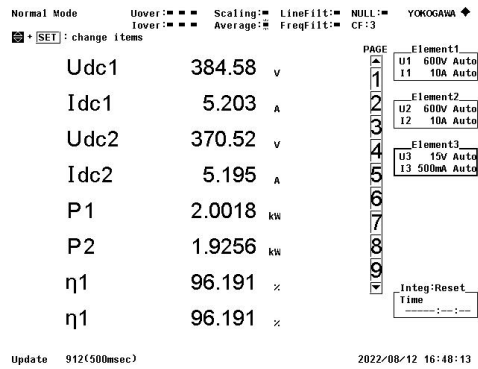


Appendix A: Efficiency of S-S compensation topology with fixed output voltage



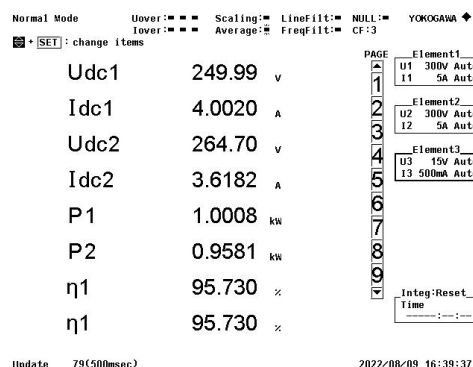
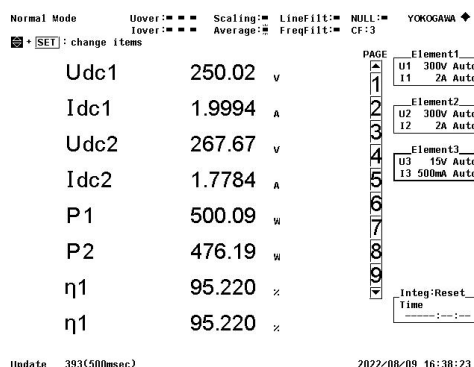
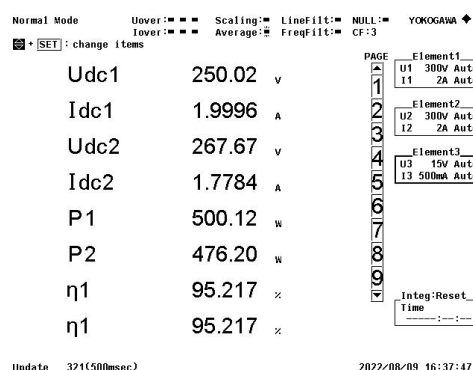
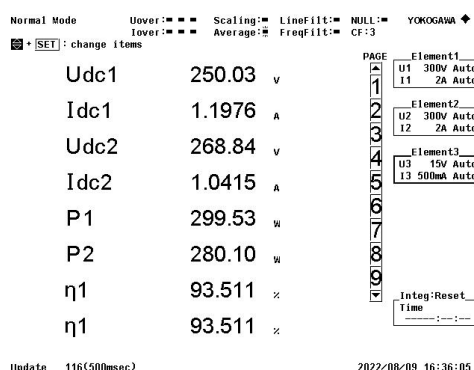


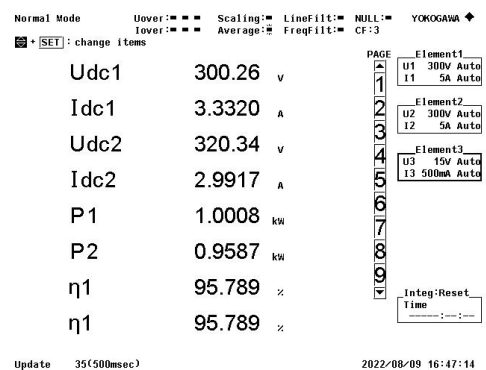
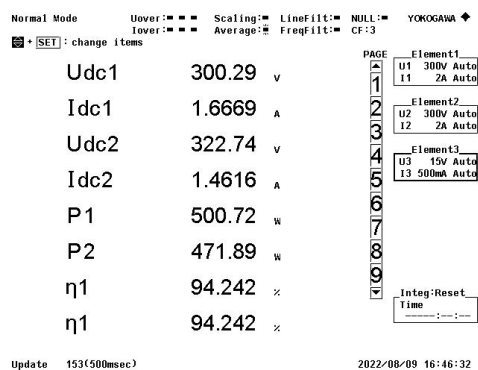
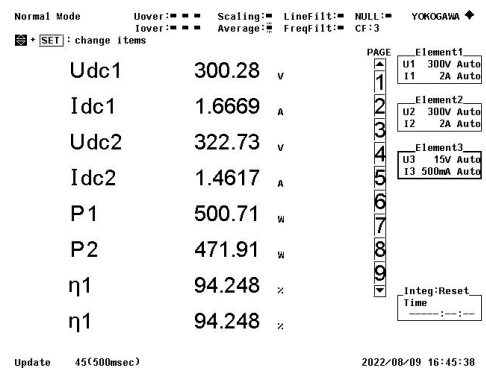
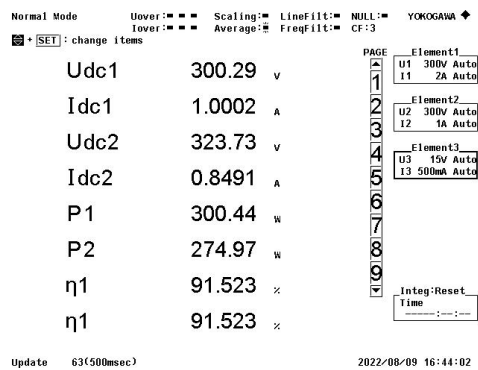
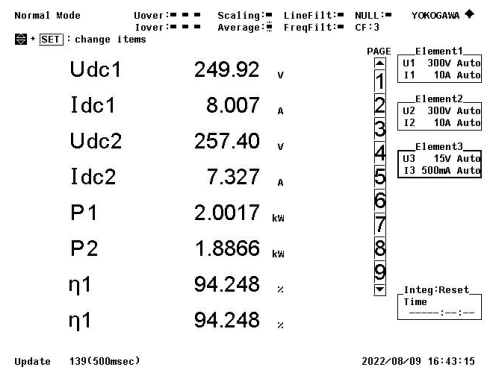
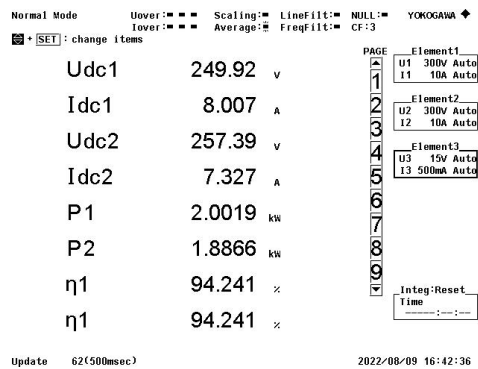
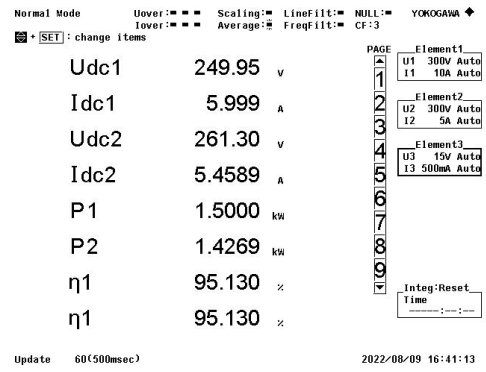
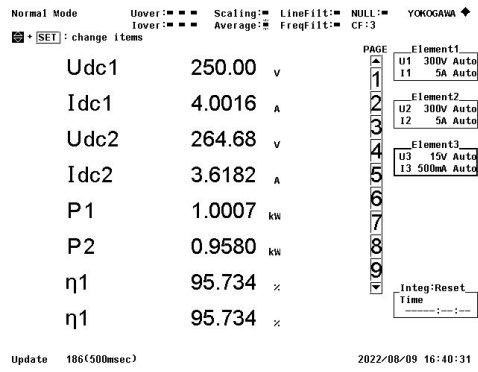


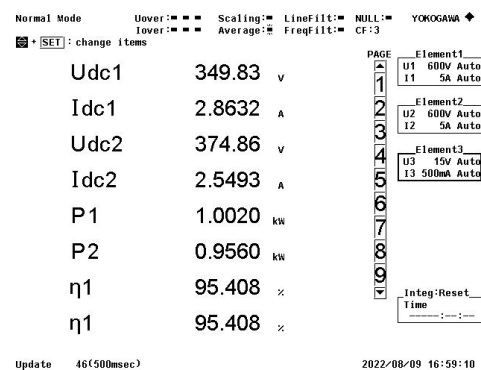
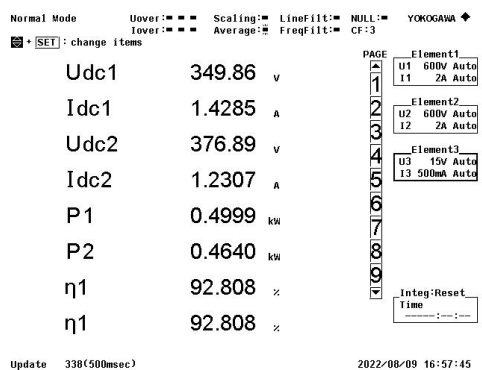
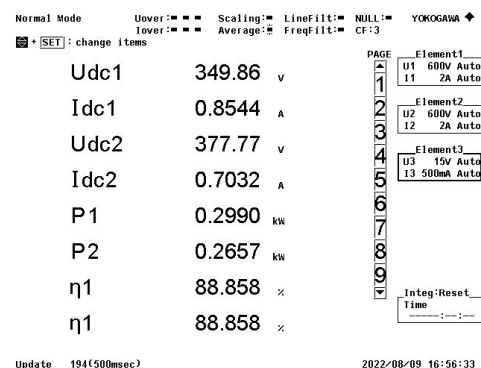
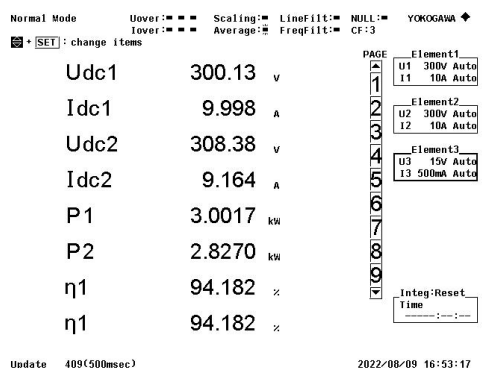
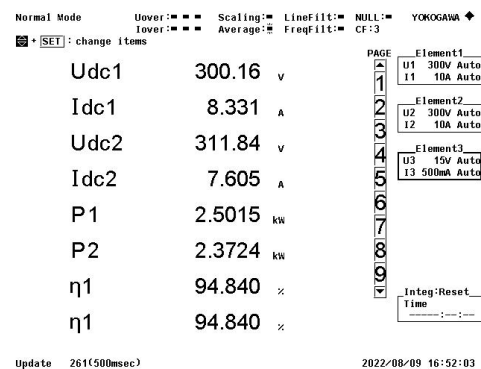
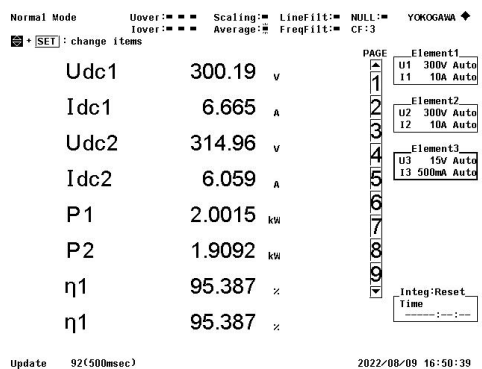
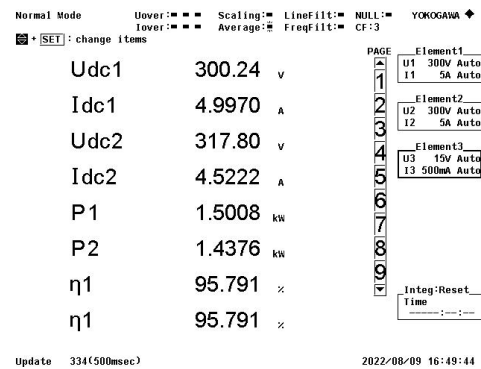
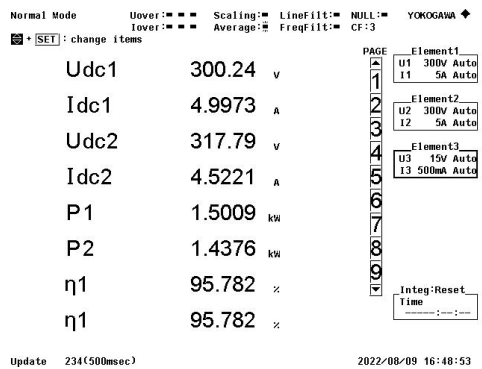


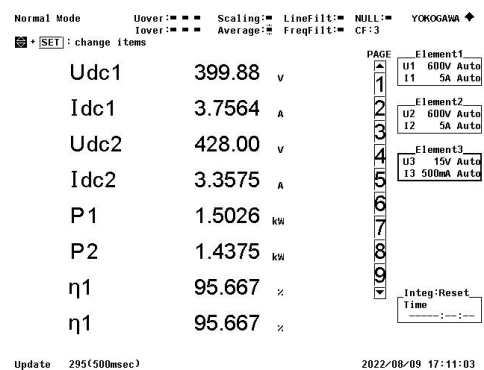
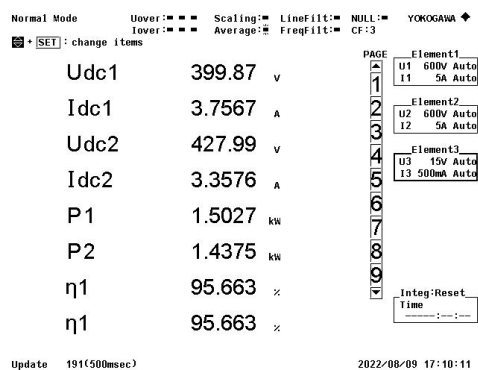
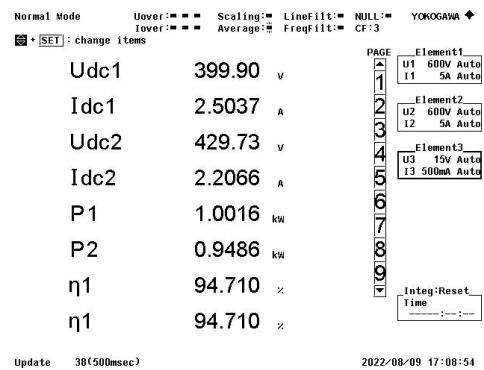
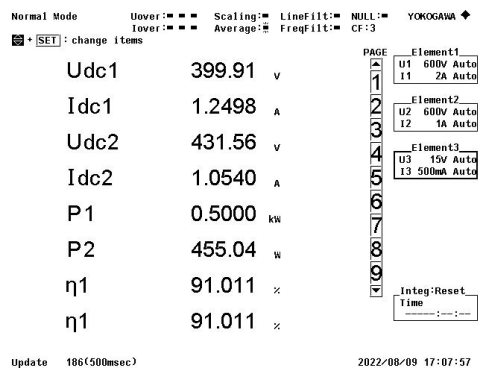
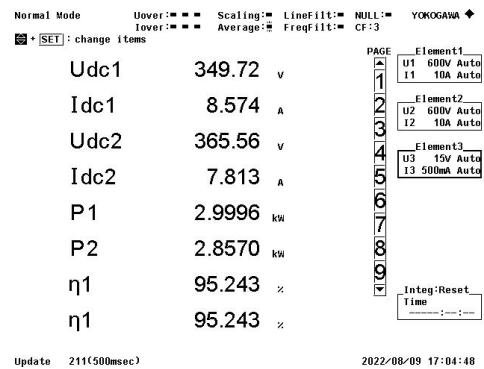
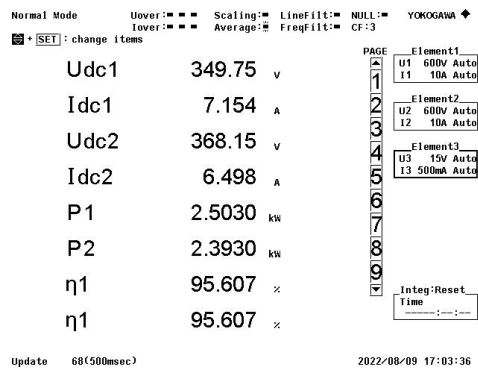
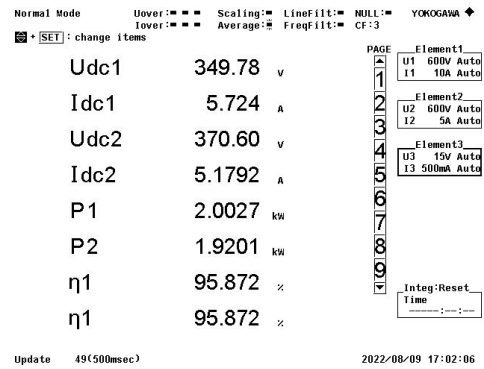
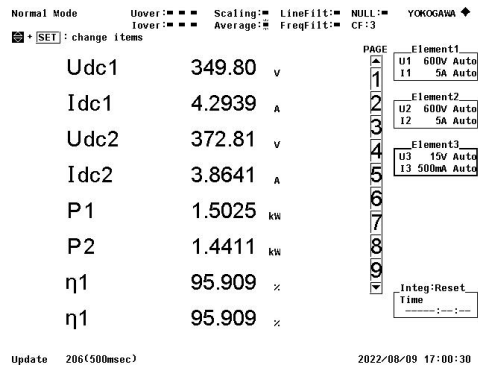
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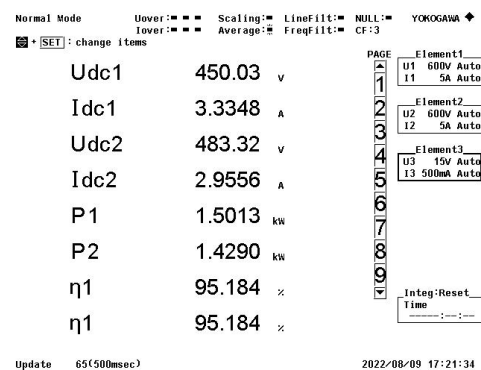
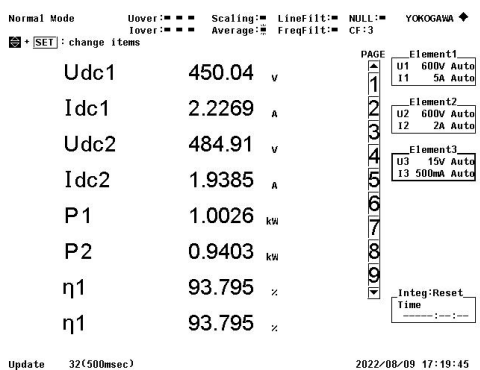
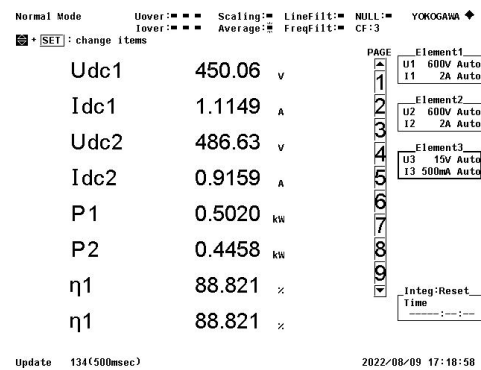
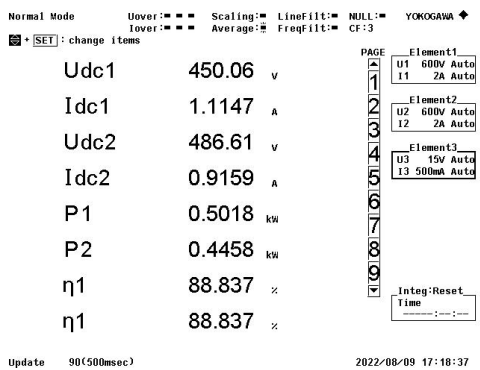
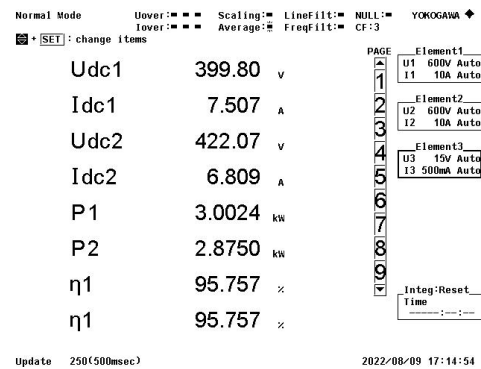
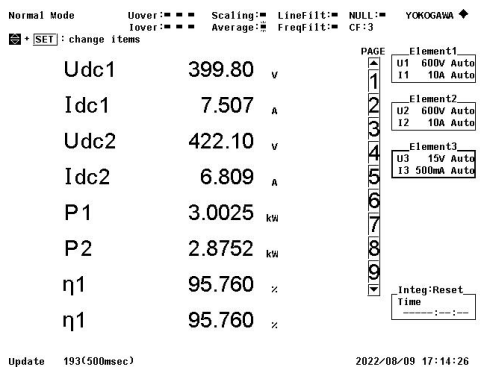
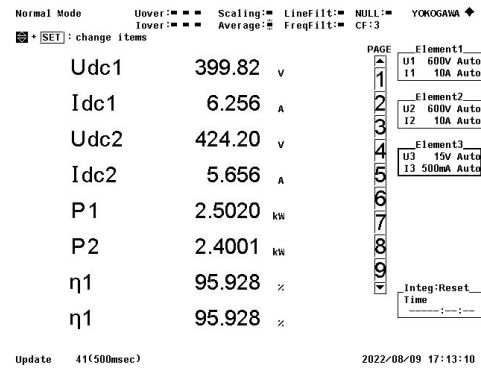
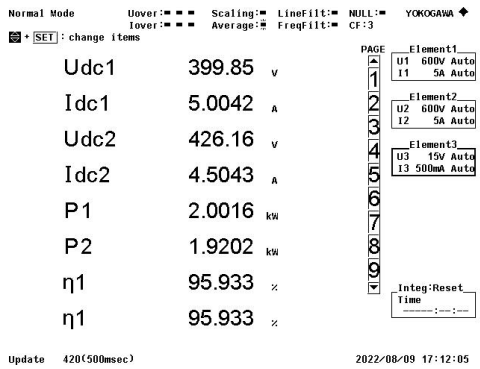
Appendix B: Efficiency of LCC-S compensation topology before tuning (M=106 μ H)

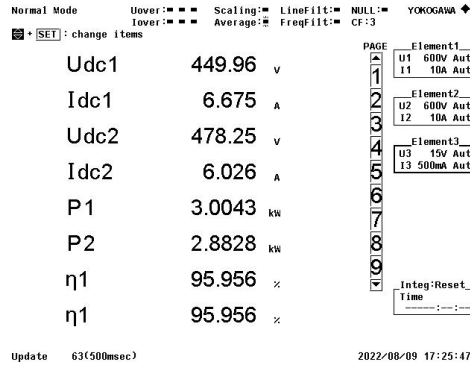
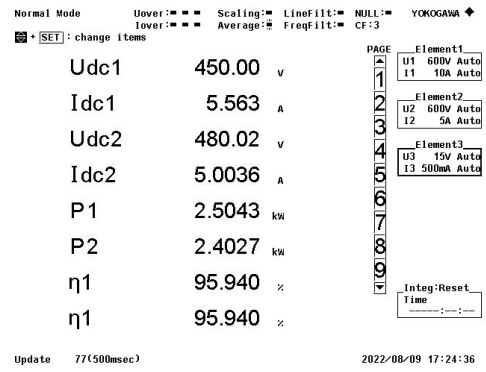
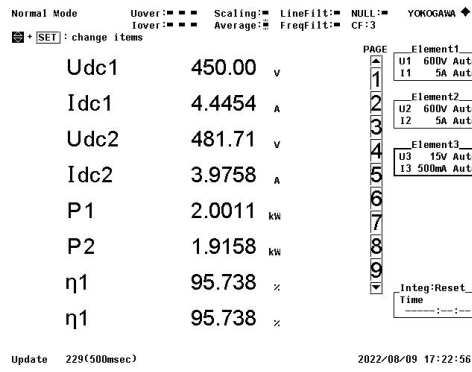






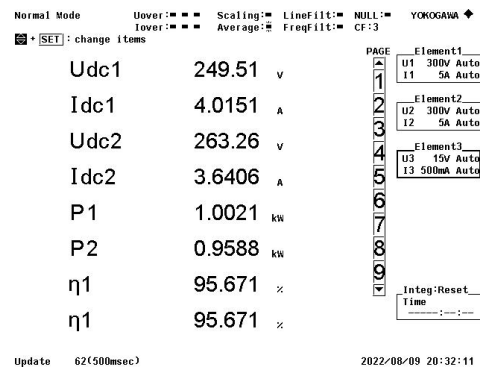
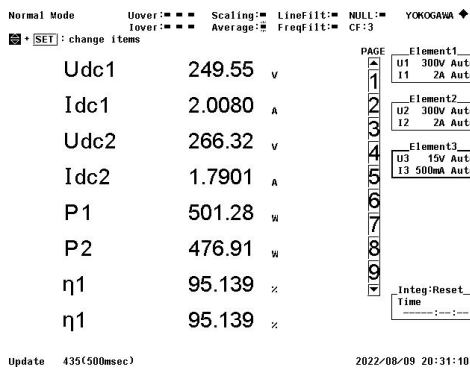
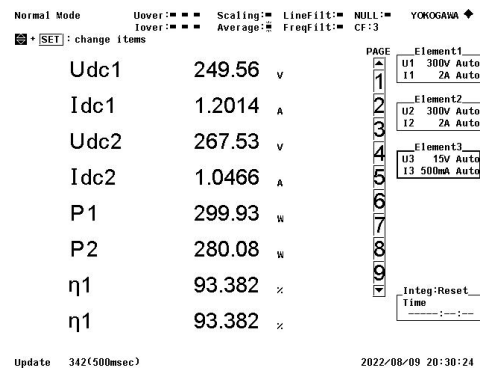
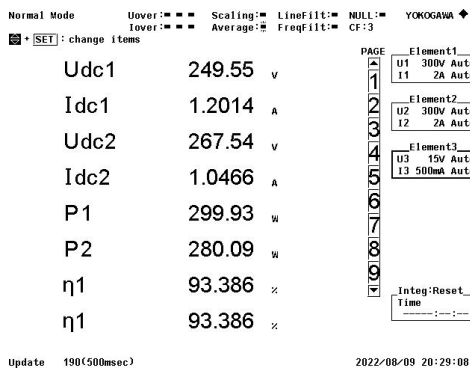


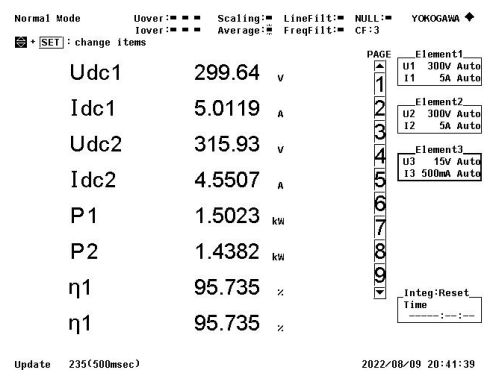
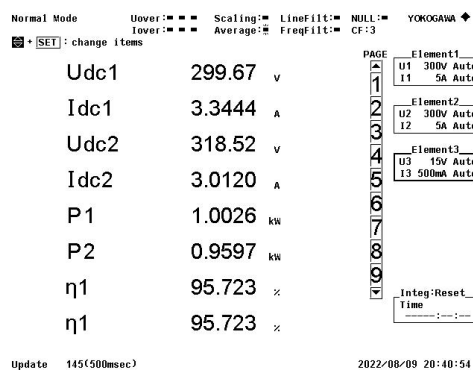
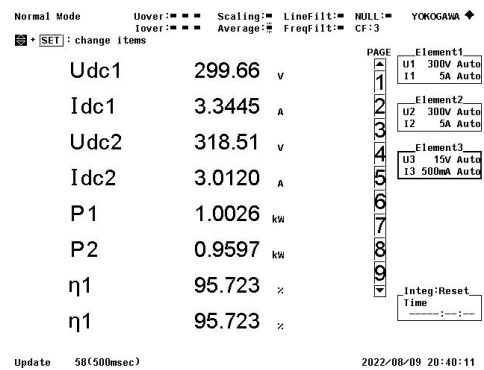
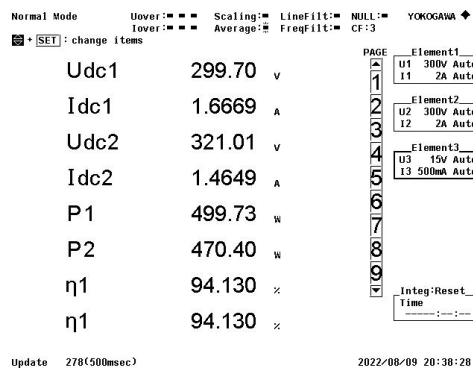
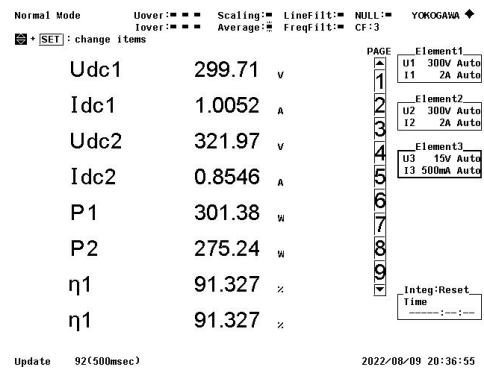
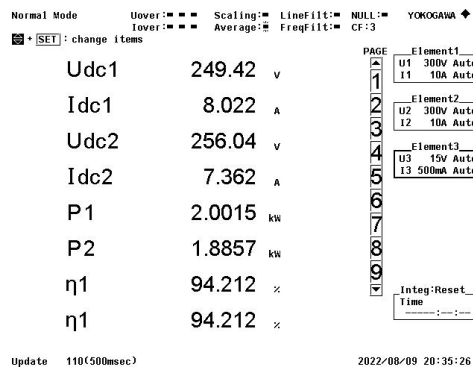
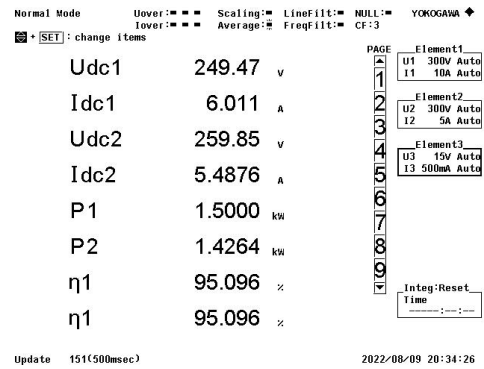
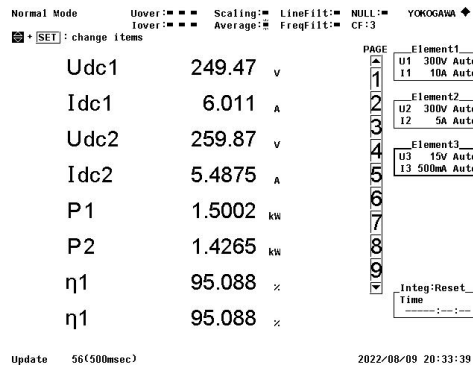


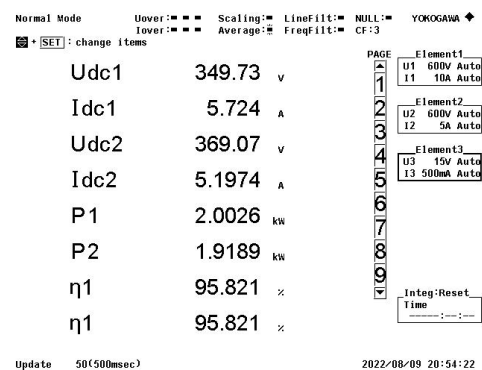
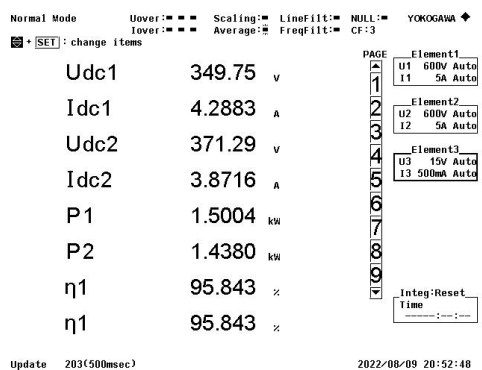
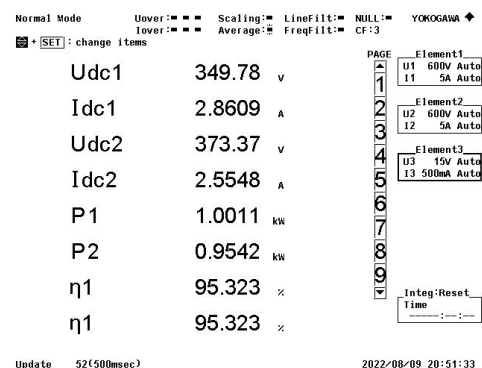
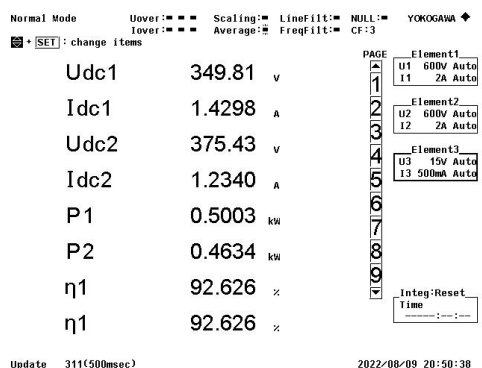
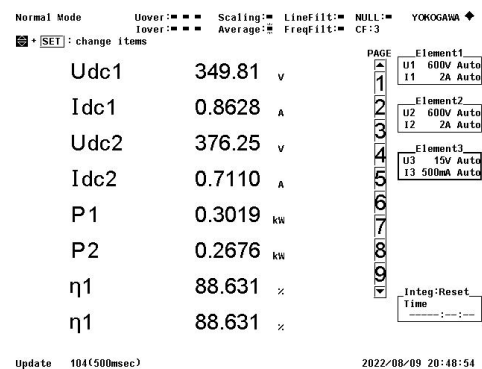
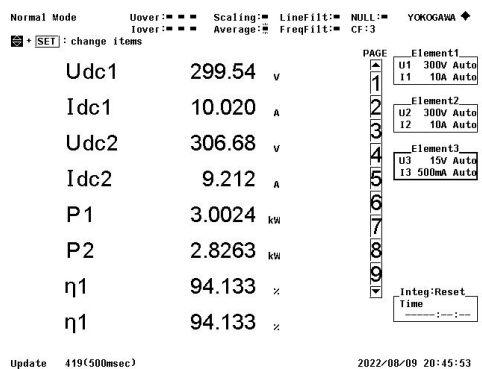
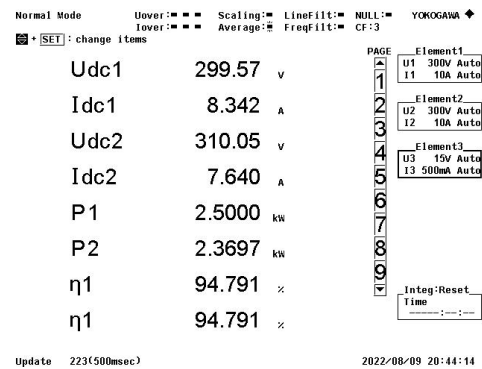
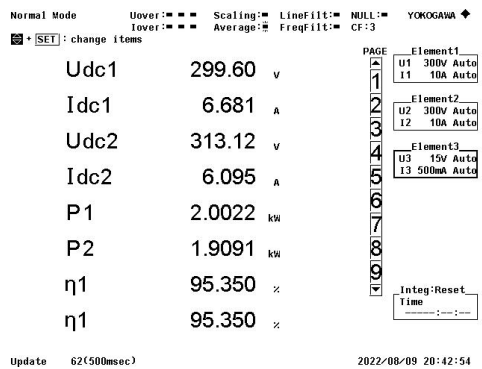


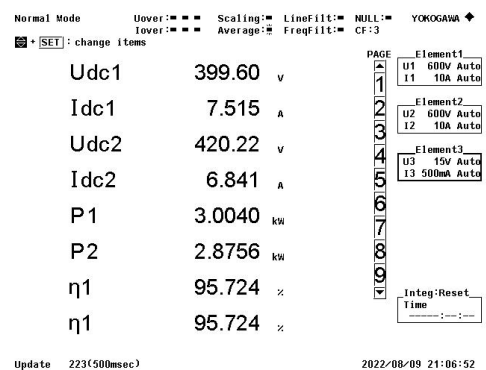
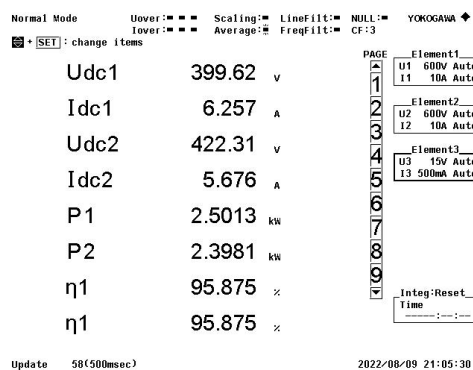
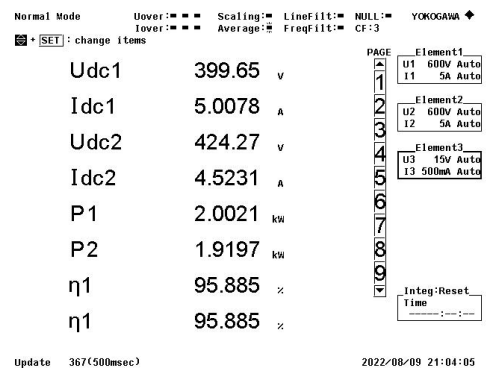
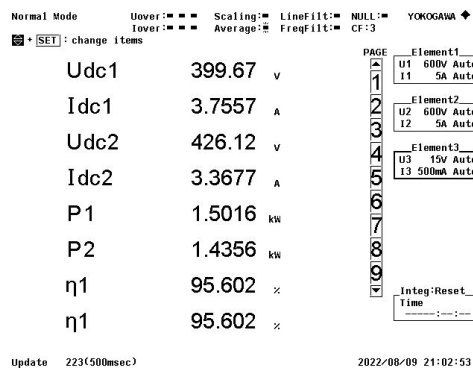
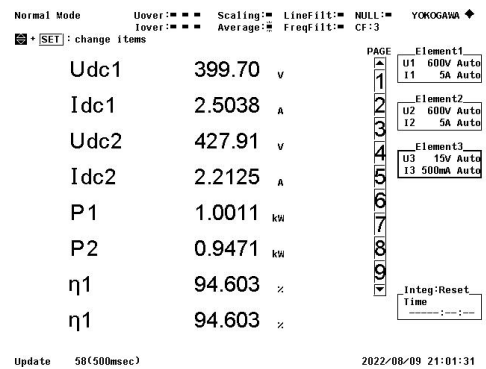
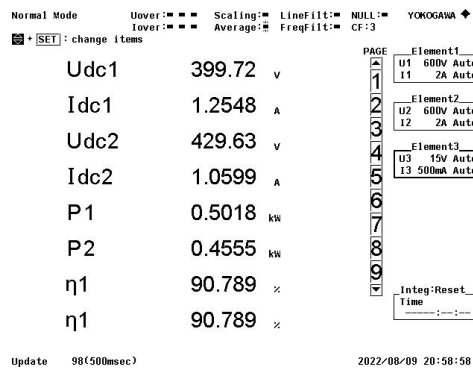
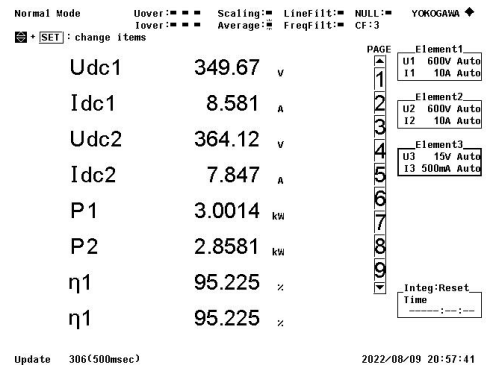
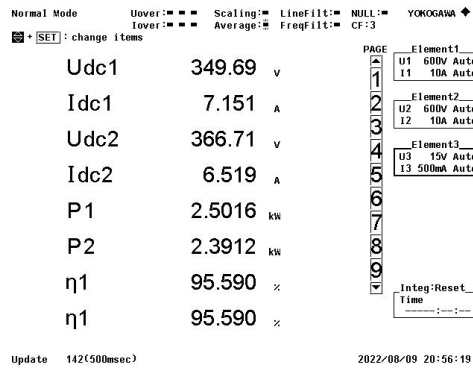
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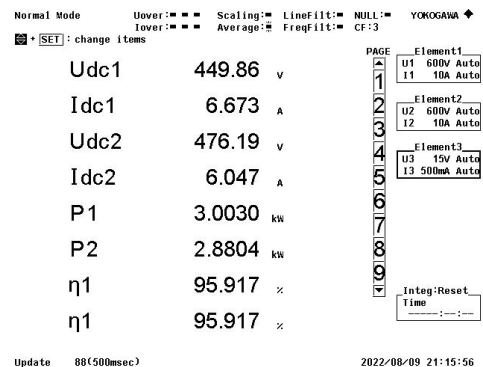
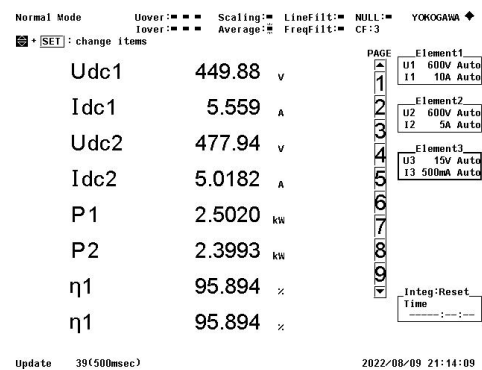
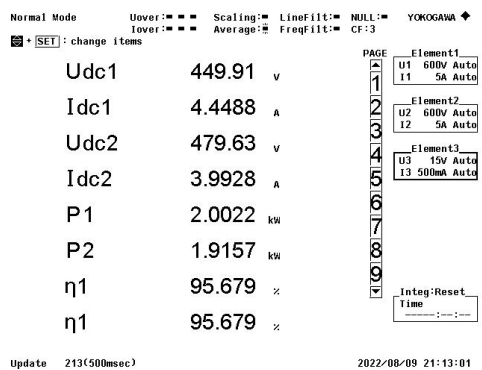
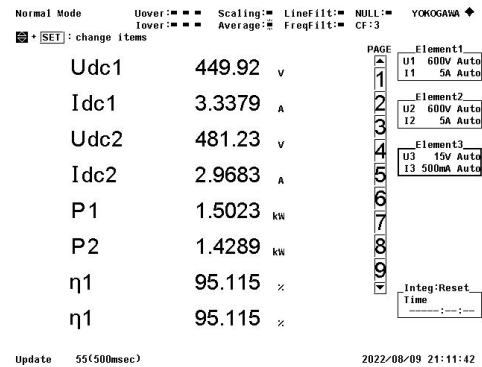
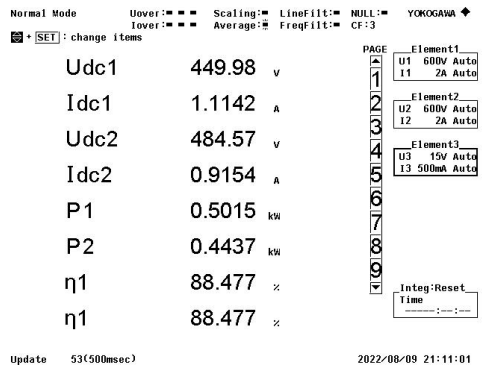
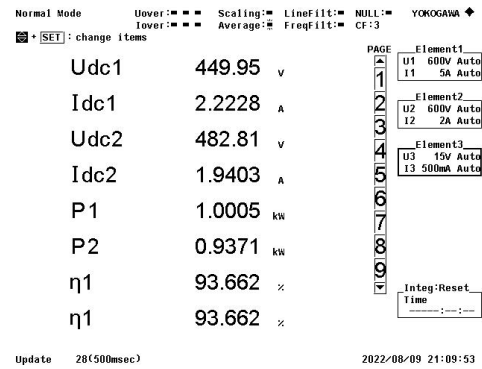
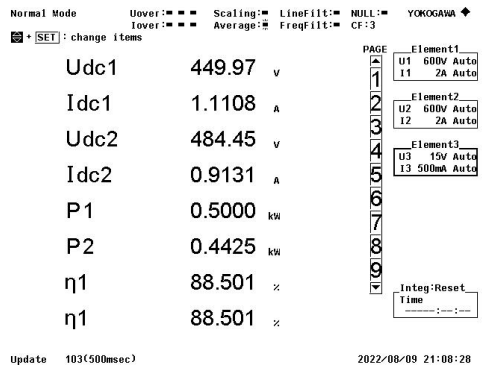
Appendix C: Efficiency of LCC-S compensation topology after tuning (M=106 μ H)

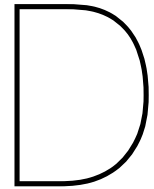




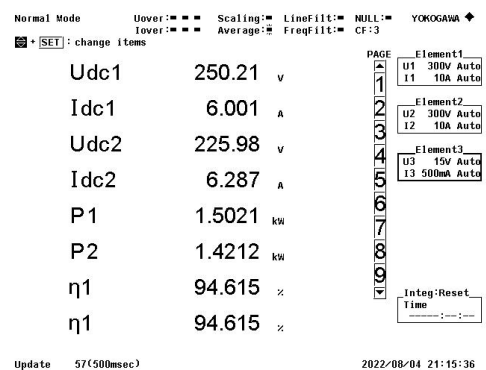
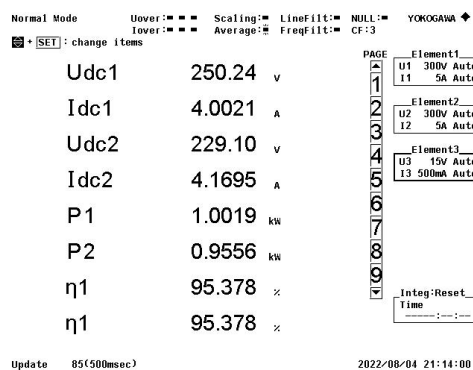
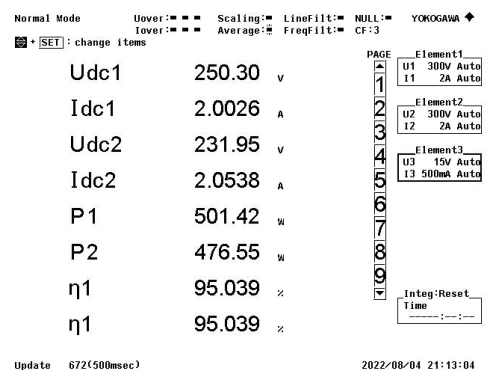
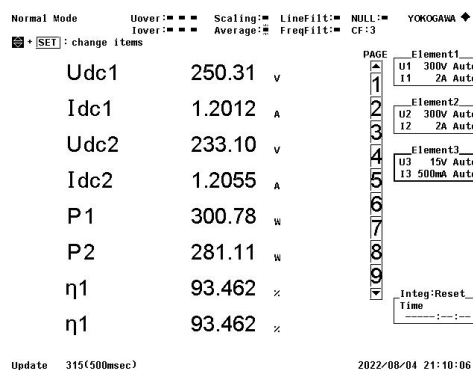


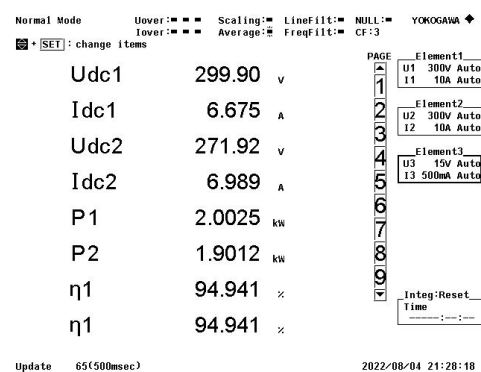
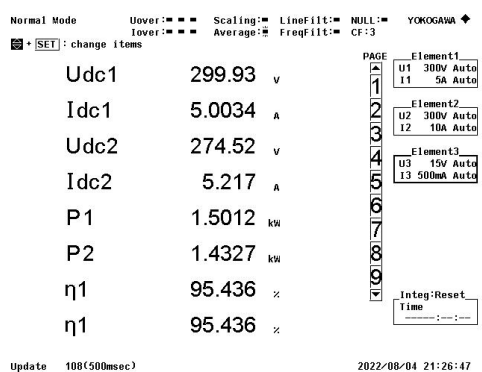
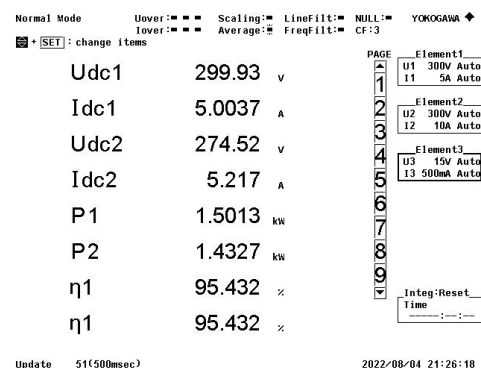
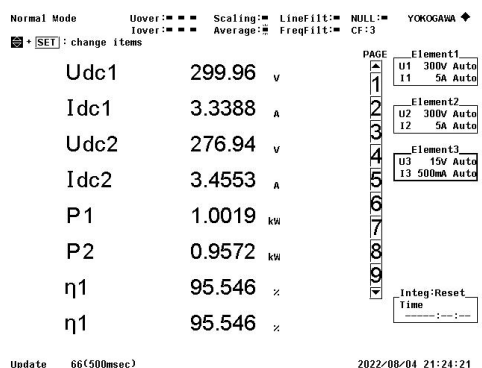
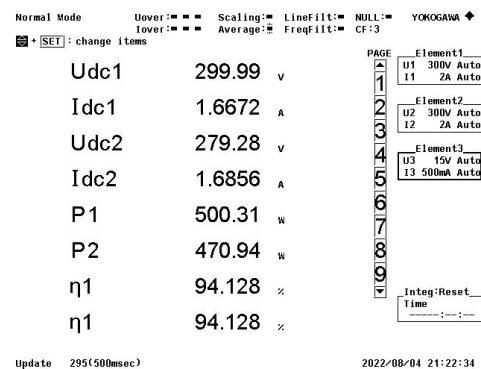
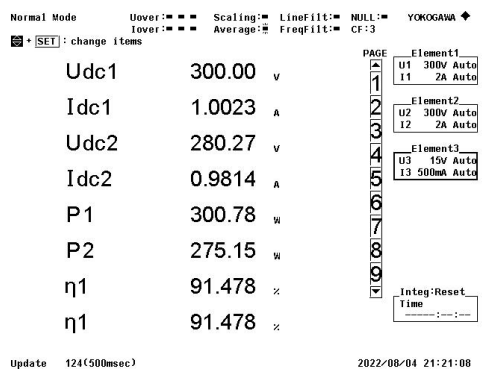
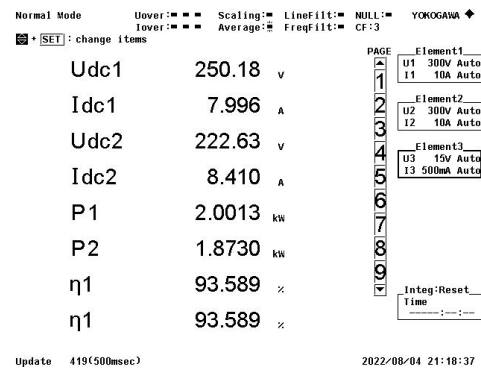
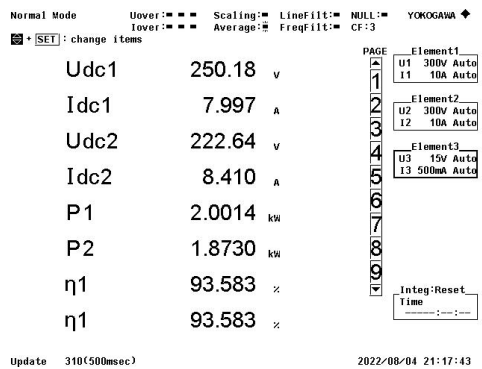


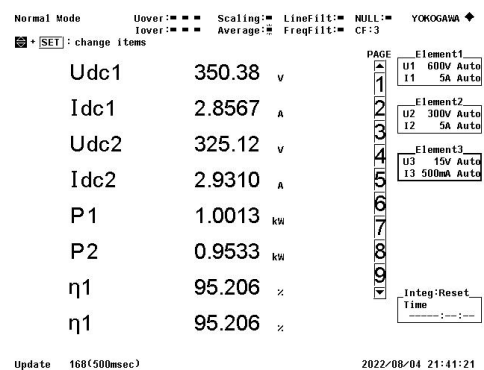
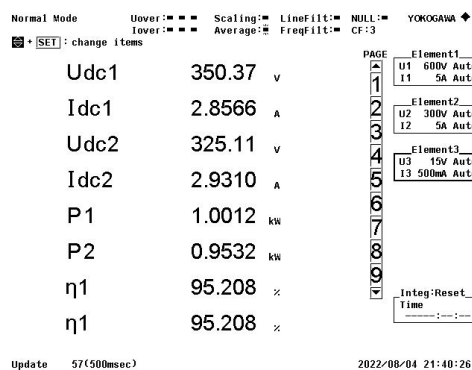
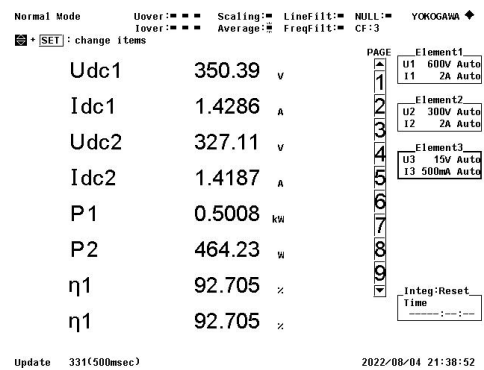
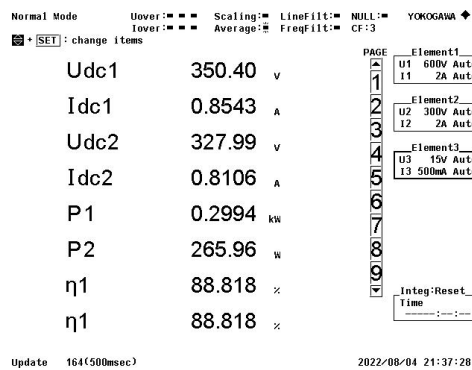
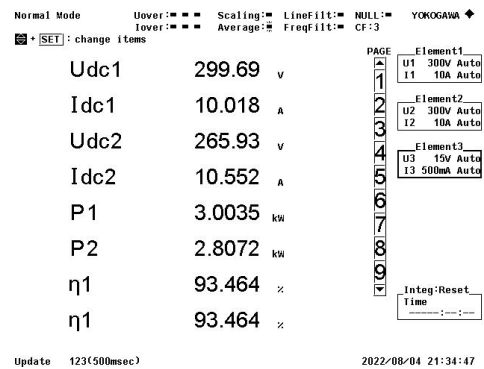
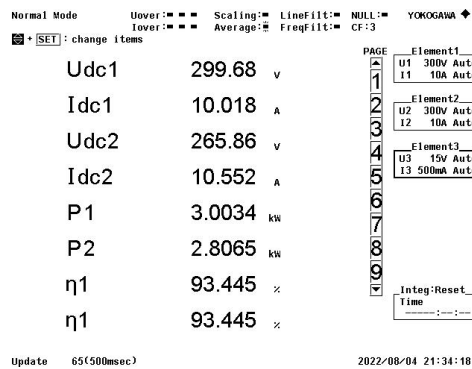
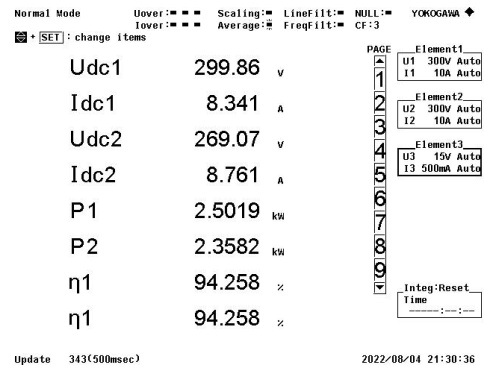
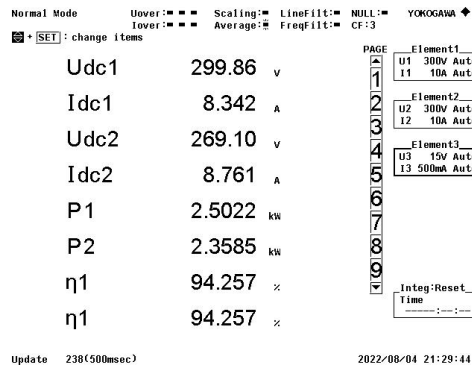


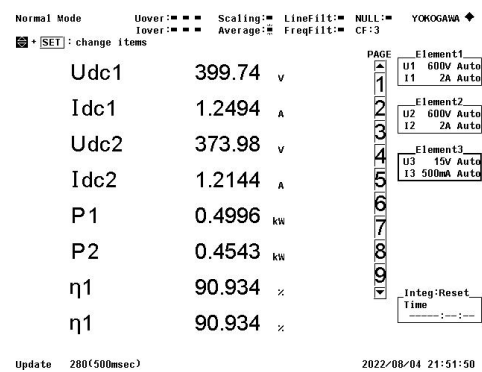
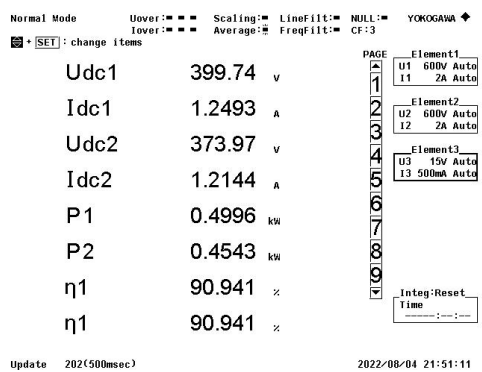
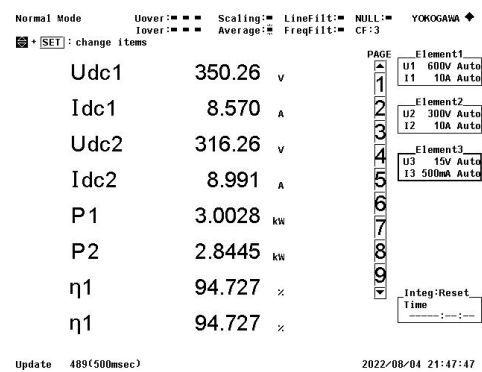
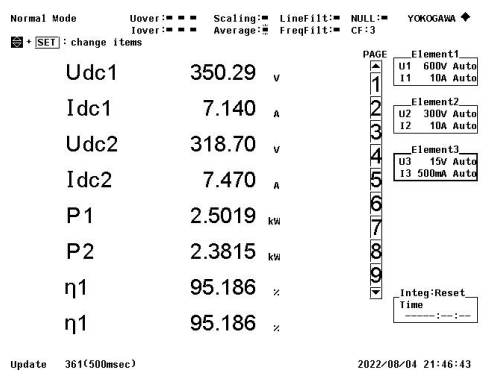
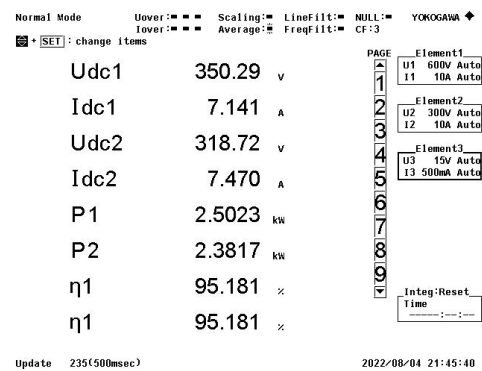
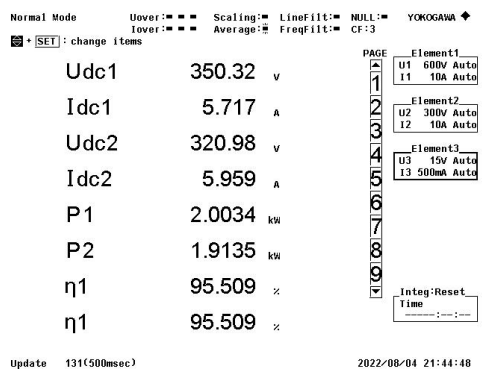
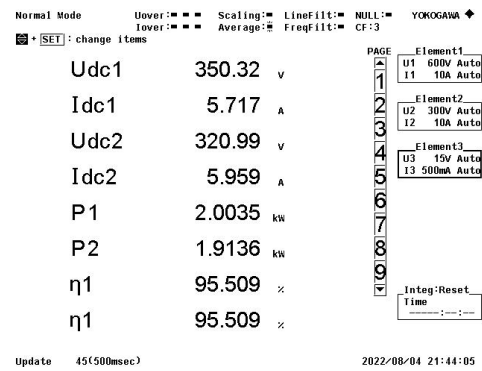
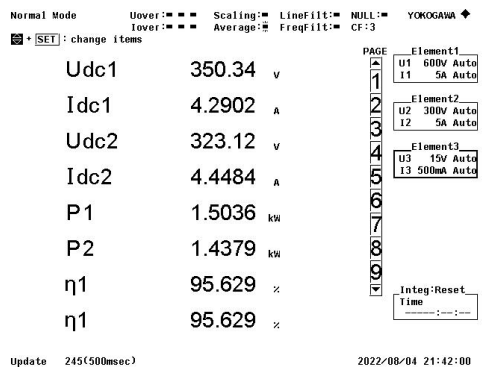


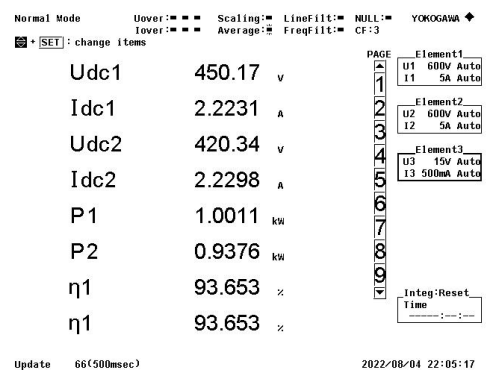
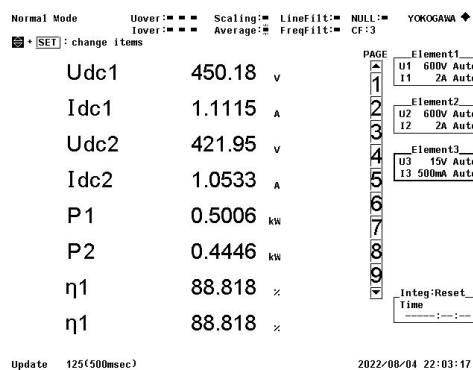
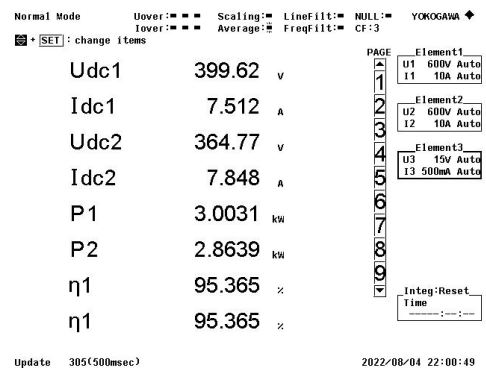
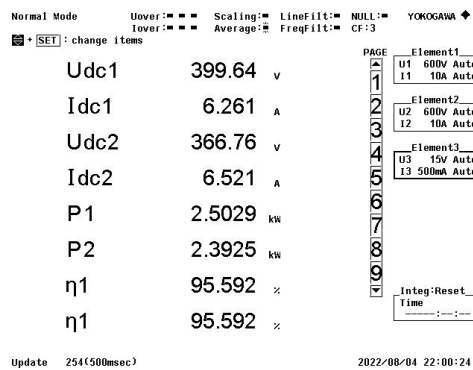
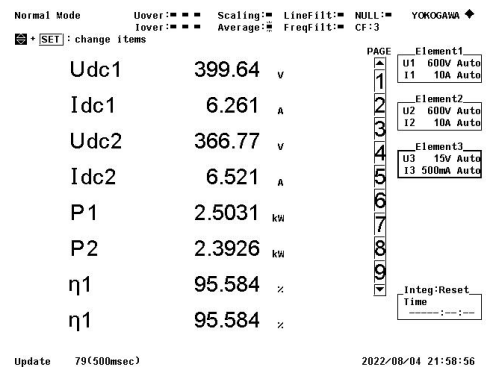
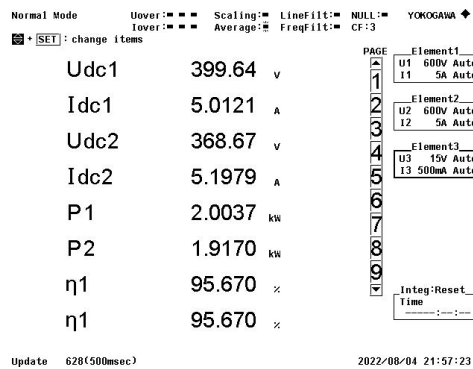
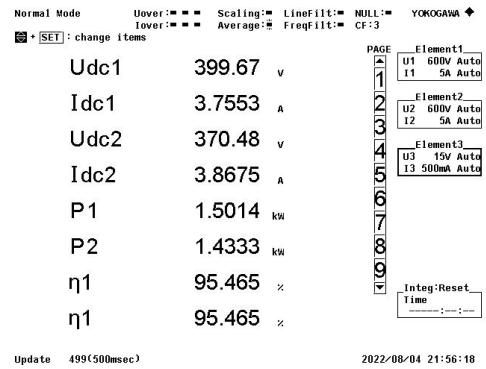
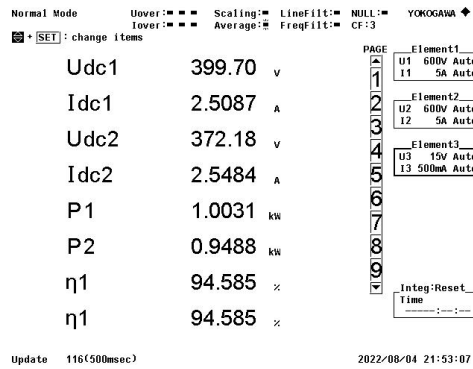
Appendix D: Efficiency of LCC-S compensation topology before tuning (M=91 μ H)











Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	450.14	V
Idc1	3.3342	A
Udc2	418.82	V
Idc2	3.4046	A
P1	1.5014	kW
P2	1.4264	kW
η1	95.009	%
η1	95.009	%

Update 264(500msec) 2022/08/04 22:06:56

PAGE 1
Element1
U1 600V Auto
I1 5A Auto
Element2
U2 600V Auto
I2 5A Auto
Element3
U3 15V Auto
I3 500mA Auto
Integ:Reset
Time

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	450.12	V
Idc1	4.4449	A
Udc2	417.25	V
Idc2	4.5797	A
P1	2.0014	kW
P2	1.9116	kW
η1	95.510	%
η1	95.510	%

Update 450(500msec) 2022/08/04 22:08:29

PAGE 1
Element1
U1 600V Auto
I1 5A Auto
Element2
U2 600V Auto
I2 5A Auto
Element3
U3 15V Auto
I3 500mA Auto
Integ:Reset
Time

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	450.10	V
Idc1	5.557	A
Udc2	415.63	V
Idc2	5.757	A
P1	2.5023	kW
P2	2.3938	kW
η1	95.665	%
η1	95.665	%

Update 148(500msec) 2022/08/04 22:11:08

PAGE 1
Element1
U1 600V Auto
I1 10A Auto
Element2
U2 600V Auto
I2 10A Auto
Element3
U3 15V Auto
I3 500mA Auto
Integ:Reset
Time

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	450.08	V
Idc1	6.673	A
Udc2	413.93	V
Idc2	6.939	A
P1	3.0045	kW
P2	2.8732	kW
η1	95.628	%
η1	95.628	%

Update 239(500msec) 2022/08/04 22:11:53

PAGE 1
Element1
U1 600V Auto
I1 10A Auto
Element2
U2 600V Auto
I2 10A Auto
Element3
U3 15V Auto
I3 500mA Auto
Integ:Reset
Time

E

Appendix E: Efficiency of LCC-S compensation topology after tuning (M=91 μ H)

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	250.04	V
Idc1	1.2054	A
Udc2	232.67	V
Idc2	1.2086	A
P1	301.50	W
P2	281.30	W
η_1	93.301	%
η_1	93.301	%

Update 124(500msec)

2022/08/05 16:34:14

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	250.04	V
Idc1	2.0076	A
Udc2	231.47	V
Idc2	2.0592	A
P1	502.14	W
P2	476.80	W
η_1	94.952	%
η_1	94.952	%

Update 477(500msec)

2022/08/05 16:37:10

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

■ + [SET] : change items

Udc1	249.99	V
Idc1	4.0063	A
Udc2	228.50	V
Idc2	4.1772	A
P1	1.0019	kW
P2	0.9548	kW
η_1	95.302	%
η_1	95.302	%

Update 70(500msec)

2022/08/05 16:37:58

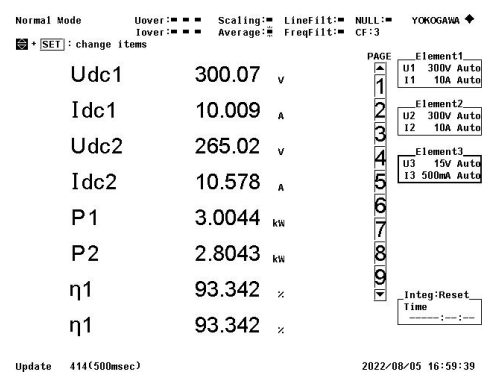
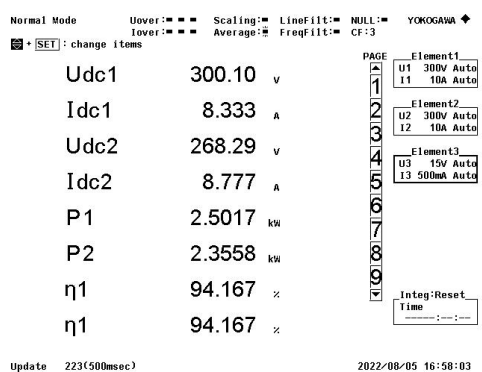
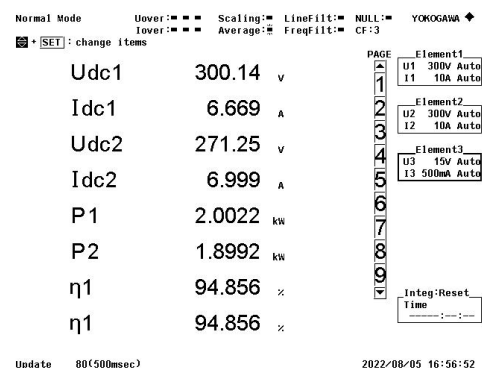
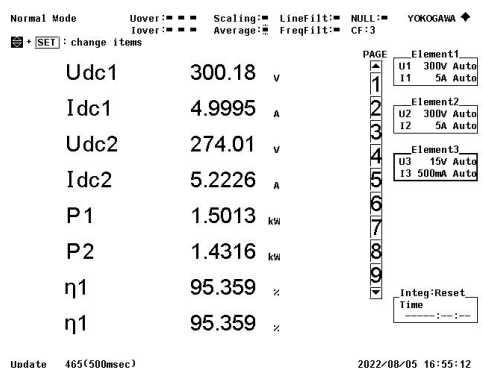
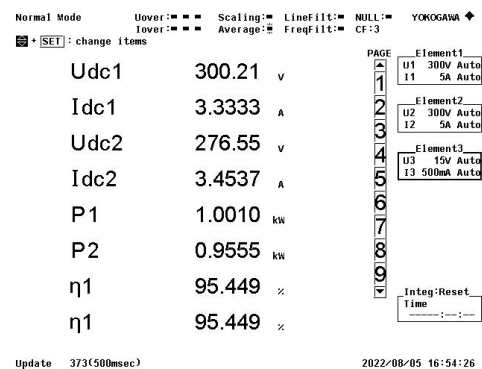
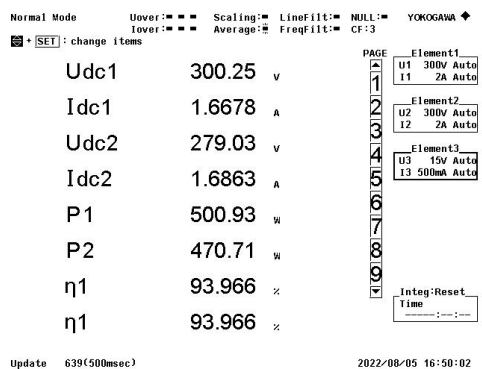
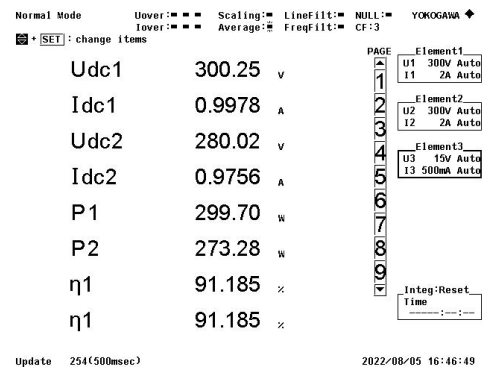
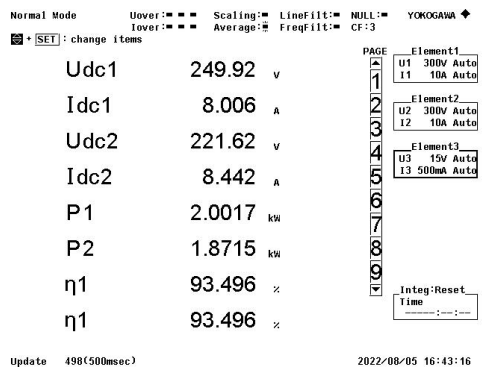
Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF: 3

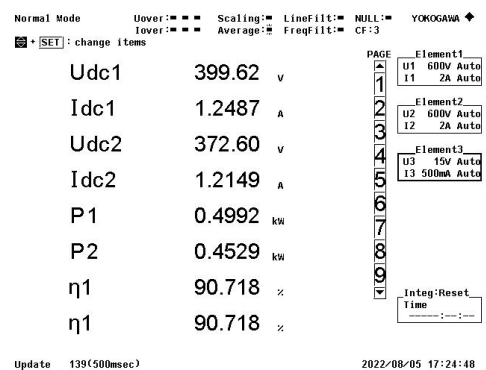
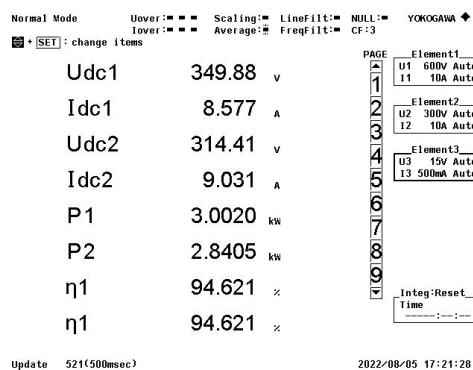
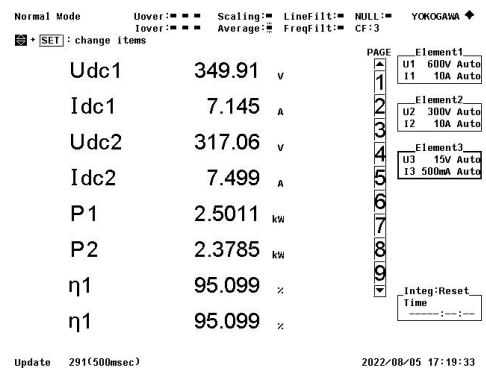
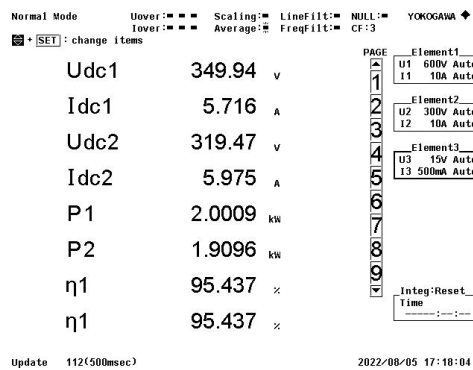
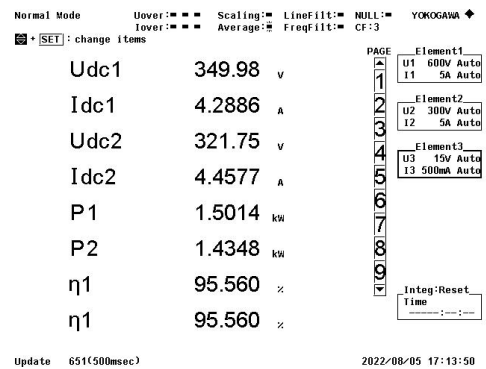
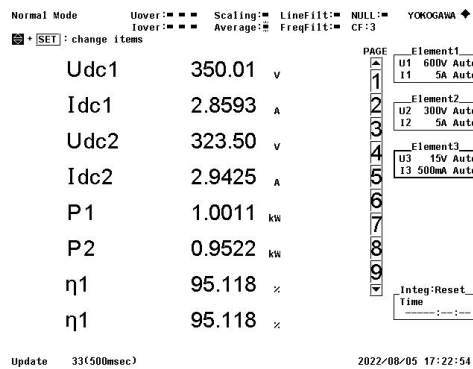
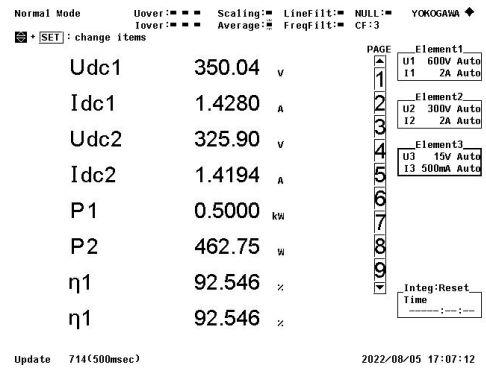
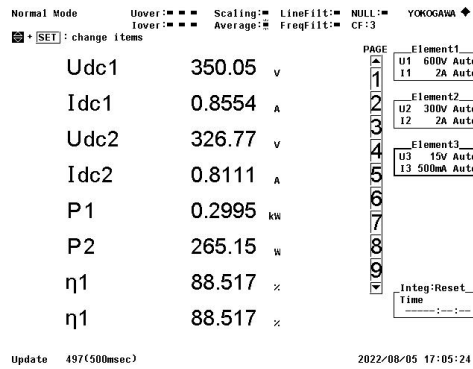
■ + [SET] : change items

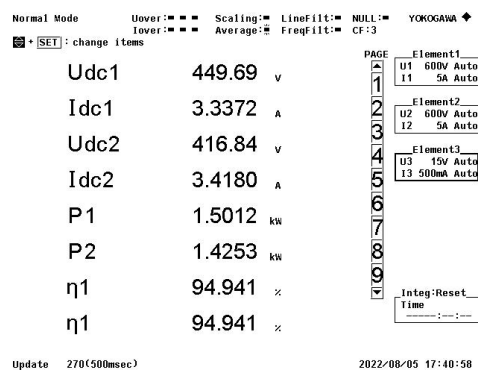
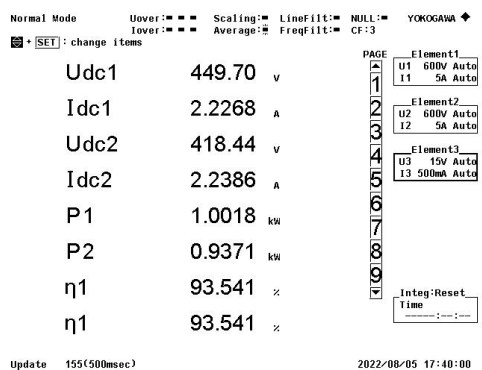
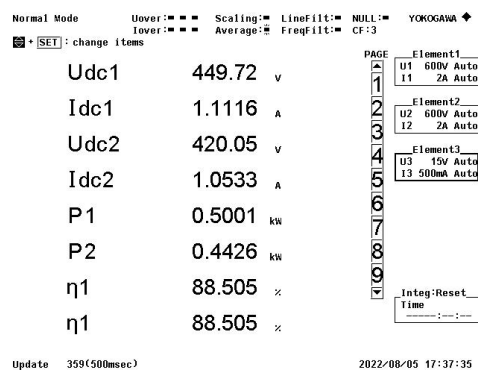
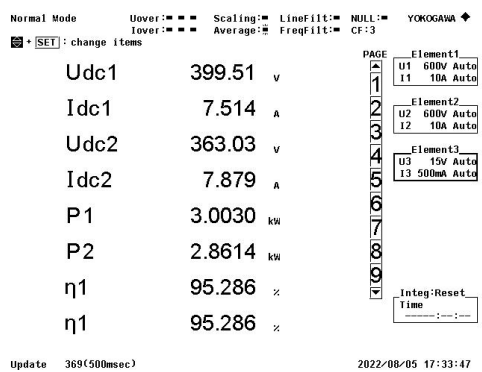
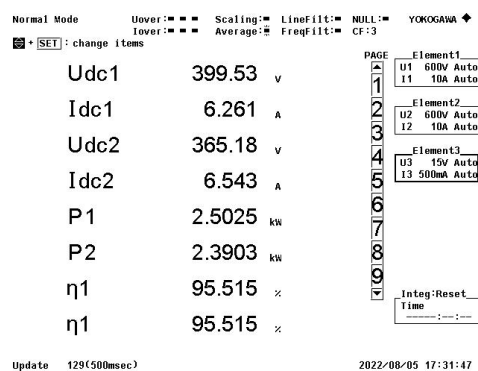
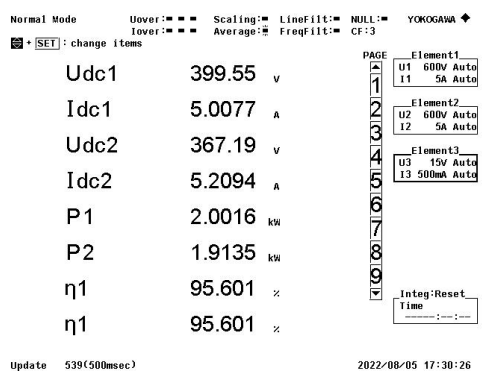
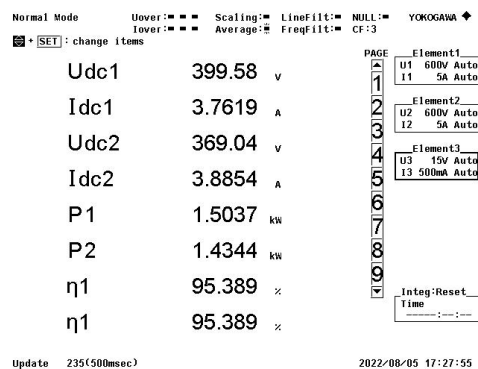
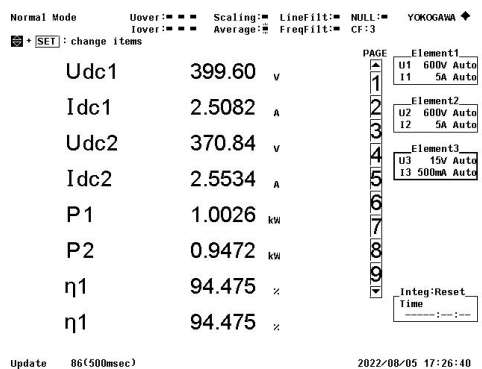
Udc1	249.96	V
Idc1	6.000	A
Udc2	225.21	V
Idc2	6.297	A
P1	1.5004	kW
P2	1.4186	kW
η_1	94.549	%
η_1	94.549	%

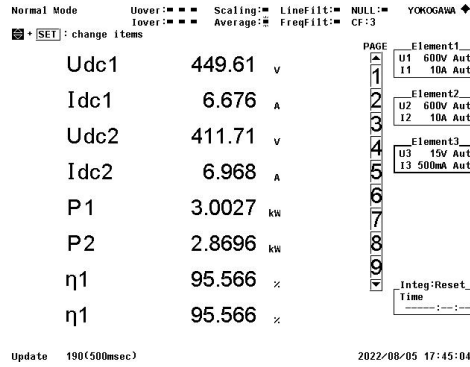
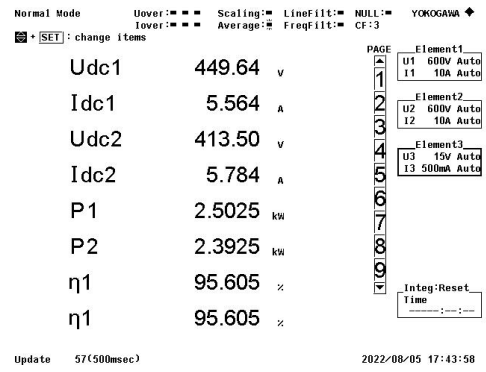
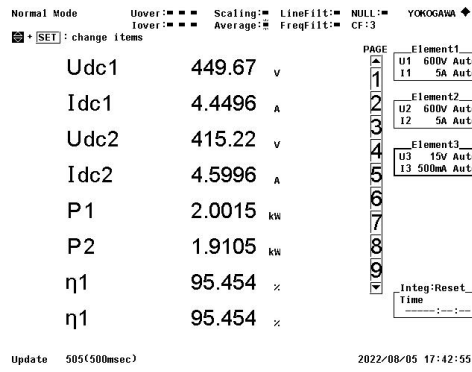
Update 179(500msec)

2022/08/05 16:40:36



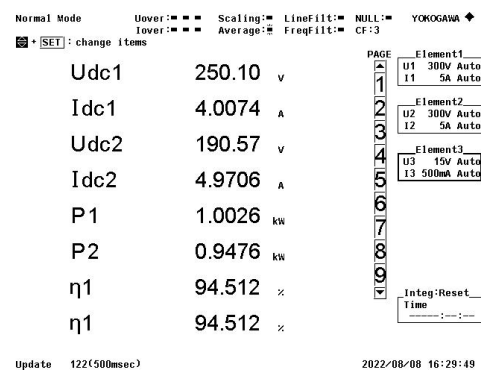
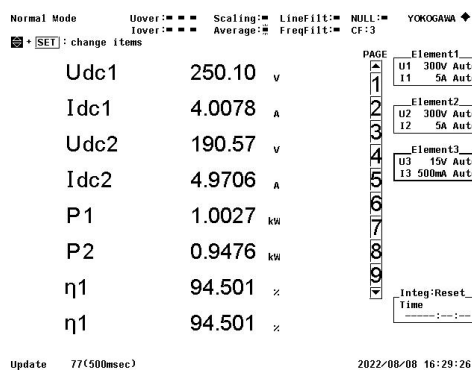
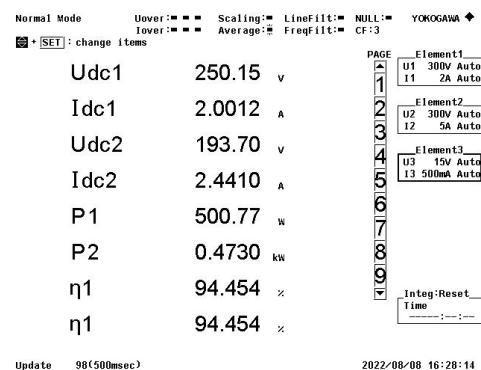
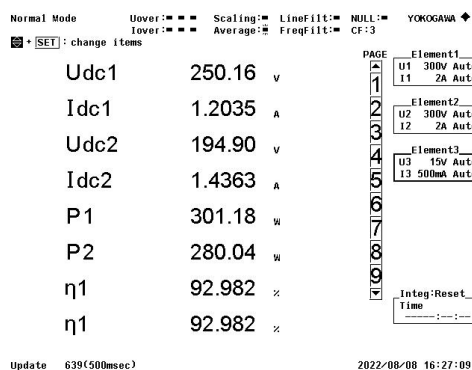


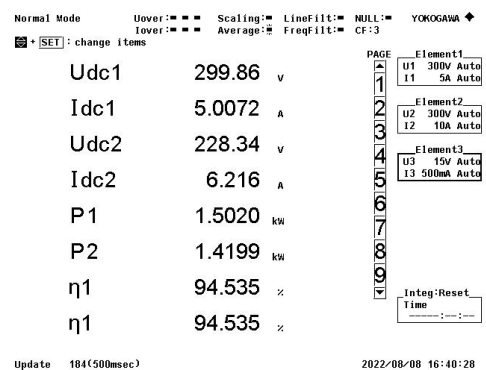
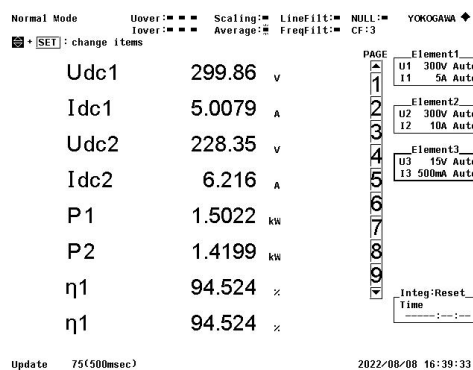
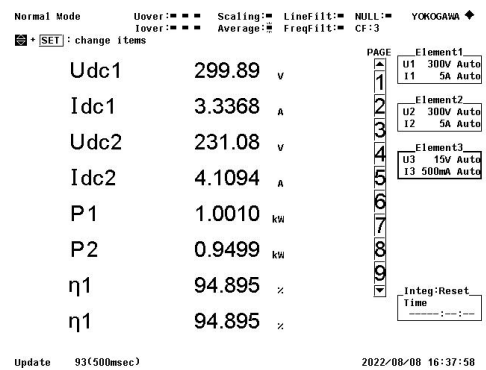
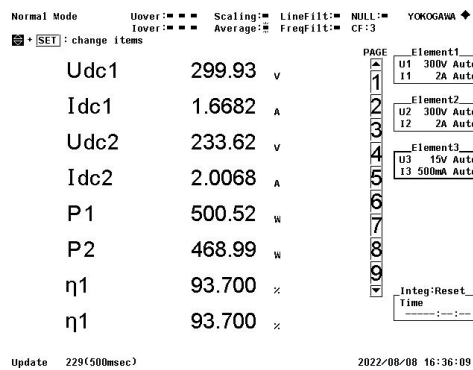
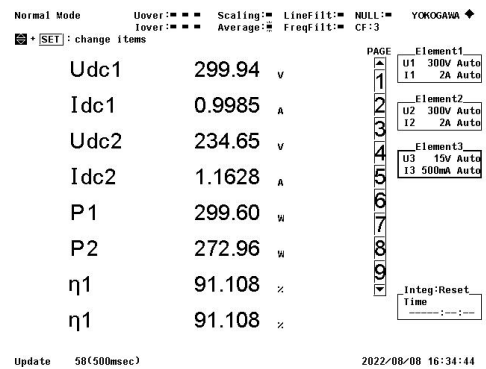
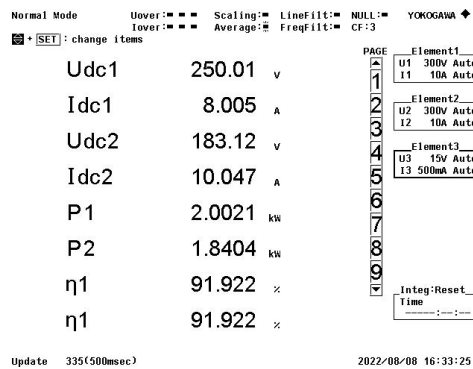
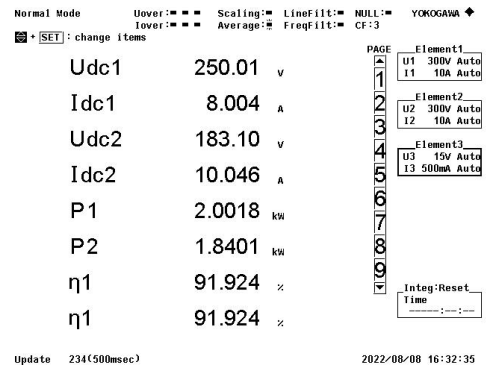
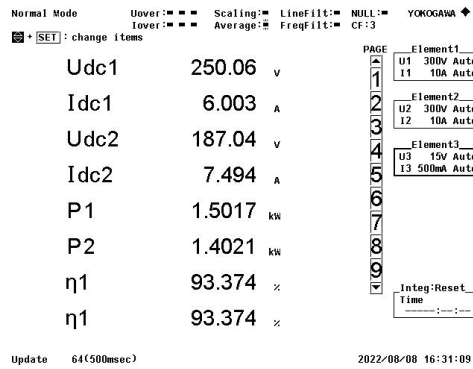


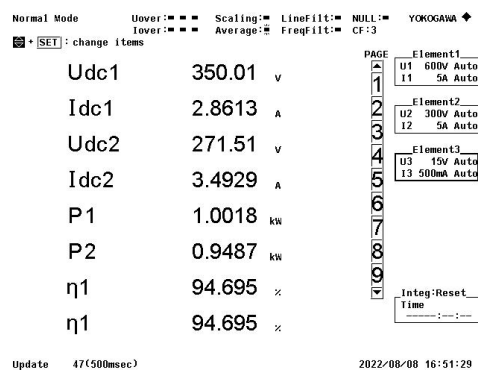
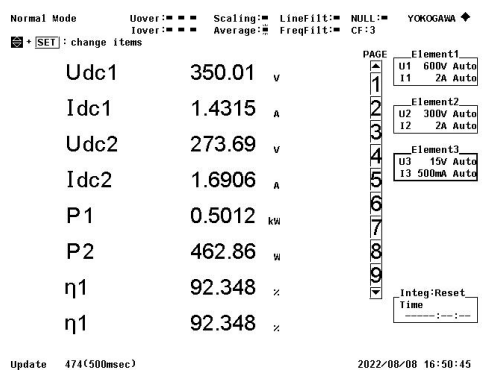
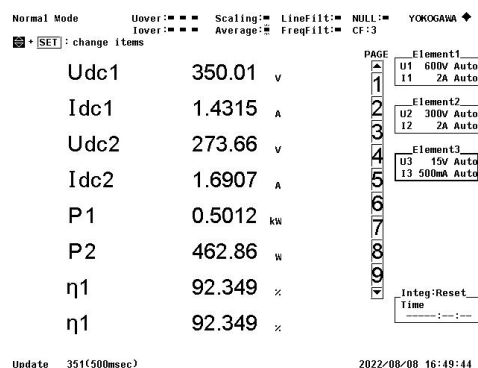
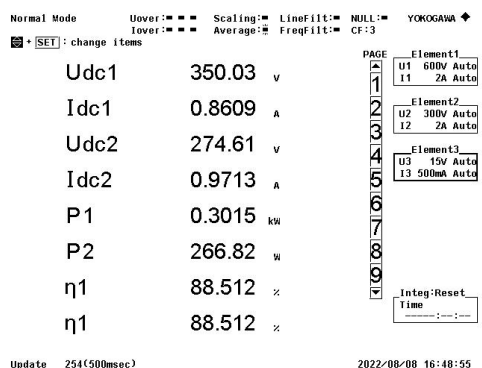
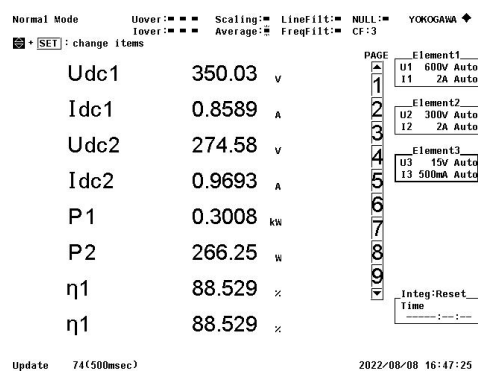
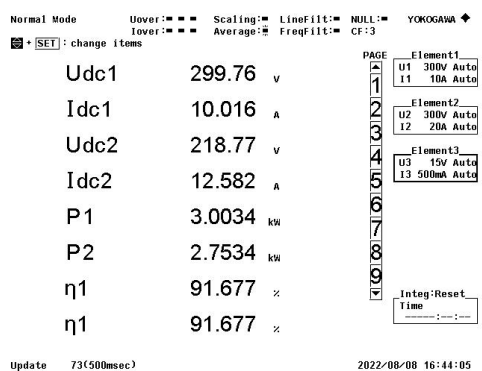
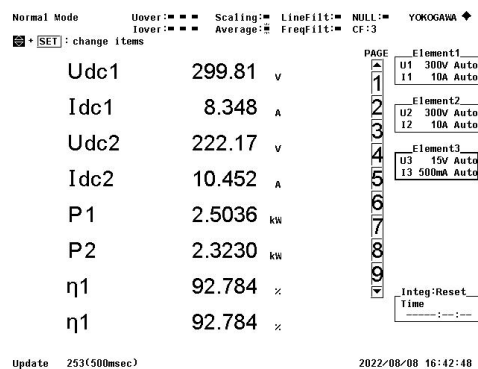
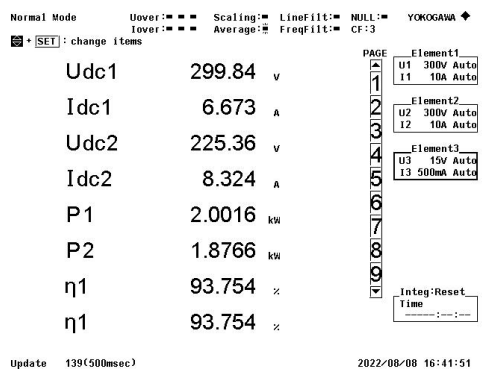


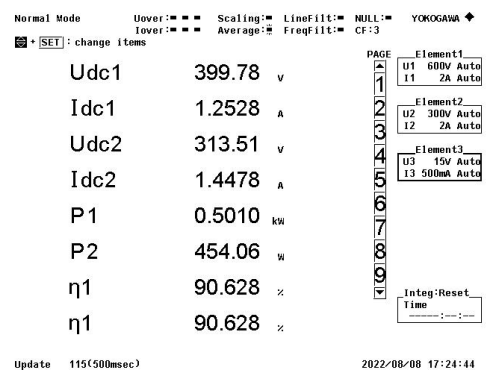
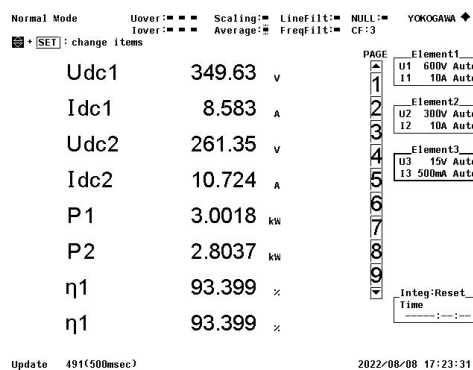
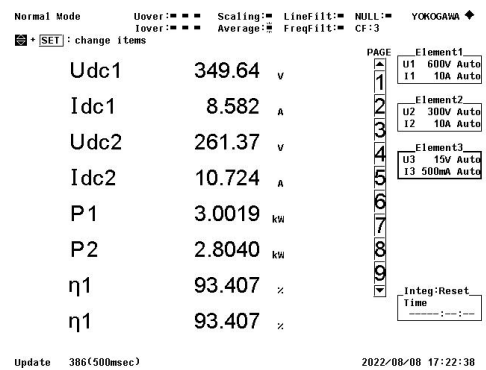
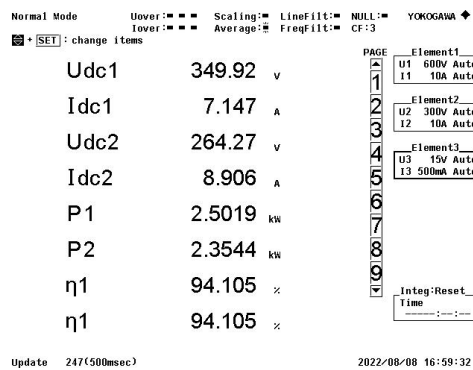
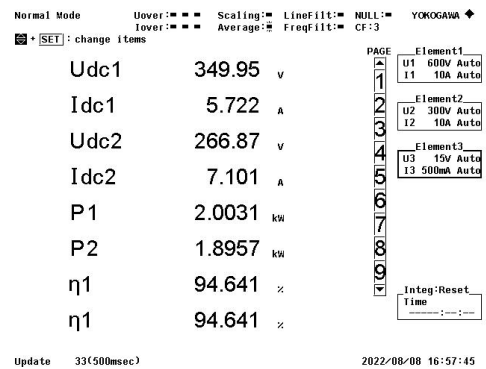
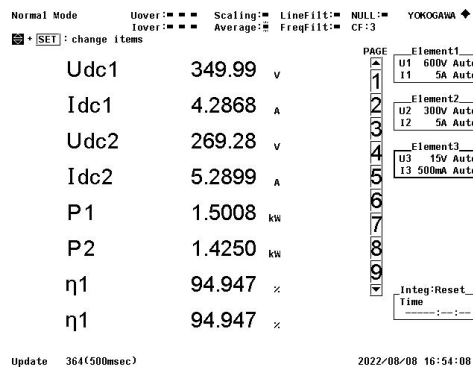
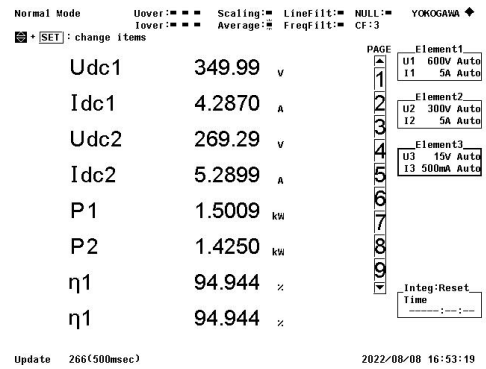
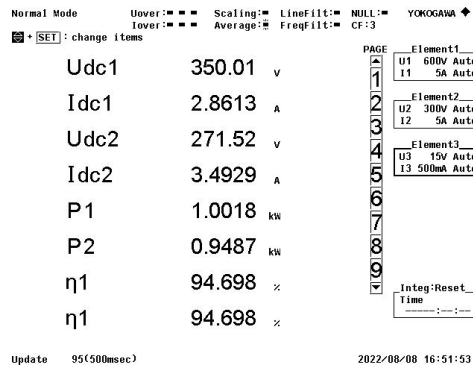
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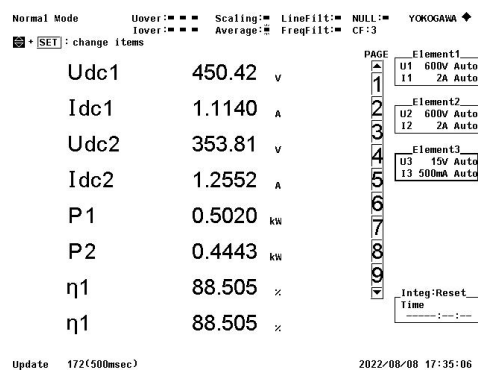
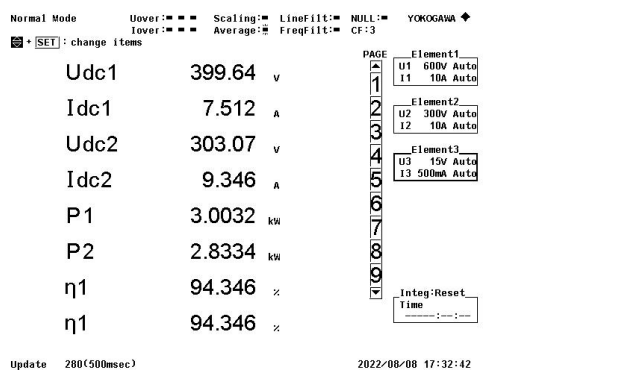
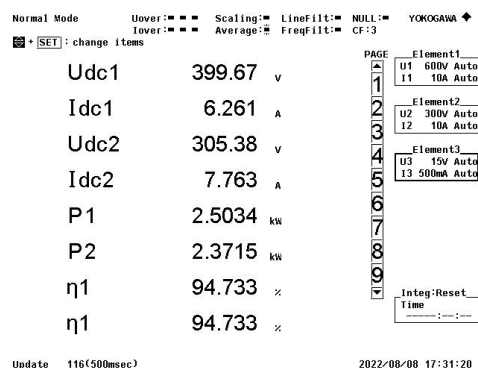
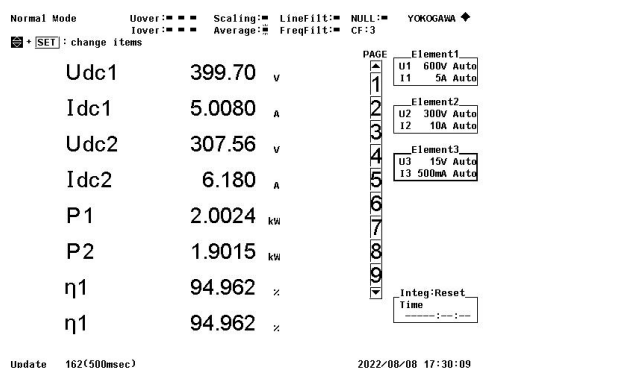
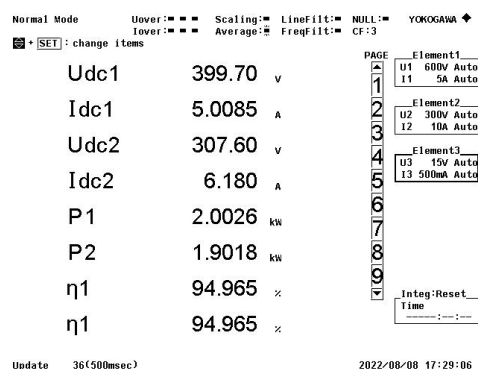
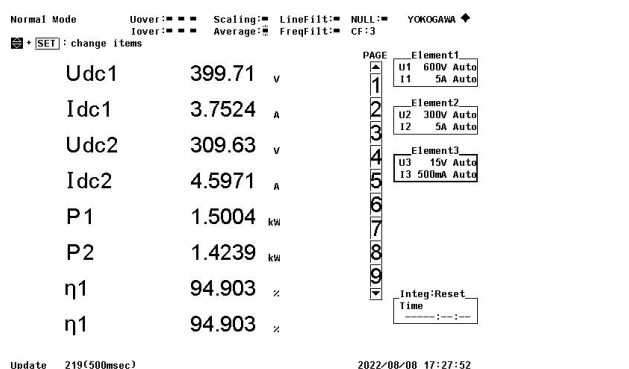
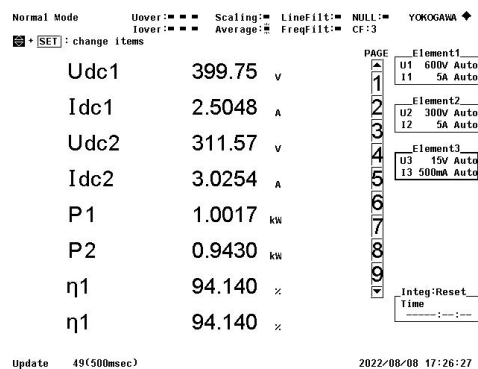
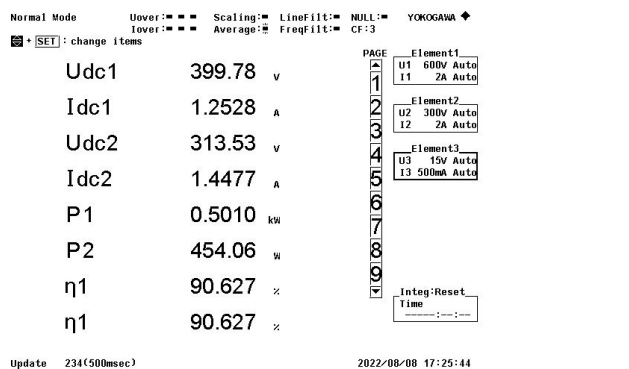
Appendix F: Efficiency of LCC-S compensation topology before tuning (M=76 μ H)

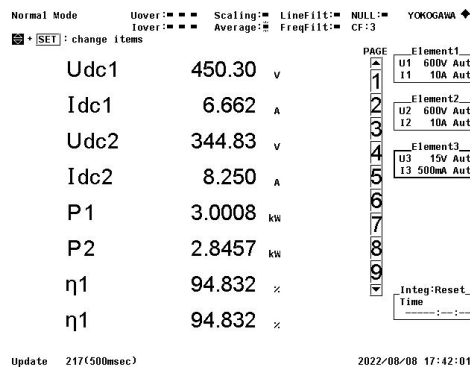
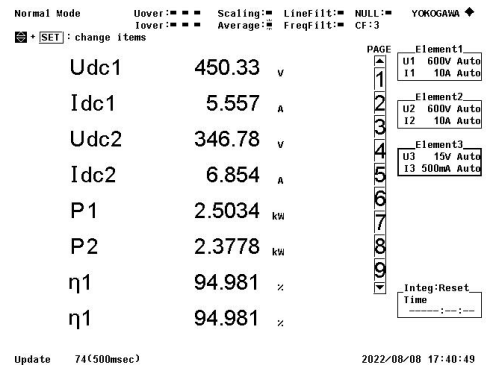
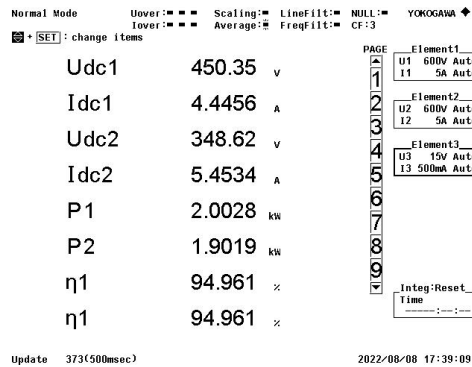
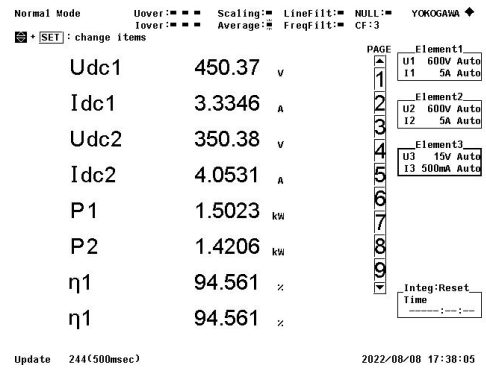
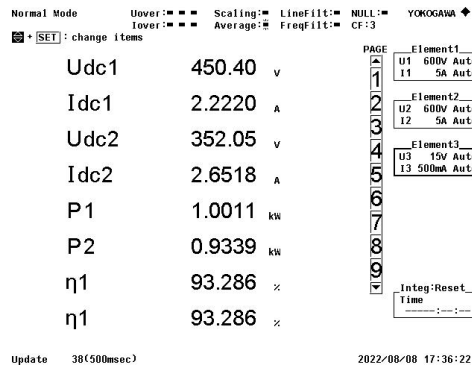






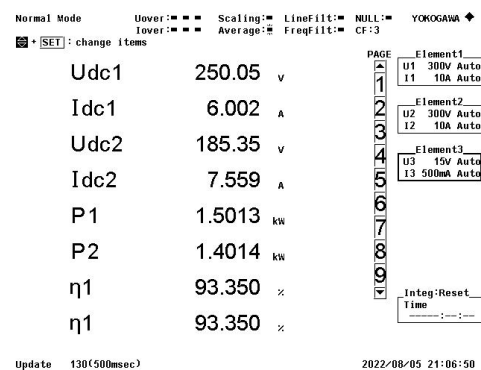
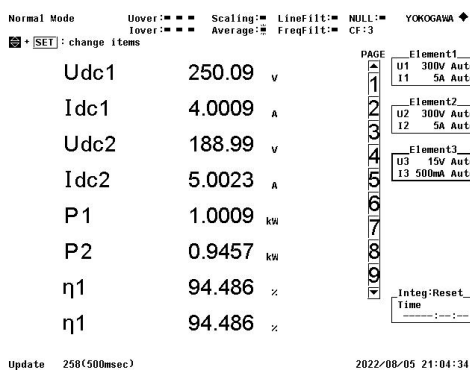
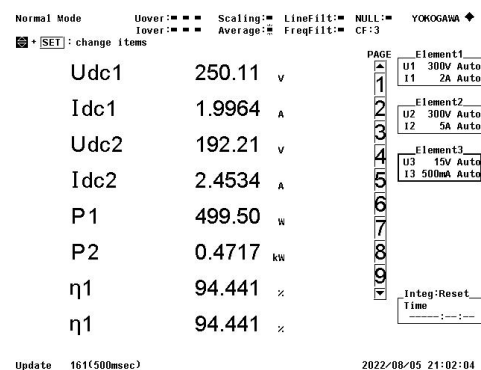
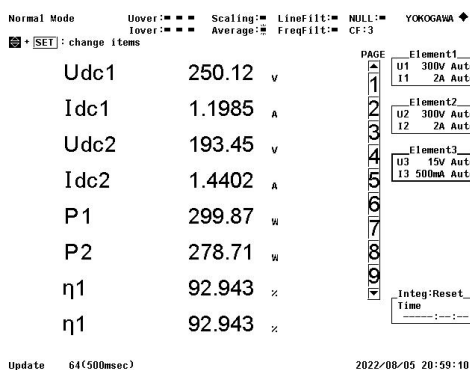


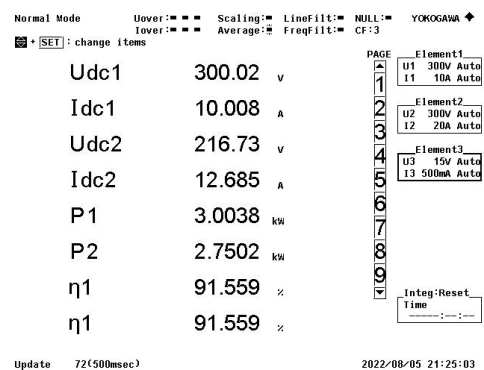
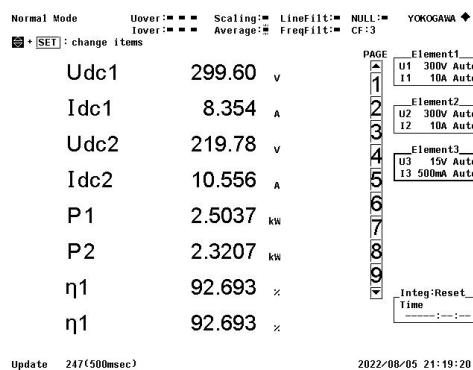
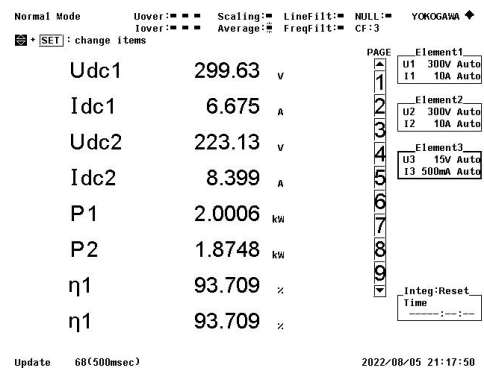
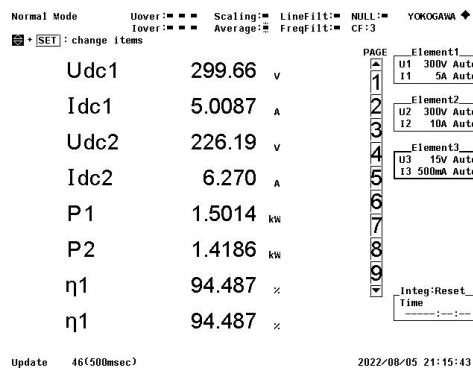
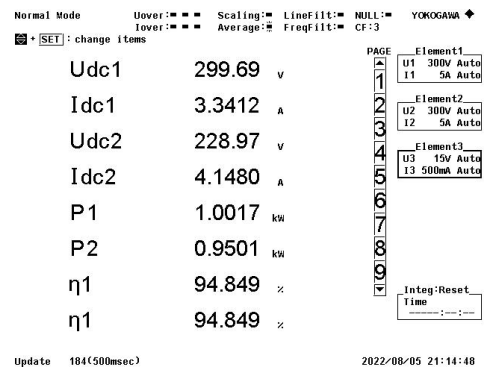
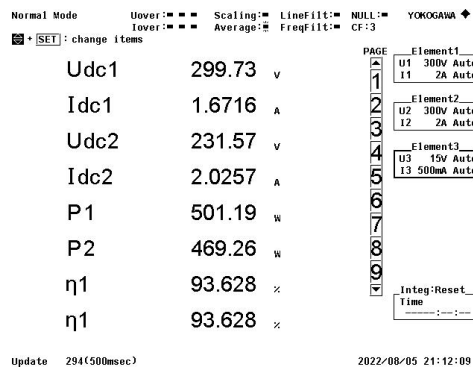
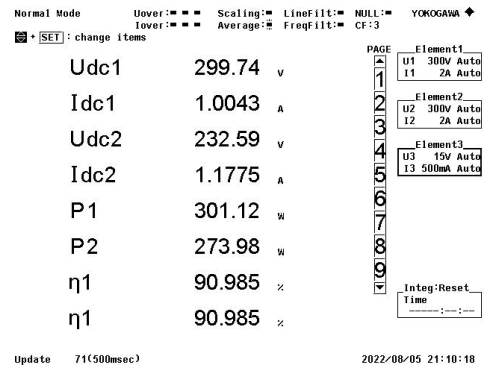
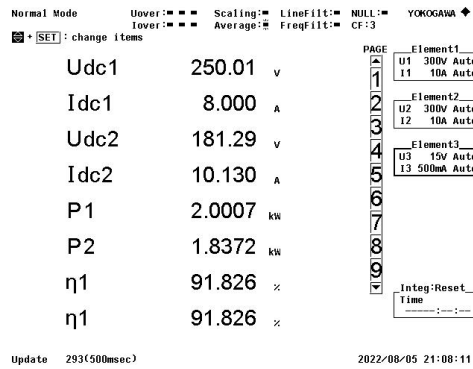


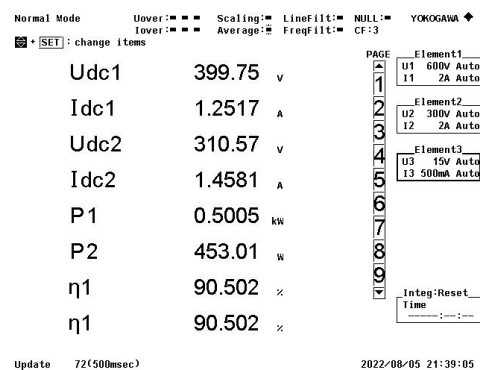
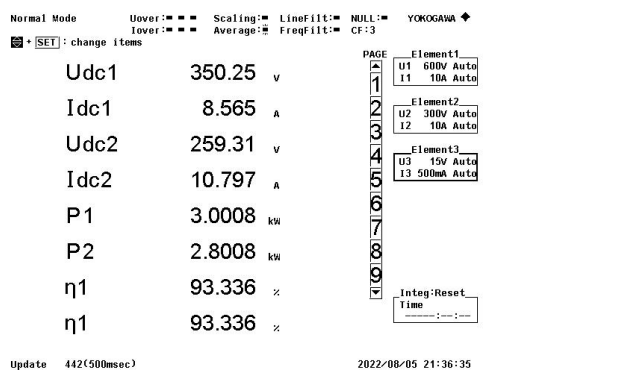
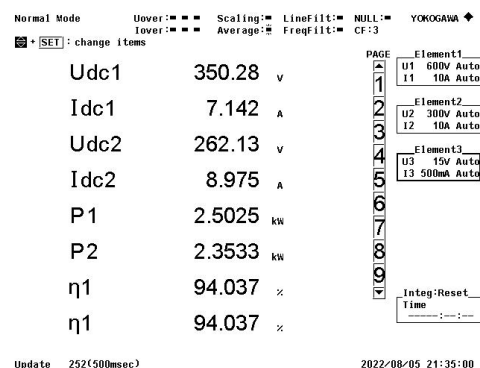
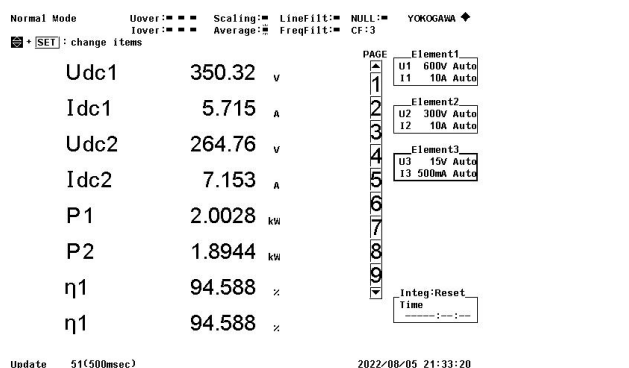
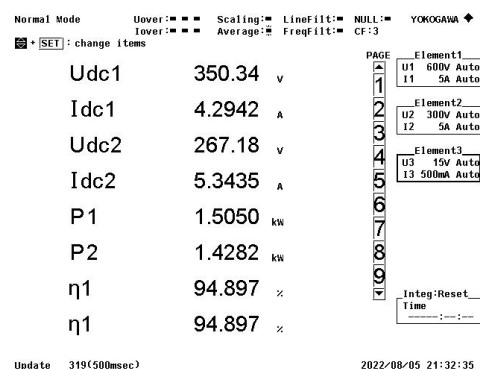
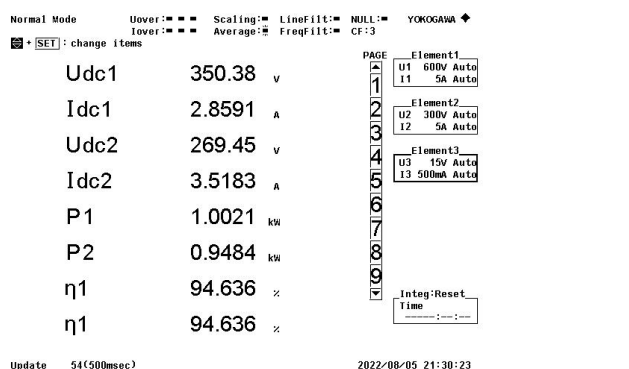
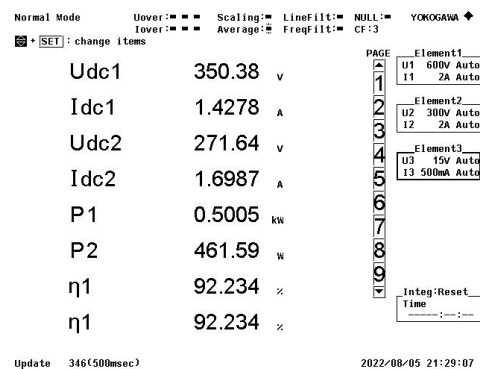
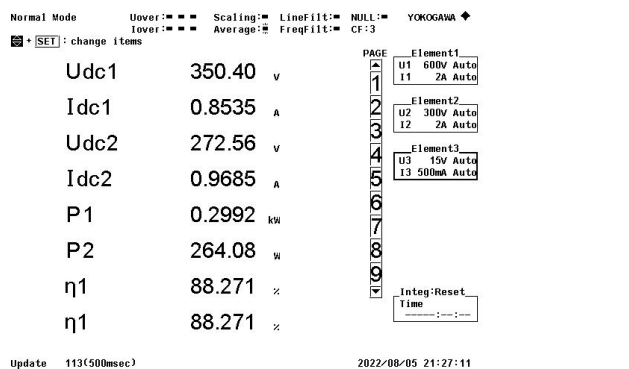


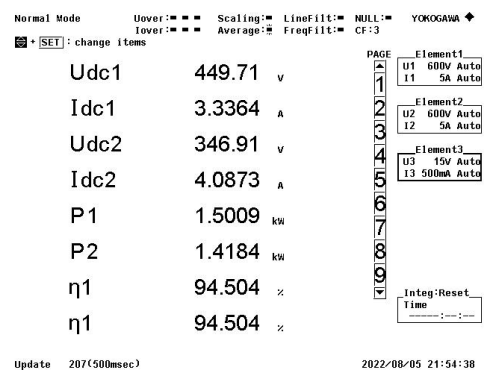
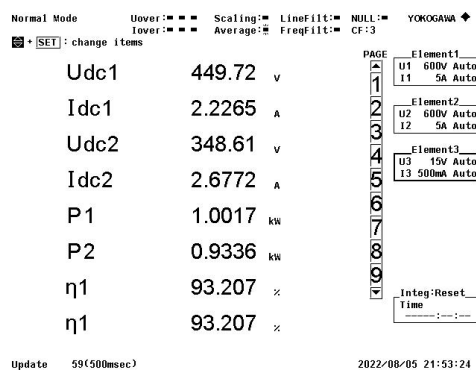
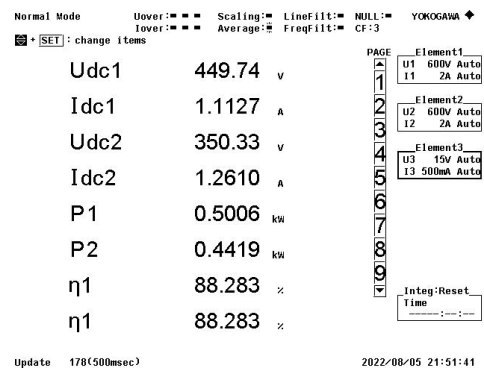
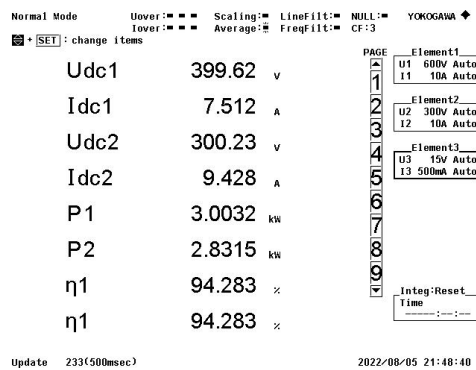
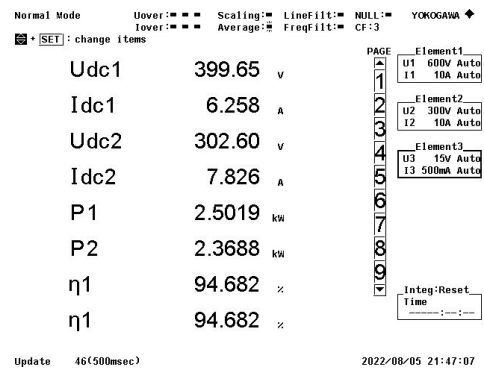
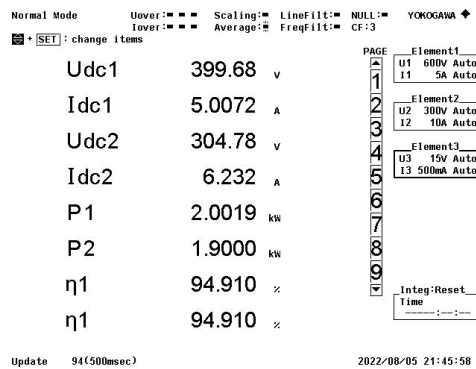
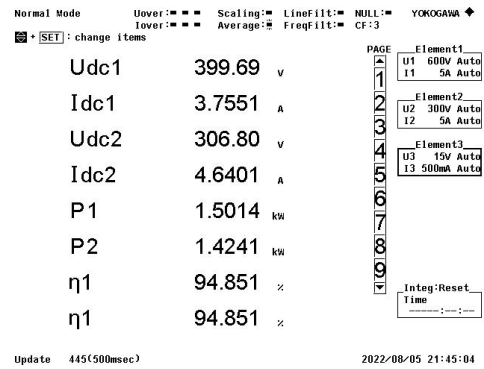
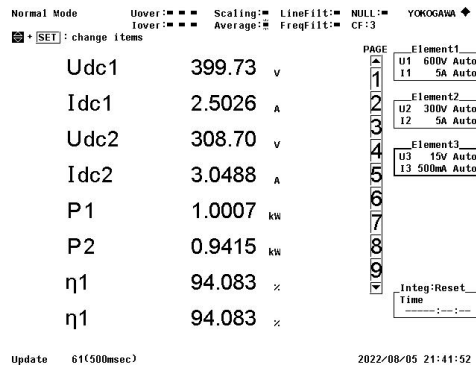
G

Appendix G: Efficiency of LCC-S compensation topology after tuning (M=76 μ H)









Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF:3

SET: change items

Udc1	449.65	V
Idc1	4.4520	A
Udc2	345.13	V
Idc2	5.505	A
P1	2.0026	kW
P2	1.9005	kW
η 1	94.904	%
η 1	94.904	%

PAGE

Element1
U1 600V Auto
I1 5A Auto

Element2
U2 600V Auto
I2 10A Auto

Element3
U3 15V Auto
I3 500mA Auto

Integ:Reset
Time
-----:--:--

Update 38(500msec) 2022/08/05 21:55:58

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF:3

SET: change items

Udc1	449.65	V
Idc1	5.559	A
Udc2	343.27	V
Idc2	6.913	A
P1	2.5003	kW
P2	2.3739	kW
η 1	94.941	%
η 1	94.941	%

PAGE

Element1
U1 600V Auto
I1 10A Auto

Element2
U2 600V Auto
I2 10A Auto

Element3
U3 15V Auto
I3 500mA Auto

Integ:Reset
Time
-----:--:--

Update 56(500msec) 2022/08/05 21:58:05

Normal Mode Uover: ■ ■ ■ Scaling: ■ LineFilt: ■ NULL: ■ YOKOGAWA ◆
Iover: ■ ■ ■ Average: ■ FreqFilt: ■ CF:3

SET: change items

Udc1	449.62	V
Idc1	6.676	A
Udc2	341.28	V
Idc2	8.336	A
P1	3.0028	kW
P2	2.8460	kW
η 1	94.776	%
η 1	94.776	%

PAGE

Element1
U1 600V Auto
I1 10A Auto

Element2
U2 600V Auto
I2 10A Auto

Element3
U3 15V Auto
I3 500mA Auto

Integ:Reset
Time
-----:--:--

Update 227(500msec) 2022/08/05 21:59:31