p^+ poly-Si(O_x) passivating contacts for double-side textured c-Si solar cell

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Abstract

Silicon solar cells account for about 95% of the total photovoltaic market share. Poly-Si passivating contacts are promising techniques enabling high performance c-Si solar cells with conversion efficiency over 26.0%. The highly absorptive nature of poly-Si materials makes the transparent passivating contacts attractive, such as poly-Si(O_x).However, the research of p^+ poly-Si(O_x) passivating contacts on a textured surface with a *in-situ* doping nature is still missing.Therefore, in this thesis, the optimization of p^+ poly-Si(O_x) carrier selective passivating contacts on double side textured wafers are given and the application in solar cells is demonstrated.

Firstly, the influences of different interfacial tunnelling oxides fabrication methods, nitric acid oxidation of silicon (NAOS-SiO_x), plasma assisted N_2O oxidation (PANO-SiO_x), and thermal oxidation (t-SiO_x) on the passivation of p^+ poly-Si(O_x) passivating contacts are explored. It is found that Si^{4+} stoichiometry in the tunnelling oxide layer is an indicator for its quality. There is a positive correlation between Si^{4+} and SiO_x density. The t-SiO_x can be denser with higher Si^{4+} compared to its counterparts NAOS-SiO_x and PANO-SiO_x. And fewer boron dopants in-diffuse phenomenon can be observed in the t-SiO_x samples. Then, different intrinsic layer deposition approaches are explored. The intrinsic layer deposited by LPCVD results in higher iV_{oc} compared to PECVD counterpart. The enhanced iV_{oc} is given by suppressing the blistering which is caused by hydrogen accumulation at the interface between intrinsic layer and SiO_x. It is assumed that less hydrogen accumulation exists in intrinsic layer deposited by LPCVD. Next, p^+ doping layer thickness is changed from 0 nm to 200 nm to observe its effect on the passivation quality. The optimum p^+ doping layer thickness is found to be 100 nm with the highest iV_{oc}. After that, the hydrogenation process is introduced to enhance chemical passivation by coating SiN_x:H and performing forming gas annealing. The highest iV_{oc} with the standard hydrogenation process is 674 mV. In order to improve the hydrogen level of p^+ poly-Si(O_x) passivating contacts, AlO_x:H inserted layer is used for the hydrogen reservoir together with SiN_x:H. It results in an improved iV_{oc} of 685 mV. It is assumed that the hydrogen in AlO_x:H diffuses into c-Si/p^+ poly-Si(O_x) interface and enhances the chemical passivation.

Besides, metallization methods of p^+ poly-Si(O_x) passivity contacts are also studied. There are two approaches to complete the metallization process. Firstly, with thin p^+ poly-Si(O_x) passivating contacts, TCO is required to provide with the lateral and vertical carrier transport as respect to the carrier collection. However, it commonly brings with the TCO introduced sputtering damage. The iV_{oc} losses are 70-90 mV when TCO is sputtered on p^+ poly-Si(O_x) passivating contacts. When the thickness of p^+ doping layer is over 50 nm, sufficient lateral conductivity can be provided with thick p^+ poly-Si(O_x) passivating contacts. Therefore, it can directly contact with metal which is the second method of metallization. However, when utilizing this metallization method, the metal induced recombinations need to be taken into consideration when contacting with p^+ poly-Si(O_x) passivating contacts. Thus, the plot of $J_{o,total}$ along with different metal fractions is fitted to extract $J_{o,metal}$ of p^+ poly-Si(O_x) passivating contacts with 100 nm p^+ doping layer. When contacting with evaporated aluminium, the measured $J_{o,metal}$ is around 91 fA/cm^2. In addition, after calculating, there is 24 mV iV_{oc} loss when p^+ poly-Si(O_x) passivating contacts contacting with metal. It is smaller than the loss induced by TCO sputtering. Therefore, the thick p^+ poly-Si(O_x) passivating contacts with 100 nm p^+ doping layer directly contacting with metal is used as metallization method for the application in c-Si solar cell. In addition, after linear fitting and calculating, ρ_c between p^+ poly-Si(O_x) passivating contacts with 100 nm boron doped layer and c-Si is about 23 m$\Omega\cdot$ cm^2.

Finally, p^+ poly-Si(O_x) passivating contact is applied in c-Si solar cells together with n^+ poly-Si(O_x) passivating contact as front surface field. The poly-poly solar cell of the highest quality has the following electrical performance : V_{oc} is 648 mV, J_{sc} is 35.9 mA/cm^2, FF is 73.1% and η is 17.0%. A roadmap to realize 22% is given by addressing the bottlenecks of poly-Si(O_x) passivating contacts based c-Si solar cells.

Contents

Acknowledgements i

Abstract ii

1 Introduction 1
1.1 Working principle of the solar cells . . . 1
1.2 Solar cell loss mechanisms . . . 4
1.2.1 Optical losses . . . 4
1.2.2 Electrical losses . . . 7
1.3 poly-Si(O_x) passivating contacts . . . 14
1.3.1 Surface formation . . . 14
1.3.2 Interfacial oxides . . . 15
1.3.3 poly-Si(O_x) thin films . . . 16
1.3.4 Crystallization . . . 17
1.3.5 Hydrogenation . . . 18
1.4 Application in c-Si solar cells . . . 18
1.4.1 Metallization . . . 18
1.4.2 Solar cells . . . 19
1.5 Motivation and objectives . . . 19
1.5.1 Motivations . . . 19
1.5.2 Objectives . . . 20
1.6 Thesis outline . . . 20

2 Experimental methods and Process techniques 22
2.1 Fabrication process . . . 22
2.1.1 c-Si absorber . . . 22
2.1.2 Passivation samples preparation . . . 23
2.1.3 Solar cells fabrication . . . 25
2.2 Characterization techniques . . . 36
2.2.1 Optical performance . . . 36
2.2.2 Surface morphology . . . 37
2.2.3 Lifetime and J_o measurement . . . 39
2.2.4 Compositional analysis . . . 41
2.2.5 Current-voltage measurement . . . 43

3 Passivation of p^+ poly-Si(O_x) passivating contacts 45
3.1 Absorber surface . . . 45
3.2 Interfacial oxides . . . 47
3.3 Ultra-thin p^+ poly-Si(O_x) thin films . . . 51
3.3.1 Intrinsic layer deposition methods . . . 51
3.3.2 t-SiO_x layer thickness . . . 53
3.3.3 Pre-annealing . . . 56
3.3.4 PECVD p^+ doping layer optimization . . . 58
3.4 Optimization of hydrogenation scheme . . . 60
3.5 TCO sputtering damage . . . 62
3.6 Thick p^+ poly-Si(O_x) thin films . . . 64
3.6.1 p^+ doped layer thickness . . . 65

4 Contact properties of p^+ poly-Si(O_x) passivating contacts 67
4.1 Contact resistivity . . . 67
4.2 Metal-induced recombination . . . 72

5 Application in c-Si solar cells **81**
5.1 Passivation optimization of ion-implanted p^+ emitter 81
5.1.1 NAOS protective layer 81
5.1.2 AlO_x:H capping layer optimization 82
5.1.3 FGA conditions 85
5.1.4 Boron doping profile 85
5.2 i-TOPCon solar cell on DST wafers 87
5.2.1 Electrical performance 87
5.3 poly-poly solar cell on DST wafers 88
5.3.1 Electrical performance 88

6 Conclusions and Outlooks **92**
6.1 Conclusions 92
6.2 Outlooks 93
6.2.1 p^+ poly-Si(O_x) passivating contacts 93
6.2.2 poly-Si(O_x) solar cells 93

References **95**

List of Figures

1.1 Percentage of Global Annual Production [30] and [63] 2
1.2 Development of Laboratory Solar Cell Efficiencies [30] and [63] 2
1.3 Best lab cells versus Best lab modules [30] and [63] 3
1.4 Simple schematic of photovoltaic effect 4
1.5 (a)Illustrating the absorption of a photon in a semiconductor with bandgap E_{G}. The photon with energy E_{ph}=hv excites an electron from E_{i} to E_{f}. At E_{i} a hole is created.(b)If E_{ph}>E_{G}, a part of the energy is thermalized.[77] 5
1.6 The doping process illustrated using the bonding model.(a) A phosphorus (P) atom replaces a Si atom in the lattice resulting in the positively-ionized P atom and a free electron.(b) A boron (B) atom replaces a Si atom resulting in the negatively ionized B atom and a hole.[77] 6
1.7 Formation of a space-charge region, when n-type and p-type semiconductors are brought together to form a junction.The coloured part represents the space-charge region.[77] . 7
1.8 A very simple solar cell model.(1)Absorption of a photon leads to the generation of an electron-hole pair.(2)Usually, the electrons and holes will recombine.(3)With semipermeable membranes the electrons and the holes can be separated.(4)The separated electrons can be used to drive an electric circuit. (5)After the electrons have passed through the circuit, they will recombine with holes.[77] 8
1.9 The *J-V* characteristics of a p-n junction in the dark and under illumination[77] 9
1.10 The loss mechanisms of solar cell[77] 10
1.11 Schematic of thermallization losses of spectral mismatch losses[77] 10
1.12 Schematic of non-absorption losses of spectral mismatch losses[77] 11
1.13 Schematic of anti-reflection coating to reduce reflection losses 11
1.14 Schematic of texturing to reduce reflection losses 11
1.15 Schematic of Shockley-Queisser efficiency[77] 12
1.16 Schematic of Radiative recombination, Auger recombination and SRH recombination [77] 12
1.17 Illustrating dangling bonds (surface defects) on a semiconductor surface[77] 13
1.18 Simple schematic of Al BSF solar cell 13
1.19 Simple schematic of PERC solar cell 13
1.20 FBC solar cell with TOPCon configuration [81] 14
1.21 Single-diode model of solar cell 14
1.22 The influences of series resistance R_s on the I-V characteristics of solar cell 15
1.23 The influences of shunt resistance R_{p} on the I-V characteristics of solar cell 15
1.24 Simple schematic of all the solar cell losses 15
1.25 Simple schematic of charge carriers transporting in n^{+} poly-Si($\mathrm{O_x}$) carrier selective passivating contacts 18
1.26 H,O chemical passivation 18

2.1 Simple schematic of LPCVD equipment 24
2.2 Simple schematic of PECVD equipment 25
2.3 Simple schematic of ion-implantation equipment 26
2.4 Schematic of ALD process flowchart 27
2.5 Simple schematic of ALD process 27
2.6 Simple schematic of thermal-ALD equipment 28
2.7 Schematic of spatial ALD 28
2.8 Simple schematic of spatial ALD equipment 29
2.9 Simple schematic of sputtering equipment 29
2.10 Simple schematic of photolithography process [59] 30
2.11 Simple schematic of evaporation equipment [93] 31

2.12 Simple schematic of i-TOPCon mono-facial solar cell on DST wafers 31
2.13 Flowchart of texturing process 32
2.14 Simple flowchart for poly-poly mono-facial solar cell 34
2.15 Schematic of the principle of Spectroscopic ellipsometry 37
2.16 Simple schematic of Spectroscopic ellipsometry by J. A. Woollam Co. 37
2.17 Simple schematic of the reflectance measurement equipment 38
2.18 Simple schematic of the components of the microscope [66] 38
2.19 Simple schematic of SEM[39] 39
2.20 Schematic of the Sinton WCT-120 lifetime tester 41
2.21 Simple schematic of Sinton WCT-120 Photoconductance Decay Lifetime Tester 41
2.22 Simple schematic of the components of SIMS[86] 42
2.23 Simple schematic of XPS measurement[87] 42
2.24 Simple schematic of ECV profiling[48] 43
2.25 Simple schematic of Wacom Current-Voltage measurement 44

3.1 The sample structure for the experiment on abosorber surface. The aim of the experiment is to explore the influences of both poly-etch duration time and and times of NAOC on the optical and electrical performance of p^+ poly-Si(O_x) passivating contacts. 45
3.2 The influences of poly-etch time and times of NAOC on the electrical performance of p^+ poly-Si(O_x) passivating contacts 46
3.3 The effects of poly-etch time and times of NAOC on the optical properties of p^+ poly-Si(O_x) passivating contacts 46
3.4 Different types of interfacial silicon oxide layers have various properties as reported by van der Vossen,R et al and Huang, Y et al. [37][85] 47
3.5 Fabrication process for experiments of different tunnelling silicon oxide types on DSP wafers 47
3.6 Fabrication process for experiments of different tunnelling silicon oxide types on DST wafers 49
3.7 Minority carrier lifetime of three samples with different tunnelling silicon oxide types on DSP wafers 49
3.8 iV_{oc} of three samples with different tunnelling silicon oxide types on DSP wafers 49
3.9 Minority carrier lifetime of three samples with different tunnelling silicon oxide types on DST wafers 50
3.10 iV_{oc} of three samples with different tunnelling silicon oxide types on DST wafers 50
3.11 XPS measurement results of three different silicon oxide types 50
3.12 SIMS measurement results of three different silicon oxide types 51
3.13 Structures for testing the blistering conditions and corresponding passivation quality . . 52
3.14 Blistering conditions of different structures observed under optical microscope. 52
3.15 iV_{oc} of four different testing structures as above mentioned after different PDA conditions 53
3.16 iV_{oc} of four different testing structures as above mentioned after hydrogenation 53
3.17 t-SiO_x thickness changes with oxidation time 54
3.18 t-SiO_x thickness changes with oxygen volume ratio during thermally oxidation 54
3.19 t-SiO_x thickness changes with oxidation temperature 54
3.20 Simple schematic of the fabricated samples with thicker t-SiO_x 55
3.21 Passivation results of samples with thicker t-SiO_x tunnelling layer 56
3.22 Passivation results of p^+ poly-Si(O_x) passivating contacts with thicker t-SiO_x tunnelling layer and pre-annealing 1025/1 57
3.23 Passivation results of p^+ poly-Si(O_x) passivating contacts with thicker t-SiO_x tunnelling layer and different pre-annealing conditions ranging from 1000/1 to 1050/1 57
3.24 Passivation results of p^+ poly-Si(O_x) passivating contacts with different O concentration during PECVD p^+ doping layer 59
3.25 Passivation results of p^+ poly-Si(O_x) passivating contacts with different B concentration during PECVD p^+ doping layer 59
3.26 Passivation results of p^+ poly-Si(O_x) passivating contacts with different p^+ doping layer thickness during PECVD 59
3.27 SIMS results of n^+ poly-Si(O_x) passivating contacts 61

3.28 SIMS results of p^+ poly-Si(O_x) passivating contacts . . . 61
3.29 The passivation results with AlO_x:H and AlO_x:H/SiN_x:H as capping layer(s) during hydrogenation process[5] . . . 62
3.30 The passivation results with different capping layer(s) during hydrogenation process and the corresponding different post deposition annealing conditions[5] . . . 62
3.31 Fabrication process of IWO sputtering damage on textured p^+ poly-Si(O_x) passivating contact . . . 63
3.32 The influences of p^+ doping layer thickness during PECVD on the TCO sputtering damage of textured surface . . . 63
3.33 The corresponding iV_{oc} degradation caused by IWO sputtering before and after oven annealing recovery . . . 64
3.34 Simple schematic of i-TOPCon solar cell . . . 65
3.35 Simple schematic of poly-poly solar cell . . . 65
3.36 Influence of p^+ doped layer thickness on the passivation quality of thicker p^+ poly-Si(O_x) passivating contacts (>50nm) . . . 66
3.37 Influence of p^+ doped layer thickness on the passivation quality of p^+ poly-Si(O_x) passivating contacts (0-200nm) . . . 66

4.1 (a) The band diagrams of a metal and an n-type semiconductor that are separated from each other.(b) The band diagram of a junction between a metal and an n-type semiconductor[77] . . . 68
4.2 I-V curve when metal contacting Si in schottky contact . . . 69
4.3 I-V curve when metal contacting Si in ohmic contact . . . 70
4.4 Schematic of transfer length . . . 71
4.5 Schematic of metal pad . . . 71
4.6 linear fitting curve of the TLM method to measure the contact resistance . . . 71
4.7 Implied open circuit voltage of the samples prepared for measuring contact resistivity through TLM . . . 72
4.8 Sheet resistance of the samples prepared for measuring contact resistivity through TLM 72
4.9 The linear fitting curve of the sample with 100 nm boron doping layer and post deposition annealing at 875°C duration for 30 minutes . . . 73
4.10 Testing structure (1) 110 nm p^+ poly-Si(O_x) passivating contact for measuring $J_{o,metal}$. 75
4.11 Testing structure (2) boron ion-implanted p^+ emitter with doping dose $1 \times 10^{15} cm^{-2}$ for measuring $J_{o,metal}$ . . . 75
4.12 Testing structure (3) 110 nm p^+ poly-Si(O_x) passivating contacts on boron ion-implanted p^+ emitter with doping dose $1 \times 10^{15} cm^{-2}$ for measuring $J_{o,metal}$ . . . 75
4.13 The mask with different metal fractions for measuring metal-induced recombination current density . . . 76
4.14 Flowchart of measuring the metal-induced recombination current density starting from photolithography . . . 76
4.15 The total recombination current density after different Al annealing conditions when the temperature is 300°C . . . 77
4.16 The total recombination current density after different Al annealing conditions when the temperature is 400°C . . . 77
4.17 $J_{,total}$ linear fitting curve of 110nm p^+ poly-Si(O_x) passivating contacts . . . 78
4.18 $J_{o,total}$ values of 110 nm p^+ poly-Si(O_x) passivating contacts . . . 78
4.19 $J_{o,total}$ linear fitting curve of p^+ emitter . . . 79
4.20 $J_{o,total}$ values of p^+ emitter . . . 79
4.21 $J_{o,total}$ linear fitting curve of 110nm p^+ poly-Si(O_x) passivating contacts on p^+ emitter . . 80
4.22 $J_{o,total}$ values of 110nm p^+ poly-Si(O_x) passivating contacts on p^+ emitter . . . 80

5.1 Recombination current density of p^+ emitter with or without NAOS on it before hydrogenation with different AlO_x:H/SiN_x:H annealing methods and conditions . . . 82
5.2 Implied open circuit voltage of p^+ emitter with or without NAOS on it before hydrogenation with different AlO_x:H/SiN_x:H annealing methods and conditions . . . 82

5.3 Implied open circuit voltage of AlO_x:H/SiN_x:H capping layer stack passivation on p^+ emitter with different AlO_x:H thickness . . . 83
5.4 Simple schematic of AlO_x:H pre annealing . . . 83
5.5 The relations between sheet resistance and doping dose during ion implantation of p^+ emitter . . . 84
5.6 Minority carrier lifetime of p^+ emitter of $161\Omega/\square$ as sheet resistance with different AlO_x:H pre annealing conditions . . . 84
5.7 Minority carrier lifetime of p^+ emitter of $39\Omega/\square$ as sheet resistance with different AlO_x:H pre annealing conditions . . . 84
5.8 Recombination current density of AlO_x:H/SiN_x:H capping layer stack passivation on p^+ emitter with different FGA conditions . . . 85
5.9 Implied open circuit voltage of AlO_x:H/SiN_x:H capping layer stack passivation on p^+ emitter with different FGA conditions . . . 85
5.10 The ECV profiling of p^+ emitter sample with the doping dose $5\times10^{14}cm^{-2}$ activated in TEMPRESS tube furnace at EKL and reference p^+ emitter sample from industry with unknown doping dose . . . 86
5.11 The ECV profiling of p^+ emitter samples of doping dose of $5\times10^{15}cm^{-2}$ with different driving-in time and reference p^+ emitter sample from industry with unknown doping dose 86
5.12 Simple schematic of i-TOPCon monofacial solar cell . . . 87
5.13 Passivation quality of poly-poly mono-facial cell precursors . . . 88
5.14 Simple schematic of poly-poly monofacial solar cell . . . 89
5.15 Electrical performance of poly-poly mono-facial cell precursors with the highest efficiency 89
5.16 Efficiency of poly-poly mono-facial cell precursors for 6 different dies with cell precursors post deposition annealing at 925 °C duration for 20 minutes . . . 90
5.17 Open circuit voltage of poly-poly mono-facial cell precursors for 6 different dies with cell precursor post deposition annealing at 925°C duration for 20 minutes . . . 90
5.18 Short circuit current density of poly-poly mono-facial cell precursors for 6 different dies with cell precursor post deposition annealing at 925°C duration for 20 minutes . . . 90
5.19 Fill factor of poly-poly mono-facial cell precursors for 6 different dies with cell precursor post deposition annealing at 925 °C duration for 20 minutes . . . 90
5.20 V_{oc} of die 1 with 4 different PDA conditions . . . 91
5.21 η of die 1 with 4 different PDA conditions . . . 91

List of Tables

2.1 TOPSIL n-type FZ c-Si wafers details and properties 22

3.1 plasma-SiO_x tunnelling oxide layer PECVD parameters 48
3.2 a-$Si(O_x)$:H intrinsic layer PECVD parameters 48
3.3 p^+ a-$Si(O_x)$:H doping layer PECVD parameters 48
3.4 XPS measurement results of three different silicon oxide types 51
3.5 Passivation of p^+ poly-$Si(O_x)$ passivating contacts of different t-SiO_x thickness and with or without pre-annealing 58
3.6 The recipe for changing the O concentration during PECVD on flat surface 58
3.7 The recipe for changing the B concentration during PECVD on flat surface 60
3.8 The iV_{oc} and minority carrier lifetime of samples with ALD AlO_x:H and PECVD SiN_x:H stacks as capping layer for the optimization of hydrogenation process 62

4.1 Metal-induced recombination current density of samples of three different structures . . 77

5.1 V_{oc} for 6 various dies with 4 different PDA conditions 91
5.2 η for 6 various dies with 4 different PDA conditions 91

1 Introduction

Energy is the foundation of the world's economic and social development. With the large consumption of traditional fossil energy and the deterioration of human living environment, the development of clean renewable energy has attracted the attention of governments all over the world. Renewable energy includes solar energy, wind energy, geothermal energy, water energy and so on. The sun is a ball of gas that generates heat through nuclear fusion reaction in its center and the radiation intensity is close to the blackbody radiation with a temperature of 6000K. Nuclear fusion reaction constantly takes place inside the sun, constantly radiating energy to the outside. So, the solar energy is inexhaustible which is the best choice to solve the problem of energy shortage in the 21st century. The utilization of solar energy is mainly divided into two ways: one is the conversion of solar energy into heat energy for utilizing. The other is the conversion of solar energy into electricity for using, namely photovoltaics.

Photovoltaics is a fast-growing market: The compound annual growth rate (CAGR) of cumulative PV installations including off-grid was 34% between year 2010 to 2020. Wafer size increased and by keeping the number of cells larger, PV module sizes are realized allowing a power range beyond 600 W per module. Si-wafer based PV technology accounted for about 95% of the total production in 2020. The share of mono-crystalline technology is now about 84% (compared to 66% in 2019) of total c-Si production that can be discovered in Figure 1.1 and [65],[63].

The record lab cell efficiency is 26.7% [91]for mono-crystalline and 24.4% for multi-crystalline silicon wafer-based technology that can be discovered in Figure 1.2 and [63], [30]. In the last 10 years, the efficiency of average commercial wafer-based silicon modules increased from about 15% to 20% and more. In the laboratory, best performing modules are based on mono-crystalline silicon with 24.4% efficiency which can be seen in Figure 1.3 and [63],[30]. Record efficiencies demonstrate the potential for further efficiency increases at the production level.

1.1. Working principle of the solar cells

The working principle of solar cells is based on the photogenerating volt effect of semiconductors. The so-called photogenerating volt effect is an effect that produces electromotive force and current when the charge distribution in the object is changed when the object is illuminated. Crystalline silicon solar cell is essentially a large area of diode, composed of PN junction, passivation film and metal electrode. The simple schematic can be discovered in Figure 1.4.

The photogenerating volt effect can be divided into three basic processes. Firstly, when illuminating, due to the absorption of photons, charge carriers are generated in the materials which can form a junction. In an ideal semiconductor, electrons can only populate energy levels below valence band edge, E_v, and above conduction band edge, E_c. However, between these two bands, the electrons cannot occupy the energy states. Hence, this energy difference is called the band gapE_G. And E_G=E_c-E_v.If the photon with an energy E_{ph} larger than band gap E_G, the electrons are excited, then a void which

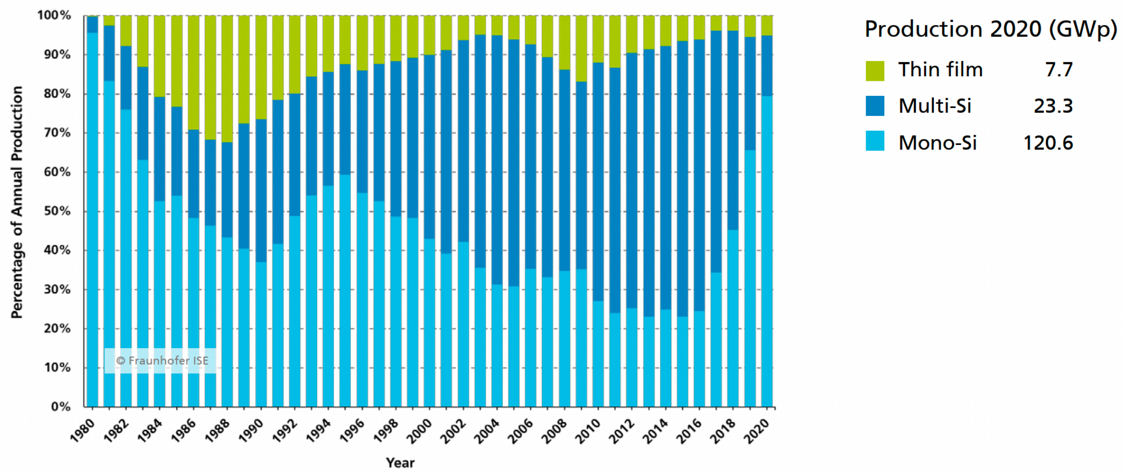


Figure 1.1: Percentage of Global Annual Production [30] and [63]

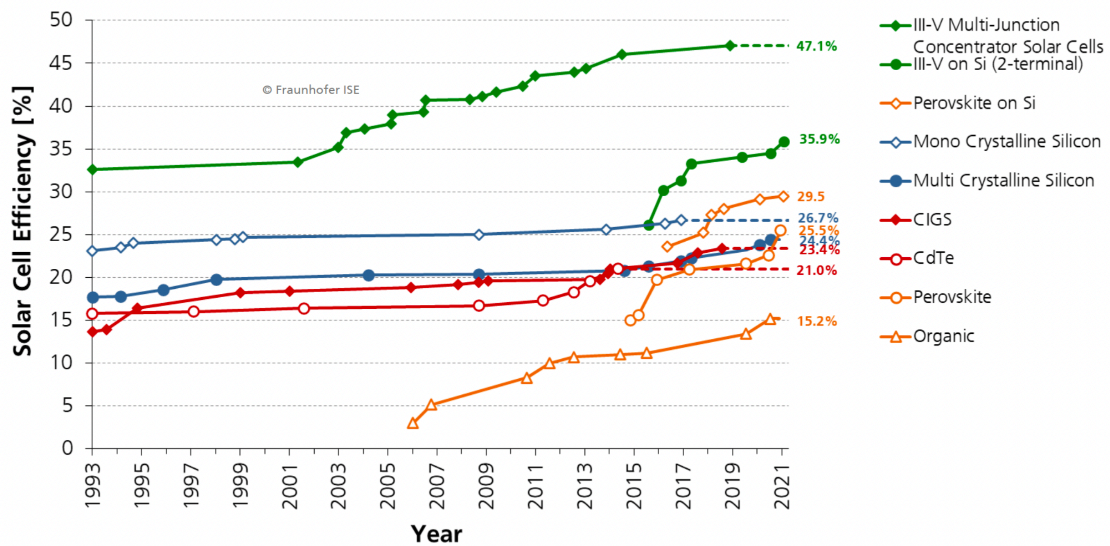


Figure 1.2: Development of Laboratory Solar Cell Efficiencies [30] and [63]

is an unoccupied energy state is left behind. The void behaves like a particle with positive elementary charge, is called a hole. The holes can also be considered as charge carriers that can move through the semiconductors. Thus, the absorption of a photon can lead to the creation of an electron-hole pair which can be discovered in Figure 1.5 and [77].Usually, the electron-hole pair will recombine and the energy will then be released.

Secondly, the photo-generated charge carriers in the junction will then be separated. Normally, the separation of charge carriers is done by a p-n junction. The p-type region is normally formed by doping with boron with three valence electrons on the outer shell which is illustrated in Figure 1.6 and [77]. One valence electron less will induce a hole and a fixed negative charge. Then in the p-doped regions, there are a lot of holes and fixed negative charges. Similarly, the n-type region is usually formed by doping with phosphorous with five valence electrons on the outer shell which can be shown in Figure 1.6. Then in the n-doped region, there are plenty of electrons and fixed positive charges. When a p-type and an n-type semiconductor are brought together, a very large difference in electron concentration between n- and p-type regions causes a diffusion current of electrons from the n-type material across the metallurgical junction into the p-type material. Similarly, the difference in hole concentration causes

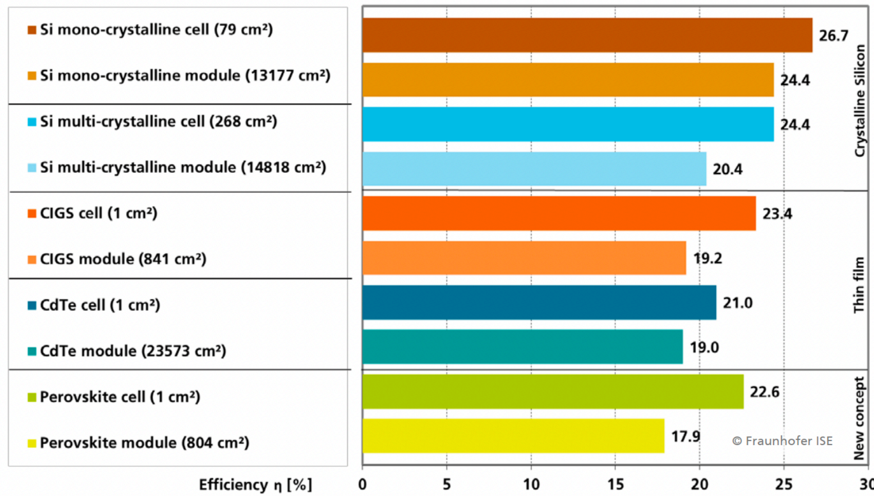


Figure 1.3: Best lab cells versus Best lab modules [30] and [63]

a diffusion current of holes from the p- to the n-type material. Due to this diffusion process, the region close to the metallurgical junction becomes almost completely depleted of mobile charge carriers. The gradual depletion of the charge carriers gives rise to a space charge created by the ionized donor and acceptor atoms that is not compensated by the mobile charges any more. This region of the space charge is called the space-charge region or depleted region. Regions outside the depletion region , in which the charge neutrality is conserved, are denoted as quasi-neutral regions which can be illustrated in Figure 1.7 and [77].

The space charge around the metallurgical junction results in the formation of an internal electric field which forces the charge carriers to move in the opposite direction than the concentration gradient. In addition, due to the electric field, a difference in the electrostatic potential is created between the boundaries of the space-charge region. Across the depletion region, the changes in the carrier concentration are compensated by changes in the electrostatic potential. Through the p-n junction, the holes and electrons are drawn to opposite polarities and ready for collecting before they combine which can be discovered in Figure 1.8 and [77].

And finally, the photo-generated charge carriers will be collected at the terminals of the junction. The external electric circuit is required to collect the electrons. The main parameters that are used to characterize the performance of solar cells are the peak power P_{max}, the short circuit current density J_{sc}, the open circuit voltage V_{oc}, and the fill factor FF. These parameters are determined from the illuminated *J-V* characteristic. The conversion efficiency η can be determined from these parameters.

The short circuit current I_{sc} is the current that flows through the external circuit when the electrodes of the solar cell are short circuited. The parameters that decide J_{sc} are the diffusion lengths of minority carriers. The open-circuit voltage is the voltage at which no current flows through the external circuit which represents the maximum voltage that a solar cell can deliver. V_{oc} can be calculated by equation 1.1, where $J_{\text{ph}} \gg J_{\text{o}}$ is the approximation.

$$V_{oc} = \frac{K_B T}{q} ln(\frac{J_{ph}}{J_o} + 1) \approx \frac{K_B T}{q} ln(\frac{J_{ph}}{J_o}) \tag{1.1}$$

V_{oc} is a measure of the amount of recombination in the device. The fill factor is the ratio between the maximum power P_{max}generated by a solar cell and the product of V_{oc} with J_{sc}. The calculation equation is 1.2,at mpp the solar cell has the maximum power output.

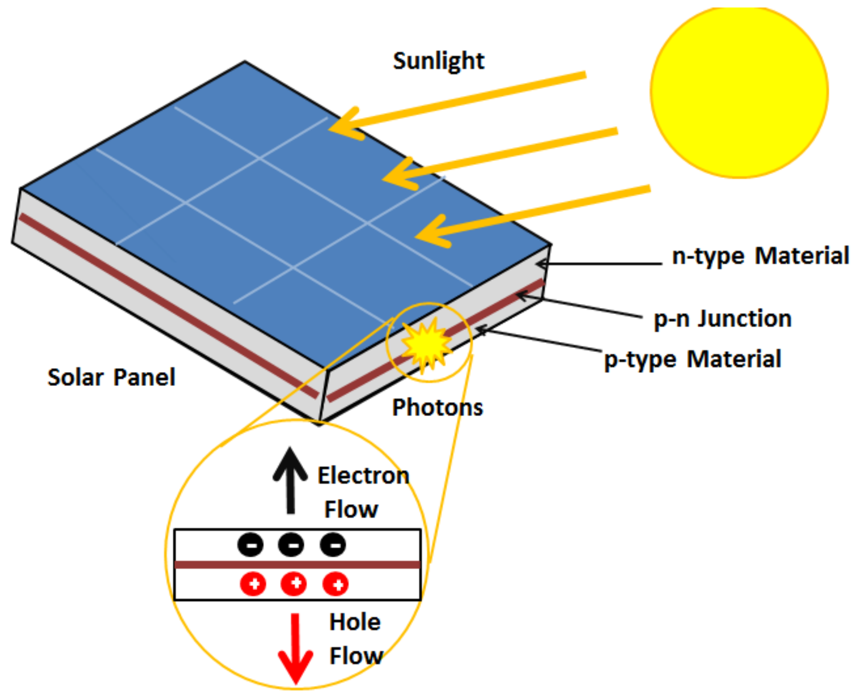


Figure 1.4: Simple schematic of photovoltaic effect

$$FF = \frac{J_{mpp}V_{mpp}}{J_{SC}V_{OC}} \tag{1.2}$$

The conversion efficiency is calculated as the ratio between the maximal generated power and the incident power. Solar cells are measured under the STC, where the incident light is described by the AM1.5 spectrum and has an irradiance of I_{in}=1000 W/m^2. It can be calculated by equation 1.3,

$$\eta = \frac{P_{max}}{I_{in}} = \frac{J_{mpp}V_{mpp}}{I_{in}} = \frac{J_{sc}V_{oc}FF}{I_{in}} \tag{1.3}$$

The *J*-*V* characteristics of a p-n junction in the dark and under illumination which is also the simple schematic of the external parameters can be shown in Figure 1.9 and [77]

1.2. Solar cell loss mechanisms

1.2.1. Optical losses

Spectral mismatch

The losses of solar cell can be divided into two parts that can be shown in Figure 1.10. One is optical losses and the other is electrical losses. The fundamental losses of optical losses are mainly spectral mismatch that includes thermalization and non-absorption. In principle, only photons with energy higher than the bandgap energy of the absorber can generate electron-hole pairs. Since the electrons and holes tend to occupy energy levels at the bottom of the conduction band and the top of the valence band, respectively. On one hand, the extra energy that the electron-hole pairs receive from the photons is released as heat into the semiconductor lattice in the thermalization process which can be discovered in Figure 1.11. The corresponding efficiency to thermallization losses is called P_{use} and the equation is shown in Equation 1.4. On the other hand, photons with energy lower than the bandgap energy of the absorber are in principle not absorbed and cannot generate electron-hole pairs which is called non-absorption losses that can be shown in Figure 1.12 and the corresponding equation is called P_{abs} that is shown in Equation 1.5. Both of these losses are thus related to the spectral mismatch between

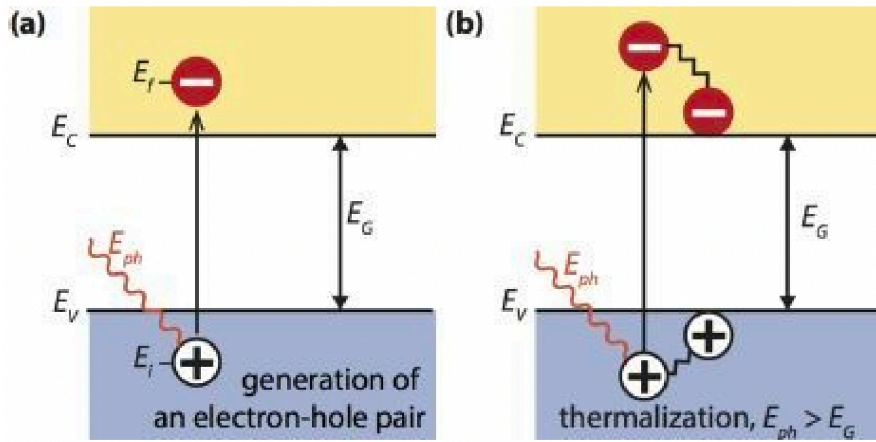


Figure 1.5: (a)Illustrating the absorption of a photon in a semiconductor with bandgap E_G. The photon with energy E_{ph}=hv excites an electron from E_i to E_f. At E_i a hole is created.(b)If E_{ph}>E_G, a part of the energy is thermalized.[77]

the energy distribution of photons in the solar spectrum and the bandgap of a semiconductor material [73].

$$P_{use} = \frac{E_G \int_0^{\lambda_G} \Phi(\lambda) d\lambda}{\int_0^{\lambda_G} P(\lambda) d\lambda} \tag{1.4}$$

$$P_{abs} = \frac{\int_0^{\lambda_G} P(\lambda) d\lambda}{\int_0^{\infty} P(\lambda) d\lambda} \tag{1.5}$$

The ultimate conversion efficiency is as the following Equation 1.6.

$$\eta_{ult} = P_{use} \times P_{abs} = \frac{E_G \int_0^{\lambda_G} \Phi(\lambda) d\lambda}{\int_0^{\lambda_G} P(\lambda) d\lambda} \times \frac{\int_0^{\lambda_G} P(\lambda) d\lambda}{\int_0^{\infty} P(\lambda) d\lambda} \tag{1.6}$$

Reflection

Part of the light is reflected and the other part is transmitted when light arrives on an interface between two media. The interface is therefore characterized by the wavelength-dependent reflectivity R(λ) and transmittance T(λ). All the reflections and transmissions at the different interfaces in the solar cell result in a total reflectance between the solar cell and the surrounding air. Hence, a part of the incident energy that can be converted into a usable energy by the solar cell is lost by reflection[77]. The corresponding equation is (1-R) and R can be calculated by Fresnel equation that can be seen in Equation 1.7.

$$R = |\frac{n_{air} - n_{Si}}{n_{air} + n_{Si}}|^2 \tag{1.7}$$

The reflection losses can be reduced by anti-reflection coating and texturing. The schematic of anti-reflection coating and texturing can be shown in Figure 1.13 and Figure 1.14.The optimum thickness for anti-reflection coating can be seen in Equation 1.8 and Equation 1.9.

$$n_1 = \sqrt{n_0 n_2} \tag{1.8}$$

$$d_1 = \lambda / 4n_1 \tag{1.9}$$

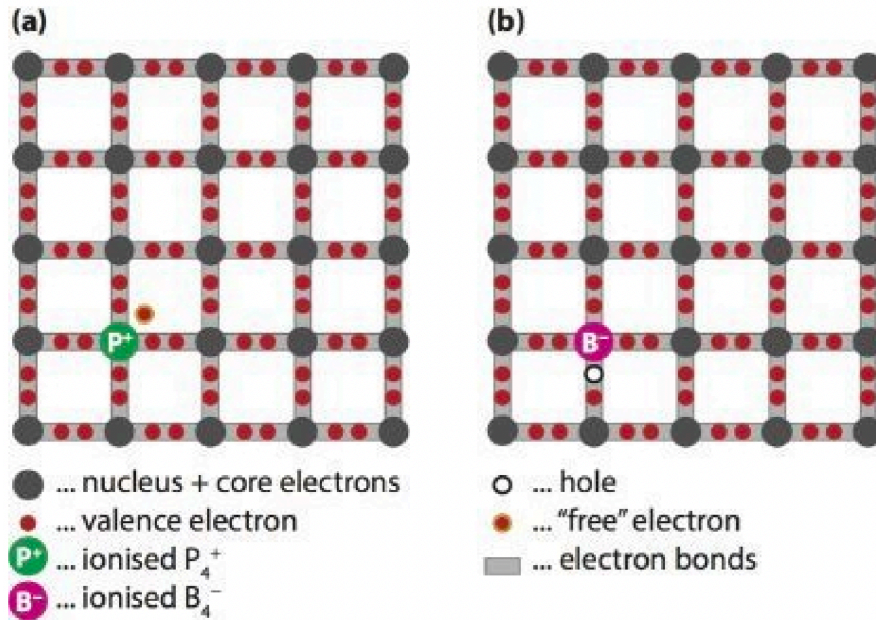


Figure 1.6: The doping process illustrated using the bonding model.(a) A phosphorus (P) atom replaces a Si atom in the lattice resulting in the positively-ionized P atom and a free electron.(b) A boron (B) atom replaces a Si atom resulting in the negatively ionized B atom and a hole.[77]

Surface shading

In most c-Si solar cells thin metal strips are placed on the front side of the solar cell that serve as front electrodes. The metal-covered area does not allow the light to enter the solar cell because it reflects or slightly absorbs the incident light. The area that is covered by the electrode decreases the active area of the solar cell. The total area of the cell as A_{tot} and the cell area that is not covered by the electrode as A_{f}, the fraction of the active area of the cell is determined by the ratio which is called the active area coverage factor C_{f} which the equation is shown in Equation 1.10. The resulting loss is called the surface shading loss.

$$C_f = \frac{A_f}{A_{tot}} \tag{1.10}$$

Not-complete absorption

Due to the limited thickness d of the absorber layer and the different absorption coefficient α with various thickness , not all the light entering the absorber layer is absorbed. Incomplete absorption in the absorber due to its limited thickness is an additional loss that lowers the energy conversion efficiency. The incomplete absorption loss can be described by the internal optical quantum efficiency IQE_{op}, which is defined as the probability of a photon being absorbed in the absorber material. Since there is a chance that a highly energetic photon can generate more than one electron-hole pair, the quantum efficiency for carrier generation η_{g}, which represents the number of electron-hole pairs generated by one absorbed photon. Usually η_{g} is assumed to be unity.Therefore, the equation corresponding to not-complete absorption can be shown in Equation 1.11 and Equation 1.12.

$$\eta = \eta_g IQE_{op} \tag{1.11}$$

$$T = exp(-\alpha d) \tag{1.12}$$

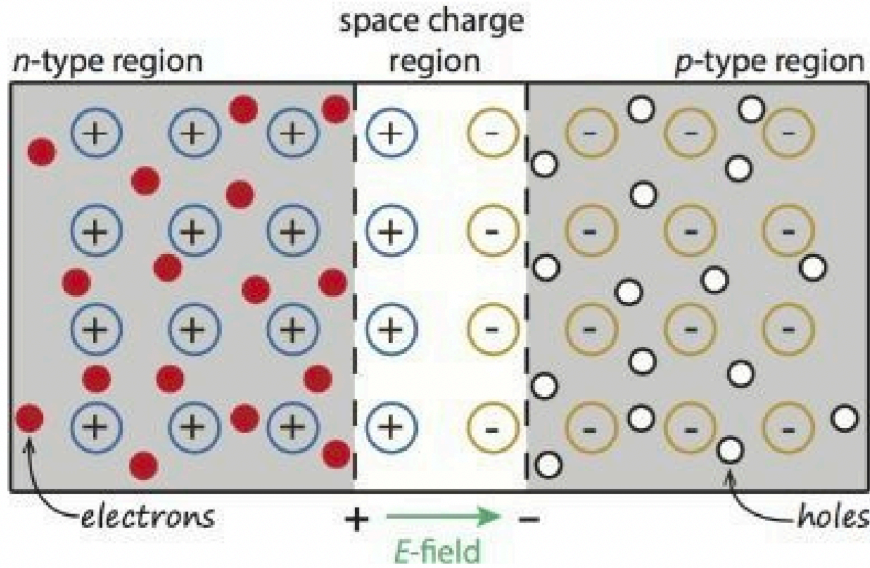


Figure 1.7: Formation of a space-charge region, when n-type and p-type semiconductors are brought together to form a junction.The coloured part represents the space-charge region.[77]

Parasitic absorption

When light penetrates into a material, it will be partially absorbed as it propagates through the material. The absorption of light in the material depends on its absorption coefficient and the layer thickness. In general, light is absorbed in all layers of the solar cell. All the absorption in layers other than the absorber layer is loss. It is called the parasitic absorption [28].

1.2.2. Electrical losses

Bandgap utillization

The bandgap utilization efficiency is given by η_v which tells the fraction of the bandgap that can be used as open circuit voltage.The corresponding equations can be discovered in the following Equation 1.13, Equation 1.14, Equation 1.15 and Equation 1.17

$$\eta_v = \frac{qV_{oc}}{E_G} \tag{1.13}$$

$$J = J_o exp[\frac{qV}{KT} - 1] - J_{ph} \tag{1.14}$$

Then,

$$V_{oc} = \frac{KT}{q} ln[\frac{J_{ph}}{J_o} + 1] \tag{1.15}$$

Thus,

$$\eta_v(E_G) = \frac{KT}{E_G} ln[\frac{J_{ph}(E_G)}{J_o(E_G)} + 1] \tag{1.16}$$

The maximum efficiency for single junction solar cell is given by Equation 1.17,
Therefore, the schematic of Shockley-Queisser efficiency can be discovered in Figure 1.15[17].

$$\eta_{sj} = \eta_{ult} \eta_v FF \tag{1.17}$$

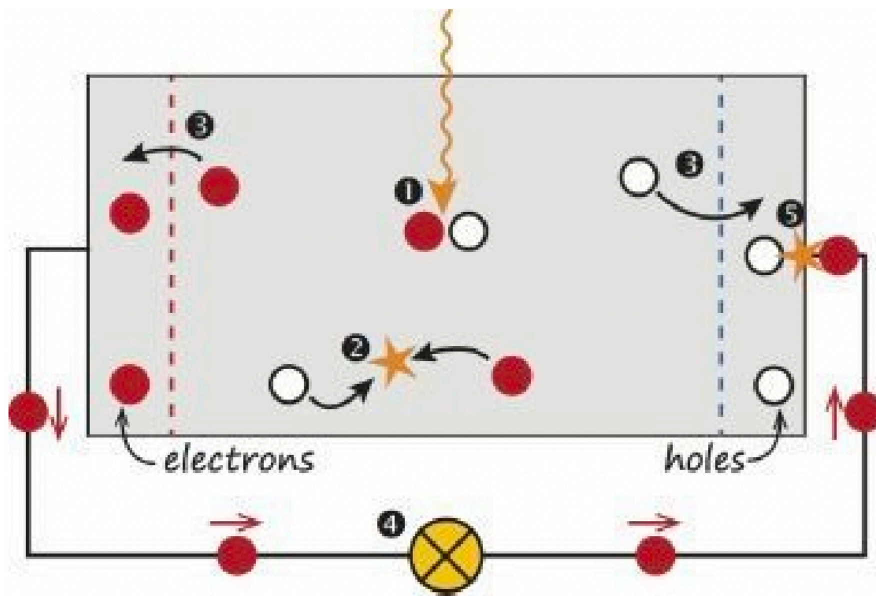


Figure 1.8: A very simple solar cell model.(1)Absorption of a photon leads to the generation of an electron-hole pair.(2)Usually, the electrons and holes will recombine.(3)With semipermeable membranes the electrons and the holes can be separated.(4)The separated electrons can be used to drive an electric circuit. (5)After the electrons have passed through the circuit, they will recombine with holes.[77]

Bulk recombination

Bulk recombination includes three different kinds of recombination, Radiative recombination, Auger recombination and Shockley-Read-Hall recombination.

Radiative recombination

Radiative recombination occurs when an electron in the conduction band recombines with a hole in the valence band and the excess energy is emitted in the form of a photon. Radiative recombination is thus the radiative transition of an electron in the conduction band to an empty state (hole) in the valence band.Radiative recombination is the recombination mechanism that dominates in direct bandgap semiconductors such as GaAs. However, Si is indirect bandgap material. Therefore, in Si, the radiative recombination can be considered negligible[33].

Shockley-Read-Hall recombination

In Shockley-Read-Hall recombination (SRH), also called trap-assisted recombination, the electron in transition between bands passes through a new energy state (localized state) created within the band gap by a dopant or a defect in the crystal lattice; such energy states are called traps.An electron can get trapped in this energy state, where it can recombine with a hole. Since traps can absorb differences in momentum between the carriers, SRH is the dominant recombination process in silicon and other indirect bandgap materials. However, trap-assisted recombination can also dominate in direct bandgap materials under conditions of very low carrier densities (very low level injection) or in materials with high density of traps such as perovskites[1][95].

The Shockley-Read-Hall recombination can be decided by Equation1.18 for holes and Equation 1.19 for electrons.

$$R_{SRH} = C_p N_T (p - p_0) = \frac{p - p_0}{\tau_{p,SRH}} \tag{1.18}$$

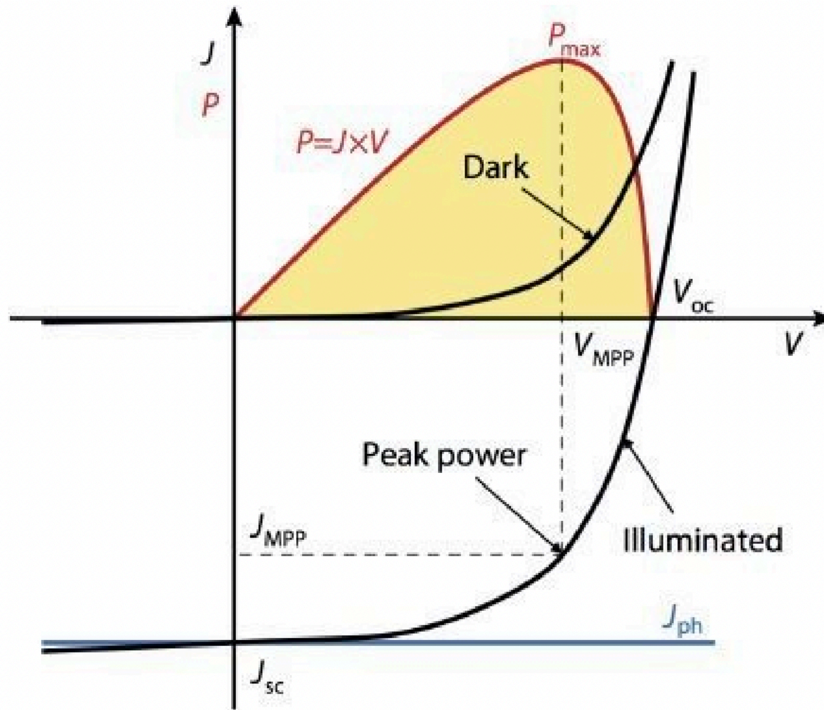


Figure 1.9: The *J*-*V* characteristics of a p-n junction in the dark and under illumination[77]

$$R_{SRH} = C_n N_T (n - n_0) = \frac{n - n_0}{\tau_{n,SRH}} \tag{1.19}$$

C_p is called the hole capture coefficient.C_n is called the electron capture coefficient. $\tau_{p,SRH}$ is the lifetime of holes in an n-type semiconductor. $\tau_{n,SRH}$ is the lifetime of electrons in an p-type semiconductor.N_T is the trap density. And p_0 is the hole concentration under thermal equilibrium. Finally, n_0 is the electron concentration under thermal equilibrium.

Auger recombination

Auger recombination is a non-radiative three particles process where the excess energy from the electron-hole recombination is transferred to electrons or holes that are subsequently excited to higher energy states within the same band instead of giving off photons (the radiative process).The Auger recombination is dominant in direct bandgap material such as Si [43][26].

Auger recombination rate can be decided by Equation 1.20.

$$R_{Aug} = R_{eeh} + R_{ehh} = C_n n^2 p + C_p n p^2 \tag{1.20}$$

As Auger recombination is a three particle process, the Auger recombination rate R_{Aug} strongly depends on the charge carrier densities for the electrons n and holes p. C_n and C_p are the proportionality constants that are strongly dependent on the temperature. R_{eeh} is dominant when the electrons are the majority charge carriers, while R_{ehh} is dominant when the holes are the majority charge carries. In strongly doped n-type silicon with a donor concentration N_D under low-level injection, it can be assumed that $n \approx N_D$ and hence that the eeh process is dominant. Similarly, for strongly doped p-type silicon with acceptor concentration N_A, it can be assumed that $p \approx N_A$ and hence the ehh process being dominant. As the Auger recombination under these conditions is proportional to the square of the doping levels, the more important it becomes, the higher the doping.

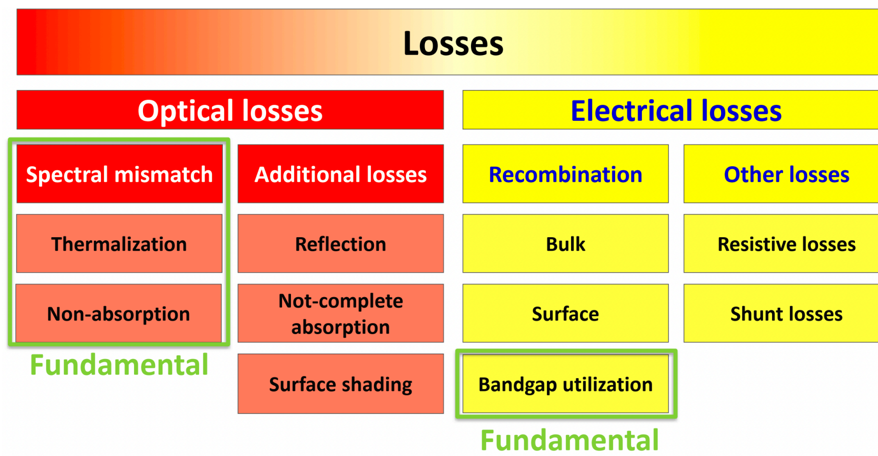


Figure 1.10: The loss mechanisms of solar cell[77]

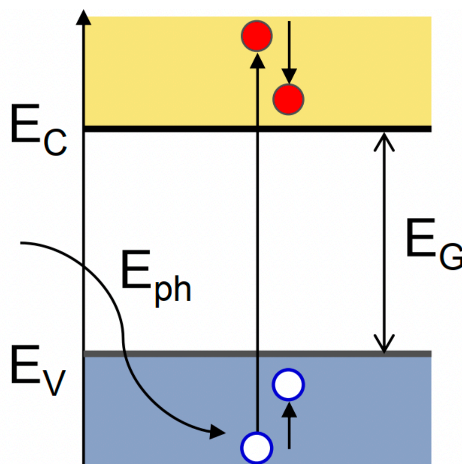


Figure 1.11: Schematic of thermallization losses of spectral mismatch losses[77]

The schematic of radiative recombination, Auger recombination and SRH recombination can be illustrated in Figure 1.16.

Surface recombination

At a silicon surface many valence electrons on the surface cannot find a partner to create a covalent bond with. The result is a so-called dangling bond, which is a defect that can be discovered in Figure 1.17. Due to these defects, many surface trap states are created within the band gap. These defects will also induce SRH recombination. In very pure semiconductors, recombination might be dominated by surface recombination.

The surface recombination rate R_s for an n-type semiconductor can be approximated with the following equation Equation 1.21,

$$R_s \approx V_{th}\sigma_p N_{ST}(p_s - p_0) \tag{1.21}$$

V_{th} is the thermal velocity in cm/s. N_{ST} is the surface trap density in cm^{-2}, and σ_{p} is the capture cross–section for holes in cm^2. p_{s} is the hole concentration at the surface and p_0 is the equilibrium hole concentration in the n-type semiconductor. For a p-type semiconductor, σ_{p} can be replaced by σ_{n}, p_{s} by n_{s}, and p_0 by n_0.

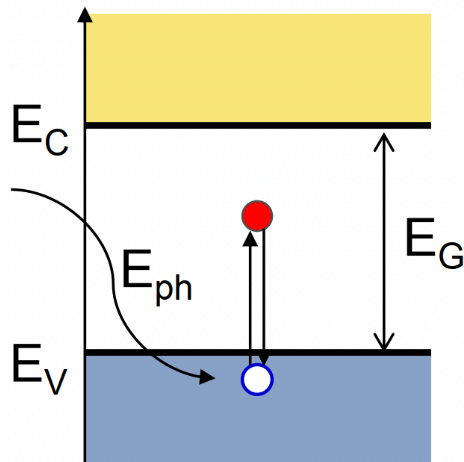


Figure 1.12: Schematic of non-absorption losses of spectral mismatch losses[77]

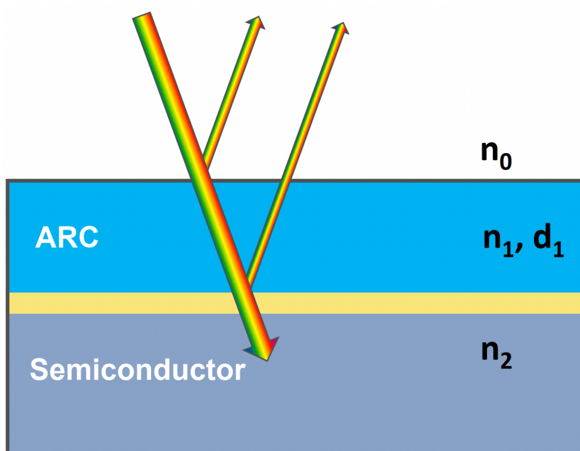


Figure 1.13: Schematic of anti-reflection coating to reduce reflection losses

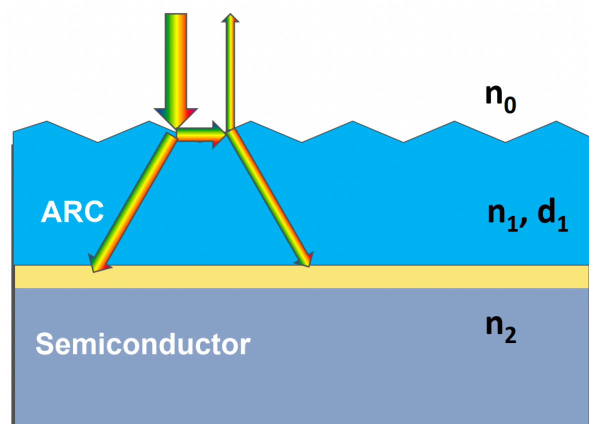


Figure 1.14: Schematic of texturing to reduce reflection losses

For high quality solar cells, it is crucial to have a low surface recombination velocity S_r, which can be achieved in two different ways: first, S_r can be made low by reducing the trap density N_{ST}. In semiconductor technology, N_{ST} can be reduced with passivation. Because of the thin layer on the surface, the valence electrons on the surface can form covalent bonds, such that N_{ST} is reduced. Secondly, the excess minority carrier concentration at the surface (p_s or n_s) can be reduced, for example by high doping of the region just underneath the surface in order to create a barrier. Because of this barrier, the minority carrier concentration is reduced and hence the recombination rate R_s [71][84].

Surface passivation

Chemical passivation

The chemical passivation reduced the dangling bonds and minimized the defect trap density N_{ST} at the surface or interface and thus reducing the surface recombination velocity and rate. The dangling bonds at the surface can be passivated by O atoms and also H atoms. It can be achieved by depositing passivating layer on the surface of the c-Si. For example, the surface dangling Si atom bonds can form Si-O bonds with the O atom in the thin passivating layer.This can largely reduce the surface recombination. Furthermore, after hydrogenation process, more Si atom dangling bonds can be passivated by H atom to form Si-H bonds that can further reduce the defect density at the surface and interface.

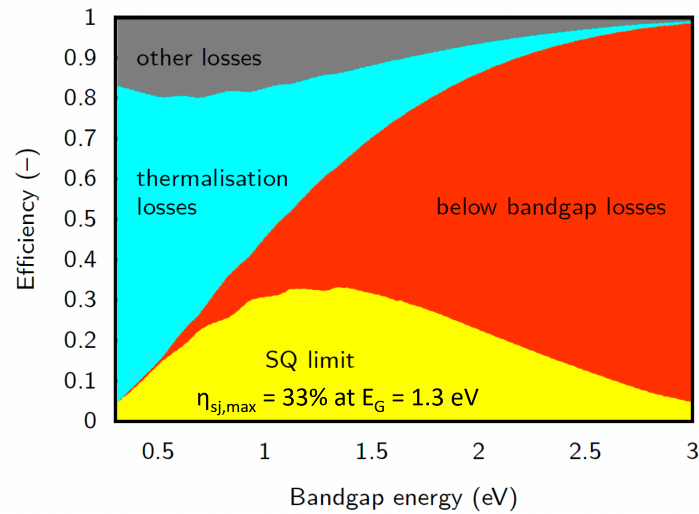


Figure 1.15: Schematic of Shockley-Queisser efficiency[77]

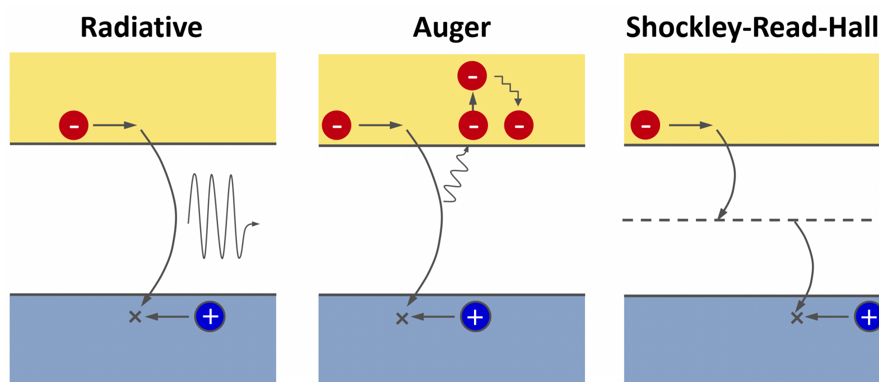


Figure 1.16: Schematic of Radiative recombination, Auger recombination and SRH recombination [77]

Field effect passivation

The field effect passivation reduced the surface recombination through reducing the excess minority carrier concentration (p_s or n_s) at the surface, for example by highly doping of the region in order to create a barrier. Because of this barrier, the minority carrier concentration is reduced and hence the recombination rate R_s is largely reduced at the same time. Field effect passivation is the formation of an internal electric field on the surface of the wafer by highly doped layers that induces majority charge carriers migration, at the same time blocking the migration of minority charge carriers to the interface. The additional highly doped layer, increases the concentration difference and the corresponding band bending between the majority charge carriers and minority charge carriers at the surface which can also be called carrier selective and thus reducing the possibility of the two carriers recombining at the interface. Apart from highly doped layer, the field effect passivation or the internal electrical field can also be achieved by adding the fixed charges like the positive charges in SiO_x and capping layer which are suitable to passivate n-type semiconductor and also the negative charges in capping layer AlO_x : H that are suitable to passivate the p-type semiconductor. In addition, by creating the work function difference like metal oxides MoO_x .etc dopants free passivation. In summary, the internal field effect and the induced band bending can attract majority charge carrier and repel minority charge carriers to reduce the surface recombination [36] ,[90] and [15].

As the development of solar cells, it is discovered that the recombination at the contact can not be ignored. Especially when the thin films contacting with metal can cause severe recombination losses that can be seen as the limit factor for the improvement of the efficiency of c-Si solar cells. Therefore, at first, it is found that there are a lot of metal-Si interface recombinations in the Aluminium BSF solar

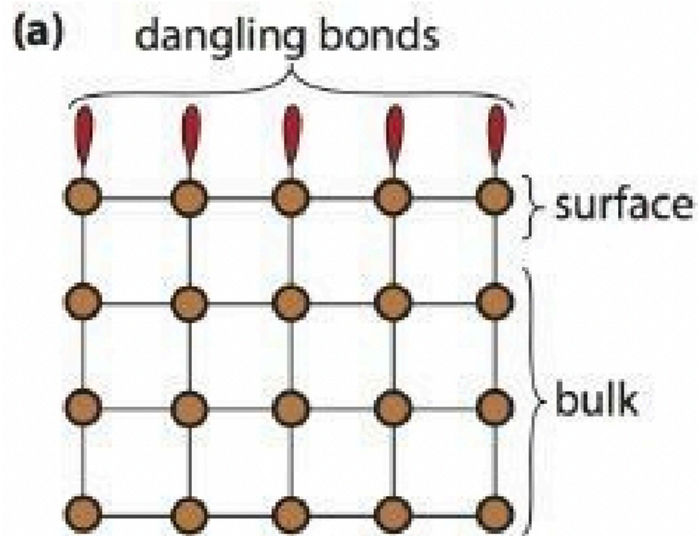


Figure 1.17: Illustrating dangling bonds (surface defects) on a semiconductor surface[77]

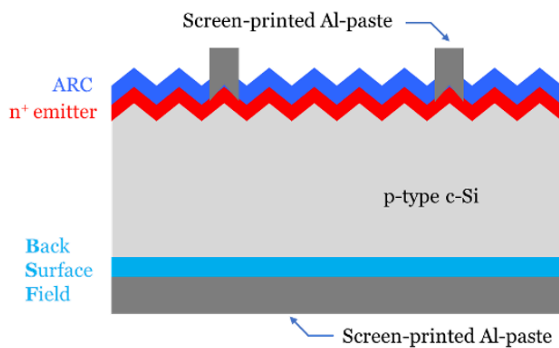


Figure 1.18: Simple schematic of Al BSF solar cell

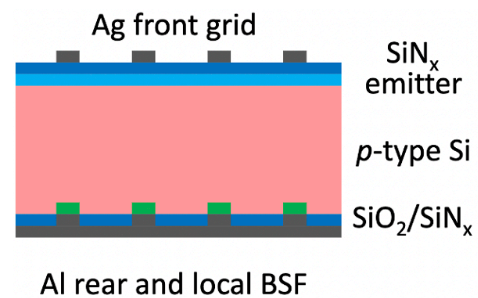


Figure 1.19: Simple schematic of PERC solar cell

cell that can be discovered in Figure 1.18. Then, in addition, the PERC solar cell is proven to be high efficiency. But, there also exist a few metal-Si interface recombinations in the PERC solar cell although it has local BSF which is illustrated in Figure 1.19. At the same time, the procedures for producing PERX solar cell seem very complicated that are required to be simplify. The carrier-selective passivating contacts can largely reduce the recombination losses at the contact with good passivation quality and in the meanwhile, it can also let Si contact with full area metal that largely reduce the complexity during producing. And it is also proven to be high efficiency.

Carrier-selective passivating contacts can largely minimize the interface defect density and without it, plenty of interface recombination will exist.The highest efficiency front-back contacted (FBC) solar cell has been completed by the TOPCon configuration with poly-Si contact[7]. It shows that TOPCon solar cell and the poly-Si(O_x) carrier selective passivating contacts have large potentials to be further explored and discovered. In this FBC TOPCon solar cell, the front side is p^+ emitter while at the rear side, n^+ poly-Si(O_x) passivating contact has been implemented contacting with full area metal back contact to collect charge carriers that can be seen in Figure 1.20. The bad passivation quality of p^+ poly-Si(O_x) passivating contacts especially on textured wafers decides that the front side can just be p^+ emitter for pursing high efficiency solar cells. The p^+ poly-Si(O_x) on flat surface have better passivation quality. However, if p^+ poly-Si passivating contact is located at front side, the optical properties and parasitic absorption will become big problems. Therefore, the exploration on improving the passivation quality of p^+ poly-Si passivating contact on textured surface is still undergoing.

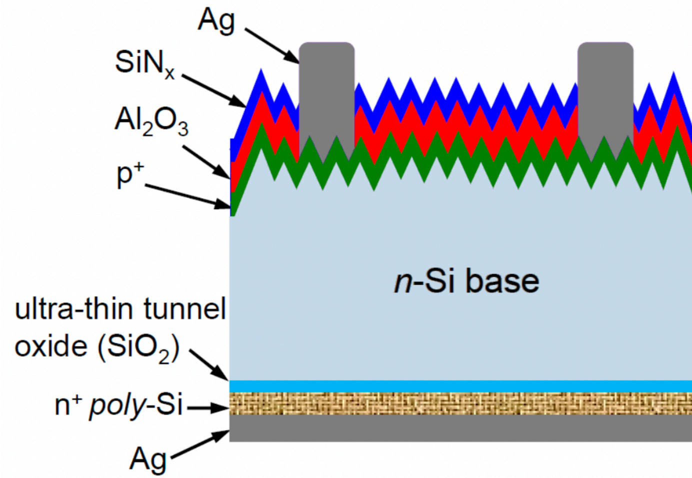


Figure 1.20: FBC solar cell with TOPCon configuration [81]

Resistive losses and Shunt losses

The single-diode solar cell model is illustrated in Figure 1.21. The series resistance R_s can be result of the bulk resistance of semiconductor, the bulk resistance of metal electrodes and the dominant contact resistance between semiconductor and metal. The influences of R_s can be seen in Figure 1.22. From the figure, it can be discovered that the larger the series resistance is , the worse the I-V characteristic of the solar cell is. The shunt resistance R_p can be result of leakage across P-N junction around the edge and crystal defects, pinholes, impurity precipitates. The influences of R_p can be seen in Figure 1.23. From the figure, it can be discovered that the larger the shunt resistance is , the better the I-V characteristic of the solar cell is. Therefore, the series resistance ought to be as small as possible and the shunt resistance should be as large as possible.

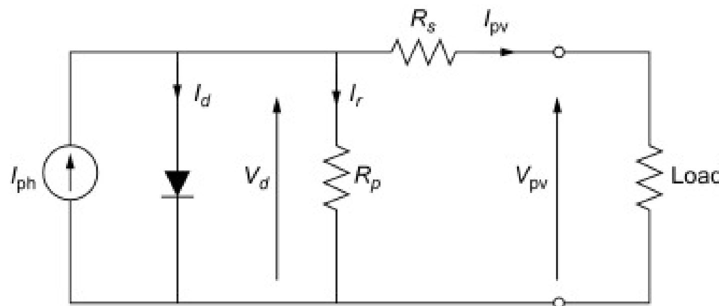


Figure 1.21: Single-diode model of solar cell

Then, finally, considering all the losses mentioned above, the efficiency η of the solar cell is given by the following formula Equation 1.22, as illustrated in Figure 1.24.

$$\eta = \frac{E_G \int_0^{\lambda_G} \Phi(\lambda) d\lambda}{\int_0^{\lambda_G} P(\lambda) d\lambda} \times \frac{\int_0^{\lambda_G} P(\lambda) d\lambda}{\int_0^{\infty} P(\lambda) d\lambda} \times \frac{A_f}{A_{tot}} \times (1-R) \times \eta_g IQE_{op} \times IQE_{el} \times \frac{qV_{OC}}{E_G} \times FF \tag{1.22}$$

1.3. poly-Si(O_x) passivating contacts

1.3.1. Surface formation

The surface of c-Si absorber can be polished or textured. The poly-Si(O_x) passivation quality on flat can be better. However, the reflection on flat surface can be very large which may do harm to the efficiency

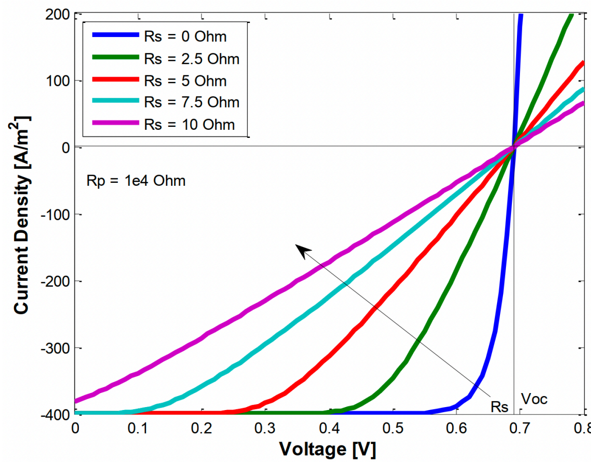


Figure 1.22: The influences of series resistance R_s on the I-V characteristics of solar cell

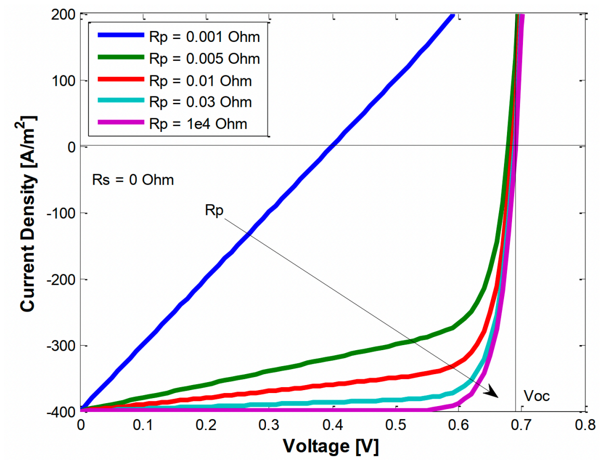


Figure 1.23: The influences of shunt resistance R_p on the I-V characteristics of solar cell

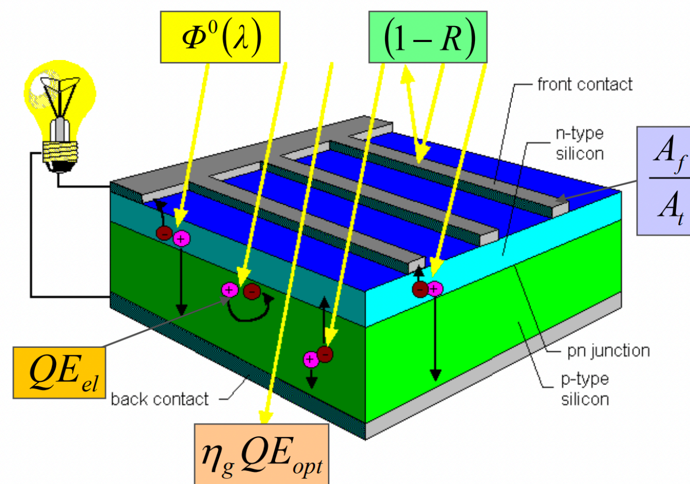


Figure 1.24: Simple schematic of all the solar cell losses

of the solar cell. Therefore, to increase the optical performance and light traping of the cell, the surface can be textured by tetramethyl ammonium hydroxide (TMAH) and potassium hydroxide (KOH) to prepare inverted pyramids on the surface. It is found that TMAH solution has higher undercut rate and lower <100> plane etch rate than KOH solution, and the <111>/<100> etch rate ratio of TMAH is two to three times that of KOH solution. Additionally, etch rate of SiO_x mask is an order of magnitude lower in TMAH than in KOH. Besides, surface morphology analysis indicates that TMAH etching can obtain much higher quality inverted pyramids of sharp vertex, smooth <111> sidewall and uncontaminated surface than KOH etching, which makes TMAH etching samples show better anti-reflection properties [18]. It reveals that TMAH is more attractive for the preparation of inverted pyramids than KOH. But TMAH can bring more organic contaminations to the c-Si wafers.

Rounding and smoothing of pyramidal structures is an imporant part to decrease the defect densities at the c-Si surface after texturing. Through immersing the samples in an anisotropic poly-Si etching solution which consists of HF and HNO_3, the sharp pyramids will be smoothed.

1.3.2. Interfacial oxides

In most cases, the poly-Si(O_x) carrier selective passivating contacts are composed of c-Si/ultra-thin SiO_x/doped poly-Si(O_x) stack. The ultra-thin SiO_x layer firstly induced Si-O bonds and therefore form-

ing chemical passivation on the dangling bonds on the c-Si surface. The defective trap density at the c-Si surface is largely reduced by adding the ultra-thin SiO_x layer on top of the c-Si bulk. In addition, the interfacial tunnelling oxide ultra-thin SiO_x layer can create the potential barrier for charge carriers. On one hand, it can prevent the in-diffuse of the dopants from the highly doped poly-Si(O_x) layer which can cause large Auger recombination at the c-Si bulk layer. On the other hand, the charge carriers can also transport through the interfacial oxide SiO_x layer to transport to the doped poly-Si(O_x) layer for the following carriers collection.

There are generally three methods for the charge carriers to transport through the ultra-thin SiO_x layer. The first one is tunnelling through oxide barrier[27]. The second one is tunnelling assisted by pinholes[13]. The last one is exclusively via pinholes[70][61]. Different SiO_x thickness can induce different carriers transporting approaches. Charge carriers can tunnel through SiO_x layer with thickness less than 2 nm[27]. When the thickness of SiO_x is betwwen 2 nm and 2.2 nm, the transport of charge carriers can be assisted by pinholes[13]. However, when thickness of SiO_x is over 2.2nm, it can only transport exclusively by pinholes[61]. The existence of pinholes in SiO_x can help the transport of charge carriers that can decrease the contact resistance. Increasing the post deposition annealing thermal budget, the pinhole density will increase and at the same time, pre-annealing approach before doping layer deposition can also help open more pinholes.However, at the same time, it can also increase the recombination current density especially, intensify the Auger recombination which can degrade the passivation quality of TOPCon. The degradation of passivation is caused by the diffusing of dopants from the highly-doped poly-Si(O_x) layer to the c-Si bulk. Thus, the pinholes can seem as defects in SiO_x layer which is required to be finely tuned the balance between the advantages for reducing resistive losses and the drawbacks for increasing the recombination losses. Generally, for a thicker SiO_x layer solely quantum mechanical tunnelling can't provide sufficient carrier transport channels and due to which series resistance value gets increased. This resulted in obtaining lower FF. However, too much transportation of charge carriers through pinholes resulted in lowering down the cell performance. Therefore, the pinhole density and pinhole size should be optimized[29]. In addition, the thickness of interfacial layer SiO_x can also not be too thin that can influence its function as potential barrier. In summary, the thickness of SiO_x layer is essential for carriers transporting which is required to find an optimum value. Actually, there are plenty of approaches to process the ultra-thin SiO_x layer like thermal oxide (t-SiO_x), nitric acid oxidation of silicon (NAOS), plasma assisted N_2O oxidation (PANO), UV/O_3, et al[31].

1.3.3. poly-Si(O_x) thin films

The high doping density in the poly-Si(O_x) layer induce a sharp diffusion profile at the c-Si surface mainly providing field-effect passivation. For example, for n^+ poly-Si(O_x) carrier selective passivating contacts, the dopants utilized are Phosphorous and the doping profile of the n^+ doped layer is high which can form the internal electrical field. In addition, the large P dopants concentration of the n^+ poly-Si(O_x) layer and interfacial tunnelling oxide layer can cause the band bending. Thus, the n^+ doped layer can repel the minority charge carriers, in this case, holes ,and attract the majority charge carriers, in this case, electrons.Through this field effect passivation, the recombination of electrons and holes are largely reduced. The simple schematic of the charge carriers transporting in n^+ poly-Si(O_x) carrier selective passivating contacts can be discovered in Figure 1.25. However, the doping profile of the doped poly-Si(O_x) layer is required to be finely optimized and balanced since too many dopants can cause the dopants diffuse into c-Si bulk and intensify the Auger recombination at c-Si bulk. In the meanwhile, since boron structually has higher diffusion coefficient than phosphorous because of smaller volume, boron is more prone to diffuse into c-Si bulk. Therefore, p^+ poly-Si(O_x) carrier selective passivating contacts generally has worse passivation quality[22][10].

The doped a-Si(O_x):H layer can be achieved by several fabrication processes such as low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD), thermal diffusion (BBr_3 and $POCl_3$)and ex-situ ion-implantation,etc. Ion implanted doped poly-Si layer. Plasma enhanced chemical vapor deposition and low pressure chemical vapor deposition techniques are widely used for the development of a-Si layer or a-Si:H layer and different types of impurities into this a-Si or a-Si:H layer may be introduced by two processes, namely in-situ doping [29],[68],[19](where

different types of doping gases such as PH_3 for n poly-Si and B_2H_6 or $B(CH_3)$ for p poly-Si are added during the growth process) and ex-situ doping (ion-implantation) [20],[67],[29]. Atmospheric pressure chemical vapor deposition (APCVD) was found to be another suitable way to develop intrinsic or doped poly-Si layer [50],[55],[29]. Physical vapour deposition (PVD) techniques such as sputtering were also used for the development of doped silicon layer [88],[29].

The thickness of a-Si(O_x):H layer and doping concentration can have influences on passivation quality. Feldmann et al. observed that an enhancement in free carrier absorption (FCA) at heavily doped poly-Si layer due to the increment of the doping concentration and thickness of poly-Si layer may play a vital role in the reduction of short-circuit current density of TOPCon solar cells [21],[29]. It concludes that the thickness and doping concentration of doped poly-Si layer should be kept as low as possible to minimize the free carrier absorption loss. However, it is also suggested that the doping level of doped poly-Si layer should not be decreased beyond 1.0×10^{20}cm^{-3} so that the contact resistivity value can be kept as low as possible. In addition, the study revealed that the surface passivation quality was not found to be severely affected due to the decrement of the thickness of poly-Si layer, given the minimum thickness of 15 nm is maintained. But such thin layers may not be able to resist the penetration of Ag pastes into it during the screen printing and firing process and hence, degradation in the passivating quality may be realized. Therefore, it is also suggested that a proper balance should be maintained among different parameters such as passivating quality, contact resistivity and free carrier absorption losses during the design of poly-Si/SiO_x contacts. Besides, high sheet resistance for thinner poly-Si films and concurrently, limitations of achieving short-circuit current density of beyond 40 mA/cm^2 for thicker poly-Si films are also one of the major concerns[29].

The different alloys with poly-Si can also have influences on the passivation. Blisters are generally formed due to the accumulation of hydrogen content at the interface of SiO_x and doped a-Si:H layer. Formation of blisters can be responsible for the degradation of the passivating quality of the TOPCon structure since it introduces inhomogeneity inside the film morphology. Lin et al. claimed that use of PECVD coated carbon-doped poly-Si layer instead of doped poly-Si layer to form the TOPCon structure might be suitable approach to restrain the effect of blistering [45],[29] since it can form C-H bonds which in turn reduced the possibility of H effusion from the passivated contacts during high temperature thermal treatment. Finally, poly-Si CSPCs are not transparent, especially when heavily doped, because of the high free carrier absorption. However, materials such as poly-SiO_x is utilized as CSPCs for solar cells. They exhibit high thermal stability. At the same time, they are more transparent than the poly-Si material due to their larger bandgap, stronger band bending which can largely reduce the parasitic absorption and improve the field effect passivation[90][54].

1.3.4. Crystallization

In addition, the post deposition annealing is crucial for cystallization to poly-Si(O_x), dopants diffusion and dopants activation. However, involvement of such high temperature annealing step undoubtedly increases the thermal budget during the fabrication of the solar cells. Through increasing the post-deposition annealing thermal budget, the dopants diffuse more into c-Si bulk, the contact resistivity may become better but at the same time, the Auger recombination can become severer that can have negative influences on the passivation quality. Therefore, the different annealing conditions in tube furnace are also very crucial for the shape of doping profile which are required to be optimized and balanced. Another approach to change amorphous silicon to poly silicon is through rapid thermal annealing. The study revealed that RTA method took very low time of about 15 minutes for the whole crystallization process where as more than 60 minutes was needed in conventional tube furnace annealing process for the same purpose. Besides, no blistering during the thermal treatment was observed when the thickness of a-Si:H layer was less than 40 nm[29]. But the passivation quality provided by RTA process was found to be slightly inferior to the passivation quality realized by using conventional tube furnace annealing process. However, a post-annealing treatment of hydrogenation with ALD coated AlO_x:H capping layer resulted in a significant improvement of the surface passivation quality of RTA processed samples[29].

1.3.5. Hydrogenation

The post-crystallization treatment is mainly a process of hydrogenation which may be realized by several ways such as treatment in remote hydrogen plasma [52],[53],[29], forming gas annealing at moderate temperature [78],[64], [47],[29]and deposition of hydrogen containing layer like ALD AlO_x:H capping layer and PECVD SiN_x:H capping layer or their stacks onto doped poly-Si layer [29].During high temperature annealing, the hydrogen may diffuse out of c-Si bulk surface. The hydrogen can provide important chemical passivation on the surface defect density and dangling bonds by the forming of Si-O bonds which can be illustrated in Figure 1.26. Thus, the effusion of hydrogen is bad for the passivation quality. Therefore, a hydrogenation process is also very crucial for improving the passivation quality and reducing the defect density at the surface.This is generally be done by forming gas annealing (10% H_2 in N_2) 400°C duration for 30 minutes and ALD AlO_x and PECVD SiN_x:H capping layers or combination of them within PVMD group.

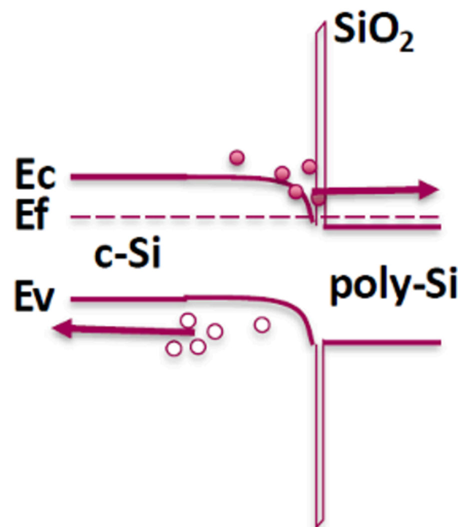


Figure 1.25: Simple schematic of charge carriers transporting in n^+ poly-Si(O_x) carrier selective passivating contacts

Figure 1.26: H,O chemical passivation

1.4. Application in c-Si solar cells

1.4.1. Metallization

In the solar photovoltaic industry, screen printing and then co-firing method using for making contact pattern accounts for majority of the metallization processes for silicon wafer solar cells. Screen printing is simply using stencil to reproduce the same print over and over again. Screen printed solar cells are the finest established, most mature technology of solar cell fabrication.The main advantage of screen

printing process is the relative simplicity. But generally, the quality of the metallization is worse than copper-planting and aluminium lift-off with larger surface shading due to thicker fingers and worse uniformity of the metal grids [40].

The other metallization technique that is widely utilized in the lab is the copper-electroplating process.It is processed by redox reaction which includes the transfer of electrons between two electrodes and an electrolyte solution copper sulphate.The wafer is placed at the cathode and the copper plates at the anode. The copper at the anode will dissolve in the electrolyte and will be deposited on the wafer surface at the cathode. This technique can provide better quality metallization with lower surface shading at room temperature due to smaller metal finger width can be achieved. The smaller finger width can induce higher short circuit current density. In addition, the smaller series resistance can also be expected. Therefore, with copper planting, the efficiency of the solar cells can be improved. However, before copper-electroplating, the opening patterns of the metal grids are required to be done by photolithography which is very expensive and complex. And the adhesion of copper is not so good which needs metal such as Ag seed layer evaporation before photolithography which adds the price and complexity. In addition, after electroplating, the photoresist used for photolithography and metal seed layer need to be removed. Thus, copper-planting can not be widely used in industry even though it can improve the efficiency of c-Si solar cells.

In this thesis, another metallizaiton process, aluminium lift-off is utilized. This approach has almost the same processes as copper-plating. But here, the metal seed layer is not required. In addition, aluminium is deposited by electron beam evaporation which can be easier than copper-electroplating. Then, the excess photoresist and aluminium can both be removed by ultrasonic bath filled with acetone. Al lift-off is also very expensive and complicated for industry. But in lab, it can improve the efficiency of the solar cell and have fewer steps then copper-plating. Therefore, in this thesis project, Al lift-off metallization method is used.

1.4.2. Solar cells

Power loss analysis

Typically, for TOPCon based solar cells. The main losses can attribute to surface recombination, Auger recombination in the bulk induced by dopants diffusing, TCO sputtering damage, metal-induced recombination during metallization process, the surface shading when utilizing Ag paste screen painting for metal grid contacting, the parasitic absorption and free carrier absorption of poly-Si thin films. The surface recombination can be dealt with chemical passivation and field effect passivation through further optimizing the passivation quality of poly-Si(O_x) passivating contacts. The Auger recombination can be reduced by optimize the doping profile and the post deposition annealing conditions. TCO sputtering damage can be reduced by optimize the recovery conditions or utilizing thick poly-Si(O_x) passivating contacts with enough lateral conductivity. The parasitic absorption of poly-Si thin films can be reduced by alloying with other elements like oxygen or carbon to increase the band gap and increase the transparency of the thin films. All these methods are discussed in this thesis project.

1.5. Motivation and objectives

1.5.1. Motivations

Why poly-Si(O_x) carrier selective passivating contacts?

The carrier selectivity means it allows one kind of charge carriers to transport but block the other carriers[92]. This function can be done by surface carrier modulation by low/high work function material such as metal oxides, heterojunction formation with wide bandgap material such as silicon heterojunction (SHJ), tunnelling/transport barrier with interfacial tunnelling oxide and highly-doped layer, finally, standard heavily doping layer like in PERL solar cell[49]. Actually, both SHJ and poly-Si technologies have recently led to a world record, >26% IBC solar cells[92]. CSPCs based on metal oxide layers, are also rapidly emerging and enable efficiencies beyond 22%[89]. However, there are still restrictions that limit the applications of such materials. Firstly, limited transparency and thermal instability are existed in SHJ cells. Secondly, metal oxides are transparent, but standard high-thermal budget metallization influ-

ences their work function and thus, their carrier selectivity. Finally, poly-Si CSPCs are not transparent, especially when heavily doped, because of the high free carrier absorption. However, materials such as poly-SiO_x is utilized as CSPCs for solar cells. They exhibit high thermal stability. At the same time, they are more transparent than the poly-Si material due to their larger bandgap, stronger band bending which can largely reduce the parasitic absorption and improve the field effect passivation[90][54].

Why p^+ poly-Si(O_x) TOPCon?

p^+ poly-Si(O_x) passivating contact might be used in double-side TOPCon solar cells by replacing the B-diffused emitter. And it can also upgrade the PERC production line which uses the same front phosphorous diffused emitter and only changes the backside procedures with a limited modification that is a great significance for industry. Furthermore, boron has higher diffusion coefficient than phosphorous which means that boron has structurally less passivation quality. Therefore, p^+ poly-Si(O_x) passivating contacts can be more challenging and very essential for bifacial solar cells. However, at the same time, not so much research is proposed concerning on this topic because it has more challenges while n^+ poly-Si(O_x) passivating contact is almost well optimized and is very mature in industry. Therefore, p^+ poly-Si(O_x) TOPCon is chosen to be researched.

Why PECVD p^+ doping layer?

PECVD can have single-side deposition which can tune layer's properties through doping with additional elements like carbon or oxygen. In addition, it is processed under high temperature that is essential for industry. Moreover, with LPCVD, the wrap-round induced damage of quartz furnaces and quartz carriers can be a problem. Finally, PECVD can promote in-situ process which is more convenient [45].

1.5.2. Objectives

Solar cell is crucial and vital sustainable energy technology which is widely used. TOPCon as a passivating contact enables record high efficiency, >26%, c-Si solar cells. PECVD is a candidate for the preparation of TOPCon passivating contact with the advantage of in-situ doping possibility and single-side deposition. In this project, PECVD approach is used to prepare the most challenging p^+ TOPCon for high-efficiency solar cells. During this project, the research objectives involved include:

- Studying the influences of process parameters of the different tunnelling oxides (NAOS-SiO_x, thermal SiO_x, PANO-SiO_x) on the SiO_x properties and their influences on the carrier selectivity of p^+ TOPCon passivating contacts.
- Studying the influence of the doping of the deposited p-type Si layer and the interfacial intrinsic layer on the carrier selectivity of p^+ TOPCon passivating contact.
- Studying the impact of metal-induced recombination current density $J_{o,\text{metal}}$ of the TOPCon structure.
- Engineering the hydrogenation processes for the optimum passivation quality of p^+ TOPCon passivating contact.
- Integration of the developed PECVD p^+ TOPCon passivating contacts into c-Si solar cells.

1.6. Thesis outline

In chapter 1, the introduction is given like solar cell principle and loss mechanisms as well as the background of the poly-Si(O_x) carrier selective passivating contacts. In chapter 2, the introduction of the experimental methods and process techniques are given. Then, the main parts of the thesis contains four different parts. Firstly, in chapter 3, the experiments are focused on optimization of the PECVD

p^+ poly-Si(O_x) carrier selective passivating contacts which mainly includes the influences of interfacial silicon oxide layer, the influences of intrinsic layer and the optimization of PECVD p^+ doping layer and also some improvements on the hydrogenation process. Next, in chapter 4, the contact properties of p^+ poly-Si(O_x) passivating contact like contact resistivity and metal-induced recombination current density are characterized and given. Then, in chapter 5, the passivation on p^+ emitter is carrier out for the following fabrication of i-TOPCon solar cell. At the same time, the electrical performance and results of two different solar cell structures : i-TOPCon solar cell with p^+ emitter as front side and n^+ poly-Si(O_x) passivating contact as rear side, also poly-poly solar cell with n^+ poly-Si(O_x) passivating contact as the front surface field and p^+ poly-Si(O_x) passivating contact as rear side. Finally, in chapter 6, the conclusions and some outlooks for the following researchers of the thesis are given.

2

Experimental methods and Process techniques

In this chapter, the main utilized process and characterization methods and equipments are introduced. The process techniques are from cleaning, texturing to poly-Si(O_x) carrier selective passivating contacts formation and metallizaiton.

2.1. Fabrication process

2.1.1. c-Si absorber

Flat surface

In this thesis, the utilized flat wafers are phosphorous doped n-type crystalline silicon float zone (FZ) wafers manufactured by TOPSIL. The details of the wafers are shown in table Table 2.1.

Table 2.1: TOPSIL n-type FZ c-Si wafers details and properties

Parameters	Values
Dopant	Phosphorous doped n-type
Orientation	<100> or <111> $+/-1°$
Thickness	$280 \pm 20 \mu m$
Diameter	99.7-100.3 mm
Resistivity	$1-5\Omega \cdot cm$
Method	float zone (FZ)

Wafer standard cleaning

The nitric acid wet chemical standard cleaning of wafers mainly contains two steps. Firstly, the wafers are immersed into 99% $HN0_3$ for 10 minutes at room temperature aiming at removing organic contaminations followed by 5 minutes DI water rinsing. And then the wafers are immersed into 69.5% HNO_3 at 110 °C to remove the inorganic metal ions contaminations for 10 minutes also followed by 5 minutes DI water rinsing and then drying with spin dryer. However, after nitric acid standard cleaning, a thin nitric acid oxidation of silicon (NAOS-SiO_x) will be grown on the surface of wafers. In addition, the wafers have native oxide layer when contacting with atmosphere. Therefore, the wafers are required to be immersed into HF 0.55% to etch and remove the above mentioned chemically grown oxide and native oxide with the duration for 4 minutes until both sides are hydrophobic and then rinsing into DI water for about 5 minutes followed by drying. Or Si Marangoni process at EKL can be utilized because of isopropyl alcohol (IPA) that can dry the wafers. Then, with Marangoni, the wafers are no need to be transferred to DI wafer bath for rinsing and then spin dryer for drying which can be more convenient.

Wafer texturing

The double side polished (DSP) n type c-Si wafers are required to be textured to increase the optical performance. Texturing is processed in alkaline solutions. The dose of KOH is 105 grams dissolving in 5 liters DI water. The method utilized for heating is water bath approach. The temperature is setting at 82 °C. And after texturing, the wafers are required to rinse in HCl bath as soon as possible. Otherwise, the KOH residues will appear on the textured wafer surface. The concentration of the HCl bath is 0.20% which can be made by 25 milliliters 40% HCl utilizied at EKL dissolving in 5 liters DI water. During texturing, the organic additive monoTEX H 2.4 is required to add into the alkaline solutions.

Firstly, the wafers are loaded into the cassettes. Then, the wafers are rinsed in DI water for about 10 seconds. Next, the wafers are immersed into the alkaline solutions with additive for about 8 minutes at 82°C. Here, the texturing assisted organic additive is required to add into the alkaline solution when the water bath sink approaching about 80°C. After texturing, the wafers are required to immersed into 0.20% HCl bath for 2 minutes as soon as possible to remove the possible KOH residues. Then, finally, after that, the textured wafers are rinsed with DI water for about 5 minutes and then loaded into the spin dryer. If more wafers are needed to do the texturing process at the same time, the adding dose of KOH is 0.8 grams KOH per wafer and the adding dose of additive is 0.5mL monoTEX H 2.4 per wafer. After texturing, the wafers are needed to be immersed into 99.9% HNO_3 at room temperature to remove the possible organic contaminations and then to finish the standard nitric acid wet chemical standard cleaning process at CR100.

Next, after standard cleaning, the textured wafers are required to be immersed into poly-Si etch solution which consists of 40%HF and 69.5% HNO_3 with the ratio 1:40 at CR100 for 2 minutes to smooth the pyramids. After poly-Si etch, the nitric acid wet chemical standard cleaning and corresponding rinsing and drying processes are also needed.

2.1.2. Passivation samples preparation

SiO_x formation

The thin interfacial tunneling oxide layer utilized as potential barrier can be formed by three methods in this thesis. Firstly, nitric acid oxidation of silicon (NAOS), where the oxide is formed in 69.5% HNO_3 at room temperature. The nitric acid reacts with the silicon and forms an oxide layer at the surface. After immersing the wafers into 69.5% HNO_3 for about 60 minutes, the obtained oxide thickness is around 1.5 nm[90] and [89].

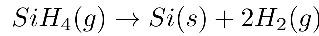
In addition, the second method is thermal oxidation (t-SiO_x), where the oxidation of silicon is initiated in an oxygen-rich atmosphere at elevated temperatures. Here the oxygen binds directly with the silicon to form a ultra-thin SiO_x layer at the surface. Normally, within PVMD group, the thermal oxidation process is performed at 675°C for 3 minutes in TEMPRESS tube furnace C1. At first , the furnace temperature ramps to 675°C in the nitrogen atmosphere. Then, after that, the oxygen is fed into the chamber to induce an oxidation reaction at the c-Si surface duration for 3 minutes with nitrogen volume 6.0 SLM and oxygen volume 0.6 SLM. This will create a SiO_x layer with thickness of approximately 1.3 nm that is measured by by Spectral ellipsometry.

Next, the third method is plasma assisted N_2O oxidation (PANO) fabricated by plasma-enhanced chemical vapor deposition (PECVD) *AMOR*.More details of PECVD will be given in the next sections. The utilized recipe during PECVD is : RF power=1.5w, deposition gas=N_2O with corresponding volume 50 sccm, deposition pressure=0.08 mbar, and deposition duration=9 minutes on flat surface. The expected silicon oxide thickness is also 1.3 nm after 9 minutes deposition.

Low pressure chemical vapor deposition equipment

The simple schematic of TEMPRESS tube furnace LPCVD system is shown in Figure 2.1 and [3]. In this project, it is used to deposit intrinsic a-Si:H layer on both sides. Firstly, the tube is evacuated and when the pressure reaches the tuned value, the tube starts heating up to the deposition temperature

to enable the precursor gas decomposition.



$$SiH_4(g) \rightarrow Si(s) + 2H_2(g)$$

The chemical reaction in the reactor is high thermal driven. The temperature is utilized 580°C and the pressure at about 150 mTorr. The recipe used during LPCVD has a deposition rate of around 2-2.2 nm/min. After deposition, the wafers are annealed at 600°C for 60 minutes to release the stress.Low pressure chemical vapor deposition (LPCVD) technique can result in a pure and high uniformity as well as denser layer because of the low pressure and long deposition time [79]. In addition, LPCVD can process a lot of wafers in one batch at one time.

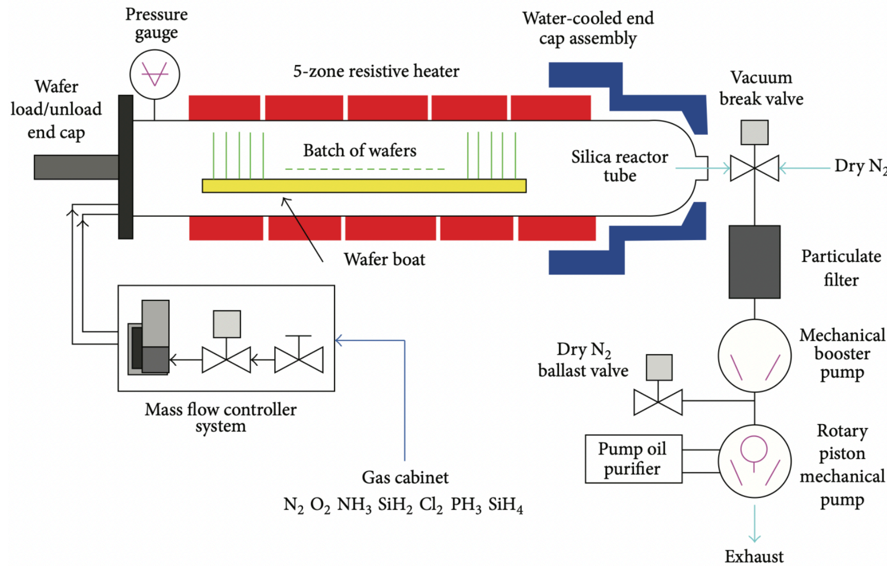


Figure 2.1: Simple schematic of LPCVD equipment

Plasma enhanced chemical vapor deposition equipment

Unlike LPCVD tube furnace, PECVD works at a lower temperature. And a rapidly oscillating magnetic field with radio frequency (RF) is applied between the two electrodes or between the electrode and the chamber wall. The molecules in the precursor gas can obtain energy from the RF oscillating magnetic field and dissociate into ions so that high energy plasmas are ignited in the chamber. With plasma presented, the energetic ions could provide energy to the reaction.Then, the charged ions are pushed by the electric field and react with the substrate which is attached on one electrode and form thin films on the wafers. The other electrode or chamber wall is also very essential for the deposition. The simple schematic sketch of PECVD equipment can be seen in Figure 2.2.

The PECVD utilized in this thesis is AMOR PECVD. It has silane (SiH_4), carbon dioxide (CO_2), methane (CH_4), hydrogen (H_2), phosphine (PH_3) and diborane (B_2H_6) as gas precursors and argon (Ar) gas for purge. The n-type doped layer deposition is done in chamber 2 with gas precursors silane (SiH_4), carbon dioxide (CO_2), hydrogen (H_2) and phosphine (PH_3). While p-type doped layer deposition is processed in chamber 1 with gas precursors silane (SiH_4), carbon dioxide (CO_2), hydrogen (H_2) and diborane (B_2H_6).Chamber 5 can be used to flip the wafers to the other side without breaking the vacuum in the chamber. In addition, before deposition, the wafers are required to preheat for at least 15 minutes to make them reach a stable temperature at around 180 °C. And the PECVD process can be influenced by RF power, deposition pressure, substrate temperature, deposition gas flow, deposition time and so forth.

Apart from AMOR, in this thesis, the Oxford instruments Plasmalab System 100 PECVD at Kavli nanolab and Novellus PECVD in EKL are also be used. Oxford instruments Plasmalab System 100 PECVD at Kavli nanolab is used to deposit SiN_x:H capping layer for hydrogenation and as anti reflection coating (ARC). The deposition gas precursors are ammonia (NH_3), silane (SiH_4) and hydrogen (H_2) with substrate tempertaure at 400 °C. While Novellus PECVD at EKL also deposit at 400 °C acting as the protective layer when fabricating i-TOPCon solar cell and also be used to protect the rear side of the wafers during single side texturing process.

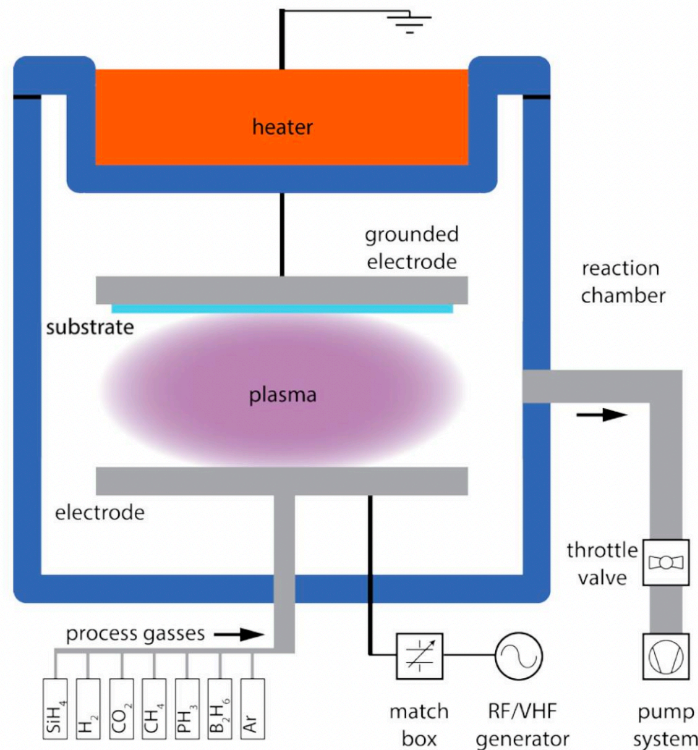


Figure 2.2: Simple schematic of PECVD equipment

Annealing process

In this thesis, there are mainly two annealing processes both in TEMPRESS tube furnace. After deposition, the wafers are required to load into tube furnace for high temperature annealing to activate the dopants and help them diffuse as well as cystallization a-Si(O_x):H thin films to poly-Si(O_x):H thin films in N_2 atmosphere. The post deposition annealing (PDA) conditions are required to be fine tuned to provide suitable doping profile and at the same time prevent from too many dopants diffusing into c-Si bulk that can cause large Auger recombination.

The other annealing process is forming gas annealing (FGA) process after SiN_x:H capping layer deposition. The annealing condition is normally 400 °C which is the same as the substrate temperature depositing SiN_x:H duration for 30 minutes. And forming gas is 10% H_2 in N_2. The FGA process is crucial for n^+ poly-Si(O_x) carrier selective passivating contacts.

2.1.3. Solar cells fabrication

Ion implantation equipment

The ion implantation equipment is utilized to process p^+ emitter at front side for i-TOPCon solar cell with boron ion-implantation. This process is done at France with the implantation energy 20 keV and doping dose $5.0 \times 10^{14} cm^{-2}$ during boron implantation to form the boron doping profile. Ions are avail-

able in the plasma. The dopants are created by plasma and accelerated by a magnetic field towards the surface of the aimed wafer. The simple schematic sketch of the ion-implantation equipment can be seen in Figure 2.3.

After implantation, boron is required to be activated at TEMPRESS tube furnace B1 at 1050 °C duration for 1 hour. Next, the boron silicon glass (BSG) formed during activation is required to be removed by BHF (buffered hydroFluoric acid) 1:7 or BOE (buffered oxide etch) 1:7 etching which is a buffered solution of 49% HF (hydroFluoric acid) and 40% NH4F (ammonium fluoride), commonly with a 1:7 ratio. The duration for BHF 1:7 etching is about 2 minutes until both sides are hydrophobic which shows that the BSG has been removed clearly.

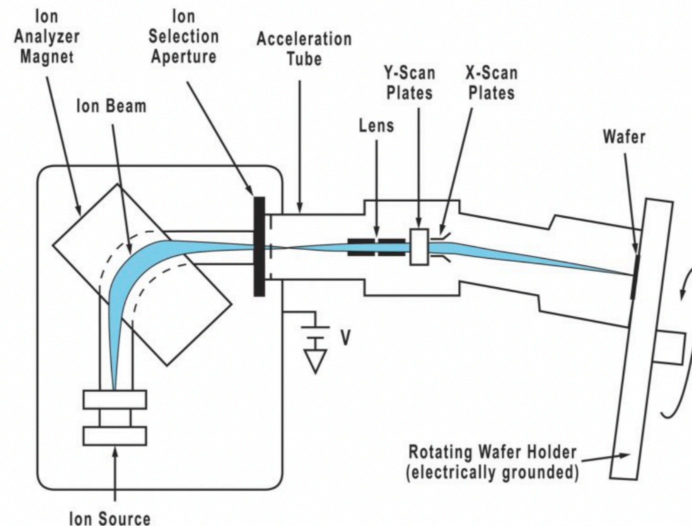


Figure 2.3: Simple schematic of ion-implantation equipment

Atomic layer deposition

Atomic layer deposition (ALD) can have precise growth and thickness control, good uniformity on large substrates as well as low substrate temperature. In this thesis, ALD is utilized to process AlO_x:H capping layer on p^+ poly-Si(O_x) carrier selective passivating contacts surface and also p^+ emitter surface for hydrogenation.

At first, it introduced TMA (tri-methyl aluminum). Then, H_2O vapor is absorbed on Si to form Si-O-H. After that, TMA reacts with hydroxyl groups to produce methane. Next, it introduced H_2O. Reaction product methane is pumped away, leaving an OH^- passivation layer on surface. Finally, one TMA and one H_2O vapor pulse form one cycle with each cycle including gas injection and pumping takes few seconds. The flowchart of ALD process can be seen in Figure 2.4 and Figure 2.5. The equipment utilized in this thesis is thermal-ALD by Oxford Instruments at Kavli Nanolab which can be illustrated in Figure 2.6. The substrate temperature for ALD AlO_x:H is set at 105 °C. And for 20nm AlO_x:H, it takes 312 cycles, around 2 hours 28 minutes with the deposition rate around 0.064 nm/cycle.

Apart from thermal-ALD at Kavli Nanolab, the spatial ALD which can be more useful in industry is also utilized for ALD AlO_x:H in this thesis. The spatial ALD is at Eindhoven S-ALD company. With spatial ALD, precursor and reactant pulsing occur at different positions. The substrate or the "ALD deposition head" must move. The purge areas created by inert gas barriers prevent chemical vapor deposition (CVD) reactions which requires operation at high pressure. And most importantly, it has no gas switching or vacuum pumps, also no deposition on the reactor walls. The schematic of spatial ALD can be seen in Figure 2.7 and Figure 2.8.The deposition substrate temperature is 200 °C and the thickness of the AlO_x:H layer is also 20 nm. This ALD process can be very fast with only 0.625 seconds per cycle.

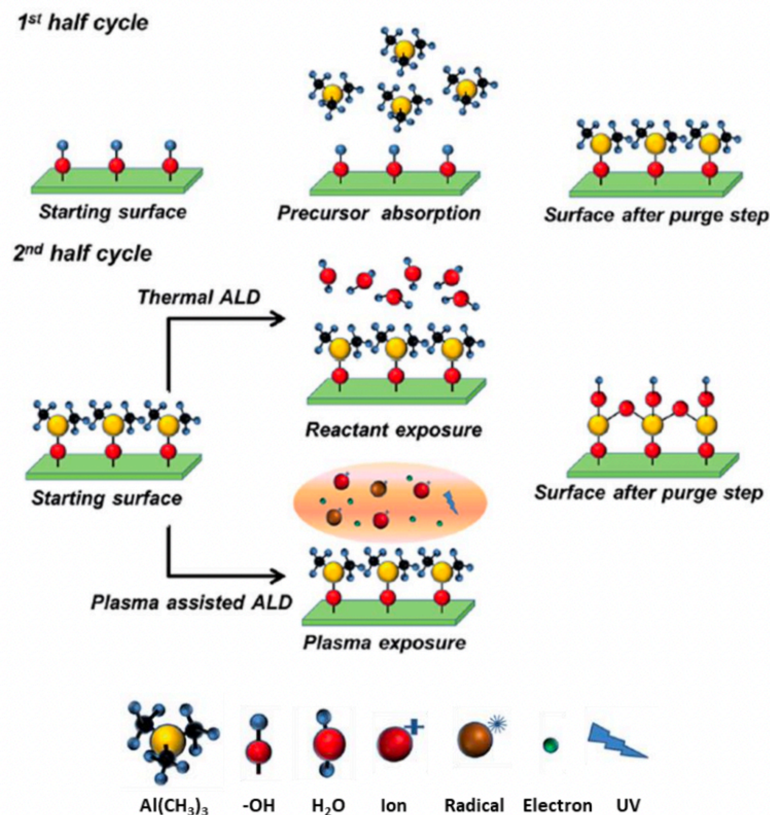


Figure 2.4: Schematic of ALD process flowchart

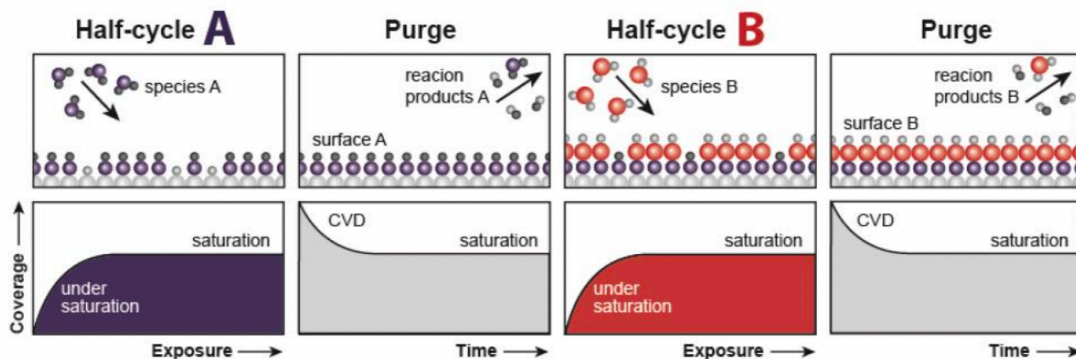


Figure 2.5: Simple schematic of ALD process

TCO sputtering equipment

In this thesis, sputtering equipment *ZORRO* by Polyteknic is used for transparent conductive oxide (TCO) sputtering for increasing the lateral conductivity and acting as anti-reflection coating (ARC). The target material is heated in vacuum. radio frequency (RF) is applied to dissociate the molecules in Argon (Ar) to ions. The generated argon ions are guided and accelerated by the magnetic field towards target material. At the same time, the argon ions also bombard the target materials. Therefore, the species are sputtered from the target material and then deposited on the wafers. The simple schematic of sputtering equipment can be illustrated in Figure 2.9. However, the passivation quality may degrade

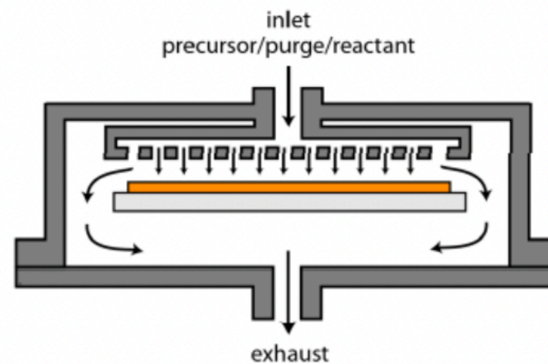


Figure 2.6: Simple schematic of thermal-ALD equipment

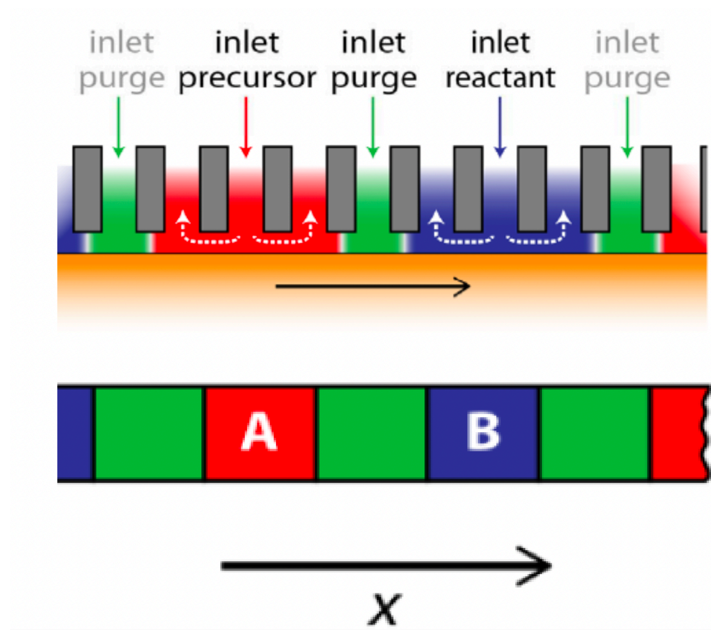


Figure 2.7: Schematic of spatial ALD

because of the sputtering damage caused by ion bombardment. In this thesis, 75 nm IWO is sputtered on the front side of n^+ poly-Si(O_x) carrier selective passivating contacts for increasing the lateral conductivity of 30 nm n^+ poly-Si(O_x) passivating contact during poly-poly solar cell fabricating and the sputtering damage is recovered by vacuum annealing at 400 °C duration for 30 minutes rather than 180 °C duration for 10 minutes oven annealing that is normally used for recovering sputtering damage within PVMD group.

In addition, before IWO sputtering, the insulator SiN_x:H capping layer after hydrogenation shoule be removed. It can be etched away by immersing the wafers into HF(0.55%) duration for 3 minutes and then BHF 1:7 duration for 10 minutes. Over-etch will have influences on the passivation quality of poly-Si(O_x) CSPCs.

Photolithography

Photolithography is utilized during metallization of fabrication of c-Si solar cells. In the photolithography process, the photoresist (PR) AZ 3027 is uniformly coated on the front side of the samples utilizing the

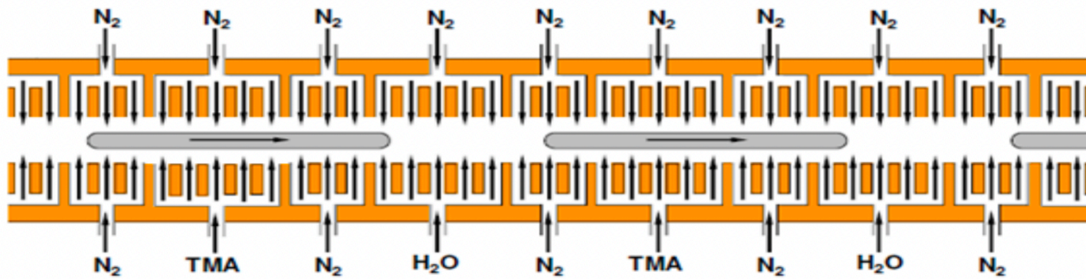


Figure 2.8: Simple schematic of spatial ALD equipment

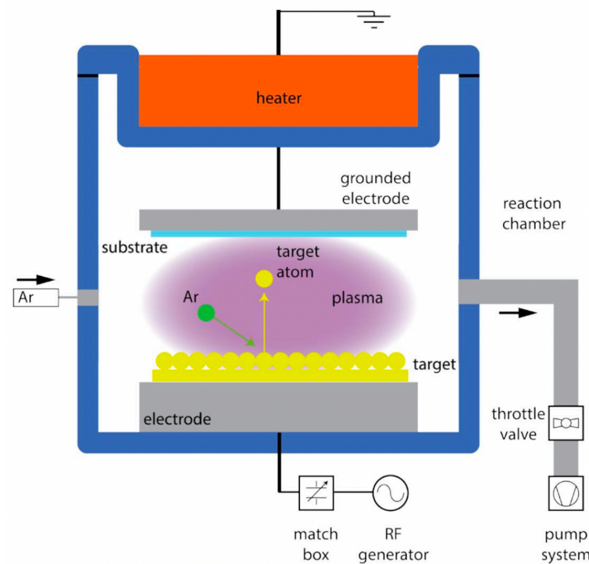


Figure 2.9: Simple schematic of sputtering equipment

Brewer science manual spinner spin-coater at Polymer Lab with the AZ 3027 ECI 4 µm recipe. The PR is required to be coated three times. Then, 12 µm PR were coated on the front side of the samples in three rounds of coating. After each round of the coating, the samples are required to be baked in the oven at 100 °C for 2 minutes, 3 minutes and 5 minutes respectively to harden the photoresist before exposure by UV light.

The front side of the photoresist coated wafers are then exposed to ultra-violet light with the 6-die mask utilizing the SUSS MicroTec MA/BA8 mask aligner equipment. The wafers are exposed under UV light for totally 100 seconds which is divided into 25 seconds for each exposure with four rounds.

After the exposure, the samples are developed for 1 minute and 50 seconds utilizing MF 322 developer and then rinsed with DI water at Polymer Lab. The used photoresist is positive. Therefore, the exposed PR opening patterns are dissolved after development. The samples are then dried and checked under the optical microscope for observe the openings of patterns. The schematic of the photolithography process can be illustrated in Figure 2.10 and [59].

Metal evaporation equipment

The metal evaporation is utilized to form the metal grids of the solar cells. Evaporation belongs to physical vapor deposition (PVD) without chemical reactions involved. With evaporation, material source is heated to high temperature in vacuum either by thermal or e-beam methods. Material is vapor transported to substrate in vacuum. It requires high vacuum that can minimize collisions of source atoms

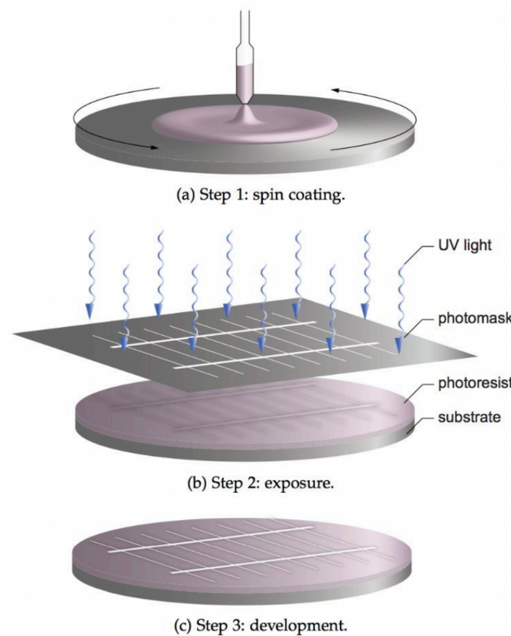


Figure 2.10: Simple schematic of photolithography process [59]

with background species. It has fast deposition rate but the film quality is low because of the energetic bombardment of ions. It has high sticking coefficient which can lead to poor conformal coverage and significant shadow but good for nanofabrication using liftoff process.

The heat for thermal evaporation comes from the resistor under high voltage. A tungsten boat is used to hold source material with lower melt point than the boat such as silver (Ag) for metallization. Thermal evaporation is simple, robust, and in widespread use. But, it has contamination from heated boat or crucible.

For e-beam evaporation, evaporation occurs at a highly localized point near the beam bombardment spot and the energy comes from the accelerated electrons which would strike into the source material. E-beam evaporation is used for material with high melt point or material that can alloy or react with tungsten. E-beam evaporation can be more complex, but extremely versatile, virtually any material. In addition, it has less contamination, less heating to wafer. However, X-rays can also be generated by high voltage electron beam. In this thesis, e-beam evaporation is utilized to evaporate aluminium (Al) for liftoff metallization. The equipment utilized is PROVAC PRO500s that can be illustrated in Figure 2.11 and [93].

i-TOPCon reference solar cell fabrication process

The fabrication flowchart of i-TOPCon reference solar cell is illustrated in Figure 2.12.

In addition, the sequential steps involved in the fabrication process are as the following:

- DSP n-type FZ c-Si wafers with thickness 280 µm and <100> orientation are utilized as bulk c-Si wafers.
- Then, the DSP n type wafers are required to be textured. Texturing is processed in alkaline solutions. The dose of KOH is 105 grams dissolving in 5 liters DI water. The method utilized for heating is water bath approach. The temperature is setting at 82 °C. And after texturing, the wafers are required to rinse in HCl bath as soon as possible. Otherwise, the KOH residues will

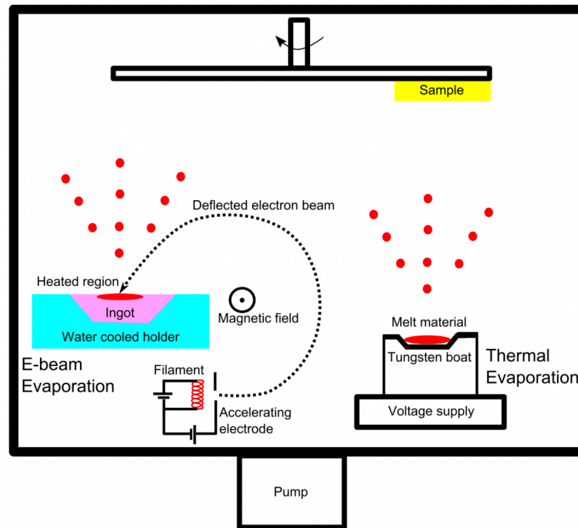


Figure 2.11: Simple schematic of evaporation equipment [93]

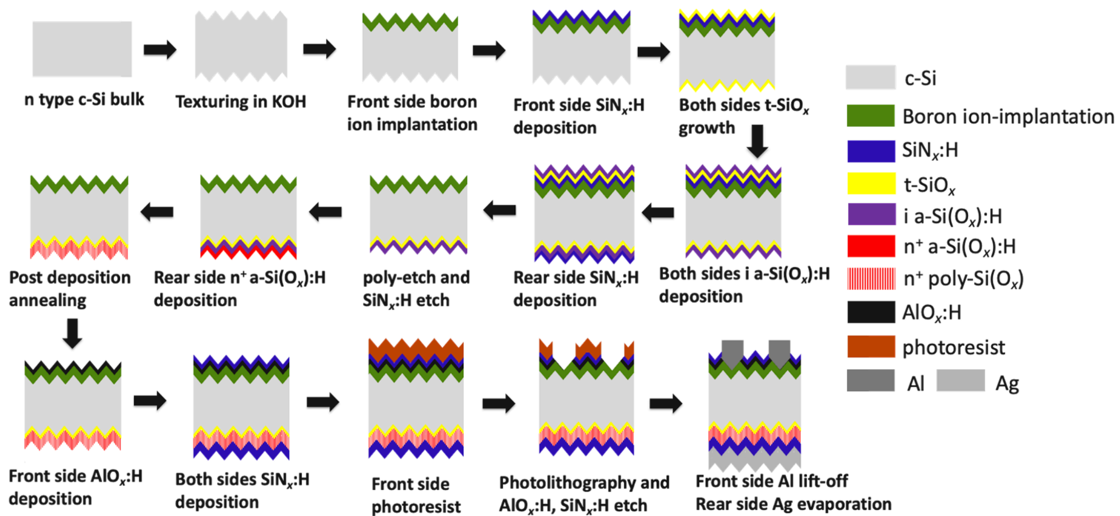


Figure 2.12: Simple schematic of i-TOPCon mono-facial solar cell on DST wafers

appear on the textured wafer surface. The concentration of the HCl bath is 0.20% which can be made by 25 milliliters 40% HCl dissolving in 5 liters DI water. During texturing, the organic additive monoTEX H 2.4 is required to add into the alkaline solutions. The whole process of texturing can be shown in Figure 2.13. Firstly, the wafers are loaded into the cassettes. Then, the wafers are rinsed in DI water for about 10 seconds. Then the wafers are immersed into the alkaline solutions with additive for about 8 minutes at 82 °C. Here, the texturing assisted organic additive is required to add into the alkaline solution when the water bath sink approaching about 80 °C. After texturing, the wafers are required to be immersed into 0.20% HCl bath for 2 minutes as soon as possible to remove the possible KOH residues. Then, finally, after that, the textured wafers are rinsed with DI water for about 5 minutes and then loaded into the spin dryer. If more wafers are needed to do the texturing process at the same time, the adding dose of KOH is 0.8 grams KOH per wafer and the adding dose of additive is 0.5 mL monoTEX H 2.4 per wafer. After texturing, the wafers are needed to be immersed into 99.9% HNO_3 at room temperature. And then the standard nitric acid wet chemical cleaning process is required to be completed at CR100.

- Next, the textured wafers are required to be immersed into poly-Si etch solution at CR100 for 2

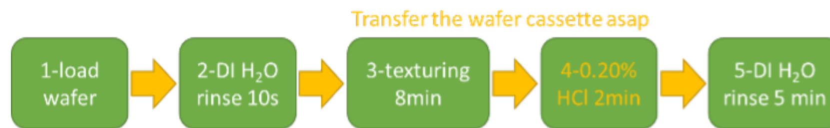


Figure 2.13: Flowchart of texturing process

minutes to smooth the pyramids. After poly-Si etch, the standard cleaning and drying process are also needed.

- Next, the double side textured wafers are shipped to France to carry out the front side boron ion-implantation with the implantation energy 20 keV and implantation doping dose $5.0 \times 10^{14} cm^{-2}$. Then, after the samples sending back, the samples are firstly needed to carry out the oxygen plasma treating in *TEPLA* and then can do the wet chemical nitric acid standard cleaning including Si^{+} and the corresponding rinsing and drying process.

- Then, the single side boron-implanted p^{+} emitter is loaded into TEMPRESS tube furnace to finish the activation of boron with the temperature at 1050 °C duration for 50 minutes in nitrogen and then 10 minutes in pure oxygen to drive-in. After p^{+} emitter boron activation, the boron silicon glass (BSG) at the surface is required to be removed by BHF 1:7 etching until both sides hydrophobic.

- After that, the activated front side is needed to be protected by SiN_x:H. The 500 nm SiN_x : H deposition utilized Novellus Concept One at CR100.

- In addition, the samples are immersed in HF(0.55%) or Marangoni duration for 4 minutes to remove the native oxide on the surface.

- Additionally, 1.3 nm thermal oxide potential barrier layer is formed at both sides at TEMPRESS tube furnace at 675 °C duration for 3 minutes. Then, after cooling down, the samples are loaded into another TEMPRESS tube furnace again to deposit 10 nm i a-Si(O_x):H layer on double sides utilizing LPCVD.

- Then, the rear side is required to be protected by SiN_x:H from the etching of intrisic layer and tunneling oxide layer on the front side. The 500 nm SiN_x:H layer is also deposited with Novellus Concept One PECVD at CR100.

- Besides, the intrinsic layer on the front side is removed by poly-Si etch solution at etching line for about 45 seconds. After that, the tunneling oxide on the front side, the SiN_x:H protective layer on both the front side and the rear side are required to be removed by BHF 1:7 solution etching until both sides are hydrophobic.

- Besides, the intrinsic layer on the front side is removed by poly-Si etch solution at etching line for about 45 seconds. After that, the tunneling oxide on the front side, the SiN_x:H protective layer on both the front side and the rear side are required to be removed by BHF1:7 solution etching until both sides are hydrophobic.

- After that, 100 nm p^{+} a-Si(O_x):H doping layer is deposited on the rear side to complete the phosphorous doping on the rear side utilized PECVD AMOR at CR10K.

- Then after high temperature post deposition annealing and crystallization with the condition 925 °C duration for 20 minutes at TEMPRESS tube furnace. The n^{+} poly-Si(O_x) passivating contact is formed.

- After that, the front side boron ion-implanted p^+ emitter is passivated by 20 nm ALD-thermal AlO_x:H at 105 °C with 312 cycles and then 75 nm PECVD SiN_x:H with substrate temperature 400 °C and the deposition time 8 minutes for textured wafers.

- Next, the AlO_x:H/SiN_x:H capping layer stack is annealed utilizing FGA at TEMPRESS tube furnace with the condition 400 °C duration for 30 minutes. The cell precursors of the mono-facial i-TOPCon solar cell are completed after this step. Here, the front side is p^+ emitter and the rear side is 100 nm n^+ poly-Si(O_x) passivating contact. The lateral conductivity of this cell precursor is good enough to transport charge carriers and let them be collected by metal grids. Then, neither of the two sides require TCO sputtering to increase the lateral conductivity. It makes the whole process easier and cheaper. In addition, more importantly, the TCO sputtering damage on the passivation of both sides can be thoroughly eliminated.

The metallization processes for the i-TOPCon mono-facial solar cell are shown as the followings:

- The metallizaiotn used Al lift-off. Firstly, in the photolithography process, the photoresist (PR) AZ 3027 is uniformly coated on the front side of the samples utilizing the spin-coater at polymer lab with the AZ 3027 ECI 4 μm recipe. The PR is required to be coated three times. Then, 12 μm PR were coated on the front side of the samples in three rounds of coating.

- After each round of the coating, the samples are required to be baked in the oven at 100 °C for 2 minutes, 3 minutes and 5 minutes respectively to harden the photoresist before exposure by ultra-violet (UV) light.

- The front side of the photoresist coated wafers are then exposed to ultra-violet light with the 6-die mask utilizing the contact aligner equipment. The wafers are exposed under UV light for totally 100 seconds which is divided into 25 seconds for each exposure with four rounds.

- After the exposure, the samples are developed for 1 minute and 50 seconds utilizing MF 322 developer and then rinsed with DI water at polymer lab. The used photoresist is positive. Therefore, the exposed PR opening patterns are dissolved after development. The samples are then dried and checked under the optical microscope for observing the openings of patterns.

- Then, the SiN_x:H and AlO_x:H capping layer stack under the opening patterns are required to be etched away for the following contacting with the metal grids since they are insulators. SiN_x:H/AlO_x:H capping layer stack are etched by BHF 1:7 for about 3 minutes and then are immersed into HF(0.55%) for about 10 minutes until the openings on the front side are hydrophobic. The accurate situations of the front side can be observed by the optical microscope to make sure they are removed thoroughly.

- After completely etching of the SiN_x:H and AlO_x:H on the front side under openings, the opening areas of the samples are then contacted with 2000 nm metal Al utilizing e-beam metal evaporation equipment PROVAC at CR10K. Here, the 2000 nm Al evaporation process can be divided into four times with each round evaporating 500 nm Al to maintain the uniformity.

- Next, the samples are immersed into ultrasonic bath filled with acetone to carry out the lift-off process. After lift-off, on front side, only the opening areas are contacting with Al. The other areas are AlO_x:H/SiN_x:H capping layer stack served as anti-reflection coating (ARC) layers.

- After that, the rear side 100 nm n^+ poly-Si(O_x) passivating contact is directly contacted with 500 nm Ag utilized 6-die hard mask which can align with the mask for photolithography. The Ag evaporation used the same evaporation equipment PROVAC but with different boats. Ag evaporation utilized the boat for thermal evaporation.

- Finally, the samples are annealed at 400 °C duration for 1-2 minutes on hotplate at ESP lab to make Al form the ohmic contact. And at the same time, it can decrease the contact resistivity.

Fabrication process of poly-poly solar cell

The fabrication flowchart of poly-poly solar cells with different post deposition annealing conditions is shown in Figure 2.14.

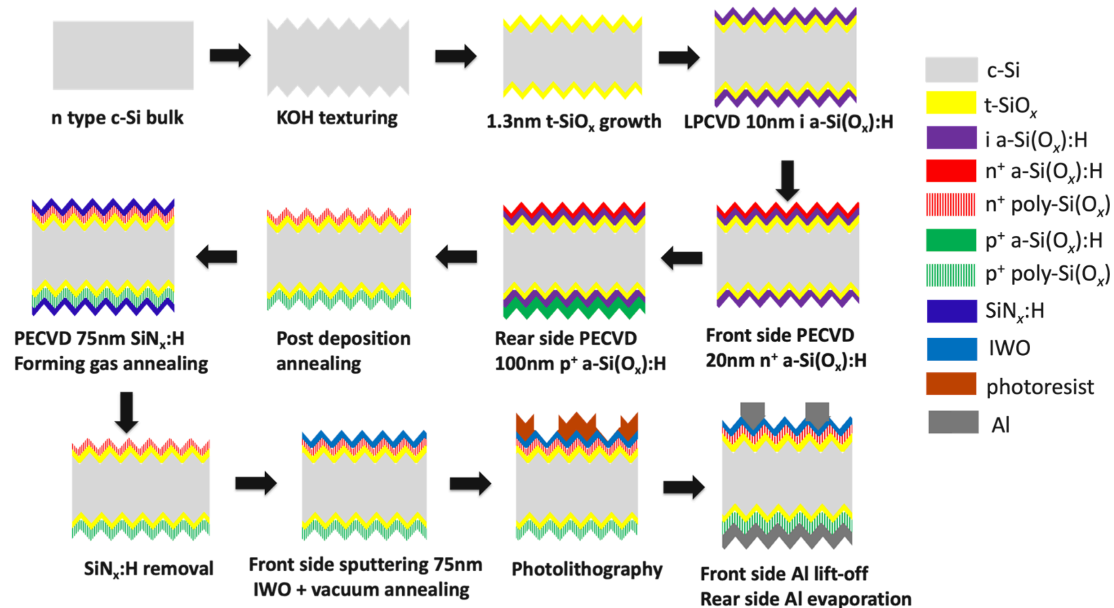


Figure 2.14: Simple flowchart for poly-poly mono-facial solar cell

And the detailed fabrication processes of poly-poly solar cells are as the followings:

- The poly-poly solar cells on DST wafers also utilize DSP n-type FZ c-Si wafers with thickness 280 μm and <100> orientation as bulk c-Si wafers.

- The texturing and cleaning process for poly-poly solar cell is the same as the above mentioned i-TOPCon solar cell.

- After texturing and wet chemical nitric acid standard cleaning process, the textured wafers are immersed into HF(0.55%) to remove the native oxide.

- The samples are then loaded into TEMPRESS tube furnace to carry out thermally oxidation. The temperature for t-SiO_x is 675 °C and duration for 3 minutes.

- Then, within 5 minutes, after t-SiO_x, the samples are required to transfer to another TEMPRESS LPCVD tube furnace to process the 10 nm intrinsic layer by LPCVD. The deposition time is 5 minutes for 10 nm intrinsic layer.

- Next, the native oxide on the intrinsic layer after LPCVD is also required to be removed which is very necessary.

- After that, the samples are loaded into AMOR PECVD to process the boron doping layer. The front side of the cell precursor is decided to be phosphorous doped n^+ poly-Si(O_x) passivating

contact and the rear side is considered to be boron doped p^+ poly-Si(O_x) passivating contact. The thickness of the front side n^+ poly-Si(O_x) passivating contact is chosen to be 20 nm which is the optimum thickness for passivation within PVMD group. In addition, the front side is n^+ poly-Si(O_x) passivating contact since the TCO sputtering damage on n^+ poly-Si(O_x) passivating contact can be largely less than the passivaiton damage on p^+ poly-Si(O_x) passivating contact. The fermi Level of n^+ poly-Si(O_x) passivating contact and TCO are both near the conduction band. However, for p^+ poly-Si(O_x) passivating contact, the fermi Level is usually near the valence band. Therefore, the band gap mismatch of p^+ poly-Si(O_x) passivating contact and TCO can be larger. And it can also form higher potential barrier that can damage the passivation. In addition, for poly-poly mono-facial solar cell, reducing the the light absorption and parasitic absorption of front side is very essential. Thus, the thickness for thin films on front side can not be very large which can induce large light absorption. At the same time, when thickness of n^+ poly-Si(O_x) TOPCon is less than 50 nm, the lateral conductivity of it is not good enough for charge carriers transporting and collecting. Therefore, TCO is a must on front side. From all the reasons above, the optimum structure is decided to be 20 nm n^+ poly-Si(O_x) passivating contact on the front side and 100 nm p^+ poly-Si(O_x) passivating contact on the rear side. 100 nm p^+ poly-Si(O_x) passivating contact has the best passivation quality on textured wafers. And at the same time, TCO is not needed when p^+ poly-Si(O_x) passivating contact thickness is thicker than 50 nm. Then, after the two sides doping layer deposition, the cell precursors for poly-poly solar cell are prepared.

- The optimum post-deposition annealing conditions for poly-poly cell precursors has not been decided. Therefore, four different PDA conditions, 875 °C annealing duration for 30 minutes, 900 °C annealing duration for 30 minutes, 925 °C annealing duration for 20 minutes, and finally, 950 °C annealing duration for 10 minutes are used. The post deposition annealing is processed also in TEMPRESS tube furnace with only nitrogen gas.

- Next, the samples are carried out the hydrogenation process. 75 nm SiN_x:H is deposited by PECVD at Kavli Nanolab on double side. 8 minutes deposition time is utilized for textured wafers. And then, the samples are loaded into TEMPRESS tube furnace to process forming gas annealing. The annealing temperature is set to be 400 °C and duration for 30 minutes. Then, the hydrogenation process for the cell precursors are completed.

- Next, the 75 nm SiN_x:H layers on double side are removed by immersing the samples into BHF 1:7 duration for 3 minutes and then into HF(0.55%) duration for 10 minutes until both sides are hydrophobic.

- Then, 75 nm IWO without hydrogen is sputtered on the front side utilizing Zorro with the optimum recipe within PVMD group.

The metallization process for poly-poly mono-facial solar cell is the same as i-TOPCon reference mono-facial solar cell.

- The metallizaiotn used Al lift-off. Firstly, in the photolithography process, the photoresist (PR) AZ 3027 is uniformly coated on the front side of the samples utilizing the spin-coater at polymer lab with the AZ 3027 ECI 4 µm recipe. The PR is required to be coated three times. Then, 12 µm PR were coated on the front side of the samples in three rounds of coating.

- Then, 4 µm PR were coated on the rear side of the samples to protect the thick p^+ poly-Si(O_x) passivating contacts on the rear side.

- After each round of the coating, the samples are required to be baked in the oven at 100 °C for 2 minutes, 3 minutes and 5 minutes respectively to harden the photoresist before exposure by UV light.

- The front side of the photoresist coated wafers are then exposed to ultra-violet light with the 6-die mask utilizing the contact aligner equipment. The wafers are exposed under UV light for totally 100 seconds which is divided into 25 seconds for each exposure with four rounds. The 6-die mask has to be able to align with the mask utilized when sputtering IWO. The alignment of photolithography mask and the TCO areas is very essential during exposure.

- After the exposure, the samples are developed for 1 minute and 50 seconds utilizing MF 322 developer and then rinsed with DI water at polymer lab. The used photoresist is positive. Therefore, the exposed PR opening patterns are dissolved after development. The samples are then dried and checked under a optical microscope for observe the openings of patterns.

- The opening areas of the front side of the samples are then contacting with 2000 nm metal Al utilizing e-beam metal evaporation equipment PROVAC. Here, the 2000 nm Al evaporation process can be divided into four times with each round 500 nm Al.

- Next, the samples are immersed into ultrasonic bath filled with acetone to carry out the lift-off process. After Al lift-off, on front side, only the openings contact with Al. On rear side, only thick 110 nm p^+ poly-Si(O_x) passivating contact existed preparing for contacting with Ag.

- After that, the rear side 110 nm p^+ poly-Si(O_x) passivating contact is directly contacted with 500 nm Al utilized 6-die hard mask which can align with the mask for photolithography and TCO sputtering.

- Finally, the samples are annealed at 400 °C duration for 1-2 minutes on hotplate at ESP lab to make front-side Al form the ohmic contact and can decrease the contact resistivity.

2.2. Characterization techniques

2.2.1. Optical performance

Spectroscopic ellipsometry

Spectroscopic ellipsometry is based on measuring the change in polarization of incident light onto a substrate that can be illustrated in Figure 2.15 and Figure 2.16.The ellipsometer from J. A. Woollam Co. was used for this thesis project to measure the thickness and the data analysis was performed with the CompleteEASE software.

Basically, the amplitude P_{si} and phase Δ should go into the software. The amplitude P_{si} and phase Δ can come from the initial figures in the CompleteEASE software which represent the pre-known measurement data. And the red curves represent the amplitude P_{si} and the green curves represent the phase Δ on the screen. The black dashed lines are illustration of the model generated data.

Firstly, the suitable substrate is chosen and the Cauchy layer is added on or under the substrate. Then, the thickness is continuously changed that can approximately make the model generated data fit the measurement data. When the thickness is bold which can show that the parameter is realizable and fit. Then changing A and B and then C, when C is negative and forcing C to zero. Sometimes the surface roughness is enabled. Until the generated mean square error (MSE) is below 10, this process is done iteratively. Then, the refractive index n and extinction coefficient k versus wavelength (nm) and the thickness can be found. If the MSE is not ideal the software will change fitting parameters until they fit.

The equations from the input of the software to the output of the software are generally as the following:

$$\rho = \frac{r_p}{r_s} = tan\Phi e^{i\Delta} \tag{2.1}$$

$$\mathbf{n} = n(\lambda) + ik(\lambda) \tag{2.2}$$

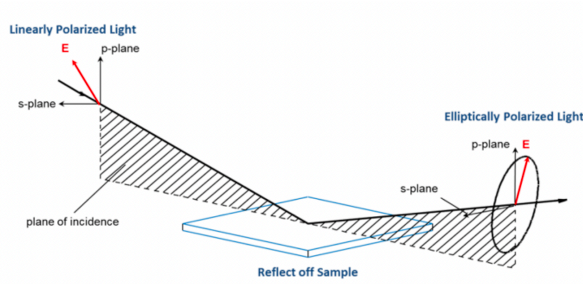


Figure 2.15: Schematic of the principle of Spectroscopic ellipsometry

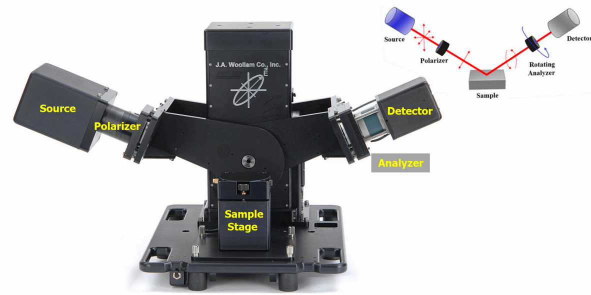


Figure 2.16: Simple schematic of Spectroscopic ellipsometry by J. A. Woollam Co.

$$n(\lambda) = \frac{C}{V(\lambda)} \tag{2.3}$$

$$k(\lambda) = \frac{\alpha(\lambda) \cdot \lambda}{4\pi} \tag{2.4}$$

ρ is complex reflectance ratio and r_{p} is the reflectance of p-polarized light while r_{s} is the reflectance of s-polarized light.Φ is amplitude ratio and Δ is phase difference. Φ and Δ are ellipsometric parameters. $n(\lambda)$ is the wavelength dependent refractive index and $k(\lambda)$ is the extinction coefficient. In addition, $\alpha(\lambda)$ is the absorption coefficient.

After simulation, the optical properties n and k, thickness, roughness and uniformity can come out of the software.

Reflectance measurement

In the reflectance measurement equipment, the monochromatic reference beam and monochromatic sample beam with high resolution are generated. The monochromatic reference beam is used to determine and correct the chamber reflection. The integrating sphere is coated with a highly reflective and scattering material. The sample light directly entered the integrating sphere and then be reflected for many times and scattered in all directions which can generate a uniform electromagnetic field inside the integrating sphere. The port plug is utilized to remove the specular reflection while only the diffuse reflection can be measured. Then, two detectors located at the bottom of the integrating sphere can measure the light density within a large range of wavelength. The simple schematic of the Reflectance measurement equipment is illustrated in Figure 2.17. In this thesis, the reflectance measurement equipment utilized is PerkinElmer Lambda 950 UV/VIS spectrometer. It is used for measuring the reflectance of textured wafers after dealing with different poly-Si etch time and times of NAOC.

2.2.2. Surface morphology

Optical microscope

The optical microscope, also referred to as a light microscope, is a type of microscope that commonly uses visible light and a system of lenses to generate magnified images of small objects. The object is placed on a stage and may be directly viewed through two eyepieces on the microscope. A camera is typically used to capture the image (micrograph). A range of objective lenses with different magnification are usually provided mounted on a turret, allowing them to be rotated into place and providing an ability to zoom-in. The maximum magnification power of optical microscopes is typically limited to around 1000x because of the limited resolving power of visible light. The vast majority of microscopes have the same 'structural' components that includes : eyepiece (ocular lens), objective turret, revolver (to hold multiple objective lenses), objective lenses, focus knobs (to move the stage), coarse adjustment , fine adjustment, stage (to hold the specimen), light source (a light or a mirror), diaphragm and condenser, mechanical stage.

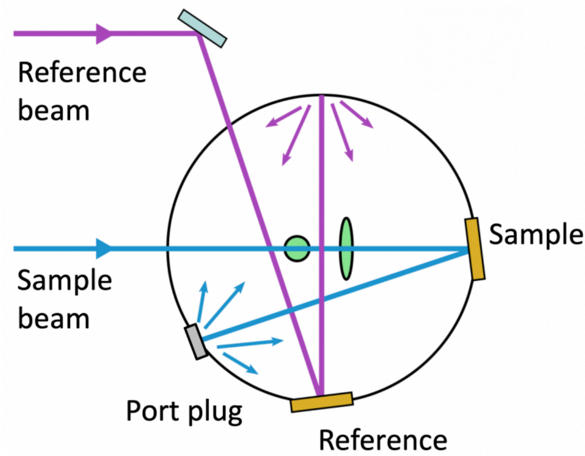


Figure 2.17: Simple schematic of the reflectance measurement equipment

The eyepiece, or ocular lens, is a cylinder containing two or more lenses; its function is to bring the image into focus for the eye. Typical magnification values for eyepieces include 5×, 10× (the most common), 15× and 20×. At the lower end of a typical optical microscope, there are one or more objective lenses that collect light from the sample. Microscope objectives are characterized by two parameters, namely, magnification and numerical aperture. The former typically ranges from 5× to 100× while the latter ranges from 0.14 to 0.7, corresponding to focal lengths of about 40 to 2 mm,respectively.Adjustment knobs move the stage up and down with separate adjustment for coarse and fine focusing. The actual power or magnification of a optical microscope is the product of the powers of the eyepiece and the objective lens. For example a 10x eyepiece magnification and a 100x objective lens magnification gives a total magnification of 1,000×.

The reflected light microscope ZEISS Axiotron that was used in this thesis can display the magnification of 100x can display the image digitally. The scale of a certain region of interest was obtained by digital means. The simple schematic of the components of the microscope can be shown in Figure 2.18 and [66]. The optical microscope in the thesis is utilized mainly for oberving the blistering conditions.

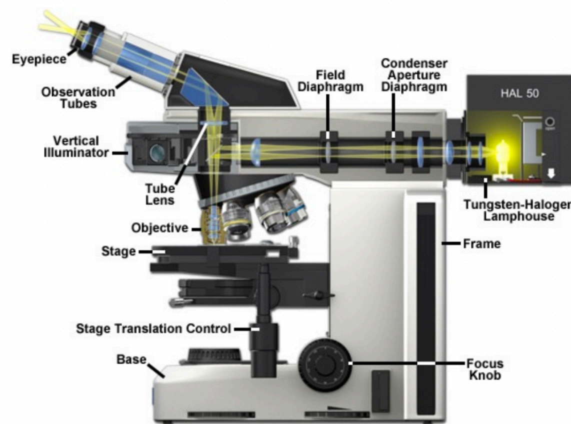


Figure 2.18: Simple schematic of the components of the microscope [66]

Scanning electron microscope

A scanning electron microscope (SEM) projects and scans a focused stream of electrons over a surface to create an image. The electrons in the beam interact with the sample, thereby producing various signals that can be used to obtain information about the surface's topography and composition.

The main SEM components include: Source of electrons, Column down which electrons travel with electromagnetic lenses, Electron detector,Sample chamber, Computer and display to view the images.Electrons are produced at the top of the column, accelerated down, and passed through a combination of lenses and apertures to produce a focused beam of electrons which then strikes the surface of the sample. The sample itself is mounted on a stage in the chamber area and both the column and the chamber are evacuated by a combination of pumps. The level of the vacuum will depend on the design of the microscope.The position of the electron beam on the sample is controlled by scan coils situated above the objective lens. These coils allow the beam to be scanned over the surface of the sample. This beam rastering or scanning enables information about a defined area on the sample to be collected. As a result of the electron-sample interaction, a number of signals are produced. These signals are then detected by appropriate detectors.The maximum resolution obtained in an SEM depends on multiple factors like the electron spot size and interaction volume of the electron beam with the sample. While it cannot provide atomic resolution, some SEMs can achieve resolution below 1 nm. Typically, modern full-sized SEMs provide resolution between 1-20 nm, whereas desktop systems can provide a resolution of 20 nm or more. The schematic of SEM can be discovered in Figure 2.19 and [39]

The utilized SEM in the thesis is Hitachi Regulus 8230 which is used for observing the textured surface formation.

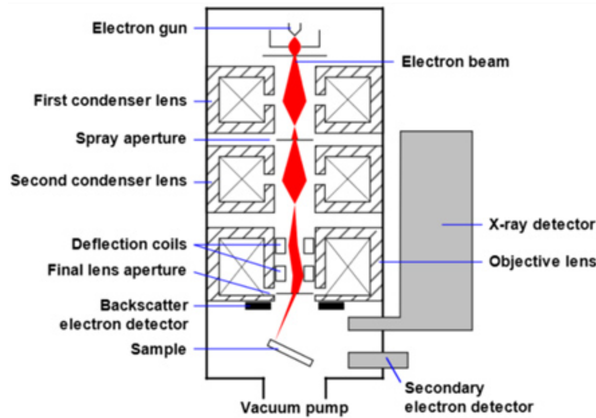


Figure 2.19: Simple schematic of SEM[39]

2.2.3. Lifetime and J_o measurement

Photoconductance lifetime tester

After illumination, the excess electrons Δn and excess holes Δp are injected into c-Si. The variation of photoconductivity σ can be expressed by,

$$\sigma = q(\mu_n n + \mu_p p) \tag{2.5}$$

$$n = n_o + \Delta n \tag{2.6}$$

$$p = p_o + \Delta p \tag{2.7}$$

q is elementary charge, μ_p and μ_n are electron and hole mobility, respectively. And n_o and p_o are equilibrium electron and hole concentration, respectively. In addition, Δn and Δp are excess electron and hole concentration, respectively.

After flash light, the excess carriers can be given by,

$$\Delta n = \frac{\Delta \sigma}{q(\mu_n + \mu_p)} \tag{2.8}$$

When assuming the identical mobilities for equilibrium Δn=Δp and Δn » n_o, Δp » p_o.

The basic continuity equation is expressed by,

$$\frac{\partial \Delta n(t)}{\partial t} = G - R = G - \frac{\Delta n(t)}{\tau_{eff}} \tag{2.9}$$

G is generation rate, *R* is recombination rate while τ_{eff} is the effective lifetime.

In Photoconductance Decay, G(t) « $\frac{\partial \Delta n(t)}{\partial t}$, then τ_{eff} is given by,

$$\tau_{eff}(\Delta n) = -\frac{\Delta n(t)}{\partial \Delta n(t)/\partial t} \tag{2.10}$$

Here, τ_{eff} is dominated by bulk and surface recombination.

Under transient mode with τ > 100μs, since the flash is very short, then, $G \rightarrow 0$. Then τ_{eff} is given by,

$$\tau_{eff} = -\frac{\Delta n}{d\Delta n/dt} \tag{2.11}$$

Δn can be calculated from the measured photoconductance. $d\Delta n/dt$ is the slope of the tangent on the curve of the time-resloved Δn decay. The recombination current density J_o can also be calculated by the figure.

Under quasi-steady state (QSS) mode with τ < 100μs. Though, the flash is very short, it is still much longer than τ, then τ_{eff} is given by,

$$\tau_{eff} = \frac{\Delta n}{G} \tag{2.12}$$

G is calculated from the light intensity detected by the photodiode.

The simple schematic of Sinton WCT-120 photoconductance decay lifetime tester utilized in this thesis can be seen in Figure 2.20 and Figure 2.21.

The implied-V_{oc} (iV_{oc}) is a prediction for the V_{oc} of the final device. It can be calculated by,

$$iV_{oc} = \frac{K_B T}{q} ln(\frac{\Delta n(N_D + \Delta n)}{{n_i}^2}) \tag{2.13}$$

Here, K_B is the Boltzmann constant. *q* is the elementary charge. *T* is the temperature. Δn is excess minority carrier electron denisty. N_D is the concentration of donors. n_i is the intrinsic concentration of carriers. The τ_{eff} and iV_{oc} are the main parameters to characterize the electrical performance of the passivation quality.

Sinton WCT-120 is used to measure minority carrier lifetime and recombination current density (J_o) in this thesis project.

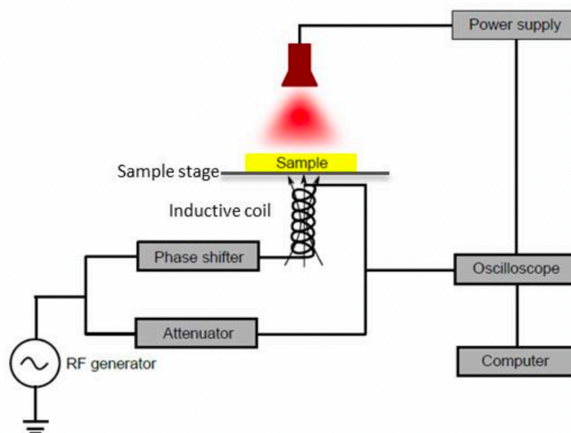


Figure 2.20: Schematic of the Sinton WCT-120 lifetime tester

Figure 2.21: Simple schematic of Sinton WCT-120 Photoconductance Decay Lifetime Tester

2.2.4. Compositional analysis

Secondary ion mass spectrometry

Secondary-ion mass spectrometry (SIMS) is a technique used to analyze the composition of solid surfaces and thin films by sputtering the surface of the specimen with a focused primary ion beam and collecting and analyzing ejected secondary ions. The mass/charge ratios of these secondary ions are measured with a mass spectrometer to determine the elemental, isotopic, or molecular composition of the surface to a depth of 1 to 2 nm. Due to the large variation in ionization probabilities among elements sputtered from different materials, comparison against well-calibrated standards is necessary to achieve accurate quantitative results. SIMS is the most sensitive surface analysis technique, with elemental detection limits ranging from parts per million to parts per billion.

Schematic of a typical dynamic SIMS instrument is shown in Figure 2.22 and [86]. High energy (usually several keV) ions are supplied by an ion gun (1 or 2) and focused on to the target sample (3), which ionizes and sputters some atoms off the surface (4). These secondary ions are then collected by ion lenses (5) and filtered according to atomic mass (6), then projected onto an electron multiplier (7, top), Faraday cup (7, bottom), or CCD screen (8).

In this thesis project, SIMS is utilized to analyze the B,O,H concentration in atom/cc for p^+ poly-Si(O_x) passivating contacts and P,O,H concentration for n^+ poly-Si(O_x) passivating contacts.

X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA), is a technique for analyzing a material's surface chemistry. XPS can measure elemental composition as well as the chemical and electronic state of the atoms within a material.XPS spectra are obtained by irradiating a solid surface with a beam of X-rays and measuring the kinetic energy of electrons that are emitted from the top 1-10 nm of the material. A photoelectron spectrum is recorded by counting ejected electrons over a range of kinetic energies. The energies and intensities of the photoelectron peaks enable identification and quantification of all surface elements (except hydrogen).XPS is a powerful measurement technique because it not only shows what elements are present, but also what other elements they are bonded to.

A typical XPS spectrum is a plot of the number of electrons detected at a specific binding energy. Each

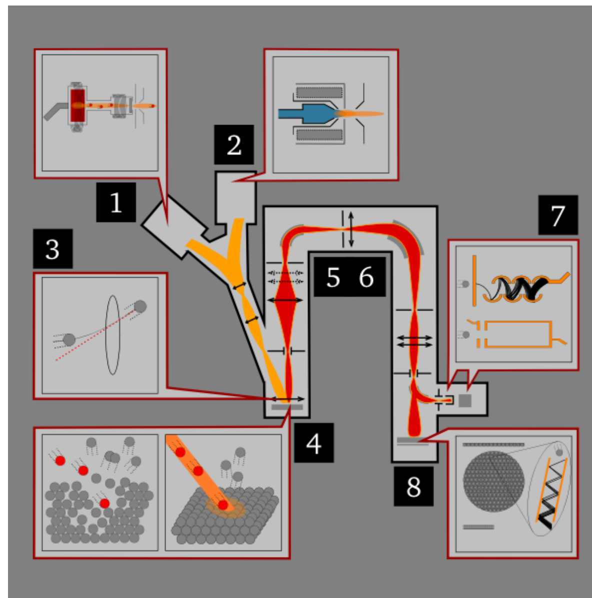


Figure 2.22: Simple schematic of the components of SIMS[86]

element produces a set of characteristic XPS peaks. These peaks correspond to the electron configuration of the electrons within the atoms, e.g., 1s, 2s, 2p, 3s, etc. The number of detected electrons in each peak is directly related to the amount of element within the XPS sampling volume. To generate atomic percentage values, each raw XPS signal is corrected by dividing the intensity by a relative sensitivity factor (RSF), and normalized over all of the elements detected. Since hydrogen is not detected, these atomic percentages exclude hydrogen.The schematic of XPS measurement can be shown in Figure 2.23. In this thesis, XPS is utilized to measure the quality of samples fabricated by different interfacial tunnelling oxides processes (NAOS-SiO_x, PANO-SiO_x and t-SiO_x).

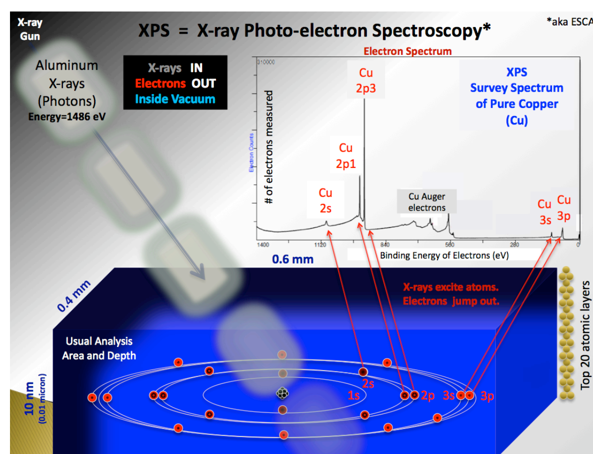


Figure 2.23: Simple schematic of XPS measurement[87]

Electrochemical capacitance-voltage profiling

The electrochemical capacitance-voltage (ECV) technique was employed to measure the active carrier concentration profiles in semiconducting layers.ECV is a common characterization method to investigate the doping profiles of semiconductor layers by a depth based CV measurement by varying the conditions at semiconductor/electrolyte interface resulting in controlled etching of the material.ECV method uses semiconductor-electrolyte Schottky contact to create a depletion region. Depletion region is the region containing immobile ionized charges (such asions) which are electrically active defects or

traps. Due to the presence of ionized charges, depletion region behaves as a capacitor. Capacitance measurements give an idea about the dopant and electrically active defect densities. Depth profile is realized by etching the semiconductor electrolytically between successive capacitance measurements.

ECV profiling involves two basis steps: (a) determination of carrier concentrations by measuring differential capacitance of the Schottky barrier produced at electrolyte/semiconductor interface; and (b) controlled removal of material via electrochemical anodic dissolution. Both steps are repeated to obtain variations in the carrier concentration with depth. In case of p-type semiconductor, the flow of holes due to forward biased barrier affect the dissolution reaction. Whereas, the holes in reverse bias promote the dissolution process in n-type semiconductor. These holes in n-type semiconductor can be generated optically by illuminating with blue light. These electrons are absorbed near the surface of the semiconductor, thereby promoting the dissolution. Typical dissolution rates are around 1 μm/h. The thickness of removed material is calculated by taking integration of dissolution current and then applying Faraday's law. Actual depth can be determined by adding this thickness to the local depletion depth.

Figure 2.24 shows the schematics of an electrochemical cell. Sample is pressed against a sealing ring in the electrochemical cell filled with electrolyte. The contact area can be controlled by the size of the ring opening. By applying a potential between the platinum electrode and semiconductor, depletion region is formed and measured with respect to the reference (saturated calomel) electrode. The varying current between semiconductor and counter electrode, can regulate etching conditions. ECV in this thesis project is used for measuring and comparing the boron doping profile of p^+ emitter with a WEP wafer profiler CVP21 , at TNO Petten.

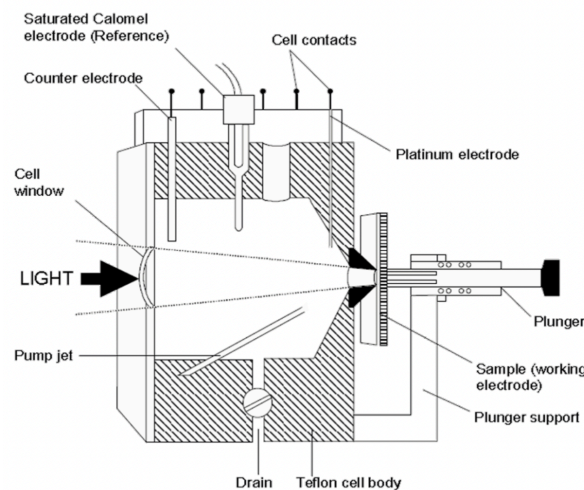


Figure 2.24: Simple schematic of ECV profiling[48]

2.2.5. Current-voltage measurement

Wacom WXS-90S-L2 solar simulator with AAA class is utilized in this thesis to measure the solar cell J-V curve which can show the electrical performance of solar cell and the corresponding external parameters like short circuit current density J_{sc}, open circuit voltage V_{oc}, Fill Factor (*FF*), the maximum power point voltage V_{mpp}, the maximum power point current density J_{mpp}, the series resistance R_s and shunt resistance R_{sh} and the most importantly, the efficiency η of solar cell.

The measurement of Wacom is executed at standard test condition (STC) with the measuring stage controlling at 25 °C by the underneath water cooling system. The light for measuring includes a Xe-lamp and a halogen lamp which has an an irradiance of 1000 w/m^2 with AM1.5 spectrum. Before measurement, the Xe and halogen lamps are required to be warmed firstly duration for about 30 minutes. And every time before measurement, the equipment is ought to be calibrated by two reference cells to make the results more accurate. The *J-V* curve of the solar cell is obtained by a 4 point probe

measurement. Two probing wires are used for voltage supply and the separate other two probing wires are utilized for the current collection. Since there will not be any current flowing through these wires. All the current will flow through the sourcemeter and thus, the measurement can be very accurate.

The fill factor (*FF*) and efficiency η can be calculated by the following equations:

$$FF = \frac{V_{mpp} \times J_{mpp}}{V_{oc} \times J_{sc}} \tag{2.14}$$

$$\eta = \frac{V_{mpp} \times J_{mpp}}{I_{in}} = \frac{V_{oc} \times J_{sc} \times FF}{I_{in}} \tag{2.15}$$

The simple schematic of this equipment can be discovered in Figure 2.25.

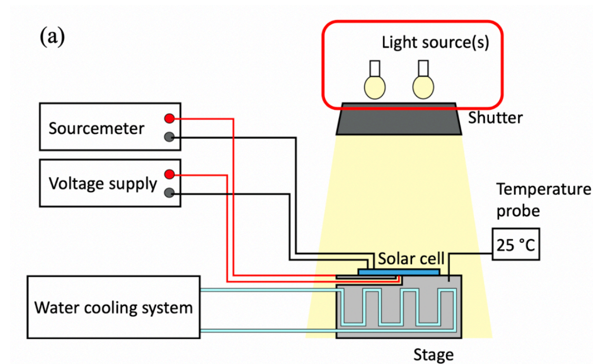


Figure 2.25: Simple schematic of Wacom Current-Voltage measurement

3
Passivation of p^+ poly-Si(O_x) passivating contacts

This chapter will focus on the optimization of p^+ poly-Si(O_x) carrier selective passivating contacts on textured surface. p^+ poly-Si(O_x) TOPCon consists of ultra-thin tunnelling SiO_x layer on the c-Si bulk to induce the chemical passivation by forming silicon oxide bonds. And on the SiO_x layer is intrinsic a-Si(O_x):H layer and then, the boron doped a-Si(O_x):H layer. After high temperature annealing, they will form p^+ poly-Si(O_x) layer which can form field effect passivation. In addition, after that, the hydrogenation process is applied to further enhance the chemical passivation. In this chapter, these aspects are explored to optimize the passivation quality of p^+ poly-Si(O_x) passivating contacts.

3.1. Absorber surface

As in chapter 1, the surface morphology plays a significant role in maximizing light trapping to improve the efficiency of the solar cell[76][60][32]. The textured surface morphology can work as efficient light trapping structures in silicon solar cells.In the wet etching process, alkaline solutions such as potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH) are commonly used for surface texturing[58][56][32].KOH is generally preferred for surface texturing of Si in photovoltaic industry as it provides high etch rate and low cost[96][57]. Wet etching of Si <100> in alkaline solution results in the formation of random upright pyramids/hillocks, which are typically bounded by four <111> planes [32].The surface of the c-Si wafers can be textured to reduce the reflection that can bring better optical performance to the solar cell.

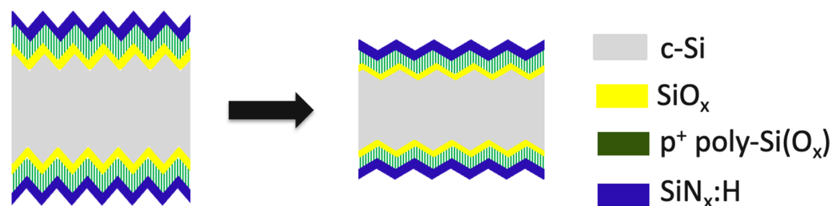


Figure 3.1: The sample structure for the experiment on abosorber surface. The aim of the experiment is to explore the influences of both poly-etch duration time and and times of NAOC on the optical and electrical performance of p^+ poly-Si(O_x) passivating contacts.

Rounding and smoothing is another approach to deal with the morphology of textured wafers. The pyramids after texturing can be very sharp which is hard for the following thin films formation. In addition, it can induce defect states on the surface that may influence passivation. Rounding and smoothing of pyramidal structures is an essential part to decrease the amount of defect densities at the c-Si surface after texturing. Through immersing the samples in the poly-Si etching solution which consists

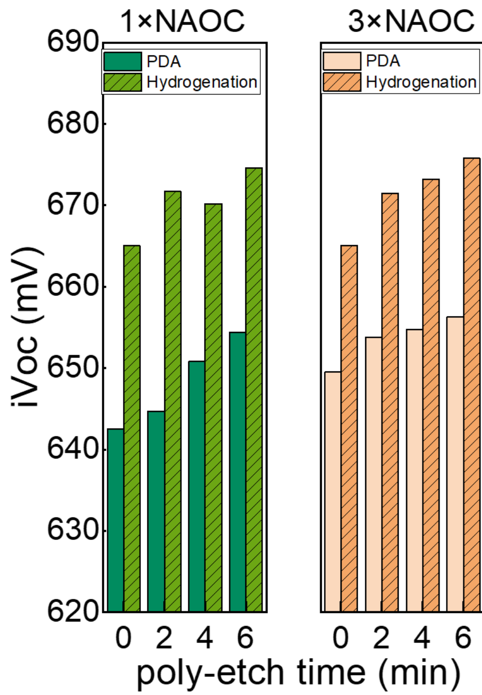


Figure 3.2: The influences of poly-etch time and times of NAOC on the electrical performance of p^+ poly-Si(O_x) passivating contacts

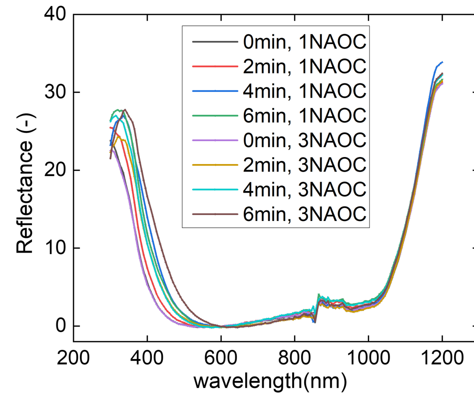


Figure 3.3: The effects of poly-etch time and times of NAOC on the optical properties of p^+ poly-Si(O_x) passivating contacts

of HF and HNO_3, the sharp pyramids will be etched and become rounding. Then, the impurities and contaminations after texturing and poly-Si etching are required to be removed by nitric acid oxidation cleaning (NAOC). One NAOC consists of one wet chemical nitric acid standard cleaning as is shown in chapter 2 and then, removing the native oxide and formed oxide by HF(0.55%) etching for 4 minutes.

During etching, etch surface morphology depends on numerous parameters such as etchant type, etching concentration, etching duration time and etching temperature. Here, for poly-Si etch, etchant type, etching concentration, etching temperature are all kept as stable, and the only changed parameter is the poly-Si etch duration time. At the same time, for NAOC process, the changed parameter is the times of NAOC after texturing and poly-Si etching. Therefore, in this experiment, the motivation is to explore the influences of both poly-etch duration time and and times of NAOC on the optical and electrical performance of p^+ poly-Si(O_x) passivating contacts. Here, the changes of surface morphology is indicated by optical and electrical performance. As above mentioned, the morphology can largely affect optical performance. It is also curious that whether it can also affect electrical performance and how to balance them.

The structure of sample utilized in this experiment can be shown in figure 3.1. The poly-etch time is changed from 0 minute to 6 minutes with the interval of 2 minutes. And the following times of NAOC are 1 NAOC and 3 NAOC, respectively. The results are shown in figure 3.2 and figure 3.3. Here, the electrical performance is characterized by implied open circuit voltage (iV_{oc}) of samples and the optical performance is characterized by reflectance of samples. In addition, the sample with poly-etch 0 minute is set as the reference sample. It can be shown from figure 3.2 that iV_{oc} of p^+ poly-Si(O_x) passivating contacts only slightly increase with poly-etch time since the surface becomes rounding. The larger iV_{oc} represents that it has better electrical performance. iV_{oc} of samples have no obvious changes with the increasing of times of NAOC. But more obviously, the reflectance becomes larger as the poly-etch time and times of NAOC increase that can be seen in figure 3.3. The larger reflectance means that it has worse light trapping and also the optical performance is worse. Therefore, to balance the electrical and optical properties of p^+ poly-Si(O_x) passivating contact, 2 minutes poly-Si etching duration time and then 1 NAOC cleaning process are chosen to deal with the morphology of the textured surface

preparing for the following experiments.

3.2. Interfacial oxides

Experiment objectives and Sample preparation

The SiO_x layer can firstly retain the hydrogen. Then, the hydrogen atoms in SiO_x can form hydrogen silicon bonds with dangling Si atoms on the c-Si bulk surface to intensify the hydrogen chemical passivation. In addition, it can serve as the potential barrier to limit the in-diffuse of dopants. The good field effect is formed because of tunnelling oxide layer which can induce field effect passivation. Furthermore, the interfacial tunnelling oxide layer can reduce the interface defect density and dangling bonds by forming silicon oxygen bonds. SiO_x layer can also have oxygen chemical passivation. Therefore, the tunnelling oxide layer is essential for p^+ poly-Si(O_x) carrier selective passivating contacts. At the same time, different types of interfacial silicon oxide layers through different fabrication processes can have various properties from van der Vossen,R et al and Huang, Y et al.[37][85]. They can affect the recombination current density (J_0), the boron doping profile and also the stochiometry that can be shown in figure 3.4. Therefore, the interfacial silicon oxides comparisons and their influences on the passivation of p^+ poly-Si(O_x) passivating contacts are explored.

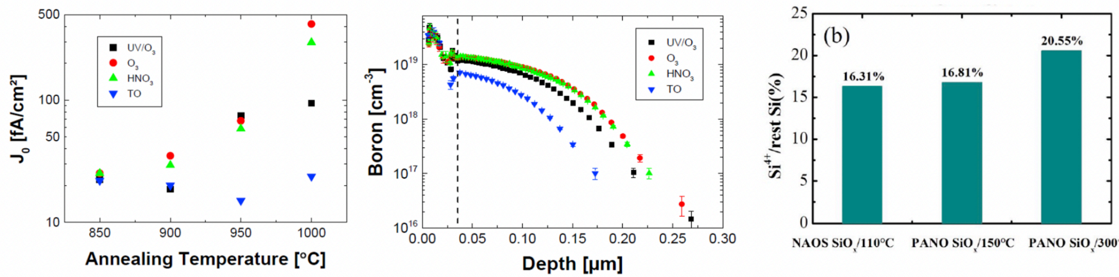


Figure 3.4: Different types of interfacial silicon oxide layers have various properties as reported by van der Vossen,R et al and Huang, Y et al. [37][85]

At first, the influences of three different types of tunnelling silicon oxides on the passivation of p^+ poly-Si(O_x) TOPCon are tested on n-type double side polished wafers. The tests adopt symmetric structure. The overview of the fabrication process is shown in Figure 3.5.

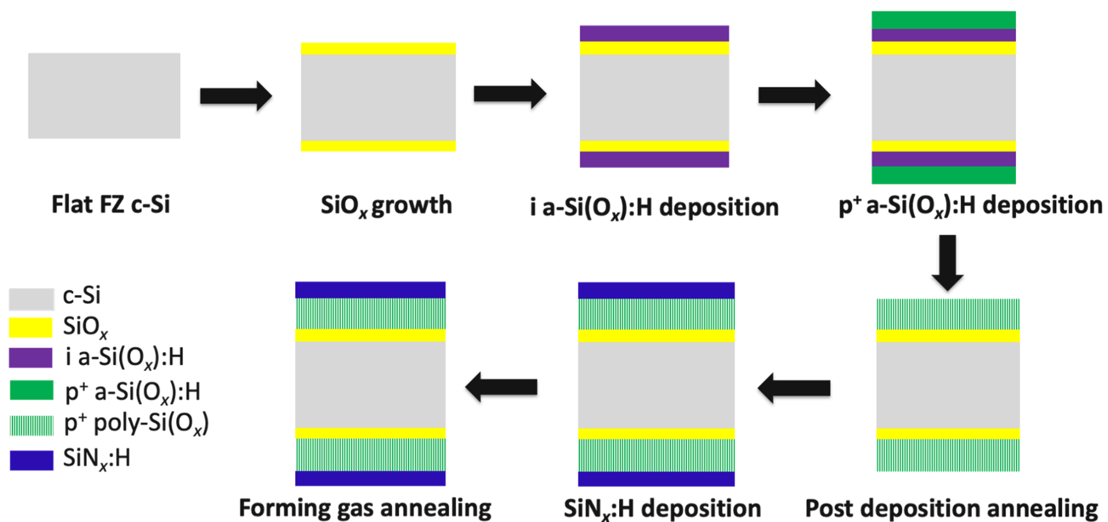


Figure 3.5: Fabrication process for experiments of different tunnelling silicon oxide types on DSP wafers

The interfacial tunnelling silicon oxides layer are created by three different methods, NAOS-SiO_x, PANO-

SiO_x and thermal oxide. The recipe for NAOS-SiO_x is immersing the samples in nitric acid (69.5%) for 1 hour. The expected silicon oxide thickness after NAOS-SiO_x is about 1.3 nm according to the research by Yang. et al[90]. Next, plasma-SiO_x is fabricated by plasma-enhanced chemical vapor deposition *AMOR*.The utilized recipe is shown in table 3.1. The expected silicon oxide thickness is also 1.3 nm after 9 minutes deposition [37]. In addition, the dry thermal oxidation is preformed in a TEMPRESS tube furnace at 675 °C duration for 3 minutes. The nitrogen gas flow and oxygen gas flow are 6.00 SLM and 0.60 SLM during the oxidation process, respectively. After measuring and fitting through spectral ellipsometer, the thickness of the silicon oxide by thermal oxide is also turns out to be around 1.3 nm.

Table 3.1: plasma-SiO_x tunnelling oxide layer PECVD parameters

RF power	Deposition gas and gas flow	Working pressure	Deposition time
1.5W	50sccm N_2O	0.08mbar	9minutes

Then, the intrinsic a-Si(O_x):H layer is also grown with plasma-enhanced chemical vapor deposition *AMOR*. The utilized recipe for intrinsic layer is shown in table 3.2. The intrinsic layer thickness is 10 nm after 1 minute and 8 seconds deposition.

Table 3.2: a-Si(O_x):H intrinsic layer PECVD parameters

RF power	Deposition gas and gas flow	Working pressure	Deposition time
5W	8sccm SiH_4,2sccm CO_2,100sccm H_2	2.00mbar	1minute 8seconds

Next, the boron doping layer is also fabricated by PECVD *AMOR*.The recipe is shown in table 3.3.The doping layer thickness is 20 nm after 2 minutes and 16 seconds deposition.

Table 3.3: p^+ a-Si(O_x):H doping layer PECVD parameters

RF power	Deposition gas and gas flow	Working pressure	Deposition time
5W	8sccm SiH_4,2sccm CO_2,5sccm B_2H_6,100sccm H_2	2.00mbar	2minutes 16seconds

Next, the samples are performed in a TEMPRESS tube furnace to carry out the high temperature post deposition annealing process. The annealing process starts from 600 °C to the peak temperature 900 °C. At 925 °C, the annealing process will last for 20 minutes with heating up rate 10 °C/minute. The aims of annealing are to anneal, activate and crystallize the a-Si(O_x):H layer, creating the p^+ poly-Si(O_x) layer. Then, the furnace will cool down to 600 °C with cooling down rate also 10 °C/minute.

Finally, the samples are processed by hydrogenation process. The standard hydrogenation process in PVMD group is firstly, PECVD 75nm SiN_x:H capping layer and then forming gas annealing duration for 30 minutes. PECVD equipment is OIPT Plasmalab 80plus from Kavli Nanolab. The utilized recipe is deposition gas and gas flow are 20 sccm SiH_4, 20 sccm NH_3 and then 980 sccm N_2. And the deposition duration is 5 minutes and 38 seconds on flat surface. The expected SiN_x:H capping layer thickness is around 75 nm which is optimum for optical performance of solar cell. Typically, the deposition substrate temperature is 400 °C. And the FGA furnace is Furnace A2 Annealing at Kavli Nanolab. Forming gas is 10% hydrogen in nitrogen by volume. The utilized recipe for FGA is forming gas volume=4.00 sccm , ramping up/down rate=10 °C/minute and peak temperature=400 °C which is the same as the SiN_x:H deposition. The forming gas annealing takes 30 minutes.

Next, the tests on textured surface are also performed.

The fabrication process of exploring the influences of three different types of tunnelling silicon oxides on the passivation of p^+ poly-Si(O_x) TOPCon on n-type DST wafers is shown in Figure 3.6. The fabrication process is almost the same as DSP wafers describing before. The difference is that the samples are required to be textured at first. The details of the texturing process are described in Chapter 2.

Typically, the texturing process utilized KOH particles and monoTEX additive at 82 °C duration for 8 minutes.

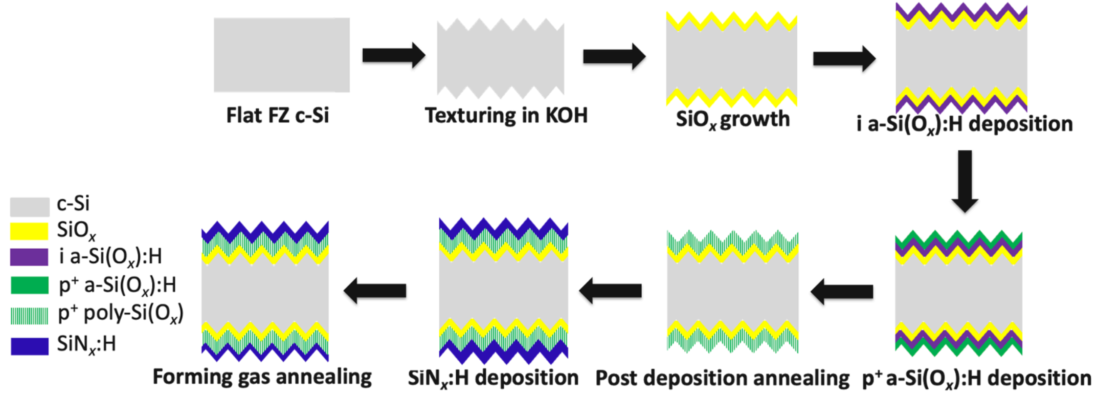


Figure 3.6: Fabrication process for experiments of different tunnelling silicon oxide types on DST wafers

Experiment results and discussion

Firstly, the influences of three different types of interfacial silicon oxides, NAOS-SiO_x, PANO-SiO_x and t-SiO_x on the passivation of p^+ poly-Si(O_x) passivating contact are tested on flat surface. The passivation results are shown in Figure 3.7 and Figure 3.8.From Figure 3.7, it can be shown that PANO-SiO_x sample has the lowest minority carrier lifetime both after post deposition annealing and hydrogenation, with 0.53 ms after PDA and 0.88 ms after hydrogenation. However, the NAOS-SiO_x sample and t-SiO_x has 2.49 ms and 1.37 ms minority carrier lifetime after PDA, respectively. From Figure 3.8, this phenomenon is more obvious. The PANO-SiO_x sample has the lowest iV_{oc} with 664 mV after PDA. However, the NAOS-SiO_x one has 699 mV iV_{oc} after PDA. And at the same time, the t-SiO_x one has almost 694 mV after PDA. The same situation can also be applied to the samples after hydrogenation. Therefore, it comes to the conclusions that PANO-SiO_x gives worse passivation quality than the two others.

Then, the tests on symmetric DST wafers are also carrier out to explore whether they have the same tendency as the experiments done on DSP wafers. The passivation results are shown in Figure 3.9 and Figure 3.10. From Figure 3.9, it can be shown that PANO-SiO_x sample still has the lowest minority carrier lifetime both after post deposition annealing and hydrogenation, with 0.159 ms after PDA and

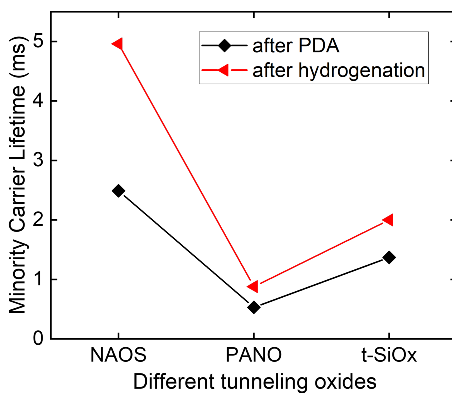


Figure 3.7: Minority carrier lifetime of three samples with different tunnelling silicon oxide types on DSP wafers

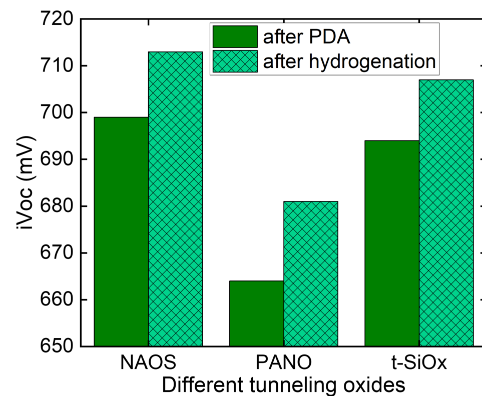


Figure 3.8: iV_{oc} of three samples with different tunnelling silicon oxide types on DSP wafers

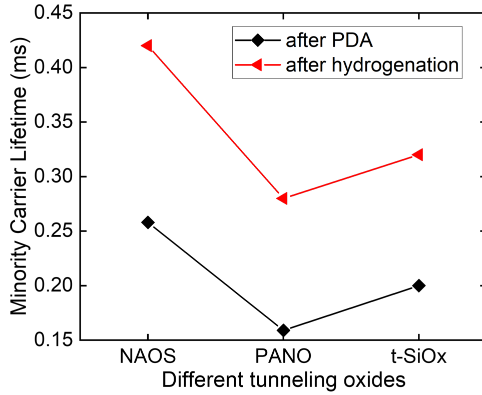


Figure 3.9: Minority carrier lifetime of three samples with different tunnelling silicon oxide types on DST wafers

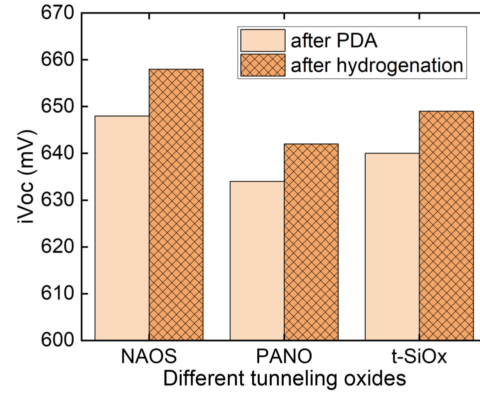


Figure 3.10: iV_{oc} of three samples with different tunnelling silicon oxide types on DST wafers

0.28 ms after hydrogenation. However, the NAOS-SiO_x sample and t-SiO_x has 0.258 ms and 0.2 ms minority carrier lifetime after PDA, respectively. From Figure 3.10, PANO-SiO_x sample also has the lowest iV_{oc} with 634 mV after PDA and 642 mV after hydrogenation. However, the NAOS-SiO_x one has 648 mV iV_{oc} after PDA. And at the same time, the t-SiO_x one has almost 640 mV after PDA. Thus, the conclusions are that PANO-SiO_x still give worst passivation results like the experiments done on flat surface. In addition, the passivation quality on textured surface is largely worse than on flat surface.

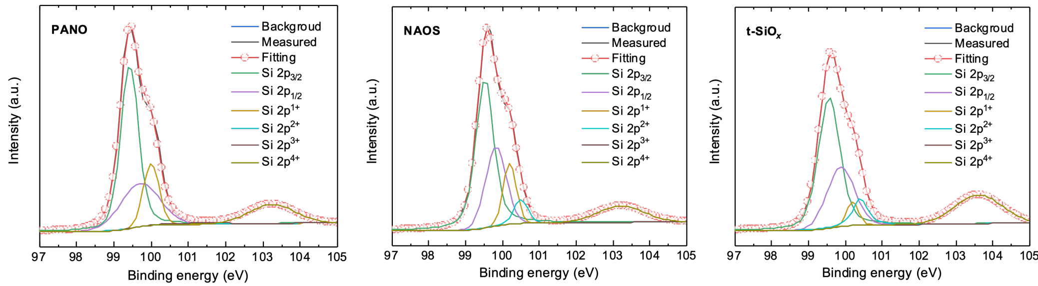


Figure 3.11: XPS measurement results of three different silicon oxide types

From the research by Huang.et al [37], it showed that post deposition annealing temperature, time, the thickness, uniformity of PANO-SiO_x and parameters during PECVD all can influence its quality as potential barrier. This may partially explain why PANO-SiO_x gives these bad passivation results. These parameters are hard to be all finely tuned and balanced. For example, changing the deposition time, the deposition gas flow, RF power, working pressure, substrate temperature during PECVD as well as the PDA thermal budget may all change the quality of PANO-SiO_x. It is difficult to control all the parameters and obtain PANO-SiO_x with good quality. Furthermore, it is guessed that plasma may cause damage on the c-Si surface which may bring more defect states. Therefore, the Auger recombination may become severer in this case. At the same time, it is assumed that the penetration of N into the ultra-thin SiO_x layer during the plasma assisted N_2O oxidation process resulted in realizing relatively poor passivation quality. Besides, it is found by Guo.et al that the optimized annealing temperature for realizing the best passivation quality was found to be different for the differently grown SiO_x layers[31]. Therefore, the optimum PDA temperature may still not be found for PANO-SiO_x since for comparing the results, here, all the samples are annealed at the same condition. PANO-SiO_x have large potentials to give better passivation. But, this thesis project is more concentrated on the optimization of p^+ poly-Si(O_x) passivating contacts and not just the function of interfacial tunnelling oxide. Therefore, PANO-SiO_x may be not suitable to be used for the following experiments.

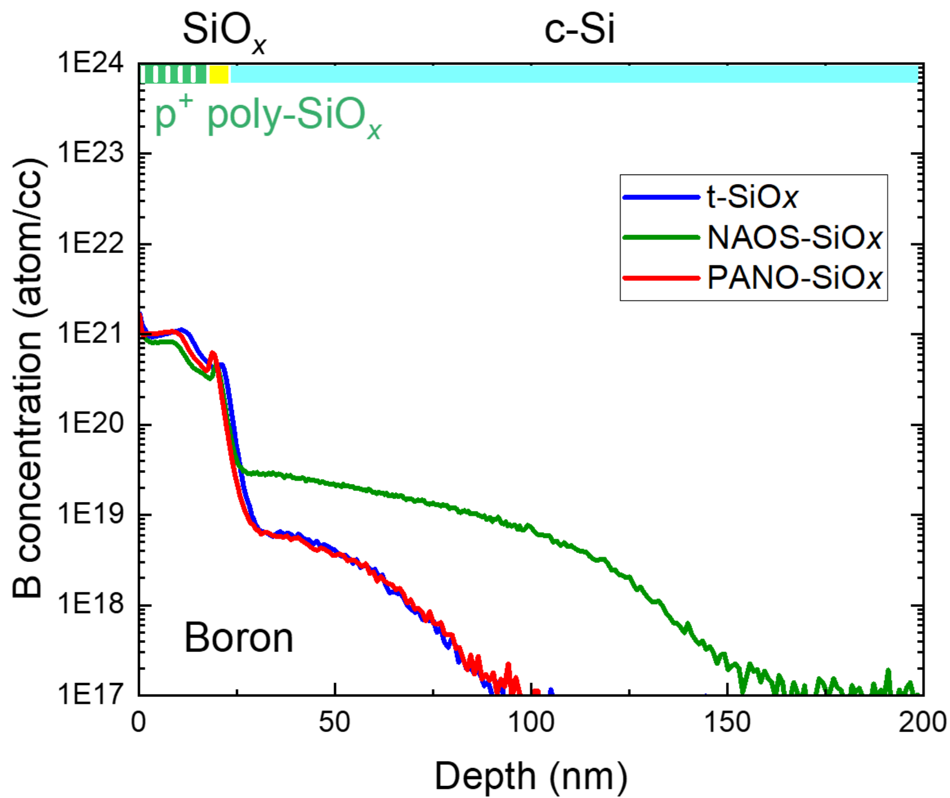


Figure 3.12: SIMS measurement results of three different silicon oxide types

Additionally, the samples with interfacial tunnelling oxides fabricated by different methods are also carried out the X-ray photoelectron spectroscopy (XPS) measurement. It is found that the differences between interfacial tunnelling oxides fabricated by various methods can result from the differences between stoichiometric Si^{4+} states. The results of XPS measurement Figure 3.11 and Table 3.4, the interfacial silicon oxide fabricated by thermal oxide has the highest quality with the highest Si^{4+} which means it is denser and therefore, has better functions as potential barrier than the two other approaches.This finding can also be found in SIMS results that can be seen in Figure 3.12. t-SiO_x has the highest quality that can reduce the in-diffusion of boron dopants into c-Si bulk from SIMS measurement. Then, the Auger recombinations in c-Si bulk can be reduced.

Table 3.4: XPS measurement results of three different silicon oxide types

	Si $2P_{3/2}$	Si $2P_{1/2}$	Si^{1+}	Si^{2+}	Si^{3+}	Si^{4+}
PANO-SiO_x	47.84%	23.83%	14.06%	0.58%	1.26%	12.42%
NAOS-SiO_x	47.46%	23.73%	11.70%	5.15%	0.93%	11.03%
t-SiO_x	46.33%	23.17%	0.38%	7.06%	0.48%	19.00%

3.3. Ultra-thin p$^+$ poly-Si(O_x) thin films

3.3.1. Intrinsic layer deposition methods

Experiment objectives and experiment method

After post deposition annealing, blisters are found on the surface of all the samples with PECVD method to fabricate the intrinsic a-Si(O_x):H layer. As reported by Choi. et al, it can attribute to the following possible reasons [8]. Firstly, the bad adhesion between SiO_x and intrinsic a-Si(O_x):H layer can cause blisters. Then, the stress accumulation between SiO_x and intrinsic layer during annealing can also induce blis-

tering conditions. Finally, blisters are formed through the release of hydrogen during high temperature annealing. More importantly, blisters will influence the passivation quality of p^+ poly-Si(O_x) passivating contact. Therefore, different tunnelling silicon oxide/intrinsic layer stack deposition methods are tested.

The structures which are shown in Figure 3.13 are utilized for testing the blistering conditions and the corresponding passivation quality. The changing of different interfacial tunnelling oxide fabrication process and different intrinsic layer deposition methods aims at changing the stress accumulation between SiO_x and intrinsic layer and see the results. The changing of the absorber surface morphology can be used to explore the influences of adhesion between SiO_x and intrinsic layer on the blisters.

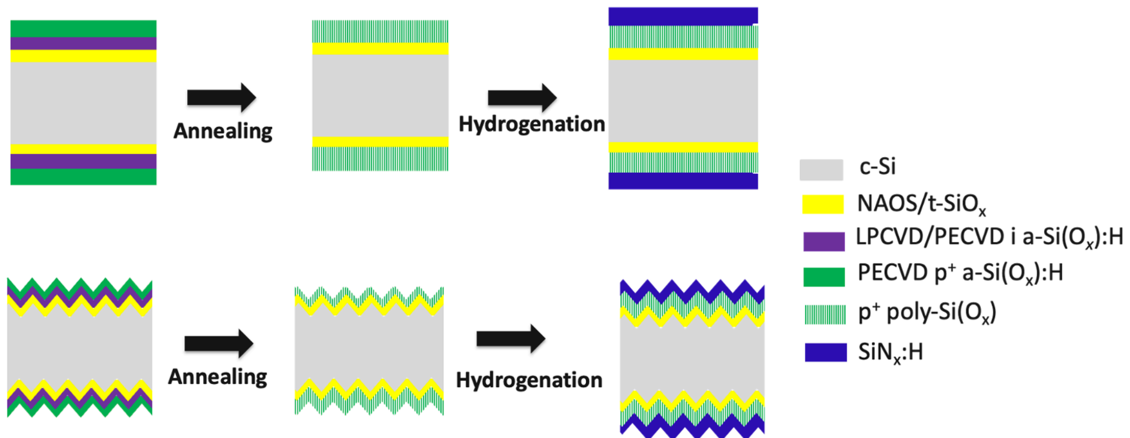


Figure 3.13: Structures for testing the blistering conditions and corresponding passivation quality

The fabrication process is almost the same as the aforementioned experiment on different silicon oxides types. However, typically, here, the intrinsic layers of two samples are processed by low-pressure chemical vapor deposition. The optimum recipe for LPCVD inside the PVMD group of TU Delft [89] has the following parameters. The deposition temperature is 580 °C. The deposition gas is SiH_4 and the corresponding gas flow is 45 sccm. The deposition rate is about 2 nm/min at present after testing. The expected thickness of intrinsic a-Si(O_x):H layer is 10 nm. Therefore, the deposition time is set at 5 minutes. In addition, for LPCVD, the samples are annealed for 1 hour at 600 °C after intrinsic layer deposition. The other utilized recipes are also the same as the former experiments.

Experiment results and discussion

Figure 3.14: Blistering conditions of different structures observed under optical microscope.

The samples mentioned above are observed under optical microscope. Several blisters are found on the sample with PECVD intrinsic a-Si(O_x):H layer from Figure 3.14. It can also be discovered that almost no blisters can be found when intrinsic layer is fabricated by LPCVD. It is mainly because that LPCVD can release the stress accumulation and improve the stress tolerance between SiO_x and intrinsic layer during its 1 hour post deposition annealing. Besides, it can also reduce the hydrogen release.

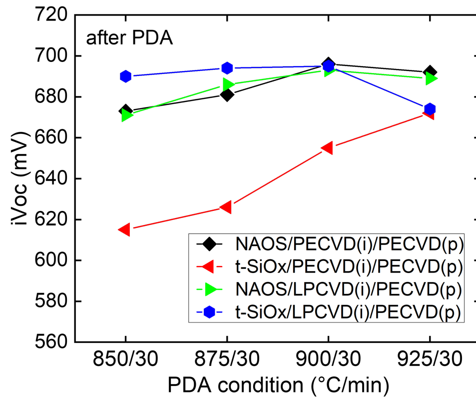


Figure 3.15: iV_{oc} of four different testing structures as above mentioned after different PDA conditions

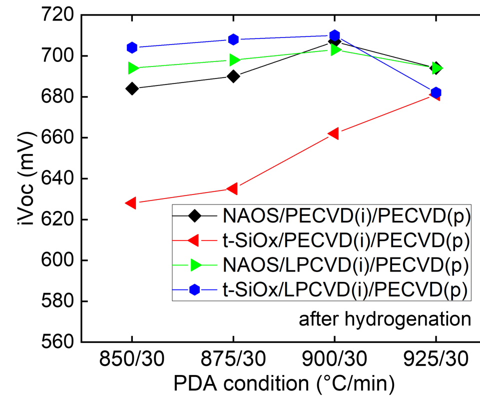


Figure 3.16: iV_{oc} of four different testing structures as above mentioned after hydrogenation

And at the same time, almost no obvious blisters are found on the sample with textured surface even the intrinsic layer is processed by PECVD method. This is mainly because that the roughness on textured surface can improve the adhesion between SiO_x and intrinsic layer. So, when intrinsic layer is processed by LPCVD on textured surface, the blistering conditions can almost be eliminated.

Next, the passivisation qualities of various tunnelling oxide/intrinsic layer stack deposition methods are tested. The passivation results are shown in Figure 3.15 and Figure 3.16. From the results, it can be discovered that the highest iV_{oc} after post deposition annealing is 696 mV obtained by t-SiO_x/LPCVD i a-Si(O_x):H/PECVD p^+ a-Si(O_x):H structure after annealing at 900 °C,duration for 30 minutes. The highest iV_{oc} after hydrogenation is 710 mV obtained also by this stack structure. And generally, sample with LPCVD intrinsic a-Si(O_x):H layer has better passivation quality than PECVD counterpart with higher iV_{oc} both after post deposition annealing and hydrogenation. The possible reason behind this is that LPCVD intrinsic a-Si(O_x):H layer can form denser barrier films and at the same time can reduce blisters largely. In addition, it can be seen that the structure of thermal silicon oxide, LPCVD intrinsic a-Si(O_x):H layer and then PECVD p^+ a-Si(O_x):H layer has the best passivation quality with 900 °C,duration for 30 minutes as the corresponding optimum post deposition annealing condition. When the PDA thermal budget is higher, the boron doapnts will in-diffuse too much that can cause severe Auger recombination. However, while the PDA thermal budget is lower, the dopants diffuse too little. The field effect passivation will be not enough which will also worsen the passivation quality. Therefore, 900 °C,duration for 30 minutes can be the optimum PDA condition.

At the same time, as mentioned above, t-SiO_x possessed highest stoichiometric Si^{4+} states which means it can give the highest quality SiO_x. And hence it may form more uniform and denser SiO_x thin films. Therefore, it can be deduced that it can give better passivation quality with lower number of interfacial defect states. Mandal. et al also reported that ultra-thin SiO_x tunnelling layer grown by thermal oxidation method demonstrated superior surface passivation quality for both polished and textured Si wafers (both n-type and p-type were used) compared to the oxide layer grown by either chemical oxidation or plasma oxidation method [46]. However, from the contact resistivity value, t-SiO_x samples was higher than its counterpart. But still the absolute value was quite low for enabling high efficiency TOPCon solar cells [29] that can be ignored. In addition, the thickness of t-SiO_x can be easily tuned by changing oxidation time, oxygen volume and oxidation temperature [52][53]. Next, with LPCVD to fabricate the intrinsic layer, the blistering conditions can largely be reduced. Finally, the structure of thermal silicon oxide, LPCVD intrinsic layer and then PECVD p^+ a-Si(O_x):H layer has the best passivation quality as described before. Therefore, this structure is used for the following experiments.

3.3.2. t-SiO_x layer thickness

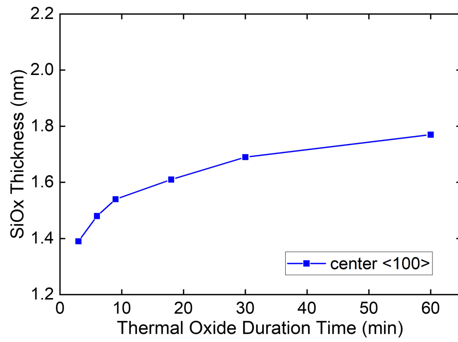


Figure 3.17: t-SiO_x thickness changes with oxidation time

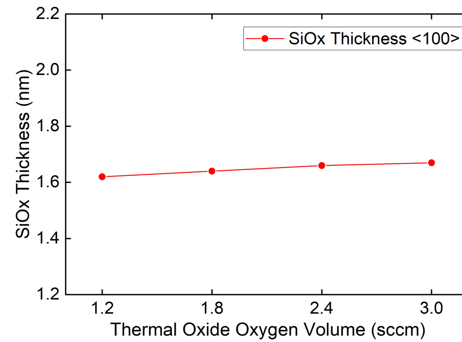


Figure 3.18: t-SiO_x thickness changes with oxygen volume ratio during thermally oxidation

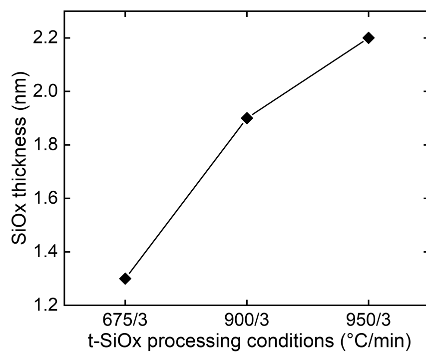


Figure 3.19: t-SiO_x thickness changes with oxidation temperature

Experiment objectives and Sample preparation

The thickness of t-SiO_x can be tuned by changing oxidation time, oxygen volume and oxidation temperature. In the following experiments, the thickness of t-SiO_x increased attempting to further reduce the Auger recombination which is induced by boron dopants diffusing into c-Si bulk layer.

At first, the process parameters that can have influences on the thickness of t-SiO_x are discovered to see whether and to what extent they can increase the thickness of t-SiO_x.

At first, the oxidation time during thermal oxidation can have influences on t-SiO_x thickness. Two <100> orientation DSP wafers are loaded into tube furnace as one group. The front side of the three wafers confront the oxygen and nitrogen gas flow. There are 6 groups of experiments with oxidation time, 3 minutes, 6 minutes, 9 minutes, 20 minutes, 30 minutes and 60 minutes, respectively. The temperature is 675 °C. The oxygen gas flow is 0.60 SLM. Nitrogen gas flow is 6.00 SLM during oxidation. And the thickness of the wafers are measured by spectral ellipsometer. The front side of the wafers that confront the gas flow is measured. And for each wafer, five points, up-left, up-right, down-left, down-right and center points are measured. And for each group, there are two wafers. Both of the two wafers are measured. Therefore, for each oxidation time, 10 data points can be obtained. Then, the average values can be acquired for each oxidation time and are plotted in one figure as is shown in Figure 3.17.From the figure, it can be found that t-SiO_x thickness increases with oxidation time, but the velocity becomes smaller and smaller. And typically, after 60 minutes oxidation, the t-SiO_x thickness will only reach 1.8 nm.

Then, the oxygen gas flow ratio during thermal oxidation can also affect the thickness of t-SiO_x. The original gas flow is 6.00 SLM nitrogen and 0.60 SLM oxygen during oxidation, respectively. And the total gas flow of these two gases are kept at 6.6 SLM constant. The ratio of oxygen gas flow increased.

The gas flows are 5.4 SLM nitrogen, 1.2 SLM oxygen; 4.8 SLM nitrogen, 1.8 SLM oxygen; 4.2 SLM nitrogen, 2.4 SLM oxygen oxygen; 3.6 SLM nitrogen, 3.0 SLM oxygen, respectively. Like the tests on oxidation time, here, for oxygen gas flow ratio, there are also two <100> orientation wafers one group that are loaded into tube furnace. Four groups are tested this time. And the oxidation other thermal oxidation conditions are kept constant, 675 °C oxidation temperature and 3 minutes oxidation time. The measurement procedure is the same as the tests on oxidation duration time. And the results ate plotted in Figure 3.18. From the figure, it can be found that increasing oxygen volume ratio during thermally oxidation does not has so much influence on the t-SiO_x thickness.

Eventually, t-SiO_x thickness can also be influenced by oxidation temperature. This experiment includes three groups. The oxidation temperature ramped up from 600 °C to 675 °C, 900 °C and 950 °C with 10 °C/minute, respectively. The oxidation time is kept constant at 3 minutes. And the gas flow is still 6.00 SLM nitrogen and 0.60 SLM oxygen during thermal oxidation. The measurement results are plotted and can be seen in Figure 3.19. It can be found that by increasing the oxidation temperature, the thickness of t-SiO_x can be easily increased. After 900 °C and 3 minutes oxidation, the thickness of t-SiO_x can reach 1.9 nm. And at the same time, after 950°C and 3 minutes oxidation, the thickness of t-SiO_x can reach almost 2.2 nm. Therefore, thicker t-SiO_x utilizing in the following experiments are all fabricated by higher oxidation temperature.

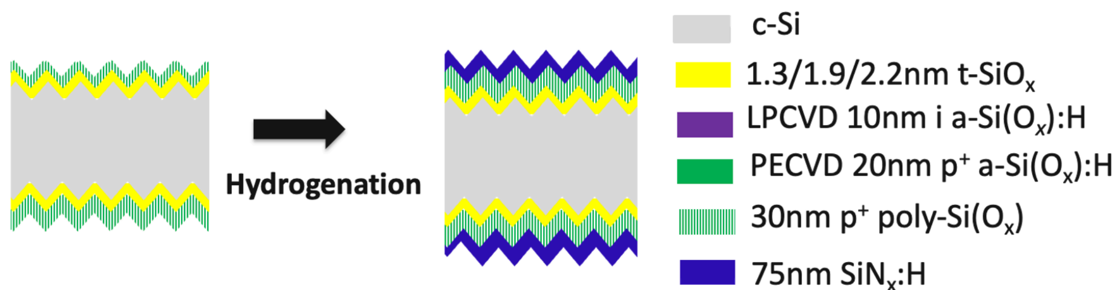


Figure 3.20: Simple schematic of the fabricated samples with thicker t-SiO_x

The fabrication process of the experiments on thicker t-SiO_x is as the following. 1.3 nm thermal oxidation is processed in TEMPRESS tube furnace at 675 °C duration for 3 minutes. 1.9 nm thermal oxidation is fabricated in the same furnace at 900 °C duration for 3 minutes. 2.2 nm thermal oxidation is created in also the same furnace at 950 °C duration for 3 minutes. During these 3 minutes oxidation time, the nitrogen and oxygen gas flow are 6.00 SLM and 0.60 SLM, respectively which are not changed. Especially, after thermally oxidation, the samples are required to be loaded into the LPCVD furnace within 5 minutes to preserve the stability and uniformity of t-SiO_x and prohibit the formation of unwanted native oxide layer. Additionally, after LPCVD intrinsic layer, the native oxide and formed oxide are required to be removed by immersing the samples into HF(0.55%) duration for 4 minutes which is an very important procedure before PECVD p^+ doping layer. The other fabrication procedures and recipes are the same as the aforementioned experiments.

Experiment results and discussion

The thickness of t-SiO_x increased trying to further reduce the Auger recombination which is induced by boron dopants diffusing into c-Si bulk layer.The passivation quality of p^+ poly-Si(O_x) passivating contact with thicker t-SiO_x are tested. The structure utilized for the test is shown in Figure 3.20. The passivation results can be found in Figure 3.21. The p^+ poly-Si(O_x) passivating contacts with 1.3 nm t-SiO_x as interfacial tunnelling oxide has 649.8 mV and 671.7 mV iV_{oc} after post deposition annealing and after hydrogenation, respectively. However, the p^+ poly-Si(O_x) passivating contacts with 1.9 nm t-SiO_x as tunnelling oxide has 647.1 mV and 664.5 mV iV_{oc} after post deposition annealing and after hydrogenation, respectively. And the p^+ poly-Si(O_x) passivating contacts with 2.2 nm t-SiO_x as tunnelling oxide has 640.6 V and 654.9 mV iV_{oc} after post deposition annealing and after hydrogenation, respectively. It can be found that by increasing the t-SiO_x thickness, the passivation results reduced

than the original one with 1.3nm t-SiO_x. In addition, the thicker the t-SiO_x layer is, the worse the passivation quality is which can also be discovered in Figure 3.21.

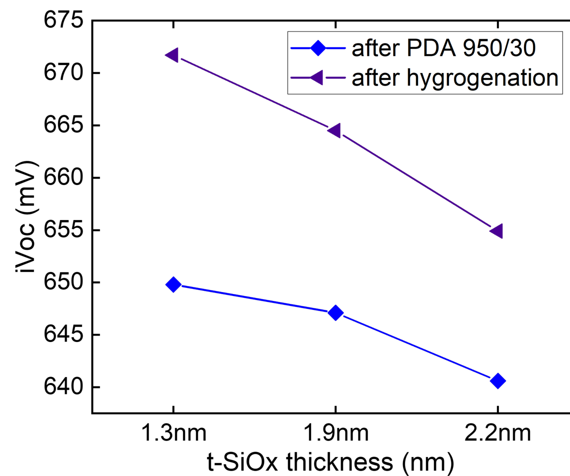


Figure 3.21: Passivation results of samples with thicker t-SiO_x tunnelling layer

As above mentioned, since t-SiO_x is very dense. Therefore, it can be assumed that with thicker t-SiO_x layer, it may have better function as potential barrier to prohibit the boron dopants from diffusing into the c-Si bulk layer. This may further reduce the Auger recombination. Therefore, originally, through increasing the thickness of t-SiO_x layer, the passivation results of p^+ poly-Si(O_x) passivating contact are ought to be better. However, at the same time, it can also be guessed that by increasing the thickness of t-SiO_x, the charge carriers are more difficult to tunnel through the interfacial tunnelling oxide layer. This may lead to reduction of collection of charge carriers. However, whether the collection of charge carriers are really reduced can also partially represent by fill factor after fabricating the solar cell. Only through the iV_{oc} which represents the passivation results, it cannot thoroughly show the reduction of charge carriers collection. Thus this may only be one of the possible reasons that may explain why the passivation quality decreases with thicker t-SiO_x tunnelling oxide layer.

3.3.3. Pre-annealing

Experiment objectives and Sample preparation

In 2016, Peibst. et al reported that the lateral homogeneous tunnelling is not solely responsible for the flow of charge carriers through the ultra-thin tunnel oxide layer. Transportation of charge carriers at poly-Si/c-Si junctions might be affected due to the localized current flow through the pinholes [69]. Lancaster. et al. also studied the formation and the influential effect of pinholes on the charge carrier transport mechanism through ultra-thin SiO_x layers. The charge carriers can diffuse through the silicon oxide potential barrier by tunnelling and also by pinholes that can assist the charge carriers diffuse through the potential barrier especially when the thickness of t-SiO_x is larger than 1.7 nm [44].

In addition, the correlation of annealing temperature and the pinhole density was investigated and the magnitude of the pinhole densities was found to be increased with the increment of annealing temperature [44][9]. It is measured that increment of annealing temperature from 800 °C to 950 °C raised the density of pinholes by a factor of 3 [44]. The pinholes can only exist when the post deposition annealing temperature is high enough. Normally, the annealing temperature is ought to be larger than 900 °C [29]. Furthermore, the simulation results demonstrated that for a thicker SiO_x layer solely quantum mechanical tunnelling can't provide sufficient carrier transport channels and due to which series resistance values gets increased. This resulted in obtaining lower FF. And suitable amount of carrier transport through pinholes may maximize the FF and thus the power conversion efficiency of the TOPCon solar

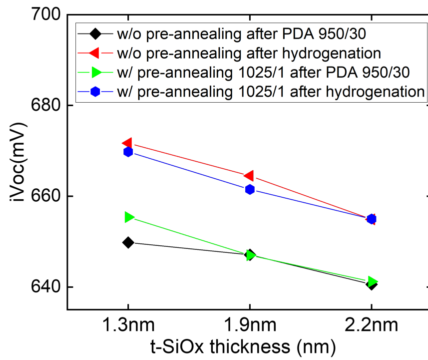


Figure 3.22: Passivation results of p^+ poly-Si(O_x) passivating contacts with thicker t-SiO$_x$ tunnelling layer and pre-annealing 1025/1

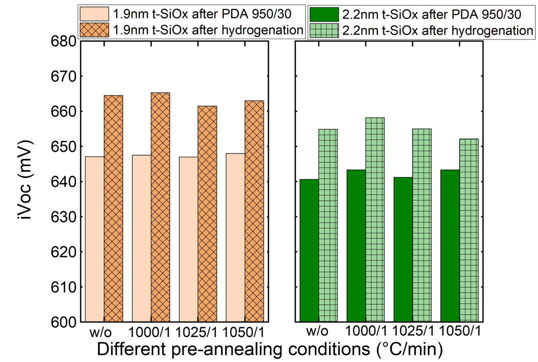


Figure 3.23: Passivation results of p^+ poly-Si(O_x) passivating contacts with thicker t-SiO$_x$ tunnelling layer and different pre-annealing conditions ranging from 1000/1 to 1050/1

cells[94].

There are generally two approaches to open more pinholes to assist the tunnelling. The first one is through further increasing the post deposition annealing temperature to directly open more pinholes during crystallization [44]. The other possible way is to add pre-annealing step before boron doping layer deposition. It is assumed that this approach may separate the formation of pinholes and boron dopants diffusion, crystallization which may be better to control the doping profile. Therefore, pre-annealing step before p^+ doping layer deposition is tried to open more pinholes assisting the tunnelling in this experiment.

Firstly, the pre-annealing process is done in TEMPRESS furnace tube with annealing temperature 1025 °C, ramping up rate 10 °C/minute and duration for 1 minute. And here, the post deposition annealing thermal budget is 950 °C duration for 30 minutes. The samples are three symmetric p^+ poly-Si(O_x) passivating contacts with different t-SiO$_x$ tunnelling oxide thickness, 1.3 nm, 1.9 nm and 2.2 nm, respectively. The other fabrication processes are the same as the experiments on thicker t-SiO$_x$. The experiment aims to explore whether and to what extent, the pre-annealing can open more pinholes and help the charge carrier transporting for thicker t-SiO$_x$ interfacial tunnelling oxide.

Moreover, the pre-annealing conditions are also changed. The pre-annealing temperatures are ranging from 1000 °C to 1050 °C with 25 °C as interval. And the samples without pre-annealing are used as references. Here, two testing structures are utilized. One is symmetric p^+ poly-Si(O_x) passivating contacts with 1.9 nm t-SiO$_x$. The other is symmetric p^+ poly-Si(O_x) passivating contacts with 2.2 nm t-SiO$_x$ on textured surface. And here, post deposition annealing condition is still kept stable at 950 °C duration for 30 minutes for comparing the results. In addition, iV_{oc} is utilized to characterize the passivation quality of p^+ poly-Si(O_x) passivating contact.

Experiment results and discussion

The first experiment about pre-annealing is carried out to explore whether pre-annealing can improve the passivation of p^+ poly-Si(O_x) passivating contacts. The passivation results are plotted in Figure 3.22. The results can also be seen from Table 3.5. From these data values above, it can be demonstrated that with pre-annealing procedure before p^+ doping layer deposition, there are few improvements on the passivation quality of p^+ poly-Si(O_x) passivating contact with thicker t-SiO$_x$.

The second experiment about pre-annealing is done to discover which pre-annealing conditions can give best passivation for p^+ poly-Si(O_x) passivating contacts. Since, maybe the optimum pre-annealing condition is still not figured out that cause the above mentioned conclusion. The results can be seen in Figure 3.23. However, from the figure, it can also be observed that with pre-annealing procedure and

Table 3.5: Passivation of p^+ poly-Si(O_x) passivating contacts of different t-SiO_x thickness and with or without pre-annealing

t-SiO_x thickness	1.3nm	1.9nm	2.2nm
iV_{oc} w/ pre-annealing after PDA	655.4mV	647mV	641.2mV
iV_{oc} w/o pre-annealing after PDA	649.8mV	647.1mV	640.6mV

changing the pre-annealing temperature from 1000 °C to 1025 °C, 1050 °C before p^+ doping layer deposition, there are few improvements on the passivation quality for p^+ poly-Si(O_x) passivating contact with thicker t-SiO_x. iV_{oc} are 647.1 mV, 647.5 mV, 647 mV and 648 mV for 1.9 nm t-SiO_x samples without pre-annealing, with 1000 °C/1 minute pre-annealing, with 1025 °C/1 minute pre-annealing and 1050 °C/1 minute pre-annealing, respectively. This tendency also can be applied to 1.9 nm t-SiO_x samples after hydrogenation and 2.2 nm t-SiO_x samples after PDA and hydrogenation. The results are not as well as expected. In addition, pre-annealing will introduce new variables for the following experiments. Therefore, the pre-annealing process may be not suitable for the following experiments. Furthermore, the passivation quality of p^+ poly-Si(O_x) passivating contact with thicker t-SiO_x on textured surface is still worse than the original one with thinner 1.3 nm t-SiO_x. Thus, p^+ poly-Si(O_x) passivating contact with optimum 1.3 nm t-SiO_x without pre-annealing is still utilized to carry out the following tests.

Here, the post deposition annealing temperature is not changed for comparison. However, it is assumed that with pre-annealing, the optimum post deposition annealing for the samples may also possibly reduce since the thermal budget for crystallizing, diffusing is enough. And therefore, it is guessed that different pre-annealing conditions may match with different optimum post deposition annealing conditions. In addition, different t-SiO_x thickness may also require different post deposition annealing conditions. The thicker t-SiO_x may be better potential barrier to keep the boron dopants from in-diffusing. Therefore, it can be deduced that thicker t-SiO_x may require higher annealing thermal budget. Thus, maybe the following researchers may further explore these phenomenons and try to form silicon oxide thickness, pre-annealing conditions mapping with different post deposition annealing conditions.

3.3.4. PECVD p^+ doping layer optimization

O,B concentration and p^+ layer thickness optimization

The influences of p^+ doping layer are discovered in this section. PECVD deposition parameters include working pressure, RF power, gas flow, deposition time and .etc. The gas flow can decide the doping profile and the crystallization fraction. For example, for p^+ poly-Si(O_x) passivating contacts, the diborane and carbon dioxide gas flow during PECVD can change the B concentration and O concentration to shape the doping profile and change the crystallization fraction, respectively. In addition, the deposition time during PECVD can change the thickness of boron doping layer. Therefore, in this part, B concentration, O concentration and p type a-Si(O_x):H layer thickness during PECVD are changed to see the corresponding changes of passivation results.

Experiment objectives and Sample preparation

The boron doping layer is fabricated by PECVD *AMOR*.The recipe for changing the O concentration during PECVD is shown in Table 3.6. To change the oxygen concentration, the CO_2 gas flow during PECVD is changed from 0.0 sccm to 10.0 sccm with 2.5 sccm as interval. The boron doping layer is kept stable at 20 nm during deposition. The recipe for changing the B concentration during PECVD is illustrated in Table 3.7. To change the boron concentration, the B_2H_6 gas flow during PECVD is changed from 0.0 sccm to 40.0 sccm with 10.0 sccm as interval.

Table 3.6: The recipe for changing the O concentration during PECVD on flat surface

RF power	Deposition gas,gas flow	Pressure	Deposition time
5W	8sccm SiH_4,0.0-10.0sccm CO_2,5sccm B_2H_6,100sccm H_2	2.00mbar	2minutes 16seconds

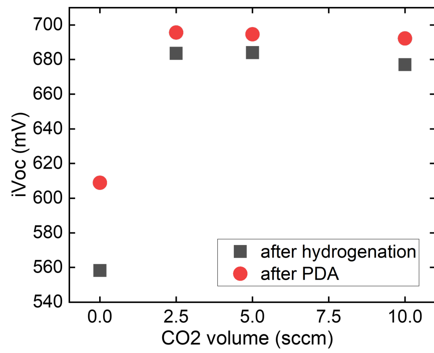


Figure 3.24: Passivation results of p+ poly-Si(O_x) passivating contacts with different O concentration during PECVD p+ doping layer

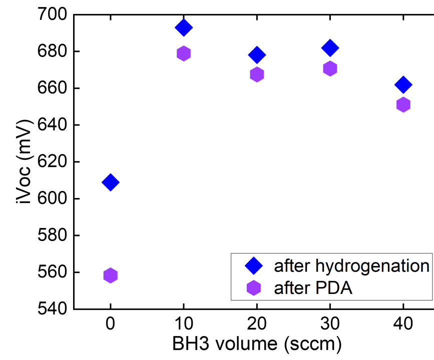


Figure 3.25: Passivation results of p+ poly-Si(O_x) passivating contacts with different B concentration during PECVD p+ doping layer

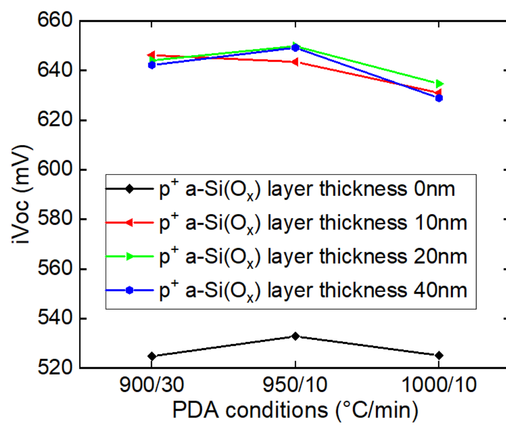


Figure 3.26: Passivation results of p+ poly-Si(O_x) passivating contacts with different p+ doping layer thickness during PECVD

Table 3.7: The recipe for changing the B concentration during PECVD on flat surface

RF power	Deposition gas,gas flow	Pressure	Deposition time
5W	8sccm SiH_4,2sccm CO_2,0.0-10.0sccm B_2H_6,100sccm H_2	2.00mbar	2minutes 16seconds

At the same time, the recipe for changing the p^+ doping layer thickness during PECVD is RF power=5 W, deposition gas=8.0 sccm SiH_4, 2.0 sccm CO_2, 5.0 sccm B_2H_6 and then 100.0 sccm H_2, deposition pressure=2.00 mbar,deposition duration=1 minute and 37 seconds on textured surface for 10nm p^+ layer thickness, deposition duration=3 minutes and 14 seconds for 20nm p^+ layer thickness, deposition duration=6 minutes and 28 seconds for 40nm p^+ layer thickness.

Experiment results and discussion

The optimum carbon dioxide gas flow can be seen in Figure 3.24. When carbon dioxide gas flow is 5.0 sccm, the iV_{oc} of p^+ poly-Si(O_x) passivating contacts gives best results after PDA and after hydrogenation with 684 mV and 695.6 mV, respectively. Therefore, the optimum carbon dioxide gas flow is 5.0 sccm. It is mainly because that when carbon dioxide gas flow is 5.0 sccm, poly-SiO_x is in a mixed-phase crystalline structure including large-size crystalline grains embedded in an a-SiO_x:H matrix that can provide an excellent tradeoff among the conductivity, passivation quality, and transparency [62]. When the carbon dioxide gas flow is less, poly-SiO_x is in a high crystalline phase. And when the carbon dioxide gas flow is more, poly-SiO_x is in an amorphous phase. Both of them is not beneficial to the passivation quality.

In the meanwhile, the optimum diborane gas flow can be discovered in Figure 3.25. It can be found that when the diborane gas flow is 10.0 sccm, the iV_{oc} of p^+ poly-Si(O_x) passivating contacts can give best results also both after PDA and after hydrogenation with 678.9 mV and 693 mV, respectively. Thus, the optimum diborane gas flow is 10.0 sccm. The diborane gas flow during PECVD can shape the doping profile of the p^+ poly-Si(O_x) passivating contacts. It can be deduced that too much diborane, the Auger recombination in the c-Si bulk layer will become severe. Too little diborane, the field effect passivation may be not strong enough to form good passivation quality.

Then, when the thickness of p^+ poly-Si(O_x) passivating contact is less than 50 nm, the highest iV_{oc} value is 649.8 mV with 20 nm p^+ a-Si(O_x):H layer. Therefore, the optimum p type a-Si(O_x):H layer thickness is 20 nm that can be discovered in Figure 3.26. In addition, from Figure 3.26, it can also be found that post deposition annealing temperature 950 °C duration for 10 minutes is the corresponding optimum PDA condition for 20nm p^+ boron doping layer on DST wafers.

3.4. Optimization of hydrogenation scheme

Experiment objectives and Sample preparation

From SIMS results that can be discovered in Figure 3.27 and Figure 3.28, it can show that the hydrogen in p^+ poly-Si(O_x) passivating contact is lower than in n^+ poly-Si(O_x) passivating contact which means that the hydrogen chemical passivation is worse in p^+ poly-Si(O_x) passivating contact. Therefore, optimization of the hydrogenation process is also essential for optimizing the passivation quality of p^+ poly-Si(O_x) passivating contact. The standard process for hydrogenation process used within PVMD research group is 75 nm SiN_x:H capping layer PECVD and then forming gas annealing at 400 °C that is the same temperature as the deposition substrate and duration for 30 minutes. According to [5] and Figure 3.29, it shows that AlO_x:H/SiN_x:H capping layers stack can have better passivation quality and AlO_x:H/SiN_x:H/AlO_x:H capping layers structure can have even better passivation results. In addition, the post capping layer deposition annealing conditions like FGA or firing can also have influences on the passivation quality after hydrogenation which is shown in Figure 3.30. As a result, the following experiments about the optimization of hydrogenation process for p^+ poly-Si(O_x) passivating contact are carrier out.

The deposition of aluminium oxide(AlO_x:H) capping layer uses thermal atomic layer deposition (ALD)

equipment from Oxford Instruments at Kavli Nanolab. The deposition temperature is set at 105 °C. The precursor gases used in ALD are water and trimethylaluminium (TMA).During the ALD process, at first, one of the precursor gas, water is coated with the other precursor gas, TMA. Then, after that, the leftover TMA and the excess by-products are purged. Next, water is purged in to react with TMA to form the first layer of AlO_x:H and finish the first cycle. Eventually, the leftover water is purged out and then the following mentioned cycle is repeated. In this experiment, the number of cycles repeated is 312. After 312 cycles, the thickness of AlO_x:H layer is approximately 20 nm. After aluminium oxide deposition, the 75 nm SiN_x:H is deposited by PECVD equipment also at Kavli Nanolab. The substrate temperature is set at 400 °C and the deposition duration time is 8 minutes for textured surface. Finally, the samples are loaded into TEMPRESS furnace tube to carry out FGA. Apart from ALD, the other steps and corresponding recipes have been described before.

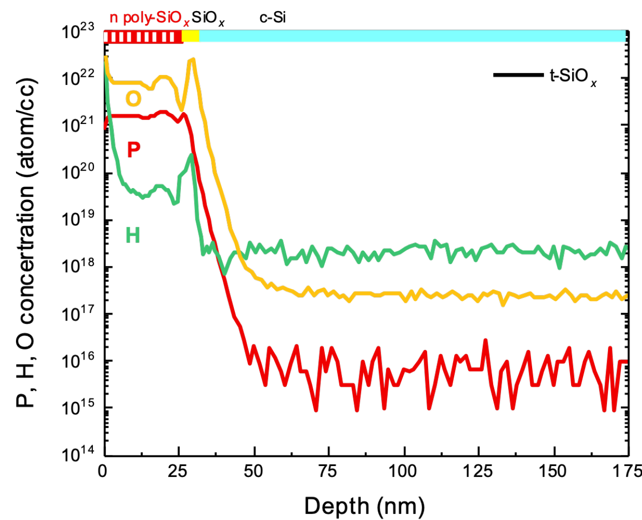


Figure 3.27: SIMS results of n^+ poly-Si(O_x) passivating contacts

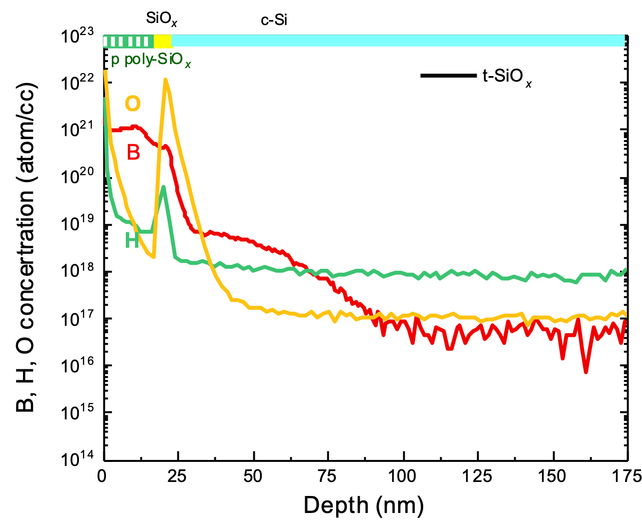


Figure 3.28: SIMS results of p^+ poly-Si(O_x) passivating contacts

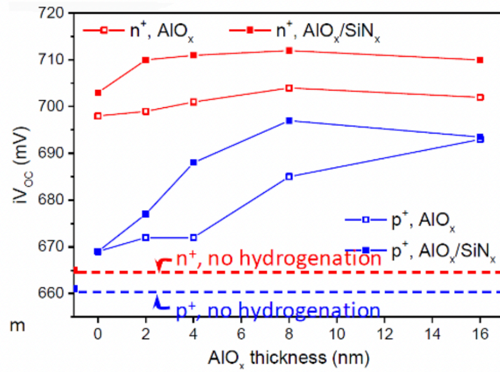


Figure 3.29: The passivation results with AlO_x:H and AlO_x:H/SiN_x:H as capping layer(s) during hydrogenation process[5]

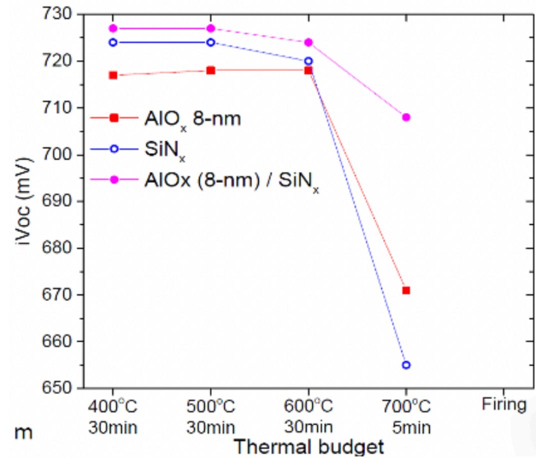


Figure 3.30: The passivation results with different capping layer(s) during hydrogenation process and the corresponding different post deposition annealing conditions[5]

Experiment results and discussion

The optimization of hydrogenation process on 110 nm p^+ poly-Si(O_x) passivating contact with 10 nm intrinsic layer and 100 nm p^+ doping layer which has the optimum passivation within thicker p^+ poly-Si(O_x) passivating contact (>50 nm) from aforementioned experiments are carried out. It comes to the conclusions that with ALD AlO_x:H and PECVD SiN_x:H stacks as capping layer, the passivation of 110 nm p^+ poly-Si(O_x) passivating contact has better quality that are shown in Table 3.8. The implied open circuit voltage approaches 686 mV and minority carrier lifetime approaches 1 ms. The passivation results are the best for the time being. It illustrates that AlO_x:H/SiN_x:H stacks as capping layer can really improve the passivation. Therefore, AlO_x:H/SiN_x:H/AlO_x:H (ANA) stacks as capping layer during hydrogenation may have even better passivation results which can be carried out by the following researchers.

Table 3.8: The iV_{oc} and minority carrier lifetime of samples with ALD AlO_x:H and PECVD SiN_x:H stacks as capping layer for the optimization of hydrogenation process

Different hydrogenation process	SiN_x:H+FGA	AlO_x:H+SiN_x:H+FGA
Minority carrier lifetime	0.77 ms	0.98 ms
iV_{oc}	674 mV	685 mV

3.5. TCO sputtering damage

The p^+ poly-Si(O_x) passivating contacts are required to be applied in double-side textured c-Si solar cell. There are two approaches to complete the metallization process. Firstly, with ultra-thin p^+ poly-Si(O_x) passivating contacts, TCO is required to increase the lateral conductivity. Solar cells are assisted by TCO to collect charge carriers and at the same time, guiding the incident light. TCO sputtered at the front of the solar cell can act as an transparent electrode with both good electrical and optical performance. For electrical performance, it can transport the photogenerating electrons to the external electrical circuit which can also form the current loop. Therefore, the efficiency of the solar cell can be improved. For optical performance, the incident light is guided by it directly to the active layer.

However,the energy required for hydrogen to form bonds to the silicon from a crystalline silicon surface or an amorphous silicon substrate is much lower than the energy during TCO sputtering when the high-energy particles bombardment on the substrates.Therefore, the silicon hydrogen bond can be easily broken during TCO sputtering. The chemical passivation decreases and at the same time,the defect densities increase. These phenomenons will cause the sputtering damage on the passivation

and further lead to the degradation of solar cell performance[2]. Therefore, the TCO sputtering damage on p^+ poly-Si(O_x) passivating contact is also necessary to explore. TCO sputtering damage on p^+ poly-Si(O_x) passivating contact of textured surface are discovered in the following experiment.

Experiment objectives and Sample preparation

Typically, after hydrogenation, the SiN_x:H capping layer is removed and then sputtering indium tungsten oxide (IWO) as TCO to increase the lateral conductivity. However, the sputtering process can cause sputtering damage on p^+ poly-Si(O_x) passivating contact that can cause passivation quality degradation. It is assumed that the sputtering damage may partially attribute to the work function mismatching of p^+ poly-Si(O_x) passivating contact and TCO. The fermi level of TCO is close to the conduction band but the fermi level of p^+ poly-Si(O_x) passivating contact is closed to the valence band that will form a work function mismatch and potential barrier.The damage can partially be recovered by oven annealing 180 °C duration for 10 minutes because of the broken silicon oxide or silicon hydrogen bonds by sputtering can be formed again after annealing. The fabrication flowchart of IWO sputtering damage on textured p^+ poly-Si(O_x) passivating contact can be discovered in Figure 3.31.

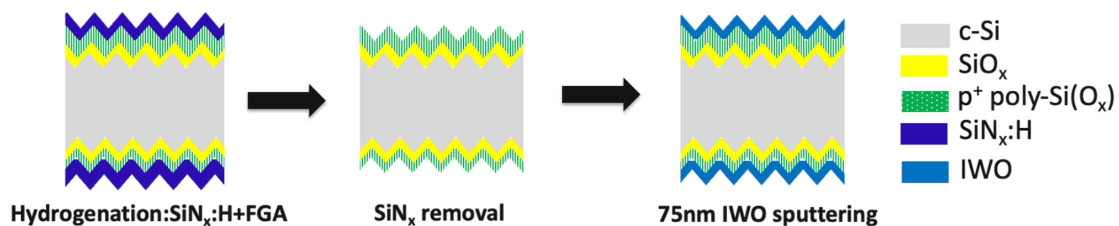


Figure 3.31: Fabrication process of IWO sputtering damage on textured p^+ poly-Si(O_x) passivating contact

Experiment results and discussion

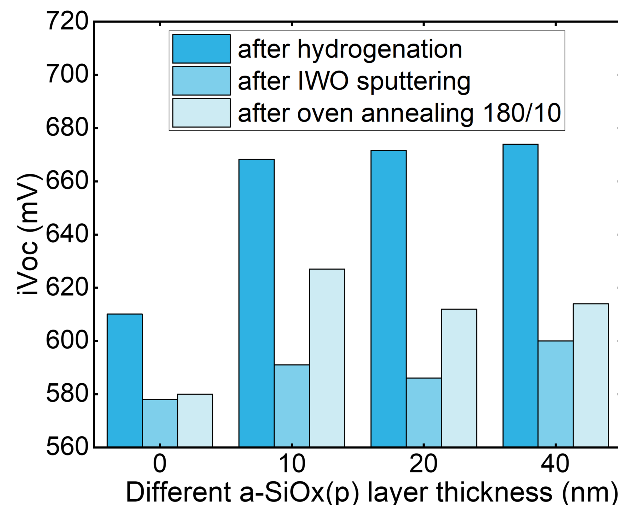


Figure 3.32: The influences of p^+ doping layer thickness during PECVD on the TCO sputtering damage of textured surface

The TCO sputtering damage of different p type a-Si(O_x):H layer thickness during PECVD for DST wafers are explored. The results can be seen in Figure 3.32 and Figure 3.33. From Figure 3.33, it can be found that when boron doping layer thickness is 20 nm, the sputtering damage is the highest both after sputtering and after oven annealing recovery. The iV_{oc} losses are 85.6 mV and 59.6 mV

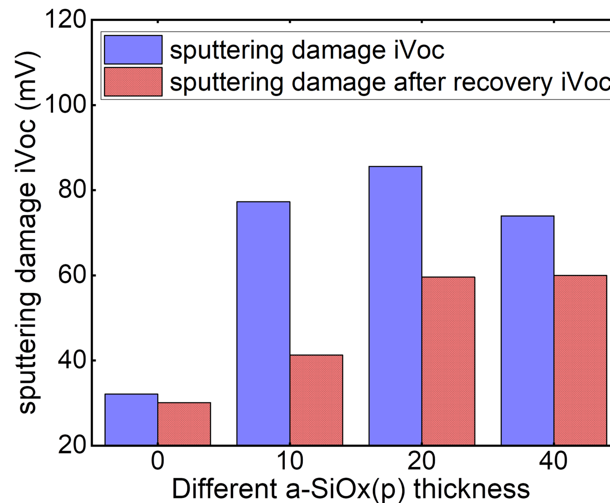


Figure 3.33: The corresponding iV_{oc} degradation caused by IWO sputtering before and after oven annealing recovery

after sputtering and annealing recovery, respectively. In addition, the sputtering damage of the other thickness that is thinner than 50 nm is also very large both after sputtering and recovery. Therefore, the conclusions are that after measuring, the iV_{oc} losses after TCO sputtering are 70-90 mV. And the losses are still 40-60 mV after 180°C and 10 minutes oven annealing recovery. The sputtering damage is difficult to be mitigated.

3.6. Thick p^+ poly-Si(O_x) thin films

When the thickness of p^+ doping layer is over 50 nm, the lateral conductivity of it is good enough. Therefore, the thick p^+ poly-Si(O_x) passivating contacts can directly contact with metal. This is the second method of metallization. Therefore, in this section, the optimization of thicker p^+ poly-Si(O_x) passivating contact which exceeds 50 nm is discovered.

The reasons are as the followings. Firstly, only the TCO sputtering damage on p^+ poly-Si(O_x) passivating contact with p^+ layer thickness less than 50 nm is discovered. IWO sputtering damage on p^+ poly-Si(O_x) passivating contact with thickness less than 50 nm of textured substrate is severe even after annealing recovery as the above mentioned. However,the situations are still unclear when p^+ poly-Si(O_x) passivating contact becomes thicker.

Next, when the p^+ doping layer of p^+ poly-Si(O_x) passivating contact exceeds 50 nm, the lateral conductivity of p^+ poly-Si(O_x) passivating contact is good enough. Therefore, no TCO is required when thicker p^+ poly-Si(O_x) passivating contact is situating at the rear side such as i-TOPCon solar cell. This can largely reduce rear side passivation quality degradation and remove the sputtering damage at rear side. For i-TOPCon solar cell, n^+ emitter is situating at the front side. Then, no sputtering damage will exist in this type of solar cell. The schematic of i-TOPCon solar cell can be discovered in Figure3.34.

In addition, for poly-poly solar cell that can be found in Figure 3.35, to reduce the light absorption at the front side, only TOPCon with thickness less than 50 nm can be accepted at the front side. But the rear side can still adopt thicker TOPCon to reduce passivation degradation. And TCO sputtering damage is smaller on n^+ poly-Si(O_x) passivating contact than on p^+ poly-Si(O_x) passivating contact because the work function mismatch between n^+ poly-Si(O_x) passivating contact and TCO is smaller than that between p^+ poly-Si(O_x) passivating contact and TCO. As a result, for poly-poly solar cell, with thin n^+ poly-Si(O_x) passivating contact, TCO situating at the front side and thicker p^+ poly-Si(O_x) passivating

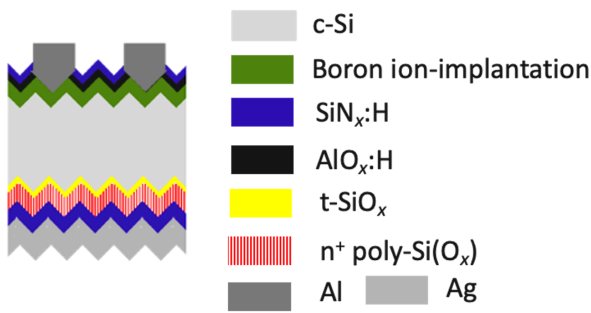


Figure 3.34: Simple schematic of i-TOPCon solar cell

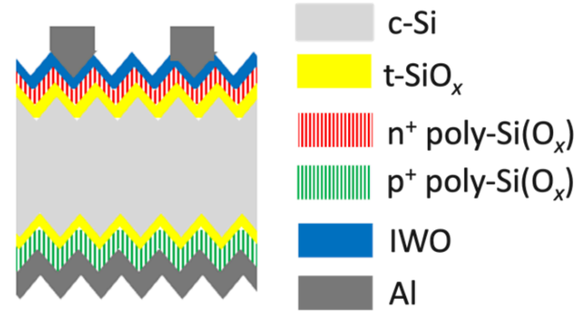


Figure 3.35: Simple schematic of poly-poly solar cell

contact situating at the rear side, the passivation damage can be largely reduced.

Due to the above-mentioned reasons, the optimization of thicker p^+ poly-Si(O_x) passivating contact (>50 nm) on textured surface is necessary.

3.6.1. p^+ doped layer thickness

Experiment objectives and Sample preparation

The experiment aims at discovering the optimum boron doping layer thickness when the thickness of p^+ poly-Si(O_x) passivating contact exceeds 50 nm. Through this, the lateral conductivity is good enough and the TCO will not be used on the p^+ poly-Si(O_x) TOPCon. Therefore, the TCO sputtering damage that is hard to be recovered can be eliminated. In addition, the passivation situation of thick p^+ poly-Si(O_x) passivating contact is still unclear. Therefore, it is fascinating to be explored.

The fabrication process of different boron doping layer thickness is shown as the following. The boron doping layer is fabricated by PECVD *AMOR*.The recipe for changing the thickness of p^+ doping layer during PECVD for achieving thick p^+ poly-Si(O_x) passivating contact is RF power=5 W, deposition gas, gas flow=8.0 sccm SiH_4, 5.0 sccm CO_2, 10.0 sccm B_2H_6 and then 100.0 sccm H_2, working pressure=2.00 mbar,deposition time=8 minutes and 5 seconds for 50 nm p^+ a-Si(O_x):H layer, deposition time=16 minutes and 10 seconds for 100 nm p^+ a-Si(O_x):H layer, deposition time=24 minutes and 15 seconds for 150 nm p^+ a-Si(O_x):H layer, deposition time=32 minutes and 20 seconds for 200 nm p^+ a-Si(O_x):H layer. In addition, the test structure is symmetric.

Experiment results and discussion

The influences of p type a-Si(O_x):H thickness during PECVD on the passivation of thicker p^+ poly-Si(O_x) passivating contact (>50 nm) are discovered. The resuls can be found in Figure 3.36. In addition, the highest iV_{oc} of 50 nm p^+ a-Si(O_x):H layer is 656 mV with PDA condition 900 °C duration for 30 minutes. The highest iV_{oc} of 100 nm p^+ a-Si(O_x):H layer is 657 mV with PDA condition 900 °C duration for 30 minutes. At the same time, the highest iV_{oc} of 150nm p^+ a-Si(O_x):H layer is 647 mV with PDA condition 1000 °C duration for 1 minute. Moreover, the highest iV_{oc} of 200 nm p^+ a-Si(O_x):H layer is 640 mV with PDA condition 950 °C duration for 10 minutes. Therefore, it comes to the conclusions that 100 nm p^+ doping layer has the optimum passivation quality. And 900 °C duration for 30 minutes is the optimum post deposition annealing condition for this 110 nm p^+ poly-Si(O_x) passivating contact.

In addition, the passivation results of ultra-thin p^+ poly-Si(O_x) passivating contacts from above mentioned experiments and the passivation results of thick p^+ poly-Si(O_x) passivating contacts in this section are concluded in one figure to see the tendency and find the optimum p^+ doping layer thickness. The results can be discovered in Figure 3.37. It is found that the passivation of 100 nm p^+ doping layer is the optimum with the highest iV_{oc}. However, when utilizing 100 nm p^+ poly-Si(O_x) passivation contacts directly contacting with metal as metallization method, the metal can also cause recombinations

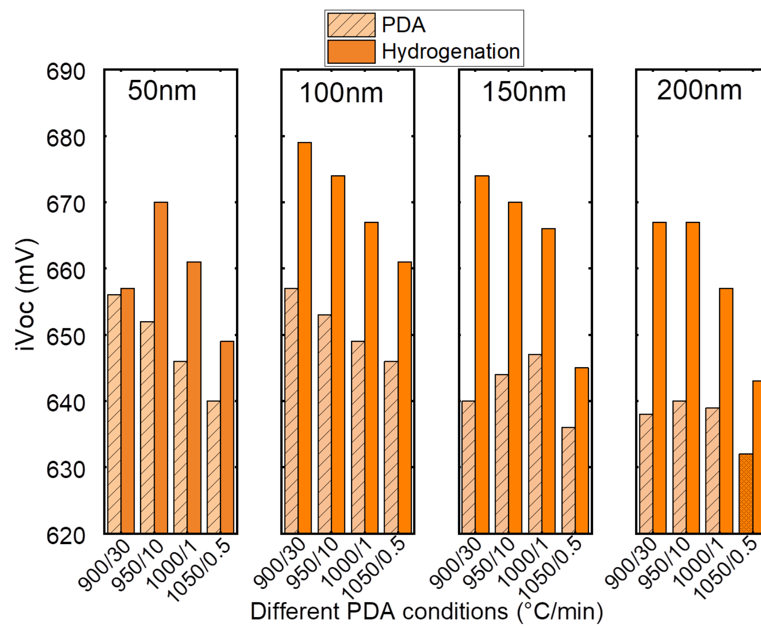


Figure 3.36: Influence of p$^+$ doped layer thickness on the passivation quality of thicker p$^+$ poly-Si(O$_x$) passivating contacts (>50nm)

when contacting with p$^+$ poly-Si(O$_x$) passivating contacts. Thus, in the next chapter, the $J_{\mathrm{o,metal}}$ of p$^+$ poly-Si(O$_x$) passivating contacts with 100 nm p$^+$ doping layer is measured. Then, the iV_{oc} losses of this can be compared with the iV_{oc} losses caused by sputtering from above mentioned results to decide the final metallization approach applied in c-Si solar cell.

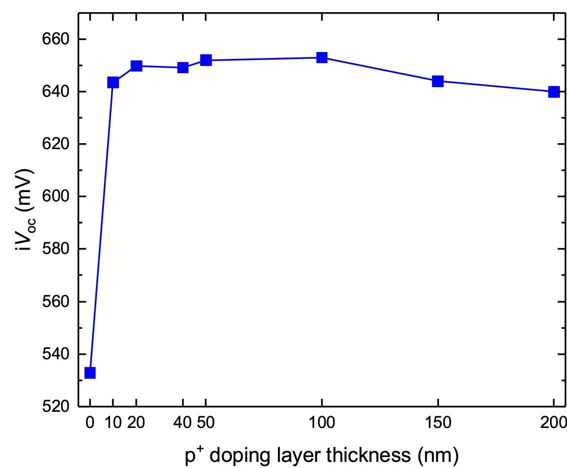


Figure 3.37: Influence of p$^+$ doped layer thickness on the passivation quality of p$^+$ poly-Si(O$_x$) passivating contacts (0-200nm)

4

Contact properties of p^+ poly-Si(O_x) passivating contacts

In Chapter 4, two important contact properties of p^+ poly-Si(O_x) passivating contact are characterized. It can be divided into two sections. In the first section, the contact resistance ρ_c of thicker p^+ poly-Si(O_x) passivating contact is measured. In the next section, the metal-induced recombination $J_{o,metal}$ of different structures is measured.

4.1. Contact resistivity

Experiment objectives and Sample preparation

In this section, the samples utilized are p type c-Si wafers. It can avoid the possible formation of p-n junction through p^+ poly-Si(O_x) passivating contact and n type c-Si bulk that can influence the measurement of the contact resistivity. In addition,in order to avoid the abnormal contact resistivity test caused by the lateral transmission of current, the test structure is designed as SiN_x:H/p^+ poly-Si(O_x)/SiO_x/p-type c-Si. transmission line measurement (TLM) method (contact metal pads with increasing different spacing between them on the same side of substrate) was used to test the contact transmission characteristics between the p^+ poly-Si(O_x) layer and the metal. Because the contact structure is a composite structure, which includes the contact resistivity between the metal Al and the doped p^+ poly-Si(O_x) layer and the contact resistivity between the boron doped poly-silicon layer and the silicon surface through the tunnelling layer. In order to create complete isolation between the two contact areas, the testing structure with TLM pattern was carried out by sulfur hexafluoride (SF_6)deep reactive ion etching, (DRIE) in which the Al electrode part was used as a shield not to be etched. The DRIE equipment is at Kavli Nanolab. Before reactive ion etching, the SiN_x:H is removed for convenience. At the same time, the unmasked layer and the p^+ poly-Si(O_x)/SiO_x stack also a little crystalline silicon region below could be removed by reactive ion etching.

The test data was the sum of the contact resistivity between metal and the p^+ doped layer and the contact resistivity between the p^+ doped layer and the silicon surface through the tunnelling SiO_x layer of the composite structure. However,the contact resistivity between metal and the p^+ doped layer is very small. As a result, in this case, the measured different contact resistivity can mostly attribute to the contact resistivity between c-Si and p^+ poly-Si(O_x) layer.

In addition, when metal contacting with semiconductor, depending on the material properties of the metal and the semiconductor, there are two types of metal-semiconductor junctions : the rectifying type and the non-rectifying type, which is also called the ohmic type. The band diagrams of a metal and an n-type semiconductor can be seen in Figure 4.1 and [77]. If the metal and the semiconductor are brought together and form an ideal contact, two requirements must be fulfilled: at thermal equilibrium and the Fermi energy must be constant throughout the junction. And the vacuum level must be

continuous. As a consequence, a barrier forms between the metal and the semiconductor, as depicted in Figure 4.1(b) and [77].For an n-type semiconductor, the height of this barrier is given by,

$$q\phi_{B_n} = q\phi_m - q\chi \tag{4.1}$$

In the case of a p-type semiconductor, the height of this barrier is given by,

$$q\phi_{B_p} = E_G - q(\phi_m - \chi) \tag{4.2}$$

In addition, an electron that wants to travel from the conduction band of the semiconductor to the metal experiences a built-in voltage,

$$V_{bi} = \phi_{B_n} - \phi_n \tag{4.3}$$

where ϕ_n is the distance between the lower edge of the conduction band and the Fermi level of the n-type semiconductor.

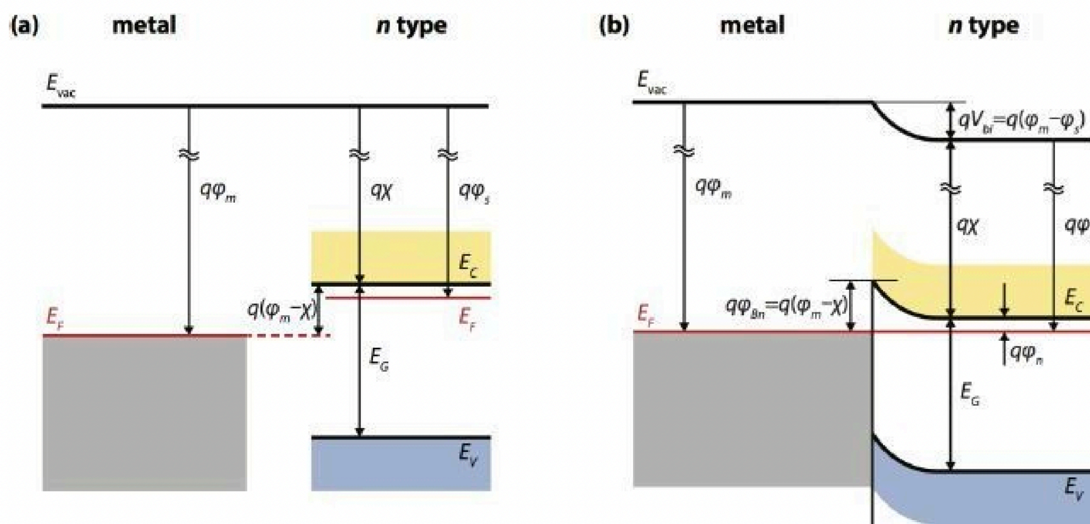


Figure 4.1: (a) The band diagrams of a metal and an n-type semiconductor that are separated from each other.(b) The band diagram of a junction between a metal and an n-type semiconductor[77]

A metal-semiconductor junction is rectifying if the barrier height is large. In addition, in contrast to p-n junctions, where current transport is mainly due to the transport of the minority carrier. For schottky barrier, the transport of the majority carriers is mainly responsible for the current transport. The dominant transport mechanism is thermionic emission of the majority carriers over the barrier into the metal. However, when metal forming rectifying contact with silicon, the possible I-V curve can be seen in Figure 4.2, the relationship between current and voltage is not linear which is not suitable for the data fitting for TLM method.

If the resistance of the metal-semiconductor junction is negligible with respect to the bulk resistance of the semiconductor, the junction is called ohmic. The specific contact resistance R_c is defined as,

$$R_C := \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \tag{4.4}$$

If the semiconductor has a low doping concentration, R_c is given by,

$$R_C := \frac{k}{eA^*T} exp(\frac{q\phi_{B_n}}{K_BT}) \tag{4.5}$$

A^* is the Richardson constant for thermionic emission.

Hence, for reducing the contact resistance, the barrier height should be kept low.

However, the situation is different when the junction is formed between a metal and a highly doped semiconductor.In this case, tunnelling can be the major current transport mechanism in ohmic contact. As a consequence, R_c is also determined by tunnelling. With the equation,

$$R_C \propto exp(\frac{4\sqrt{m_n^*}\epsilon_S\phi_{B_n}}{\sqrt{N_D}h}) \tag{4.6}$$

Here,ϵ_S is silicon dielectric constant. h is Planck's constant. m_n^* is the effective electron mass for n-type semiconductor. N_D is the surface doping concentration and ϕ_{B_n} is the schottky barrier height. If the doping concentration is increased, the contact resistance decreases. Additionally, when metal contacting with Si in ohmic contact, the possible I-V curve can be discovered in Figure 4.3. The I-V curve or current-voltage characteristics is linear or quasi linear for ohmic contacts which is beneficial for the fitting curve by TLM method. Moreover, ohmic contacts should not inject minority carrier carriers. And the voltage drop over them should be small compared to the voltage drops across the active device regions. Therefore, the ohmic contact between metal and Si or poly-Si(O_x) is essential for using TLM method to measure the contact resistivity.

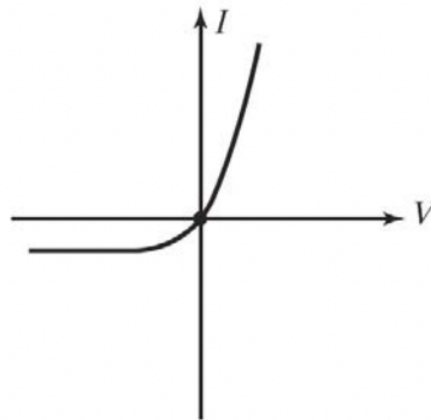


Figure 4.2: I-V curve when metal contacting Si in schottky contact

As a result, metal Al is chosen to contact with p^+ poly-Si(O_x) passivating contact on p-type wafer for measuring the contact resistivity. It is mainly because Al can form ohmic contact with p^+ poly-Si(O_x) passivating contact on p-type wafer. Usually, silver does not form ohmic contact to silicon. It is possible in case of highly doped Si. However, from [12] and [4], silver can form ohmic contact with highly doped n-type silicon emitter. Conversely, Ag contacting with p-Si should have schottky contact if the doping of Si is very high. Thus, Ag can not be chosen as the metal contacting with p^+ poly-Si(O_x) passivating contact on p-Si. But, according to [41] and [25], Al can form ohmic contact with p type Si since Al is p-type dopant. However, Al can only form rectifying contact(schottky barrier) with n-type Si. But when Al contacting with n^+ poly-Si(O_x)/n-Si, it can still form ohmic contact after suitable annealing. Moreover, Al can form better ohmic contact when contacting with p^+ poly-Si(O_x)/p-Si. Here, in this experiment, Al is electron beam evaporated by PROVAC at EKL with the thickness of 500 nm. In addition, after e-beam evaporation, Al requires to be annealed. And the suitable annealing temperature for Al is 400 °C duration for 1-2 minutes according to [25] and [74] also the research results within PVMD group. The Al annealing is done at ESP lab hot plate which the highest temperature can reach 550 °C.By Al

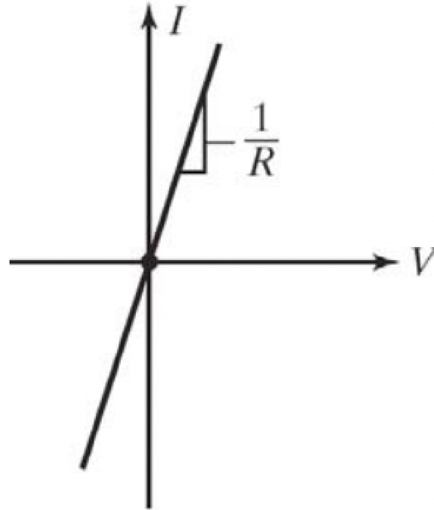


Figure 4.3: I-V curve when metal contacting Si in ohmic contact

annealing, the contact resistivity can be lower and the contacting can be better.

From Equation 4.6, the barrier height and doping concentration will influence the contact resistivity. Reducing the barrier height is often not possible as the materials that determine the barrier cannot be optimized for the barrier height as they fulfil other purposes. As a result, by changing the doping concentration, the contact resistivity can be changed. Therefore, different post deposition annealing conditions are changed to change the doping concentration of boron. Generally, with higher annealing thermal budget, the doping concentration of boron will be higher and the corresponding contact resistivity will become smaller. Therefore, in this experiment, p^+ poly-Si(O_x) passivating contacts with 100 nm p^+ a-Si(O_x):H layer are annealed at 8 different post deposition annealing conditions to measure the contact resistivity.

Experiment results and discussion

At first, the details and corresponding equations of TLM method to measure ρ_c are shown here. The total resistance R_T can be divided into three parts: (1) the resistance of the metal R_m (2) the contact resistance R_c (3) the semiconductor or emitter resistance R_{semi}

$$R_T = 2R_m + 2R_c + R_{semi} \tag{4.7}$$

In most situations, the resistance of the metal in the contact is so low that can be ignored. Thus,

$$R_T = 2R_c + R_{semi} = 2R_c + R_{sheet}\frac{L}{W} \tag{4.8}$$

However, the current does not flow uniformly in the contact. The physical length and width of the contact can not be used to determine the contact area. Then, the average distance that an electron or hole travels in the semiconductor beneath the contact before it flows up into the contact can be determined as below:

$$L_T = \sqrt{\frac{\rho_C}{R_{sheet}}} \tag{4.9}$$

L_T is called the transfer length. Therefore, for the cases that L_T < contact metal pad dimensions L, the effective area of the contact can be calculated as $L_T W$. The simple schematic can be seen in Figure

4.4. The contact resistance is then:

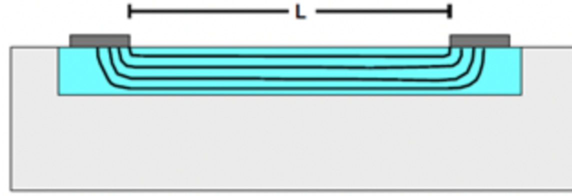


Figure 4.4: Schematic of transfer length

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_{sheet} L_T}{W} \tag{4.10}$$

$$R_T = 2R_c + R_{semi} = 2R_c + R_{sheet}\frac{L}{W} = R_{sheet}\frac{L}{W} + 2\frac{\rho_C}{L_T W} = R_{sheet}\frac{L}{W} + 2\frac{R_{sheet} L_T}{W} \tag{4.11}$$

$$R_T = \frac{R_{sheet}}{W}(L + 2L_T) \tag{4.12}$$

The simple schematic of the metal pad used in this experiment can be discovered in Figure 4.5

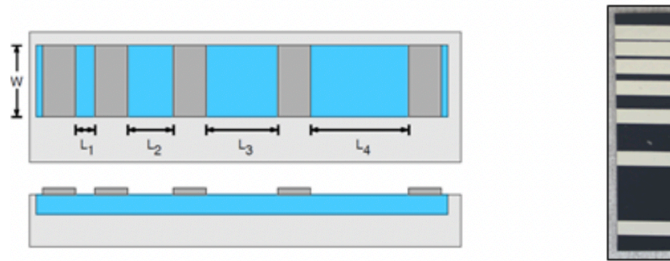


Figure 4.5: Schematic of metal pad

Then, the linear fitting curve of the TLM method can be discovered in Figure 4.6

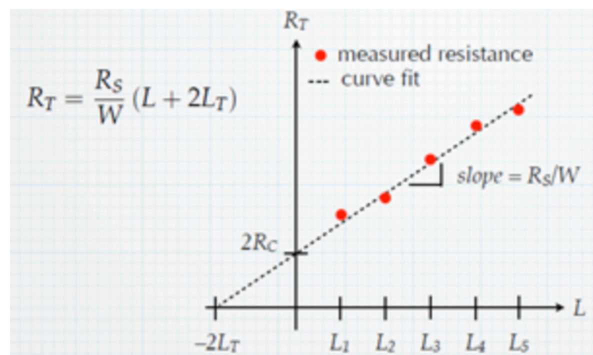


Figure 4.6: linear fitting curve of the TLM method to measure the contact resistance

After fitting, the slope and intercept of the curve can be discovered. Then, the contact resistance R_c can be calculated by Intercept$/2$. The sheet resistance R_{sh} can be calculated by slope $\times$ W. The transfer length L_T can be calculated by $\frac{R_c}{\text{slope}}$. And the specific contact resistivity ρ_c can be calculated by

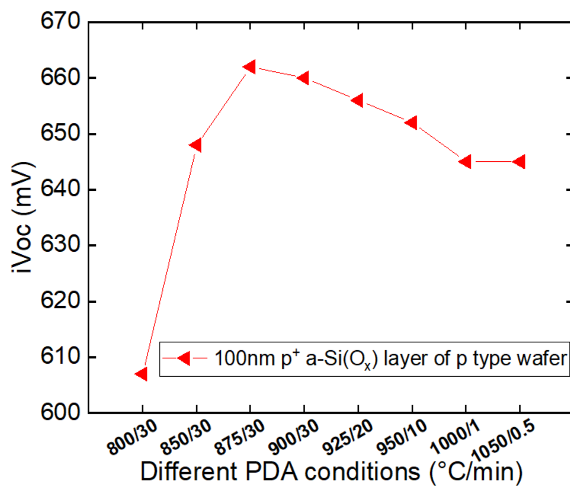


Figure 4.7: Implied open circuit voltage of the samples prepared for measuring contact resistivity through TLM

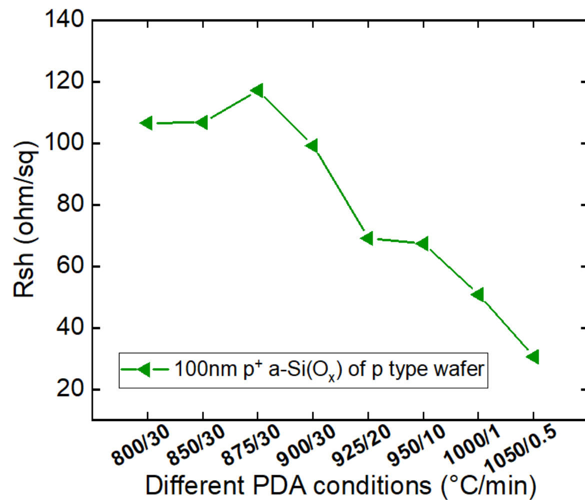


Figure 4.8: Sheet resistance of the samples prepared for measuring contact resistivity through TLM

$R_c \times L_T \times W$

The passivation quality (implied open circuit voltage) and sheet resistance of 8 different samples with 8 different post deposition annealing conditions can be discovered in Figure 4.7 and Figure 4.8. It can be seen from the figures that with higher annealing temperature, the sheet resistance of samples become smaller which can show that the dopants diffuse more into c-Si bulk. And therefore, the boron doping concentration becomes higher. With higher doping concentration, the contact resistance of the samples will become smaller. As a result, it can deduce that with higher post deposition annealing conditions, the contact resistance between c-Si surface and p^+ poly-Si(O_x) will become smaller which are beneficial to the electrical performance of solar cells.

However, from the passivation results in Figure 4.7, it can also be discovered that when the post deposition annealing is very high, the passivation of p^+ poly-Si(O_x) passivating contact is bad since the Auger recombination is very high after plenty of boron dopants in-diffuse. Therefore, the contact resistivity and passivation quality are trade-offs. As a result, contact resistivity of the sample with the highest passivation quality that are annealed at 875°C duration for 30 minutes is measured with TLM method firstly to see the contact resistivity. And typically, here, the optimum PDA condition is different from the above mentioned experiments. It is mainly because these samples are p^+ poly-Si(O_x) passivating contact on p-type c-Si textured wafers for measuring contact resistivity. The former experiments are all done on p^+ poly-Si(O_x) passivating contact on n-type c-Si textured wafers. This may cause the difference of the optimum PDA condition.

The sample with post deposition annealing condition 875°C duration for 30 minutes is chosen to measure the contact resistivity. The linear fitting curve can be seen in Figure 4.9. After fitting and calculating, the specific contact resistivity of sample with 100 nm boron doped layer which is annealed at 875°C duration for 30 minutes is about 22.846 $m\Omega\cdot cm^2$ which seems quite larger than expected.

4.2. Metal-induced recombination

Apart from contact resistivity ρ_c, there's another important parameter to characterize the contact quality of the solar cell: recombination current density J_o which combines recombination from the heavily doped region and the interfacing layer into a single parameter. The total recombination saturation current density is typically measured using quasi-steady-state photoconductance (QSSPC) with the method of Kane and Swanson [42].ρ_c and J_o are both required to be as low as possible to improve the open circuit voltage and fill factor of the solar cell. However, when the contact resistivity of the contact is low, the recombination current density can be relatively high. Therefore, there exists a trade-

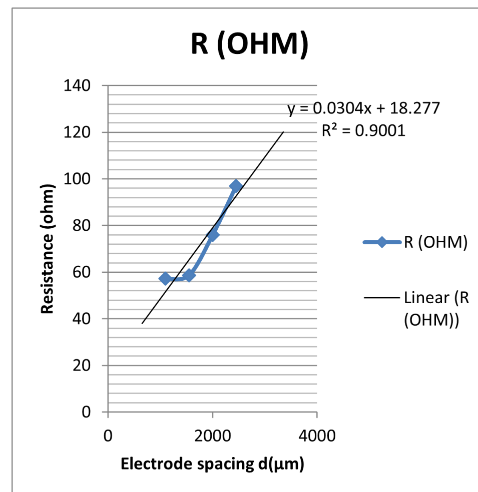


Figure 4.9: The linear fitting curve of the sample with 100 nm boron doping layer and post deposition annealing at 875°C duration for 30 minutes

off between these two parameters. Moreover, most of the recombination current density is from metal contacting with the thin films. As a result, the metal-induced recombination current density is important to be minimized and optimized. But, QSSPC method cannot be utilized to measure the cells after metallization since the conductance of the metal will become dominant which make the results far from correct [6].

Photoluminescence (PL) method can be used to measure the metal-induced recombination current density. According to [75], the test metallization pattern with regions of different front metal contact fractions is screen printed to create special test cells. After that, the special test pattern cells are analyzed using intensity-dependent photoluminescence imaging (Suns-PL). In addition, the measured data are analyzed in two ways. The first approach utilizes graphical fitting to fit the Suns-PL plots within the regions of interest. And the second method uses a detailed finite element method (FEM) based simulation and numerical fitting. Robert Dumbrell. et al [16]further improve the PL method to measure the metal-induced recombination current density. The newly developed system, based on the quasi steady state PL (QSSPL) technique [83] [82] can avoid assumptions and numerical modelling that are necessary for other PL imaging based approaches [24] [23] since the PL measurements are dynamically calibrated. David Herrmann .et al [34] also tried to optimize the PL method. By means of an interpolation scheme of the photoluminescence signal, it can mostly eliminate the necessity for the assumptions of perfect sample homogeneity.

At the same time, by measuring the total recombination current density along with different metal coverage, the metal-induced recombination current density can also be measured. The linear fit through the total recombination current density with different metal fractions can reveal $J_{\text{o,metal}}$ [80][38].

From [11] and [51], it can be discovered that the thickness of poly-Si, textured or flat surface and n or p type poly-Si can all have influences on the metal-induced recombination current density.

Experiment objectives and Sample preparation

Here, the methods utilized for measuring the metal-induced recombination current density is through acquiring the total recombination current density along with the different metal fractions. The metallization is done on single side. And by varying the metal fraction, the different $J_{\text{o,metal}}$ values can be measured by Sinton photoconductance lifetime measurements. And then the data values can be fitted linearly to calculate the value of $J_{\text{o,metal}}$.

Three different testing structures are showed in Figure 4.10, Figure 4.11 and Figure 4.12. The fabrica-

tion process of all the samples have already been described in details in the former experiments and chapters. Typically, here, the doping dose of boron ion-implanted p^+ emitter is $1 \times 10^{15}cm^{-2}$. The hydrogenation process for all the three samples are 20 nm ALD AlO_x:H and 75 nm PECVD SiN_x:H capping layer stack followed by FGA 400°C duration for 30 minutes. In addition, after post-deposition annealing and hydrogenation, the passivation results of all the samples are required to be measured by photoconductance decay lifetime tester to monitor the quality and uniformity of the thin films.

The most important process in this experiment is metallization. The metallization utilizes Al lift-off. Firstly, positive photoresist AZ3027 is spin-coated on the front side of the samples three times with each time 4μm thickness. After the first manual spin-coating, the baking time in the oven is (100°C) duration for 1 minute. After the second manual spin-coating, the baking time in the oven is (100°C) duration for 3 minutes. After the third manual spin-coating, the baking time in the oven is (100°C) duration for 5 minutes.The back side of the samples are spin-coated with photoresist only once for protecting. After that, the samples are manually aligned and exposed under ultraviolet light duration for 100 seconds. 100 seconds exposure time contains four cycles. The exposure time in each cycle is 25 seconds. The positive photoresist AZ3027 can then dissolve in a developer solution MF322 after ultraviolet light exposure. The development duration time is about 1 minute and 50 seconds and then rinsing in DI water duration for 1 minute. The exposed finger area can dissolve in the developer solution, leaving an open area to contact with the metal Al finger. The masks used for exposure are shown in Figure 4.13, where metal fractions for four quarters are 0%, 5.17%, 9.33% and 17.0%, respectively. Since AlO_x:H and SiN_x:H capping layers are both insulators. Then, to make the thin films contact with the metal, the AlO_x:H and SiN_x:H layers on top of the exposed areas are required to be removed by BHF 1:7 etching duration for 3 minutes and then HF(0.55%) etching duration for about 10 minutes until the opening areas are hydrophobic. Then, the samples can be observed under optical microscope to see the situations of the etching and make sure AlO_x:H and SiN_x:H have been removed thoroughly.

After the photolithography process, the Al is evaporated on the front side of the samples by e-beam evaporation using PROVAC equipment at EKL. The thickness of Al is 500 nm. Finally, the excess Al and photoresist from the not exposed area are required to be removed. Then, the process called lift-off is utilized. The photoresist can dissolve in acetone. The samples are put into an ultrasonic bath filled with acetone dedicated for lift-off. After lift-off by acetone, only Al on the exposed areas are left behind.

For correctly measuring the metal-induced recombination current density, Al metal grids are required to be annealed to form ohmic contact with thin films. The optimum Al annealing conditions are tested as the following. After that, the final step is Al etch to remove Al on the samples since Al can influence the measurement of implied open circuit voltage and minority carrier lifetime by Sinton photoconductance decay lifetime tester. The Al can be removed by PES 77-19-04 composed of CH_3COOH and HNO_3 as well as H_3PO_4 with etching time about 8-12 minutes.

The other fabrication processes are all described in details in the former experiments and chapters. The flowchart of measuring the metal-induced recombination current density starting from photolithography can be discovered in Figure 4.14. Here, the 110 nm p^+ poly-Si(O_x) passivating contact sample is chosen as an example. The flowchart of the other two samples are the same as this.

Experiment results and discussion

Firstly, the optimum Al annealing condition should be discovered to measure the $J_{o,metal}$ more correctly. The results are meant to be an increasing recombination current density measured by Sinton WCT-120 for increased metal fractions. However, after measuring directly after metallization, the results are not in right orders. It may because, after metallization, Al have not yet contacted with c-Si. Thus, Al does not induce very much recombination there. In addition, the highly conductive metal Al may have influences on the measurement results of lifetime tester. The annealing process are considered to make the recombination current density higher which is beneficial for the correct fitting of data. The Al annealing condition tests are carried out at hotplate at ESP lab. The results are shown in Figure 4.15 and Figure 4.16. The conclusions are that when the temperature of the hotplate is set as 400°C. Due to the dummy wafer under samples and the problem of the heating of the hotplate, the actual temperature of

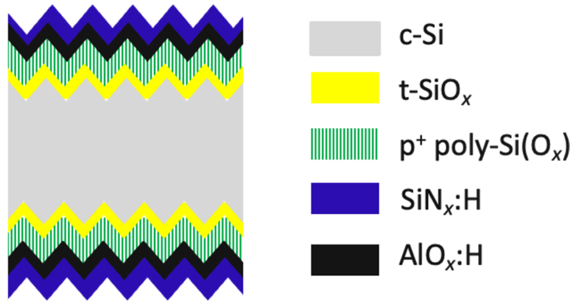


Figure 4.10: Testing structure (1) 110 nm p$^+$ poly-Si(O$_x$) passivating contact for measuring $J_{\text{o,metal}}$

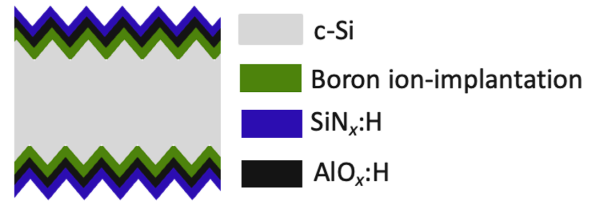


Figure 4.11: Testing structure (2) boron ion-implanted p$^+$ emitter with doping dose 1 $\times$ 10^{15}cm^{-2} for measuring $J_{\text{o,metal}}$

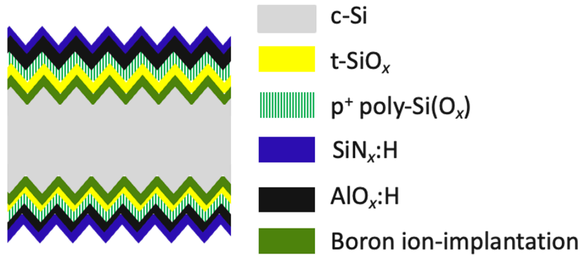


Figure 4.12: Testing structure (3) 110 nm p$^+$ poly-Si(O$_x$) passivating contacts on boron ion-implanted p$^+$ emitter with doping dose 1 $\times$ 10^{15}cm^{-2} for measuring $J_{\text{o,metal}}$

samples during annealing are about 300°C by testing. However, 300°C is not enough to make $J_{\text{o,total}}$ in right order as the increasing of metal fractions by enlarging the duration time to 40 minutes. Then, the temperature is increased to 300°C. After 400°C duration for 20 minutes annealing at the hot plate in atmosphere, the orders of $J_{\text{o,total}}$ of different metal fractions are becoming correct. Therefore, this condition is chosen as the suitable Al annealing condition for measuring metal-induced recombination current density.

The results of samples of three different structures are measured by the methods mentioned above since the PL images from TNO are not clear enough for us to fit the results of $J_{\text{o,metal}}$. Then, $J_{\text{o,total}}$ is measured by Sinton Lifetime Tester and fitted according to the following equations.

$$J_{o,total} = J_{o,bulk} + J_{o,rear,passiv} + (1 - F_m) \cdot J_{o,front,passiv} + F_m \cdot J_{o,metal} \tag{4.13}$$

Here, $J_{\text{o,metal}}$ means metal-induced recombination current density. $J_{\text{o,bulk}}$ means the recombination current density of c-Si bulk. $J_{\text{o,front}}$ can be divided into two parts. One part is not contacting with metal which has the equation $(1 - F_m) \cdot J_{\text{o,front,passiv}}$. The other part is contacting with metal to achieve metallization that has the equation $F_m \cdot J_{\text{o,metal}}$. And the passivation also includes two parts. One is the aforementioned front side passivation $J_{\text{o,front,passiv}}$. And the other one is the rear side passivation $J_{\text{o,rear,passiv}}$. The total recombination current density is composed of all the items mentioned above.

$$J_{o,total} = J_{o,bulk} + J_{o,rear,passiv} + J_{o,front,passiv} + F_m \cdot (J_{o,metal} - J_{o,front,passiv}) \tag{4.14}$$

The sample is symmetric. Therefore, the front side and the rear side has almost the same passivation quality.

$$J_{o,front,passiv} = J_{o,rear,passiv} = \frac{1}{2} \times J_{o,total} \tag{4.15}$$

The recombination current density of c-Si bulk is very small that can be neglected. Then the intercept of the linear fitting curve has only two items $J_{\text{o,front,passiv}}$ and $J_{\text{o,rear,passiv}}$. The sum of them is just the

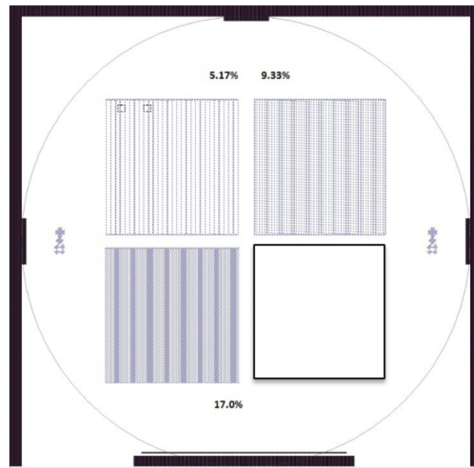


Figure 4.13: The mask with different metal fractions for measuring metal-induced recombination current density

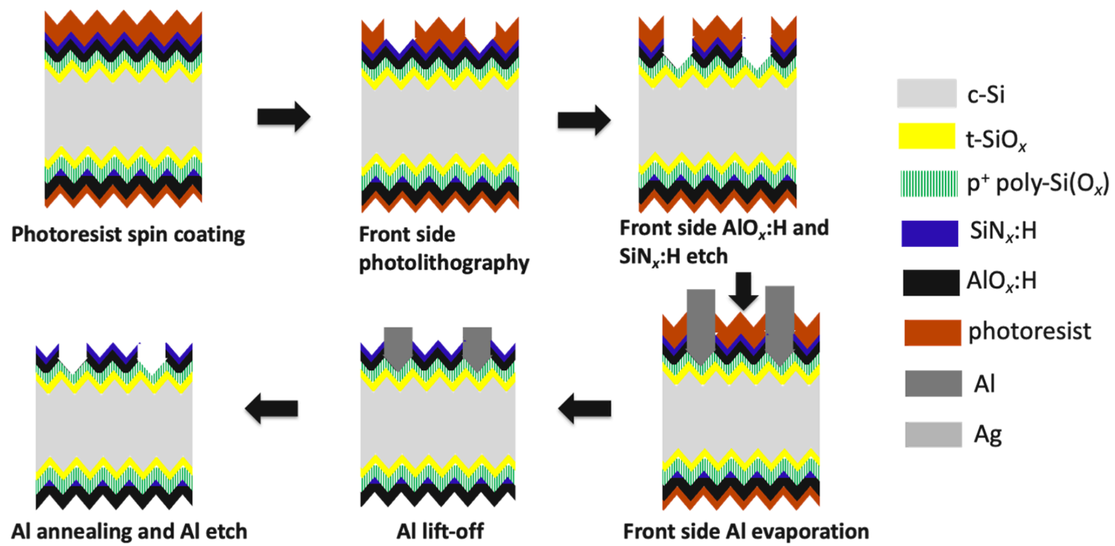


Figure 4.14: Flowchart of measuring the metal-induced recombination current density starting from photolithography

total recombination current density measured by Sinton lifetime tester before metallization.

$$Intercept_{fitting_{curve}} = J_{o,total,before_{metallization}} \tag{4.16}$$

$$Slope_{fitting_{curve}} = J_{o,metal} - \frac{1}{2} \times J_{o,total,before_{metallizaiton}} = J_{o,metal} - \frac{1}{2} \times Intercept_{fitting_{curve}} \tag{4.17}$$

Then, $J_{\text{o,metal}}$ can be calculated by the following equation after the linear fitting of the data of four different metal fractions.

$$J_{o,metal} = Slope_{fitting_{curve}} + \frac{1}{2} \times Intercept_{fitting_{curve}} \tag{4.18}$$

After fitting and calculating, the results of samples of three different structures are shown in Table 4.1.

The approximate values of metal-induced recombination current density of different structures are measured in this experiment. However, this experiment has some assumptions and can not measure the

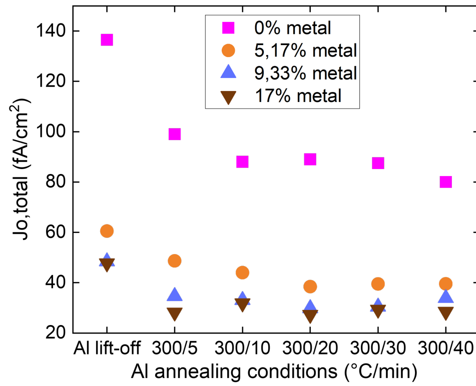


Figure 4.15: The total recombination current density after different Al annealing conditions when the temperature is 300°C

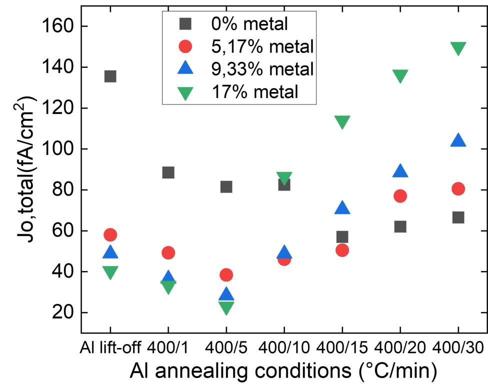


Figure 4.16: The total recombination current density after different Al annealing conditions when the temperature is 400°C

Table 4.1: Metal-induced recombination current density of samples of three different structures

Different structures	110nm p^+ TOPCon	p^+ emitter	110nm p^+ TOPCon on p^+ emitter
$J_{\text{o,metal}}$	$90.8 \pm 16.5\text{fA}/\text{cm}^2$	$581.5 \pm 40.3\text{fA}/\text{cm}^2$	$530.9 \pm 32.1\text{fA}/\text{cm}^2$

$J_{\text{o,metal}}$ in very details. And in addition, to make different quarters of various metal fractions in correct orders for the linear fitting, this experiments utilized contact annealing to deal with the samples after metallization. The contact annealing can also affect the passivation of the non-metallized areas. This can also be discovered in Figure 4.18, Figure 4.20 and Figure 4.22. After annealing, the recombination current density of non-metallized areas increased which represents that the passivation has been damaged.

Apart from that, the uniformity of the passivation of samples are important in the measurement of metal-induced recombination current density. However, unfortunately, after measuring the lifetime of the utilized four different quarters. The uniformity of the samples can not be guaranteed which can also do harm to the measuring results.

Nevertheless, the measuring $J_{\text{o,metal}}$ still represented that the p^+ poly-Si(O_x) passivating contact structure can largely reduced the metal-induced recombination which is a large advantage of it.

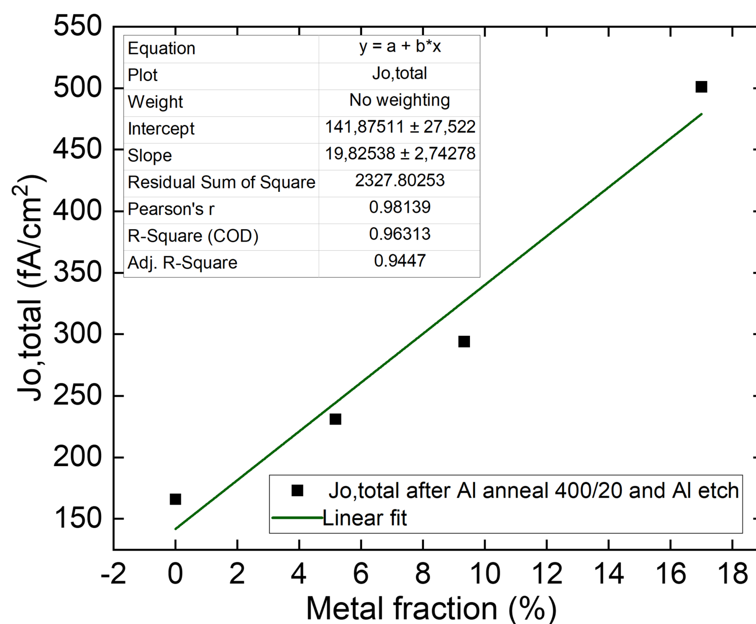


Figure 4.17: $J_{,\text{total}}$ linear fitting curve of 110nm p^{+} poly-Si(O$_x$) passivating contacts

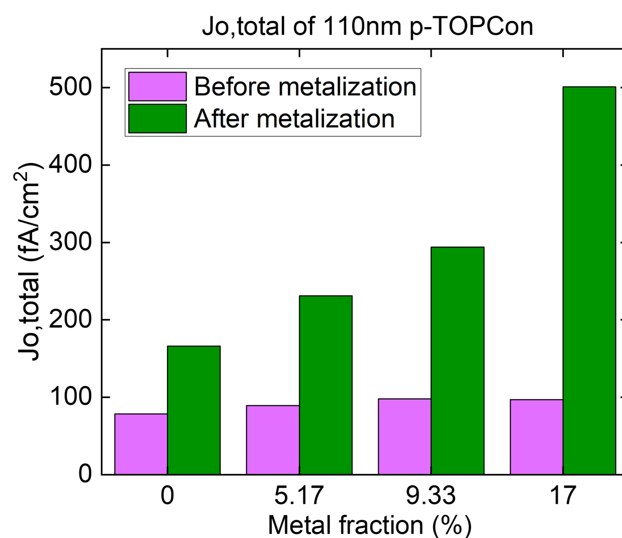


Figure 4.18: $J_{o,\text{total}}$ values of 110 nm p^{+} poly-Si(O$_x$) passivating contacts

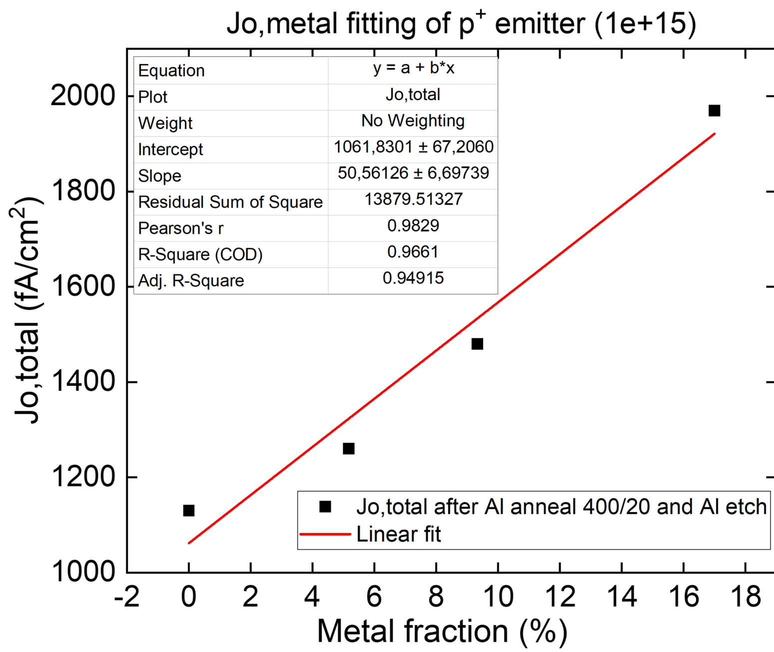


Figure 4.19: $J_{\text{o,total}}$ linear fitting curve of p$^+$ emitter

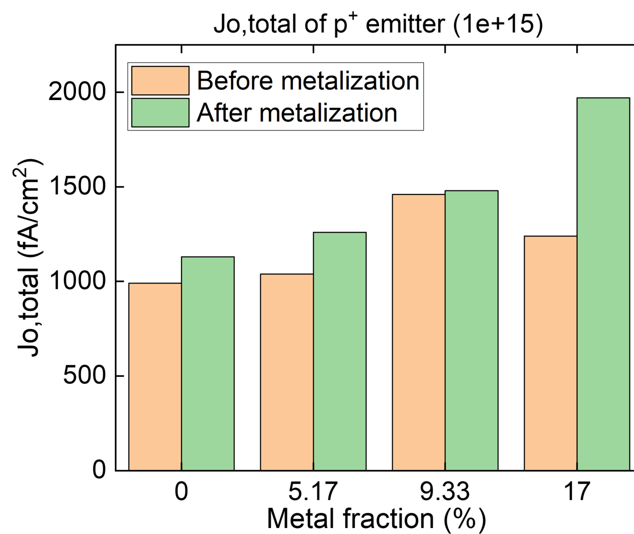


Figure 4.20: $J_{\text{o,total}}$ values of p$^+$ emitter

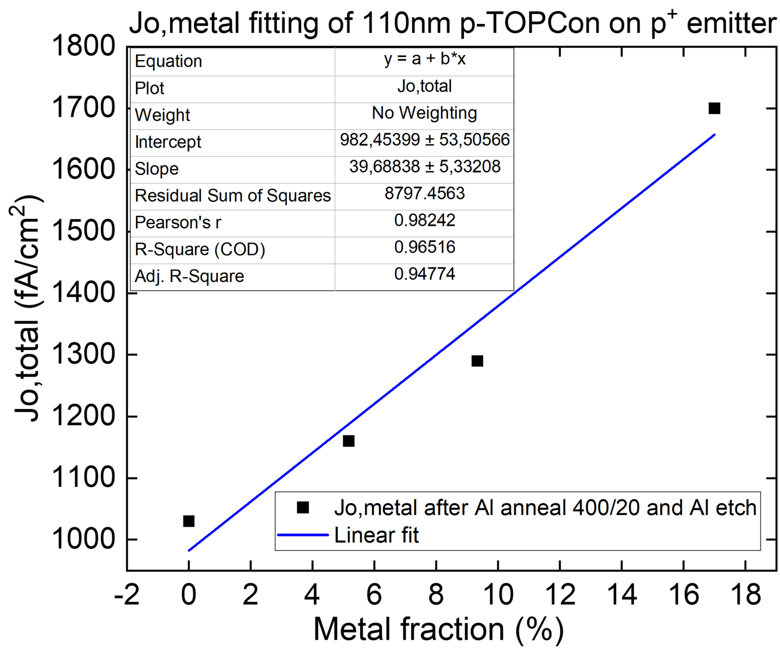


Figure 4.21: $J_{o,\text{total}}$ linear fitting curve of 110nm p$^+$ poly-Si(O_x) passivating contacts on p$^+$ emitter

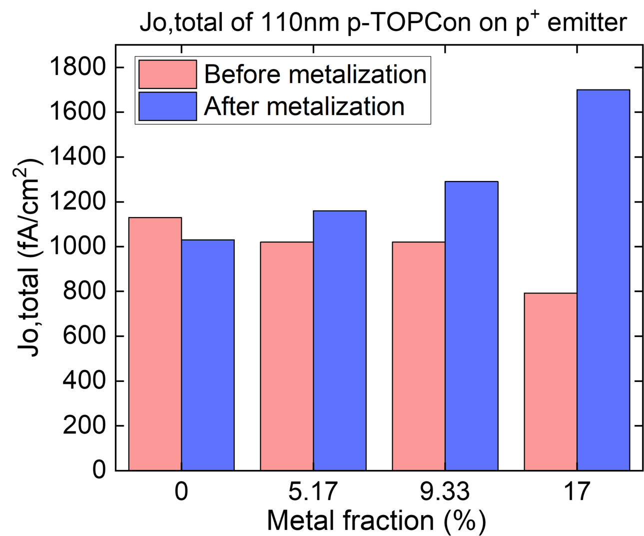


Figure 4.22: $J_{o,\text{total}}$ values of 110nm p$^+$ poly-Si(O_x) passivating contacts on p$^+$ emitter

5

Application in c-Si solar cells

5.1. Passivation optimization of ion-implanted p^+ emitter

5.1.1. NAOS protective layer

Experiment objectives and Sample preparation

In this experiment, two different ALD equipments are utilized. The first one by Oxford Instruments from Kavli Nanolab is described in details from the aforementioned chapter 3.The other one is spatial-ALD from S-ALD company in Eindhoven that the ALD quality is good and the efficiency is very high. However, the Oxford ALD at Kavli Nanolab and Spatial-ALD in Eindhoven both have some distances from EKL cleanroom 10K wet bench. The cleaning of p^+ emitter surface is very important for the following experiments. Therefore, it causes the following experiment. Whether with thin NAOS-SiO_x on p^+ emitter before hydrogenation process, the passivation quality will be better or not? If with NAOS-SiO_x on p^+ emitter, the passivation results are better, then the experiments on p^+ emitter will be carried out more easily and correctly in the future.

Typically, two different post deposition annealing approaches are utilized in this experiment to see whether FGA or rapid thermal annealing (RTA) can have better passivation results. FGA used TEMPRESS tube furnace at Kavli Nanolab which also has been described in details from the aforementioned experiments. The FGA process in this experiment used forming gas to anneal the samples after AlO_x:H/SiN_x:H stack capping layer deposited on p^+ emitter. The FGA conditions are 400 °C duration for 30 minutes and 450 °C duration for 30 minutes, respectively. Typically, the 450 °C FGA requires changing recipe from FGA_Yang to other recipe that can change the annealing temperature during FGA. The recipe FGA_Yang can only change the annealing time. But the annealing temperature is fixed to 400 °C.

The RTA used Surface Science Integration (SSI) Solaris rapid thermal processors (RTP) equipment also at Kavli Nanolab to simulate the firing process used in industry. The SSI Solaris RTP can heat silicon wafers up to 1100 °C in a matter of several seconds. The rapid heating and slow cooling gives the ability to modify the electrical properties of the wafers. The Solaris uses a unique PID process controller that ensures accurate temperature stability and uniformity. The system can accommodate four interlocked MFCs for gas mixing and forming gas processing. In this experiment, the RTA process also utilized forming gas to anneal the samples at 600° C duration for 10 minutes and at 750 °C duration for 30 seconds,respectively.

Experiment results and discussion

From Figure 5.1 and Figure 5.2, it can be found that with NAOS on p^+ emitter, the recombination current density J_o is lower, and the passivation quality is better. This may attribute to the very thin NAOS-SiO_x film on the p^+ emitter before hydrogenation also forms chemical passivation on the surface through si-O bonds. Furthermore, it is assumed that the thin NAOS-SiO_x film can retain the hydrogen from the hydrogenation process which is also beneficial for the chemical passivation. In addition, with RTA

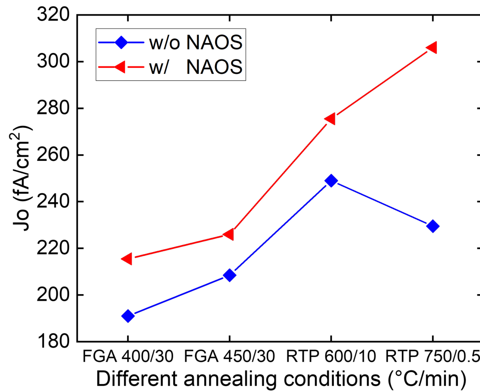


Figure 5.1: Recombination current density of p^+ emitter with or without NAOS on it before hydrogenation with different AlO_x:H/SiN_x:H annealing methods and conditions

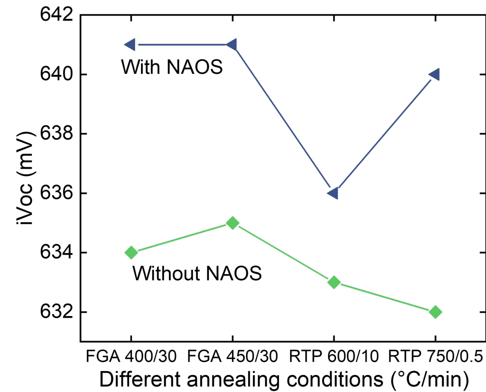


Figure 5.2: Implied open circuit voltage of p^+ emitter with or without NAOS on it before hydrogenation with different AlO_x:H/SiN_x:H annealing methods and conditions

process to anneal the AlO_x:H/SiN_x:H stacks capping layer is worse than with FGA to anneal and activate it which can also be found in Figure 5.1 and Figure 5.2. It may because SSI Solaris RTP at Kavli Nanolab has no ability to cool down the samples immediately. Then, as a result, the hydrogen may release when the annealing temperature remains very high for a while. Due to the release of hydrogen, the chemical passivation will become worse.

5.1.2. AlO_x:H capping layer optimization

Influences of different AlO_x:H thickness

Firstly, experiments are designed to explore the influences of AlO_x:H thickness on the passivation of p^+ emitter. AlO_x:H thickness is changed by changing the cycles of ALD. The 5 nm and 20 nm AlO_x:H layers are deposited by thermal ALD at Kavli Nanolab. The substrate temperature is 105 °C. However, for 5 nm AlO_x:H capping layer, the number of cycles is 75. For 20 nm AlO_x:H capping layer, the number of cycles is 312.

From Figure 5.3, it can be shown that thicker 20 nm ALD AlO_x:H as capping layer gives much better passivation results on p^+ emitter than thinner one with the AlO_x:H thickness of 5 nm. Therefore, 20 nm AlO_x:H deposited at 105 °C during ALD is utilized for the following experiments and solar cells. However, the optimum AlO_x:H thickness may still occur between 5 nm and 20 nm or over 20 nm [72]. At the same time, the optimum substrate temperature during ALD is also very essential according to [72]. Due to time restriction, the interested following researchers can explore more about the influence of AlO_x:H thickness and ALD substrate temperature on the passivation quality of p^+ emitter.

Influence of AlO_x:H pre-annealing

Experiment objectives and experiment methods

From the above mentioned experiments, AlO_x:H and SiN_x:H capping layers are annealed together after depositing. Then, whether pre-annealing the first capping layer AlO_x:H can bring better passivation results on p^+ emitter? It is said that AlO_x:H pre-annealing can give better passivation results on p^+ emitter theoretically [35], [14] and [72]. Since after AlO_x:H pre-annealing, a thin SiO_x layer will form between the AlO_x:H and p^+ emitter interface that will induce chemical passivation caused by si-O bonds on the surface. Apart from that, AlO_x:H pre-annealing can active the negative fixed charges containing in AlO_x:H which will repel minority charge carriers, electrons and attract majority charge carriers, holes. And as a result, the field effect passivation will be further improved. The shcematic of this can be seen in Figure5.4).

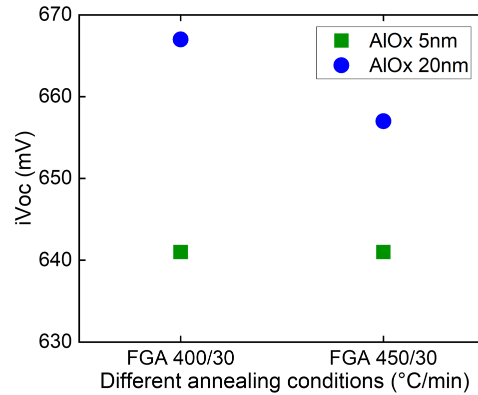


Figure 5.3: Implied open circuit voltage of AlO_x:H/SiN_x:H capping layer stack passivation on p^+ emitter with different AlO_x:H thickness

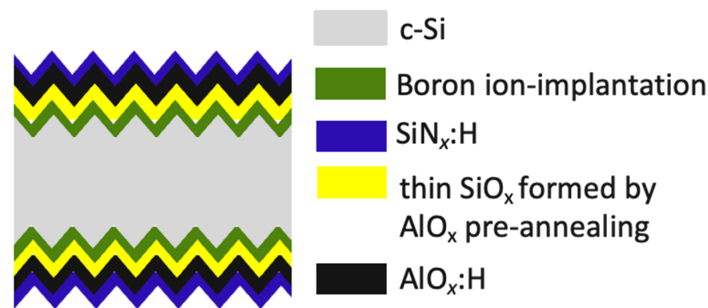


Figure 5.4: Simple schematic of AlO_x:H pre annealing

Additionally, in this experiment, the AlO_x:H is deposited by spatial-ALD at S-ALD company in Eindhoven.The substrate temperature is 200 °C. The utilized precursor gases are still water and TMA for ALD AlO_x:H. The velocity and efficiency of their equipment are very high due to clever designing. 20 nm high quality ALD AlO_x:H only takes less than 10 minutes. However, the Oxford ALD at Kavli Nanolab will take about 2 hours and 30 minutes to deposit 20 nm AlO_x:H with 312 cycles. In addition, AlO_x:H is pre-annealed with different conditions using SSI Solaris RTP equipment for simulating the firing process in industry. The pre-annealing conditions utilized are as the followings: 400 °C, 450 °C and 475 °C annealing tempertuare duration for 30 minutes in nitrogen gas atmosphere; 450 °C duration for 30 minutes , 60 minutes in forming gas atmosphere. The RTA conditions are designed to firstly explore the influence of AlO_x:H RTA temperature, then, the influence of RTA gas atmosphere and finally, the influence of RTA duration time on the passivation results of p^+ emitter.

Finally, this experiment also adopts p^+ emitter with different doping profile since different doping of p^+ emitter can also affect the passivation quality. The different doping profile and sheet resistance are obtained by different doping dose during boron ion implantation. The relations between sheet resistance and doping dose of different p^+ emitter can be found in Figure 5.5. The higher the doping dose is, the heavier the doping is and thus, the lower the sheet resistance R_{sh} is. In this experiment, the samples with sheet resistance of 161 $\Omega/\square$(doping dose 1×10^{15}cm^{-2}) and sheet resistance of 39 $\Omega/\square$ (doping dose 5×10^{15}cm^{-2}) are chosen to carry out the AlO_x:H pre annealing experiments. This experiment design aims at discovering the influence of doping profile of p^+ emitter on the passivation of p^+ emitter at the same time.

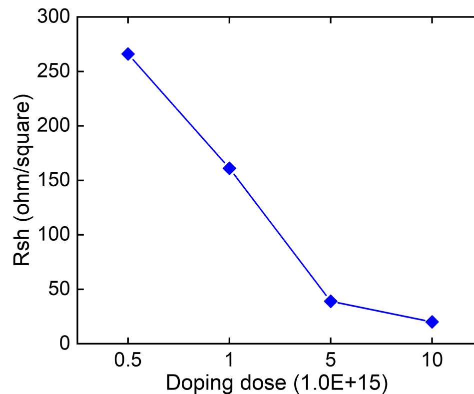


Figure 5.5: The relations between sheet resistance and doping dose during ion implantation of p^+ emitter

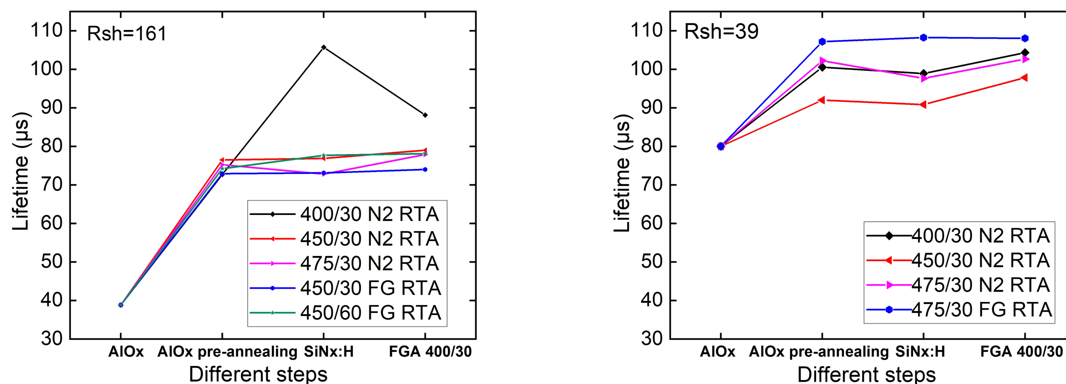


Figure 5.6: Minority carrier lifetime of p^+ emitter of 161Ω/□ as sheet resistance with different AlO_x:H pre annealing conditions

Figure 5.7: Minority carrier lifetime of p^+ emitter of 39Ω/□ as sheet resistance with different AlO_x:H pre annealing conditions

Experiment results and discussion

The experiment is designed to explore whether AlO_x:H pre-annealing is necessary. In addition, it can discover the influence of different AlO_x:H pre-annealing conditions with different tempertuare, duration and gas atmosphere on the passivation quality of p^+ emitter. At the same time, it can also find the influence of p^+ emitter doping dose on the passivation. It is discovered that with AlO_x:H pre-annealing, the passivation of AlO_x:H/SiN_x:H stack on p^+ emitter is better which can be seen in Figure 5.6 and Figure 5.7.

However, the optimum pre-annealing conditions can not be found and the influences of different pre-annealing conditions are still unclear. In the meanwhile, the influences of different p^+ emitter doping dose during ion implantation on the passivation of p^+ emitter also can not be discovered from Figure5.6 and Figure5.7. Although the experiments are subtly designed with plenty of ambitions, the results are totally not as good as expected. It may because that there is still a boron rich layer (BRL) after p^+ emitter high temperature activation and boron silicon glass(BSG) removal by BHF 1:7. BRL can induce very high defect densities and recombination at the surface of p^+ emitter. As a result, all the samples have very very low lifetime that make it hard to compare the results and jump to the conclusions. Last but not least, the doping profile of p^+ emitter may also have some problems that can affect the results. The doping profile of p^+ emitter can be measured through electrochemical capacitance-voltage (ECV) profiling from TNO.

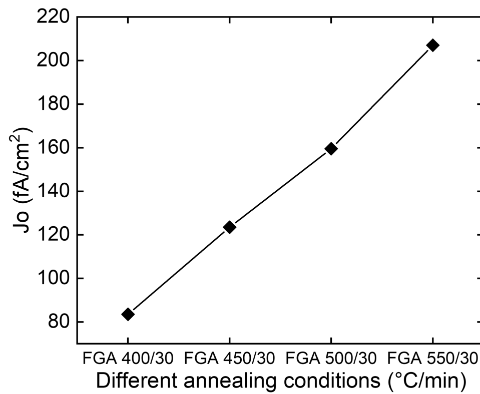


Figure 5.8: Recombination current density of AlO_x:H/SiN_x:H capping layer stack passivation on p^+ emitter with different FGA conditions

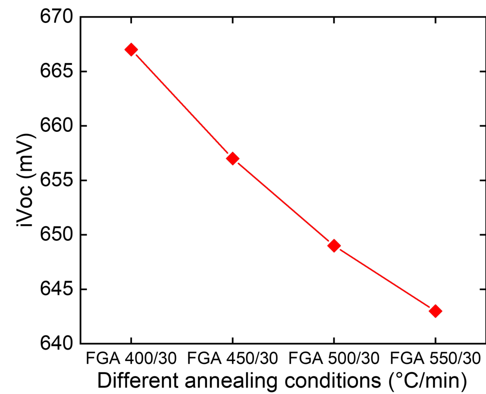


Figure 5.9: Implied open circuit voltage of AlO_x:H/SiN_x:H capping layer stack passivation on p^+ emitter with different FGA conditions

5.1.3. FGA conditions

Experiment objectives and methods

The following experiments are designed to discover the optimum FGA conditions for AlO_x:H and SiN_x:H capping layer stack. The FGA temperatures are set at 400 °C, 450 °C,500 °C and 550 °C with the same annealing duration for 30 minutes.

Experiment results and discussion

It can be clearly seen in Figure 5.8 and Figure 5.9 that FGA with annealing temperature 400 °C duration for 30 minutes is the optimum condition for annealing AlO_x:H/SiN_x:H capping layer stack with the lowest recombination current density and highest implied open circuit voltage. This may because that the deposition temperature for SiN_x:H is also 400 °C. Thus, increasing the post deposition annealing temperature above 400 °C, the hydrogen from SiN_x:H deposition process may release. However, from the tendency in Figure 5.8 and Figure 5.9, 400 °C FGA may be still too high that may also cause the hydrogen release and reduction of the chemical passivation. The p^+ emitter passivation results after forming gas annealing with temperature below 400 °C are still unclear. The following researchers that are interested can use lower SiN_x:H PECVD temperature and the corresponding same lower FGA temperature to explore the passivation results on p^+ emitter.

5.1.4. Boron doping profile

Experiment objectives and experiment methods

The ECV profiling of p^+ emitter with doping dose $5\times10^{14}cm^{-2}$ activated in TEMPRESS tube furnace at EKL is compared with the p^+ emitter from industry with unknown doping dose and doping profile to observe the differences of boron doping profile. The p^+ emitter from Jollywood is proven to have very good passivation quality with AlO_x:H/SiN_x:H capping layer stack. From the results which can be seen in Figure 5.10, it can be observed that the doping of p^+ emitter activated at EKL is smaller and shallower than the sample from industry. As a result, the following experiment is designed. The doping dose of p^+ emitter is changing from $5\times10^{14}cm^{-2}$ to $5\times10^{15}cm^{-2}$. In addition, changing the time ratio of oxidation (gas flow is all nitrogen) and driving-in process (gas flow is all oxygen) during p^+ emitter boron activation and to discover the corresponding changes of sheet resistance and doping profile.

Experiment results and discussion

By increasing the driving-in time during boron activation, since the gas flow is oxygen during this process. Then, the silicon oxide on the p^+ emitter after activation will become thicker. The pure and uni-

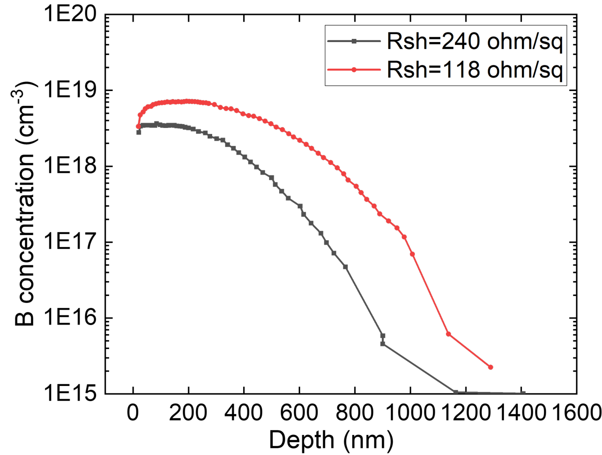


Figure 5.10: The ECV profiling of p^+ emitter sample with the doping dose $5\times10^{14}\text{cm}^{-2}$ activated in TEMPRESS tube furnace at EKL and reference p^+ emitter sample from industry with unknown doping dose

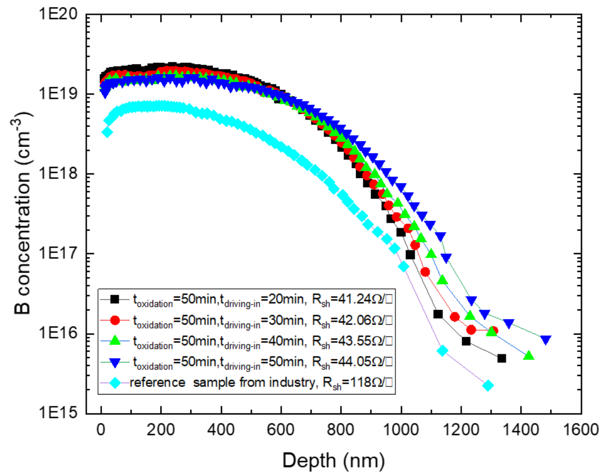


Figure 5.11: The ECV profiling of p^+ emitter samples of doping dose of $5\times10^{15}\text{cm}^{-2}$ with different driving-in time and reference p^+ emitter sample from industry with unknown doping dose

form thermal oxide on p^+ emitter can decrease the boron induced defects produced during p^+ emitter activation. In addition, the thermal oxide will be removed later with BSG by BHF 1:7 etching for about 2-3 minutes. Then, the boron dopants contained in this high quality thermal oxide layer are also removed. As a result, the doping will become lower and the sheet resistance will become larger because of worse conductivity. From the aforementioned experiments, the doping of p^+ emitter with doping dose $5\times10^{14}\text{cm}^{-2}$ at our lab is smaller and shallower than the sample from industry. Therefore, to simulate the doping profile of the sample from industry, the doping dose is increased from $5\times10^{14}\text{cm}^{-2}$ to $5\times10^{15}\text{cm}^{-2}$ to increase the doping. In addition, the time of driving-in process is changed to tune the doping profile of p^+ emitter.

The results which can be discovered in Figure 5.11 show that after increasing the boron doping dose from $5\times10^{14}\text{cm}^{-2}$ to $5\times10^{15}\text{cm}^{-2}$ with the same activation time and temperature. The doping depth of p^+ emitter is long enough. At the same time, by increasing the driving-in time, the sheet resistance of p^+ emitter becomes larger. And doping of p^+ emitter becomes smaller. But the doping of p^+ emitter with the longest driving-in time, 50 minutes is still larger than expected. As a result, the following researchers that are interested can further try to increase the driving-in time or decreasing the boron doping dose from $5\times10^{15}\text{cm}^{-2}$ to $1\times10^{15}\text{cm}^{-2}$ and carry out the same experiments series to see the

corresponding ECV results and changes.

The next two sections of this chapter are concentrated on the fabrication of two different structures of solar cells. The first structure of solar cell is i-TOPCon mono-facial solar cell. It can be used as the reference solar cell to compare with the electrical performance of poly-poly mono-facial solar cell. Therefore, when fabricating this solar cell, no variables are changed. The second structure of solar cell is poly-poly mono-facial solar cell. Here, the post deposition annealing conditions are changed to find the optimum PDA conditions for the poly-poly solar cell cursors. In these two sections, the results and discussions of this two kinds of solar cells are shown.

5.2. i-TOPCon solar cell on DST wafers

5.2.1. Electrical performance

The electrical performance of the i-TOPCon monofacial solar cell can be measured by solar simulator Wacom as described in Chapter 2.

The flowchart of the fabrication process of i-TOPCon monofacial solar cell can be found in details in Chapter 2.

The simple schematic of i-TOPCon monofacial solar cell is illustrated in Figure 5.12.

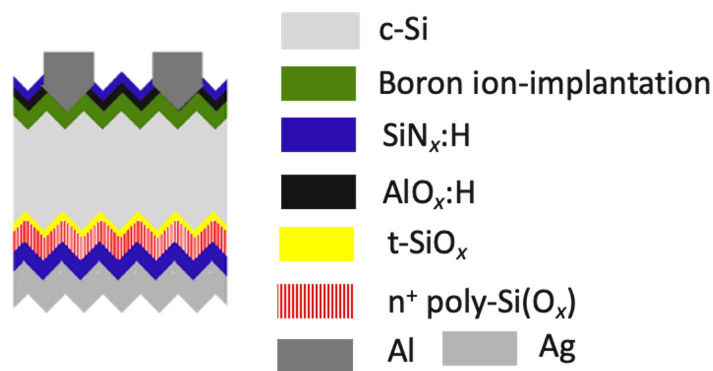


Figure 5.12: Simple schematic of i-TOPCon monofacial solar cell

The electrical performance of i-TOPCon solar cells are V_{oc} is 569 mV, J_{sc} is 34.8 mA/cm^2, FF is 71.3% and η is 14.1%

The efficiency is low and no more than 15% which is abnormal because the series resistance R_s is very high which can cause poor fill factor. In addition, since the hydrogenation process requires 75 nm SiN_x:H deposited by PECVD on the rear side. Then, unlike copper-planting metallization process. Here, the rear side can not be protected by photoresist. The SiN_x:H on the rear side requires to be removed by BHF 1:7 together with the AlO_x:H/SiN_x:H capping layer stack under the openings on the front side.

Then, it induces the following problems. To make sure the front side openings are fully hydrophobic to contact with metal Al, only BHF 1:7 is utilized with etching time 6 minutes. However, BHF 1:7 can etch away the n^+ poly-Si(O_x) passivating contact with relatively higher velocity than p^+ poly-Si(O_x) passivating contact. Due to the rare experiments on n^+ poly-Si(O_x) passivating contact, BHF 1:7 over etch too much on the rear side which will largely decrease and break the surface passivation and make n^+ poly-Si(O_x) passivating contact not uniform. This will largely decrease the V_{oc} of solar cell. The n^+ poly-Si(O_x) unlike poly-Si, the etch rate of BHF 1:7 on it is very fast. However, poly-Si can against the etch of BHF 1:7.

Thus, the following researchers ought to pay attention to this phenomenon. And through experiments on this, the optimum etching condition is 3 minutes etching in BHF 1:7 and then 10 minutes etching in HF(0.55%) by which the etch rate on n^+ poly-Si(O_x) passivating contact is slower. The correct flowchart is updated according to this.However, due to the time restriction of project, no time is allowed to re-fabricate the i-TOPCon monofacial solar cell on DST wafers. The following researchers who involved can explore more on this according to the updated flowchart. And the electrical performance of the i-TOPCon solar cells may give better results. Besides, all of my work is concentrated on the optimization of the electrical performance. Therefore, here, the optical performance of the solar cells like external quantum efficiency (EQE) is not characterized.The following researchers can try to further improve the optical performance and measure the corresponding EQE value to show its optical performance.

5.3. poly-poly solar cell on DST wafers

5.3.1. Electrical performance

The passivation quality of the poly-poly mono-facial cell precursors can be discovered in Figure 5.13

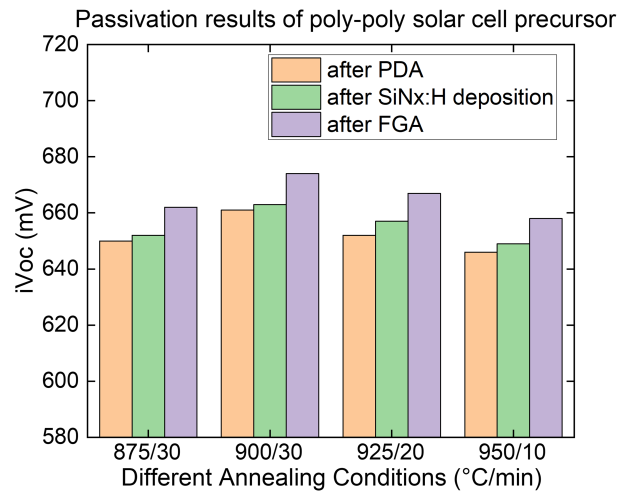


Figure 5.13: Passivation quality of poly-poly mono-facial cell precursors

From Figure 5.13, it can be discovered that, 900 °C annealing temperature and duration time for 30 minutes is the optimum post deposition annealing condition for poly-poly mono-facial cell precursors.

The flowchart of the fabrication process of poly-poly monofacial solar cell can be found in details in Chapter 2.

The simple schematic of poly-poly monofacial solar cell is illustrated in Figure 5.14.

The electrical performance of poly-poly mono-facial solar cell is measured. The best electrical performance with the highest efficiency can be discovered in Figure 5.15. However, the highest efficiency solar cell is originated from the cell precursor that post deposition annealing at 925 °C annealing temperature duration for 20 minutes. In addition, the efficiency η, V_{oc}, J_{sc} and *FF* of the cell precursor with the highest efficiency for different 6 dies can be seen in Figure 5.16, Figure 5.17, Figure 5.18 and Figure 5.19.

From the figures, it can be discovered that, the V_{oc} is not so high even the rear side TCO sputtering damage has been removed. The front side TCO sputtering damage on n^+ poly-Si(O_x) passivating

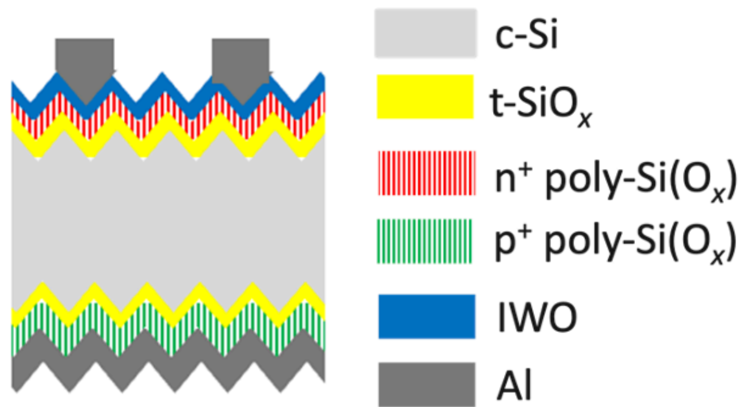


Figure 5.14: Simple schematic of poly-poly monofacial solar cell

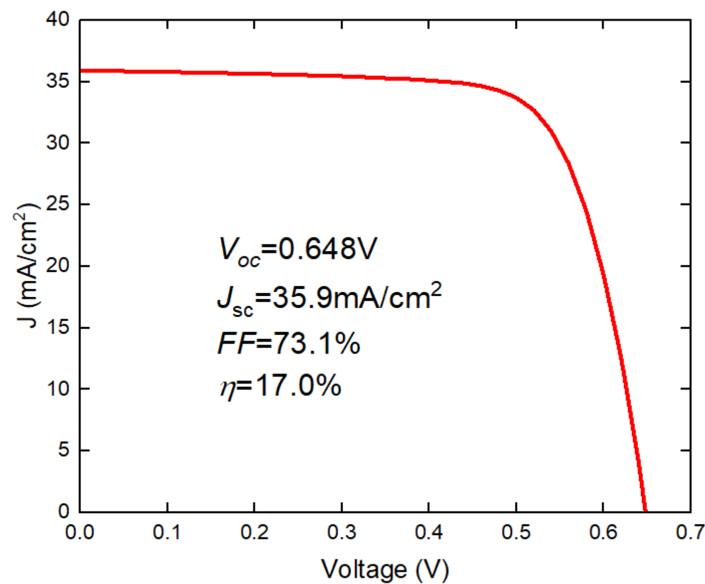


Figure 5.15: Electrical performance of poly-poly mono-facial cell precursors with the highest efficiency

contact of textured wafers and the metal-induced recombination current density for both sides can still largely affect the open circuit voltage. The optimum TCO sputtering damage recovery conditions can be further optimized for textured wafers. 400 °C vacuum annealing duration for 30 minutes is the optimum IWO sputtering damage recovery condition for n$^+$ poly-Si(O$_x$) passivating contact on flat surface within PVMD group. However, no more optimization is given on textured surface to further reduce the IWO sputtering damage and the corresponding recovery conditions. Furthermore,the metal annealing condition can be further optimized to further reduce the contact resistivity and form better contacting.

From Figure 5.16, Figure 5.17, Figure 5.18 and Figure 5.19, it can be discovered that the V_{oc} of the solar cells had almost the same tendency as the efficiency of the solar cells. For die 6, the short circuit current density J_{sc} is very high. Therefore, although the V_{oc} is not high, the efficiency is still high. Therefore, generally, increasing V_{oc} can increase the efficiency of the solar cells.

From above, the efficiency and V_{oc} has almost the same tendency. Therefore, the open circuit voltage V_{oc} and efficiency η for 6 dies with 4 different PDA conditions are shown in the following Table 5.1 and Table 5.2.

In addition, the V_{oc} and η of die 1 with 4 different PDA conditions are shown in Figure 5.20 and Figure

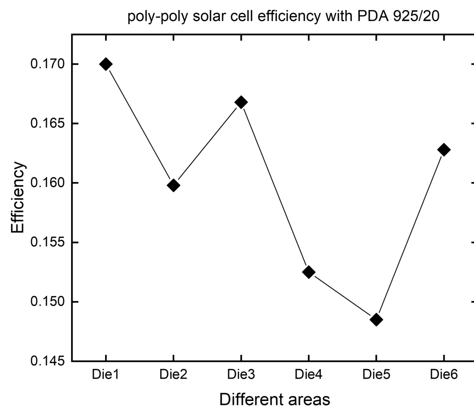


Figure 5.16: Efficiency of poly-poly mono-facial cell precursors for 6 different dies with cell precursors post deposition annealing at 925 °C duration for 20 minutes

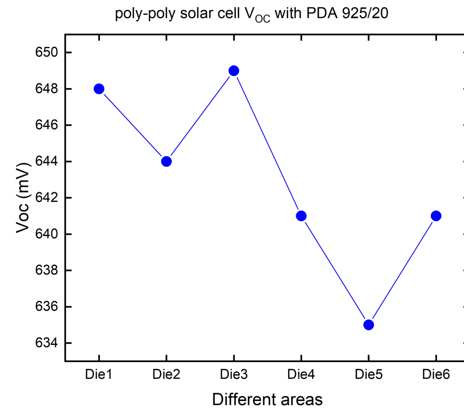


Figure 5.17: Open circuit voltage of poly-poly mono-facial cell precursors for 6 different dies with cell precursor post deposition annealing at 925°C duration for 20 minutes

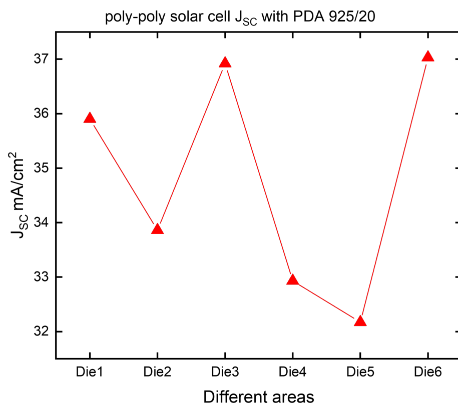


Figure 5.18: Short circuit current density of poly-poly mono-facial cell precursors for 6 different dies with cell precursor post deposition annealing at 925°C duration for 20 minutes

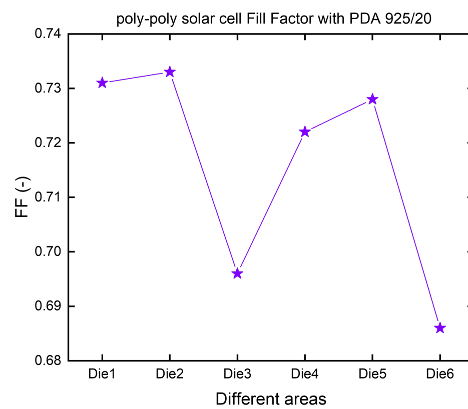


Figure 5.19: Fill factor of poly-poly mono-facial cell precursors for 6 different dies with cell precursor post deposition annealing at 925 °C duration for 20 minutes

Table 5.1: V_{oc} for 6 various dies with 4 different PDA conditions

	After PDA 875/30	After PDA 900/30	After PDA 925/20	After PDA 950/10
V_{ocDie1}	635mV	649mV	648mV	629mV
V_{ocDie2}	628mV	648mV	644mV	629mV
V_{ocDie3}	637mV	649mV	649mV	636mV
V_{ocDie4}	630mV	650mV	641mV	621mV
V_{ocDie5}	630mV	644mV	635mV	622mV
V_{ocDie6}	640mV	645mV	641mV	631mV

Table 5.2: η for 6 various dies with 4 different PDA conditions

	After PDA 875/30	After PDA 900/30	After PDA 925/20	After PDA 950/10
η_{Die1}	14.9%	16.8%	17.0%	13.6%
η_{Die2}	12.6%	16.1%	16.0%	13.5%
η_{Die3}	15.3%	16.9%	16.7%	14.2%
η_{Die4}	14.4%	14.0%	15.3%	12.1%
η_{Die5}	15.4%	15.5%	14.9%	14.0%
η_{Die6}	16.4%	14.6%	16.3%	14.8%

5.21, respectively.

From Figure 5.20 and Figure 5.21,also Table 5.1 and Table 5.2, it can be discovered that, generally, the higher the iV_{oc} for cell precursors after post deposition annealing are, the higher the efficiencies of the solar cells are. However, the passivation quality of poly-poly mono-facial solar cell precursors is not the only parameter that can decide the efficiency of the solar cell. The TCO sputtering process and more importantly, the metallization process can also decide the efficiency of the solar cell. A higher FF can also induce higher efficiency for poly-poly solar cells.

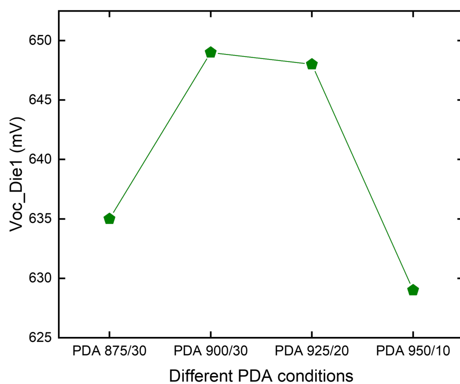


Figure 5.20: V_{oc} of die 1 with 4 different PDA conditions

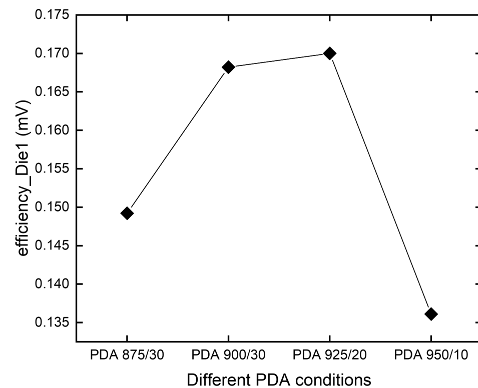


Figure 5.21: η of die 1 with 4 different PDA conditions

6

Conclusions and Outlooks

6.1. Conclusions

This thesis aims at optimizing the passivation of p^+ poly-Si(O_x) carrier selective passivating contacts on double side textured wafers and fabricating corresponding solar cells. Firstly, the optimization of p^+ poly-Si(O_x) passivating contact is explored. The interfacial tunnelling oxides, intrinsic a-Si(O_x):H layer formation, p^+ a-Si(O_x):H deposition, crystallizing and hydrogenation process are optimized. Then, two important contact properties, contact resistivity ρ_c and metal induced recombination current density $J_{o,metal}$ are characterized for fabricating solar cells. Finally, the poly-poly c-Si solar cell is fabricated with p^+ poly-Si(O_x) passivating contacts.

Firstly, the fabrication processes of the p^+ poly-Si(O_x) passivating contacts are optimized in terms of passivation quality as an indicator. The passivation quality can be decided by field effect passivation and chemical passivation. And the SiO_x layer is necessary for balancing the field effect passivation and carrier transport to enhance high iV_{oc}. The influences of different interfacial tunneling oxides on the carrier selectivity of the p^+ poly-Si(O_x) passivating contacts are compared. PANO-SiO_x gives the lowest implied open circuit voltage among the silicon oxides that were studied. This may partially attribute to the non-uniformity of ultra-thin SiO_x layer during the plasma assisted oxidation process. Besides,from XPS results, it can be found that the differences between interfacial tunnelling oxides fabricated by various methods can result from the differences between stoichiometric Si^{4+} states. It is also found that t-SiO_x has the highest Si^{4+} percentage in oxides. In addition, from SIMS results, SiO_x with higher stoichiometry is denser and can serve as a strong barrier which is beneficial for prohibiting the boron dopants in-diffusing. t-SiO_x is a feasible interfacial oxide formation technique that can balance highly Si^{4+} concentration and controllability of the thickness as well as retaining the uniformity.

The influences of intrinsic layer deposition methods on the passivation quality of p^+ poly-Si(O_x) passivating contacts are discovered. Blistering phenomenon is observed on the samples of intrinsic layer fabricated by PECVD. However, with intrinsic layer deposited by LPCVD, almost no blistering condition is found. It is mainly because LPCVD deposition approach can reduce the stress accumulation between interfaces. As a result, the passivation of p^+ poly-Si(O_x) passivating contacts with intrinsic layer processed by LPCVD has a higher iV_{oc} than PECVD counterpart. With the aim at finding better processing windows, the B_2H_6/SiH_4 ratio and CO_2/SiH_4 ratio of p^+ doping layer PECVD deposition are explored. The optimum gas flow parameters are 8 sccm SiH_4, 5 sccm CO_2, 10 sccm B_2H_6 and 100 sccm H_2 during PECVD. Then, the p^+ doping layer thickness is studied. It is confirmed that the optimum p^+ doping layer thickness is 100 nm which results in the highest iV_{oc} of 685 mV.

After that, the hydrogenation process is studied.The highest iV_{oc} with the standard hydrogenation process is 674 mV. It can be shown that the passivation of p^+ poly-Si(O_x) passivating contacts on textured surface is improved by adding AlO_x:H/SiN_x:H bi-layer stack. AlO_x:H inserted layer is used for the hydrogen reservoir together with SiN_x:H to improve the hydrogen level of p^+ poly-Si(O_x) passivating contacts.

Moreover, the metallization is applied to evaluate the carrier collection and recombination regarding the contact resistivity and metal induced recombination current density. Evaporated Al is utilized to contact with p^+ poly-Si(O_x) passivating contacts. ρ_c of p^+ poly-Si(O_x) passivating contacts with 100 nm boron doped layer is about 23 m$\Omega\cdot$ cm^2. The measured $J_{o,metal}$ is around 91 fA/cm^2. With the same method, for p^+ emitter, the measured $J_{o,metal}$ is about 582 fA/cm^2. The results show that p^+ poly-Si(O_x) passivating contacts comparing with p^+ emitter can reduce the metal-induced recombination current density. In addition, it is indicated that the iV_{oc} loss caused by Al/p^+ poly-Si(O_x) passivating contacts is smaller than the loss induced by TCO sputtering. Therefore, the thick p^+ poly-Si(O_x) passivating contacts with 100 nm p^+ doping layer directly contacting with metal is used as metallization method for poly-poly c-Si solar cell. Finally, poly-poly monofacial solar cells on double-side textured surface are fabricated. The best poly-poly solar cell has the following electrical performance : V_{oc} is 648 mV, J_{sc} is 35.9 mA/cm^2, *FF* is 73.1% and η is 17.0%.

6.2. Outlooks

There are still some spaces that can be improved to enhance the performance of poly-Si(O_x) solar cells. Here, we address the main concerns for improvement of the poly-Si(O_x)) solar cells regarding the optimization of p^+ poly-Si(O_x) passivating contacts and device. This is a roadmap to realize more than 22% efficiency of c-Si solar cells with p^+ poly-Si(O_x) passivating contacts.

6.2.1. p^+ poly-Si(O_x) passivating contacts

- **Interfacial tunnelling oxides** : For the optimization of interfacial tunnelling oxides, there are still many boron dopants in-diffusing into the c-Si bulk and causing the Auger recombination. Therefore, the different process parameters of tunnelling oxides can be further explored to control the Si^{4+} percentage. In addition, the pinholes in the tunnelling oxides layer can also be discovered. They can assist the charge carriers transporting.

- **Intrinsic a-Si layer** : Firstly, as for the intrinsic layer fabricated by PECVD, blistering phenomenon should be suppressed to obtain a higher iV_{oc} by tuning such as substrate temperature, hydrogen gas flow et al. Concerning the LPCVD techniques, the thickness of the intrinsic layer should be studied to prevent the dopants in-diffusion so as to realize steep doping curve.

- **Boron doped a-Si layer depositions** : Only the activated boron can induce field effect passivation. It is reported that the doping efficiency of p^+ doping layer is difficult to improve by simply increasing the gas flow of diborane. Additionally, the thickness of p^+ poly-Si(O_x) still needs to be optimized to obtain the balance between electrical and optical properties.

- **Crystallizing process** : The objective of crystallization process is to activate boron dopants and drive the dopants in-diffuse into the c-Si bulk. Therefore, an accurate control of temperature ramping up curve is required to activate the boron dopants effectively and to obtain a steep doping curve. For example, RTA process can be applied to control the ramping up of the annealing temperature more precisely.

- **Hydrogenation process** : It is confirmed that the hydrogen concentration in p^+ poly-Si(O_x) is generally less than n^+ poly-Si(O_x). Therefore, how to improve hydrogen concentration is a key to realize high quality p^+ poly-Si(O_x). Hydrogen rich dielectric thin films can be studied to improve the passivation quality of p^+ poly-Si(O_x). In addition, the other dielectric thin films that have porous structure which can maintain the hydrogen can also be applied as capping layer.

6.2.2. poly-Si(O_x) solar cells

The optimization of metallization process contains the optimization of electrical and optical performance. Regarding the electrical part, resistive loss and recombination loss should be minimized. For example, the contact resistivity between p^+ poly-Si(O_x) and c-Si as well as the metal grids resistive losses can

be alleviated. As for the optical part, metal shading loss, surface reflectance loss and absorptive loss should be reduced to increase the carrier generation.

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