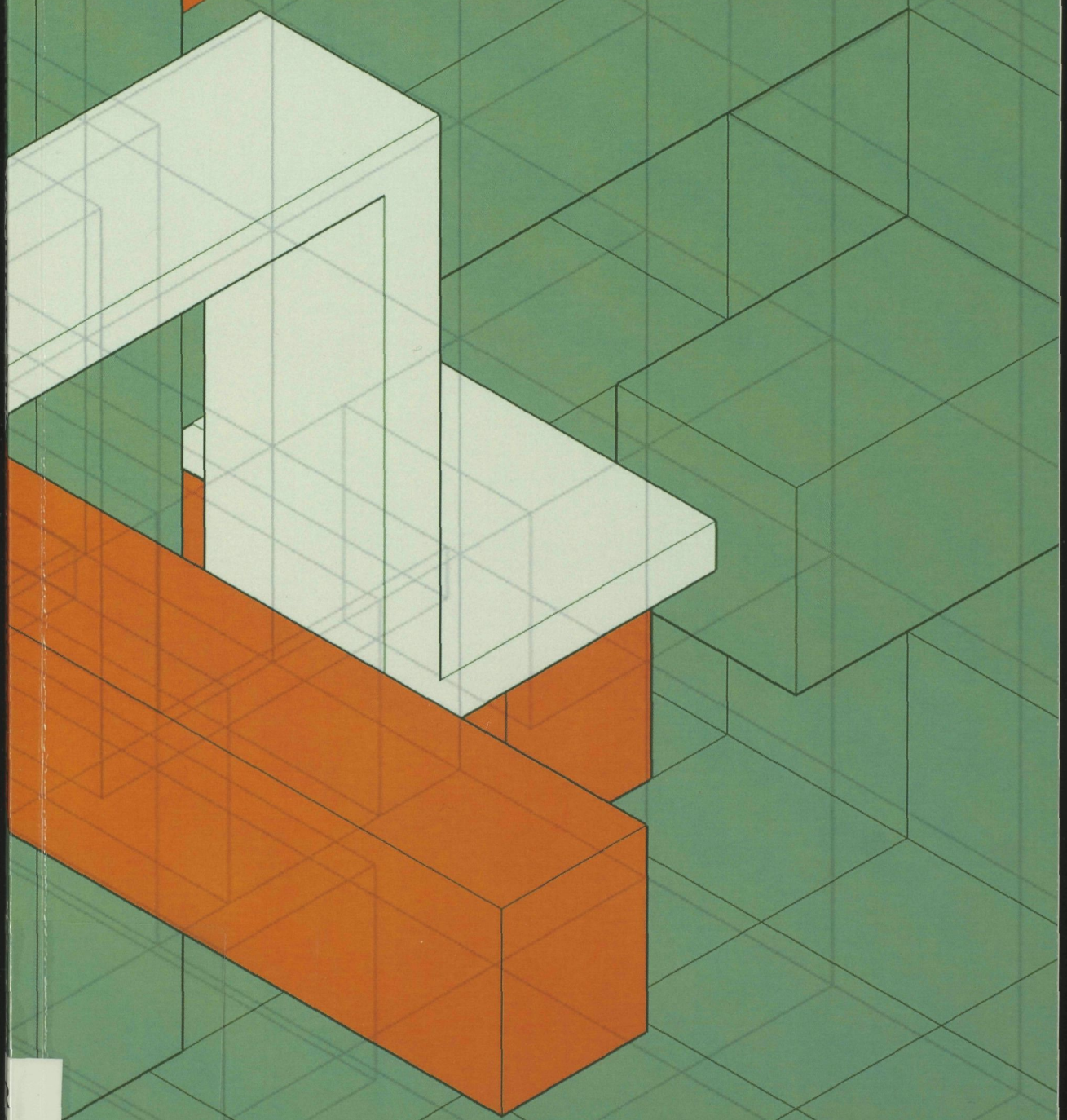
Monolithic 3D Integration of Single-Grain Silicon TFTs



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Contents

Chapter 1

Introduction

The goal of this chapter is to introduce to the research done for this dissertation. The key issues, motives and challenges will be highlighted to justify the content and structure of the following chapters.
Below, the reasons for studying three-dimensional integrated circuits (3D ICs) will be presented and an overview of existing 3D IC technologies and approaches will be given. The structure of this thesis will also be outlined.

1.1 The need for the third dimension

Since the invention of the Integrated Circuit (IC) in 1958, the growth of the semiconductor industry has been rapid [1]. ICs are now applied in every aspect of our daily lives. From early on, there was a trend in the growth of IC performance which directly related to a reduction in the size of its main building blocks, the Complementary Metal-Oxide-Semiconductor (CMOS). Gordon Moore described this trend in 1965, predicting that the density of integrated circuits would double every one and a half years [2]. This miniaturization of the CMOS was called downscaling and it is still the most important and effective way of keeping up with the growth trend. In order to maintain a constant electric field in a CMOS device, many of its design parameters must be scaled. In the following sections, the problems caused by the downscaling will be described in greater details. After description of each issue, the solutions offered by 3D ICs will be discussed. Thus the term 3D IC needs to be defined. Here, 3D ICs refer to integrated circuits which have devices (transistors, sensors, etc.) placed on multiple layers of active materials. These devices can be connected with each other both horizontally and vertically. Different types of 3D ICs are categorized based on the basis of their

level of integration and will be described in more depth in Section 1.2.

1.1.1 Physical limitations of downscaling

The trend towards the shrinking of the channel length of CMOS transistors has been very aggressive. This law has tendacy prevailed by due to the incorporation of advanced lithography, strained silicon transistors, high-k/metal gates, Cu metallization, and low-k inter-level dielectric (ILD) layers in down scaled CMOS. All of these measures mentioned are designed to control the gate leakage, threshold voltage and other short-channel phenomena. However, the development of smaller channel dimensions will soon cease due to fundamental physical limitations. Most current semiconductor theories are defined in terms of regimes, in which the channel length is assumed to be much larger than electron wavelength. Else, electrons can no longer be treated as particles while ICs have been designed upon on this assumption. The International Technology Road map for Semiconductors (ITRS) reports gate lengths down to 10 nm [3, p.11] by 2015. It is certain that conventional downscaling has an expiration date which is close and only vertical and 3D structures can prolong the continuation of this trend [4]. A very basic advantage of 3D IC schemes is that the chip area will be reduced, without shrinking the dimensions of a single transistor.

1.1.2 Interconnect delay

The first integrated circuit utilized external interconnects. But it did not take long for interconnects to be implemented on-chip. This transition reduced interconnect length drastically and thus increased the performance of the chip [5]. Every interconnect may be seen as a delay element in an integrated circuit. This, the so-called RC delay, is caused by the resistance of the conducting material and the capacitance of the dielectric, isolating them. This causes power loss, speed reduction and noise addition [6]. Figure 1.1 suggests that interconnects are becoming a bottleneck in chip performance, with power consumption increasing because capacitance needs relatively large power drivers and limits transistor performance [7, 8].

On the material level, the RC delay can be reduced by decreasing the resistance and capacitance of the conducting and dielectric material, respectively. [10–12]. On the architectural level, several optimizations are possible. A multilevel interconnect architecture that optimizes the interconnect cross-sectional dimensions of each metal layer, thereby reducing cycle time, power consumption and the

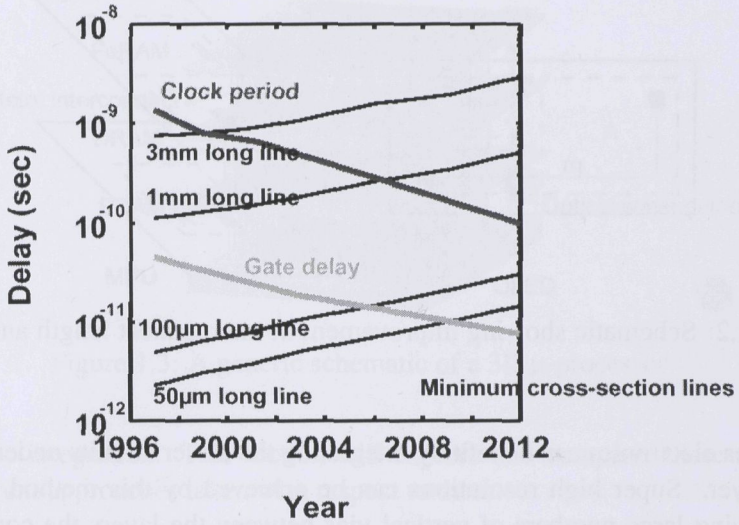


Figure 1.1: Transition of interconnect delay time (black lines for different length), gate delay time and clock period of VLSI over the years [9].

number of metal layers, was introduced by [13]. Noises and parasitic delays as a result of neighboring interconnects can be reduced by shielding as mentioned in [14, 15]. Transmitters and detectors can be used to connect to multiple layers of metal without using a metal line. Moreover, optical interconnects can be introduced to reduce the power loss and cross talk at critical locations of the chip [16]. All of these improvements can also be employed in a 3D IC scheme. In addition, by replacing the long horizontal by short vertical interconnects one can reduce power consumption and delay without interfeing in the technology [17]. It has been proven that three-dimensional integration offers the opportunity to reduce the length of the longest global interconnects in a distribution by as much as 75 percent [18]. Chip performance (speed) can also improved by 145 percent by incorporating 3D IC methods for interconnects [19].

1.1.3 Efficient integration methods

Emerging technologies in sensing applications often require new and novel integration techniques. 3D ICs can be of benefit to these technologies in two ways. First, by separating the sensor layer from the logic and memory layers, a more effective sensing area is created. Higher fill factors are beneficial in fields of photon-detectors [20], image sensors [21] and X-ray detectors [22]. Moreover,

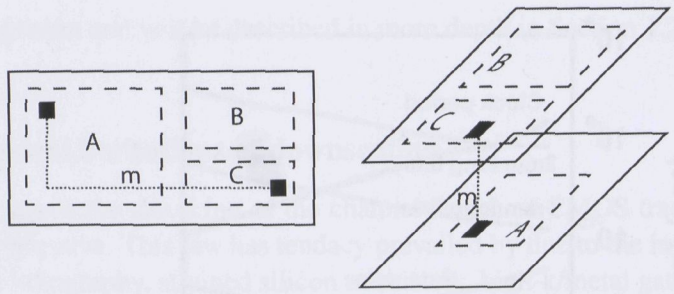


Figure 1.2: Schematic showing improvement in interconnect length and area reduction

large area electronics can benefit by integrating the driver circuits underneath the pixel layer. Super high resolutions can be achieved by this method. Second, by allowing large numbers of vertical vias between the layers the construction of wide bandwidth buses between the functional blocks in different layers is enabled. Consequently, parallel processing needed for applications such as artificial retinas can be realized [23].

To summarize, 3D IC technology is a common solution for all the problems specified above. First, it shortens the interconnect length and thus lowers power consumption. Second, it offers higher chip density without any reduction in transistor dimensions. It also enables an increase in the speed of the system without any increase in power consumption. Third, it increases the functionality of a chip by enabling the integration of a sensor layer on top of it. Each active layer can be processed independently and consequently different technology can be integrated into one system. Finally, since the 3D ICs can stack many device layers, integration density can be improved simply by having the additional integration direction. A schematic of the concept of 3D ICs is shown in Figure 1.3, depicting the principle of the third dimension, with Several layers of active devices and sensors integrated.

1.2 Overview of 3D IC technologies

The challenges, advantages and technologies associated with 3D ICs vary depending on the type of integration. Based on the level of integration, the technologies can be categorized into three groups: package level, wafer level and

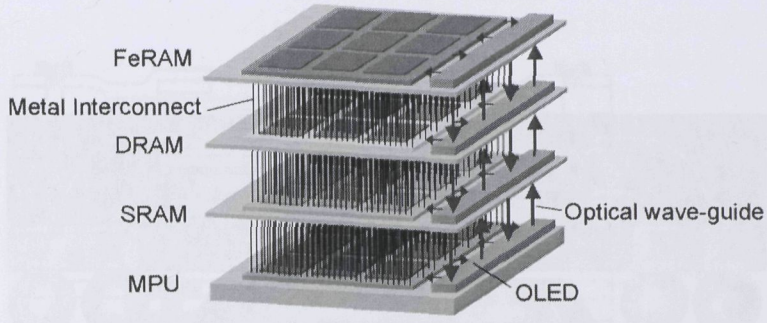


Figure 1.3: A generic schematic of a 3D μ-processor

monolithic integration. This section will explore and compare, these methods and different approaches taken with respect to them.

1.2.1 Package level integration

The move towards the third dimension started with three dimensional packaging. In Package-on-Package (PoP) systems, multiple packages of memory are assembled on fully packaged chips containing logic circuits. An example of such an implementation is shown in Figure 1.4. Traditionally, the interconnect scheme between the several packages is either wire or solder ball bonding [24] . This creates package-in-package (PiP) systems in case of wire bonding, or package-on-package (PoP), which are effective when designing with a limited footprint. They also benefit from relatively matured technologies, being the first method implemented in 3D ICs. However, the density of vertical interconnects is limited due to the large size of solder balls. Thus, when focusing on high-end applications with high interlayer interconnect densities, the advantages of this category of integration are limited. [25]

1.2.2 Wafer level integration

In the mid-1990s, another approach to the realization of the 3D ICs attracted attention: wafer level stacking technology [28, 29]. Stacking the fully processed and packaged ICs led first to the development of the so-called system-in-package (SiP). As shown in Figure 1.6, this technique entails bonding the wafers, which are fabricated using conventional methods, etching-back one of the wafers.

Figure 1.5 shows an advanced SiP incorporating solder balls and through silicon vias (TSV).

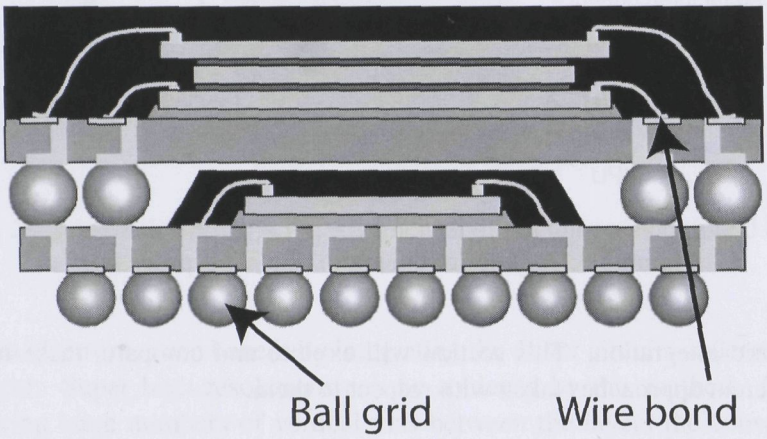


Figure 1.4: A PoP system with two fully assembled packages stacked on top of each other [26].

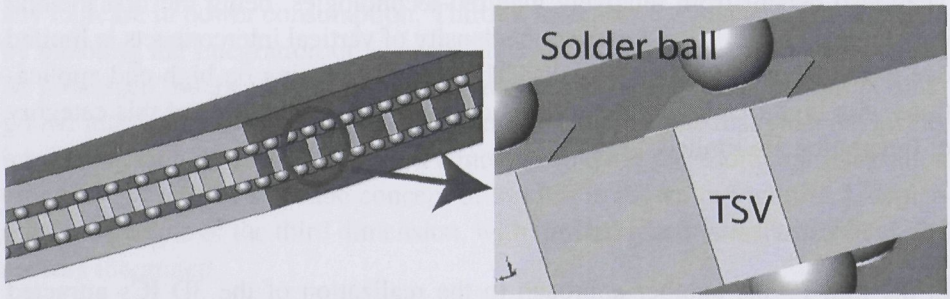


Figure 1.5: Advanced flip-chip bonding employing TSVs and solder balls. The large size of TSV and solder balls limits interconnect density [27]

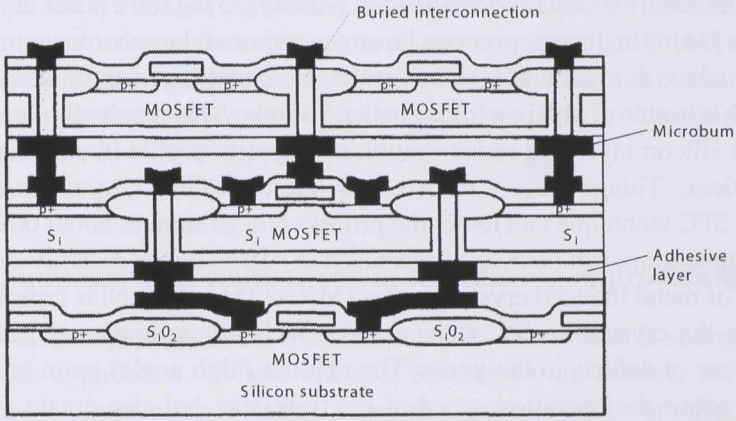


Figure 1.6: Wafer level stacking showing micro bumps [28]

Successful implementation of a multi-layer image sensor system with a digital processing circuit has been demonstrated with "micro-bumps", which connect different layers and improve the uniformity of the bonding. However the bumps occupy a rather large area and, as a result, communication between different layers of the circuit is limited by the small number of the the available bumps. Wafer stacking not only lacks the advantages in terms of performance, but also has numerous technological drawbacks. The pitch between the TSV and micro bumps is strongly dependent on the thickness of the wafer. This is mainly due to process limitations such as aspect-ratio requirements for etching and electroplating. Wafer thinning processes are applied in all successful wafer stacking technologies. This step is not conventional the cleanrooms and has proven challenging in terms of reproducibility [30]. The strain caused by the TSV also affects the transistor properties [31]. Moreover, the best critical alignment dimension reported to date is in the order of micrometers [32]. This is not comparable to monolithic integration which uses a wafer stepper's critical dimension for alignment which results in having an alignment accuracy in the order of nanometers.

1.2.3 Monolithic integration

The idea of monolithic 3D ICs is not new. Attempts to develop 3D integration had already begun in the 1980s. Technically, this was driven mainly by recrystallization of Si film, rather than the direct formation of a c-Si layer on an insulator. Various techniques have been proposed and studied for the enlargement of the grain

size, such as zone-melting recrystallization (ZMR) [33] or solid phase crystallization (SPC) [34]. The former process, however, required the substrate temperature to be maintained at around 1000 °C to assist in the melting of the silicon directly underneath a heater to obtain a high-quality Si films. This resulted in contamination of the silicon layer and redistribution of impurity profile in existing bottom active devices. This process was also slow due to the low output power of the laser. The SPC technique can lower the process temperature to about 600°C. The process temperature can be further decreased to 450°C by the recently developed technique of metal induced crystallization (MIC) [35], where Ni is typically used to catalyze the crystallization. However, this technology inherently generates a huge number of defects in the grain. The random (high angle) grain boundaries not only reduce the operation speed of the transistor, but also create a leakage path. Consequently, a high-temperature annealing is necessary for SPC and MIC material to remove these in-grain defects. Proper device operation could only be obtained after a high-temperature annealing at about 900°C [36]. Because of the difficulties in forming a high-quality Si layer on the insulator, this activity ceased in the late 1980s.

To make monolithic stacking a serious candidate in the industry, some technological issues need to be resolved. First, low defect crystalline silicon should be fabricated at low temperatures. The key to the success of monolithic 3D integration lies in obtaining high-quality substrate material for the upper lying active layers. The μ-Czochralski process which will be described in Section 2.1 is a promising approach with respect to making monolithic integration competitive and attractive. In order to determine a benchmark for "quality" of various substrate, field-effect mobility of the transistors built on those substrates are compared. Field-effect mobility, which characterizes how fast a charge carrier can move through the channel of the transistor, is a suitable measure for benchmarking the quality of several technologies, and comparing them to crystalline silicon (c-Si). The order of the mobilities amorphous silicon (a-Si), polysilicon (poly-Si) and single-grain silicon (SG-Si) are displayed in Table 1.1.

This Table proves the superiority of the μ-Czochralski process compared to other

Table 1.1: Order of mobilities for TFTs based on different substrates

Substrate type	a-Si [37]	poly-Si [38]	c-Si(SOI)	SG-Si [39]
Mobility [cm^2/Vs]	1	100	600	450-1100

low-temperature approaches. Among different 3D IC technologies, monolithic stacking offers the greatest freedom in design, which leads to the most innovative

solutions to the challenges mentioned in the previous section. It also has the potential to have low manufacturing costs, as no expenses are required to develop new equipment or new deep sub-micron processes and no bulk wafer is needed for the upper layers of active logic and sensors since this is obtained during the process.

1.2.4 Summary and comparison of the existing approaches

The choice among the different methods of 3D IC fabrication is strongly dependent on the application. Where low-cost electronics are needed, and the only challenge is to reduce the footprint, for example pico satellite applications [40], package level integration offers the cheapest solution. It simply solves the problem offered by the application. Flip-chip bonding is cheap and may be done at higher temperatures (due to packaging) compared to its competitors. However, this method does not address the current downscaling demands, since the inter package interconnect density is extremely limited according to the pitch road map for this technology, reported in [24].
In cases that require high interlayer interconnect density, wafer level stacking and monolithic integration are the remaining solutions. The advantage of wafer level stacking is that most deep sub-micron technologies can be applied to different wafers, prior to wafer stacking. Furthermore, this method can be applied before low-temperature processes are developed for certain devices which are to be integrated. However, the issues regarding TSV technologies (size, mechanical stress and aspect ratio) and the complexity of the integration process truly limits the prospects for this category of 3D ICs.
With respect to costs, a complete comparison is available in [41]. Monolithic integration is still too novel for any definite statement to be made about costs. However, since no expenses are required for developing new equipment for integration processes, it can be argued that monolithic integration, may be a candidate for the cheapest technology among all existing approaches.

1.3 Structure of this dissertation

The main goal of this dissertation is to study the building blocks of a monolithic 3D IC. Chapter 2 describes the concepts associated with the technologies used and characterizations which recur during this work. The purpose of this chapter is to give a technical introduction to various aspects of monolithic integration.

Laser processing, low-temperature oxides and crystallization methods suitable for monolithic ICs are treated.
Chapter 3 gives a description of two simulation methods, heat transfer and phase-field which are used for thermal simulations during this thesis. Both methods are then compared and it is argued that they have an advantage into being used for a specific goal. This chapter mainly discusses the methods and approaches rather than results. Specific results will be presented in the related discussions throughout the remainder of the dissertation.
Chapter 4 introduces the pulsed laser induced epitaxial growth process, which is proposed as the most promising building block for 3D ICs. This method primarily focuses on high-end applications such as CPU, memory and high speed drivers. The necessity and possibility of obtaining a location- and crystallographic orientation controlled silicon layer will be discussed.
Chapter 5 proposes a lateral P-I-N photo-diode made on single-grains, which can be fabricated at a low temperature. It will be shown that these diodes perform much better than the conventional poly-silicon lateral P-I-N photo-diodes. The application of the μ-Czochralski process in the fabrication and improvement of these diodes will be described. Challenges regarding increasing the thickness of the crystallized silicon will also be addressed.
Chapter 6 demonstrates the possibility of obtaining high performance 3D ICs using the proposed monolithic integration methods. Here, transistors are fabricated on successive silicon layers. Moreover, a comparison will be made between two building blocks of 3D ICs, Single-Grain Thin-Film-Transistors (SG TFTs) based on μ-Czochralski and the PLEG process. Finally, Chapter 7 will present the conclusions of this work and the recommandations that can be made according to the current state of the research.

Chapter 2

Experimental concepts

The aim of this chapter is to explain the concepts behind the technologies associated with the fabrication of single grain thin film transistors (SG-TFTs) which can be used as the building blocks of 3D ICs. The μ-Czochralski process will be explained in Section 2.1. Section 2.3 explains the methods of silicon depositions used in this work. Moreover, the term low-temperature will be defined. Section 2.4 examines excimer laser annealing and its possibilities as a key process in our low-temperature process flow. Another important element in any process leading to high quality transistors is the quality of the dielectric. In Section 2.5 several possibile methods for a obtaining a low-temperature oxide (LTO) are described and compared and the final choice will be justified.

2.1 Location-controlled single grain silicon

The necessity of obtaining high quality silicon containing low defect densities was explained in Chapter 1. The μ-Czochralski process offers the location-control of large single grains created by means of excimer laser crystallization using low temperatures [42]. By controlling the position of the crystallized grains, the channel of the MOS transistors can be designed to fit within such grains. The principle of design in shown in Figure 2.1. The lack of grain boundaries in such grains enables fabrication of high mobility transistors. TFTs with mobilities as high as 600 cm^2/Vs have been obtained [43]. The basic material is a silicon wafer with 750 nm thermal oxide grown on top of it. This layer can be replaced by a low-temperature SiO_2 deposition such as mentioned in Section 2.3. The μ-Czochralski begins by etching 700 nm deep holes with diameters of 1 μm into the thermal oxide. The diameter of the holes is reduced to around 100 nm by

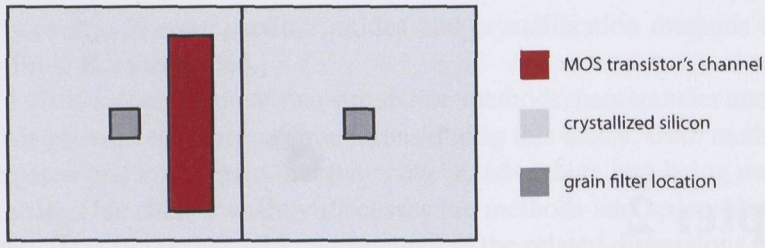


Figure 2.1: Principle of design in location-controlled single grain films

depositing 845 nm thick SiO_2 at 350 °C, with a tetra-ethyl-ortho-silicate (TEOS) precursor, using plasma-enhanced CVD (PECVD). It should be noted that the SiO_2 covers the bottom of each hole, separating the Si layer from the c-Si wafer. In other words, the c-Si wafer is merely a handling substrate and therefore it can be replaced by a glass or quartz substrate. A 250-nm-thick layer of a-Si is deposited using Low-pressure CVD (LPCVD) at 545 °C. The a-Si is then doped with phosphorus and boron dopants with doses in the order of 10^{11} cm^{-2}. This doped layer is then crystallized into arrays of 6x6 μm^2 large silicon grains. Crystallization is then performed by means of a pulsed XeCl excimer laser with wavelength of 308 nm. The 25-ns-long laser pulse has an energy in the order of 1400 mJ/cm^{-2}, limited by ablation of a-Si, which is considered the upper limit of energy density in the μ-Czochralski process. During the crystallization the substrate is heated to a temperature of 400 °C.
The laser melts the silicon to a certain depth in each hole. Solid silicon at the bottom of the hole will act as solidification seed. As the silicon prior to melting is small-grain polysilicon, several grains will grow out of that seed. However, the high aspect ratio of each hole (~8) will filter a majority of the orientations during the process of solidification. Hence the name "grain filter" is given to these holes. Moreover, only one grain can grow out of the seed. Thus the solidified location-controlled grains will have one *random* crystallographic orientations. Figure 2.2(a) shows the schematic structure of the μ-Czochralski process.

2.2 Crystallographic- and location control of single grain silicon

Although the average mobility of SG-TFTs is as high as 600 cm^2/Vs, standard deviation has been as high as 20 percent [43]. This is mainly due to the fact that

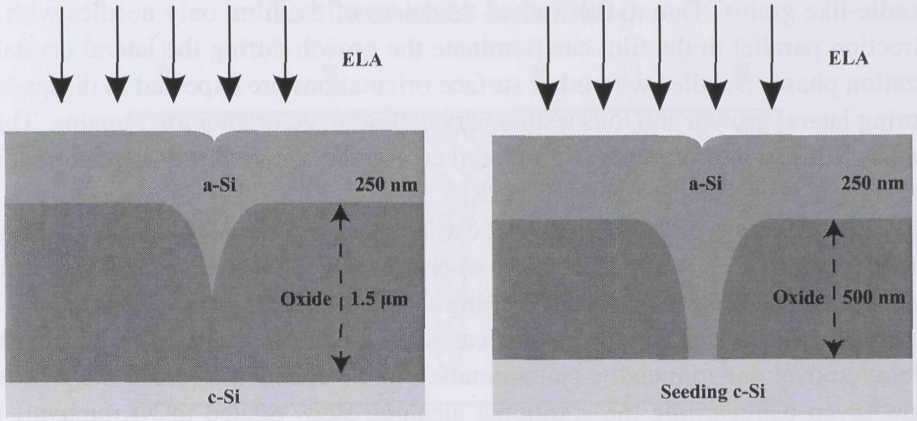


Figure 2.2: The schematic of the final structure shown in (a) and (b) for the µ-Czochralski and PLEG process, respectively

the field-effect mobility of the transistors is anisotropic to the crystallographic orientation of the silicon grains [44]. Thus, in order to reduce variations in the mobility of SG-TFTs, the crystallographic orientation of the silicon in the channel must be controlled. The principle of the design will remain unchanged: the µ-Czochralski process and is used as shown in Figure 2.1. Here we see two adjacent silicon grains with a channel of the TFT positioned in a grain-boundary-less area. In addition to the previous case, the silicon inside the grain has one (that of the seed) crystallographic orientation. In the past, Metal Induced Lateral Crystallization (MILC[1]) has been reported to achieve this goal. The MILC process is a promising approach that can create defect free silicon, enabling fabrication of SG-TFTs with high mobilities. These SG-TFTs have a lower standard deviation in their electrical characteristics compared to SG-TFTs made by the µ-Czochralski process [45]. MILC can reduce the temperature of solid phase crystallization and decrease the time needed for crystallization. The schematic of the process is shown in Figure 2.3. Ni first diffuses vertically and forms NiSi at a temperature below 350°C. After an annealing step above 500°C, the NiSi layer changes into $NiSi_2$ silicides with a <111> orientation. This is possible due to a small crystal mismatch between the two silicides. This transition then propagates laterally in all directions around the Ni pattern. The film is crystallized into

[1] not to be confused with MIC, explained as on of the early approaches in the 1980s to create low-defect silicon at low temperatures

needle-like grains. Due to the limited thickness of the film, only needles with a direction parallel to the film can dominate the growth during the lateral crystallization phase. Needles with other surface orientations are expected to disappear during lateral growth and thus a single crystallographic orientation remains. This makes MILC a good candidate for a seed crystal that can control orientation during the μ-Czochralski process [46, p.28].
However, there are disadvantages that can be related to the MILC process. First, the use of metal (Ni) at the location where the SG-TFT channel will lie, is an unconventional and risky process. Careful and complete removal of this Ni is necessary as the leakage current increases drastically in the case of an incomplete removal due to metallic contamination in the channel. Second, the process flow (even disregarding the additional cleaning steps related to Ni removal) is long and complicated. This leads to the variability of the electrical characteristics of the transistors over the wafer. In case of high-end application such as CPU and memory, a more simple process which guarantees the control of the location- and crystallographic orientation of the silicon grains is needed. The proposed solution in this work is Pulsed-Laser-induced epitaxial growth (PLEG). This in principle adds a seeding layer to the conventional μ-Czochralski process. The schematic of the process is shown in Figure 2.2(b). The process is explained in details in Chapter 4. By opening a hole reaching the seeding layer e.g. bulk c-Si, the amorphous silicon (a-Si) can contacts the seed layer. The principle of this solution is that after melting the a-Si down to the interface with seeding c-Si, the solidification starts from the seed and the molten silicon inherits the crystallographic orientation of the seed during solidification. By using a pulsed laser system one can minimize the thermal damage to the underlying layers during this step. While there has been some research done in the field of laser induced epitaxy [47], a comprehensive study on the subject is still lacking. , as proposed in this work, for lateral overgrowth of orientation-controlled silicon.

2.3 Clarifying "low-temperature"

The term "low-temperature" is used regularly in this work. In the field of semiconductors, this terminology can take on multiple meanings depending on the application. low-temperature electronics can deal with reliability aspects of cryogenic silicon technologies which operate at the temperature of liquid helium and below [48]. Flexible electronics often need temperatures as low as 150 °C since plastic like materials are involved [49]. This limit is also increasing due to ad-

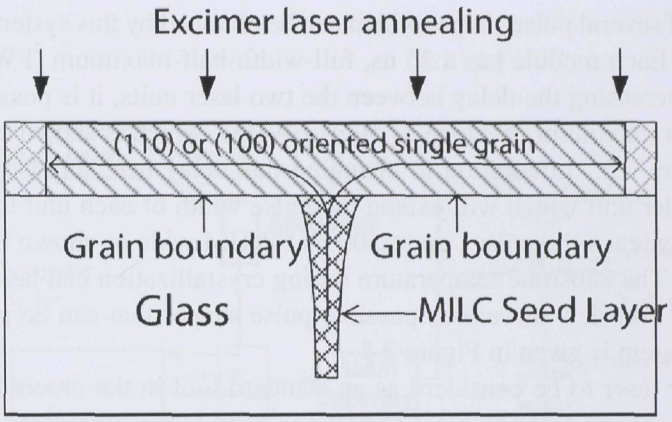


Figure 2.3: Schematic of the MILC process [46]

vances in materials science. Some modern flexible materials can resist temperatures of 350 °C [50].
Another example is the low-temperature used in the classic epitaxy process, which may be anything below 700 °C [51]. The term low-temperature in this thesis, is defined with respect to the monolithic integration of electronics. The upper limit is the temperature at which the underlying active layers will show electrical degradation due to dopant redistribution. However, if metals such as aluminum are used, this temperature will be even lower than that which causes the redistribution of dopants. Thus, this will be the temperature bottleneck of the whole process flow. The hottest step of the process is the deposition of silicon, at 545 °C, any temperature lower than this is thus considered "low". aluminum which is usually used for interconnects cannot survive this temperature. Thus, it may be replaced by a silicide layer. This deposition step can be reduced by using alternative methods such as sputtering or ICP-PECVD. However, this exceeds the scope of this thesis.

2.4 Excimer laser

An excimer laser lies at the heart of the research reported here. A pulsed XeCl excimer laser (λ=308 nm), was used to produce a major part of the results. A schematic of the laser system is shown in Figure 2.4. There are two laser modules which can emit light independently, but can also operate in combination with a certain delay set by the pulse generator unit. The smoothed and normalized

envelopes of several pulse shapes which can be obtained by this system are shown in Fig. 2.5. Each module has a 25 ns, full-width-half-maximum (FWHM), long pulse. By increasing the delay between the two laser units, it is possible a pulse width with a maximum envelope of 50 ns FWHM, which is shown by the green line in Figure 2.5. In addition to changing this delay, we can also engage the pulse extender unit which will extend the pulse width of each unit to 250 ns for each. This extends the pulses up to 500 ns FWHM wide as shown by the black dotted line. The substrate temperature during crystallization can be raised up to 450 °C. An overview of various possible pulse shapes that can be produced by this laser system is given in Figure 2.5.
For excimer laser to be considerd as an standard tool in the process flow of IC fabrication, several technological limitations need to be considered. The main limitations of utilizing an excimer laser are as follows:

- The energy density stability: The physical process that leads to creation of the laser beam causes a variation of the energy density between the pulses. The state of the art excimer laser still suffer from a pulse to pulse energy density variation in the order of 1 percent. This energy density variation may not always be neglected.

- The pulse rate: The state of the art in the case of maximum pulse rate is in the order of 100 Hz. This can act as the bottleneck of the process flow in various applications.

- The spot size: The pulsed excimer laser as mentioned in here, has a limited spot size. There exist an area of overlap between the two adjacent shots. The areas that are shot two times, experience a different thermal history than others. This may ultimately translate into non-usable areas on the silicon wafer. Enlarging the spot size is challanging, yet possible. However, it has its drawbacks such as exponentially higher cost due to the optics of the system, and loss in homogenity

- The energy homogenity: The variation of the energy across the spot size is an issue that combined with the above problems, may lead to final process variation.

2.5 Low-temperature oxide

Silicon dioxide is widely used in integrated circuits. This layer can act as an insulating layer to prevent short-circuits, to provide a gate dielectric in Metal-On-

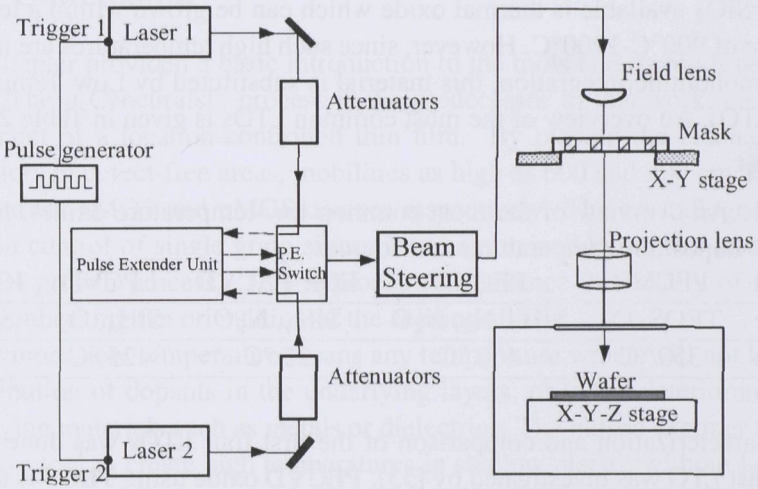


Figure 2.4: Schematics of XeCl pulsed excimer laser system

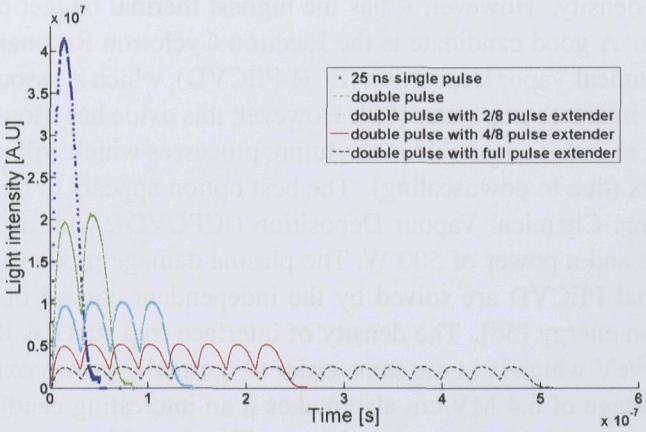


Figure 2.5: Several pulse shapes which can be produced with this excimer laser system.

Oxide Field-Effect Transistors (MOSFET), and as a passivation layer with excellent heat confinement characteristics, whose utility will be discussed throughout this thesis.
The best SiO_2 available is thermal oxide which can be grown within a temperature range of 900°C-1200°C. However, since such high temperatures are not suitable for monolithic integration, this material is substituted by Low-Temperature Oxide (LTO). An overview of the most common LTOs is given in Table 2.1

Table 2.1: An overview of the most common low-temperature oxides, together with their deposition temperatures and sources

Method	PECVD	PECVD	ECR-PECVD	LPCVD	ICPECVD
Source	TEOS, O_2	SiH_4, N_2, N_2O	SiH_4, N_2O	SiH_4, O_2	SiH4, O_2
Temp	350 °C	400 °C	25 °C	425 °C	250 °C

A characterization and comparison of the first four LTOs was done in [52] and the last LTO was investigated by [53]. PECVD oxide using TEOS is the conventional gate oxide for the poly-Si TFTs in LCDs and can produce reasonable results [54]. However the damage done to the silicon surface due to the presence of enhanced plasma during the deposition causes a high density of interface trap states. This is why the alternative methods must be investigated for high performance TFTs. LPCVD oxide leaves a smoother surface and can lower the interface trap density. However, it has the highest thermal budget compared to other methods. A good candidate is the Electron Cyclotron Resonance Plasma-Enhanced Chemical Vapor Deposition (ECR-PECVD), which is associated with a low density of interface trap states [55]. However, this oxide has a low breakdown voltage which makes it unsuitable in the future processes which will contain thinner gate oxides (due to downscaling). The best option appears to be Inductively Coupled Plasma Chemical Vapour Deposition (ICPCVD), with an ICP source of 13.56 MHz and a power of 500 W. The plasma damage problems associated with the normal PECVD are solved by the independent control of ion current density and ion energy [56]. The density of interface trap states is the lowest at $2.2x10^{10}cm^{-2}/eV$ which is in the same order of thermally grown oxide. A good breakdown voltage of 6.4 MV/cm also makes it an interesting candidate for extremely thin gate oxides in the order of 5 nm. The deposition occurs at 250 °C. There are two steps to this deposition: the pre-deposition step in which only O_2 gas alone is fed at a pressure of 0.025 mbar and the following deposition step in which SiH_4 and O_2 are added at a pressure of 0.025 mbar. The total thickness of the gate oxide is 30 nm. The standard deviation of thickness of the deposited

oxide using ICPCVD is only 8 percent.

2.6 Conclusion

This Chapter provided a basic introduction to the tools and methods used in this work. The μ-Czochralski process is the predecessor to this work, enabling the attainment of a location-controlled thin film. By placing the channel of TFT transistors in defect-free areas, mobilities as high as 600 and 200 cm^2/Vs can be obtained for nMOS and pMOS devices respectively. The crystallographic- and location control of single grain silicon can be obtained by pulsed laser induced epitaxial growth process. This approach can enhance the quality of the SG-Si film by inheriting the orientation of the seeding silicon.
Furthermore, low-temperature means any temperature which will not lead to the redistribution of dopants in the underlying layers, or to the deterioration of the underlying materials such as metals or dielectrics. The pulsed excimer laser is an attractive tool to create high temperatures in shallow places, without heating the entire structure. The laser used in this work can have a heated substrate of 450 °C. It contains two laser sources, each having a 25 ns long FWHM pulse. There is also a pulse extender unit which can be utilized to obtain a longer pulse. The LTOs chosen were PECVD for passivation, and ICPCVD for the gate dielectric. ICPCVD shows superior characteristics compared to the rest.

Chapter 3

Numerical analysis of the pulsed excimer laser annealing process

This chapter discusses several numerical methods for simulating the excimer laser annealing. The main goal of these simulations is to gain a solid understanding of the melting and solidification of thin films (Si, Ge and $TiSi_2$) when irradiated by laser beam. Each method has its strength and weaknesses. The methods shown in here will be used as the basis for the discussion and comparison in the following chapters. In this chapter, Section 3.1 presents the key physical constants used in all simulations. The modeling of the heat source, being mainly but not only the excimer laser, is also discussed. In Section 3.2 three types of simulation methods are explained, all of which are implemented using the Finite Element Method (FEM). Section 3.3.1 deals with the simulations of a μ-Czochralski process using a thick layer of silicon. The simulation of the Pulsed Laser induced Epitaxial Growth (PLEG) will be demonstrated in Section 3.3.2. Controlled crystallization of germanium is also reported. The simulations related to this process are being discussed in Section 3.3.3. Finally, the thermal behavior of the silicon and titanium during the laser induced silicide formation are simulated , in Section 3.3.4.

3.1 Material constants and expressions

Regardless of the method of simulation, macroscopic constants of a thermodynamic system are needed. The main expressions are shown in Table 3.1.

Here, ρ is the mass density, $K(T)$ the temperature dependent heat conductivity, $c(T)$ the temperature dependent specific heat capacity, T the temperature,

Table 3.1: The main thermodynamic properties of the materials used in the numerical simulations

Mass density ρ [Kg/m^3]	
SiO_2, α-Si, l-Si and c-Si	2200, 2250, 2520 and 2330 (resp.)
Thermal conductivity $K(T)$[W/m·K]	
SiO_2 [57]	$(1.005+1.298\times10^{-3}\times T)\times H(T-1170)+$ $2.512\times H(1170-T)$
α-Si [58]	$1.3\times10^{-9}(T-900)^3+1.3\times10^{-7}(T-900)^2+$ $10^{-4}(T-900)+1$
c-Si [57]	$1.5\times10^5\times T^{-1.226}\times H(T-1200)+900\times$ $T^{-0.502}\times H(1200-T))$
l-Si [57]	$50.2+2.99\times10^{-2}(T-1687)$
Specific heat capacity $c(T)$[J/kg·K]	
SiO_2 [57]	$708+0.299\times T$
α-Si & c-Si [57]	$810+0.13\times T-1.26\times10^6\times T^{-2}$
l-Si [59]	$909-0.227\times(T-1687)+4.871\times10^{-4}(T-$ $1687)^2$
Reflectivity [a.u]	
α-Si , c-Si , l-Si and SiO_2	R = 0.55 , 0.65, 0.7 and 0 (resp.)
Absorption coefficient [m^{-1}]	
α-Si [57]	$\alpha = 1.5\times10^8$
Melting point [K]	
α-Si & c-Si [59]	1420 & 1687 (resp.)
Latent heat (solid/liquid) [J/kg]	
α-Si	1.32×10^6
c-Si	1.79×10^6

and x and t are the space and time coordinates, respectively. $c(T)$ and $K(T)$ are obtained from the literature [listed in Table 3.1]. The initial and ambient temperatures vary from 0 to 450 °Cdepending on the simulation. $L(x,t)$ [W/m^3]is the heat source of the simulation:

$$L(x,t) = (1 - R_{surface})E_{laser}Pulse(t)\alpha \exp(-\alpha x) \tag{3.1}$$

Here, $R_{surface}$ is the reflectivity of the surface material, Pulse(t) [s^{-1}] the time dependent profile of the laser pulse, α [m^{-1}]] the absorption coefficient of the absorbing material and E_{laser} is the energy density [J/m^2] of the laser light. Reflection of the light between the upper and underlying layers is neglected. In case of silicon, no power will penetrate deep to the underlying layer. In case of SiO_2, this layer is completely transparent to this specific wavelength. Furthermore, in all of the methods of simulation explained in Section 3.2, α and $R_{surface}$ change with the state of the surface material. If a material melts, both these values are then changed to make the laser heat modeling more accurate. E_{laser} and Pulse(t) act to model of the laser light and are divided in to an intensity element, E_{laser}, and a duration and shape part Pulse(t). The remainder of the equation deals with how material experiences the incoming light, by specifying reflection and absorption coefficient. This method of modeling allows an optimal and convenient comparison between the different types of pulses as explained in Section 2.4.

Boundary conditions Laser processing occurs in a high vacuum and heat dissipation through convection is thus negligible. The ambient temperature is set by applying heat to the wafer holder. Since the mass of the wafer holder is infinite in comparison to the wafer, the wafer temperature does not affect the temperature of the wafer holder. Thus, the bottom of the wafer is set to have a Dirichlet boundary condition with a constant temperature. All other boundaries with air are set to have a Neumann boundary condition which indicates that the heat flux is continues at these interfaces [60].
Surface emissivity is a phenomenon that contribes to the heat flux streaming out of the surface of the simulation. This can be simulated using the boundary condition set on the surface of the sub domain, which absorbs the laser light. Surface emissivity indicates thermal radiation from a body through the conversion of a body's thermal energy at any temperature greater than absolute zero. The rate at which this occurs is a product of emissivity and the Stefan-Boltzmann constant. The thermal radiation from the heated silicon to the vacuum chamber can be calculated using equation 3.2. Despite the high temperatures that silicon reaches

during the annealing process, it becomes obvious that the added value by of this source of cooling is over 15 orders smaller than the laser source. Therefore, the effect of surface emissivity was omitted in the following simulations.

$$E = \epsilon\sigma(T_{amb}^4 - T^4) \tag{3.2}$$

In this equation ϵ is the Stefan-Botlzmann constant and σ is the surface emissivity of silicon. The ambient temperature can have a value between room temperature and 450 °C, depending on the type of simulation.

3.2 Methods of simulation

3.2.1 Heat diffusion method

A heat diffusion method allows for the simplest modeling a thermal processing step such as laser annealing. It's most simple form is shown in equation 3.3. This method entails a set of partial differential equations (PDEs) based on Fourier's law of conduction.

$$\rho C_p \frac{\partial T}{\partial t} + \nabla(-K\nabla T) = Q \tag{3.3}$$

Q is the heat source or the external thermal input of the system, $K(T)$ the thermal conductivity, ρ the mass density and $C_p(T)$ the specific heat capacity [61]. Since there is a thermal gradient across the sub domains, the temperature is location dependent. All the physical constants are well explained in Table 3.1. One of the advantages of this method, along with its simplicity is the short calculation time. The simulation times are in the order of seconds for one dimensional structures, and in the order of minutes for three dimensional structures. With respect to the accuracy of the simulated temperature history, this depends on the modeling efforts that are included in the equations. The term Q may merely contatin the laser source as in equation 3.1, or it may also include the latent heat created from the melting and solidification of the material. The addition of the latter makes the simulation more accurate, but also significantly slower. Melting can be simulated by converting the constants described in Table 3.1, mainly, heat capacity, conductivity, mass density and reflectivity into step functions. Once enough heat is applied into the system to elevate the temperature up to the melt temperature and provide the latent heat needed for phase transition, these constants will change abruptly. However, with this simple modification, the annealed silicon will also solidify at the melt temperature of amorphous silicon (becomes amorphous again after melting) which is not realistic. This transition is shown in Figure 3.1.

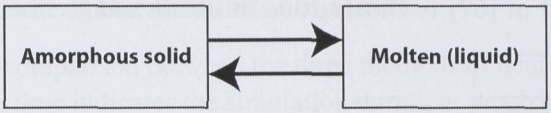


Figure 3.1: This schematics describes the phase transitions in case of heat diffusion method. Since the temperature is the only unknown, the subdomains can consist of two phases, seperated by the melt temperature.

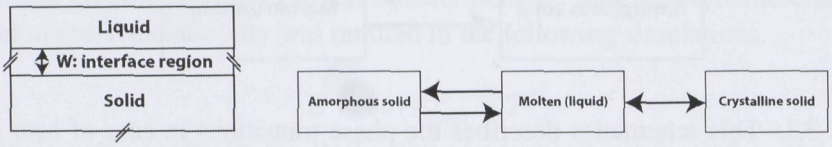
3.2.2 Heat diffusion method with adaptive meshing

As it will be seen below, phase-field simulation produces highly precise results. However, observation of the trend of relative values often satisfies to draw relevant conclusions. Addition of the latent heat to the heat diffusion method leads to having a simple phase transition. However, this increases the simulation time drastically. Thus, in cases that preciese phase detection with multiple transitions is needed, as shown in Figure 3.2(b), SEPRAN finite element package, a code developed an in-house at TU Delft [62], appears to be the best compromise. This program incorporates a smart meshing technique that allows the mesh to be smaller only when it is necessary, that is the interface of the solid and liquid. In this way, one can achieve thermal and phase history close to the phase field method with simulation times in the order of the standard heat transfer by conduction method.

3.2.3 Phase-field method

Phase field models offer a different approach to solving the problem of the temperature evolution of the system. The actual unknown here is the position of the interface between the solid and liquid material. The velocity of the interface is temperature dependent [63]. These kind of models are designed to solve the Stefan problem [64–66]. Phase-field methodology offers solutions to the free boundary problems introduced by the melting and solidification of films after excimer laser annealing (ELA). The main advantage of this methodology is that the position of the interface between two different phases is known as a phase variable(Ψ) . This variable has a finite width and couples the macroscopic physical constants, such as heat capacity and conduction, to microscopic ones such as surface tension and diffusivity. The dynamics of phase transitions can be modeled using two partial differential equations (PDEs) which are coupled together by coupling equations. There are different methods for choosing the coupling equations. The

method explained in [67] is chosen, due to its advantage in convergence. The



(a) (b)

Figure 3.2: (a) shows the three existing regions within a sub domain after a melt is initiated. W is the width of the interface region, between the solid and liquid. The transition between three phases is depicted in (b).

basic phase-field equations are as follows:

$$\tau \partial_t \Psi = W^2 \nabla^2 \Psi - \frac{\partial F(\Psi, \lambda u)}{\partial \Psi} \tag{3.4}$$

$$\partial_t u = D \nabla^2 u + \partial_t h(\Psi)/2 \tag{3.5}$$

where $u(T,t) \equiv (T - T_M)/(L/c_p)$ is the dimensionless temperature field, W the interface thickness between the solid and liquid phases, τ the measure for surface relaxation time, λ a dimensionless parameter that controls the coupling between the phase and diffusion fields, L the latent heat and c_p the phase-dependent specific heat capacity of the material in the sub domain. F is a function of Ψ and λu, and can be separated into two functions of f and g as follows:

$$F(\Psi, \lambda u) = f(\Psi) + \lambda g(\Psi) u \tag{3.6}$$

$$g(\Psi) = \frac{b}{2} h(\Psi) \tag{3.7}$$

where b is a normalization factor obtained from the values of $h(\Psi)$ at solid and liquid state (between +1 and -1). The coupling between the heat diffusion equation and phase equation is set in this way manner.

In practice, we have a three phase system: amorphous, crystalline and liquid. To optimize the simulation time, the amorphous phase is removed by introducing a flag which can change the properties of the amorphous domain permanently once melting has occurred. In this way one extra PDE becomes no longer essential.

Figure 3.2(a) explains the definition of the three main regions within a sub domain after melting. Solid, liquid and the interface region between them can all have independent PDE equation sets. The most common equation sets are those for the dopant evolution during an ELA process, which may be addressed independently for each region.

3.2.4 Comparison of the simulation methods

Table 3.2 shows a comparison between the three methods of heat simulation used in this work. Here, time indicates the simulation duration; precision the similarity of the results to the experimental data, convergence the difficulty of making the simulation converge, customizability the ease of changing the layer stack with the guarantee of convergence, and expandability that indicates whether the simulation method is suitable to being expanded with new sets of equations that simulate physical phenomena, such as the segregation of dopants during excimer laser annealing.

Table 3.2: A comparison between three simulation methods utilized in this work.

	Time	Convergence	Customizability	Expandability
Diffusion	+	-	++	- -
Adaptive mesh	++	+	++	-
Phase field	- -	++	- -	++

3.3 Overview of the simulations performed

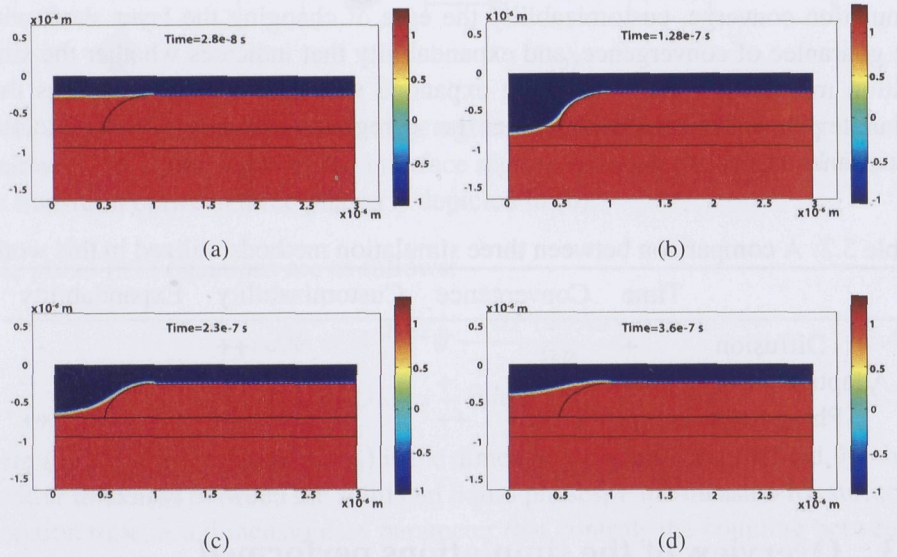
3.3.1 Simulation of the μ-Czochralski process

The μ-Czochralski process is explained in Section 2.1. A 2D heat transfer method was used to simulate the μ-Czochralski process. A phase-field method is not required as the exact melt depth is not crucial to the mechanism of growth. Moreover, whether the melted front fails to or succeeds in reaching the bottom of the grain filter, its effect on the size of the grains is negligible.

3.3.2 Simulation of the pulsed laser induced epitaxial growth of silicon

The PLEG process is described in details in Chapter 4. A three-dimensional phase-field simulation was used to track the melt front, and examine its behaviour upon reaching the a-Si/c-Si interface at the bottom of the seeding hole. Figure 3.3.2 shows the evolution of the phase element of this simulation. One can observe that the absorption of the laser energy is uniform across the grain area. However, as the time passes, the areas containing more silicon i.e. the seeding hole, heats up earlier. In this simulation, a 250 ns long laser pulse was used with

an energy density of 1900 cm^2/Vs. The temperature of the substrate was elevated to a temperature of 450 °C. Using these parameters, it is predicted that the epitaxial growth would be performed from the c-Si of the seeding layer.



(a) (b)

(c) (d)

Figure 3.3: These figures show the evolution of the Ψ in time. First the top surface is melted. Silicon has a higher conductivity than SiO_2 and thus it gets heated faster in the grain filter in comparison with planar areas. The non linear front of solidification is a essential for an understanding of the role of the sidewall angle in defect formation.

3.3.3 Simulation of the µ-Czochralski process with germanium

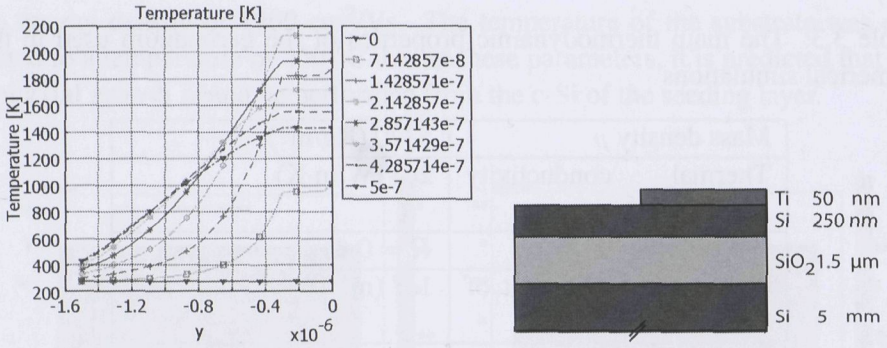
The thermodynamic properties of germanium needed for a numerical simulation are presented in Table3.3. The main difference in the thermal character of germanium in comparison with silicon lies in its much lower reflectivity, lower melting temperature and less thermally dependent conductivity. The lower reflectivity of the Germanium leads to a more optimal absorption of laser power. The absorption coefficient is about one order higher in the magnitude than that of silicon. This means that more heat will be absorbed at a thinner depth from the surface.

Table 3.3: The main thermodynamic properties of the germanium used in the numerical simulations

Mass density ρ	5320 (Kg/m^3)
Thermal conductivity $K(T)$	2e4 (W/m·K)
Reflectivity (Ge)	$R = 0.4$
Absorption coefficient of Ge [57]	1e7 (m^{-1}])
Melting point Ge [59]	1211 K

3.3.4 Simulation of silicide formation during the excimer laser annealing

The thermodynamic properties of titanium needed for a numerical simulation are presented in Table3.4. Titanium has the highest absorption coefficient and lowest reflectivity. These two characteristics ensure that using a capping layer of titanium, one can selectively create a hot-spot while maintaining the lower temperatures in the open areas. This characteristic is also used for activation of the source and drain dopants of extremely downscaled MOS transistors. Here, this allows one to make the Ti/Si region as hot as 2200 K, with fluencies of approximately 500 mJ/cm^2. The simulation of the silicidation process is based on the heat transfer by conduction method, explained in 3.2.1, with no melt depth following. A thermal history of different thicknesses of titanium against the depth of the structure with several process conditions is depicted in Figure 3.4(a). This reveals that Si is completely melted whereas Ti is not melted. Silicide grows at a solid-Ti/molten-Si interface.



(a) (b)

Figure 3.4: A thermal history of different thicknesses of titanium against the depth of the structure is shown in (a). (b) shows the schematic of the stack during the silicide formation at source and drain regions of the transistors.

Table 3.4: The main thermodynamic properties of the titanium used in the numerical simulations

Mass density ρ	4.5e3(Kg/m^3)
Thermal conductivity $K(T)$	2.1e6 (W/m·K)
Reflectivity (Ti)	$R = 0.38$
Absorption coefficient of Ti [57]	1e8 (m^{-1}])
Melting point Ti [59]	1941 K

3.4 Conclusions

In this Chapter, three methods of simulation, the diffusion method, the diffusion method with adaptive mesh and the phase-field approach were explained and compared.

phase-field is precise and provides data about the phase between a solid and liquid. This makes it an attractive approach for PLEG process simulation, where the melt depth is an important aspect. However, it is relatively slow. The diffusion method is highly adaptable, since commercially available software can be used. Diffusion method with adaptive mesh, allows the system to be heavily meshed, in

places where this is required. Thus it offers a proper ratio of speed and precision. It is superior to the standard diffusion method in all cases. However, editing the structure, or 3D structures are more challenging to realize using this method.

Chapter 4

The pulsed laser induced epitaxial process

SG TFTs are the building blocks of a 3D monolithic IC. While the μ-Czochralski process enabled the fabrication of these high mobility transistors, the pulsed laser enduced epitaxial growth (PLEG) process is as an approach able to control the crystallographic orientation of the location-controlled SG-Si films. This control of orienatation is needed in order to increase the overall uniformity of the electrical characteristics of SG TFTs which use these films as the channel material.

4.1 Introduction to the PLEG

This section will explain the PLEG process will be explained. The process flow will be described, followed by the crystallographic orientation inheritance and the critical requirements for a successful epitaxial process. This process is simple and reproducible in comparison to other proposed methods, such as MILC. This process can be used for monolithic 3D integration in compared to its predecessor, 3D integrated SG TFTs based on the μ-Czochralski process.

4.1.1 Process flow for the PLEG

The steps of the PLEG process are shown in Figure 4.1. The process starts with deposition of 500 nm thick SiO_2 by plasma enhanced chemical vapor deposition (PECVD) on top of a <100>-oriented wafer, which is either bulk or silicon-on-insulator (SOI). This is performed at 350 °C by using tetra-ethyl-ortho-silicate

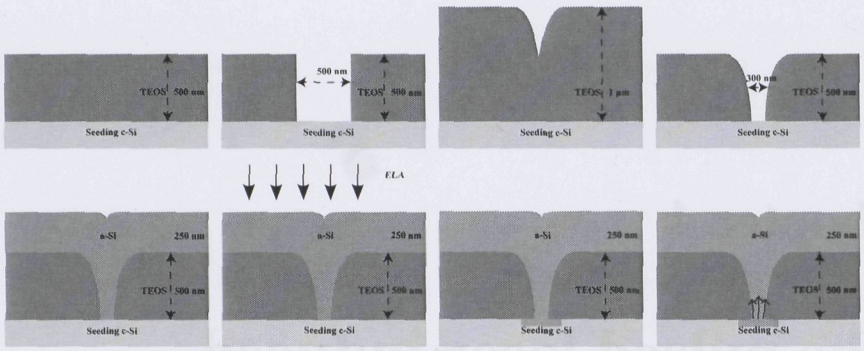


Figure 4.1: The PLEG Process Steps

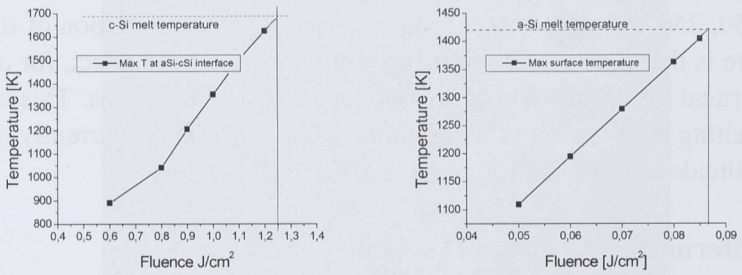
(TEOS) as precursor. We pattern 500 nm [1] wide holes by dry etching the SiO_2. The diameter of the holes is reduced by deposition of a 500 nm of SiO_2, followed by mask-less anisotropic dry etching. The spacers created in this manner reduce the hole diameter down to 200-300 nm. The cavities are filled with 250 nm thick low-pressure chemical vapor deposition (LPCVD) a-Si at 545 °C. Pulsed XeCl excimer laser (λ=308 nm), explained in Section 2.4, is used to melt the silicon.

4.1.2 Orientation inheritance

Upon laser irradiation, the energy is absorbed in the first few nanometers of the a-Si layer. This heated layer melts and serves as a heat source for the underlying layers. As a result of explosive crystallization, the surface will soon cool down [68]. However, this phenomenon was not implemented in the simulations. As the melting continues to sink deeper into the a-Si layer, the c-Si seeding layer is reached by the melt front. Since the melting temperature of the c-Si is almost 200 °C higher than a-Si, it does not always melt just by coming into contact with the molten-Si front. In the case that the c-Si interface is not reached, the seed for solidification will be fine grain polysilicon. Thus the crystallized layer will have multiple crystallographic orientations which means that the epitaxial growth will not succeed. We define the onset of epitaxial growth to be when the laser energy density by provides sufficient energy to raise the temperature at the interface of seeding c-Si and a-Si to crystalline silicon's melting point of c-Si and provides the required latent heat from the c-Si for melting. This results in

[1] For means of process observation and monitoring, hole diameters in the masks were varied from 0.5 to 2 µm. Final hole diameters are from 300 nm to 2 µm. Yet, the SG TFTs are made using the film crystallized op top of the 500 nm wide holes

a successful epitaxial process in which, the crystallized a-Si layer will have the same crystallographic orientation as the c-Si of the seeding layer.



(a) (b)

Figure 4.2: Simulated maximum temperature reached at the a-Si/c-Si at the interface of the seed openings is shown in (a) with different irradiation energy densities. Simulated maximum temperature reached at the a-Si surface is given in (b), which indicates how high the surface temperature will rise. The simulation was performed for a 250 nm thick a-Si layer irradiated with a pulse duration of 250 ns at an elevated substrate temperature of 400 °C.

The maximum temperature at the a-Si/c-Si interface is shown as a function of the laser energy density in Figure 4.2(a). During several simulations, we monitor the temperature of this interface while increasing the laser energy density. It was observed that the onset of epitaxial growth was realized at least 1400 mJ/cm^2 laser energy density. With densities lower than this value, the c-Si interface will not melt and growth will then start from an explosively formed poly-Si seed. This laser energy was then used further to investigate the mechanism of epitaxial growth. Figure 4.2(b) compares the temperature difference between the surface of a-Si and the seeding window interface. From extrapolating this data we may conclude that the melting of the Si surface starts at approximately 100 mJ/cm^2. The melted depth is in the order of several nanometers and is related to the absorption length.

4.2 Pulsed laser induced epitaxy of PECVD silicon

This section investigates a-Si deposited at low temperatures, for use as basic material of the PLEG process. The highest process temperature during the fabrication (550 °C) and integration of multiple layers of active devices occurs in

the LPCVD deposition of silicon. While this is still a valid low temperature for monolithic 3D IC, using this high temperature limits the number of flexible materials, to be used as the substrate in order to realize the 3D ICs on glass and flexible plastic substrate. Glass, kapton, PEN and PET can withstand temperatures of 450, 350, 250 and 150 °C respectively. Another limitation of this high temperature is the impossibility of using aluminum as interconnect, for underlying and vertical interconnect between two layers of active devices. This is due to the low melting temperature of aluminum ($\sim$ 660 °C). This is currently resolved by using silicide as it will be further described in Chapter 6.

4.2.1 Alternatives to LPCVD silicon

There are several methods of low temperature silicon deposition. However, since the aim here was to develop a process which could be seamlessly integrated into current process flows, evaporation was not investigated due to its potential low throughput. The practical options remain sputtering and PECVD methods. Efforts to make sputtering a reliable process can be found in [69]. Due to high stress, Argon incorporation and worse step-coverage of sputtered silicon, the efforts in this work were aimed at PECVD silicon. The step-coverage of PECVD films was found to be approximately 70 percent, thus enough to fit to the PLEG process as it is shown in Figure 4.3. PECVD silicon can be deposited at 350 °C[2] with a high hydrogen incorporation of roughly 10 percent. Laser crystallization of these films was not successful. Excimer laser crystallization was performed with a sweep of energy density, from 500 to 1200 mJ/cm^2, with both at room temperature and at 400 °C elevated chuck temperature. Figure 4.4(a) shows that explosion of silicon due to a high hydrogen concentration was severe and caused the film to become porous. From other experiments, porous films are known to be unable to form large grains.

4.2.2 Pre-annealing methods for crystallization quality improvement

In order to make the PECVD silicon films suitable for crystallization, furnace annealing was performed in a vacuum for 0.5,1 and 2 hours at 600°C, to dehydrogenate the layer prior to the excimer laser crystallization. An example of a furnace-annealed sample after crystallization is shown in Figure 4.4(b). As it is visible in this figure, the number of voides has been reduced.

The Infrared (IR) laser annealing is an alternative approach for annealing the films. With its millisecond irradiation regime, it offers a less "harsh" method of

[2]It can also be deposited at 300 °C, but the quality is not satisfactory.

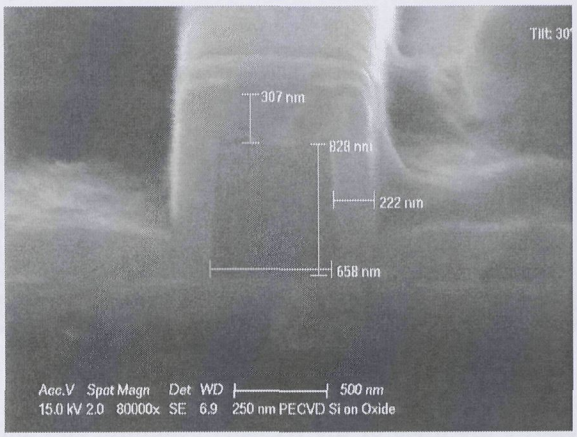
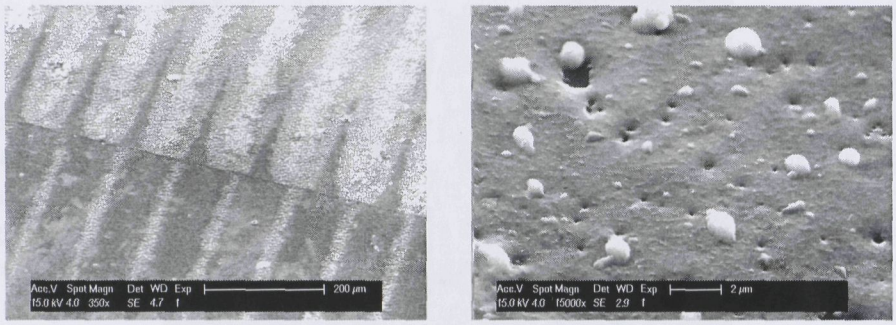


Figure 4.3: The cross-sectional SEM image showing step-coverage of PECVD a-silicon deposited at 350 °C

(a) (b)

Figure 4.4: (a) displays the crystallization attempt for a 300 nm thick as-deposited PECVD film, while (b) shows the SEM image of the film which has received furnace annealing at 600 °C followed by a laser crystallization.

annealing. Thus, it is a suitable candidate for pre-anneling the silicon films prior to the excimer laser crystallization. The process parameters of this laser, to gather with the conditions used for the pre-annealing is explained by [70]. Figure 4.5(a) shows the IR laser scanning and annealing prior to crystallization. It is concluded that the amount of degassing of the film is comparable to the furnace annealing. Thus, the addition of the IR pre-annealing to the excimer laser crystallization does not lead to large single grain formation.



(a) (b)

Figure 4.5: (a) shows the lines of the IR laser scanning and annealing the film, prior to crystallization. (b) shows a more magnified SEM image of the annealed film. Degassing of the PECVD film with higher temperatures remains unsolved.

Novel deposition methods, with in-situ annealing may be the best option for a PECVD silicon with a low hydrogen content deposited at low temperatures [71].

4.3 Pulsed laser induced epitaxy of LPCVD silicon

By using the LPCVD method the deposited silicon contains less hydrogen i.e. 5 percent less, and thus is more suitable for crystallization. This can be used in a preliminary stage allowing research on other aspects of 3D IC.

4.3.1 The effect of substrate type and substrate temperature

The temperature at specific positions in both SOI and bulk wafer seeding structures was plotted against the increasing laser fluency. A substrate temperature of 450 °C and a pulse width of 70 ns were considered in the phase-field simulation. The schematic of each structure is shown in Figure 4.8.

Figure 4.6 shows the onset of epitaxial growth with both SOI and a bulk seed layer against increasing laser energy density. The structure with SOI wafer seeding reaches the onset of epitaxial growth with at approximately 100 mJ/cm^2 less energy density than that of the bulk wafer seeding, which means that one less laser energy is required for an epitaxial growth in the structure with SOI wafer seeding. The SOI wafer also has a thinner seeding silicon layer at the seeding

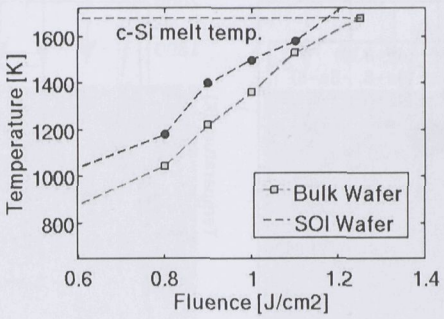


Figure 4.6: The onset of epitaxial growth with both SOI and a bulk seed layer against increasing laser energy density.

area. Since c-Si has a higher thermal conductivity than SiO_2, the SOI seeding also offers a greater heat confinement.

Table 4.1: Overview of process window, with respect to various process conditions and seeding substrates

Pulse width	25 [ns]		250 [ns]	
Seed type	Ablation	Epitaxy	Ablation	Epitaxy
SOI	1500	1400	2000	1500
Bulk	1550	—	2200	1600

4.3.2 The effect of the pulse width

A simulation based on heat transfer through conduction as described in Section 3.2.2 using two pulses of 25 ns and 250 ns produces Figure 4.7. Here the temperature history is shown for several coordinates in the structure. The x coordinate stands for the lateral position in [m], from the center of the epitaxy hole and the y values for the depth of the structure from the surface, in [m]. The schematic of each structure is shown in Figure 4.8.

One can observe that while the c-Si/a-Si interface reaches the same temperature ($\sim$ 850 K) within similar times, the maximum surface temperature is decreased by 600 K less using the longer pulse. The ablation temperature of silicon is assumed to be roughly around its boiling point of 3200 K [72, 73]. Although

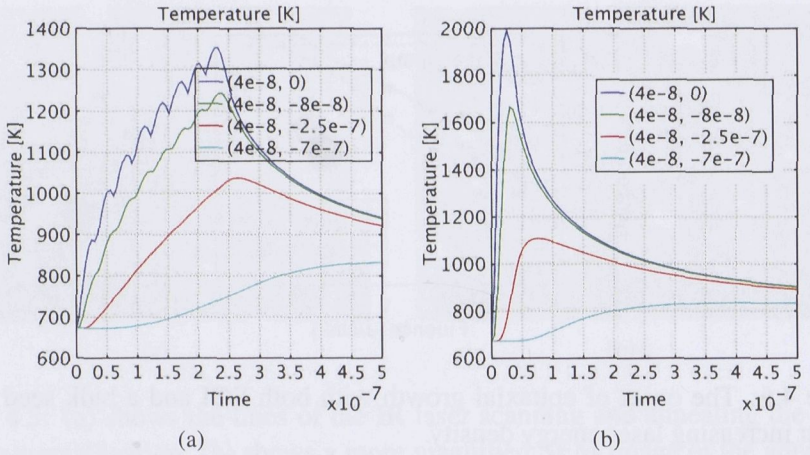


Figure 4.7: Simulated temperature history, for two different pulse widths of (a), 25 ns and (b), 250 ns , with the same energy density of 1400 mJ/cm^2. Bulk seeding was considered in this calculation. The coordinates depicted are in [m]. The x value stands for the lateral position, zero begin the being center of the epitaxy hole, and y for the depth of the structure.

this temperature was not reached in this simulation, the surface temperature of both structures can be relatively compared. It was found that the ablation threshold is increases due to a more uniform temperature profile in terms of depth. In the case of a long pulse causing more energy to be given to the structure and resulting in a deeper melt. By using shorter pulses, the heating is more abrupt, causing the maximum surface temperature to reach the ablation temperature. The experimental counterparts of these results are summarized in Table 4.1, showing the onset of epitaxial growth and the time required to reach the ablation threshold. The process window is defined to be the energy density difference between the onset of epitaxy and the ablation threshold. Ablation is not an abrupt event at die level. Comparing the onset of epitaxy between using the short and long pulses, it is obvious that the process window is increased by using longer pulses. This is valid for both SOI and bulk wafer seeding. This can be explained by the more uniform temperature profile in the case of a longer pulse, which is due to the more uniform heat flow in to the system. One may observe that while using the shorter pulses, the SOI wafer still leads to successful epitaxy. However, the onset of epitaxy is so close to the ablation threshold of the bulk wafer seeding structure, that no large area epitaxy is observed. The bulk wafer responds better

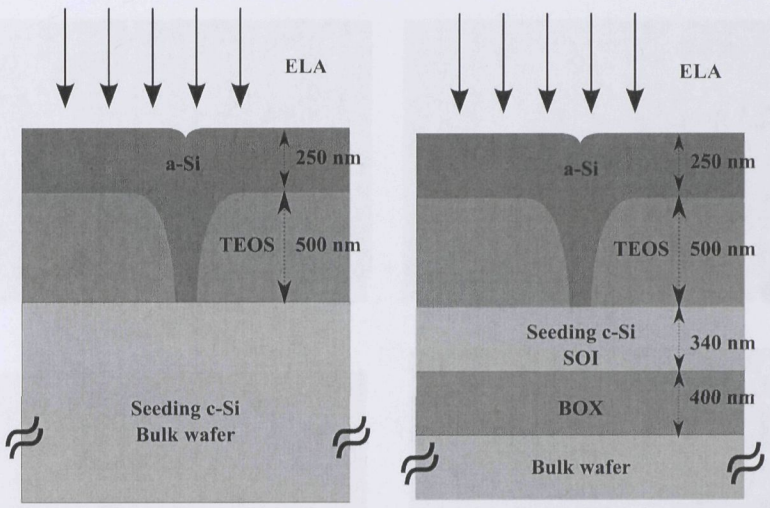


Figure 4.8: The schematics of the PLEG process with different seeding substrates is shown.

using a longer pulse since the increase in process window larger in case of the bulk wafer seeding. Moreover, The heat sink of this structure is better than the SOI wafer causing the flux towards the heat sink to be larger in magnitude. In other words, while the surface is not ablated which occurs in the case of short pulses, the surface remains cooler and allows more heat to flow into the system without reaching the ablation threshold.

Figure 4.9 shows the SEM image of an array of grains crystallized at 1400 mJ/cm^2 laser energy density. Since this energy is lower than that required for the onset of epitaxial growth, no epitaxial growth will occur. The red lines are drawn to emphasize the contrasts that exist within each large grain, which indicate the existence of several sub-grains. Figure 4.10(c) and 4.10(d) show an EBSD measurement of a 25 x 25 μm^2 large array of grains, similar to the SEM image in Figure 4.10(a) and 4.10(b). This indicates that there are many crystallographic orientations exist in the surface of the crystallized layer. Figure 4.10 the SEM image of an array of grains, which were crystallized by a 250 ns pulse with an energy density of 2000 mJ/cm^2. This energy is higher than values mentioned as for the onset of epitaxy in Table 4.1. One can observe that the epitaxy in the case of bulk wafer seeding appears less defective. This could be due to the fact that the crystalline quality of bulk wafer is generally higher than an SOI wafer. Figure 4.10 shows a EBSD measurement of 25 x 25 μm^2 large grain array, similar to the SEM image of Figure 4.10 . This indicates that the <100> is the

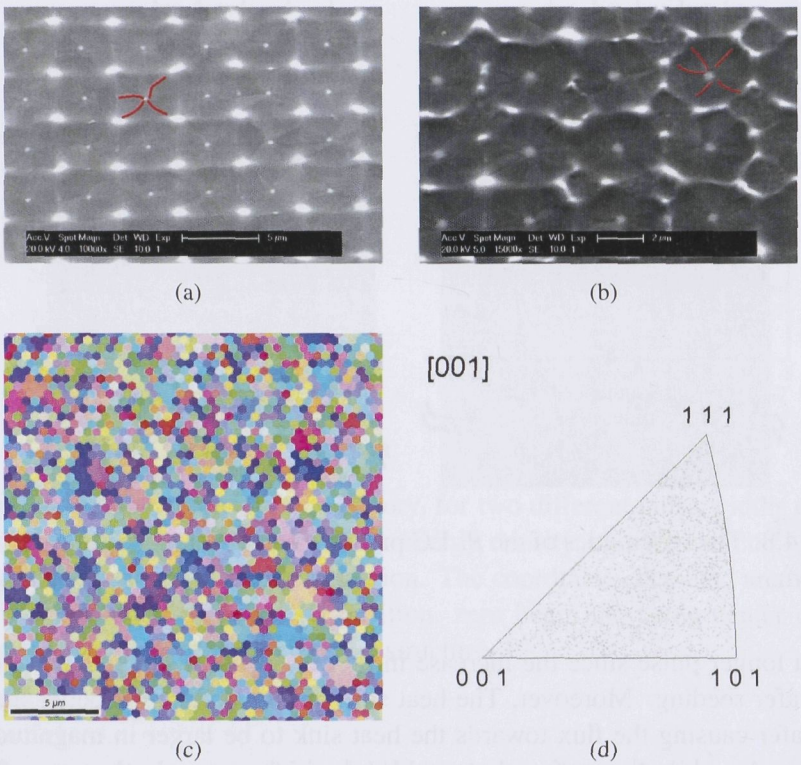


Figure 4.9: Unsuccessful epitaxial process for (a) SOI and (b) bulk wafer with <100> orientation by a laser fluency of 1400 mJ/cm^2 which appears to be insufficient. EBSD mapping (c) and pole figure (d) of an epitaxially grown sample with (100) bulk wafer seeding. No crystallographic orientation-control is achieved.

main crystallographic orientation present in the surface of the crystallized layer. In EBSD and pole figure, the existence of four secondary sub-grains is visible. A TEM cross-sectional image of an epitaxial process with a laser fluency of 2000 mJ/cm^2 is shown in Figure 4.12. In this figure, we can see a successful epitaxial process, but also the formation of the sub-grains due to twin formation originating from the oxide sidewall.

Grain size evaluation The underlying oxide thickness is important with respect to maintaining order to keep the heat. The substrate thickness is also important. Grains as large as 4x4 µm^2 can always be produced. However, the maximum grain size occurs in case of an undoped silicon and can reach as large

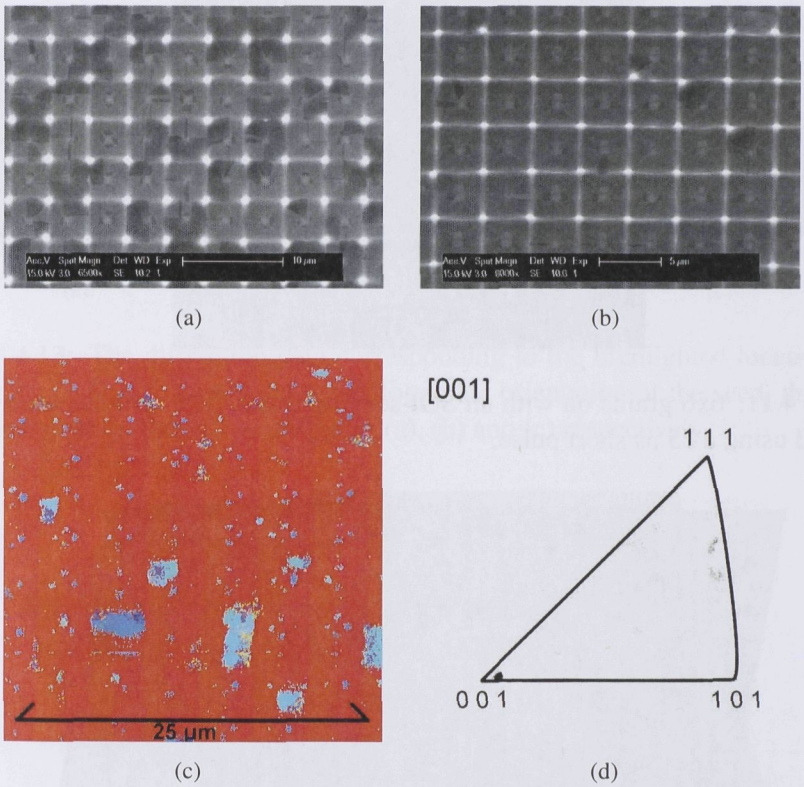


Figure 4.10: Successful epitaxial process for SOI (a) and bulk (b) wafer with (100) orientation by a laser fluency of 1900 mJ/cm^2 which appears to be sufficient. EBSD mapping (c) and pole figure (d) of an epitaxially grown sample with (100) bulk wafer seeding. <100> crystallographic orientation is achieved.

as 6x6 µm^2 is possible to achieve as it is shown by the SEM image in Figure 4.11.

4.3.3 Two shots process in order to remove subgrains

It is shown that the the PLEG process will lead to successful location and orientation-controlled grains. However, the subgrains that are created by the twin formation at the oxide sidewalls, are still unfavorable to the quality of the substrate, and thus to the mobility of the MOS transistors.

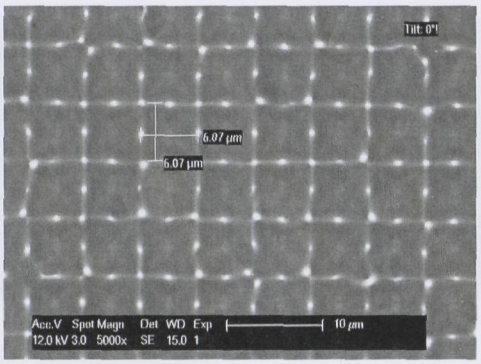


Figure 4.11: 6x6 grains on with an SOI seeding wafer. The samples were crystallized using a 25 ns short pulse.

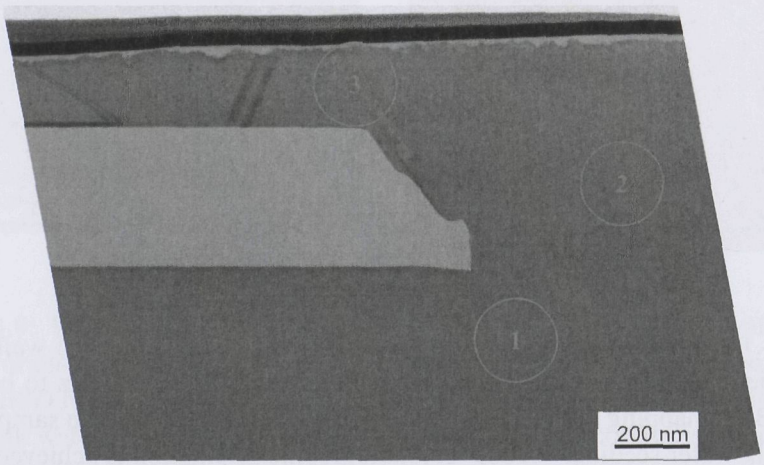
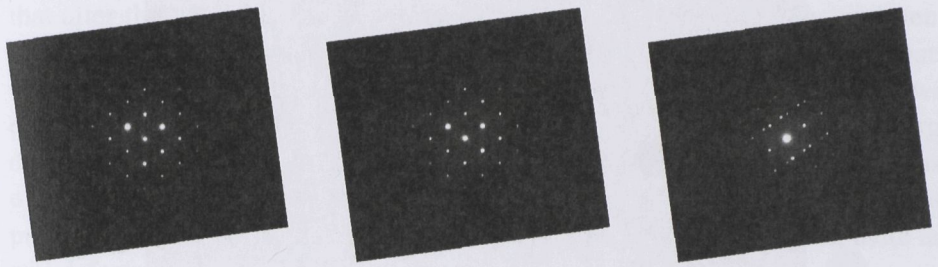


Figure 4.12: This TEM image shows a successful epitaxy of <100> orientation from a bulk wafer. Twin formation at the SiO_2 sidewall is visible.

Facet formation the SiO_2 sidewalls is the cause of the defects generated defects during the vertical growth phase of the epitaxial process. Depending on the materials at the sidewall, and the angle between the two materials, twins will be formed at the three-phase boundary of the two materials. These twins are shown in Figure 4.14. Twinning in the diamond cubic and zinc blended semiconductor lattices is represented by a 60 °rotation from the normal to the 111 twinning plane. To understand the crystallographic orientation of the twins, diffraction analysis was performed on the samples. The diffraction data for the TEM image is shown



(a) (b) (c)

Figure 4.13: The diffraction data corresponding to the highlighted locations in Figure 4.12. This indicates the crystallographic orientation of the seed, the hole and the defects at the SiO_2 sidewall in (a), (b) and (c) respectively.

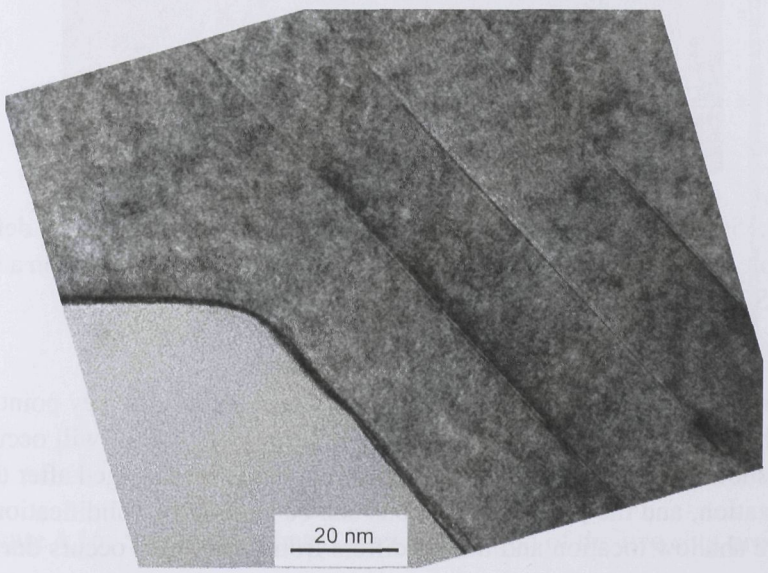


Figure 4.14: TEM image of a twin orientation created at the SiO_2 sidewall with pulse width of approximately 250 ns. For all experiments, the substrate temperature was elevated to 400 °C. These twin boundaries grow along the sidewall, extend outside the opening and eventually form the subgrain.

in Figure 4.13. The pattern of the silicon in the grain filter hole is the same as the seed, which proves a successful epitaxy of <100> orientation. The crystallographic orientation of the silicon at the SiO_2 sidewall is found to be <111>.

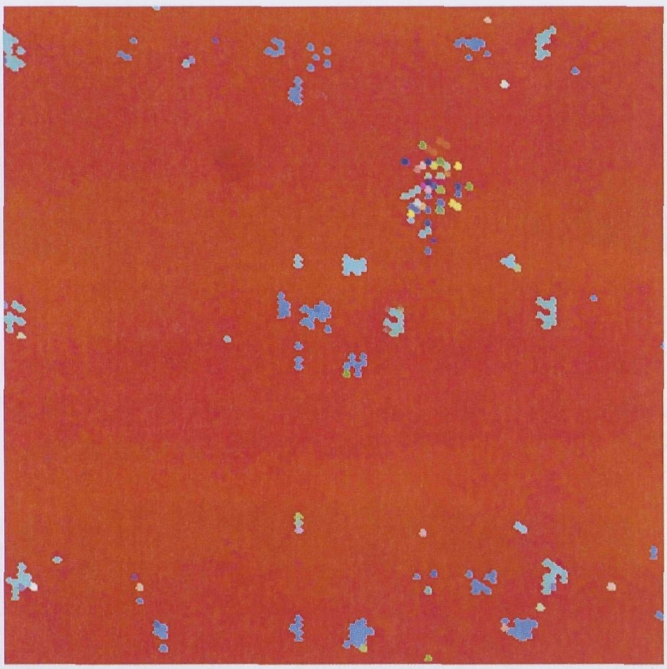


Figure 4.15: EBSD of the two shot process showing reduced number of defects in the sample. Here, an initial energy density of 1950 mJ/cm^2 was used on a sample with an SOI seed, followed by a second shot of 1750 mJ/cm^2.

To remove the subgrains, the two shot process is proposed. The key point to this approach is that after the first shot of laser, the epitaxial process will occur after the first shot of the laser. Since the material properties are changed after the first crystallization, and the process conditions can be varied, the solidification starts at a more shallow location and thus is differs from that which occurs during the first shot process.

Three types of energy profile were tested. In the first scheme, the second shot was given the same fluency as the first shot. In the other two type of experiments, the second shot had approximately 200 mJ/cm^2 less or more energy density respectively, than the previous shot. This test was performed on the samples with bulk silicon seeding. The first energy density for a successful epitaxy was 1950 mJ/cm^2 belonging to an extend pulse width of approximately 250 ns. For all experiments, the substrate temperature was elevated to 400 °C.

The EBSD results depicted in Figure 4.15 show a successful decrease in the number of unwanted orientations. The premise behind the success of this process is

that after the first shot, the a-Si is melted and solidified as c-Si. The melt temperature of c-Si is approximately 270 °C higher than that of a-Si, as mentioned in Table 3.1. This means that even the same energy density would melt a lower depth of c-Si compared to the previous a-Si case. In the case of increasing energy density, not much change in the defect density is visible. However, in the case of a lower or constant second shot, the defect density is decreased. This process promises to improvement to the quality of the epitaxial film. However, there are still defects remaining on the surface.

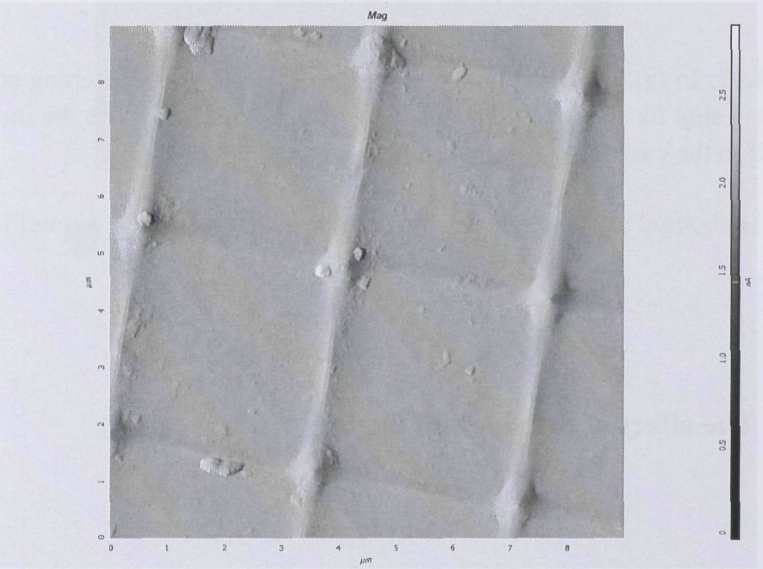
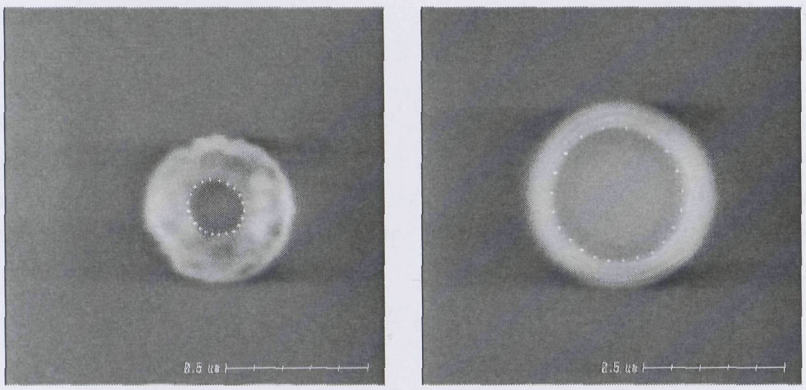


Figure 4.16: Surface roughness after completion of the two shot process.

Although the misorientations decrease, it can be observed that the surface of the grains is rough. The volume increase during solidification leads to lateral mass transport and thus the surface roughness increases. The second shot cannot completely remove these non-uniformities completely. The AFM measurements in Figure 4.16 show these non-uniformities. Translating the magnitude values into actual height data, the non-uniformity of the surface is found to be roughly 5 nm.



(a) (b)

Figure 4.17: In (a), the SEM image of a hole created by a dry etching combined with a wet step for the landing part is depicted. Figure (b) shows the more steep side wall in the case that no soft landing is used.

4.3.4 The effect of the sidewall angle

The thickness of the 500 nm underlying SiO_2 layer is optimized for a minimum reflectance during the lithography step, since the variations due to exposure energy fluctuations must be minimized. Figure 4.17 shows the SEM images of the holes after etching. Left has been etched by purely dry-etching, while the right sample has been etched partly dry with a wet landing step. The bright ring around the opening is a measure for the slope of the oxide sidewall, knowing that the diameter of the patterned holes were initially equal after the photo resist patterning. The angle of the side wall varies from 60°to 84°with straight forward geometric calculations.

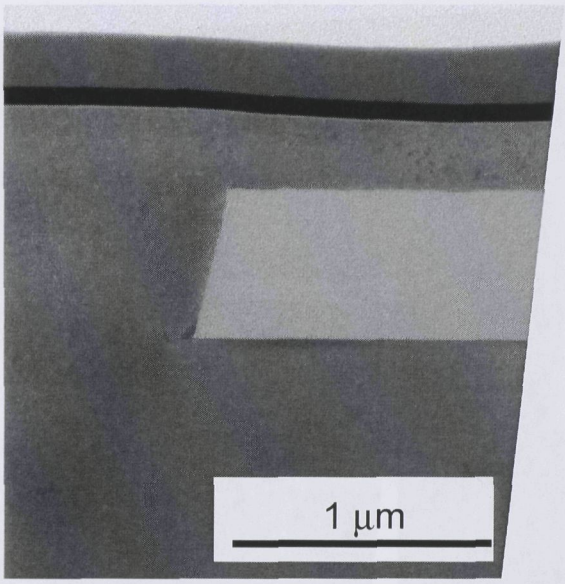


Figure 4.18: Successful epitaxial process, with single laser shot.

The main hypothesis formulates that the defects at the SiO_2 sidewalls are created because the angle of the sidewall is less than 45 °. One can test the validity of this hypothesis, by changing the angle of the sidewall. By incorporating a different etching process, a less isotropic profile can be achieved. This results in a more steeper hole. The TEM image in Figure 4.18 indicates that by using this method, no twin formation will occur. This process was done to the samples with bulk silicon seeding. The energy density required for a successful epitaxy was 1900 mJ/cm^2 using an extended pulse width of approximately 220 ns. The substrate temperature was elevated to 400 °C for all the experiments. The most critical part of this process is the etching of the hole, and landing on the seeding material.

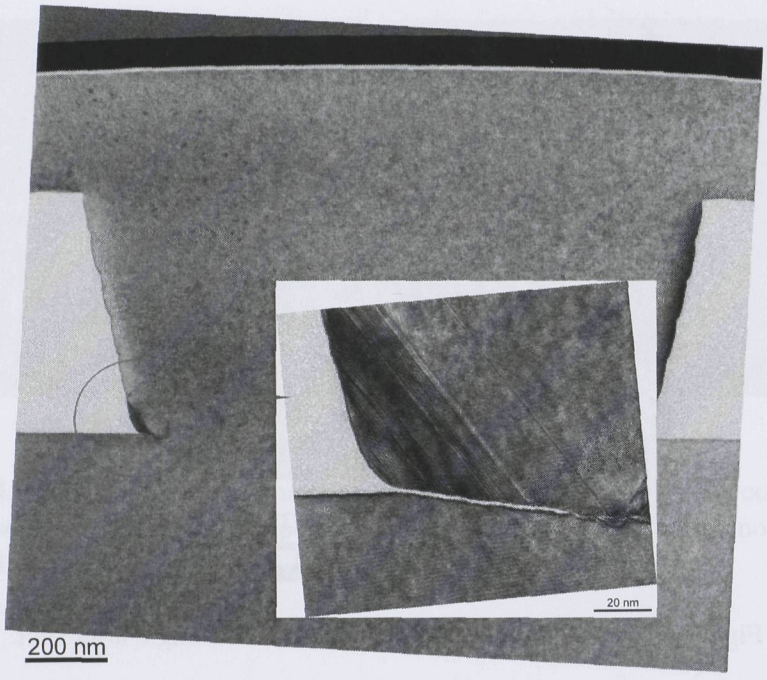


Figure 4.19: The angle of the growth of the misorientations is less than the angle of the wall. Thus filtering out the unwanted orientations are filtered.

The further away from the grain filter location, the higher probability of having a defect nucleation. This is due to the fact that the duration of solidification increases as the distance to the hole. The difference in the solidification duration is simulated to be approximately 100 ns. This is shown in Figure 4.20. The simulation is set for an SOI seeded epitaxial process, at an elevated temperature of 400 °C with a short pulse width of 25 ns. The energy density used in this simulation was 1000 mJ/cm^2.

4.4 Conclusion

Silicon grains with an area of 4 x 4 μm^2 were obtained on top of the holes. Arrays of SiO_2 openings of an 84 °sidewall with a 4 μm pitch were designed. Areas as large as 2.5 x 1.7 mm^2, which is the laser beam spot size, were crystallized. The orientations of these grains have been investigated using EBSD measurement. A preferred orientation of <100> was observed for samples of both bulk and SOI seeding layers. In the case of a 250 ns pulse, the energy density required for crys-

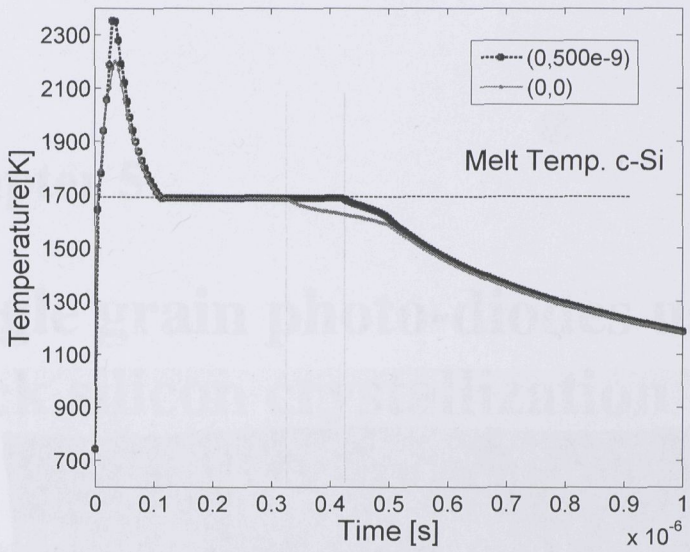


Figure 4.20: Difference in the solidification time between the surface of the silicon (0,0) and 500 nm away from the grain filter hole.

tallization was less than 1500 mJ/cm^2 for an SOI seeding wafer and 1600 mJ/cm^2 for bulk wafer seeding, which does not melt the c-Si seed layer. Consequently, the seed for nucleation consists of several orientations.
Longer pulse durations result in deeper melt depths and a higher surface ablation threshold. Seeding from an SOI wafer appears to require less laser energy density due to a better heat confinement of the structure. This is due to a thinner seeding silicon and the low thermal conductivity of the underlying buried oxide layer. However, by increasing the pulse duration in the case of the bulk wafer, there is a larger increase in the process window and more suitable to be used as a seeding layer in epitaxy. The quality of the crystallized layer appears to be better in the case of a bulk wafer which can be explained by the better quality silicon. The oxide sidewall angle can be varied by changing the etching type. Steeper holes lead to more filtering of the created twins at the SiO_2 sidewall. This study achieved the successful location- and orientation-controlled of large 4 x 4 µm^2 silicon grains, with an orientation of <100>, which can be used for the transistor layer of the building blocks of high quality 3D ICs, applicable in SRAMs and SoCs, for example.

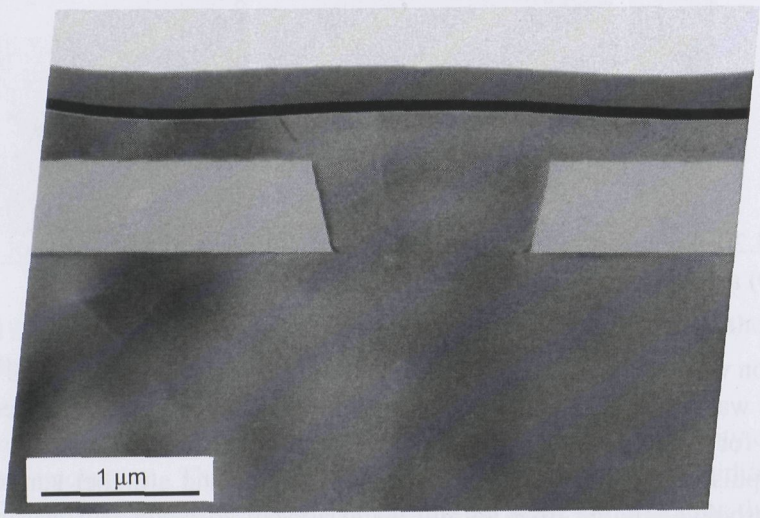


Figure 4.21: The defect formed outside the grain filter area due to random nucleation.

Chapter 5

Single grain photo-diodes using thick silicon crystallization

In the previous chapter, the PLEG process was introduced as an excellent method for realizing high quality electronics using a low temperature. It was shown that location and crystallographic orientation controlled silicon islands, as large as 6x6 μm^2 can be grown. A wide spectrum of sensors, actuators or energy scavenging devices could be integrated on top of the transistor layers. The aim of this chapter is first to fabricate photo-diodes made of the SG-Si. Photo-diodes using the SG-Si are promising, since they can be fabricated using low temperatures. Lack of grain boundaries allows them to have fast responses. Second, to make them more sensitive to light, a process to increase the thickness of the absorption region of the diodes (intrinsic region in P-I-N) will also be developed. Here, the reason for this motivation and its associated challenges will be discussed.

5.1 Introduction

The P-I-N photo-diode is a type of photo-diode which was invented in 1950 [74]. An schematic of such a diode is shown in Figure 5.1. There is an intrinsic region of silicon of semiconductor sandwiched between two heavily doped n^{++} and p^{++} regions. The charges (induced by external light) will be swept out of the intrinsic region and collected by an electric field, at the highly doped regions. The main advantage of this type of device compared with the PN junction type is its high sensitivity and low dark current. The relatively wider depletion region in the intrinsic area provides more carriers generated solely by light illumination.

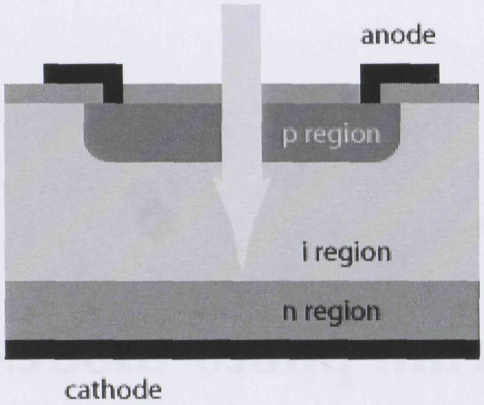


Figure 5.1: Schematic of a conventional c-Si vertical P-I-N photo-diode.

Currently, P-I-N photo-diodes are being used as receivers in optical fiber communications [75]. In addition, by incorporating III-V materials such as InGaAs, infrared detectors for low-light detection can be realized [76].
The possibility of integrating an image sensor layer on top of one or multiple layers of logic is very intriguing. This technology can be utilized in many products. An artificial retina [77], large-area processor-integrated X-ray image sensors [22] or advanced electronic paper [78] are examples of systems that can be realized using this technology.

5.1.1 C-Si P-I-N photo-diodes

Traditionally, c-Si is used to fabricate P-I-N photo-diodes. A silicon epitaxy process combined with a high-temperature (furnace) activation process, allows the definition of the p, n and i regions in these process flows. The temperatures used for the these steps is higher than the thermal budget affordable in a monolithic 3D IC system [79, 80]. This is the main issue with regard to the use of the c-Si P-I-N photo-diodes in 3D ICs. The high temperatures needed during the fabrication process are simply not affordable in monolithic 3D IC process flow. Consequently, since the focus of this thesis is the development of photo-diodes for monolithic integration purposes, c-Si is not a suitable candidate to be considered.
The thermal budget issues can be solved by using poly-Si which can be deposited at lower temperatures [81]. The fundamental difference between the poly-Si and the c-Si photo-diodes is that the mobility of carriers in poly-Si is roughly four

times lower than in c-Si, as reported in [82]. This makes the poly-Si diodes slower than the latter [83].

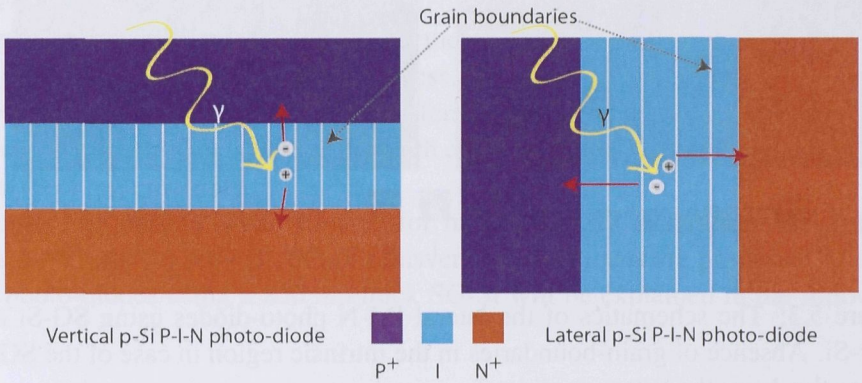


Figure 5.2: Schematics of vertical(left) and lateral(right) poly-Si photo-diodes.

5.1.2 Low-temperature P-I-N photo-diodes

There are two methods of realizing P-I-N photo-diodes: vertical and lateral. Both schematics are drawn in Figure 5.2. The direction of electron and hole absorption by both the N^{++} and the P^{++} regions are varies depending on the structure. In the vertical P-I-N, the generated electron-hole pair is separated orthogonally with respect to the top and bottom of the intrinsic layer. In the case of the lateral structure, this direction is parallel to the light absorbing surface. It is apparent that the generated electron-hole pair experience more recombination sites in the lateral structure due to the larger number of grain boundaries. The generated pairs in case of the vertical structure (assuming a high-quality poly-Si with columnar grains) are more likely to reach both the anode and the cathode, leading to higher output current. The vertical type is thus advantageous in the case of poly-Si photo-diodes. Theoretically, it is possible to fabricate vertical P-I-N photo-diode using poly-Si. In order to make a vertical diode using poly-Si, the following steps are required. First, the n+ region at the bottom needs to be deposited, implanted, laser activated and passivated. After these steps, a deposition of the intrinsic region and the P^{++} region should take place. The implantation and activation of this region will then occur. Thus, it is apparent that the process flow to realize such a device is long and complicated. So far, no practical implementation of such or comparable structure, fabricated in low-temperatures ($\sim$600°) is reported.

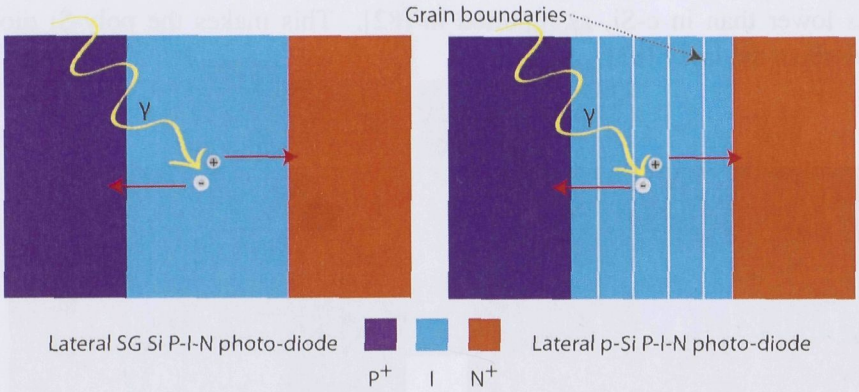


Figure 5.3: The schematics of the lateral P-I-N photo-diodes using SG-Si and poly-Si. Absence of grain-boundaries in the intrinsic region in case of the SG-Si makes this layer the better candidate.

Realization of the vertical P-I-N photo-diodes using SG-Si layer is also challenging. Lateral diodes have thinner intrinsic regions as they are not fabricated on the bulk silicon of the wafer. This reduces their absorption spectrum. However, There are several advantages that make the utilization of these photo-diodes extremely interesting. First, they are suitable for light detection within the blue and UV wavelength range. In this range, the optical absorption length of silicon is a few nanometers. However, the lateral P-I-N photo-diodes are not limited by the absorption length of the incident light since the carrier path and incident light direction are different. This light detection in this range is possible, since unlike the vertical structure, the depletion region of lateral P-I-N photo-diodes is at the surface. Second, as the three regions are exposed on the surface, they can be annealed using low temperatures posterior to implantation steps. On this basis, it is clear that lateral structure is the best option for monolithic 3D integration.
Figure 5.3 shows the schematics of the lateral sturcture using both the SG-Si and poly-Si. Theoretically, there are no grain boundaries in a SG-Si film. The boundaries within each grain are mostly CSL boundaries [84]. Not all CSL boundaries are detrimental to electrical current. The absence of grain-boundaries in the intrinsic region in case of the SG-Si makes this layer the better candidate

5.2 SG P-I-N photo-diodes

There are several advantages in using SG-Si for lateral P-I-N photo-diodes. First, the photo-diode can easily be integrated with thin-film transistors (TFTs) since the SG-Si which forms the channel of the TFTs and the body of the P-I-N diodes is prepared by the μ-Czochralski process. Second, the carrier mobility in the SG-Si layer is in the order of c-Si. This offers the potential of having a fast response. Therefore, SG-Si is the candidate which can both be made using low temperatures and have high mobility.
In order to make a diode suitable for monolithic 3D integration with a faster response than the poly-Si, SG-Si transverse photo-diodes are proposed. The P-I-N photo-diodes using a 250 nm thick SG-Si will be explained in the following.

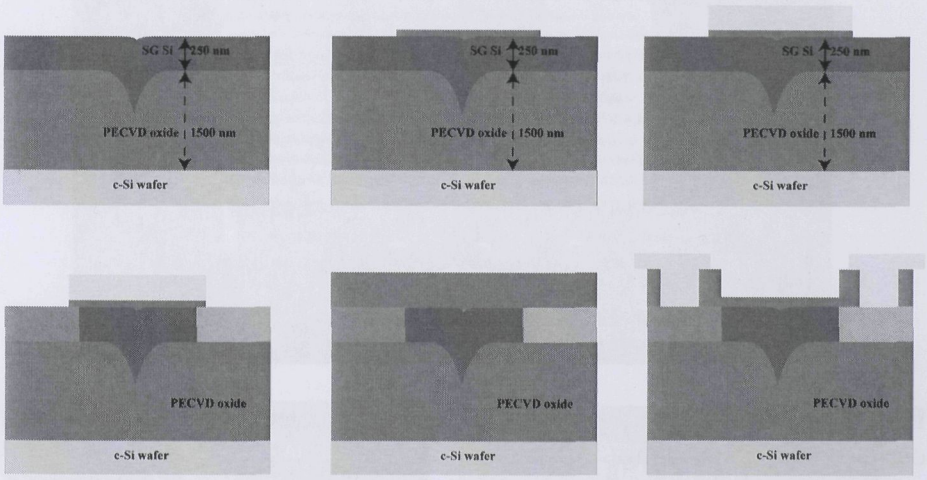


Figure 5.4: Fabrication process of SG P-I-N photo-diodes

5.2.1 Fabrication of the SG P-I-N photo-diode

One can fabricate the SG TFTs and the photo-diodes simultaneously. However, for the sake of simplicity, here, the flowchart specific to the photo-diodes is explained first. Afterwards, the integration of this process with an SG TFT process is discussed. The process is started by creating a high quality substrate for the photo-diodes. This is done using the μ-Czochralski process as explained in Sec-

tion 2.1. After the crystallization of the silicon and the formation of single grains, an island mask is applied to define the silicon islands using a dry etching process. The 250 nm thick crystallized silicon is then removed from unprotected areas. After marangoni drying [85], a 30 nm thick PECVD oxide is deposited to serve as a buffer layer between the silicon island and the protective metal. A 675-nm thick aluminum is sputtered at 50 °C to serve as the protective metal. Aluminum is then patterned and removed by dry etching to reach to the regions which are to be highly doped. The patterned protection metal is shown in Figure 5.5. Two

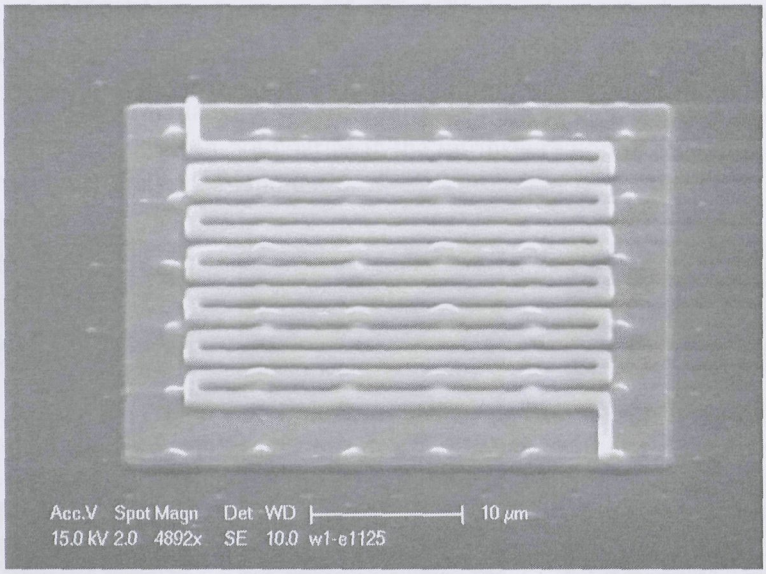


Figure 5.5: SEM image of the aluminum lines, protecting the intrinsic region during the laser annealing

regions of n^{++} and p^{++} are implanted using Phosphorus and Boron respectively. A dose of 1e16 cm^{-1} is used to achieve a doping in the order of $\sim$20 cm^{-3} . Following this, the dopants are activated using the excimer laser at room temperature with a sweep of 250 to 400 mJ/cm^2 laser fluencies. The annealing energy is crucial and has significant effect on the efficiency of photo-diodes. Aluminum is then removed from the top of the photo-diodes by applying a mask and dry etching. Then an 800 nm thick PECVD oxide is deposited on wafers and contact holes were opened to access the anodes (p^{++}) and cathodes (n^{++}) of the photo-diodes. Using the same mask that we used to remove the protection metal, oxide is then etched back to become 300 nm thick on top of the intrinsic regions with

the aim of maximum quantum efficiency. Finally 1.5 µm aluminum is sputtered and patterned to create the metal pads and connect the diodes to them.
Figure 5.4 shows a schematic of the fabrication process for the P-I-N photo-diodes.

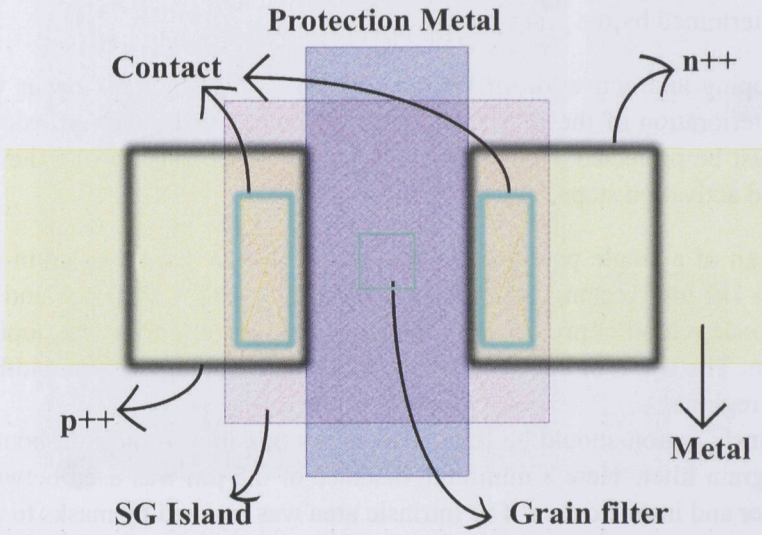
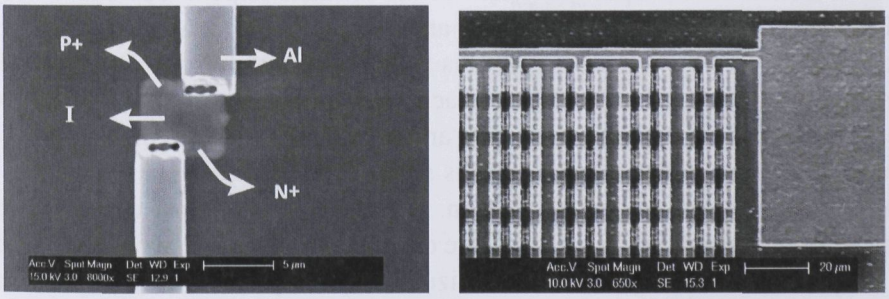


Figure 5.6: Design of a SG photo-diode



(a) (b)

Figure 5.7: (a) shows an SEM image of a lateral photo-diode using one single-grain and (b), shows an SEM image of an array of SG P-I-N photo-diodes

5.2.2 Design and characterization of a lateral P-I-N photo-diode

There are two main design requirements to be considered.

1. Grain filters are 1x1 μm^2 squares, set at 6 μm distance. To avoid the grain boundaries (defects) in the intrinsic region, it (the intrinsic region) needs to fit within a square. Moreover, the maximum size of the photo-diode is also determined by the grain size.

2. Doping and activation of the n^{++} and p^{++} regions must occur without deterioration of the intrinsic region. In other words, the intrinsic region must be protected against the diffusion of the dopants during the doping and activation steps.

The design of a single photo-diode is shown in Figure 5.6. The grain filter is the green 1x1 μm^2 rectangular in the middle of the 6x6 μm silicon island (pink). The intrinsic region is protected by the protective metal during the doping and activation. The width of the metal is crucial for determining the real width of the intrinsic region.
The intrinsic region should be located as far as possible from grain boundaries and the grain filter. Here a minimum distance of 0.5 μm was used between the grain filter and intrinsic area. The intrinsic area was covered by masks to prevent implantation during anode and cathode doping and laser annealing for activation of the dopants. The green rectangles are contact holes providing access to the anode and cathode regions. The anode and cathode are depicted by two large black rectangles. In several designs, the width of the intrinsic area is altered in order to determine the optimum width of the intrinsic region. Too small width will cause a short circuit between the p and n regions. Too long intrinsic region width will cause high resistance of this region, and ensures that many of the generated electron-hole pairs do not reach the anode and cathode. The yellow area is metal, which connects the anode and cathode to the metal pads.
The length of the intrinsic region of this specific cell is 2 μm and its width is 6 μm resulting 12 μm^2 of intrinsic region. To increase the output current of the photo-diodes and solar cells, the cells are designed in finger configurations. Such an array is shown in Figure 5.8. The size of this array is 300x300 μm^2. Since there are 50 cells in each row and each column, a total intrinsic area of 30 mm^2 is obtained. The connection of the finger structures to the metal pads is shown in Figure 5.9. This translates into a fill-factor of 33 percent. Other designs with a different length of the intrinsic area will result in different effective area of the photo-diodes and thus a different fill-factor.

An array of fabricated SG P-I-N photo-diodes are shown in the SEM image of Figure 5.7(b).

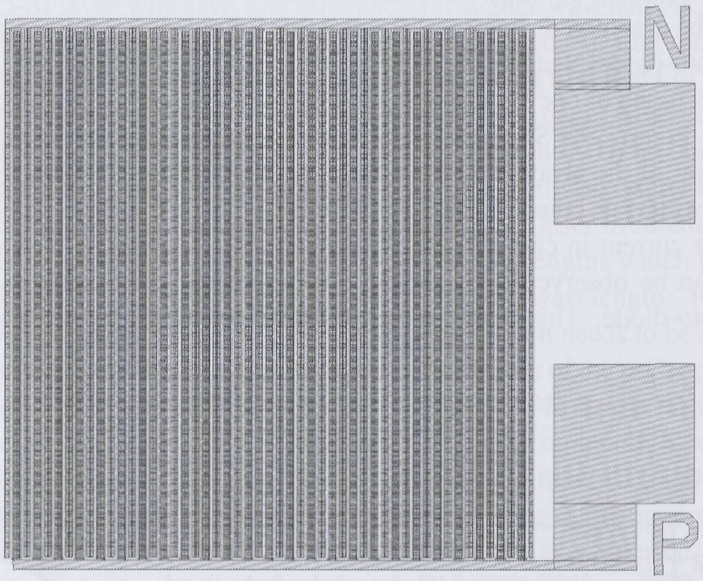
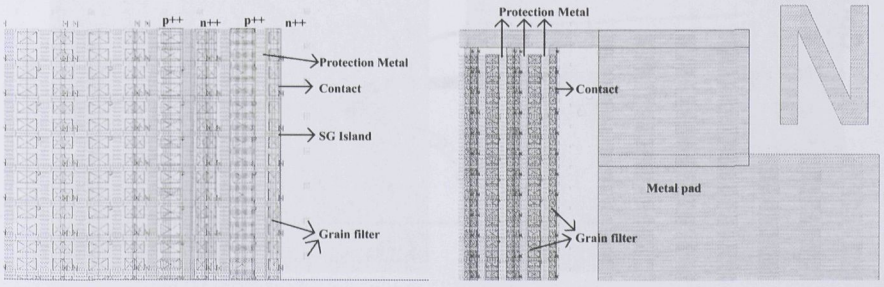


Figure 5.8: Arrays of photo-diode covering a 300 x 300 μm^2 area



(a) (b)

Figure 5.9: Figure (a) shows the array configuration of photo-diodes; the metallization scheme is given in Figure (b).

5.2.3 I-V characteristics of a single grain photo-diode

The design and the fabrication of the P-I-N photo-diodes on a SG-Si layer have been explained in the pervious sections. Here the I-V characteristic of the photo-diodes will be disscussed. Figure 5.10 shows the output curves related to the two types of photo-diodes that have been fabricated. The small cell is 6 x 6 μm^2 large photo-diode, based of one single-grain, and the other is an array of 300 x 300 μm^2 large photo-diodes. The SEM images of both devices is given in Figure 5.7. The output current of the array structure is 3 orders higher that that of a single cell. Both devices have a comparable sensitivity to light, as the difference between their reverse current in case of illuminated and dark conditions, is roughly one order. It can be observed that there is a negative built-in bias in case of the smaller photo-diode. This bump in the bias is due to the trapped charges in the oxide layer.

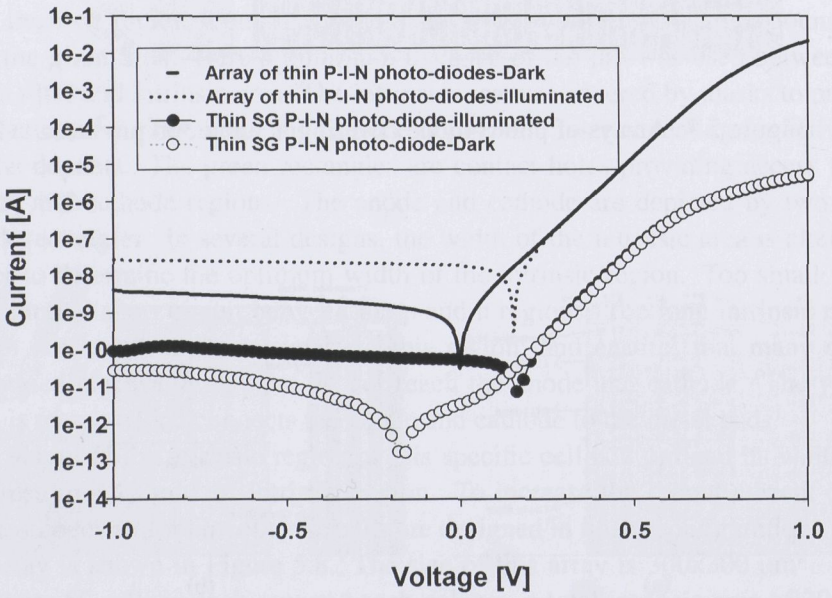
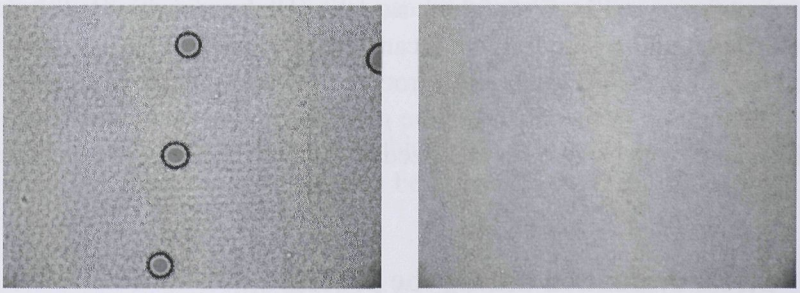


Figure 5.10: I-V characteristics of a lateral P-I-N photo-diode using one single grain

5.3 Thick silicon crystallization process

A thin SG-Si layer will have low efficiency for higher wavelengths. In order to improve the absorption range, thicker silicon is needed. In this section, the μ-Czochralski process is used to crystallize thick layers of silicon of 1 μm. The thickness of the recrystallized Si is determined by melt depth which is dependent on the pulse duration of the laser. For a pulse duration of 20 ns, the maximum melt depth of Si is about 400 nm [86]. This section will also study the effect of light pulse duration on the melt depth during excimer-laser irradiation to the Si. The thickness of the silicon affects the range of wavelengths which it is capable of absorbing. 250 nm lacks sensitivity to an infrared wavelength. To widen the range of absorbable frequencies, the thickness of silicon needs to be increased.
The process described below entails modifications from of the μ-Czochralski process, which was explained in Chapter 2.1, for thicker a-Si layers. Cavities with 1 μm diameter were made in a 700 nm thick SiO_2 layer on a bulk-Si wafer. After filling the cavities with 500 nm,750 nm and 1000 nm thick LPCVD a-Si at 545 °C, excimer laser annealing was performed (λ=308 nm). To increase the melt depth, pulse durations as long as 25 ns,170 ns and 250 ns were used. The energy densities needed for crystallizing were varied between 2000 to 4000 mJ/cm^2, depending on the thickness of the a-Si.



(a) (b)

Figure 5.11: A microscope image of two samples with 1μm thick silicon, on top of two different PECVD oxides, using (a) TEOS, and (b) silane.

5.3.1 The effect of the dielectric material

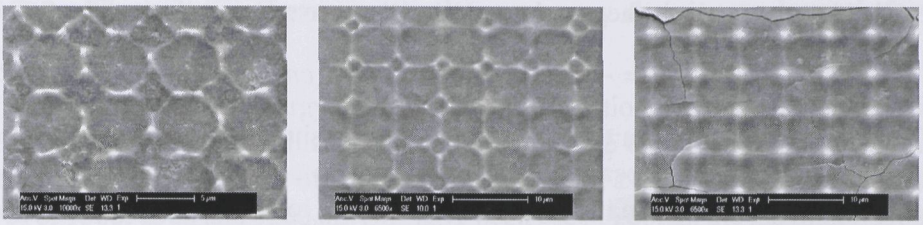
To increase the melt-depth, the laser fluencies used for thick silicon crystallization were increased ($\sim$ 3500 mJ/cm^2). This induced a large amount of thermal stress on the underlying oxide. In order to determine whether the underlying oxides might limit the process window, a comparison of the two possible oxides for this process was made. Figure 5.11 shows two typical microscope pictures of two types of PECVD oxides, one with a TEOS and O_2 precursor and the other with a SiH_4 and N_2O precursor. it can observed that ablations using the TEOS occur at 250 mJ/cm^2 lower fluencies in comparison with that of the SiH_4. The thickness of the a-Si is 1 µm and the process is performed with an elevated substrate temperature of 450 °C. The energy density which is used in this figure is approximately 2100 mJ/cm^2 delivered by a 250 ns long pulse.

5.3.2 Exploring the maximum silicon thickness

The thickness of the a-Si in the µ-Czochralski process was increased to 500nm , 750nm , 1000 and 1300 nm. The crystallization results for the first three samples are shown in Figure 5.12. The samples were crystallized at room temperature by a 170 ns pulse, with energy densities of 2000, 2700 and 3200 mJ/cm^2 were used to obtain the results. Figure 5.13 shows 2 µm holes, before and after crystallization in 5.13(a) and 5.13(b) respectively. The mass transfer of molten silicon during the crystallization process causes the grain filter holes to be filled in Figure 5.13(b). An energy density of 3000 mJ/cm^2 with an elevated substrate temperature of 450 °C was used for crystallization of these samples. Higher densities led to ablation. Since no single grains were formed, it can be concluded that the process window was too short for the µ-Czochralski process. In other words, ablation occured prior to the melting of the silicon in the grain filter. The maximum thickness of the silicon layer which can be crystallized with an excimer laser lies around 1300 nm.

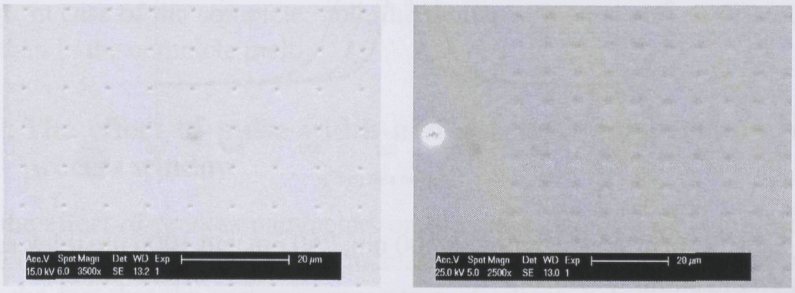
5.3.3 Stress evaluation during the process

Excimer laser crystallization of silicon creates a tensile stress in the crystallized films. This is mainly caused by a difference in the thermal expansion coefficients of the silicon and the underlying material (SiO_2).
Raman spectroscopy was used to study the stress behavior for different film thicknesses. The Raman spectrum of Figure 5.14 shows that all of the Si films are



(a) (b) (c)

Figure 5.12: The effect of the silicon thickness on crack formation is shown in here. The samples were crystallized at room temperature by an 170 ns pulse. The thickness of the samples are 500, 750 and 1000 nm for (a), (b) and (c) respectively. Energy densities of 2000, 2700 and 3200 mJ/cm^2 were used to obtain the maximum grain size.



(a) (b)

Figure 5.13: The maximum a-Si that can be crystallized lies between 1 and 1.3 µm.

fully crystallized throughout the film thickness as there is no broad peak of a-Si present. The thermal stress σ_{th} can be estimated from the following expression [87]:

$$\sigma_{th} = (\alpha_f - \alpha_s)\Delta T \frac{E_f}{1 - y_p} \tag{5.1}$$

where α_f and α_s are the average thermal expansion coefficients of the film and the substrate respectively. T is the difference between the crystallization temperature and the initial temperature of the film, E_f is the elastic (Youngs) modulus of the film and y_p is the Poissons ratio. The thermal stress built into the film is

tensile if $\alpha_f > \alpha_s$, as is the case here. Using the conversion rule given by [87]:

$$\sigma_{th} = -0.27(GPa/cm^{-1})\Delta\omega(cm^{-1}) \tag{5.2}$$

This shows a change from tensile stress to compressive stress on increasing the thickness of a-Si. As the peak shifts towards a positive direction, the stress at the center of a 6 x 6 μm^2 grain increases from -270 MPa to 1.08 GPa for 1000 nm to 500 nm thick a-Si samples, respectively.

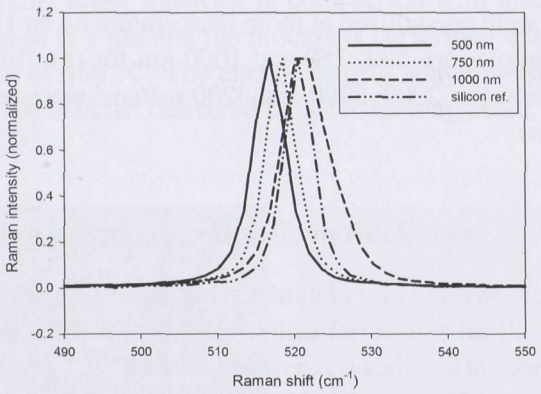
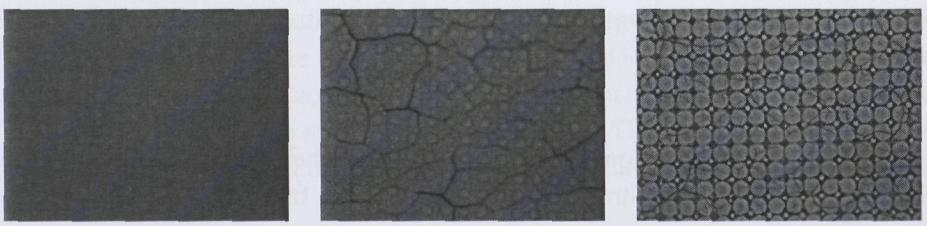


Figure 5.14: Raman spectroscopy of 500 nm, 750 nm and 1000 nm thick samples after crystallization.



(a) (b) (c)

Figure 5.15: The effect of the laser energy density on crack formation is shown in here. The samples were crystallized at a 450 °C substrate temperature by an 250 ns long pulse. The thickness of the samples is 1000 nm as reference. Energy densities of (a) 1500, (b) 2500 and (c) 3200 mJ/cm^2 have been used to obtain the maximum grain size.

5.3.4 The relation between the laser energy density and crack formation

The effect of the laser energy density on crack formation is shown in Figure 5.15. The samples were crystallized at a 450 °C substrate temperature by an 250 ns long pulse. The thickness of the samples is 1000 nm as reference. Energy densities of 1500, 2500 and 3200 mJ/cm^2 have been used to obtain the maximum grain size. Three regimes of grain-formation is observed. In Figure 5.15(a), the energy density of 1500 mJ/cm^2 is not sufficient to form large grains. By increasing the energy density to 2500 mJ/cm^2 as in Figure 5.15(b), SG-Si is formed. However, the amount of cracks in the layer is extremely high. By increasing the energy density to 3200 mJ/cm^2, the number of cracks is severely decreased. The difference in the amount of cracks are related to the different melt regimes regarding this process. In the case of the energy density of 2500 mJ/cm^2, there is near-complete melt will occur, as opposed to the complete melt in the case of the highest energy density. In case of the complete melt, the molten silicon is able to discard more stress than in the complete melt.

5.3.5 The effect of pulse width and substrate temperature on the process window

Here, the effect of process parameters on the grain size of a of 1 μm thick a-Si sample is discussed. The grain size increases with pulse duration. This is mainly due to the fact that the surface temperature of silicon is lower when shot by a longer pulse. The same amount of heat is transferred to the system, but 10 times slower. The process window will then increase as the ablation occurs at a higher energy density.
When using a heated substrate, it is essential to use lower energy densities. This also affects the ablation threshold and increases the process window. Logically, the biggest grain sizes are reached when combining an elevated substrate temperature with a long pulse width.

Table 5.1: The effect of process parameters on grain size of 1 μm thick a-Si sample

Pulse Width [ns]	25	170	250
Substrate Temperature [°C]	450	RT	450
Maximum grain size [μm^2]	6 x 6	6 x 6	8x8
Energy densities [mJ/cm^2]	2500	4000	3400

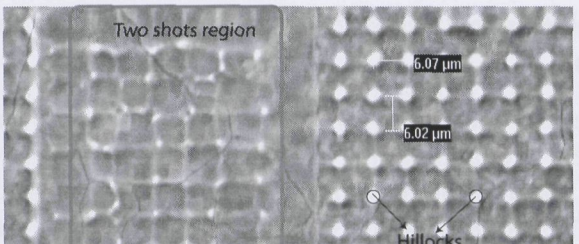


Figure 5.16: Two shot process in order to remove the hillocks. In the right part of the figure, the grains are visible which were only shot one time. Inside the red rectangle in the left part, the grains are visible that were shot twice. From the contrast of the SEM image, it can be concluded that the height of the hillocks are reduced.

5.3.6 Non-uniformity reduction by two shot process

To ensure the single grain areas have no grain boundaries, the distance between the two grain filters must be smaller than the maximum achievable grain size. This leads to the location control of the grain boundaries. During the solidification of the molten film, the melt front of the adjacent grains collides at the grain boundaries. This adds surface roughness to the crystallized films. Hillocks are created specially at the intersection point of four grains. The height of the hillock is dependent on the thickness of the silicon. In the case of the thick silicon, the hillock height exceeds 1 µm. Thus, it has unfavorable effects on the absorption of the laser beam. In an experiment to remove the hillocks, a second shot was introduced, with an energy density of 2000 mJ/cm^2. The reason behind this was to melt the hillock without melting the surface and deteriorating the crystallized single grains. It is shown in the left part of the figure that the hillocks were successfully removed. Figure 5.16 shows a comparison between a one and two shot process. The energy density required to obtain large single grains, was 3300 mJ/cm^2 using a 250 ns pulse and an elevated chuck temperature of 450 °C.

5.4 I-V characteristics of a single grain photo-diode on a thick layer of silicon

A comparison of the I-V characteristics of two types of lateral P-I-N photo-diodes based on one single-grain is shown in Figure 5.17. The sensitivity of the photo-diode with 1μm thick SG-Si is up to an order larger than the 250 nm thick SG-Si. The hypothesis of gaining sensitivity with thicker silicon is proved. Both structures suffer from a trapped charges in the SiO_2, as the negative shift in the bias voltage is present. The comparison between the array of these two types of photo-diodes is lacking. This is due to the crack-formation in the thick silicon. The larger arrays suffer from yield issues and can not produce a responding I-V curve.

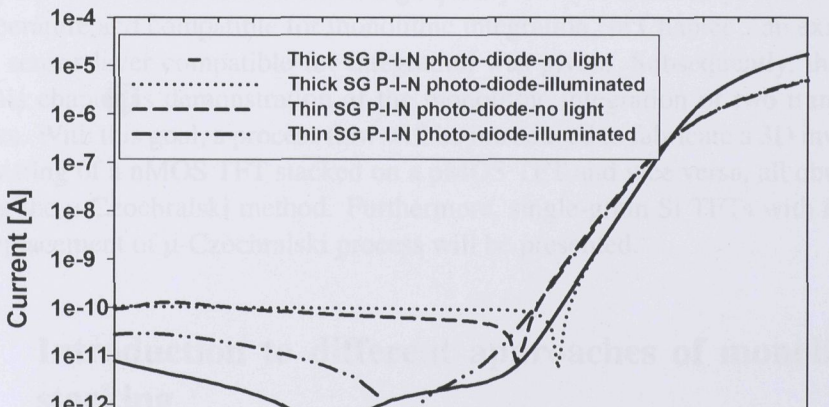


Figure 5.17: Comparison of single grain photo-diodes using the 250 nm thick and the 1 μm thick layer SG-Si. The thicker layer of SG-Si increases the sensitivity of the photo-diode.

5.5 Conclusions

A novel method of realizing high speed photo-diodes suitable for 3D integration is proposed. These photo-diodes are fabricated using low-temperatures. The μ-Czochralski process is used to enable a low-defect substrate for the intrinsic region of the P-I-N photo-diodes. In order to increase the sensitivity of these photo-diodes, maximum Si thickness that can be crystallized using the μ-Czochralski process was investigated. Silicon layers with a maximum thickness of 1 μm were crystallized. Elongation of pulse duration and substrate heating are effective in increasing the maximum Si thickness. However, cracks in crystallized films were reduced by substrate heating. Location-controlled grains with 1 μm thick Si was obtained successfully. Single grain P-I-N photo-diode was fabricated inside of these thick SG-Si. Dark current of 100 μm x 100 μm size arrays are on the order of 0.1 nA for SG-Si photo-diodes with 1 μm, 1.5 μm and 2 μm intrinsic region length.

Chapter 6

Demonstration of a monolithic 3D IC

Chapter 4 showed the realization of high quality Si layer formed by PLEG at low temperature and compatible for monolithic integration. In Chapter 5 an example of a sensor layer compatible for integration was given. Subsequently, the aim of this chapter is demonstration of the monolithic integration of two transistor layers. With this goal, a process flow will be introduced to fabricate a 3D inverter, consisting of a nMOS TFT stacked on a pMOS TFT and vice versa, all obtained using the μ-Czochralski method. Furthermore, single-grain Si TFTs with PLEG as replacement of μ-Czochralski process will be presented.

6.1 Introduction to different approaches of monolithic stacking

Monolithic integration was described in Section 1.2. Several approaches exist within this type of integration. In one approach, the active blocks of each layer are fabricated and if necessary, interconnected using a metal layer. After a passivation step, the next layer of active devices can be created on top of this layer. The first approach may be viewed as the ultimate form of the monolithic integration: allowing materials such as aluminum to be used freely through the stack, adds much freedom to the design. However, it demands a decrease of the thermal budget of the process, preventing the deterioration of these metals.
Another approach is to complete the processing of each active layer until the point of contact formation (front-end). Following the passivation, again perform-

ing the front-end processing of the next active layer. After completion of the last active layer, a single metallization (back-end) step for all underlying layers will be done. The main advantage of this approach is that no metal layers need to be used in the underlying layers. This increases the thermal budget of the process. However, in here, the number of connections to the underlying layers is limited due to the aspect ratio of the vias and the transistor density of the underlying active layers.
In this work, the second approach is pursued. As explained in Section 2.3, unless the LPCVD deposition of the a-Si is replaced by an alternative low-temperature step, using metal layers will be impossible. Next section will describe the details of the fabrication process according to this approach.

6.2 Monolithic 3D IC fabrication process flow

6.2.1 Front-end processing

The flowchart required for fabrication of a 3D IC using the μ-Czochralski method is shown in Figure 6.1. The process flow starts by the μ-Czochralski process, de-

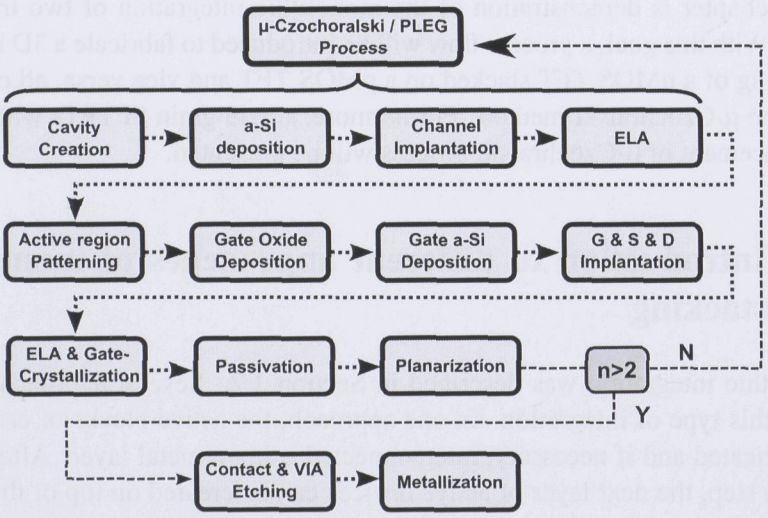


Figure 6.1: Process flow for stacking two layers of SG TFTs.

scribed in Section 2.1. After completion the ELA, the substrate consists of an arrays of SG-Si. The process flow after the μ-Czochralski process up to the back-end processing is depicted in Figure 6.2.

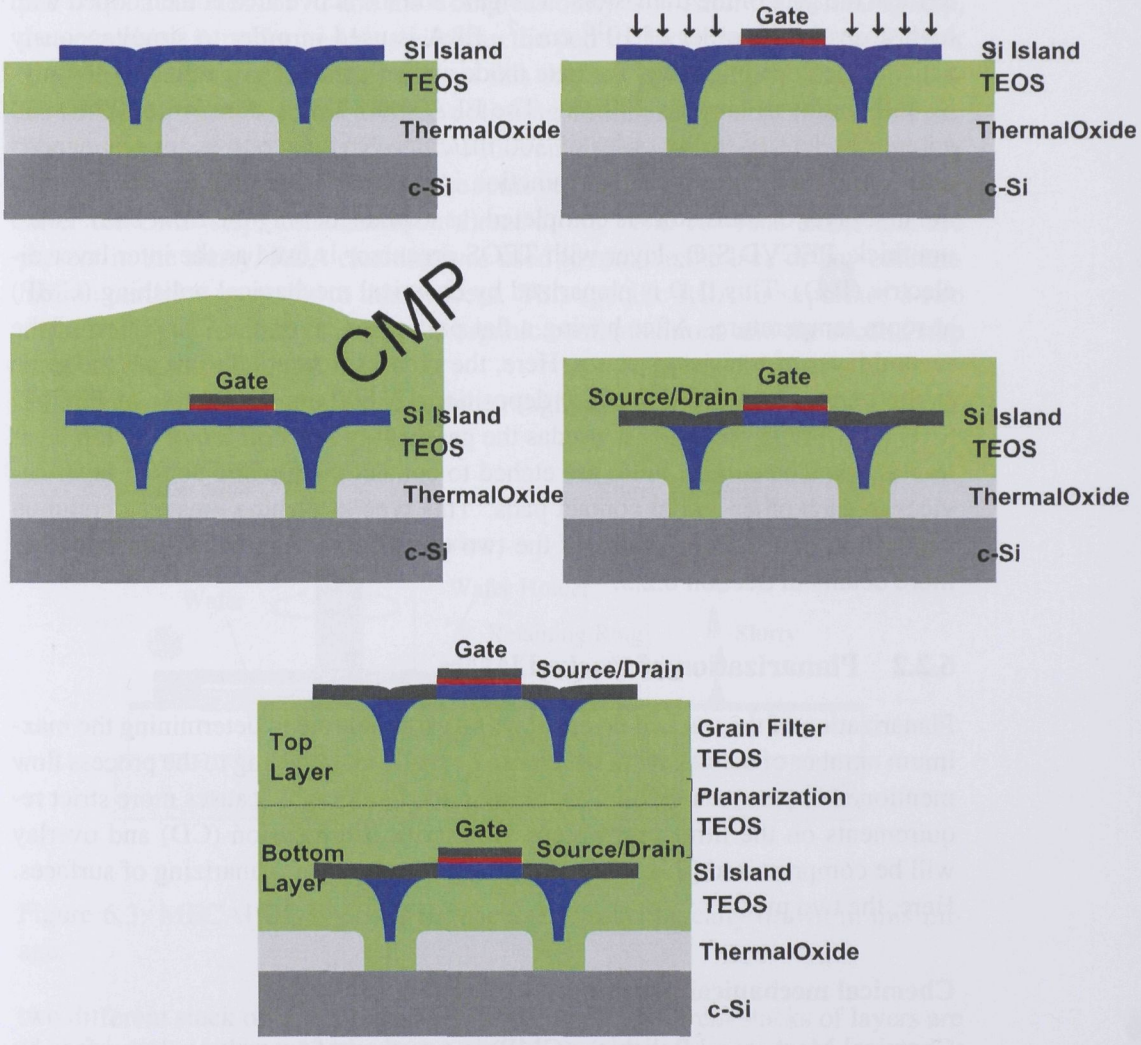


Figure 6.2: The process flow of the 3D IC until the contact formation and metallization.

The SG-Si layer will be etched to leave the body of the transistors. Thus no isolation is needed from one active device to the other, as there is no conducting material in between. The active region of transistors is then patterned by dry etching. A 30 nm thick SiO_2 is then deposited at 250 °C using inductively coupled pressure-enhanced CVD (ICPCVD) which serves as the gate oxide. Next follows

the LPCVD of 250 nm thick a-Si which is patterned together with the gate oxide to form the gate of the transistors. The gate and the active area is then doped with high doses in the order of 10^{16} cm^{-2}. ELA is used in order to simultaneously activate the dopants, anneal the gate oxide and crystallize the gate a-Si into poly-Si with grains as large as 100 nm. The ELA shots have a duration of 25 ns and an energy density in the order of 300 mJ/cm^2. No substrate heating is needed during this step since a shallow junction is the goal of this ELA step. By this, the first layer of transistors is completed (as explained, only the front end). A 1.6 µm thick, PECVD SiO_2 layer with TEOS precursor is used as the inter layer dielectric (ILD). This ILD is planarized by chemical mechanical polishing (CMP) at room temperature. After having a flat passivated layer, the fabrication of the second layer of transistors starts. Here, the process flow conditions are the same as the bottom layer until the ILD deposition. A 800 nm thick layer of PECVD SiO_2 with TEOS precursor is usedas the passivating layer on top of the top layer transistors. The contact holes are etched to contact the top and bottom layer devices to each other and to contact pads. This type of etching creates a common connection between the drains of the two transistors. This will be described in more details in Section 6.2.3.

6.2.2 Planarization of stacked layers

Planarization of the stacked layers plays an essential role in determining the maximum number of active layers which can be realized according to the process flow mentioned in pervious section. Increase in the topography, causes more strict requirements on the lithography step. Both critical dimension (CD) and overlay will be compromised [88]. There are several methods of planarizing of surfaces. Here, the two most

Chemical mechanical polishing

Chemical Mechanical Polishing (CMP) is a method of smoothing the surface by subsequent steps of corrosion, etching and polishing [89]
The CMP system used in here is a *MECAPOL E460*. This CMP system, shown in Figure 6.3, can be used to remove stepheight of several materials such as aluminum, silicon and oxide. There are 2 major steps of planarization and smoothing. The major parameters like slurry flow rate, time of each step, backpressure and down-force can be changed to optimize the process to achieve best planarization and surface roughness. The slurry that is used is Rodel ILD1300 which has a PH of 10.7 and is optimized for polishing SiO_2. It has a removing rate of 339

nm/min and uniformity of around 6% (both parameter dependent). The polishing pad is has a hardness of 72 and the Compressibility is 7. After the polishing step, the smoothing is performed by switching the pad to a soft pad called the Politex Supreme. The wafer is rubbed against this surface with addition of slurry. After this step, water is added and the polishing continues for around one minute. The main goal of this step is to remove the remaining slurry particles before they harden and thus become difficult to be removed.

After the CMP step, contamination threat of Na^+ and K^+ ions exists that are present in the slurry. RCA cleaning was used to remove the lack of any contamination particles posterior to this process. This specific RCA incorporates a two step cleaning. First step removes the organic contaminations and the second step removes the metallic ones.

In order to examine the effect of surface roughness on quality of crystalllization,

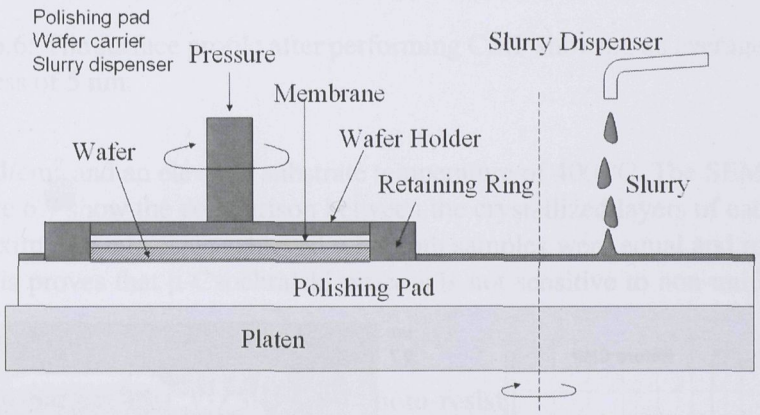
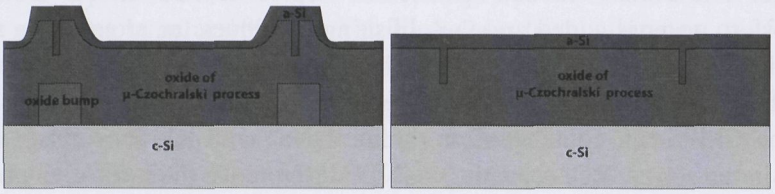


Figure 6.3: MECAPOL E460 CMP machine is schematically drawn in this image.

two different stack of layers have been crystallized. Different stacks of layers are shown in Figure 6.4(a). In Figure 6.4(a), the a-Si is deposited on a step height of 700 nm, created by a dummy PECVD SiO_2 depostion and patterning. In Figure 6.4(b), standard µ-Czochralski process is performed.

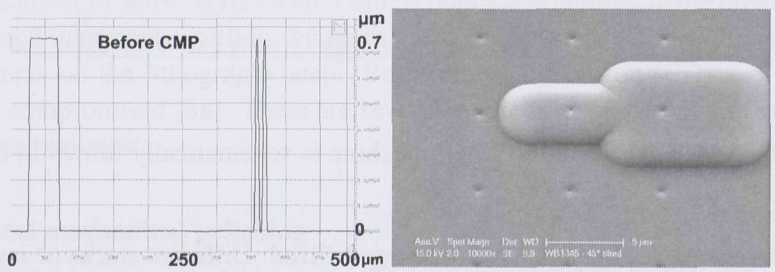
The SEM image of the test structure and its measured step-height is shown in 6.5. Figure 6.6 visualizes the typical stepheights, related to previously shown stepheights, after performing the CMP step. Steps of 700 nm height are turned reduced to an average surface roughness of 5 nm.

The samples were both irradiated by a 25 ns pulse, with an energy density of



(a) (b)

Figure 6.4: Schematics of the experiment designed to determine the effect of surface roughness on the quality of crystallization.



(a) (b)

Figure 6.5: The typical step heights prior to CMP step are in the order of 700 nm, as shown in Figure (a); Figure (b) shows an SEM image of such an island.

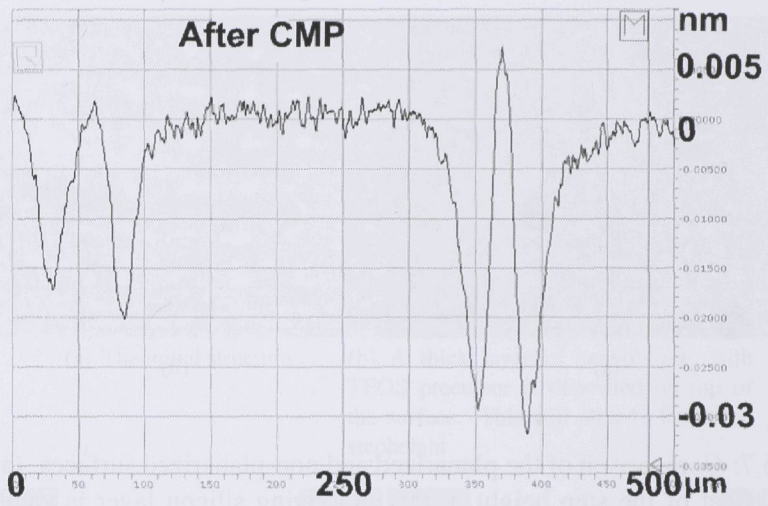
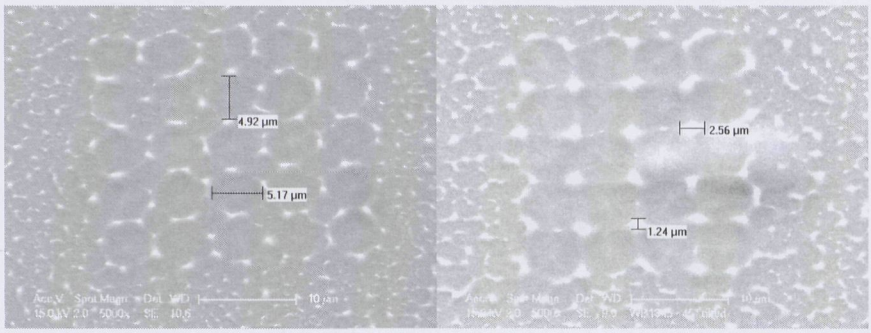


Figure 6.6: The surface profile after performing CMP showing an average surface roughness of 5 nm.

1400 mJ/cm^2 and an elevated substrate temperature of 400 °C. The SEM images in Figure 6.7 show the comparison between the crystallized layers of each stack. The maximum grain sizes achieved with both samples were equal and roughly 6 µm. This proves that µ-Czochralski process is not sensitive to non-uniformities of order.

The etch-back of PECVD SiO_2 and photo-resist

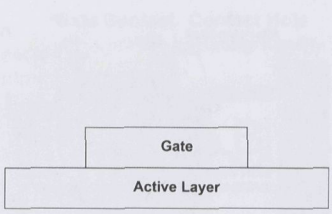
As it was mentioned in the previous section, CMP adds contaminations to the process. These were mentioned to be removable by the RCA cleaning. Since the µ-Czochralski process is found to insensitive to the roughness of the surface, alternatives for the CMP process have been explored. An incomplicated alternative to this method of planarization, is the etch-back of PECVD SiO_2 and photo-resist. The idea behind this method is that by controlling the plasma settings, SiO_2 and photoresist can be etched by the same etch-rate. Initially, the photoresist makes the surface planar since it is a liquid, 2 µm thick and can be span with high speed over a substrate just after deposition. This planar surface can be etched without creating a step height when reaching the SiO_2 as they are both etched with a same etch rate. Dependening on the step height, by utilizing the propper inversed mask, it can be reduced. Figure 6.8 describes this process more clearly. The process starts with having a step height on the surface. A 2 µm thick PECVD SiO_2



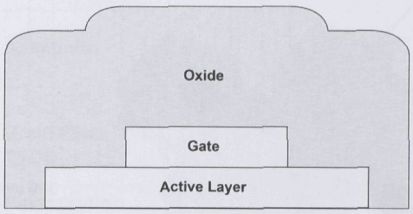
(a) (b)

Figure 6.7: Comparison of the planarized and non-planarized surfaces. (a) shows the the effect of the step height of the underlying silicon layer is vanished by performing a CMP step. The crystallization of a successive silicon layer on top of a non-planarized surface is shown in (b).

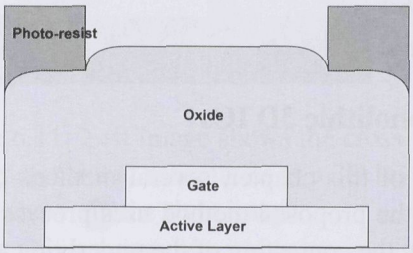
with TEOS precursor is deposited at 350 °C. This deposition already reduces the step height and makes the surface more uniform. In case of step heights larger than roughly 1 µm, planarization using etching the SiO_2 and resist with the same rate will not lead to adequate planarization. An extra masking step using the inverted mask of the process step which introduced the original step height is then used to reduce the roughness. Moreover, if the the aim is to planarize the gate area, the inversed mask of the gate patterning is used. After this patterning step using the inversed gate mask, an isotropical etching using buffered HF solution is performed. Photo-resist is then removed, and a new layer of 2 µm thick of photo-resist is deposited on the wafer. This resist does not need any patterning or development. After this deposition, this structure is now planarized. If the photo resist is etched with the same rate as the oxide, this planarity will be shifted to a lower depth. The deposited photo-resist and partially the SiO_2 layer will be removed leading to complete removal of the initial step height . A dry etching step is used to etch the stack unisotropically. Once the surface of the oxide is reached, the etcher will change the plasma composition, thus etching the photo-resist faster than the oxide . Figure 6.9 shows a initial step height present on the wafer with the results of the planarization with PECVD SiO_2 with TEOS precursor etch-back method. The final step heights are in orders of tens of nanometers. This is roughly an order higher than the results achieved with the CMP step. However, in many cases, this trade-off acceptable for having a less complex process.



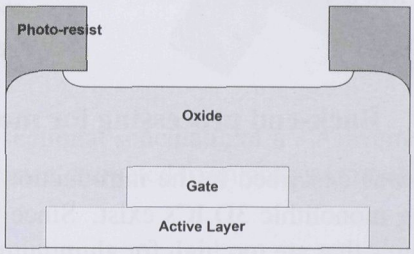
(a) The initial structure



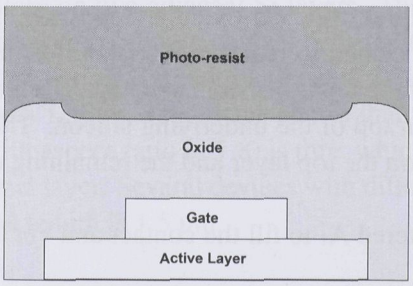
(b) A thick layer of pecvd SiO_2 with TEOS precursor is deposited on top of the surface. This will already lower the stepheight



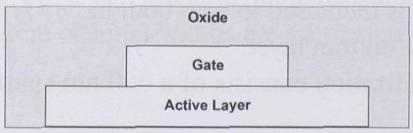
(c) Coating with photo resist and patterning it with inverse of the gate mask.



(d) Wet etching of the open area to lower the step height.



(e) Depositing a thick layer of photo resist, and baking it without any development.



(f) Etching back the pecvd SiO_2 with TEOS precursor and the photo resist with the same etch rate.

Figure 6.8: The procedure of SiO_2 etch-back planarization.

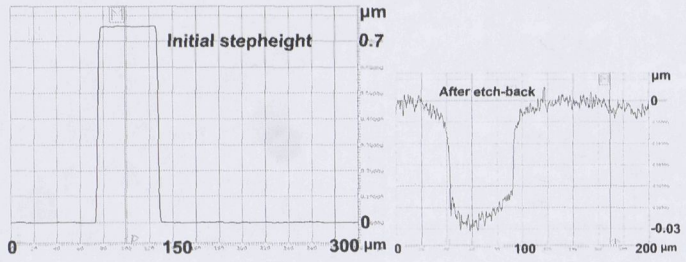


Figure 6.9: Figure (a) shows the initial step height of the stack of layers. The results of planarization using the etch-back of PECVD SiO_2 and photo-resist is given in Figure (b).

6.2.3 Back-end processing for monolithic 3D ICs

As it was described in the introduction of this chapter, several methods of realizing monolithic 3D ICs exist. Since the proposed method uses process temperatures that are too high for aluminum, the contacting of the underlying active devices is postponed to the final step. The process of making the contacts for the top and bottom layer devices is shown in Figure 6.10. After completion of the second layer transistors, a 800 nm thick PECVD oxide is deposited. First, through a via mask, 800 nm of SiO_2 is etched to reach to the island of the top transistor. Thereafter, the silicon body of the top transistor is etched. The etching continues until 800 nm of SiO_2 is left on top of the underlying silicon. The CO mask is then used to etch both the SiO_2 on the top layer and the remaining oxide on the bottom layer.

Metalization consists of a 650 nm sputtered Al to fill the contact and via holes.

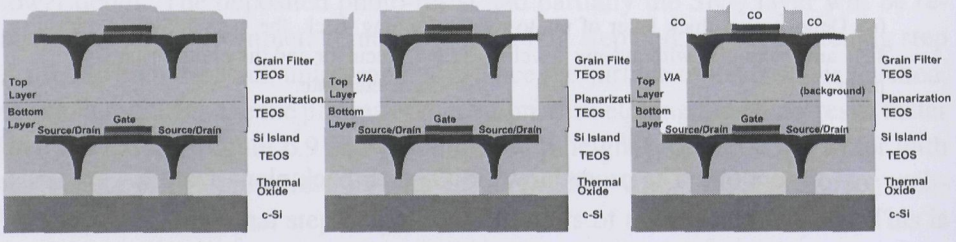


Figure 6.10: Back-end processing of the monolithic 3D ICs

The drain extension of the bottom layer transistor and common connection of the S&D of the inverter is shown. This scheme is shown in Figure 6.11.

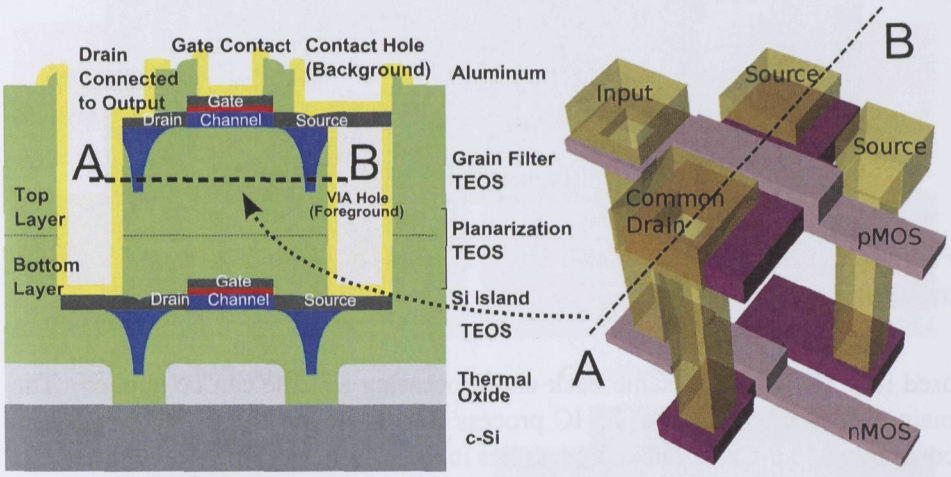


Figure 6.11: Left image shows the cross-sectional schematic of a 3D inverter. A three dimensional schematics of a 3D inverter, extracted form process simulation tool is shown in the right image.

After completion of the back-end processing, the transistors in successive layers are connected with each other. Figure 6.12 shows the TEM image of two transistors on two adjacent Si layers. This cross section is made across the gate and shows the common contact between the two layers as it was discussed in the previous section. The bottom layer is 2.7 μm deep from the top surface and width of vias is 1.5 μm. The image shows that the thickness of Al at the bottom of the via (with aspect-ratio of 1.8) is thin, which causes an increase in the resistance of the metal layer. Several devices with different channel widths are fabricated. The channel length is 1.5 μm.

6.2.4 Fabrication of PLEG Si TFTs

In previous section, the fabrication process flow for a 3D monolithic IC using SG-Si TFT was described. The PLEG layer was investigated in Chapter 4 and presented as a promising candidate to replace the μ-Czochralski process. In order to use PLEG Si TFTs as a building block of a monolithic 3D IC, minor changes need to be applied to the presented process flow. Figure 6.13 shows the process flow for fabrication of a TFT on a PLEG layer. In case these TFTs are to be

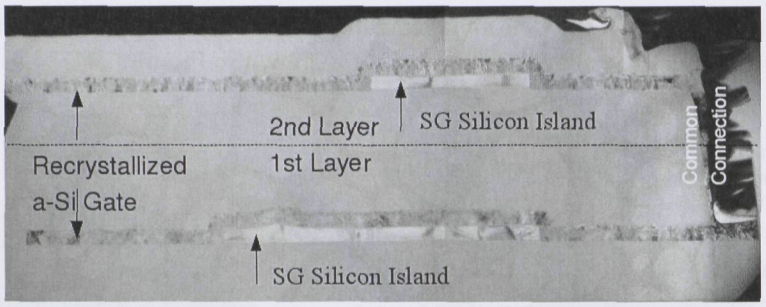


Figure 6.12: TEM image of two layer of a nMOS stacked on top of a pMOS transistor.

used in a 3D structure, same back-end processing scheme can be applied. The main difference between a 3D IC process flow based on the PLEG process, in comparison to μ-Czochralski process lies in the cavity creation step. In the PLEG process, the cavity must land on the seeding layer.

6.3 Design methods of SG TFTs based on μ-Czochralski and PLEG processes

The design rules according to which the SG TFTs can be fabricated is given in Table 6.1. The The corresponding masks to fabricate a PLEG Si TFT are presented in Figure 6.14. The design rules related to fabrication of a TFT on a PLEG substrate is in many aspects similar to the ones of the μ-Czochralski SG TFTs. However, in the design of a 3D IC based on PLEG TFTs, more conisderations are required. Figure 6.15 shows the comparison between the area efficiency between two films, obtained by μ-Czochralski and PLEG process. It is visible that in the case of a 3D design, areas need to be reserved for the seeding to the second layer. Figure 6.16 is the schematic representation of a 3D IC based on both approaches. Here, it is shown that due to the critical dimension of the lithography step used here, the grains must be reserved for seeding of the upper layer. In other words, there is not enough space to form a TFT channel in a single grain, while acting as a seed for the successive silicon layer. This reduces the efficiency of the PLEG process. Thus, PLEG becomes attractive for processes with repeatable design routines, such as 3D SRAM. In custom designs with little repeated patterns, the freedom of design is highly compromised. This loss of efficiency is less apparent

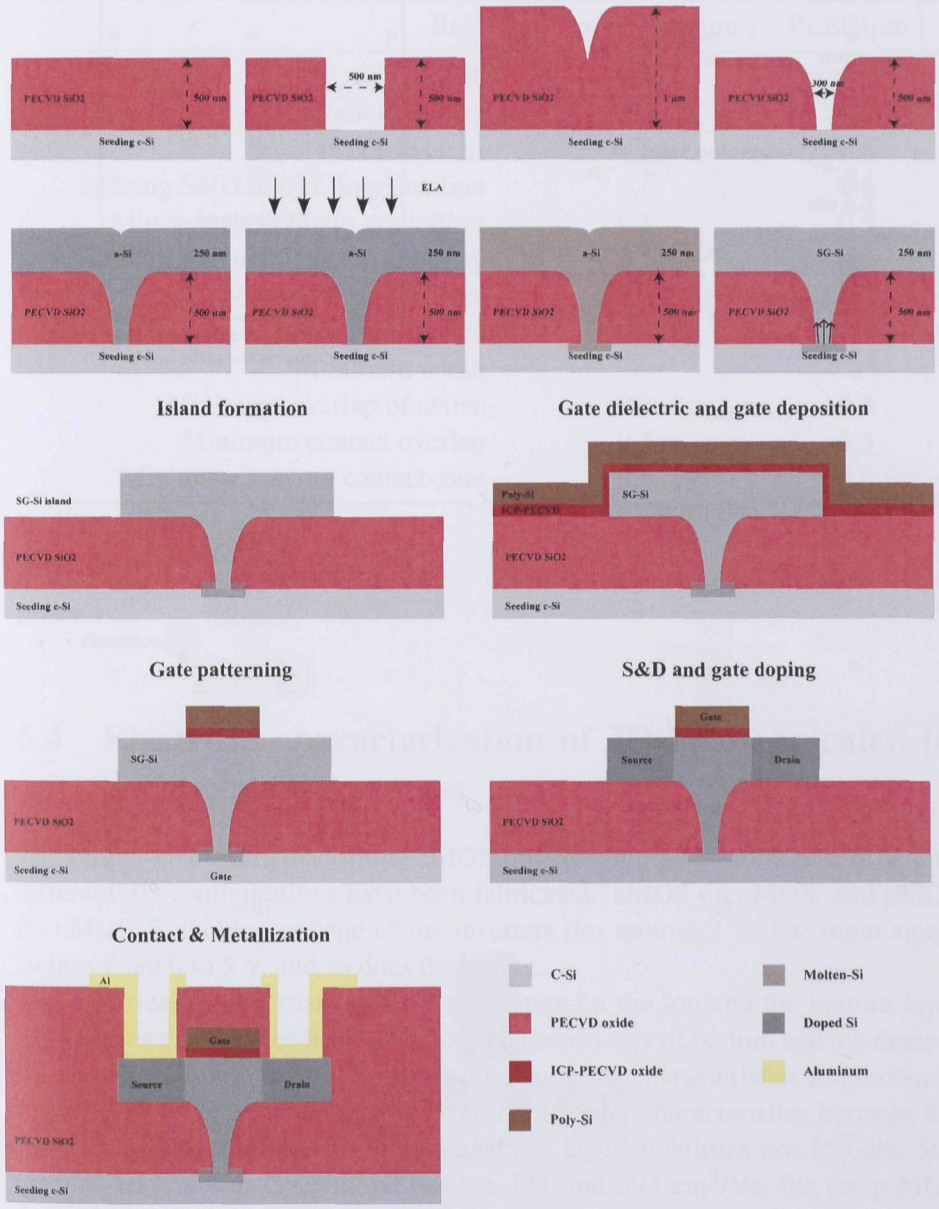


Figure 6.13: Schematics of fabrication of a TFT on top of a PLEG silicon

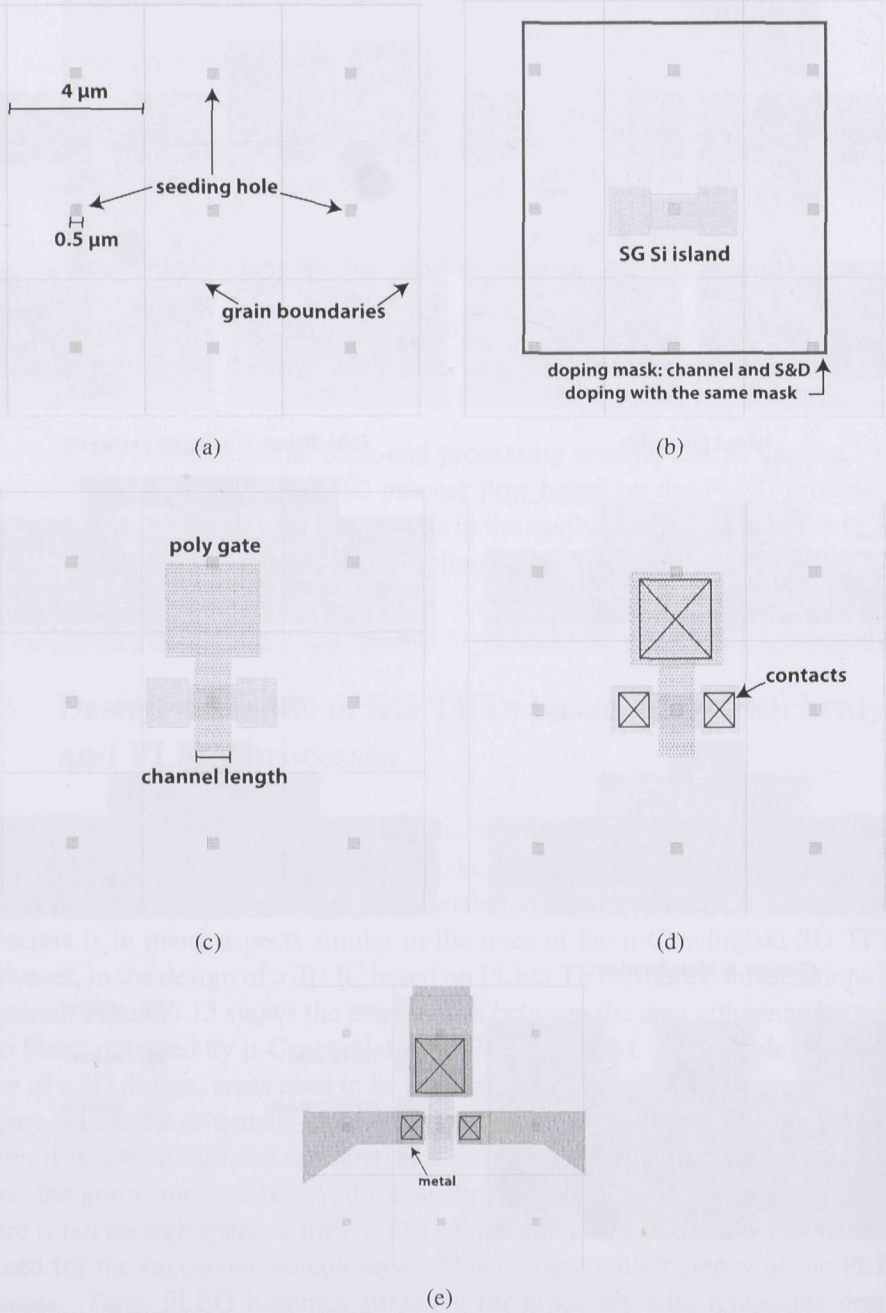


Figure 6.14: The masks that are used to fabricate a PLEG Si TFT are presented

Table 6.1: The design rules followed for fabrication of monolithic 3D ICs

Rule	μ-Czochralski [μm]	PLEG[μm]
Grain Pitch	6x6	4x4
Grain filter size	1	0.5
Spacing active areas	0.6	0.6
Spacing S&D of diff. implantation	0.6	0.6
Minimum spacing to grain filter	0.5	0.5
Minimum spacing to grain boundary	0.5	0.5
Minimum contact size	1.5x1.5	1x1
Minimum via size	2.5x2.5	2.5
Minimum width	1	1
Minimum overlap of active	0.3	0.3
Minimum contact overlap	0.5	0.3
Minimum spacing contact-gate	0.6	0.6

as the devices are down scaled. This will not be an issue in a more downscaled process.

6.4 Electrical characterization of 3D ICs fabricated by μ-Czochralski process

The output characteristics of the CMOS inverters are given in Figure 6.19 Two different 3D configurations have been fabricated: nMOS on pMOS, and pMOS on nMOS. Switching voltage of the inverters lies around 2 V. The input signal swings from 0 to 5 V, and so does the output.
The electrical characteristics of the transistors on the top and the bottom layer SG-Si layer are reported here. The I_dV_g characteristics of bottom and top devices are shown in Figure 6.17. The corresponding I_dV_d characteristics are shown in Figure 6.18. A good matching between the transfer characteristics between the top and bottom transistors is observed. Top layer mobilities are 159 and 565 cm^2/Vs and bottom layer mobilities are 141 and 393 cm^2/Vs, for the p-MOS and n-MOS devices respectively. The field-effect mobility of the transistors is calculated using the following equation:

$$\mu_{eff-max} = \frac{gm_{max}L}{WC_{ox}V_{ds}} \tag{6.1}$$

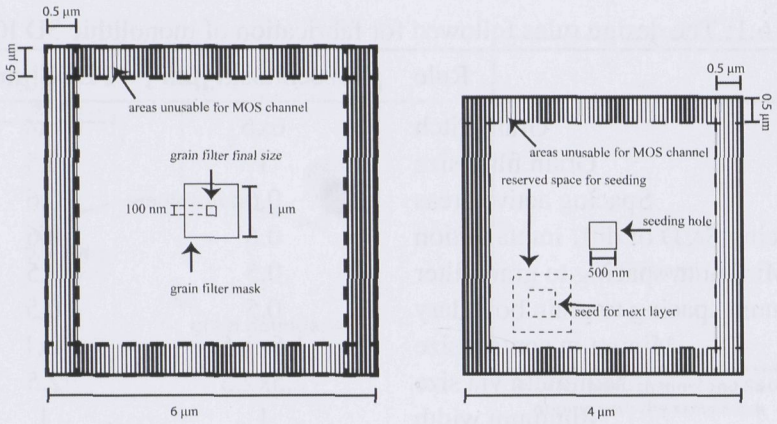
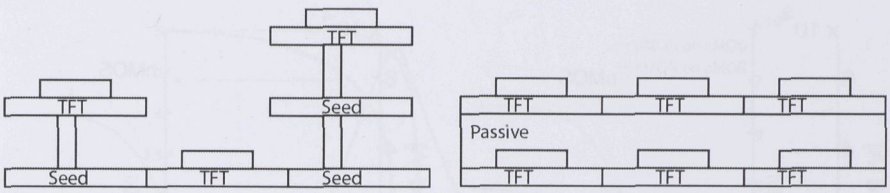


Figure 6.15: Comparison of area efficiency for grainfilter and epitaxial process.

Here is $\mu_{eff-max}$ the maximum field-effect mobillity of the charge carriers, gm_{max} the maximum transconductance, L the channel length, W the channel width, V_{ds} the drain voltage used during the I_dV_g measurement and C_{ox} the capacitance of the gate oxide. The latest can be calculated according to the following equation:

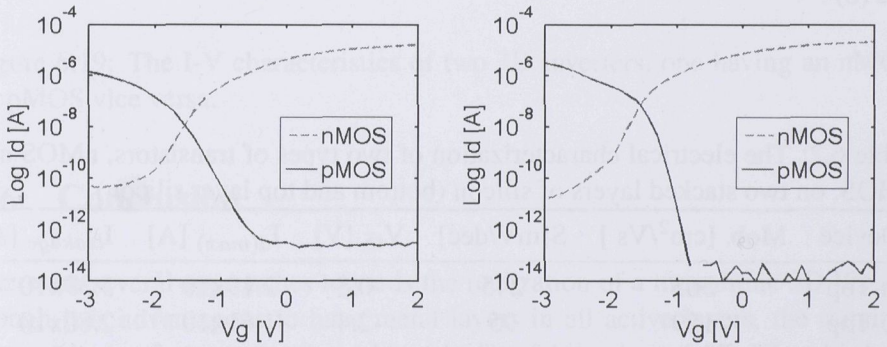
$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{T_{ox}} \tag{6.2}$$

Here, ϵ_{ox} is the relative permittivity of the SiO_2, ϵ_0 the permittivity of vacume and T_{ox} the SiO_2 thickness of the gate.
Table 6.2 reports the average characteristic values for different devices on each layer. The devices on the top layer have slightly better performance than those on the bottom layer. This is due to process variations such as better gate patterning by dry etching. Threshold voltage variation was found to be about 0.1 V. The maximum drain current ($I_{d(max)}$) is measured at V_{ds} =0.1 V. $I_{leakage}$ is measured at V_{gs}= 2 and -3 V for the p- and nMOS devices, respectively. The main reason for the high drain leakage ($I_{leakage}$) of the bottom layer TFTs, is over-etching of Si island by gate patterning process at the source and drain regions. The electrical characteristics matching between the top and bottom devices is one proof of the fact that the laser crystallization of the top layer devices does not damage the bottom layer devices.



(a) (b)

Figure 6.16: The difference between the seeding scheme of a PLEG process, (b), and the stacking of the μ-Czochralski process, (b) is depicted. This schematic shows that with the design rules mentioned in Table 6.1, a single grain can only be used to form the channel of a TFT, or to be used as the seed for the successive layer.



(a) (b)

Figure 6.17: The I_dV_g characteristics of bottom and top devices are shown in (a) and (b)

6.5 Electrical characterization of TFTs based on PLEG Si substrate

The I_dV_g characteristics of a nMOS transistor on a PLEG Si layer is shown in Figure 6.20. The corresponding I_dV_d curves are shown in Figure 6.22. The ouput curves show transistor characteristics. In case of the pMOS, the on current is low. This is mainly due to the high source and drain resistance. This can be concluded from the difference in on current at V_d=0.1 and V_d=5 in Figure 6.20(a). The I_dV_g curves show that compared to μ-Czochralski SG TFTs, the leakage current is the fabricated PLEG TFTs is roughly 2 orders higher. This high leakage can

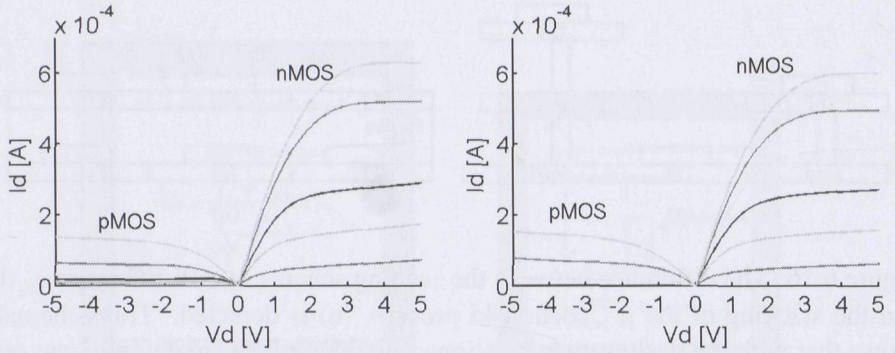


Figure 6.18: The I_dV_d characteristics of bottom and top devices are shown in (a) and (b)

Table 6.2: The electrical characterization of two types of transistors, nMOS and pMOS, on two stacked layers of silicon (bottom and top layer silicon).

Device	Mob. [cm^2/Vs]	S[mV/dec]	V_{th} [V]	$I_{d(max)}$ [A]	$I_{leakage}$ [A]
n-Top	565	245	-0.8	$2.19x10^{-5}$	$5.39x10^{-12}$
p-Top	159	95	-2.4	$1.61x10^{-5}$	$2.80x10^{-13}$
n-Bot.	393	280	-0.6	$1.81x10^{-5}$	$1.49x10^{-10}$
p-Bot.	141	151	-2	$1.43x10^{-5}$	$9.20x10^{-13}$

be explained to non-optimal source and drain activation step. The I_dV_d curves in Figure 6.22 prove the existance of all three modes of operation, being cut-off, linear and saturation, to be present in these devices.

The transconductance is calculated as the slope of the I_dV_g curve in the linear scale. The transconductance and the μ_{eff} plotted against the gate voltage is shown in Figure 6.21. The $\mu_{eff-max}$ is calculated according to the equation 6.1. With a gate oxide thickness of 50 nm, and the W/L ratio of 2, mobilities of 530 cm^2/Vs and 214 cm^2/Vs are found for nMOS and pMOS respectively. This curves and the high mobility proves the PLEG process to be suitable candidate for monolithic fabrication of 3D ICs.

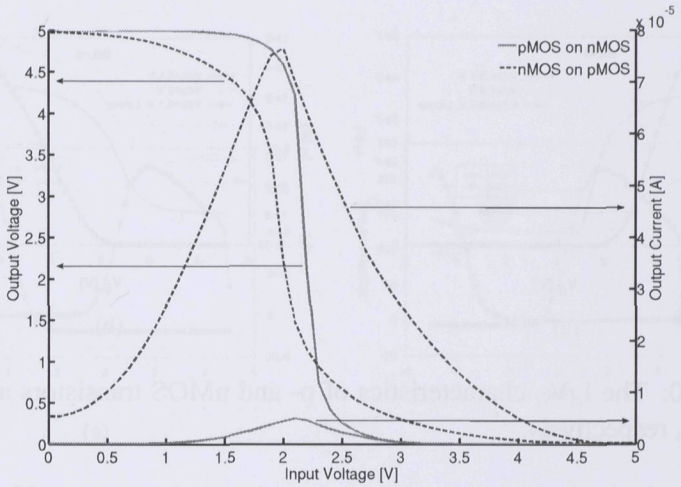


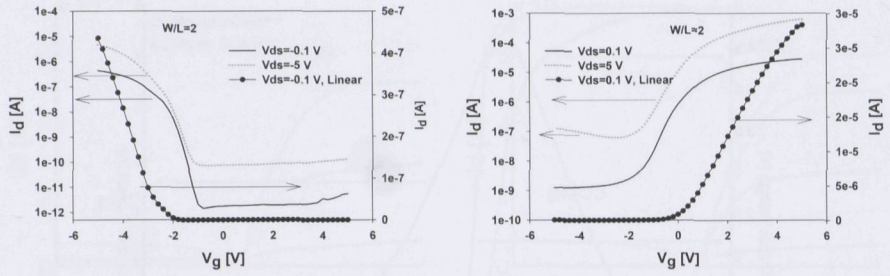
Figure 6.19: The I-V characteristics of two 3D Inverters, one having an nMOS on pMOS vice versa.

6.6 Conclusion

There are several approaches towards the realization of a monolithic 3D IC. Although it is advantagous to have metal layers in all active layers, the required thermal budget can not yet be achieved. For fabrication of 3D ICs with both the µ-Czochralski and the PLEG process, the front-end processing of each active layer is done. Finally in one back-end process, all devices in each layer will be contacted and metallized.

Planarization of the active layers is a key element in 3D ICs. First, it is proven that the µ-Czochralski process is weakly dependent of the non-uniformities of the underlying layers. However, these non-uniformities form a limiting factor for the lithography step and thus must be removed. Using CMP, the step heights in orders of µm s can be reduced to roughly 5 nm. The CMP step adds many contaminations to the process. It is proposed that in the cases if perfoming a CMP step is not essential, it can be replaced by a simpler step using subsequent deposition and etching of SiO_2 and photo-resist. This approach will lead to final step heights in the order of tens of nanometer.

The 3D IC fabrication process for PLEG is proven to be similar to a 3D IC fabrication process using the µ-Czochralski process. Vertical stacking of SG TFTs by the µ-Czochralski process is successfully demonstrated. Electrical characteristics



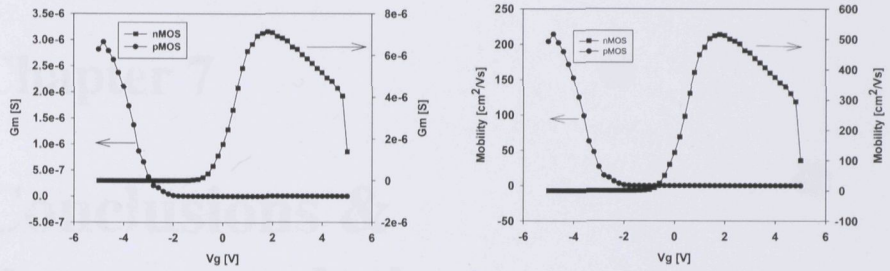
(a) (b)

Figure 6.20: The I_dV_g characteristics of p- and nMOS transistors are shown in (a) and (b), respectively.

matching between the top and bottom devices proves that the laser crystallization of the top layer devices does not damage the bottom layer devices. Top layer mobilities are 159 and 565 cm^2/Vs and bottom layer mobilities are 141 and 393 cm^2/Vs, for the pMOS and nMOS devices respectively. Two kinds of 3D CMOS inverters are constructed; nMos SG TFT stacked on pMOS type and vice versa. These inverters are capable of full voltage swing and have symmetric voltage characteristics.

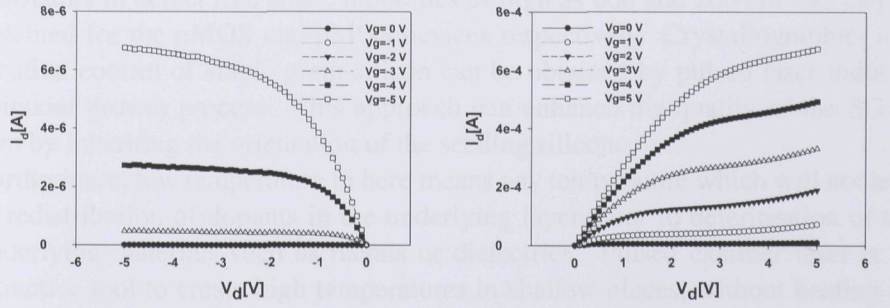
The efficiency of the PLEG process as a candidate for the active layer of a monolithic 3D IC is compared to the µ-Czochralski process. The critical dimension of the lithography has a decisive role determining if the PLEG process will be as efficient of the µ-Czochralski process.

The Transistors made on PLEG Si layer show high mobilities of 512 cm^2/Vs and 214 cm^2/Vs for the nMOS and pMOS, respectively. The I_dV_d output curves proves that these devices are capable of acting in all three regimes of operation of a MOS transisotrs.



(a) (b)

Figure 6.21: The transconductance against the gate voltage for both nMOS and pMOS PLEG transistors is shown in (a). The corresponding The μ_{eff} using the process and design parameters is given in (b).



(a) (b)

Figure 6.22: The I_dV_d characteristics of p- and nMOS transistors are shown in (a) and (b)

Chapter 7

Conclusions & Recommendations

7.1 General conclusions

7.1.1 Experimental

In this Chapter, an introduction is given to the commonly used tools and methods during this work. The μ-Czochralski process is the predecessor of this work, enables obtaining a location-controlled thin film. By placing the channel of TFT transistors in defect free areas, mobilities as high as 600 and 200 cm^2/Vs can be obtained for the nMOS and pMOS devices respectively. Crystallographic- and location control of single grain silicon can be obtained by pulsed laser induced epitaxial growth process. This approach can enhance the quality of the SG-Si film by inheriting the orientation of the seeding silicon.
Furthermore, low temperature in here means any temperature which will not lead to redistribution of dopants in the underlying layers, nor to deterioration of the underlying materials such as metals or dielectrics. Pulsed excimer laser is an attractive tool to create high temperatures in shallow places, without heating up the whole structure. The laser used in this work may have a heated substrate up to 450 °C. It owns two laser sources with each a 25 ns, full width half maximum(FWHM) long pulse. There is a pulse extender unit which can be utilized to obtain a longer pulse. The choices for the LTO is PECVD for passivation, and ICPCVD for gate dielectric. ICPCVD shows superior characteristics compared to the rest. PECVD is fast, has degassing and step-coverage sufficient for the processes during this work.

7.1.2 Numerical analysis of pulsed excimer laser annealing process

Calculation time, price and accuracy of a simulation are crucial factors to decide what type of simulation one needs. The choice of simulation method is always the compromise between accuracy of the results and the needed calculation time. The main question that the simulation must answer determines in which ratio of this two parameters must be compromised.
Three methods of simulation, diffusion method, diffusion method with adaptive mesh and phase-field approach are explained and compared.
phase-field is accurate and contains data about the phase between a solid and liquid. This makes it very attractive approach for PLEG process simulation, where the melt depth is an important aspect. However, it is a relatively slow simulation and thus in cases which less accuracy is required, diffusion method is used. Diffusion method is very adaptable, since commercially available software offer this method. Diffusion method with adaptive mesh, allows the system to be heavily meshed, in places where it is needed. Thus is offers a proper ratio of speed and accuracy. It is superior to the standard diffusion method in all cases. However, editing the structure, or 3D structures are more challenging to realize.

7.1.3 Pulsed laser induced epitaxial process

Silicon grains with 4 x 4 μm^2 area were obtained on top of the holes. Arrays of SiO_2 openings of 84 °sidewall with 4 µm pitch were designed. Areas as large as 2.5 x 1.7 mm^2, which is the laser beam spot size, were crystallized. By EBSD measurement, the orientations of these grains have been investigated. Preferred (100) orientation have been observed for samples of both bulk and SOI seeding layers. In case of 250 ns pulse, energy density for crystallization is less than 1500 mJ/cm^2 for a SOI seeding wafer and 1600 mJ/cm^2 for bulk wafer seeding, we do not melt the c-Si seed layer. Thus the seed for nucleation consists of several orientations.
Longer pulse durations result in deeper melt depths and higher surface ablation threshold. Seeding from a SOI wafer seems to require less laser energy density due to better heat confinement of the structure, due to thinner seeding silicon and the low thermal conductivity of underlying buried oxide layer. However, by increasing the pulse duration, bulk wafer has a larger increase in process window and more suitable to be used as seeding layer for epitaxy. The quality of the crystallized layer appears to be better in case of bulk wafer which can be explained by the better quality silicon. The oxide sidewall angle can be varied by

changing the etching type. However, the defect density remained mostly equal for both sidewall angels. This study shows successful location- and orientation-controlled large 4 x 4 μm^2 silicon grains, with (100) orientation, which can be used for transistor layer of the building blocks for high quality 3D-IC, applicable for e.g. SRAMs and SoCs. Longer pulse durations result in deeper melt depths and higher surface ablation threshold. Seeding from a SOI wafer seems to require less laser energy density due to better heat confinement of the structure, due to thinner seeding silicon and the low thermal conductivity of underlying buried oxide layer. However, by increasing the pulse duration, bulk wafer has a larger increase in process window and more suitable to be used as seeding layer for epitaxy.

7.1.4 Single grain photo-diodes using thick silicon crystallization

Maximum Si thickness that can be crystallized was investigated in the μ-Czochralski process with excimer laser. Elongation of pulse duration and substrate heating are effective in increasing the maximum Si thickness. Cracks in crystallized films were reduced by substrate heating. Location-controlled grains with 1 μm thick Si was obtained successfully. Single grain P-I-N photo-diode was fabricated inside of these thick SG-Si. Dark current of 100 μm x 100 μm size arrays are on the order of 0.1 nA for SG- photo-diodes with 1 μm, 1.5 μm and 2 μm intrinsic region length.

7.1.5 Demonstration of a monolithic 3D IC

There are several approaches towards the realization of a monolithic 3D IC. Although it is advantagous to have metal layers in all active layers, the required thermal budget can not yet be achieved. For fabrication of 3D ICs with both the μ-Czochralski and the PLEG process, the front-end processing of each active layer is done. Finally in one back-end process, all devices in each layer will be contacted and metallized.

Planarization of the active layers is a key element in 3D ICs. First, it is proven that the μ-Czochralski process is weakly dependent of the non-uniformities of the underlying layers. However, these non-uniformities form a limiting factor for the lithography step and thus must be removed. Using CMP, the step heights in orders of μm s can be reduced to roughly 5 nm. The CMP step adds many contaminations to the process. It is proposed that in the cases if perfoming a CMP step is not essential, it can be replaced by a simpler step using subsequent depo-

sition and etching of SiO_2 and photo-resist. This approach will lead to final step heights in the order of tens of nanometer.
The 3D IC fabrication process for PLEG is proven to be similar to a 3D IC fabrication process using the μ-Czochralski process. Vertical stacking of SG TFTs by the μ-Czochralski process is successfully demonstrated. Electrical characteristics matching between the top and bottom devices proves that the laser crystallization of the top layer devices does not damage the bottom layer devices. Top layer mobilities are 159 and 565 cm^2/Vs and bottom layer mobilities are 141 and 393 cm^2/Vs, for the p-MOS and n-MOS devices respectively. Two kinds of 3D CMOS inverters are constructed; nMos SG TFT stacked on pMOS type and vice versa. These inverters are capable of full voltage swing and have symmetric voltage characteristics.
The efficiency of the PLEG process as a candidate for the active layer of a monolithic 3D IC is compared to the μ-Czochralski process. The critical dimension of the lithography has a decisive role determining if the PLEG process will be as efficient of the μ-Czochralski process.
The Transistors made on PLEG Si layer show high mobilities of 512 cm^2/Vs and 214 cm^2/Vs for the nMOS and pMOS, respectively. The I_dV_d output curves proves that these devices are capable of acting in all three regimes of operation of a MOS transisotrs.

7.2 Recommendations

7.2.1 Vertical P-I-N photo-diodes using SG-Si

The advantages of SG-Si obtained by the μ-Czochralski process for making high-quality P-I-N photo-diodes have been extensively discussed in Chapter 5. The pros and cons of lateral P-I-N have also been explained. It is possible to use the SG-Si for realizing vertical P-I-N photo-diodes. By doing so, the diode density and thus the quantum efficiency of the system can drastically increase. However, several serious issues need to be considered before realizing this devices.
In the vertical pin diode, it is hard to control the highly-doped regions. since the excimer laser is used to for annealing, controlling the depth of dopants are challenging. during the crystallization part of the μ-Czochralski process, the deposited a-Si will melt completely at no-grain areas. Since at liquid state, the diffusivity of the dopants in silicon are extremely high, maintaining the original distribution of the doped region at the bottom of the structure is impossible. a

possible solution is to perform a high energy implantation, to trap the dopants at the si/ox interface. this happens after the μ-Czochralski process. to anneal this layer excimer laser with its shallow absorption length is not the most efficient tool. moreover, a non-melt annealing regime at 1 μm depth is required. This could theoretically be possible, as it can be proven by Figure . In this figure is shown that the temperatures at the depth of 1 μm reach 1000 mJ/cm^2 and thus suitable for non-melt annealing However, this reproducibility of this process is extremely challenging. annealing the top doped region is less challenging since ELA is a highly effective tool for activation of implanted shallow junctions.

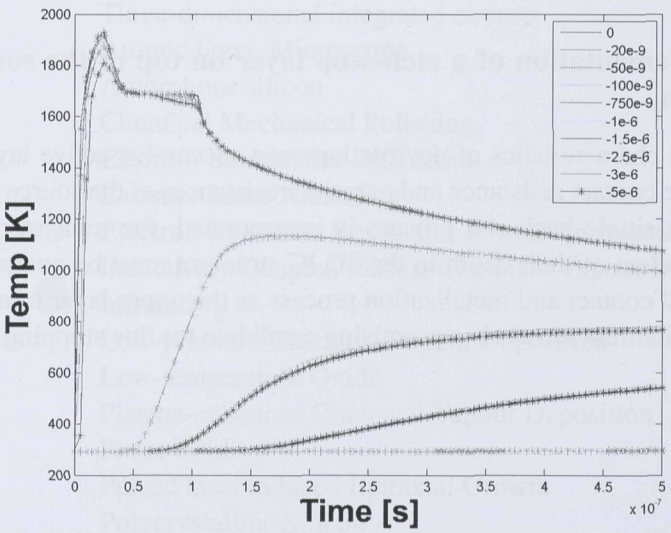


Figure 7.1: The simulation shows the theoretical possibility of activation of the top layer P^{++} layer, without deteriorating the underlying doped layer.

7.2.2 Stress engineering in thick silicon crystallization

The changing of the underlying material for the thick silicon crystallization has not been successful. According to the theory, the underlying material will play an important role to the stress formation in the crystallized layer. However, this may suggest that the main reason of the stress formation is the volume increase during the excimer laser annealing. Green laser, with its higher absorption depth, induces less stress in the crystallized films. As a result of this observation, green

laser must be investigated as a proper candidate for crystallization of a-Si films thicker than 500 nm.

7.2.3 3D ICs based on PLEG-Si layer

In order to realize a 3D IC using the PLEG-Si layer, without downscaling "privileges", an LDD process needs to be integrated into the PLEG process flow. Since without the downscaled transistors, the transistor density of the upper lying active layers is low, each layer must have its own back-end process. The silicon area which is preserved for the means of seeding to the successive layers, will then be used as routing areas for the underlying active layers.

7.2.4 Implementation of a etch-stop layer on top of the source and drain

The electrical characteristics of devices between successive active layers is dependent on the contact resistance and parasitic resistances of the source and drain. In case that a single back-end process is incorporated, the transistors on each layer, independent of their depth in the 3D IC structure must be guaranteed of a exact identical contact and metalization process as the upper layer transistors. A thin layer of titanium nitride is a promising candidate for this stopping layer.

List of abbreviations

μ-Czochralski	Micro-czochralski
3D IC	Three-dimensional integrated circuits
AFM	Atomic Force Microscope
a-Si	Amorphous silicon
CMP	Chemical Mechanical Polishing
EBSD	Electron Backscatter Diffraction
ELA	Excimer Laser Annealing
ECR-PECVD	Electron Cyclotron Resonance Plasma-enhanced Chemical Vapor Deposition
ICPECVD	Inductively Coupled Plasma Chemical Vapour Deposition
IR	Infrared
LPCVD	Low-pressure Chemical Vapour Deposition
LTO	Low-temperature Oxide
PECVD	Plasma-enhanced Chemical Vapour Deposition
PF	Phase-field
PLEG	Pulsed laser induced Epitaxial Growth
Poly-Si	Polycrystalline Silicon
SEM	Scanning Electron Microscope
SG	Single-grain
SG-Si	Single-grain Silicon
SG-TFT	Single-grain Silicon Thin-film Transistors
SOI	Silicon-on-Insulator
TEM	Transmission electron microscopy
TEOS	Tetra-ethyl-ortho-silicate

Summary

Down-scaling of transistors increases the density of the chip and the interconnects. The higher device density needs more space reserved for routing purposes, which does not take the full advantage of the down-scaling. Interconnect delay decreases not as fast as the gate delay reduction and will become a limiting factor for total system performance. Three-dimensional (3D) integration is a solution for those issues as it shortens the interconnect length and reduces power consumption, while increasing the functionality of a chip by enabling the integration of a sensor layer on top of it. There are three categories of 3D ICs: package level, wafer level and monolithic integration. Monolithic integration results in the largest decrease in interconnect length, highest density of interconnects between the successive active silicon layers and offers the most freedom of design. The key to the success of monolithic 3D integration lies in obtaining high-quality substrate material for the upper lying active layers. The μ-Czochralski process offers the location-control of large single grain silicon (SG-Si) created by means of excimer laser crystallization using low temperatures. By controlling the position of the crystallized grains, the channel of the MOS transistors can be designed to fit within such grains. The lack of grain boundaries in such grains enables fabrication of high mobility transistors. However, the crystallized grains consist of multiple crystallographic orientations with random boundaries present in between them. the field-effect mobility of the transistors is anisotropic to the crystallographic orientation of the silicon grains. Thus, in order to reduce variations in the mobility of SG-TFTs, the crystallographic-orientation of the silicon in the channel must be controlled. The proposed solution in this work is Pulsed-Laser-induced epitaxial growth (PLEG). Inheritance of the crystallographic orientation of the seeding layer by the a-Si film happens during a consequent melt and solidification phase transition, by an pulse excimer laser irradiation. The maximum temperature used in this process is 545 °C, belonging to the LPCVD process step. In this work, this process is considered a low-temperature process. A definition of the term low-temperature is given and discussed. Pulsed excimer laser is the

key element to this process. The strengths and limitation of this tool is summed up. Furthermore, in order to realize 3D ICs using low temperatures, a LTO is needed. The ICPCVD SiO_2 is the perfect candidate to serve as the gate dielectric of the TFTs.

The crystallization of a-Si is a process consisting a melt and solidification step. In order to gain a better understanding of this process, simulation tools are needed. Phase-field approach is used to follow the melt-front during the PLEG process. Phase-field simulations are slow and complex in terms of convergence. In the case of a simple thermal evaluation of the system, a simple heat diffusion simulation is proposed. The compromise between the phase-field and the heat diffusion method can be found in a custom simulation tool, made in TU Delft, which combines the heat diffusion method with melt-front tracking and non-linear meshing in order to improve the duration.

Using the phase-field simulation, a better understanding of the PLEG process is obtained. Type of the seeding layer, excimer laser pulse duration and energy density and the aspect ratio of the seeding cavity are found to be of great relevance to this process. Silicon grains with an area of 4 x 4 μm^2 are obtained on top of the seeding holes. A preferred orientation of $<100>$ is observed for samples of both bulk and SOI seeding layers, using EBSD measurement. Longer pulse durations result in deeper melt depths and a higher surface ablation threshold. Seeding from an SOI wafer appears to require less laser energy density due to a better heat confinement of the structure. By increasing the pulse duration in the case of the bulk wafer, there is a larger increase in the process window and more suitable to be used as a seeding layer in epitaxy. The oxide sidewall angle can be varied by changing the etching type. Steeper holes lead to more filtering of the created twins at the SiO_2 sidewall.

A novel method of realizing high speed photo-diodes suitable for 3D integration is proposed. These photo-diodes are fabricated using low-temperatures. The μ-Czochralski process is used to enable a low-defect substrate for the intrinsic region of the P-I-N photo-diodes. In order to increase the sensitivity of these photo-diodes, maximum Si thickness that can be crystallized using the μ-Czochralski process was investigated. Silicon layers with a maximum thickness of 1 μm were crystallized. Elongation of pulse duration and substrate heating are effective in increasing the maximum Si thickness. However, cracks in crystallized films were reduced by substrate heating. Location-controlled grains with 1 μm thick Si was obtained successfully. Single grain P-I-N photo-diode was fabricated inside of these thick SG-Si. Dark current of 100 μm x 100 μm size arrays are on the order of 0.1 nA for SG-Si photo-diodes with 1 μm, 1.5 μm and 2 μm intrinsic region

length.

For fabrication of 3D ICs with both the μ-Czochralski and the PLEG process, the front-end processing of each active layer is done. Finally in one back-end process, all devices in each layer will be contacted and metallized. Planarization of the active layers is a key element in 3D ICs. Two methods of planarization are proposed: CMP and SiO_2 etch-back. Although CMP offers a superior outcome, SiO_2 etch-back process is simpler cleaner. It is proven that the μ-Czochralski process is weakly dependent of the non-uniformities of the underlying layers. The 3D IC fabrication process for PLEG is shown to be similar to a 3D IC fabrication process using the μ-Czochralski process. Vertical stacking of SG TFTs by the μ-Czochralski process is successfully demonstrated. Electrical characteristics matching between the top and bottom devices proves that the laser crystallization of the top layer devices does not damage the bottom layer devices. Top layer mobilities are 159 and 565 cm^2/Vs and bottom layer mobilities are 141 and 393 cm^2/Vs, for the pMOS and nMOS devices respectively. 3D inverters are capable of full voltage swing and have symmetric voltage characteristics. The critical dimension of the lithography has a decisive role determining if the PLEG process will be as efficient of the μ-Czochralski process. The Transistors made on PLEG Si layer show high mobilities of 512 cm^2/Vs and 214 cm^2/Vs for the nMOS and pMOS, respectively.

Samenvatting

Door Down-scaling van transistoren neemt de dichtheid van de chip en de aansluitingen toe. De hogere dichtheid van transistoren, heeft behoefte aan meer ruimte voor routering, waarin de down-scaling niet meer voordelig is. De interconnect vertraging die niet zo snel af neemt als de poortvertraging van de transistoren wordt zo een beperkende factor voor totale prestaties van het systeem. Driedimensionale integratie (3D) is een oplossing voor deze kwesties. Het verkort de interconnectie lengte en vermindert het stroomverbruik, terwijl de functionaliteit van chip integratie wordt verhoogd door een sensor laag boven de geintegreerde schakelingen te maken. Er zijn drie categorien van 3D-IC's: verpakkingsniveau, wafer niveau en monolitische integratie. Monolithische integratie resulteert in de grootste daling in interconnectie lengte, de hoogste dichtheid van interconnecties tussen de opeenvolgende actieve silicium lagen en biedt tevens de meeste vrijheid in het ontwerp. De sleutel voor het succes van monolitische 3D integratie ligt in het verkrijgen van hoge kwaliteit substraatmateriaal voor de boven-liggende actieve lagen. Het μ-Czochralski proces biedt de locatie-controle van grote korrel silicium (Si-SG), gemaakt door middel van excimer laser kristallisatie in lage temperaturen. Door het regelen van de positie van het gekristalliseerde korrels kan het kanaal van de MOS transistoren ontworpen worden om te passen binnen die korrels. Het ontbreken van korrelgrenzen in deze korrels leidt tot verkrijging van hoge mobiliteit transistoren. De gekristalliseerde korrels bestaan uit meerdere kristallografische orintaties met ertussen willekeurige grenzen aanwezig. De mobiliteit van de transistoren is afhankelijk aan de kristallografische orintatie van de polysiloxankorrels. Om variaties te verminderen in de mobiliteit van SG-TFT zal de kristallografische-orintatie van het silicium in hetkanaal moeten worden gecontroleerd. De voorgestelde oplossing in dit werk wordt Pulsed-Laser-induced epitaxial growth (PLEG). Erving van de kristallografische orintatie het zaailaag, door de a-Si film, gebeurt tijdens een opeenvolgende smelt en stol faseovergangen, welke door een Gepulseerde excimer laserbestraling gedaan worden. De maximale temperatuur in deze werkwijze is 545

°C, behorend tot het LPCVD processtap. In dit proefschrift wordt dit proces als een lagetemperatuurproces gezien. Een definitie van de term lagetemperatuur wordt gegeven en besproken. Gepulseerde excimer laser is de sleutel element aan dit proces. Hiertoe zijn de sterke punten en beperkingen van dit apparaat samengevat. Teneinde om 3D ICs met lage temperaturen te realiseren, is een LTO nodig. De ICPCVD SiO_2 is de perfecte kandidaat om te dienen als dielektrische materiaal voor de poort van de TFTs.
Kristallisatie van a-Si is een proces bestaande uit een smelt en stol stap. Om dit proces beter te begrijpen zijn simulatie-instrumenten nodig. Phase-field benadering wordt gebruikt om het smelt front tijdens de PLEG te volgen. Phase-field simulaties traag en complex op het gebied van de convergentie. In het geval van een eenvoudige thermische evaluatie van het systeem wordt een eenvoudige simulatie warmtediffusie voorgesteld. Het compromis tussen de phase-field en de warmtediffusie methode zijn in een aangepaste simulatietool in TU Delft, die de warmte diffusiemethode met smelt-front tracking en niet-lineaire weven gecombineerd om de duur verbeteren.
Met de phase-field simulatie wordt een beter begrip van de PLEG, verkregen. Het Type van zaailaag, excimer laser pulsduur en energiedichtheid en de verhouding van de seeding holte blijken van groot belang voor deze taak te zijn. Polykristalijnen korrels met een gebied van 4 x 4 μm^2 zijn verkregen bovenop de seeding gaten. Een geprefereerde orintatie van $< 100 >$ is waargenomen voor de monsters van zowel bulk-en SOI zaailagen. Langere puls lengtes geven een dieper smelt diepte en een grotere oppervlakte ablatie drempel. Een SOI wafer als een zaailaag lijkt door een betere warmteverdeling en warmteopsluiting minder laserenergie dichtheid te vereisen. Door de toename van de pulsduur bij de bulk wafer is er een grotere toename in het procesvenster. Dit is dus meer geschikt om te worden gebruikt als een zaailaag voor epitaxie. De oxide zijwand hoek kan worden gevarieerd door het etsen type. Steilere gaten leiden tot meer filtering van de gemaakte tweeling op de SiO_2 zijwand.
Een nieuwe methode voor het realiseren snelle fotodiodes geschikt voor 3D integratie is voorgesteld. Deze fotodiodes worden vervaardigd met behulp van lage temperaturen. Het µ-Czochralski proces wordt gebruikt om een laag-defect substraat voor de intrinsieke gebied van de P-I-N fotodiodes mogelijk te maken. Om de gevoeligheid van deze fotodiodes te verhogen, is de maximale silicium dikte die kan worden gekristalliseerd volgens de µ-Czochralski proces onderzocht. Siliciumlagen met een dikte van 1 µm zijn gekristalliseerd. Verlenging van de pulsduur en bodemverwarming blijkt effectief te zijn voor het verhogen van de maximale silicium dikte. De scheuren in de gekristalliseerd films werden

verminderd door bodemverwarming. Een-korrelige P-I-N fotodiode werd vervaardigd binnen deze dikke SG-Si laag. Donkerstroom van 100 µm x 100 µm grootte arrays zijn in de orde van 0,1 nA voor SG-Si fotodiodes met 1 µm, 1,5 µm en 2 µm intrinsieke regio lengte.
Voor de productie van 3D ICs met zowel het µ-Czochralski en PLEG proces wordt de front-end verwerking van elke actieve laag gedaan. Tot slot in een back-end proces, zullen alle apparaten in elke laag worden gecontacteerd en gemetalliseerd. Een vlak ontwerp van de actieve lagen is een sleutelelement in 3D-IC's. Er zijn twee methoden van planarisatie voorgesteld: CMP en SiO_2 terugets. Hoewel CMP een superieure uitkomst biedt, is het SiO_2 terugets proces eenvoudiger en schoner. Het is bewezen dat het µ-Czochralski proces zwak afhankelijk van de ongelijkmatigheden van de onderliggende lagen is. Het 3D IC fabricageproces voor PLEG blijkt vergelijkbaar te zijn met een 3D IC fabricageproces met het µ-Czochralski proces. Verticale stapeling van SG TFTs door het µ-Czochralski proces is met succes aangetoond. Gelijke elektrische eigenschappen tussen de bovenste en onderste transistoren bewijst dat de laser kristallisatie van de toplaagapparaten, de onderlaagapparaten niet beschadigen. De mobiliteiten zijn 159 en 565 cm^2/Vs voor de toplaag en 141 en 393 cm^2/Vs voor de onderlaag pMOS en nMOS apparaten respectievelijk. 3D omvormers zijn in staat om de volledige spanning bereik te hebben en tonen symmetrische spanningkenmerken. De kritische dimensie van de lithografie is een beslissende rol in het bepalen of het PLEG proces net zo efficint is als het µ-Czochralski proces. De Transistoren gemaakt op PLEG-Si laag vertonen een hoge mobiliteiten van 512 cm^2/Vs en 214 cm^2/Vs voor respectievelijk de nMOS en pMOS.

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List of Publications

Journal Publications

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- J. Derakhshandeh Kheljani, **M.R. Tajari Mofrad**, R. Ishihara, J. van der Cingel & C.I.M Beenakker "A study of the CMP effect on the quality of thin silicon films crystallized by using the μ-Czochralski process". *Korean Physical Society Journal*, 54(1), (2009) p. 432-436.

- **M.R. Tajari Mofrad**, A. La Magna, R. Ishihara, H. Ming, & C.I.M. Beenakker "A three-dimensional phase-field simulation of pulsed laser induced epitaxial growth of silicon", *Journal of Optoelectronics and Advanced Materials*, 12(3), (2010)701-706.

- J. Derakhshandeh Kheljani, N. Golshani, R. Ishihara, **M.R. Tajari Mofrad**, M. Robertson, T. Morrison, T & C.I.M Beenakker "Monolithic 3-D integration of SRAM and image sensor using two layers of single-grain silicon" *IEEE Transactions on Electron Devices*, 58(11), (2011) p. 3954-3961.

- Yoshifumi Nakamine, **M. R. Tajari Mofrad**, Michiel van der Zwan, Johan van der Cingel, Koichi Usami, Tetsuo Kodera, Ken Uchida, Yukio Kawano, Ryoichi Ishihara, and Shunri Oda "Laser Annealing of Silicon Nanocrystals Prepared by a Very High Frequency Plasma Deposition System", Submitted to Jpn. J. Appl. Phys.

- Ryoichi Ishihara, **M. R. Tajari Mofrad**, and C. I. M. Beenakker "Formation of thick, location-controlled grains by μ-Czochralski process", to be

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- R. Ishihara, J. Derakhshandeh, **M. R. Tajari Mofrad**, T. Chen, N. Golshani and C. I. M. Beenakker "Monolithic 3D-ICs with single grain Si thin film transistors", Solid-State Electronics 71, 80 (2012).

3. Ryoichi Ishihara, **M. R. Tajari Mofrad**, Ming He, and C. I. M. Beenakker "Elimination of defects in pulsed-laser-induced epitaxially grown silicon", to be submitted

Conferences & Workshops

- **M.R. Tajari Mofrad**, R. Ishihara, J. Derakhshandeh Kheljani, A. Baiano, A, Cingel, J. van der Cingel & C.I.M. Beenakker "Monolithic 3D integration of single-grain Si TFTs". *Material Research Society: Amorphous and polycrystalline thin-film silicon science and technology* (2008) pp. 1-4.

- **M.R. Tajari Mofrad**, J. Derakhshandeh Kheljani, R. Ishihara & C.I.M. Beenakker "Monolithic three-dimensional stacking of integrated circuits with a low-temperature process. *The annual workshop on semiconductor advances for future electronics and sensors*(2008) pp. 596-599

- J. Derakhshandeh Kheljani, **M.R. Tajari Mofrad**, R. Ishihara, J. van der Cingel & C.I.M Beenakker "Optimizing chemical mechanical polishing process in 3D-IC". *The annual workshop on semiconductor advances for future electronics and sensors* (2008) pp. 461-464.

- J. Derakhshandeh Kheljani, **M.R. Tajari Mofrad**, R. Ishihara, J. van der Cingel & C.I.M Beenakker "A study on CMP effect on the quality of thin silicon film characterized by micro czochraslki process with excimer-laser irradiation". *The proceeding of the 4th international TFT conference*(2008) pp. 327-330.

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- J. Derakhshandeh Kheljani, **M.R. Tajari Mofrad**, R. Ishihara & C.I.M Beenakker "Analog and digital output lateral photodiodes fabricated by - Czochralski process at low temperature" *Proceedings of 67th IEEE Device Research Conference* (2009) pp. 93-94

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Book subchapter

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