A 6.4 nW 1.7% Relative Inaccuracy CMOS Temperature Sensor Utilizing Sub-thermal Drain Voltage Stabilization and Frequency Locked Loop

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DOI
10.1109/LSSC.2020.3025962

Publication date
2020

Document Version
Accepted author manuscript

Published in
IEEE Solid-State Circuits Letters

A 6.4 nW 1.7% Relative Inaccuracy CMOS Temperature Sensor Utilizing Sub-thermal Drain Voltage Stabilization and Frequency Locked Loop

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***Abstract*— A 6.4 nW 1.7 % relative inaccuracy (R-IA) CMOS sub-thermal drain voltage-based temperature sensor is proposed. The proposed stabilized sub-thermal drain voltage current generator achieves a highly linear PTAT output without nonlinearity fitting or post-fabrication trimming, and increases the accuracy of the sensor. A combination of the current generator and a frequency-locked-loop relaxes the tradeoff between power and temperature stability of the current-to-frequency converter, and achieves supply-voltage-independent operation. Measured results of the prototype fabricated in a 65 nm CMOS process show that the proposed temperature sensor has a -1.0/+0.7 °C inaccuracy (= R-IA of 1.7 %) while achieving a resolution of 75 mK over a temperature range of -30 to 70 °C. The line sensitivity of the sensor is 2.8 °C/V.**

***Index Terms*— CMOS, low power, temperature sensor, temperature sensing, temperature-to-digital converter.**

I. Introduction

Temperature sensing is one of the typical applications in the Internet of Things (IoT). Recently, the demand for nW temperature sensors is increasing looking ahead to the expansion of energy-autonomous sensors utilizing sub-μW-power-level energy harvesters. Temperature sensing based on the sub-threshold current of MOSFET is attractive to realize ultra-low-power operations. These temperature sensors, however, tend to be less accurate compared with BJT based temperature sensors since they use nonlinear characteristics of the sub-threshold MOSFETs. [1] shows that a 570 nW current-to-frequency converter based fully integrated temperature sensor can achieve a relative inaccuracy (R-IA) of 1.5 % with the help of a fitting model. However, [1] requires off-chip processing for calculating a logarithm function and a nonlinearity fitting to compensate systematic nonlinearity. Although [2] presents a gate-leakage-based temperature sensor for achieving low energy performance, the utilization of gate-leakage current is limited by a fabrication technology. Besides, the temperature characteristic is nonlinear and additional nonlinearity fitting is required. [3] proposes a nonlinearity-fitting-free PTAT digital output temperature sensor based on sub-thermal drain voltage temperature sensing. However, the R-IA of the sensor is still over 2 % in the temperature range of -20 to 80 °C.

Our goal is to propose a nW temperature sensor that has a high accuracy covering a commercial temperature range of 0 to 70 °C. In this work, we report a 6.4 nW temperature sensor with an R-IA of 1.7 % in the range of -30 to 70 °C. To reduce the inaccuracy, we propose a new current generator topology that enhances the linearity of the PTAT output. Furthermore, we introduce a frequency locked loop (FLL) based current-to-frequency converter that improves both the power consumption and the tolerance to the supply voltage variation of the temperature sensor.

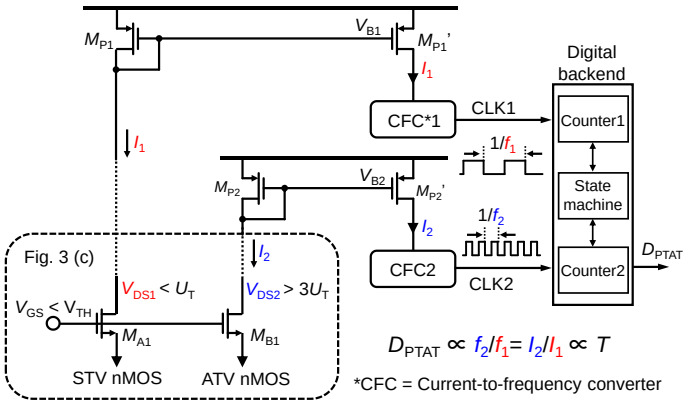

Fig. 1 Operation of proposed temperature sensor.

II. System Architecture

Fig. 1 shows the overall diagram of the proposed temperature sensor. The temperature sensing mechanism is based on the sub-thermal drain voltage temperature sensing [3]. A pair of MOSFETs (M_{A1} and M_{B1}) operating in the sub-threshold region are biased with two different V_{DS} values. A sub-thermal voltage (STV) that is lower than the thermal voltage U_T (= kT/q = 26 mV at 27 °C where k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge) is applied to V_{DS1} of M_{A1}, and above U_T voltage (ATV) that is higher than $3U_T$ is applied to V_{DS2} of M_{B1}. The ratio of I_2 to I_1 is expressed as

$$\frac{I_2}{I_1} = \frac{1}{1-\exp(\frac{-V_{DS1}}{U_T})} \approx \frac{U_T}{V_{DS1}} + C, \quad (1)$$

where C is a temperature-independent offset that can be removed from 1-point calibration. When V_{DS1} is sufficiently smaller than U_T, the current ratio I_2/I_1 can be approximated as a linear function of U_T/V_{DS1} that shows a PTAT characteristic. In Fig. 1, these two currents I_1 and I_2 are obtained from a current generator and converted into frequencies f_1 and f_2, respectively, by current-to-frequency converters (CFCs). f_2/f_1 shows the same PTAT characteristic as I_2/I_1. In the digital backend, two counters Counter1 and Counter2 count CLK1 and CLK2, respectively. Once the CLK1 is counted up to a pre-defined number

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LSSC.2020.3025962, IEEE Solid-State Circuits Letters

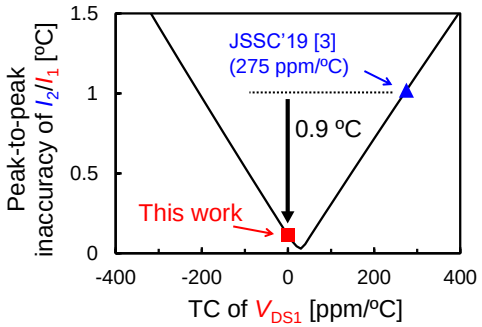

Fig. 2 Theoretical inaccuracy of sensor over -40 to 80°C calculated from I_2/I_1 as function of TC of V_{DS1} when V_{DS1} at -40 °C is 8 mV and 2-point calibration at -20 °C and 50 °C are performed.

N_{C1} (=2^{11} in this work), the value of Counter2 is latched as the output of the sensor (D_{PTAT}). Therefore, D_{PTAT} shows a PTAT characteristic as $D_{PTAT} = N_{C1} \times f_2/f_1 = N_{C1} \times I_2/I_1$.

As shown in eq. (1), V_{DS1} of M_{A1} must be temperature-independent since the temperature dependency of V_{DS1} decreases the linearity of I_2/I_1. Fig. 2 shows a theoretical inaccuracy of the sensor in the temperature range of -40 to 80 °C calculated from eq. (1) when V_{DS1} is set as 8 mV at -40 °C and the temperature coefficient (TC) of V_{DS1} is defined from a 1st order approximation. The analysis shows the inaccuracy of I_2/I_1 increases due to the TC of V_{DS1}. In [3], V_{DS1} does not settle to a constant voltage due to the inherent temperature dependence of the current generator and has a TC of 275 ppm/°C which results in a peak-to-peak inaccuracy of 1.0 °C. In this work, we propose a new current generator topology that improves the linearity of I_2/I_1 by keeping V_{DS1} temperature independent.

III. Proposed Temperature-to-Digital Converter

A. *Stabilized Sub-thermal Drain Voltage Current Generator*

Fig. 3 (a) shows the basic concept of the current generator for generating I_1. To ensure a fixed ΔV value across M_{A1}, a local feedback-loop composed of an op-amp and a transistor M_R is used. The challenge of the topology is to ensure that V_{DS1} is regulated to $\Delta V = 8$ mV, precisely. Since the input voltage of the op-amp is just 8 mV, a typical op-amp does not provide a sufficient gain of the feedback loop. One straight forward way to solve this problem is to apply voltage level shifters into the input of the op-amp to convert the voltage level of the input pair. However, it consumes a static current and results in additional power consumption. Another challenge of Fig. 3 (a) is reducing the offset voltage of the op-amp V_{OS}. Since V_{OS} directly shows up in V_{DS1}, it must be much smaller than $\Delta V = 8$ mV for ensuring the sensitivity of I_2/I_1. Also, the TC of V_{OS} reduces the linearity of I_2/I_1 and increases the inaccuracy of the sensor. For example, the offset voltage of a typical sub-threshold op-amp [4] has TC of 2.5 µV/°C (= 312 ppm/°C when ΔV is 8 mV), which causes a theoretical inaccuracy of 1.2 °C in Fig. 2. To cancel the offset, we need a technique such as auto-zero or chopping. These techniques, however, increase the power consumption of the sensor because of the additional circuit blocks and clock sources.

Fig. 3 (b) shows the concept of the proposed stabilized sub-thermal drain voltage current generator. $N\Delta V$ where $N = 20$ in our design is applied to the negative input of the op-amp. V_N is divided by the voltage divider and the effect of V_{OS} on V_{DS1} is reduced to V_{OS}/N. In this way, the inaccuracy of V_{DS1} due to the offset of the op-amp is improved without using auto zero or chopping techniques. Furthermore, the level shifters are not required because the input voltage level of the op-amp is $N\Delta V$ = 160 mV which provides a sufficient loop gain of the feedback. Fig. 3 (c) shows the schematic of the proposed current generator. In the current generator, I/O transistors

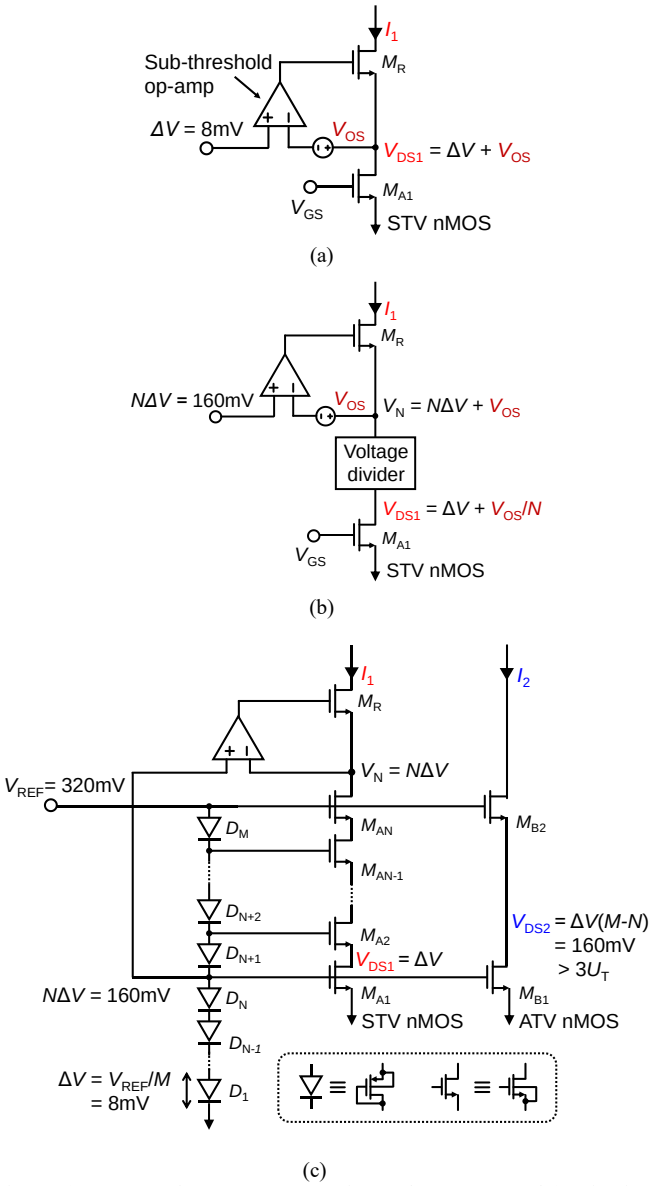

Fig. 3 (a) Concept of current generator for I_1. (b) Concept and (c) circuit schematic of proposed stabilized sub-thermal drain voltage current generator.

are used to reduce the gate-leakage of the MOSFETs. A reference voltage V_{REF} of 320 mV is divided by a voltage divider composed of M (= 40) diodes to generate ΔV of 8 mV. A feedback-loop composed of a sub-threshold op-amp and M_R whose loop gain is over 60dB is applied to regulate the drain node of M_{AN} (V_N) to $N\Delta V$ ($N = 20$ in our design). V_N is divided by the stacked devices (M_{A1} to M_{AN}) and V_{DS1} is stabilized at ΔV. Although the op-amp has a temperature-dependent offset voltage V_{OS}, the stacked transistors M_{A1} to M_{AN} divide V_{OS} and reduce its effect on V_{DS1}. To confirm the performance of the current generator, simulated V_{DS1} at each process corner is shown in Fig. 4 (a). The TC of V_{DS1} is reduced to less than 1 ppm/°C which results in 0.1 °C peak-to-peak inaccuracy in Fig. 2. The fixed offset of V_{DS1} is a negligibly small value of 0.5 µV. Since the process variation in the voltage dividers and stacked transistors affect the TC of V_{DS1}, a 1000-times Monte Carlo simulation is performed for the entire current generator. The TC of V_{DS1} is calculated from the slope of V_{DS1} at 60 °C. The TC at the ±σ variation is simulated as ±28 ppm/°C as shown in Fig. 4 (b). This result shows that the inaccuracy of I_2/I_1 is only 0.47 °C in Fig. 2 even under the condition that the fabricated chip suffers from a severe ±3σ random mismatch. Similar simulations are performed at

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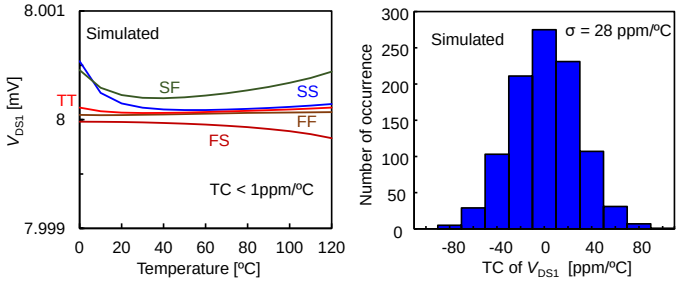


(a) (b)

Fig. 4 (a) Simulated V_{DS1} of proposed current generator at each process corner. (b) TC of V_{DS1} obtained from 1000 times Monte-Carlo simulation.

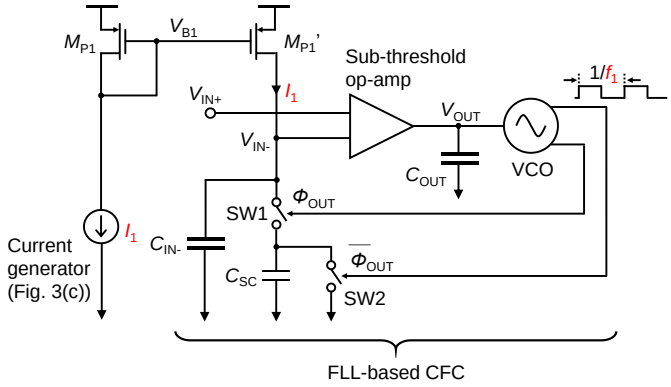


Fig. 5 Circuit schematic of current-to-frequency converter combined with proposed current generator.

0 °C and 120 °C. The σ are 42 ppm/°C and 22 ppm/°C, respectively. The worst ±3σ is expected to be 0.66 °C.

B. *FLL-based Current-to-Frequency Converter*

In Fig. 1, the CFCs convert I_1 and I_2 into f_1 and f_2, respectively. A relaxation oscillator utilizing a comparator is a typical CFC used in many types of sensors [3]. However, the comparator has a temperature-dependent propagation delay which decreases the linearity of f_2/f_1. As a result, the power consumption of the comparator must be increased to improve temperature stability by reducing the propagation delay. To improve the power consumption of the CFCs, the proposed temperature sensor utilizes an FLL [4] that do not require power-consuming comparators. At the same time, temperature and supply voltage independent current-to-frequency conversion is also achieved.

Fig. 5 shows the block diagram of the proposed temperature-to-digital converter for f_1. The current generator shown in Fig. 3 (c) is combined with the FLL [4]. f_2 can be obtained similarly by simply replacing I_1 into I_2. In the FLL, SW1, SW2, and C_{SC} (=120fF) configure a switched capacitor resistor. I_1 generated in the current generator is copied by a current mirror composed of M_{P1} and M_{P1}' and flows through C_{SW}. The closed-loop system composed of a sub-threshold op-amp, a VCO, and the switched capacitor composes negative feedback and forces V_{IN-} to be matched to V_{IN+}. As long as the loop gain is sufficiently large, the output frequencies of the FLLs are expressed as $f_1 = I_1/C_{SC}V_{IN+}$ in CFC1 and $f_2 = I_2/C_{SC}V_{IN+}$ in CFC2, respectively. The ratio of f_2/f_1 shows the same PTAT characteristic as I_2/I_1 and is irrelevant to V_{DD}. In this design, V_{REF} is reused as V_{IN+}. C_{OUT} works as a loop filter to ensure the stability of the loop and remove the ripple on V_{OUT}. C_{OUT} of 100 pF is implemented to reduce the cutoff frequency to ~ Hz. Moreover, C_{IN-} of 6.3 pF is implemented to attenuate the ripple on V_{OUT} to less than 10 µV. At room temperature, the lock frequencies are 2.7 kHz for CFC1 and 10 kHz for CFC2. The gains of the VCOs are 73 k/Hz and 263 k/Hz, respectively. The gain of the amplifier is 60 dB.

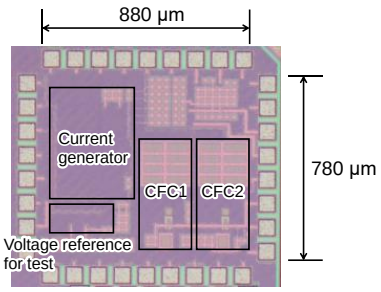
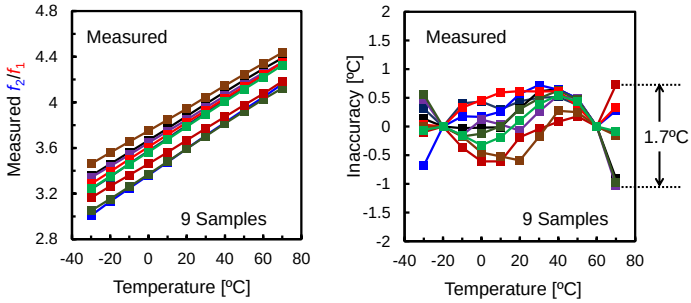
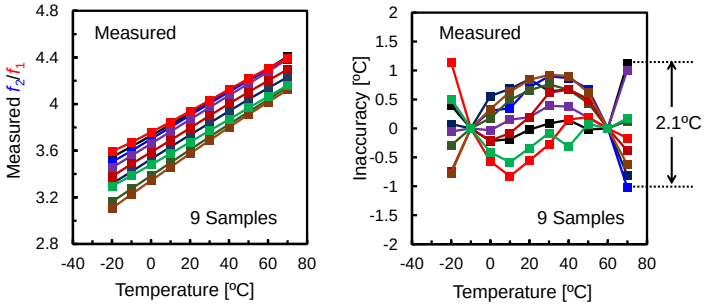


Fig. 6 Prototype of proposed temperature sensor.



(a) (b)

Fig. 7 (a) Measured f_2/f_1 and (b) inaccuracy of temperature sensor after 2-point calibration when external V_{REF} = 320 mV is applied.



(a) (b)

Fig. 8 (a) Measured f_2/f_1 and (b) inaccuracy of temperature sensor after 2-point calibration when on-chip V_{REF} is used.

Since the finite output impedances of M_{P1} and M_{P1}' in the current mirror increase the V_{DD}-dependence of the sensor, a cascode current mirror is applied by stacking an additional current mirror. The simulated output impedances are over 330 GΩ. The current variations of I_1 and I_2 due to the V_{DD} variation from 0.75V to 1.05V are less than 0.2 %. The size of M_{P1} and M_{P1}' are increased to L = 0.4 µm and W = 240 µm to reduce the effect of the mismatches in the current mirrors. When there are mismatches in the current mirrors, the worst spread of the inaccuracy is σ = 24mK after 2-point calibration in a Monte-Carlo simulation in the temperature range of 0 to 120 °C.

Thanks to the FLL-based CFC topology, power-consuming comparators are removed from the CFCs and the tradeoff between the power consumption and the temperature stability is relaxed.

IV. Measurement Results

The proposed temperature sensor is fabricated in a 65-nm LP CMOS process that provides low leakage devices. In this work, the digital backend including an 11-bit counter and 15-bit counter is implemented externally. The power consumption of the digital block is obtained from a SPICE simulation. The LSB and the RMS resolution of the D_{PTAT} at 20°C are 43.7 mK and 75.2 mK when CLK1 is counted up to 11-bit by Counter1. Fig. 6 shows a chip photograph of the proposed temperature sensor. The core area of the sensor is 0.32 mm^2. First, to measure the accuracy of the core of the temperature sensor, a reference

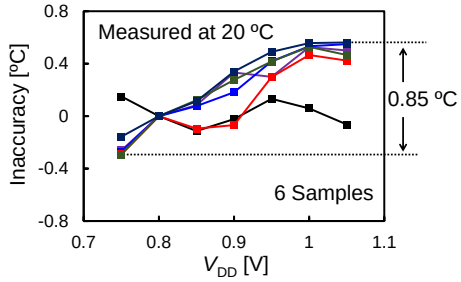


Fig. 9 V_{DD} dependence of temperature sensors.

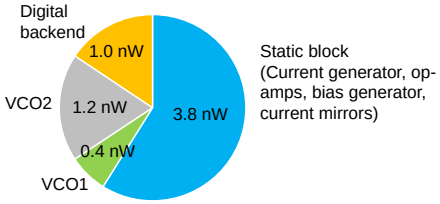


Fig. 10 Breakdown of power consumed in temperature sensor.

voltage of 320 mV is applied externally. Fig. 7 (a) and (b) show the measured f_2/f_1 and the inaccuracy of the temperature sensor for 9 samples. After a 2-point calibration, the peak-to-peak inaccuracy is -1.0/+0.7 °C in the temperature range of -30 to 70 °C (= 1.7% R-IA). For applications that cannot provide the reference voltage, a CMOS voltage reference [8] is implemented on the same chip. The measured power consumption of the voltage reference is 2.2 nW. Fig. 8 (a) and (b) show f_2/f_1 and the inaccuracy for 9 samples when the voltage reference is applied to the sensor. After a 2-point calibration, the peak-to-peak inaccuracy is -1.0/+1.1 °C in the temperature range of -20 to 70 °C (= 2.3% R-IA). With the voltage reference, the spread and temperature dependence of V_{REF} limit the minimum operating temperature to -20 °C and deteriorate the R-IA. We think this can be improved by applying an individual calibration to the voltage reference [9]. Fig. 9 shows the V_{DD}-dependence of the temperature sensor at 20 °C among 6 samples. The inaccuracy is 0.85 °C when V_{DD} varies from 0.75 to 1.05 V. The calculated line sensitivity is 2.8 °C/V. Fig. 10 shows the breakdown of the power consumption of the temperature sensor at room temperature of 20 °C. When the power supply is 0.8 V, the total power consumption is 6.4 nW. VCO1 and VCO2 are the VCOs in CFC1 and CFC2 whose operating frequencies are 2.7 kHz and 10 kHz, respectively. The power consumption of the analog part is 5.4 nW while the simulated power of the digital back-end is 1.0 nW. The low power operation of the digital part is achieved thanks to its simple implementation and low voltage, low frequency operation.

Table I summarizes the performance of the proposed and conventional temperature sensors. We select the state-of-the-art MOSFET based nW temperature sensors that cover the commercial temperature range of 0 to 70 °C. The proposed temperature sensor achieves 1.7 % R-IA without any nonlinearity fitting or post-fabrication trimming. Furthermore, the line sensitivity is reduced to 2.8 °C/V.

V. Conclusions

In this work, a 6.4 nW 1.7 % R-IA sub-thermal drain voltage-based temperature sensor is proposed. The proposed stabilized sub-thermal drain voltage current generator improves the accuracy of the sensor by increasing the linearity of the PTAT output. Furthermore, the combination of the current generator and FLL based current-to-frequency converter relaxes the tradeoff between the power consumption and the temperature stability of the sensor, and improves the tolerance to V_{DD} variation. The measured results of the fabricated chip in a 65-nm CMOS process show that the sensor consumes 6.4 nW while achieving an R-IA of 1.7 % in the temperature range of -30 to 70 °C without any off-chip nonlinearity fitting or post-fabrication trimming. The measured resolution and the line sensitivity are 75 mK and 2.8 °C/V, respectively.

TABLE I. Comparison with Previously Published nW MOSFET-Based Temperature Sensors

	This work	JSSC'19 [3]	JSSC'19 [6]	JSSC'14 [5]	CICC'19 [2]
Sensing principle	**Stabilized Sub-U_T**	Sub-U_T	3-transistor PTAT	2-transistor PTAT	Gate leakage
CMOS process [nm]	65	180	65	180	65
Off-chip nonlinearity fitting	**No**	No	No	No	Yes
Calibration point	2	2	2	2	2
Inaccuracy [ºC] (# of samples)	**-1.0/0.7** (9)	-0.9/1.2 (9)	-1.5/1.6 (12)	-1.4/1.5 (18)	-2.7/1.8 (7)
Relative Inaccuracy [%]	**1.7**	2.1	3.1	2.9	3.8
Temp. range [ºC]	-30 ~ 70	-20 ~ 80	0 ~ 100	0 ~ 100	-20 ~ 100
Resolution [mK]	**75**	145	300	300	250
Power [nW]	6.4	11	0.76	71	0.64
Energy/conversion [nJ]	4.9	8.9	0.23	2.2	0.022
Resolution FoM*1 [nJ·K²]	**0.027**	0.19	0.020	0.19	0.0014
Line sensitivity [ºC/V] (# of samples)	**2.8** (6)	3.8 (5)	8.4 (13)	14 (1)	N/A
Area [mm²]	0.32	0.074	0.63	0.09	0.013

*1 Resolution FoM = (Energy/Conversion) × (Resolution)² [7]

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