

## Solution-processed polycrystalline silicon on paper

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Printing electronics has led to application areas which were formerly impossible with conventional electronic processes. Solutions are used as inks on top of large areas at room temperatures, allowing the production of fully flexible circuitry. Commonly, research in these inks have focused on organic and metal-oxide ink materials due to their printability, while these materials lack in the electronic performance when compared to silicon electronics. Silicon electronics, on the other hand, has only recently found their way in solution processes. Printing of cyclopentasilane as the silicon ink has been conducted and devices with far superior electric performance have been made when compared to other ink materials. A thermal annealing step of this material, however, was necessary, which prevented its usage on inexpensive substrates with a limited thermal budget. In this work, we introduce a method that allows polycrystalline silicon (poly-Si) production directly from the same liquid silicon ink using excimer laser irradiation. In this way, poly-Si could be formed directly on top of paper even with a single laser pulse. Using this method, poly-Si transistors were created at a maximum temperature of only 150 °C. This method allows silicon device formation on inexpensive, temperature sensitive substrates such as polyethylene terephthalate, polyethylene naphthalate or paper, which leads to applications that require low-cost but high-speed electronics.

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Printing electronics has aroused great interest in recent years in view of the low-cost manufacturability of electronic devices as well as the simplicity when compared to conventional device processing methods that require lithography and vacuum systems. Semiconductors printed as inks on arbitrary substrates have led to applications that were formerly impossible such as rollable displays or flexible bio-sensing systems. Semiconducting inks commonly researched in this field are organic and metal-oxide semiconductors. 1-6 These materials have also found their way on paper substrates by using low temperature fabrication methods.<sup>7–9</sup> These semiconductors, however, lack in their field-effect mobilities and reliability when compared to silicon. Silicon inks have also been investigated in recent years using cyclopentasilane (CPS); a silicon precursor which is liquid at room temperature and can transform into solid silicon by curing the ink to a polysilane and CPS sol-gel with ultraviolet (UV) light, causing the CPS ring-molecules to open and connect end-toend. <sup>10</sup> The polysilane chains cross-link with each other when heated to a temperature of at least 350 °C forming hydrogenated amorphous silicon (a-Si:H). A following excimer laser irradiation can transform the amorphous silicon (a-Si) film into polycrystalline silicon (poly-Si), a common method for silicon crystallization. Using this silicon ink, a-Si solar cells have been created, 11 as well as poly-Si thin-film transistors (TFTs) with mobilities that were more than 100 times higher than TFTs made from organic and metal-oxide inks. 10-13 By essentially using silicon as the base material, other advantages arise such as stability, knowledge of the material, and low-power consumption by being able to create

complementary metal-oxide semiconductor (CMOS) circuitry, which is often a challenge with the other ink materials. This silicon ink requires an annealing temperature of at least 350 °C in order for the polysilane gel to cross-link sufficiently, 14 which is too high to be used on low-cost flexible substrates that have a low thermal budget such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN) or paper. Lower temperatures result in insufficient cross-linking and lead to oxidation of the ink. This cross-linking energy of polysilane needs to be provided in a different way that would not harm an underlying substrate.

In this work, we show a direct transformation of the polysilane, produced by the CPS silicon ink, to poly-Si by using an excimer laser treatment instead of an intermediate a-Si formation step and therefore omitting the thermal annealing process. By avoiding the thermal annealing step, inexpensive substrates with a low thermal budget can now be used. The excimer laser is a good alternative, since the pulse-duration is only in the range of nanoseconds, which would limit the heat diffusion.

TFTs have been fabricated using this method at a maximum temperature of 150 °C. Inexpensive, biodegradable, recyclable, and flexible silicon devices can now be fabricated, and different applications will arise such as ultrahighfrequency RFID tags (UHF-RFID), low-cost flexible sensors, or trillions of sensor-nodes communicating with each other in an Internet of Things system.

CPS has been coated onto a target substrate using a doctor-blade, inside a contained environment with low oxygen and water levels ( $O_2 < 0.1$  ppm and  $H_2O < 0.1$  ppm). The film has then been polymerized in 365 nm UV light and subsequently exposed to a XeCl excimer laser (308 nm and 28 ns). The thickness of the final film is approximately 200 nm.

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Depending on the irradiation-recipe used for the excimer laser treatment, different types of solid silicon could be created from polysilane. Multiple low energy density pulses have led to a-Si, whereas slightly higher energy density pulses to microcrystalline silicon ( $\mu$ c-Si). Even a single higher energy pulse led to poly-Si. The film changes color from transparent to light brown associated with the bandgap narrowing of the semiconductor. The transformations were confirmed by Raman spectroscopy (Figures 1(a)–1(c)). Transmission electron microscopy (TEM) images were taken from the single shot and multishot films (Figures 1(d) and 1(e)). These images show that grains as large as 150 nm could be obtained with even a single excimer laser pulse of 300 mJ/cm<sup>2</sup> directly from polysilane.

Although polysilane is reactive to oxygen and water, the EDS results taken inside the formed grains even after exposing the film to open air for several days do not show any sign of oxygen levels at the corresponding 0.5 keV mark (Figure 1(f)). This adds to the notion that the film is fully transformed.

The film has been treated on top of paper (PowerCoat®HD). 15 Forming electronic devices on paper generally brings issues in device performance due to porosity and roughness of the substrate. The paper used in this work,

however, has been optimized for these types of printing processes and have a significantly lower root mean square (RMS) roughness of <20 nm, confirmed with atomic force microscopy (AFM). The RMS roughness of the polysilane film formed on top of this substrate resulted in approximately 130 nm, comparable to the roughness of the film when formed on top of a silicon substrate. The effects of roughness and porosity of this paper on our devices are therefore expected to be marginal.

Figure 1(g), the backside of the paper, is shown to be unharmed and the change in color is clearly observed in Figure 1(h), representing the crystallized silicon film. Stability of the film has been verified by measuring the Raman spectrum after 9 months of leaving the film in open air. A clear poly-Si peak at 522 cm<sup>-1</sup> was found (Figure 1(i)).

The TFTs fabricated in this work have been conducted on top of a silicon substrate with 850 nm plasma-enhanced chemical vapor deposition (PECVD) SiO<sub>2</sub> from tetraethyl orthosilicate (TEOS) deposited on top as a rigid base for the ease of handling. With this method, other more temperature sensitive substrates however could be used. After the cyclopentasilane ink is cured and crystallized, the resulting film

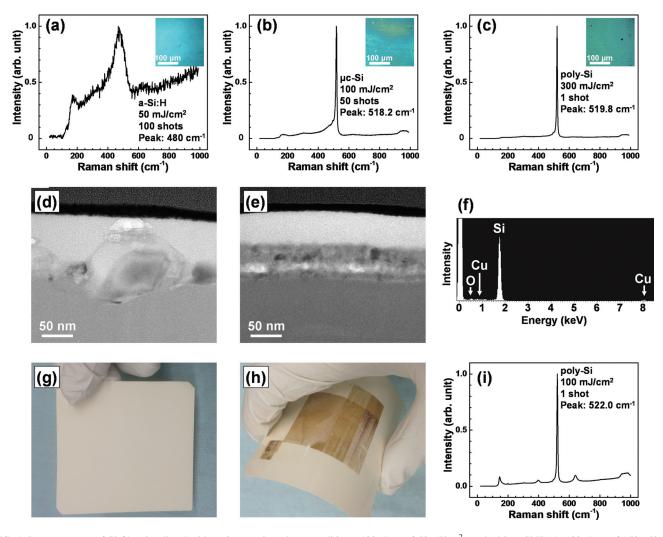


FIG. 1. Raman spectra of Si films irradiated with various excimer laser conditions. 100 shots of  $50\,\text{mJ/cm}^2$  resulted in a-Si:H (a), 100 shots of  $150\,\text{mJ/cm}^2$  resulted in  $\mu$ c-Si (b), and 1 shot of  $300\,\text{mJ/cm}^2$  led to poly-Si (c). TEM images of Si grain formation for a single shot  $(300\,\text{mJ/cm}^2)$  (d) and multiple shot  $(25\,\text{shots of }25\,\text{mJ/cm}^2)$  (e) recipe. Energy dispersive spectroscopy results of the Si grains observed in the TEM images (f). Picture of poly-Si on paper. Unharmed backside of the paper after excimer laser annealing (g). Poly-Si (brown) found on paper (h). Raman spectroscopy results of the poly-Si after nine months; the result corresponds to poly-Si (i).

is a stable solid material and could be used in following lithography steps. The TFT channel is patterned in the transformed poly-Si surface by dry-etching. 50 nm of SiO<sub>2</sub> has been deposited by atomic layer deposition (ALD) at a 100 °C using H<sub>2</sub>Si[N(C<sub>2</sub>H<sub>5</sub>)<sub>2</sub>]<sub>2</sub> as the Si precursor gas. An Al/Si (99%/1%) gate has been deposited by sputtering at 50 °C and patterned by dry-etching. This gate is then used to block part of the ions that are accelerated toward the channel surface for doping purposes. This leads to self-alignment of the source and drain regions with respect to the gate. The implanted ions are annealed using excimer laser irradiation pulses (150–200 mJ/cm<sup>2</sup>). Contact openings are produced inside the gate oxide film for reaching the

source and drain surfaces. Again Al/Si (99%/1%) has been sputtered at 50 °C and patterned to form source and drain electrodes. Note that there is no passivation oxide introduced. The whole device fabrication process has not exceeded a maximum temperature of 150 °C for the substrate. Moreover, the maximum temperature has not been reached by the transformation process of CPS to poly-Si, but comes from photoresist baking in lithography procedures. The full schematic of the process and TFT structure has been illustrated in Figure 2(a).

Negative and positive MOS devices (NMOS and PMOS) have been constructed with channel lengths and widths of only 1, 2, and 4  $\mu$ m, and a comparison has been

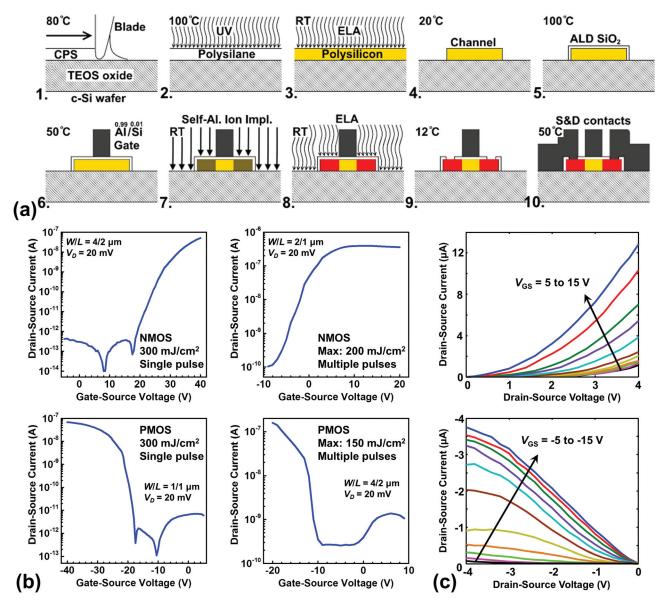


FIG. 2. (a) Low temperature fabrication schematic: in step 1, CPS is coated on the  $80\,^{\circ}$ C heated substrate by a doctor blade. Step 2: the CPS is polymerized using a UV source at  $100\,^{\circ}$ C. Step 3: the excimer laser irradiation crystallizes the polysilane directly into poly-Si. Step 4: the transistor channels are etched. Step 5:  $SiO_2$  gate oxide is deposited using ALD at  $100\,^{\circ}$ C. Step 6: the gate metal Al/Si is deposited at  $50\,^{\circ}$ C and etched at  $25\,^{\circ}$ C. Ion implantation and conducted at room temperature in step 7 and dopant ion activation using excimer laser at room temperature in step 8. In step 9, the oxide is removed and in step 10, the contacts are deposited and etched at  $50\,^{\circ}$ C and  $25\,^{\circ}$ C, respectively. Consequently, the maximum process temperature is a  $150\,^{\circ}$ C from the lithography process. (b) Transfer characteristics of the NMOS and PMOS poly-Si TFTs both crystallized with a single excimer laser shot of  $300\,\text{mJ/cm}^2$ , and of the NMOS and PMOS of multiple laser irradiated TFTs: 20 shots of 25, 50, 75, 100, and 200 for the NMOS and 1 shot of 25, 50, 75, 100, and 20 shots of  $150\,\text{mJ/cm}^2$  for the PMOS. All measurements were conducted with a drain voltage of  $20\,\text{mV}$ . For the single shot devices, the gate voltage has been swept in the off direction prior to measurement. (c) Output characteristics of the PMOS (bottom) and NMOS (top) devices. Both exposed with multiple laser shots. The gate voltage was varied from -5 to  $-15\,\text{V}$  and 5 to  $15\,\text{V}$  for the p-type and n-type transistors, respectively. For single-shot devices, similar output characteristics were obtained.

TABLE I. Summary of single and multiple excimer laser irradiated PMOS and NMOS device properties.

	Single shot PMOS	Single shot NMOS	Multishot PMOS	Multishot NMOS
$\mu_{FE}$ (cm <sup>2</sup> /Vs)	3.9	2.6	23.5	21.0
$V_{th}\left(\mathbf{V}\right)$	-21	30	-11.2	-1.5
S (mV/dec)	341	363	1017	1968
$I_{on}/I_{off}$	10 <sup>4</sup>	$10^{4}$	$10^{2}$	10 <sup>3</sup>

made between those that have been irradiated with a single excimer laser pulse, and those with multiple pulses. Transfer properties of both types of devices were analysed (Figure 2(b)). Single pulse devices were irradiated with a laser energy density of 300 mJ/cm<sup>2</sup>, whereas multiple pulse devices did not exceed a laser energy density of 200 mJ/cm<sup>2</sup>. The summary of the results is given in Table I. For the single pulse devices, charge carrier mobilities of 2.6 and 3.9 cm<sup>2</sup>/Vs were obtained, whereas multiple pulse devices reached mobilities of 21.0 and 23.5 cm<sup>2</sup>/Vs for the NMOS and PMOS devices, respectively. Although mobilities were found to be higher for the multiple pulse devices, the subthreshold slope and the on/off current ratio were better in the single pulse case. An analysis to the difference in device performance could be explained from the TEM images of Figures 1(d) and 1(e). Due to the limited number of grain boundaries and therefore less interface-trap states in the single pulse case, the subthreshold slope decreases and the on/ off current increases. As more pulses are irradiated on the film, the surface roughness decreases, and the maximum obtainable mobility for a material decreases due to smaller grains. The obtained mobilities were comparable to conventional poly-Si TFTs.

Output properties of the devices show common transistor behaviour (Figure 2(c)). However, current crowding can be observed near the origin. High parasitic resistances in the source and drain regions cause the curves to deviate from the ideal. Process conditions can be optimized by various parameters such as doping concentration, excimer laser irradiation conditions for both crystallization as well as dopant laser activation, ALD oxide deposition, and passivation oxide.

In summary, we have introduced a method of creating poly-Si from Si ink cyclopentasilane that can be used to form poly-Si directly on low-temperature substrates such as paper. This is done by exposing cured cyclopentasilane directly to excimer laser pulses, which would omit both the thermal step formerly necessary at 350 °C as well as an intermediate transformation to a-Si. This method has been used in the creation of NMOS and PMOS TFTs with mobilities of 21.0 and 23.5 cm<sup>2</sup>/Vs, respectively, at a process temperature of only 150 °C. This technique allows silicon to be directly integrated on inexpensive substrates for applications such as low-cost UHF-RFID tags.

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