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From 2D Lithography to 3D Patterning

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Lithography as developed for IC device fabrication is a high volume high accuracy patterning technology with strong 2 dimensional (2D) characteristics. This 2D nature makes it a challenge to integrate this technology in a 3 dimensional (3D) manufacturing environment. This article addresses the performance of a waferstepper (ASML PAS5000) in several 3D processes ranging form waferbonding and thinning to dual side processing with through silicon vias (TSV). Four different generic expose/etch strategies are discussed to fabricate vertical micro sieves, vertical through wafer silicon plate springs, dual side interconnect with TSV and vertical electrodes in deep silicon channels. It is concluded, that despite the 2D nature of advanced waferstepper lithography a wide range of 3D structures can be fabricated. The multi point alignment capabilities of a waferstepper can improve the overlay in several 3D manufacturing processes and the high accuracy alignment system can be used as a metrology tool for further development of 3D integration processes.

Introduction

The trend to further integrate and miniaturize MEMS and electronic systems generates the need to improve the diverse manufacturing technologies for 3-Dimensional (3D) micro fabrication, 3D-integration, advanced wafer level packaging (WLP) etc. Miniaturization has proven to be a very successful strategy in integrated circuit (IC) technology, which evolved into a high accuracy mass production technology, and capable to integrate more than 10^8 transistors in one planar system. It is therefore likely that advanced MEMS and other 3 dimensional (3D) integration and micro fabrication technologies will also employ this successful planar manufacturing approach.

The key technology in miniaturization is lithography and tools like wafersteppers, originally developed for early CMOS downscaling are nowadays integrated in the MEMS and 3D process lines. However, lithography as it is optimized for IC technology has a strong 2D nature. After all, the IC fabrication process flow comprises a sequence of stacking many virtually 2 dimensional (2D) high precision process layers. The layout of each layer is designed in terms of XY positions and dimensions, defining either opaque or transparent areas; a binary mask. The 3rd dimension (Z) is usually not coded on the mask and the substrate topography is expressed in nm rather than in μm.

Exposure tool requirements for 3D device fabrication

In 3D processing, there is no common manufacturing technology, dual side processing is customary, substrate topography can be several 100 μm and resist films are sometimes very thick, leading to long exposure and development times etc. Therefore, the

lithographic requirements for 3D micro fabrication are more diverse. The main consequences of this diversity for alignment and exposure are discussed below.

Alignment and Overlay. Contrary to IC fabrication, in 3D micro fabrication, the alignment plane and imaging plane are no longer confined in one 2D XY plane. A thick resist layer or process layer implies that the alignment plane and image plane are separated by a distance ΔZ perpendicular to the XY plane. Furthermore, many 3D micro fabrication processes require dual side processing with front to back alignment (FTBA) capabilities. Therefore FTBA hardware in the form of infra red alignment or additional optics is an almost indispensible option on 3D exposure tools.

The alignment system measures the position of an alignment marker relative to a corresponding marker on the photomask. Generally it is an optical process for which the accuracy is determined by the system and marker characteristics. The alignment results on each marker are used to establish an exposure grid over the wafer in which the exposure locations can be defined. Minimal two points are required to define the grid, but obviously with more points, the exposure grid is more precisely defined. This will result in a better overlay. Overlay, the result of an alignment-exposure-development process, is one of the key benchmarks for a lithographic process.

The alignment process in contact aligners is based on conventional optics and pattern recognition [1] thus the alignment performance depends on the optical quality of the marker images. Alignment accuracies of 0.1 μm are reported [2]. For FTBA an overlay accuracy of 0.5 μm (3sigma) is reported [1]. However, alignment on a contact aligner is a two-point alignment and does not compensate for non-uniform mask or wafer distortions, non-linear wafer distortion etc.

The overlay accuracy for front side processing on an advanced waferstepper is much better than 100 nm. The FTBA overlay accuracy is usually less accurate, for an ASML PAS5500 waferstepper, 200 nm (3σ) is specified [3]. Although wafersteppers are not designed for alignment on non-planar 3D like substrates it is shown that a waferstepper alignment system, based on phase gratings is fully functional in a wide range of processes used in 3D device fabrication. On an ASML PAS5000 waferstepper, used in this work, an overlay accuracy of 0.3 μm (3σ) or better was obtained in processes with 500 μm out-of-focus alignment [4].

Exposure. For contact aligners, the resolution for proximity printing is limited to about 2 μm [5]. However with vacuum contact printing, a resolution of 200 nm lines / 800 nm spaces is reported [6]. With specially designed illumination optics, contact aligners are capable to resolve 30 μm lines/spaces at a mask-substrate distance of 500 μm [7], a valuable asset for 3D patterning. Furthermore, the whole wafer is exposed in one single step, which is particularly useful for exposures in thick resist

Projection aligners like wafersteppers and waferscanners are the industries workhorses. A high end projection aligner like a waferscanner can print features down to 32 nm, but high resolution projection aligners have a very low depth of focus (DOF) [8], not a very good property for patterning 3D structures. Even for a typical I-line projection aligner with a resolution of 500 nm the DOF is limited to 1-2 μm. Nevertheless, to employ the superior imaging characteristics on high topography substrates, existing I-line wafersteppers are equipped with novel exposure technologies like multi step imaging (MSI) [9]. This feature allows the independent control of exposure dose and focus offset enabling more control over the resist profile in thick resist films.

Not only early generation wafersteppers are being converted and used for 3D processing, already for more than a decade, dedicated wafersteppers with broadband illumination in combination with low numerical aperture lens design [10] are available. This design combines both enhanced throughput and DOF compared with conventional I-line steppers. Throughput is an issue, particularly when imaging in thick conventional I-line photoresist films. But nowadays, chemically amplified photo-resist (CAR), sensitive for I-line exposure are available. CAR like SU-8 [11], NR44 [12] (both negative tone) or SIPR7120 [13] (positive tone) requires much lower exposure energies compared with conventional I-line photoresist, providing an interesting alternative.

From 2D to 3D.

For 3D micro fabrication, the 2D mask layout is transferred into a 3D device layer by lithography and subsequent subtractive processing, like etching, or additive processing like plating [14]. In some cases, the final resist pattern itself is a functional device layer [15]. Examples are the use of gray scale lithography [16] to fabricate cost effective TSV (figure1a) and HAR electrodes in micro fluidic channels [17] a potential candidate to fabricate chip to wafer (C2W) interconnects (figure 1b).

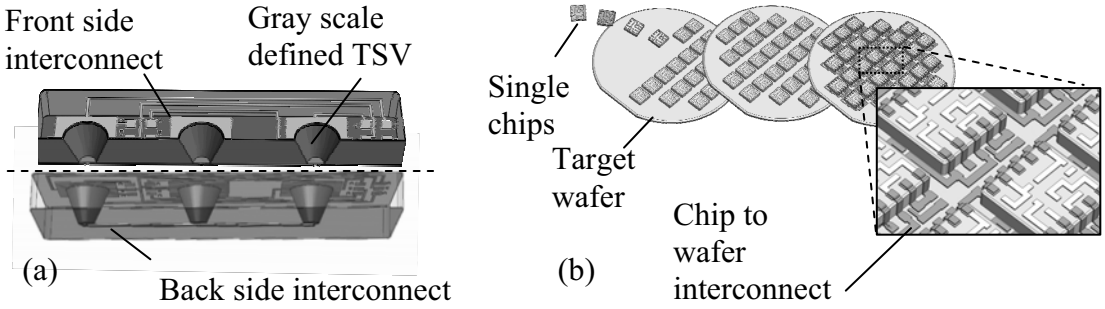

Figure 1. Dual side interconnect with tapered vias using gray scale lithographic processing (a) and a potential application of MEMS sidewall electrodes in C2W interconnect (b).

The 3D device architecture and its associated substrate topography, determines to a large account which align and exposure strategy must be used for optimal result. Furthermore, the post-litho process, used to convert the 2D pattern into 3D structures may contribute to or even dominate the overlay errors in the resulting 3D structure. Besides that, handling of wafers with high aspect ratio (HAR) structures, thin membranes etc. remain an issue. Consequently different alignment, expose and etch strategies may be required for a successful fabrication of 3D structures. The technologies used for 3D integration MEMS and other micro fabrication technologies are very diverse and today, no clear litho requirements and roadmaps are defined.

The main consequences of 3D processing for alignment/overlay and expose/develop/etch are discussed in 3 sections. The section below: *Overlay characterization* discuses the basic overlay measurement principles and 3D consequences herein. The next section, *Alignment and overlay case studies* will discuss three examples of 3D processing; wafer to wafer (W2W) bonding, thick film processing and TSV processing. The overlay performance of an ASML PAS5000 waferstepper is evaluated in all examples and general conclusions for waferstepper alignment strategies are being discussed.

Finally, the section *Expose and etch strategies* will give four examples for the fabrication of a wide range of 3D structures with processes ranging from pure conventional litho/etch combinations till advance dual side processing with FTBA.

Overlay characterization

Common overlay characterizations procedures are based on optical principles like pattern recognition or diffraction and can be used for in-line overlay measurements. Non-optical methods are based on electrical measurements of patterned conducting thin films. Because of the required additional processing electrical overlay measurements are off-line measurements. A precise characterization of overlay requires large amounts of measurements over the wafer hence the overlay measurement tools are usually automated.

The measurement principle of optical overlay measurements is based on pattern recognition of customized targets. Often dedicated equipment is used for such measurements [18].A typical layout of a basic optical overlay target for automated measurements is shown in figure 2 [19]. The a-symmetry of a box-in-box structure is a measure for the shift of layer 2 relative to layer 1. For accurate measurements, both layers should yield a clear image and be in focus simultaneously. This may be obvious for conventional front-end processing but it is not always the case for substrates used in back-end processing.

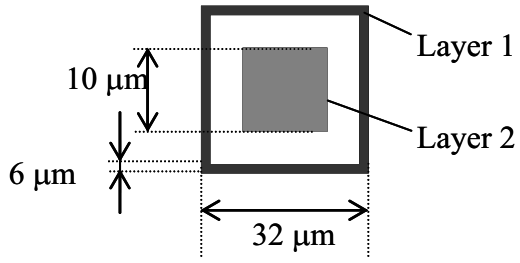

Figure 2. Typical optical overlay test structures for optical overlay measurements.

Alternatively, the alignment system of a waferstepper/waferscanner can be used as a measurement tool. Commonly, overlay test procedures are a part of the maintenance test on these tools. On a wafer with primary alignment markers, a number of image fields are exposed using a reticle with an array of alignment markers in the image field (see figure 3). Using the same reticle, a second layer is exposed with a programmed shift. After development, all the alignment markers are measured using the waferstepper alignment system. The difference between the measured vs. theoretical positions of corresponding markers in both layers is the overlay error. This method can be applied on product wafers and yields useful data of the exposure tool/process performance in production.

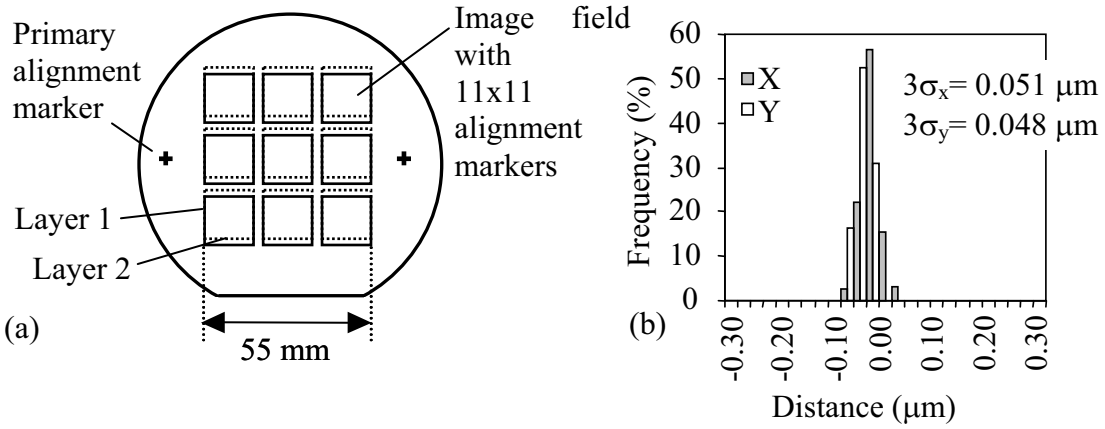

Figure 3. Field layout of the overlay test pattern on a 100 mm wafer (a) and measured overlay using the PAS500 waferstepper alignment system as a metrology tool (b). The measurements are performed on a bare silicon wafer with photoresist.

In case the optical access to one of the layers is blocked or out of focus, electrical overlay measurement can be used. The principle of an electrical overlay test structure is shown in figure 4. The test structure includes two layers sequentially patterned in the same thin conductive film. The first layer (layer 1), consists of probe pads and a set of combined resistors (figure 4a). The second layer (layer 2, figure 4b), defines an area in which the conductive material is removed in the subsequent etching (figure 4c). Accordingly, the width of the resistors is defined by the placement accuracy and dimensions of layer 2. Using high precision resistance measurements, the overlay (layer 1 – layer 2) and dimensions of layer 2 can be calculated from the measured resistances. The reproducibility of electrical overlay test structures depends on biasing and thin film properties values of 11 nm (3σ) are reported [20].

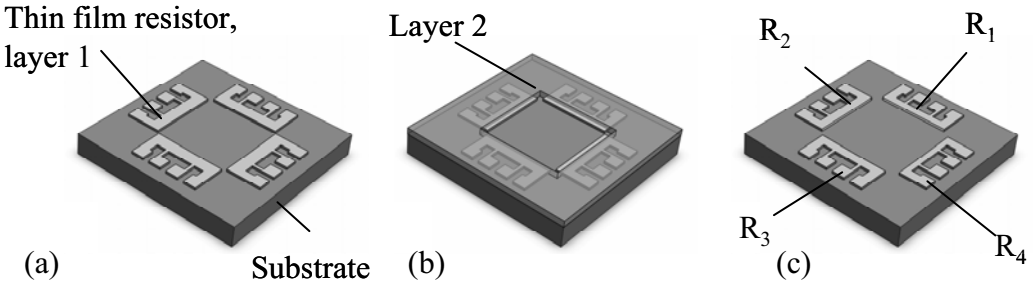

Figure 4. Process sequence of an electrical overlay test structure.

Alignment and overlay case studies

Usually the post litho processing in CMOS technology does not affect the overlay, mainly because the process layers involved are very thin compared to the overall device dimensions. But in 3D processing, the photoresist patterns are often transferred into underlying thick films by reactive ion etching (RIE) assuming a perpendicular anisotropic pattern transfer. However, the perpendicularity of the RIE process is the result of a complex interaction of ions with neutral gas species in an internally biased electric field which depends on etch tool layout and process parameters. As a result, the etch profiles will not be strictly perpendicular to the wafer surface but shows some angular deviation. Particularly for deep etch profiles, like in TSV processing, this angular deviation will

affect the overlay performance. It is therefore important to consider the post-etch overlay and in this case electrical overlay test structures are particularly useful.

To get more insight in the performance of a waferstepper alignment system, the ASML PAS5000 in this case, the alignment and overlay is assessed for four different cases where ΔZ ranges from practically zero to the full wafer thickness (in this work 525 μm). The alignment system of a PAS5000 waferstepper is based on diffraction. The alignment marker is a phase grating. When illuminated with a HeNe laser (λ = 633nm) it reflect precisely defined diffracted orders that are optically processed to yield the alignment marker position. Although this alignment system is quite specific, the processes and measurement principles discussed here are also applicable to other alignment systems.

Case 1: wafer bonding and thinning

In aligned wafer bonding and thinning, the wafers are bonded face-to-face. After thinning of the added device wafer TSV's are processed [21] to connect the device layers on both wafers. One would expect that the face-to-face overlay accuracy is solely determined by the alignment accuracy of the waferbonder, typically 1-2 μm. But the bonding and wafer thinning process can introduce a substrate distortion that reduces the overlay accuracy. Furthermore, the optical access to the alignment markers goes through the remaining silicon of the thinned top-wafer, and the device patterns and the alignment markers on device-layer 2 are mirrored (see figure 5). This all can have consequences for the overlay accuracy.

Figure 5. Face to face waferbonding result in mirrored device layers and alignment markers after bonding and thinning.

Using mirror symmetric alignment markers [22], the substrate distortion in waferbonding and thinning processes can be characterized employing the waferstepper as a measurement tool [23, 24], the process is summarized in figure 6a and 6b. A silicon wafer is patterned with layer 1 of an overlay test pattern like in figure 3. The patterns are etched into the silicon and the alignment marker positions are measured and stored in a dataset. Next a silicon dioxide or low stress silicon nitride is deposited on the wafer after which the wafer is bonded to a carrier wafer. After bonding, the silicon wafer is removed in a wet chemical etch process and the alignment markers of layer 1 are exposed to the surface. To enhance the optical reflectivity, 100 nm aluminum is sputtered on top of the alignment markers.

Again layer 1, which is now mirrored, is measured as an overlay test layer. This measurement is mirrored and compared with the previous measurements. The shift between pre- and post-bond measured positions of the very same markers is a measurement of the distortion in the substrate transfer process. Note that the primary marker positions can also be affected by the substrate distortion. As a consequence, the exposure grid can be shifted as well. A correction method for this effect is given in [25].

Different kind of carrier wafers and different bonding technologies are investigated, and the results are summarized in table 1.

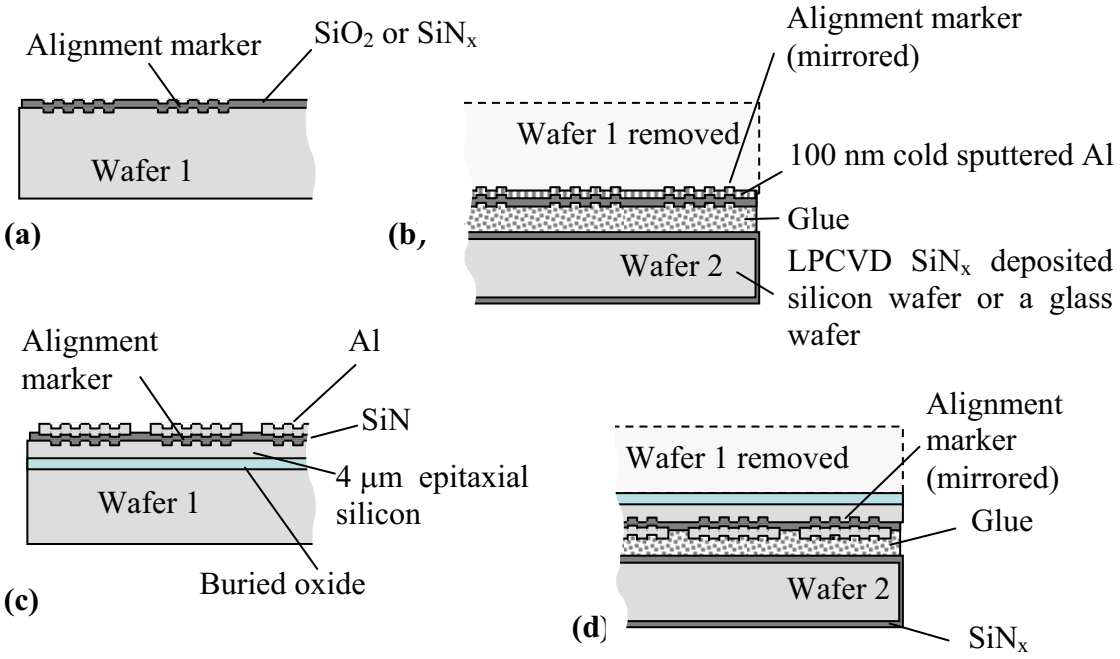

Figure 6. Face to face waferbonding and tinning process to fabricate alignment test wafers for two different processes; only alignment markers are transferred (a) and a device layer of 4 μm thick silicon is transferred (b).

Table 1. Measured substrate distortion for different wafer bonding and thinning processes

Wafer nr.	Bonding process	Substrate wafer material	Standard alignment ⇓ / Align through 4μm silicon ⇓	Substrate distortion $3\sigma_X$ (μm)	Substrate distortion $3\sigma_Y$ (μm)
1	anodic bonding at 250 °C	glass	x	0.37	0.33
2	anodic bonding at 300 °C	glass	x	0.33	0.26
3	anodic bonding at 400 °C	glass	x	0.48	0.52
4	adhesive bonding	glass	x	0.15	0.13
5	adhesive bonding	glass	x	0.19	0.2
6	sodium silicate bonding (silicate thickness = 10 nm)	silicon	x	0.76	0.47
7	adhesive bonding wafer A (see figure 7)	silicon	x	0.69	0.68
8	adhesive bonding wafer B (see figure 7)	silicon	x	0.18	0.42

In the process given in figure 6b, the silicon carrier wafer is completely removed. However, in a W2W integration processes, a silicon device layer is left after thinning. To asses the alignment and overlay performance in a more practical situation, substrates with a silicon device layer of 4 μm thick were fabricated and characterized. On SOI wafers (wafer 1, figure 6c) alignment markers are etched in the silicon and the wafer is coated with 500 nm LPCVD low-stress SiN_x. To enhance the optical reflection, aluminum pads are fabricated on top of the alignment markers. Next, the wafer is glued on a carrier wafer (wafer 2). The carrier wafer is etched in a KOH solution and the buried oxide (300 nm) is used as an etch stop (figure 6d).

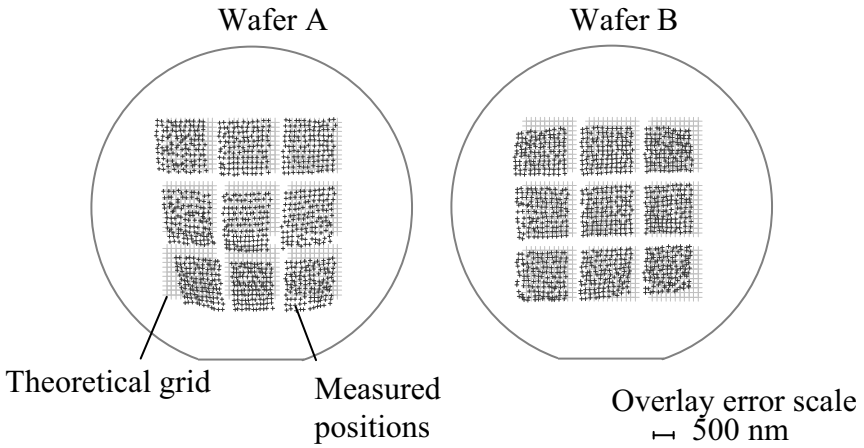

Figure 7. Measured substrate distortion on two bonded and thinned wafers.

After the bonding and thinning process, the very same alignment markers (now mirrored) are measured again. The alignment is now performed through a silicon layer of 4 μm thick, hence the optical path through the silicon is 8 μm. The optical transmission for the alignment wavelength in this case is about 6%, still within the specification of the alignment system (0.1%). The measurement results of two wafers, fabricated in this process are shown in figure 7. Clear inter-die distortion patterns can be recognized. The distortion of the two wafers, expressed in 3σ values, differs significantly which indicates that overlay measurements provide a precise quantitatively method of describing the wafer distortion.

Multi point alignment and the ability to align through thin silicon films can provide more accurate alignment in several 3D integration processes. For example when aligned waferbonding is used to join two wafer, the overlay error between the two exposure grids on each wafer is determined by the bonding process; mainly the alignment accuracy of the bondtool. With multi point alignment trough the thinned top wafer, the exposure grids of both wafers are precisely characterized and a new exposure grid can be calculated that minimize the overlay errors. Such alignment strategies are only possible with flexible multipoint alignment algorithms available on wafersteppers.

Case 2: Alignment performance through 15μm thick transparent films

Both contact aligners and wafersteppers use the wafer surface as a reference plane for the exposure settings. Hence if thick films are processed, the alignment marker buried under the thick film is shifted away from the reference plane. This shift, earlier referred to as ΔZ can be as large as 50 μm. This can have consequences for the overlay accuracy if for example the optical axis of the alignment system is not perpendicular to the wafer surface. Furthermore, for optical alignment systems based on pattern recognition the large ΔZ may result in focus issues.

The fabrication of test structures to characterize the overlay in this case is given in figure 8. The start material is a 100 mm wafer coated with 500 nm LPCVD low stress silicon nitride (SiN_x) and 100 TiN. First, the TiN film is patterned with layer 1 of the electrical overlay test structure. Next, a thick PECVD SiO_2 film is deposited, due to stress and tool limitations the SiO2 film thickness is 15 μm. After the SiO_2 deposition, layer 2 of the test pattern is printed in photoresist on top of the oxide. Both layers carry not only electrical test patterns, also optical alignment markers are integrated. In this way, optical and electrical overlay measurements can be performed on the same wafers.

After the exposure and development, the overlay of layer 2 to layer 1 is measured using the wafersteppers alignment system. As a reference, wafers with no deposited oxide are measured ($\Delta Z = 0$). The results are given in figure 9. The effect of ΔZ on optical image quality is illustrated in figure 9c and 9d, here manual overlay read-out patterns are given. The image in figure 9d is focused on the wafer-oxide interface, image 9d is focused on the oxide surface. Clearly the image quality will strongly reduce the accuracy of the overlay measurement.

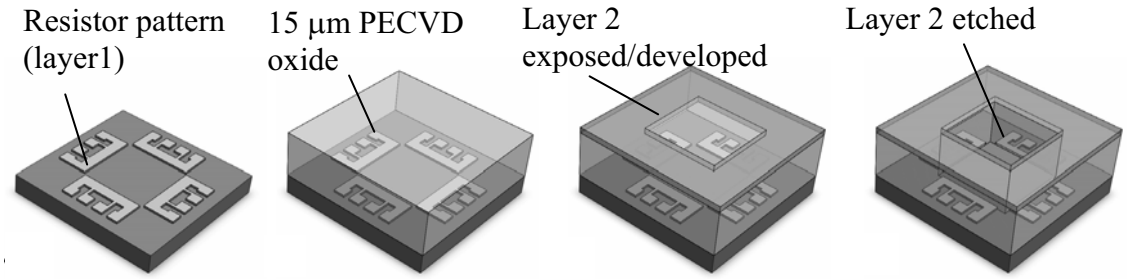

Figure 8. Process flow to fabricate overlay test structures where layer 1 and layer 2 are separated with $\Delta Z = 15$ μm.

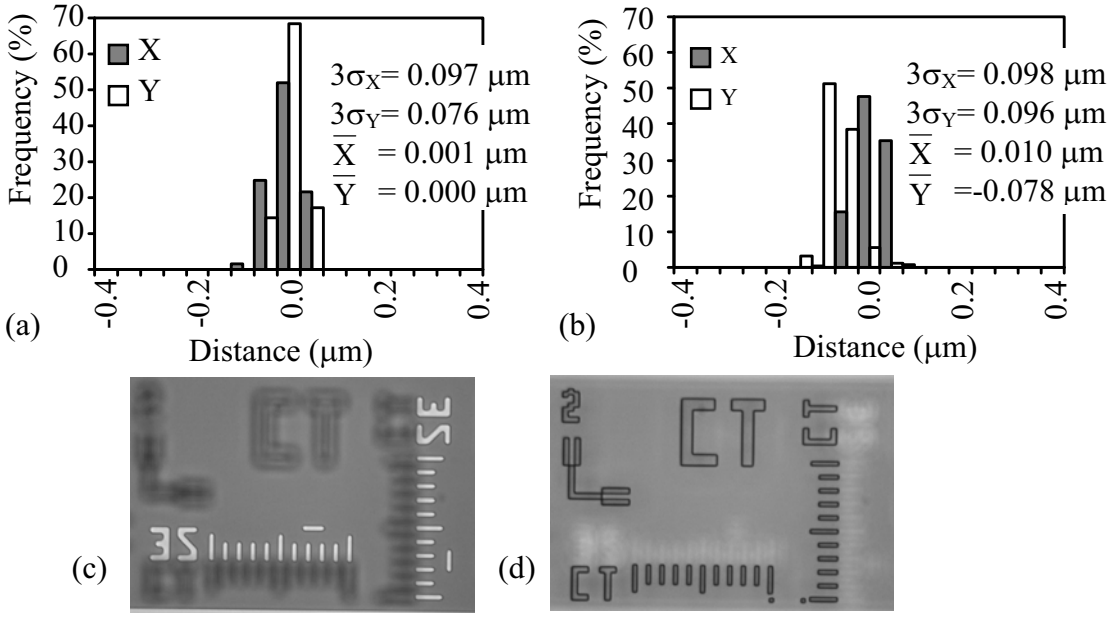

Figure 9. Optical overlay measurements on a wafer with layer 1 and layer 2 separated with $\Delta Z = 0$ μm (a) and with $\Delta Z = 15$ μm (b). Microscope images with focus on the silicon oxide interface (c) and on the oxide surface (d).

After the optical measurements, layer 2 is etched through the oxide and the TiN films defining the final dimension of the resistors. To gain access to the electrical test structures, the oxide film is removed in a buffered hydro fluoric solution (BHF) solution. In BHF, the SiN_x and TiN are virtually not etched. The measurement results of the electrical overlay measurements are given in Fig. 10. The results indicate that the optical measured overlay is virtually unaffected by ΔZ. However, the overlay of the contact openings after etching through 15 μm oxide is deteriorated. Clearly the etching over relative large ΔZ does affect the overlay.

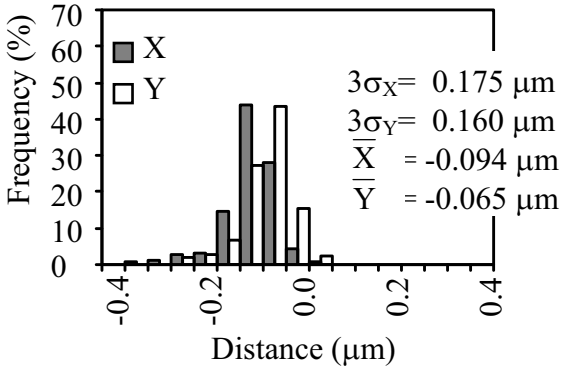

Figure 10. Electrical overlay measurements on a wafer with ΔZ = 15 μm.

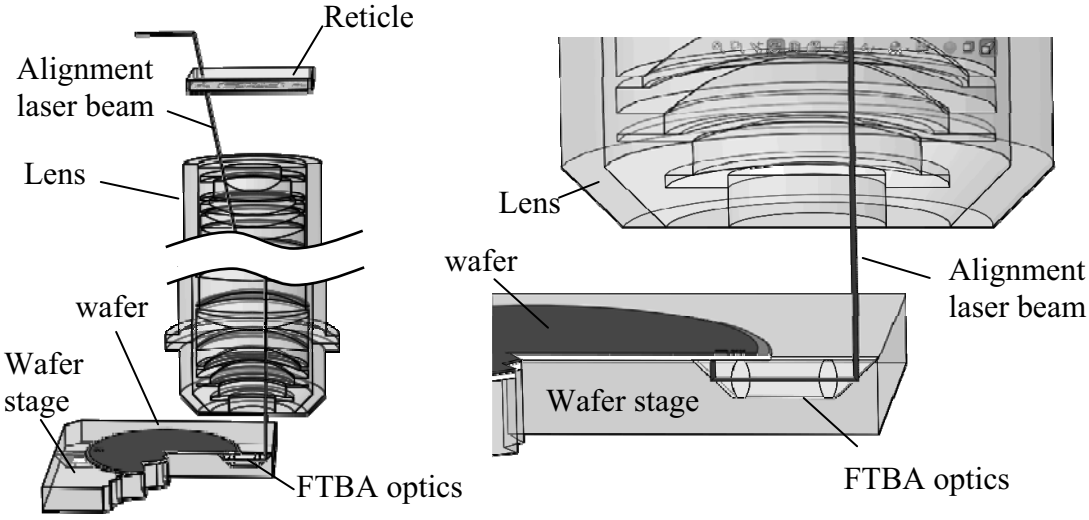

Figure 11. The ASML phase grating alignment system with FTBA extension.

Case 3: Dual side alignment. For dual side interconnect with TSV, the wafers are processed on both sides. In this case, optical access to an alignment marker on the backwafer is only possible using dedicated FTBA optics (figure 11). The alignment accuracy of an FTBA system is verified using KOH through wafer etching [20], the overlay accuracy on a PAS5000 waferstepper is better than 500 nm (3σ).

Using this calibrated FTBA system, a deep RIE trough wafer etch process can be characterized as follows: On the front side of a double side polished wafers a 100 nm thick LPCVD SiN_x film and a 100 nm PVD TiN film are deposited (Layer 1). Next a PECVD oxide etch stop layer is deposited on the front side of the wafer (figure 12a), followed by the deposition of a 6 μm PECVD hard mask on the backside. Layer 2 is aligned on the backside (figure 12b) using an ASML PAS 5000 waferstepper with a FTBA alignment system. After patterning in the oxide hardmask, layer 2, is etched through the wafer, through the SiN_x and through the resistors into the etch-stop oxide (figure 12c). The etch process is a time multiplexed Bosch process. To access the TiN resistors for measurement, the remaining oxide on both sides of the wafer is removed with BHF. A schematic cross section and a micrograph of the through wafer overlay test structure is given in figure 12d.

The overlay measured after etching through a 525 μm thick wafer is given in figure 13 and indicates clearly that, through wafer etch is the overlay limiting factor.

However, very precise dual side alignment systems in combination with the method described above can be used to benchmark and improve the DRIE process [26].

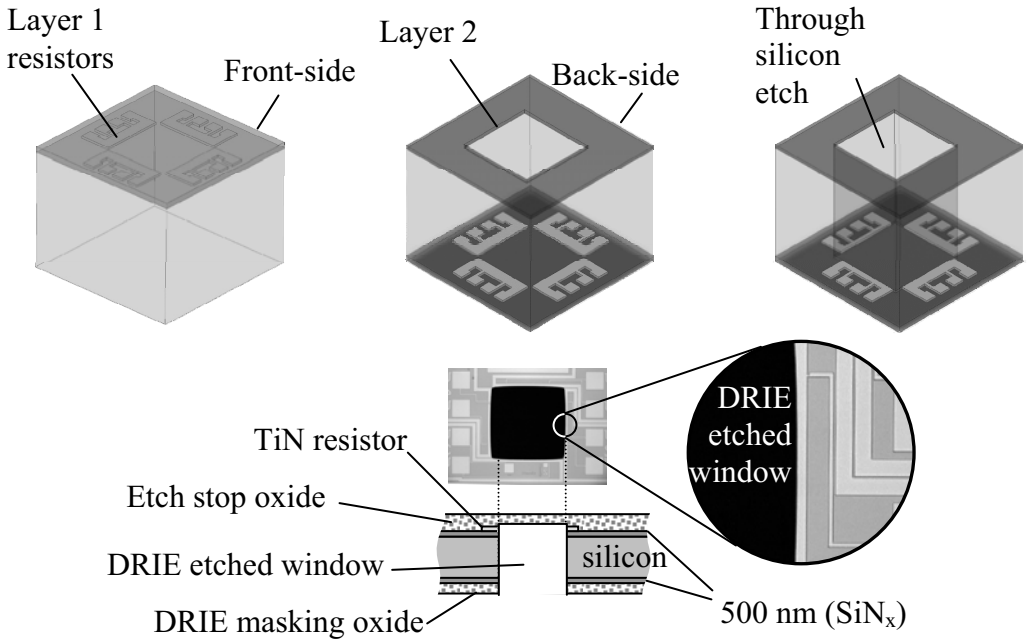

Figure 12. Fabrication process of through wafer overlay test structures (a, b and c) and a schematic cross section and micrograph (d).

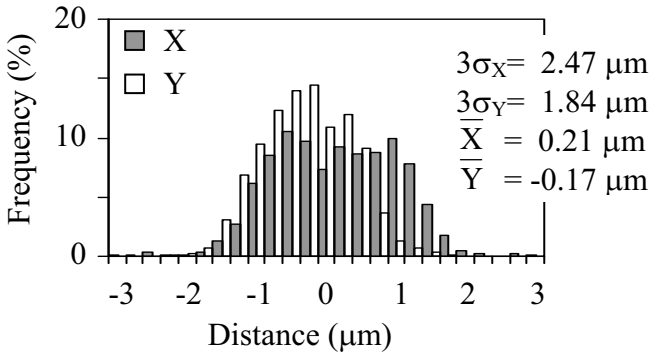

Figure 13. Measured overlay after TSV etching using deep RIE through a 525 mm thick wafer.

Exposure and etch strategies

The 3D device architecture and its associated substrate topography, determines to a large account which exposure and etch strategy must be used for optimal result. A few examples, to illustrate different exposure and etch strategies, are listed below. Unless otherwise mentioned, the exposures are performed on an ASML PAS 5000 waferstepper.

Planar processing with conventional lithography: microsieve fabrication

In this example, the 3D functionality is enshrined in a stack of deposited thin films with different properties. The 2D binary lithographic pattern is vertically etched into the film stack followed by an isotropic selective etch to create the required structure(s) to fabricate a microsieve [27].

The fabrication process is schematically depicted in figure 14. The first step is to prepare a sandwich structure that will eventually become the sieve's wall (figure 14a). Three silicon nitride layers and three 100 nm thick silicon oxide layers are deposited alternatively on a silicon wafer. The silicon nitride forms the structural layers for the microsieve and the silicon oxide works as sacrificial layers. A photo resist layer is spin coated, the shape of sieve walls are patterned and then dry etched through the sandwich into the silicon substrate to build the "walls" (figure 14b).

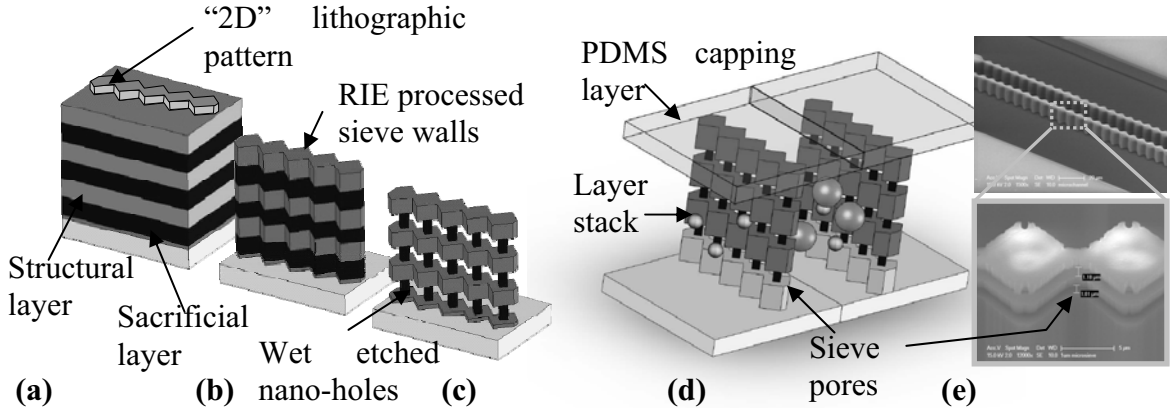

Figure 14: Schematic view of the process flow to fabricate the vertical-wall microsieve (a-c), a schematic detail of the completed device (d) and a SEM picture before PDMS capping (e).

All sacrificial layers are then removed in a single wet chemical etching step using BHF (figure 14c). The channels are sealed with a PDMS capping layer (figure 14d). Nanochannels with a precisely controlled height of 100nm are thus formed on the walls. A SEM picture of a fabricated structure before sealing is shown in figure 14e.

Planar processing with conventional lithography: vertical silicon plate springs

Here a sequence of conventional 2D masking layers in combination with (deep) anisotropic etching processes is employed to create the required structures. To keep the topography compatible with the 2D nature of conventional lithography, all the masking layers are applied before the (deep) etching processes are performed. This approach enables the use of conventional lithographic equipment and processes to fabricate the devices.

In this example, a vertical silicon plate spring (figure 15) [28] is fabricated with three masks. A back side cavity (BC) and a front side cavity (FC) to define the plate spring thickness and a device release cavity (DRC) to separate the devices. An overview of the process flow is given in figure 2, the fabrication starts with the deposition of 6 μm silicon oxide on both sides of double side polished silicon wafer. This oxide serves as hard masks for the deep reactive ion etch (DRIE) process. First the BC layer is exposed on the wafer back side and etched through the oxide. Next the DRC mask is exposed and 1.5 μm of oxide is etched. With a combined DRC-FC masking, the remaining oxide is removed

at the DRC with a shorter oxide etch (figure 2b), which leaves 1 μm of oxide at the FC layer. At this point, all the 2D patterning is completed and can be converted into a 3D device using a sequence of DRIE process steps.

The BC areas are partially etched into the backside of the wafer followed by a BC lining oxide deposition (see figure 15c). Next the DRC is etched partly into the silicon, the remaining FC oxide blocks the silicon etch in the FC areas (figure 15c). After the partial DRC silicon etch, the remaining FC oxide is removed using a maskless oxide RIE and the FC and DRC areas are further etched into the silicon (figure 15e). Finally, about 30 μm silicon is left in the FC areas to connect mass to the upright plate spring. The remaining oxide is removed using wet chemical etching to release the devices. From mass-spring resonance measurements, the plate spring thickness and thus FTBA overlay error was calculated and found to less than 300 nm [29].

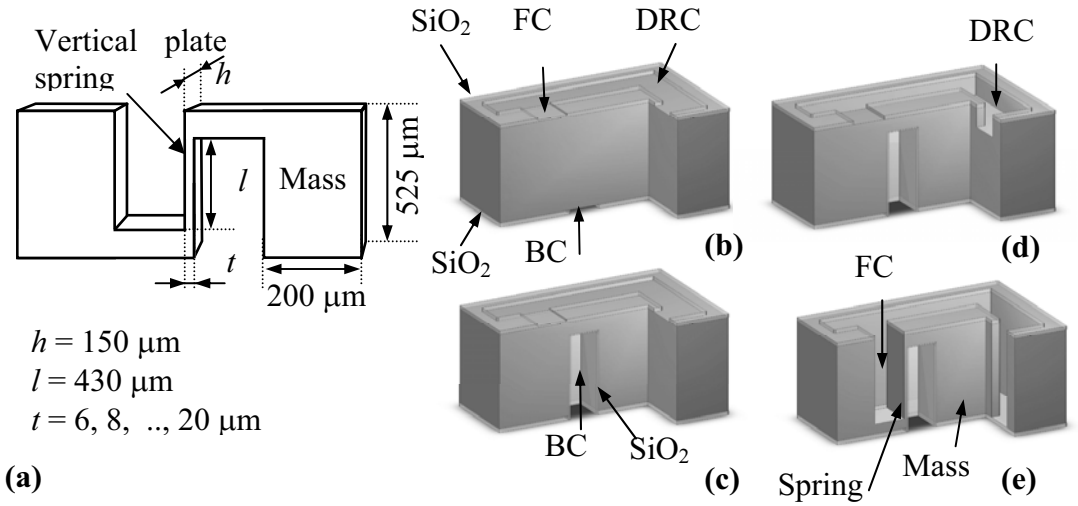

Figure 15. Schematic 3-D view of the mass-spring system with upright plate springs and the mass-spring dimensions used in this work (a). The process flow (b - e,) is explained in the text.

Planar processing with gray scale lithography: dual side interconnect

With gray scale lithography, the 3rd dimension is coded in the transmission of the photomask. In this way, non-binary 3D resist patterns are formed after exposure and development. The relative thin 3D photoresist pattern is extruded into the 3rd dimension using (deep) reactive ion etching. This approach is used to fabricate a cost effective dual side interconnect for 3D integration purposes with through silicon vias (TSV) [30]. The formation of the TSV is given in figure 16.

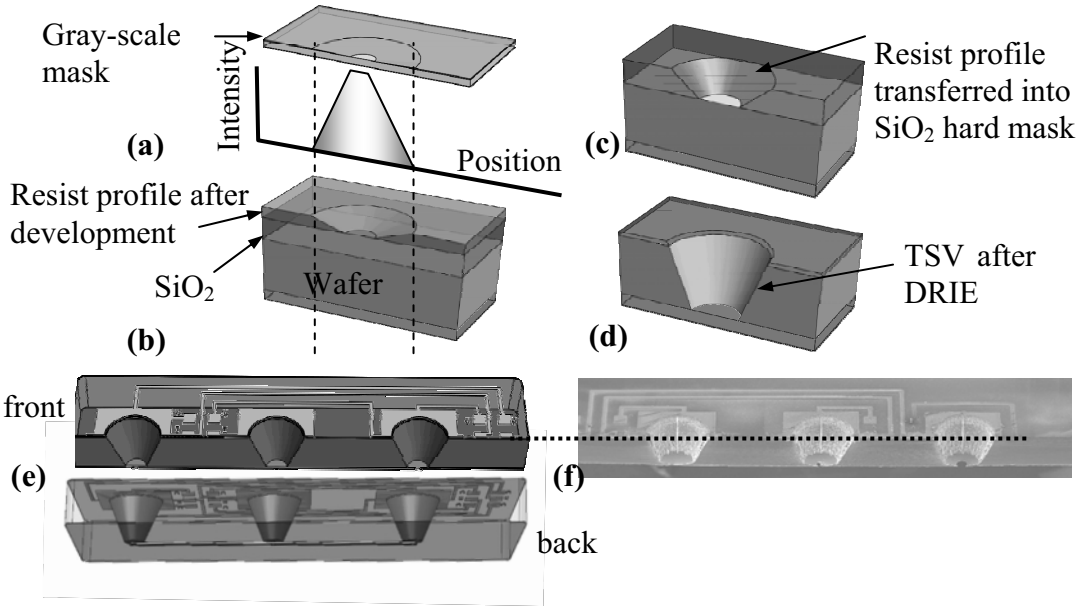

Figure 16: With gray scale fabricated TSV process flow (b-d), a schematic drawing of a Kelvin test structure with dual side interconnect test pattern with TSV (e) and a SEM image of a fabricated test structure (f).

A gray scale mask exposure (figure16a) is used to form a resist profile with sloped sidewalls (figure 16b). This profile is transferred into the underlying oxide layer with RIE (figure 16c) and further transferred through the silicon to form a TSV with lithographically designed sloped sidewalls (figure 16d). A schematic diagram of a Kelvin test structure with dual side interconnects is given in figure 16e, a SEM cross-section is shown in figure 16f. The TSV slope is determined by a designed mask transmission, not by a tuned DRIE process enabling more design freedom. An example of a TSV with partial vertical and partial sloped sidewalls is given in figure 17a, an SEM cross section of such a via is given in figure 17b.

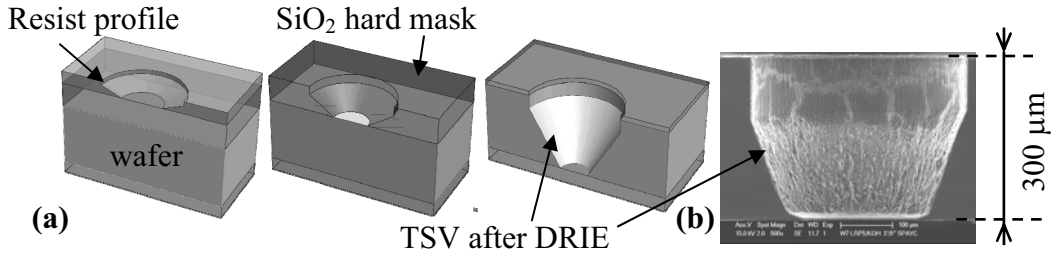

Figure 17: An example of a TSV with partial vertical and partial sloped sidewalls

Topography processing with thick photoresist: pattern transfer on vertical sidewalls

A binary mask exposure in thick photoresist, covering high topography structures can define structures on the sidewalls of that topography enabling for example vertical electrode definition in cavities [17].

Figure 18 shows a schematic description of the fabrication steps. First, 60 µm deep cavities are etched into the silicon substrate (figure 18a) by deep reactive ion etching (DRIE) and a 3 µm thick aluminum layer is deposited (figure 18b). Next, SU-8 photoresist is applied, completely covering the high topography surface (figure 18c). The photoresist both in the cavities and on the wafer surface is exposed using a contact aligner

and developed (figure 18d). After aluminum etching, the SU-8 mask is removed (figure 18e). A SEM image of a sidewall electrode is given in figure 18f.

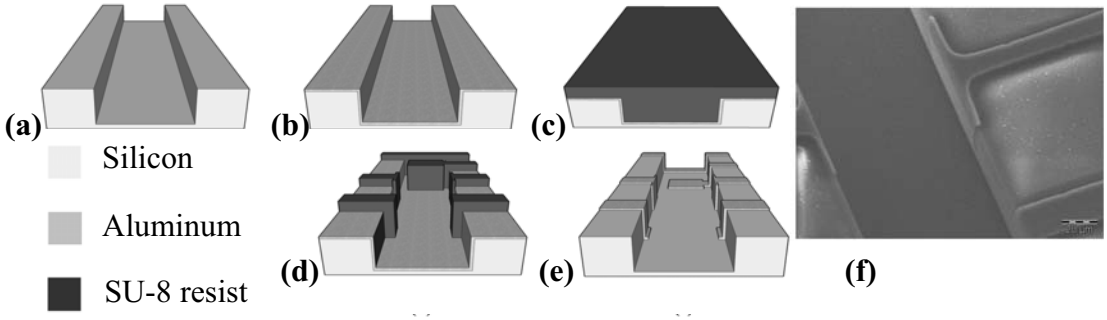

Figure 18: Schematic process flow for the fabrication of vertical sidewall electrodes (a-e), the process is explained in the text. SEM image of a vertical electrode (f).

Conclusions

Mainstream lithography is optimized for IC fabrication. It is a mature production technology designed for high volume manufacturing. But the pattern transfer has a strong 2D nature. Today a wide range of etching techniques is available ranging from wet chemical isotropic etching till highly anisotropic DRIE (Deep reactive Ion Etching). It is the combinations of process sequences of wet/dry deep/shallow etching with 2-D lithography that allow us to fabricate a wide range of 3D structures.

A waferstepper alignment system, based on phase gratings is fully functional in a wide range of processes used in 3D integration and WLP. The measured overlay performance is better than currently needed. Besides that, W2W bonding and (deep) RIE processing is limiting the post etch overlay accuracy. However multi point alignment available on wafersteppers has the capability to reduce the process induced overlay errors. Furthermore it is expected that with improved etch processes and further miniaturization, the performance of a phase grating alignment system will be fully exploited in the near future. Accurate overlay measurements in 3D integration can play an important role in further development of these processes.

References

1. K. Cooper, K. Cook, B. Whitney, D. Toennies, R. Zoberbier, K. J. Kramer, K. Weilermann, and M. Jacobs, *Proc. of Pan Pacific Microelectronics Symposium*, pp. 74-82 (2008)
2. M. Muhlberger, I. Bergmair, W. Schwinger, M. Gmainer, R. Schoftner, T. Glinsner, Ch. Hasenfuß, K. Hingerl, M. Vogler, H. Schmidt, E.B. Kley, *Microelectronic Engineering*, 84 pp. 925–927, (2007)
3. ASML PAS 5500 product catalog
4. H. W. van Zeijl, K. Simon, J. Slabbekoorn, W. v. Buel and C. Q. Gui, *MRS Symposium Proc. Vol. 729 - BioMEMS and Bionanotechnology*, (2002)
5. M. S. Hibbs, in *Micro lithography, science and technology/2007*, K. Suzuki and B. W. Smith, Editors,p. 11, CRC press, Boca Raton, FL (2007)
6. B. Meliorisz , S. Partel, T. Schnattinger, T. Fuhner, A. Erdmann, P. Hudek, *Microelectronic Engineering* 85 pp.744–748 (2008)

7. product information Suss Mircotech, http://www.suss-microoptics.com/downloads/Publications/SUSS%20MicroOptics,%20MO%20Exposure%20Optics%20Gen1.pdf (2010)
8. B.W. Smith, in *Micro lithography, science and technology/2007*, K. Suzuki and B. W. Smith, Editors,p. 11, CRC press, Boca Raton, FL (2007)
9. P. Maury, J. M. Quemper, S. Pocas, D. van Vliet, N. Noordam, P. ten Berge, K. Best, *Conf. Proc Micro Nano Engineering*, Volume 87 , Issue 5-8 ,pp 904-906 (2010)
10. P. Cheang, W. Staud, G. Newman, *Proc. of Advanced Manufacturing Technologies Seminar (1997)*
11. B Todd, W. W. Flack, and S. White., *Proc. of Micromachining and Microfabrication Process Technology V* , pp. 330-344 (1999)
12. M. Schirmer, D. Perseke, E. Zena, D. Schondelmaier, I. Rudolph and, B. Loechel., *Microsyst Technol*, 13 pp 335-338, 2007
13. ShinEstu MicroSi SIPR-7120 data sheet
14. T. Horiuchi, Y. Furuuchi, R. Nakamura, K. Hirota, *Microelectronic Engineering* 83 pp 1316–1320,(2006)
15. A del Campo, C Greiner, J. *Micromech. Microeng.* 17 pp 81-95, (2007)
16. D. Liu, H.W.van Zeijl, P. M. Sarro, , *Proc. MME* , page 133-136, (2008)
17. T. M Verhaar, J Wei and P M Sarro, *J. Micromech. Microeng.,* 19 No 074018 (6pp) (2009)
18. Y. Tsung Lin, C. Chou Hsu, S. Tseng, *IEEE International Symposium on Multimedia Workshops,* pp. 63 – 69, (2007),
19. M., Adel, M., Ghinovker, B., Golovanevsky, P., Izikson, E., Kassel, D., Yaffe, A., M. Bruckstein, R., Goldenberg, Y., Rubner, and M. Rudzsky, *IEEE Trans. On Semiconductor Maunfacturing* Vol. 17 No. 2, p166-p179, (2004)
20. H.W. van Zeijl, F. G. C. Bijnen, and J. Slabbekoorn, , *Proc. SPIE, MEMS, MOEMS and Micromachining*, Vol. 5455, pp. 398-406, (2004)
21. C. Keast, B. Aull, J. Burns, N. Checka, C. L. Chen, C. Chen, J. Knecht, B. Tyrrell, K. Warner, B. Wheeler, V. Suntharlingam, D. Yost., *Proc. MRS 2006 Fall Meeting,* (2006)
22. H. W. van Zeijl, J. Slabbekoorn, L. K. Nanver, Paul W. Van Dijk, Axel Berthold, and T. Machielsen., *Proc. of SPIE Challenges in Process Integration and Device Technology*, Vol. 4181, pp. 200-207, (2000)
23. H. W. van Zeijl and J. Slabbekoorn. *Proc. international conference on semiconductor technology*, Vol. 2001-17, pp 356-367, (2001)
24. L. Marinier, W. van Noort, R. Pellens, B. Sutedja,R. Dekker,H. W. van Zeijl, *Micro electr. Eng*., vol. 83 pp. 1229 – 1232 (2006)
25. H. W. van Zeijl, PH. D. Thesis Delft University of Technology, ISBN: 90-8559-045-0 (2005)
26. N. Launay, H. W. van Zeijl and P. M. Sarro, *Conf. Proc. IEEE MEMS 2008*, pp.311-314, (2008)
27. C.Shen, H.T.M.Pham, P.M.Sarro, *Conf. Proc IEEE MEMS*, (2009)
28. S. L. Paalvast, H. W. van Zeijl, J. Su, P. M. Sarro, and J. v. Eijk, *Journal of Micromechanics and Microengineering*, vol. 17, no. 7, pp. S197– S203 (2007)
29. H.W.van Zeijl, S.L.Paalvast, J.Su, J.van Eijk, P.M.Sarro, *Proc. Transducers,* pp. 1605-1608 (2007)
30. H. W. van Zeijl, D. Liu and P. M. Sarro, *Conf. Proc, Eurosensors XXIII*, (2009)