Compact Neural Amplifier for Next-Generation Brain-Machine Interfaces

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MSc thesis

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Compact Neural Amplifier for Next-Generation Brain-Machine Interfaces

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering

by

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July 4, 2022

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Abstract

Brain-machine interfaces (BMI) are electronic devices that form an interconnection between the users brain and an external device through which the user can control the device and the device can apply stimulation to the users brain or nervous system. BMIs have undergone a rapid evolution in development and applications. While the first generation of BMI were exclusively used as proof of concept in research experiments, now more and more clinical applications in humans are becoming a reality. In recent years, various neurodegenerative diseases such as locked-in syndrome, epilepsy and retinitis pigmentosa, for which there currently exist no cures, have been successfully treated using implantable BMIs.

BMI development is continuously striving towards increasing the recording resolution and number of recording channels. As a result of recent innovations in electrode design and implementation, the recording of single brain cells has become possible, enabling the development of BMI with single-cell recording resolution. The primary bottleneck preventing more recording channels in single-cell resolution BMIs is caused by the neural amplifiers required to amplify the neural signals from the electrodes. Large amounts of recording channels require large arrays of neural amplifiers which in turn require large chip area and power, both of which are resources that are limited in implantable BMI applications.

The primary focus of this work is the development of a neural amplifier for use in next-generation single-cell resolution BMI. The neural amplifier is developed in 40nm CMOS technology and exploits the spatial correlation of the neural signal to implement a novel shared feedback system that reduces the power and area per recording channel. The amplifier is designed and verified with post-layout simulations, achieving a gain of 45 dB over a bandwidth from 93.8Hz to 5.44kHz, power usage of 600 nW per recording channel and an input referred noise voltage of 9.00 μV_{rms} with a total chip area of 2190 μm^2 per recording channel.

Contents

Introduction

Brain-machine interfaces (BMI), also known as brain-computer interfaces (BCI), have undergone a rapid evolution in development and applications. The first generation of BMI were exclusively used on animals and served more as a proof of concept devices rather than anything that could be useful for human applications. In recent years however, various neurodegenerative diseases such as locked-in syndrome, epilepsy [1] and retinitis pigmentosa [2] [3], for which there currently exist no cures, have been successfully treated using BMI.

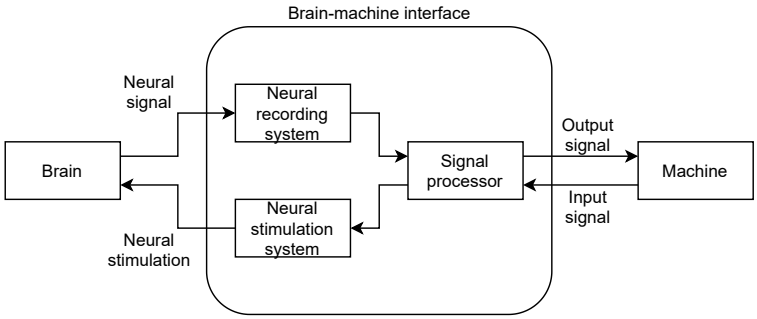


Figure 1-1: High level overview of a BMI.

Given in figure 1-1 is a high level system overview of a bi-directional BMI. BMI form an interconnection between the users brain and an external device through which the user can control the device and the device can apply stimulation to the users brain or nervous system. BMI achieve this by utilizing dedicated neural recording and stimulation systems. The neural recording system extracts neural signals from the brain. The neural stimulation system applies stimulation to the brain according to signals received from the machine. BMI may also possess a signal processor unit for incoming and/or outgoing signal processing purposes. Uni-directional BMI that can only perform neural recording or stimulation also exist.

Research interest in BMI has been on the rise in recent years. Given in figure 1-2 is a graph depicting the number of IEEE publications with "brain-machine interface" or "brain-computer interface" as search term over the time period from the year 2000 to 2020. This figure shows an increasing trend in research into BMI, a trend that is expected to only increase further as BMI technology continues to improve.

Given in Table 1-1 are a selection of multi-channel neural recording systems found in literature and the contribution of the amplifier system to the total size and power usage of the neural recording system. From this table it can be determined that the amplifier requires the largest amount of chip area and consumes the largest amount of power compared to the other components of the neural recording system.

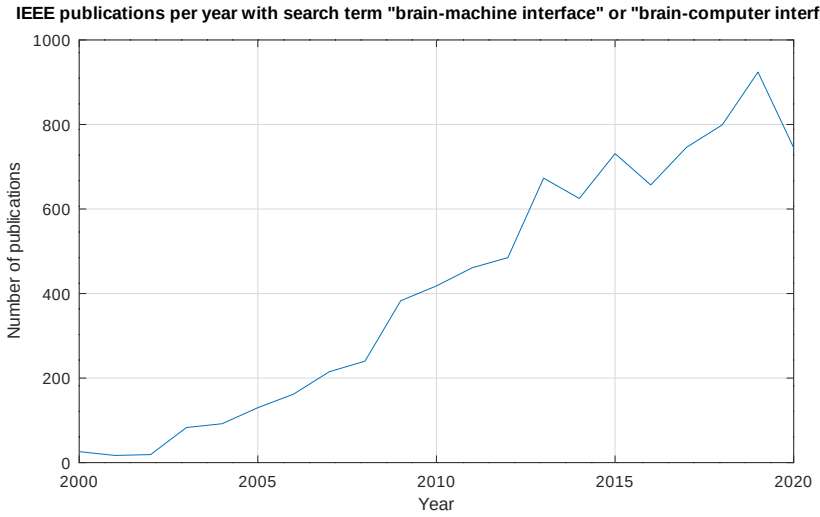


Figure 1-2: IEEE publications per year with search term "brain-computer interface" or "brain-machine interface".

Table 1-1: A selection of state of the art recording systems from literature and the contribution of the amplifier system to the total chip area and power consumption of the recording system.

Ref.	**Recording channels**	**Chip area(mm^2)**	**Amplifier area**	**Amplifier power usage**
[5]	64	18.4	73.1%	88%
[6]	16	15.6	78%	62.6%
[7]	56	8.7	52.9%	78.5%
[8]	200	13.4	61.9%	79.7%
[9]	2048	106.8[a]	41.9%[a]	-
[10]	100	25	81.8%	77.7%
[11]	256	12.8[b]	70.1%[b]	-

[a] Recording system IC includes an on-chip electrode array.

[b] Recording system IC includes an on-chip neurostimulator.

As a result of innovations in electrode design and implementation, the recording of single brain cells, called neurons, in BMI applications has become possible. [12] Neurons are the structural units of the nervous system through which information is transported to and from the brain. Neurons are the smallest units of the nervous system and are therefore the smallest units from which neural information can be extracted.

Neurons communicate via electrical signals called action potentials (AP). AP can be sensed from the extracellular fluids by placing electrodes close to the neuron. AP measured from the extracellular fluid are called extracellular action potentials (EAP). Neurons can fire AP in rapid succession. Given in figure 1-3 is an example of a EAP recording obtained from a zebra finch. [13] Due to the waveform resembling a spiky train of pulses, EAP are sometimes referred to as spikes. Each spike indicates an AP produced by the neuron.

Illustrated in figure 1-4 is the method with which spike train signals can be recorded. Obtaining a spike train signal can be achieved by placing an electrode in the neural tissue. This

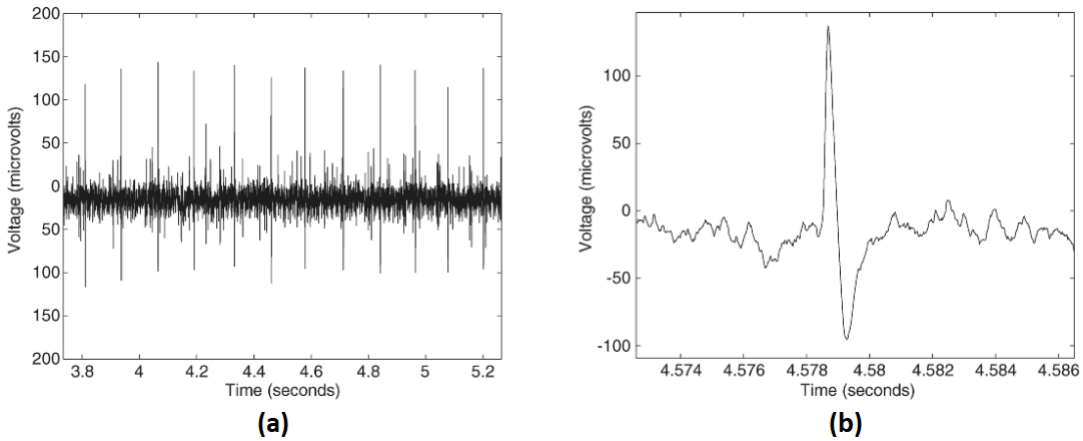


Figure 1-3: EAP signal recording obtained from a zebra finch. Recording of (a) spike train and (b) single spike [13].

electrode measures the EAP signals from multiple neurons near the electrode which are then amplified, producing a raw data signal. The resulting raw data signal contains the EAP signals of multiple neurons. In order to obtain the spike trains from individual neurons, a method called spike sorting is used. Spike sorting identifies all the spikes present in the raw data signal and sorts each spike to correspond with the neuron from which it originated. When all spikes have been detected and sorted, the spike train signals for each individual neuron are then generated. Thus achieving single-cell recording resolution.

As BMI development is continuously striving towards increasing the recording resolution and number of recording channels, the total chip area and power consumption of the amplifiers increases as well. The primary bottleneck preventing higher amounts of recording channels in single-cell resolution BMI is therefore caused by the amplifiers.

Given in Table 1-2 are the main requirements for the amplifier of a single-cell resolution BMI. Achieving these requirements is a non-trivial task since an amplifier can be made using various different circuit topologies which significantly differ in terms of area and total power usage per recording channel. Design trade-offs, particularly in power versus noise performance, add to the challenge of implementing an optimal amplifier system.

Table 1-2: Requirements for a neural amplifier for use in single-cell resolution BMI.

Parameter	**Value**	**Justification**
Area/channel	$<50\mu m \times 50\mu m$	Single cell resolution
Gain	50 - 100 V/V	EAP range from $50\mu V_{pp}$ to $500\mu V_{pp}$. [14]
Power	$<1 mW/mm^2$	Avoid tissue damage [15], prolongs battery life [14].
Noise	$<10\ \mu V_{rms}$	Differentiate noise from EAP spikes [14].
Bandwidth	100Hz - 5kHz	Frequency range of EAP [16].

This introductory chapter serves as a literature review with the primary focus being on the

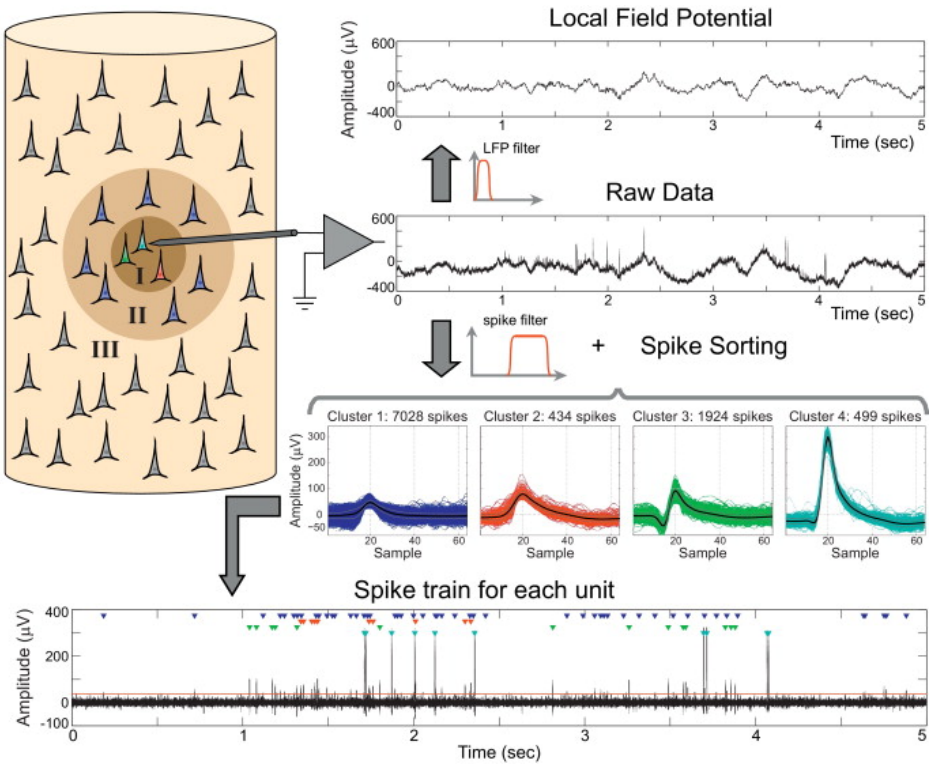


Figure 1-4: Illustrative example depicting the acquisition of EAP spike signal train from single neurons using spike sorting [12].

amplifier system of the neural recording system. In this review, amplifiers published in recent literature are evaluated for use in single-cell resolution BMI based on the requirements given in table 1-2 in order to determine the optimal neural amplifier topology for use in single-cell resolution BMI.

In order to properly conduct this review, this paper is divided into 4 sections. Section 1-1 presents and reviews amplifier topologies that have been used in literature to perform neural recording. In this section the focus is on the area per recording channel required by the amplifier topology. Section 1-2 presents and reviews OTA architectures. In this section the focus is on the noise behaviour and power usage of the OTA. Recommendations for future work are presented in section 1-3. Finally, section 1-4 provides the conclusion of this literature review.

1-1 Amplifier architecture

The focus of this section of the review is on the amplifier topology and its performance per area per channel. First, a set of figures of merit are defined by which the performance of the amplifier topology are quantified. Amplifier architectures are presented and their performance is evaluated based on the defined figures of merit. Noteworthy applications of these architectures in neural recording systems are presented and their performance and implementation is briefly discussed. The reviewed amplifier architectures are compared based

on the obtained figures of merit. Based on this comparison the most optimal architectures for use in single-cell resolution BMI are chosen. Finally, commonly used and recently proposed methods used to reduce the size of passive components used in amplifier systems are presented and discussed.

1-1-1 Figures of merit

Quantifying the performance of amplifier architectures requires a set of figures of merit by which the performance of these architectures and the requirements given in table 1-2 can be compared to each other.

Consider an amplifier system consisting of an ideal bipolar junction transistor (BJT). Let B be the bandwidth of the amplifier system, I_{tot} be the total current usage of the amplifier system, k be the Boltzmann constant, T be the absolute temperature of the device and $V_T = \frac{kT}{q}$ be the thermal voltage with q the magnitude of electrical charge of an electron. The input referred RMS noise of an ideal BJT is then given by equation 1-1 [17].

$$V_{bjt,n,rms} = \sqrt{\frac{4\pi V_T kTB}{2I_{tot}}} \tag{1-1}$$

A commonly used figure of merit used to quantify and compare the performance of amplifier systems is the noise efficiency factor (NEF). The NEF is defined as the ratio of total input referred root-mean-square (RMS) voltage of the amplifier system divided by the input referred RMS noise voltage of an ideal BJT. Let $V_{in,n,rms}$ be the total input referred RMS noise voltage of an amplifier system, The NEF is then defined by equation 1-2. [17]

$$NEF = \frac{V_{in,n,rms}}{V_{bjt,n,rms}} = V_{in,n,rms}\sqrt{\frac{2I_{total}}{4\pi V_T kTB}} \tag{1-2}$$

The NEF provides circuit designers with a quantity by which amplifier performance can be measured and compared in terms of noise. A limitation of the NEF is that it does not provide any information with regards to the noise-power trade-off that is especially important in the design of lower power amplifiers. In order to quantify and compare the performance of amplifier systems in terms of noise and power usage, the power efficiency factor (PEF) is often used as an additional figure of merit. The PEF is defined by equation 1-3 with V_{dd} defined as the supply voltage of the amplifier [18].

$$PEF = NEF^2 \cdot V_{dd} \tag{1-3}$$

In order to quantify the performance of the reviewed amplifier architectures in this section of the review, the figures of merit that are used are gain, PEF and power per area per channel. In order to determine if a given amplifier is viable for use in a single-cell resolution BMI, the amplifiers obtained figures of merit are compared to the requirements given in table 1-2 are used.

1-1-2 AC-coupled capacitive feedback network amplifier

Given in figure 1-5 is a circuit diagram of the AC-coupled capacitive feedback (CFN) amplifier topology [19]. This amplifier topology is by far the most widely used neural amplifier topology currently. The gain of this topology is given by equation 1-4.

$$\frac{V_{out}}{V_{in}} = \frac{C_{in}}{C_{fb}} \tag{1-4}$$

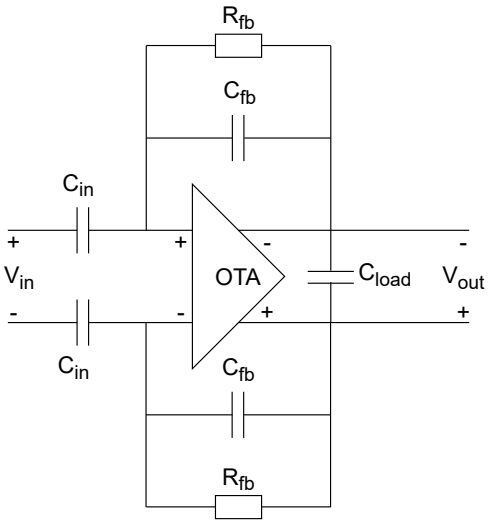


Figure 1-5: Capacitive feedback network (CFN) amplifier topology circuit diagram [19].

Capacitor ratios can be made with high accuracy resulting in CFN amplifiers obtaining highly accurate gain values. From equation 1-4 it can be determined that in order to achieve high gain values the input capacitance C_{in} must be chosen to be a large value relative to the feedback capacitance C_{fb}. Large capacitance values require large on-chip capacitors which consume large amounts of chip area.

Presented in [8] is a 200 channel neural recording system consisting of 100 current and 100 voltage sensing channels. The voltage channel consist of three CFN amplifier stages with a combined chip area of $0.03mm^2$ per channel, a PEF of 19.4, a power usage of $12.1\mu W$ per channel and a variable gain of 51.5 / 59.5 / 65.5 dB. The circuit diagram of the voltage channel is given in figure 1-6(a).

Given in figure 1-6(b) is a die micrograph of the CFN amplifier depicted in figure 1-6(a). Indicated in the red box are the input capacitors of the first gain stage C_1. The input capacitors account for roughly 88% of the first gain stage chip area and more than 50% of the entire amplifier chip area.

The input capacitors of the CFN topology take up the vast majority of the area per channel and are therefore the main bottleneck in terms of area per channel. By reducing the required input capacitance the area per channel of the amplifier can therefore be decreased.

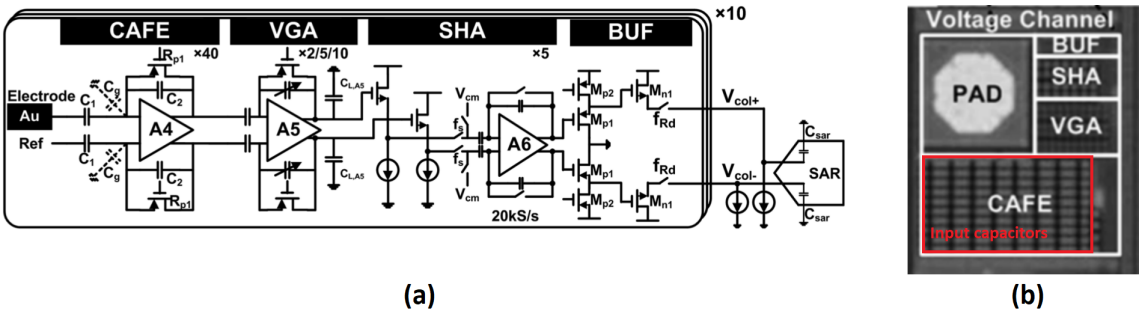


Figure 1-6: A 3-stage CFN amplifier based neural recording system (a) circuit diagram and (b) die micrograph. Depicted in the red box are the input capacitors of the first gain stage C_1. [8]

1-1-3 AC-coupled capacitive feedback network amplifier with T-network

Given in figure 1-7 is a general circuit diagram of the AC-coupled capacitive feedback amplifier with T-network (CFN+T). [20] The feedback network consists of 2 equal capacitors C_u and a shunt capacitor C_T. The equivalent feedback capacitance of this architecture is given by equation 1-5. The gain of this architecture is given by equation 1-6.

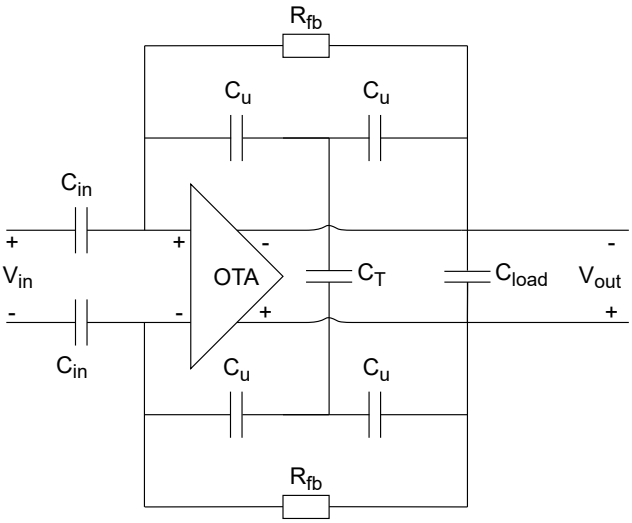


Figure 1-7: CFN with T-network (CFN+T) amplifier topology circuit diagram. [4]

$$C_{eq,fb} = \frac{C_u}{2(\frac{C_T}{C_u} + 1)} \tag{1-5}$$

$$\frac{V_{out}}{V_{in}} = \frac{C_{in}}{C_{eq,fb}} \tag{1-6}$$

Equation 1-5 implies that the use of a T-network results in a lower equivalent feedback capacitance compared to the conventional CFN amplifier. With the CFN+T architecture, the same gain specifications can be achieved with smaller input capacitors resulting in a reduction of required chip area. The lower equivalent feedback capacitance does require that

the feedback resistor R_{fb} is increased in order to maintain the bandwidth of the amplifier, which in turn leads to higher thermal noise due to the larger resistance value. [4]

Presented in [21] is a 4 channel neural amplifier system that consists of two gain stages. A circuit diagram of the used amplifier topology is given in figure 1-8(a). The amplifier system consists of two gain stages. The first stage using a CFN+T architecture and the second stage consisting of a variable gain CFN amplifier resulting in a total area per channel of $0.072mm^2$. This system achieves a PEF of 6.77, a power usage of $6\mu W$ per channel and a gain of 38.04dB.

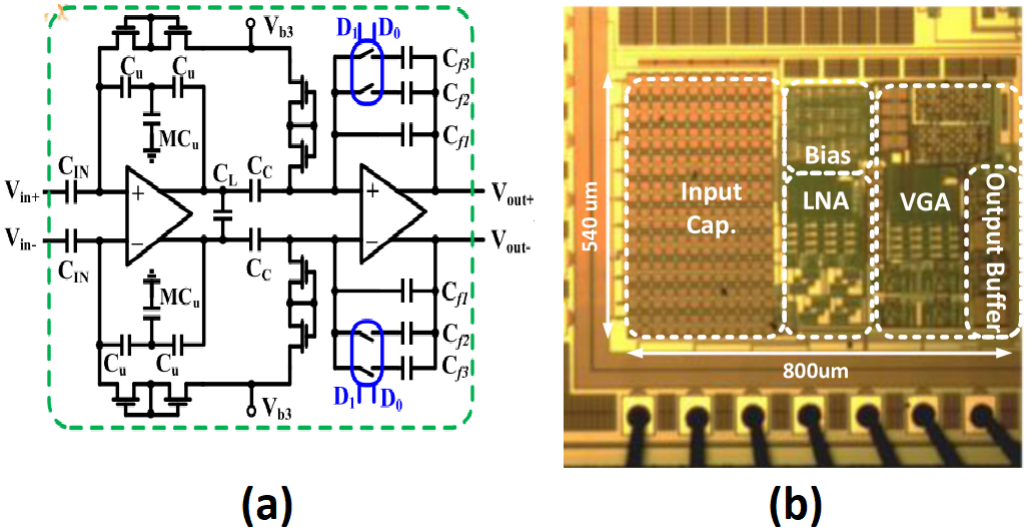


Figure 1-8: A 2 stage CFN+T amplifier based neural recording system (a) circuit diagram and (b) die micrograph. [21]

Figure 1-8(b) presents a die micrograph of the neural amplifier system. From this figure it can be concluded that the total area of the input capacitor compared to the area of the entire amplifier is reduced. Although the area of the capacitor relative to the complete system is reduced, the majority of the channel area is still dominated by the input capacitors.

1-1-4 AC-coupled open-loop amplifier

In both capacitive feedback amplifier topologies the input capacitors requires a large amount of chip area in order to provide a high gain value. By utilizing an AC-coupled open-loop amplifier the gain of the amplifier is completely determined by the gain of the OTA, thereby reducing the required size of the input capacitor pair. Figure 1-9 presents a block diagram of the general topology of an open-loop amplifier.

Compared to CFN and CFN+T architectures, open loop amplifiers suffer more from gain variations due to IC process variations. In [22] the performance of CFN and open loop amplifiers with similar gain were compared with regards to area per channel and gain variations. Figure 1-10 presents a tapeout of the CFN and open loop amplifiers. From this figure it can be concluded that the input capacitor of the open loop amplifier is approximately 7.5 times smaller compared to the input capacitor of the CFN.

The obtained gain variations in this paper were 2.1% and 0.05% for the open loop and CFN amplifier architecture respectively. Gain variations are desired to be as low as possible

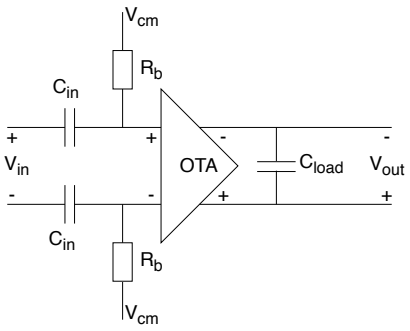


Figure 1-9: Open-loop amplifier topology circuit diagram. [4]

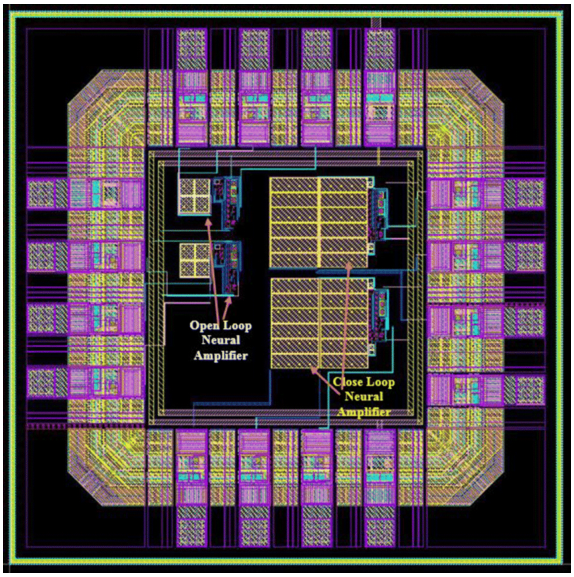


Figure 1-10: Layout level implementation of open-loop and CFN amplifiers. [22]

in amplifier systems that require high amplification precision. Note that when recording extracellular action potentials the goal is to detect the presence of spikes via spike sorting rather than specific voltage levels. Spike detection, as depicted in figure 1-4, does not require high accuracy amplification, rather, it requires enough amplification such that spikes can be detected and differentiated from the background noise present in the raw data signal. As a result, the increased gain variations of an open-loop topology in comparison to a CFN topology are not detrimental to the performance of spike detection as long as spike sorting can still be performed.

Presented in [9] is an neural recording system consisting of 2048 recording channels. The circuit diagram of this system is given in figure 1-11. The system consists of two stages, an initial AC-coupled open loop amplifier followed by a variable gain CFN amplifier. The gain of this system is further increased by the switched capacitor amplifiers A_3 and A_4. This system achieves an area per channel of $0.022mm^2$ a PEF of 13.2, a power usage of $16\mu W$ per channel and a maximum gain of 77dB.

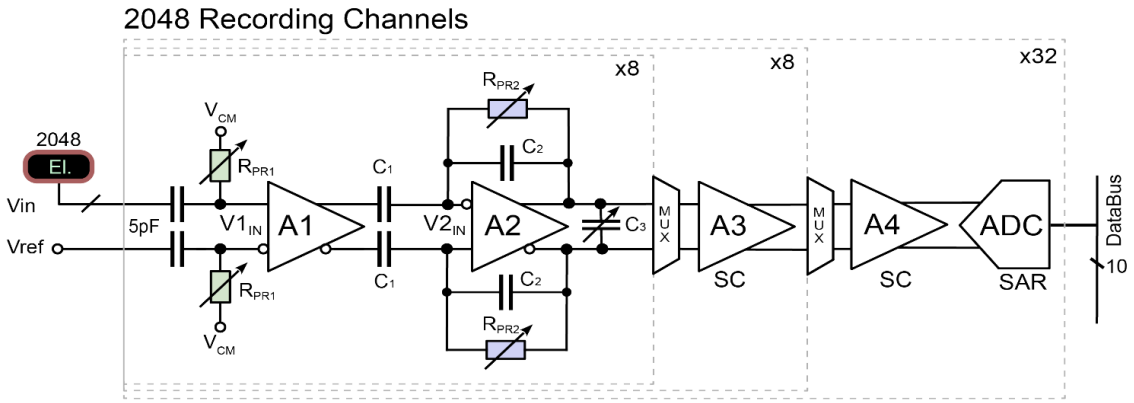


Figure 1-11: An open-loop amplifier based neural recording system [9].

1-1-5 DC servo loop amplifier

Figure 1-10 shows that, although the size of the input capacitor of an open-loop architecture is significantly smaller than that of a CFN architecture, the input capacitor still requires a roughly half of total amplifier chip area. In order to reduce or to completely remove the input capacitor while still filtering out DC and low frequency signals, Amplifiers architectures using DC servo loop (DSL) feedback have been used in literature to enable both AC and DC-coupled amplifier systems to be used for neural recording.

Figure 1-12 presents a block diagram of the general topology of a DC-coupled DSL amplifier. The gain of this architecture is provided by the amplifier gain stage consisting of an amplifier A_1 and the low-pass frequency is implemented by a low-pass filter with time constant τ_1. The DSL utilizes an amplifier A_2 and a low-pass filter with time constant τ_2 in its feedback path, creating a high-pass frequency pole at the input of the amplifier. Given in equation 1-7 is the transfer function of the amplifier. The resulting high-pass frequency f_{hp} implemented by the DSL is given by equation 1-8 [4]. Using this topology, the need for an input capacitor in order to filter out low frequencies is eliminated.

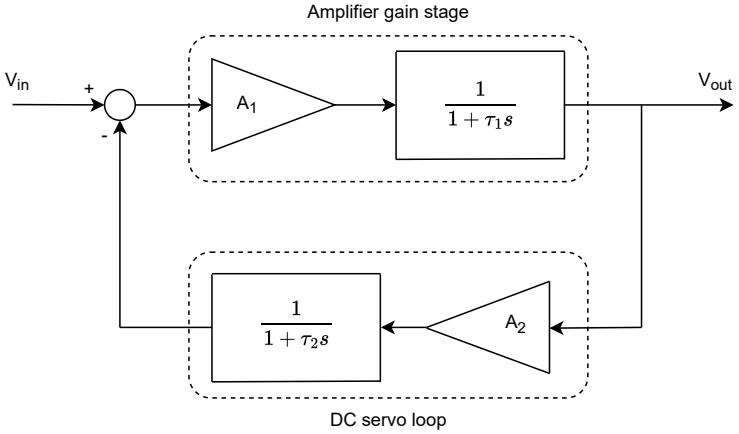


Figure 1-12: High level block diagram of a DC servo loop amplifier topology [4].

$$H_{dsl}(s) = \frac{A_1(1+\tau_2 s)}{(1+\tau_1 s)(1+\tau_2 s)+A_1 A_2} \tag{1-7}$$

$$f_{hp} = f_{dsl,0}\,(1+A_1A_2)\ \text{, with } f_{dsl,0} = \frac{1}{2\pi\tau_2} \tag{1-8}$$

Unlike the previously discussed AC-coupled amplifiers which completely remove the DC-offset component at the input, the DSL amplifier only attenuates the DC-offset present at the input of the amplifier system. The attenuation factor of the DC-offset is calculated by equation 1-9. The choice of value A_2 depends on a trade-off between the desired DC-offset attenuation and required high pass frequency f_{hp}. In order suppress the DC-offset as much as possible, a high value for A_2 is required. An increasing value of A_2 results in an increasing value of f_{hp} as can be concluded from equation 1-8. In order to reduce the f_{hp} value, a low value of $f_{dsl,0}$ is required. A low value for $f_{dsl,0}$ requires the use of large capacitor values which in turn requires large amounts of chip area. Therefore a design trade-off needs to be made between the area per recording channel and the desired DC-offset attenuation when implementing DSL amplifiers.

$$lim_{s\to 0} H_{dsl}(s) = \frac{A_1}{1+A_1A_2} \approx \frac{1}{A_{dsl}} \tag{1-9}$$

Presented in [38] is an 8 channel neural recording system using a DC-servoloop amplifier system. Using an integrator to implement the low-pass filter in the feedback network, this system achieves an area per channel of $0.071mm^2$ with a PEF of 28.8 and a gain of 26dB. This system also contains a positive feedback loop used to increase the DC input impedance to $300M\Omega$.

The most area efficient DSL amplifier architecture is presented in [7]. Presented in this paper is a 56 channel neural recording system using a DC-coupled DSL amplifier system. The circuit diagram of this system is given in figure 1-13. This system achieves an area per channel of $0.018mm^2$ with a PEF of 58.5 and a gain of 52dB.

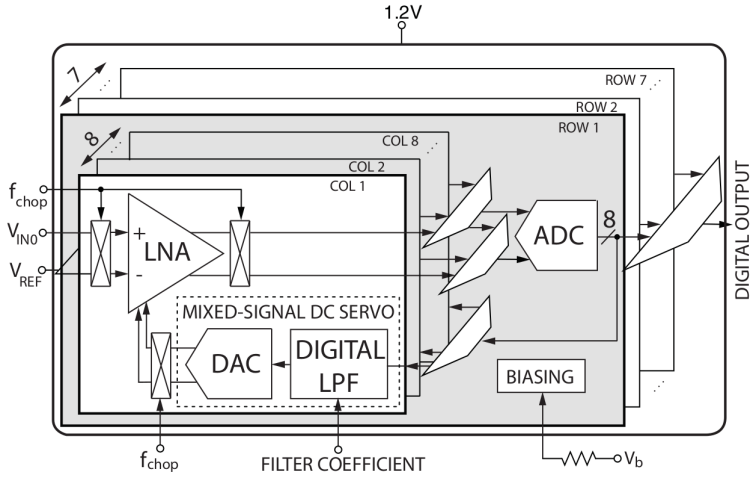


Figure 1-13: A mixed-signal DC servo loop neural recording system presented in [7].

As can be seen in the circuit diagram given in figure 1-13, this recording system uses a mixed-signal DSL feedback network consisting of digital and analog signal processing components. The low-pass pole in this DSL architecture is implemented using a digital low-pass filter. Low-pass filtering in the digital domain has the benefit of being both power and area efficient [23].

This system also uses chopper modulation to reduce the effects of $1/f$-noise which dominate at the lower frequencies. The chopper modulation frequency f_{chop} regulates the switching frequency of the chopper. Chopper modulation also leads to a reduction in input impedance of the amplifier, the implementation of chopper modulation therefore requires a design trade-off to be made with regards to the $1/f$-noise and input impedance [24].

The addition of active feedback introduces a significant amount of noise to the amplifier resulting in relatively high NEF/PEF values compared to the previously studied architectures. The authors of [24] addressed the increased noise of the DSL by designing an AC-coupled CFN amplifier with 3 transconductance blocks where the DSL is employed over the second and third transconductance block. By doing so, the input referred noise contribution of the DSL is attenuated by the gain of the first transconductance block. The circuit diagram of the amplifier is given in figure 1-14 [24].

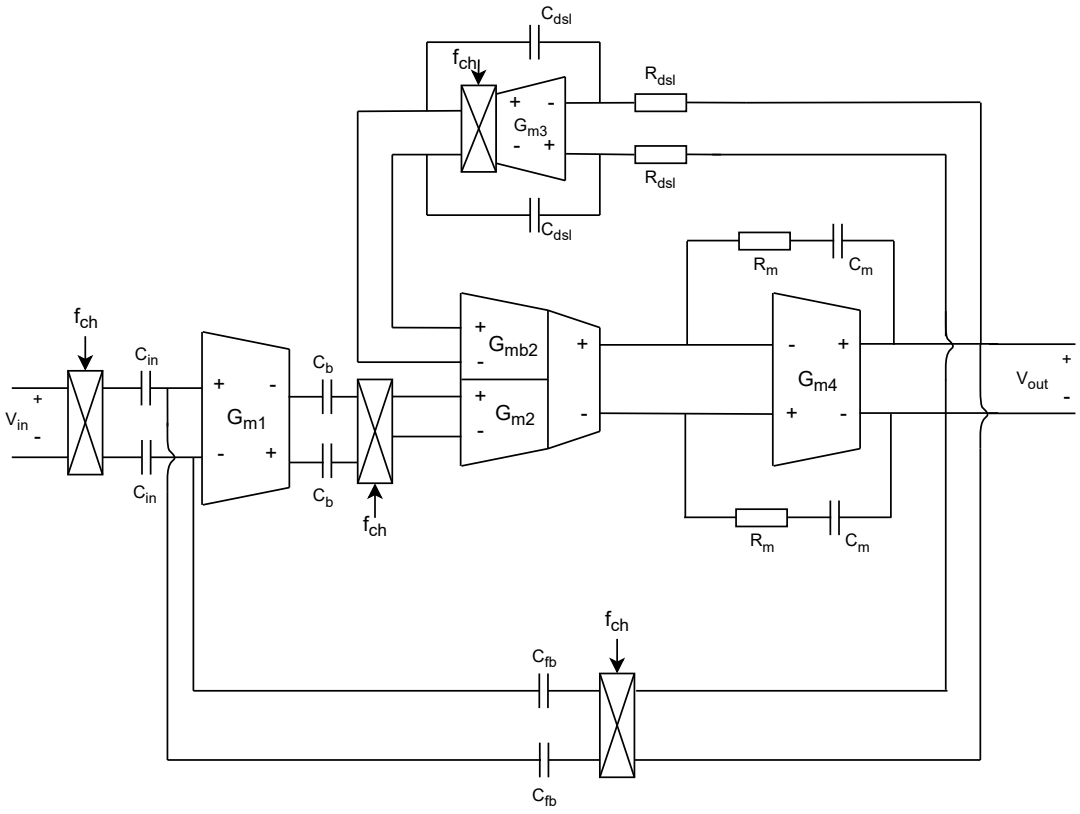


Figure 1-14: An amplifier with a DC servo loop over G_{m2} and G_{m4} using body controlled feedback presented in [24].

Rather than using passive components to employ feedback, the authors of [24] employ feedback from the output of the amplifier to the body terminal of the input transistor devices of G_{m2}. The circuit level implementation of the body controlled feedback of G_{m2} is illustrated in figure

1-15. The advantage of this technique is that the noise of the DSL is attenuated by the ratio of the body transconductance divided by the transconductance $\eta = \frac{G_{mb2}}{G_{m2}}$. This attenuation ratio in combination with the attenuation of due to G_{m1} results in the total input referred noise contribution of the DSL to be 12.5%.

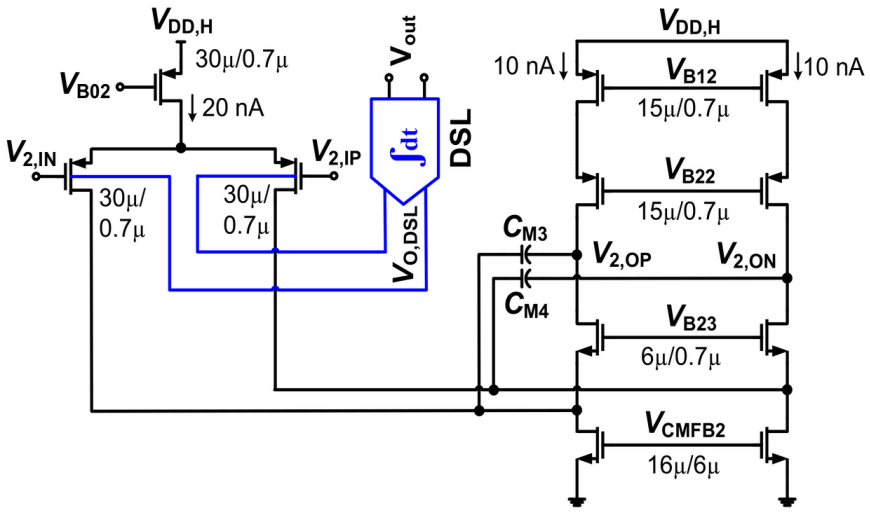


Figure 1-15: OTA implementation of G_{m2} using body controlled feedback on input transistor devices presented in [24].

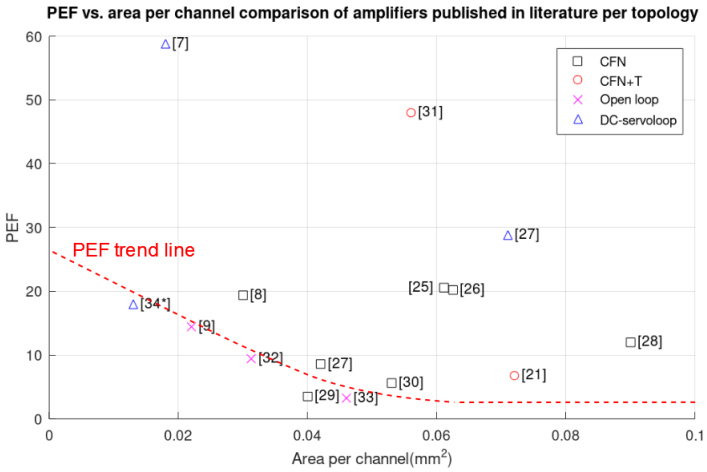
When employing body controlled feedback, care should be taken to prevent the body diode of the transistor device from becoming forward biased in order to ensure proper functioning of the transistor device. In order to achieve this, the voltage at the body terminal must not exceed the cut-in voltage of body diode. Due to this requirement, the maximum allowable voltage swing of the DSL is limited. This results in body controlled feedback being unable to be used in applications where large voltage swings are required by the DSL.

1-1-6 Comparison

In order to determine which architectures offer the best performance for use in single-cell resolution BMI, recently published neural recording amplifier systems used in are compared based on PEF and gain per area per channel.

Given in figure 1-16 the PEF per area per channel values of the studied amplifier designs during this literature review. Of all the studied architectures, The open-loop and DC-servoloop architectures provide the best performance in terms of PEF per area per channel . Of these two architectures the open loop architecture achieves the lowest PEF value. The resulting PEF trend line shows that for decreasing area per channel the PEF increases.

Given in figure 1-17 are the gain per area per channel values of the of the studied amplifier designs during this literature review. In general, all architectures are capable of achieving the specified gain requirement with the open loop architecture providing the highest gain per area per channel. The gain trend line shows that for decreasing area per channel the gain decreases.



* Uses off-chip components

Figure 1-16: A comparison in terms of PEF versus area per channel of amplifiers published in literature.

Based on figures 1-16 and 1-17, the results of the comparison are given in Table 1-3. Of the amplifiers studied during this review, the architecture that performed the best in terms of gain per area per channel is the open loop amplifier architecture followed by the DC-servoloop. The DC-servoloop architecture achieved the best area per channel.

Table 1-3: Results of amplifier topology comparison

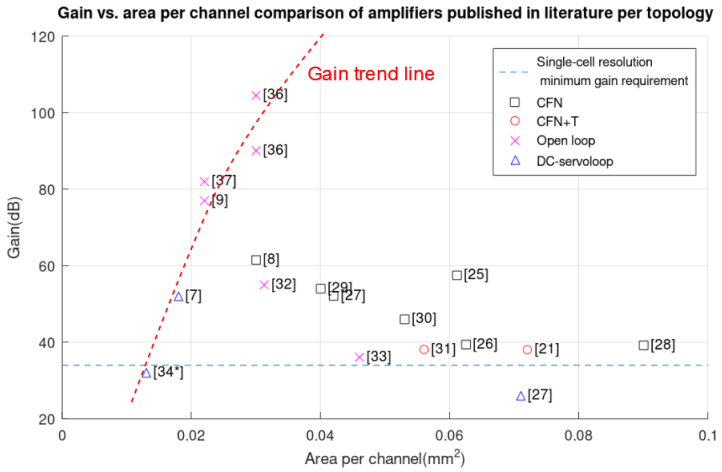
Topology	References	Area	Gain	PEF
CFN	[8], [25], [26], [28–30], [39–48]	-	+	++
CFN+T	[20], [21], [31], [32]	- -	+	+
Open-loop	[9], [33], [34], [35], [36]	+	++	++
DC-servoloop	[7], [24], [37], [38]	++	+	- -

1-1-7 Passive components

The studied amplifier architectures show that large amounts of chip area are consumed by the passive components present in the circuit. In recent literature, various novel methods have been presented to decrease the size of these passive components in order to achieve both lower area requirements and to decrease the noise contributions of the components.

In order to implement low cut-off frequencies, high time constants are needed which require large resistance values. Standard resistors require large amounts of chip area as the value of the resistor increases [14]. Since the thermal noise of a resistor is proportional to the square root of the resistance value, large resistor values result in high thermal noise sources, decreasing the noise performance of the amplifier system.

Rather than using standard resistors, transistor devices can be used to substitute the resistances used in amplifier designs. These transistors are referred to as pseudo-resistors and often used in neural amplifier systems. [49] Presented in figure 1-18 are circuit diagram of a commonly used pseudo resistors, the performance of which are further discussed in [50].



* Uses off-chip components

Figure 1-17: A comparison in terms of gain versus area per channel of amplifiers published in literature.

The resistance through the pseudo resistor is controlled by biasing the gates of the transistor devices. Compared to standard resistors, the use of pseudo-resistors results in both a reduction in generated noise and a reduction of required chip area, making pseudo-resistors good alternatives for conventional resistors. [51]

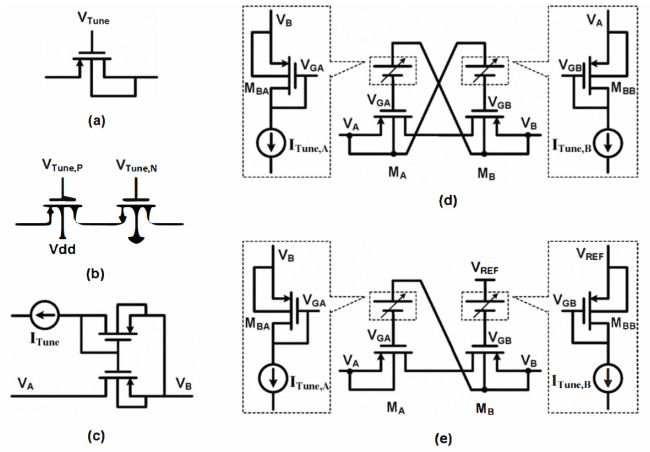


Figure 1-18: Five types of pseudo resistors used in literature. (a) voltage-controlled transistor, (b) complementary structure, (c) current-controlled transistor, (d) cross-coupled structure, and (e) pseudo cross-coupled structure. [50]

Pseudo resistors are widely used in the design of neural amplifier systems but the performance of these devices is highly sensitive to process variations, voltage variations and temperature. [52] Due to these sensitivities, resistance values may vary by a factor of 100. [38] Pseudo resistors are also known to be very nonlinear. [38] Presented in [53] and [54] are pseudo resistor implementations that achieve enhanced robustness against process variations. Although these pseudo resistor implementations are more robust then the resistors presented in figure 1-18, implementation of these pseudo resistors introduces both an increased area and power overhead due to the required additional pseudo resistor biasing circuitry.

An alternative to pseudo resistors is used in [38]. The amplifier system presented in this paper uses a DC-servoloop to filter out the low frequency signals, the integrator used in the DC-servoloop still requires the use of passive components that take up a large amount of chip area. In order to reduce the size of these components, duty-cycled resistors are used. Illustrated in figure 1-19 is the opamp-based integrator used to implement the DC-servoloop of this amplifier system. Using this integrator a low-pass frequency of $f_{ugb} = 0.2$Hz was achieved using $C_{int} = 20$pF and $R = 1$MΩ duty-cycled at $D = 1/40000$ with a 25kHz clock signal, resulting in an equivalent resistance $R_{eq} = 40$GΩ.

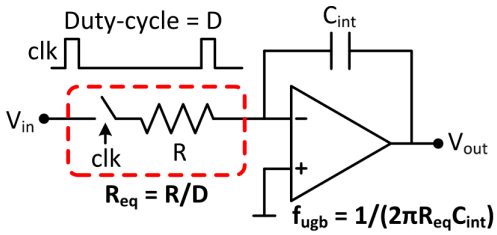


Figure 1-19: DC-servoloop integrator implementation using a duty-cycled resistor. [38]

Duty-cycled resistors can achieve very high resistance values while being area efficient using relatively simple switching circuitry compared to the biasing circuitry required for pseudo resistors. With the duty-cycled resistors presented in [38], resistance values were achieved with an overall variation of 35%. Duty-cycled resistors can therefore be used as an alternative to pseudo resistors.

1-2 OTA architecture

Whereas the total required chip area of an amplifier system is dominated by the passive components of the amplifier architecture, the power usage and noise behaviour of the amplifier is dominated by the active components of the OTA. In this section, OTA architectures are presented and discussed. The performance of each presented OTA architecture is reviewed based on the theoretical minimum obtainable NEF and PEF values, CMRR and PSRR. Notable applications of each OTA architectures published in literature are presented and briefly discussed.

1-2-1 Differential pair

The most straightforward and commonly used OTA architecture is the differential pair amplifier. Given in figures 1-20(a) and (b) are differential pair amplifier diagrams using ideal load and biasing with NMOS and PMOS input devices respectively.

Let $g_{mn,mp}$ be the small-signal transconductance, $r_{on,op}$ be the small-signal output resistance and γ the device specific noise factor. The small-signal gain and input referred noise voltage are then given by equations 1-10 and 1-11 respectively.

$$A_{diff} = \frac{V_{out}}{V_{in}} = -g_{mn,mp} r_{on,op} \tag{1-10}$$

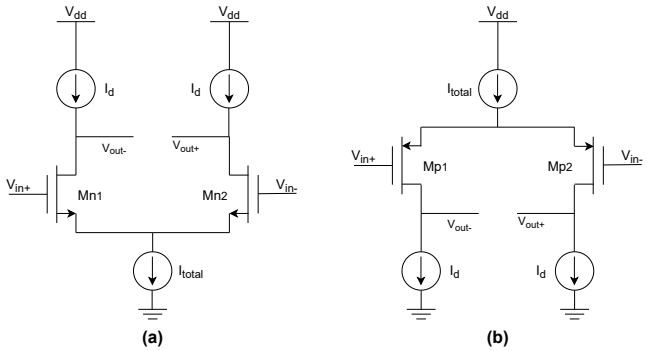


Figure 1-20: Diagrams of differential pair using ideal load and supply current sources using (a) NMOS and (b) PMOS input devices

$$V_{in,rms,diff}^2 = 2 \cdot \frac{4kT\gamma B}{g_{mn,mp}} \tag{1-11}$$

Substitution of equation 1-11 in equation 1-2 then yields the NEF of a differential pair OTA using ideal current sources in equation 1-12. Assuming $\gamma = 1$, $V_T = 26\text{mV}$ and $\frac{g_{mn,mp}}{I_D} = 25V^{-1}$, the minimum obtainable NEF value using a differential pair OTA is given in equation 1-13.

$$NEF_{diff} = \sqrt{\frac{8\gamma}{\pi V_T} \cdot \frac{I_D}{g_{mn,mp}}} \tag{1-12}$$

$$NEF_{diff,min} \approx 2 \tag{1-13}$$

Assume that the load current sources and tail current source are implemented using single MOS transistors, also assume the voltage drop over the input transistors, load and tail current source is equal to the minimum required drain-source voltage $V_{ds,min}$. The minimum required supply voltage $V_{dd,min}$ is then calculated to be $V_{dd,min} = 3V_{ds,min}$. Recalling the definition of the PEF given in equation 1-3 and the minimum obtainable NEF for the differential pair given by equation 1-13, the minimum obtainable PEF is then given by equation 1-14.

$$PEF_{diff,min} \approx 12V_{ds,min} \tag{1-14}$$

Many differential pair OTA for use in neural recording amplifiers have been published in literature. An example of an often used differential pair implementation is found in [55], the circuit diagram of this OTA is given in figure 1-21. The folded-cascode architecture is used to increase the gain and output resistance of the OTA while also lowering the required supply voltage. By using the folded-cascode architecture, the authors of [55] achieved a NEF and PEF of 2.31 and 4.27 respectively.

1-2-2 Inverter-based

Equation 1-12 provides an expression of the NEF as a function of the g_m/I_D ratio. From this equation it can be determined that by increasing the g_m/I_D ratio the minimum obtainable NEF and PEF can be decreased. The g_m/I_D ratio can be increased by increasing the

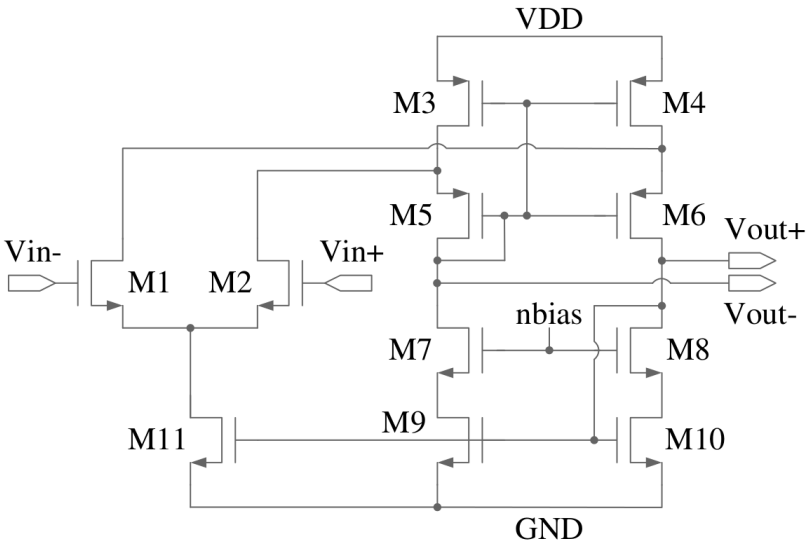


Figure 1-21: Circuit diagram of a differential pair OTA using a folded-cascode architecture. [55]

equivalent transconductance of the amplifier g_m while maintaining a constant drain current I_D.

The inverter-based OTA achieves this using both NMOS and PMOS transistors as input devices. Given in figure 1-22 is a diagram of the inverter-based OTA architecture. Given in equations 1-15 and 1-16 are the small-signal gain and input referred RMS noise voltage of the inverter-based OTA architecture respectively.

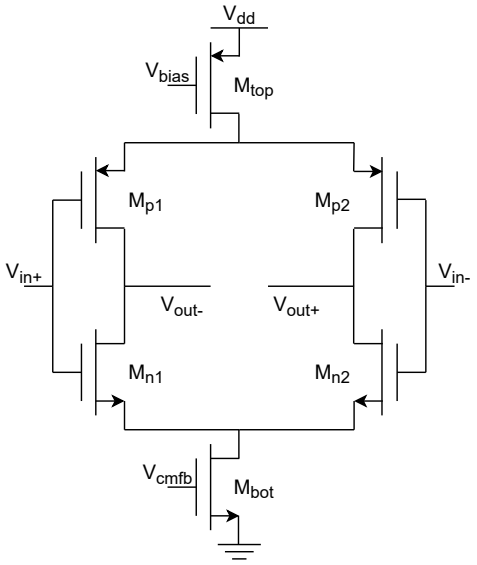


Figure 1-22: Diagram of an inverter-based OTA

$$A_{inv} = \frac{V_{out}}{V_{in}} = -(g_{mn} + g_{mp})(r_{on}||r_{op}) \tag{1-15}$$

$$V_{in,rms,inv}^2 = 4 \cdot \frac{4kT\gamma(g_{mn}+g_{mp})B}{(g_{mn}+g_{mp})^2} = \frac{16kT\gamma B}{g_{mn}+g_{mp}} \tag{1-16}$$

Assuming the transconductance of the PMOS g_{mp} and NMOS g_{mn} to be equal to g_m, the total equivalent transconductane of the inverter-based OTA is then given by $g_{mn}+g_{mp} = 2g_m$. Assuming again the values $\gamma = 1$, , $V_T = 26$mV and $g_m/I_D = 25V^{-1}$, the minimum obtainable NEF of the inverter-based OTA is then given by equation 1-18. Assume as well that the tail current sources are implemented with single MOS transistors and that the voltage drop over each transistor equals $V_{ds,min}$, the minimum supply voltage is then calculated to be $V_{dd,min} = 4V_{ds,min}$ and the minimum obtainable PEF is then given by equation 1-19.

$$NEF_{inv} = \sqrt{\frac{4\gamma}{\pi V_T} \cdot \frac{I_d}{g_{mn}+g_{mp}}} \tag{1-17}$$

$$NEF_{inv,min} \approx 1.4 \tag{1-18}$$

$$PEF_{inv,min} \approx 7.84V_{ds,min} \tag{1-19}$$

Compared to the obtained minimum NEF and PEF results of the differential pair architecture given in equations 1-13 and 1-14 respectively, the inverter-based architecture achieves improved minimum obtainable NEF and PEF values. From the obtained results it can be concluded that increasing the equivalent transconductance of the OTA results in a higher g_m/I_D ratio and in a decrease in minimum obtainable NEF and PEF values.

Inverter-based OTA are increasingly being used in neural recording amplifier applications due to its higher equivalent transconductance compared to the differential pair OTA. Presented in [56] is a CFN amplifier using a self-biased inverter-based OTA. The OTA architecture is given in figure 1-23. The use of self-biasing allows for a low power and low area OTA implementation that does not require common-mode feedback to set the output common-mode voltage.

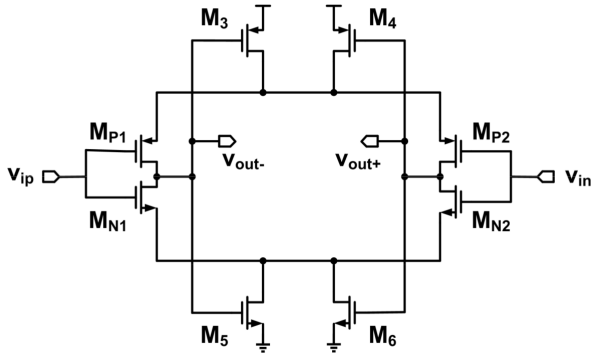


Figure 1-23: A self-biased invirter-based OTA [49] [56].

Presented in [44] is a CFN amplifier using a telescopic inverter-based OTA, the circuit diagram of this OTA is given in figure 1-24. This architecture achieves higher gain an output impedance due to the addition of cascode devices $M_{5,6,7,8}$. Using this architecture the final amplifier achieved a gain of 26dB, a NEF and PEF of 1.52 and 2.77 respectively, a CMRR of $>$ 60dB, a PSRR of $>$ 80dB and a total power usage of 0.43μW

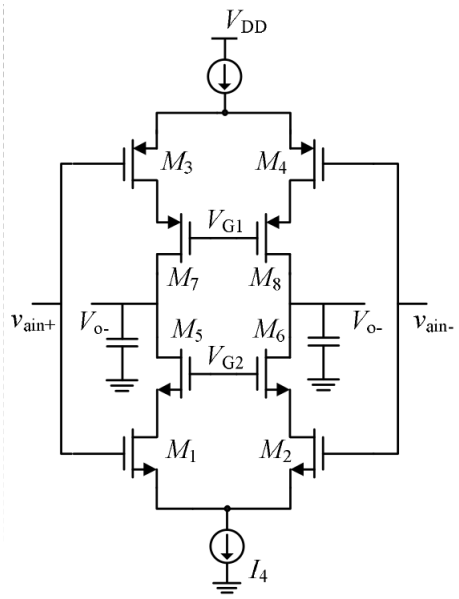


Figure 1-24: A telescopic inverter-based OTA.

Presented in [57] is a CFN amplifier that uses a squeezed inverter-based input stage followed by a two stage folded-cascode OTA. Given in figure 1-25 is a circuit diagram depicting the squeezed inverter-based input stage concept. The input stage operate at a supply voltage of 0.2V while the folded-cascode stage operates at a supply voltage of 0.8V. The low voltage input stage is used to draw a high current in order to reduce the input referred noise while the higher voltage gain stage is used to provide the gain and output signal swing. By using this method, the amplifier achieves high noise efficiency, high gain and signal swing. The final amplifier presented in this paper achieved a gain of 57.8dB, a NEF and PEF of 2.1 and 1.6 respectively, a CMRR of 80dB and a PSRR of 80dB.

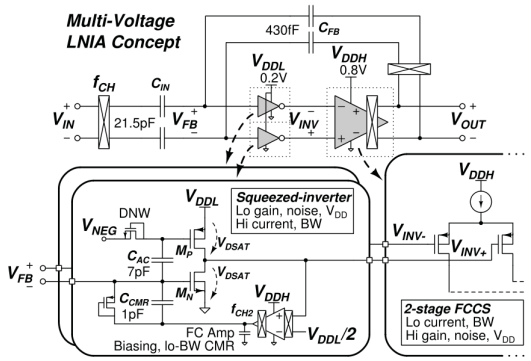


Figure 1-25: Circuit diagram of the squeezed inverter OTA presented in [57].

1-2-3 Amplifier stacking

Notice that the inverter-based OTA architecture depicted in figure 1-22 achieves a higher equivalent transconductance by effectively reusing the same drain current that flows through

the PMOS input devices for the NMOS input devices, resulting in an increased equivalent transconductance g_m while maintaining a constant drain current I_D. This concept of current reuse can be further exploited by using a single current source to supply a current for multiple OTAs. Given in figure 1-26 is a diagram in which this current reuse amplifier stacking technique is depicted. By effectively reusing the supply current I_{total} over the N-times stacked OTA devices the drain current I_D is kept constant while the amount of input device is multiplied by N. Resulting in the gain and g_m/I_D ratio given by equations 1-20 and 1-21 respectively.

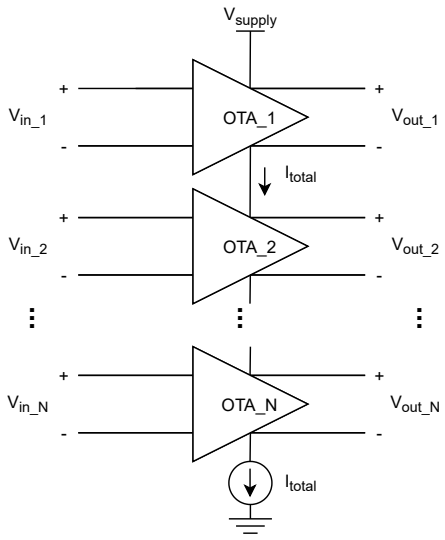


Figure 1-26: High level overview diagram of the amplifier stacking technique using N OTA [58].

$$\left(\frac{V_{out}}{V_{in}}\right)_{N-stack} = \frac{V_{out\_1}}{V_{in\_1}} = \frac{V_{out\_2}}{V_{in\_2}} = ... = \frac{V_{out\_N}}{V_{in\_N}} \tag{1-20}$$

$$\left(\frac{g_m}{I_D}\right)_{N-stack} = \frac{g_{m1}}{I_D} + \frac{g_{m2}}{I_D} + ... + \frac{g_{mN}}{I_D} = N \cdot \frac{g_m}{I_D} \tag{1-21}$$

The OTAs used in the amplifier stacking topology given in figure 1-26 can either be implemented using a differential pair or an inverter-based topology. Substitution of equation 1-21 in equations 1-12 and 1-17 yields the NEF value of an N times stacked differential pair and inverter-based amplifier given by equations 1-22 and 1-23 respectively.

$$NEF_{diff,N-stack} = \sqrt{\frac{8\gamma}{\pi N V_T} \cdot \frac{I_D}{g_{mn,mp}}} \tag{1-22}$$

$$NEF_{inv,N-stack} = \sqrt{\frac{8\gamma}{\pi N V_T} \cdot \frac{I_D}{g_{mn} + g_{mp}}} \tag{1-23}$$

Assuming again that $\gamma = 1$, $V_T = 26\text{mV}$ and $\frac{g_m}{I_D} = 25V^{-1}$ the minimum obtainable NEF values for an N times stacked differential pair and inverter-based amplifier can be calculated using equations 1-22 and 1-23 respectively. The results of these calculations are given in figure

1-27. From this figure it can be concluded that the minimum obtainable NEF decreases as the number of stacked OTA N increase. From the figure it can also be determined that $NEF < 1$ values are achieved when $N \geq 2$ for inverter-based amplifiers and $N \geq 4$ for differential pair amplifiers.

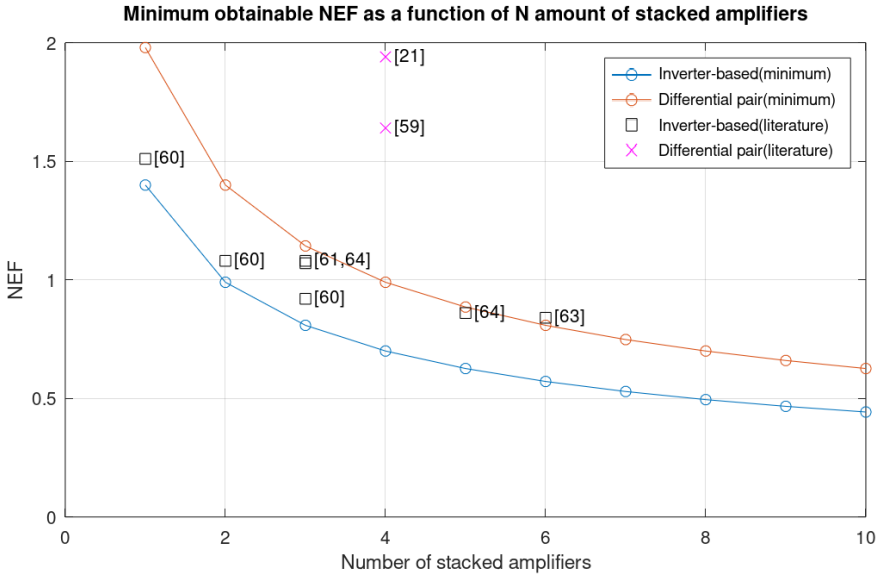


Figure 1-27: Minimum obtainable NEF values of the N-stacked differential pair and inverter-based OTA architecture as a function of N. Included in the figure are the obtained NEF values of OTA found in literature

Assuming again that the tail current sources are implemented with single MOS transistors and that the voltage drop over each transistor equals $V_{ds,min}$. The minimum required supply voltages for an N-times stacked differential pair and inverter-based OTA are then given by equations 1-24 and 1-25 respectively. The resulting PEF as a function of N of the differential pair and inverter-based OTA are then given by equations 1-26 and 1-27 respectively.

$$V_{dd,diff,N} = NV_{ds,min} + 2V_{ds,min} = (N+2)V_{ds,min} \tag{1-24}$$

$$V_{dd,inv,N} = 2NV_{ds,min} + 2V_{ds,min} = (2N+2)V_{ds,min} \tag{1-25}$$

$$PEF_{diff,N-stack} = \left(1 + \frac{2}{N}\right)\left(\frac{8\gamma}{\pi V_T} \cdot \frac{I_d}{g_m}\right) V_{ds,min} \tag{1-26}$$

$$PEF_{inv,N-stack} = \left(1 + \frac{1}{N}\right)\left(\frac{8\gamma}{\pi V_T} \cdot \frac{I_d}{g_m}\right) V_{ds,min} \tag{1-27}$$

Using equations 1-26 and 1-27 the PEF of the differential pair and inverter-based N-stack can be plotted as a function of N. Given in figure 1-28 are the normalised minimum obtainable PEF as a function of N using differential pair and inverter-based OTA stacking. From this figure it can be concluded that OTA stacking using both architectures results in a reduction in minimum obtainable PEF. Included in this figure as well are the PEF values obtained in literature using N-times stacked OTA architectures.

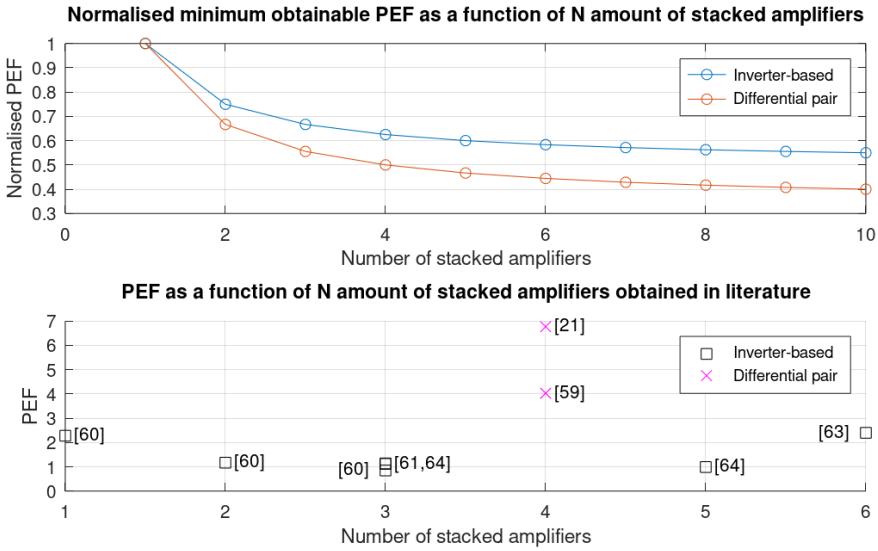


Figure 1-28: Comparison of minimum obtainable normalised PEF values(top) and PEF values found in literature(bottom) of the N-times stacked differential pair and inverter-based OTA architecture.

Summarised in Table 1-4 are the effects of OTA stacking on various OTA parameters based on the results obtained in this subsection and [58]. From this table it can be concluded that the best NEF and PEF values are obtained when N is chosen to be as high as possible. In practical applications however, the amount of stacked OTA is limited by the available supply voltage, required input and output impedance and required output voltage swing.

Table 1-4: The effects on OTA performance parameters of an N-times stacked differential pair and inverter-based OTA architecture [58]

Parameter	**Effect**	
	Differential pair N-stack	**Inverter-based N-stack**
Gain	-	-
gm/Id ratio	$\uparrow$ N $\times$	$\uparrow$ N $\times$
NEF_{min}	$\downarrow \sqrt{N}$ $\times$	$\downarrow \sqrt{N}$ $\times$
PEF_{min}	$\downarrow$(1+(2/N)) $\times$	$\downarrow$(1+(1/N)) $\times$
$\text{V}_{dd,min}$	$\uparrow$(N+2) $\times$	$\uparrow$(2N+2) $\times$
Z_{in}	$\downarrow$ N $\times$	$\downarrow$ N $\times$
Z_{out}	$\downarrow$ N $\times$	$\downarrow$ N $\times$
Chip area	$\uparrow$ N $\times$	$\uparrow$ N $\times$

1-2-4 Partial OTA sharing

Presented in [26] is a CFN amplifier using a partial OTA sharing architecture. Given in figure 1-29 is a circuit diagram of the partial OTA sharing architecture. This architecture utilises

a shared reference branch for multiple input branches, resulting in a more area and power efficient OTA architecture.

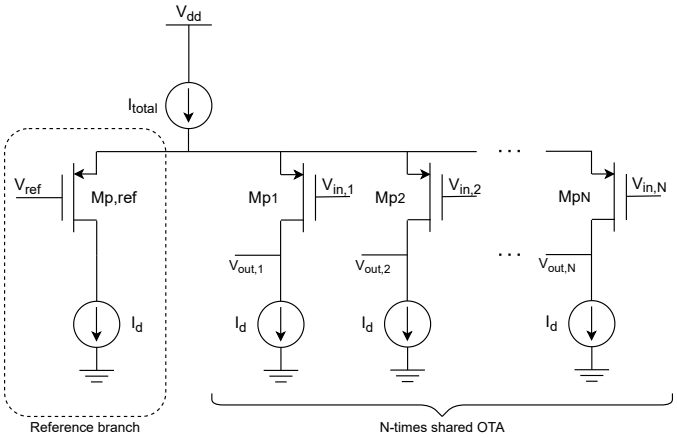


Figure 1-29: Circuit diagram of a partial OTA sharing architecture using N PMOS differential pair OTA with ideal tail and load current sources. [26]

Let N be the amount of partial shared OTA. The NEF of the N-times shared OTA is then given by equation 1-28 [26]. Similar to the amplifier stacking, the equation shows that the NEF decreases as N increases.

$$NEF_{diff,N-shared} = NEF_{diff}\sqrt{\frac{N+1}{2N}} \tag{1-28}$$

Compared to the stacking OTA architecture, the minimum required supply voltage of the partially shared OTA does not increase as N increase. Unlike the stacked OTA architecture however, the total supply current increases by a factor of $1 + N$. The partially shared OTA architecture is therefore a better option than the stacked OTA architecture when using low supply voltages.

The main drawback of the partially shared OTA is caused by the common-source node of the input transistor devices. In conventional OTA this node forms a virtual ground due to the symmetry of the circuit. In partially shared OTA implementations this symmetry is no longer present and thus the common-source node is no longer a virtual ground. This results in a phenomena where a signal presented at input $V_{in,i}$ with $1 \leq i \leq N$ will result in an output signal at a non-corresponding output $V_{out,j}$ with $j \neq i$. This phenomena is called gain leakage and is defined by equation 1-29 [26].

$$H_{leak}(s) = \frac{V_{out,j}(s)}{V_{in,i}(s)} \text{ , with } 1 \leq i, j \leq N \text{ and } i \neq j \tag{1-29}$$

Let $H_s(s)$ be the gain of the partially shared OTA input $V_{in,i}$ to output $V_{out,i}$, the crosstalk caused the by gain leakage from one of the inputs to a non-corresponding output is then given by equation 1-30 [26]. Assuming that the output of the amplifier is connected to an analog-to-digital converter. In order to accurately amplify and further process the input signals without interference from gain leakage, the crosstalk must be lower than the dynamic range of the

analog-to-digital converter. As stated in [26], the crosstalk is a function of the amount of branches N of the partially shared OTA and therefore forms the main bottleneck limiting N. As a result, the authors of [26] limited the amount of the N-shared OTA to $N = 4$ to achieve a crosstalk of -43.5dB in order to allow for a 7 bit analog-to-digital converter. In this paper the authors reported a gain of 39.4dB, a CMRR of 70.1dB, a PSRR of 63.8dB and a NEF and PEF of 3.35 and 20.2 respectively.

$$Crosstalk = 20log_{10} \left| \frac{H_{leak}(s)}{H_s(s)} \right| \tag{1-30}$$

1-3 Future work

In this section, future work regarding neural amplifier designs for single-cell resolution BMI are discussed based on the results presented in this review.

In neural amplifier system, resistors are commonly implemented using pseudo resistors. Based on the passive component review in section 1-1, the duty-cycled resistance method used in [38] can be used to achieve better resistance implementations compared to the more commonly used pseudo resistors, although they achieve lower resistance values compared to pseudo resistors. Based on the requirements of the specific BMI implementation, a choice needs to be made regarding which resistor implementation is to be used.

Based on the results presented in figures 1-16 and 1-17 and in table 1-3, both the studied open-loop and DC-servoloop amplifier architectures have the gain and area per channel requirements stated in table 1-2. Based on the requirements of the specific BMI implementation, a choice has to be made between an open-loop and DC-servoloop amplifier topology.

All OTA architectures presented in section 1-2 have been successfully used in neural recording systems. Some of the presented amplifier systems even use both differential pair and inverter-based OTA to implement multiple gain stages. Depending on the requirements of the specific BMI implementation, a choice has to be made regarding which OTA architectures are to be used.

In the event that a stacked OTA architecture is to be used. Based on the results presented in figures 1-27 and 1-28, choosing higher values of N for an N-times stacked OTA leads to lower NEF and PEF values. In practical applications the value of N is limited mainly by the available supply voltage, required voltage output swing and input and output impedance. These parameters are application specific. Therefore a choice has to be made for the value of N of the N-times stacked OTA.

Instead of a stacked OTA architecture, a partially shared OTA architectures can also be used. Like the stacked architecture, partially shared OTA offer lower NEF and PEF values while not being limited to the available supply voltage. In the event that a partially shared OTA architecture is to be used. Choosing higher values of N for an N-times partially shared OTA leads to lower NEF and PEF values but increases the crosstalk between recording channels.

All presented OTA architectures in section 1-2 assumed ideal tail and load current sources. In practically applications, these current sources are implemented using MOS transistor devices which require biasing in order to deliver the required biasing current. Biasing requires the implementation of separate biasing circuits. Self-biasing, as presented in [56] can also be used.

1-4 Conclusion

High channel count, single-cell resolution BMI require neural amplifier designs that are area, noise and power efficient. The necessity, challenges and requirements of the amplifier were presented and briefly discussed within the context of single-cell BMI applications. This literature reviewed both amplifier architectures and OTA architectures for use in single-cell resolution BMI.

Amplifier architectures were discussed and compared based on gain and PEF per area per channel obtained in recently published literature. Novel methods used in literature to reduce the required area of passive components used in amplifier architectures were also briefly discussed. The amplifier architecture comparison concluded that both the open-loop and DC-servoloop architectures achieved the best performance for use in single-cell BMI applications.

OTA architectures were evaluated on theoretical minimum obtainable NEF and PEF values, required minimum supply voltage and input and output impedance. The performance of OTA architectures published in recent literature were compared and briefly discussed. By opting for an inverter-based OTA, the NEF and PEF of the amplifier can be improved compared to the conventional differential pair OTA. NEF and PEF values can be further improved by opting for a stacked OTA architecture or by using a partial OTA sharing architecture.

System level design overview

In this chapter the system level design of the proposed compact neural amplifier for next-generation single-cell resolution BMI is presented and discussed. Section 2-1 presents the system level design considerations of pixel matched neural amplifier systems based on findings in the literature review of chapter 1 and introduces the main concept of the proposed amplifier. Section 2-2 discusses the cross-correlation of neural signals recorded in close proximity and its application in the proposed amplifier. To conclude, section 2-3 presents the system level design of the proposed neural amplifier and the required specifications.

2-1 Amplifier architecture considerations

The amplifier must enable the BMI to detect action potentials. Both the AC-coupled open-loop (OL) and DC servo loop (DSL) amplifier architectures offer the best performance for single cell resolution neural amplification, as discussed in Chapter 1. Since neural recording is performed on multiple electrodes simultaneously to capture the spatiotemporal correlation of neural signals, the amplifier is placed within an amplifier array structure called a pixel array. In order to maximise the number of recording channels the pixel pitch must match the neuron pitch of$50\mu m$, as per the specifications for the single-cell resolution amplifiers given in Table 1-2.

Various amplifier architectures can be used to implement the pixel amplifier, a selection of these architectures were studied in Chapter 1 based on suitibility for use in single-cell resolution recording systems. In terms of power efficiency factor (PEF) per area per recording channel, the OL and DSL performed the best compared to the other studied architectures as can be concluded from figure 1-16. From this figure it was determined that the DSL achieved the best area per channel at the cost of a higher PEF value compared to OL architectures. The choice in architecture therefore depends on a trade-off between power usage and chip area requirement.

In an effort to reduce the power usage and area requirement per channel, various forms of resource sharing amplifier architectures have been proposed in literature, such as the amplifier stacking and partial OTA sharing presented in Chapter 1. Additionally, resource sharing can be further utilized by exploiting the high signal correlation characteristic of neural signals recorded in close proximity. For example, the authors of [65] exploited the high signal correlation of neural signals recorded in close proximity in order to reduce the power consumption of their data transmission system.

The amplifier proposed in this chapter is based on the previously mentioned resource sharing techniques. The proposed amplifier consists of separate recording channels and a shared

reference block which is utilized by all recording channels. Depicted in figure 2-1 is the high level block diagram of the proposed macro pixel amplifier system. The macro pixel accepts N_{ch} input signals and a single reference input. As the macro pixel accepts N amount of input signals, the maximum area of the macro pixel is then calculated to be $50\sqrt{N_{ch}}\mu m \times 50\sqrt{N_{ch}}\mu m$.

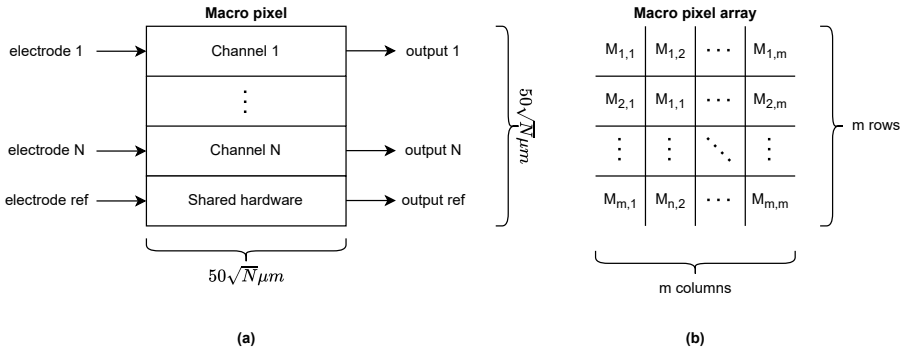


Figure 2-1: High level overview of the (a) proposed macro pixel and (b) macro pixel array.

2-2 Neural signal correlation

Low frequency signals recorded in the extracellular fluids are generated by the combined activity of neurons in close proximity to the recorded neuron [66], these signals are called local field potentials (LFP). When the recording electrodes are positioned in close proximity, the LFP signals recorded by each electrode are highly correlated [65].

In order to quantify the signal correlation as a function of recording electrode distance, the data set provided by [67] is used. This data set contains the raw neural signal recordings obtained from the neocortex of twenty different rats. The recordings were made over a total time period of 30 minutes at a sampling frequency of $f_s = 20kHz$. The recordings were performed using a 4×32 shank electrode array with a recording electrode pitch of 22.5μm.

Let S_1 and S_2 be neural signals recorded simultaneously over a time interval $T_{rec} = N_s T_s$ by different recording electrodes separated by distance d_{rec}. Defining $s_{1,2,i}$ to be samples from $S_{1,2}$ with $1 \leq i \leq N_s$, the standard deviation $\sigma_{S_{1,2}}$ and covariance $\rho_{S_{1,2}}$ of the recorded signals is then calculated by equations 2-1 and 2-2 respectively. The average normalised cross-correlation μ_ρ and standard deviation σ_ρ for N_{rec} recordings are then calculated by equations 2-3 and 2-4 respectively.

$$\sigma_{S_{1,2}} = \sqrt{\frac{1}{N_s}\sum_{i=1}^{N_s}\left(s_{1,2,i} - \overline{S_{1,2}}\right)^2}\ , \text{ with: } \overline{S_{1,2}} = \frac{1}{N_s}\sum_{i=1}^{N_s} s_{1,2,i} \tag{2-1}$$

$$\rho_{S_{1,2}} = \frac{cov(S_1, S_2)}{\sigma_{S_1}\sigma_{S_2}}\ , \text{ with: } cov(S_1, S_2) = \frac{1}{N_s - 1}\sum_{i=1}^{N_s}(s_{1,i} - \overline{S_1})(s_{2,i} - \overline{S_2}) \tag{2-2}$$

$$\mu_\rho = \frac{1}{N_{rec}}\sum_{n=1}^{N_{rec}} \rho_n \tag{2-3}$$

$$\sigma_\rho = \frac{1}{N_{rec}} \sum_{n=1}^{N_{rec}} \sigma_n \tag{2-4}$$

Given in figure 2-2 are the calculated average normalised cross-correlation coefficient and standard deviation as a function of the distance between the two separate recording electrodes. The results obtained in figure 2-2 show that frequencies lower than 100Hz are highly correlated for low electrode distances while frequencies higher than 5kHz are significantly less correlated. The high correlation of LFP can be explained by the fact that for two neighbouring electrodes, the neurons in close proximity causing the LFP signals at one electrode are largely identical to the neuron causing LFP signals at the neighbouring electrode. Both electrodes will thus sense an LFP signal that is approximately similar. The higher frequency signals consist mostly of device noise sources which are uncorrelated.

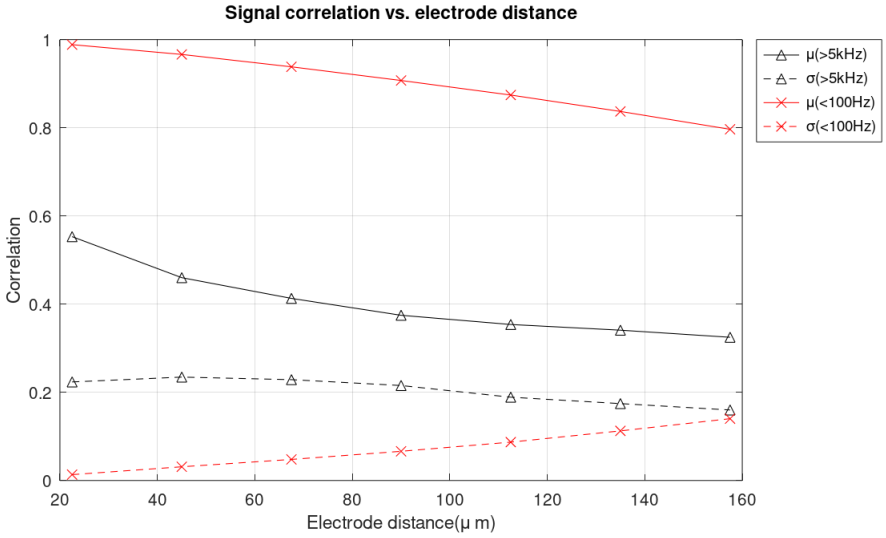


Figure 2-2: Correlation of neural signals as a function of electrode distance with signal recording time $T_{rec} = 10$s and $N_{rec} = 96$.

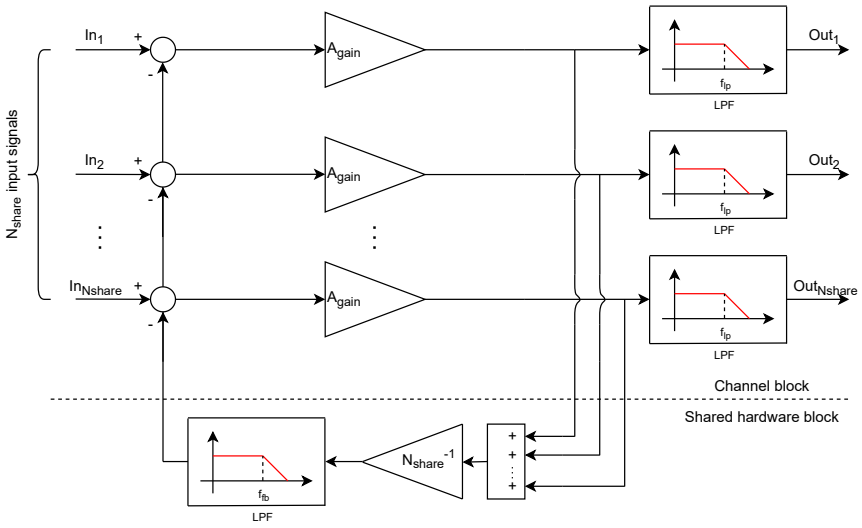
In addition to LFP signals, a DC-offset voltage is also present at the input of the amplifier. This DC-offset voltage is caused by electrochemical reactions at the interface between the tissue and the recording electrode. The resulting DC-offset voltages range from $+/-50mV$. Due to the localised nature of the electrochemical reactions, the resulting DC-offset voltages differ per recording electrode [68] and are thus uncorrelated.

2-2-1 Exploiting high signal correlation using shared feedback

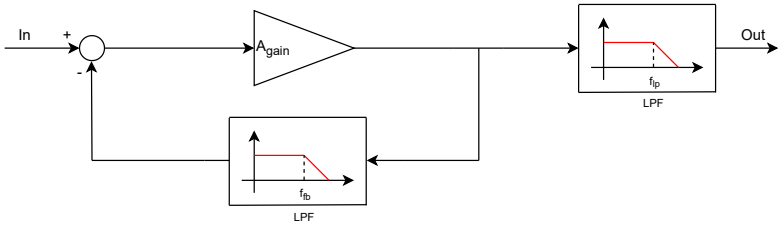
The high signal correlation for frequencies below 100Hz presented in figure 2-2 implies that these signals can be approximated to be equal. For N_{elec} amount of recording electrodes located in close proximity, let $s_{\leq 100Hz}$ be a $\leq$ 100Hz signal component of a recorded raw neural signal. For these signals equation 2-5 then holds true.

$$\frac{1}{N_{share}} \sum_{i=1}^{N_{share}} s_{i,\leq 100Hz} \approx s_{i,\leq 100Hz} \tag{2-5}$$

The approximation given in equation 2-5 can be exploited to create an amplifier system with a shared high pass filtering system. Presented in figure 2-3(a) is the high level system diagram of an amplifier with a shared feedback path. The system accepts N_{share} input signals which are amplified by a gain factor equal to A_{gain}. The shared feedback block calculates the average of all N_{share} signals after amplification and filters out frequencies below 100Hz using negative feedback. The low pass filter at the output filters out frequencies above 5kHz.



(a)



(b)

Figure 2-3: High level system diagram of the (a) shared feedback amplifier and (b) baseline amplifier.

The system of figure 2-3 is implemented using MATLAB Simulink with $A_{gain} = 100$, $f_{lp} = 5$kHz. Frequency f_{hp} is chosen such that frequencies below 100Hz are filtered out. The amplifier given in figure 2-3(b) serves as a baseline to which the shared feedback system is compared. The performance of the proposed shared feedback implementation is evaluated using MATLAB Simulink. Given in figure 2-4 are the obtained results of a single recording over a time interval of $T_{rec} = 60$ s with $N_{share} = 4$.

The signals obtained from the shared feedback amplifier in figure 2-4 are relatively highly correlated to the baseline signal. However, spike train signals are known to have high temporal sparsity [65] with the signal between two separate spike events carrying no relevant data for EAP recording. A high signal correlation with the baseline after amplification and filtering

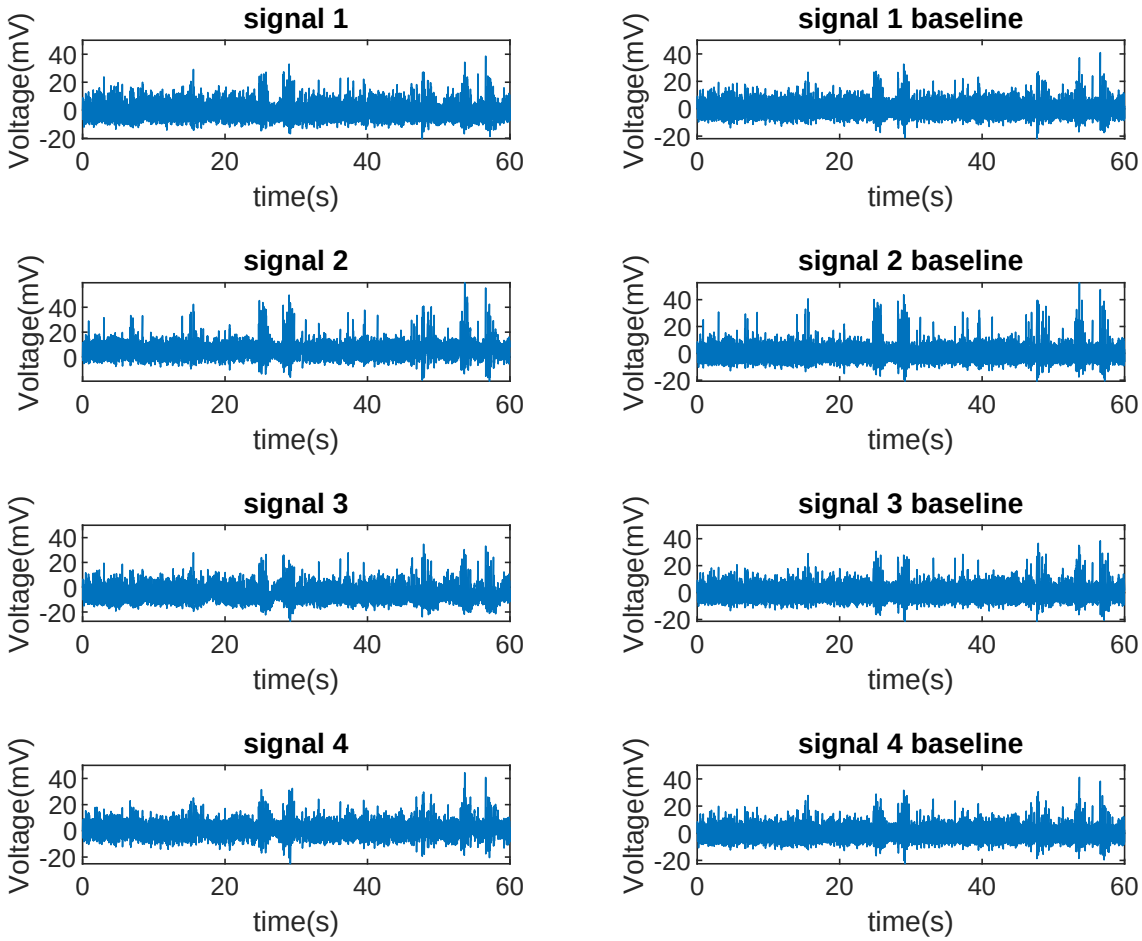


Figure 2-4: Example of obtained output signal recordings using the shared feedback (left column) and baseline amplifier (right column). The calculated correlation values of each signal to its corresponding baseline signal are 0.9064, 0.8826, 0.8456 and 0.8760 for signals 1, 2 ,3 and 4 respectively.

therefore does not necessarily imply that both system have comparable performance. Instead, we need to look at the correlation only during spiking activity.

To more accurately quantify and compare the performance of both systems, spike sorting is performed on the output signals of the shared feedback and baseline amplifier. The spike sorting algorithm wave_clus [69] is used to determine the amount of spike events within a given recording. The amount of spikes detected by the output signal obtained from the amplifier given in figure 2-3(b) serves as the baseline to which the shared feedback system is compared.

Presented in figure 2-5 are the obtained spikes using wave_clus of the signals presented in 2-4. The wave_clus algorithm detects spikes and sorts the detected spike waveforms into clusters based on the amplitude of the detected spike. Clusters 2 and 3 contain the spikes with the largest amplitude values and also shows the same amount of spikes for both the marco-pixel and baseline amplifier systems in the case of cluster 2. The spikes of these clusters are within close proximity ($\leq 50\mu m$) to the recording electrodes [69]. Clusters 1 contains spikes that can

not be allocated to any single neuron and are typically within a range of $50\mu m$ to $150\mu m$ [69]. Cluster 0 contains spikes that were not able to be allocated to any cluster. In terms of total detected spikes, the the macro-pixel and baseline amplifier detect 846 and 851 spikes respectively.

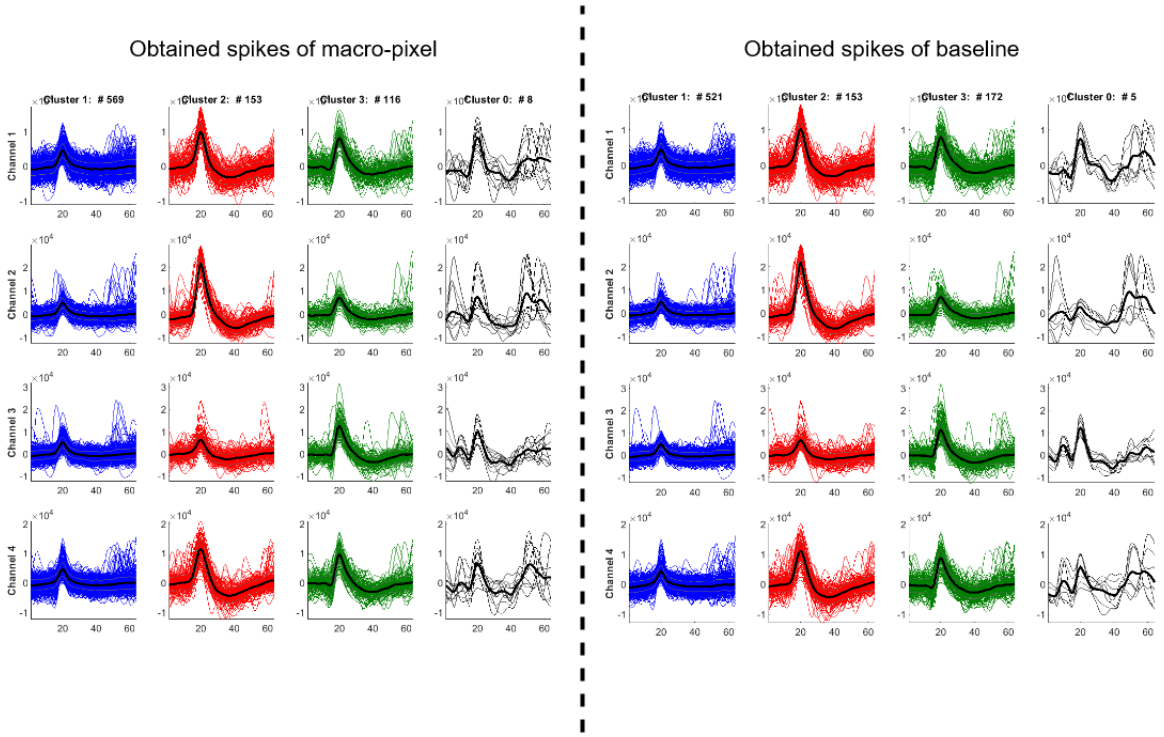


Figure 2-5: Obtained spikes using wave_clus of the macro-pixel (left side of dotted line) and baseline (right side of dotted line) amplifier for $T_{rec} = 60$ s.

To compare the spike detecting capabilities of both amplifier implementations, let $\lambda_{N_{share}}$ and λ be the total number of spikes obtained after spike sorting of the N_{share}-times shared feedback amplifier and baseline recording amplifier, respectively. For $N_{cluster}$ amount of recordings, the normalised root-mean-squared error $\epsilon(N_{share})$ for an N_{share}-times shared amplifier is then calculated by equation 2-6.

$$\epsilon(N_{share}) = \sqrt{\frac{1}{N_{cluster}} \sum_{i=1}^{N_{cluster}} \left(\frac{\lambda_{N_{share},i} - \lambda_i}{\lambda_i} \right)^2} \tag{2-6}$$

For $N_{share} = 4$, the obtained $\epsilon(4) = 0.025$, this value shows that the shared feedback implementation achieves relatively comparable spike sorting results as the standard amplifier implementation. The high correlation of low frequency LFP signals can thus be exploited by utilizing a share negative feedback path to implement the high pass filter of the amplifier system.

Influence of gain variations on detected spikes

The comparative analysis between the shared feedback system and the baseline system assumed a uniform gain of $100V/V$ for each recording channel. In circuit level implementations, especially when using open-loop amplifier architectures, the gain is subject to process variations.

In order to determine the robustness of the shared feedback amplifier to process variations, the spike detection simulations are repeated using randomly generated gain values A_Δ from a normal distribution with mean $\mu = 100V/V$ and standard deviation $\sigma = 3V/V$.

Let $\lambda_{A_{baseline}}$ be the total amount of spikes obtained by the baseline shared feedback amplifier with gain $A_{baseline} = 100V/V$ and λ_{A_Δ} be the total amount of spikes obtained by the shared feedback amplifier with gain A_Δ. The resulting normalised root-mean-squared error as a results of gain variations is then calculated using equation 2-7, resulting in $\epsilon_\Delta = 5.14 \cdot 10^{-3}$. This low normalised error value implies that the total amount of obtained spikes after spike sorting is highly invariant to gain variations.

$$\epsilon_\Delta = \sqrt{\frac{1}{N_{cluster}} \sum_{i=1}^{N_{cluster}} \left(\frac{\lambda_{A_\Delta,i} - \lambda_{A_{baseline}}}{\lambda_{A_{baseline}}} \right)^2} \tag{2-7}$$

2-3 Proposed amplifier design

Based on the conclusions made in Chapter 1 and Section 2-2, the complete proposed system level design implementation of the single-cell resolution neural amplifier is given in figure 2-6. The proposed amplifier system consists of two open-loop gain stages, a combined DC servo loop, a DC-offset filter and a low-pass filter.

2-3-1 Gain stages

The gain requirement is achieved by using two gain stages A_1 and A_2. Amplification is done in two stages, so that the DC servo loop can be fed back after A_1 to reduce its noise contribution to the total input-referred noise of the amplifier.

Gain values A_1 and A_2 are chosen such that the total gain of the amplifier system $A_{tot} = A_1 + A_2 \geq 40$dB. A_1 is chosen to be larger than A_2 in order to reduce the noise contribution of the second gain stage, the shared DC servo loop and the low-pass-filter.

The amplifier uses a 4-times partially shared OTA structure based on [26] to reduce area and power consumption. Resource sharing is limited to $N_{share} = 4$ due to the relatively low improvement in NEF values for $N_{share} > 4$ as depicted in figure 1-27 and due to the reduction in signal correlation for increasing electrode distances as depicted in figure 2-2.

2-3-2 Shared DC servo loop

The high pass frequency pole $f_{hp} = 100Hz$ of the amplifier is implemented using a DC servo loop (DSL) which is shared by all 4 recording channels. The input signals from the 4 recording

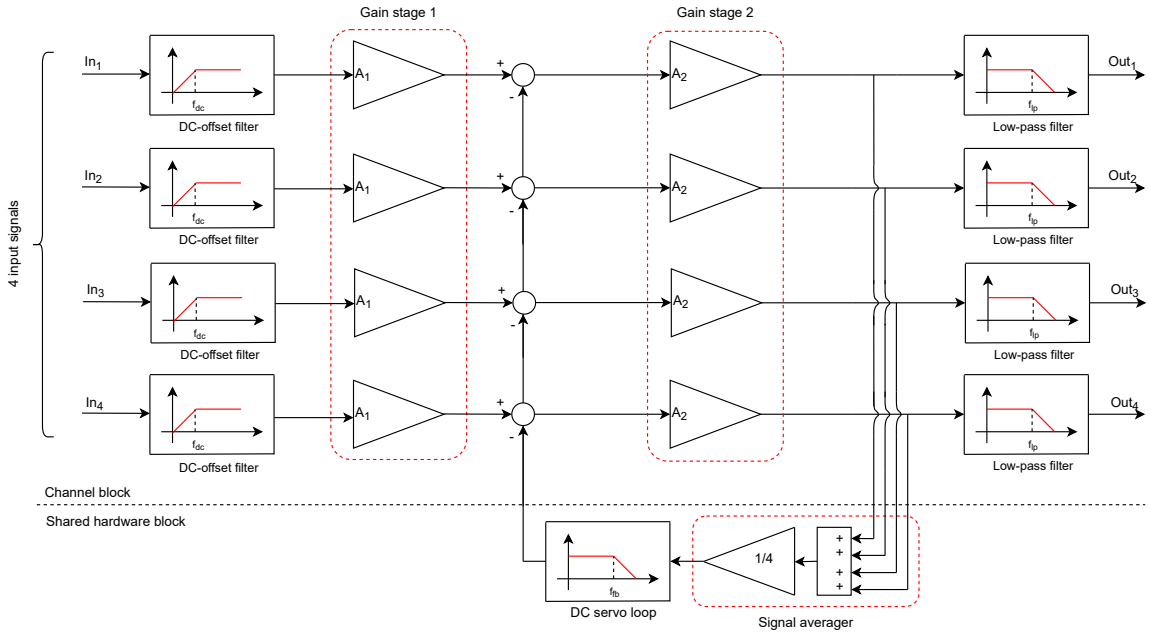


Figure 2-6: Proposed neural amplifier architecture for single-cell resolution amplification.

channels are averaged using a signal averager. The feedback is applied over the second gain stage in order to reduce the contribution of the DC servo loop on the total input referred noise of the amplifier.

2-3-3 DC-offset filter

The DC-offset filter is included to remove any DC-offset voltage that may be present at the input terminals of the amplifier system and prevent the first gain stage from saturating. The DC-offset filter is necessary due to the offset voltage introduced by the recording electrode. This offset is present on each channel and it is not correlated among channels as discussed in section 2-2. Hence, it cannot be filtered by the shared DC servo loop.

2-3-4 Low-pass filter

The low-pass filter is implemented such that the specified low pass frequency $f_{lp} = 5kHz$ is achieved. Signals beyond $5kHz$ are filtered out since these signals do not contain any EAP signals. Low-pass filtering is also applied to limit the noise bandwidth of the amplifier.

2-3-5 Specifications

Based on the findings in Chapter 1 and the chosen value of $N_{share} = 4$. The complete list of specifications for the proposed macro pixel presented in figure 2-6 is given in Table 2-1.

Table 2-1: Proposed macro pixel for single-cell resolution BMI amplifier specifications.

Parameter	**Value**
Technology	40nm CMOS
Supply voltage	1.1V
Area/macropixel	$<100\mu m \times 100\mu m$
Gain	$\geq$40dB
Power	$\leq$1mW/mm^2
Input referred noise	$\leq$10 μV_{rms}
High-pass frequency	100Hz
Low-pass frequency	5kHz

Circuit level design implementation

In this chapter the circuit level design implementation of the proposed amplifier system of chapter 2 is presented and discussed. Section 3-1 presents the circuit level implementation of the proposed amplifier and justification of each system block given in the figure 2-6. Section 3-3 presents the design procedure used to generate the circuit component values.

3-1 Amplifier circuit level design

In this section the circuit level implementation of all amplifier blocks of the proposed amplifier system given in figure 2-6 are presented and discussed. The circuit diagram of the entire proposed amplifier system is given in figure 3-1. The circuit level implementations and justifications of the DC-offset filter, gain stages, DC servo loop and low-pass filter are presented and discussed in subsections 3-1-1, 3-1-2, 3-1-3, 3-1-4 respectively. The noise analysis of the system is given in subsection 3-1-5

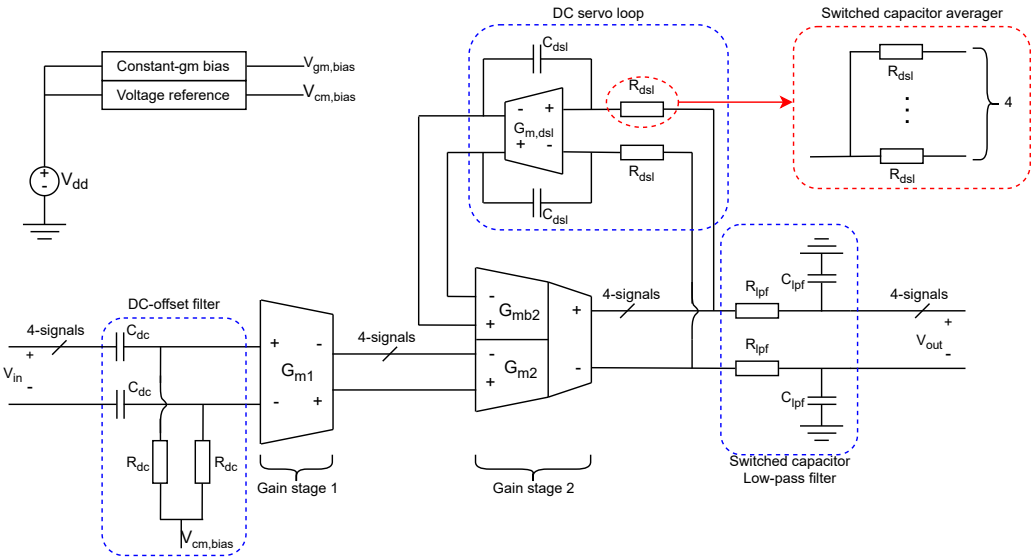


Figure 3-1: Proposed neural amplifier architecture for single-cell resolution amplification.

3-1-1 DC-offset filter

The DC-offset filter is implemented using a first-order high-pass filter depicted in figure 3-2a consisting of a capacitor C_{dc} and pseudoresistor R_{dc}. Given in figure 3-2b is the implementation of the pseudoresistor structure with the parasitic body diodes D_p highlighted [70]. The equivalent resistance value of a single PMOS device in the pseudoresistor is given by equation 3-1 with n the sub-threshold slope, μ_p the mobility of the charge carriers, $C_{ox,p}$ the gate oxide capacitance per area, L_{pr} and W_{pr} the gate length and width of $M_{pr,dc}$ respectively, V_T the thermal voltage and $V_{th,p}$ the threshold voltage of the PMOS device $M_{pr,dc}$ [70]. The cut-off frequency of a first-order high pass RC filter $f_{hpf,dc}$ using this pseudoresistor structure is then given by equation 3-2.

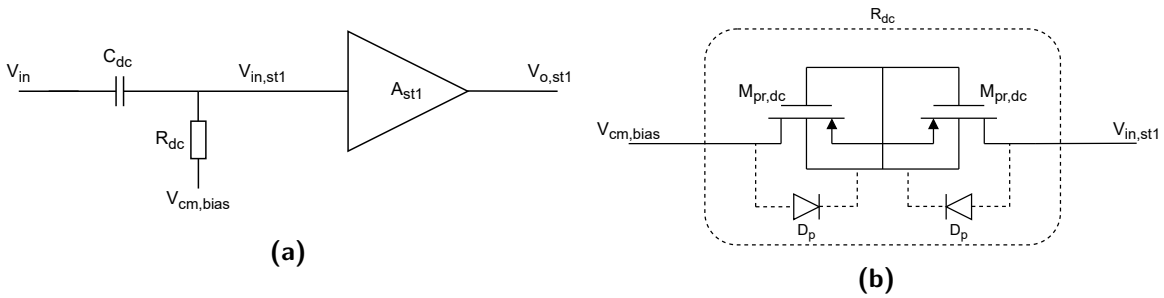


Figure 3-2: Implementation of (a) DC-offset filter and (b) transistor level implementation of pseudo resistor R_{dc}.

$$r_{eq} = \frac{1}{4n\mu_p C_{ox,p} V_T} \left(\frac{L_{pr}}{W_{pr}}\right) exp\left(\frac{|V_{th,p}|}{nV_T}\right) \tag{3-1}$$

$$f_{hpf,dc} = \frac{1}{2\pi R_{dc} C_{dc}} \text{ , with } R_{dc} = 2r_{eq} \tag{3-2}$$

The pseudoresistor structure given in figure 3-2b suffers from resistance non-linearity as the voltage across it changes. However, the expected maximum input swing of extracellular action potentials equals +/-0.5mV, resulting in a maximum voltage swing of +/-0.5mV over the pseudoresistor. This results in a negligible non-linearity and the resistance value can be assumed to be constant.

Parameter $|V_{th,p}|$ is known to be heavily dependant on process variations resulting in r_{eq} being very dependant on process variations as well. This in turn results in high pass frequency $f_{hpf,dc}$ varying significantly as a result of process variations. Worst case variations of the pseudoresistor value range from -50% to $+100\%$. Therefore $f_{hpf,dc}$ must be implemented such that $f_{hpf,dc} < 100$Hz for all process corners in order to not interfere with the high pass frequency implemented by the shared feedback system.

3-1-2 Gain stages

For both gain stages of the amplifier system, inverter based OTA are chosen due to the higher power efficiency as concluded in Chapter 1. Given in figures 3-3a and 3-3b are the transistor

level implementation of the OTA used in gain stages 1 and 2 respectively. Partial OTA sharing architectures are used for both OTA in order to increase the power and area efficiency. The gain A_1 of the first and A_2 of the second stage are given by equations 3-3 and 3-4 respectively. The resulting total gain A_{tot} of the amplifier system is then calculated by equation 3-5.

$$A_1 = -(g_{mn,1} + g_{mp,1})(r_{on,1}||r_{op,1}) \tag{3-3}$$

$$A_2 = -(g_{mn,2} + g_{mp,2})(r_{on,2}||r_{op,2}) \tag{3-4}$$

$$A_{tot} = A_1 A_2 = (g_{mn,1} + g_{mp,1})(g_{mn,2} + g_{mp,2})(r_{on,1}||r_{op,1})(r_{on,2}||r_{op,2}) \tag{3-5}$$

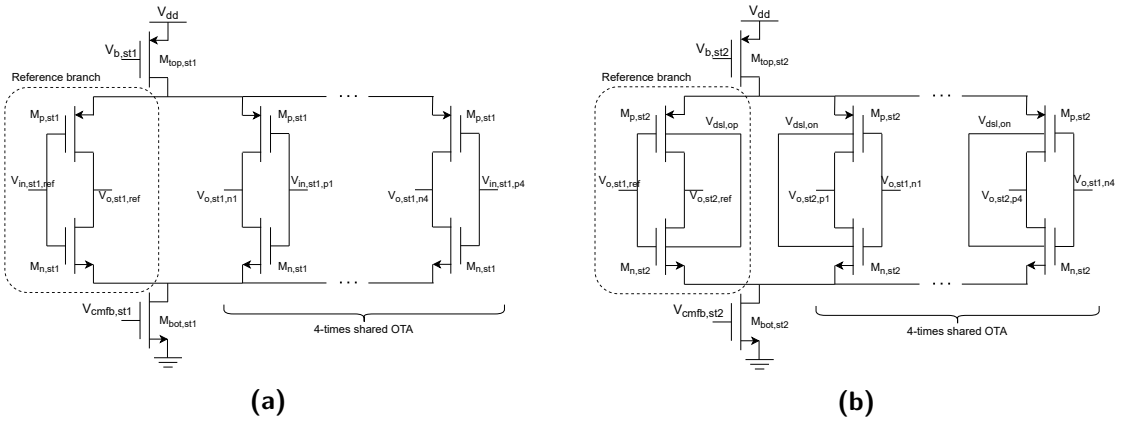


Figure 3-3: Transistor level OTA implementation of (a) gain stage 1 and (b) gain stage 2.

The body terminals of the input PMOS and NMOS devices of the second gain stage OTA are used to implement the negative feedback of the combined DC-servo loop. The common-mode body voltage of the input devices is chosen to be $V_{cm,body,st2} = \frac{1}{2}V_{dd}$. In order to control the body voltage of both PMOS and NMOS devices in a p-type substrate, the NMOS devices are places in a deep n-well structure. The body controlled feedback factor η is given by equation 3-6 with G_{m2} and G_{mb2} the large-signal transconductance and body transconductance respectively.

$$\eta = \frac{G_{mb2}}{G_{m2}} \tag{3-6}$$

Due to the differential architecture of the OTA, a common-mode feedback (CMFB) circuit is required to set the common-mode output voltage level $V_{cm,o}$ of the OTA to $V_{cm,o} = \frac{1}{2}V_{dd}$. Given in figure 3-4 is the circuit diagram of the CMFB circuit used to set the common mode output voltage of the first and second gain stage. Two PMOS devices $M_{pr,cmfb}$ are used to implement pseudo resistors with large resistance values. All output nodes of the gain stages are connected with a pseudo resistor to the positive input node of OTA G_{cmfb}. The negative input node of G_{cmfb} is connected to the common mode voltage bias $V_{cm,bias} = \frac{1}{2}V_{dd}$, resulting in the voltage level of the positive input node to also equal $\frac{1}{2}V_{dd}$. The transistor level implementation of G_{cmfb} is given in figure 3-5.

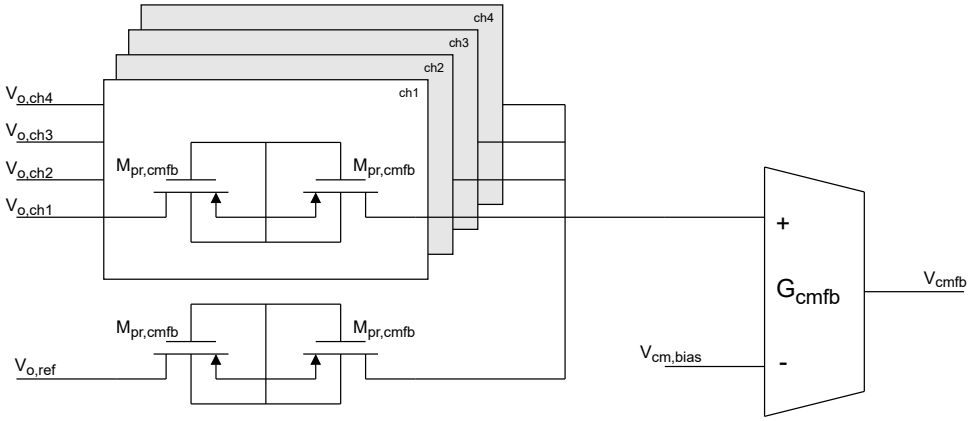


Figure 3-4: Circuit diagram of the CMFB circuit used in gain stages 1 and 2.

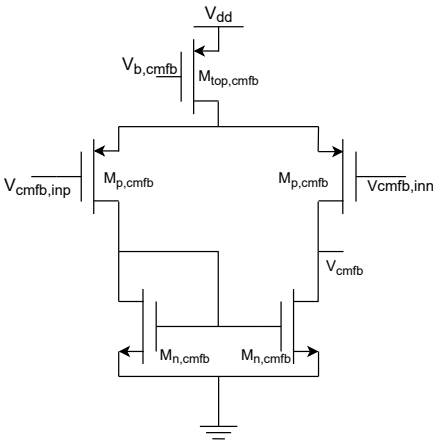


Figure 3-5: Circuit diagram of OTA G_{cmfb} used in the CMFB circuit.

3-1-3 Switched capacitor shared DC servo loop

The shared DSL implements the high pass frequency pole used to filter out signals below 100Hz. Given in figure 3-6 is the circuit diagram of the parasitic insensitive switched capacitor (SC) analog integrator [71] used to implement the shared DC servo loop. The SC resistor can be be calculated by equation 3-7 for clock frequency f_{clock}. The available clock frequency in this application is given to be $f_{clock} = 20kHz$. The high pass frequency f_{hp} implemented by the DC servo loop is then given by equation 3-8, where A_{dsl} is the gain of OTA $G_{m,dsl}$.

$$R_{dsl} = \frac{1}{f_{clock} C_{sw,dsl}} \tag{3-7}$$

$$f_{hp} = f_{dsl,0}(1 + A_2 A_{dsl}\eta) \text{ , with } f_{dsl,0} = \left(\frac{2\pi}{f_{clock}} \cdot \frac{C_{dsl}}{C_{sw,dsl}} \cdot |A_{dsl}| \right)^{-1} \tag{3-8}$$

The circuit diagram of the DSL OTA $G_{m,dsl}$ is given in figure 3-7a with gain A_{dsl} calculated by equation 3-9. Due to the differential nature of the DSL OTA, the CMFB circuit depicted in figure 3-7b is used to set the output common-mode voltage to $V_{o,dsl,cm} = \frac{1}{2}V_{dd}$.

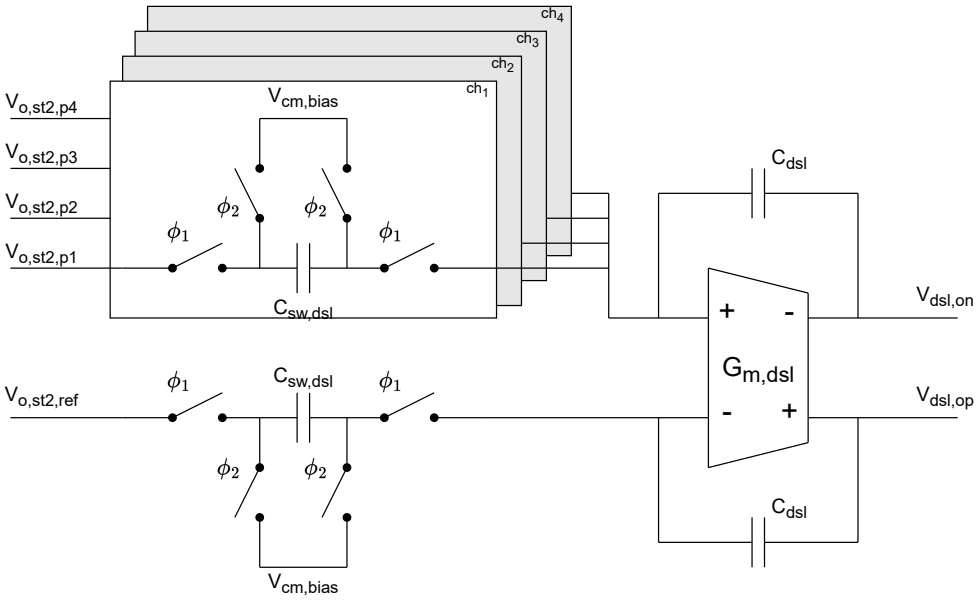


Figure 3-6: Circuit diagram of the 4-times shared, parasitic insensitive switched capacitor analog integrator.

$$A_{dsl} = -g_{m,p,dsl}(r_{o,p,dsl}||r_{o,n,dsl}) \tag{3-9}$$

The switches are implemented using low threshold voltage NMOS devices M_{sw} depicted in figure 3-8a. low threshold voltage NMOS devices are used in order to facilitate a large input voltage swing. Two non-overlapping clock signals ϕ_1 and ϕ_2 with clock frequency $f_{clock} = 20$kHz are used to drive the switch gates as illustrated in figure 3-8b.

3-1-4 Switched capacitor low pass filter

Given in figure 3-9a is the SC low pass filter used to implement the low pass frequency pole at 5000 Hz. Stacked capacitors, as depicted in figure 3-9b, are used to implement the capacitors of the LPF. Stacked capacitors consist of an NMOS capacitor C_{NMOS} placed underneath a metal-oxide-metal (MOM) capacitor C_{MOM} and provide the highest possible capacitance per area of $9fF/\mu m^2$ in the used technology. The LPF uses the same non-overlapping clock signals and switches used to implement the switched capacitors of the shared DSL.

For switched capacitors, the continuous-time approximation of the switched capacitor resistance value calculated by equation 3-7 only holds true when the implemented low pass frequency $f_{-3dB} << f_{clock}$ [72]. If this criterion does not hold, a discrete-time analysis of the circuit is required. The charge stored in capacitors $C_{sw,lpf}$ and C_{lpf} during clock cycle ϕ_1 are calculated by equations 3-10 and 3-11 respectively. The charge at the output node V_{out} stored in capacitors $C_{sw,lpf}$ and C_{lpf} during clock cycle ϕ_2 is calculated by equation 3-12. By equalizing the sum of equations 3-10 and 3-11 to equation 3-12, the transfer function of the switched capacitor low pass filter in the digital domain is then calculated and given by equation 3-13.

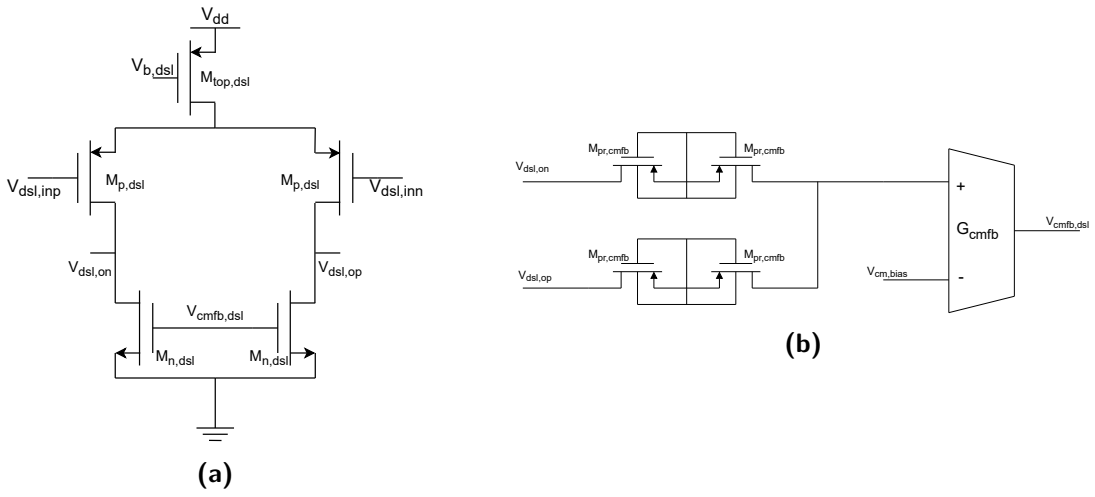


Figure 3-7: Transistor level implementation of (a) DSL OTA and (b) DSL CMFB.

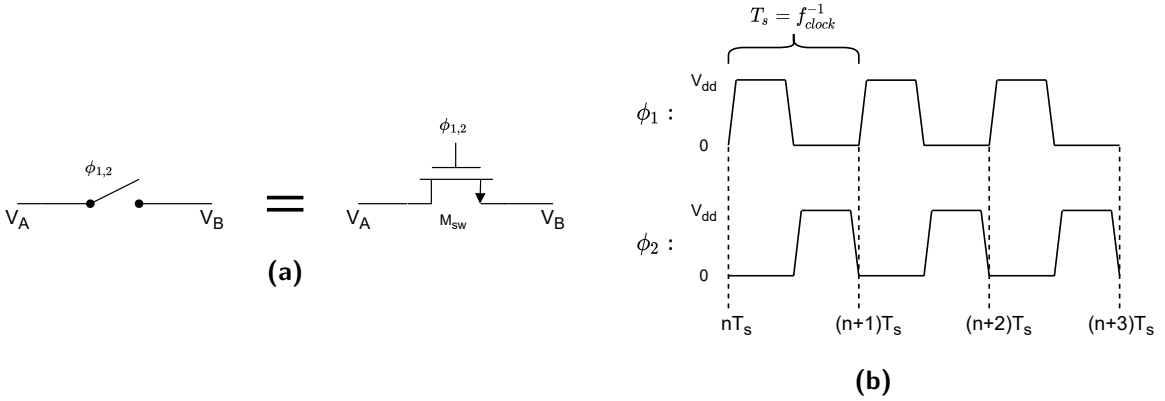


Figure 3-8: Transistor level implementation of (a) DSL OTA and (b) DSL CMFB.

$$Q^{\phi_1}_{Csw,lpf} = C_{sw,lpf} V_{o,st2}[nT_s] \tag{3-10}$$

$$Q^{\phi_1}_{Clpf} = C_{lpf} V_{out}[nT_s] \tag{3-11}$$

$$Q^{\phi_2}_{out} = (C_{sw,lpf} + C_{lpf}) V_{out}[(n+1)T_s] \tag{3-12}$$

$$H_{lpf}(z) = \frac{z^{-1}}{1 + \frac{C_{lpf}}{C_{sw,lpf}} - \frac{C_{lpf}}{C_{sw,lpf}} z^{-1}} \text{ , with } z = exp\left(2\pi i \frac{f}{f_{clock}}\right) \tag{3-13}$$

3-1-5 Noise analysis

The noise equations for all circuit implementations are calculated as follows. Let $k = 1.38064852 \cdot 10^{-23} \text{JK}^{-1}$ be the Boltzmann constant and $T = 310\text{K}$ be the temperature under which the designed system is to perform. Defining $K_{p,n}$ and $C_{ox,n,p}$ to be the process-dependant $1/f$-noise constant and gate oxide capacitance per area respectively. The input

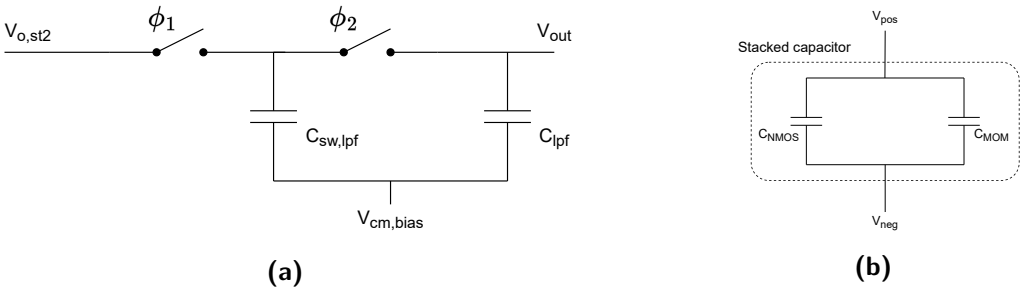


Figure 3-9: Circuit diagram of (a) the switched capacitor low pass filter and (b) the stacked capacitor structure used to implement $C_{sw,lpf}$ and C_{lpf}.

referred noise voltage of the inverter based OTA used in both gain stages is then given by equation 3-14 over an equivalent noise bandwidth B_{enb}. The output noise voltage of the shared DSL OTA is then given by equation 3-15. The noise contribution of the switched capacitors used in the shared DSL and LPF are then calculated by equations 3-16 and 3-17 respectively. The total input referred noise of the amplifier is then given by equation 3-18. Equation 3-18 is further simplified to equation 3-19 when $\frac{\eta^2}{A_1^2} << 1$ and $\frac{1}{A_1^2 A_2^2} << 1$.

$$\overline{V_{in,n,OTA}^2} = \frac{16kT\gamma}{g_{mn}+g_{mp}} \cdot B_{enb} + \left(\frac{2K_n}{C_{ox,n}W_nL_n} + \frac{2K_p}{C_{ox,p}W_pL_p}\right)\int_{f_{low}}^{f_{high}} \frac{1}{f} df \tag{3-14}$$

$$\overline{V_{n,out,dsl}^2} = 8kT\gamma B_{enb} g_{mp} r_{op} + \frac{2K_p g_{mp}^2 r_{op}^2}{C_{ox,p}W_pL_p}\int_{f_{low}}^{f_{high}} \frac{1}{f} df \tag{3-15}$$

$$\overline{V_{n,Rdsl}^2} = \frac{kT}{C_{dsl}} \tag{3-16}$$

$$\overline{V_{n,Rlpf}^2} = \frac{kT}{C_{lpf}} \tag{3-17}$$

$$\overline{V_{n,in,tot}^2} = \overline{V_{n,in,A1}^2} + \frac{1}{A_1^2}\left(\overline{V_{n,in,A2}^2} + \eta^2\overline{V_{n,out,dsl}^2}\right) + \frac{1}{A_1^2A_2^2}\left((N+1)\,\overline{V_{n,Rdsl}^2} + 2\overline{V_{n,Rlpf}^2}\right) \tag{3-18}$$

$$\overline{V_{in,n,tot}^2} \approx \overline{V_{in,n,OTA1}^2} + \frac{1}{A_1^2}\overline{V_{in,n,OTA2}^2} \tag{3-19}$$

3-2 Biasing circuit level design

In this section the constant-g_m and voltage bias circuits used to provide the biasing to the amplifier are presented and discussed.

3-2-1 Constant-g$_m$ biasing

Presented in figure 3-10a is the constant-g_m biasing circuit used to bias both gain stages and the DSL OTA of the amplifier system. Constant-g_m biasing is chosen in order to obtain accurate high pass filtering by the DSL due to the dependency of the high pass frequency pole on the gain of the second gain stage and DSL OTA, as can be concluded from equation 3-8. The given biasing circuit provides the biasing voltage for all OTA of the amplifier, thus $V_{b,st1} = V_{b,st2} = V_{b,dsl} = V_{b,cmfb} = V_{gm,bias}$.

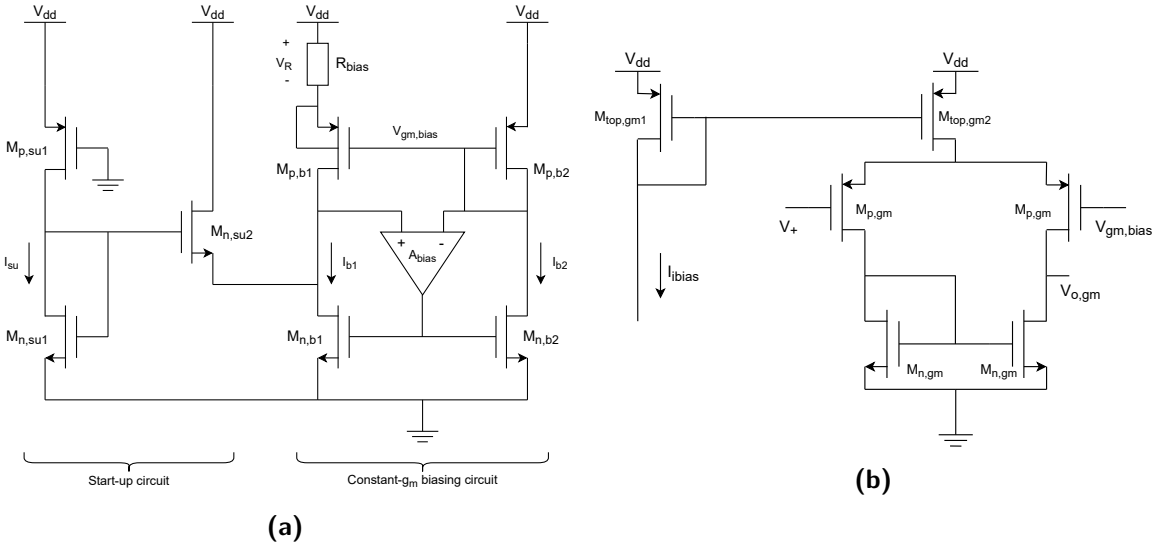


Figure 3-10: Circuit diagram of (a) the constant-g$_m$ biasing circuit and (b) OTA A_{bias}.

Let K be the multiplication factor of devices $M_{p,b1}$ and $M_{p,b2}$ such that the device aspect ratios $(W/L)_{bp,1} = K(W/L)_{bp,2}$. Equation 3-20 then yields the transconductance $g_{mp,2}$ of device M$_{bp,2}$.

$$g_{mp,2} = \frac{2\left(1 - \sqrt{\frac{1}{K}}\right)}{R_{bias}} \tag{3-20}$$

Due to the relatively low value of V_{dd}, channel length modulation caused by differences in the drain-source voltages $V_{ds,p,b1}$ and $V_{ds,p,b2}$ over $M_{p,b1}$ and $M_{p,b2}$ respectively result in differing drain currents for both devices. Significant differences in drain currents lead to incorrect behaviour of the circuit. Thus, amplifier A_{bias} is required to set the drain voltages of devices $M_{p,b1}$ and $M_{p,b2}$ to be equal such that the drain-source voltage $V_{ds,p,b1} \approx V_{ds,p,b2}$ and thereby significantly reducing the effects of channel length modulation. OTA A_{bias} is implemented using the OTA presented in figure 3-10b.

The constant-g_m biasing circuit presented in figure 3-10 is a non-linear circuit with two possible operating points. One operating point sets $I_{b1} = I_{b2} = 0$ A, and may occur when the complete system starts up and the supply voltage V_{dd} rises from 0V to its nominal value. A separate start-up circuit is therefore required to ensure that the biasing circuit operates in the desired operating point.

At startup, device $M_{p,su1}$ enters the saturation state when $V_{dd} > V_{th,p,su1}$, resulting in a non-zero current flowing through the drain of the device which also flows through the drain of $M_{n,su1}$. This drain current induces a voltage at the gate of $M_{n,su1}$ which is equal to the gate voltage of $M_{n,su2}$. The gate voltage of $M_{n,su2}$ causes a non-zero current to be injected into the drain of device $M_{n,b1}$ via $M_{n,su2}$. This mechanism avoids the circuit to remain in the undesired zero-current operating state.

3-2-2 Voltage reference

A voltage reference is required to produce a reference voltage $V_{cm,bias} = \frac{1}{2}V_{dd}$. Due to the constant temperature the body provides for implantable devices, a temperature insensitive voltage reference is not necessary. Since the reference voltage is a function of the supply voltage, the reference additionally does not require to be independent of the supply voltage. Therefore the voltage reference is designed to only be process invariant.

Given in figure 3-11 is the implementation of the voltage reference circuit. The circuit consists of a 2 identical resistors R_{div} forming a resistor voltage divider with $V_{ref} = \frac{1}{2}V_{dd}$.

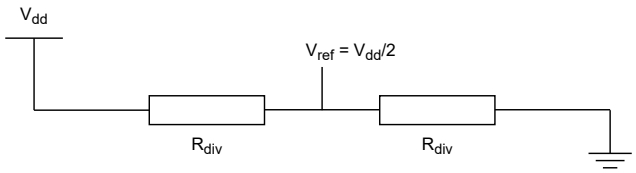


Figure 3-11: Circuit diagram of the voltage reference circuit.

3-3 Circuit design procedure

In this section the circuit design procedure used to generate the values of the circuit components is presented and discussed. The circuit design procedure is mainly based on the circuit design method presented in [73]. This method utilizes pre-computed lookup tables and uses the g_m/I_D value as the central design variable for the sizing of transistor devices.

3-3-1 Gain stage device parameters

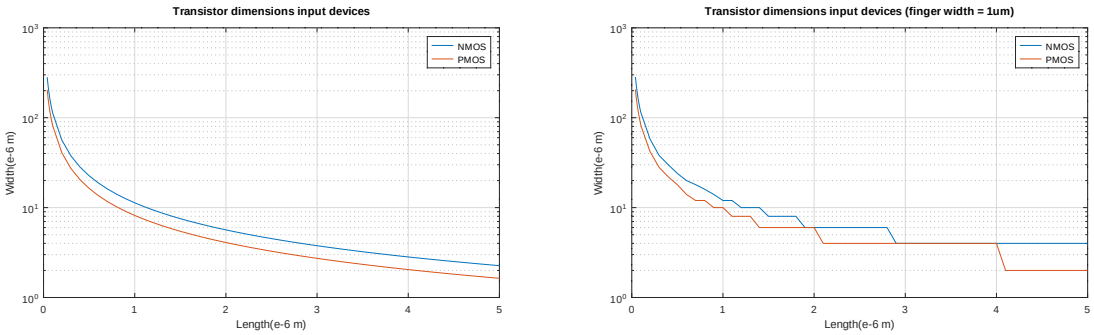
Gain stage 1

The total input referred noise of the inverter based OTA given by equation 3-14 consists of a thermal and $1/f$-noise component. The dimensions of the input devices are therefore mainly determined by the contribution of the $1/f$-noise component to the total noise of the OTA.

Rewriting the $1/f$-noise component equation, The minimum required widths of PMOS and NMOS input devices $W_{p,min}$ and $W_{n,min}$ are then given by equations 3-21 and 3-22 respectively. Choosing the $1/f$-noise component $\overline{V_{fn,max}^2} = \frac{1}{2}\overline{V_{in,n,OTA}^2}$ then yields figures 3-12a and 3-12b. In order to account for the noise folding and the influence of out of bound noise, $f_{low} = 10Hz$ and $f_{high} = 50kHz$ are chosen.

$$W_{p,min} = \frac{4K_p}{C_{ox,p}\overline{V_{fn,max}^2}L_p} \cdot ln\left(\frac{f_{high}}{f_{low}}\right) \tag{3-21}$$

$$W_{n,min} = \frac{4K_n}{C_{ox,n}\overline{V_{fn,max}^2}L_n} \cdot ln\left(\frac{f_{high}}{f_{low}}\right) \tag{3-22}$$



(a) **(b)**

Figure 3-12: Gain stage 1 input device dimensions (a) calculated minimum input device dimensions using equations 3-21 and 3-22 and (b) input device dimensions using $W_{finger} = 1\mu$m and rounding upwards to the nearest even integer.

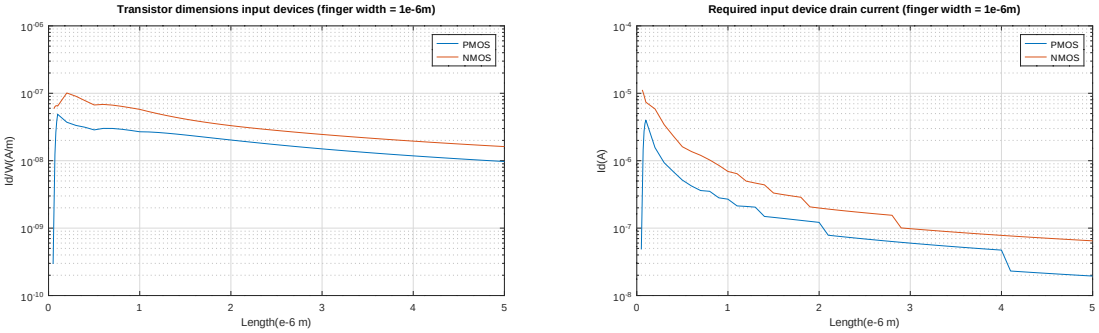
To determine the required drain currents of the transistors, both the g_m/I_D values and desired drain-source voltages of all transistor devices have to be chosen. For both the devices $M_{n,st1}$ and $M_{p,st1}$, $g_m/I_D = 25$ is chosen to maximise the noise efficiency of the OTA with drain saturation voltage $V_{dsat} \approx \frac{2}{g_m/I_D} = 80mV$. For $M_{top,st1}$ and $M_{bot,st1}$ the $g_m/I_D = 25$ as well resulting in $V_{dsat} \approx 80mV$. By allocating a drain-source voltage of $200mV$, both devices are given $120mV$ headroom to operate in saturation. The resulting drain-source voltages of $M_{n,st1}$ and $M_{p,st1}$ are then equal to $350mV$.

For the chosen g_m/I_D value and drain-source voltages, the drain current per device width I_D/W as a function of the device length L is then plotted in figure 3-13a. The input device drain current required to achieve the chosen g_m/I_D as a function of the device length is then given in figure 3-13b.

The intrinsic gain of the input devices for the chosen g_m/I_D is plotted in figure 3-14a. Using the intrinsic gain plot in conjunction with the device current plot given in figure 3-13b and equation 3-3, the gain of the first gain stage as a function of the gate length of $M_{n,st1}$ is then calculated and plotted in figure 3-14b.

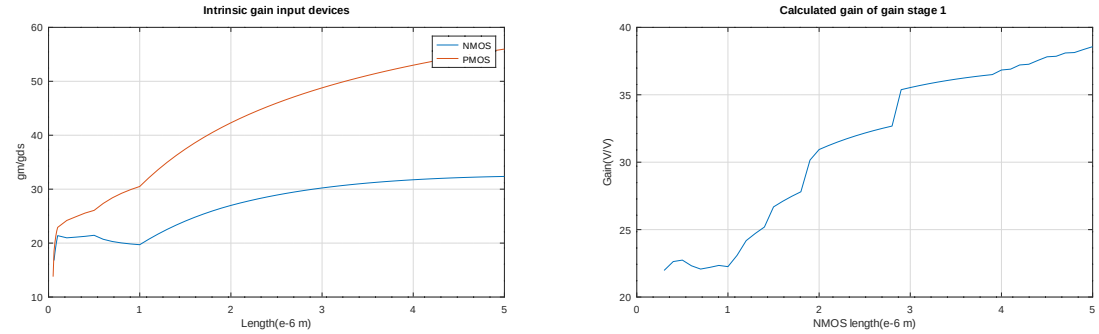
The total input referred noise of the first gain stage is calculated using equation 3-14 and plotted in figure 3-15 as a function of the NMOS input device length. By choosing the desired input referred noise voltage of the first gain stage, the noise plot is used to determine the corresponding NMOS device length. Given the NMOS device length value in conjunction with figures 3-12b and 3-13b the corresponding input device dimensions and required drain current I_d are determined respectively.

In order to provide noise variation headroom due to process variation and headroom for the noise produced by the second gain stage, the input-referred noise of the first gain stage is



(a) **(b)**

Figure 3-13: Gain stage 1 input device (a) Id/W for $g_m/I_D = 25$ and (b) I_D given $W_{finger} = 1\mu$m.



(a) **(b)**

Figure 3-14: Gain stage 1 (a) input device intrinsic gain for $g_m/I_D = 25$ and (b) total OTA gain as function of input NMOS device length.

chosen to be $V_{in,n,OTA1} = 8.0\mu V_{rms}$. Using figure 3-15 the required length of NMOS devices $M_{n,st1}$ is then determined to be $L_{n,st1} = 1.5\mu m$. Using figure 3-13b the required drain current is determined to be $I_D = 0.35\mu A$, which sets the length of the corresponding PMOS input device to be $L_{p,st1} = 0.9\mu m$. Using figure 3-12b the width of the NMOS and PMOS devices are determined to be $W_{n,st1} = 8\mu m$ and $W_{p,st1} = 10\mu m$. Since the finger width of the transistors equals $1\mu m$, the M-factors of the NMOS and PMOS devices are determined to be $M_{n,st1} = 8$ and $M_{p,st1} = 10$ respectively. The resulting gain of the first gain stage is then determined to be $A_1 = 27V/V$.

For the required drain current I_D, the total required gain stage current I_{tot} is calculated using equation 3-23 with $N = 4$. The drain current per device width I_D/W as a function of the device length L is then plotted in figure 3-16a. In order to prevent the devices from becoming excessively large, the g_m/I_D for $M_{top,st1}$ and $M_{bot,st1}$ are chosen to be 23 and 24 respectively. The I_D/W values and resulting dimensions of the current source devices for the chosen g_m/I_D value are then presented in figure 3-16a and 3-16b respectively.

$$I_{tot} = (N + 1)I_D \tag{3-23}$$

The chosen length of the current source devices $M_{top,st1}$ and $M_{bot,st1}$ equals $L_{bias} = 1\mu m$, this

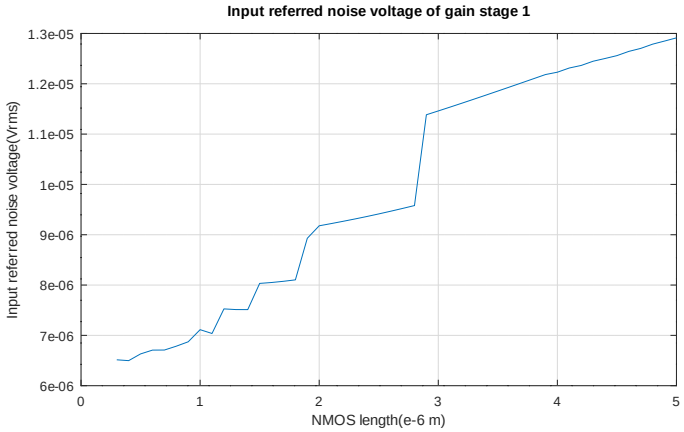
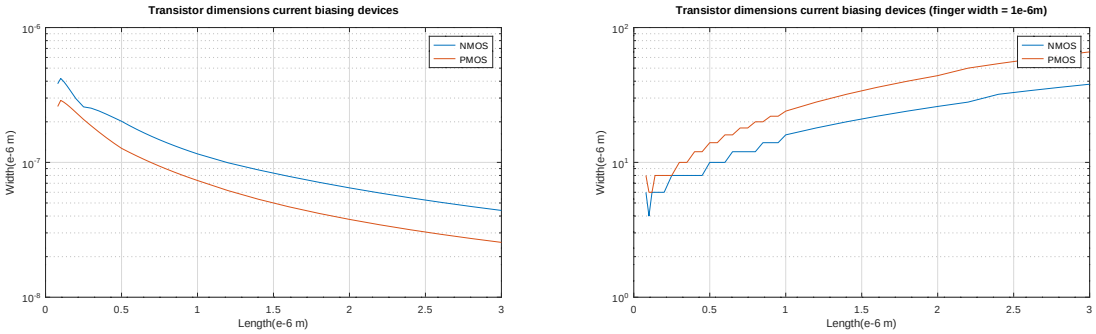


Figure 3-15: Calculated input-referred noise of gain stage 1 as a function of the input NMOS device length.



(a) **(b)**

Figure 3-16: Gain stage 1 current source (a) I_D/W (b) device dimensions.

length is chosen in order to reduce the effects of channel length modulation. Using the plot given in figure 3-16b, the required device width equals $W_{top,st1} = 24\mu m$ and $W_{bot,st1} = 16\mu m$ resulting in M-factors $M_{top,st1} = 24$ and $M_{bot,st1} = 16$.

The final device parameters of the first gain stage are summarised in Table 3-1. The final device parameters of the CMFB circuit for gain stage 1 are given in Table 3-2.

Table 3-1: Final device sizes and parameters of gain stage 1.

Device	**L**(μm)	**W**$_{finger}$(μm)	**M**	**gm/Id**	**Id**(μA)
$M_{top,st1}$	1	1	24	23	1.65
$M_{p,st1}$	0.9	1	10	25	0.33
$M_{n,st1}$	1.5	1	8	25	0.33
$M_{bot,st1}$	1	1	16	24	1.65

Table 3-2: Final device sizes and parameters of the CMFB OTA.

Device	**L**(μm)	**W**(μm)	**M**	**gm/Id**	**Id**(nA)
$M_{top,cmfb}$	1	1	1	25	138
$M_{p,cmfb}$	0.1	1	2	25	69
$M_{n,cmfb}$	1	1	2	25	69
$M_{pr,cmfb}$	1	0.12	1	-	-

Gain stage 2

The choices for g_m/I_D and the allocated drain-source voltages of the second gain stage are as follows. For $M_{top,st2}$ and $M_{bot,st2}$ the chosen $g_m/I_D = 25$ with a drain-source voltage of $200mV$. The resulting drain-source voltages of $M_{n,st2}$ and $M_{p,st2}$ are then equal to $350mV$. The g_m/I_D of $M_{n,st2}$ and $M_{p,st2}$ are chosen to be the maximum value for the given gate length.

The device length of the input devices are chosen such that the specified gain requirement are achieved. In order to simplify the layout implementation of gain stage 2, the device lengths of $M_{n,st2}$ and $M_{p,st2}$ are chosen to be equal. Given in figure 3-17 is the gain of the second gain stage calculated using equation 3-4 as a function of the input device length of the second gain stage. From this figure it can be concluded that any device length, the specified gain of $A_{tot} = A_1A_2 > 40$dB is achieved. In order to minimise the area consumption of the second gain stage, a gate length equal to $40nm$ is chosen. The resulting gain stage 2 gain and total gain of the amplifier are then $A_2 = 7.5V/V$ and $A_{tot} = 202V/V$ respectively.

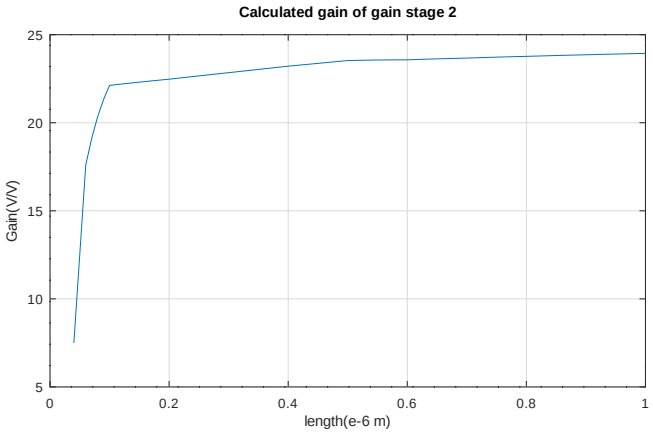


Figure 3-17: Calculated gain of gain stage 2 as a function of the input NMOS and PMOS device length.

Due to first gain stage, the noise contribution of the second gain stage on the total input referred noise of the amplifier system is attenuated by the gain of the first gain stage. Using equation 3-14 the contribution of the second gain stage to the input-referred noise of the amplifier is calculated to be $3.66\mu V_{rms}$. Using equation 3-19 the total input-referred noise of the amplifier is then calculated to be $8.80\mu V_{rms}$ resulting in $4.75\mu V_{rms}$ noise headroom. The value of η is determined by ways of simulation to equal 0.46.

The final device parameters of the second gain stage are summarised in table 3-3. The final

device parameters of the CMFB circuit for gain stage 2 are given in Table 3-2.

Table 3-3: Final device sizes and parameters of gain stage 2.

Device	**L**(μm)	**W**(μm)	**M**	**gm/Id**	**Id**(nA)
$M_{top,st2}$	1	1	4	25	275
$M_{p,st2}$	0.04	1	2	20	55
$M_{n,st2}$	0.04	1	2	20	55
$M_{bot,st2}$	1	1	4	25	275

Gain stage 2 uses body controlled feedback to implement the DSL. As mention in Chapter 1, this is only possible when the cut-in voltage of the body diode is not exceeded. Since body controlled feedback is employed on both the NMOS and PMOS devices, both the cut-in voltage of the NMOS and PMOS devices determine the maximum output voltage swing of the DSL. In order to determine the maximum voltage range of the DSL output, the body diode current as a function of the body voltage is plotted in figure 3-18. From this figure the cut-in voltages of the NMOS and PMOS devices are approximately equals to $710mV$ and $410mV$ respectively. The resulting maximum output swing of the DSL is then calculated to be approximately $300mV$

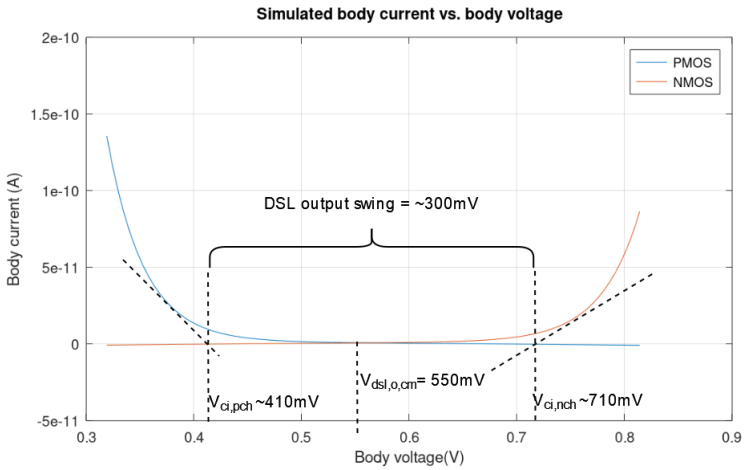


Figure 3-18: Body diode current as a function the body voltage of the NMOS and PMOS devices of gain stage 2 with annotated cut-in voltages, DSL common-mode voltage and maximum DSL output voltage swing.

3-3-2 Shared DSL device parameters

Determining the minimum capacitor values of the shared DSL required to achieve the desired high pass frequency pole is accomplished by rewriting equation 3-8 to equation 3-24. When $A_2 A_{dsl} \eta >> 1$ the equation is further simplified to equation 3-25. By choosing a value for either the switched capacitor $C_{sw,dsl}$, the value of feedback capacitor C_{dsl} is calculated using the capacitor ratio given by equation 3-25.

$$\frac{C_{dsl}}{C_{sw,dsl}} = \frac{1 + A_2 A_{dsl}\eta}{2\pi \frac{f_{hp}}{f_{clock}} |A_{dsl}|} \tag{3-24}$$

$$\frac{C_{dsl}}{C_{sw,dsl}} \approx \frac{A_2 \eta}{2\pi \frac{f_{hp}}{f_{clock}}} \tag{3-25}$$

The transistor dimensions of the DSL OTA are to be chosen such that the approximations given by equations 3-19 and 3-25 are valid. The device length of devices $M_{n,dsl}$ is chosen to be $1\mu m$ to reduce the effects of channel length modulation.

The choices for g_m/I_D and the allocated drain-source voltages of the DSL OTA are as follows. For $M_{top,dsl}$ the chosen $g_m/I_D = 25$ with a drain-source voltage of $200mV$. The resulting drain-source voltage of $M_{p,dsl}$ is then equal to $350mV$. The g_m/I_D of $M_{p,dsl}$ is chosen to be the maximum possible value of the given gate length. The resulting drain-source voltage of $M_{p,dsl}$ is then equal to $550mV$ with a chosen $g_m/I_D = 25$.

Given in figure 3-19 is the gain of the DSL OTA as a function of the input device $M_{p,dsl}$ channel length as calculated using equation 3-9. From this figure it is determined that for an input device length $L_{p,dsl} = 100nm$, the gain of the DSL OTA $A_{dsl} = 21.2V/V$ resulting in $A_2 A_{dsl}\eta = 66.8$.

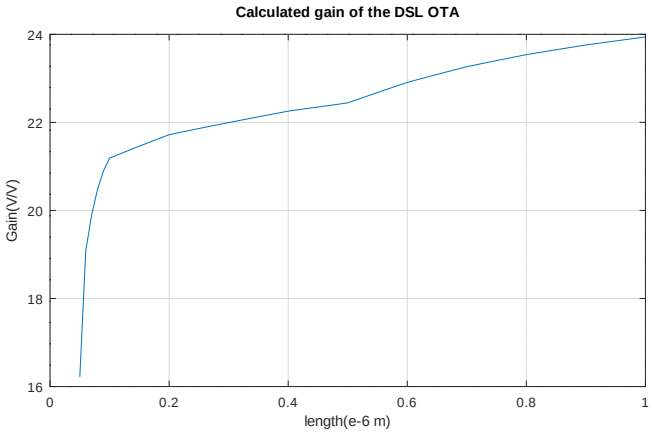


Figure 3-19: Calculated gain of the DSL OTA as a function of the input NMOS and PMOS device length.

Capacitor value $C_{sw,dsl}$ is chosen to be $10fF$. Using equation 3-25 and choosing $f_{hp} = 90Hz$ in order to allow $10Hz$ headroom for process variations, the value of capacitor $C_{sw,dsl}$ is calculated to be $1.23pF$.

The final values of the DSL OTA, switches and capacitor values are given in Tables 3-4, 3-5 and 3-6 respectively. The final device parameters of the CMFB circuit for the DSL are given in Table 3-2.

3-3-3 DC-offset filter

Designing the resistance value R_{dc} by calculating the equivalent resistance of the pseudo resistor structure using equation 3-1 requires that device parameters μ_p and $C_{ox,p}$ are known.

Table 3-4: Final device sizes and parameters of the shared DSL OTA.

Device	**L**(μm)	**W**(μm)	**M**	**gm/Id**	**Id**(nA)
$M_{top,dsl}$	1	1	2	25	138
$M_{p,dsl}$	0.1	1	2	25	69
$M_{n,dsl}$	1	1	2	25	69

Table 3-5: Final device sizes the switches.

Device	**L**(μm)	**W**(μm)	**M**
M_{sw}	0.04	1	1

The calculation of the resistance value is further complicated by the non-zero gate leakage current of the input devices of the first gain stage. The leakage current results in a non-zero voltage drop over the pseudo resistor, resulting in the resistance value calculated by equation 3-1 to no longer be accurate.

The values of the R_{dc} and resulting $f_{hpf,dc}$ are therefore determined via post-layout simulations of the high pass filter. Choosing capacitor value C_{dc} and the device parameters of $M_{pr,dc}$ given in Table 3-7 for $C_{dc} = 624f$F. The DC-offset frequency pole $f_{hpf,dc}$ for the TT, FF and SS process corners are then calculated and given in Table 3-8.

3-3-4 Switched capacitor low pass filter

Given equation 3-13 with low pass frequency $f_{lp} = 5$kHz, the transfer function per definition then yields $\left|H_{dsl}(z|f = f_{lp})\right|^2 = \frac{1}{2}$ resulting in the equality given by equation 3-26. Equation 3-27 calculates the value of $C_{sw,lpf}$ for a chosen value of $f_{enb} = 50kHz$. Given the resulting value for $C_{sw,lpf}$, the capacitor ratio given by equation 3-26 then calculates the value for C_{lpf}. Choosing $f_{lp} = 5.5kHz$ in order to allow $0.5kHz$ headroom for process variations, the final values for both capacitors are given in Table 3-9.

$$\left| \frac{exp\left(-2\pi i \frac{f_{lp}}{f_{clock}}\right)}{1 + \frac{C_{lpf}}{C_{sw,lpf}} - \frac{C_{lpf}}{C_{sw,lpf}} exp\left(-2\pi i \frac{f_{lp}}{f_{clock}}\right)} \right|^2 = \frac{1}{2} \tag{3-26}$$

$$C_{sw,lpf} = \frac{1}{4 f_{enb} R_{o,st2}} \tag{3-27}$$

3-3-5 Constant-g$_m$ biasing device sizing

The required gate voltage $V_{gm,bias}$ to bias the gain stage OTA, DSL OTA and CMFB OTA of the amplifier is determined to be $V_{gm,bias} = 0.77V$ using the precalculated lookup tables. Given $V_{gm,bias}$ the drain-source voltages of devices $M_{p,b2}$ and $M_{n,b2}$ are calculated to be $|V_{ds,p,b2}| = V_{dd} - V_{gm,bias} = 0.33V$ and $V_{ds,n,b2} = V_{gm,bias} = 0.77V$ respectively. Allocating a voltage drop $V_R = 50mV$ over bias resistor R_{bias}, the resulting drain-source voltages

Table 3-6: Capacitor parameters of the shared DSL.

Device	**Value**
$C_{sw,dsl}$	10fF
C_{dsl}	1.25pF

Table 3-7: Final device sizes and parameters of the DC-offset filter.

Device	**L(μm)**	**W(μm)**	**M**
$M_{pr,dc}$	1	120	1

$|V_{ds,p,b1}| = V_{dd} - V_R - V_{gm,bias} = 0.28V$. The drain currents are chosen to be $I_{b1} = I_{b2} = 1.8\mu A$. The g_m/I_D value is chosen to be 25 for all devices.

For the chosen I_{b1} value, the width of $M_{p,b2}$ must equal $24\mu m$. Using the lookup tables, the I_D/W values of $M_{n,b1,2}$ and $M_{p,b1}$ are determined to be $1.1242 \cdot 10^{-8} A/\mu m$ and $1.1242 \cdot 10^{-8} A/\mu m$ respectively. The resulting device width of of $M_{n,b1,2}$ and $M_{p,b1}$ are then calculated to be $12\mu m$ and $144\mu m$ respectively.

$M_{p,su1}$ is sized by choosing a low W/L ratio in order to reduce the drain current I_{su} through the device. $M_{n,su1}$ is then sized to operate in weak inversion. The dimensions of $M_{n,su2}$ are chosen to match those of $M_{n,su1}$.

The final values for the constant-g$_m$ biasing circuits are given in Tables 3-10 and 3-11.

Table 3-8: DC-offset filter parameters per process corner (N = 18).

Parameter	**TT**	**FF**	**SS**
$f_{hpf,dc}(Hz)$	34.59	76.58	17.05
$R_{dc}(G\Omega)$	7.73	3.33	15.0

Table 3-9: Resistor and capacitor parameters of the constant-g$_m$ biasing circuit.

Device	**Value**
$C_{sw,lpf}$	1.23pF
C_{lpf}	256fF

Table 3-10: Final device sizes and parameters of the constant-g$_m$ biasing circuit.

Device	**L**(μm)	**W**(μm)	**M**	**gm/Id**	**Id**(μA)
$M_{p,b1}$	1	1	144	25	1.8
$M_{p,b2}$	1	1	24	25	1.8
$M_{n,b1,2}$	1	1	12	25	1.8
$M_{p,su1}$	10	0.12	1	25	0.44
$M_{n,su1}$	1	1	2	25	0.44
$M_{n,su2}$	1	1	2	-	-

Table 3-11: Resistor parameters of the constant-g$_m$ biasing circuit.

Device	**Value**
R_{bias}	30.3 kΩ

Simulation results

This chapter discusses the post-layout simulation results of the proposed amplifier. Section 4-1 presents the layout and dimensions of the amplifier. Section 4-2 presents the performance parameters of the amplifier in post-layout simulations. The influence of process variations on the obtained performance parameters are discussed in section 4-2-1.

4-1 Layout

The final layout of the amplifier is given in figure 4-1 with each system block annotated. The total area consumption of the complete amplifier equals $89.3\mu m \times 98.11\mu m = 8761\mu m^2$, resulting in a total area per recording channel of $2190\mu m^2$. The layout is used in all simulations performed in this section using temperature $T = 310$K to simulate the operating temperature for which the amplifier is designed.

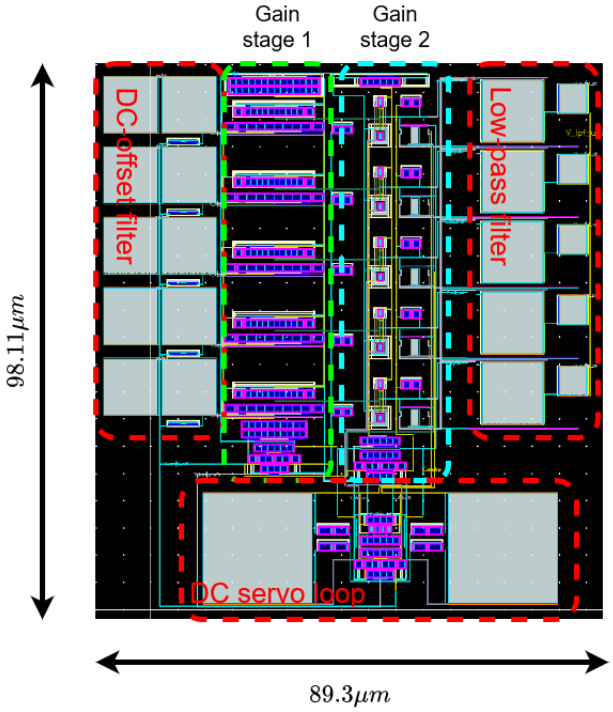
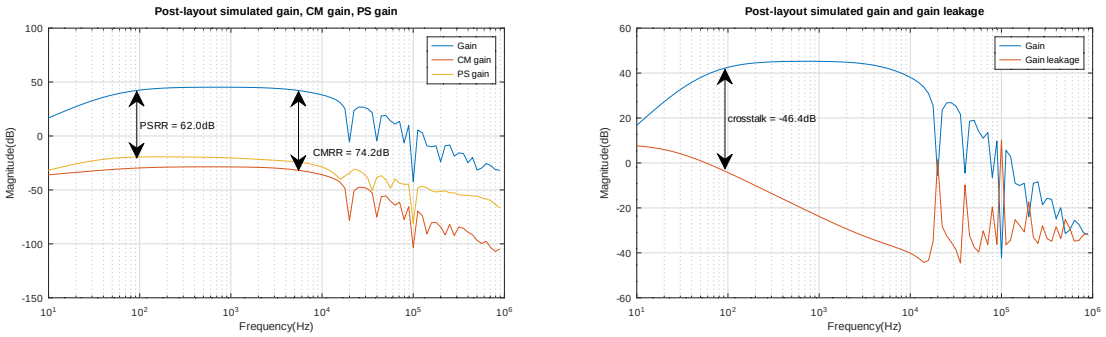


Figure 4-1: Final layout of the amplifier.

4-2 Post-layout simulation results

The gain, common-mode (CM) gain and power supply (PS) gain are plotted in figure 4-2a. From this plot the high and low pass frequencies are determined to be 93.8Hz and 5.44kHz respectively with a midband gain of 45.24dB, which is in close agreement with the results obtained in the pre-layout simulations.

The common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) are determined to be 74.2 dB and 62.0 dB, respectively. The gain and gain leakage as defined by equation 1-29 are plotted in figure 4-2b, the resulting worst-case crosstalk is determined to be -46.6dB at the high pass frequency pole.



(a) **(b)**

Figure 4-2: Obtained plots of (a) simulated gain, CM gain and PS gain with annotated CMRR and PSRR and (b) Simulated gain and gain leakage with annotated crosstalk.

The input-referred noise density of the amplifier is plotted in figure 4-3. The total input noise is calculated over a noise integration bandwidth of [10Hz - 50kHz], resulting in a total input noise of $9.01\mu V_{rms}$. This obtained value is in close agreement with the value found in pre-layout simulations.

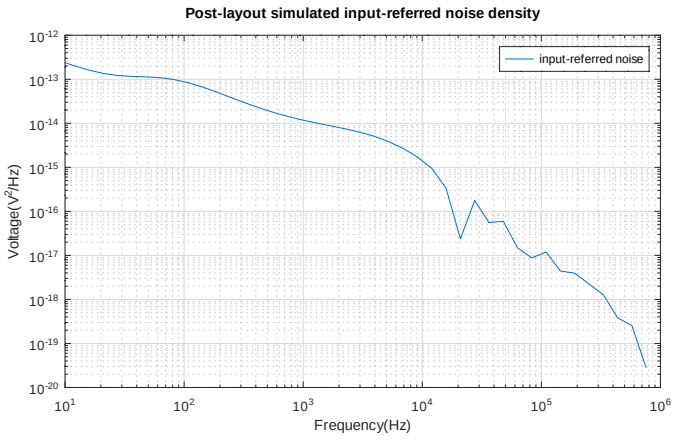


Figure 4-3: Post-layout simulated input-referred noise density plot.

Summarised in table 4-1 are the obtained results of the amplifier during post-layout simulation compared to the required specifications. The obtained results all conform with the stated specifications.

Table 4-1: Obtained performance parameters after post-layout simulation of the amplifier system compared to the specifications

Parameter	**Obtained**	**Specification**
Gain(dB)	45.24	≥ 40
Area/channel(μm^2)	2190	< 2500
Supply voltage(V)	1.1	1.1
Supply current(μA)	2.19	–
Power/channel(μW)	0.603	–
Power/Area(mW/mm^2)	0.275	≤ 1
Low pass frequency(Hz)	93.8	100
High pass frequency(kHz)	5.44	5
Input-referred noise(μV_{rms})	9.00	< 10
NEF	3.40	–
PEF	12.7	–
PSRR(dB)	62.0	–
CMRR(dB)	74.2	–

4-2-1 Monte Carlo corner analysis

To determine the dependency of the performance parameters on random process variations, Monte Carlo corner analysis is performed for all process corners (TT,FS,SF,FF and SS). Choosing the amount of Monte Carlo samples $N = 18$ results in a 95% confidence interval for 1 standard deviation. The obtained values for the gain, high pass and low pass frequency are given in figures 4-4, 4-5 and 4-6 respectively. Based on the obtained values the resulting mean μ and standard deviation σ of the performance parameters per process corner are calculated and given in Table 4-2. The obtained results show a relatively low spread in performance parameters for all process corners.

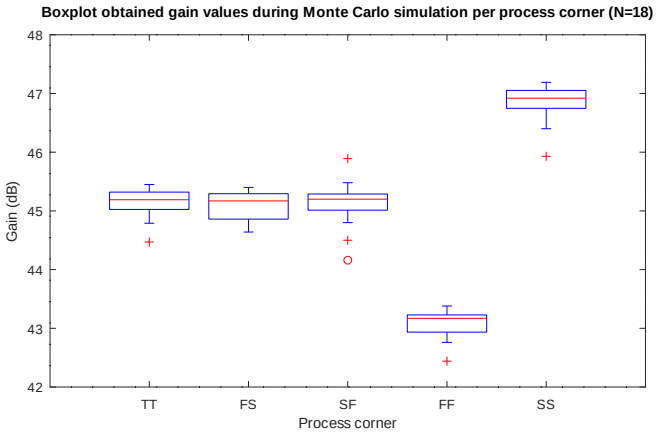


Figure 4-4: Boxplot of obtained gain values for 18 samples per process corner.

Additionally, the gain variations between the individual recording channels of the macro-pixel due to process variations were simulated. The obtained values of the interchannel gain variations are given in figure 4-7. Based on the obtained values the resulting mean μ and

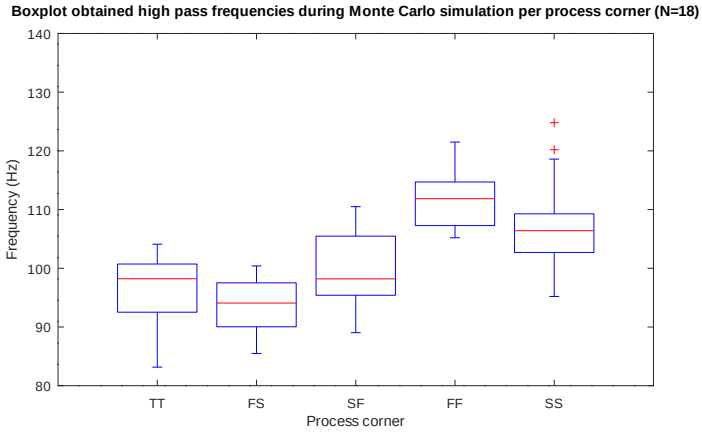


Figure 4-5: Boxplot of obtained high pass frequency values for 18 samples per process corner.

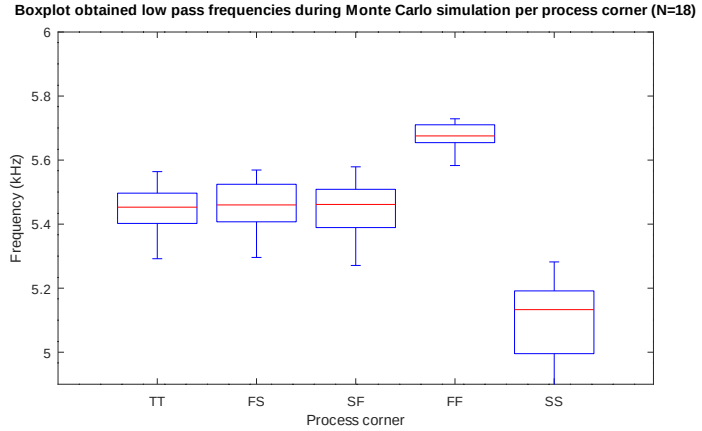


Figure 4-6: Boxplot of obtained low pass frequency values for 18 samples per process corner.

standard deviation σ of the interchannel gain variations per process corner are calculated and given in Table 4-3. The obtained results show low gain differences between the individual channels of macro-pixel for all process corners.

Table 4-2: Performance parameters mean μ and standard deviation σ values obtained from Monte Carlo simulation using $N = 18$ samples per process corner.

Process corner	**Gain**		**High pass frequency**		**Low pass frequency**	
	μ(dB)	σ(dB)	μ(Hz)	σ(Hz)	μ(kHz)	σ(kHz)
TT	45.15	0.25	96.78	5.84	5.45	0.077
FS	45.10	0.24	93.65	4.63	5.46	0.082
SF	45.11	0.38	100.0	6.23	5.45	0.095
FF	43.08	0.25	112.0	5.40	5.68	0.04
SS	46.84	0.31	107.0	7.93	5.09	0.15

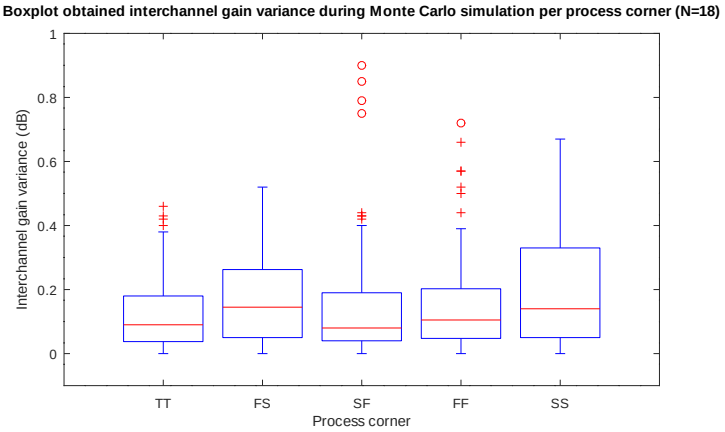


Figure 4-7: Boxplot of obtained interchannel gain variation values for 18 samples per process corner.

4-3 Comparison with state of the art

Given in Table 4-4 are the obtained performance parameters of amplifier compared to the performance parameters of a selection of state of the art amplifiers published in literature. The comparison shows that the proposed amplifier achieves a lower area per recording channel while also obtaining comparable NEF and PEF values.

Table 4-3: Interchannel gain variation mean μ and standard deviation σ values obtained from Monte Carlo simulation using $N = 18$ samples per process corner.

Process corner	**Interchannel gain variation**	
	mu(dB)	sigma(dB)
TT	0.12	0.04
FS	0.17	0.05
SF	0.15	0.10
FF	0.15	0.06
SS	0.20	0.07

Table 4-4: Performance parameters of this work compared to other published works

Parameter	[7]	[8]	[9]	**This work**
Gain(dB)	52	65.5[a]	76.4[b]	45.5
Area/channel(mm^2)	0.018	0.03	0.022	0.0022
Supply voltage(V)	1.2	1.8	1.8	1.1
Supply current/channel(μA)	1.03	5.06	8.89	0.559
Power/channel(μW)	1.24	9.1	16	0.615
Low pass frequency(Hz)	1	1	300	95.4
High pass frequency(kHz)	5	10	10	5.4
Input-referred noise(μV_{rms})	5	4.07	2.4	9.01
NEF	7	3.28	2.71	3.45
PEF	58.8	19.4	13.2	13.1
PSRR(dB)	–	–	–	62.0
CMRR(dB)	65	–	–	74.2

[a] Variable gain of 51.5dB / 59.5dB / 65.5dB.
[b] Maximum gain.

Conclusion

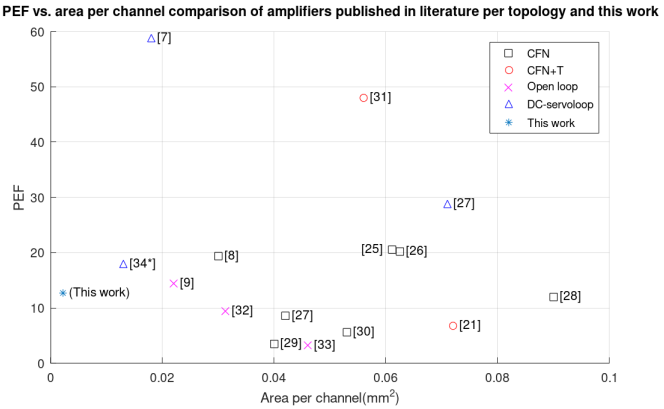
The next generation of brain-machine interfaces (BMI) require neural recording systems with the ability to record the neural activity of large amounts of neurons with single-cell specificity. Here, the design and implementation of a neural amplifier for use in a single-cell resolution BMI was presented and discussed.

A brief overview of neural amplifiers published in literature was presented which served as a prestudy upon which this work was based. The prestudy highlighted and compared amplifier design techniques used in literature to reduce chip area and improve noise and power efficiency.

The main concepts and justification of shared feedback was presented and discussed based on conclusions drawn in the prestudy. The main specifications of the amplifier system were defined and a high level system overview was presented.

The circuit level implementation of the amplifier system was presented and justified such that the main specifications of the system were met.

The proposed amplifier was implemented on layout level and simulated in post-layout simulations. The resulting amplifier achieved a gain of 45.24dB, a chip area consumption of $2190\mu m^2$ per recording channel with a noise and power efficiency factor of $NEF = 3.40$ and $PEF = 12.7$, respectively. The achieved PEF and area of the proposed amplifier and those of amplifiers published in literature is compared in figure 5-1. Monte Carlo simulation were performed and showed that the system is relatively insensitive to process variations.



* Uses off-chip components

Figure 5-1: A comparison in terms of PEF versus area per channel of amplifiers published in literature with the proposed amplifier of this work.

5-1 Future work

The concept of resource sharing presented in this work opens up various possibilities for further research and development, which are discussed below.

1. Although the proposed amplifier uses a DC servo loop to filter out low frequency signals, the amplifier still requires input capacitors to block the DC-offset of the electrodes. These input capacitors consume a substantial amount of chip area. The DC-offset can be largely suppressed by only using a DC servo loop, but this comes at the cost of higher power usage and reduced noise efficiency.

2. Implementing the DC servo loop using a digital low pass filter, as was done by the authors of [7], may further reduce the area per recording channel.

3. The high pass frequency pole filters out local field potentials (LFP) below 100Hz. Some BMI applications may require the measurement of these lower frequency LFP signals. This requires even lower high pass frequency poles. Significantly lower and adjustable high pass frequency poles can be implemented using high value tunable pseudo resistors. The implementation of pseudo resistors does require additional biasing circuitry however.

4. The first gain stage of the proposed amplifier amplifies the input signal by a factor of $28V/V$. Given that the maximum input signal amplitude equals $500\mu V$, the maximum output voltage range equals $536mV \leq V_{o,st1} \leq 564mV$. However the maximum voltage range within which the input devices of the first gain stage are in saturation equals roughly $280mV \leq V_{o,st1} \leq 820mV$. The result of this is that the first gain stage has a significantly larger output voltage swing than is necessary. By supplying the first gain stage with a lower supply voltage, as was done by the authors of [57], the required voltage range to amplify the $500\mu V$ input signal can be achieved while the total power usage of the amplifier can be further reduced.

Finally, the proposed amplifier still needs to be fabricated and measured in an in-vitro experiment.

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