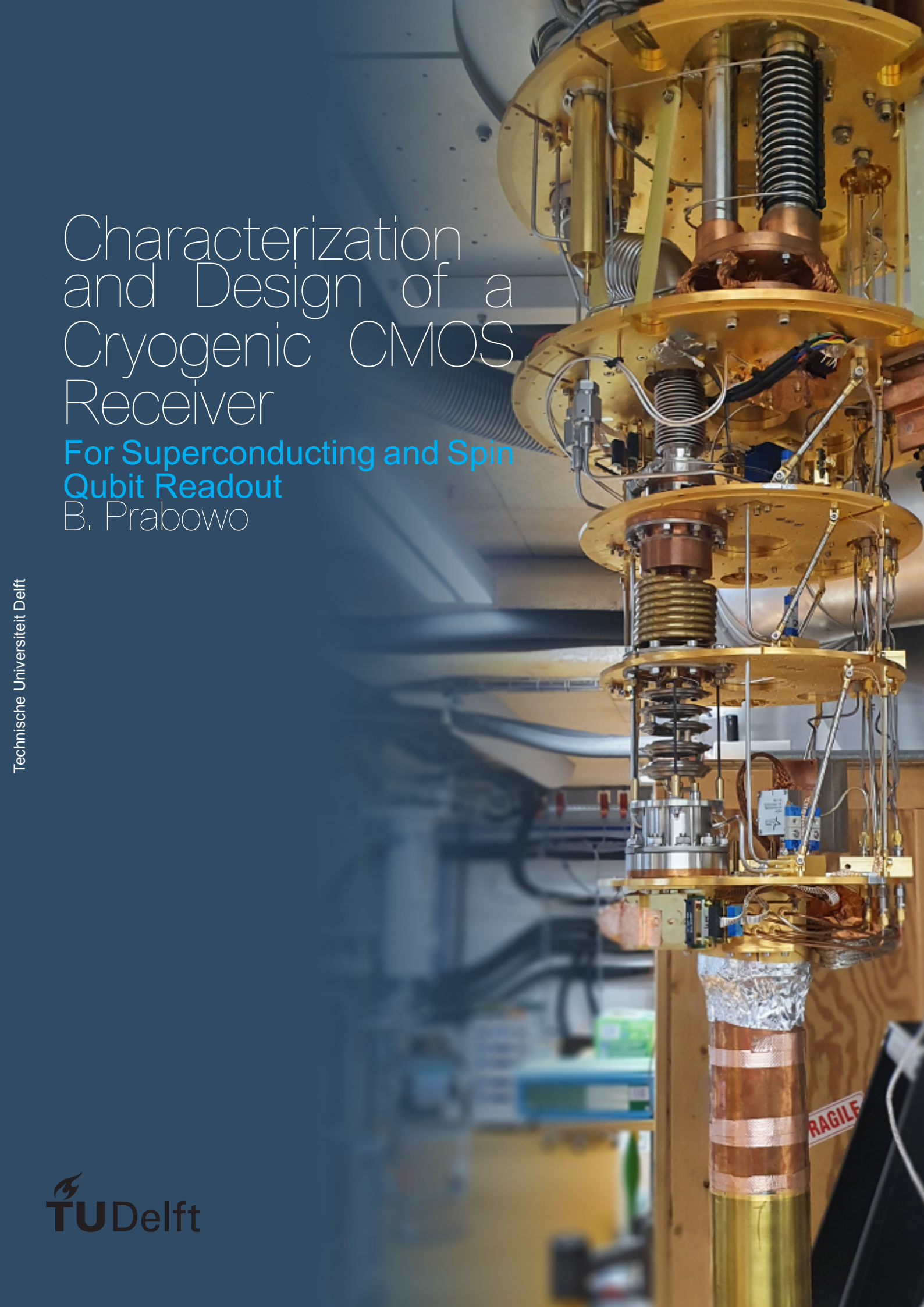
Characterization and Design of a Cryogenic CMOS Receiver

For Superconducting and Spin Qubit Readout

B. Prabowo

Technische Universiteit Delft



TU Delft

Characterization and Design of a Cryogenic CMOS Receiver

For Superconducting and Spin Qubit Readout

by

Bagas Prabowo

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday October 26, 2020 at 9:30 AM.

Student number:	4438655	
Project duration:	August 15, 2019 – October 26, 2020	
Thesis committee:	Dr. M. Babaie,	TU Delft, supervisor
	Dr. F. Sebastiano,	TU Delft
	Dr. M. Spirito,	TU Delft

This thesis is confidential and cannot be made public until October 26, 2023.

TU Delft

Acknowledgments

First of all, I would like to thank my parents for their constant support and encouragement throughout all these years.

I would like to also express my sincere gratitude to my supervisor Dr. Masoud Babaie and to Dr. Fabio Sebastiano for giving me the chance to work on this exciting project. I would also like to thank them for all the discussions we had during the meetings. Overall, the project has been a great learning experience for me. It has been a major collaborative effort between our group and Lieven's group to accomplish this project, and I am thankful for their massive support to make this project happen.

I want to also thank Dr. Marco Spirito for accepting the proposal to be on my thesis committee and sparing his time to read my thesis.

I want to thank Milad for designing and taping out the chip that is used for this project. Without his work, this project would not have been possible. I would also like to thank Milad for the technical support in this project.

I would like to thank all the CoolGroup members for all the technical support, discussion, and the fun times we had. It was an absolute pleasure to be able to work with all of you during this project. A special thanks to Bishnu for all the technical discussions and for assisting me with the different measurements throughout the year. I would also like to thank Zu Yao and Lukasz for their technical help in PCB design and helping me with the countless chip bondings. Thank you to Olaf Benningshof and Nico Alberts too, for assisting me in the enclosure design.

Lastly, I would like to express my thank to Guoji, Patrick, and Jurgen for all the help with the qubit experiments and fruitful discussions. The qubit measurements would not have been possible without your help. I am incredibly grateful for all the support, from installing the chip in the dilution refrigerator to making the last minute measurement before the ISSCC deadline.

B. Prabowo
Delft, October 2020

Abstract

Quantum computers hold a promise to solve intractable problems that can not be solved with classical computers. In quantum computers, information is processed in qubits as opposed to bits. The proper operation of qubits requires them to be operated in a quantum state; hence they need to be cooled down to temperatures well below <1K. Using qubits and their quantum mechanical property, quantum computers can achieve exponential speedup in solving certain computing problems compared to classical computers. However, this can only be achieved by employing thousands of qubits. At the current state of play, quantum computers are still far from practical. The current state-of-the-art solution dictates that each qubit needs multiple interconnects towards room temperature and requires bulky room temperature instruments for qubit readout and control. Clearly, this current solution will not scale well for a quantum computer with many qubits. In an effort to solve this issue, it has been proposed to realize dedicated integrated circuits for control and readout of the qubits and operate them closer to the qubits' operating temperature to enable scalability.

The thesis presents the implementation of an integrated RF receiver for spin and superconducting qubit readout applications. The work aims to replace the bulky room temperature electronics with an integrated solution that operates at 4K to enable scalability and simplification of the quantum computing architecture. The receiver has been designed in the TSMC 40nm CMOS technology and has been characterized in room temperature and 4K. The measured performance shows that the receiver features a gain of 58 dB and a minimum double-sideband noise figure of 0.6 dB at 4K with an operating frequency of 6-8 GHz; a comparable performance to the current state-of-the-art room temperature electronics used for qubit readout. Moreover, this work demonstrates a qubit readout experiment with the integrated receiver in both room temperature and 4K. The qubit readout experiment shows a comparable qubit readout performance with the integrated receiver at room temperature. However, due to oscillation problems, a degradation in qubit readout performance with the chip operating at 4K is observed.

Contents

1 Introduction **1**
- 1.1 Quantum Computing . . . 1
- 1.2 Cryogenic RF Readout . . . 2
- 1.3 Thesis Organization . . . 2

2 Fundamentals of Qubit Readout **5**
- 2.1 Quantum Information . . . 5
- 2.2 Spin Qubit . . . 6
  - 2.2.1 Charge and Stability diagram of DQD . . . 6
  - 2.2.2 Spin Qubit Readout . . . 8
- 2.3 Superconducting Qubit Readout . . . 12
- 2.4 Readout Survey . . . 13
  - 2.4.1 Readout electronics for Qubit Readout . . . 13
  - 2.4.2 State of the art solution . . . 13

3 System Design **15**
- 3.1 Behavior of CMOS process in Cryogenic Environment . . . 15
  - 3.1.1 DC Transistor Behaviour . . . 15
  - 3.1.2 Dynamic Transistor Behaviour . . . 15
  - 3.1.3 Passives Behaviour . . . 16
- 3.2 Receiver Architecture . . . 18
  - 3.2.1 Noise Figure . . . 18
  - 3.2.2 Gain . . . 19
  - 3.2.3 Linearity . . . 20
  - 3.2.4 Power . . . 21
  - 3.2.5 Specification Summary . . . 21
- 3.3 LNA . . . 21
  - 3.3.1 Analysis of a CS Stage Amplifier . . . 22
  - 3.3.2 Design of the Readout LNA . . . 23
  - 3.3.3 Simulation Result . . . 27
- 3.4 Mixer . . . 29
  - 3.4.1 Design and Consideration . . . 29
  - 3.4.2 Simulation Result . . . 31
- 3.5 IF Amplifier and Buffer . . . 32
  - 3.5.1 Design and Consideration . . . 32
  - 3.5.2 Simulation Result . . . 32
- 3.6 LO Driver . . . 34
  - 3.6.1 Design and Consideration . . . 34
  - 3.6.2 Simulation . . . 35
- 3.7 RX Chain . . . 36
  - 3.7.1 Simulation Result . . . 36
- 3.8 FDMA Qubit Readout Architecture . . . 38

4 Measurement **41**
- 4.1 Dip-stick Measurement . . . 41
  - 4.1.1 Hot and Cold Y-Factor Measurement . . . 42
  - 4.1.2 Measurement Setup . . . 43
  - 4.1.3 Result . . . 44
  - 4.1.4 Power . . . 44

4.2 Probe-Station Measurement . . . 45
4.2.1 Setup . . . 45
4.2.2 Gain . . . 45
4.2.3 S11 . . . 47
4.2.4 EVM . . . 48
4.2.5 Linearity . . . 49
4.3 RX Performance Summary . . . 50
4.4 Qubit Measurement . . . 51
4.4.1 Background . . . 51
4.4.2 RT Qubit Measurement Setup . . . 52
4.4.3 RT Qubit Measurement Result . . . 52
4.4.4 4K Qubit Measurement Setup . . . 55
4.4.5 4K Qubit Measurement Result . . . 55
4.5 Comparison to the State-of-the-art . . . 57

5 Conclusion **59**
5.1 Main Conclusion . . . 59
5.2 Future Work . . . 60

Bibliography **61**

A Coupled Transformer Derivation **65**

B Cold Attenuation Y-Factor Derivation **67**

1 Introduction

1.1. Quantum Computing

Suggested at almost four decades ago by Feynman [16], the idea of quantum computing has seen significant growth and interest throughout the years from academia and industry. Over the course of decades, the field has achieved significant advances from different disciplines that is involved into developing a practical quantum computer [5, 43, 45].

What makes quantum computers different than classical computers is how information is represented and processed. In quantum computers, information is represented by the quantum states of the quantum bits or qubits. Unlike classical computers, however, qubits are probabilistic in nature and possess special properties, namely superposition and entanglement [16]. By exploiting the quantum mechanical behavior of qubits, quantum computers can enable new computing frontiers such as drug and material synthesis, big prime number factorization for cyber-security application, and probabilistic random number generators [44].

At the current state of play, quantum computers are still far from practical. For quantum computers to run practical algorithms, quantum computers need thousands of qubits to be manipulated coherently with known quantum algorithms and error correction methods [17]. The current solution dictates that each qubit, operating inside a dilution refrigerator at mK temperatures, requires several room tempera-

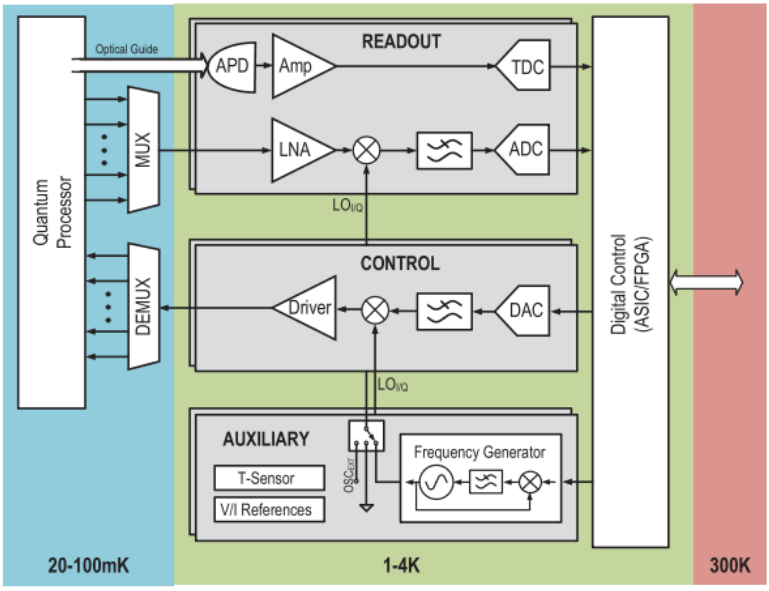


Figure 1.1: Schematic block diagram of a scalable quantum computer. The system is composed of an integrated readout and control circuitry operating at 1-4K. Image adapted from [36].

ture (RT) instruments for control and readout processes. This approach, however, would be a limitation for scalability as the number of qubits grows. Furthermore, the long cables that interface the qubits inside the dilution fridge can add significant delays, which is undesirable in a quantum computer with a quantum error correction loop [17].

To address quantum computers' scalability, research suggests that control and readout electronics need to be co-integrated closer to the qubit's operating temperature [36]. The proposed architecture is depicted in Figure 1.1, where it can be seen that all electronics are placed at the 1-4 K stage of the dilution refrigerator. Following this approach, interconnect and delay issues regarding control and readout of the qubits from RT are alleviated, thus reducing the system cost and complexity. However, it does come with other challenges. Firstly, cooling power inside the current state-of-the-art dilution refrigerators is limited. Hence, any electronics designed to be operated in the dilution refrigerator has to be very power efficient. Secondly, transistor behavior at cryogenic operation is still mostly unexplored. Currently, transistors' behavior at cryogenic temperatures is still an ongoing research subject, leading to more empirical-based electronic designs.

1.2. Cryogenic RF Readout

Currently, multiple qubit implementation exists, and each of them offers different benefits and drawbacks. Solid-state qubits, such as spin and superconducting qubits, are among the leading candidates for qubits used in a large scale quantum computer as qubit control and readout can be done electrically.

Research has recently shown that spin and superconducting qubits can be read out using a similar readout technique called the dispersive readout technique [22, 49]. Much interest is observed from the community in using this readout technique as it allows the possibility of a single readout circuitry to support two different qubit platforms. As it will be explained further in Chapter 2, reading the qubit's state will involve detecting the qubit structure's state-dependent frequency response through an S-parameter like measurement. By sending an RF probe signal to the qubit's structure, the different amplitude/phase state-dependent response can be observed using an I/Q demodulation. Currently, readout with this technique requires bulky, power-hungry components operating at RT. As mentioned previously, this method is not favorable towards realizing a large-scale quantum computer. Hence, there is a need for a better-integrated solution for readout.

This thesis will focus on the implementation of a wideband cryogenic CMOS RF receiver that supports the dispersive qubit readout technique for spin and superconducting qubits. The work aims to tackle the scalability issue by replacing the bulky, power-hungry RT instruments used for qubit readout. This work proposes integrating the qubit readout circuitry closer to the qubit's operating temperature to alleviate the interconnects and delay issues that can arise in a large-scale quantum computer.

It should be noted that the cryogenic CMOS RF receiver presented in this thesis has been taped-out and designed prior to the start of the project. This thesis mainly contributes to the characterization of the chip's performance in RT and 4K along with the integration of the designed chip with the qubits inside the dilution refrigerator for qubit readout experiments. Nevertheless, the chip's architecture will still be discussed in this work, with its main novelty highlighted.

1.3. Thesis Organization

The thesis is divided into the following chapters:

- Chapter 2 discusses the fundamentals of qubit readout. An introductory discussion on the operation and readout techniques used for spin qubits is shown in this section with an emphasis on the dispersive spin qubit readout. A brief review of the superconducting qubit readout is also discussed as this type of qubit uses the same technique used in the dispersive spin qubit readout.

- Chapter 3 mainly discusses the system architecture of the chip. The chapter starts with a review of CMOS technology's behavior at cryogenic temperatures and moves to the design of each receiver's block, namely the LNA, mixer, IF amplifiers, buffers, and LO drivers. Design considerations are discussed in each respective RX component along with their simulation results. Moreover, a discussion on the FDMA architecture for qubit readout is presented in this chapter.

- Chapter 4 presents the result of the characterization of the chip in both RT and 4K. Furthermore, the chapter also presents qubit measurement results from integrating the RX chip with a qubit sample in the dilution fridge.
- Chapter 5 concludes the thesis and the future outlook derived from this project for further improvements.

2

Fundamentals of Qubit Readout

The following chapter will discuss mainly the fundamentals of qubit readout for a quantum computer. A brief introduction to quantum information is presented in this chapter to introduce how information is encoded in a quantum computer. This chapter will mostly emphasize the fundamentals of readout for spin qubits. However, a brief discussion is still done on how this type of readout can still apply to superconducting qubits. A section dedicated to the survey of different qubit readout setup will also be presented in this chapter, motivating some system design specifications.

2.1. Quantum Information

The state of a quantum system are often represented in the state equation shown in equation 2.1. Represented in Dirac notation [1], the $|1\rangle$ and $|0\rangle$ equivalently represents the classical state 1 and 0, respectively. The peculiarities of a quantum state can also be observed from equation 2.1. From the equation shown, it can be seen that the system's total state is represented by both $|1\rangle$ and $|0\rangle$ due to the ability of a quantum state to hold a superposition state. The variable α and β are complex coefficients and satisfies $|\alpha|^2 + |\beta|^2 = 1$ in which the magnitude of the coefficients represents the probability of each respective state.

Equation 2.1 can be visually represented to what is known as a Bloch sphere, as shown in Figure 2.1. The equivalent state description of the Bloch sphere is presented in equation 2.2. The qubit's state can be anywhere on the Bloch sphere's surface. The state of the qubit ($|\psi\rangle$) can be understood as a vector that points into a state and can be manipulated through the use of quantum gates [33]. While it may seem that a qubit can represent an infinite number of states, the act of measuring a qubit will effectively 'projects' the quantum state into one of the axes of the Bloch sphere[2]. Moreover, any superposition state of the qubit also collapses into $|1\rangle$ or $|0\rangle$ by the act of measurement.

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \tag{2.1}$$

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle \tag{2.2}$$

The state of a qubit will not last very long due to the interaction with its environment. This process is often called decoherence. For instance, the excited state of a qubit $|1\rangle$ will eventually decay into $|0\rangle$. The decay time is often characterized as the T_1 time. Another figure-of-merit that is often quoted is the T_2^* time of the qubit. This value defines how well the qubit can hold a superposition state. It is a measure of how long a qubit state can hold its phase value ($e^{i\phi}$) before it starts to dephase, as shown in equation 2.2. Together, the two parameters can define how good the qubit is and determine how fast one can control and readout the qubit. It is essential that readout is done in 'one-shot' and be

[1] Often also called Bra-Ket notation. With Bra noted as $\langle x|$ and Ket as $|x\rangle$.

[2] Canonically, measurement basis of the measurement is the z-axis of the Bloch sphere. Consequently, the act of measuring a qubit will only give the output $|1\rangle$ or $|0\rangle$ with a certain probability.

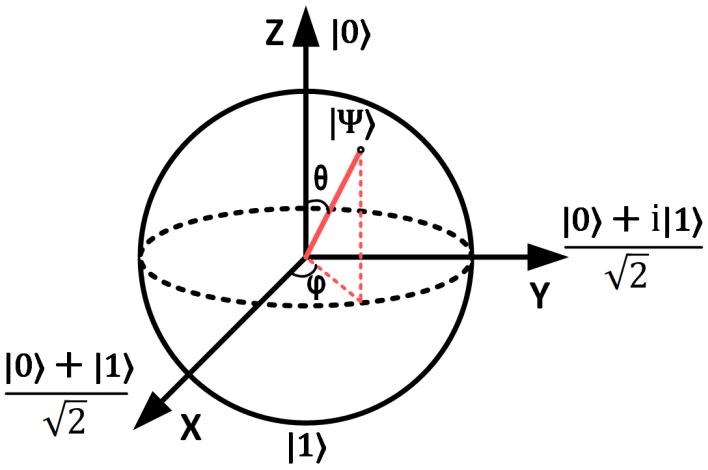


Figure 2.1: Bloch sphere diagram representing the state of the qubit.

done significantly faster than the T_1 time. When quantum error correction is considered, the readout will need to be faster than the T_2^* to be able to correct the encoded qubit states [17].

Physically, the state $|1\rangle$ and $|0\rangle$ are always mapped from the degrees of freedom of the quantum system. Depending on the qubit technology, the state $|1\rangle$ and $|0\rangle$ will be mapped to different quantized aspects of the quantum system. For instance, in the case of spin qubits, the state $|1\rangle$ and $|0\rangle$ are canonically mapped to spin-up and spin-down of an electron. Other qubit technologies such as superconducting qubits (i.e., Charge qubit) make use of the number of charges/Cooper pairs occupying the system to indicate the state $|1\rangle$ and $|0\rangle$ [26]. In general, qubit control and readout of one platform can not be applied to another. However, the readout technique presented in this thesis is one of the few exceptions. The readout technique explained in this thesis can be applied to both superconducting qubits and spin qubits, which is advantageous in terms of flexibility in the application.

2.2. Spin Qubit

In spin qubits, quantum information is encoded in the spin states of the electrons where the spin states, spin-up or spin-down, is mapped into the $|1\rangle$ and $|0\rangle$ basis, respectively. The realization of spin qubits is achieved by fabricating quantum dot structures such as shown in Figure 2.2, where it can be implemented in GaAs, SiGe, or Si substrate. In this thesis, only double quantum dot (DQD) spin qubits are considered (for a more extensive review of spin qubits in quantum dots, refer to Ref [20]).

In the DQD structure shown in Figure 2.2, spin qubits are formed by trapping free electrons in a potential well. The potential well is created by manipulating the 2D-electron gas (2DEG) layer formed from the interface between the AlGaAs layer and the GaAs substrate [20]. By applying voltages at the gate on top of this 2DEG layer, a potential well (or equivalently, quantum dot) can be shaped in the interface layer in which electrons can hop into. By controlling the device's gates, one can control the electron population in the potential well by filling it discretely. In other words, the potential well ensures that the population of electrons in the quantum dot is quantized, allowing control of a single electron that is necessary for a spin qubit.

2.2.1. Charge and Stability diagram of DQD

The operation of a DQD is dependent on how the device is biased. The DQD behaves as a function of the population of charges[3] occupying the dot and the charges' spin orientation. There are two essential diagrams which characterize the quantum dots: the charge stability diagram and the energy level diagram. For a DQD, the charge stability diagram and the energy level diagram is shown in Figure 2.3. It should be noted that V_{LP} and V_{RP} correspond to the left and right plunger gates of the device shown in Figure 2.3d.

The charge stability diagram indicates the number of electrons that are confined in the dot. The

[3]This thesis will focus on electron charges in this thesis. There are, however, implementations of DQD qubits with holes.

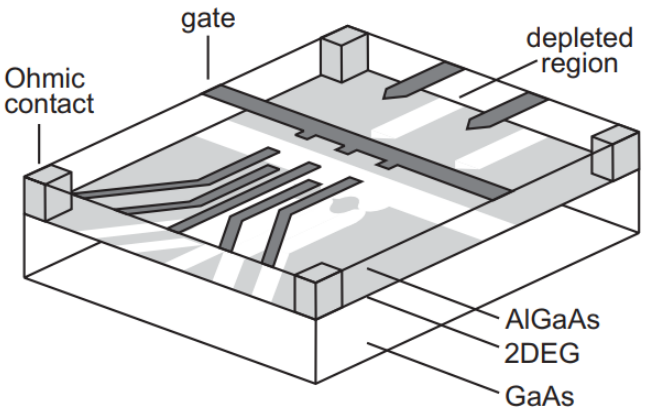


Figure 2.2: Double Quantum Dot (DQD) structure in GaAs substrate. Grey shaded region shows the 2D-electron gas layer while white shaded region shows the depleted regions where no electrons existed.[20]

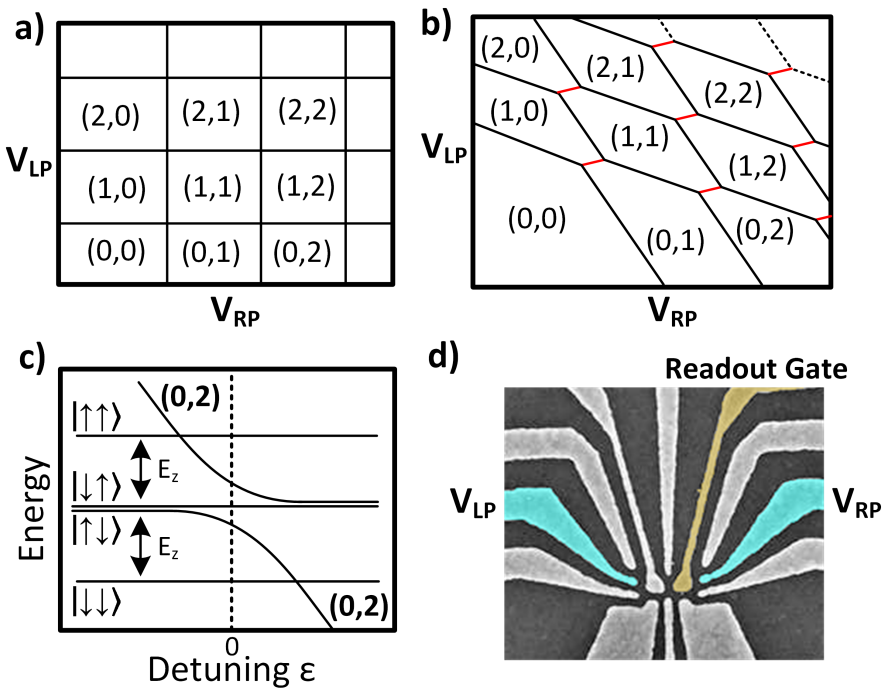


Figure 2.3: a) Sketch of charge stability diagram without coupling. (N_L,N_R) describes the number of charges inside the left and right dot, respectively. Black lines indicate the point at which an additional charge is added to each quantum dot. b) Charge stability diagram with coupling. c) Corresponding energy diagram of a coupled DQD at the (1,1)-(0,2) regime. d) SEM image of a DQD. Left and right plunger gates indicated in blue, and the gate connected to a resonator colored in yellow.

black transition lines in the sketch indicate the point where electron from the reservoir can tunnel into the dot, thereby increasing the population of electrons inside the dot. The numbers (N_L, N_R) represent the number of electrons inside the left and right dot, respectively. In the case of no coupling between the two dots, the charge stability diagram resembles two overlapping stability diagrams of a single quantum dot, as shown from 2.3a. When the coupling is introduced between the two dots, the charge stability diagram transforms to Figure 2.3b. Due to coupling, the neighboring dot's occupation influences the other dot's charging energy and hence requires higher gate voltages to overcome the electronic repulsion. Moreover, an important regime for the operation of a DQD qubit is the interdot crossing. Indicated by the red line between the 'triple points' of the charge state, the interdot crossing regime marks where the electron can move from one dot to another while keeping the number of electrons between the two dots constant. This regime will be necessary for the spin qubit readout techniques used for this thesis.

A sketch of the energy level diagram of a DQD is shown in Figure 2.3c. In this case, the energy diagram shows the energy level of different electronic states at the (1,1)-(0,2) charge regime where the spin qubit is usually biased. The detuning on the x-axis represents the electrochemical potential difference between the two quantum dots. This parameter is controlled by the voltage applied on the plunger gates (V_{LP} and V_{RP}) shown in Figure 2.3d. At 0 detuning, the electrochemical potential between the two dots is zero. At this point, the DQD is biased at the interdot crossing regime. The label (0,2) in the diagram indicates the charge state's energy band in which both electrons occupy the right quantum dot[4]. At large negative detuning, the electrons move into the (1,1) charge state. In this regime, the two electrons in the system are spatially separate and occupy each corresponding dots. The labels shown in the diagram ($|\uparrow\uparrow\rangle$, $|\downarrow\uparrow\rangle$, $|\uparrow\downarrow\rangle$, and $|\downarrow\downarrow\rangle$) represents the spin state of each electron in each respective left and right dot with its corresponding energy level in each configuration. E_z, on the other hand, denotes the Zeeman splitting energy of the spin states due to an external magnetic field application. Without an application of an external magnetic field, all the states ($|\uparrow\uparrow\rangle$, $|\downarrow\uparrow\rangle$, $|\uparrow\downarrow\rangle$, $|\downarrow\downarrow\rangle$) at negative detuning will become degenerate[5] [39], preventing one from differentiating the spin states and preventing the DQD from acting as a qubit. As discussed later, this work will only focus on the two-level system between $|\uparrow\downarrow\rangle$ and $|\downarrow\downarrow\rangle$. The right dot is used as a reference qubit to measure the left qubit's relative spin orientation in this spin qubit readout scheme.

2.2.2. Spin Qubit Readout

DC Readout

Due to the difficulty in directly reading an electrons' spins, multiple techniques have been researched to correlate the spin of an electron into other observable variables. In most cases, this involved correlating the qubit's spin state to information based on the qubit charges. For instance, the DC readout method, such as the 'Elzerman technique,' depends on the electron's occupation inside the quantum dot itself [14]. Due to the spin-up and spin-down states' energy gap, the qubit can be biased during readout such that only a particular electron with a specific spin can tunnel out of the quantum dot back and go back into the reservoir. As the electron tunnels out of the quantum dot, a voltage/current pulse can be registered and detected by a nearby electrometer. The electrometer can be realized by a quantum point contact (QPC) or a single electron transistor (SET) structure. However, this technique is often bandwidth limited due to the parasitic capacitance between the electrometer and the amplifier used for readout [13], thus making fast readout difficult. Moreover, such a readout scheme is limited by the high 1/f noise observed in cryogenic temperatures, as discussed later on.

Reflectometry Readout

One of the most popular RF readout technique that is used currently for a spin qubit is the reflectometry readout with QPC/SET structures. The schematic of this measurement setup is shown in Figure 2.4. Like DC readout, the QPC/SET structure is used to sense the quantum dot's population changes. Any changes in the dot population will effectively influence the biasing of the nearby QPC/SET structure and consequently change the structure's impedance [20]. By applying an RF probe signal into the QPC/SET structure, one can measure the changes in the QPC/SET structure's impedance by observing how much power is reflected. An I/Q receiver is typically used to detect any phase/amplitude changes of the incident RF wave. However, this method requires additional QPC/SET structures along with

[4] A more accurate description is that this state is a Singlet (0,2) state in which the electrons have opposite spins. In some cases, this state is used as a ground state in which the qubits can be initialized.

[5] An energy level is said to be degenerate when the energy level represents two or more quantum states.

the qubit, which increases its overall footprint of the device and hinders the potential for scalability. Moreover, such a method requires a bulky off-chip matching network that is problematic for large scale quantum computing platforms. The relatively low Q of the discrete passives used in this method can also limit the SNR of the readout signal.

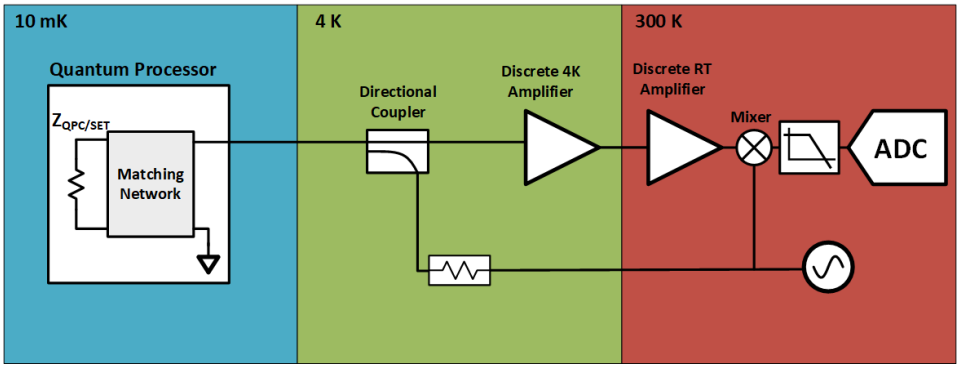


Figure 2.4: Typical measurement setup for gate based measurement readout. Note that the readout chain's I/Q path is not illustrated in this figure for simplicity purposes.

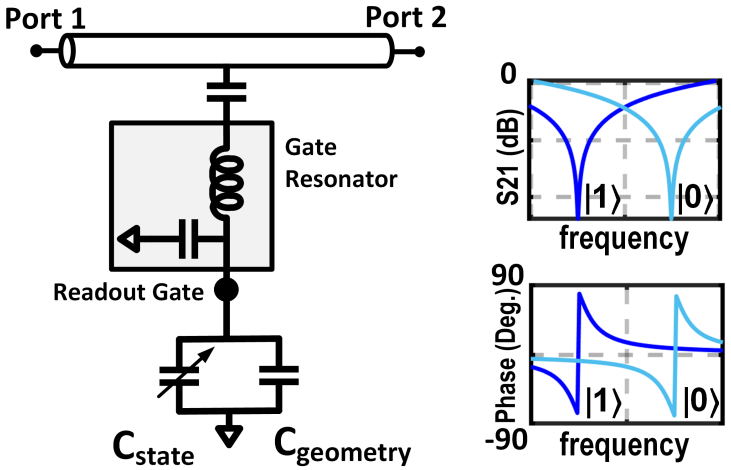


Figure 2.5: Equivalent model of a DQD in a gate dispersive readout architecture.

Gate-Dispersive Readout

A more recent method of reading the spin qubit's state is through a technique known as dispersive gate readout [12, 35, 49]. This is realized by coupling the gate of the DQD to a superconducting resonator (See Figure 2.3 and Figure 2.5). This type of readout, which is the focus of this thesis, offers some advantages compared to reflectometry techniques. For instance, due to the significantly high Q of the superconducting resonator used at the gate, this measurement method provides benefits in terms of increased SNR [49]. Moreover, in contrast to SET/QPC reflectometry readout, no additional structures are required for this type of readout as gate electrodes are already present in a DQD device.

An equivalent circuit model of this readout method is illustrated in Figure 2.5. The equivalent impedance of the DQD structure can be modeled as two parallel capacitors composed of a state-dependent capacitor and a fixed geometric capacitance of the DQD [31]. Together with the gate resonator, the qubit will have a state-dependent resonant frequency response (typically resonant shift in the order of 5 MHz) when probed from the common readout line, as shown in Figure 2.5. The typical measurement setup for such a system is shown in Figure 2.6. Similar to the ones showed in the Figure 2.4, the measurement setup in Figure 2.6 is composed of LNAs, I/Q mixer, and baseband amplifiers to detect the changes in the modulated RF signal.

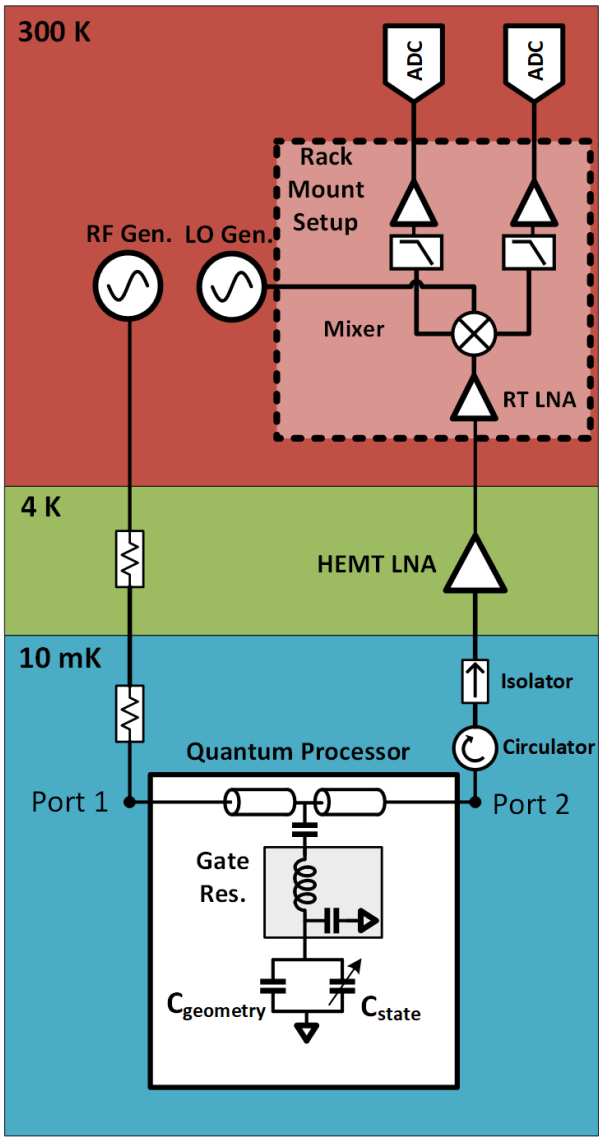


Figure 2.6: Typical measurement setup for gate based measurement readout.

A typical readout process of a spin qubit with dispersive technique is explained below and illustrated in Figure 2.7. As mentioned previously, this work will only focus on the two-level quantum states formed by the $|\uparrow\downarrow\rangle$ and $|\downarrow\downarrow\rangle$ states. The simplified energy level diagram and the stability diagram are shown in Figure 2.7b and 2.7c, respectively. It should be noted that other charge states and energy levels are omitted for simplicity.

1. To start any quantum operation, the qubit needs to be initialized to a known state. One possible way to initialize the qubit is to bias the qubit at the point I, as labeled from Figure 2.7b where the qubit is biased at positive detuning. This effectively initialized the qubit to be at the $|\downarrow\downarrow\rangle$ (0,2) ground state as shown from 2.7a.

2. Before manipulating the left qubit, the electrons in the quantum dot needs to be separated. This is accomplished by biasing the qubit into the negative detuning allowing it to be in the (1,1) charge state where both electrons are in each dots. Lowering the detuning of the DQD can be done by lowering the voltage (V_{RP}) of the right plunger gate, which is indicated in Figure 2.3d.

3. Manipulation occurs at negative detuning (point M in Figure 2.7b) where a microwave signal is applied to the left qubit to execute single-qubit gate operations. No microwave pulse should be applied to the right qubit as it will be used as a reference spin for readout.

4. After manipulation occurs, qubit readout can be done by bringing the qubit back to the interdot crossing ($\epsilon = 0$). This biasing point is labeled as R1 and R2 in Figure 2.7b. At this point, the electrochemical potential difference between the two quantum dots is 0. Consequently, the electron on the left dot is allowed to tunnel to the right dot if and only if it has an opposite spin relative to the right dot due to the Pauli exclusion principle.

5. The readout is done by applying an RF signal at the gate of the DQD with the frequency equivalent to the gate's resonant frequency for a duration of t_{int} (integration time). Due to the application of RF wave at the gate of the DQD, the electron from the left dot can oscillate between the two dots and induced an additional capacitance[6] which increases the total capacitance of the DQD. This is illustrated at the bottom of Figure 2.7a. Through I/Q demodulation, the amplitude/phase variation experienced by the RF probe signal can be observed, allowing one to distinguish the qubit's states.

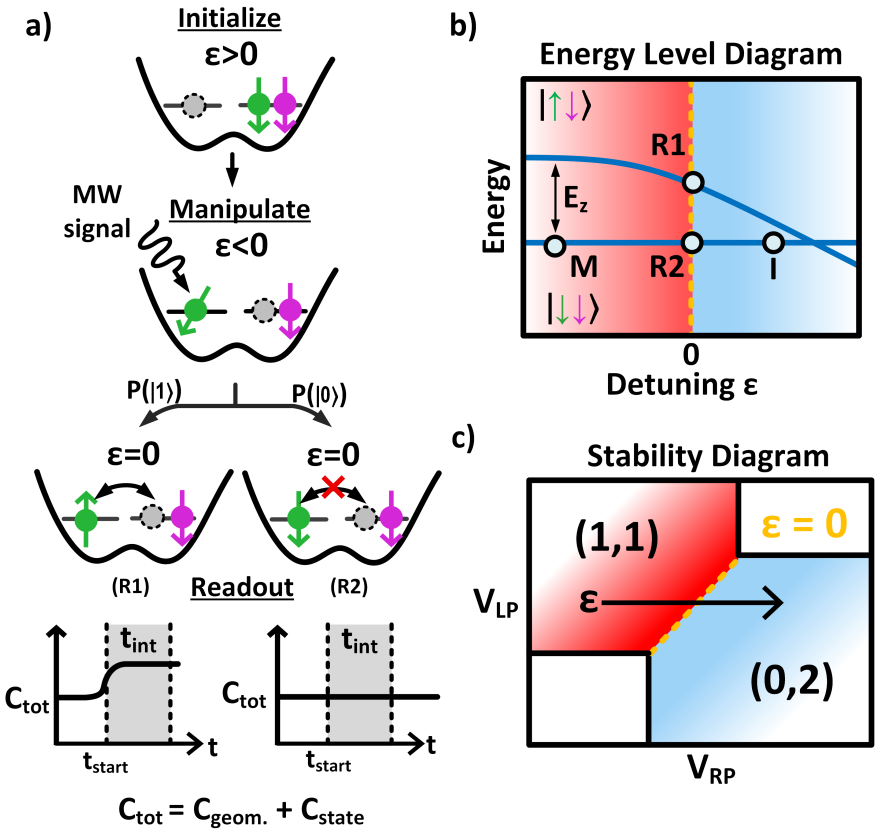


Figure 2.7: Operation of a DQD with gate dispersive readout architecture. a) Sketch of the qubit in different steps of manipulation b) Simplified energy level diagram of the two-level system. c) Stability diagram of the DQD at (1,1)-(0,2) regime.

[6] More accurately described as the tunneling capacitance [31].

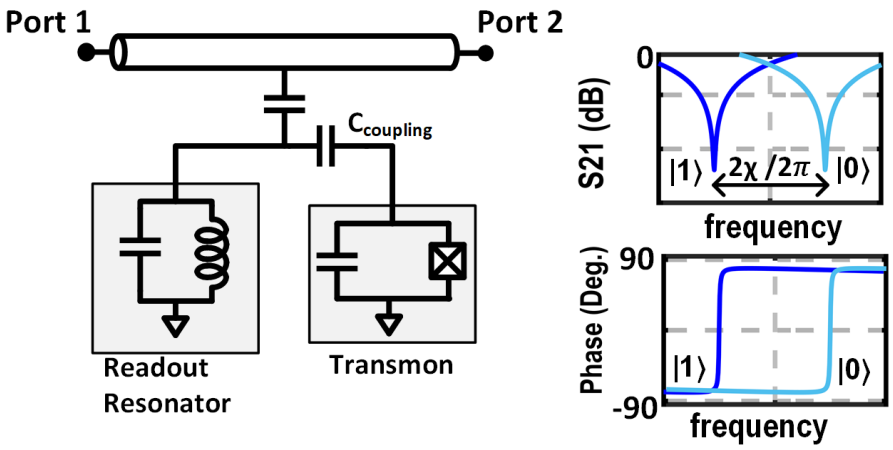


Figure 2.8: Equivalent model of a Transmon readout line.

2.3. Superconducting Qubit Readout

While this thesis mainly emphasizes on RF gate spin qubit readout, the technique still applies to the superconducting qubit. Both readout method ultimately relies on dispersive readout techniques and hence behaves similarly. Currently, several different types of superconducting qubits exist. However, this section will only limit itself and briefly discuss the readout of the transmon superconducting qubit. For further details on different superconducting qubits, the reader is advised to read Ref [26].

The realization of a transmon qubit is based on a superconducting LC circuit that utilizes the Josephson junction. The transmon qubit is capacitively coupled to a superconducting readout resonator, which is also capacitively coupled to a common readout line. This is depicted in Figure 2.8. The Hamiltonian[7] that describes the behavior of the system in shown in equation 2.3 [25].

$$H = \hbar(\omega_r + \chi\sigma_x)a^\dagger a + \frac{\omega_q \hbar}{2}\sigma_z \tag{2.3}$$

Where ω_r is the resonator's resonant frequency, ω_q is the qubit's state transition frequency, a ($a^\dagger$) is the creation (annihilation) operators, σ_i is the Pauli operators, and χ is the state dependent "pull" frequency.

From the simple Hamiltonian model shown in equation 2.3, χ describes the positive (negative) resonant shift of the resonator due to the ground (excited) state of the qubit, as shown in figure 2.8. Similar to dispersive readout for spin qubits, the qubit state is detected by observing the resonator's state-dependent frequency response. The readout is typically done by probing an RF signal at the center frequency between the possible resonant shifts. Doing so would produce a phase modulated RF signal at the output of port 2.

A typical readout setup for transmons is shown in Figure 2.9. Setup shows that transmon readout is very similar to the ones used for gate-based spin qubit readout. However, Some critical differences between the two readout setup can be noted. For example, the total receiver gain for transmon readout is >120 dB, significantly higher than for spin qubit gate based readout. The high gain is required because transmon qubit can only be read out by low power RF signal to keep the transmon in the dispersive regime. Parametric amplifiers are also used in the transmon readout to conserve the readout chain's noise figure performance.

[7], The following Hamiltonian, is only valid when the system is in the dispersive regime where the difference in the resonator's resonant frequency and the qubit transition energy is vastly different from the coupling rate between the resonator and the qubit [25].

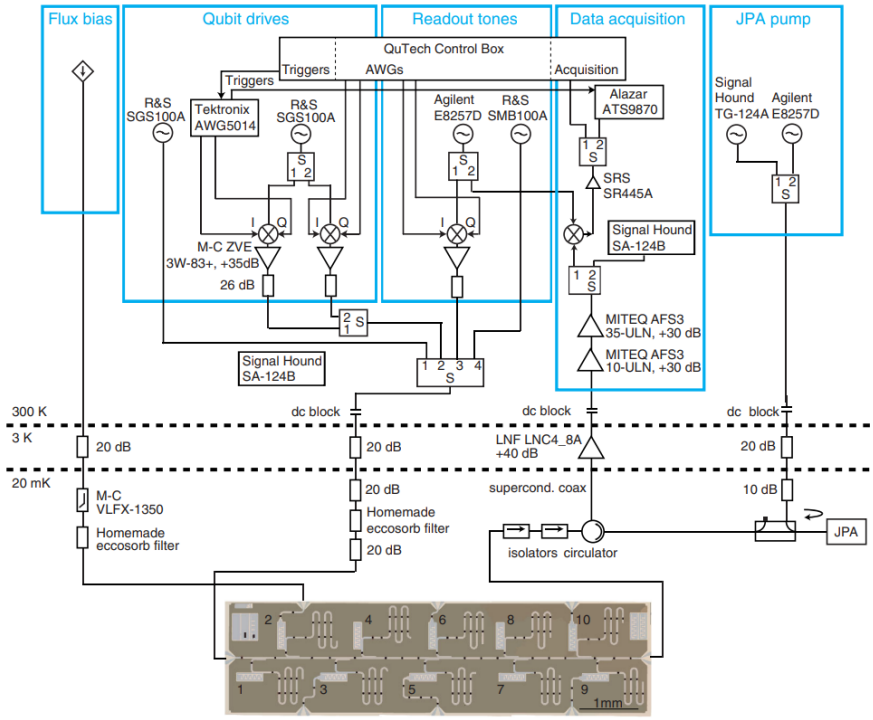


Figure 2.9: State of the art Transmon control and readout setup [9]

	P. Krantz, 2016[25]	J. Heinsoo, 2018[22]	G. Zheng, 2019[49]	A. West, 2019[47]	C. Barthel, 2010[7]
Qubit Type	Transmons	Transmons	Spin Qubit	Spin Qubit	Spin Qubit
Readout Type	Dispersive	Dispersive	Dispersive	Dispersive	Reflectometry
Operating Frequency	4 - 8 GHz	4 - 8 GHz	4 - 8 GHz	4 - 8 GHz	<1 GHz
t_{read}	600 ns	80 ns	1 us	2.6ms	100ns
Readout BW	-	15 MHz	10 MHz	7 MHz	1.5 MHz
SNR $(S/N)^2$	11.5	3.5	6	<2	9
Fidelity	98.7%	97%	98%	74.5%	-
Par. Amplifier	Yes	Yes	No	No	No

Table 2.1: Comparison table of different RF readout setups for spin and transmon qubits.

2.4. Readout Survey

2.4.1. Readout electronics for Qubit Readout

Based on the previous discussion, it is clear that qubit readout requires an I/Q receiver to detect any amplitude/phase changes of the RF probe signal. A discrete HEMT/SiGe LNA operating at 4K is used to improve noise figure performance in most readout techniques. Typically, this LNA will have a noise figure of $\ll$1dB ($T_n \approx 5K$) and a gain of >40dB. Moreover, readout schemes such as for transmons require an additional parametric amplifier that possesses near quantum-limited noise figure ($T_{Quantum} = \hbar\omega/2k_b$). As we will see later in chapter 3, such type of performance in CMOS technology is very challenging.

2.4.2. State of the art solution

One of the most crucial figure-of-merit in the readout system is the fidelity of the system. The fidelity of a system describes the 'goodness' of the readout. Mathematically this is defined as equation 2.4 where F is the fidelity, P(1|0) is the probability of measuring the state 0 given a qubit state of 1, and P(0|1) is the probability of measuring the state 1 given a qubit state of 0. However, the system's fidelity depends on numerous parameters such as qubit decoherence, resonator performance, readout time, and SNR.

$$F = 1 - (P(1|0) + P(0|1)) \tag{2.4}$$

To get a better idea of the system specification, several other electrical parameters, such as operating frequency and baseband bandwidth is also noted in the table.

Based on the different readout setup shown in table 2.1, several key considerations for the receiver can be derived. This is listed below:

- For dispersive type readout, the operating receiver frequency should be somewhere between 4 - 8 GHz.
- Based on the references listed in table 2.1, the gain of the entire receiver chain is typically bigger than 100 dB.
- The readout bandwidth between different setups can vary but mostly depends on the resonator's bandwidth and the amount of dispersive shift. Based on the literature, the resonator's bandwidth lies between 2-5 MHz, and we should expect a dispersive frequency shift of at least half of that bandwidth. A reasonable and conservative assumption of the bandwidth of each qubit is around 10 MHz.
- The SNR of the system is also dependent on the readout time. From the table 2.1, we see that for an SNR of 10 with a readout time of $\approx 1\mu$s, the qubit readout fidelity is between 97%-98%. However, this is below the 99% fidelity threshold to allow for quantum error correction to be effective [17]. Hence we should expect SNR > 10 for higher fidelity readout.
- The 4K HEMT LNA [1] and the parametric amplifier mostly dictate the receivers' noise figure performance. Considering the HEMT LNA and the parametric amplifier is used in the receiver, a noise figure of typically $\ll$1 dB is observed for the whole readout chain [9, 25, 49]. The HEMT/SiGe amplifier's noise temperature is observed at $\approx$5K based on literature studies, while the parametric amplifier's target noise temperature is at $\approx$0.03K.

3

System Design

In this chapter, each component of the readout chain will be discussed. Prior to the design of each RX block for the proposed integrated receiver, a brief discussion on the behavior of the CMOS process in cryogenic temperatures will be presented. Furthermore, a general target specification will be derived in this chapter for the proposed integrated receiver based on the considerations discussed in the previous chapter.

Taking into account that the proposed integrated receiver has already been taped-out and designed before the start of the project, this chapter will only focus on analyzing the proposed receiver on a schematic level based on the already designed chip. The following chapter will highlight the design choices made in each RF block of the designed receiver with the simulation results shown afterward.

3.1. Behavior of CMOS process in Cryogenic Environment

Considering that the design needs to operate in 4K, CMOS's behavior in cryogenic temperatures needs to be understood and know how it will affect the design. Several works have been done to characterize the DC and dynamic behaviour of CMOS devices in cryogenic operation [11, 23, 30, 38]. This section will discuss the considerations needed to make a successful cryogenic electronic design.

3.1.1. DC Transistor Behaviour

The DC Performance of 0.16μm and 40nm CMOS process in 4K and RT is summarized in table 3.1 [23]. From the following work, several key design rules for cryogenic circuit implementations can be derived that will be used in the following chapter.

From the results shown in table 3.1, it is observed that the threshold voltage of the device increases by ≈100 mV regardless of the process node at 4K. Consequently, in terms of circuit design, this translates to lower available overhead voltage. This effect limits the circuit architecture choice for low supply process voltage requirements, such as the 40nm CMOS process. However, a possible solution, such as back-biasing in the SOI process, is also possible to tune V_t back to its original value.

The gm/Id from both processes are seen to increase in 4K at weak inversion regime. Hence, the design can be made more efficient with a given biasing current. Considering that power dissipation in the dilution refrigerator is limited, designers can take advantage of this property to make the circuit more efficient. As we will see later in section 3.2, we can take advantage of this behavior in the circuit design to achieve more gain with the drawback of sacrificing the linearity performance of the architecture.

Noise behavior in a CMOS process is also a primary point of interest. Research [36] has shown that the thermal noise does indeed goes down with temperature as expected. However, an increase in 1/f noise is also observed at cryogenic temperatures. With both phenomena considered, a high 1/f noise corner frequency is expected in cryogenic temperatures, influencing the receiver architecture's design choices.

3.1.2. Dynamic Transistor Behaviour

Figure 3.1 shows small-signal behaviour of a 32nm SOI CMOS process [11]. The work presented here can be useful regarding the design of an LNA for the qubit readout receiver. Some observation from

Technology		**0.16 μm**		**40 nm**	
Temperature		**4 K**	**300 K**	**4 K**	**300 K**
Device W/L	[$\mu m/\mu m$]	2.32 / 0.16		1.2 / 0.04	
V_T	[V]	0.55	0.40	0.50	0.38
SS	[mV/dec]	22.8	87.0	27.7	88.2
n	[-]	28.7	1.5	34.9	1.5
I_{on}	[A]	$2 \cdot 10^{-3}$	$1.5 \cdot 10^{-3}$	$6 \cdot 10^{-4}$	$5.3 \cdot 10^{-4}$
I_{off}	[A]	$< 3 \cdot 10^{-11}$	$< 1.6 \cdot 10^{-10}$	$< 1.5 \cdot 10^{-12}$	$< 1.4 \cdot 10^{-10}$
I_{on}/I_{off}	[A/A]	$> 6.7 \cdot 10^{7}$	$> 9.4 \cdot 10^{6}$	$> 4.0 \cdot 10^{8}$	$> 3.8 \cdot 10^{6}$
Gate delay	[ps]	30.60	38.30	-	-
λ	[V^{-1}]	3.3	0.6	4.0	1.3
		Weak Inversion			
g_m/I_D	[V^{-1}]	70	27	92	27
Intrinsic gain = $g_m/(\lambda I_D)$	[V/V]	21.2	45.0	23.0	20.8
		Strong Inversion (at $V_{ov} = 0.2$ V)			
g_m/I_D	[V^{-1}]	6	9	9	10
Intrinsic gain = $g_m/(\lambda I_D)$	[V/V]	1.8	15.0	2.2	7.7

Table 3.1: DC characterization of 0.16um and 40nm CMOS process in RT and 4K. Table replicated from Ref [23].

this data is as follows.

Figure 3.1a shows the minimum noise temperature (T_{min}) that can be achieved in the 32nm process. From the figure, one key observation that can be derived is that the T_{min} does not necessarily scale well with temperature. Despite the ≈50x reduction in temperature, only a ≈10x is observed for the T_{min}.

Figure 3.1b and figure Figure 3.1c shows the R_{opt} and X_{opt} noise parameter of the transistor respectively. It is observed that R_{opt} decreases with temperature while X_{opt} shown by Figure 3.1c is temperature independent. R_n in Figure 3.1d on the otherhand shows that it is lower with decreasing temperature. In terms of design, a lower R_n at cryogenic temperature indicates that the NF performance will be insensitive to Y_{gen} and Y_{opt} mismatch as shown from equation 3.1. Hence, it should be expected that a better low noise performance over a wide range of frequency in cryogenic temperature is observed when compared to its RT performance.

$$F = F_{min} + \frac{R_n}{G_g}\left[(G_{opt} - G_{gen})^2 + (B_{opt} - B_{gen})^2\right] \tag{3.1}$$

3.1.3. Passives Behaviour

The work regarding passive component behavior in CMOS process has been shown in Ref [38]. Some critical observations can be derived from this work and applied to cryogenic receiver design.

Figure 3.2a displays the trans-impedance behavior of a wideband matching network terminated by a 50Ω load. The figure shows an increase in bandwidth due to the overall decrease in capacitance and inductance values at cryogenic temperatures. This effect can also be seen to influence the shift in transimpedance transfer function towards a higher frequency. A higher peaking at the resonant frequency is also observed in the 4K transimpedance measurement. As explained by in Ref [38], this behavior naturally arises due to the decrease in metal resistance at cryogenic operations. Similar behavior can also be seen for the S_{21} response of a transformer matching network shown in Figure 3.2b. The result shows similar behavior regarding bandwidth extension at a higher frequency and lower insertion loss due to the lower metal resistance at cryogenic temperature.

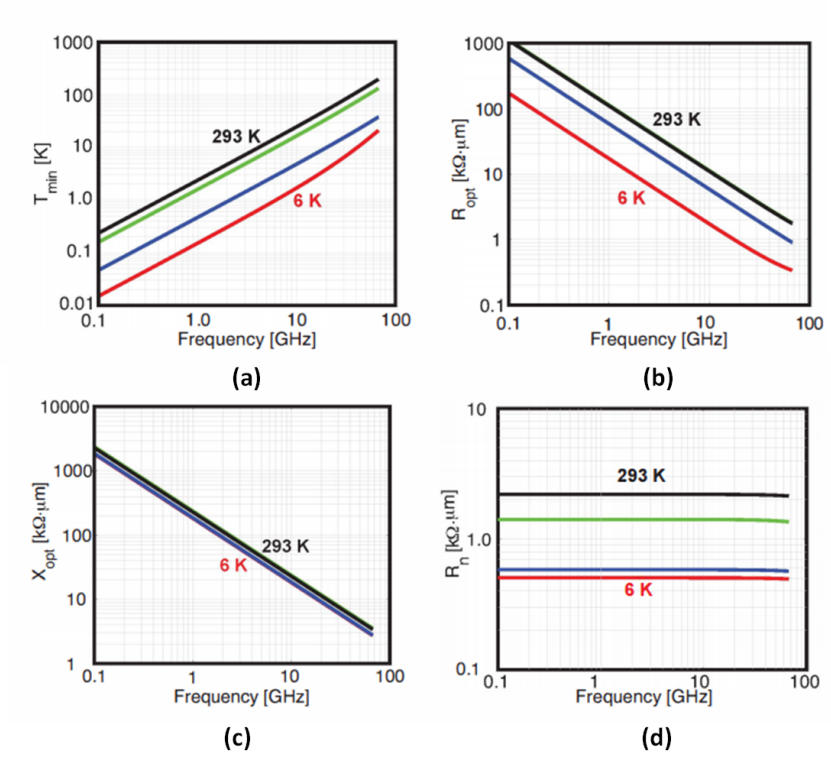


Figure 3.1: Small signal transistor behaviour for 32nm SOI process [11].

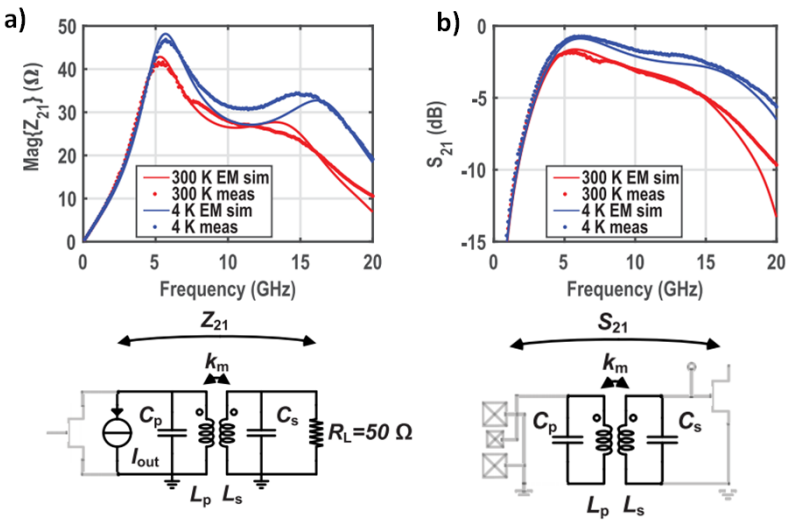


Figure 3.2: Behaviour of transformer matching network in RT and 4K temperature .Replicated from [38]

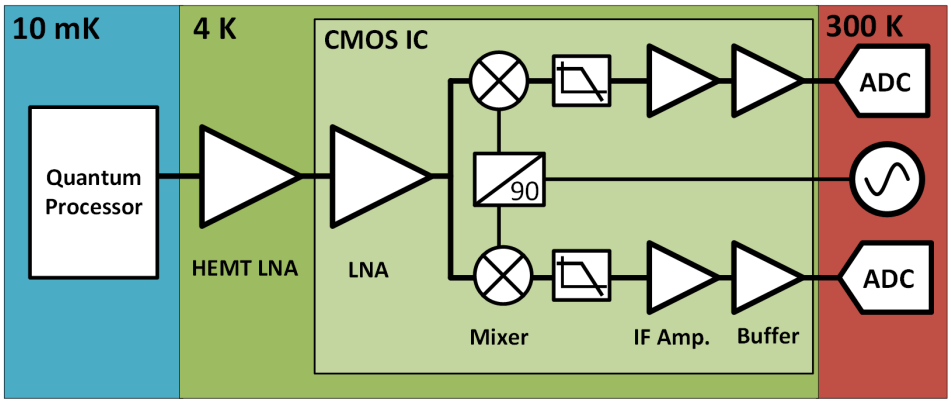


Figure 3.3: RX architecture used for dispersive qubit readout.

3.2. Receiver Architecture

As previously explained from chapter 2, the readout chain for RF qubit readout is similar to that of a standard RX telecommunication architecture. It is shown previously that spin or superconducting qubit readout systems are composed of a parametric amplifier, HEMT/SiGe LNA, mixers, and IF amplifiers. From the survey discussed in section 2.4, it can be concluded that the NF of the current state of the art readout systems is well below 1 dB. As it is seen later in this section, this performance is far below the CMOS process's capabilities. Hence, in general, HEMT/SiGe amplifiers are still needed to keep the NF of the system sufficiently low.

Considering the HEMT LNA's NF performance, this work aims instead to replace the room temperature rackmount setup used for qubit spin and superconducting qubit readout. We proposed to replace the RT components used in the setup of Figure 2.6 and 2.9, with an integrated chip operating at 4K. The proposed architecture is depicted in Figure 3.3.

From Figure 3.3, a CMOS LNA is still used as the first stage of the receiver. Since the noise from the first stage will be amplified significantly throughout the chain, the receiver's first stage must contribute as little noise as possible to make the noise contributions of consecutive stages negligible at the output. The mixer follows after the LNA with the purpose of frequency downconversion. The mixer will downconvert RF readout signals between 6-8 GHz to an IF frequency of 0-2 GHz in this architecture. An IF architecture opted mainly to avoid the high 1/f noise at cryogenic temperatures, which can degrade the SNR of the readout. Following the mixer, an IF amplifier is used for additional receiver gain. As mentioned previously, the whole receiver chain needs to amplify small readout signals (≈-130 dBm [42]) significantly to allow for detection by the ADCs at the output of the receiver. While achieving high gain in the LNA is possible, it is often not desirable as it puts a high linearity constraint for the mixer. Thus, an IF amplifier is used to give flexibility in the LNA and the mixer's design and achieve the receiver's required overall gain. Lastly, a buffer is designed at the receiver's end to match the system's characteristic impedance.

3.2.1. Noise Figure

Noise figure (NF) is one of the most critical parameters to consider in this design. As explained in section 2.4, it is desirable not to limit the qubit's readout signal intrinsic SNR. To investigate the required specification for the receiver, the NF of the whole qubit readout's chain shown in Figure 3.3 will be investigated.

From Figure 3.3, the architecture consists of multiple cascaded stages. The total noise factor of cascaded stages is determined by the Friis equation shown in equation 3.2. The NF value can be calculated through equation 3.3.

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_N - 1}{G_1 \ldots G_{N-1}} \tag{3.2}$$

$$NF_{sys} = 10 \log(F_{sys}) \tag{3.3}$$

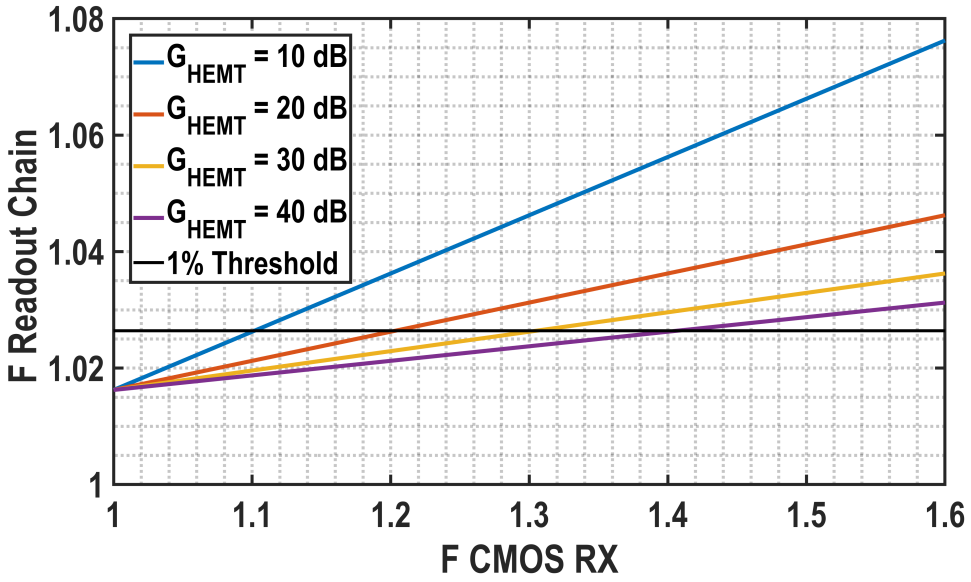


Figure 3.4: Noise factor plot of the readout chain versus different noise factor performance of the CMOS RX chip.

Equation 3.2 indicates that the noise contribution of each subsequent stage becomes less critical as the noise contribution of the previous stage will dominate the noise of the next stage provided that there is a significant gain. Hence, as mentioned before, the first stage must have the lowest noise factor as it limits the minimum NF that can be achieved in a cascaded system.

A typical noise temperature for a HEMT LNA is around 5K [1]. Equivalently, this is a noise factor of 1.0162. In this design, we wish to have the CMOS IC to only increase the readout chain's total noise factor by 1% relative to the HEMT LNA. A study on the effect of the CMOS RX's chip noise performance on the total noise factor of the readout chain is shown in Figure 3.4. Note that the total noise factor of the readout chain plotted in Figure 3.4 includes the HEMT LNA operating in front of the CMOS RX chip which is assumed to have a noise factor of 1.0162.

In the study done in Figure 3.4, the noise factor of the CMOS IC is varied. The corresponding effect on the readout chain's total noise factor based on the equation 3.2 is plotted. Different HEMT LNA gain is also plotted to see how it affects the CMOS RX chip's noise factor requirement. Moreover, the noise factor 1% threshold is also plotted in Figure 3.4. It is observed that a higher gain introduces a more relaxed noise factor requirement for the CMOS RX chip. With a typical gain of a HEMT LNA at around 40 dB [1], a noise factor of 1.407 (NF = 1.5 dB) is required from the RX chip in order for the RX chip only to alter the readout chain noise factor by 1%.

Based on the total readout chain's NF specification of 1.5 dB, the NF budget for each RX block can be decided. The NF target of each component is shown in table 3.2. The performance of the readout chain is observed to be strongly dependent on the performance of LNA. It is imperative to maximize the LNA gain in this design and minimize the LNA's NF as low as possible. With 30 dB gain at the first stage, the NF of the mixer, IF amplifier, and buffer can be relaxed.

From table 3.2, it is observed that the SSB NF is above the required specification stated previously. Assuming a white noise spectrum is present at the image band, the SSB NF's performance will be 3 dB higher than the DSB NF due to noise at the signal's image frequency translated to the same IF frequency of the desired signal. Hence, for an IF receiver, it is critical to suppress the image's noise as much as possible to reduce this effect.

3.2.2. Gain

The gain specification is derived based on the readout survey done in 2.4. Considering that the receiver is targetting readout application for spin and superconducting qubit, a total readout gain of ≈100 dB is expected. Moreover, it is also assumed that the HEMT amplifier is still used in the readout chain, as shown in Figure 3.3. Typically, the HEMT amplifier possesses a gain of 40 dB when operated in

	Gain [dB]	NF [dB]
LNA	30	1.4
Mixer	10	15
IF Amplifier	15	5
Buffer	5	5
$NF_{sys,DSB}$	1.5 dB	
$NF_{sys,SSB}$	4.5 dB	

Table 3.2: NF and gain budget for qubit readout chain. Note that the $NF_{sys,DSB}$ is calculated from equation 3.2 based on the given budget of each stage. $NF_{sys,SSB}$ is derived by adding 3 dB to its DSB value assuming that white noise is present at the image of the desired signal bandwidth.

cryogenic temperatures. With this consideration, it should be expected that the CMOS RX chip provides a gain of at least 60 dB to reach a total readout gain of 100 dB.

3.2.3. Linearity

The linearity specification for a readout system is expected to be more relaxed in comparison to the NF requirement. Unlike wireless receivers, the readout chain operates in a clean spectrum where no large blockers exist. Despite this, linearity is still relevant in readout systems, as demonstrated in this section. A minimum tolerable IIP3 and IIP2 specification needs to be quantified in order to achieve the desired SNDR to enable high fidelity readout.

Consider an FDMA system for qubit readout. In such a system, multiple qubits can be probed simultaneously, producing a multi-tone input. Nonlinearities from the readout components will introduce various intermodulation products given this multi-tone input. In the case of IM3 components, they can land in-band and have a great chance of occupying another qubit readout frequency. Additionally, IM2 components are also relevant for the IF architecture proposed here. Because of second-order nonlinearity, a low-frequency component can be generated in the system. This low-frequency component can exist at the IF frequency band of the receiver and possibly interfere with the downconverted readout signal, thus degrading the signal's quality.

The IIP3 specification is calculated below, where the calculation is made using several assumptions. In this section it is assumed that an SNR requirement of 15 dB is needed for the readout system. This specification is motivated based on the readout survey done in section 2.4, where it is observed that an SNR > 10 dB was needed to obtain fidelities of higher than 99%. Moreover, considering the qubit readout probe power of -130 dBm and a HEMT LNA gain of 40 dB, it is expected that a signal power of -90 dBm observed at the CMOS receiver's input.

Equation 3.4, refers to the desired IM3 component's power referred at the input of the CMOS receiver. Using the SNR requirement of 15 dB, the IM3 component will be 15 dB lower than the input power observed at the input of the CMOS chip in order for the IM3 component to be below the noise floor. Hence:

$$P_{IM3} < P_{in} - SNR = -90 \text{ dBm} - 15 \text{ dB} \tag{3.4}$$

$$P_{IM3} < -105 \text{ dBm} \tag{3.5}$$

Following the equation above, the IIP3 is derived in equation 3.6. Note that we assume all blocker components will have the same qubit readout power. Thus, we expect any blocker that exists in the system would have a power of -130 dBm.

$$IIP3 = \frac{3P_{Blocker} - P_{IM3}}{2} = \frac{3 \cdot (-90 \text{ dBm}) - (-105 \text{ dBm})}{2} = -82.5 \text{ dBm} \tag{3.6}$$

As shown by the result of equation 3.6, linearity specification is observe to be relatively low thus a non critical specification in comparison to the NF. Nevertheless, an IIP3 of -82.5 dBm should complied in order to keep the targeted SNDR of 15 dB.

The same analysis can be applied to the IM2 products. The IIP2 is derived similarly using the same

assumption. Doing the same calculation leads to the following requirement:

$$P_{IM2} < P_{in} - SNR = -90 \text{ dBm} - 15 \text{ dB} = -105 \text{ dBm} \tag{3.7}$$

$$IIP2 = 2P_{Blocker} - P_{IM2} = 2(-90 \text{ dBm}) - (-105 \text{ dBm}) = -75 \text{ dBm} \tag{3.8}$$

Similar to the IIP3 specification, the IIP2 requirement shown here does not pose a strict requirement for the readout chain considering the use of differential signaling for the receiver.

The linearity of the receiver becomes essential in the case of simultaneous qubit readout in an FDMA scheme. When simultaneous qubit readout signals are sent, their total peak power can saturate the receiver. Take, for example, a qubit readout receiver that can cover a 2 GHz bandwidth. Assume that each qubit occupies a 10 MHz channel. In such a system, the receiver would be able to cover readout of 200 qubits. If all the qubits are simultaneously read out by using a -90 dBm probe signal, we should expect that the IP1dB of the receiver to be:

$$IP1dB > -90 + 20\log(200) = -43.97 \text{ dBm} \tag{3.9}$$

3.2.4. Power

A power target of 1 mW/qubit is targeted for a scalable quantum computer [36]. With a target bandwidth of 2 GHz for the readout system, the receiver will cover 200 qubits assuming a 10 MHz bandwidth for each qubit. Equivalently, the receiver is expected to consume 200 mW of power. However, this value is very much dependent on the performance of the resonators used for readout. In this design, we took the liberty of choosing a maximum power dissipation of 100 mW for the readout chip. This is also well below the cooling power of the 4K stage of the dilution fridge (1 Watt). The power budget of each stage of the receiver is listed in table 3.3.

	Power [mW]
LNA	40
Mixer	30
IF Amplifier	15
Buffer	15

Table 3.3: Power budget of each stage of the receiver.

As seen from 3.3, most of the power budget is distributed to the LNA. It is clear from the previous section that the LNA's gain and NF are imperative towards achieving the desired specification. A big chunk of the power budget is also distributed to the mixer. As discussed in the next section, a relatively low NF is also needed from the mixer since it is the second stage of the CMOS receiver. In the following section, it can be seen that the power consumption of the mixer can be a trade-off with its NF performance.

3.2.5. Specification Summary

The specification of the receiver is listed in table 3.4 based on the previous discussion. Again, it should be noted that these specifications listed here are derived based on the assumption that a HEMT LNA is placed before the proposed CMOS IC in the readout chain.

	Gain	NF	IIP3	IIP2	IP1dB	Power
Specification	>60 dB	<1.5 dB	>-82.5 dBm	>-65 dBm	>-43.97 dBm	<100 mW

Table 3.4: Main specification of the CMOS IC receiver.

3.3. LNA

The LNA will be the first stage of the readout chip. While the HEMT LNA precedes the CMOS LNA, it is still imperative to design the LNA with a low NF to conserve the overall SNR of the readout chain for a high fidelity readout.

The choice for an LNA architecture is severely limited due to noise matching and impedance matching requirements. As it will be shown in this chapter, this requirement can not always be solved simultaneously. Often, additional components are required in order to optimize for both input and noise match conditions. Moreover, as shown from section 3.1, the headroom becomes an issue due to the increase of V_t at cryogenic temperatures. Such behavior also limits the choice of architecture.

In the following section, the CS amplifier will be analyzed. As we will see in this section, the CS architecture can provide a low NF and allows conjugate matching without the need for resistive components that can degrade the NF.

3.3.1. Analysis of a CS Stage Amplifier

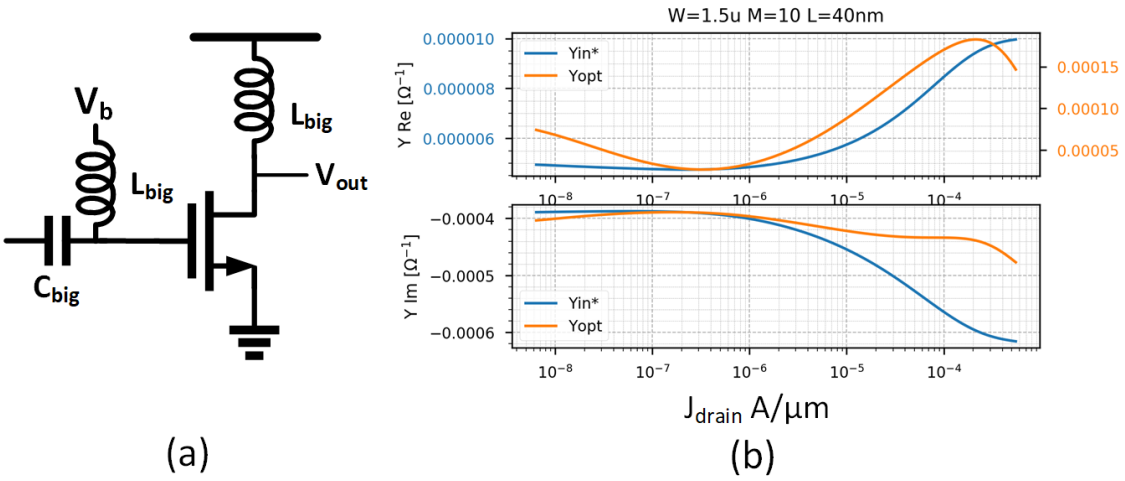


Figure 3.5: (a) A common source amplifier stage. (b) Plot of the required source admittance for optimum noise match and conjugate match.

A study of a common source amplifier is presented below. The circuit for a typical common source amplifier is depicted in Figure 3.5a. The following analysis will provide important insights that will be taken into account for the intended design.

Consider the noise match requirement of the circuit shown in Figure 3.5a. The NF of the circuit is dictated equation 3.10. Where, in equation 3.10, G represents the conductance, B the susceptance, and R_n the equivalent noise sensitivity. For the circuit to obtain minimum NF, the optimum noise admittance ($Y_{opt} = G_{opt} + jB_{opt}$) must be equal to the generator's admittance ($Y_g = G_g + jB_g$). In the case of a CMOS CS stage, Y_{opt} is expressed in equation 3.11 as derived by Lee [27].

$$F = F_{min} + \frac{R_n}{G_g}\left[(G_{opt} - G_g)^2 + (B_{opt} - B_g)^2\right] \tag{3.10}$$

$$Y_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\epsilon\delta}{\gamma}(1 - |c|^2)} - j\omega C_{gs}\left(1 + \alpha|c|\sqrt{\frac{\epsilon\delta}{\gamma}}\right) \tag{3.11}$$

Where $\alpha = gm/gm_{d0}$ (gm_{d0} drain-source conductance at zero V_{ds}), γ is the transistor excess noise factor, δ is the gate noise coefficient, c is the correlation factor between the drain noise source and the gate noise source, and $\epsilon = 1/(5gm_{d0})$ or equivalent gate resistor [27].

From equation 3.11, one can observe that the real part of the admittance will be zero in the case where the gate noise is neglected ($\epsilon = 0$, assuming no gate resistance). Under this condition, Y_{opt} will only yield an imaginary part implying the need for an inductive source behavior for optimum noise match. In contrast, for a conjugate match, the admittance presented to the input must be equal to the conjugate of the source admittance ($Y_{source} = Y_{in}^*$). The two criteria shown from the previous analysis imply that noise match and impedance match can not be done simultaneously in a simple CS stage amplifier.

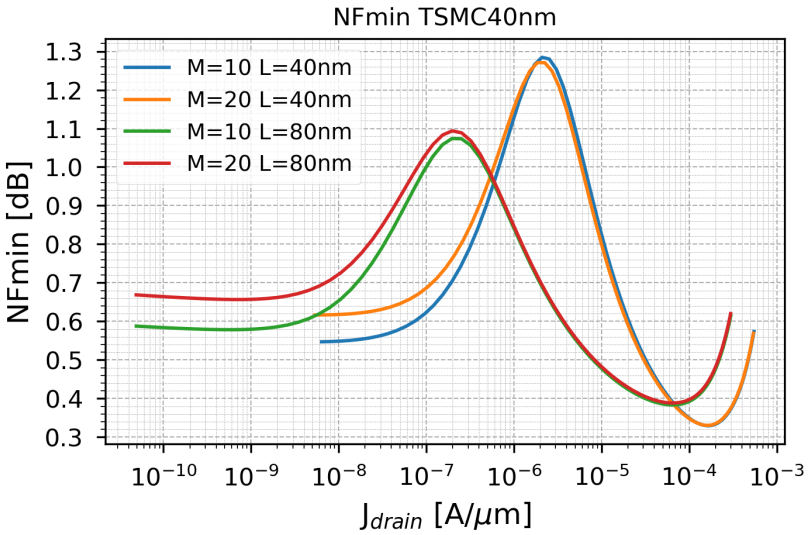


Figure 3.6: NF_{min} plot with respect to bias current density for different transistor sizes with unit width W=2μm and different multiplication factor and length.

The behavior of the previous analysis can also be verified in simulation. This behaviour is shown in Figure 3.5b. The figure shows Y_{opt} and Y_{in}^{*} of the CS amplifier with respect to the bias current. The figure reveals that the real part of the admittance for noise and conjugate match does not cross each other as they have different values. Moreover, $\mathbb{Re}(Y_{opt})$ is observed to have a low admittance requirement due to the small ϵ; the equivalent gate resistor (See equation 3.11). The reactance of Y_{opt} and Y_{in}^{*}, on the other hand, shows some similarities. This is expected since equation 3.11 shows that the imaginary part of Y_{opt} is in multiples of C_{gs}.

The NF_{min} of the CS amplifier will now be investigated. Analytically, the NF_{min} of the amplifier can be expressed as shown in equation 3.12 [27]. From the equation, smaller transistors can provide us a lower NF through higher ω_T [27]. This observation is also supported in the simulation shown in Figure 3.6.

The plot illustrated in Figure 3.6 shows how the NF_{min} varies with respect to the bias current density of the CS amplifier. The first observation that can be derived from the figure is that NF_{min} is independent of the transistor's width. For a given transistor width, the transistor must be biased according to the optimum current density that corresponds to the lowest NF_{min}. The second observation that can be extracted from the graph is that smaller channel length corresponds to lower NF_{min}, as expected. However, doing so would lead to a lower gain due to the transistor's lower output resistance (ro).

$$F_{CMOS,min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{3.12}$$

3.3.2. Design of the Readout LNA

A good starting point in the LNA design is the cascoded common source amplifier shown in Figure 3.7a. An additional cascode is added here compared to Figure 3.5 as it will maximize the single-stage gain of the LNA and increases the stability of the amplifier by making the single-stage amplifier unilateral.

The LNA design begins with characterizing the behavior of the circuit shown in Figure 3.7a. Bias sweep is initially done to find the optimum bias point for the transistor to obtain minimum NF and to observe the circuit's corresponding gain at that bias point. The simulation is run with the CS stage terminated with a 50 Ω load and a 50 Ω source resistance. The transistor's length was initially chosen to be 80nm for this design due to the higher achievable intrinsic gain in larger transistors.

Figure 3.7b plots the noise NF_{min} and the gain of the CS amplifier with respect to the device's current density. Figure 3.7b indicates that there is a trade-off in terms of gain and NF_{min}. It is observed that the maximum gain does not correspond to the lowest NF_{min}. However, considering the minimum variation

of NF_{min} at its lowest point, the amplifier can be biased at a slightly higher current density to achieve higher gain. A higher gain can also be achieved by sizing the transistor's width as it is proportional to the gm of the device (See Figure 3.7b). However, it should be noted that a bigger width will result in a higher biasing current to satisfy the low noise figure regime. The maximum width is set by the desired power budget and the f_t of the device, which needs to be higher than the system's frequency of operation.

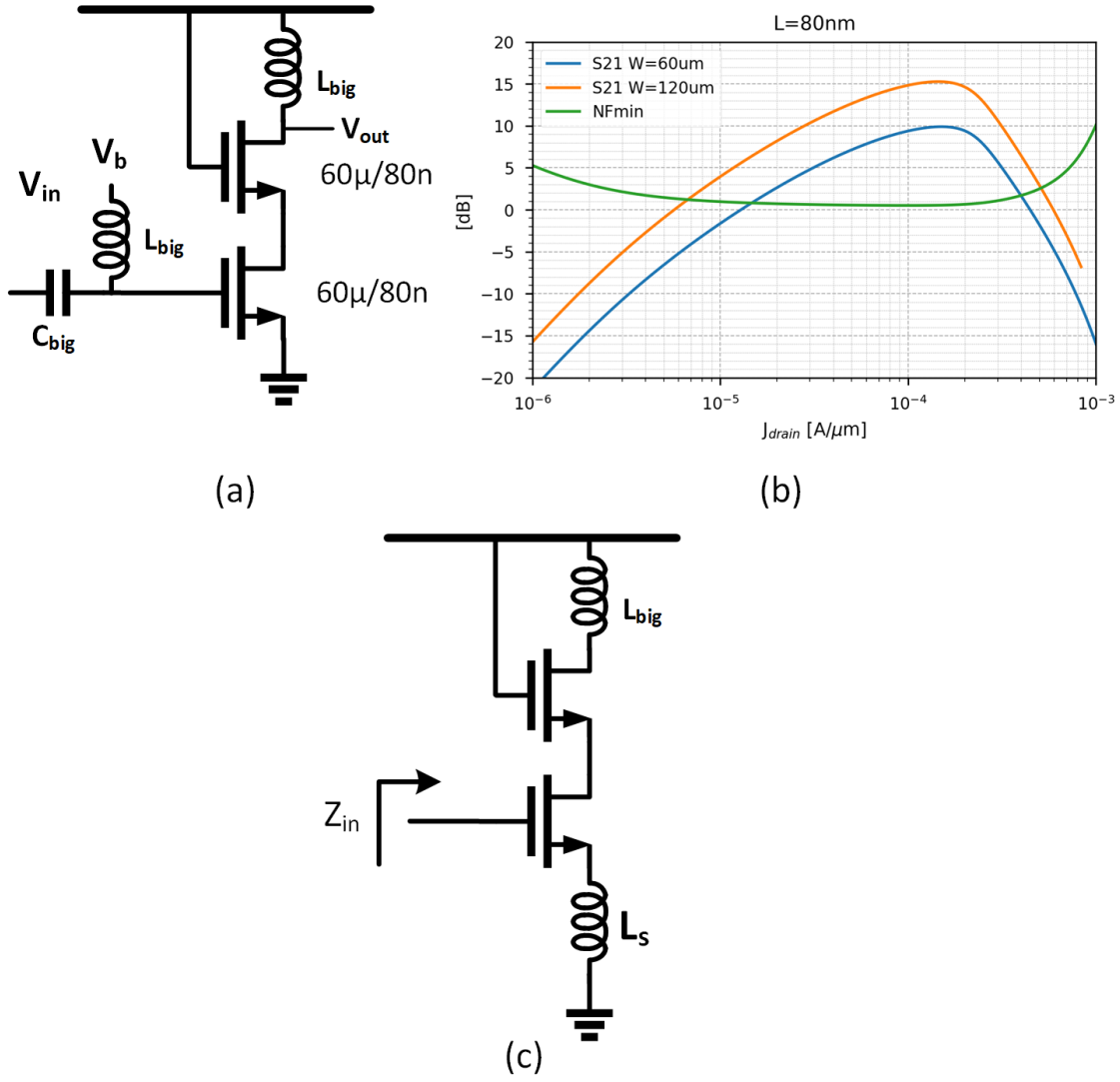


Figure 3.7: (a) Schematic of the cascode CS stage. (b) NF and S21 with respect to the drain current density for different transistor's width. (c) Schematic of the inductive degenerated CS LNA stage.

An inductor (L_s) at the CS input transistor source can be added to the circuit once the bias current for low noise operation is determined along with the resulting gain. The circuit is shown in Figure 3.7c. The value of the inductor depends on the required input impedance for matching purposes. Ignoring the output impedance (ro) of the transistor, the input impedance of the inductive degenerate cascode CS amplifier is defined in equation 3.13.

$$Z_{in} = \frac{gmL_s}{C_{gs1}} + j\left(\omega L_s - \frac{1}{\omega C_{gs1}}\right) \tag{3.13}$$

By setting the real part of equation 3.13 to the source impedance (50 Ω), a corresponding inductor value can be found. The capacitive 'residue' of the impedance shown in equation 3.13 can be cancelled

out by placing an inductor at the gate yielding a conjugate match. Note however that this condition only applies to only one frequency which is not desired in a qubit readout system with FDMA. To solve this issue, a transformer based matching network is used in this design to achieve wideband operation. This is analyzed in the next section.

Interstage Matching

A transformer-based matching network can be used at the CS stage input to provide wideband matching, as shown below. The idea behind using this matching network is to allow the transformer coupled resonators to resonate out the imaginary part of the Z_{in} (See equation 3.13) at two different frequencies. At this resonant frequency, only the real part of Z_{in} needs to be matched to the source impedance. Effectively, this can creates a broadband matching condition. The equivalent lumped model of the transformer matching network is shown in Figure 3.8.

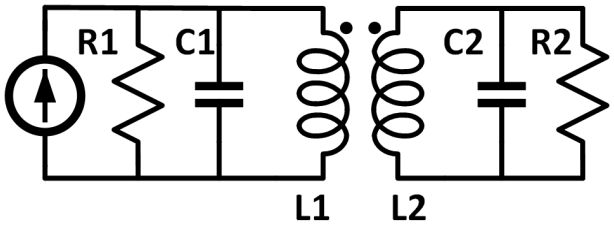


Figure 3.8: Lumped model equivalent of transformer-based matching. R_2 and C_2 can be thought of as the equivalent parallel load presented by the LNA or any other following stage.

Based on the lumped model shown in Figure 3.8, the trans-impedance transfer function can be calculated. The transfer function from the current source to V_2 can be derive by using the ABCD matrix of each component (See Appendix A). In this analysis, an equivalent T-model is considered to model the non-idealities of the transformer. Performing this analysis will yield a transfer function shown in equation 3.14.

$$\frac{V_2}{I_{in}} = \frac{kR_1R_2\sqrt{L_1L_2}s}{As^4 + Bs^3 + Cs^2 + Ds + E} \tag{3.14}$$

Where A,B,C,D, and E are the denominator's coefficient listed in table 3.5.

Coefficients	
A	$L_1L_2C_1C_2R_1R_2(1-k^2)$
B	$L_1L_2(C_1R_1 + C_2R_2)(1-k^2)$
C	$[(L_1C_1 + L_2C_2)R_1R_2 + L_1L_2(1-k^2)]$
D	$(L_2R_1 + L_1R_2)$
E	R_1R_2

Table 3.5

Under the condition that $L_1C_1 = L_2C_2$, the transfer function can be simplified in which an analytical solution for the resonant frequencies can be derived. The analysis will yield an equation for the resonant frequencies expressed in equation 3.15 and equation 3.16. At this resonant frequency, power matching is simply a problem of matching the real part of the CS stage's input impedance to the source's input resistance through the transformer. Moreover, the required coupling coefficient can be derived as equation 3.17.

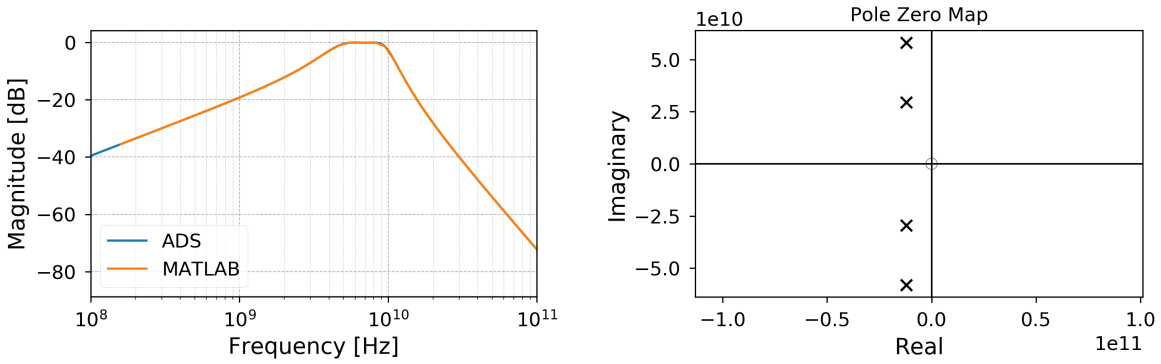


Figure 3.9: (a) S21 behaviour of both analytical and simulation. (b) Pole zero map of the transfer function. Shows a 2 two-pair conjugate poles along with a zero at DC in accordance to the transfer function derived in equation 3.14.

$$\omega_H = \frac{1}{\sqrt{L_1C_1(1-k)}} = \frac{1}{\sqrt{L_2C_2(1-k)}} \tag{3.15}$$

$$\omega_L = \frac{1}{\sqrt{L_1C_1(1+k)}} = \frac{1}{\sqrt{L_2C_2(1+k)}} \tag{3.16}$$

$$k = \frac{\omega_H^2 - \omega_L^2}{\omega_H^2 + \omega_L^2} \tag{3.17}$$

The analytical result derived previously is verified by ADS. This is shown in Figure 3.9a. An operating point of 6-8GHz is targeted and achieved as illustrated in the graph. The bandpass behaviour indicates a 60 dB/dec roll-off at higher frequency and a 20 dB/dec slope at lower frequencies. This behaviour is expected due to pole-zero cancellation at higher frequencies as shown from the pole-zero plot in Figure 3.9b.

To achieve conjugate matching between two arbitrary stages, the following generic procedure below can be followed. The procedure is used for the LNA input matching network and the inter-stage matching between the LNA and the mixer.

1. Measure the S-parameters of the two stages that needs to be matched to find the corresponding input/output impedance of the two stages.
2. Calculate the required transformer ratio n ($n^2 = R_1/R_2 = L_1/L_2$) based on the ratio of the input/output resistance of the stages.
3. Calculate the coupling coefficient of k based on the desired bandwidth. See equation 3.17.
4. Calculate the required inductance L based on the required n and equation 3.15 and 3.16.
5. If L is too big, add additional capacitors.

Full LNA Schematic

The full schematic of the LNA is shown in Figure 3.10. The LNA consists of two stages. The first stage is mainly responsible for achieving a low NF, while the second stage focuses on adding more gain to the LNA to obtain the 30 dB LNA gain requirement stated in the previous section.

At the first stage, a transformer input matching network is used for impedance matching purposes. The transformer is tuned to match the CS stage between 6-8 GHz. The transformer design was derived through the method shown in the previous section, where the equivalent input impedance of the degenerated CS stage was measured through an S-parameter measurement and matched to the source's impedance through sizing the tuned transformer appropriately. A large capacitance C_s is used at the input transistor's gate to provide a low impedance AC ground path at the gate. This circumvents the need for bond-wire inductance at the transistor's gate, which can add additional inductance to the transformer's secondary inductor.

Following the first stage, another transformer-based matching network is used to couple the first stage of the LNA to the second stage of the LNA. The transformer also acts as a balun to convert the single-ended signal into a differential signal. This is done to improve the signal's voltage swing and reduce the second-order nonlinearities of the receiver. The reduced second-order nonlinearities will be beneficial in the case of an IF receiver designed here as it can minimize the low-frequency IM2 component at the IF band which can degrade quality of the downconverted signal.

An additional differential amplifier is implemented after the first CS inductive degeneration stage. A pseudo-differential architecture is opted for this design to maximize the gain of the second stage given the limited headroom at cryogenic temperatures. The resistor at the input of the second stage is used to minimize the transformer ratio's sizing. The resistor is placed to provide a defined resistive load instead of the transistor's open load gate impedance. Additional capacitance at both sides of the transformers is used to balance both sides of the coupled resonators in order to have a flat frequency response, as discussed previously. Finally, a transformer-based matching network is used at the LNA's second stage output to match with the mixer's input.

The biasing of the first and second stage of the LNA is handled by a current mirror. The current mirror features a ≈150 MHz low pass filter at the gate transistor to filter high frequency noise.

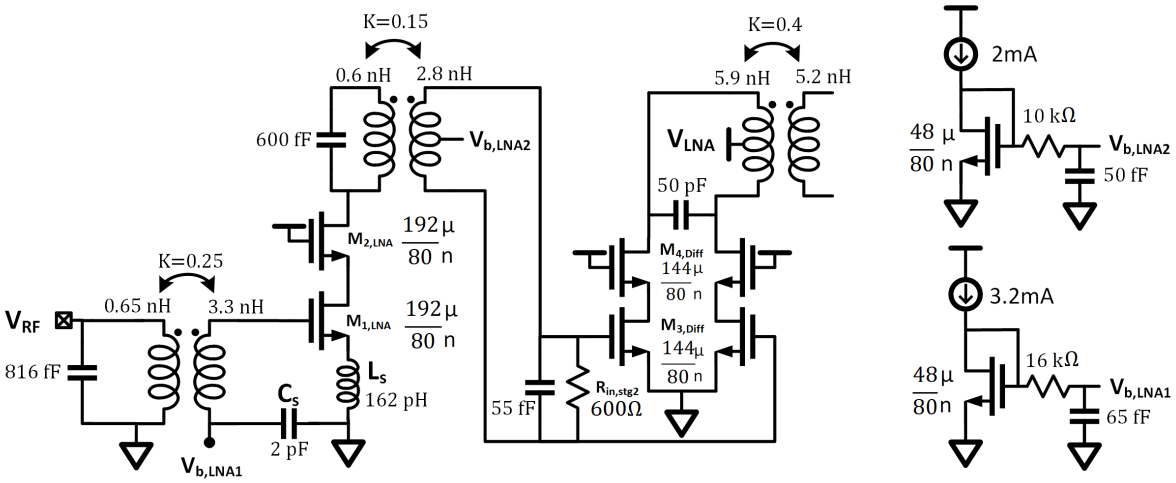


Figure 3.10: Schematic of the LNA used for the readout.

3.3.3. Simulation Result

The simulation result of the LNA will be presented in this section. It should be noted that the simulation is executed in RT due to the limitations of the models used to predict the behaviour of the transistors in 4K.

Figure 3.11a depicts the S11 behavior of the LNA. The simulation indicates that the S11 is below -15 dB throughout the desired bandwidth (6-8 GHz). Notice that the two resonant frequencies are visible at around 6 and 8 GHz. It can be concluded that a wideband matching condition is achieved by using the transformer matching network.

Figure 3.11b shows the voltage gain of the LNA. As seen from the graph, the LNA achieves approximately 30 dB of gain at the desired frequency range. The gain behavior, however, shows a non-flat frequency response. Such behavior has already been observed and analyzed from several other works [8, 29]. As discussed by Bhagavatula [8], this characteristic stems from the imbalance of $L_1C_1 = L_2C_2$ and the different Qs of the designed inductors for the transformers.

The NF of the LNA is shown in Figure 3.11c. A NF of 2.5 dB is obtained for the LNA. This value is approximately 1 dB higher than the targeted NF of the LNA. It is expected, however, that the overall NF of the LNA will improve at lower temperature as observed from [11]. Moreover, due to the improvement of the insertion loss of the input transformer matching network at 4K, one can obtain a lower minimum NF at cryogenic temperatures.

Lastly Figure 3.11 demonstrates the linearity performance of the LNA. The IP1dB is seen to be -24.32 dBm. Furthermore, the IIP3 and the IIP2 of the LNA is observed to be -16.07 dBm and +7.38 dBm respectively from simulation.

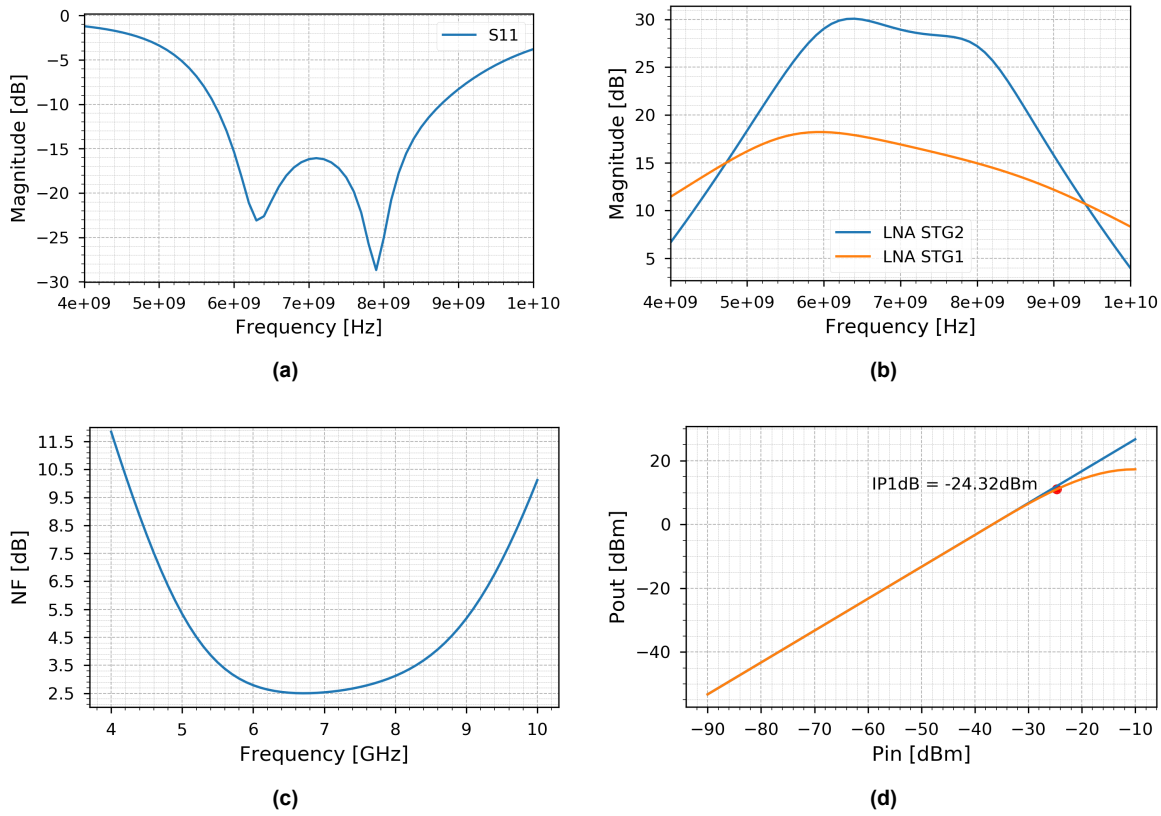


Figure 3.11: Simulation result of the LNA. Note that all simulations are run at room temperature. (a) S11 parameters of the LNA. (b) AC Gain of the first and the second stage of the amplifier. (c) NF of the system in RT. (d) Input P1dB point of the 2-stage LNA.

Noise Contribution

The total integrated noise observed at the output of the LNA is listed in Table 3.6. The resulting noise power was integrated from 6-8 GHz.

From Table 3.6, it is observed that the biggest contribution to the output noise of the LNA is the thermal noise of the resistor of the input-matching transformer itself. This is as expected, considering that the transformer is the first component in the chain; thus, its noise will get amplified the most. The next biggest contributing factor to the output noise is the M1 transistor's channel thermal noise. Again, this is to be expected as the noise of this transistor gets amplified significantly throughout the LNA stage. Note that the biasing circuit's noise contribution is non-existent in this list as it is filtered by the LPF.

From the observation listed above, it is clear that the transformer's noise will somewhat limit the performance of the LNA. Hence, there is a benefit in increasing the transformer's Q factor to further reduce the noise contribution from the transformer. However, this is sometimes not preferable as it will result in a non-flat frequency response of the transformer, as shown by [8].

	Integrated noise power between 6-8 GHz (V^2)	Percentage to Total noise
$R_{s,TF}$	4.19×10^{-7}	11.92%
$M_{1,LNA,id}$	2.16×10^{-7}	6.24%
$R_{in,stg2}$	1.12×10^{-7}	3.18%
$M_{2,LNA,id}$	0.75×10^{-7}	2.12%
$M_{1,LNA,gate}$	0.69×10^{-7}	1.96%
$M_{3,Diff,Pos}$	0.12×10^{-7}	0.72%
$M_{3,Diff,Min}$	0.12×10^{-7}	0.72%

Table 3.6: Noise power observed at the output of the two-stage LNA integrated over the 2 GHz bandwidth.

3.4. Mixer

3.4.1. Design and Consideration

Based on the requirement of the receiver, the mixer is required to contribute a positive gain on the system. Thus, an active mixer will be used for this purpose. The mixer, as stated before in section 3.2, will need to have a gain of 10 dB and a NF of 15 dB with a power consumption of 30 mW.

Considering the specification, a bleeding mixer architecture is opted for this design. The reasoning for the choice of this architecture is because a bleeding mixer can circumvent the limited gain given the limited headroom in a 1.1V V_{DD} system. By examining the maximum conversion gain of a standard double balance mixer (shown in equation 3.18 [41]), it is observed that the gain is supply voltage limited as expressed by $V_{R,max}$. The expression states that for a fixed current, higher gain requires larger R_D which will consume headroom. This is worsen at cryogenic temperature due to the increase of V_t. Furthermore, one can observe that the gain of the mixer directly trades off with the linearity of the system since the overdrive voltage of the input transistor is proportional to the IIP3 [41].

$$A_{v,max} = \frac{2}{\pi} gm R_{D,max} = \frac{4}{\pi} \frac{V_{R,max}}{V_{gt,gm}} = \frac{4}{\pi} \frac{V_{R,max}}{V_{gs,M1} - V_t} \tag{3.18}$$

$$R_{D,max} = \frac{V_{R,max}}{I_D} \tag{3.19}$$

$$V_{R,max} = V_{DD} - \left[V_{gt,gm} + \left(1 + \frac{\sqrt{2}}{2} \right) V_{gt,swt} \right] \tag{3.20}$$

The bleeding current alleviates the dependencies of the current and the voltage headroom issues that persist in a standard double balance mixer. By adding an external current source at the RF path to provide most of the bias current, the current flow through R_D can be reduced (See Figure 3.12). This allows designer to increase the load resistance and hence the gain of the mixer. For instance, provided that the bleeding current source supplies $|I_{bleed}|$=0.75$|I_{D,M1}|$, R_D will only carry 0.25$|I_{D,M1}|$. Hence, R_D can be effectively doubled to accommodate for the lower current through the branch. Furthermore, the reduction of the bias current through the switching transistor will reduce the overdrive voltage and thus leads to a more abrupt switching. Mathematically, the relationship of the new conversion gain can be expressed as shown in 3.21.

$$A_{v,max} = \frac{2}{\pi} \frac{gm_{M1}}{I_{D,M1}} R_D \frac{I_{bleed}}{\alpha} \tag{3.21}$$

Where $\alpha = I_{bleed}/I_{D,M1}$ with $\alpha < 1$.

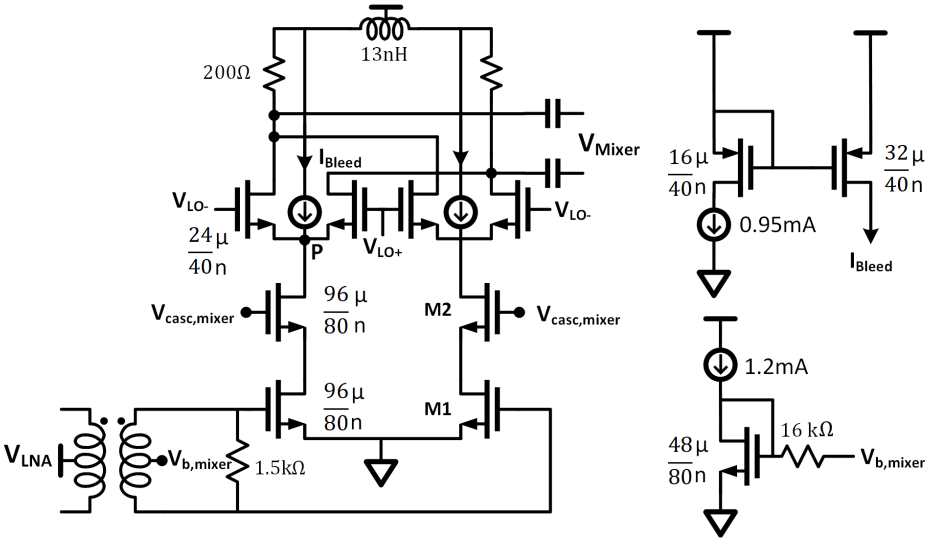


Figure 3.12: Schematic of the bleeding mixer used for the readout system. Current mirror biasing circuit is also shown for the input transistor and the bleeding current source. Note that $V_{casc,mixer}$ voltage bias is generated externally.

Additional cascode transistor M2 is also added in this design. While adding such transistor reduces the headroom of M1 and adds noise, the cascode transistor is necessary in order to isolate the LO signal from the RF port. The LO power used for the switches is in practice several magnitudes bigger than the input signal. When the large LO signal is coupled to the input, the input transcoductance device can saturate earlier then the intended design thereby reducing the linearity of the mixer.

Furthermore, the cascode also limits the modulation at the drain of the input transistor M1 due to the input signal itself. Without the use of the cascode, the drain voltage of M1 will swing proportionally to the input voltage [41] which can bring the transistor into the triode region. In contrast, when a cascode is added, the swing at the drain of M1 is suppressed by the intrinsic gain of the cascode and can be written as:

$$V_{drain,M1} \approx gm_{M1} V_{in} \frac{R_P}{gm_{M2} ro_{M2}} \tag{3.22}$$

Where R_P is the average resistance of the switches seen at the common source of node P (1/gm||1/gm) at equilibrium. In practice, $gm_{M1}R_P$ is approximately unity [41]. Hence, it can be observed that the cascode does indeed reduce the influence of the input signal at the drain of the input transistor.

In terms of noise design, the mixer can be tuned to its required noise performance by scaling the transistor and resistor used in the mixer. This method, however, trades-off with the power consumption of the circuit. In principle, by scaling all the transistor widths and current by a factor β and the load resistor by $1/\beta$, the input-referred voltage noise will fall by a factor of $\sqrt{\beta}$. This technique can also alleviate the large 1/f noise issue caused by the minimum size switching transistors. Because of scaling, the 1/f noise is also expected to decrease by $\sqrt{\beta}$. However, it should be noted that the transistors' parasitic capacitance will also scale with β. Hence, large transistor scaling can cause the LO driver of the switching pair to consume more power as the switching transistor presents a higher loading capacitance. Moreover, the higher parasitic capacitance of the switching transistor can lower the mixer's IF bandwidth due to the larger load capacitance manifested at the IF output.

In this design, an inductive load is added to the IF path. This is done to increase the overall gain-bandwidth product of the mixer. A higher mixer conversion gain can be obtained by resonating out the capacitive parasitics of the switching transistors.

3.4.2. Simulation Result

The simulation result of the mixer is shown in Figure 3.13. The behaviour of the conversion gain, NF, and the IP1dB is characterized as shown from the plot. Similar to the LNA, the mixer is simulated in room temperature.

Figure 3.13a depicts the conversion gain of the mixer for inputs between 6-8 GHz. The conversion gain is seen to vary by 2.5 dB across the 6-8 GHz bandwidth. This behaviour is as expected since it is caused by the pole at the output due to the stray capacitance of the switching transistor and the load capacitance of the following stage.

The NF of the mixer is shown in Figure 3.13b. An in-band NF of approximately 11 dB to 12.5 dB is observed from the circuit. Similar to the LNA, it is expected that this NF will decrease as the temperature decreases. To get a lower NF, power must be sacrificed as stated earlier by sizing all the transistor width by a factor β. However, doing so would effectively increase the parasitic capacitance at the mixer's output, consequently reducing the mixer's gain at higher frequencies.

Figure 3.13c shows the saturation point of the mixer. As indicated from the graph, the IP1dB of the mixer is listed as -17.14dBm. Based on the interpolation of IM products, the IIP3 and the IIP2 of the mixer is -10 dBm and +46.13 dBm respectively.

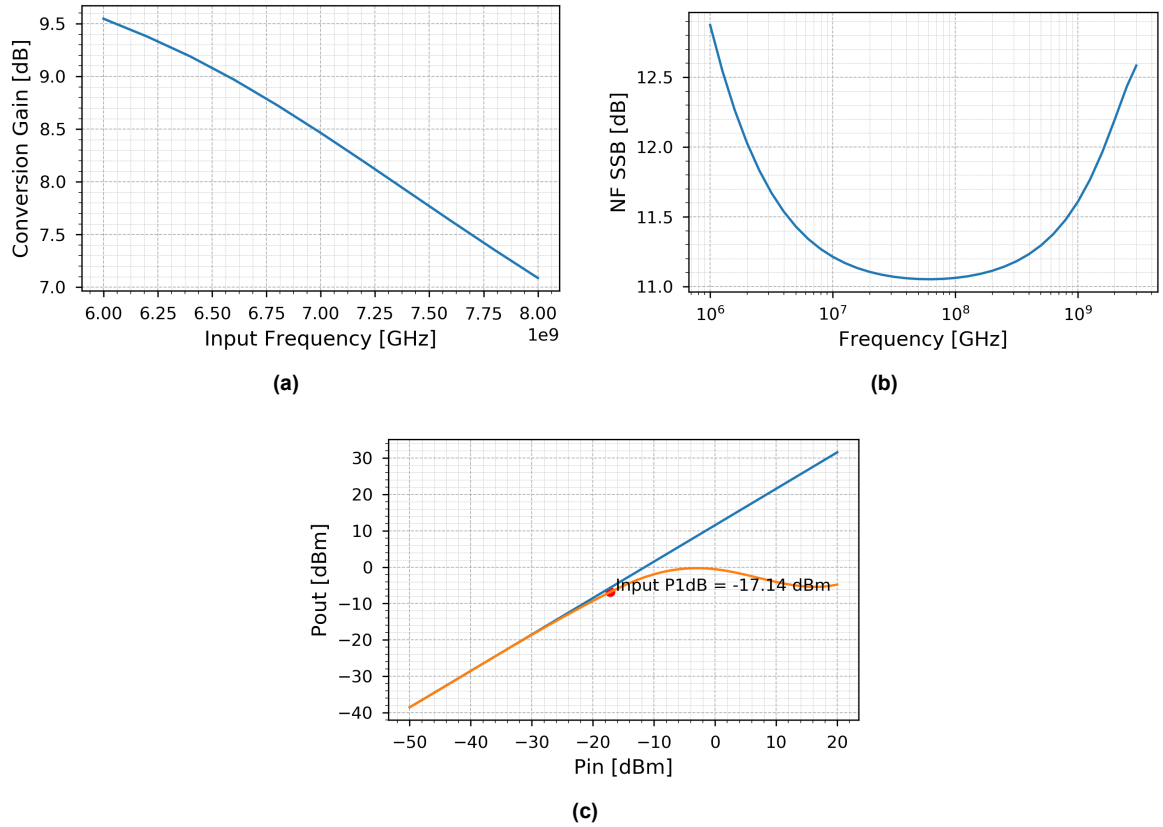


Figure 3.13: Simulation result of the Mixer. Note that all simulations are run at room temperature. (a) Conversion Gain with respect to the output frequency of the mixer. (b) SSB NF of the mixer with respect to the output frequency. (c) Input P1dB point of the mixer.

3.5. IF Amplifier and Buffer

3.5.1. Design and Consideration

As explained in previous section, an IF amplifier is necessary to ease the specification of the mixer and the LNA in terms of gain and linearity. A buffer is also designed at the output of the RX receiver chain in order to match the impedance of the receiver to the characteristic impedance of the system. In terms of architecture, the IF amplifier and the buffer uses the same circuit as shown in Figure 3.14.

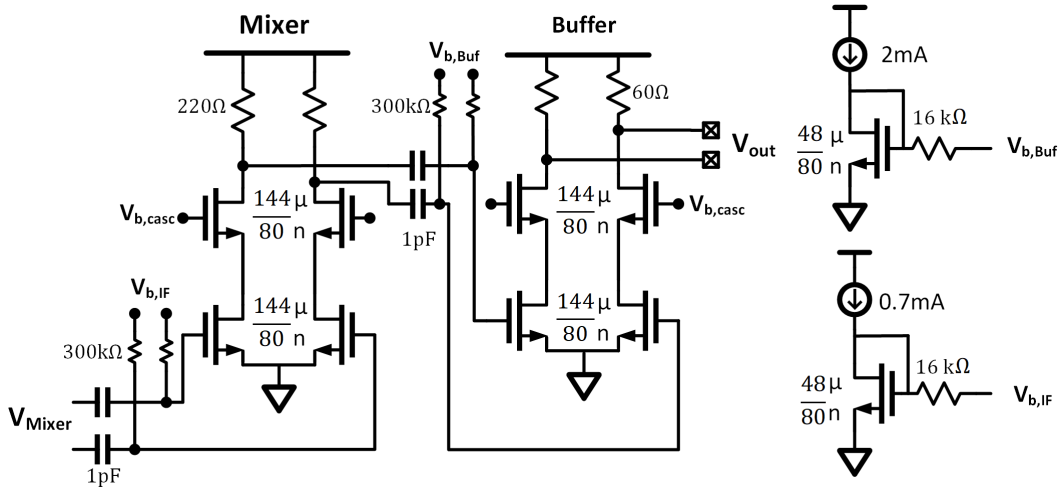


Figure 3.14: Schematic of the IF amplifier and the buffer. The two stages only differs from its biasing and load resistance. Biasing circuitry is also shown. The biasing voltage for the cascodes ($V_{b,casc}$) are generated externally by using a voltage source.

The IF amplifier is simply designed as a quasi-differential amplifier. The main reasoning for this design choice is gain and headroom. Since the circuit will operate in 4K, some flexibility is required in order to compensate for the increase of V_t. A tail current source and a cascode transistor above the input transistor will not fit the $1.1V_{DD}$ in this application. And considering that gain is important for this design, the overdrive budget is used for a cascode transistor instead. In the case of the IF amplifier, the gain is simply expressed in equation 3.23.

$$A_v = gm_1(gm_2ro_2ro_1||R_L) \tag{3.23}$$

$$Z_{out} \approx (gm_2ro_2ro_1||R_L) \tag{3.24}$$

Lastly, a buffer is required for the receiver for measuring purposes. In the design, the buffer is required to present 100Ω at the output for impedance matching purposes. This is achieved by biasing the amplifier accordingly. In essence, the output impedance of the amplifier is expressed by equation 3.24. Considering the large impedance presented by the cascode transistors, the output impedance Z_{out} is dictated by the value of R_L. Thus, to match the 100Ω load, R_L can be set to ≈50Ω. Notice that due to the low load resistance, more current is required in order for the buffer to produce the required gain set by the specification in section 3.2.

3.5.2. Simulation Result

The simulation result of both the IF amplifier and the buffer is shown in Figure 3.15 and Figure 3.16 respectively. The gain, NF, and linearity of each component are simulated and will be discussed below.

NF plot of the amplifier and the buffer is shown in Figure 3.15a and 3.16a respectively. The figure shows that both components do indeed come close to the target specification of 4 dB. A jump in NF close to DC is observed and expected as it is due to the transistor's 1/f noise. At cryogenic temperature, the 1/f corner frequency will increase, and thus careful IF frequency planning is required in order not to degrade the SNR of the readout signal.

The gain of both circuit is visualized in Figure 3.15b and 3.16b. The IF amplifier shows a voltage gain close to 14 dB with a cut-off at 4 GHz. On the other hand, the buffer shows a gain of around 5 dB

and a cut-off frequency at 12 GHz.

The linearity performance of the IF amplifier and the buffer stage is shown in Figure 3.15c and 3.16c. The IP1dB of the IF and the buffer is shown to be -12.85dBm and -2.2dBm respectively.

An essential parameter of the buffer is its output impedance. As seen from Figure 3.16d, the buffer does indeed provide a match to a 100Ω load. The S22 is approximately below -10dB throughout the 2.5 GHz bandwidth, indicating a good matched condition.

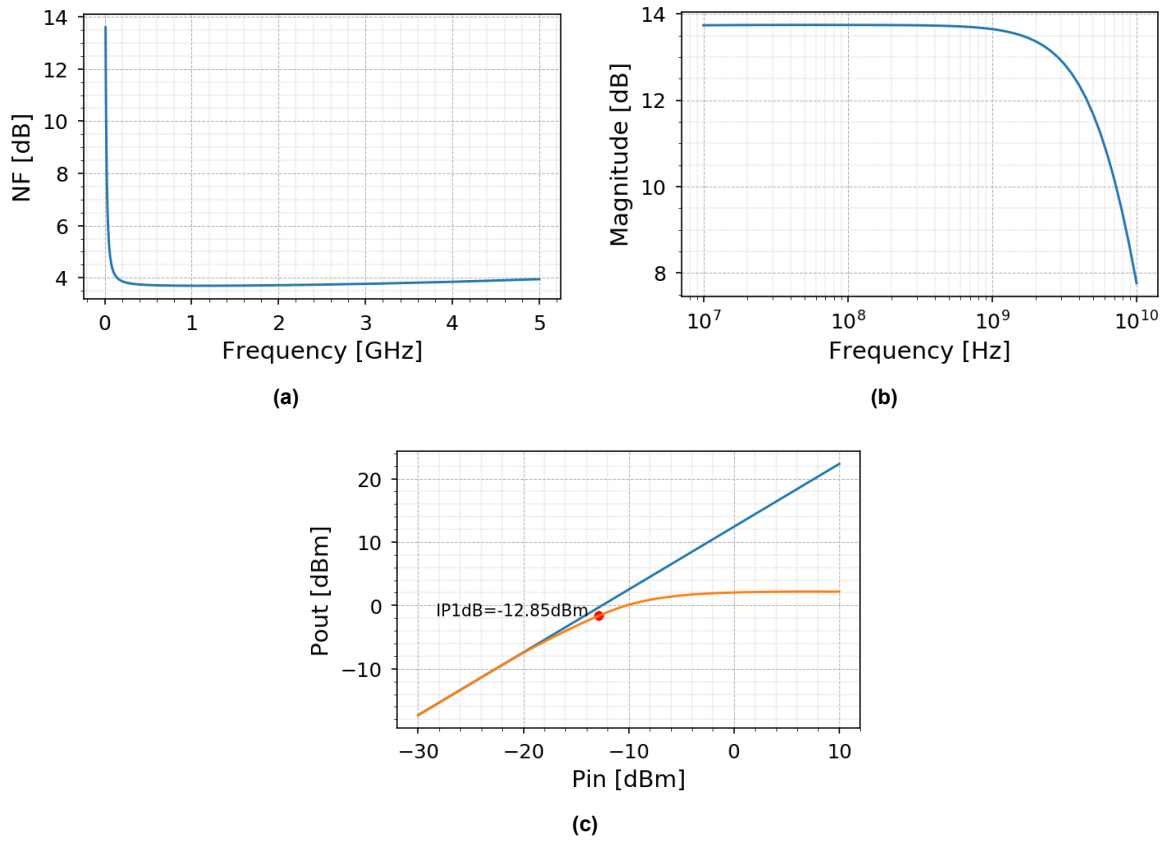


Figure 3.15: (a) NF of the IF amplifier. Shows a minimum NF throughout the 4 GHz frequency band (b) Frequency response of the IF amplifier. (c) Pin sweep of the IF amplifier.

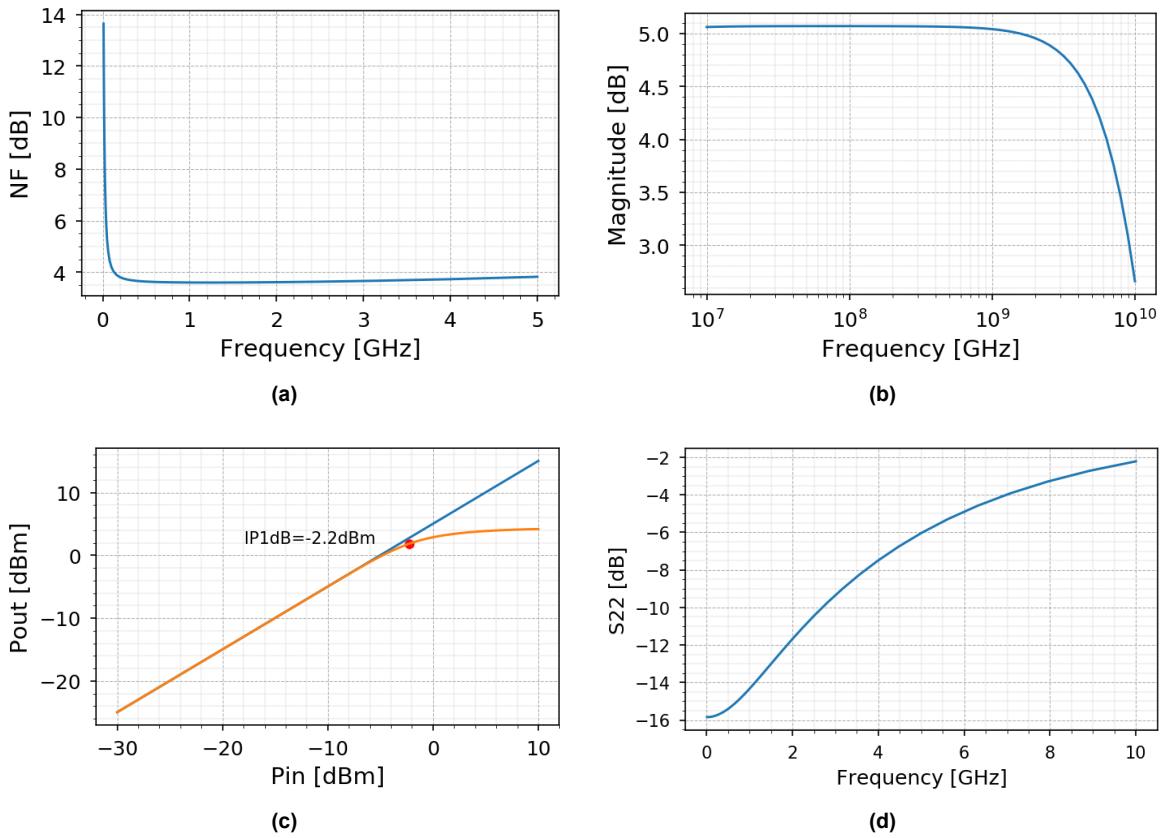


Figure 3.16: (a) NF profile of the buffer. Figure shows an NF of approximately 4dB across the desired bandwidth. (b) Frequency response of the buffer.(c) Pin sweep response of the buffer indicating its saturation point. (d) S22 response of the buffer indicating matched condition towards a 100Ω load.

3.6. LO Driver

3.6.1. Design and Consideration

The LO driver is also an important part of the receiver. It is responsible for driving the switch transistor of the mixer with sufficient voltage swing. Moreover, the LO driver is also responsible for matching its input with the system's characteristic impedance for maximum power transfer. This consideration is essential since if the LO driver's input is not matched to the source, the LO driver will experience a length-dependent power transfer. Thus, there is an uncertainty in the voltage swing applied to the mixer's switching transistor. The schematic of the I/Q LO driver used in this receiver is shown in Figure 3.17a. The I/Q LO signal is generated off-chip through a hybrid, as shown in Figure 3.17b.

In this design, the LO drivers' input matching performance is dictated by the 90°hybrid couplers. The principle of I/Q LO generation for this chip is similar to a balanced amplifier. As shown from Figure 3.17b, due to the hybrid coupler's phasing properties, the reflected waves from the LO driver's input get canceled out at the hybrid coupler's input port (V_{LO}). Provided that both I/Q LO drivers offer the same reflection coefficient, the input port will see no reflection. Thus, the source will effectively see a matched input when looking towards the LO driver.

Furthermore, the LO mixer also features a balun at the input to convert the single-ended I/Q LO signal into a differential signal to drive the double balance mixer's switches. A DC LO bias port is also shown in Figure 3.17b. This ensures proper DC biasing in the mixer's switches in order for them to turn on and off properly during operation. Similar to the IF amplifier and buffer seen in Figure 3.14, the cascode voltages used in this circuit are biased externally through a voltage source.

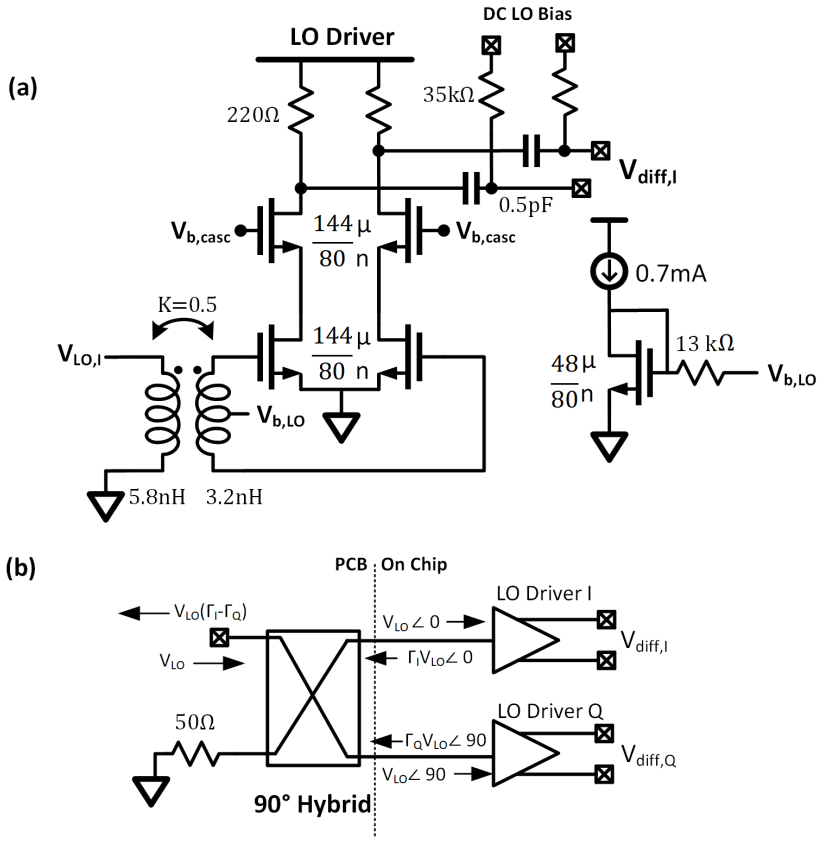


Figure 3.17: (a) On chip LO driver schematic. (b) Schematic of LO I/Q signal generation with on chip hybrid.

3.6.2. Simulation

The simulation results of the LO driver is shown in figure 3.17.

Figure 3.18a depicts the voltage gain of the LO driver. The simulation was executed with a 50fF load capacitor to emulate the mixer's switching transistor's impedance. A maximum gain of 15 dB was achieved at 7 GHz for both the I/Q LO drivers. The simulation also shows that the LO driver can provide a gain of >10 dB for a wide range of frequency, allowing flexibility in choosing the LO frequency.

Figure 3.18b shows the S11 performance of the LO driver. A good matching performance below -20 dB was achieved between 4-8 GHz. As mentioned before, this is achieved through the cancellation of both LO drivers' reflected waves when a hybrid coupler is used.

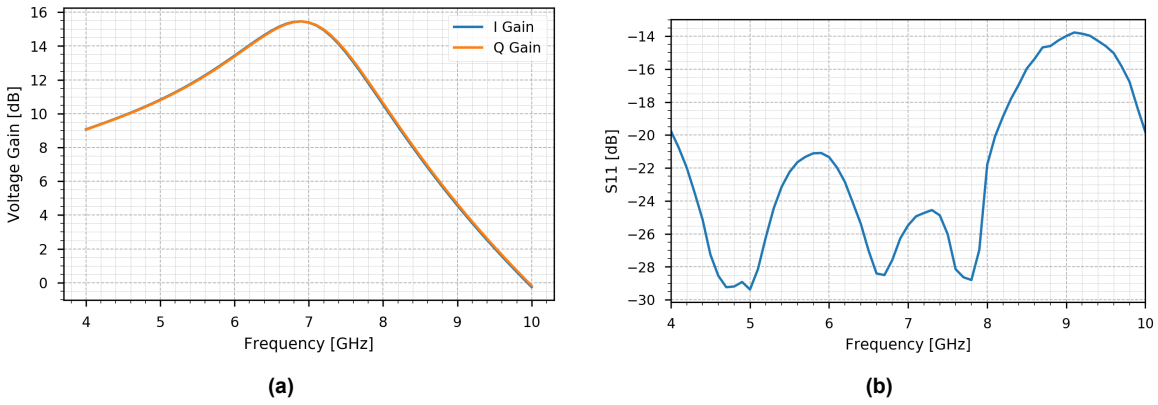


Figure 3.18: (a) LO driver voltage gain for I/Q path. (b) S11 of the LO driver seen from the input of the hybrid coupler.

3.7. RX Chain

The total performance of the receiver can now be examined. Each sub-blocks is integrated according to the architecture shown previously. As discussed throughout the chapter, the LNA and the mixer is coupled through a transformer. Whereas the mixers, IF amplifiers, and buffers are AC coupled. The full schematic of the RX chip is shown in Figure 3.19.

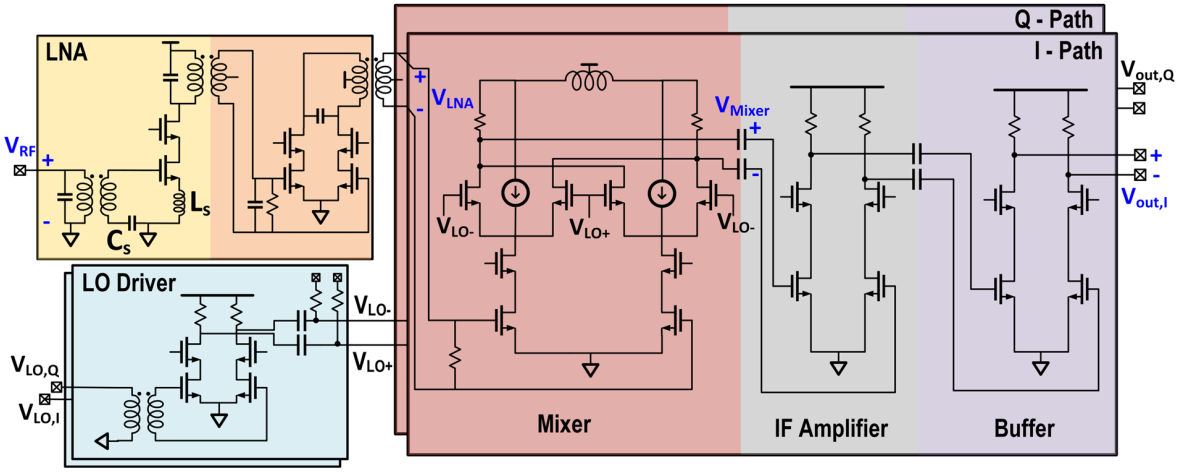


Figure 3.19: Full schematic of RX chain.

3.7.1. Simulation Result

The simulation results of the readout chain can be observed in Figure 3.20, Figure 3.21 , and Figure 3.22. Note that, similar to the other components shown here, the simulation is done in room temperature.

Figure 3.20 and Figure 3.21 depicts the receiver's voltage gain and NF behaviour. The simulation is obtained with a source impedance of 50 Ω and an output load of 100 Ω. The total voltage gain of the receiver is seen to be 58 dB while the NF performance of the receiver shows an SSB NF_{min} of 3.2 dB (DSB NF=2.5 dB) at RT with LO of 6 GHz. The performance shown here is close to the desired specification stated earlier. It should be expected that, by going to cryogenic temperature, an increase in gain and a decrease in NF will be observed.

Several observations can be deduced from Figure 3.21. First, it is observed that better NF performance can be obtained for f_{LO}<6 GHz. This phenomenon is due to the folding of the in-band noise of the receiver. Considering that the receiver is intended to receive signals from 6-8 GHz, an LO of 6.2 GHz would result in a folding of the inband image noise between 6-6.2 GHz to overlap with the noise in the 6.2-6.4 GHz frequency band. Furthermore, we can see an increase in NF at the lower frequencies (≈100 MHz). The biggest contribution of this effect comes from the performance of the LNA itself. As seen from Figure 3.11a, the LNA's NF performance starts to degrade at frequencies outside the 6-8 GHz bandwidth. Moreover, the 1/f noise from the baseband circuitry also contributes to the increase of NF at a lower frequency. This contribution, however, is smaller compared to the noise from the LNA.

The linearity performance of the receiver is illustrated in Figure 3.22. An IP1dB of -55.71 dBm is observed from the simulation. This value is ≈ 10 dB lower than the specification derived in section 3.2.3. However, this IP1dB value was deemed acceptable, considering that the receiver's main performance metric is the NF performance. Furthermore, an IIP3 of -46.6 dBm and an IIP2 of -23.28 dBm is obtained from the simulation. Comparing to the specifications derived in section 3.2.3, this performance is significantly higher than what is required for a qubit readout system.

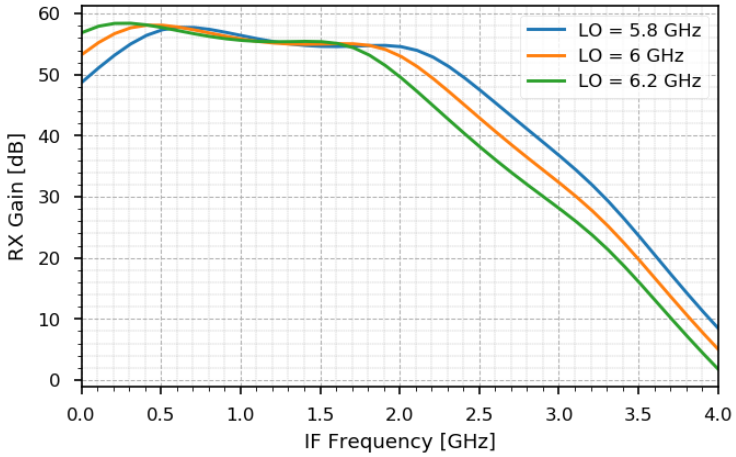


Figure 3.20: Gain and NF performance of the whole readout chain for different LO frequency.

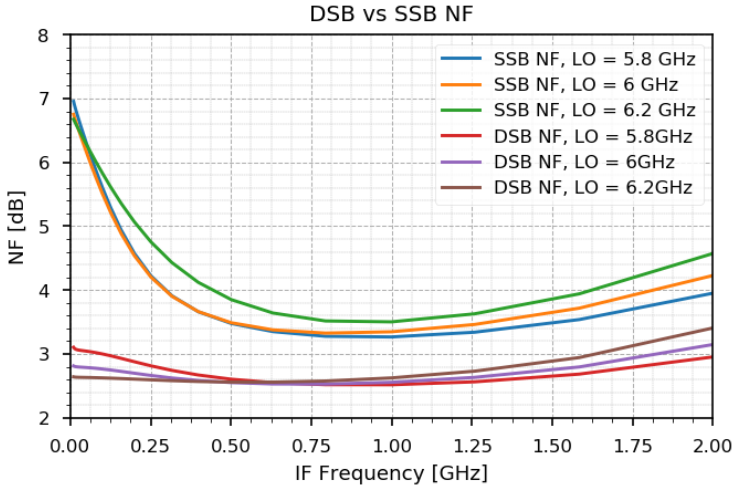


Figure 3.21: Gain and NF performance of the whole readout chain for different LO frequency.

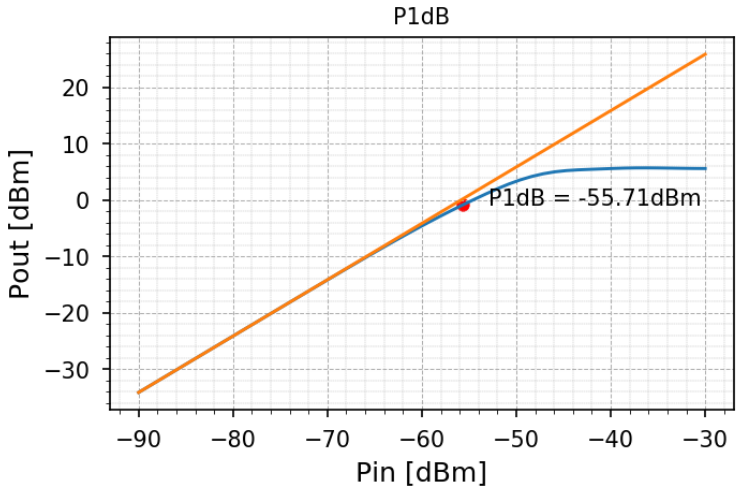


Figure 3.22: Linearity behaviour of the readout chain. An IP1dB of -55.71dBm can be observed based on the input power sweep.

3.8. FDMA Qubit Readout Architecture

As previously mentioned, the qubit readout architecture should support FDMA to enable scalability. This section is dedicated to the discussion of how this receiver can contribute towards this goal. The two possible methods of reading the state of the qubit with this receiver are discussed below.

A typical architecture of the qubit readout system is shown in Figure 3.23a. In this architecture, the receiver that has been designed in this work is responsible for the analog part of the readout chain. The analog receiver will downconvert readout signals from the 6-8 GHz frequency band to an IF frequency of 0-2 GHz.

Two different cases can be observed here. In the first case, the ADC will sample at 4 GSps. This implies that the ADC will be able to sample the full IF bandwidth of the receiver (see Figure 3.23b). In this architecture, any readout signal in the IF bandwidth can be digitized immediately. Following after the ADC, a digital quadrature mixer is employed to downconvert the I/Q IF signal to DC. The digital quadrature mixer is used to select which qubit is going to be readout. By tuning the digital mixer's LO frequency to the qubit's readout frequency, the readout probe signal can be directly converted to DC, where amplitude/phase variations can be detected from the I/Q information. Furthermore, a digital filter should also be employed after the digital mixer to further increase the SNR of the signal.

The biggest drawback in the realization shown above is the higher power consumption of the system. Running the ADC at 4 GSps at cryogenic temperature can be too demanding in terms of power due to the dilution refrigerator's limited power dissipation.

The second case is observed when an ADC has a lower sampling rate than the receiver's bandwidth. If it assumed that a 1 GSps ADC is used, the sub-sampling technique could downconvert the readout signal to the first Nyquist zone. Considering the sampling frequency of 1GSps, the 2 GHz IF bandwidth is divided into 500 MHz wide channels (see Figure 3.23c). In this scheme, the system needs to keep track on which Nyquist zone the probe signal lies. This is done to account for the mirroring effect of the sub-sampling technique. Following after the ADC, a similar digital quadrature mixer shown in the first example can downconvert the selected qubit for state detection.

A possible advantage in terms of power is obtained by realizing the second implementation with the 1 GSps ADC. However, the biggest problem with the second scheme proposed above is that the noise in other Nyquist zones will fold to the first Nyquist zone, which effectively degrades the overall NF performance.

Frequency generation is also an important aspect in qubit readout. Because of the short burst of readout signals ($\approx 1\mu$s) used, it is possible that the side lobes of the readout signal's spectrum will overlap with the neighbouring qubit's readout frequency. Consequently, this can influence the operation of the neighbouring qubit. For quantum processor with high qubit density, it is likely that some sort of envelope shaping is needed.

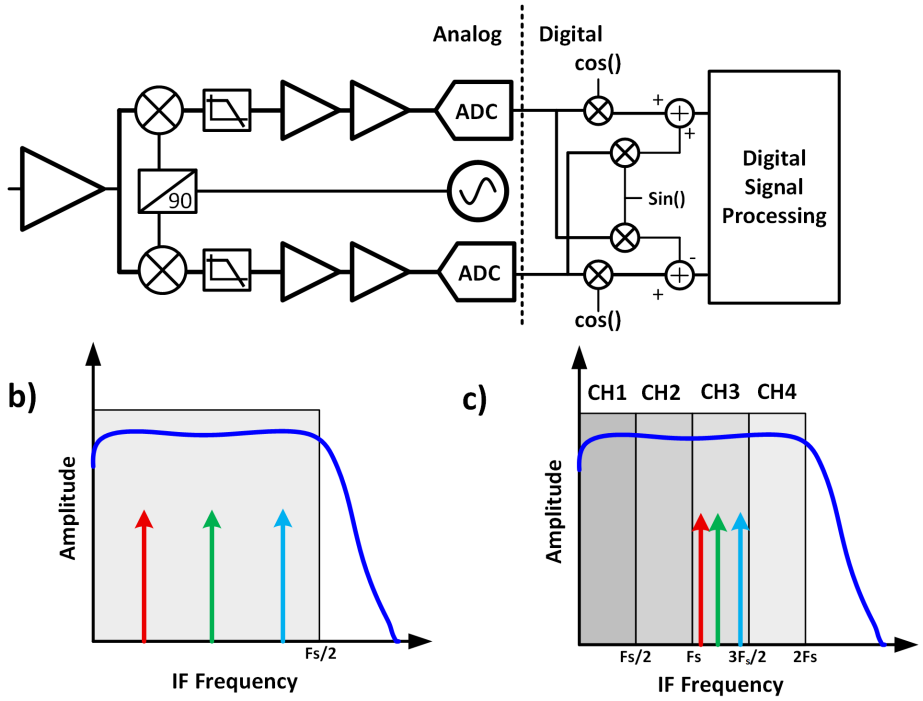


Figure 3.23: (a) A typical receiver architecture for qubit readout with its analog and digital part. (b) and (c) shows the frequency spectrum of the receiver before digitizing with different ADC sampling frequency performance.

4

Measurement

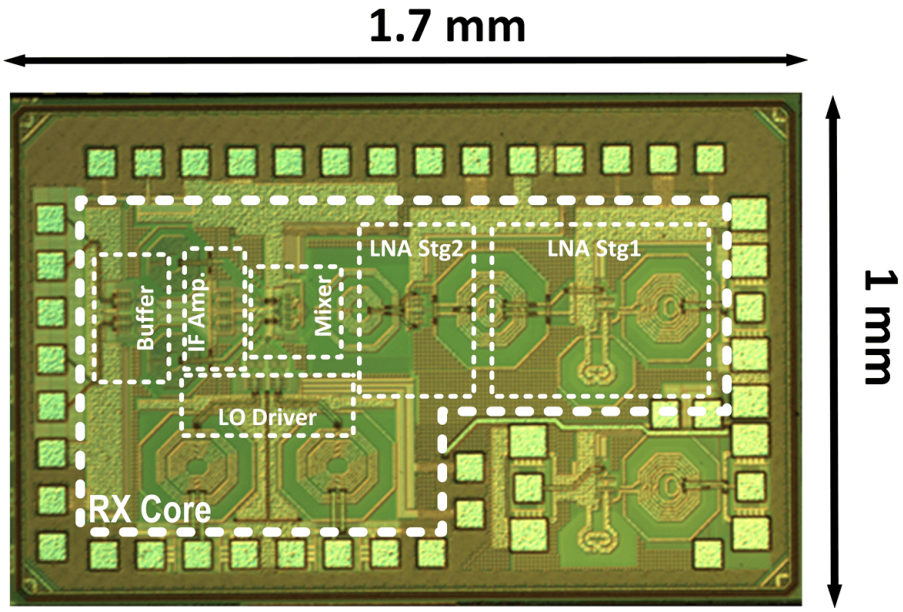


Figure 4.1: Chip Micrograph of the qubit readout receiver.

This chapter will focus on the measurement results obtained from the RX chip. The chapter will cover the measurement methodology and analyze the results obtained from the dipstick and probe station measurement setup. Moreover, the chapter will demonstrate qubit readout measurements that have been done in the dilution fridge with the chip operating at 4K.

The chip has been taped out in the 40nm bulk CMOS process. The chip micrograph is depicted in Figure 4.1. The stages of the RX chain are labeled accordingly in the chip micrograph. It should be noted again that the CMOS receiver presented in this work has been taped-out prior to the start of the thesis project. The schematic behavior of the chip shown in the previous chapter is based on the already taped-out chip.

4.1. Dip-stick Measurement

In this section, the noise figure measurement will be presented. The measurement will be executed by using a dipstick to ensure that the measurement is done at 4K ambient temperature with sufficient cooling power.

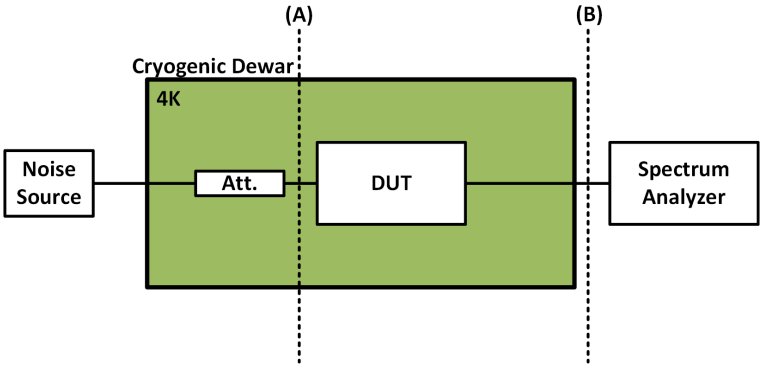


Figure 4.2: Noise figure measurement setup with cold attenuator.

4.1.1. Hot and Cold Y-Factor Measurement

Before going into the measurement results, this section will first discuss into the theory used for noise figure (noise temperature) measurements in cryogenic temperatures.

Noise figure measurements are often done using the Y-factor method. This method relies on the application of a wideband noise source at the input of the device under test (DUT). The Y-factor is obtained from the ratio of the noise power at the DUT's output under 'hot' (N_{hot}) and 'cold' (N_{cold}) noise source excitation (see equation 4.1). By using the Y-factor and equation 4.2, the noise temperature of the DUT can be calculated [4].

$$Y = \frac{N_{hot}}{N_{cold}} \tag{4.1}$$

$$T_{DUT} = \frac{T_{hot} - YT_{cold}}{Y - 1} \tag{4.2}$$

T_{hot} and T_{cold} in this equation are defined as the noise source's noise temperatures at its on and off state, respectively. The value of T_{hot} is dependent on the excess noise ratio (ENR) parameter of the noise source, which is defined as:

$$ENR_{dB} = 10\log\left(\frac{T_{hot} - T_{cold}}{T_0}\right) \tag{4.3}$$

Where T_0 is defined as the reference temperature of the calibrated noise source (which in most cases is usually at 290K).

For RT applications, the Y-factor measurement method can be very effective. There are, however, some shortcomings when applying such a method to cryogenic measurements. Take, for an example, the setup shown in Figure 4.2. In the case of cryogenic measurements, the device is enclosed in a cryogenic chamber. Any signals used for measurements will need to go through a lossy line towards the DUT. The noise temperature applied at reference plane (A) without the attenuator can become uncertain due to the lossy cables, making noise figure measurement inaccurate. Moreover, the noise source impedance for on and off states is significantly different. This can affect the system's overall noise figure since the noise performance depends on the difference between the generator's impedance and the optimum noise impedance. To overcome this problem, a cold attenuator can be introduced at the input of the DUT [15].

In the case of noise figure cryogenic measurements with a cold attenuator, equation 4.2 can not be used. An alteration needs to be done for equation 4.2 to account for the attenuator added. The resulting equation for noise temperature measurement in cryogenic temperature is shown equation 4.4. The full derivation of this equation is shown in the appendix B.

$$T_{DUT} = \frac{1}{L}\frac{T_h - YT_c}{Y - 1} - \left(\frac{L - 1}{L}\right)T_{cryo} \tag{4.4}$$

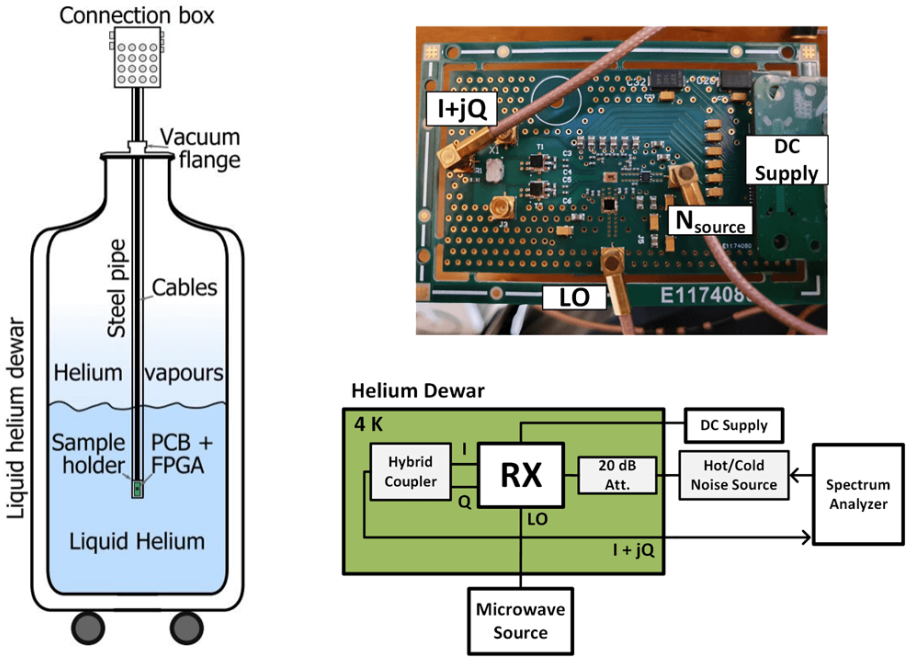


Figure 4.3: Dipstick measurement setup to measure the noise figure of the RX chip.

Where T_{cryo} is the ambient temperature of the attenuator at cryogenic temperature, and L is the total attenuation preceding the DUT at 4K. In this thesis, the following method is used to measure the noise performance of the RX chip. From the equations above, T_{DUT} can be calculated. Conversion to noise figure value referenced at room temperature can be done through the following equation:

$$NF_{dB} = 10\log\left(\frac{T_{DUT}}{T_0} + 1\right)$$

4.1.2. Measurement Setup

The measurement setup for the noise figure measurement is shown in Figure 4.3. The spectrum analyzer controls a noise source at RT. A 20dB attenuator (HMC658) at 4K is placed between the RX chip and the noise source. As shown from Figure 4.3, the RX chip will be submerged in liquid helium inside the Dewar. Furthermore, the differential output of the chip is converted back to single-ended output due to the lack of RF lines in the measurement setup and to avoid any significant gain/phase mismatch of the quadratures. A 90-degree hybrid coupler (X3C07F1-03S) is also used in the PCB at the I/Q output to combine both branches and to calculate the receiver's double-sideband noise figure. In principle, the hybrid coupler effectively combines the two I/Q signals and noise to emulate downconversion to DC. This is done considering that direct downconversion is not possible in the design due to the AC coupling used in the IF stages. Moreover, directly combining both I/Q output prevents I/Q mismatches from influencing the NF measurements. It should be noted that the hybrid coupler used in the PCB is specified for 0.6 - 0.9 GHz.

A noise source (FMNS1006) with an ENR of 15 dB is used for this measurement. An LO of 5.9 GHz is generated at room temperature from a microwave source. The output is captured by a spectrum analyzer to obtain the hot and cold noise response, which consequently gives the Y-factor of the DUT. Equation 4.4 are then used to calculate the noise temperature (and effectively noise figure) of the system. A temperature sensor (DT-670) is placed on the PCB close to the chip to measure T_{cryo} of equation 4.4.

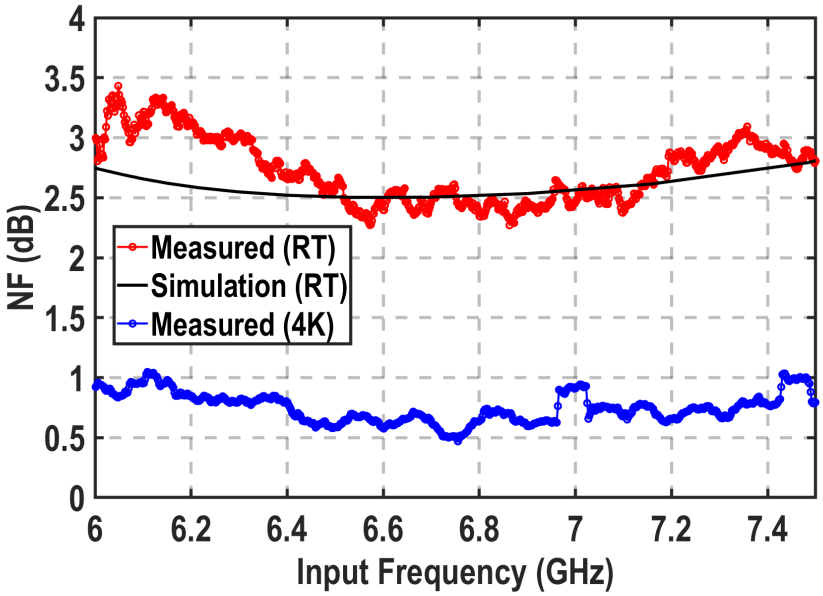


Figure 4.4: DSB Noise figure measurement of the RX chip at RT and 4K. Simulations are also plotted for comparison.

4.1.3. Result

The result is shown in Figure 4.4. Considering that the hybrid is specified for ≈0.6-0.9 GHz range, the DSB result shown in Figure 4.4 is only accurate for ≈6.5-6.8 GHz considering the 5.9 GHz LO. The choice of the frequency range is based on the expected minimum noise figure from the simulations.

In the case of RT measurement, a noise figure of 2.5 dB is obtained. An agreeable result in comparison to the simulations. At higher/lower frequency values, a higher noise figure is observed, which is contributed by two factors. The increases in the noise figure itself and the hybrid coupler's bandwidth capability which introduce incorrect phase combinations between the I/Q path.

A noise figure of ≈0.6 dB is observed at 4K. The 4K measurement result shows that the noise figure is ≈4x lower than the RT value. This reduction is comparably small relative to the reduction of temperature from RT to 4K (≈70x temperature reduction). It should be noted that just like the behavior discussed in section 3.1.2, the noise performance is seen to saturate. A possible explanation of this is the now dominant shot noise of the transistor at 4K, which is temperature independent. Another effect that comes into play in this measurement is the self-heating effect of the transistor's junction temperature. The self-heating effect can effectively increase the transistors' operating temperature and make it seem that the transistors are operating at a higher temperature. Hence, knowing this temperature is critical, especially for the transistors of the LNA. Unfortunately, no temperature sensors were designed in the proximity of the LNA of the RX chip. Hence, such a phenomenon can not be verified.

The noise figure's performance at 4K is slightly flatter compared to the noise figure performance at RT. This can be explained as the reduction of one of the noise parameters, namely the R_n. As mentioned in section 3.1.2, lower R_n corresponds to lower sensitivity variation in noise figure due to generator/input impedance mismatch. Hence, a more wideband low noise performance is observed at cryogenic temperature.

4.1.4. Power

The power consumption of the receiver is measured in the dipstick setup to ensure a 4K ambient temperature operation. The chip is biased with the same current biasing value for both RT and 4K case. In the case of RT, the receiver consumes a total power of 70 mW. Whereas at 4K, the receiver consumes a total power of 66 mW. Both cases satisfies the specification stated in the previous section, where a power consumption of <100 mW is desired.

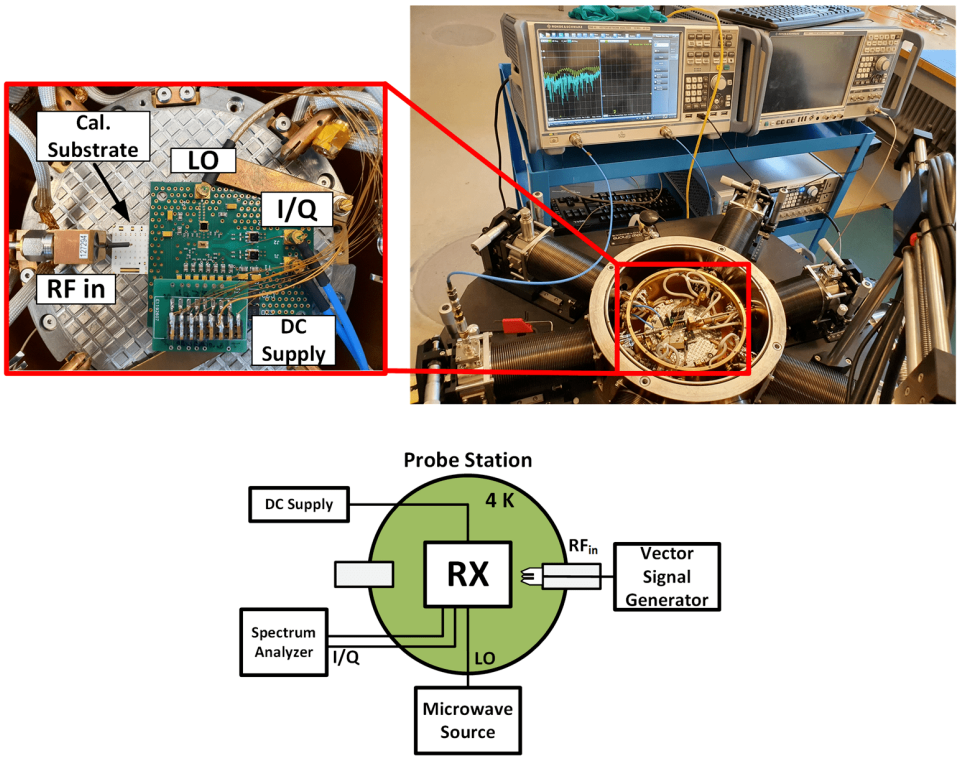


Figure 4.5: Gain, S11, EVM, and linearity measurement setup with the probestation.

4.2. Probe-Station Measurement

Measurement of gain, S11, EVM, and linearity of the RX chip is accomplished in a cryogenic probe station. The following section will discuss the methods used for each measurement and discussed the results obtained from the measurement itself.

4.2.1. Setup

The setup for the measurement is shown in Figure 4.5. Top left of Figure 4.5 shows the PCB inside the probe station for gain, S11, EVM, and linearity measurement. Depending on the measurement, a VNA or a VSG is used to excite the system. An RF probe arm is used to provide input to the chip as it also allows for S11 measurements. The calibration substrate was also used to de-embed the RF probe arm for S-parameter measurements. Due to the limited RF ports in the cryogenic probe station, the differential output of RX chip is also converted to a single-ended signal using a balun. The single-ended I/Q output of the chip is then brought towards RT through SMP cables, as shown from Figure 4.5.

4.2.2. Gain

Two samples were measured for the gain of the RX chip. Both samples are measured in RT and 4K. For clarity, only the quadrature part of the system is plotted in this section. The result of both samples is plotted in Figure 4.6 and Figure 4.7.

Based on the two samples, the two-room temperature performance is very similar in terms of frequency response. Similar peaks can be found at the same frequency for both samples. A difference of 4 dB of gain is observed between the two samples due to process variations. Big discrepancies can be seen, however, when compared to the simulation data; especially at higher frequencies. A possible explanation for this is due to the performance of the buffer itself. A higher capacitive load is observed at the output which brings down the output pole frequency.

The gain of the system at 4K increases by ≈5 dB. A similar increase in gain is also observed from the work of [6, 24]. Such behavior is expected due to mostly the increase in transistor's mobility. The peaks of the conjugate poles at 4K of the transformers are also more pronounced compared to RT data due to the decrease in Q in cryogenic temperatures. Moreover, the RX chip's bandwidth is observed

to be larger due to the reduction of the transformer's inductance and capacitance value at 4K [36]. Another factor that helps to increase the overall bandwidth of the receiver is the output buffer itself. Due to the higher gm observed at cryogenic temperatures, the output buffer can drive the parasitic capacitive load better. Hence, a higher output pole can be observed, as seen in Figure 4.6 and Figure 4.7.

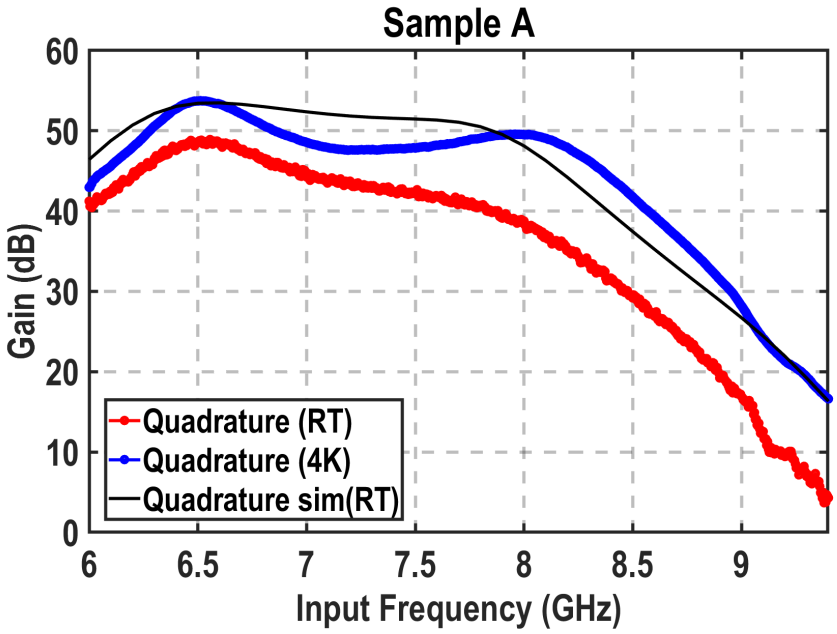


Figure 4.6: RX chip gain at RT and 4K with simulation data for Sample A.

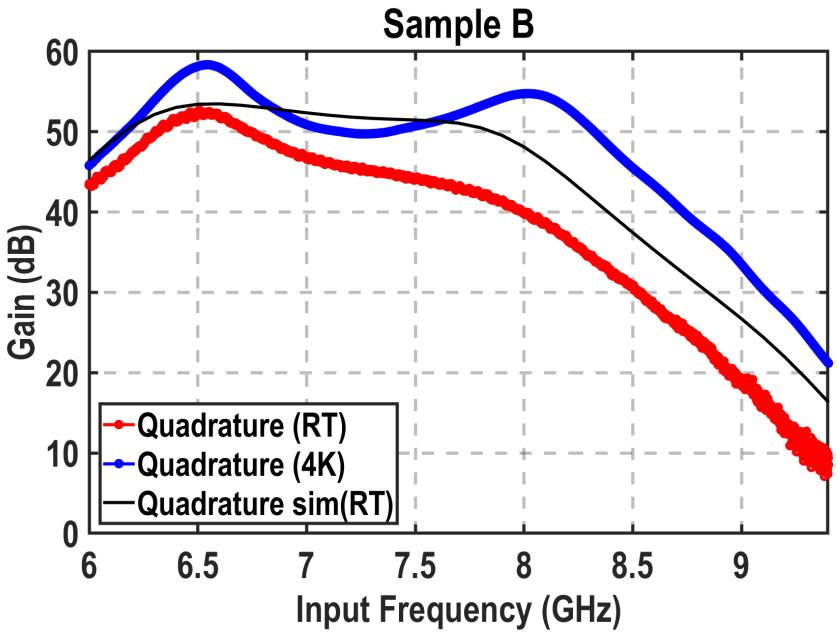


Figure 4.7: RX chip gain at RT and 4K with simulation data for Sample B.

4.2.3. S11

The result of the S11 measurement of the RX chip is illustrated in Figure 4.8 and Figure 4.9. Similar to the gain, the chip is measured in RT and 4K. Before taking any S11 measurement, a full 1-port reflection calibration (open, short, match) is executed on the calibration substrate's RF probe. This is done at RT and 4K.

The first thing to note from the result shown in both Figure 4.8 and Figure 4.9 is that there is an LC product imbalance between the two sides of the transformer. Consequently, the S11 response is not symmetric. The higher conjugate pole frequency has a better matching (>-10dB) than the lower frequency conjugate pole. Similar to the behavior observed for the chip's gain, the two conjugate poles are seen to move slightly further apart and slightly shifts to a higher frequency. Again, this is mainly due to the change of inductor and capacitance value alongside the coupling factor's changes k.

In comparison from RT to 4K measurement, a degradation of S11 at cryogenic temperature is observed. It should be noted that this is due to the changes in the parameter gm, L_s, and C_{gs} value. As seen from 4.5, the impedance of the CS LNA is dependent on these variables. Moreover, as seen from section 3.1, temperature dependence behavior is expected on these parameters.

$$Z_{in} = \frac{gmL_s}{C_{gs1}} + j\left(\omega L_s - \frac{1}{\omega C_{gs1}}\right) \tag{4.5}$$

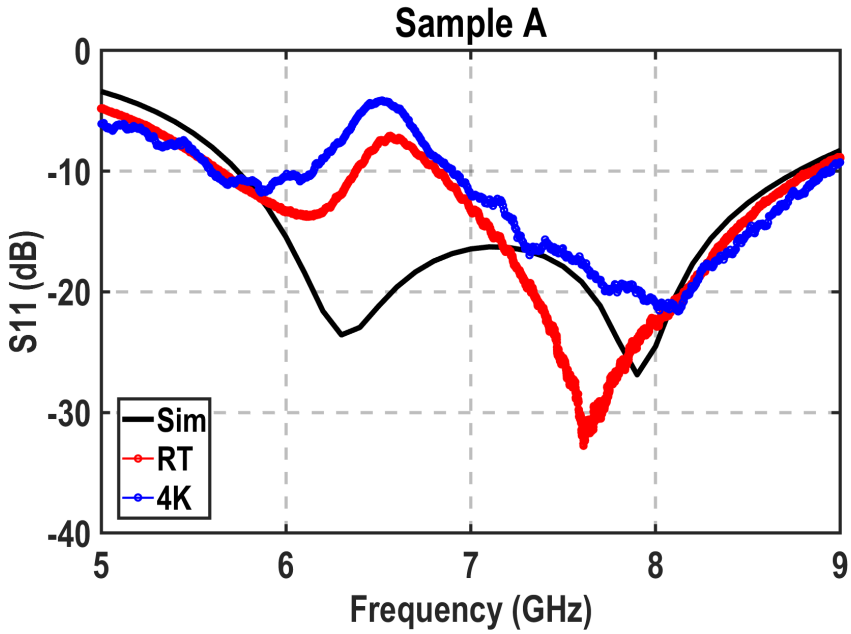


Figure 4.8: S11 of Sample A

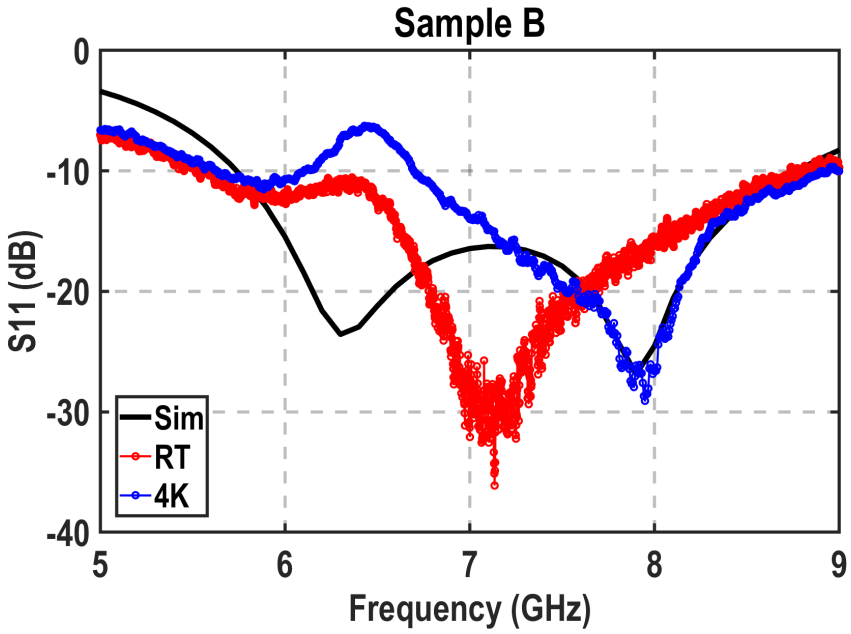


Figure 4.9: S11 of Sample B

4.2.4. EVM

EVM measurement of the receiver is shown in Figure 4.10. The measurement was executed in both RT and 4K. The EVM was measured by using a 40 MSps 16-QAM signal with a carrier frequency of 6.5 GHz. The signal was brought back to an IF of 100 MHz. Time traces were recorded at the output with an oscilloscope, and the result is post-processed in MATLAB. An LPF of 200 MHz was used between the chip and the oscilloscope's input to capture the IF signal.

The result shows that an EVM of -18.96 dB and -21.25 dB was achieved for 4K and RT operation, respectively. A degradation of ≈2 dB was observed at cryogenic temperature. This disparity can stem from different variables. However, it is suspected that EVM's degradation is mostly due to the increased mismatch of the transistor behavior in deep cryogenic temperatures [21]. From [21], it is observed that the mobility of the transistor can vary in cryogenic temperatures, thus leading to ,for instance, a gain mismatch of the I/Q path.

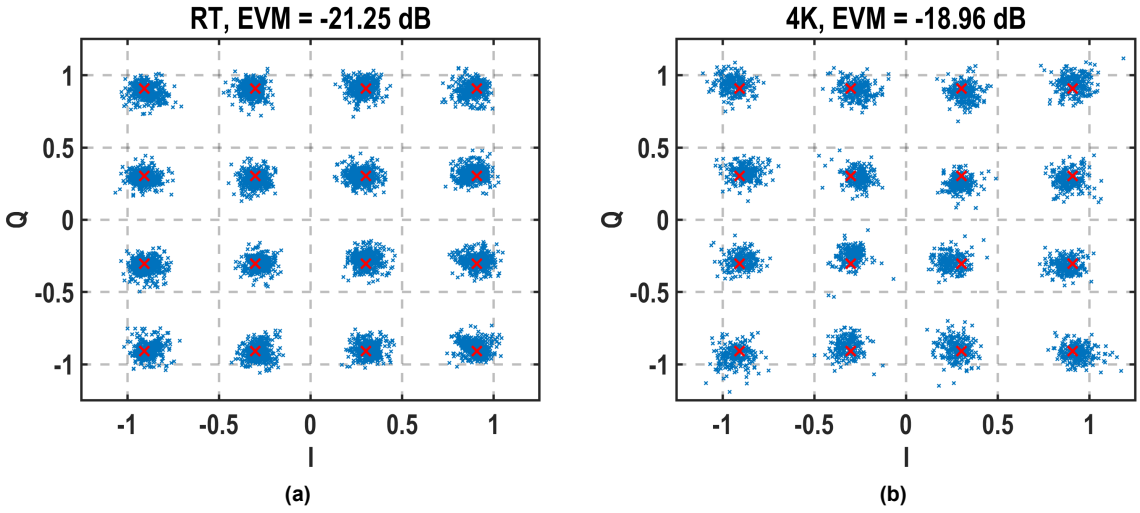


Figure 4.10: (a) RT EVM measurement with 16 QAM modulation. (b) 4K EVM measurement with 16 QAM modulation

4.2.5. Linearity

Different parameters regarding the linearity of the RX chip is measured. This result is shown in Figure 4.12, 4.13, and 4.14.

A two-tone test was done to measure the linearity properties of the RX chip. A two-tone signal with 50 MHz spacing and a center frequency at 6.5 GHz was used to measure Figure 4.12 and Figure 4.14. In the Figure 4.12, the two-tone input power was swept from -70 dBm to -50 dBm. A spectrum analyzer at room temperature records the output spectrum. An LO of 5.9 GHz was again used for this test.

Figure 4.13 shows the result of the two-tone power sweep of the RX chip in RT and 4K. A linear fit line is also extrapolated from the data to calculate the IIP3 and IP1dB of the chip. As expected, a 1 dB rise in the output power of the fundamental frequency for every 1 dB increase in input power is observed. Similarly, a 3 dB increase in the IM3 product is observed for every 1 dB increase in input power.

When comparing the RT and 4K behavior of the fundamental frequency, a ≈5 dB difference between the two power outputs is noted. This is consistent with the gain measurement shown in the previous section. Moreover, considering the 5 dB difference between the two fundamental responses, a corresponding 15 dB difference is reported between the RT IM3 and the 4K IM3 products as expected.

Based on extrapolation, the IIP3 and the IP1dB of the RX chip can be obtained. From the measurement, the chip possesses an IIP3 of -44.9 dBm and -50.8 dBm at RT and 4K, respectively. Furthermore, an IP1dB of -55 dBm and -58.4 dBm at RT and 4K, respectively. Based on Figure 4.12, it is seen that the OIP3 does not change with temperature. Hence, it can be deduced that the reduction of IIP3 is simply due to the higher gain of the RX chip at cryogenic temperature.

The IP1dB is also measured through the behavior of the gain versus input power. This is illustrated in Figure 4.13. From this plot, it is confirmed that the IPdB of the system is -58 dBm and -55 dBm at 4K and RT, respectively.

The frequency spectrum of the two-tone test is illustrated in Figure 4.14. Considering that no attenuators were used in the RX chip's input, the graph reports a similar noise floor value. Again, a difference of ≈5 dB was observed between the fundamental power in RT and 4K. However, it is observed that there is an asymmetry between the lower and higher IM3 product. This phenomenon can understoond from the example shown in Figure 4.11. The two tones will experience different amplitude and phase response by recognizing that the second harmonic of the two-tone input lies outside the desired bandwidth. Through the non-linearity property of the second stage, the two-tone second harmonics can be brought back and combine with the original IM3 component leading to asymmetries.

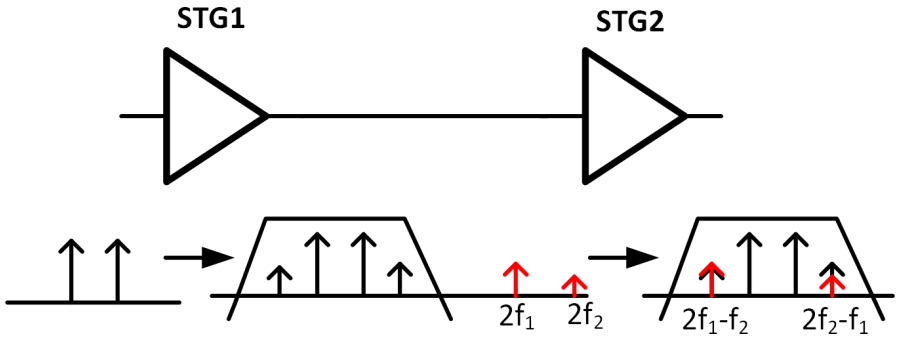


Figure 4.11: A sketch of the mechanism that gives an asymmetric IM3 product.

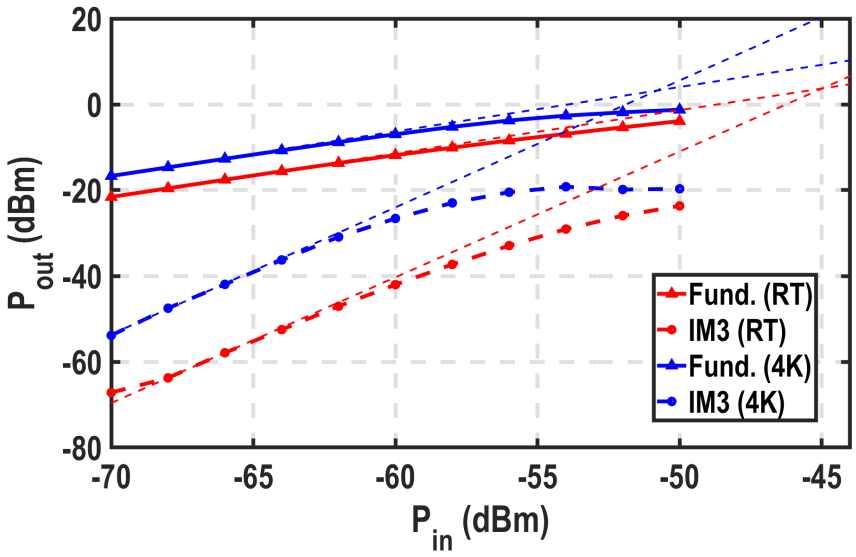


Figure 4.12: Fundamental and IM3 product output power with respect to the input power of a two tone signal with 50 MHz spacing.

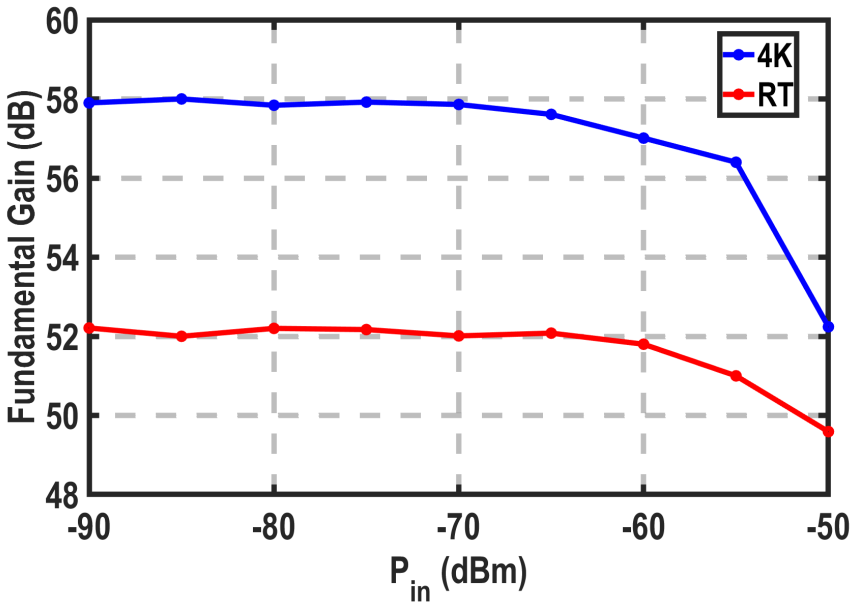


Figure 4.13: Input power sweep versus gain of the RX chip at RT and 4K.

4.3. RX Performance Summary

The performance of the circuit is summarized below. The targeted specification is also listed here again for convenience.

Under the assumption that the RX chip operates at 4K, it can be deduced from table 4.1 that the RX chip achieves close to the required specification. Note that the specification for the noise figure listed in the table is specified for SSB performance. However, minimum noise folding from the image band is expected, as previously shown in section 3.7.

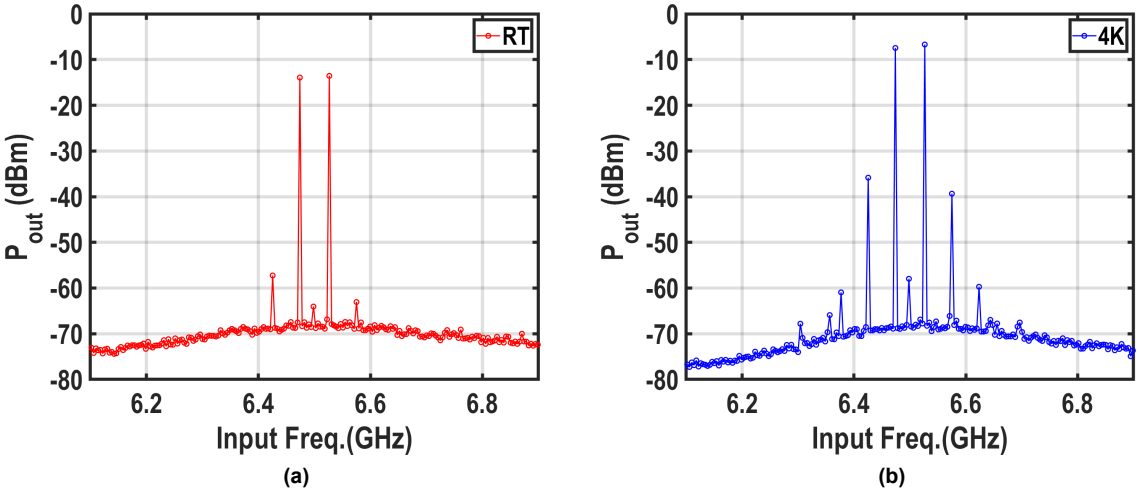


Figure 4.14: Frequency spectrum at RT and 4K. Note that the same input power and frequency spacing was used for both measurement case. P_{in} of -65 dBm was used for the IM3 tests.

	This Work		Specification
Operating Temperature	300 K	4K	
Operating BW	6-8 GHz		4-8 GHz
Gain	52 dB	58 dB	60 dB
NF	2.5 dB*	0.6*dB	1.5 dB†
IIP3	-44.9 dBm	-50.8 dBm	-82.5 dBm
IP1dB	-55 dBm	-58.4 dBm	-44 dBm
Power	70 mW	66 mW	100 mW

† SSB noise figure from specification derivation.
* Measured DSB noise figure.

Table 4.1: Comparison table between the measured performance and the desired specification.

4.4. Qubit Measurement

4.4.1. Background

This section will discuss the experiments done to replace the gate-based spin qubit readout setup used in Ref [49]. The setup has been previously shown in chapter 2 in Figure 2.6. Here, we propose to replace the RT LNA, I/Q Mixer, and IF amplifier of the readout system with the RX chip that has been designed in this project. This section will investigate the qubit readout performance when the chip is in RT and at 4 K.

The measurement process for gate based spin qubit readout has been explained extensively in chapter 2. The process will be repeated in this qubit experiment. In essence, the readout is done by observing the dispersive shift of the resonator's frequency. An RF probe will be sent out at the expected resonant frequency to observe the resulting transmission response. Any amplitude changes, in this case, can be detected by downconverting the probe signal to baseband. Further details on the experimental setup will be explained in each respective section.

In terms of specifications, table 4.2 summarizes the performance of the RT rackmount setup. It should be noted again that the 4K HEMT LNA will still be used for this readout chain and placed before the RX chip.

In comparison to the performance above, we can see that the designed receiver's performance is adequate, thus allowing us to replace the RT instruments with a solution that has less power and a smaller form factor. This is a crucial step towards making a scalable quantum computer.

	Gain [dB]	NF [dB]
AFS3 10-ULN LNA	28	1
IQ-0307XLP Mixer	-5.5	5.5
SR 445A	14	17
Total/Effective Gain and NF	36.5	1.9

Table 4.2: Rack Mount receiver specification

4.4.2. RT Qubit Measurement Setup

As a stepping stone, the spin qubit is measured with the RX chip operating in RT first. The experimental setup of the measurement is shown in Figure 4.15. A microwave source in RT provides the RF probe signal. The input probe signal is attenuated by -70 dB before reaching the qubit sample to reduce RT noise floor. A circulator and an isolator prevent any reflected waves from going back to the qubit sample. A HEMT LNA is still used for this experiment since the CMOS RX chip can not compete with the NF of the HEMT LNA. The RF probe signal is eventually processed by the RX chip and thus be downconverted to a 100 MHz IF frequency. An ADC running at 1GSps with a 120 MHz LPF is used for digitizing the signal. After digitization has taken place, the signal is downconverted digitally to DC further and filtered by a 10 MHz digital filter. The setup explained here is the same measurement setup, as shown in section 3.8.

An enclosure was also designed, as shown in the bottom of Figure 4.20, to reduce the interference effect on the circuit. The PCB used here is similar to the ones used previously. The PCB features an on PCB hybrid to produce I/Q LO signals close to the RX chip. The RX chip's differential output is also converted to a single-ended signal by a balun operating up to 6 GHz.

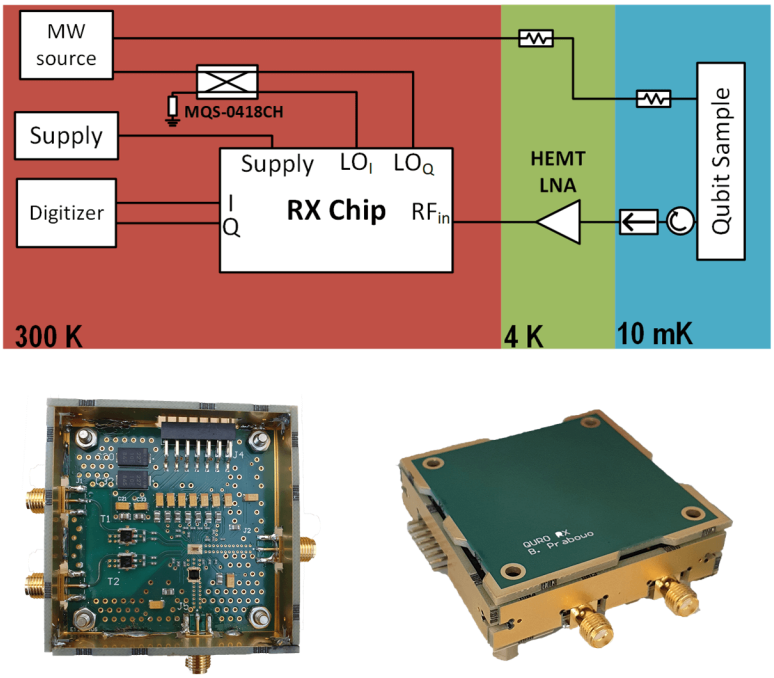


Figure 4.15: Sketch of the measurement setup along with the PCB used for RT measurement.

4.4.3. RT Qubit Measurement Result

Before readout is executed, the readout resonator will be characterized first. The resonator's transmission response was initially tested to locate the resonance frequency in which the result is shown in Figure 4.16. It can be observed that the resonator's resonance frequency is at 6.916 GHz. A bandwidth (FWHM) of 3 MHz and a corresponding Q of 2305 was observed. These values are calculated through a Lorentzian fit, as shown from Figure 4.16.

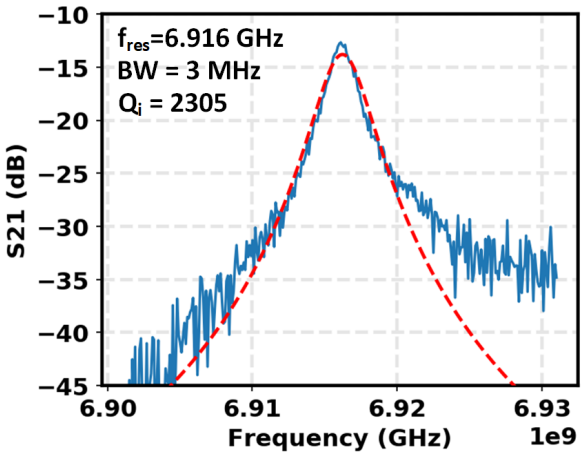


Figure 4.16: Transmission response of the qubit's gate resonator. The red line indicates the Lorentzian fit used to find the characteristic of the resonator.

The charge stability diagram of the DQD can now be measured. The result is shown in Figure 4.17. For this measurement, an RF tone at 6.916 GHz is applied to the resonator, while V_{LP} and V_{RP} are swept. The corresponding S_{21} response is observed. From the figure, a decrease in the S21 at the interdot crossing is observed. The reasoning behind this is discussed earlier in chapter 2; where due to the RF excitation, the electron will oscillate between the two dots and thus shifting the resonator's resonant frequency towards a lower frequency due to the additional tunneling capacitance. Moreover, different charge regimes are seen in this plot. However, we will only concern ourselves with the (1,1)-(0,2) charge regime for qubit operation.

The readout performance is shown in Figure 4.18. In this experiment, the SNR of the readout system is characterized by varying different integration times. A close up at the (1,1)-(0,2) interdot crossing is seen in the top left of Figure 4.18. The line cut response through the interdot crossing is depicted on the top right of Figure 4.17. The figure shows that for higher integration time, a higher SNR can be observed. A pronounced dip is also seen at $V_{RP}\approx$240 mV due to the shift in the resonance frequency. State detection in this scheme is done by observing the amplitude response at the interdot crossing. Note, however, that only the $|1\rangle$ state was measured here (see Figure 2.7). Due to time constraints, we did not manage to experimentally load the left qubit with different spin orientations in order to observe $|1\rangle$ and $|0\rangle$ state readout.

The SNR performance of the readout chain is summarized in Figure 4.18. The performance of the chip is compared to the original measurement setup. The SNR in this measurement is defined by the variable A and B where A is defined as the dip's height at the interdot crossing, and B is the RMS noise amplitude measured at the Coulomb blockade region ($V_{RP}\approx$240 mV). By measuring this SNR at different integration times, the graph shown in Figure 4.18 is obtained. A comparable performance between the two setups can be concluded from the t_{min} of the system. Where t_{min}, defined as when the readout SNR=1, indicates the minimum measurement time of the qubit.

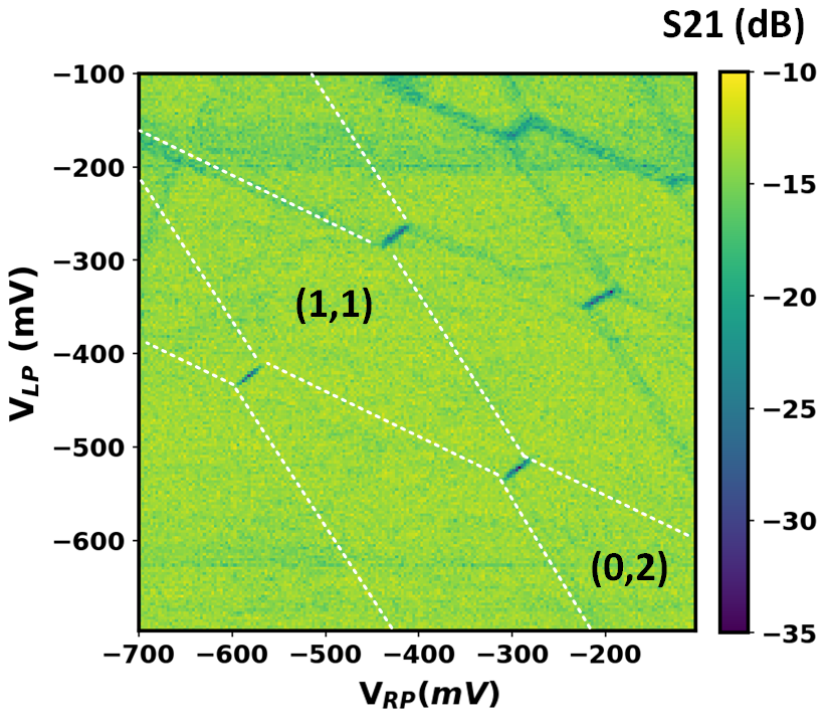


Figure 4.17: Stability Diagram measurement with the CMOS chip at RT.

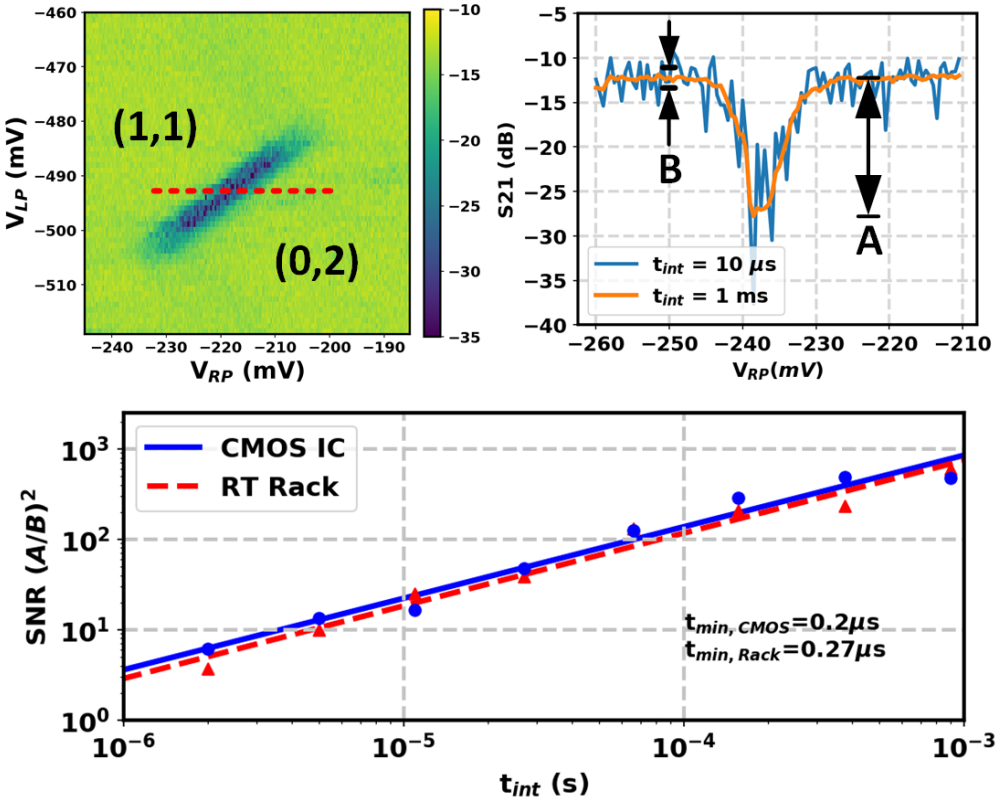


Figure 4.18: Qubit readout performance with the RX chip operating at RT compared to rack mount setup.

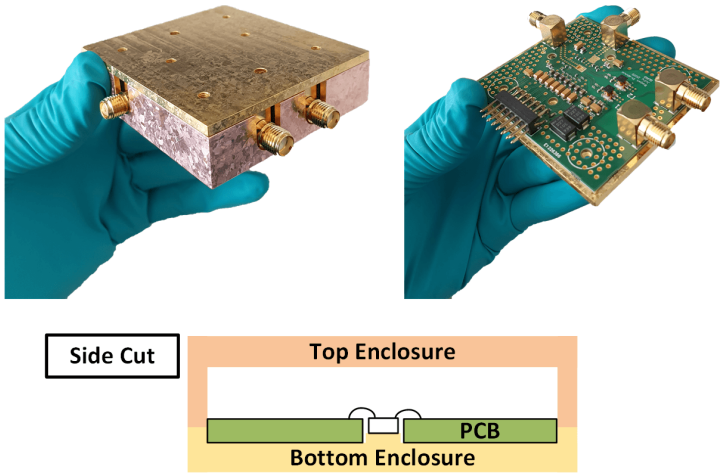


Figure 4.19: Gold plated copper enclosure for the RX chip that is designed to be fitted in the 4K stage of the dilution fridge.

4.4.4. 4K Qubit Measurement Setup

This section will discuss the readout setup used for qubit measurements with the RX chip placed inside the dilution refrigerator.

An enclosure was built for the chip to be mounted in the dilution refrigerator. This ensures that the RX chip is thermalized correctly and will operate as close as possible to 4K. In this design, a gold plated copper enclosure is made, as shown in Figure 4.19. The enclosure is realized in two parts. The bottom section would be the essential part of the enclosure as it has direct contact with the flange of the dilution refrigerator. This part of the enclosure would be gold-plated to reduce the thermal contact resistance between the enclosure and the flange.

A unique solution to thermalizing the chip is also shown in Figure 4.19. The chip will be glued on with silver paste directly onto the copper enclosure as shown instead of the PCB. This ensures that the heat dissipated by the chip will go to the bottom section, which is directly in contact with the fridge itself. A reduction of bond wire length in this method can be achieved by embedding the chip inside the PCB cut-out, as shown from the sketch. This way, the pads on the chip will be on the same level as the PCB plane.

The measurement setup for the cryogenic qubit readout is shown in Figure 4.20. The dilution refrigerator used for the qubit measurement is shown on the left of Figure 4.20. The enclosure will be placed on the 4K flange of the dilution refrigerator, as illustrated. The qubit sample will sit under the mixing chamber to achieve an ambient temperature of 10 mK. An RF switch is also placed at 4K to allow for different measurement configurations. The RF switch allows us to measure just the RX chip itself at 4K, bypassing the RX chip, and do a full qubit readout with the RX chip. Due to the limited amount of DC lines available at the 4K stage of the fridge, some biasing voltages/currents are connected to reduce the number of pins to RT.

4.4.5. 4K Qubit Measurement Result

The result of the experiment is summarized in Figure 4.21. A charge stability scan and an SNR measurement are also executed in this setup.

The charge stability scan resulting from different readout setup is illustrated here for comparison. It is observed that similar results were obtained between the RT rackmount and RX chip operating in RT. The result of the CMOS IC in 4K, on the other hand, shows a significantly lower gain. This is because, during the experiment, it is observed that the whole RX readout chain is oscillating at 150 MHz. The root of this problem has been identified. We suspect that the RX chip's oscillating behavior is due to the circuit's feedback path through the coupled RX chip stages' biasing lines. More specifically, the oscillation is most likely due to the cascode voltage biasing lines that couple the LO drivers, IF amplifier, and the buffer stage.

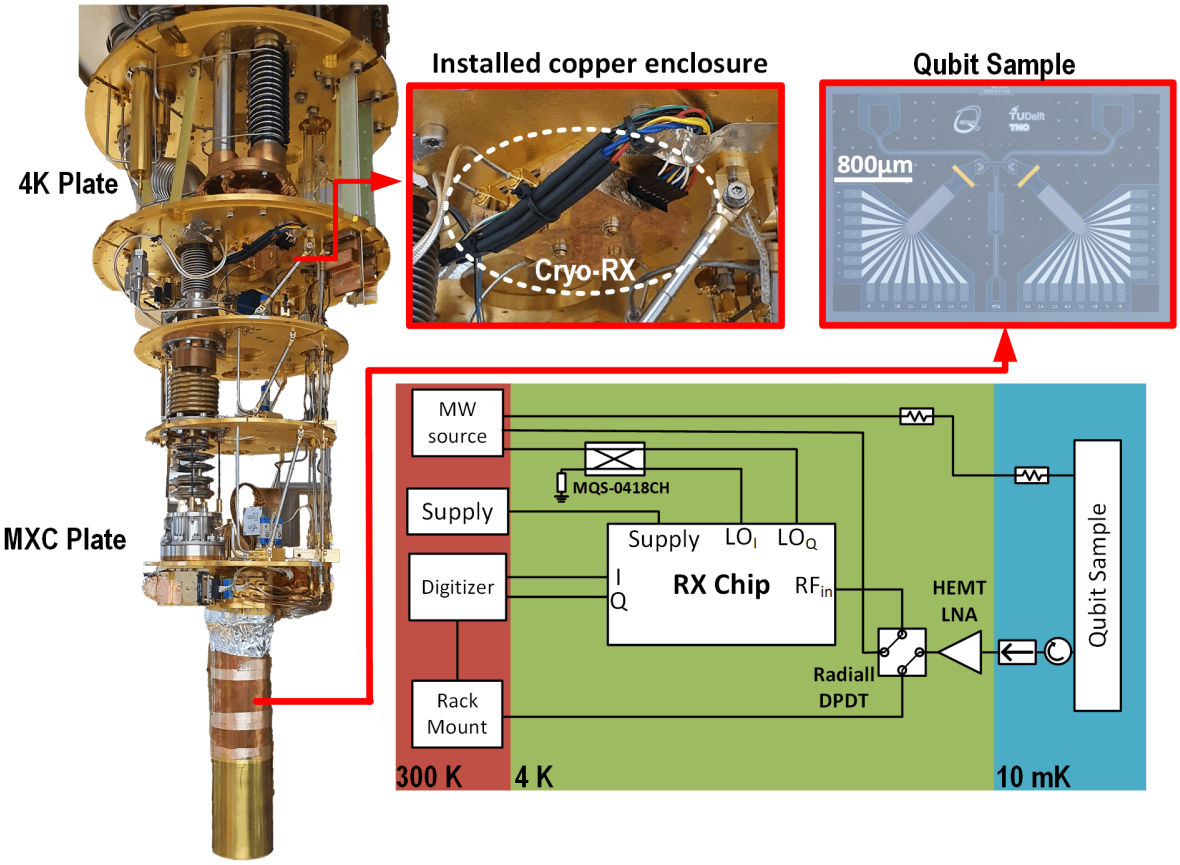


Figure 4.20: Dilution fridge setup for qubit readout. Figure depicts where the RX chip will be placed in the dilution refrigerator. The qubit sample is also shown along with a sketch of the measurement setup.

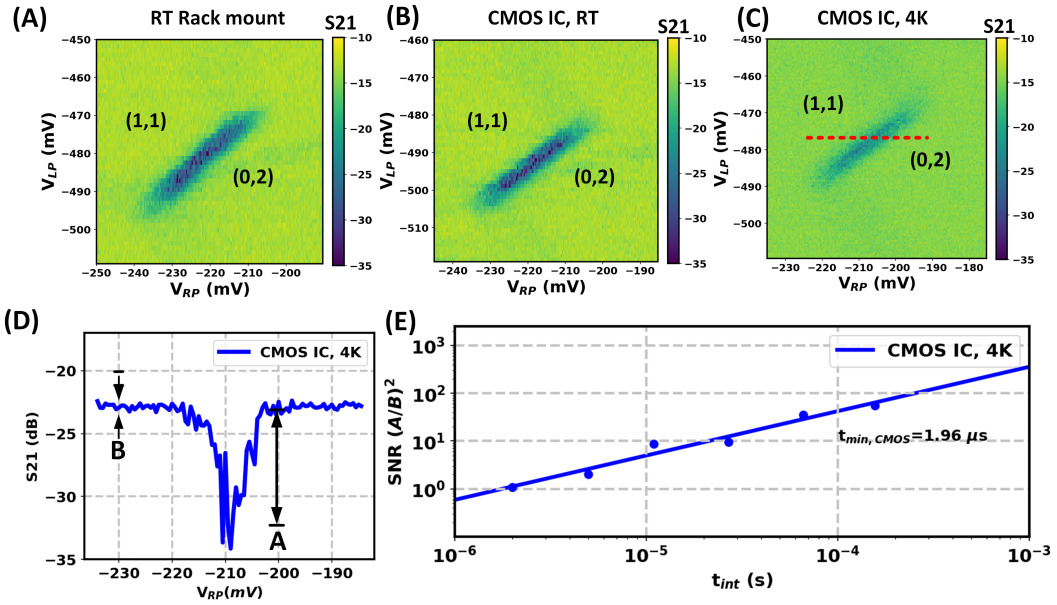


Figure 4.21: (a) Stability diagram measured with RT rackmount. (b) Stability diagram measured with CMOS IC at RT (c) Stability diagram measured with CMOS IC at 4K. (D) Corresponding line-cut measurement of (c) through the indicated red line. (E) SNR readout performance of the CMOS IC at 4K with a t_{min} of 1.96μs.

	This work		RT Rack mount
Operating Temp.	300 K	4.2 K	300 K
Technology	Bulk CMOS 40nm		-
Operating Freq.	6 - 8 GHz		4 - 8 GHz
Gain	52 dB	58 dB	36.5 dB
NF (DSB)	2.5 dB	0.6 dB	1.9 dB
IIP3	-44.9 dBm (Δ=50 MHz)	-50.8 dBm (Δ=50 MHz)	-9.2 dBm*
IP1dB	-55 dBm	-58.4 dBm	-19.2 dBm*
Power Dissipation	70 mW	66 mW	3 W#
Area	0.68 mm²		Rack mount

	This work	L.Guevel, ISSCC'20
Readout scheme	Gate-based RF readout	DC readout
FDMA	Yes	No
Components	LNA, Mixer, baseband amplifier	TIA
Operating temperature	4.2 K	110 mK
P_{DC}/qubit	170 µW	1 µW
Readout BW	2 MHz	1.1 kHz
Min. readout time (t_{min})	1.96 µs	1 ms
Energy/Qubit†	333 pJ	1 nJ

† Energy/qubit = (P_{DC} / qubit) × t_{min}

* Linearity performance only considering the commercial LNA and Mixer from the datasheet

Power excluding the SR445 Preamplifier

Table 4.3: Performance comparison between three state-of-the-art setups. The table compares the performance of the chip characterized in this work with the RT rack mount used for dispersive qubit readout. The RX chip is also compared to the current state-of-the-art DC readout integrated solution shown in Ref [19].

The readout chain's oscillating behavior is mitigated by lowering all the stages' gain, including the HEMT LNA. Consequently, all LNA stages are not at their optimum point where they can provide minimum NF. The consequence of this noise figure degradation is evident in the SNR performance of the readout and the line-cut plot of the interdot crossing. From the figure, it is observed that the t_{min} degrades from 0.2μs to 2μs; a 10x reduction in readout time.

A revision on the PCB is required in order to make better measurement results. A series of resistance on some of the coupled voltage biasing lines can be added to kill the gain of the positive feedback loop.

4.5. Comparison to the State-of-the-art

A comparison to the current state-of-the-art integrated solution is discussed here. At the time of writing this thesis, no integrated RF solution for gate dispersive readout application exists. Hence, a comparison can only be made to the original rackmount setup used for dispersive readout. Moreover, a comparison to the current State-of-the-art DC readout is also considered. The performance of all the three setups is summarized in Table 4.3.

Based on the comparison table shown in Table 4.3, the RX chip's overall performance is similar to the performance of the RT rack mount when operated at cryogenic temperatures. The solution proposed by this work shows that the chip offers comparable performance with less area and power—an essential metric for a scalable quantum computer.

Compared to the current state-of-the-art DC readout solution, it becomes clear that the RF readout technique offers a lot more advantages and lends itself better for large-scale quantum computers due to its FDMA capabilities. Under the assumption that high Q resonators are used for the gate-based readout, a 5 MHz frequency spacing between the qubits can be expected. Thus, with this specification, the RX chip can cover 400 qubits in a 2 GHz bandwidth that results in a P_{DC}/qubit of 170μW/qubit. Considering that the receiver will only turn on during readout, the Energy/Qubit of this work offers a 3x better efficiency with the assumption of the reported minimum readout times.

5 Conclusion

5.1. Main Conclusion

This work presents the design and characterization of a cryogenic CMOS receiver for spin and superconducting qubit readout. The work serves as a stepping stone towards a scalable quantum computer by demonstrating the integration of readout electronics, operating at cryogenic temperature, with qubits inside a dilution refrigerator.

In this thesis, a specification was derived for a high-fidelity qubit readout receiver. The specifications were mostly derived empirically based on the current state-of-the-art readout systems. From the initial analysis done in chapter 3, it is concluded that at this moment, the RX CMOS chip is unable to replace the 4K HEMT LNA due to its NF performance. On that note, the RX chip will instead replace the current room temperature electronics used for qubit readout. Based on the calculations done in chapter 3, it is concluded that for dispersive qubit readout, the receiver should satisfy the following requirements:

	Gain	NF	IIP3	IIP2	IP1dB	Power
Specification	>60 dB	<1.5 dB	>-82.5 dBm	>-65 dBm	>-44 dBm	<100 mW

Table 5.1: Main specification of the CMOS IC receiver.

Characterization of the designed chip was also done in this thesis. The characterization was done to verify its functionality at both RT and 4K. Gain, EVM, linearity, and noise figure were measured at RT and 4K. The observations indicate that better electrical performance can be achieved at 4K compared to RT in terms of noise and gain performance. Moreover, the characterization also confirmed some of the previously observed behavior of passives and active devices in cryogenic temperatures. The performance of the RX chip can be summarized as follows:

	This Work		Specification
Operating Temperature	300 K	4K	
Operating BW	6-8 GHz		4-8 GHz
Gain	52 dB	58 dB	60 dB
NF	2.5 dB*	0.6*dB	1.5 dB†
IIP3	-44.9 dBm	-50.8 dBm	-82.5 dBm
IP1dB	-55 dBm	-58.4 dBm	-44 dBm
Power	70 mW	66 mW	<100 mW

† SSB noise figure from derived specification.
* Measured DSB noise figure.

Table 5.2: Comparison table between the measured performance and the desired specification.

The thesis demonstrates, for the first time, qubit gate readout with an integrated circuit. Two different readout cases were tested, one in which the RX chip is operating at RT and one where the RX chip

operates at 4K. The initial RT qubit readout result shows promising qubit readout performance. During RT testing, the RX chip matches the rack mount setup's performance in terms of SNR. A respectable readout t_{min} of 0.2μs for the RX chip was achieved. Problems occur, however, when moving to 4K. As discussed in section 4.4, oscillations are observed in the readout chain of the experimental setup. It is suspected that this oscillation is due to the coupling between the cascodes voltage biasing line used for the LO driver, IF amplifier, and the output buffer. The issue was mitigated by lowering the chip's gain and the HEMT LNA, which was achieved by lowering each component's biasing current. In the case of the 4K qubit readout experiment, we report a t_{min} of 1.96 μs; approximately 10x degradation in performance in comparison to the RT experiment setup. Note that there is more performance to be gained from this setup. Significant improvement in the readout performance can be obtained by revising the RX chip's PCB for 4K operating temperature.

A comparison was also made to the current state-of-the-art integrated DC readout electronics. It can be concluded from the comparison that RF readout techniques offer a better solution towards a large scale quantum computer due to its FDMA support and better efficiency.

In summary, this work demonstrates that an integrated solution for readout is possible. The work presents a significant step towards the integration of quantum computing electronics for a scalable quantum computer which also supports FDMA. Improvements, however, are still possible. These are described in the next section.

5.2. Future Work

Several improvements and possible future work are presented here:

- Currently, specifications for the RX chip are derived mostly on an empirical approach. More specifically, the specifications are derived based on the current state of the art readout setup's performance. A more analytical approach for deriving the specification is needed to allow for better optimization.
- The noise figure measured in this thesis was seen to not scale well with temperature. It is uncertain whether the noise figure measured is influenced by the self-heating of the LNA's transistor. An on chip temperature sensor should be placed close to the LNA to give an accurate analysis.
- Additional digital features on the chip can be beneficial. For instance, having a tunable capacitor array in the LNA matching network can improve the chip's S11 response. A variable gain amplifier can also be implemented at baseband to account for the receiver's non-flat gain response. Some digital calibration can also be implemented to account for the higher mismatch at cryogenic temperature.
- A new PCB design for the 4K qubit readout experiment should be revised to mitigate the chip's oscillation behavior. Resistors should be placed in series to the transistors' gate to kill any feedback loop of the tied voltage biasing line for the receiver's cascode transistors.
- A cryo ADC can be added to this design to demonstrate an even higher level of integration.
- A multi-tone test to emulate FDMA qubit readout behavior can be done to investigate simultaneous qubit readout performance.
- Full qubit readout measurement with the receiver should be done. As mentioned in section 4.4, the current experiment only detects the $|1\rangle$ state of the qubit. A new experiment needs to be devised to load the qubit with the $|0\rangle$ state be read out by the receiver.

Bibliography

[1] URL https://www.lownoisefactory.com/files/7015/7825/6000/LNF-LNC4_8C.pdf.

[2] Influences on atomic energy levels. URL http://hyperphysics.phy-astr.gsu.edu/hbase/Atomic/atstruct.html.

[3] Quantum theory, the church–turing principle and the universal quantum computer. *Proceedings of the Royal Society of London. A. Mathematical and Physical Sciences*, 400(1818):97–117, 1985. doi: 10.1098/rspa.1985.0070.

[4] The y factor technique for noise figure measurements, 2019. URL https://www.rohde-schwarz.com/us/applications/the-y-factor-technique-for-noise-figure-measurements-application-note_56280-15484.html.

[5] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. S. L. Brandao, D. A. Buell, and et al. Quantum supremacy using a programmable superconducting processor. *Nature*, 574(7779):505–510, 2019. doi: 10.1038/s41586-019-1666-5.

[6] S. Balamurali. Cryogenic cmos lna based onresistive-feedback for rf readout of spin-qubits title. Master's thesis, 2018.

[7] C. Barthel, M. Kjærgaard, J. Medford, M. Stopa, C. M. Marcus, M. P. Hanson, and A. C. Gossard. Fast sensing of double-dot charge arrangement and spin state with a radio-frequency sensor quantum dot. *Physical Review B*, 81(16), 2010. doi: 10.1103/physrevb.81.161308.

[8] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell. An ultra-wideband if millimeter-wave receiver with a 20 ghz channel bandwidth using gain-equalized transformers. *IEEE Journal of Solid-State Circuits*, 51(2):323–331, 2016. doi: 10.1109/jssc.2015.2504411.

[9] C.C. Bultink, M.A. Rol, T.E. O'Brien, X. Fu, B.C.S. Dikken, C. Dickel, R.F.L. Vermeulen, J.C. De Sterke, A. Bruno, R.N. Schouten, and et al. Active resonator reset in the nonlinear dispersive regime of circuit qed. *Physical Review Applied*, 6(3), 2016. doi: 10.1103/physrevapplied.6.034008.

[10] M. A. Castellanos-Beltran and K. W. Lehnert. Widely tunable parametric amplifier based on a superconducting quantum interference device array resonator. *Applied Physics Letters*, 91(8):083509, 2007. doi: 10.1063/1.2773988.

[11] A.h. Coskun and J.c. Bardin. Cryogenic small-signal and noise performance of 32nm soi cmos. *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014. doi: 10.1109/mwsym.2014.6848614.

[12] A. Crippa, R. Ezzouch, A. Aprá, A. Amisse, R. Laviéville, L. Hutin, B. Bertrand, M. Vinet, M. Urdampilleta, T. Meunier, and et al. Gate-reflectometry dispersive readout and coherent control of a spin qubit in silicon. *Nature Communications*, 10(1), 2019. doi: 10.1038/s41467-019-10848-z.

[13] M. J. Curry, M. Rudolph, T. D. England, A. M. Mounce, R. M. Jock, C. Bureau-Oxton, P. Harvey-Collard, P. A. Sharma, J. M. Anderson, D. M. Campbell, and et al. Single-shot readout performance of two heterojunction-bipolar-transistor amplification circuits at millikelvin temperatures. *Scientific Reports*, 9(1), 2019. doi: 10.1038/s41598-019-52868-1.

[14] J. M. Elzerman, R. Hanson, L. H. Willems Van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven. Single-shot read-out of an individual electron spin in a quantum dot. *Nature*, 430(6998):431–435, 2004. doi: 10.1038/nature02693.

[15] J. E. Fernandez. A noise-temperature measurement system using a cryogenic ..., 1998. URL https://ipnpr.jpl.nasa.gov/progress_report/42-135/135F.pdf.

[16] Richard P. Feynman. Simulating physics with computers. *Feynman and Computation*, page 133–153. doi: 10.1201/9780429500459-11.

[17] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland. Surface codes: Towards practical large-scale quantum computation. *Physical Review A*, 86(3), 2012. doi: 10.1103/physreva.86.032324.

[18] J. Gong, Y. Chen, F. Sebastiano, E. Charbon, and M. Babaie. 19.3 a 200db fom 4-to-5ghz cryogenic oscillator with an automatic common-mode resonance calibration for quantum computing applications. *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020. doi: 10.1109/isscc19947.2020.9062913.

[19] Loick Le Guevel, Gerard Billiot, Xavier Jehl, Silvano De Franceschi, Marcos Zurita, Yvain Thonnart, Maud Vinet, Marc Sanquer, Romain Maurand, Aloysius G. M. Jansen, and et al. 19.2 a 110mk 295µw 28nm fdsoi cmos quantum integrated circuit with a 2.8ghz excitation and na current sensing of an on-chip double quantum dot. *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020. doi: 10.1109/isscc19947.2020.9063090.

[20] Ronald Hanson. *Electron spins in semiconductor quantum dots*. s.n., 2005.

[21] P. A. 't Hart, J. P. G. Van Dijk, M. Babaie, E. Charbon, A. Vladimircscu, and F. Sebastiano. Characterization and model validation of mismatch in nanometer cmos at cryogenic temperatures. *2018 48th European Solid-State Device Research Conference (ESSDERC)*, 2018. doi: 10.1109/essderc.2018.8486859.

[22] J. Heinsoo, C. Kraglund Andersen, A. Remm, S. Krinner, T. Walter, Y. Salathé, S. Gasparinetti, J.C. Besse, A. Potočnik, A. Wallraff, and et al. Rapid high-fidelity multiplexed readout of superconducting qubits. *Physical Review Applied*, 10(3), 2018. doi: 10.1103/physrevapplied.10.034040.

[23] R. M. Incandela, L. Song, H.a.r. Homulle, F. Sebastiano, E. Charbon, and A. Vladimirescu. Nanometer cmos characterization and compact modeling at deep-cryogenic temperatures. *2017 47th European Solid-State Device Research Conference (ESSDERC)*, 2017. doi: 10.1109/essderc.2017.8066591.

[24] R. M. Incandela. Cryogenic cmos lna for rf readout of spin qubits title. Master's thesis, 2016.

[25] P. Krantz, A. Bengtsson, M. Simoen, S. Gustavsson, V. Shumeiko, W. D. Oliver, C. M. Wilson, P. Delsing, and J. Bylander. Single-shot read-out of a superconducting qubit using a josephson parametric oscillator. *Nature Communications*, 7(1), 2016. doi: 10.1038/ncomms11417.

[26] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver. A quantum engineer's guide to superconducting qubits, Aug 2019. URL https://aip.scitation.org/doi/10.1063/1.5089550.

[27] Thomas H. Lee. *The design of CMOS radio-frequency integrated circuits*. Cambridge Univ. Press, 2012.

[28] M. Malnou, D.A. Palken, Leila R. Vale, Gene C. Hilton, and K.W. Lehnert. Optimal operation of a josephson parametric amplifier for vacuum squeezing. *Physical Review Applied*, 9(4), 2018. doi: 10.1103/physrevapplied.9.044023.

[29] A. Mazzanti and A. Bevilacqua. Second-order equivalent circuits for the design of doubly-tuned transformer matching networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 65(12):4157–4168, 2018. doi: 10.1109/tcsi.2018.2846029.

[30] M. Mehrpoo, B. Patra, J. Gong, P. A.t Hart, J. P. G. Van Dijk, H. Homulle, G. Kiene, A. Vladimirescu, F. Sebastiano, E. Charbon, and et al. Benefits and challenges of designing cryogenic cmos rf circuits for quantum computers. *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019. doi: 10.1109/iscas.2019.8702452.

[31] R. Mizuta, R. M. Otxoa, A. C. Betz, and M. F. Gonzalez-Zalba. Quantum and tunneling capacitance in charge and spin qubits. *Physical Review B*, 95(4), 2017. doi: 10.1103/physrevb.95.045414.

[32] W. Walden. Mumford and E. H. Scheibe. *Noise performance factors in communication systems*. University Microfilms, 1968.

[33] Michael A. Nielsen and Isaac L. Chuang. *Quantum computation and quantum information*. Cambridge University Press, 2000.

[34] P. Padalia. Design of cmos voltage references for ultra-wide temperature ranges. Master's thesis, 2019.

[35] P. Pakkiam, A.V. Timofeev, M.G. House, M.R. Hogg, T. Kobayashi, M. Koch, S. Rogge, and M.Y. Simmons. Single-shot single-gate rf spin readout in silicon. *Physical Review X*, 8(4), 2018. doi: 10.1103/physrevx.8.041032.

[36] B. Patra, R. M. Incandela, J. P. G. Van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and et al. Cryo-cmos circuits and systems for quantum computing applications. *IEEE Journal of Solid-State Circuits*, 53(1):309–321, 2018. doi: 10.1109/jssc.2017.2737549.

[37] B. Patra, J.P. G. Van Dijk, S. Subramanian, A. Corna, X. Xue, C. Jeon, F. Sheikh, E. Juarez-Hernandez, B. P. Esparza, H. Rampurawala, and et al. 19.1 a scalable cryo-cmos 2-to-20ghz digitally intensive controller for 4×32 frequency multiplexed spin qubits/transmons in 22nm finfet technology for quantum computers. *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020. doi: 10.1109/isscc19947.2020.9063109.

[38] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie. Characterization and analysis of on-chip microwave passive components at cryogenic temperatures. *IEEE Journal of the Electron Devices Society*, 8:448–456, 2020. doi: 10.1109/jeds.2020.2986722.

[39] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard. Coherent manipulation of coupled electron spins in semiconductor quantum dots, Sep 2005. URL https://science.sciencemag.org/content/309/5744/2180.full.

[40] R. Pettai. *Noise in receiving systems*. Wiley, 1984.

[41] B. Razavi. *RF Microelectronics*. Dorling Kindersley, 2014.

[42] Y. Salathé, P. Kurpiers, T. Karg, C. Lang, C. K. Andersen, A. Akin, S. Krinner, C. Eichler, and A. Wallraff. Low-latency digital signal processing for feedback and feedforward in quantum computing and communication. *Physical Review Applied*, 9(3), 2018. doi: 10.1103/physrevapplied.9.034011.

[43] Peter W. Shor. Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer. *SIAM Journal on Computing*, 26(5):1484–1509, 1997. doi: 10.1137/s0097539795293172.

[44] L. Vandersypen and A. V. Leeuwenhoek. Quantum computing - the next challenge in circuit and system design. *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017. doi: 10.1109/isscc.2017.7870244.

[45] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst. Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Information*, 3(1), 2017. doi: 10.1038/s41534-017-0038-y.

[46] T. Walter, P. Kurpiers, S. Gasparinetti, P. Magnard, A. Potočnik, Y. Salathé, M. Pechal, M. Mondal, M. Oppliger, C. Eichler, and et al. Rapid high-fidelity single-shot dispersive readout of superconducting qubits. *Physical Review Applied*, 7(5), 2017. doi: 10.1103/physrevapplied.7.054020.

[47] A. West, B. Hensen, A. Jouan, T. Tanttu, C. Yang, A. Rossi, M. Fernando Gonzalez-Zalba, F. Hudson, A. Morello, D. J. Reilly, and et al. Gate-based single-shot readout of spins in silicon. *Nature Nanotechnology*, 14(5):437–441, 2019. doi: 10.1038/s41565-019-0400-7.

[48] M.P. Westig and T.M. Klapwijk. Josephson parametric reflection amplifier with integrated directionality. *Physical Review Applied*, 9(6), Nov 2018. doi: 10.1103/physrevapplied.9.064010.

[49] N. Zheng, G.and Samkharadze, M. L. Noordam, N. Kalhor, D. Brousse, A. Sammak, G. Scappucci, and L. M. K. Vandersypen. Rapid gate-based spin read-out in silicon using an on-chip resonator. *Nature Nanotechnology*, 14(8):742–746, 2019. doi: 10.1038/s41565-019-0488-9.

[50] L. Zhong, E. P. Menzel, R. Di. Candia, P. Eder, M. Ihmig, A. Baust, M. Haeberlein, E. Hoffmann, K. Inomata, T. Yamamoto, and et al. Squeezing with a flux-driven josephson parametric amplifier. *New Journal of Physics*, 15(12):125013, Nov 2013. doi: 10.1088/1367-2630/15/12/125013.

A

Coupled Transformer Derivation

The following chapter is dedicated to the derivation of the coupled transformer transfer function used for the receiver. Multiple configurations of this coupled transformer exist; however, only some configuration can be solved analytically and provide insights into the design. One example of a coupled transformer that can be solved analytically is shown in figure A.1.

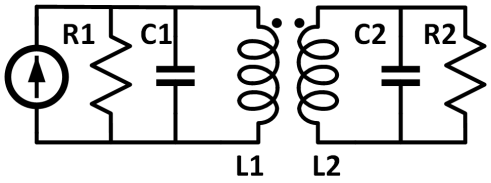


Figure A.1

We start by taking a look at the model of the coupled transformer, as shown in figure A.1. We can remodel the transformer into an equivalent T-model illustrated in figure A.2. Note that $M = k\sqrt{L_1 L_2}$, where k is the coupling factor of the transformer. The transfer function from the current source to V_2

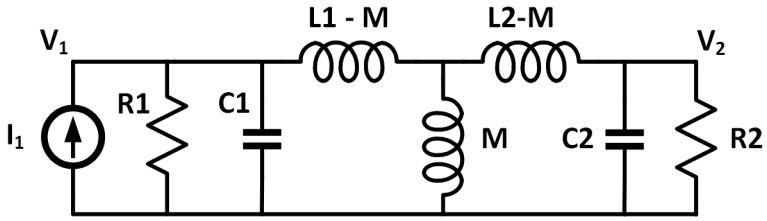


Figure A.2

is obtained by finding the transmission ABCD matrix. The relevant forms of the ABCD matrix used for this calculation are summarized in table A.1. From the definition, the ABCD matrix is expressed as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \left.\frac{V_1}{V_2}\right|_{I_2=0} & \left.\frac{V_1}{I_2}\right|_{V_2=0} \\ \left.\frac{I_1}{V_2}\right|_{I_2=0} & \left.\frac{I_1}{V_2}\right|_{V_2=0} \end{bmatrix} \tag{A.1}$$

Thus, the total ABCD matrix of the circuit shown in A.2 is expressed as in equation A.2. The resulting matrix multiplication can be calculated in Maple.

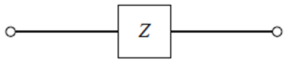
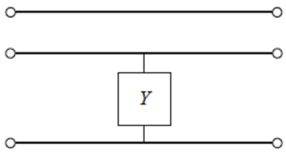
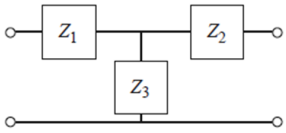
Circuit	*ABCD* Parameters	
	$A = 1$ $C = 0$	$B = Z$ $D = 1$
	$A = 1$ $C = Y$	$B = 0$ $D = 1$
	$A = 1 + \frac{Z_1}{Z_3}$ $C = \frac{1}{Z_3}$	$B = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3}$ $D = 1 + \frac{Z_2}{Z_3}$

Table A.1: ABCD Parameters used for the calculation of the coupled transformer matching network.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{R_1} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_1 & 1 \end{bmatrix} \begin{bmatrix} 1 + \frac{j\omega(L_1 - M)}{j\omega M} & j\omega(L_1 - M) + j\omega(L_2 - M) + \frac{j\omega(L_1 - M)j\omega(L_2 - M)}{j\omega M} \\ \frac{1}{j\omega M} & 1 + \frac{j\omega(L_2 - M)}{j\omega M} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_2 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_2} & 1 \end{bmatrix} \tag{A.2}$$

For the case of the model shown in figure A.2, we concern ourselves with the variable 1/C (V_2/I_1). The resulting transfer function (V_2/I_1) is shown in A.3.

$$\frac{V_2}{I_1} = \frac{kR_1R_2\sqrt{L_1L_2}s}{As^4 + Bs^3 + Cs^2 + Ds + E} \tag{A.3}$$

Where A,B,C,D, and E are the denominator's coefficient listed in table A.2.

Coefficients	
A	$L_1L_2C_1C_2R_1R_2(1 - k^2)$
B	$L_1L_2(C_1R_1 + C_2R_2)(1 - k^2)$
C	$[(L_1C_1 + L_2C_2)R_1R_2 + L_1L_2(1 - k^2)]$
D	$(L_2R_1 + L_1R_2)$
E	R_1R_2

Table A.2

B

Cold Attenuation Y-Factor Derivation

This chapter explains the derivation of the Y-factor measurement formula used in chapter 4. Before going to the derivation of the formula, some preliminary theories will be shown beforehand.

We first consider figure B.1. For an arbitrary system with components at different temperatures, the output noise observed at (a)-(a') will be:

$$v_n^2 = 4kT_{eff}R_{eq} \tag{B.1}$$

We define R_{eq} as the Thevenin equivalent resistance of the circuit and T_{eff} to represent the effective temperature of the circuit. Provided that the load (Z_{eq}) as shown from figure B.1 is a complex conjugate of the source, then:

$$v_n^2 = \frac{v_n^2}{4R_{eq}} = kT_{eff} \tag{B.2}$$

We can expand equation B.2 further to give a better understanding of T_{eff}. This is shown below.

$$S_n = \frac{4k(|A_1|^2R_1T_1 + ... + |A_N|^2R_NT_N)}{4R_{eq}} \tag{B.3}$$

$$S_n = k\left(\frac{|A_1|^2R_1T_1}{R_{eq}} + ... + \frac{|A_N|^2R_NT_N}{R_{eq}}\right) \tag{B.4}$$

$$S_n = k\left(\alpha_1T_1 + ... + \alpha_NT_N\right) = kT_{eff} \tag{B.5}$$

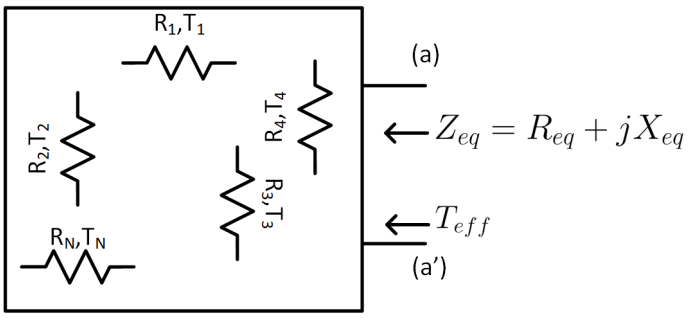


Figure B.1: Power transfer in an arbitrary system with different temperature.

From equation B.5, we can see that the output noise is the result of the resistor's temperature in combination with the weighted variable α_N. The total contribution of αT$_N$ is equivalently written as T_{eff}. However, finding these coefficients can be tedious. We can also interpret the solution differently. By following Pierce's rule [32] we can interpret it as follows

When a unit of power is delivered to a linear, passive, two-terminal network, the fraction α_N can be interpreted as the the power absorbed by R_N.

We can apply this concept to the case shown in figure B.2. This will be relevant in deriving the noise temperature at the DUT's input for cryogenic noise figure measurement. Let us consider the setup in figure B.2. When a unit of power is applied to (a)-(a'), the power dissipation of each component is:

$$1 = \alpha_L + \alpha_{att} \tag{B.6}$$

$$\alpha_L = \frac{1}{L} \tag{B.7}$$

$$\alpha_{att} = 1 - \frac{1}{L} = \frac{L-1}{L} \tag{B.8}$$

Where α_L is the power dissipated in R_L and α_{att} is the power dissipated by the attenuator. Hence, by using Pierce's interpretation we can see that T_{eff} at (b)-(b') is:

$$T_{eff} = \frac{T_L}{L} + \left(\frac{L-1}{L}\right) T_x \tag{B.9}$$

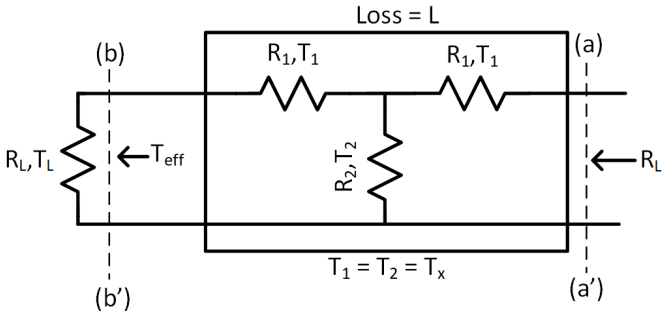


Figure B.2: Lossy power transfer to a matched load.

Knowing this, we can now move on to the cryogenic noise figure measurement setup, as shown in figure B.3. We can now calculate the effective temperature at each reference point indicated by (a)-(a'), (b)-(b'), and (c)-(c'). Two different cases are considered: when the noise source is 'hot' and when the noise source is 'cold'.

At (a)-(a'):

$$T_a = \frac{T_{h/c}}{L_1} + \left(\frac{L_1 - 1}{L_1}\right) T_{cryo} \tag{B.10}$$

At (b)-(b'):

$$T_b = \left[\frac{T_{h/c}}{L_1} + \left(\frac{L-1}{L}\right) T_{cryo} + T_{DUT}\right] G_{DUT} \tag{B.11}$$

At (c)-(c'):

$$T_c = \frac{T_b}{L_2} + \left(\frac{L_2 - 1}{L_2}\right) T_{cryo} \tag{B.12}$$

When we take equation B.12 and refer back to (a)-(a'), we will get the following equation:

$$T_{a,ref} = \left[\frac{T_{h/c}}{L_1} + \left(\frac{L-1}{L}\right) T_{cryo} + T_{DUT}\right] + \frac{L_2}{G_{DUT}} \left(\frac{L_2 - 1}{L_2}\right) T_{cryo} \tag{B.13}$$

Under the assumption that the gain G_{DUT} is high and low cable loss at the output, the second term will become negligible.

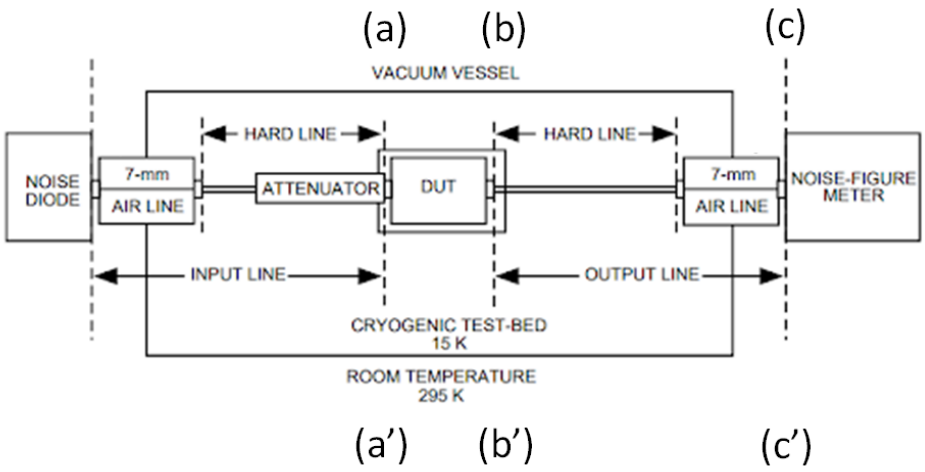


Figure B.3: Cold attenuator measurement setup. Image from [15].

Using equation B.13, we can now calculate the new Y-factor formula for the setup. As discussed in the main text, the Y-factor is the noise power ratio observed at the output when the noise source is 'hot' or 'cold'. Moreover, this ratio is proportional to the noise temperature observed at the output. Thus, Mathematically this is expressed in equation B.13.

$$Y = \frac{T_{a,ref,h}}{T_{a,ref,c}} \tag{B.14}$$

By plugging in equation B.13 for hot and cold cases to equation B.14, we obtain the following solution:

$$T_\alpha = \frac{1}{L_1}\frac{T_{hot} - YT_{cold}}{Y-1} \tag{B.15}$$

$$T_\alpha = \left(\frac{L_1 - 1}{L_1}\right)T_{cryo} + T_e \tag{B.16}$$