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A Pitch-Matched Transceiver ASIC With Shared Hybrid Beamforming ADC for High-Frame-Rate 3-D Intracardiac Echocardiography

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***Abstract*— In this article, an application-specific integrated circuit (ASIC) for 3-D, high-frame-rate ultrasound imaging probes is presented. The design is the first to combine element-level, high-voltage (HV) transmitters and analog front-ends, subarray beamforming, and in-probe digitization in a scalable fashion for catheter-based probes. The integration challenge is met by a hybrid analog-to-digital converter (ADC), combining an efficient charge-sharing successive approximation register (SAR) first stage and a compact single-slope (SS) second stage. Application in large ultrasound imaging arrays is facilitated by directly interfacing the ADC with a charge-domain subarray beamformer, locally calibrating interstage gain errors and generating the SAR reference using a power-efficient local reference generator. Additional hardware-sharing between neighboring channels ultimately leads to the lowest reported area and power consumption across miniature ultrasound probe ADCs. A pitch-matched design is further enabled by an efficient split between the core circuitry and a periphery block, the latter including a datalink performing clock data recovery (CDR) and time-division multiplexing (TDM), which leads to a 12-fold total channel count reduction. A prototype of 8×9 elements was fabricated in a TSMC 0.18-μm HV BCD technology and a 2-D PZT transducer matrix with a pitch of 160 μm, and a center frequency of 6 MHz was manufactured on the chip. The imaging device operates at up to 1000 volumes/s, generates 65-V transmit pulses, and has a receive power consumption of only 1.23 mW/element. The functionality has been demonstrated electrically as well as in acoustic and imaging experiments.**

***Index Terms*— 3-D ultrasound, high-frame-rate, high-voltage (HV) transmitter, hybrid analog-to-digital converter (ADC), intracardiac echocardiography (ICE), subarray beamforming, successive approximation register (SAR)/single-slope (SS) ADC, ultrasound application-specific integrated circuit (ASIC).**

I. Introduction

SEVERAL cardiovascular conditions can be addressed using minimally invasive interventions, including the treatment of cardiac arrhythmia through electrophysiology and catheter ablation, trans-catheter valve replacement, closure of atrial septal defects, and occlusion of the left atrial appendage [1], [2]. Real-time guidance of these interventions is traditionally achieved through fluoroscopy. However, this is associated with a low resolution of soft tissue and exposure of the patient and the physician to harmful ionizing radiation [3].

Ultrasound imaging can alleviate these disadvantages. But simply obtaining images of the heart from outside the body with a hand-held probe, in a so-called transthoracic echocardiogram (TTE), suffers from a limited acoustic window through the chest and requires a dedicated operator [4]. It is possible to obtain unobstructed, high-resolution ultrasound images from within the body by imaging from the esophagus in a transesophageal echocardiography (TEE) procedure or from within the heart in an intracardiac echocardiography (ICE) procedure [5]. The latter can often work on the same local anesthesia as the actual intervention as opposed to the, more risky, general anesthesia required for working from the esophagus. This has made ICE one of the most commonly applied ultrasound tools for minimally invasive cardiac interventions [4].

Until recently, a drawback of ICE probes was their limitation to 2-D images. This was mostly due to the integration and wiring challenge posed by the larger transducer matrix that is generally required for 3-D imaging [6]. The probes are limited to a diameter of around 3 mm to enable accessing the heart through the vascular system, as shown in an example with entry from the inferior vena cava in Fig. 1(a). Within this space, the transducer array has to be accommodated at

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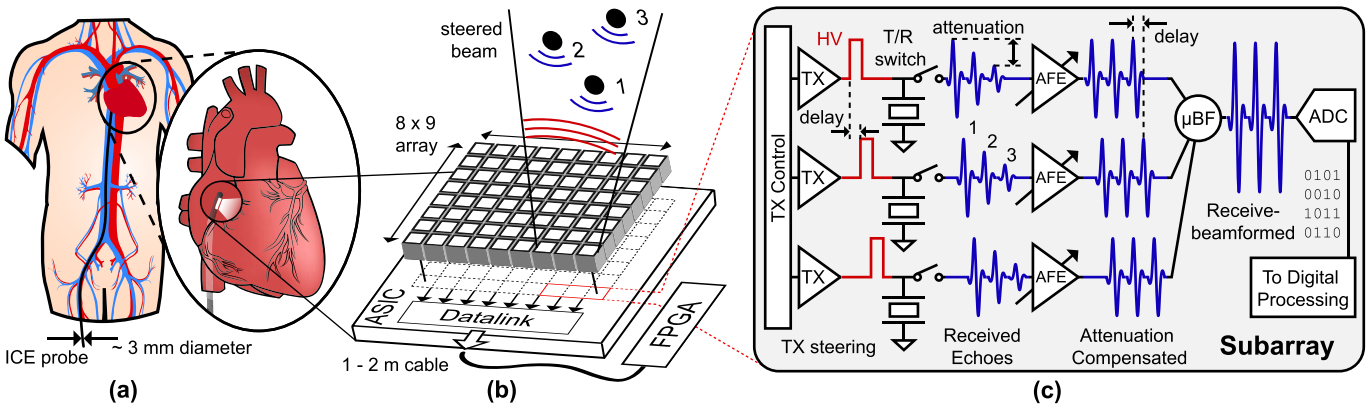

Fig. 1. (a) Example of an ICE procedure with catheter entry from the inferior vena cava and imaging of the left ventricle from the right atrium. (b) Transducer matrix array integration overview. (c) Schematic of a 1×3-element subarray including transmit (TX) and receive circuitry.

the tip and all external connections in the shaft. To enhance the visualization for the physician, 3-D images were initially created from either manual [7] or motorized [8] rotation of 1-D transducer arrays, sacrificing real-time imaging capability or resulting in very low frame rates. In [9], a helical 1-D array was applied instead, enabling 3-D imaging at higher frame rates at the cost of a limited elevation opening angle of just 22°. The class of forward-looking, ring-shaped probes [10], [11] showed a similar issue in being able to provide 3-D images but only for a small volume ahead of the device and therefore not being applicable for the full range of procedures. A way to achieve a sufficient field of view and imaging rate is provided with the advanced integration of 2-D transducer arrays in the catheter tip. However, the problem is that for individual connection from each transducer element to an imaging system outside the body, the interconnect becomes limiting to the array size, resulting in insufficient image quality [12], [13], [14].

Subarray beamforming has recently been investigated as an approach to interface large arrays, such as the approximately 1000 elements of a typical 3-D ICE device [6], [15]. The method shifts part of the receive beamforming, usually applied in the imaging system, into the catheter in the form of delay-and-sum operations on the received signals of a subarray [16]. This effectively reduces the number of connections needed inside the catheter shaft as only the combined signal is transmitted. However, it does not provide the raw data of the full array and introduces focusing errors [17]. These result in increased grating and sidelobe levels as well as broadening of the main beam, all negatively impacting image quality. Narrower transmit beams can be used to mitigate these effects but require more acquisitions per volume, ultimately leading to a trade-off between subarray size, with related channel count reduction, and achievable frame rate [18].

A reduction in frame rate leads to worse motion tracking and can prevent the use of upcoming imaging modes like high-frame-rate blood flow or electromechanical wave imaging [19], which offer more diagnostic potential to physicians but require about 1000 volumes/s. A method to manage the impact on frame rate while still offering cable count reduction is provided by multiplexing multiple channels onto one cable in analog or digital form. Analog multiplexing has been demonstrated in the time [20], [21] and frequency [22] domains but is constrained by the limited bandwidth across the commonly applied micro-coaxial cables and suffers from channel-to-channel crosstalk [23]. Digital time-domain multiplexing (TDM), on the other hand, has been shown to benefit from better tolerance to crosstalk, interference, and noise [15]. The availability of digital receive signals in the catheter moreover opens the possibility for future cointegration with emerging image processing such as data reduction with machine-learned compression [24], [25] or adaptive beamforming [26]. A major benefit of multiplexing lies in the compatibility with subarray beamforming, as has been shown in digital beamforming of element-level signals [27], [28], [29] and analog beamforming with subsequent digitization and TDM [15], [30], [31]. While the former requires an analog-to-digital converter (ADC) per element, the subarray area available for the latter makes the scheme more feasible for large arrays.

Both ways, current digital ICE probe designs still suffer from large ADCs. This expresses itself in the reported designs not being able to match the element-level circuitry to the transducer pitch [28], [31], a requirement for a scalable system, or the associated silicon area requirement making cointegration with adequate transmit circuitry impossible [15], [32], [33]. These transmitters need to excite the transducer elements with high-voltage (HV) pulses to obtain sufficient signal-to-noise ratio (SNR) for around 10-cm imaging depth, requiring the use of HV transistors with large isolation rings [6].

In this article, a scalable application-specific integrated circuit (ASIC) with a cointegrated 160-μm×160-μm transducer array is presented [34]. While [15] has already shown a large channel count reduction through the combination of subarray beamforming and digital TDM with a beamforming ADC, the presented converter was too big to be able to include transmitters. Moreover, its associated subarray size of 3×3 elements precludes frame rates on the order of 1000 volumes/s. To address these issues, this article presents a novel hybrid beamforming ADC, consisting of an efficient charge-sharing successive approximation register (SAR) first stage and a compact single-slope (SS) second stage. The ADC architecture achieves the smallest reported power consumption and area

among miniature ultrasound probe ADCs, enabling a subarray size of only 1×3 elements and thereby pushing the maximum frame rate to the targeted 1000 volumes/s. Moreover, it allows for the integration of per-element 65-V transmitters [35] and front-ends, analog subarray beamformers, and digitization in a pitch-matched fashion. The system has a 12-fold data channel count reduction, resulting in 96 data channels for the envisioned full system [17]. In a trade-off between the available circuit area and the achievable image quality, the transducer pitch was chosen just above the half-wavelength margin. The resulting grating lobe artifacts stay below an acceptable level [17] and can be further reduced through coherent compounding of subvolume acquisitions [36] and potentially further mitigated through recently shown machine-learning-based image processing techniques [37], [38].

This article is organized as follows. Section II presents the system architecture, with the circuit implementation of the ADC being further detailed in Section III. Section IV covers the fabricated prototype and discusses electrical, acoustic, and imaging experiments. This article ends with a comparison to the prior art and a conclusion.

II. System Design

A. Overview

An overview of the conceptual system, showing common techniques in ultrasound imaging applied in this design, is given in Fig. 1(c). Each transducer element is used for the transmission (TX) of pressure waves and the subsequent reception (RX) of echoes, generated by reflectors in the imaged medium, in a pulse-echo (PE) cycle. The shared element usage between TX and RX maximizes the achievable aperture in size-constrained probes, as displayed in Fig. 1(b).

During the TX phase, HV pulsers are driving the transducer elements based on the inputs from a TX controller. The controller applies delays to achieve TX beam steering, forming diverging waves to scan the whole volume with a small number of transmissions. To protect the low-voltage (LV) RX circuits from HV operation of the transmitter, a transmit/receive (T/R) switch is placed between the two sections of the design.

Once the transmission is completed, the switch closes and a readout circuit can access the transducer. A common issue in ultrasound imaging systems is the large dynamic range (DR) accumulated by propagation in an exponentially attenuating medium. The attenuation A, in dB, is proportional to the distance z, the attenuation coefficient α, and, for heart tissue, approximately the frequency f [39]

$$A = 2 \cdot z \cdot f \cdot \alpha. \tag{1}$$

The imaging frequency has to be determined based on a trade-off between the axial resolution and the imaging depth and is in this design set to 6 MHz with a depth of 10 cm [17]. Combined with an attenuation coefficient of about 0.5 dB/MHz/cm for heart tissue [39], the attenuation could reach 60 dB. Considering an instantaneous DR of 40 dB, the total DR can therefore reach 100 dB. As not all that range is of interest throughout an RX period and the attenuation is time-dependent, the DR to be handled by the RX circuits can, however, be reduced by a procedure called time gain compensation (TGC). This is achieved by giving the analog front-end a variable gain that can be adjusted during one PE cycle, giving equally strong reflectors at different distances from the transmitter a similar output and easing the design requirements for the following circuitry [40].

The received signals from each channel in the device are combined in a beamforming operation to reconstruct the information of each voxel in the imaged volume. An SNR gain of $\sqrt{N}$ for N elements in the beamformer is possible if the system SNR is limited by uncorrelated noise and can aid in the design for a large DR. To reduce the number of connections from the probe to a beamforming system, part of the reconstruction can already be performed in the probe per subarray. This subarray beamforming, also referred to as micro-beamforming (μBF), applies delay-and-sum operations to individual signals of a subarray, effectively steering the RX beam to target the previously insonified area [16]. The combined signals can then be digitized for further local processing and sent to an imaging system.

An overview of the cointegration of the ASIC and a bulk piezoelectric PZT transducer matrix array is given in Fig. 1(b). The 160-μm pitch stack is an optimized version of what has been presented in [41] and gets manufactured directly on the surface of ASIC. It connects to exposed top metal pads on one side and a shared aluminum ground foil on the other side, as shown in Fig. 2(a). The 8×9-element assembly serves as a prototype with an architecture and layout design suitable for scaling to a full array of 64×18 elements [17]. While the prototype has a reduced aperture, it is already tailored toward the intended imaging scheme of acquiring a 70°×70°×10 cm volume in front of the transducer matrix at a frame rate of 1000 volumes/s. Given an imaging depth z of 10 cm and the speed of sound c of 1540 m/s in tissue, a maximum pulse repetition frequency (PRF) $= c/(2z)$ of 7.7 kHz can be reached. This provides seven PE cycles for the formation of each volumetric image at a rate of 1000 volumes/s. To optimize their usage toward the best image quality, the beam profile and subarray receive beamformer size are determined in a trade-off with the required channel count reduction and necessary circuit area. This work applies seven transmit beams of 70° divergence in the azimuth direction and 10.7° divergence in the elevation direction in a sweep of the elevation steering angle to cover the full 70°×70°×10 cm volume. In receive, subarrays of three elements along the elevation direction are applied which presteer the received signal in the same direction as the transmit beams [17].

B. Architecture

The implemented system architecture of the prototype is shown in Fig. 2(b). Each transducer element's bottom plate is connected to an individual pulser and a variable-gain analog front-end (AFE), implementing TGC. The TX part is realized as a unipolar, 65-V design with a pull-up and a pull-down path provided by DMOS transistors. To facilitate test modes and reduce the complexity, the TX control signals are provided externally per row, with an area reserved for an integrated TX controller in a future version. A single LV transistor, protected

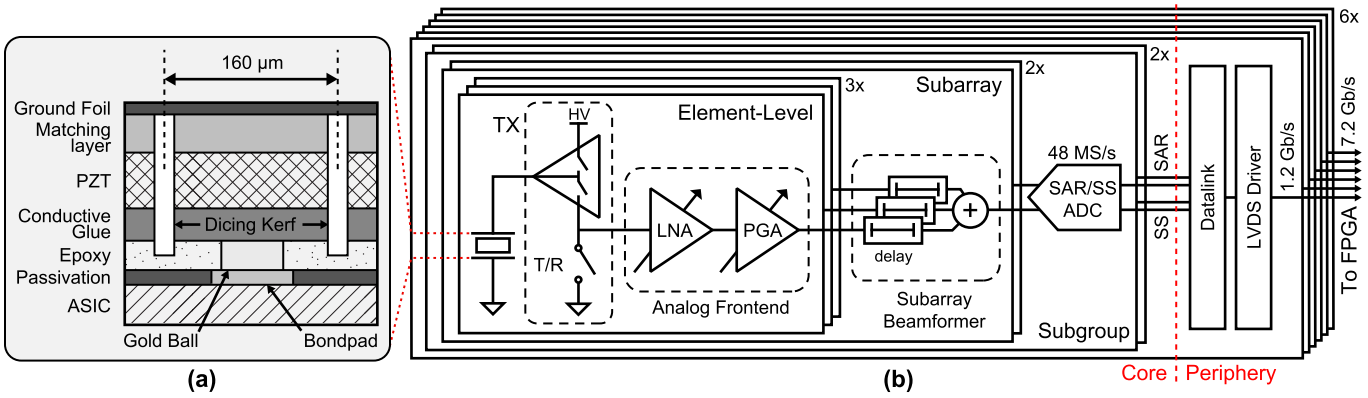

Fig. 2. (a) Conceptual sketch of the transducer stack. (b) System architecture including element-level pulsers and analog front-ends, subarray beamformers, and a shared hybrid ADC structure per subgroup. On the periphery, each channel is connected to an FPGA via a datalink and an LVDS driver.

against voltage breakdown by the HV NMOS of the pulser, enables T/R switching to the input of a low-noise amplifier (LNA) [42] in the receive phase [35]. LNA is configurable to a voltage gain between −12 and 24 dB at a step size of 18 dB and, together with the second-stage programmable gain amplifier (PGA) that provides 6–24 dB at a step size of 6 dB, achieves a total variable gain between −6 and 48 dB at a step size of 6 dB [15]. In each PE cycle, the gain is gradually switched from the lowest to the highest gain setting to first grant sufficient linearity for the initially received strong echoes and later enough gain to detect strongly attenuated echoes out of the noise floor. The PGA is a voltage amplifier with a compact T-type capacitive feedback network [43], configured for quick settling after switching the gain during active operation. To provide rejection of common interference in the following signal chain, it converts the single-ended signal into a differential output.

The outputs of three element-level circuits are merged in a 1×3-element subarray beamformer, of which two are combined in a 2×3-element subgroup. Each subgroup shares a hybrid SAR/SS ADC structure that separately digitizes the two channels at 24 MS/s with a resolution of 10 bits each. The outputs of two subgroups are received by a periphery-level block, providing a datalink to process the received data and applying TDM onto an LV differential signal (LVDS) driver to transfer the data to an OFF-chip field-programmable gate array (FPGA). Each periphery block serves a 4×3 matrix of elements, and six of these are arranged to form the prototype of 8×9 elements. A total channel count reduction of 12 is implemented by the subarray beamformer size of 3 and TDM of the digital outputs of four subarrays onto one channel.

C. Hybrid ADC

To cover the discussed DR of up to 100 dB, a 10-bit resolution is chosen to complement the 54-dB TGC and $\sqrt{N}$ beamforming gain. The sampling frequency should be at least four times higher than the frequency of the transducer to maintain an acceptable sidelobe level [44], leading to a 24-MHz sampling rate for the 6-MHz device. For similar specifications, SAR ADCs have been shown to be an effective solution due to their high efficiency and Nyquist rate sampling [45]. Similar to [15], SAR conversion is performed in the charge domain to benefit from direct integration with a subarray beamformer into a beamforming ADC. However, this design uses a capacitive digital-to-analog converter (CDAC) with metal–oxide–semiconductor capacitors (MOSCAPs). While their voltage-dependent capacitance excludes them from use in charge redistribution ADCs, in charge-sharing topologies MOSCAPs reduce area through high integration density and improve comparator offset as well as noise tolerance [46].

One drawback of SAR ADCs in general is the exponential increase in CDAC size per added bit of resolution in the binary search algorithm. This can be alleviated by means of combination with a slope ADC that digitizes the residual of an SAR first stage in a hybrid converter [33], [47]. A slope ADC can be compact but suffers in efficiency when converting with a high resolution and sampling rate. In the following, the architecture of a hybrid SAR/SS beamforming ADC operating in the charge domain is presented. An optimal split between the two stages is found in a 6-bit SAR and a 5-bit SS conversion with one bit of redundancy between them. This considers the required size reduction in SAR stage and added complexity to the slope stage of the design. To benefit from the reduction in CDAC size, the gained area must outweigh that of the added SS blocks. As the unit capacitor of CDAC is still sized for 10-bit linearity, this is mainly achieved by enabling a CDAC size that is actually linearity-limited, good MOSCAP matching, and the overhead reduction due to a reduced number of unit capacitors.

The ADC is interfacing with the subarray beamformer as shown in Fig. 3, avoiding the need for an additional high-bandwidth buffer compared with converters with conventional sampling [33], [47]. The delaying of the received signals is implemented by means of capacitive sample-and-hold (S/H) cells, similar to [48]. The summation of the delayed signals can then be achieved passively by switching the right cells together at the input of the ADC, as in [15]. In contrast to [15], the control logic of the subarray beamformer, as shown in Fig. 4(a), can also provide delay quantization independent of the sampling frequency. This is enabled by separate read and write pointers, S_{RDx} and S_{WRx}. The former is advancing based on completed ADC conversion cycles, ADC_{RDYC}, while the

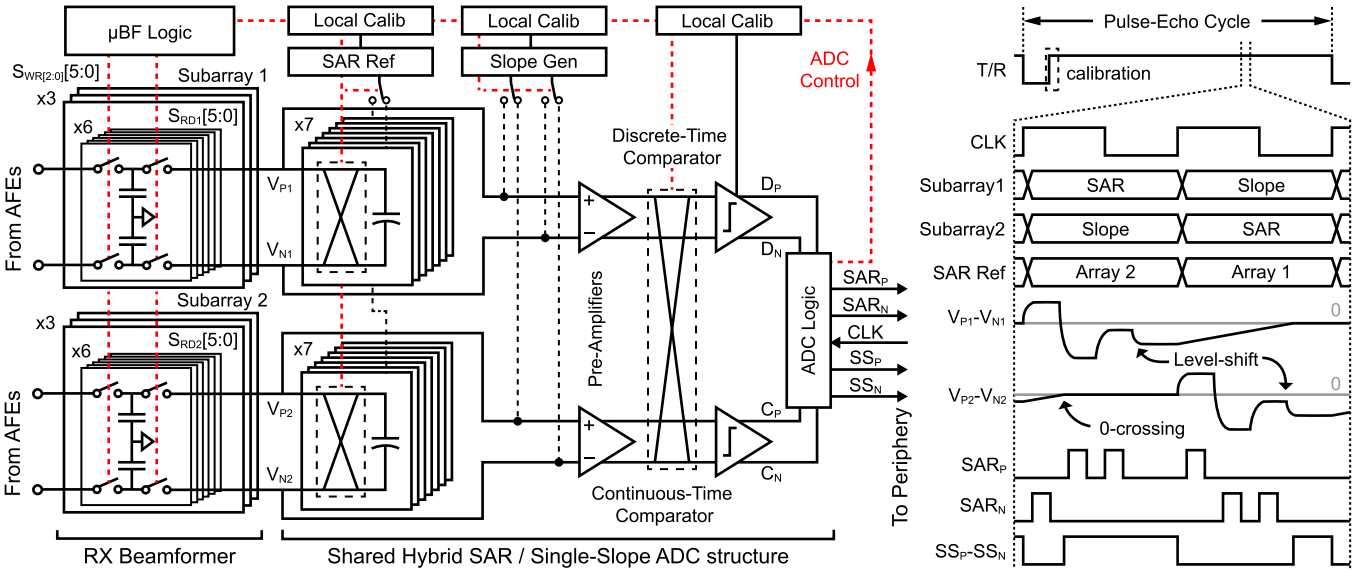

Fig. 3. Architecture of the proposed hybrid ADC formed between am SAR first stage and an SS second stage with a conceptual timing diagram showing essential nodes and how two subarray outputs are digitized by the shared structure.

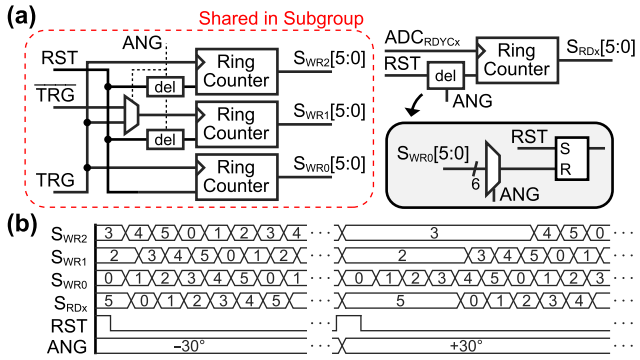

Fig. 4. (a) Schematic overview of the subarray beamformer. (b) Conceptual S/H-cell timing diagram with maximum positive and negative angles.

latter advances based on an adjustable input trigger, in this case a locally generated 24-MHz signal and its 180°-phase-shifted version, TRG and $\overline{\text{TRG}}$. While each ADC requires its own read pointer, the write pointers can be shared between multiple channels. The pointers are realized as ring counters, and different steering angles, determined by ANG, can be realized by delaying the reset signal between the pointers. An area-efficient implementation of this delay is achieved by reusing the pointer of one AFE, AFE0, as the reference counter for the delay. Based on ANG, this can be used to implement the delay with a simple multiplexer and a compact set–reset (SR) latch. The resulting S/H-cell switching patterns are shown for a maximum positive and negative steering angle in Fig. 4(b). A delay resolution of 20.8 ns is achieved with a range up to 125.0 ns, offering steering capability of the axis of the beam in a ±30° window.

Following the subarray beamformer, the combined charge can be quantized through the positive or negative connection of binary-scaled units of a precharged CDAC and detection of the polarity with a discrete-time comparator (DTC). After this SAR conversion, the possible residual charge range between nodes V_{Px} and V_{Nx} has been reduced to least significant bits (LSBs) and can thereafter be digitized by applying a differential slope with compact current sources on the same nodes. To have the redundant range between the two stages work for positive and negative decision errors in SAR conversion, part of CDAC is switched after the first phase to implement a level shift, placing the SAR residual in the middle of the SS conversion range. As long as the residual is not contaminated and they are within the redundant range, all the SAR decision errors, such as DTC noise, CDAC settling errors, and mismatch between the SAR and SS comparator offset, can be covered.

High area efficiency is achieved by hardware-sharing between two neighboring subarrays, forming one shared ADC structure. The two phases of the conversion are executed in two periods of a 48-MHz clock, twice as high as the ADC sample rate, and while the first subarray performs SAR conversion, the second applies the slope and vice versa. In this fashion, the SAR reference precharger and the slope generator can be shared, and a drawback that is typically introduced in the hybrid architecture can be mitigated: Usually, the combination of an SAR and an SS stage requires the introduction of an asynchronous DTC for an efficient SAR part and a continuous-time comparator (CTC) to avoid a high-frequency comparator clock for SS [33], [47]. While this is still the case, they can be shared between the two subarrays with the addition of a small preamplifier that provides isolation and serves as part of both comparisons. Another benefit of hardware-sharing is that SAR CDAC can be switched out and slowly precharged during slope conversion. Compared to designs with conventional references [33], [47], this allows for the use of a low-bandwidth reference with a constant current drawn from the supply. Moreover, it does not require an additional CDAC used for ping-pong operation as in [15].

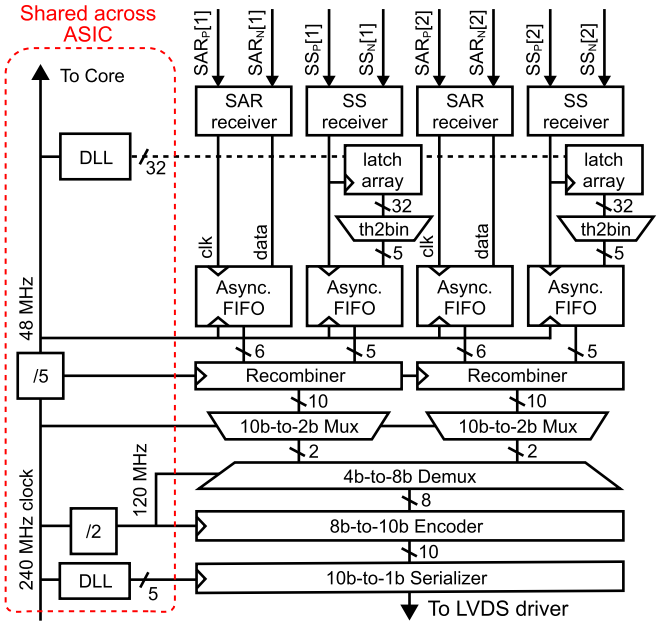

Fig. 5. Datalink block diagram showing processing of the outputs of four ADCs and the clocking scheme shared across ASIC.

To further facilitate application in large imager arrays, critical nodes in the circuit, including SAR reference, slope generator, and DTC offset, are calibrated against mismatch.

As in ultrasound probes, the area underneath the transducer matrix is typically very limited to achieve a scalable, pitch-matched design but there is more space available at the periphery [32], [40], [48], and the received signals are brought out of the core as soon as they are quantized. This applies to return-to-zero (RZ), asynchronous SAR outputs, SAR_P and SAR_N, which are gated versions of the DTC outputs, D_P and D_N, and the SS outputs, SS_P and SS_N. The SAR and SS outputs of both the converted channels are each carried on one connection to the periphery and correctly merged there to minimize the interconnect space.

D. Datalink

An overview of the datalink is shown following Fig. 5. The SAR and SS outputs of two shared ADC structures, serving 12 elements in total, are captured on the periphery by separate receivers. The SAR receiver recovers the SAR output data, as well as a clock that can be used to sample the data in the following stage, directly from the asynchronous RZ SAR output [15]. The SS receiver, on the other hand, converts the differential time-domain output of the SS into a short pulse. This pulse is used to latch the output of a delay locked loop (DLL) that divides the 48-MHz clock period into 32 segments, corresponding to a 5-bit word. As the SS comparison in the core is based on the same time reference, this word is an accurate representation of the second-stage ADC output. The resulting 32-bit word is then converted from a thermal into a binary code to simplify further processing and can be sampled with the same pulse as the latch array. The asynchronous SAR and SS data can subsequently be synchronized to the periphery clock by dual-clock first-in, first-out (FIFO) memories. To reduce the final data bandwidth to the imaging system, the recombination block merges the 6-bit SAR and 5-bit SS codes into the actual 10-bit output code of the ADC. This is done by summing both the parts and removing the redundancy introduced between the two stages in the following manner [47]:

SAR		1	0	0	1	0	1	-1		
SS	+						1	0	1	0	1
Combined		1	0	0	1	0	1	1	1	0	1

The subtraction of the redundancy is implemented with the two's complement. The outputs of two recombiners are subsequently merged through TDM, realized by arranging two 10-bit words at 48 MHz to 8-bit words at 120 MHz. The following structures are based on [15] and first apply 8b10b-encoding to enable a standard transmission protocol [49]. The 10-bit output words are then serialized to a 1.2-Gbps output stream to the conventional LVDS drivers with timing provided by a DLL. Both the DLLs are based on [56], shared among the whole ASIC and operate on a single 240-MHz system clock provided from an FPGA. A 120-MHz clock is generated locally at the periphery for the encoder and TDM, while a 48-MHz clock provides the timing for all core circuitry and data reconstruction on the periphery. While a balanced clock distribution in the core is required as a time reference for the generation of the intended RX and TX beams, the 48-MHz clock phase of the core does not need to be precisely matched to that of the periphery as only the clock period is relevant for clock data recovery (CDR).

III. Circuit Implementation

A. Timing

As the key enabling block of the system, the implementation of the shared hybrid ADC structure is further detailed in this section. The timing can be followed in Fig. 6(c). A nonoverlapping (NOV) clock generator, as shown in Fig. 6(a), creates a division of the 48-MHz system clock, CK_{SYS}. The resulting synchronous NOV signals are used especially in the operation of SAR reference and SS circuitry and prevent interference from sharing blocks. The SAR reference, as shown in Fig. 7(a), is configured as a voltage-controlled current source with a calibrated input $V_{CAL\text{-}SAR}$ and source degeneration R_S to increase its linearity and lower its transconductance. The current in the precharger is always running and steered between the two DACs of the converter in fixed time intervals, with a short reset period applied at the beginning of each charging. The slope generator in Fig. 7(b) is also implemented as a steered voltage-controlled current source between the two parts of the shared ADC structure and calibrated by $V_{CAL\text{-}SS}$. A very short NOV period SS_x is generated locally to prevent connection of the preamplifier input nodes of the two involved ADCs, V_{Px} and V_{Nx}, while still having the slope period closely matched to that of CK_{SYS}. If SS_{RDYx} indicates an SS conversion has finished, the input of the corresponding preamplifier is connected together to a mid-rail node V_{CM}, setting up the next conversion.

While the reference circuits require determined timing, particularly the comparators benefit from more flexible control

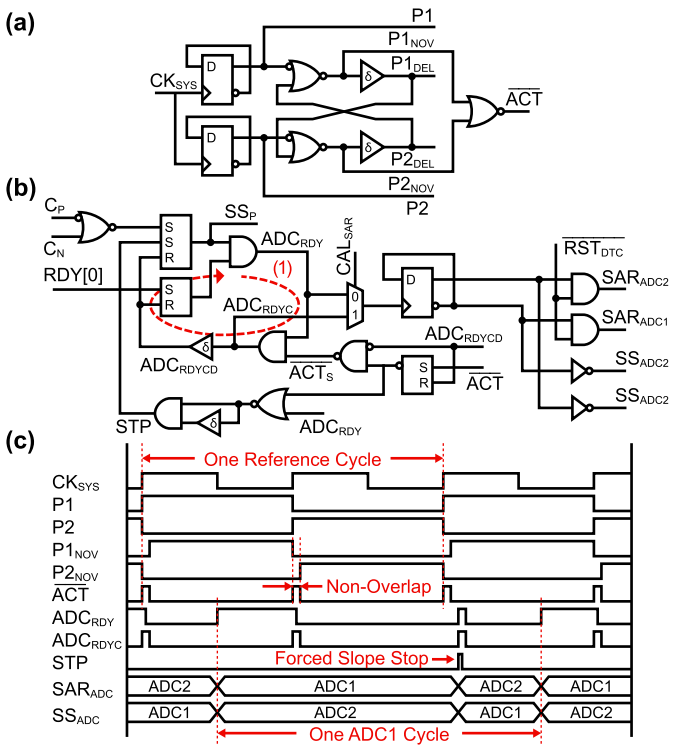

Fig. 6. (a) Synchronous timing generator of the shared converter. (b) Loop determining asynchronous ADC timing. (c) Conceptual timing diagram.

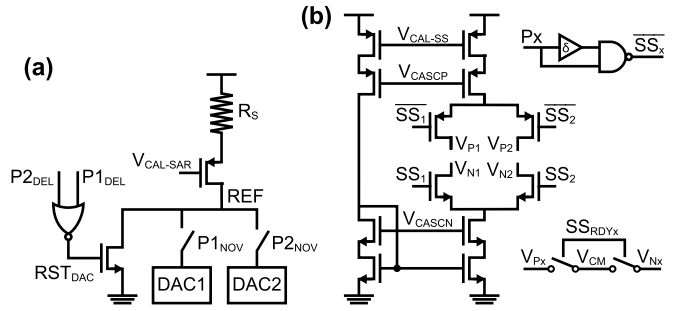

Fig. 7. (a) Schematic of the CDAC reset and precharger. (b) Slope generator schematic with reset and switching blocks.

to make most efficient use of the CK_{SYS} period. Feedback loop (1) in Fig. 6(b) offers this by applying control signals not based on a clock but based on finished ADC conversion parts. Two area-efficient SR latches determine a completed conversion from CTC outputs $C_{P/N}$ and RDY[0] signal of the last bit in the SAR logic. If both the parts are ready, an internal flip-flop (FF) is in regular operation directly toggled with ADC_{RDY}, indicating that the state of the converter structure shifts and CTC and DTC can be switched, enabling a longer settling period for the preamplifier before the next part of conversion starts. The reset of SR latches for the next conversion part is determined by the combination of ADC_{RDY} and ACT_S signal, the second being a latched version of the active signal indicating the passing of an NOV period. The signal needs to be latched as SS conversion can extend over the period in which the slope generator is applied because of the delay of CTC. To still enable successful conversion, the comparators can be connected longer and, while the slope

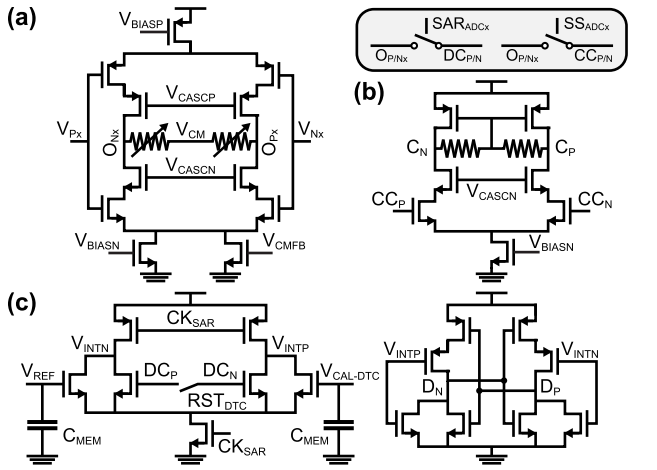

Fig. 8. (a) Schematic of the preamplifier with switches to second stages. (b) Schematic of the continuous-time comparator. (c) Schematic of the DTC.

generator is already shifting to the other converter part, still retrieve the output. To prevent loss of synchronization with the periphery in the case of a fault in SAR residual, a stop signal STP is also issued by ACT_S. This signal can force a stop of slope conversion by setting the SR latch and has a delay designed to be just above the delay of CTC. The following SAR conversion typically does not suffer from an overranging slope conversion as it is timed asynchronously with sufficient margin. The following SS conversion can also still complete successfully as the overranging period would usually fall into the conversion range covering the redundant range.

B. Comparator

Each ADC has its own preamplifier to shield the signal to be quantized from the interference of the switching and operation of the following stages as displayed in Fig. 8(a). An efficient current reuse topology is used and complemented with cascoding transistors to increase the output impedance. Part of the tail current source is split off to enable common-mode regulation of the differential amplifier with a small auxiliary amplifier sensing the output nodes. The structure can be configured to be part of SAR and SS comparison by adjusting the impedance at the output nodes, O_{Px} and O_{Nx}. During slope conversion, a high impedance is set to provide a first gain stage for CTC, while during SAR conversion a low impedance is implemented to enhance the amplifier bandwidth and SAR timing.

A second gain stage is used in the SS phase to amplify small slope residuals to logic levels within the conversion time. The differential amplifier has a passive common-mode feedback architecture and tail cascodes to increase the output impedance as shown in Fig. 8(b). The DTC in Fig. 8(c) is based on [50] and, despite the preamplifier, still uses an additional dynamic preamplifier as the benefit from shielding the continuous preamplifier outputs from kick-back during slope conversion outweighs the added cost. It can, moreover, be used to calibrate the offset of the DTC similar to [51], first-order matching the SAR and SS stage offsets given that the large preamplifier gain during SS conversion significantly reduces the impact of the second stage continuous amplifier offset.

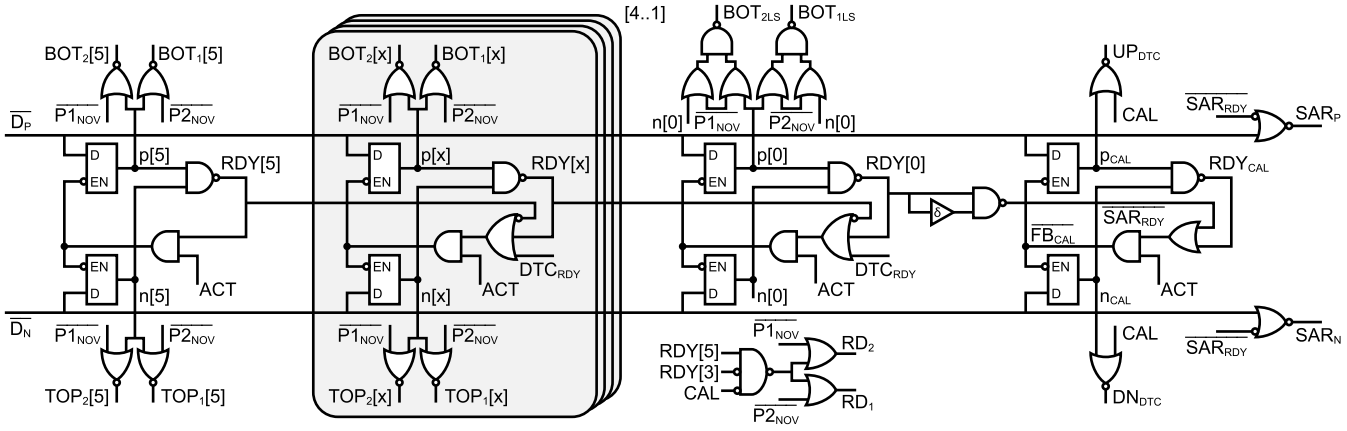

Fig. 9. Asynchronous ADC logic core determining CDAC switching, SAR output code, and DTC calibration.

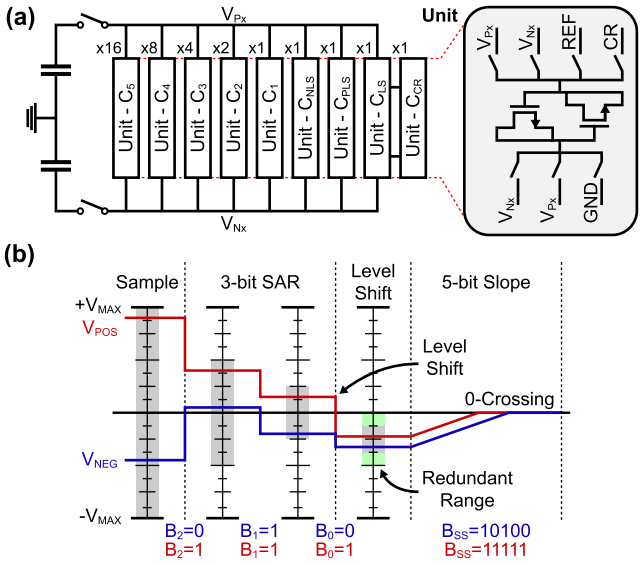

Fig. 10. (a) Overview of SAR DAC with unit cell details. (b) Exemplary conversion diagram showing the residual on sampling capacitors.

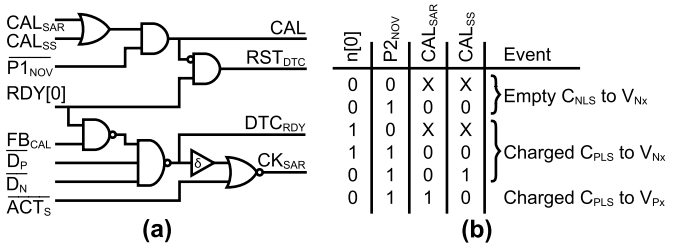

Fig. 11. (a) Asynchronous dynamic comparator clock and reset generator schematics and (b) level shifter state diagram.

C. Logic and CDAC

Fig. 9 shows the logic controlling SAR switching. An overview of CDAC is given in Fig. 10(a), and example conversions of one positive and one negative input are illustrated in Fig. 10(b). DAC has a binary scaled section, $C_{5..1}$, for the 6-bit SAR conversion and is controlled with $\mathrm{TOP_x}$ and $\mathrm{BOT_x}$ to switch the unit to either raise or lower the difference between V_{Px} and V_{Nx}. The structure is laid out symmetrically as multiples of a unit cell to mitigate effects such as mismatch and charge injection. Charge redistribution to create binary charge levels without an exponentially growing CDAC, as in [52], is only applied to generate a level half of C_1. This is used to shift the SAR residual to the middle of the redundant range for slope conversion because matching of that level has less impact on converter linearity. The process is realized by first including C_{CR} during the precharging of CDAC with $\mathrm{Px_{NOV}}$ and then, controlled by $\mathrm{RD_x}$, sharing its charge with the unit used for level-shifting, C_{LS}, through the shared node CR. This is done between the first and third SAR comparison unless SAR or SS calibration is performed. Regardless of the outcome of the last SAR bit, C_{LS} is always switched in to lower the residual with $\mathrm{BOT_{xLS}}$. The last SAR bit decision does, however, influence the switching of the two remaining DAC units, the regularly precharged C_{PLS} and the empty unit C_{NLS}, as shown in Fig. 11(b). In regular operation, C_{PLS} is switched in for a positive SAR residual, effectively mapping it onto the negative range as it is similar to C_1 in charge. C_{NLS}, on the other hand, is switched in with the same polarity but only for negative SAR residuals with the purpose of closer matching of the voltage attenuation posed by CDAC for both the cases. The process is illustrated in Fig. 10(b) and enables the slope to always run in the same direction, reducing the SS complexity.

The SAR logic is based on latches due to their area efficiency and works together with the asynchronous DTC timer in Fig. 11(a). To ensure locking of the result of a DTC decision and settling of CDAC before the next comparison, an additional delay is introduced in the SAR clock generator. To also avoid sampling more than one bit per comparator decision, delay cells could be added between the stages of SAR logic. But in this design, it is instead chosen to lock the stages with $\mathrm{DC_{RDY}}$ to save power and area. To still function well in the case of an overranging SS conversion, the whole latch array is cleared with ACT and the SAR clock $\mathrm{CK_{SAR}}$ is halted by the set active signal $\mathrm{ACT_S}$. This makes sure that there is no switching of CDAC before the correct sample is applied and that new SAR conversion only begins after the correct comparator is switched in.

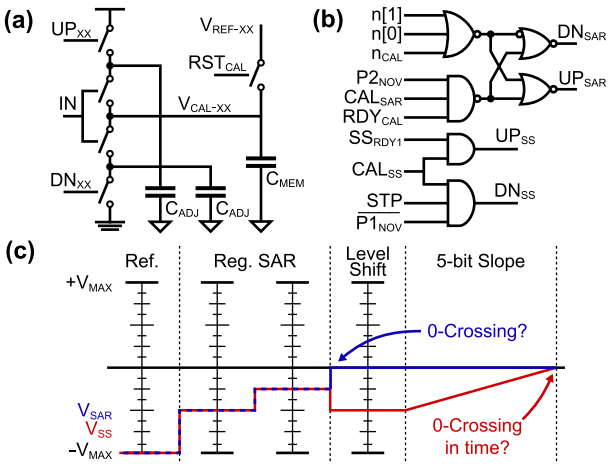

Fig. 12. Conceptual diagram of (a) calibration charge pumps, (b) related SAR and SS controls, and (c) calibration switching overview.

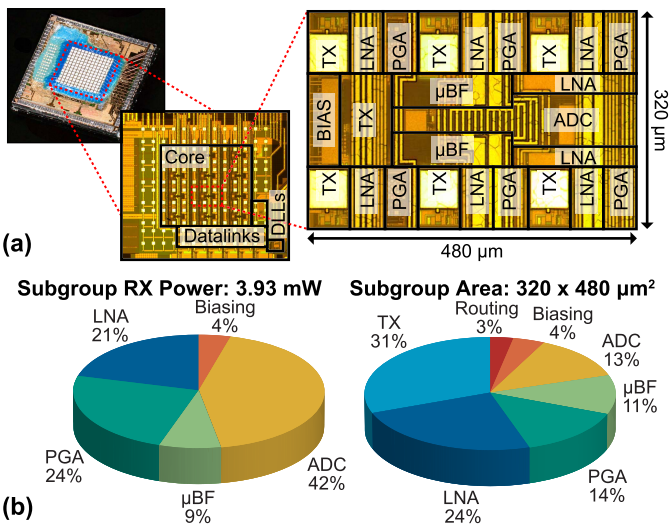

Fig. 13. (a) Micrograph of the chip including transducer matrix array with magnifications of the core and subgroup areas. (b) Distribution of receive power and area per subgroup of 3×2 elements.

D. Calibration

The last stage of the SAR logic is used to calibrate the offset of DTC. After the last SAR comparison, the preamplifier is disconnected and the input of the DTC is shorted together with $\mathrm{RST_{DTC}}$, such that the following comparison samples the polarity of the offset [15]. To optimize precision, the next comparison is not triggered regularly but delayed by halting the seventh $\mathrm{CK_{SAR}}$ pulse of SAR cycle, effectively enhancing settling. This is achieved with a delayed $\mathrm{SAR_{RDY}}$ and $\mathrm{FB_{CAL}}$ signal, as shown in Fig. 9. The sampled offset polarity is then used to switch the control inputs of a regulator for the $V_{\mathrm{CAL\text{-}DTC}}$ node of the DTC, $\mathrm{UP_{DTC}}$ and $\mathrm{DN_{DTC}}$. All the calibration circuits in this design work in a negative feedback loop and with charge pumps as conceptually displayed in Fig. 12(a). The comparator calibration can, except for during SAR or slope calibration, determined with CAL, always run in the background but is not required to complete each conversion cycle. To minimize the chance of losing synchronization with the periphery, and therefore one PE cycle, the calibration step is therefore not required for setting $\mathrm{ADC_{RDY}}$ and is skipped without harming the operation if there is a seventh SAR decision that takes a long time to converge.

The SAR and SS references are additionally calibrated to adjust for interstage gain errors, process mismatch, and temperature variation. The procedure first follows regular SAR operation with a negative full-scale reference input provided through PGA and then makes use of the C_{PLS} DAC unit cell to assess the current status. As listed in Fig. 11(b) and illustrated in Fig. 12(c), it is used to either fully reduce the residual to zero for SAR calibration or, for slope calibration, to get a residual equal to the maximum SS input, including the redundant range. Using the same cell, just with different polarity, enables accurate slope calibration to the maximum SAR residual range irrespective of a preamplifier offset. However, as the offsets of the two preamps can be different, calibration is only obtained with one DAC. The other part of the shared ADC structure still performs DTC offset cancellation in parallel. While this one-sided calibration generally introduces an offset between the two converters due to preamplifier offset differences, there are no implications from DAC mismatch beyond regular linearity investigation and no significant performance difference could be measured between shared structures.

The modified residuals are ultimately used to first adjust the SAR reference, $V_{\mathrm{CAL\text{-}SAR}}$, based on detecting whether there was a zero-crossing in the seventh comparator decision. This is realized by checking the three LSBs of SAR ADC, as shown in Fig. 12(b). The additional delay for improved settling in the seventh comparator cycle is still applied while the comparators are not switched early to ensure the calibration completes. The slope control voltage, $V_{\mathrm{CAL\text{-}SS}}$, on the other hand, is adjusted based on letting the full residual run in a regular SS operation. It is then detected if it was completed early with $\mathrm{SS_{RDY1}}$, or needed to be stopped with STP.

IV. Experimental Results

The reported design has been fabricated in a 0.18-μm HV BCD process with an active area of about 1.8 $\mathrm{mm^2}$ for the 8×9-element core and about 0.8 $\mathrm{mm^2}$ for the periphery circuitry. A chip with a prototype transducer array manufactured on its surface is shown in Fig. 13(a). It measures 5×5 $\mathrm{mm^2}$ to ease the prototype transducer manufacturing and includes two rings of dummy transducers to reduce edge effects of the small array. The array is designed to have a center frequency of 6 MHz and a fractional bandwidth in the order of 50%. A magnification shows the pitch-matched floor plan of a 3×2-element subgroup consisting of element-level pulsers, two 3×1-element subarray beamformers, and two hardware-sharing ADCs. The transmit circuits operate from a 65-V HV supply, a 5-V supply to drive the pulser transistors, and a 1.8-V supply for logic-level control. All receive circuitry is powered from a 1.8-V supply with the addition of a 1.2-V supply for DLL delay cells and a 2.3-V supply for SAR reference. An overview of the area and receive power distribution per subgroup is given in Fig. 13(b). Due to area-intense HV isolation, the pulser circuits (TX) occupy the

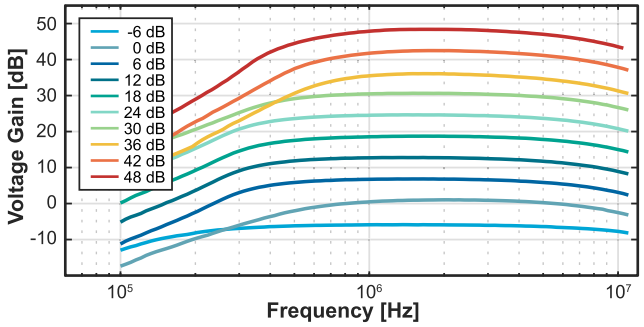

Fig. 14. Receive transfer function measured across frequency for all the gain settings of the analog front-end.

largest part of the subgroup area with 31%, while the hybrid ADCs cover only 13% of the space and consume about as much power as the analog front-end. As the TX operation has a very small duty cycle, the total power consumption is dominated by the receiver, with 0.65 mW/element in the core and 1.23 mW/element including the datalink and LVDS drivers.

Electrical and acoustic experiments have been conducted. The chips are wire-bonded to separate daughter boards, and samples for electrical characterization have additional wire bonds to connect transducer pads to PCB while acoustic samples have a cointegrated transducer array. All the daughter boards are mounted on a common, custom mother board that is connected to a commercial FPGA [53]. The measurements are conducted by observing the ADC outputs as provided through the datalink, received by the FPGA and forwarded to a PC. Characterization of the TX part has previously been shown in [35] and is not covered in this section.

A. Electrical Measurements

The characterization of the receive transfer function shown in Fig. 14 is obtained by providing sinusoidal inputs of varying frequencies to the transducer pads from a waveform generator and referring the ADC output to the output of AFE. The circuit shows the expected mid-band gain range of 54 dB in ten steps from −6 to 48 dB with an 8.1-MHz cut-off frequency in the highest gain setting. The difference among the gain steps in low-frequency roll-off is caused by the feedback configuration and does not affect the imaging as the output is filtered around the center frequency of the transducer. Fig. 15(b) shows the time-domain recording of an ADC output code with an exponentially decaying 6-MHz sinusoidal signal provided at the input of the analog front-end. By switching through the ten gain settings of the analog front-end, the output amplitude can be kept within the observable range, verifying functional time-gain compensation within one receive period, with a small settling time after gain switching. Combined with the ability to operate at the intended PRF of 7.7 kHz, corresponding to a pulse repetition interval (PRI) of 130 μs, as demonstrated in Fig. 15(a), this verifies that the chip enables recording of the full imaging depth at the targeted frame rate.

The peak ADC output power spectral density is shown in Fig. 16, measured with a 5.95-MHz sinusoidal signal from

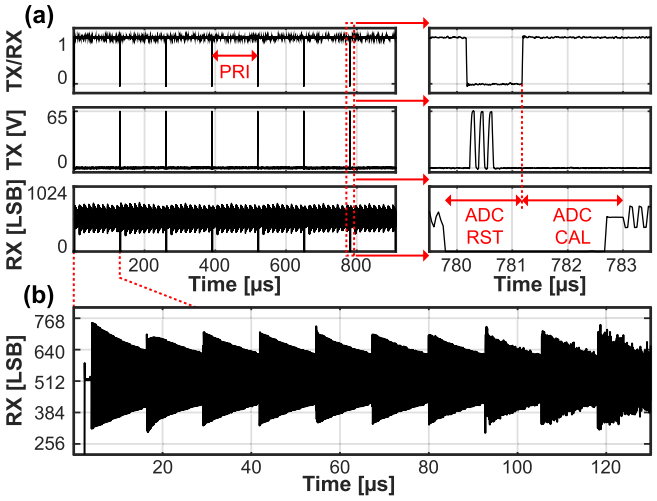

Fig. 15. (a) TX/RX control, TX voltage, and RX output code recorded with the intended PRI, with zoom-in of the switching period. (b) Recording of one RX output with an exponentially decaying sinusoidal signal at the analog front-end input and active time gain compensation.

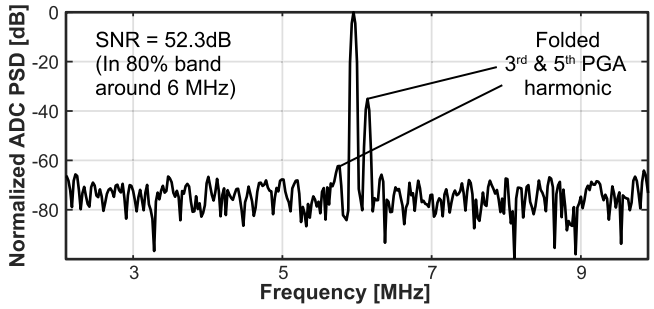

Fig. 16. Power spectral density plot showing the peak SNR of the entire receive signal path with a 5.95-MHz sinusoidal input to the analog front-end.

a waveform generator. As the waveform is provided at the analog front-end input, the whole receive path is characterized to a peak SNR of 52.3 dB, with a folded −35-dB third harmonic and −62-dB fifth harmonic from the PGA output stage in an 80% bandwidth around the transducer center frequency.

A test mode in which the ADC output of one channel can be read without recombination of the SAR and slope output data is used to follow the ADC calibration procedures. The global starting potentials for SAR and slope reference can be individually set in a reset state and are prior to this test placed away from the final settling points. Fig. 17(a) shows how the SAR and slope local calibration nodes converge to the final values at the example of the bottom-right and bottom-left output codes of the SAR and slope stage. The SAR algorithm tries to fully reduce a full-scale input, leading to a settled value at an output code of zero. The slope algorithm, on the other hand, adjusts the slope current to detect the zero-crossing of a full-scale slope stage input just at the end of the associated time interval and therefore settles around the maximum slope output code. An overview of the combined SAR and slope calibration time until a settled state is reached from the same starting point is shown per shared ADC structure in Fig. 17(b), giving an indication of the channel-to-channel mismatch.

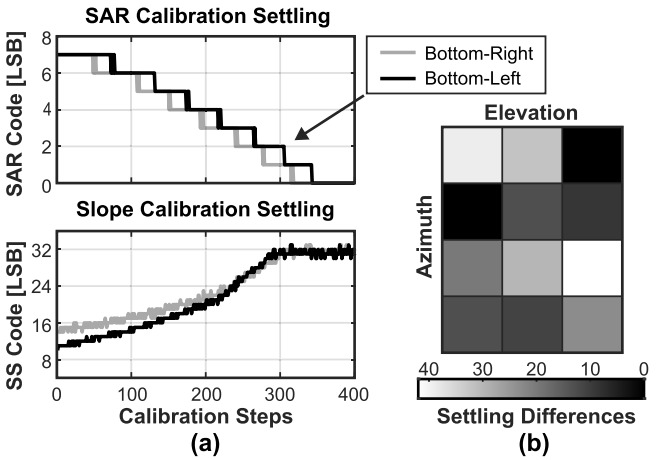

Fig. 17. (a) Example of the SAR and SS calibration procedures of two different ADCs. (b) Heatmap showing the relative difference in the total calibration settling time from a common starting point across ASIC.

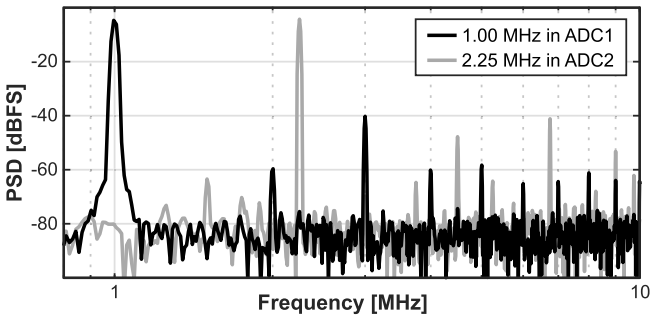

Fig. 18. Interference test showing the power spectral densities of both the outputs of one shared ADC structure with concurrent 1-MHz and 2.25-MHz inputs.

To investigate how the high integration density and hardware-sharing within each subgroup and at the periphery affect the crosstalk between channels, an electrical measurement, studying the outputs of the two cointegrated subgroup ADCs, is performed. Their inputs can be accessed separately and are concurrently driven by two outputs of a waveform generator, in this example at 1.00 and 2.25 MHz. The corresponding output spectra of the two ADCs are both plotted in Fig. 18 and show no significant tones at the fundamental or harmonic frequencies of the other channel. This implies that a circuit crosstalk better than −75 dBc is achieved and that other sources such as mechanical crosstalk in the transducer array should be dominant.

Table I summarizes the performance of the hybrid ADC and gives a comparison to the state-of-the-art. In contrast to general-purpose converters, this design implements several application-oriented features such as direct integration with a subarray beamformer, allowing for a low-bandwidth ADC driver and including a low-bandwidth SAR reference. Therefore, Table I shows comparison of the design with prior ADC designs targeting miniature ultrasound probes. Set against the most comparable design [15], the ADC occupies more than 4x less area and consumes more than 1.5x less power. Even in comparison to the more general designs [32], [33], the efficient architecture enables the lowest reported area and power consumption.

TABLE I
PRIOR ART COMPARISON IN MINIATURE ULTRASOUND PROBE ADCS

	This Work	JSSC'21 [32]	VLSI'19 [33]	JSSC'18 [15]
Architecture	**SAR & SS**	SAR	SAR & SS	SAR
Resolution	**10 bit**	10 bit	10 bit	10 bit
Sample Rate	**24 MHz**	20 MHz	30 MHz	30 MHz
Low BW Driver	✓	×	×	✓
Reference Included	✓	×	×	✓
Area *	**0.010 mm²**	0.026 mm²	0.013 mm²	0.046 mm²
Power *	**0.82 mW**	1.23 mW	1.14 mW	1.42 mW

* Per Subarray

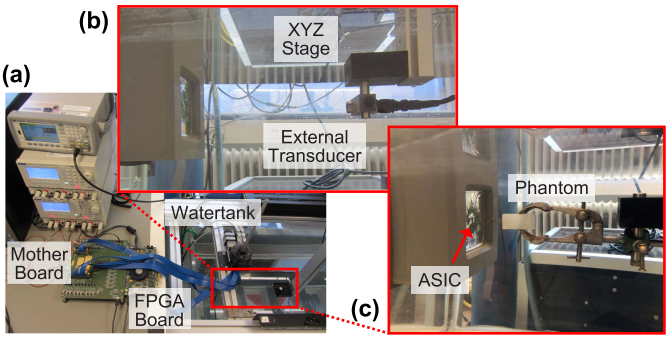

Fig. 19. (a) Overview of the acoustic measurement setup. (b) Inset showing watertank with external transducer. (c) Imaging experiment details.

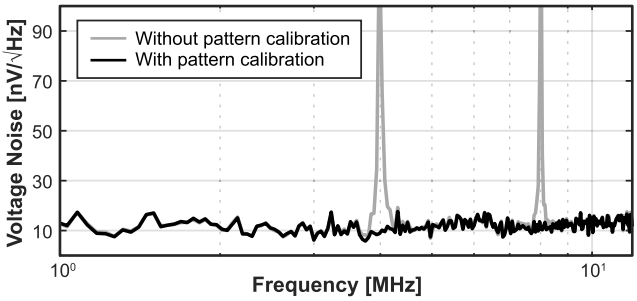

Fig. 20. Input-referred spectral voltage noise density with and without calibration of the static mismatch pattern of the subarray beamformer.

B. Acoustic Measurements

An overview of the acoustic measurement setup is given in Fig. 19(a). All the acoustic measurements are obtained with the daughter board and ASIC with the transducer array directly interfacing with a watertank. Fig. 20 shows the input-referred voltage noise spectral density in the highest gain setting with the transducer elements loaded by water. Two tones appear in the spectrum at $f_s/6$ and its second harmonic, f_s, being the sampling frequency of the ADC. These are generated by mismatch of the subarray beamforming cells and can be removed by recording and subtracting the static pattern as shown. The input-referred voltage noise density is 12.7 nV/$\sqrt{}$Hz at 6 MHz, around 5 nV/$\sqrt{}$Hz higher than what the electronics are designed for, with the difference being attributed to the thermal noise of the transducer.

Fig. 21 displays a sweep of the transducer surface peak pressure with measured ADC output for all gain settings, used

TABLE II
COMPARISON WITH THE PRIOR ART IN CATHETER-BASED ULTRASOUND IMAGERS

	This Work	JSSC'21 [32]	JSSC'20 [40]	VLSI'19 [33]	JSSC'18 [15]	TUFFC'16 [6]
Technology	**180 nm BCD**	180 nm	180 nm BCD	180 nm	180 nm	N/A
Transducer	**2D PZT**	2D PMUT	1D CMUT	2D PZT	2D PZT	2D PZT
Array Size	**8 × 9**	6 × 6	64	4 × 4	6 × 24	60 × 14
Integrated transducer	✓	✗*	✓	✓	✓	✓
Center Frequency	**6 MHz**	5 MHz	7 MHz	5 MHz	5 MHz	5.6 MHz
Pitch-matched	✓	✗†	✓	✓	✓	✓
Element Pitch	**160 µm × 160 µm**	250 µm × 250 µm	205 µm × 1800 µm	150 µm × 150 µm	150 µm × 150 µm	110 µm × 180 µm
Integrated TX	✓	✓	✓	✗	✗	✓
Max. TX Voltage	**65 V**	13.2 V	60 V	N/A	N/A	40 V
Digitization	✓	✓	✗	✓	✓	✗
RX architecture	**AFE + µBF + ADC + Datalink**	AFE + ADC	AFE	AFE + ADC	AFE + µBF + ADC + Datalink	AFE + µBF
Channel Reduction	**12-fold**	N/A	N/A	N/A	36-fold	15- to 20-fold
Supported Frame Rate	**1000 vol/s**	N/A	N/A	N/A	200 vol/s	50 vol/s
Active Area / El.	**0.032 mm² §**	0.063 mm²	0.464 mm²	0.023 mm²	0.026 mm² §	N/A
RX power / El.	**1.23 mW §**	1.14 mW	5.2 mW	1.54 mW	0.91 mW §	< 0.12 mW
Input DR	**91 dB**	N/A	82 dB	N/A	85 dB	N/A
Peak SNR	**52.3 dB**	57.8 dB ‡	N/A	49.8 dB	52.8 dB	N/A

* Transducers on separate board connected with wires.
† Scalability limited by transducer connection outside of pitch.
§ Including the Datalink and LVDS drivers.
‡ ADC only, excluding AFE.

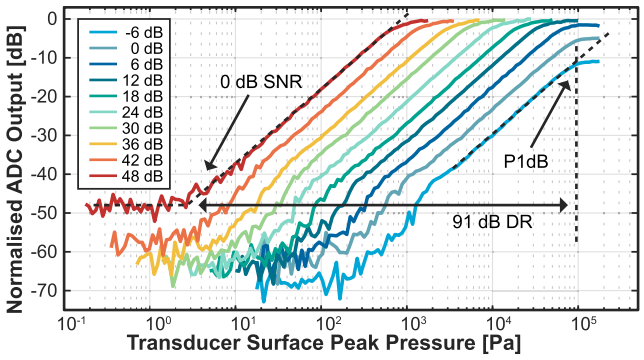

Fig. 21. ADC output measured during sweep of the transducer surface pressure in all gain settings, showing a 91-dB DR.

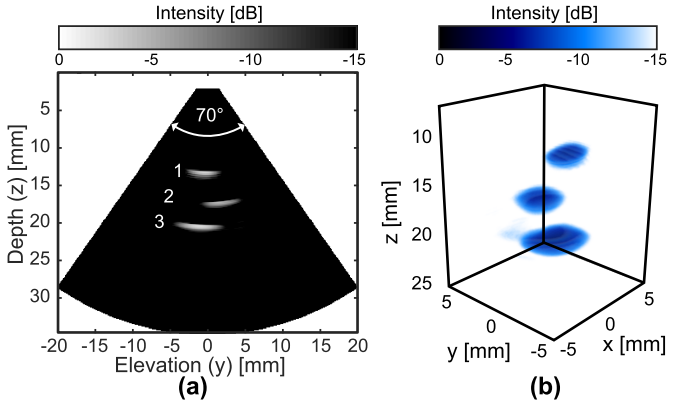

Fig. 22. (a) Elevation plane image of the three-needle phantom recorded at 1000 volumes/s with the prototype. (b) Rendered 3-D image of the same recording.

to characterize the DR of the receive path. The pressure waves are generated from an external commercial transducer [54] connected to a waveform generator that transmits sinusoidal waves at 5.5 MHz as shown in Fig. 19(b). The displayed surface pressure is calibrated with a commercial hydrophone [55] with known sensitivity in the place of ASIC before the measurement. A total DR of 91 dB is recorded between the 0-dB SNR point of the highest and the 1-dB compression point of the lowest gain setting.

An overview of the measurement setup used for imaging experiments is given in Fig. 19(c). A phantom of three needles with a total spacing of 7 mm is immersed in a watertank about 13 mm from an acoustic window used to interface with a daughter board carrying a chip with cointegrated transducers. Cables with a length of 1 m connect the PCB assembly to an FPGA board that receives the high-bandwidth LVDS data via a motherboard and forward it to a measurement PC that performs the image reconstruction based on conventional delay-and-sum operations. In seven transmit/receive cycles, the ASIC first excites 6-MHz pressure waves with 65-V pulses and then records generated echoes from the phantom with the seven subarray beamformer settings. Fig. 22 shows the resulting image once in an elevation plane in a) and once as a rendered 3-D image in b). While the aperture is too small to provide the resolution of a full array, the needle heads can clearly be distinguished in 3-D space, demonstrating the functionality of the prototype.

A summary of the system characteristics and comparison to the prior art in catheter-based ultrasound systems [6], [15], [32], [33], [40] is provided in Table II. This work describes the first design to integrate element-level HV transmitters and analog front-ends, subarray beamforming, and in-probe digitization in a scalable fashion for 3-D imaging. A dedicated architecture enables the highest reported frame rate with a channel count reduction sufficient to enable an array with less

than 100 data channels in the catheter when scaled to full size.

V. Conclusion

A transceiver ASIC combining HV transmission with subarray beamforming and in-probe digitization for catheter-based 3-D ultrasound probes has been presented. A pitch-matched design is facilitated by an area- and power-efficient hybrid beamforming ADC tailored to the application in large imaging arrays. The novel architecture enables a high frame rate of 1000 volumes/s while also providing sufficient data channel reduction through subarray beamforming and time-division multiplexing. A prototype with a cointegrated transducer matrix has been manufactured and successfully applied in a 3-D imaging experiment. Together with competitive power consumption and large DR, the system is a promising solution for future miniature ultrasound probes.

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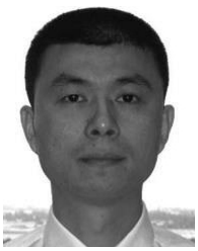

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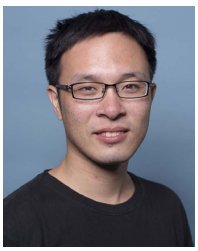

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