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DOI
10.1109/JESTPE.2020.3043018

Publication date
2021

Document Version
Final published version

Published in
IEEE Journal of Emerging and Selected Topics in Power Electronics

Citation (APA)
Wang, J., Liu, X., Peng, Q., Xun, Y., Yu, S., Jiang, N., Wang, W., & Hou, F. (2021). Co-Reduction of Common Mode Noise and Loop Current of Three-Level Active Neutral Point Clamped Inverters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *9*(1), 1088-1103. Article 9285288. https://doi.org/10.1109/JESTPE.2020.3043018

Co-Reduction of Common Mode Noise and Loop Current of Three-Level Active Neutral Point Clamped Inverters

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***Abstract*— The increased switching frequency and speed of silicon carbide (SiC) MOSFETs lead to higher power density of inverters, but meanwhile resulting in weak electromagnetic interference (EMI). The impedance balance technique is a good way to reduce the common mode (CM) noise by making the voltage across the line impedance stabilization network (LISN) as small as possible. However, a side effect of this technique is the generation of relatively large loop current that circulates in the inverter. It can cause additional losses and cost, which can be a factor that stops the increase of the switching frequency by SiC MOSFET. This article, for the first time, analyzes the relationship between the CM noise and loop current of the three-level active neutral point clamped (ANPC) inverter, and proposes a co-reduction method for both. First, the CM noise and loop current are clarified for the ANPC inverter, and the analytical models for both are established. The conflict between the CM noise and loop current is introduced with a specific case by the existing design method. Then a co-reduction method is proposed and elaborated, which can both suppress the CM noise and the loop current. The extra cost and volume by the proposed method are also analyzed and are negligible. The design guideline is further shown for clarity. Finally, the analysis and proposed method is validated by the experiment.**

***Index Terms*— Active neutral point clamped (ANPC), co-reduction method, common mode (CM) noise, electromagnetic interference (EMI).**

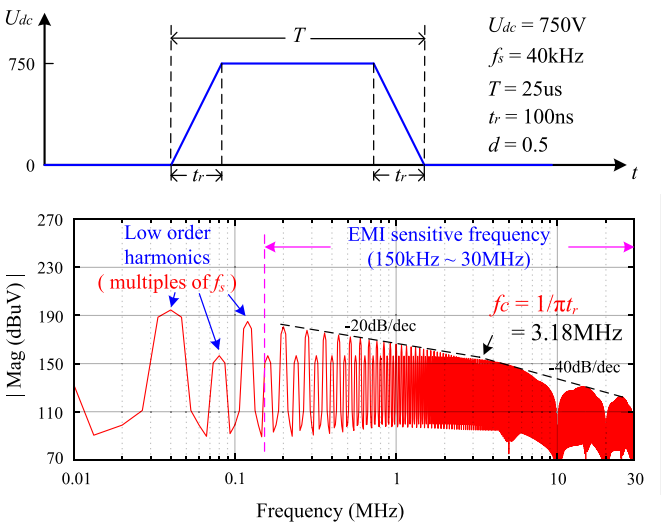

Fig. 1. Trapezoidal spectrum with U_{dc} = 750 V, f_s = 40 kHz, T = 25 μs, t_r = 100 ns, and d = 0.5.

I. Introduction

THE three-level active neutral point clamped (3L-ANPC) inverter is widely used in the medium and high power applications in recent years [1]–[3]. It is derived from neutral point clamped (NPC) topology that by replacing the clamping diodes with two active switches that can actively distribute the loss evenly on each semiconductor [4], [5]. However, the power density of inverter is difficult to be further improved due to the limitation of switching frequency of silicon (Si) devices. With the emergence of silicon carbide (SiC), this issue can be solved. The higher switching frequency capability and junction temperature tolerance of SiC devices make the switching frequency of inverter potentially increase by a magnitude [6]–[8]. But the price of SiC devices is twice more than that of Si devices. To achieve significant performance improvement at low cost, a 4-Si/2-SiC hybrid 3L-ANPC topology is proposed. The dedicated modulation strategy makes the SiC devices operate with high frequency and the Si device operates with low frequency [9], [10].

With the excellent performance of SiC devices, some risks are emerging. One of the most obvious problems is the deterioration of electromagnetic interference (EMI) [11]–[13]. Fig. 1 shows a simulated spectrum of symmetrical trapezoidal pulse

Manuscript received July 19, 2020; revised October 27, 2020; accepted November 30, 2020. Date of publication December 7, 2020; date of current version January 20, 2021. This work was supported by grants from the Power Electronics Science and Education Development Program of Delta Group, Institute of Energy, Hefei Comprehensive National Science Center under Grant 19KZS207, in part by the Key-Area Research and Development Program of Guangdong Province under Grant 2019B010128002, and in part by 111 Project under Grant BP0719039. Recommended for publication by Associate Editor Yam Siwakoti. *(Corresponding author: Shaolin Yu.)*

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Digital Object Identifier 10.1109/JESTPE.2020.3043018

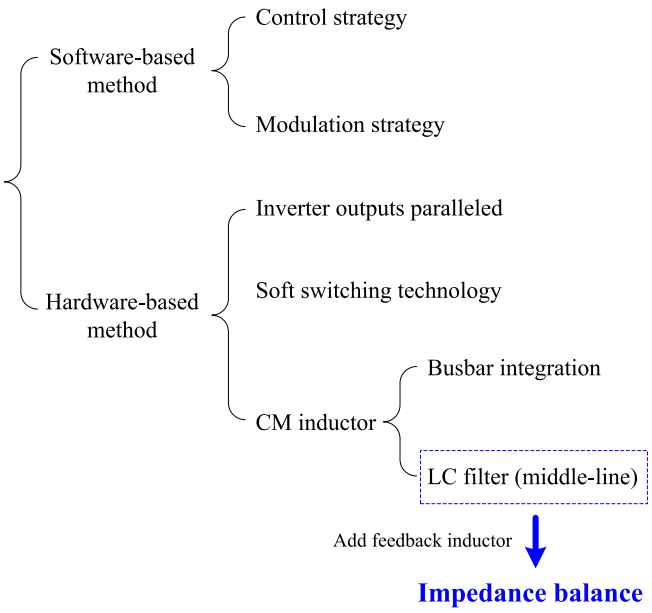


Fig. 2. Summary of CM noise suppression methods.

with dc voltage $U_{\rm dc} = 750$ V, duty cycle $d = 0.5$, switching frequency $f_s = 40$ kHz, rise and fall time $t_r = 100$ ns. First, when the switching frequency increases, the low-order harmonics become close to or even enter the frequency range (150 kHz–30 MHz) that is concerned by the conducted EMI. Second, the high $\mathrm{d}v/\mathrm{d}t$ of the pulse can increase the magnitude of high-frequency range beyond the corner frequency between the envelopes with -20 and -40 dB/dec attenuation rate [14], [15]. These issues can increase the magnitude of the noise and intent to break the limitation of standards, such as NB/T 32004-2018 [16].

Common-mode (CM) EMI is an important type of the conducted EMI, which is influenced by the CM noise and the network of the inverter system. CM EMI can cause a series of damage to the system, such as the malfunction of a residual current breaker [17], thus it should be strictly limited according to some standards. To well design a CM filter, the CM model of the inverter should be established, including the noise source and the network. Wang *et al.* [18] address the CM model of the 3L-ANPC with key parasitics and can be directly used in this article.

To well suppress the CM noise, many suppression methods are proposed. These methods can be simply divided into two categories, as shown in Fig. 2. The first is the software-based method, which modifies the modulated pulses by changing the control or modulation strategy to reduce the system CM voltage. Guo *et al.* [19] and Liu *et al.* [20] measure the CM current in real time and feed it back to the control loop, then change the gate control strategy to suppress the CM voltage. This method is useful but makes the control complex and requires additional sensors. References [21]–[25] suppress the CM voltage by selecting appropriate modulation vectors and changing their distributions in switching periods. However, this method will worsen the total harmonic distortion (THD) of the output currents. The second is the hardware-based method, which usually improves the circuit network to suppress the response CM current. Some researchers connect the outputs of two inverters in parallel to make that the CM voltage can cancel each other [26], [27]. However, it is not suitable for single inverter. Charalambous *et al.* [14] use the soft switching technique to smooth the square waveform to reduce the high-frequency noise. But this technique needs too many auxiliary devices. In [28]–[33], a CM inductor is added to the ac or dc side of the inverter to attenuate the CM noise current. This is a convenient and effective method, but the CM inductor will be very large if a significant suppression is required. The large CM inductor intends the notable increase of volume and cost. Some researchers expect to integrate CM inductors with busbars, but the busbar is difficult to be used to realize an inductor with multiturns; thus, the inductance is usually small with tens of nH [33]. Connecting the middle point of the capacitors of ac output filter back to dc side or heatsink, which is called the middle line, a *LC* filter is formed by the CM inductor and the filter capacitors [29]–[32]. It has stronger attenuation ability than the filter only with an inductor. However, this method does not consider the influence of the switch parasitics. The low impedance of parasitic capacitance in high frequency will break the topology of the filter, making its suppression effect very poor. For further improvement, references [18] and [34]–[36] propose a balance method by adding a small feedback inductor to the middle line; the CM EMI can be suppressed more effectively when the feedback inductor meets the design guidelines.

Impedance balance method do not require any software modification, and can well suppress the CM noise with a small extra cost. However, this method only focuses on the reduction of CM noise, but causes another important problem. Fig. 3 shows the topology of three-phase 3L-ANPC inverter with impedance balance technique. Comparing to the system without the middle line, the adding of the middle line largely reduces the total CM impedance by paralleling an impedance branch to the original system. Resultantly, there can be a large loop current $i_{\rm LOOP}$ that flows out of the phase nodes A, B, C and circulates back through parasitic capacitances, the middle line, and the ground resistance R_g, which brings extra losses, neural point voltage shift, device current stress rise, and so on [37], [38]. The negative impact of large $i_{\rm LOOP}$ can offset the improvement of efficiency and power density brought by SiC devices, which is the main reason to use SiC devices. Thus, it can become a key obstacle to the further wide application of SiC. How to effectively reduce the CM noise and the loop current at the same time is the topic that this article needs to discuss.

In this article, the models of CM noise and loop current are established and their expressions are derived first. Second, the conflict between the CM noise and the loop current is introduced with a specific case. Third, the co-reduction method is proposed. Then, the volume and cost of the co-reduction method is discussed. Furthermore, the guidelines of co-reduction method are given. Finally, the simulation and experiment are used to verify the above theory.

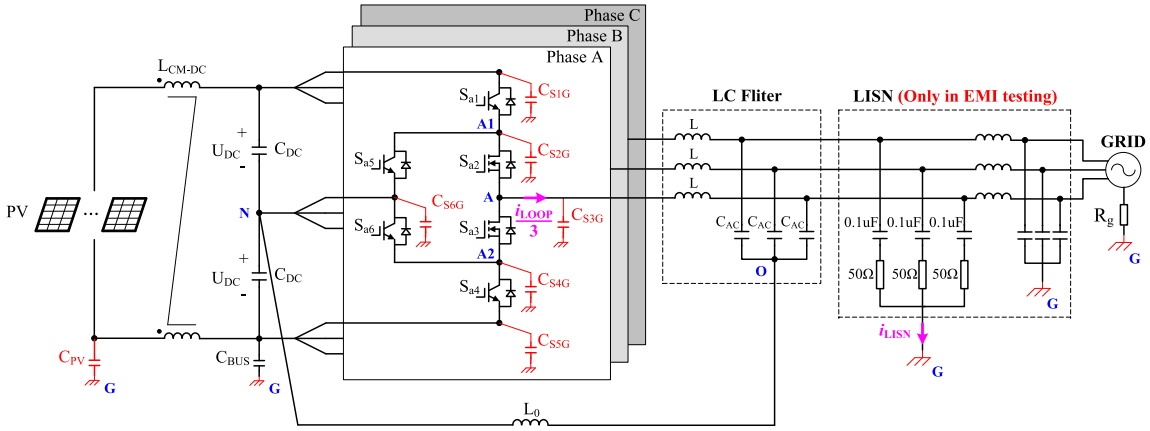


Fig. 3. Three-phase 3L-ANPC PV inverter with impedance balance technique.

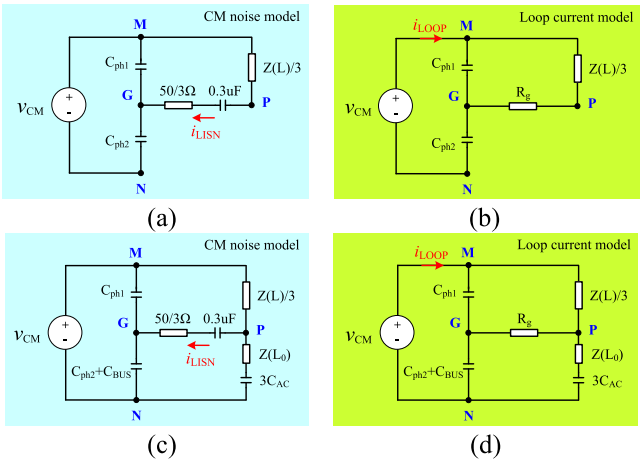


Fig. 4. Models of 3P-3L-ANPC. (a) CM noise model of original circuit. (b) Loop current model of original circuit. (c) CM noise model of balanced circuit. (d) Loop current model of balanced circuit.

II. Modeling of the CM Noise and Loop Current

A. Models of the CM Noise and Loop Current

First, the Si/SiC hybrid three-phase 3L-ANPC topology shown in Fig. 3 is briefly introduced here. Phase A, S_{a2}, and S_{a3} are SiC switches that operate in high frequency and the others are Si switches that operate in low frequency. C_{S1G}–C_{S6G} are the parasitic capacitances between the switches and the ground. Phase B and phase C are the same as phase A. C_{dc} is the dc capacitor that is usually more than 1 mF. The parasitic inductance of C_{dc} can be very low because C_{dc} is composed of many film capacitors with low ESL in parallel. The *LC* filter consists of inductors L and capacitors C_{ac}. Photovoltaic (PV) panels with total parasitic capacitance C_{PV} are connect to the dc side of the inverter, and a CM inductor L_{CM-dc} is placed between them to eliminate the influence of uncertain C_{PV} on the balance [18]. The ac side of inverter is connected to the grid and the grid ground resistance is marked as R_g. A line impedance stabilization network (LISN) that satisfies GB/T 6113.102-2018/CISPR 16-1-2:2014 [39] is placed between *LC* filter and grid when the inverter is in EMI testing.

Second, the CM noise model and loop current model should be discussed. The CM noise modeling has already been done in [18] and is simply reviewed here. The models are shown in Fig. 4(a) and (c). C_{ph1} and C_{ph2} are composed of C_{S1G}–C_{S6G}, and their expressions are shown in (1) and (2). C_{BUS} is a nanofarad-level capacitance that is added between bus and ground to adjust the impedance balance of the system, and its CM model is in parallel with C_{ph2}. The branch consists of L_{CM-dc} and C_{PV}, which can be ignored because its impedance is much larger than that of $C_{ph2} + C_{BUS}$ in high frequency. Three identical inductors L can be regarded as parallel in the CM noise model and their total impedance can be expressed as $Z(L)/3$, where $Z(L)$ is equal to ωL. The LISN is simplified as a series branch of 50 Ω/3 resistance and 0.3-μF capacitance, and the current flowing through the resistance can be called CM noise current i_{LISN}

$$C_{ph1} = 3C_{S3G} \tag{1}$$

$$C_{ph2} = 3(C_{S1G} + C_{S2G} + C_{S4G} + C_{S5G} + C_{S6G}). \tag{2}$$

The CM noise source v_{CM} is expressed as

$$v_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3}. \tag{3}$$

When the middle line and feedback inductor L_0 is added, the branch consists of $Z(L_0)$ and $3C_{ac}$ is connected between points P and N that is shown in Fig. 4(c). Obviously, the network is converted into a Wheatstone bridge and i_{LISN} can be eliminated when the L_0 satisfies the following equation that is called impedance balance:

$$Z(L_0) = \frac{C_{ph1}}{C_{ph2} + C_{BUS}} \times \frac{Z(L)}{3}. \tag{4}$$

The difference between loop current model and CM noise model is that the branch GP in loop current model only consists of R_g, as shown in Fig. 4(b) and (d). This is because the inverter is directly connected to the grid while in practical process, so only R_g needs to be considered. The loop current discussed in this article is i_{LOOP} that is marked in red in Fig. 4(d).

Here, the influence of middle line and feedback inductor (branch PN) on loop current is analyzed from the model.

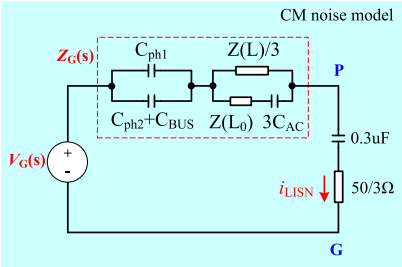


Fig. 5. Thevenin circuit of CM noise model in Fig. 4(c).

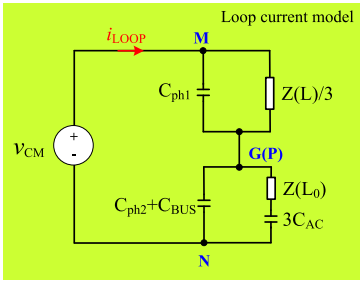


Fig. 6. Simplified model of loop current mode in Fig. 4(d).

It is obvious that the impedance of branch PN reduces the impedance of branch MN and increases the i_{LOOP}. On the one hand, the connection of the branch PN can eliminate the CM noise i_{LISN}, but on the other hand, it causes larger loop current to the system, which is a side effect of this technique. As a result, a co-reduction of both CM noise and loop current is very important for the potential high-frequency application of SiC devices.

Third, the expressions of CM noise and loop current are derived. The Thevenin circuit of the CM noise model is shown in Fig. 5. Parameters V_{G} and Z_{G} can be expressed as follows:

$$V_{\mathrm{G}}(s)=\left[\frac{Z(L_0)+1/(3sC_{\mathrm{ac}})}{Z(L_0)+1/(3sC_{\mathrm{ac}})+Z(L)/3}-\frac{C_{\mathrm{ph1}}}{C_{\mathrm{ph1}}+C_{\mathrm{ph2}}+C_{\mathrm{BUS}}}\right]\times V_{\mathrm{CM}}(s) \tag{5}$$

$$Z_{\mathrm{G}}(s)=\frac{1}{s\left(C_{\mathrm{ph1}}+C_{\mathrm{ph2}}+C_{\mathrm{BUS}}\right)}+\frac{[Z(L_0)+1/(3sC_{\mathrm{ac}})]\times Z(L)/3}{Z(L_0)+1/(3sC_{\mathrm{ac}})+Z(L)/3}. \tag{6}$$

Then the CM noise $I_{\mathrm{LISN}}(s)$ can be expressed as follows:

$$I_{\mathrm{LISN}}(s)=\frac{V_{\mathrm{G}}(s)}{Z_{\mathrm{G}}(s)+1/(s\times 0.3\ \mu\mathrm{F})+50/3}=G_{\mathrm{LISN}}(s)\times V_{\mathrm{CM}}(s). \tag{7}$$

When the bridge is in balance, the voltage between points P and N is 0 and then the R_g can be regarded as short circuit in the loop current model. But in practical implementation, the bridge cannot be in perfect balance due to the nonideal components. A slight imbalance will not lead to much error in this simplification because R_g is usually much smaller than the impedance of other branches. Based on these conditions, the loop current model can be simplified as Fig. 6. The

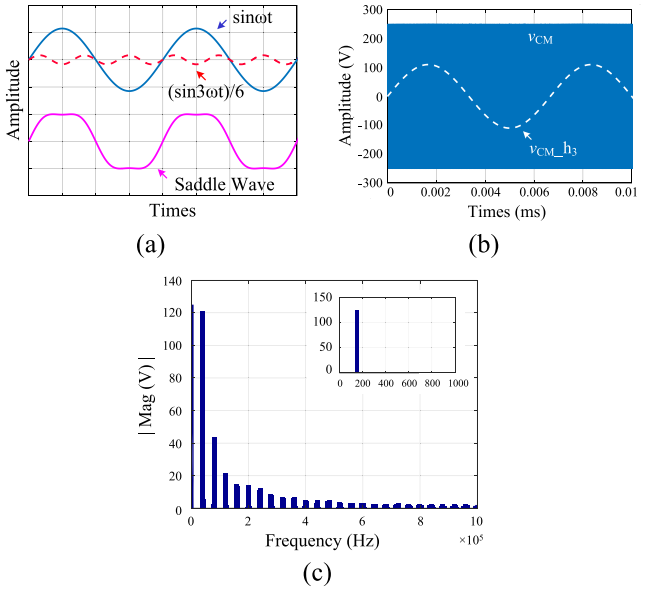


Fig. 7. (a) THIPWM6 modulation. (b) Simulated CM noise source v_{CM}. (c) Specturm of the simulated CM noise source v_{CM}.

expression of i_{LOOP} is

$$I_{\mathrm{LOOP}}(s)=\frac{V_{\mathrm{CM}}(s)}{\frac{Z(L)/3}{1+s\left(C_{\mathrm{ph1}}\right)\times Z(L)/3}+\frac{Z(L_0)+1/(3sC_{\mathrm{ac}})}{1+s\left(C_{\mathrm{ph2}}+C_{\mathrm{BUS}}\right)\times[Z(L_0)+1/(3sC_{\mathrm{ac}})]}}=G_{\mathrm{LOOP}}(s)\times V_{\mathrm{CM}}(s). \tag{8}$$

To evaluate the effect of loop current on the loss, the expression of root mean square (rms) of i_{LOOP} is given [31]

$$i_{\mathrm{LOOP\text{-}RMS}}=\frac{\sqrt{2}}{2}\sqrt{\sum_{n=0}^{N}|I_{\mathrm{LOOP}}(f=2\pi n\times 50)|^2}. \tag{9}$$

From (5)–(9), it can be seen that the i_{LISN} and i_{LOOP} are determined by v_{CM}, G_{LISN}, and G_{LOOP} at the same time. Before discussing the admittance G_{LISN} and G_{LOOP} of inverter, the v_{CM} should be modeled.

B. Modeling of the Noise Source v_{CM}

The CM noise source v_{CM} is closely related to the modulation strategy of the inverter. The common modulation method THIPWM6 is applied in the inverter, which can extend the maximum linearity by 15.47% and reduce the THD in the output by injecting a 150-Hz reference with one-sixth amplitude into the 50-Hz sinusoidal modulated wave [40]–[42]. The THIPWM6 modulation and simulated CM noise source v_{CM} are shown in Fig. 7(a) and (b). Due to the injection of third harmonic, a 150-Hz harmonic component named $v_{\mathrm{CM\_h3}}$ will be reflected in the CM voltage.

The fast Fourier transform (FFT) result of v_{CM} is shown in Fig. 7(c). It consists of two parts, as shown in Fig. 8. One part includes low-frequency harmonics, which are mainly the 150-Hz harmonic and its side bands. The other part includes high-frequency harmonics, which mainly are the integral multiples of 40 kHz and their side bands. If the input voltage and modulation strategy are unchanged, the harmonics of the v_{CM}

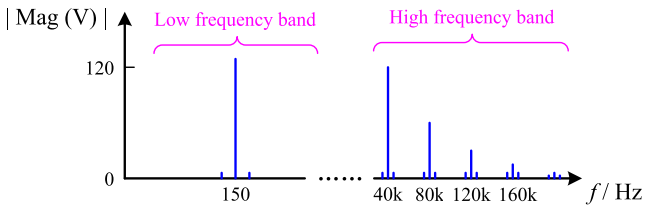


Fig. 8. Distribution of harmonics of CM noise source in the frequency band.

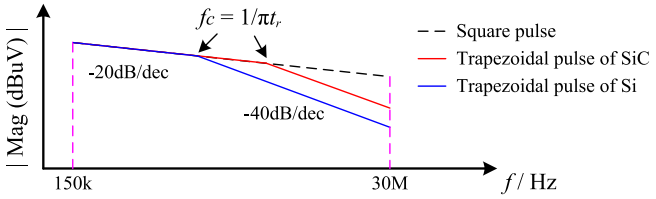


Fig. 9. Envelopes of the spectra of square pulse and trapezpidal pulse of Si and SiC [14].

TABLE I
KEY PARAMETERS OF THE 3P-3L-ANPC INVERTER

$2U_{DC}$	1500 V	L	90 uH
P	140 kW	C_{AC}	3 uF
f_s	40 kHz	R_g	2 Ω
t_r	100 ns	C_{BUS}	7.9 nF

are nearly invariant under different output power levels except for the fundamental component.

In addition, the effect of dv/dt is also noteworthy. The dv/dt is determined by two elements: the magnitude and the rise or fall time. The magnitude influences the amplitude of the FFT result, and the rise/fall time influences the initial frequency f_c of −40-dB/dec attention. The application of SiC devices does not change the voltage magnitude, but only reduce the rise/fall time t_r to less than 100 ns. According to the expression $f_c = 1/(\pi * t_r)$, f_c increases to more than 3 MHz, as shown in Fig. 9. It is obvious that the CM voltage spectrum increases in the high-frequency band. Thus, the CM noise in high-frequency range increases as dv/dt increases. However, the loop current depends on the summation of all the harmonics. The magnitude of the harmonics with frequency beyond f_c is quite low compared to that of low-frequency harmonics. Accordingly, the high dv/dt has small influence on the loop current.

III. CONFLICT BETWEEN THE CM NOISE AND LOOP CURRENT

In this section, the conflict between CM noise and loop current is introduced by a practical ANPC case. The system parameters are shown in Table I. The input voltage $2U_{dc}$ is 1500-V dc and the power is 140 kW. The switching frequency f_s is set to 40 kHz. The inductor L and capacitor C_{ac} are designed as 90 and 5 μF, respectively, according to [43] and

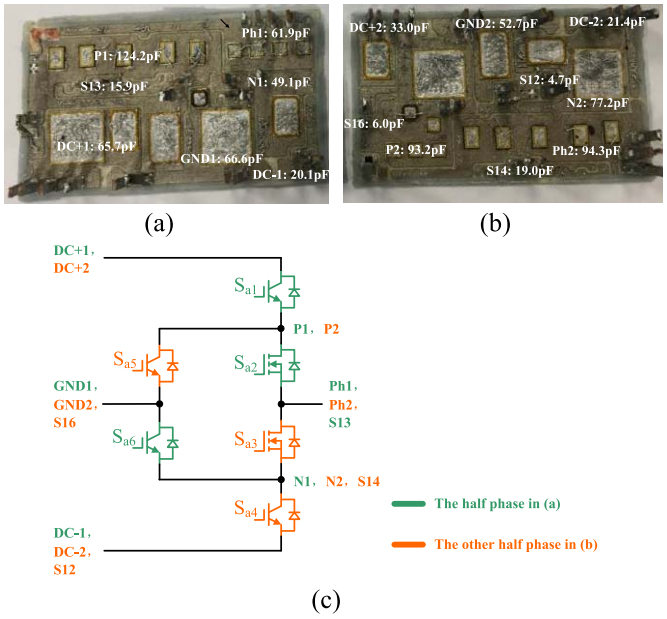


Fig. 10. Measured parasitic capacitances. (a) Parasitics of the module for half phase. (b) Parasitics of the module for the other half. (c) Labels of the conductive layers in the bridge.

TABLE II
PARASITIC CAPACITANCES FOR SINGLE PHASE

Symbol	C_{S1G}	C_{S2G}	C_{S3G}	C_{S4G}	C_{S5G}	C_{S6G}
Value / pF	98.6	217.4	172.1	145.3	46.2	125.3
Symbol		C_{ph1}			C_{ph2}	
Value / pF		516.3			1898.4	

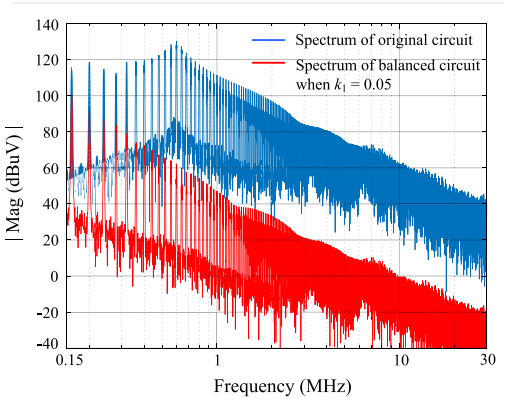
[44]. The minimum value of R_g recommended by the IEEE standards is 2 Ω [31].

In this inverter, module Vincotech ANPC-SPILT-1500V-SG-02T is used and directly mounted on the grounded heatsink. The parasitic capacitances of the switches to the ground mainly depend on the module package. Each module includes half of one phase that contains two Si IGBT (S_{a1}, S_{a6} or S_{a4}, S_{a5}) and one SiC MOSFET (S_{a2} or S_{a3}). The parasitic capacitances are measured by impedance analyzer WK6500B between the chip bottom surface and the conductive layer on the substrate by cutting all the bonding wires. The results are shown in Fig. 10(a) and (b).

According to the positions of every conductive layer, the parasitics can be integrated into C_{S1G}–C_{S6G} and listed in Table II. Then, the C_{ph1} and C_{ph2} are calculated as 516.3 and 1898.4 pF, respectively, by (1) and (2).

A. Balanced Case to Show the Conflict Between CM Noise and Loop Current

To well suppress the CM noise in the above inverter, the balance technique is applied, as introduced before. By this technique, the ratio of the two impedances in each leg in the bridge shown in Fig. 4(c) should be equal to each, which means the bridge is in a balanced state. Wang *et al.* [18] define k_1 and k_2 to represent the impedance ratio of branches



(a)

Condition	$i_{\text{LOOP-RMS}}$
Original	1.50 A
$k_1 = 0.05$	16.37 A

(b)

Fig. 11. Comparision of CM noise and loop current of original circuit and balanced circuit when k_1 is 0.05.

MGN and MPN, and their expressions are reviewed in (10) and (11). Thus, a balanced design means that k_1 is equal to k_2. In industrial applications, the C_{BUS} is usually tens nanofarad or even bigger. Here, in this case, the C_{BUS} is set to a reasonable parameter 7.9 nF. Then, the related L_0 and k_1 can be designed as 1.58 μH and 0.05, respectively,

$$k_1 = \frac{C_{\text{ph1}}}{C_{\text{ph1}} + C_{\text{ph2}} + C_{\text{BUS}}} \tag{10}$$

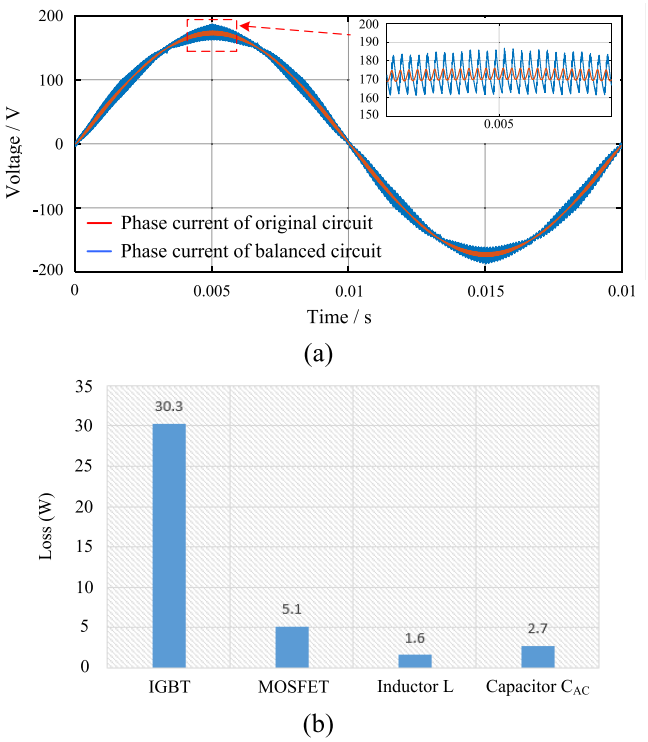
$$k_2 = \frac{Z(L_0) + 1/(3sC_{\text{ac}})}{Z(L)/3 + Z(L_0) + 1/(3sC_{\text{ac}})}. \tag{11}$$

The CM noise and loop current rms of the above balanced case are shown in Fig. 11. Obviously, the CM noise is effectively reduced, but the rms of loop current is significantly increased from 1.50 to 16.37 A. If the input voltage and modulation strategy are unchanged, the loop current will be nearly invariant under different output power.

B. Disadvantages of the Loop Current

The disadvantages of loop current are discussed in this part. The loop current is caused by charging and discharging of capacitors C_{ac} and parasitic capacitances in the loop current model, and it flows through switches, inductors, and so on. Fig. 12(a) shows the phase current in the original circuit and the balanced circuit. It can be seen that the amplitude of the current in the balanced circuit is about 10 A larger than that of original circuit. It brings extra losses and current stress to the switches, the inductors L, and capacitors C_{ac}. The losses can be estimated here to show an impression of the side effect with the conditions below.

1) The V_{DS} of Si-IGBT is 2.1 V.
2) The $R_{\text{DS-on}}$ of SiC MOSFET is 20 mΩ.
3) The equivalent resistance of an inductor L is 18.9 mΩ when the skin effect is considered.
4) The equivalent resistance of a capacitor C_{ac} is 31.85 mΩ.



(a)

(b)

Fig. 12. Disadvantage of loop current in the above balance case. (a) Extra current stress. (b) Distribution of extra losses.

The purpose of this section is to show the disadvantage of the loop current, so the estimated loss is adopted. Although the $R_{\text{DS-on}}$ of MOSFET is proportional to the junction temperature, in this section, it is assigned as 20 mΩ in certain temperature that can be used to estimate the loss. The distribution of losses is shown in Fig. 12(b). It should be noted that the losses are nearly constant under different output power. Thus, the efficiency of the whole system can be notably reduced when the inverter is running in low power in the early morning or the late afternoon in a photovoltaic application. Besides, the losses bring extra heat and need larger cooling system.

In this case, it can be clearly seen that the design only considering the elimination of CM noise will bring side effect to the inverter. This conflict should be well solved by a co-reduction method that is shown next.

IV. Co-Reduction Method of the CM Noise and Loop Current

The above conflict is caused by the decrease of total CM network impedance after adding C_{BUS}, the middle line, and the inductor L_0. Thus, the most direct solution is to increase the total CM impedance, namely decrease the total admittance, while keeping the system in balance. The simplified model is shown in Fig. 6. The capacitances C_{ph1} and C_{ph2} are determined by the switch module and the L is designed based on the requirement of the harmonics of the inverter. They are fixed parameters after the equipment is built. The remaining two variables are C_{BUS} and L_0. These two parameters can be represented by k_1 and k_2. When the circuit is balanced, k_1 is

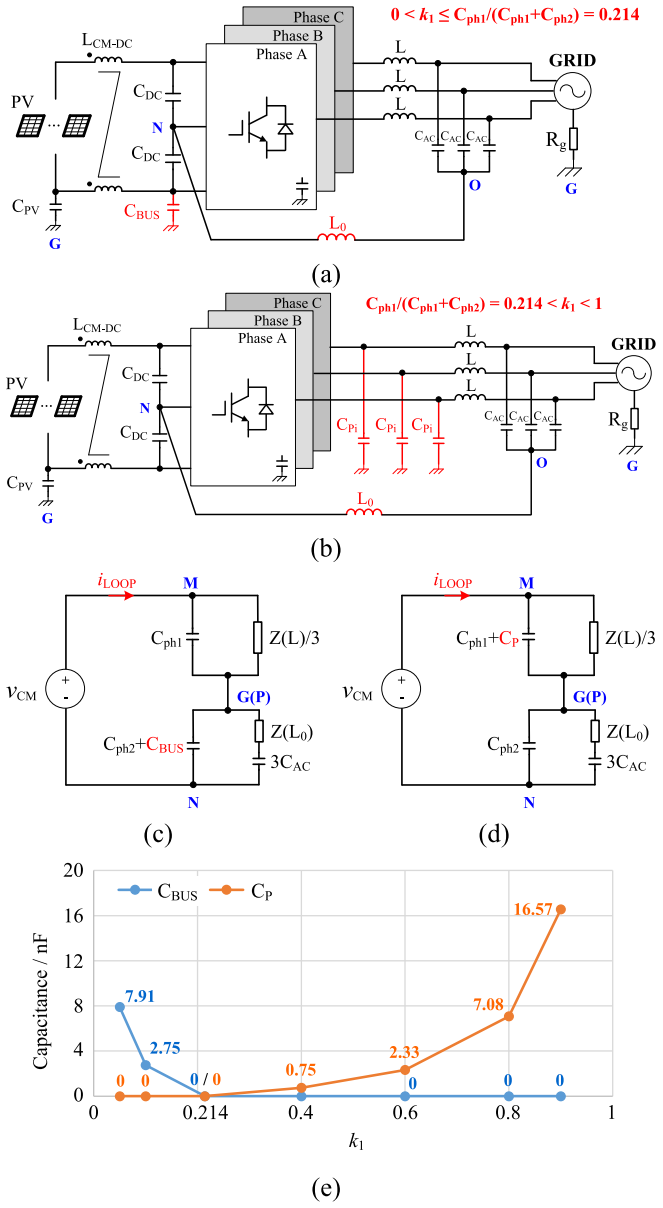


Fig. 13. Improved impedance balance technique to expand the range of k_1. (a) Topology when k_1 is from 0 to $C_{ph1}/(C_{ph1}+C_{ph2})$. (b) Topology when k_1 is from $C_{ph1}/(C_{ph1}+C_{ph2})$ to 1. (c) Loop current model of (a). (d) Loop current model of (b). (e) Configurations under different k_1.

equal to k_2, so the independent variables can be limited to only k_1 or C_{BUS}.

In theory, the value of k_1 can vary from 0 to 1. But only with change of C_{BUS}, the range is limited. If C_{BUS} is much larger than C_{ph1}, the k_1 is nearly 0 according to (10). However, when the C_{BUS} is reduced to 0, the k_1 can only be increased to the maximum value $C_{ph1}/(C_{ph1}+C_{ph2})$ that is dependent on the switch modules. The C_{ph1} and C_{ph2} are 516.3 and 1898.4 pF, respectively, in Section III, so the $C_{ph1}/(C_{ph1}+C_{ph2})$ is 0.214 in this article. It means that the k_1 can only vary from 0 to 0.214 by only adjusting C_{BUS}, as shown in Fig. 13(a).

To expand the range of k_1, the topology is improved as shown in Fig. 13(b), which adds three capacitors C_{Pi} to the output nodes of three phases. In the loop current model, the three capacitors C_{Pi} are in parallel and simplified to C_P, as shown in Fig. 13(d). The C_P is usually several nanofarad and has little influence on the DM output of inverter. In this case, the expression of k_1 is updated from (10) to

$$k_1 = \frac{C_{ph1} + C_P}{C_{ph1} + C_{ph2}}. \tag{12}$$

When the C_P is much larger than $C_{ph1} + C_{ph2}$, the k_1 will be 1. In theory, the C_{BUS} and C_P can be added at the same time to adjust the k_1. However, in this article, only one of them is used. First, more capacitors lead to larger admittance, resulting in larger loop current. Second, the parameter k_1 can be well adjusted by only one of them to achieve balance state, which reduces the system cost and volume.

In practice, C_{BUS} and C_P cannot be very large. For safety, C_{BUS} and C_P are usually served by Y capacitors that use enhanced insulation technology. In industry, the maximum capacitance of Y capacitor is about several tens nanofarad. First, the requirements of producing the large Y capacitors are stringent, so the number of suppliers is limited. Second, the small Y capacitors can reduce the leakage current between the dc bus and the heatsink. Therefore, the maximum value of C_{BUS} in this article is set as 7.91 nF. It means that the k_1 is analyzed from 0.05 instead of 0 in the following paragraphs.

The limit of Y capacitance is also applicable to C_{Pi}. Besides, there is another restriction. From Fig. 13(e), when k_1 is 0.9, the C_P is 16.57 nF, namely, each C_{Pi} is about 5.5 nF, then the L_0 is determined by the following equation that is 270 μH:

$$Z(L_0) = \frac{C_{ph1} + C_P}{C_{ph2}} \times \frac{Z(L)}{3}. \tag{13}$$

Further increase of k_1 means that C_P and L_0 will become larger, which brings larger volume and cost, so it is rarely used in actual inverter. Therefore, the k_1 ends at 0.9 and not 1 in this article.

It can be seen from Fig. 8 that the harmonics of CM noise source exist in two frequency bands. One is the low-frequency band around 150 Hz, and the other is the high-frequency band of 40 kHz and above. Different rules can be found for the dependence of the loop current on the parameter k_1 regarding the low- and high-frequency band. Thus, the following separately discusses them by studying the admittance that determines the loop current with a given source.

A. Dependence of $G_{LOOP}(s)$ on k_1 in Low-Frequency Band (Around 150 Hz)

In low frequency, the parasitic capacitance, C_{BUS} and C_{Pi} can be ignored because of their small admittance, and the loop current model can be simplified as shown in Fig. 14 that is a simple LC filter.

In this LC filter, only L_0 is left with respect to k_1. According to (13) and Fig. 13(e), when the k_1 changes from 0.05 to 0.9, L_0 changes from 1.58 to 270 μH. Although the admittance of L_0 is reduced by 170 times, this admittance is still much larger than that of $3C_{ac}$ in 150 Hz, so the variation of k_1 has little effect on $G_{LOOP}(s)$ in low-frequency band.

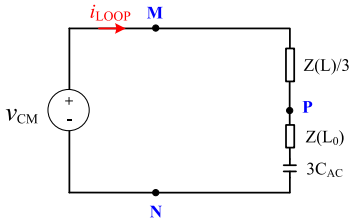
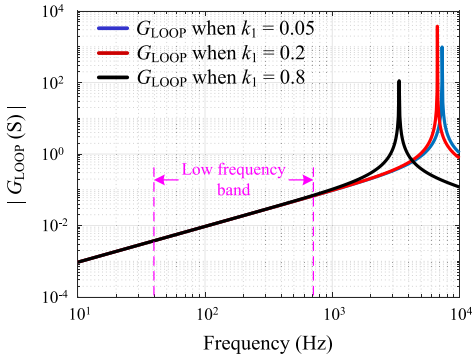


Fig. 14. Loop current model in low-frequency range (around 150 Hz).



(a)

k_1	L_0
0.05	1.58 uH
0.2	7.5 uH
0.8	120 uH

(b)

Fig. 15. Comparison of G_{LOOP} when k_1 are 0.05, 0.2, and 0.8. (a) Curves. (b) Parameters configurations.

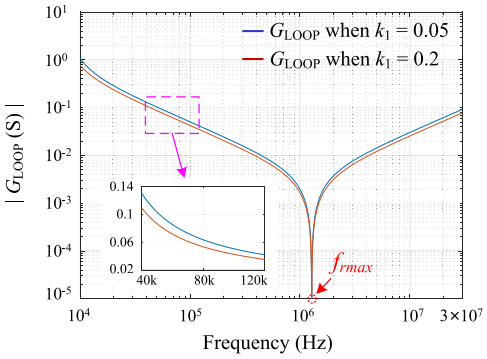
Fig. 15 shows the $|G_{LOOP}(s)|$ curves when k_1 are selected as 0.05, 0.2, and 0.8 for examples. From Fig. 15, the admittance is nearly unchanged in k_1 in low-frequency band (around 150 Hz). The obvious change is that the resonant frequency is reduced with the increase of k_1. However, it is still in the range of 1–10 kHz, far from 150 Hz and 40 kHz, which has no influence on loop current. In addition, the i_{LOOP} in 150 Hz is only a small part of the total $i_{LOOP-rms}$.

B. Dependence of $G_{LOOP}(s)$ on k_1 in High-Frequency Band (Larger Than 40 kHz)

In high frequency, the discussion needs to be divided into two cases. The case A refers to the circuit only with C_{BUS} that decreases from 7.91 nF to 0, namely, k_1 changes from 0.05 to 0.214. The case B refers to the circuit only with C_{Pi} that increases from 0 to 16.6 nF, namely, k_1 changes from 0.214 to 0.9. The following cases elaborate how the admittance $|G_{LOOP}|$ changes with k_1 in each case.

1) Case A : 0.05 < k_1 ≤ 0.214, Inverter With Only the Capacitor C_{BUS} Shown in Fig. 13(a): In the high-frequency band, the large capacitance of $3C_{ac}$ can be regarded as short, so (8) can be simplified as

$$I_{LOOP}(s) = \frac{V_{CM}(s)}{\frac{Z(L)/3}{1+s(C_{ph1})\times Z(L)/3} + \frac{Z(L_0)}{1+s(C_{ph2}+C_{BUS})\times Z(L_0)}} = G_{LOOP}(s) \times V_{CM}(s). \quad (14)$$



(a)

k_1	C_{BUS}	L_0
0.05	7.91 nF	1.58 uH
0.2	166.8 pF	7.5 uH

(b)

Fig. 16. Comparison of the admitatance $|G_{LOOP}|$ when k_1 are 0.05 and 0.2. (a) Magnitude–frequency curves. (b) Corresponding parameters.

Combining (4), (10), and (14), the $G_{LOOP}(s)$ can be derived as

$$|G_{LOOP}(s)| = (1-k_1)\left|sC_{ph1} + \frac{3}{Z(L)}\right|. \quad (15)$$

Based on (15), Fig. 16 shows the magnitude–frequency curve of the admittance $|G_{LOOP}(s)|$. It can be seen that there is a valley referring to the resonant frequency named as f_{rmax} that is caused by the resonance of C_{ph1} and $Z(L)/3$. Since these two parameters are constant in the inverter, the frequency f_{rmax} does not change with the variation of k_1 in the case A. It can be seen later that f_{rmax} is the maximum frequency within all the resonant frequencies as k_1 varies from 0 to 1. It can be easily observed from Fig. 16 and (15) that the $|G_{LOOP}(s)|$ decreases with the increase of k_1, which helps to reduce the loop current.

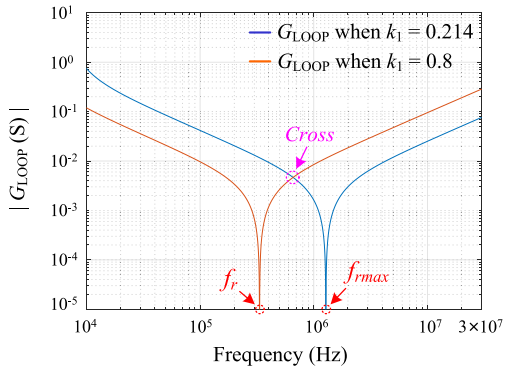
On the other hand, it can be seen that even if the C_{BUS} is reduced from 7.91 nF to 0, which means k_1 increases from 0.05 to 0.214, the decrease of $|G_{LOOP}(s)|$ is limited. Thus, to obtain better suppression effect of the loop current, the range of k_1 should be expanded.

2) Case B : 0.214 < k_1< 0.9, the Inverter With Only the Capacitor C_{Pi} Shown in Fig. 13(b): The loop current model in the case B is shown as in Fig. 13(d). The capacitors C_{Pi} are simplified as C_P that is in parallel with C_{ph1}, and the admittance can be expressed as

$$|G_{LOOP}(s)| = (1-k_1)|s(C_{ph1}+C_P) + \frac{3}{Z(L)}|. \quad (16)$$

Similarly, there is a valley regarding the magnitude–frequency curve of the admittance in this case, which refers to the resonant frequency f_r determined by $(C_{ph1}+C_P)$ and $Z(L)/3$. As a result, the resonant frequency can vary as C_P changes. It is noted that the resonant frequency decreases starting from the frequency f_{rmax} as C_{Pi} increases from 0 to 16.6 nF.

Fig. 17 shows the admittance $|G_{LOOP}(s)|$ as k_1 varies from 0.214 to 0.8 in the case B. As k_1 increases, the resonant frequency of $|G_{LOOP}(s)|$ decreases, and there is a cross between



(a)

k_1	C_P	L_0
0.214	0 pF	8.16 uH
0.8	7.08 nF	120 uH

(b)

Fig. 17. Exhibition of $|G_{LOOP}|$ when k_1 changes from 0.214 to 0.8. (a) Magnitude–frequency curves. (b) Corresponding parameters.

the two curves. The cross frequency f_{Cross} is expressed as follows:

$$f_{Cross} = \frac{1}{2\pi\sqrt{\frac{k_1+A}{2-k_1-A}} \times C_{ph2} \times L/3} \tag{17}$$

in which A is $C_{ph1}/(C_{ph1} + C_{ph2})$ that is 0.214.

It is noted that the $|G_{LOOP}(s)|$ is significantly reduced before the frequency f_{Cross} but increased after it. From Fig. 7(c), the source amplitudes of low-order harmonics beyond the switching frequency of 40 kHz are much larger than those of the high-order harmonics. Thus, f_{Cross} is critical to determine how the loop current changes with k_1. If f_{Cross} is designed much larger than the frequency range that the low-order harmonics exist in, then the increase of the loop current at high-frequency range that is caused by the admittance increase as k_1 increases only take small part in the total value because of the small high-order harmonics of the noise source. However, once f_{Cross} decreases close to or even enter the low-frequency range, the opposite change before and after the cross frequency is comparable to each other. As a result, it is hard to estimate how the total current changes as k_1 increases.

From the above analysis in part A and B, it can be seen that the change of k_1 has little influence on the low-frequency component of the loop current around 150 Hz. The dependence of the loop current on the parameter k_1 is determined by the rules discussed in the high-frequency range beyond 40 kHz in part B. When k_1 increases from 0.05 to 0.214, the loop current decreases, but with a small amplitude. As k_1 increases from 0.214 to 0.9, if the cross frequency is much larger than the frequency range that low harmonics exist in, the total current also decreases with the increase of k_1, but with a large amplitude.

Regarding a given inverter, the f_{rmax} is fixed after the main circuit design. If f_{rmax} is as low as in the frequency range that low harmonics of the switching frequency f_s exist in, then k_1 equal to $C_{ph1}/(C_{ph1} + C_{ph2})$, which is 0.214 in this article, is around the optimum value to suppress the loop current to the minimum. The further increase of k_1 can possibly increase the loop current. If f_{rmax} is high enough, then k_1 can be further increased by adding C_{Pi} until the cross frequency enters the critical frequency range that low harmonics are. Further increase of k_1 can have the risk of increasing the loop current.

TABLE III
PARAMETERS OF INDUCTORS L_0 IN DIFFERENT k_1

k_1	L_0	$I_{L0(max)}$	A_P	Magnetic ring
0.05	1.58 uH	40.2 A	0.71 cm^4	0R42212TC
0.1	3.33 uH	37.1 A	1.27 cm^4	0P43806TC
0.2	7.5 uH	32.9 A	2.26 cm^4	0R43610TC
0.3	12.86 uH	28 A	2.8 cm^4	0R43813TC
0.4	20 uH	25 A	3.47 cm^4	0R43615TC
0.5	30 uH	20.1 A	3.37 cm^4	0R43615TC
0.6	45 uH	15.9 A	3.16 cm^4	0R43813TC
0.7	70 uH	12.8 A	3.19 cm^4	0R43813TC
0.8	120 uH	9.1 A	2.76 cm^4	0R43813TC
0.9	270 uH	6.9 A	3.57 cm^4	0R43615TC

The critical frequency range mentioned above depends on the spectrum of the noise source v_{CM}. Regarding the equipment shown in this article, based on the spectrum of v_{CM} in Fig. 7(c), the amplitude of the v_{CM} harmonics with frequency larger than the 10th harmonics of switching frequency is much lower than the fundamental harmonic of switching frequency at 40 kHz, so the frequency of 400 kHz can be approximately regarded as the maximum boundary of the critical frequency range. In this case, the f_{rmax} is around 1.28 MHz, thus k_1 can be further increased by adding C_{Pi}. It is found even k_1 is 0.9, the f_{Cross} is 595 kHz that is still larger than 400 kHz. Thus, here the loop current can be well suppressed by increasing the parameter k_1. However, if the C_{ph2} or L of an inverter is large, or the switching frequency becomes even higher, the cross frequency can enter the frequency range of low harmonics as increasing k_1. As mentioned before, the loop current will decrease first and then increase as k_1 increases. The optimal point can only be obtained by calculation.

V. VOLUME AND COST

The co-reduction method is realized by adjusting the inductor L_0 and capacitor C_{BUS} or capacitor C_{Pi}. In this section, the additional volume and cost by the method are discussed.

First, the inductor is designed by area-product method and the expression is given as follows [45]:

$$A_P = \frac{L_0 I_{L_0(max)}^2}{K_u J_{RMS} B_S}. \tag{18}$$

The quantities K_u, J_{RMS}, and B_S are the window utilization factor, the rms current density of the winding, and the saturation flux density, respectively. In this article, K_u is set as 0.3, J_{RMS} is 5 A/mm^2, and B_S is 240 mT. The A_P of L_0 in different k_1 is shown in Table III. The ring cores are selected from the company Magnetics [46].

As the parameter k_1 increases, the inductance L_0 increases with the current flowing through decreases. The A_P increases

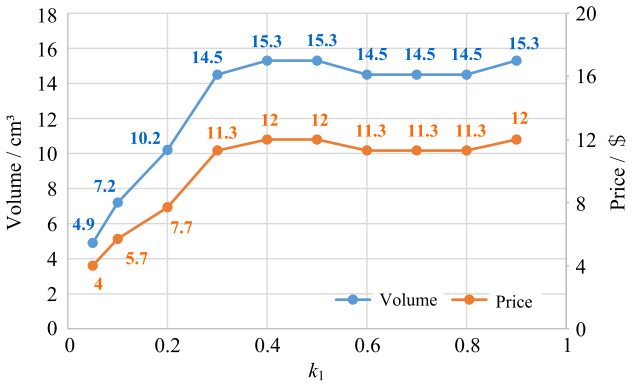


Fig. 18. Volume and price of inductors L_0 with different k_1.

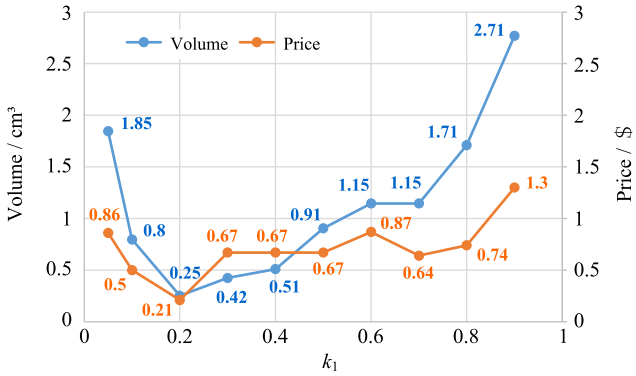


Fig. 19. Volume and price of the capacitors C_{BUS}/C_P with different k_1.

TABLE IV
PARAMETERS OF CAPACITORS C_{BUS}/C_P IN DIFFERENT k_1

k_1	C_{BUS}/C_P	Capacitor
0.05	7911.3 pF	DE1E3RA472MA4BQ01F
0.1	2478.3 pF	DE1E3RA332MA4BQ01F
0.2	166.8 pF	DE1B3RA151KA4BQ01F
0.3	99.1 pF*3	DE1B3RA101KA4BQ01F
0.4	249.8 pF*3	DE1B3RA221KA4BQ01F
0.5	460.7 pF*3	DE1B3RA471KA4BQ01F
0.6	777.1 pF*3	DE1B3RA681KA4BQ01F
0.7	1304 pF*3	DE1E3RA152MA4BQ01F
0.8	2359 pF*3	DE1E3RA222MA4BQ01F
0.9	5523 pF*3	DE1E3RA472MA4BQ01F

in the beginning and then keeps varying in a small scale. The corresponding volume and price are shown in Fig. 18.

Regarding the capacitors C_{BUS} or C_P, Y capacitors from the company Murata are chosen [47] and shown in Table IV. The volume and price of the capacitors are proportional with the capacitance, as shown in Fig. 19. It can be seen that the volume and price decrease as k_1 changes from 0.05 to 0.214, namely, when the capacitance C_{BUS} decreases from 7.9 nF to 0. Then they rise because of the increase of the capacitor C_{Pi}.

Regarding the L_0, even the co-reduction method is not adopted, it is also needed for normal balance technique. Thus, the main side effect of the co-reduction method is the extra volume and cost of the capacitors. However, the volume and cost of the capacitor are just around 1/10 of that of the inductor L_0, that is negligible compared to the 140-kW inverter.

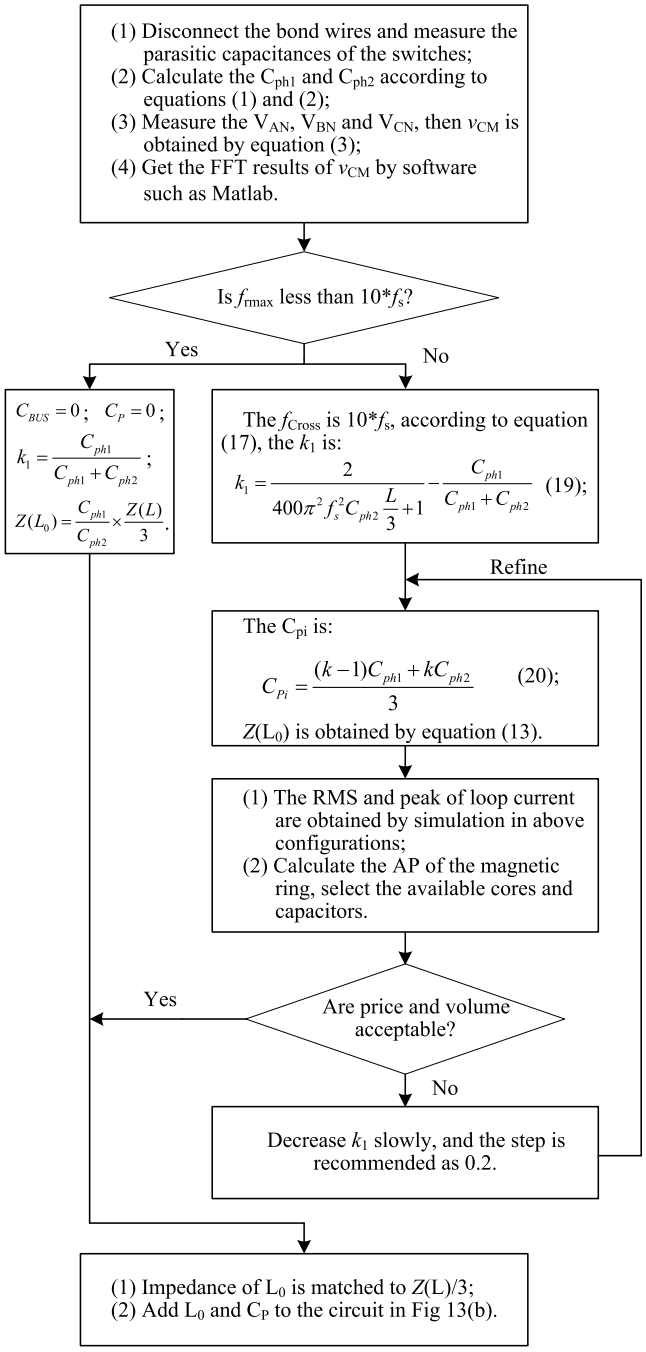


Fig. 20. Guidelines of the co-reduction method.

VI. GUIDELINES

The guidelines of applying the co-reduction method to an inverter is given in Fig. 20. In general, the suppression of the loop current and the CM noise at the same time can be realized by adjusting the parameter k_1 through designing the capacitor C_{BUS} or C_{Pi}, while keeping the bridge equal in CM noise model. The design procedure is shown below.

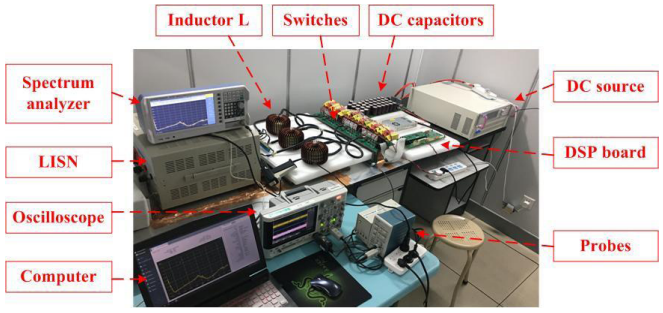


Fig. 21. Experimental setup.

First, the parasitic capacitances and CM noise source v_{CM} should be measured. Then, the resonant frequency $f_{r\max}$ should be calculated according to C_{ph1} and $L/3$.

If $f_{r\max}$ is less than $10{*}f_s$, then the k_1 can be set as $C_{\mathrm{ph1}}/(C_{\mathrm{ph1}}+C_{\mathrm{ph2}})$ by connecting no capacitor C_{BUS}. It is almost the optimum case for suppressing the loop current.

If $f_{r\max}$ is larger than $10{*}f_s$, the optimum k_1 can be set by increasing C_{Pi} until the cross frequency f_{cross} decreases to $10{*}f_s$, as given in (19). Then components L_0 and C_{Pi} can be determined by (13) and (20). Next, the volume and cost of the components can be determined. If they are acceptable, the design ends with minimum CM noise and loop current. Otherwise, the k_1 can be reduced slowly to make a tradeoff between the loop current and the extra volume and cost. Regarding the inverter shown in this article, k_1 can be chosen as 0.8 that achieves good overall performances that include good CM noise reduction, small loop current, and small extra volume and cost.

VII. Experimental Verification

Due to the power limit in the laboratory, the dc voltage of the 140-kW inverter is set at 300 V for the experiment. The other parameters of the inverter are the same as Table I. The change of the dc voltage only proportionally changes the magnitude of the spectrum of the noise source v_{CM} as shown in Fig. 7(c), but has little influence on the dependence of the i_{LISN} and i_{LOOP} on the network. Thus, the low-voltage experiment can also validate the above theory.

Regarding the EMI test, the LISN is connected between the inverter and the load. The LISN used in this article is ZN3770B that is V-type 50 Ω/50-μH circuit defined in GB/T 6113.102-2018/CISPR 16-1-2:2014 [39]. Since the noise collected by the ZN3770B is a mixed signal of CM noise and DM noise, three 2-μF lead-through capacitors with low parasitic inductance are connected in parallel between the three inputs of LISN to filter the DM current. The CM spectrum is tested by spectrum analyzer Rohde&Schwarz FPC1000. The testing result of the spectrum is the voltage on the 50-Ω resistance, which is proportional to i_{LISN}. The experiment setup is shown in Fig. 21.

In the loop current test, the LISN is removed. The loop current is obtained by testing the current through the capacitor C_{BUS} or $C_{\mathrm{P}}$and by calculating based on the parallel relationship between the capacitance C_{BUS} or $C_{\mathrm{P}}$and the parasitic

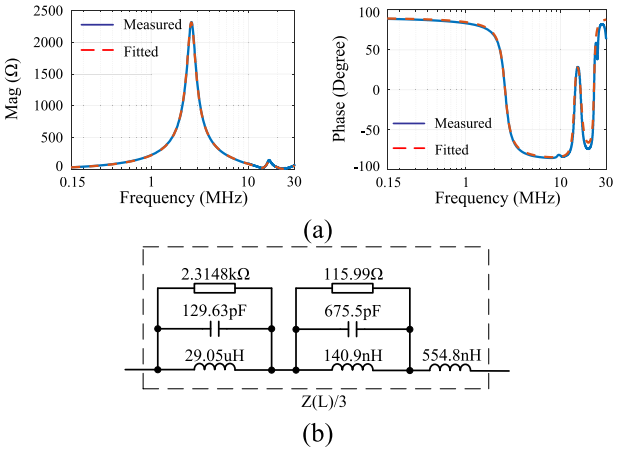


Fig. 22. Modeling of the filter inductor $L/3$. (a) Measured and fitted magnitude and phase angle. (b) Inductor model for curve fitting.

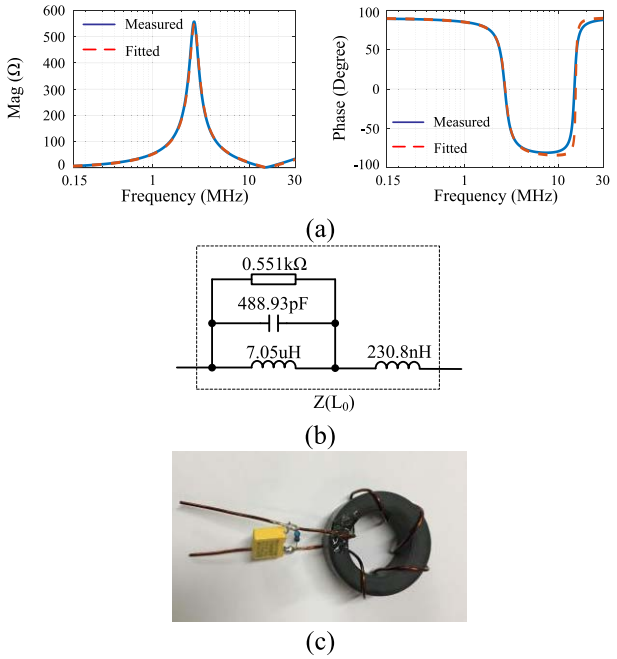
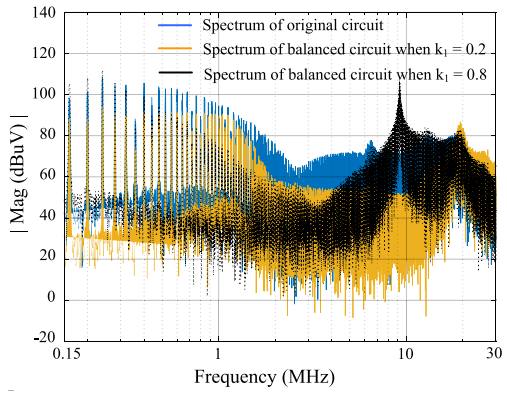


Fig. 23. Modeling of the matched inductor L_0 when k_1 is 0.2. (a) Measured and fitted magnitude and phase angle. (b) Inductor model for curve fitting. (c) Demonstrator.

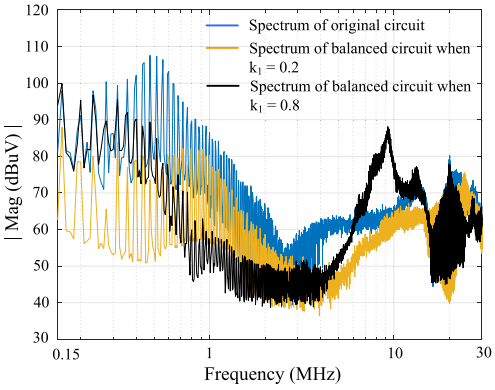
capacitances. The current is measured by probes Tektronix TCPA300 and YOKOGAWA 701918, and analyzed by scope KEYSIGHT DSOX3034T.

Because of the parasitic capacitance between turns, the inductor L is not ideal. The magnitude–frequency and phase–frequency curves of $Z(L)/3$ and its fitted model are shown in Fig. 22. Its resonance frequency is 2.59 MHz that is far away from the frequency that the low-order harmonics of v_{CM} exist in, which means that it can be considered as an ideal inductance in the analysis of i_{LOOP}.

To suppress the CM noise, the inductor L_0 needs to be compensated by a *RLC* network to match the impedance curve of the inductor L. Fig. 23 shows an example when k_1 is 0.2. Before matching, the inductor L_0 can be regarded as an



(a)



(b)

Fig. 24. Spectra comparison between original circuit and balanced circuit when k_1 are 0.2 and 0.8. (a) Simulation. (b) Experiment.

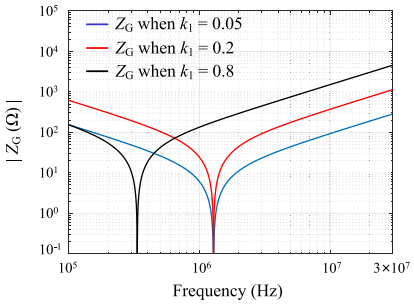
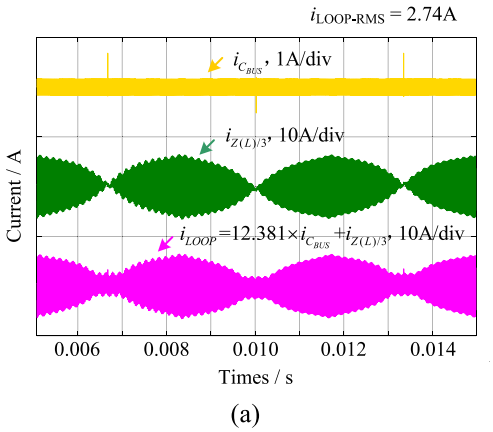
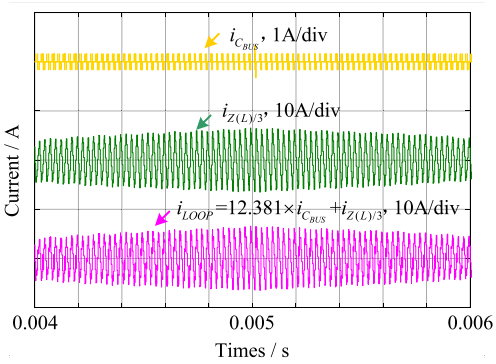


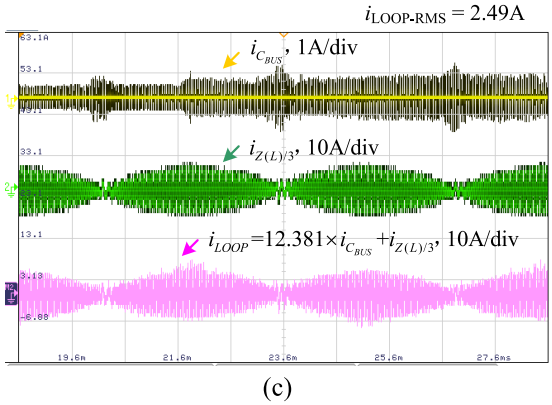
Fig. 25. Comparison of Z_G when k_1 are 0.05, 0.2, and 0.8.



(a)



(b)



(c)

Fig. 26. Waveform of i_{LOOP} when k_1 is 0.2. (a) Simulated results. (b) Details of the simulated results. (c) Experimental results.

ideal inductance because the parasitic capacitance between its wings is very small. Then a 490-pF capacitor and a 550-Ω resistor are added in parallel with the inductor L_0 to match the first stage of $Z(L)/3$. Compared with the $Z(L)/3$ in Fig. 22, the impedance matches well in the frequency from 150 kHz to 15 MHz.

But in the frequency above 15 MHz, since the second stage inductance in the model of $Z(L)/3$ is small, the exact matching for balance requires another stage in the model of $Z(L_0)$ containing inductance only about 35 nH. Even if this inductance is exactly made, it will be overwhelmed by the parasitic inductance of the middle line. Thus, it is no longer made in the experiment. The middle-line parasitic inductance of 230.8 nH is connected in series with the first stage of the L_0 model, as shown in Fig. 23(b). As a result, the impedance beyond 15 MHz is not well matched leading to a weaken suppression effect of the CM noise.

The spectra of original circuit and balanced circuit when values of k_1 are 0.2 and 0.8 are shown in Fig. 24 as an example. The spectra of CM noise are suppressed obviously when the circuit is balanced. In the frequency less than 2.59 MHz, the noise level when k_1 is 0.8 is lower than that when k_1 is 0.2. The impedance $Z_G(s)$, as shown in Fig. 5, when k_1 is 0.8 is bigger than that when k_1 is 0.2. However, as shown in Fig. 25, the impedance $Z_G(s)$ with k_1 of 0.8 is lower than that of 0.2 in the low-frequency range which results in higher noise level as shown in Fig. 24. When the frequency is larger than 2.59 MHz,

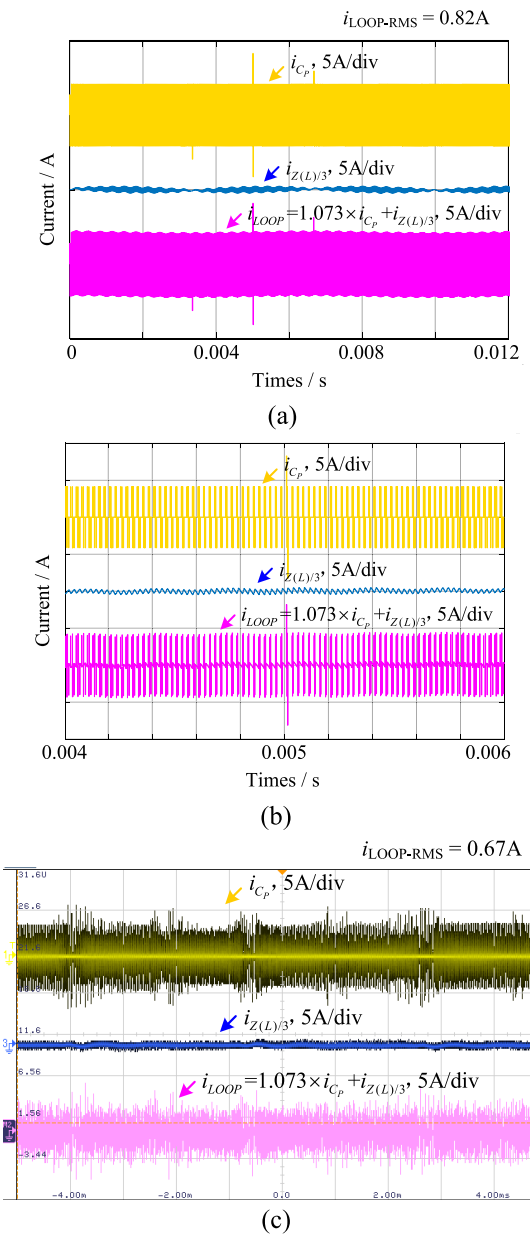


Fig. 27. Waveform of i_{LOOP} when k_1 is 0.8. (a) Simulation results. (b) Details of the simulated results. (c) Experimental results.

the noise level in the case with k_1 of 0.8 worsens again when compared to that of 0.2, especially at the frequency 9.1 MHz where a noise peak exists. It is caused by the lead parasitic inductance of C_{P} that is around 100 nH. This problem can be solved in the future design by reducing the lead length of C_{P}.

Then, the waveforms of loop current when values of k_1 are 0.2 and 0.8 are shown as examples. Because the current flowing through the parasitic capacitance is difficult to measure, it can only be obtained by measuring the current through the added capacitor, for example, C_{BUS}, and converting with the following equation:

$$i_{\mathrm{LOOP}} = \frac{C_{\mathrm{ph2}}}{C_{\mathrm{BUS}}} \times i_{C_{\mathrm{BUS}}} + i_{C_{\mathrm{BUS}}}. \tag{19}$$

The loop current when k_1 is 0.2 is shown in Fig. 26, the rms values of simulation and experiment are 2.74 and 2.49 A; the

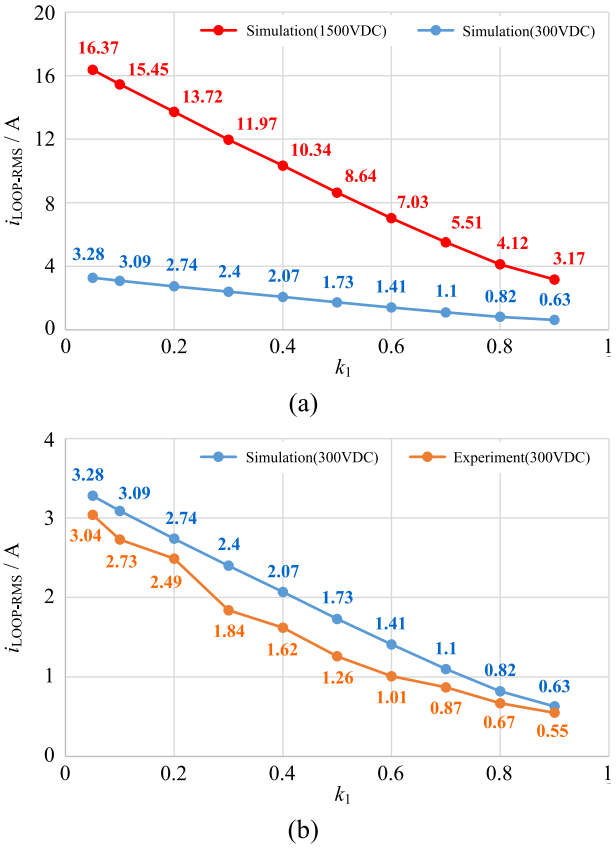


Fig. 28. $i_{\mathrm{LOOP-rms}}$ of simulation and experiment in different k_1. (a) Simulated results when $2U_{\mathrm{dc}}$ are 1500 V and $2U_{\mathrm{dc}}$ = 300 V. (b) Simulated and experimental results when $2U_{\mathrm{dc}}$ = 300 V.

slight numerical difference between them is mainly due to the distributed resistance in the system.

Fig. 27 shows the loop current in the condition of k_1 is 0.8. Compared to Fig. 26, the current flowing through L_0 is reduced significantly. The simulated and experimental results are 0.82 and 0.67 A, respectively. It is obvious that the loop current rms is reduced with the increase of k_1.

The rms of the current $i_{\mathrm{LOOP-rms}}$ with different k_1 is shown in Fig. 28. First, the simulated results, when $2U_{\mathrm{dc}}$ are 1500 and 300 V, respectively, are compared. It is easy to see that $i_{\mathrm{LOOP-rms}}$ in 1500 V is approximately five times as much as that in 300 V. Thus, in the normal operation, the loop current is notable and needs to be reduced. Then, Fig. 28(b) shows the curves of simulated and experimental $i_{\mathrm{LOOP-rms}}$ in 300-V case. It shows that the two curves are close to each other, which verifies the theoretical calculation. It can be seen that the $i_{\mathrm{LOOP-rms}}$ is reduced with the increase of k_1, which further proves the co-reduction method in this article.

VIII. Conclusion

With the application of SiC devices, the efficiency and power density of inverters can be further improved by the high speed and high-frequency switching, but possibly resulting in a worsening CM noise. Impedance balance is a good method to reduce the CM noise but it can significantly increase the loop current in the system concerning the bridge balance, which

can add additional losses and costs to the system and prevent the high efficiency or power density led by the uses of SiC devices.

In this article, the CM noise and loop current are clarified first and their analytical models are established. Their conflict is shown in a case and a co-reduction method is proposed. To well reduce the CM noise and the loop current, it is suggested that the balance of the bridge should be realized and then, more importantly, the bridge should be carefully designed to set an optimal balance coefficient k_1 to suppress the loop current. The exact value needs to be calculated based on the application and the setup based on the guidelines to reduce the CM noise and loop current at the same time. Compared with the case that balance coefficient k_1 is 0.05, the loop current is reduced by more than 75% when the circuit operates in the optimal balance coefficient. This method can effectively reduce the CM noise and loop current, and only has little volume and cost because the current flowing through the feedback inductor is very small and is suitable for the applications of SiC inverters.

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