Structure electronic design of a crystal filter for high accuracy multi-mode crystal oscillator

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by

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Preface

This thesis is part of the Master's Degree in Electrical Engineering, Microelectronics, at Section ELCA, Delft University of Technology, the Netherlands. This thesis has been carried out under the financial support of Persitec B.V. and technical support of SemiBlocks B.V.

Abstract

Modern communication systems have a strong need for low-cost and high-stability frequency references. Although low-cost crystal oscillators can easily be realized and are available to the market in large quantities, crystal oscillators with frequency stability in the ppb(10^{-9}) range over a wide temperature range are only available at high costs. In 2018, SemiBlocks B.V. proposed an improved technique so-called *Multi-Mode Crystal Oscillator*(MMXO)[24]. The MMXO determines the output frequency through a triple mode oscillator and corrects this by an algorithm running on the internal microprocessor. The advantage of the MMXO is that it uses regular AT-Cut crystals and the whole circuitry can be implemented in silicon, and the frequency selective network is implemented by digital technology. This results in a low-cost and high-stability crystal oscillator solution.

However, the measurement result of the first generation MMXO showed that the large temperature dependent phase shift of the analog crystal chain significantly influences frequency stability of the MMXO. This inaccuracy is out of the compensation ability of the multi-mode system since it is highly dependent on the analog network rather than the crystal. For the improvement of the next generation MMXO product, this thesis aims at designing a *CMOS crystal filter*, which should reflect the characteristic of crystal accurately. Any change of resonance frequency of the tested crystal should accurately match that of the frequency characteristic of the crystal filter. The objective is to control frequency error below 10ppb for the three resonance tones of the tested crystal over -40 to 100 °C.

The design of the crystal filter follows a structured methodology and combines analysis and simulations in Cadence together with SLICAP (Symbolic Linear Circuit Analysis Program), which helps researchers quickly find the early design solution and show-stopper before circuit design. The crystal filter is a two-stage amplifier. The first stage is a transadmittance stage, which reflects the frequency characteristic of the crystal by a current output. The second stage is a transimpedance stage, which makes the output of the TA stage observable to the ADC of the MMXO system. The pre-layout simulations show the the frequency error of the base tone and the third overtone is close to 10 ppb, while the fifth overtone has a large frequency error around 252 ppb. The crystal filter allows full range input of the tested ADC and is stable under all typical corners, with $12.83\mu W$ power consumed by crystal, $95.6mW/pixel$ total current usage, and the chip area $1.75 \times 10^{-8} mm^2/pixel$. The output-referred noise PSD of the base tone and the third overtone is $3.4 \times 10^{-13} V^2/Hz$ and $7.3 \times 10^{-15} V^2/Hz$. which meets the noise requirements with enough design margin, while

the fifth overtone fails with noise specs due to the quantization noise and aliased noise caused by ADC.

Acknowledgments

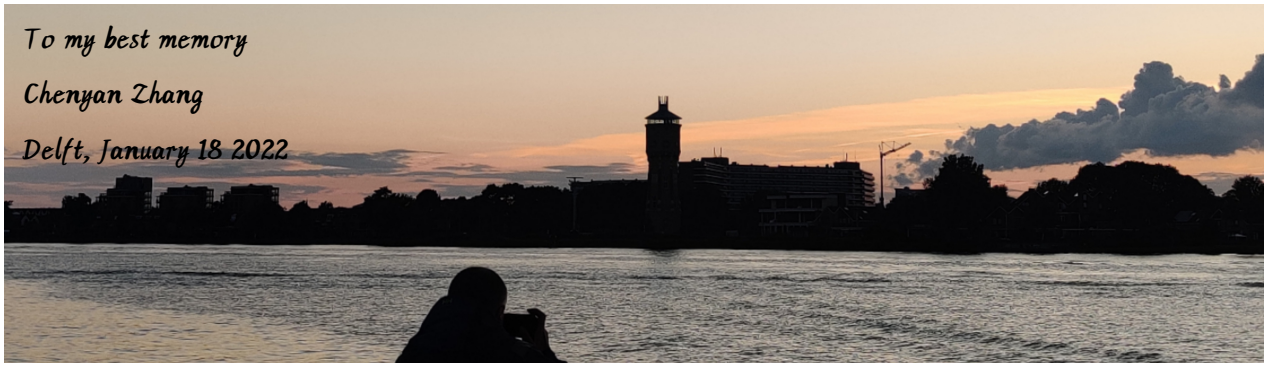
First, I would like to thank SemiBlocks B.V. and my company supervisor Rob van der Valk. This project would not have been carried out without the great idea and product from SemiBlocks B.V. and the technical support from Rob.

I would also like to thank Dr. Chris Verhoeven and Anton Montagne for their course SED (Structured Electronic Design). When I tried to learn SED two years ago, I almost fell asleep at every lecture. It was hard for me to follow the course since I had no background knowledge. I was so lucky that Chris and Anton were very kind and patient in instructing me to finish my course project. The knowledge from SED gives me solid foundations of system design and logical thinking, which helps me gradually become an independent designer.

Sincere thanks again to Anton Montagne as my daily supervisor. Due to the pandemic and my relative's death, my mental and physical state was terrible at the beginning of my thesis project, especially when I worked at home alone. Anton was kind to offer me a place in his workshop to work and took me biking after work to release bad emotions. Although my graduation project progressed slowly at first, I gradually felt the happiness from my life with his help. During my thesis project, Anton instructed me on analog circuit design and shared his wisdom toward work and life. His passion, critical thinking, and professional knowledge inspire me. I hope to become an excellent circuit designer like Anton by my efforts.

I am grateful to my family. Due to the pandemic, I have not been home for two and a half years. It is impossible for me to finish my master's program without the unconditional support of my family.

Lastly, I would like to express my love to my grandmother. Thank you for your continuous love and care throughout my life. When I left China for the Netherlands, You stood in front of the security gate for a long time and watched me leaving. I dared not look back at you because I was afraid I would cry. That was the last time I saw you in my life. How I wish I could look back and see your kind face again. I know if there is a heaven, you must be there. And I will take your kindness and love to the rest of my life.



Contents

Acronyms

AGM Asymptotic Gain Model.

CNR Carrier-to-Noise Ratio.

CPCS Complementary Parallel Common-Source.

DFCS Differential Common-Source.

DHMXO Dual-Harmonic-Mode Crystal Oscillator.

LP Loopgain- Poles.

MCXO Microprocessor-Controlled Crystal Oscillator.

MMXO Multi-Mode Crystal Oscillator.

NF Noise Figure.

OCXO Oven-Controlled Oscillator.

PLL Phase-Locked Loop.

ppb part per billion.

PSD Power Spectral Density.

SED Structure Electronics Design.

SLICAP Symbolic Linear Circuit Analysis Program.

TA Trans-Admittance.

TCXO Temperature-Controlled Crystal Oscillator.

TI Trans-Impedance.

VF Voltage Follower.

CHAPTER 1

Introduction

1.1 Background

Crystal oscillators are used as frequency and timing reference in electronic equipment. The mechanical resonance of a vibrating crystal creates an electrical signal with a constant frequency. This frequency is often used to keep track of time to provide a stable clock signal for mixed-signal circuits, and to stabilize frequencies for radio transmitters and receivers[10].

Modern communication systems have a strong need for low-cost and high-stability frequency references. Low-cost, low-noise crystal oscillators can easily be realized and are available to the market in large quantities. However, frequency references that exhibit frequency stability in the ppb(10^{-9}) range over a wide temperature range, are only available at high costs. For example, atomic clock, which is based on the interaction of electromagnetic radiation with the excited states of certain atoms, has instability of 10^{-10} to 10^{-15} typically[13]. However, it is expensive and power consuming and thus impractical to be widely applied in commercial IC design.

Crystal clock placed in temperature-controlled chamber(OCXO) is a common application of frequency reference in IC industry. The chamber of OCXO maintains crystal at a constant temperature to prevent changes of resonance frequency due to temperature variations. A temperature sensor is integrated in OCXO and precisely controls temperature with feedback circuit. The typical instability is 10^{-6} to 10^{-9}[15]. However, this solution is power consuming , occupies large dimensions, and has a limited working temperature range.

A low-cost solution for reducing the temperature drift is to measure the crystal's temperature and correct oscillation frequency by detuning the oscillator with an electrically controlled device. Crystal oscillators based on this principle are called Temperature Compensated Crystal Oscillators, or shortly TCXOs. The relation between the temperature and the tuning voltage is determined and stored during calibration and reused during operation. The improvement of the temperature stability is limited because the temperature of the sensor does not perfectly track that of the crystal under all circumstances. Due to factory calibration, the crystal needs to be paired with the electronics. The typical inaccuracy of TCXOs is 10^{-6} to 10^{-7}[15].

Microprocessor-Controlled Crystal Oscillators(MCXOs) is one of the kinds of TCXOs. It uses a microprocessor to provide processing to enable more accurate compensation under a variety of circumstances. While performance is a little better, costs are above those of the other forms of TCXO. The typical inaccuracy of MCXOs is 10^{-7} to 10^{-8}[15].

In 1989, Schodowski[23] introduced a different technique for MCXO with the aid of a

(a) (b) (c)

Figure 1.1: Three different kinds of high-stability frequency references. (a) NIST Unveils chip-scale atomic clock. Source[1]; (b) IQD 10MHz OXCO oscillator. Source[11]; (c) IQD 20MHz MXCO oscillator. Source[12]

dual mode SC-cut crystal oscillator and corrected by cascading it with a microprocessor-controlled frequency synthesizer. He developed his design based on the harmonic effect of crystal[2], which indicates the normalized resonance frequency-temperature (f-T) characteristics of crystal as:

$$\frac{\triangle f_M}{f_M} = a_M \triangle T + b_M \triangle T^2 + c_M \triangle T^3 \tag{1.1.1}$$

where the normalized frequency $\frac{\triangle f_M}{f_M}$ and the difference temperature $\triangle T$ are referenced at the inflection temperature and the a_M, b_M, and c_M are the first, second, and the third-order temperature coefficients.

By exciting a pair of harmonically related resonators in a dual-mode crystal oscillator (Figure 1.2) and combining their signals, a beat frequency is obtained which can be used to compensate the frequency error. The beat frequency f_β is the frequency difference between

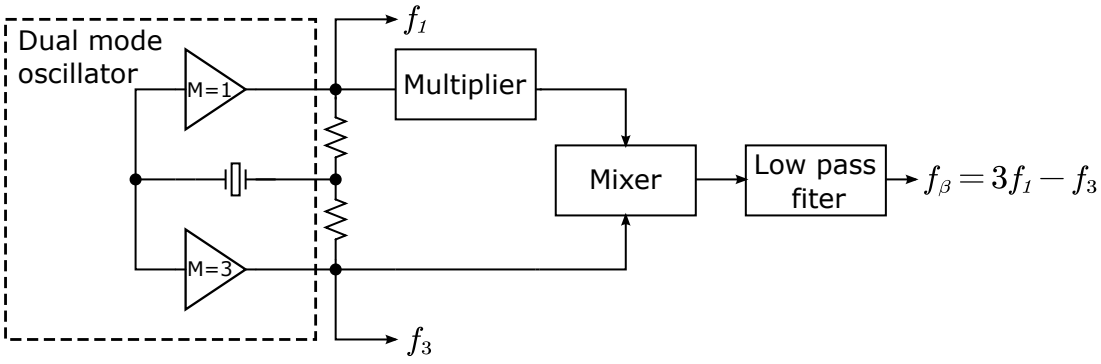


Figure 1.2: Illustration of the dual mode thermometry method. Source[23], edited

a M_{th} overtone resonance frequency and the M times fundamental resonance frequency of the crystal. In figure 1.2, the fundamental frequency f_1, is is multiplied by three and then mixed with the higher harmonic (M=3) to obtain the beat frequency:

$$f_\beta = 3f_1 - f_3 \tag{1.1.2}$$

Mode	Freq[MHz]	a $10^{-6}/°\mathrm{C}$	b $10^{-8}/°\mathrm{C}^2$	c $10^{-11}/°\mathrm{C}^3$
f_1	5	0.13	-1.69	5.45
f_3	14.843	1.15	-1.60	5.58
f_β	0.157	-96.33	-9.94	-7.24

Table 1.1: Typical SC-cut harmonic and beat frequency temperature coefficients. Source[23]

The (f-T) characteristic of the beat frequency [9] may be described as:

$$\frac{\triangle f_\beta}{f_\beta} = \frac{3}{3-n}\frac{\triangle f_1}{f_1} - \frac{n}{3-n}\frac{\triangle f_3}{f_3} \tag{1.1.3}$$

where n is the non-integer ratio of the frequencies for the harmonic pair, i,e., $n = f_3/f_1$. Values of n ranging from 2.94 to 2.98 for a SC-cut designs inspected[9]. Combined with equation 1.1.1, equation 1.1.3 can be written as:

$$\frac{\triangle f_\beta\,(T)}{f_\beta} = \frac{3a_1 - na_3}{3-n}\Delta T + \frac{3b_1 - nb_3}{3-n}\Delta T^2 + \frac{3c_1 - nc_3}{3-n}\Delta T^3 \tag{1.1.4}$$

where a_1. b_1, c_1 and a_3, b_3. c_3 are the temperature coefficients of frequency for the fundamental and third overtone, respectively. Schodowski found the first order term $(3a_1 - na_3/3 - n)$ in equation 1.1.4 is much dominant than the second and third order term. Table 1.1 provides the computed temperature coefficients of an SC-cut crystal for the base tone , third overtone and the beat frequency. The linear (f-T) characteristic makes the beat frequency suitable for accurate temperature measure over a wide operating temperature range.

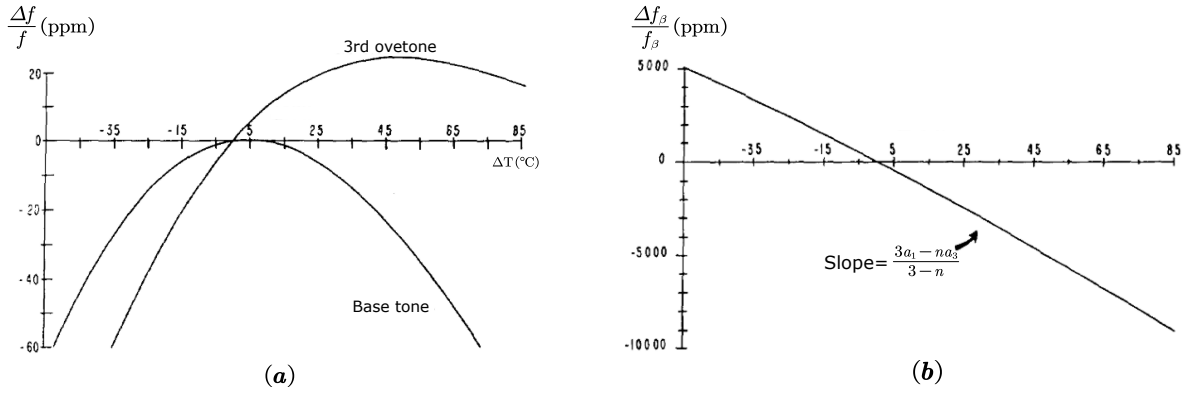


Figure 1.3: (a) Fundamental and the third overtone f-T characteristic of a typical SC-cut resonator. (b) The beat frequency f_β of a typical SC-cut resonator. Source[23]

Figure 1.4[23] shows the proposed circuit of The Dual-Harmonic-Mode Crystal Oscillator (DHMXO) and the concept of the MCXO system. In DHMXO, two Colpitts oscillators work at different resonance frequencies sharing a common SC-cut crystal. Two emitter degeneration proves negative feedback that behaves like a high Q band-pass filter filtering out all frequencies except the desired resonance frequency (f_1 or f_3). Implementation of

the self-temperature sensing method is shown by the MCXO simplified block diagram of Figure 1.4(b). Schodowski[23] indicated a calibration system, which is consist of a reciprocal counter and a correction circuit, to store the relation of f_β and temperature. During operation, it is used by a microprocessor-controlled frequency synthesizer to correct one of the output frequencies of the dual-mode oscillator.

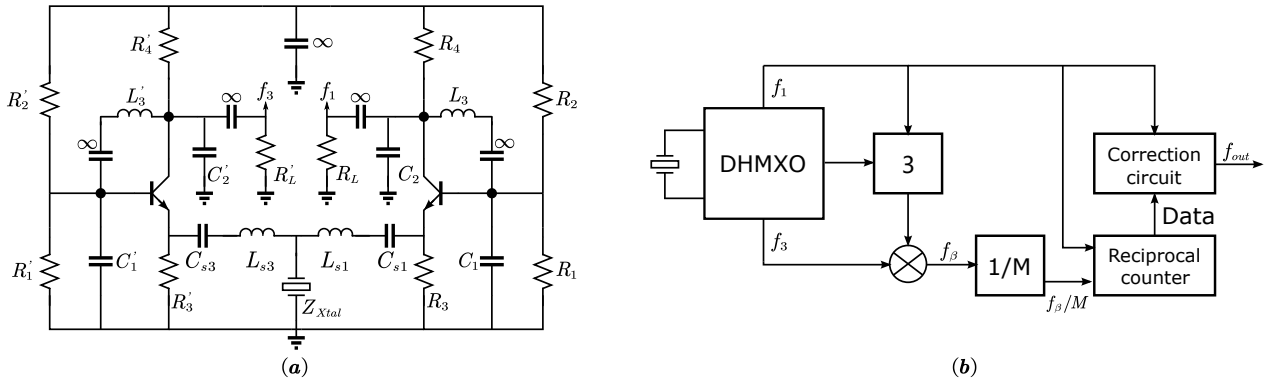


Figure 1.4: (a) A double gain loop DHMXO (Colpitts oscillators). (b) A concept of the MCXO system. Source[23], edited

Theoretically, temperature compensation in the DHMXO performs much better than traditional TCXOs because the information of the frequency change is derived from the crystal itself, rather than from a temperature sensor. However, The implementation of the DHMXO turned out to be a failure. This is mainly because the beat frequency does not solely depend on temperature; it also depends on mechanical stress in the crystal resonator. Apart from a static component, mechanical stress may vary over time and thermal history due to different thermal expansions coefficients of the crystal. Hence, retrace and aging cannot be compensated for if the compensation is solely based upon the instantaneous value of the beat frequency.

The other reason is that the frequency selectivity network in figure 1.4(a) shows a design contradiction in quality factor and selectivity. For high selectivity of resonance frequency, the design of oscillator preferred a high Q band-pass filter to avoid oscillation in undesired frequency. However, the temperature detuning of the analog band-pass filter is much higher than that of the crystal. We will see later that the temperature detuning of the high Q analog band-pass filter significantly deteriorates frequency stability of the oscillator in section 2.1. In this case, applying a low Q frequency selectivity network is the only solution. But the implementation of the low Q analog band-pass filter inevitably sacrifices the selectivity. Therefore, the design of analog frequency selectivity network is not a feasible solution.

1.2 The Multi-Mode Crystal Oscillator

The resonance modi of mechanical resonators such as piezo crystal resonators, ceramic resonators and MEMS resonators depend on the mass, the stiffness, the dimensions, and the mechanical shape of the materials in the resonator. Most of those are accurately fixed by fabrication, but some of them may depend on the operating conditions of the resonator. For example, in crystal resonators, the dimensions of the crystal depend on temperature

and, because to which the crystal is subjected, its stiffness may depend on temperature and lifetime.

Improved correction of the changes in the output frequency of a crystal oscillator could be based upon a state space description of the resonator, in which the parameters are the mass, the stiffness, and the dimensions of all the components used in the crystal resonator.

Direct measurement of these mechanical variables, however, is impractical. If the temperature drift and the retrace are predominantly affected by the dimensions and the stiffness of the crystal, then direct or indirect measurement of these two parameters already provides a solid base for frequency correction, including retrace.

Indirect determination of these mechanical variables may mean that the mechanical variables are determined by means of measurement of the electrical resonance parameters, such as the electrical losses, the equivalent inductance, and the equivalent capacitance of the resonator. In addition, if a change in the value of these variables manifests itself differently for different resonance frequency of the crystal, such indirect determination may as well be achieved by measuring the output frequencies of a multi-mode crystal oscillator. In fact: over an operation region for which these resonance frequencies form an independent set of electrical resonance parameters that maps onto the mass, the stiffness, and the dimensions of the crystal. The correction can be found from a modified state space description of the crystal, in which the mechanical operating states are represented by the resonant frequencies.

In 2018, SemiBlocks B.V. proposed an improved technique so-called *SmartXtal* or *Multi-Mode Crystal Oscillator*(MMXO)[24]. The MMXO determines the output frequency by means of a triple mode oscillator and corrects this by means of an algorithm running on the internal microprocessor. The difference between the 3 frequencies is highly temperature dependent. This relationship is stored during calibration and during operation used by a frequency synthesizer to correct one of the outputs of the triple mode oscillator. The advantage of this is that it uses regular AT-Cut crystals and the whole circuitry can be implemented in silicon, and the frequency selective network is implemented by digital technology. This results in a small and very cost effective, high performance crystal oscillator solution. In addition, the MMXOs has a much wider working temperature range than traditional OCXOs since it does not stabilize temperature to realize frequency accuracy. The current MMXO product and its test-bench is shown in figure 1.5.

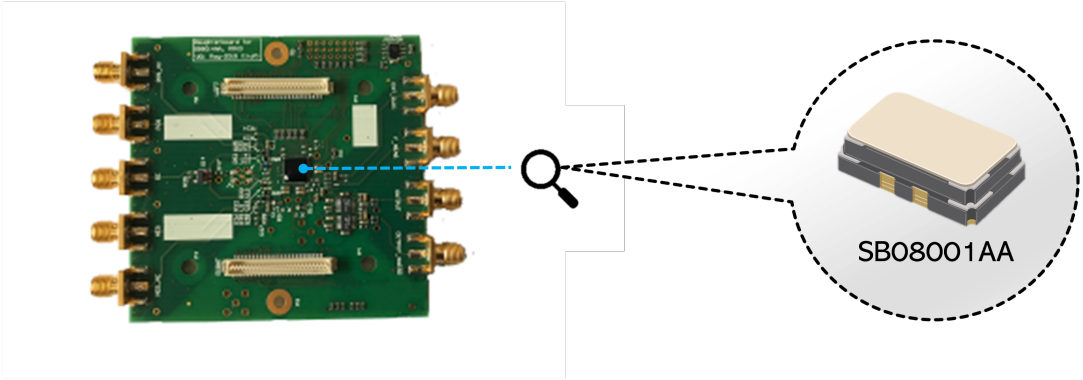


Figure 1.5: First generation MMXO SB08001AA and its test-bench. The package size of MMXO is 6.0 by 6.0 mm, it has 8 pins and a SPI interface. Source[24],edited

Structure (top-level)

The MMXO comprises a solution for an electronic oscillator that uses a mechanical resonator, in which the output frequency of the oscillator is corrected by cascading it with a digitally controlled frequency synthesizer and in which the frequency correction data is obtained from determination of the dominant mechanical parameters of the resonator. Figure 1.6 shows a simplified functional representation of the MMXO [16]. The core of the invention consists of:

- A triple-mode crystal oscillator
- A frequency measurement system
- A frequency validator
- A 3D array implemented in non-volatile memory
- A data interpolator
- A fractional synthesizer

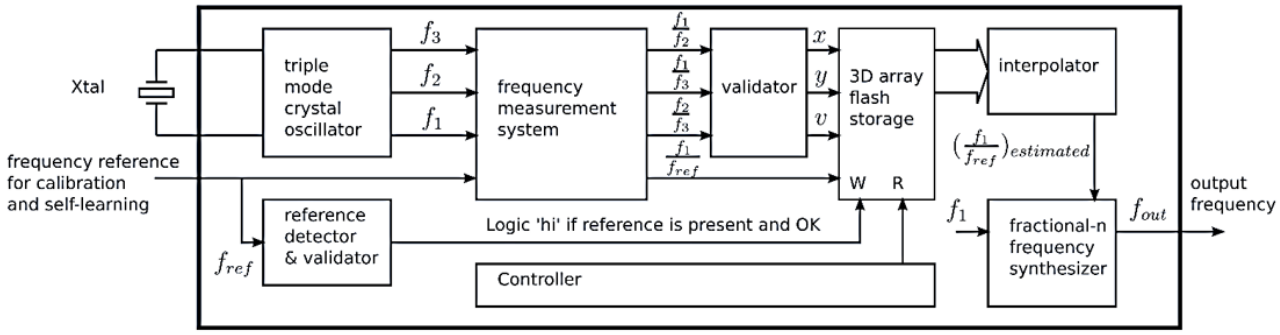


Figure 1.6: Concept structure of the MMXO. Source[16]

One of the frequencies generated by the triple-mode crystal oscillator is selected as the reference frequency for the fractional synthesizer that generates the output frequency. If a high-quality frequency reference signal is applied to the input of the MMXO, it is capable of writing to its memory. The MMXO is then in its self-learning or calibration mode. The frequency measurement system determines the three different ratios of frequencies generated by the triple mode crystal oscillator as well as the frequency correction factor, which is the ratio of the selected base frequency and the reference frequency($\frac{f_1}{f_{ref}}$ in picture1.6)

The frequency correction factor is stored (appended to existing data) together with a timestamp and a weighting coefficient, determined by the validator, at a memory location (x, y) in which x and y uniquely correspond to two ratios of frequencies ($\frac{f_1}{f_2}$ and $\frac{f_1}{f_3}$) generated by the triple-mode oscillator. The memory addresses x and y thus represents the values of the two modified mechanical parameters that correspond to the specific operating conditions of the crystal and that change over time with the applied operating conditions.

With slow and rapid changing operating conditions(e.g. changing temperature) of the MMXO, frequency correction data with time stamps and weighting coefficients are continuously stored at many different memory locations that map onto the many different

operating states of the crystal. This map, obtained two frequencies ratios ($\frac{f_1}{f_2}$ and $\frac{f_1}{f_3}$), is taken as the multiplication factor $\delta(t)$ to correct output frequency.

$$\delta(t) = \begin{bmatrix} \left(\frac{f_1}{f_2}\right)_{10} & \left(\frac{f_1}{f_2}\right)_{11} & \cdots & \left(\frac{f_1}{f_2}\right)_{1t} \\ \left(\frac{f_1}{f_3}\right)_{20} & \left(\frac{f_1}{f_3}\right)_{21} & \cdots & \left(\frac{f_1}{f_3}\right)_{2t} \end{bmatrix} \begin{bmatrix} \phi\,|_1^0 & \phi\,|_2^0 \\ \phi\,|_1^1 & \phi\,|_2^1 \\ \cdots & \cdots \\ \phi\,|_1^t & \phi\,|_2^t \end{bmatrix} \tag{1.2.1}$$

Where (ϕ_1, ϕ_2) are mapped operating states of $\frac{f_1}{f_2}$ and $\frac{f_1}{f_3}$ respectively.

The interpolator estimates the frequency correction data from the data stored in the memory. The fractional synthesizer generates its output frequency from the base frequency and the estimated correction data. The input data for the interpolator is updated with every read cycle. In this way, the output frequency is continuously accurately matched to the original frequency reference.

Oscillation principle

Sustained oscillations in an harmonic oscillator, are obtained by exact compensation of resonator losses. In order to compensate for the losses and achieve stable oscillation, the oscillator is fed with an amplified version of its output signal as shown in figure 1.7(a). A series resonance mode oscillator based on this view of point is shown in figure 1.7(b). Sustained harmonic oscillations are obtained if the transimpedance gain ξ of the amplifier equals the reciprocal value of the crystal's equivalent series resistance for the selected resonance mode, based on the impedance measurements of the crystal.

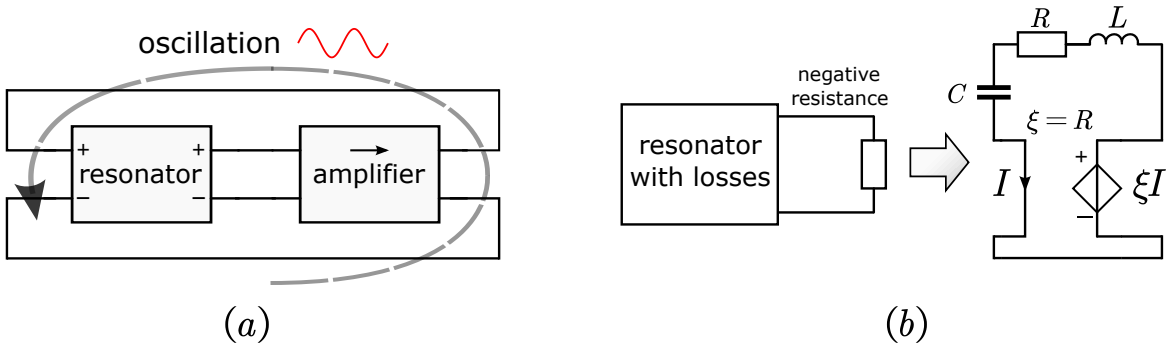


Figure 1.7: (a) Feedback model of an oscillator. (b) Oscillator with non-inverting transimpedance amplifier and series resonator.

The resonator introduces two poles in the loop transfer function $A\beta$. The *Barkhausen conditions* are essential to make sustained oscillations possible. Taking into consideration that $A\beta$ is a complex quantity, the *Barkhausen conditions* is expressed as:

$$|A\beta| = 1 \tag{1.2.2}$$

$$\arg A\beta = 2k\pi, k = \pm 1, \pm 2, \pm 3... \tag{1.2.3}$$

If these conditions are met, the poles of the closed-loop transfer function are exactly on the imaginary axis and the solution of the differential equation is an undamped sinusoid.

Therefore, **a amplitude/phase detection and control system** is indispensable to control the magnitude of the loop gain such that the *Barkhausen conditions* are satisfied at the resonance frequency. In addition, the temperature drift of frequency selective networks in amplifier based oscillators, may seriously limit the achievable temperature stability of an MCXO equipped with it. A **Low-Q and accurate frequency selectivity network is preferred for high-stability MCXOs**.

A large freedom in the selection of resonance modes can be combined with a high temperature stability and with a high spurious suppression in frequency conversion oscillators [16]. Figure 1.8 shows the design of a single resonance loop of MMXO. In such a loop, the resonator (crystal), together with a phase detector and a low-pass filter establish a quadrature frequency detector. The unity-gain limiter between the output of the loop filter and the input of the controlled oscillator, explicitly models a limiting operation on the controlled oscillator's input signal. The $\pi/2$ phase shift defines the frequency operating point of the oscillator. With a linear phase detector, zero output signal is obtained if the phase shift of the resonator is $0 + n\pi$ degrees. With negative feedback, sustained oscillations are found at phase resonance of the crystal.

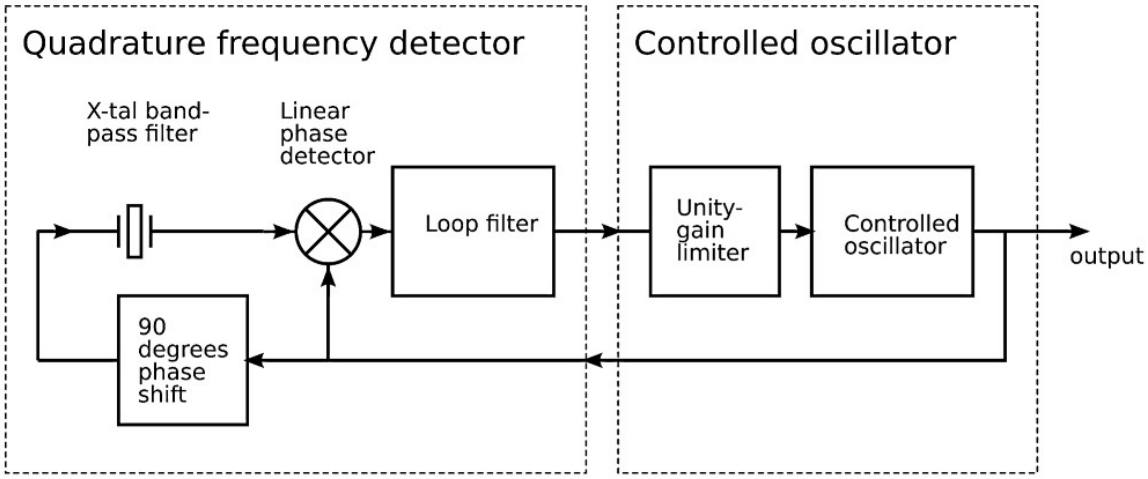


Figure 1.8: A frequency conversion oscillator constructed from a loop of a quadrature frequency detector and a controlled oscillator. Source[16]

Compared to the DHMXO[23], the PLL (Phase-Locked Loop) structure of the MMXO allows the accurate choice of oscillation frequency while not suffering large temperature dependency of analog filter. The frequency error of the MMXO caused by temperature variation is mainly from the output offset of the phase detector[16]. Compared to the design of a low temperature-dependent analog filter, the design of a low temperature-dependent phase detector by digital techniques is much more feasible.

The circuit implementation of MMXO

The circuit implementation of highly-digital frequency-conversion MMXO is shown in figure 1.9. The mixers, filters and NCOs are digital/software blocks that make the crystal oscillate at additional overtones. The "MMXO temperature compensation" is the digital/-software block that keeps the DCO frequency stable, while the individual overtones change over temperature.

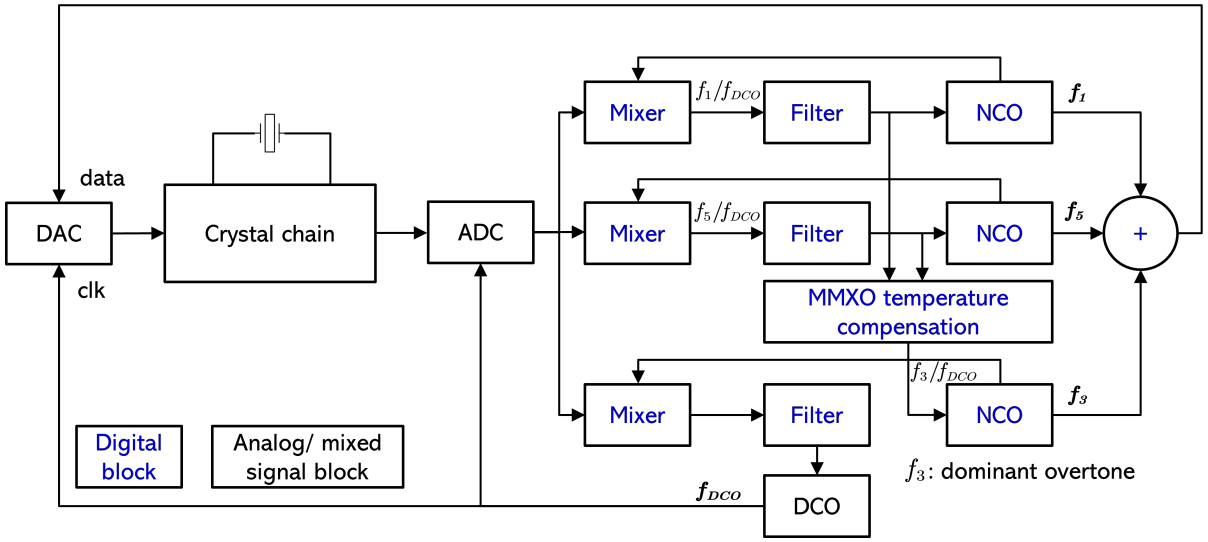


Figure 1.9: Functional circuit implementation of evolved highly-digital frequency-conversion MMXO

	IT3200C [21]	Model 578 [5]	RFPO55 [22]	Model 197 [4]	The MMXO [27]
Type	TCXO	TCXO	OCXO	OCXO	MMXO
Oscillation frequency(MHz)	10 to 40	5 to 52	10 to 26	10	10 to 50
Supply voltage (V)	2.4 to 3.7	3, 3.3 or 5	2.7 to 5.5	5	1.8 or 3.3
Power (mW)	5	4	400	2000	300
Temperature range °C	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 105
Frequency variations over temp. (ppb)	500	280	10	0.2 to 1	10
Phase noise @1 kHz offset (dBc/Hz)	-132	-142	-146	-145	-147
Die area(mm^2)	8	35	141	972	36
Start-up time (ms)	2ms	2ms	4min	5min	1min

Table 1.2: Comparison with current Xtal oscillator products

1.3 Status Quo

The aim of MMXO is to replace OCXO for timing application with lower price and equal performance by using TSMC 40nm CMOS technology instead of an expensive oven. The RFPO55 OCXO[22] , which has 10ppb frequency instability over -40 to 85 °C, has been selected as a reference for the first generation MMXO. A summary of the performances of the MMXO and a comparison with current crystal oscillator products are shown in table 1.2. The design trade-offs are mainly between frequency stability, power consumption, start-up time, and chip size. In order to get high frequency stability, the Xtal oscillators require slow start-up speed, large size, and power consumption.

Although the first generation MMXO achieved the required frequency accuracy in 2020. The measurement result indicated that the large temperature dependent phase shift of the analog crystal chain in figure 1.9 significantly influences frequency stability of the MMXO. This inaccuracy is out of the compensation ability of the multi-mode system since it is highly dependent of the analog network rather than the crystal.

1.4 Scope of the thesis: The CMOS crystal filter

Objective

To improve the next generation MMXO product, SemiBlocks B.V. plans to explore the potential of decreasing frequency instability of MMXO by further research of the mechanism behind the crystal chain. This CMOS circuit network's function is to accurately transform crystal's physical property into electrical quantity. In other words, it behaves like an accurate filter for crystal. Therefore, *CMOS crystal filter* is named for the crystal chain.

The content of this thesis project is to design a crystal filter based on TSMC 40nm technology. The CMOS crystal filter should reflect the characteristic of the crystal accurately. Any change of resonance frequency of the tested crystal should accurately match that of the frequency characteristic of the crystal filter. In other words, any temperature change, or the change of operating condition of the electronics of the crystal filter, should not affect this matching accuracy. The objective is to control frequency error below 10ppb for the three resonance tones of the tested crystal over -40 to 100 °C.

SemiBlocks require no other hard specifications. From an engineer's perspective, we do our best efforts based on a solid understanding of related knowledge and predict feasible solutions before implementing the design. Following this belief, the specifications are discussed and given in section 3.3 after study of the concept.

Test-bench

The provided test-bench are AD-FMCDAQ2-EBZ AD/DA converter evaluation boards[6][7]. The crystal applied for analysis and measurement is according to the data provided in the technical document [27]. This crystal has three resonance frequencies around 16MHz(the base tone), 48MHz(the third overtone), and 80MHz(the fifth overtone). Since the third overtone is the reference/dominant frequency in the former MMXO system, it is taken as the example overtone for most of analysis in this paperwork. Figure 1.10 shows the crystal filter with DA/AD converter developed from analog block of figure 1.9.

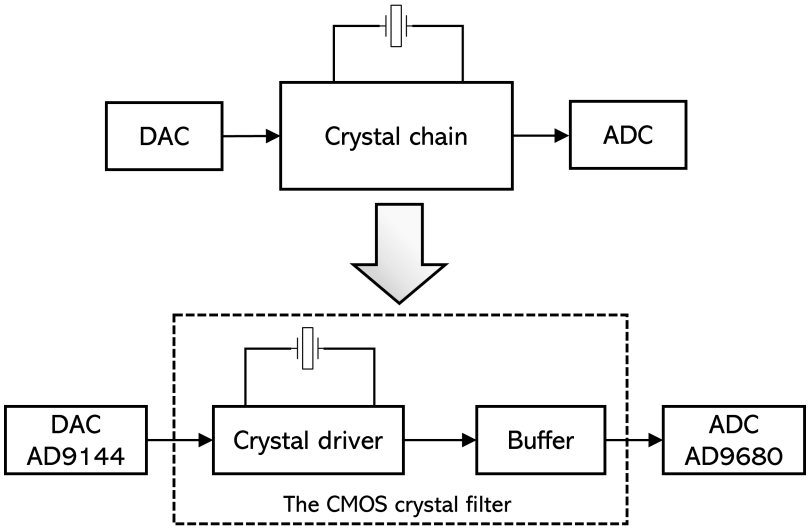


Figure 1.10: Model of crystal filter with AD/DA converters

Design approach

The design approach applied in this thesis project is Structure Electronic Design (SED)[18]. SED uses proper sequencing and orthogonalization of design steps, based on solid principles from physics, information processing, control theory, and network theory. It provides a hierarchically structured top-down design method with a bottom-up awareness [18].

According to SED, the design of an analog amplifier is flamed into noise, drive capability, bandwidth and accuracy, frequency compensation, and biasing. SED carefully considers the order of those procedures and keeps their interaction as low as possible. Once a decision is made in a certain procedure, it should not affect the new decision in the next phase. In this case, the design risks do not propagate over phases. For a more detailed study, please refer to the book [*Structure Electronics Design*] of A.J.M. Montagne[18].

Thesis structure

This project includes seven chapters and one appendix. The system design in chapter 2 and 3 cover the study of crystal characteristics and the discussion of series and parallel working mode of crystal. The system structures of the crystal filter are explored and assessed based on the study of crystal, to select a feasible solution and set up corresponding specifications. All steps and decisions to design the crystal filter are presented in chapter 4 and 5. The results in Chapter 6 include the relevant simulations and analysis of the overall system. Based on the knowledge from the existing design, some suggestions are proposed to effectively improve the crystal filter without changing the design structure. The discussions in chapter 7 summarise those results and propose suggestions for future works.

Design tool

This thesis combines the simulations in Cadence together with SLICAP (Symbolic Linear Circuit Analysis Program). SLICAP is mainly for the system design. The design of controller and verification is finished with Cadence.

SLICAP [17] is an open-sourced symbolic simulator package based on Python and MATLAB. It has the following functions:

- Calculate design equations
- Calculate Laplace transfer functions.
- Powerful noise analysis
- Enable analysis among time-domain and S-domain for both Cartesian and Polar coordinate systems.
- Symbolic and numeric variance analysis for determination of budgets for biasing imperfections.

The input of SLICAP is a SPICE netlist document. SLICAP has built-in parameterized sub-circuits with small-signal models of active devices. Operating conditions and device geometry parameters can be passed to these sub-circuits, while technology-specific parameters and device equations are defined within the sub-circuit. The parameters of the small-signal device model are calculated from the device equations in the sub-circuit. SLICAP is preferred over traditional SPICE simulation software, such as LTspice and Cadence, as

an initial circuit design tool. The compatible functions of SLICAP for both symbolic and numeric analysis help users quickly find the early design solution and show-stopper before engaging in detailed circuit design. It facilitates the engineering process from the early stage of design and promotes knowledge understanding of designers.

CHAPTER 2

Technology profile

In this chapter, we will introduce the technology profile as preparation work for the crystal filter design. In addition, this chapter covers the necessary knowledge of crystal characteristics, the modeling results of transistors of TSMC 40nm technology, and essential parameters of the AD/DA test-bench and bonding.

2.1 Crystal characteristic

The electrical characteristic of a crystal can be modeled as an electrical network as shown in figure 2.1. The impedance of this network can be written as:

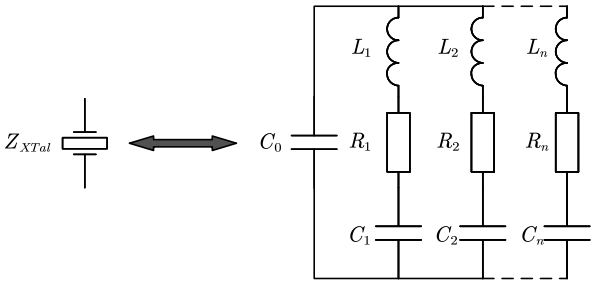


Figure 2.1: The equivalent circuitry of crystal

$$Z(s) = \left(\frac{1}{sC_0}\right) || \left(\frac{1}{sC_n} + sL_n + R_n\right) \tag{2.1.1}$$

It can be transformed to:

$$Z(s) = \frac{s^2 + s\frac{R_n}{L_n} + \omega_s^2}{(sC_0)\left(s^2 + s\frac{R_n}{L_n} + \omega_p^2\right)} \tag{2.1.2}$$

Based on the impedance of crystal, there are two working modes to drive the crystal, which are series resonance mode and parallel resonance mode. Figure 2.2 shows the ideal circuity to drive a crystal in series(b) and parallel(a) resonance mode. In series resonance mode, a

voltage source drives the crystal and the current output is measured. The transfer function of series resonance mode is:

$$Y_{vs} = \frac{I_{out}}{V_{in}} = \frac{1}{Z\left(s\right)} = \frac{\left(sC_0\right)\left(s^2 + s\frac{R_n}{L_n} + \omega_p^2\right)}{s^2 + s\frac{R_n}{L_n} + \omega_s^2} \tag{2.1.3}$$

In parallel resonance mode, a current source drives the crystal and the voltage output is measured. The transfer function of parallel resonance mode is:

$$Z_{vp} = \frac{V_{out}}{I_{in}} = Z\left(s\right) = \frac{s^2 + s\frac{R_n}{L_n} + \omega_s^2}{\left(sC_0\right)\left(s^2 + s\frac{R_n}{L_n} + \omega_p^2\right)} \tag{2.1.4}$$

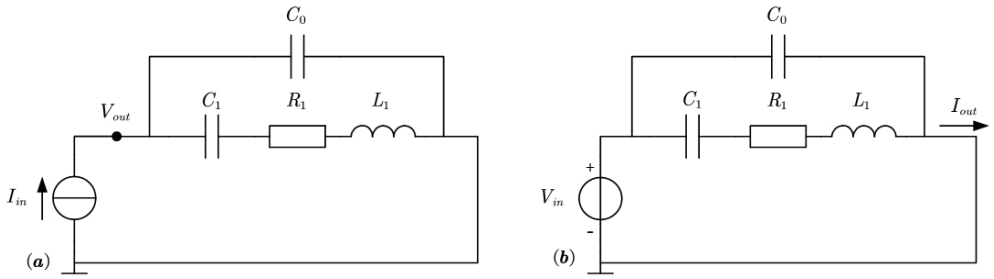


Figure 2.2: Ideal circuity to drive a crystal in series(b) and parallel(a) resonance mode

The gain plot of series and parallel resonance mode is shown in figure 2.3. We could observe that two frequencies correspond to the extreme gain magnitude and zero phase shift in both modes. The two frequencies are series and parallel resonance frequency. In series resonance mode, the gain in the series resonance frequency is much higher than the gain at the parallel resonance frequency. On the contrary, the gain at the series resonance frequency is much lower than the gain at the parallel resonance frequency in parallel resonance mode. At first glance, there are four solutions to drive a crystal. Crystal can work either at series resonance frequency or parallel resonance frequency for both resonance modes. Section 3.2 will further discuss the design choices.

Series and parallel resonance frequency

According to Eq 2.1.2, Eq 2.1.5 provides symbolic expressions for series and parallel resonance frequency. The series angular resonance frequency is the root of the ratio of the nonzero coefficient of the lowest order and highest order of s of the numerator of Eq 2.1.2. Similarly, the parallel angular resonance frequency can be derived in this way. The lowest series/parallel frequency is the fundamental frequency of crystal resonator, the other resonance frequencies are corresponding overtones. They are approximately odd multiples of the fundamental frequency.

$$\omega_s = \sqrt{\frac{1}{L_n C_n}}\ ; \omega_p = \sqrt{\frac{C_n + C_0}{L_n C_0 C_n}} = \omega_s\sqrt{1 + \frac{C_n}{C_0}} \tag{2.1.5}$$

Actually, Eq 2.1.5 are simplified equations to calculate resonance frequencies. According to the definition of resonance frequency, the phase shift of voltage and current through the

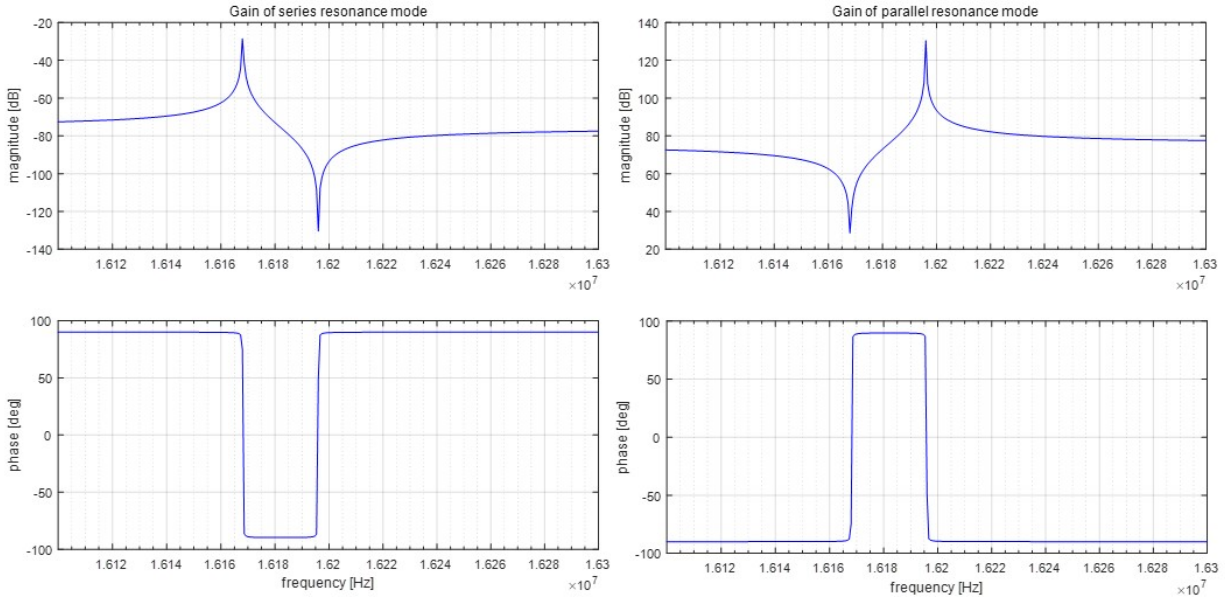


Figure 2.3: Gain of series and parallel resonance mode

crystal equals zero . Since the symbolic expressions of the accurate definitions are complex, Eq 2.1.5 is suited to estimate resonance frequencies. Since $\frac{C_n}{C_0} \ll 1$, series resonance frequency and parallel resonance frequency are close to each other.

Quality factor analysis

Quality factor Q is a decisive factor of frequency stability. Its effect could be explained by figure 2.4, which illustrates the difference between high Q and low Q systems. Assuming outside electronics cause a temperature-dependent phase shift, the high Q system suffers fewer frequency variations than the low Q system. Therefore, maintaining a low phase shift caused by outside electronics and a high Q factor of crystal is critical to achieve high frequency stability.

Two definitions exist for quality factor: one is based on energy loss, while the other uses resonance frequency and bandwidth. Basic physics defines the Q as equation 2.1.6. The quality factor relates the maximum or peak energy stored in the circuit (the reactance) to the energy dissipated (the resistance) during each cycle of oscillation.

$$Q = 2\pi \frac{energy\ stored}{energy\ disppated\ per\ cycle} \tag{2.1.6}$$

Resonant circuit normally exhibits a bandpass transfer function as shown in figure 2.5. The ”sharpness” of the magnitude of the frequency response is defined as the quality factor of the circuit. More specifically, Q is defined as the resonance frequency divided by the two-side -3dB bandwidth as equation 2.1.7.

$$Q = \frac{f_0}{f_2 - f_1} = \frac{f_{resonance}}{BW} \tag{2.1.7}$$

According to equation 2.1.6 and the crystal structure as shown in figure 2.1. Quality factor

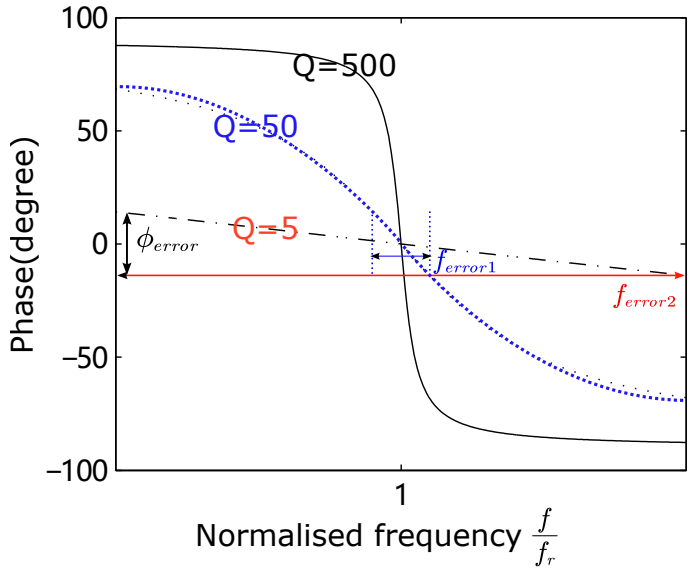


Figure 2.4: Comparison of frequency sensitivity between low Q and high Q system, Source:[26] edited

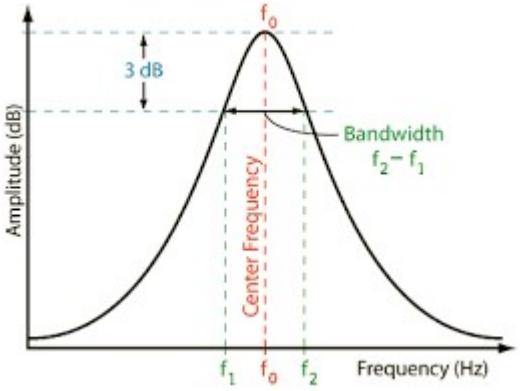


Figure 2.5: A definition of Q

of crystal at series resonance frequency could be calculated as:

$$Q_s = \frac{\omega_s L_n}{R_n} = \frac{1}{R_n}\sqrt{\frac{L_n}{C_n}} \tag{2.1.8}$$

The derivation of quality factor Q_p for parallel resonance frequency is shown in Appendix. For large Q_s, the quality factor at both resonance frequency are almost equal since the term $\frac{1}{Q_s}\frac{C_0^2}{C_n^2}$ is negligible compared to Q_s. In later analysis, we will assume $Q_p = Q_s$.

$$Q_p \approx Q_s + \frac{1}{Q_s}\frac{C_0^2}{C_n^2} \tag{2.1.9}$$

Equivalent parallel resistance R_p

At series resonance frequency, the resonance is determined by the branch of C_n,R_n , and L_n. At parallel resonance frequency, the shunt capacitance C_o interacts with the inductive branch of C_n,R_n , and L_n. The parallel LC resonance introduces a much larger equivalent

resonance resistance. Based on $Q_s = Q_p$, the equivalent parallel resistance R_p could be calculated from R_n. The transformation process is shown in figure 2.6, L_p and C_p cancel out each other at parallel resonance frequency. R_p behaves as an equivalent resistance to present power loss.

$$\begin{aligned} Q_s = Q_p \Rightarrow \omega_p R_p^{'} C_p &= \frac{\omega_s L_n}{R_n} \\ R_p &= \frac{L_n C_n}{R_n C_0 \left(C_0 + C_n\right)} \end{aligned} \tag{2.1.10}$$

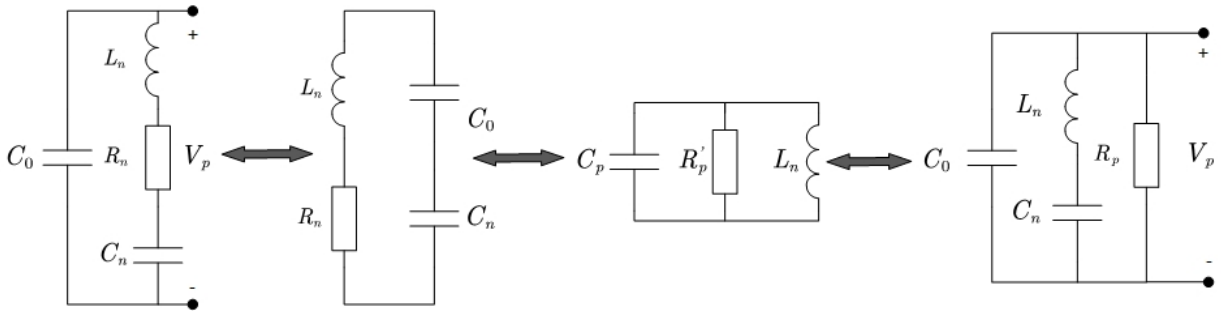


Figure 2.6: Equivalent circuitry of crystal in parallel resonance mode

Section A(Appendix) shows the derivation of R_p and its related power budget. Table 2.1 shows the basic parameters of the tested crystal. There is a huge difference of R_p among the three tones at the parallel resonance frequency. In later analysis, we will see this large variation causes many unbalanced design budgets for parallel resonance frequency.

	f_r[Hz]	R_n[Ω]	C_n[fF]	L_n[mH]	C_0[pF]	Q	R_p[Ω]
The base tone	16.05M	6.14	5.78	16.99		2.8×10^5	5854000
The third overtone	47.93M	52.33	0.5	22.05	1.65	1.27×10^5	77362
The fifth overtone	79.96M	308.1	0.15	26.15		4.28×10^4	4675

Table 2.1: Basic parameters of the tested crystal. Source[27]

Conclusion

Based on the above analysis, we find several possible options to drive the crystal. Because the design aims at a low frequency error, it is important to further explore the relations between quality factor and frequency error. In this case, we introduce the definition of detuning v to describe the performance of crystal around resonance frequency.

$$v = \frac{\omega}{\omega_r} - \frac{\omega_r}{\omega} \approx \frac{2\Delta\omega}{\omega_r} \tag{2.1.11}$$

where $\Delta\omega = \omega - \omega_r$ is the frequency offset from the angular resonance frequency ω_r. A 1 percent frequency off set from resonance corresponds to about 2 percent relative detuning

v. The relation between the resonator's relative detuning v and its phase shift ϕ can be found as

$$\phi = \arctan(vQ) \Longleftrightarrow v = \frac{1}{Q}\tan\phi \tag{2.1.12}$$

A small phase shift error $\phi \ll 1^{\circ}$ causes a detuning that can be obtained as:

$$v = \frac{\phi}{Q} \Longleftrightarrow \frac{\Delta f}{f_r} = \frac{\phi}{2Q} \tag{2.1.13}$$

According to equation 2.1.13 , we find two causes of frequency error $\frac{\Delta f}{f_r}$:
1. Phase shift in the loop amplifier.
2. Deviation of the quality factor from its desired value.

As an example, one degree phase shift error and a quality factor of 10^5 for the crystal resonator, result in a detuning v of 175 [ppb], which corresponds to a relative frequency error $\frac{\Delta f}{f_c}$ of 87.5[ppb].

The characteristic of crystal indicates several important insights. The key points are highlighted in following lines:

- According to the transfer function of crystal, there are two working modes (series and parallel resonance mode) of crystal. For each mode, there are two resonance frequencies (series and parallel resonance frequency) with almost equal quality factor.
- Although the quality factors of the two resonance frequencies are almost equal, the variation of resonance resistance at parallel resonance frequency among the three tones is huge.
- The quality factor of crystal and the phase shift caused by outside electronics directly influences its frequency sensitivity. In order to acquire a high frequency stability, the design needs to have a high quality factor and a low temperature dependent phase shift.

Now we can understand why the DHMXO in figure 1.4(a) is not a feasible solution. Consider a frequency selective LRC network with a quality factor Q_{sel} is inserted into the amplifier loop. Assume it has been tuned to the desired overtone frequency of a crystal resonator. Now, also assume v_{sel} is the detuning of this network due to temperature variations. With the aid of equation 2.1.13, the detuning of the crystal oscillator can then be described as [16]:

$$v_{osc} = \frac{Q_{sel}}{Q_{osc}} v_{sel} \tag{2.1.14}$$

in which Q_{osc} is the quality factor of the crystal.

Expression 2.1.14[16] states that the detuning of an harmonic crystal oscillator with a band-pass filter for mode selection, equals that of its mode selection band-pass filter times the ratio of the quality factor of that filter and the quality factor of the crystal resonator. Consider for example a band-pass filter with a quality factor of 30, and a temperature detuning of 0.002 [1/K]. If the crystal's quality factor at the selected resonance mode equals 10^5, the frequency selective network contributes 300 [ppb/K] to the frequency drift of the crystal oscillator. If the temperature dependent detuning of this network is not matched to that of the crystal, this figure can be regarded as the upper limit of the frequency stability of an MCXO equipped with it. Therefore, instead of using analog band-pass filter, the MMXO applies highly digital frequency conversion technique as shown in figure 1.8 to achieve low-Q and high stability.

2.2 Transistors modelling in SLICAP

The design of amplifiers in SLICAP needs the data of transistors. The EKV model is applied in SLICAP to mimic the characteristic of transistors. Enz and Vittoz developed this model and first applied it in their paper[8] in 1996. This model describes characteristics of transistors by different inversion levels. It also considers the influence of the second-order parameters of MOS transistors, such as the channel length modulation(CLM), the velocity saturation, and the vertical field mobility reduction (VFMR) to get enough accuracy in early-stage design. For the detailed description of transistor modeling, please refer to the former work [28] of the author.

Table 2.2 shows the basic device parameters for MOS transistors in the EKV model. With these parameters and all the methods introduced in the report[28] and book[18], the characteristic of a MOS transistor could be built by the EKV model.

Parameters	**Unit**	**Description**
V_t	V	threshold voltage
θ	V^{-1}	vertical field mobility reduction coefficient
E_{CRIT}	$\mathrm{V/m}$	lateral field strength for velocity saturation
n	$-$	substrate factor
μ_0	m^2/Vs	zero field carrier mobility
C_{jbo}	$\mathrm{F/m}$	gate-bulk overlap capacitance
C_{gso}	$\mathrm{F/m}$	gate-source and gate-drain overlap capacitance
C_{jbo}	$\mathrm{F/m}^2$	source/bulk drain/bulk capacitance
L	m	length of drain and source
t_{ox}	m	oxide thickness
V_{AL}	$\mathrm{V/m}$	Early voltage per unit of length
KF	$-$	flicker noise coefficient
AF	$-$	flicker noise coefficient

Table 2.2: MOS device parameters for EKV2.6 model. Source[18]

Figure 2.7 shows a comparison of transistor characteristics generated from the EKV model (SLICAP) and the BSIM4 model (Cadence). The interested characteristics are small signal parameters and the noise spectrum. The adjustment is made by comparing graphs from Cadence and SLiCAP until they basically match. Table 2.3 summarizes the EKV model parameters after transformation for eight basic MOS transistors in TSMC 40nm technology.

Transistors	V_t	θ	E_{CRIT}	n	μ_0	C_{jbo}	C_{gso}	C_{jbo}	L	t_{ox}	V_{AL}	KF	AF
RFNMOS2.5	0.4	0.2	6.4m	1.32	55m	0	1p	1m	270n	6.3n	100m	2e-23	0.86
RFPMOS2.5	-0.4	0.35	25m	1.35	19m	0	0.6p	1m	270n	5.9n	80m	7e-24	1.1
RFNMOS1.1	0.47	0	20m	1.6	18.1m	0	47p	1m	40n	2.05n	40m	2.8e-24	0.91
RFPMOS1.1	-0.43	0	24m	1.62	6.8m	0	26p	1m	40n	1.8n	120m	3e-23	1.1
nch2.5	0.4	0.2	6m	1.32	63m	0	1p	1m	270n	6.9n	100m	2e-23	0.86
pch2.5	-0.42	0.35	27m	1.35	21m	0	0.6p	1m	270n	6.6n	100m	9e-25	1.1
nch1.1	0.47	0	20m	1.6	24.5m	0	47p	1m	40n	2.8n	40m	1.8e-24	0.91
pch1.1	-0.43	0	23m	1.62	9.8m	0	26p	1m	40n	2.5n	120m	2e-23	1.1

Table 2.3: Technology parameters of some transistors after transformation. Source[28]

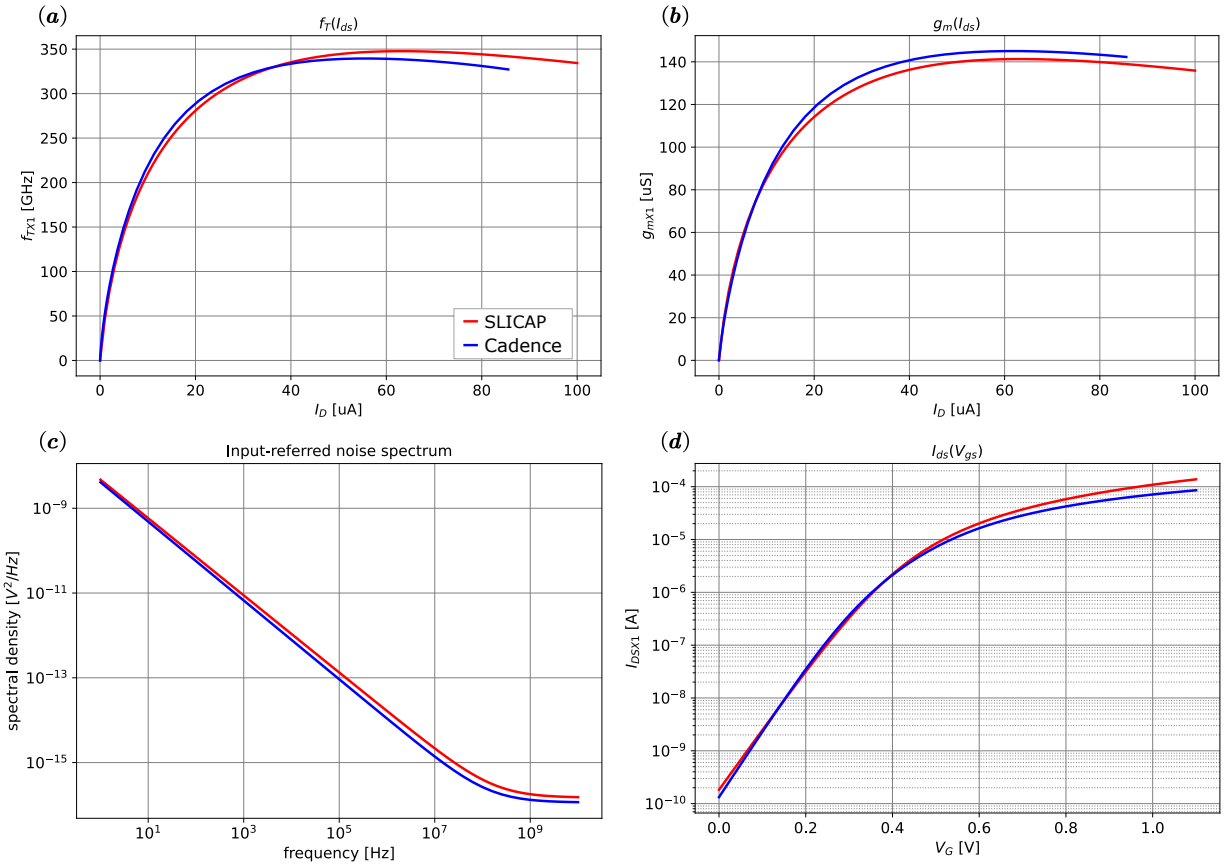


Figure 2.7: The characteristic curves of a smallest size (W=120n, L=40n) N-channel MOS transistor with highest V_{DS}=1.1V in TSMC 40nm technology. (a) f_T versus I_D. (b) g_m versus I_D. (c) input-referred PSD of voltage noise. (d) I_D versus V_{DS}. The red and blue trace in all graphs is obtained with the EKV model and the BSIM4 model, respectively. The adjustment process is repeated for the PMOS transistors and 270nm transistors with highest V_{DS}=2.5V. Because the process-related data is confidential, the information of tuned parameters is not listed. Source[28]

2.3 Important technology parameters

Bonding

In addition to the parameters of transistors from TSMC 40nm technology, the parameters of bonding are also important since the bondwires and bondpads are directly connected with the tested crystal, which cannot be isolated by the amplifier. Later we will see they have a certain influence on the performance of the crystal filter. Paper [19] [20] [25]provide a method to estimate the parasitics of bonding, which is based on the shape of bondpads and bondwires. Combined with the data provided by TSMC 40nm technology. We may assume inductance L_w of bondwire approximates 1.5nH and capacitance C_w of bondpad approximates 35fF.

Test-bench

The specifications set-up of the crystal filter needs the parameters of test-bench. Table 2.4 summarizes the important technology parameters of the tested AD/DA converter[6][7].

AD9144 (DAC)	AD9680 (ADC)
Resol: 16bits Output impedance: differential 100Ω Full-scale output range: (0,1)V RMS Maximum sample rate: 2.8GSPS	Resol: 14bits/ ENOB: 11bits Input impedance: differential 100Ω Full-scale input range: (0.48,0.64)V RMS Maximum sample rate: 1.25GSPS Input full power bandwidth: 2GHz

Table 2.4: Important parameters of the tested AD/DA converter. Source[6][7]

CHAPTER 3

System design

3.1 Working principle of the crystal filter

The analysis of crystal characteristic shows the importance of the quality factor and phase shift to frequency stability. In the ideal case, we expect the source to load transfer behaves like figure 2.2 so that there is no loss of quality factor and no extra phase shift caused by outside electronics. However, the outside electronics, such as the source and load impedance, will inevitably affect frequency stability. The model of crystal with outside electronics is shown in figure 3.1. L_m, C_m and R_m stands for the parasitics of outside electronics.

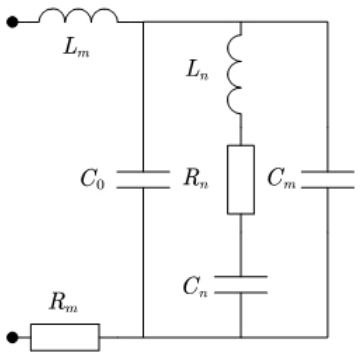


Figure 3.1: Crystal model with outside electronics

To get some intuitions, we first assume L_m and C_m are negligible compared with the intrinsic L_n and C_n of crystal. In series resonance, a 100Ω input/output impedance R_m can cause the Q of the third overtone around 2 times lower and that of the base tone around 20 times lower! According to equation 2.1.13, there is a large frequency error introduced. **Therefore, we need to design a crystal filter to isolate/nullify the influence of the outside electronics.** Figure 3.2 shows a transadmittance amplifier structure for series resonance mode. As a result, the series outside electronics are isolated by the nullor and have no effect on the intrinsic transfer of crystal.

However, the design of amplifier always introduces extra noise as shown in figure 3.2(b). In addition, a non-ideal controller has its port impedance and also causes a phase shift, which affects the frequency stability. These influences are exactly what we should consider for the design of a low noise, low frequency error crystal filter.

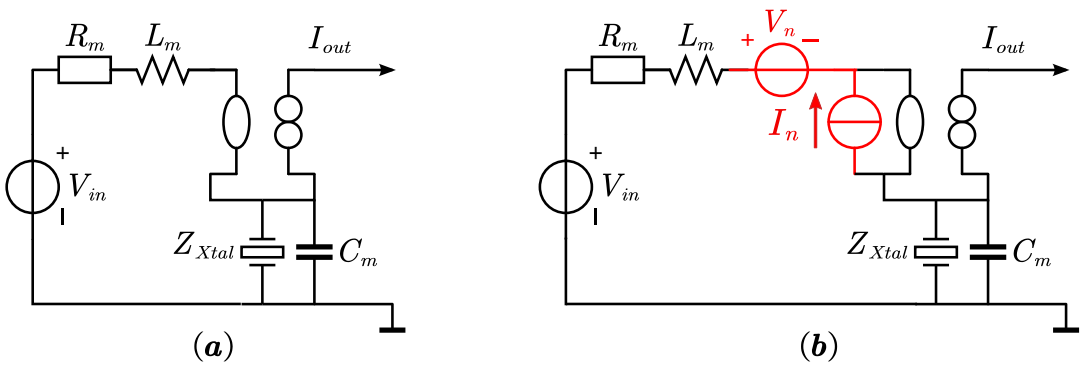


Figure 3.2: (a) Apply a transadmittance amplifier as the crystal filter to isolate the series outside electronics. (b) The controller adds extra noise sources.

3.2 Discussion of structures and working frequency

Based on the expected performance of the crystal filter and the characteristic of the system, we develop the concept from figure 1.10 to figure 3.3. As we have mentioned in section

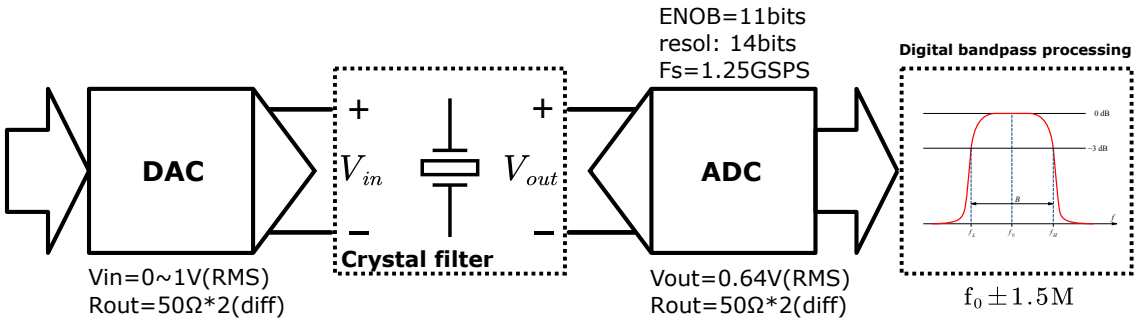


Figure 3.3: Crystal filter with AD/DA converter and a band-pass filter. This figure is updated from figure 1.10. The test-bench are AD-FMCDAQ2-EBZ AD/DA converter evaluation boards which provides differential input/output. The available technology is TSMC40nm(1.1V) and 270nm(2.5V). The band-pass filter is a digital processing to choose the signal around resonance. Because AD/DA converter provides voltage output/input respectively, the design of the crystal filter should provide corresponding voltage input/output.

2.3[Important technology parameters], the bondwires and bondpads are directly connected with the tested crystal, which cannot be isolated by the amplifier. Therefore, there are some useful insights by considering the influence of bonding before we start to design the structure of the crystal filter. As shown in figure 3.1, L_m and C_m can be modelled as the bondwire inductor L_w and bondpad capacitance C_w, respectively. At series resonance frequency, assuming there is a αL_w change of bondwire inductor over -40 to 100 °C. We can derive the budget for α if the total frequency error should be less than 10ppb:

$$\frac{\Delta f_s}{f_s} = \left| \frac{\sqrt{\frac{1}{(L_n+L_w)C_n}} - \sqrt{\frac{1}{[L_n+(1+\alpha)L_w]C_n}}}{\sqrt{\frac{1}{(L_n+L_w)C_n}}} \right| < 10^{-8} \tag{3.2.1}$$

Similarly, if there is a βC_w change of bondpad capacitor at parallel resonance frequency, we can derive the budget for β if the total frequency error should be less than 10ppb:

$$\frac{\Delta f_p}{f_p} = \left| \frac{\sqrt{\frac{1}{(L_n+L_w)C_n}\left(1+\frac{C_n}{C_0+C_w}\right)} - \sqrt{\frac{1}{[L_n+(1+\alpha)L_w]C_n}\left(1+\frac{C_n}{C_0+(1+\beta)C_w}\right)}}{\sqrt{\frac{1}{(L_n+L_w)C_n}\left(1+\frac{C_n}{C_0+C_w}\right)}} \right| < 10^{-8} \qquad (3.2.2)$$

According to Eq 3.2.1 and 3.2.2, Fig 3.4 (A) and (B) show the total frequency error of the third overtone versus α and β at series and parallel resonance frequency, respectively. The series resonance frequency is much less sensitive to parasitics compared to the parallel resonance frequency, which is highly dependent on the shunt capacitor. From this point of view, we may see series resonance frequency shows its better performance. If the temperature coefficient of β is too large, we can find the show-stopper for working at parallel resonance frequency. Since there are no materials to know the temperature coefficient of bonding, we can not judge that driving crystal at parallel resonance frequency is not feasible. Next, we will discuss the feasibility of optional structures of the crystal filter and assess their performance at series and parallel resonance frequency.

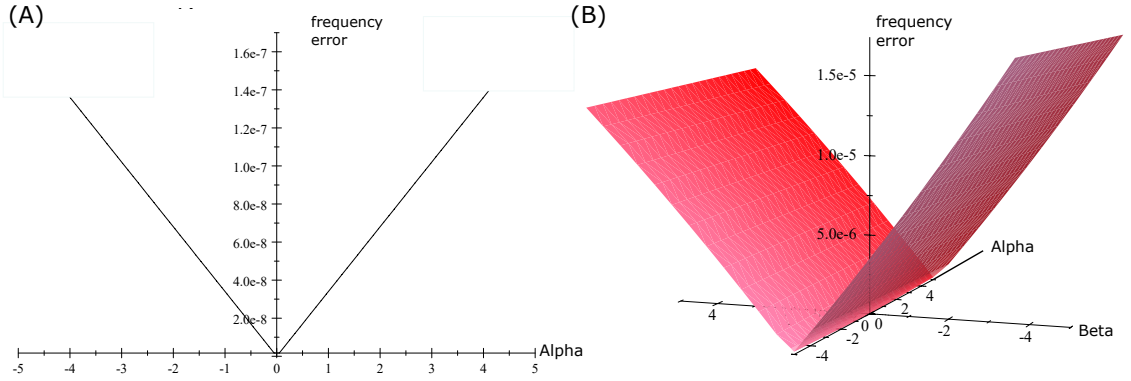


Figure 3.4: (A)Total frequency error of the third overtone versus α at the series resonance frequency. (B)Total frequency error of the third overtone versus α and β at the parallel resonance frequency.

Voltage amplifier

Figure 3.5 shows the voltage amplifier configuration of the crystal filter. Its transfer function $V_{out}/V_{in} = 1 + 2Z_f/Z_{XTal}$ shows that it is a series resonance mode. Because the AD/DA test-bench provides voltage output/input respectively, the design of the crystal filter should provide corresponding voltage input/output. The main design difficulty for the voltage amplifier configuration is that there is an extra "+1" term in the transfer function. This "+1" term needs to be compensated by a digital feedback loop with AD/DA converter, which is not the design interest of this thesis. Another method is to compensate the "+1" term by extra analog stage, which changes the design of a voltage amplifier to a multiple-stage amplifier, such as transadmittance + transimpedance amplifier.

Transadmittance + Transimpedance

Figure 3.6 shows the Transadmittance(TA) + Transimpedance(TI) configuration for the crystal filter. Its transfer function $V_{out}/V_{in} = 2Z_f/Z_{XTal}$ shows that it is a series resonance mode.

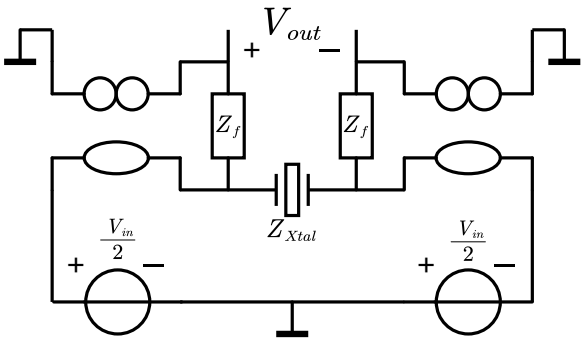


Figure 3.5: Voltage amplifier configuration of the crystal filter

The dual amplifier structures decouple the design for noise and frequency stability. In the transadmittance amplifier, we design the input stage with high gain and boost the bandwidth by its output stage. In the transimpedance amplifier, we design the output stage with high gain to get the required drive capabilities and boost the bandwidth by its input stage. Since the two amplifiers are cascaded, the bandwidth of the final design is large if both of them have large bandwidth.

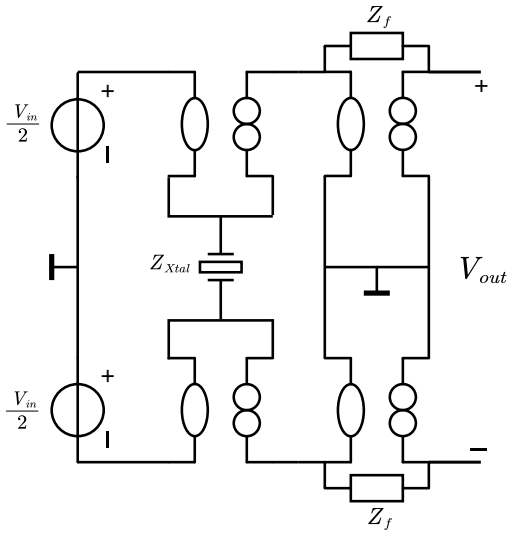


Figure 3.6: Transadmittance + Transimpedance configuration of the crystal filter (the nullor is assumed to be a two stage controller).

The next step is to explore the choices between series and parallel resonance frequency. The crystal filter in the current MMXO product works at series resonance frequency with resistive feedback. Because the shunt capacitor C_0 leads to a large transfer in high frequency, There was an aliased noise from ADC above 1GHz which deteriorates the noise figure of the fifth overtone. For exploring feasible structures to avoid aliased noise, the application of capacitive feedback is included in this discussion.

Combined with the data of crystal in table 2.1, the transfer function of TA+TI configuration could be expanded according to different overtones. Equation 3.2.3 shows the result for resistive TI feedback at series and parallel resonance frequency. Equation 3.2.4 shows the result for capacitive TI feedback at series and parallel resonance frequency.

$$\text{Series}\begin{cases} A_{vn.1st} = \frac{2R_f}{R_{n1}} = \frac{2R_f}{6.14} \\ A_{vn.3rd} = \frac{2R_f}{R_{n3}} = \frac{2R_f}{52.33} \\ A_{vn.5th} = \frac{2R_f}{R_{n5}} = \frac{2R_f}{308.1} \end{cases} \quad \text{Parallel}\begin{cases} A_{vp.1st} = \frac{2R_f}{R_{p1}} = \frac{2R_f}{5.85e6} \\ A_{vp.3rd} = \frac{2R_f}{R_{p3}} = \frac{2R_f}{7.74e4} \\ A_{vp.5th} = \frac{2R_f}{R_{p5}} = \frac{2R_f}{4.68e3} \end{cases} \tag{3.2.3}$$

$$\text{Series}\begin{cases} A_{vn.1st} = \frac{1}{\pi C_f f_1 R_{n1}} = \frac{1}{6.14\pi f_1 C_f} \\ A_{vn.3rd} = \frac{1}{\pi C_f f_1 3 R_{n3}} = \frac{1}{157\pi f_1 C_f} \\ A_{vn.5th} = \frac{1}{\pi C_f f_1 5 R_{n5}} = \frac{1}{1540\pi f_1 C_f} \end{cases} \quad \text{Parallel}\begin{cases} A_{vp.1st} = \frac{1}{\pi C_{fp} f_1 R_{p1}} = \frac{1}{5.85e6\pi C_f f_1} \\ A_{vp.3rd} = \frac{1}{\pi C_{fp} 3 f_1 R_{p3}} = \frac{1}{2.32e5\pi C_f f_1} \\ A_{vp.5th} = \frac{1}{\pi C_{fp} 5 f_1 R_{p5}} = \frac{1}{2.34e4\pi C_f f_1} \end{cases} \tag{3.2.4}$$

Table3.1 shows a simple version of a decision matrix for crystal filter. '✗' means a show-stopper, more '✓' means better performance. The following lines explain the arguments for the assessments:

Working frequency	Feedback of TI	Dynamic range	Noise figure	Aliased noise	SNR	Power consumption	Frequency stablility
Series	Resistive	Best	✓✓	✓	✓	✓	✓✓
	Capacitive	✓	✓	✓✓	Best		✓
Parallel	Resistive	✗	Best	✓	✗	✓✓	✓✓
	Capacitive	✓	Best	✓✓	✗		✓

Table 3.1: Decision table of the TA+TI configuration

- **Dynamic range**: In resistive feedback, the parallel resonance frequency shows a large gain variation between the fifth overtone and the base tone because of the large difference of R_p. This phenomenon shows two adverse effects: First, it is extremely hard to allocate their output value for ADC. An unbalanced allocation leads to a severe loss of resolution. In addition, the large noise contribution of the base tone will propagate to the third and fifth overtone, which deteriorates the dynamic range of the system.
- **Noise figure**: Noise figure of the crystal filter is defined as the ratio of total output referred noise to the output referred noise contributed by crystal. It is easy to see the parallel resonance frequency has a better noise figure than series resonance frequency since R_p is much larger than R_s.
- **Aliased noise**: The capacitive feedback attenuates the effect of the shunt capacitance C_o of crystal in high frequency and avoids noise aliasing.
- **SNR**: Although the noise figure at parallel resonance frequency is much less than that at series resonance frequency, the crystal at parallel resonance frequency is very 'noisy'. Under the same input level, SNR of the base tone at the parallel resonance frequency is 60dB less than that of the series resonance frequency.
- **Power consumption**: Parallel resonance frequency shows its advantage in power consumption. The detailed analysis in Appendix shows the comparison of power budgets between two resonance frequencies.
- **Frequency stability**: The design of capacitive feedback may increase the order of the system and introduce more poles. It is more difficult to compensate for capacitive feedback than resistive feedback.

Table 3.1 indicates the show-stopper for the parallel resonance frequency in TA+TI configuration are SNR and dynamic range. For the series resonance frequency, although capacitive feedback shows its advantage in reduction of noise aliasing, it has a worse dynamic range than resistive feedback and introduces difficulties in frequency compensation. Therefore, driving crystal at the series resonance frequency with resistive feedback is the design decision for TA+TI (series resonance mode) structure.

Transadmittance + Voltage follower

Figure 3.7(a) shows the Transadmittance (TA) + Voltage follower (VF) configuration for the crystal filter. Its transfer function $V_{out}/V_{in} = Z_{XTal}/Z_f$ shows that it is a parallel resonance mode. At parallel resonance frequency, the TA+VF configuration significantly improves the signal-to-noise ratio compared to the TA+TI configuration. However, there is a design contradiction between noise figure and biasing current. With maximum power consumed by crystal $P_{crystal} = 20\mu W$, the maximum RMS signal current approximates $13\mu A$, which implies a low-power design to drive the crystal at parallel resonance frequency. However, as long as there is a need to increase the biasing current, the noise sources contributed by the biasing of the controller in the TA stage would significantly deteriorate the noise figure. Figure 3.7(b) indicates the noise of biasing current source. These currents directly flow through the crystal and add extra noise.

Another option is to drive the crystal at series resonance frequency. However, with a large signal swing at the output of the VF stage, the design of the VF stage has to totally switch from 40nm technology to 270nm technology to avoid damage of transistors. This implies a limitation of performance, especially for the high bandwidth and low phase shift design.

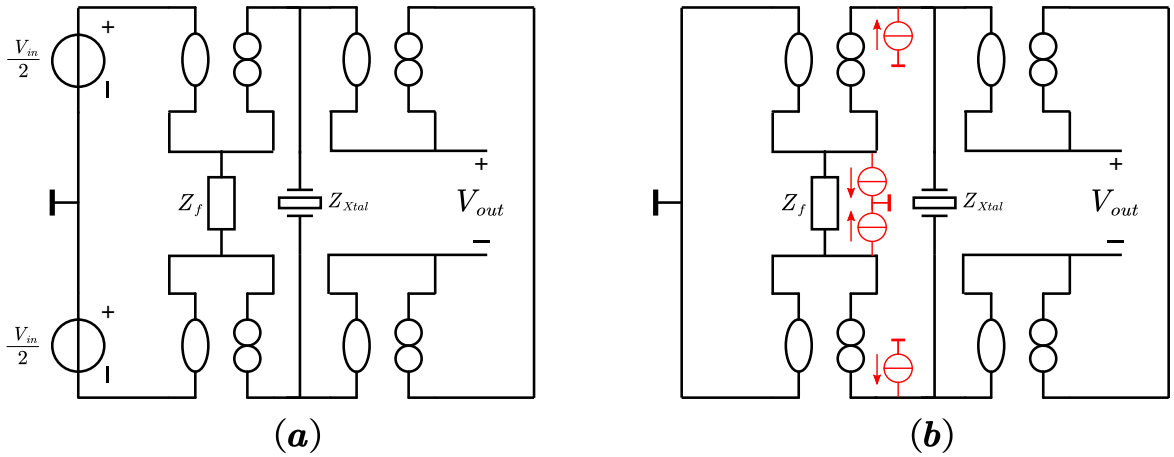


Figure 3.7: (a) Transadmittance + Voltage follower configuration of the crystal filter. (b) Consider the noise contribution of TA biasing

Conclusion

In this section, we have discussed the feasibility to drive the crystal at series/parallel resonance frequency in series resonance mode (single voltage amplifier and TA+TI configuration) and parallel resonance mode (TA+VF configuration). The following lines summarize the highlights of the discussion:

- From the perspective of parasitics, working at series resonance frequency is better than working in parallel resonance frequency, since series resonance frequency is less dependent on the temperature coefficient of parasitics, such as bonding.
- The voltage amplifier is the most intuitive configuration to realize the function of the crystal filter. However, the '+1' term should be subtracted by the TA+TI configuration with one more feedback stage.
- In the TA+TI configuration, the show-stoppers to drive the crystal at the parallel resonance frequency is mainly because of the large equivalent resistance R_p and a large variation of R_p among the three tones. The large equivalent resistance R_p causes a disparity between the SNR and the noise figure. The large variation of R_p leads to very unbalanced design budgets of dynamic range, among the three tones. Since a balanced performance between the three tones is the design interest, it is better to drive the crystal at the series resonance frequency.
- In the TA+VF configuration, the parallel resonance frequency exhibits a biasing defect. The biasing sources of the TA stage may significantly deteriorate noise figure. In addition, working at series resonance mode will cause the VF stage totally applies 270nm technology instead of 40nm technology.

In conclusion, driving the crystal at the series resonance frequency by the series resonance mode (TA+TI configuration) is most promising design decision. This configuration allows a relatively balanced performance among three tones, a better dynamic range, and less complexity.

3.3 Amplifier modeling and specifications

Table 3.2 shows the expected performance as introduced in section 2.1 and 3.1. Based on table 3.2, this section will discuss the initial model of the TA+TI amplifier and derive important parameters that the system must achieve.

Parameter	**Value/ Expectation**
Maximum $P_{crystal}$	20 μW [27]
Input V_{RMS}	differential [0,1]V
Output V_{RMS}	differential [0.48,0.64]V
Gain	-
Bandwidth	large
Frequency variations (ppb) over -40 to 100 °C	10
Noise	Low

Table 3.2: The expected performance of the TA+TI amplifier

3.3.1 Gain configuration

Table 3.3 shows the configuration of gain and its related parameters for the three tones. We design $R_f = 400\Omega$ to satisfy the maximum power limitation of crystal and maximum

input/output requirements (the total output is approximately the full-range input of ADC). In addition to the gain configuration, the allocation of $P_{crystal}$ is about the consideration of phase noise. The feedback resistance R_f also contributes to output referred noise. we will discuss the noise design in the next topic and see this gain configuration perfectly matches the required noise specifications.

	$R_f[\Omega]$	$R_n[\Omega]$	RMS $V_{in}[mV]$	RMS $V_{out}[mV]$	V_{out}/V_{in}	$P_{crystal}[\mu W]$
The base tone	400	6.14	2.0	260.6	$\frac{2R_f}{R_n}$	0.69
The third overtone		52.33	16.4	250.0		5.14
The fifth overtone		308.1	46.4	119.6		7
Total			<1000	<636		<20

Table 3.3: Gain configuration of the crystal filter

3.3.2 Noise configuration

Output-referred noise

As illustrated in figure 3.3, the digital band-pass filter in the system chooses signals around the resonance frequencies. The noise performance around those resonance frequencies is thus the design interest. Combing with the definition of detuning v, we can express both the admittance Y_n of the LRC branch, the admittance $Y_{crystal}$ of the crystal, and the PSD noise of the crystal as a low pass function of detuning v:

$$Y_n = \frac{\frac{1}{R_n}}{1 + jQ_s v} \; ; Y_{crystal} = Y_n + j2\pi v f_r \; ; S_{vR_n} = 4kTR_n \frac{|Y_n|^2}{|Y_{crystal}|^2} \tag{3.3.1}$$

In low detuning v (around the series resonance frequency), $Y_n = Y_{crystal}$ and $S_{vR_n} = 4kTR_n$. Figure 3.8 shows the equivalent noise filtering of the differential TA+TI crystal filter, including the noise sources of the controllers, source/load/feedback resistance, and ADC.

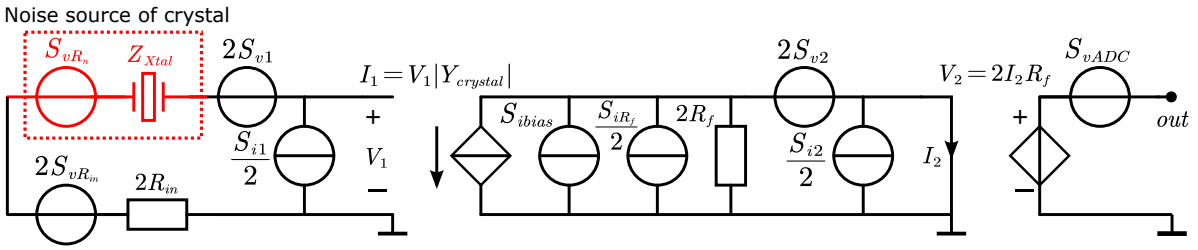


Figure 3.8: The differential TA+TI crystal filter with noise sources. S_v and S_i stand for PSD noise sources. The coefficients in front of noise sources represent differential effects. Source/load/feedback/biasing generate thermal noises so-called S_{vs}, S_{vload}, S_{iRf} and S_{ibias} respectively. It is important to notice that S_{ibias} stands for the total noise generated by the biasing current of the TA stage. The quantization noise of ADC is expressed as a noise source S_{vADC}. S_{vR_n} is the noise generated by crystal.

We can divide the output referred noise spectrum into the noise contributed by crystal $S_{vcrystal}$, the resonance noise $S_{vresonance}$ and the noise floor S_{vfloor}:

$$S_{vout} = S_{vresonance} + S_{vfloor} + S_{vcrystal} \tag{3.3.2}$$

where

$$S_{vcrystal} = S_{vR_n} \left(2|Y_n|R_f\right)^2 \tag{3.3.3}$$

$$S_{vresonance} = \left(2S_{i1}R_{in}^2 + 2S_{vR_{in}} + 2S_{v1}\right) \left(2|Y_n|R_f\right)^2 \tag{3.3.4}$$

$$S_{vfloor} = \left(\frac{S_{i1} + S_{iR_f} + S_{i2}}{2} + S_{ibias} + \frac{2S_{v2}}{\left(2R_f\right)^2}\right) \left(2R_f\right)^2 + S_{vADC} \tag{3.3.5}$$

$S_{vcrystal}$ stands for the output referred noise contributed by crystal. This noise is inevitable and thus stands for the best case of output referred noise. The resonance noise $S_{vresonance}$ describes the extra noise caused by electronics around resonance frequency. Equation 3.3.2 shows this noise is highly dependent on Y_n. This noise will soon dissipate when the circuit is off-resonance frequency. The noise floor S_{vfloor}, however, is independent on Y_n . It describes the output referred white noise band. Figure 3.9 indicates the output referred noise spectrum versus detuning v of the crystal filter.

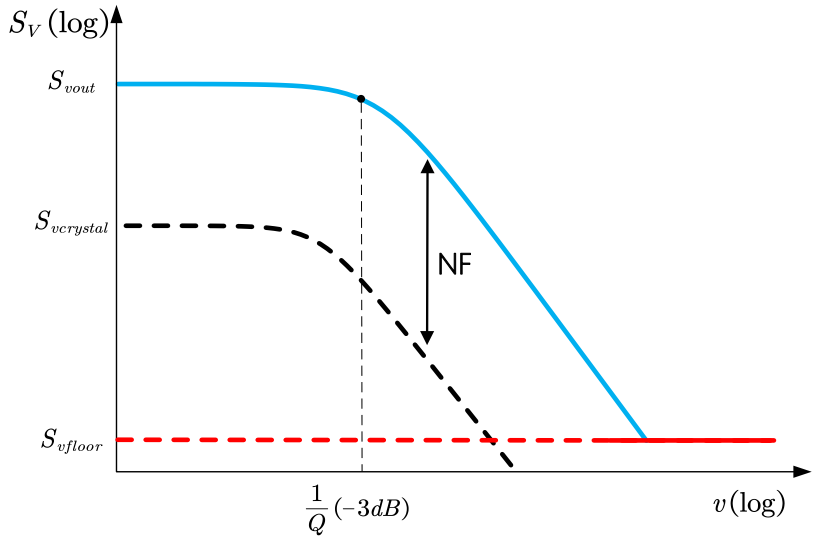


Figure 3.9: Output referred noise PSD of the crystal filter versus detuning v

Considerations of noise budgets

The noise requirements of the crystal filter could be derived from the phase noise specs of the MMXO as shown in table 1.2. To study the relations between the three resonance frequency and their corresponding phase noise, we first define the noise figure NF of the

system. According to Fig 3.9, the noise figure NF of the crystal filter is defined as the ratio of total output referred noise to the output referred noise contributed by crystal.

$$NF = 10\log\left(\frac{S_{vout}}{S_{vcrystal}}\right)[\text{dB}] \tag{3.3.6}$$

Generally, $S_{vresonance}$, which is much higher than S_{vfloor} and $S_{vcrystal}$, dominates noise performance of the crystal filter around resonance frequency. Equation 3.3.6 could be expressed as equation 3.3.7 around resonance frequency when S_{vfloor} is non-dominant:

$$NF = 10\log\left(1+\frac{S_{vresonance}}{S_{vcrystal}}\right) = 10\log\left(1+\frac{2S_{i1}R_{in}^2+2S_{vR_{in}}+2S_{v1}}{S_{vR_n}}\right)[\text{dB}] \tag{3.3.7}$$

The carrier-to-noise (CNR) ratio, which is a measure of the received carrier strength relative to the strength of the received noise, could be expressed as equation 3.3.8 around resonance frequency. For the design of an oscillator system, CNR stands for signal-to-noise ratio (SNR) of a modulated carrier signal.

$$CNR = 10\log\left(\frac{P_{crystal}/R_n}{S_{vR_n}|Y_n|^2 10^{NF/10}}\right) = 10\log\left(\frac{(1+Q^2v^2)\,P_{crystal}}{4kT}\right) - NF\,[\text{Hz}\cdot\text{dB}] \tag{3.3.8}$$

If we assume α percent (α=0.4 to 0.6) total noise around resonance frequency transforms to phase noise. We can express phase noise contributed by the crystal filter by simply changing the format of equation 3.3.8.

$$V_{nphase} = 10\log\left(\frac{4\alpha kT}{(1+Q^2v^2)\,P_{crystal}}\right) + NF\,[\text{dBc/Hz}] \tag{3.3.9}$$

CNR (or phase noise) and NF are two important measurements for the quality of resonance signal. We expect a high CNR and a low NF to get a high quality resonance signal. We can derive the most lenient requirement of noise figure NF at 1kHz frequency offset for each tone based on table 2.1(quality factor), 1.2 (phase noise of the MMXO) and equation 3.3.10. This equation is considered as the most lenient case because there are other electronics in the MMXO system which also contribute to noise. The phase noise requirement for the crystal filter should be lower than -147dBc/Hz. In addition, the decrease of quality factor Q and power consumed by crystal $P_{crystal}$ also make the noise figure lower.

$$NF_{max} = V_{nphase} - 10\log\left(\frac{4\alpha kT}{(1+Q^2v^2)\,P_{crystal}}\right) = -147 + 10\log\left(\frac{(1+Q^2v^2)\,P_{crystal}}{4\alpha kT}\right) \tag{3.3.10}$$

According to equation 3.3.7, the best case (or the lowest case) of noise figure is set by input impedance $R_{in} = 50\Omega$ as shown in equation 3.3.11. The noise figure NF at 1kHz offset must be larger than NF_{min} and should not exceed NF_{max}. The variation is mainly dependent on the input-referred noise of the TA controller.

$$NF_{\min} = 10\log\left(\frac{2S_{vR_{in}}}{S_{vR_n}}\right) = 10\log\left(\frac{2R_{in}}{R_n}\frac{|Y_{crystal}|^2}{|Y_n|^2}\right) \tag{3.3.11}$$

During the analysis of NF, we first assumed the noise floor S_{vfloor} is much less than the resonance noise $S_{vresonance}$ around resonance frequency to simplify equation 3.3.2. We need

to verify this assumption for the three tones. Simplifying equation 3.3.5 by neglecting S_{i1} and S_{i2}, we can get:

$$S_{vfloor} = 4S_{ibias}R_f^2 + S_{vADC} + 2S_{v2} + 8kTR_f \tag{3.3.12}$$

The signal-to-quantization noise (SQNR) of ADC is given by:

$$SQNR = 1.762 + 6.02ENOB \ \ [\text{dB}] \tag{3.3.13}$$

The noise bandwidth of the ADC is fs/2. With 1.8V peak to peak full range input, 11bits ENOB and 1.25GHz sampling frequency, the quantization noise S_{vADC} could be calculate as $2.08 \times 10^{-16}\,[\text{V}^2/\text{Hz}]$. The noise contribution of feedback resistance $8kTR_f$ is $1.32 \times 10^{-17}\,[\text{V}^2/\text{Hz}]$. In this case, **the quantization noise of ADC dominates the noise floor** if we well control the noise of biasing current S_{ibias} in TA stage and the input-referred noise S_{v2} of TI stage. For example, g_m of the biasing current and the input stage of TI is higher than 2.5m so that we get $4S_{ibias}R_f^2 + 2S_{v2} > 18kTR_f = 3 \times 10^{-17}\,[\text{V}^2/\text{Hz}]$. This value is still much less than S_{vADC}.

To get some impressions of the difference between the noise floor S_{vfloor} and the resonance noise $S_{vresonance}$. We first assume that only the input impedance R_{in} contributes to $S_{vresonance}$ (the case of lowest $S_{vresonance}$) at resonance frequency, the output referred $S_{vresonance}$ is $2.81\times10^{-14}\,[\text{V}^2/\text{Hz}]$ for the base tone, $3.91\times10^{-16}\,[\text{V}^2/\text{Hz}]$ for the third overtone, and $1.1 \times 10^{-17}\,[\text{V}^2/\text{Hz}]$ for the fifth overtone. In this case, the noise floor S_{vfloor} is 12.8dB higher than $S_{vresonance}$ of the fifth overtone, 2.7dB lower than $S_{vresonance}$ of the third overtone, and 21.3dB lower than that of the base tone. If we consider the other noise sources besides the input impedance R_{in}, we can draw the conclusion that **the noise floor S_{vfloor} is non-dominant for the base tone and the third overtone** as long as the noise of biasing current S_{ibias} in TA stage and the input-referred noise S_{v2} of TI stage is controlled to an acceptable level. However, **the noise floor may dominate noise performance of the fifth overtone**. For the fifth overtone, the assumption of Eq 3.3.7 is invalid. In this case, the calculation of phase noise and noise figure for the fifth overtone is given by:

$$V_{nphase\_5th} \approx 10\log\left(\frac{\alpha S_{vADC}}{P_{crystal}/R_n \cdot |2R_f|^2}\right)\,[\text{dBc/Hz}] \tag{3.3.14}$$

$$NF_{5th} = 10\log\left(\frac{S_{vADC}}{S_{vcrystal}}\right) = 10\log\left(\frac{S_{vADC}\,(1+Q^2v^2)}{4kT\,(2R_f/R_n)^2}\right)\,[\text{dB}] \tag{3.3.15}$$

Figure 3.10 shows the noise figure versus detuning v for the three tones by sweeping the input-referred noise S_{v1} of the TA controller. We assume that only quantization noise contributes to output referred noise floor S_{vfloor}. At the low detuning (around the resonance frequency), the value of noise figure confirms our expectation. For the fifth overtone, the noise figure is now dominated by the noise floor S_{vfloor} and independent of S_{v1} so that it barely changes with S_{v1}. Table 3.4 summarizes the related noise budgets of the three tones or the corresponding explanations for the settings. In order to get a relative balanced noise performance and satisfy the phase noise requirements of the MMXO, the input-referred voltage noise spectral of the TA stage S_{v1} should be lower than $5.3 \times 10^{-18}\,[\text{V}^2/\text{Hz}]$.

Figure 3.11 shows the voltage PSD of output-referred noise with $S_{v1} = 5.3\times10^{-18}\,[\text{V}^2/\text{Hz}]$. We can clearly see the differences between S_{vfloor}, $S_{vcrystal}$ and S_{vout} for the three tones.

Stage	Specifications	The basetone	The 3rd overtone	The 5th overtone	Explanations
Total	Minimum noise floor S_{vfloor} [V^2/Hz]	2.2×10^{-16}			(a)
	Minimum S_{vout} [V^2/Hz]	2.82×10^{-14}	5.98×10^{-16}	2.2×10^{-16}	(b)
	Maximum S_{vout} [V^2/Hz]	3.4×10^{-13}	7.52×10^{-15}	N/A	(b)
	Noise figure @1kHz [dB]	(12.2, 23)	(4.69, 15.6)	>8.0	(c)
	Phase noise @1kHz [dBc/Hz]	(-157.8,-147)	(-157.9,-147)	>-139.5	(d)
TA	Maximum S_{iout} [A^2/Hz]	5.32×10^{-19}	1.18×10^{-20}	4.60×10^{-22}	(x)
	Minimum S_{iout} [A^2/Hz]	4.41×10^{-20}	1.26×10^{-21}	3.25×10^{-22}	(x)
	Output floor noise [A^2/Hz]	(0, 3.25×10^{-22})			(f)
	S_{v1} [V^2/Hz]	(0, 5.3×10^{-18})			(e)
	S_{i1} [A^2/Hz]	(0, 2.65×10^{-22})			(f)
TI	Output-referred noise [V^2/Hz]	(0, 2.08×10^{-16})			(x)
	S_{v2} [V^2/Hz]	(0, 1.04×10^{-16})			(g)
	S_{i2} [A^2/Hz]	(0, 6.5×10^{-22})			(h)

Table 3.4: Noise configuration of the crystal filter. Here are the explanations for the settings of parameters: (a) S_{vADC} dominates the noise floor. (b) The minimum S_{vout} is set by the minimum noise floor and noise figure. The maximum S_{vout} is set by the requirement of phase noise (Eq 3.3.10). For the fifth overtone, there is no requirements for the maximum S_{vout} since its lowest phase noise is -139.5dBc/Hz , which is already higher than required value. (c) The minimum noise figure is decided by input resistance R_{in}, the maximum noise figure is calculated from (b). (d) The minimum phase noise of the base tone and the third overtone is given by Eq 3.3.10 and 3.3.9. The minimum phase noise of the fifth overtone is given by Eq 3.3.14 and 3.3.15 (e) According to the simulation result of figure 3.10. (f) S_{ibias} and S_{i1} contribute to noise floor together. Both $2S_{i1}R_{in}^2 < S_{vADC}$ and $4(S_{ibias} + S_{i1}/2)R_f^2 < S_{vADC}$ need to be satisfied. (g) $2S_{v2} < S_{vADC}$. (h) $2S_{i1}R_f^2 < S_{vADC}$. (x) Output-referred noise of the TA and TI stage, which could be derived from the above explanations. The output-referred noise of the TI stage should be smaller than S_{vADC}.

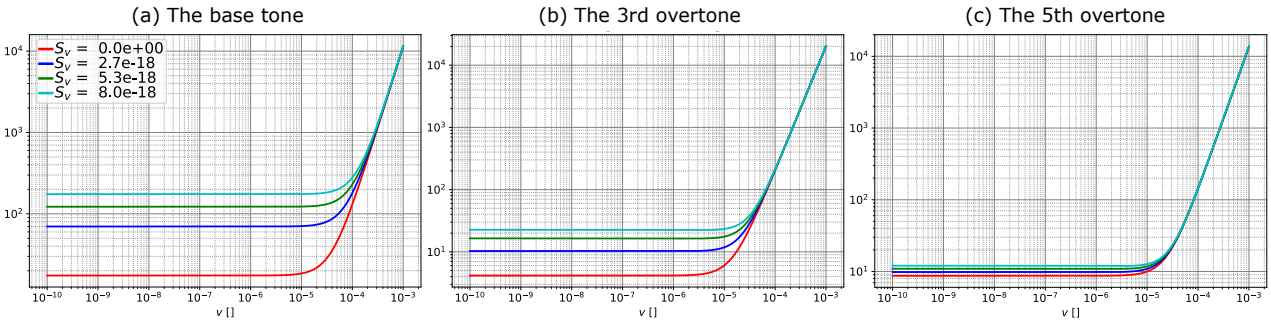


Figure 3.10: The output referred noise figure versus detuning v for the base tone(a), the third overtone(b), and the fifth overtone(c). The noise figure increases in high detuning because the noise contribution of crystal dissipates. The calculation of the noise figure is according to equation 3.3.2 considering the influence of S_{vfloor}. The building of test-bench is according to figure 3.8: [The differential TA+TI crystal filter with noise sources] and figure 3.6: [Transadmittance + Transimpedance configuration of the crystal filter].

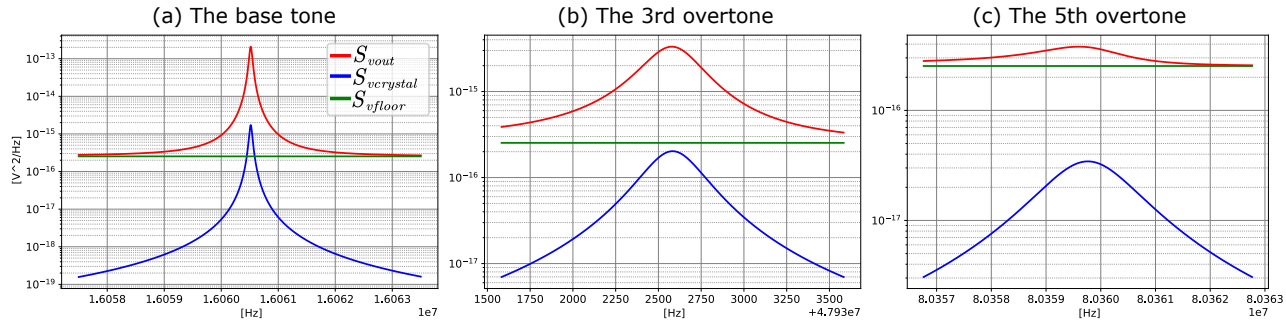


Figure 3.11: Output referred voltage noise PSD of the three tones. The relations between S_{vfloor}, S_{vout} and $S_{vcrystal}$ confirms the calculations from equation 3.3.2 to 3.3.5 and the output referred noise figure as shown in figure 3.10.

The limitation of the noise figure for the 5th overtone implies a higher phase noise than -147[dBc/Hz] (table 1.2). Because the tested phase noise in table 1.2 is measured with the final output signal, it is hard to predict how this requirement propagates to the fifth overtone so far. we need further study of the MMXO system and its related algorithms to derive fair budgets for the three overtones. In this stage, the noise performance of the fifth overtone is not the show-stopper for the crystal filter since it is not the reference tone.

3.3.3 Frequency response

The working principle of the crystal filter (section 3.1) indicates the importance of bandwidth and quality factor to frequency stability. To explore their relations, we first build up a equivalent test-bench for bandwidth measurement at series resonance frequency as shown in figure 3.12.

In figure 3.12, we define the detector quantity as the voltage (V_{o+}, V_{o-}) on the crystal. The total phase shift of the transfer from (V_{in+}, V_{in-}) to (V_{out+}, V_{out-}) can be divided into three parts:

- ϕ_{TA}**:** (V_{in+}, V_{in-}) **to** (V_{o+}, V_{o-})**.** The phase shift caused by the imperfections of the TI controller and bonding wire inductance. There is no phase shift ($V_{in+} - V_{in-} = V_{o1} - V_{o2}$) if $L_n = 0$ and the TA controller behaves like a nullor.

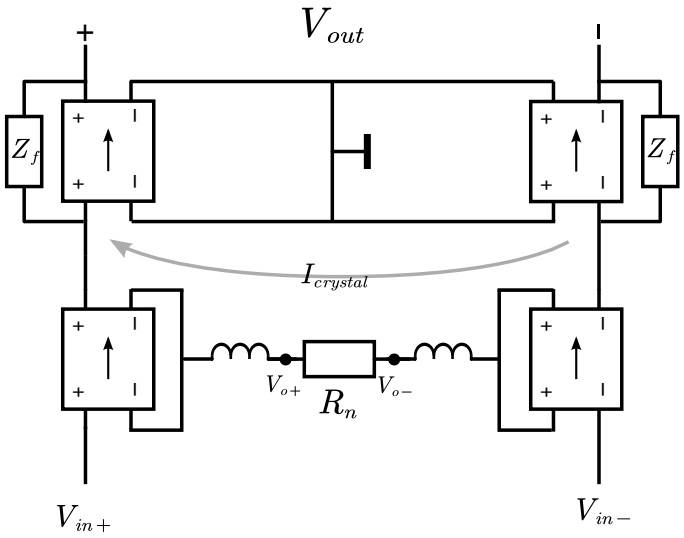


Figure 3.12: Equivalent bandwidth test-bench of the TA+TI crystal filter at series resonance frequency

- $\phi_{crystal}$**:** (V_{o+}, V_{o-}) **to** $I_{crystal}$. The phase shift caused by the crystal itself. This temperature dependent phase shift reflects the properties of crystal, which is a important information for compensation mechanism of the MMXO system. In this case, we do not consider that this phase shift contributes to frequency error.
- ϕ_{TI}**:** $I_{crystal}$ **to** (V_{out+}, V_{out-})**.** The phase shift caused by the imperfections of the TA controller. There is no phase shift ($I_{crystal} \times 2R_f = V_{out+} - V_{out-}$) if the TI controller behaves like a nullor.

The total temperature dependent phase shift could be expressed as:

$$\phi_{total}(T) = \phi_{TA}(T) + \phi_{TI}(T) \tag{3.3.16}$$

According to equation 2.1.13, the frequency error caused by the crystal filter could be written as equation 3.3.17 if temperature changes from T_0 to T_1:

$$f_{error} = \frac{\Delta f}{f_r} = \frac{\phi_{TA}(T)|_{T_0}^{T_1} + \phi_{TI}(T)|_{T_0}^{T_1}}{2Q} \tag{3.3.17}$$

We have concluded two causes of frequency error are temperature dependent phase shift and decrease of quality factor. Based on equation 3.3.17 and the structure of the TA+TI amplifier, we can further develop this conclusion and give suggestions to decrease frequency error.

- Low $\phi_{TI}(T)$ and $\phi_{TA}(T)$ at the resonance frequency requires a much higher equivalent bandwidth of the TI and TA stage than the resonance frequency of the three tones. In this case, bandwidth of TA and TI amplifier should be much higher than 80 MHz.
- Low $\phi_{TA}(T)|_{T_0}^{T_1}$ and $\phi_{TI}(T)|_{T_0}^{T_1}$ at the resonance frequency also require a low sensitivity to temperature variation. Although there is a large phase shift at the resonance frequency, the phase shift does not vary with temperature if sensitivity is zero.

- Maintaining the high quality factor of crystal requires that the TA amplifier should have a low port impedance seen from two sides of the crystal at the resonance frequencies.

The temperature sensitivity of ϕ_{TI} and ϕ_{TA} highly depends on the temperature model of circuit components in TSMC 40nm technology library. It is extremely hard to predict their influence on the temperature dependent phase shift before the design of a complete circuit. Therefore, we focus on the first and the third suggestion which provides more information in the early design. In figure 3.12, the interaction between bonding wire inductance L_w and the equivalent crystal model at resonance (parallel connection of C_0 and L_n) establishes the bandwidth limitation for the TA amplifier. Assuming the TA controller is a nullor, we can express the transfer function from (V_{in+}, V_{in-}) to (V_{o+}, V_{o-}) as:

$$A_v = \frac{1}{2C_o L_w s^2 + \frac{2L_w}{R_n} + 1} \tag{3.3.18}$$

Figure 3.13 shows the bode plots of the magnitude and phase characteristics of equation 3.3.18. The bondwire inductance L_w is approximately 1.5nH. The bandwidth of the third and fifth overtone is limited around $f_c = \frac{1}{2\pi\sqrt{2L_m C_0}}$ =2.26 GHz. The bandwidth of the base tone is less (325MHz) since the small equivalent resistance significantly undamps the parallel resonance (L_w and C_0). Figure 3.13(b) shows their phase shift at low frequency. The

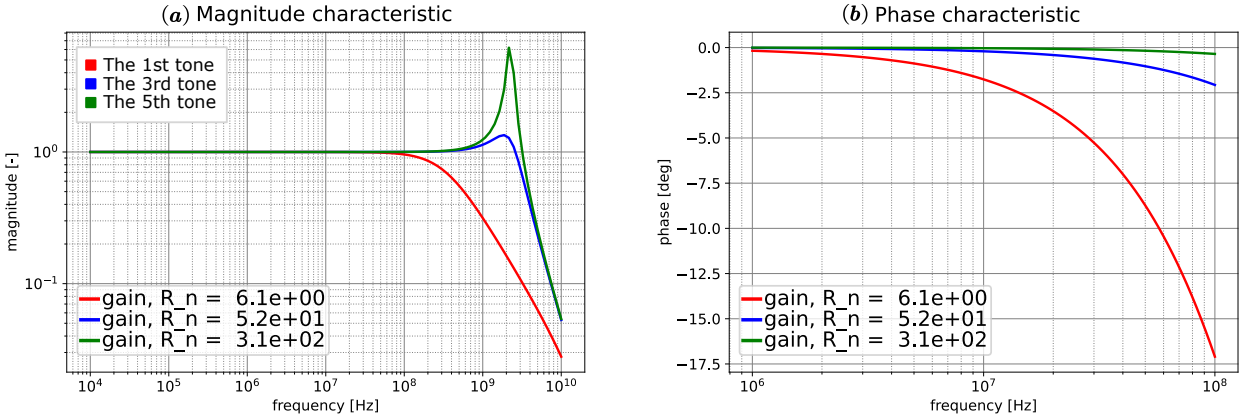


Figure 3.13: Equivalent Magnitude(a) and phase(b) characteristics of the TA amplifier at the three resonance frequency. The transfer function is defined as equation 3.3.18

lowest phase shift at 16MHz, 48MHz, 80MHz is -3.3deg, -1.1deg, and -0.31deg, respectively. They stand for the best case of phase shift ϕ_{TA} at the three resonance frequency. The imperfections of the TA controller add extra phase shift on ϕ_{TA}. To keep the extra phase shift as low as possible, we expect the equivalent bandwidth of the TA amplifier should be close to its bandwidth limitation. Because the TI amplifier is cascaded with the TA amplifier, the bandwidth of the TI amplifier should be at least equal to that of the TA amplifier to avoid the decrease of final bandwidth. The bandwidth of the TI amplifier is independent of resonance characteristics. We expect its bandwidth should be larger than 2.26GHz so that $\phi_{TI} \approx \phi_{TA}$ for the third and fifth overtone and $\phi_{TI} \ll \phi_{TA}$ for the base tone.

In order to break the bandwidth limitation and get a lower phase shift at the three resonance frequency, we can apply some techniques [19] in layout to reduce the effective inductance of bonding wire. We will discuss this topic in chapter 6 as a part of layout proposal.

As an initial setting, the bandwidth of the TA amplifier should be close to 2.26GHz at the third and fifth overtone and close to 325MHz at the base tone.

Maintaining the high quality factor of crystal requires that the TA controller has a low impedance seen from two sides of the crystal. We can further derive budgets for equivalent transconductance G_m by applying MOS controller model as shown in figure 3.14. The input impedance of the TI amplifier R_{TI} is first assumed to be zero. The single sided port impedance R_{port} could be calculated as:

$$R_{port} = \frac{V_o}{I_{in}} = \frac{R_{out}}{G_m R_{out} + 1} \frac{1 + sC_g R_{in}}{1 + s\frac{R_{in}+R_{out}}{G_m R_{out}+1} C_g} \tag{3.3.19}$$

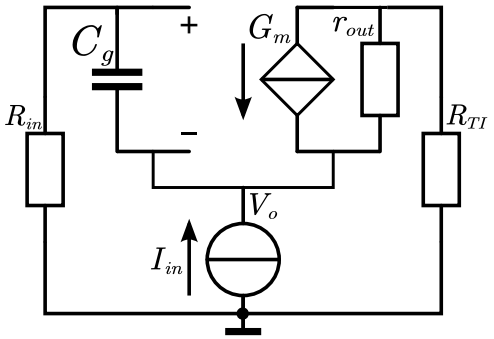


Figure 3.14: Equivalent test-bench for port impedance from two sides of the crystal

At low frequency, $R_{port} \approx 1/G_m$. Since R_{in} should be much lower than $R_n/2$ to guarantee most of power consumed by R_n at resonance frequency, we can get:

$$G_m \gg \begin{cases} 1/3 \,@\, R_n = 6.1 \\ 1/26 \,@\,, R_n = 52.3 \\ 1/154 \,@\, R_n = 308.1 \end{cases} \tag{3.3.20}$$

For example, if $G_m = 3$, the base tone loses half of its quality factor, the third overtone loses 10% of its quality factor, and the fifth overtone loses 2% of its quality factor. To decrease the loss of quality factor, we need to increase the effective transconductance G_m. In other words, it requires a large loop gain of the TA amplifier. The corresponding requirement for DC loop gain can be simply expressed as:

$$L_{DC} \gg 1@ \text{ Three resonance frequency} \tag{3.3.21}$$

Table 3.5 summarizes the specifications regarding the frequency characteristics of the crystal filter.

Stage	Specifications	The basetone	The 3rd overtone	The 5th overtone	Argumentation
TA	Effective Bandwidth @ resonance [GHz]	$\geqslant$0.32	$\geqslant$2.26	$\geqslant$2.26	To reach bandwidth limtation
	Effective G_m [S]	$\gg$0.330	$\gg$0.038	$\gg$0.007	To avoid Q loss
	DC loop gain L_{DC}	$\gg$1			
TI	Effective Bandwidth @ resonance [GHz]	$\geqslant$2.26	$\geqslant$2.26	$\geqslant$2.26	To reach bandwidth limtation

Table 3.5: Frequency characteristics configuration of the crystal filter

CHAPTER 4

Design of the transadmittance stage

In this chapter, we will discuss the design of the transadmittance stage. Table 4.1 summarizes the specifications for the TA stage from section 3.3. In this chapter, we will discuss the orthogonal design of the TA stage, which is divided into 5 parts, which are noise, drive capability, bandwidth, frequency compensation, and biasing.

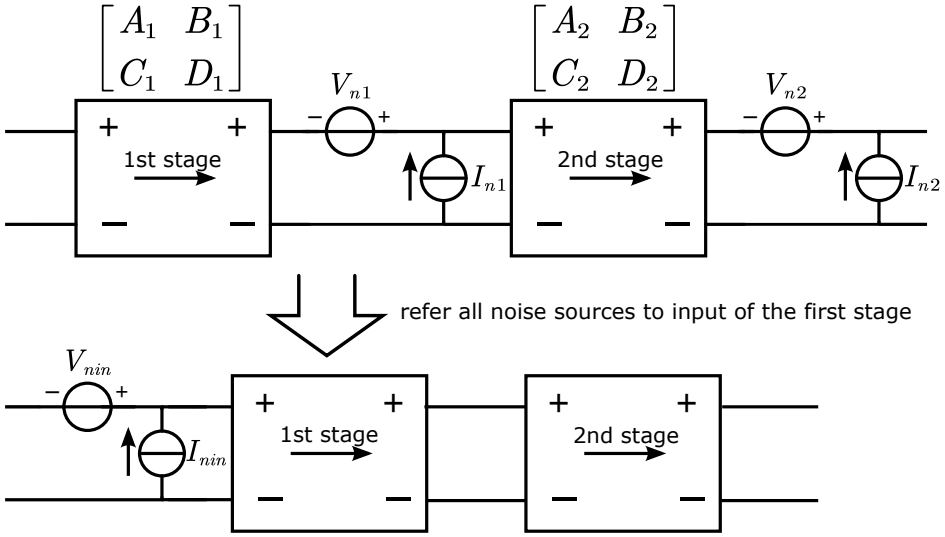
Stage	**Specifications**	**The basetone**	**The 3rd overtone**	**The 5th overtone**
TA	Drive capability [mA]	$\geqslant$0.8 RMS(a)		
	Effective G_m @ resonance[S]	$\gg$0.330	$\gg$0.038	$\gg$0.007
	DC loop gain L_{DC}	$\gg$1		
	Effective Bandwidth @ resonance [GHz]	$\geqslant$0.32	$\geqslant$2.26	$\geqslant$2.26
	Maximum S_{iout} [A^2/Hz]	5.32×10^{-19}	1.18×10^{-20}	4.60×10^{-22}
	Minimum S_{iout} [A^2/Hz]	4.41×10^{-20}	1.26×10^{-21}	3.25×10^{-22}
	S_{v1} [V^2/Hz]	(0, 5.3×10^{-18})		
	Output floor noise [A^2/HZ]	(0, 3.25×10^{-22})		
	S_{i1} [A^2/Hz]	(0, 2.65×10^{-22})		

Table 4.1: Specifications of the transadmittance stage. (a) The drive capability should be at least larger than the signal current. The maximum signal current is set by the total RMS value of the three tones.

4.1 Noise optimization

In a multiple-stage amplifier design, the noise of the amplifier is mainly decided by its input stage. This assumption is based on each stage of the controller is a nullor-like(unilateral) stage[18], which proves to be very common in analog multiple-stage amplifier design. Figure 4.1 indicates the mechanism behind this assumption. If we refer all noise sources to the input of the first stage, the noise contribution of the second stage is attenuated twice. Therefore. the noise contributions of the first stage(V_{n1} and I_{n1}) are more dominant.

For the design of a MOS controller, a common-source (CS) input stage is preferred since it behaves more like a nullor than a common-gate (CG) or common-drain (CD) stage[18].



$$V_{nin} = A_1(V_{n1} + A_2V_{n2} + B_2I_{n2}) + B_1(I_{n1} + C_2V_{n2} + D_2I_{n2})$$
$$I_{nin} = C_1(V_{n1} + A_2V_{n2} + B_2I_{n2}) + D_1(I_{n1} + C_2V_{n2} + D_2I_{n2})$$

Figure 4.1: Transformation of noise sources of two-stage controller to its input. (A_1,B_1; C_1,D_1) is the transmission-1 matrix of the first stage. (A_2,B_2; C_2,D_2) is the transmission-1 matrix of the second stage. V_{n1} and I_{n1} stands for the equivalent output-referred noise source of the first stage. V_{n2} and I_{n2} stands for the equivalent output-referred noise source of the second stage.

This is because CD and CG stages are non-energetic local feedback versions of CS stage. With local feedback technique, their transmission-1 matrix fix one parameter of transmission-1 matrix equalling 1, which makes them less like a nullor. Figure 4.2 shows the SLICAP test-bench to simulate the input-referred noise of an N channel CS stage.

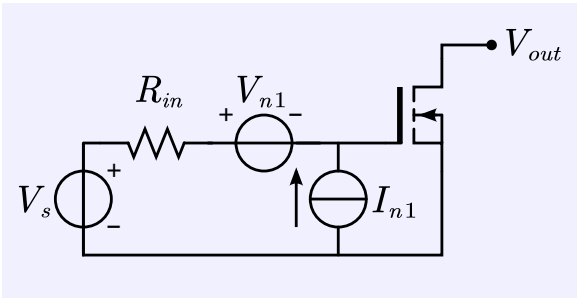


Figure 4.2: The SLICAP test-bench to simulate the input-referred noise of an N-channel CS stage. The NMOS is preferred than the PMOS since generally it has better performance. If there is no limitation caused by biasing, we will first consider NMOS for the design of signal path. The input-referred source is V_s

The voltage spectral density of the source-referred noise can be obtained after transformation of the current noise sources into voltage noise sources. If we assume I_G=0, the spectral density S_{Vs} of the total source-referred (voltage) noise is obtained as:

$$S_{Vs} = 4kTR_{in} + \left(\frac{4kTn\Gamma}{g_m} + 4kTR_{in}^2 n\Gamma g_m \frac{f^2}{f_T^2}\right)\left(1 + \frac{f_l}{f}\right) \tag{4.1.1}$$

Figure 4.3 illustrates the distribution of S_{Vs}. In low frequency, the flicker noise is dominant. In the frequency range of interest, $4kTR_s$+$4kTn\Gamma/g_m$ presents a noise floor. In the

range of frequency above f_T, the source-referred current spectral S_{i1} gradually become dominant. Since we already considered the noise contribution of source impedance when we specified S_{v1} and S_{i1}. In the subsequent analysis, We will assume R_{in} is noise-free so that $4kTR_{in} = 0$.

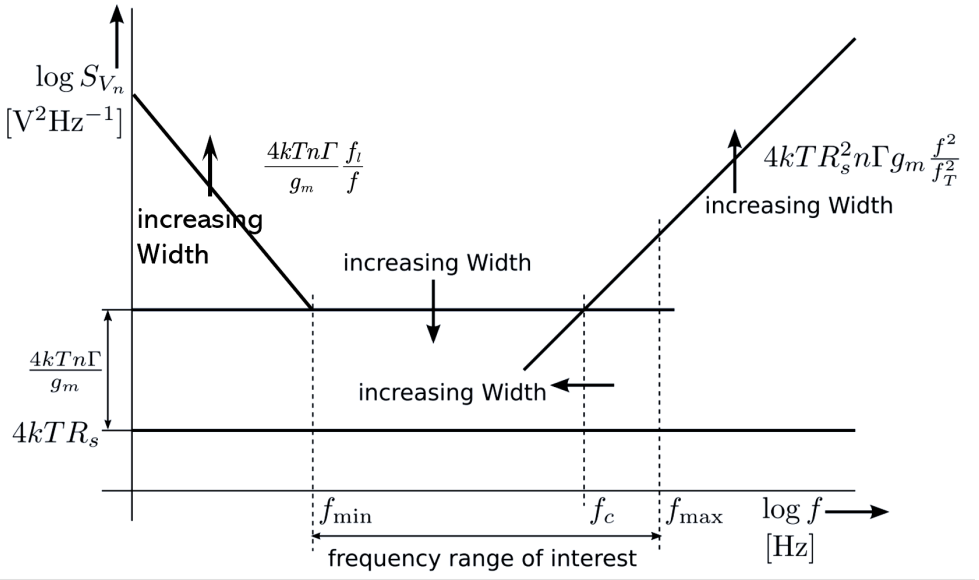


Figure 4.3: The distribution of the source-referred voltage noise PSD of a MOS transistor with input impedance $R_{in} = 50\Omega$. The contribution of the gate-induced noise to the total RMS noise over the frequency range of interest is made equal to the contribution of the equivalent input voltage noise. Source[18], edited

Based on the noise characteristics of MOS transistors, the author proposes a method for noise optimization. The principle is to ensure a large FOM (enough g_m and f_T, low power consumption and size) during the optimization. First, we assume the three resonance frequencies are in the range of (f_{min}, f_c) so that there is no flicker noise and high-frequency noise propagating to the resonance frequencies. The starting point is to set the smallest size and highest f_T for the transistor. According to figure 2.7, we set $W = 120n$, $L = 40n$, and drain current $I_D = 50\mu$. In this case, the transistor presents the smallest total input capacitance C_{iss} and the highest f_T. However, its g_m may be too low to satisfy the noise requirement. In this case, we keep I_D constant and try to scale the width of the transistor up as shown in figure 4.4(a).

With the increase of the size, while maintaining the same drain current, the operation region of the transistor gradually switches from strong inversion to weak inversion. In weak inversion, g_m is purely a function of I_d and independent of size. Therefore, we can observe that the noise spectrum in the frequency range of interest reaches its minimum value around $S_{v1} = 10^{17}\,[\mathrm{V}^2/\mathrm{Hz}]$, which is set by conditions of weak inversion. S_{v1} is still much higher than the required value ($5.3 \times 10^{18}\,[\mathrm{V}^2/\mathrm{Hz}]$). Since it is now impossible to improve noise by increasing the size, the only way is to increase the drain current and switches the operation region back to moderate inversion as shown in figure 4.4(b).

As an initial decision, we set width $W = 400\mu$ and $I_D = 0.5m$. In this case, S_{v1} is smaller than $2 \times 10^{18}\,[\mathrm{V}^2/\mathrm{Hz}]$ for frequency larger than 10MHz. However, the transistor implies a low f_T in moderate inversion. In the subsequent analysis, in order to increase f_T, we can further increase the drain current or decrease the width of the transistor slightly since we have left some design margins for noise.

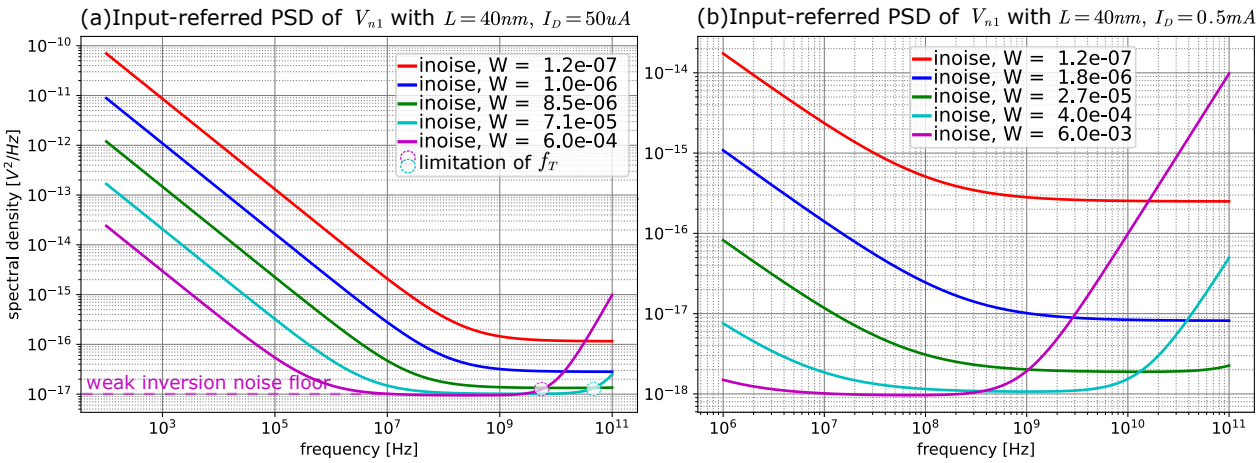


Figure 4.4: input-referred voltage noise spectrum of the single transadmittance stage. (a) Start tuning transistor with minimum size ($W = 120n$, $L = 40n$) and maximum f_T until its noise performance cannot be improved by increasing size. (b) Try to increase I_D and repeat the process of (a) until finding a feasible noise solution in the interested frequency range.

4.2 Drive capabilities

Different from the noise, drive capability is mainly dependent on the output stage in a multiple-stage amplifier if each stage of the controller is a nullor-like stage. The analysis of drive capability is under specific operating conditions, which is established by adding bias sources. Figure 4.5 illustrates a biasing network for an NMOS. This network creates a zero voltage $V_l = 0$ and the zero current $I_l = 0$ condition for the external circuitry. The transistor works under the operating point (V_{DSQ},I_{DSQ}).

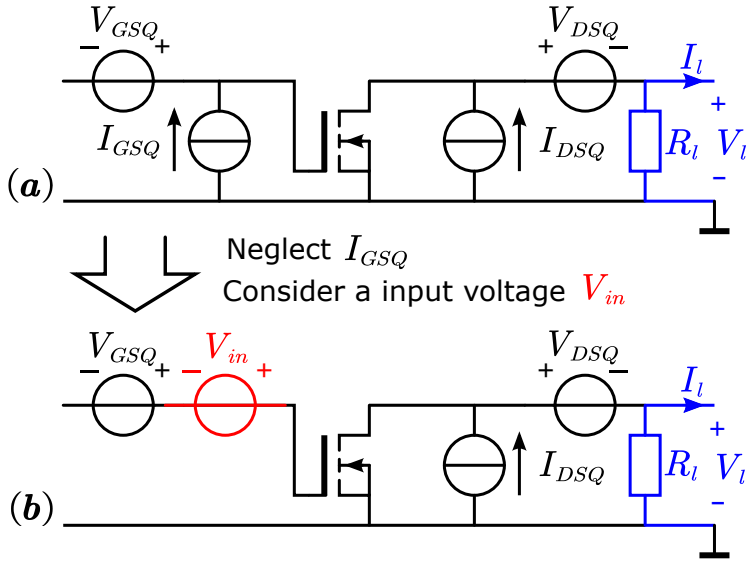


Figure 4.5: A biased N-channel MOS transistor with load impedance R_L. (a) Complete biasing with 4 bias sources. (b) Neglect the influence of the input current bias since it has little effect in the MOS controller, and assume that there is a signal input V_{in}.

To see the output swing of the transistor, we neglect I_{DSQ} and apply an input voltage

swing V_{in} as shown in figure 4.5(b). Here are the situations that may occur:

- Assume we input a negative input swing V_{in} to decrease V_{gs}. At a certain moment, the transistor is completely off. The operating current will only flow through the load impedance R_l and create the output voltage $V_l = I_{DSQ}R_l$.
- Another output headroom occurs when there is a large positive input swing. The transistor needs to generate more current with the large V_{gs}. However, the transistor is a passive device that cannot generate current by itself. The maximum current that the biasing network can provide is the biasing current I_{DSQ} together with the current generated by V_{DSQ}/R_l. In this case, the output voltage is $-V_{DSQ}$ and the corresponding output current is $-V_{DSQ}/R_l$.

In fact, the first situation is easy to achieve when the transistor works in cut-off region. However, the second situation, which is mainly dependent on the amplification ability of the transistor and the maximum positive swing of V_{gs}, is not always the case. We define the maximum current that a transistor can drive under the maximum V_{gs} provided as its *drive capability*. If this current is $I_{DriveCap}$, the output current swing could be expressed as:

$$-\frac{V_{DSQ}}{R_l} \leqslant -I_{DriveCap} \leqslant I_l \leqslant I_{DSQ} \tag{4.2.1}$$

Equation 4.2.1 indicates that the biasing conditions of the output stage set the output swing limits of the controller. In order to prevent clipping during large signal excursions at the output port, we need to design a proper biasing network. To improve drive capability, we need to make $I_{DriveCap}$ close to the limit ($-V_{DSQ}/R_l$) by increasing the positive input voltage or the gain of the output stage. Since there is always a limit of the input range, increasing the gain of the output stage is more feasible. Therefore, drive capability imposes the requirements for biasing and sizing of the output stage. A single-stage solution could be feasible if those values are compatible with the requirements of the input stage.

Biasing and sizing requirements

Based on the above analysis, the drive capability of the transadmittance stage can be expressed as:

$$-I_{DriveCap} \leqslant I_l \leqslant I_{DSQ} \tag{4.2.2}$$

where I_{DSQ} sets the upper limit of the output current swing I_l. Assuming that the signal current of the three tones added together at certain moment, the maximum peak-to-peak signal current could be calculated from table 3.3 as:

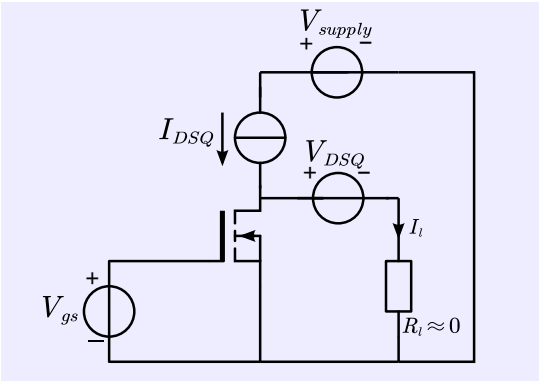
$$I_{npp} = 2\sqrt{2}\left(\frac{V_{in1st}}{R_{n1}} + \frac{V_{in3rd}}{R_{n3}} + \frac{V_{in5th}}{R_{n5}}\right) = 2.26\,[\mathrm{mA}] \tag{4.2.3}$$

According to the differential structure shown in figure 3.6, there are at least two transistors driving I_{npp} together. Thus, I_{DSQ} of one transistor should be higher than half of the peak signal current $0.56\mathrm{mA}$ to ensure that the output stage can drive the maximum positive swing of the signal current.

As indicated in Eq 4.2.1, $I_{DriveCap}$ sets the lower limit of the signal current, which is the maximum negative swing of the output current I_l. The sizing of the output transistor

under I_{DSQ} must ensure that it can at least handle the negative peak signal current. A test bench for an NMOS output stage, as shown in figure 4.6(a), is used to verify the size of the transistor. Figure 4.6(b) shows the simulation results of the output current I_l versus V_{gs} for $W = 400\mu$, $L = 40n$. I_{DSQ} is set to 2mA to leave enough output margin. V_{DSQ} is set to 1V to guarantee the transistor is in forward saturation. The biasing and sizing conditions are enough to drive the signal current.

(a) Test-bench of output drive capability



(b) Output current - DC sweep

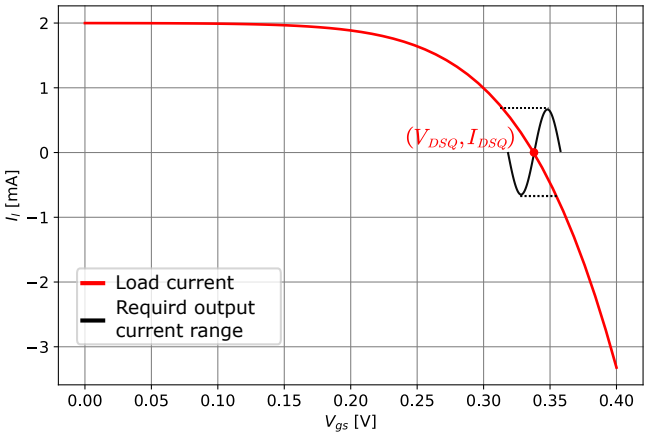


Figure 4.6: (a) The test-bench of output drive capability of the output transistor in the TA stage when $W = 400\mu$, $L = 40n$, $I_{DSQ} = 2\text{mA}$, and $V_{DSQ} = 1\text{V}$. The load resistance is assumed to be zero since the input impedance of the transimpedance stage approximates zero. (b) The load current I_l versus input voltage V_{gs} of the output transistor.

Feasibility of a one-stage TA amplifier

The design of a one-stage amplifier may be feasible if the requirements of noise and drive capability are compatible. The discussion of the noise optimization of the input stage indicates that the input transistor needs to have $W = 400\mu$, $L = 40n$ and $I_{DSQ} \geqslant 0.5\text{mA}$ to ensure its input-referred voltage noise PSD is smaller than $2 \times 10^{18}\,[\text{V}^2/\text{Hz}]$. The requirements derived from noise are compatible with that from drive capability, which needs $W = 400\mu$, $L = 40n$, and $I_{DSQ} = 2\text{mA}$ for the output transistor. There is no show-stopper for the one-stage design until now. Therefore, we will start with the discussion of the one-stage design in next section [Bandwidth and accuracy].

4.3 Bandwidth and accuracy

In this section, we will design the bandwidth and the DC loop gain according to table 4.1 such that they satisfy the bandwidth and accuracy requirements. The calculations and analysis of loop gain and LP product (Loop gain Poles product) are based on the AGM (Asymptotic Gain Model)[18]. The discussion will start with the one-stage TA amplifier design. If it cannot satisfy the requirements, we will further explore the design of a multiple-stage TA amplifier.

One stage design: CS

The analysis of noise and drive capability indicates a one-stage TA amplifier solution with a CS controller. As explained in section 4.1 [Noise optimization] and 4.2[Drive capability], for the design of a multiple-stage amplifier, the CS stage is the best in terms of noise and drive capability compared with CG and CD stages, which are the local feedback versions of CS stage. Figure 4.7(a) shows the one stage transadmittance amplifier with a CS controller and the tested crystal as the feedback component. The transistors have $W = 400\mu$, $L = 40n$, and $I_{DSQ} = 2\mathrm{m}$ to meet with both noise and drive capability. Its equivalent single-ended small-signal diagram at resonance frequency is shown in figure 4.7(b).

In section 3.3[Frequency response], we have seen that the bondwire inductance L_w limits the bandwidth. It might be surprising that L_w has been set to zero. This is mainly because the analysis of L_w in the very early stage will add design complexity and interrupt the analysis of loop gain. Actually, the influence of L_w could be considered as an excessive phantom zero compensation. We will discuss this effect later in section 4.4.

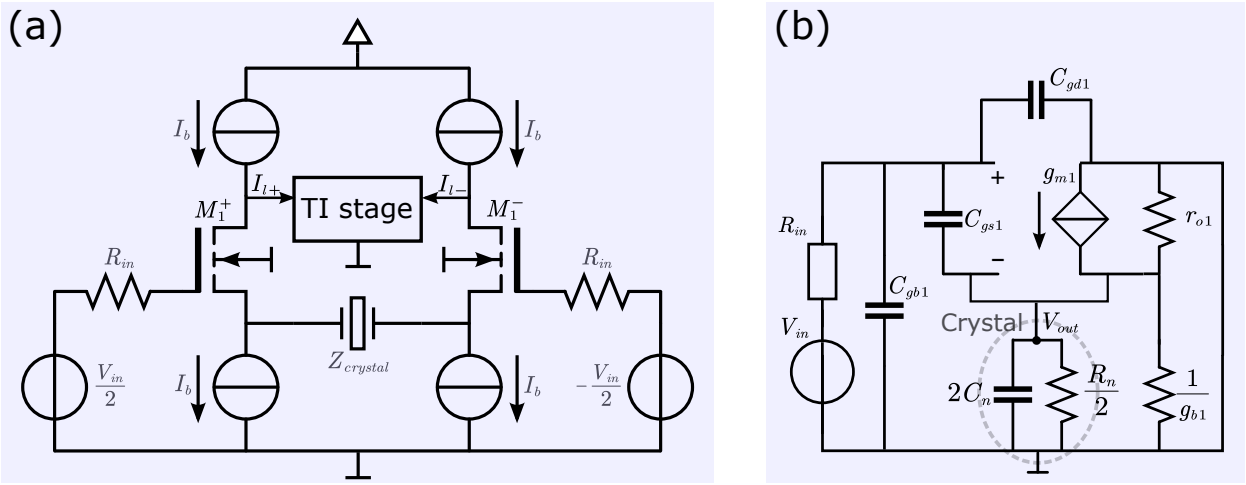


Figure 4.7: (a) One stage transadmittance amplifier with a CS controller. The voltage biasing sources are not shown. (b) Equivalent single-ended small-signal diagram of (a). At resonance frequency, R_n =6.14, 52.33, and 308.1 stands for the equivalent small-signal diagram for the base tone, the third overtone and the fifth overtone, respectively. At high frequency, R_n is opened and the crystal is purely capacitive.

Based on the small-signal diagram in figure 4.7(b). The quick estimation of circuit performance can be realized with SLICAP. The SLICAP script provides the function to plot the loop gain, meanwhile calculating its poles and zeros, and all relevant EKV parameters such as g_m, f_T, and parasitics. Keeping track of the poles and zeros from an early design stage gives designers more insights into the design. For example, we can estimate which component in the circuity is dominant at certain performance, so that we can better know how to adjust the parameters of transistor and compensate for undesired frequency response. Table 4.2 shows a summary of the poles and zeros according to figure 4.7(b). The hand calculation of the poles and zeros is based on the equivalent loop gain calculation diagram as shown in figure 4.8.

The DC loop gain of the one-stage amplifier could be calculated by Eq 4.3.1 according to figure 4.7(b). The bandwidth of the one-stage amplifier could be calculated by LP product[18]. LP_1 of the system is given by Eq 4.3.2. Observing the poles' positions in table

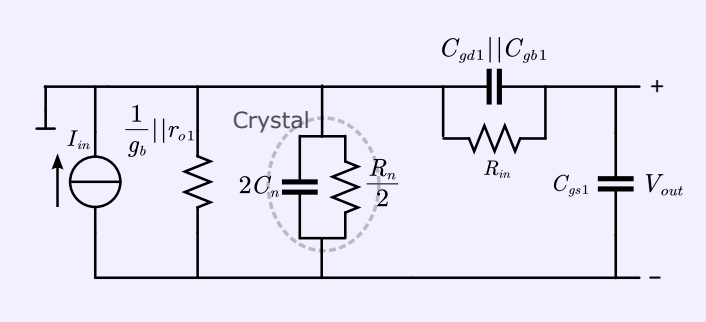


Figure 4.8: Equivalent loop gain calculation diagram of one-stage transadmittance amplifier. The voltage controlled current source g_{m1} is set to zero to break the loop and create loop gain reference. Loop gain of the amplifier could be calculated as V_{out}/I_{in}.

Pole/Zero	Status	Hand Calculation		SLiCAP
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	new	$\frac{-1}{2\pi\left(\frac{R_n}{2}\|\|r_{o1}\|\|\frac{1}{g_{b1}}\right)2C_n}$	$\frac{-1}{2\pi\left(\frac{R_n}{2}\|\|800\|\|43\right)\cdot 3.3p} = -[15.7G, 3.01G, 1.26G, 1.12G]$	$-[13.7G, 2.85G, 1.41G, 1.11G]$
Source pole P_2 [Hz]	new	$\frac{-1}{2\pi R_{in}\left(C_{gs1}+C_{dg1}+C_{gb1}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot(0.15+0.018+0.024)p} = -16.7G$	$-[19.9G, 17.1G, 17.0G, 17.0G]$
Source zero Z_1 [Hz]	new	$\frac{-1}{2\pi R_{in}\left(C_{dg1}+C_{gb1}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot 0.042p} = -75.8G$	$-[73.2G]$

Table 4.2: Loop gain pole-zeros of the one-stage TA amplifier with a CS controller and a crystal settling the gain. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero. The column under SLICAP shows the simulation results for $R_n = [6.14, 52.33, 308.1, \infty]\,\Omega$. $R_n = \infty$ stands for the frequency response off resonance, which is the interest of frequency compensation.

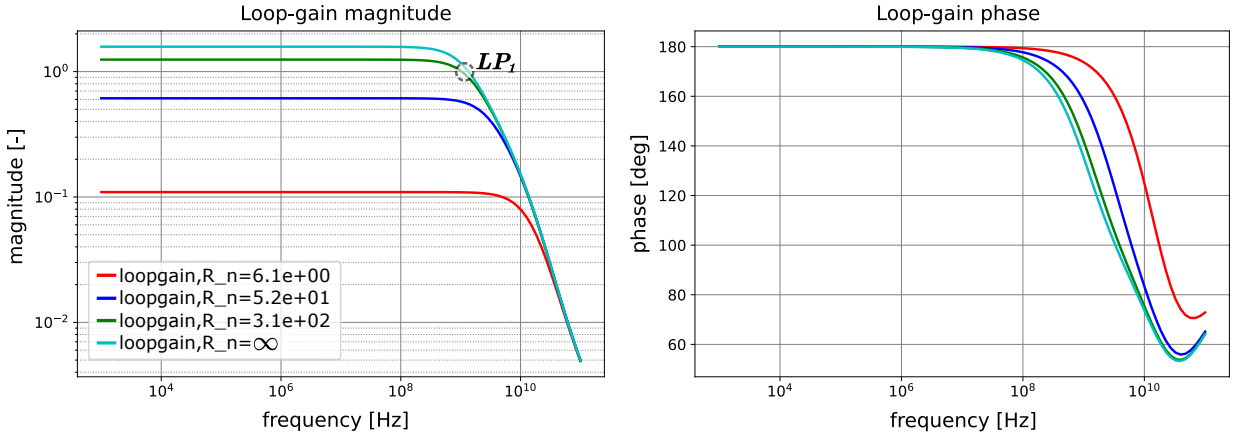


Figure 4.9: Loop gain magnitude and phase of the one-stage TA amplifier. For the base tone and the third overtone, the loop gain is less the unity so that their bandwidth is ineffective. The effective bandwidth, LP_1, is given by the intersection point of loop gain and X-axis, which is almost equal for the three tones.

4.2, P_2 is far away from LP_1. Therefore. the system is a first order system whose bandwidth can be estimated by LP_1.

$$L_{DC} = -g_m\left(\frac{R_n}{2}||r_{o1}||\frac{1}{g_{b1}}\right) \tag{4.3.1}$$

$$LP_1 = (1 - L_{DC}) \cdot P_1 \approx \frac{g_{m1}}{2\pi \cdot 2C_n} \,[\text{Hz}] \tag{4.3.2}$$

According to the numeric values of the small-signal parameters provided by the SLICAP script, we can estimate the DC loop gain and bandwidth for the different R_n. For example, the DC loop gain of the third overtone could be calculated as $L_{DC} = -0.038 \times (26.16||800||43) = -0.63$, which is less than unity. Its effective bandwidth, which is independent of R_n, could be calculated as $LP_1 = -0.038/4\pi \cdot 3.3p = -916\,[\text{MHZ}]$. Figure 4.9 shows the loop gain plot of the SLICAP script.

In conclusion, the low DC loop gain and bandwidth prove that the one-stage TA amplifier is not a feasible solution. An extra stage is needed to enhance DC loop gain and bandwidth. In addition, the second term($\frac{R_n}{2}||r_{o1}||\frac{1}{g_{b1}}$) of Eq.4.3.1 shows that the bulk effect of the transistor severely limits the DC loop gain. In order to eliminate the influence of bulk effect, a differential CS input stage could be applied with the price of extra power consumption, extra noise, and decrease of g_m.

One stage design: differential CS

Figure 4.10(a) shows the one stage transadmittance amplifier with a differential CS controller. Although this configuration causes noise twice, it is not a show-stopper we have left enough margins when we designed noise. Its equivalent single-ended small-signal diagram at resonance frequency is shown in figure 4.10(b). The conductance g_{b1} becomes a common-mode conductance and be eliminated from the small-signal diagram. The expression of DC loop gain and LP product changes from Eq.4.3.1 and Eq.4.3.2 to:

$$L_{DC} = -\frac{1}{2} g_{m1} \left(\frac{R_n}{2} || 2r_{o1} \right) \tag{4.3.3}$$

$$LP_1 = (1 - L_{DC}) \cdot P_1 \approx \frac{1}{2} g_m 2\pi \cdot 2C_n \,[\text{Hz}] \tag{4.3.4}$$

Compared with the unbalanced version, one disadvantage of the differential version is that the DC loop gain and LP product are half due to the half of g_m. Therefore, there is a trade-off between g_m and g_b. Either we choose to lose half g_m for the three tones or we deteriorate the performance of the third and fifth overtone more than half. Since we expect a relatively balanced performance among three tones, the design of a differential CS input could be a feasible solution. However, the one-stage amplifier with differential CS input still shows a low DC loop gain and bandwidth. Table 4.3 updates the pole/zero information for the differential version according to figure 4.10(b). The corresponding loop gain plot is shown in figure 4.11.

Discussion of two-stage design solutions

The design of a one-stage TA amplifier fails because of its low DC loop gain and bandwidth, which cannot meet the design specifications. To further boost DC loop gain and bandwidth, we need to add an extra stage. Establishing correct signal path with negative feedback, the two solutions are CS+CD and DFCS (differential common-source) + CS as shown in figure 4.12.

The main difference between the two structures is where the bulk effect exists. In CS+CD structure, the input stage has bulk effect while the output stage barely suffers from

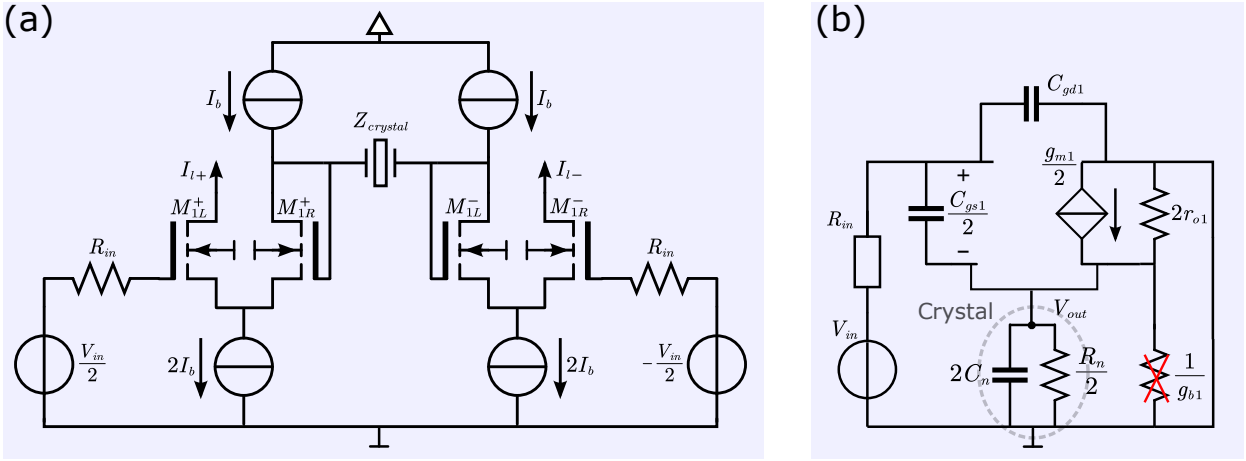


Figure 4.10: (a) One stage transadmittance amplifier with a differential CS controller. The voltage biasing sources are not shown. (b) Equivalent single-ended small-signal diagram of (a).

Pole/Zero	Status	Hand Calculation		SLICAP
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	modified	$\frac{-1}{2\pi\cdot\left(\frac{R_n}{2}\|\|2r_o\right)\cdot(2C_n)}$	$\frac{-1}{2\pi\cdot\left(\frac{R_n}{2}\|\|1600\right)\cdot 3.3p}$ $-[15.6G, 1.85G, 315M, 30M]$	$-[15.0G, 1.82G, 333M, 29.3M]$
Source pole P_2 [Hz]	modified	$\frac{-1}{2\pi R_{in}\left(C_{gs1}/2+C_{dg1}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot\left(\frac{0.174}{2}+0.02\right)p}=-29.7G$	$-[30.6G]$
Source zero Z_1 [Hz]	modified	$\frac{-1}{2\pi R_{in}C_{dg1}}$	$\frac{-1}{2\pi\cdot 50\cdot 0.02p}=-160G$	$-[169G]$

Table 4.3: Loop gain pole-zeros of the one-stage TA amplifier with a differential CS controller. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero. The column under SLICAP shows the simulation results for $R_n = [6.14, 52.33, 308.1, \infty]\,\Omega$. $R_n = \infty$ stands for the frequency response off resonance, which is the interest of frequency compensation.

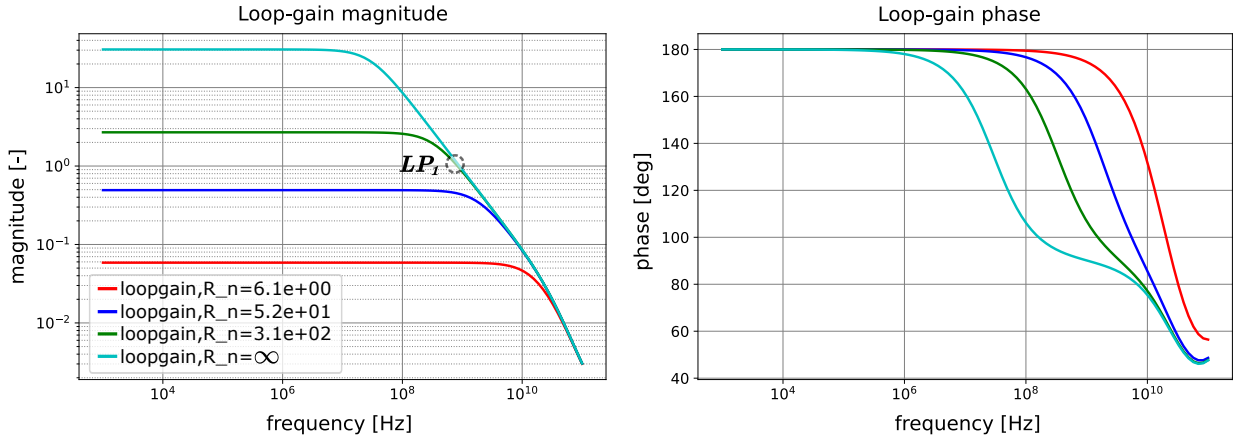


Figure 4.11: Loop gain magnitude and phase of the one-stage TA amplifier with a differential CS controller. For the base tone and the third overtone, the loop gain is less the unity so that their bandwidth is ineffective. The effective bandwidth, LP_1, is given by the intersection point of loop gain and X-axis, which is almost equal for the three tones. Comparing with Fig 4.9, both DC loop gain and bandwidth are less.

bulk effect since it drives a transimpedance amplifier. In the DFCS+CS structure, only output stage has bulk effect. Since the simulation result shows the bulk effect of the input stage

will significantly influence frequency response, we prefer to eliminate the bulk effect of the input stage. Therefore, we will apply a DFCS+CS structure for the two-stage design. If the bulk effect of the second stage becomes a show-stopper, we can also change the second stage to a DFCS stage later.

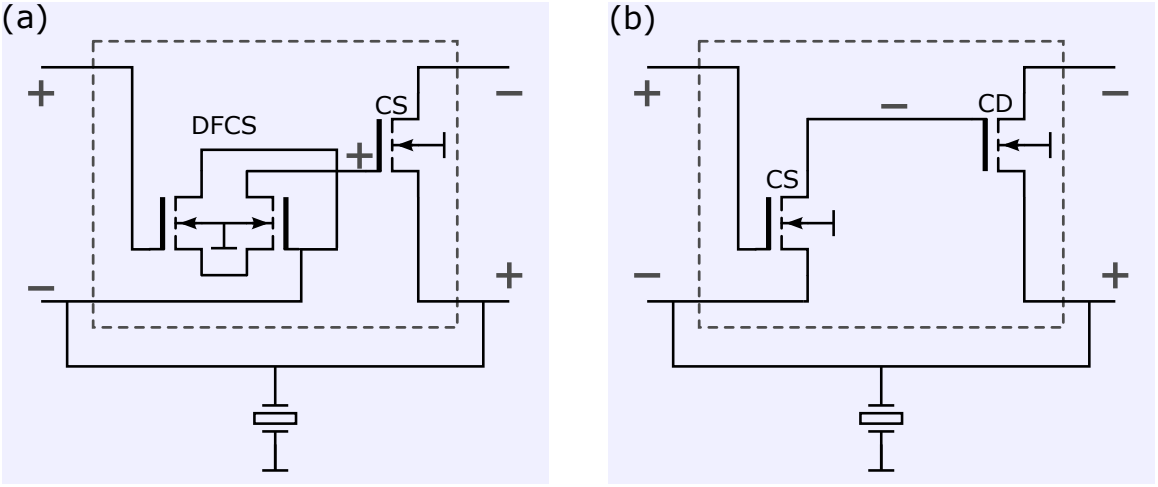


Figure 4.12: The structures of two-stage design solutions. (a) DFCS + CS. (b) CS + CD. The biasing sources are not shown. Only single-ended signal path is presented to avoid complexity.

Two stage design: DFCS + CS

Figure 4.13 shows the two stage transadmittance amplifier with a DFCS+CS controller. Its equivalent single-ended small-signal diagram at resonance frequency is shown in figure 4.14. The initial sizing of the input DFCS stage uses the same settings ($W = 400\mu$, $L = 40n$ and $I_D = 0.5m$) derived from noise analysis. The sizing of the output CS stage uses the same settings ($W = 400\mu$, $L = 40n$, and $I_{DSQ} = 2\mathrm{m}$) derived from drive capability analysis.

The new loop gain plot is shown in Fig.4.15. A new intermediate pole is introduced by the input capacitance of the second stage and the output impedance of the input stage. The feedback pole P_1 is limited by the bulk effect of the second stage. A new zero is introduced due to the direct transfer through the miller capacitance of the second stage, which interacts with the source zero Z_1. Table 4.4 summarize the poles/zeros of the two-stage TA amplifier. The estimations are obtained based on the small-signal diagram in Fig.4.14 and compared with the calculation results of the SLICAP script.

The DC loop gain of the two-stage TA amplifier is given by:

$$L_{DC} = -g_{m1}g_{m2}r_{o1}\left(\frac{R_n}{2}||r_{o2}||\frac{1}{g_{b2}}\right) \tag{4.3.5}$$

The design of the second stage introduced a dominant pole P_3, which may increase the order of the system. Because the source pole P_2 is non-dominant, the bandwidth estimated by LP product is updated to Eq 4.3.6 for higher order system.

$$BW = \min\{LP_1, LP_2\} = \min\begin{cases} LP_1 = (1 - L_{DC}) \cdot P_1 \approx \frac{1}{2\pi} g_{m1}\frac{g_{m2}}{C_{iss2}}\left(\frac{R_n}{2}||r_{o2}||\frac{1}{g_{b2}}\right) \\ LP_2 = \sqrt{(1 - L_{DC}) \cdot P_1 \cdot P_3} \approx \frac{1}{2\pi}\sqrt{g_{m1}\frac{g_{m2}}{C_{iss2}}\frac{1}{2C_n}} \end{cases} \tag{4.3.6}$$

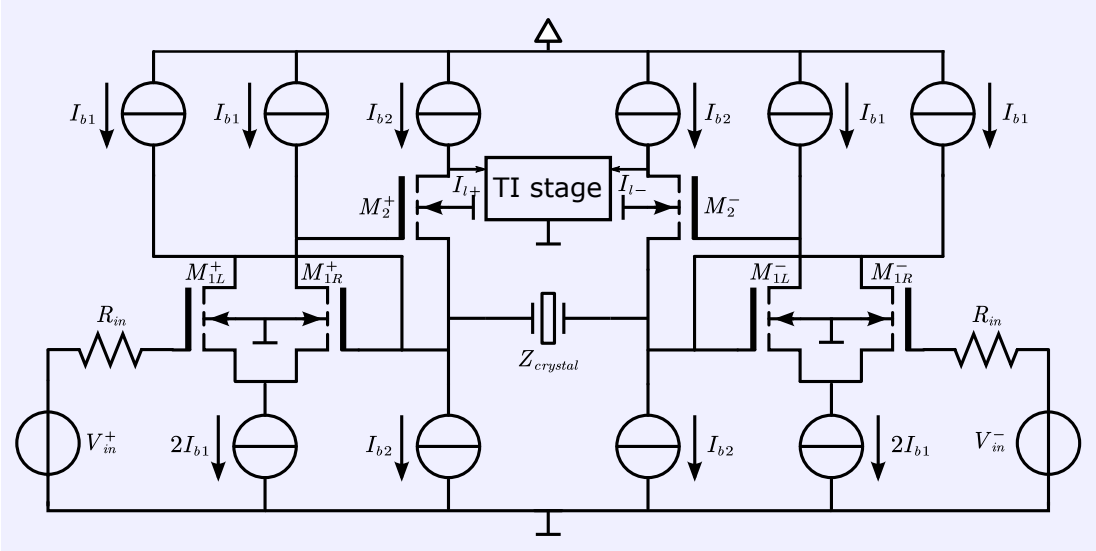


Figure 4.13: Two stage transadmittance amplifier with a DFCS+CS controller. The voltage biasing sources are not shown.

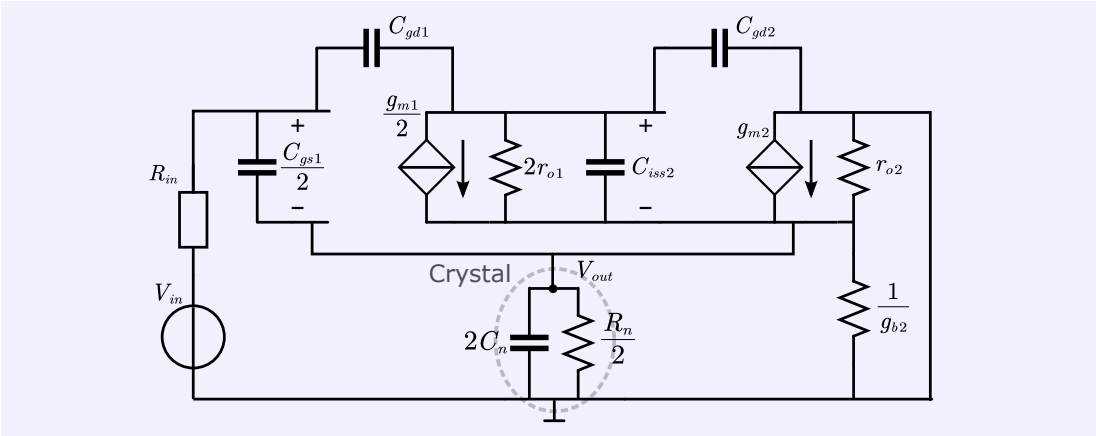


Figure 4.14: Equivalent single-ended small-signal diagram of Fig 4.13

For example, the DC loop gain of the third overtone could be calculated as $L_{DC} = -11m \cdot 38m \cdot 667 \cdot (26.16||250||43) = -4.46$. Its bandwidth could be calculated as $LP_2 = -1/2\pi \cdot \sqrt{11m \cdot 31G \cdot 1/3.3p} = -1.62$[GHz]. For the base tone, the DC loop gain could be calculated as $L_{DC} = -11m \cdot 38m \cdot 667 \cdot (3.07||250||43) = -0.86$, which is still less than unity. Its bandwidth could be simply calculated as $LP_1 = -1/2\pi \cdot 11m \cdot 31G \cdot (3.07||250||43) = -163$[MHz], since its P_1 is non-dominant. The loop gain plot in Fig 4.15 confirms the above calculations.

The initial settings of the two-stage TA amplifier show insufficiency in DC loop gain and bandwidth, especially for the base tone. According to Eq 4.3.5 and Eq 4.3.6, we can enhance both L_{DC} and bandwidth by increasing the g_m of the two stages. At the same time, increasing output impedance r_{o1} of the first stage and cut-off frequency ($f_{T2} = g_{m2}/C_{iss2}$) of the second stage is helpful to boost DC loop gain and bandwidth, respectively, without triggering a design contradiction.

Based on this strategy, the drain current I_D of the first stage and the second stage is set to 5mA and 3mA. Since the input transistors are most likely working in weak inversion as the analysis in section 4.1[Noise optimization], the term $g_{m1}r_{o1}$ in Eq 4.3.5 will not change

Pole/Zero	Status	Hand Calculation		SLICAP
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	modified	$\frac{-1}{2\pi\cdot\left(\frac{R_n}{2}\|\|r_{o2}\|\|\frac{1}{g_{b2}}\right)\cdot(2C_n)}$	$\frac{-1}{2\pi\left(\frac{R_n}{2}\|\|250\|\|43\right)\cdot 3.3p}$ $-[15.7G, 3.01G, 1.26G, 1.12G]$	$-[15.6G, 2.93G, 1.46G, 1.11G]$
Source pole P_2 [Hz]	unmodified	$\frac{-1}{2\pi R_{in}\left(C_{gs1}/2+C_{dg1}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot\left(\frac{0.174}{2}+0.02\right)p} = -29.7G$	$-[30.6G]$
Intermediate pole P_3 [Hz]	new	$\frac{-1}{2\pi\cdot 2r_{o1}\cdot C_{iss2}}$	$\frac{-1}{2\pi\cdot 1334\cdot 0.2p} = -596M$	$-[542M, 552M, 570M, 585M]$
Source zero Z_1 [Hz]	modified	N/A(a)		$[-14.9G - 19.4G\cdot i]$
Direct zero Z_2 [Hz]	new	N/A(a)		$[-14.9G + 19.4G\cdot i]$

Table 4.4: Loop gain pole-zeros of the two-stage TA amplifier with a CSDF+CS. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero. The column under SLICAP shows the simulation results for $R_n = [6.14, 52.33, 308.1, \infty]\,\Omega$. $R_n = \infty$ stands for the frequency response off resonance, which is the interest of frequency compensation. (a) The interaction between the original source zero Z_1 and the zero Z_2 caused by direct transfer of the new CS stage makes it difficult to do hand calculation.

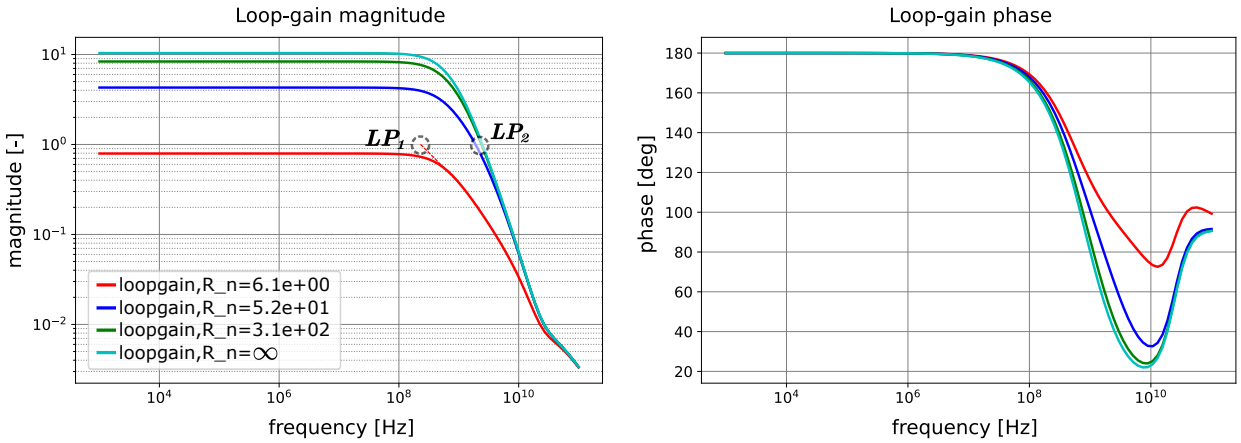


Figure 4.15: Loop gain magnitude and phase of the two-stage TA amplifier with a DFCS+CS controller. For the base tone, the loop gain is less the unity so their bandwidth is ineffective. The effective bandwidth of the base tone is given by LP_1. The bandwidth of the third and fifth overtone is decided by LP_2.

too much by increasing drain current I_{D1}. To effective boost L_{DC}, the width and length of the first stage are tripled to $W_1 = 1200\mu$, $L_1 = 120n$ so as to increase r_{o1}. The width of the second stage is decreased to $W_2 = 100\mu$ to increase f_{T2} while still having enough drive capability. The loop gain plot after the adjustment is shown in Fig.4.16. Table 4.5 tracks the poles/zeros after the adjustment.

4.4 Frequency compensation

A low phase margin when $R_n = \infty$ as shown in figure 4.16 implies a critical stability problem. The compensation techniques[18], such as phantom zero and pole splitting, need to be applied to acquire a stable frequency response.

Pole/Zero	Status	Hand Calculation		SLICAP(a)
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	modified	$\frac{-1}{2\pi\cdot\left(\frac{R_n}{2}\|\|r_{o2}\|\|\frac{1}{g_{b2}}\right)\cdot(2C_n)}$	$\frac{-1}{2\pi\left(\frac{R_n}{2}\|\|189\|\|65\right)\cdot 3.3p}$ $-[15.7G, 2.6G, 1.07G, 1.00G]$	$-[17.8G, \|1.69G\|, \|1.21G\|, \|1.06G\|]$
Source pole P_2 [Hz]	modified	$\frac{-1}{2\pi R_{in}\left(C_{gs1}/2+C_{dg1}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot\left(\frac{1.46}{2}+0.05\right)p} = -4.08G$	$-[3.6G, 6.2G, 5.6G, 5.4G]$
Intermediate pole P_3 [Hz]	modified	$\frac{-1}{2\pi\cdot 2r_{o1}\cdot C_{iss2}}$	$\frac{-1}{2\pi\cdot 500\cdot 0.13p} = -2.45G$	$-[1.6G, \|1.69G\|, \|1.21G\|, \|1.06G\|]$
Source Zero z_1 [Hz]	modified	N/A		$-\|33.5G\|$
Direct Zero z_2 [Hz]	modified	N/A		$-\|33.5G\|$

Table 4.5: Loop gain pole-zeros of the two-stage TA amplifier with a CSDF+CS after adjustment. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero. The column under SLICAP shows the simulation results for $R_n = [6.14, 52.33, 308.1, \infty]\,\Omega$. $R_n = \infty$ stands for the frequency response off resonance, which is the interest of frequency compensation. (a) The complex poles/zeros are expressed with their magnitude.

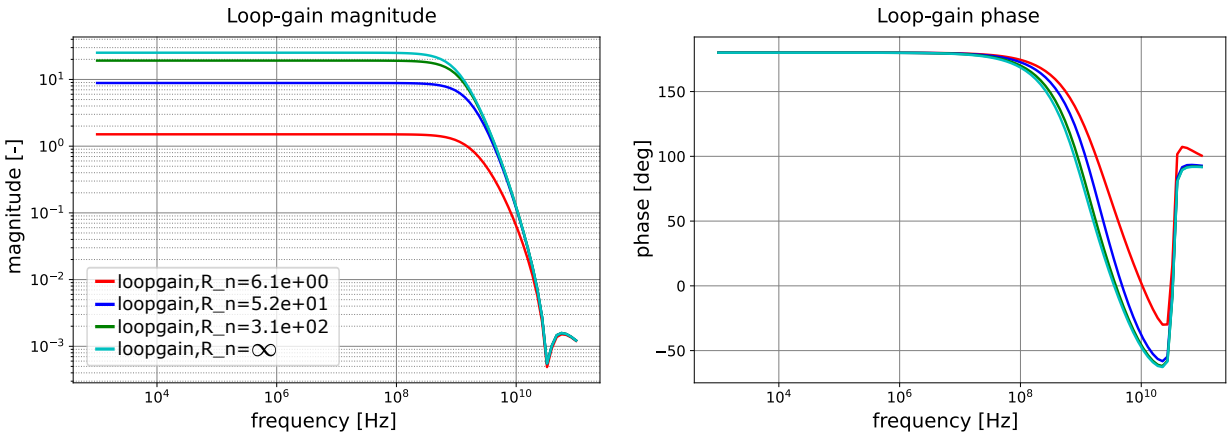


Figure 4.16: Loop gain magnitude and phase of the two-stage TA amplifier with a DFCS+CS controller after adjustment. Although the amplifier meets with the requirements of DC loop gain and bandwidth, its stability ($R_n = \infty$) becomes critical because low phase margin.

Phantom zero

As stated in section 3.3.3[Frequency response], the bondwire inductance L_w behaves like a pair of inevitable phantom zeros to limit the bandwidth. Eq 3.3.18 indicates the bondwire L_w terminates the asymptotic gain at low frequency, which is the target bandwidth to be achieved. In addition, it also deteriorates stability since it has high Q interaction with the shunt capacitance C_o of crystal. In order to undamp the high Q interaction and correct undesired frequency response, we need to add resistance in series with L_w and change the position of the original phantom zero pair. It is important to know that the changed phantom zeros cannot increase bandwidth since the attenuation happens in asymptotic gain not loop gain. To enhance the effective bandwidth, the only way is to reduce the inductance of the bondwire. Figure 4.17 shows the TA amplifier after implementation of phantom zero technique.

In order to design a MFM system, the value of the phantom zero resistance R_{phz} could

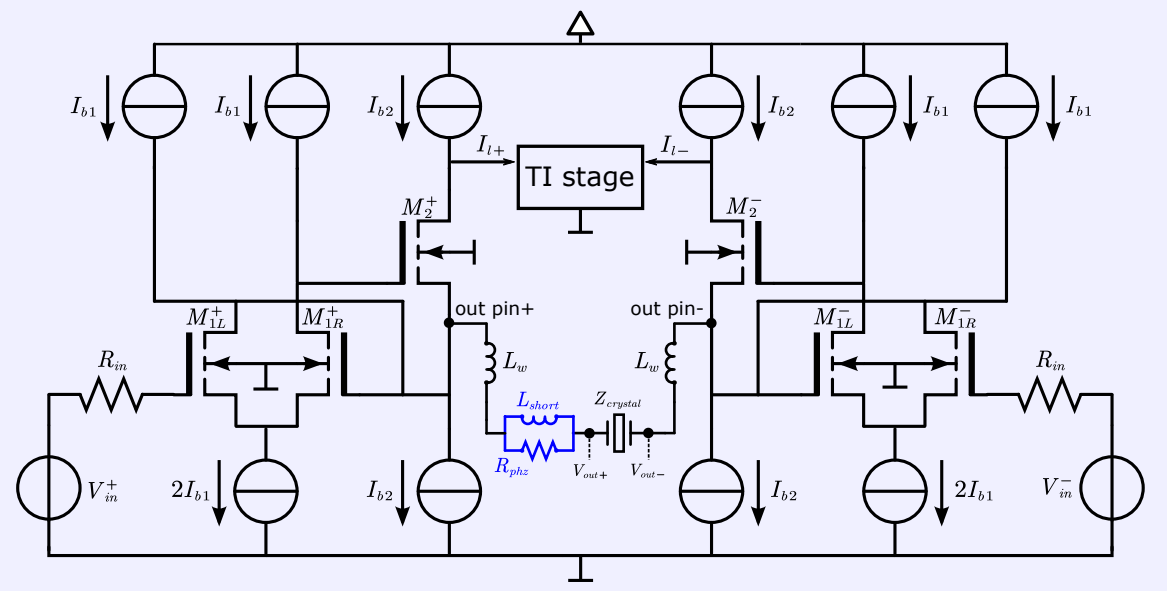


Figure 4.17: Two stage transadmittance amplifier with a DFCS+CS controller with phantom zero (blue part) implemented in series with crystal. The voltage biasing sources are not shown.

be calculated as:

$$R_{phz} = \frac{1}{Q}\sqrt{\frac{2L_w}{C_o}} = \sqrt{2}\sqrt{\frac{2 \cdot 1.5n}{1.65p}} = 60\,[\Omega] \tag{4.4.1}$$

Fig 4.18(a) shows the root locus after implementation of R_{phz} with a capacitive crystal feedback($R_n = \infty$). With the increase of R_{phz}, quality factor of the dominant poles gradually decrease and the system becomes an MFM system when $R_{phz} = 60\Omega$. Fig 4.18(b) shows the magnitude transfer function ($(V_{out+} - V_{out-})/V_{in}$) before and after phantom zero compensation for $R_n = \infty$. The damping of the system is eliminated without a decrease in bandwidth.

However, the design of R_{phz} inevitably limits the asymptotic gain for the three tones which are resistive at resonance frequency. As a result, the DC magnitude transfer is limited by R_{phz}, which means serious deterioration of quality factor and CNR, especially for the base tone and the third overtone. Fig 4.19(a) illustrates this effect. To avoid the loss of DC gain, an inductor L_{short} is inserted in parallel with R_{phz} to short R_{phz} at low frequency. But, L_{short} makes the phantom zero compensation less effective since it reduces the effective resistance. Since the settling time and overshoot of the system are not the design interest, we allow certain damping of frequency response, as shown in Fig 4.19, to exchange lower phase shift at resonance frequency in the premise of system stability. In this case, L_{short} is set to 2[nH]. Table 4.6 tracks the poles/zeros after implementation of phantom zero.

Pole splitting

The design of in-chip inductor may cost a large size and makes phantom zero compensation less attractive. One solution is to make the compensation component (R_{phz} and L_{short}) outside the chip. The other solution is to use miller capacitor at the second stage to compensate undesired frequency response. A capacitor C_{ps} is added in between the gate and the drain of the second stage to implement the pole splitting with a series resistor $R_{ps} = 1/g_{m2}$.

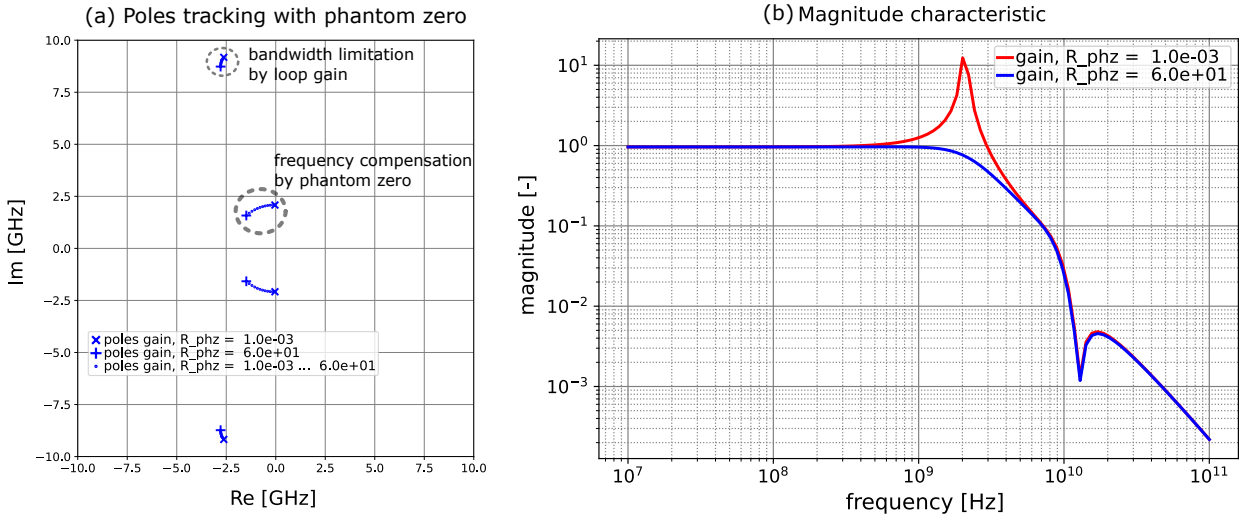


Figure 4.18: (a) Positions of poles vary with the value of R_{phz}. The bandwidth limitation of loop gain (or servo function) is larger than 8GHz, which is much higher than the bandwidth limitation of phantom zero. The system becomes an MFM system when R_{phz}=60Ω. (b) Magnitude characteristics before and after the implementation of phantom zero. The system is undamped by R_{phz}

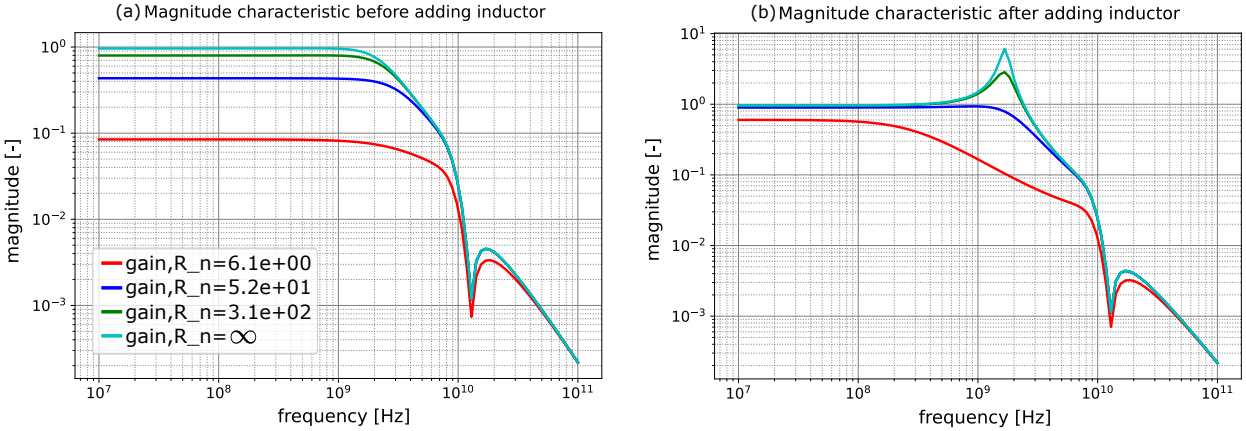


Figure 4.19: (a) Magnitude characteristic before adding inductor L_{short}. The DC gain of the three tones are limited by R_{phz}. (b) Magnitude characteristic after adding inductor L_{short}. Now the DC magnitude transfer meets with the design requirement, but the phantom zero compensation becomes less effective.

This resistor compensates for the positive zero coming from the direct transfer through the pole splitting. Figure 4.17 shows the TA amplifier after implementation of phantom zero technique.

The bandwidth limitation is due to the phantom zero caused by L_w and the crystal. The pole splitting causes the feedback pole P_1 and the intermediate pole P_3 to split away from each other and this influence gradually propagates to the phantom zero. Fig 4.21(a) illustrates this effect. The change of loop gain bandwidth limitation is much more dominant than that of phantom zero bandwidth limitation. The system gradually becomes stable because the pole splitting decreases the overall loop bandwidth and quality factor as shown in Fig 4.21(b). To make the compensation effective, C_{ps} and R_{ps} is set to 0.9pF and 38Ω. Table 4.7 summarizes the poles/zeros after the implementation of pole splitting.

Pole/Zero	Status	Hand Calculation/ Explanation		SLICAP(a)
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	unmodified	$\frac{-1}{2\pi\cdot\left(\frac{R_n}{2}\|\|r_{o2}\|\|\frac{1}{g_{b2}}\right)\cdot(2C_n)}$	$\frac{-1}{2\pi\left(\frac{R_n}{2}\|\|189\|\|65\right)\cdot 3.3p}$ $-[15.7G, 2.6G, 1.07G, 1.00G]$	$-[17.8G, \|1.69G\|, \|1.21G\|, \|1.06G\|]$
Source pole P_2 [Hz]	modified	$\frac{-1}{2\pi R_{in}\left(C_{dg1}\|\|\frac{C_{db}}{2}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot 15f} = -212G$	$-263G$
Intermediate pole P_3 [Hz]	unmodified	$\frac{-1}{2\pi\cdot 2r_{o1}\cdot C_{iss2}}$	$\frac{-1}{2\pi\cdot 500\cdot 0.13p} = -2.45G$	$-[1.6G, \|1.69G\|, \|1.21G\|, \|1.06G\|]$
Phantom Z. pole P_4, P_5 [Hz]	new	Complex poles caused by phantom zero.(b)		$-[2.67G, \|3.14G\|, \|2.91G\|, \|2.86G\|]$
Phantom Z. pole P_6 [Hz]	new	Pole caused by L_{short}.		$-[9.20G, 8.33G, 7.70G, 7.70G]$
Source Zero Z_1 [Hz]	unmodified	N/A		$-33.5G$
Direct Zero Z_2 [Hz]	unmodified	N/A		$-33.5G$
Phantom Z. zero Z_3, Z_4 [Hz]	new	$\frac{-1}{2\pi\sqrt{2L_wC_0}}$	$\frac{-1}{2\pi\sqrt{2L_wC_0}} = \frac{-1}{2\pi\sqrt{2\cdot 1.5n\cdot 1.5p}} = -2.26G$	For base tone, $Z_3 = -0.2G, Z_4 = -15.2G$ For the others, $Z_3 = Z_4 = -\|1.78G\|$ (c)
Phantom Z. zero Z_5 [Hz]	new	Zero caused by L_{short}.		$-[8.25G, 8.33G, 8.41G, 8.42G]$

Table 4.6: Loop gain pole-zeros of the two-stage TA amplifier with a CSDF+CS after phantom zero compensation. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The column under SLICAP shows the simulation results for $R_n = [6.14, 52.33, 308.1, \infty]\,\Omega$. $R_n = \infty$ stands for the frequency response off resonance, which is the interest of frequency compensation. (a) The complex poles/zeros are expressed with their magnitude. (b)Their frequency should be higher than phantom zero Z_3 and Z_4 to ensure effective compensation. (c) the mismatch between hand calculation and SLICAP results is because L_{short} decreases the frequency where bandwidth limitation happens.

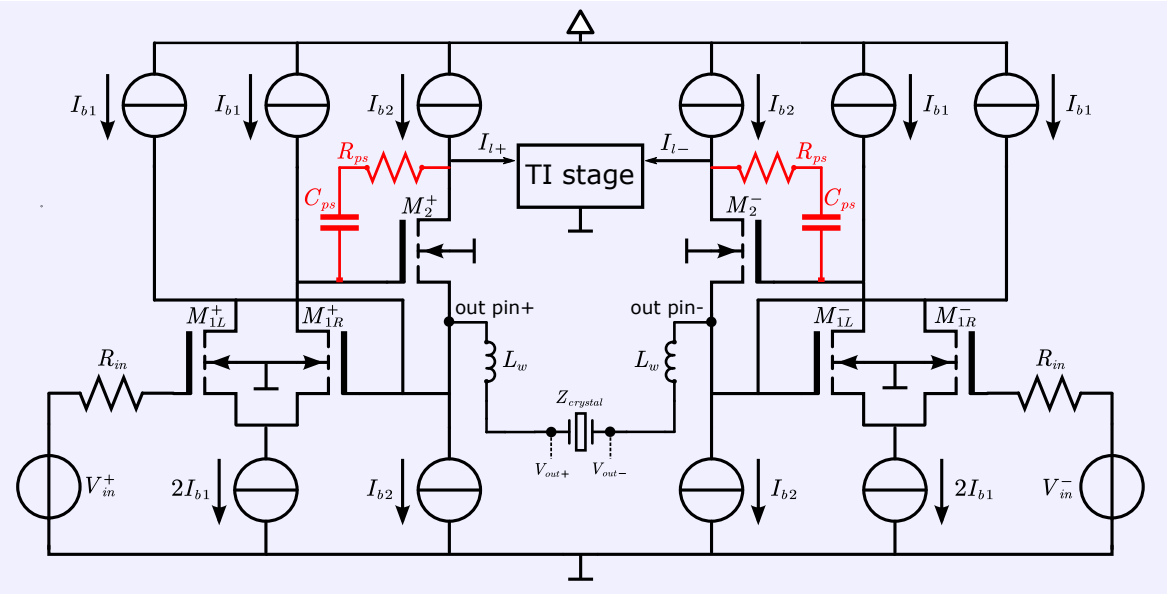


Figure 4.20: Two stage transadmittance amplifier with a DFCS+CS controller with pole splitting (red part) implemented in between the gate and the drain of the second stage. The voltage biasing sources are not shown.

Conclusion

Unlike the phantom zero compensation, the pole splitting does not interrupt DC transfer since there is no extra resistor in series with the crystal. A comparison of compensated

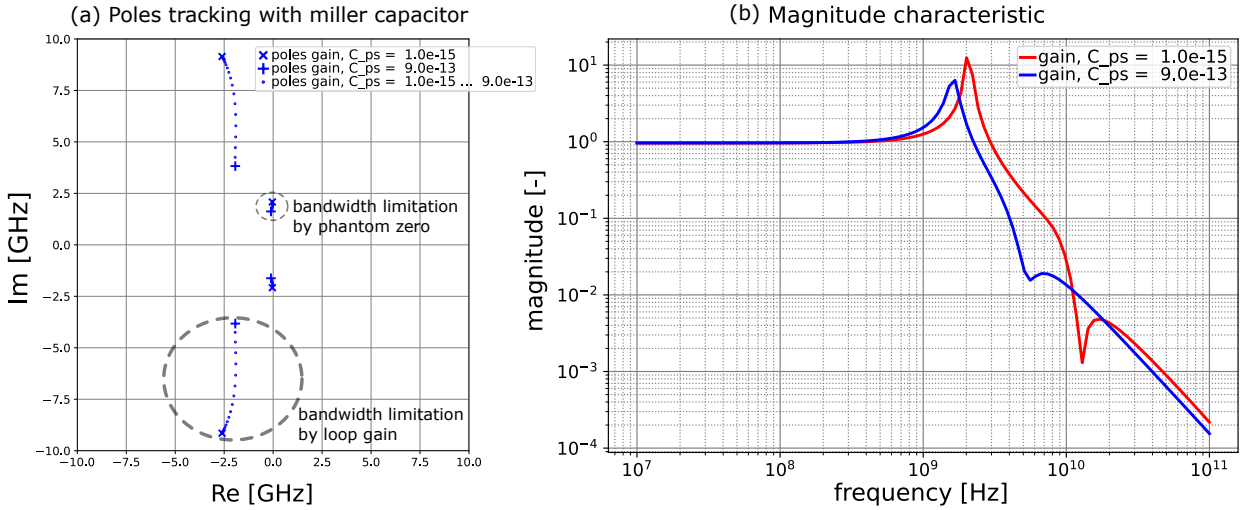


Figure 4.21: (a) Positions of poles vary with the value of C_{ps}. The bandwidth limitation of loop gain (or servo function) decreases and gradually propagates its effect to that of phantom zero. The system becomes stable with less bandwidth. (b) Magnitude characteristic before and after the implementation of pole splitting.

Pole/Zero	Status	Hand Calculation/ Explanation		SLICAP(a)
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	modified(b)	$\frac{-1}{2\pi\cdot\left(\frac{R_n}{2}\|\|r_{o2}\|\|\frac{1}{g_{b2}}\right)\cdot(2C_n)}$	$\frac{-1}{2\pi\left(\frac{R_n}{2}\|\|189\|\|65\right)\cdot 3.3p}$ $-[15.7G, 2.6G, 1.07G, 1.00G]$	$-[15.3G, \|677M\|, \|466M\|, \|400M\|]$
Source pole P_2 [Hz]	modified	$\frac{-1}{2\pi R_{in}\left(C_{dg1}\|\|\frac{C_{db}}{2}\right)}$	$\frac{-1}{2\pi\cdot 50\cdot 15f} = -212G$	$-400G$
Intermediate pole P_3 [Hz]	modified(b)	$\frac{-1}{2\pi\cdot 2r_{o1}\cdot C_{iss2}}$	$\frac{-1}{2\pi\cdot 500\cdot 0.13p} = -2.45G$	$-[278M, \|677M\|, \|466M\|, \|400M\|]$
Phantom Z. pole P_4, P_5 [Hz]	new	Complex poles caused by phantom zero.		$-[\|3.05G\|, \|3.83G\|, \|3.87G\|, \|3.85G\|]$
P.s. pole P_6 [Hz]	new	Pole caused by R_{ps}.		$-20.6G$
Source Zero Z_1 [Hz]	modified	N/A		$-\|5.5G\|$
Direct Zero Z_2 [Hz]				
Phantom Z. zero Z_3, Z_4 [Hz]	new	$\frac{-1}{2\pi\sqrt{2L_wC_0}}$	$\frac{-1}{2\pi\sqrt{2L_wC_0}} = \frac{-1}{2\pi\sqrt{2\cdot 1.5n\cdot 1.5p}} = -2.26G$	For base tone, $Z_3 = -0.3G$, $Z_4 = -15.2G$ For the others, $Z_3 = Z_4 = -\|2.26G\|$ (c)
P.s. zero Z_5 [Hz]	new	Zero caused by R_{ps}.		$-178G$

Table 4.7: Loop gain pole-zero tracking of the two-stage TA amplifier with a CSDF+CS after pole splitting. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The column under SLICAP shows the simulation results for $R_n = [6.14, 52.33, 308.1, \infty]\,\Omega$. $R_n = \infty$ stands for the frequency response off resonance. (a) The complex poles/zeros are expressed with their magnitude. (b) The pole splitting causes the feedback pole P_1 and the intermediate pole P_3 to split away from each other.

results between two techniques is shown in Fig 4.22. Considering size and design difficulty, the pole splitting is preferred than the phantom zero compensation. A good strategy is that we first design the TA amplifier with the pole splitting. If the compensation is turned out to be insufficient, we can later design the phantom zero outside the chip.

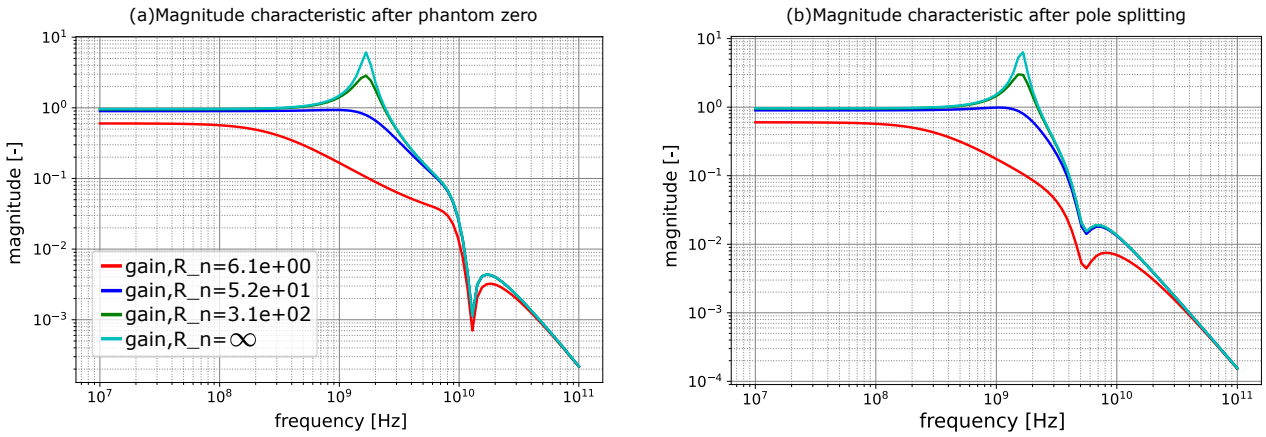


Figure 4.22: (a) Magnitude characteristic after phantom zero compensation. This figure is the same with Fig 4.19(b). (b) Magnitude characteristic after pole splitting. The high frequency response over 10GHz of pole splitting is more smooth than that of phantom zero since pole splitting undamps the overall loop but phantom zero only undamps the response where bandwidth limitation happens.

4.5 Implementation of biasing

The last step of an amplifier design is to bias the transistors in the signal path to achieve operating points, at which all the design specifications are met. Besides, the biasing network should not cause an excessive deterioration of circuit performance. The biased single-ended TA amplifier is shown in Fig 4.23(c).

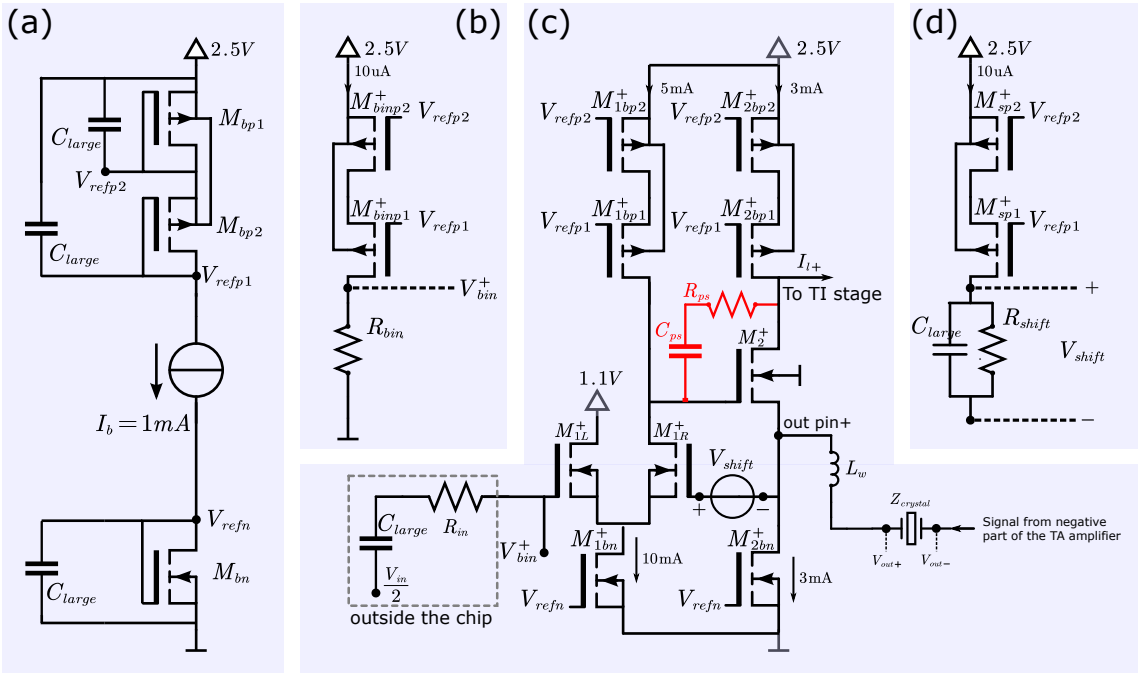


Figure 4.23: (a) The original current source which has $I_b = 1mA$. (b) The input biasing. (c) The biased single-ended TA amplifier. The negative part of the TA amplifier, which has the same structure, is not shown. One branch of the input stage is shorted to V_{DD} due to biasing limit. This would result in a bit less DC loop gain. (d) A voltage shift to provide stable biasing through negative feedback.

Current sources

The following lines show the requirements to design a current source:

- A ideal current source has infinite output impedance so that there is no loss of signal power due to the current source. A common solution is using biased transistors as current sources, which should have large r_o.
- In order to present a large r_o and avoid non-linearity, those transistors should always work in strong inversion under the maximum signal swing.
- The design of current sources by transistors should not introduce excessive noise.

Based on the above principles, the first design step is to test when the performance of the circuit starts to deteriorate due to the decrease of output impedance of the current sources, and derive related design specifications. This could be realized by connecting a RC branch in parallel with the ideal current sources. This RC branch has a large capacitor and a small resistor αR_{bias}, where α is the coefficient smaller than 1 and R_{bias} is the output impedance of the original current source. In DC, the ideal current sources bias the network. In AC, they behave lower output impedance.

Considering a design of 1mA original NMOS current source M_{bn} which has output impedance R_{biasn}. Due to the same length, the bottom current biasing M^+_{1bn} and M^+_{2bn} has output impedance $0.1R_{biasn}$ and $0.33R_{biasn}$, respectively. According to the simulation results shown in Fig 4.24, R_{biasn} should be larger than 2200Ω. The analysis also suits PMOS current sources. Similarly, we can derive the output impedance R_{biasp} of the original PMOS current source should be larger than 4200Ω.

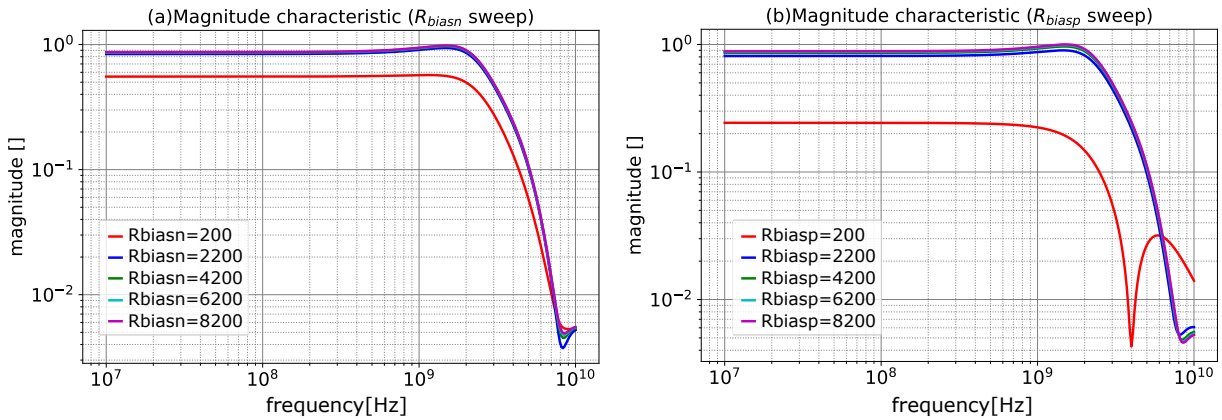


Figure 4.24: Magnitude transfer function ($(V_{out+} - V_{out-})/V_{in}$) of the third overtone ($R_n = 52$). (a) Sweep output impedance R_{biasn} of the original NMOS current source. (b) Sweep output impedance R_{biasp} of the original PMOS current source.

In order to keep the biased current sources in saturation region, the drain-source voltage of those transistors should be always higher than V_{dsat}. For example, the minimum V_{DS} of M^+_{1bn} could be calculated as:

$$V_{DS} = V^+_{bin} - V_{gs1} - \frac{V_{pp}}{2} \tag{4.5.1}$$

In this case, the range of V_{refn} is given by:

$$V^+_{bin} - V_{gs1} - \frac{V_{pp}}{2} + V_{thn} > V_{refn} > V_{thn} \tag{4.5.2}$$

$$720 > V_{refn} > 430\,[\mathrm{mV}] \tag{4.5.3}$$

The signal swing $V_{pp}/2$, the threshold voltage V_{thn}, and V_{gs1} could be obtained from the former analysis. Considering M_{1L}^{+} is a 1.1V transistor, the range of V_{refn} could be calculated as Eq 4.5.3 if V_{bin}^{+} =1V. Similarly, the range of V_{refp1} could be estimated around (1,1.3)V. Based on the derived output impedance and operating points, we can size the original

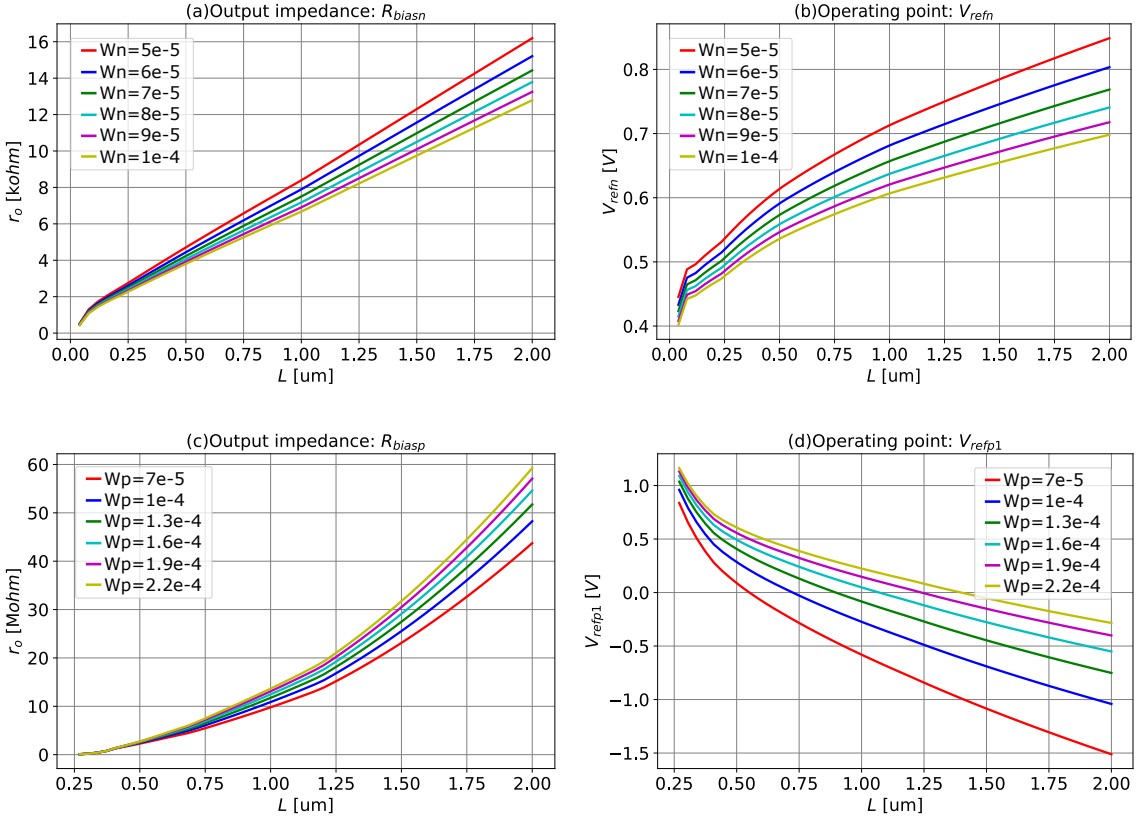


Figure 4.25: Sweep width and length of M_{bn}, M_{bp1} and M_{bp2} (the size of M_{bp1} and M_{bp2} are equal) to choose proper operating points and output impedance. A feasible solution is found at $W_{Mbp1,Mbp2} = 175\mu m$, $L_{Mbp1,Mbp2} = 270nm$, $W_{Mbn} = 50\mu m$, and $L_{Mbn} = 800nm$.

current source, which has NMOS at the bottom, and cascoded PMOS at the top, to meet the specifications. The original current source is shown in Fig 4.23(a). Fig 4.25 helps to select the proper size of biasing. Setting $W_{Mbp1,Mbp2} = 175\mu m$, $L_{Mbp1,Mbp2} = 270nm$, $W_{Mbn} = 50\mu m$, and $L_{Mbn} = 800nm$, we get $V_{refn} = 678mV$, $V_{refp1} = 1.11V$, $R_{biasn} = 7k\Omega$, and $R_{biasp} = 1.5M\Omega$. Extra noise is mainly contributed by M_{1bp2}^{+} since it is the top current biasing of the first stage. The noise excess factor (NEF) could be estimated by Eq 4.5.4 considering M_{1bp2}^{+} is in saturation region. Because we also optimized noise in section 4.3[Bandwidth and accuracy] by increasing drain current. A small NEF is acceptable.

$$NEF = 1 + \frac{g_{m,M1bp2}}{g_{m,M1}} \approx 1 + \frac{(W/L)_{M1bp2}}{(W/L)_{M1}} = 1.32 \tag{4.5.4}$$

In addition, we should consider the value of C_{large} in Fig 4.23(a) carefully. Those capacitors should be large enough to avoid corss-talk between the two stages and eliminate influence of the original current source at high frequency. This could be tested by simply

sweeping the value of C_{large} until there is basically no difference of frequency response before and after basing. The value of C_{large} is set to $1pF$ after verification.

Voltage shift and input biasing

Fig 4.23(b), (d) show the implementation of the input biasing and a voltage shift network, respectively. The input biasing provides a DC operating point for the gate of M_{1L}^{+}. Its influence on noise could be neglected if R_{bin} is large enough. The voltage shift provides a voltage difference between the gate of M_{1R}^{+} and the drain of M_{2}^{+} in DC, which establishes a stable biasing for both stages through negative feedback and avoid M_{1R}^{+} working under excessive drain voltage. A large capacitor C_{large} needs to be connected with R_{shift} in parallel to avoid the large noise contributed by R_{shift} propagates to the three tones.

4.6 Summary

As a summary, Fig 4.26 shows all the transistor sizes and the values of added capacitors and resistors of the final TA amplifier.

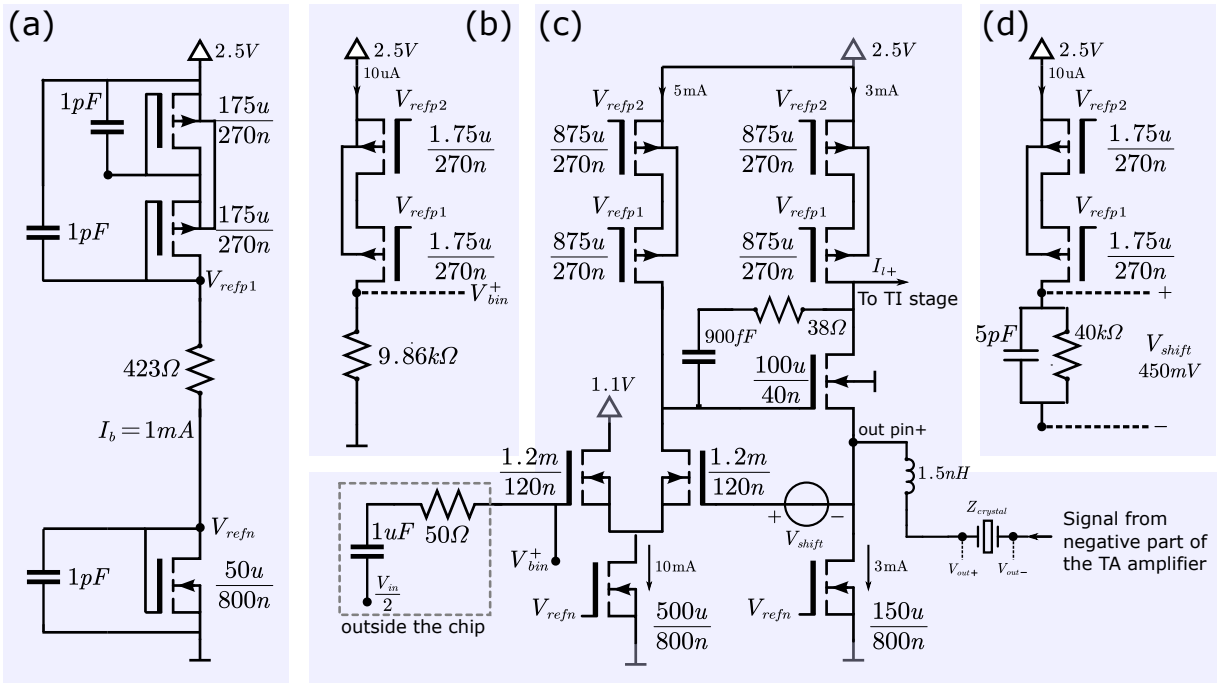


Figure 4.26: (a) The original current source which has $I_b = 1mA$. (b) The input biasing. (c) The biased single-ended TA amplifier. The negative part of the TA amplifier, which has the same structure, is not shown. One branch of the input stage is shorted to V_{DD} due to biasing limit. This would result in a bit less DC loop gain. (d) A voltage shift provides stable biasing through negative feedback.

Table 4.8 shows a summary of the specifications after the design of the TA amplifier. The final results generated from Cadence, which highly match the analysis in SLICAP, are presented in the following topics.

Stage	Specifications	The basetone	The 3rd overtone	The 5th overtone
TA	Drive capability [mA]	$\geqslant$0.8(a)		
	DC loop gain L_{DC}	1.0	5.0	8.2
	Effective Bandwidth @ resonance [Hz]	$315M$	$1.7G$	$1.7G$
	Output-referred noise $[A^2/HZ]$	3.2×10^{-21}	2.4×10^{-21}	1.2×10^{-21}
	Output floor noise $[A^2/HZ]$	1.5×10^{-21}		
	Frequency error @ -40 to 100 °C [ppb]	1.25	6	210
	Phase margin [deg]	48.38		
	Chip area $[m^2]$	9.826×10^{-9} (c)		
	Power consumption $[mW]$	53.5		

Table 4.8: Specifications of the transadmittance stage after design (a) The drive capability should be at least larger than the signal current. The maximum signal current is set by the total RMS value of the three tones. (c) The capacitor of the voltage shift network in Fig 4.26(d) occupies $4.884 \times 10^{-9} m^2$ area, which is almost half of the total area.

Noise

Fig 4.27 shows the total output-referred noise of the TA amplifier over the frequency range of interest. At the resonance frequency, the noise of the base tone and the third overtone is lower than the required value (5.32×10^{-29} and 1.18×10^{-20} $[A^2/HZ]$, respectively). However, the noise of the fifth overtone is around 3 times than the required value (4.6×10^{-22} $[A^2/HZ]$) due to the excessive noise floor. In order to suppress the output-referred noise floor of the TA stage, g_m of the biasing sources $M^+_{2bn}, M^+_{2bp1}, M^+_{2bp2}$ in Fig 4.23 need to be decreased.

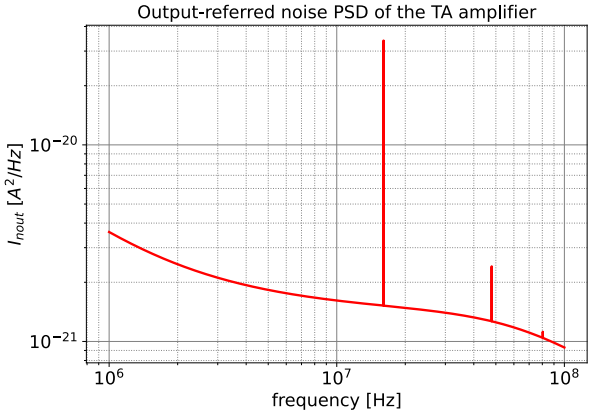


Figure 4.27: Output-referred noise PSD of the TA amplifier.

Bandwidth and stability

Fig. 4.28 shows the gain plot of the TA amplifier for the base tone ($R_n = 6.14\Omega$), the third overtone ($R_n = 52.3\Omega$), the fifth overtone ($R_n = 308.1\Omega$), and the capacitive crystal ($C_0 =$

$1.65pF, R_n = \infty$). It is important to notice that the gain of the TA amplifier is defined as (V_{in+}, V_{in-}) to (V_{o+}, V_{o-}) in Fig 3.12 because the phase shift (V_{o+}, V_{o-}) to $I_{crystal}$ caused by crystal should not be considered.

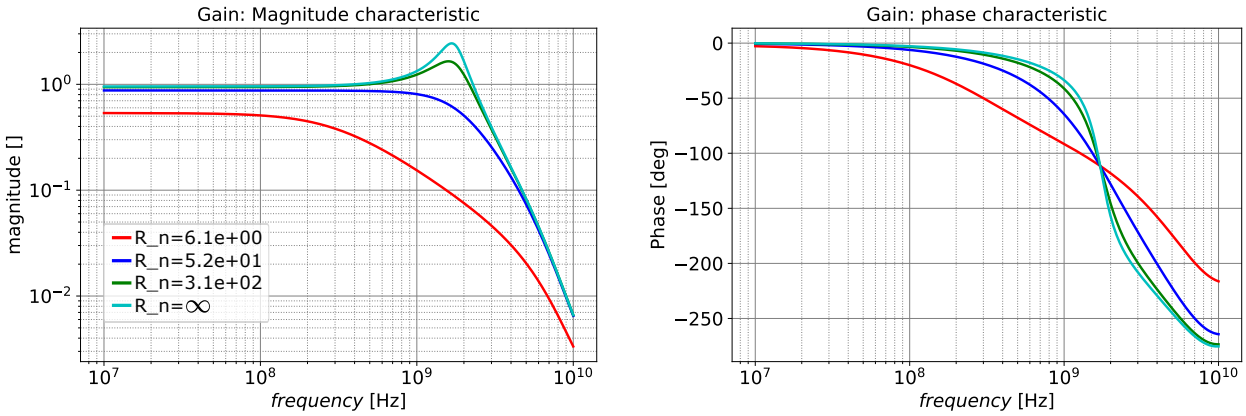


Figure 4.28: Gain plot of the TA amplifier. The equivalent bandwidth of the base tone is 315MHz. The equivalent bandwidth of the third overtone and fifth overtone is around 1.7GHz.

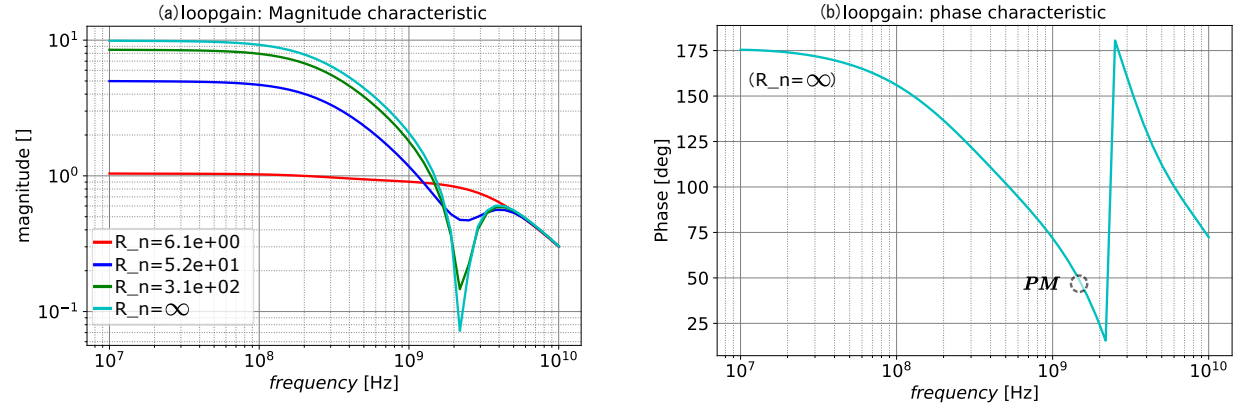


Figure 4.29: loop gain plot of the TA amplifier. The DC loop gain for the three tones is larger than unity. $R_n = \infty$ stands for high frequency response of crystal. The phase margin is 48.38 deg at 1.58 GHz.

Fig. 4.29(a) shows the loop-gain magnitude plot for the three tones and the pure capacitive crystal. The DC loop gain for the three tones is larger than unity. Fig 4.29(b) shows the loop-gain phase plot for the pure capacitive crystal since it decides the stability of the TA amplifier in high frequency. The low phase margin is due to the phantom zero caused by bondwire L_w and shunt capacitor C_o of crystal. In order to enhance the stability, the inductance of bondwire need to be reduced.

Frequency error

Fig 4.30 shows magnitude and phase plot of transfer function (V_{in+}, V_{in-}) to (V_{o+}, V_{o-}) and (V_{in+}, V_{in-}) to $I_{crystal}$ for the three tones with the tested crystal as the feedback. The frequency error, which is calculated as $\triangle f/f_r$, could be obtained from Fig 4.30(b),(d),(f). The frequency error of the base tone and the third overtone is within requirement but becomes excessive large for the fifth overtone.

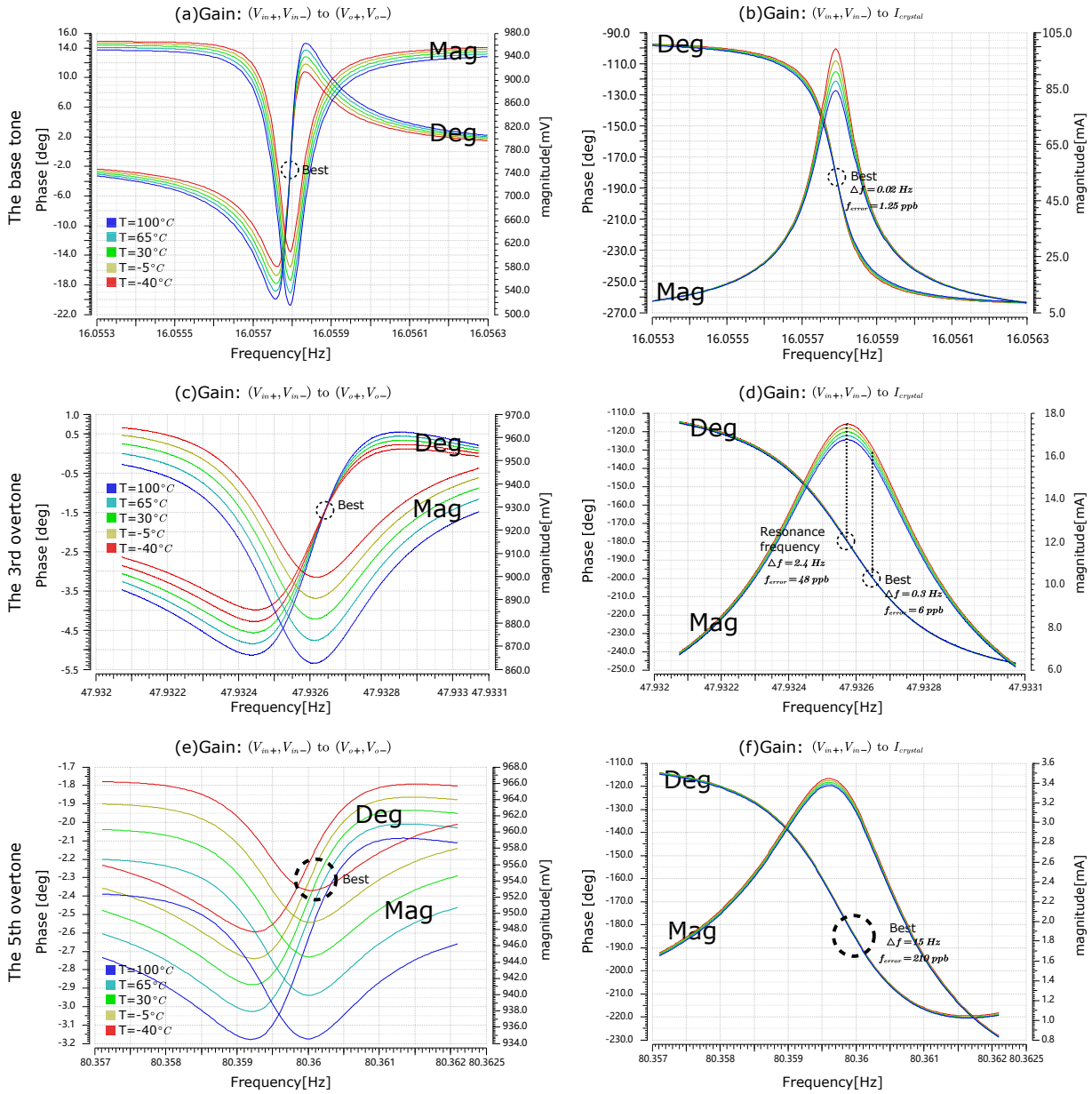


Figure 4.30: Magnitude and phase plot of transfer function (V_{in+}, V_{in-}) to (V_{o+}, V_{o-}) and (V_{o+}, V_{o-}) to $I_{crystal}$.(a)(b) For the base tone, the best performance is at the resonance frequency. (c)(d) For the third overtone, the best performance is not at the resonance frequency. In order to get the best performance, the input frequency should be 80Hz higher than the resonance frequency. This would result in a less CNR for the third overtone. (e)(f) The frequency error for the fifth overtone is much larger than the required value, which is mainly because its quality factor is much lower than that of the base tone and the third overtone.

CHAPTER 5

Design of the transimpedance stage

In this chapter, we will present a design overview of the transimpedance stage. The concept diagram of the TI stage is shown in Fig 3.6. Driving differential 50Ω load, the TI stage transfers the current output from the TA stage to the voltage input for the ADC. To avoid the deterioration of frequency error caused by the TI stage, the phase shift ϕ_{TI} of the TI stage should be kept as low as possible as explained in section 3.3.3 [Frequency response]. Table 5.1 summarizes the specifications for the TI stage from section 3.3. Similar to the TA stage, the orthogonal design of the TI stage is divided into 5 parts, which are noise, drive capability, bandwidth, frequency compensation, and biasing.

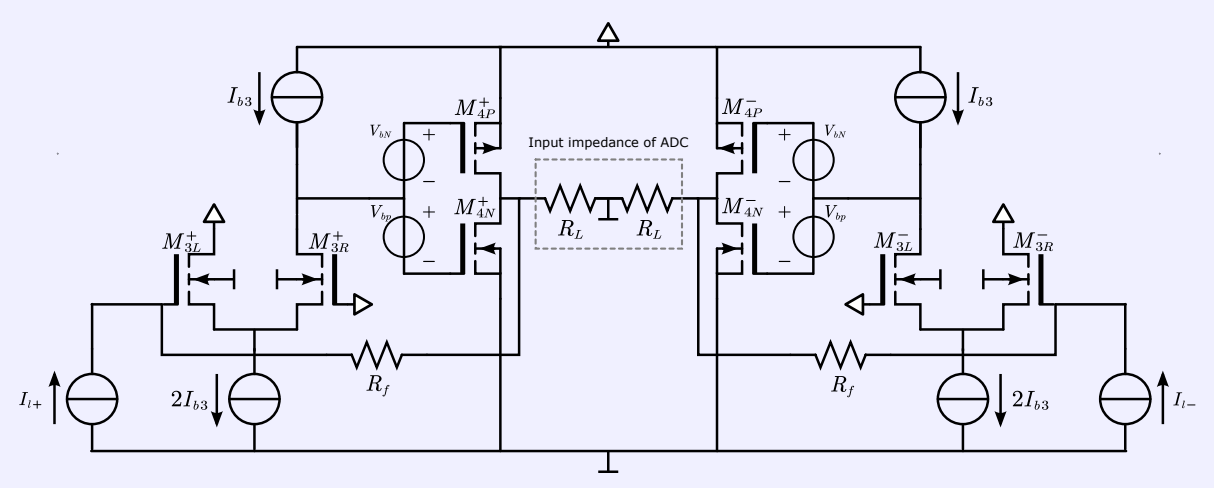


Figure 5.1: Two stage transimpedance amplifier with a DFCS+CPCS controller. The biasing diagram and components for compensation are not complete.

Figure 5.1 shows the a design overview of the two-stage transimpedance amplifier with a DFCS input, a CPCS (Complementary Parallel Common-Source) output, and resistive feedback. The DFCS input mainly decides the noise performance of the TI stage. To drive a large signal current with low power consumption, the CPCS stage, known as a class AB stage, is applied as the output stage of the TI amplifier.

Stage	Specifications	Values
TI	Drive capability [mA]	$\geqslant 12.8$ with 50Ω load (a)
	Gain $A_v = 2R_f$	2×400
	Bandwidth[GHz]	$\geqslant 2.27$
	Output-referred noise $[\mathrm{V}^2/\mathrm{Hz}]$	$(0, 2.08 \times 10^{-16})$
	S_{v2} $[\mathrm{V}^2/\mathrm{Hz}]$	$(0, 1.04 \times 10^{-16})$
	S_{i2} $[\mathrm{A}^2/\mathrm{Hz}]$	$(0, 6.5 \times 10^{-22})$

Table 5.1: Specifications of the transimpedance stage. (a) The maximum signal current driving differential 50Ω load is set by the total RMS value of the three tones according to Tab 3.3.

5.1 Noise and drive capability

Using the same sizing strategy as explained in section 4.1 [Noise optimization], the initial width, length, and drain current of the input stage is set to $W_3 = 200\mu m$, $L_3 = 40nm$, $I_D = 0.5mA$. If sizing requirements of drive capability is compatible with that of noise. one-stage design is feasible.

In order to drive a large signal current with low power consumption, a CPCS stage is applied as the output stage. The CPCS stage is a parallel connection of a biased PMOS CS stage and a biased NMOS CS stage. To handle single-ended $18.2mA$ peak-to-peak current, both NMOS and PMOS should be able to handle $9.1mA$ peak current (or $450mV$ peak voltage). It is better not to use $40nm$ transistor because its low power supply limit($1.1V$) may cause sever damage to the transistors. Fig 5.2(A),(B) shows the test-bench for the NMOS and PMOS stage, respectively. Since we want to fix the operating voltage and current at

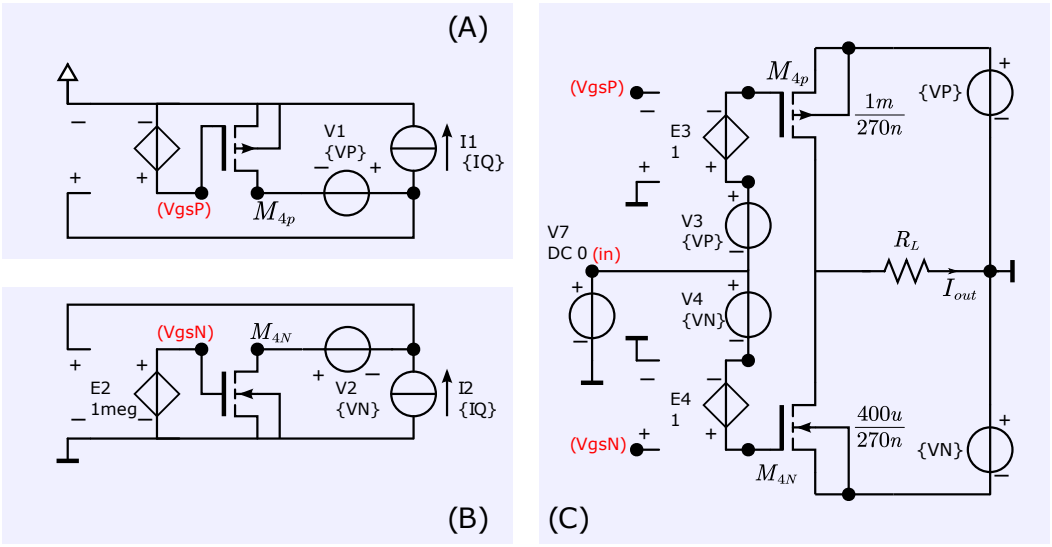


Figure 5.2: Cadence test bench for determination of the operating voltage-to-current transfer of the CPCS stage. (A) Circuit for determination of V_{GSQ} of the PMOS. (B) Circuit for determination of V_{GSQ} of the NMOS. (C) Biased CPCS stage. Source[18],edited.

the output port of an amplifier stage, we need to determine the input bias voltage V_{GSQ}

for fixing I_{DSQ} at a given value of V_{DSQ}. The width of the PMOS has been taken 2.5 times larger than that of the NMOS because the zero field mobility of electrons is larger than the mobility of holes. Using the same strategy as explained in section 4.2[Drive capabilities], the width and length of NMOS and PMOS are set to $W_{4N} = 400\mu m$, $W_{4P} = 1mm$ and $L_{4N} = L_{4P} = 270nm$.

Fig 5.2(C) shows the biased CPCS stage driving $R_L = 50\Omega$. The output current is the sum of the drain currents and the common-mode current is half the difference between the two currents. Fig 5.3 shows the differential-mode output current and the common-mode current both as a function of the input voltage. At zero input signal, the common-mode current equals the quiescent operating current. The CPCS stage is capable of delivering a differential output current much larger than its quiescent current. To avoid cross-over distortion, I_Q should be higher than $2mA$. In addition, I_Q decides f_T of the output stage, which is important for bandwidth design. Calculating the DC operating points in Fig 5.2 for a given I_Q, we can derive the voltage difference between the gate of PMOS and NMOS and implement biasing later. We first assume $I_Q = 4mA$ to meet drive capability while keeping a low non-linearity.

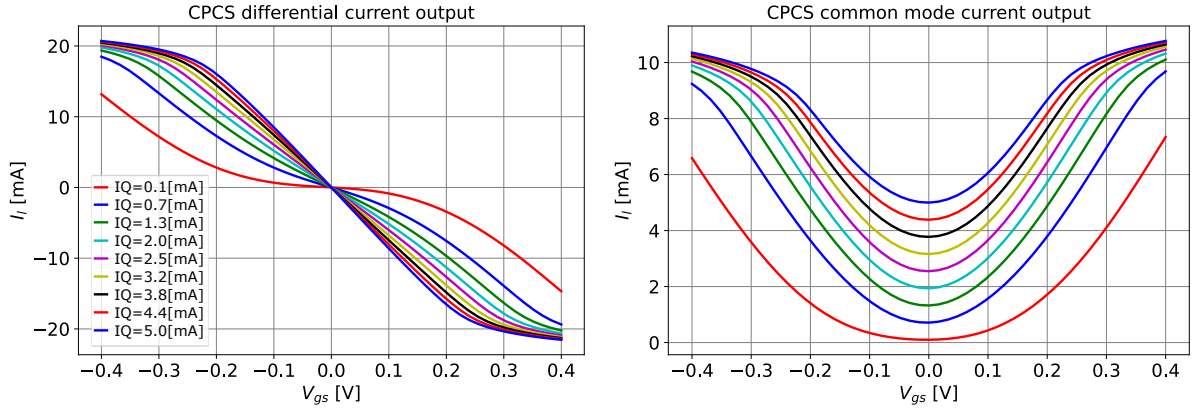


Figure 5.3: Characteristics of the CPCS stage, operating from weak inversion to strong inversion. Left: Output current versus differential input voltage. Its drive capability is much higher than the required value ($18.2mA$ peak-to-peak). Right: Common-mode current versus differential input voltage.

Fig 5.4(A) shows the one-stage TI amplifier design solution with resistive feedback and the CPCS stage as a controller. Fig 5.5(A) shows its small-signal diagram (single-ended) with dominant parasitic capacitors. Fig 5.4(C) indicates its input-referred noise PSD is compatible with noise specification. However, its low loop gain/servo shown in Fig 5.4(B) causes an insufficient gain. Therefore, the one-stage solution is not suitable for the TI stage. Table 5.2 summarizes the initial poles/zero according to Fig 5.5(A).

5.2 Bandwidth design

Fig 5.5(B) shows the small-signal diagram (single-ended) of Fig 5.1, which is a two-stage TI amplifier, with dominant parasitic capacitors. The width, length, and drain current of the input stage is set to $W_3 = 370\mu m$, $L_3 = 40nm$, $I_D = 3mA$ to increase its f_T. Table 5.3 updates poles/zero.

Pole/Zero	Status	Hand Calculation/ Explanation		SLICAP
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	new	$\frac{-1}{2\pi\left(R_f+R_L\right)C_{gs}}$	$\frac{-1}{2\pi\cdot 450\cdot 1.3p} = -2.72M$	$-2.37M$
Load pole P_2 [Hz]	new	$\frac{-1}{2\pi\left(R_f\|\|R_L\right)C_{db4}}$	$\frac{-1}{2\pi\cdot 44\cdot 0.4p} = -9.05G$	$-9.44G$
Feedback Zero Z_1 [Hz]	new	$\frac{-1}{2\pi R_f C_{gd4}}$	$\frac{-1}{2\pi\cdot 400\cdot 1f} = -398G$	$-392G$

Table 5.2: Loop gain pole-zero tracking of the one-stage TI amplifier with a CPCS controller. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero.

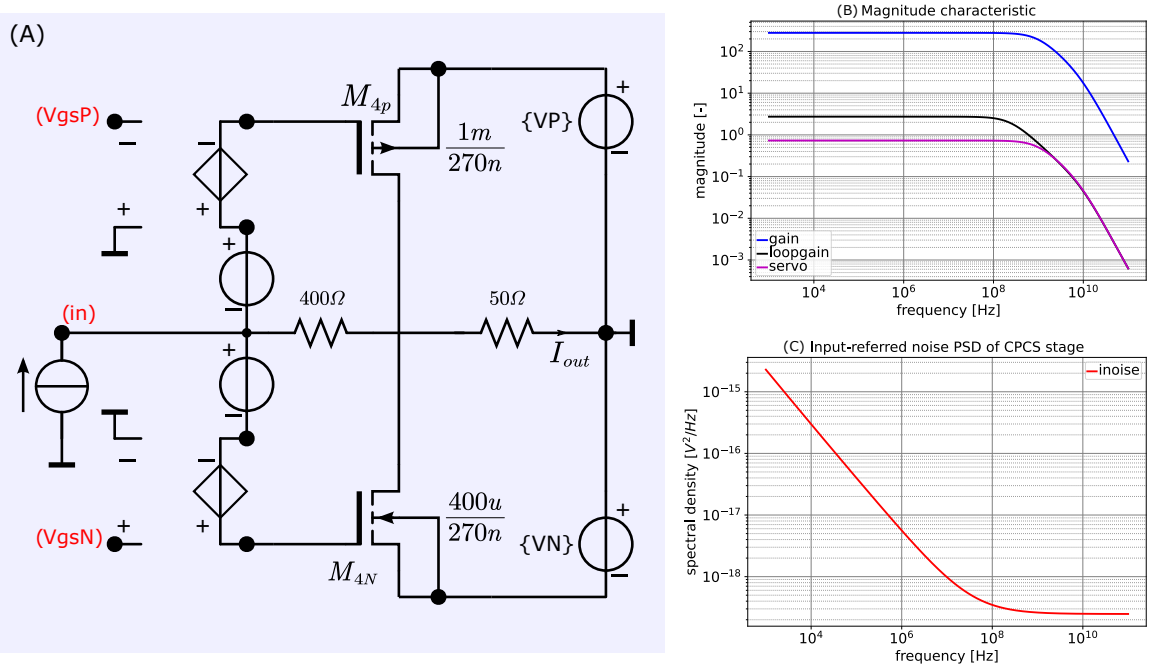


Figure 5.4: (A)Cadence/SLICAP Test-bench of one-stage TI stage. (B) Low loop gain/servo causes gain is much lower than 400. (C) Intrinsic input-referred noise of the CPCS stage is tested by setting $R_f = \infty$ since we already decoupled noise contribution of R_f in the former analysis. In the frequency range of interest, $S_{v2} < 1.04 \times 10^{-16}\ \left[\mathrm{V^2/Hz}\right]$.

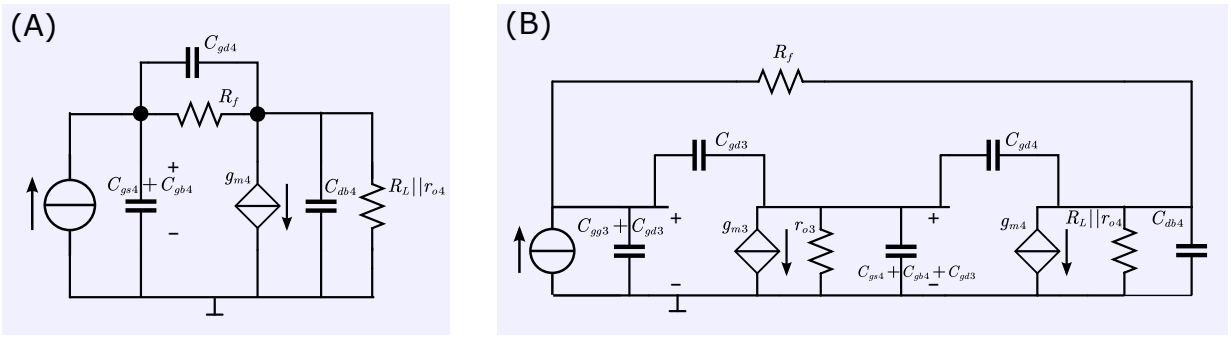


Figure 5.5: Single-ended small-signal diagram of the TI amplifier. (A)One-stage TI amplifier with a CPCS controller. (B)Two-stage TI amplifier with a DFCS+CPCS controller.

Pole/Zero	Status	Hand Calculation/ Explanation		SLICAP
		Symbolic	Numeric	
Feedback pole P_1 [Hz]	modified	$\frac{-1}{2\pi\left(R_f+R_L\right)\left(C_{gd3}+C_{gg3}\right)}$	$\frac{-1}{2\pi\cdot 450\cdot(44+55)f}=-3.57G$	$-3.3G$
Load pole P_2 [Hz]	modified	$\frac{-1}{2\pi\left(R_f\|\|R_L\right)C_{db4}}$	$\frac{-1}{2\pi\cdot 44\cdot 0.38p}=-9.5G$	$-10.0G$
Intermediate pole P_3 [Hz]	new	$\frac{-1}{2\pi r_{o3}\left(C_{gs4}+C_{gd3}+C_{gb4}\right)}$	$\frac{-1}{2\pi\cdot 200\cdot(1.3+0.16)p}=-545M$	$-514M$
Source Zero Z_1 [Hz]	modified	-	-	$-1392G$

Table 5.3: Loop gain pole-zero tracking of the two-stage TI amplifier with a DFCS+CPCS controller. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero.

Assuming the transadmittance stage has infinite output impedance, its DC loop gain, LP product, DC gain could be calculated as:

$$L_{DC}=\frac{-g_{m3}r_{o3}g_{m4}}{\left(\frac{1}{R_L}+\frac{1}{r_{o4}}\right)}=\frac{-23m\cdot 200\cdot 85m}{\left(\frac{1}{50}+0.24m\right)}=-19.6 \tag{5.2.1}$$

$$Gain_{DC}=\frac{-L_{DC}}{1-L_{DC}}R_f=\frac{19.6}{20.6}\cdot 400=380.583 \tag{5.2.2}$$

$$BW=LP_2=\sqrt{(1-L_{DC})\cdot P_1\cdot P_3}\approx\sqrt{\frac{f_{T3}f_{T4}}{\left(\frac{1}{R_L}+\frac{1}{r_{o4}}\right)}\frac{1}{(R_f+R_L)}}=5.7\,[\text{GHz}] \tag{5.2.3}$$

The first stage rises the order of the system and contributes its f_T to the overall bandwidth. To enhance the overall bandwidth, we can increase f_T in both stages. Because the first stage and the second stage are both in weak inversion, their f_T could effectively increase by a higher drain current. The effective DC gain is lower than 400 due to the finite loop gain. We can simply increase R_f to 420 and acquire the target gain, with a slight decrease of bandwidth.

Fig 5.6 shows the transfer functions of the asymptotic gain model for the two-stage TI amplifier with $R_f=420$. In order to eliminate undesired frequency response at the frequency of bandwidth limitation, we will discuss the application of frequency compensation in the next topic.

5.3 Frequency compensation

Fig 5.7 shows the two-stage TI amplifier after implementation of phantom zero technique. A capacitor C_{phz} connected in parallel with the feedback resistor R_f, to create a zero in the loop-gain, coinciding with a pole in the ideal gain. To eliminate the undesired damping around $5GHz$, its value could be approximated by:

$$C_{phz}=\frac{1}{2\pi R_f\cdot BW}=\frac{1}{2\pi\cdot 420\cdot 5\times 10^9}=7.57881\times 10^{-14}\ \ [\text{F}] \tag{5.3.1}$$

Fig 5.8(A) shows the root locus after implementation of C_{phz}. With the increase of C_{phz}, quality factor of the dominant poles gradually decrease and the system becomes an third

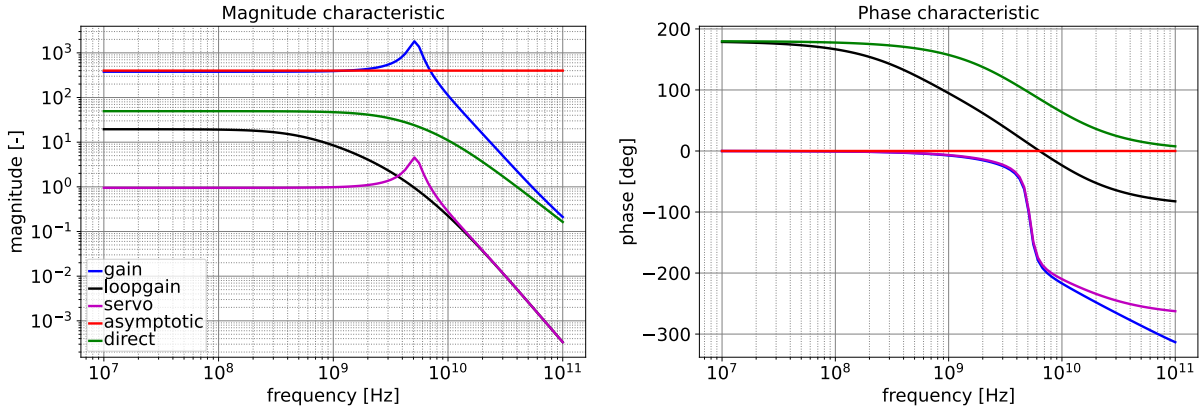


Figure 5.6: Transfer functions of the asymptotic gain model for the two-stage TI amplifier. The servo function indicates the bandwidth of the amplifier and gain error in the frequency range of interest. Generally, the direct transfer is much less than the gain, which does not interfere with the result.

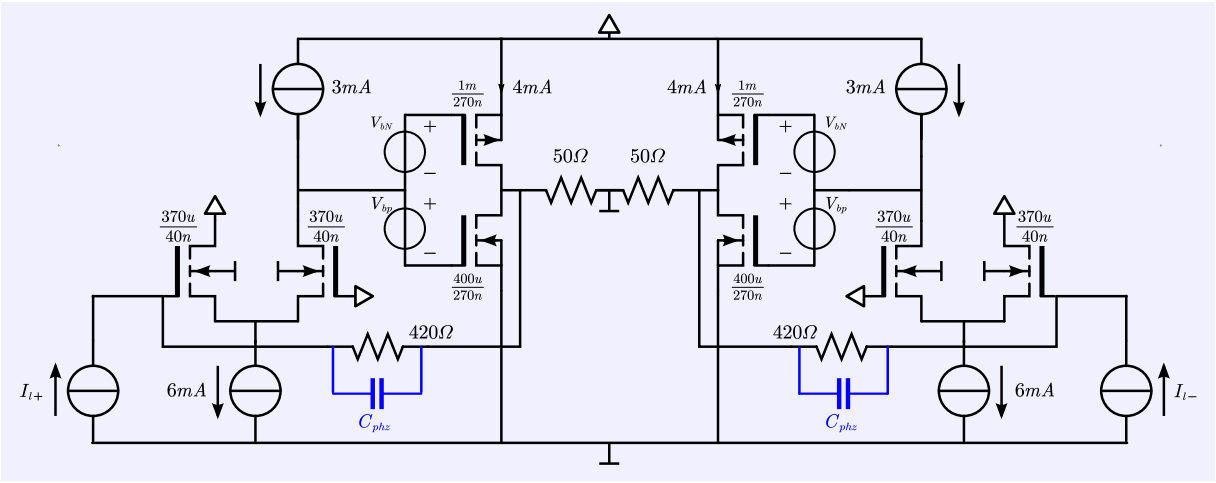


Figure 5.7: Two stage transimpedance amplifier after implementation of phantom zero. The phantom zero is created by inserting a capacitor C_{phz} in parallel with the feedback resistor.

order MFM system when $C_{phz} = 100fF$. The inserted phantom zero not only improves the stability of the system but also corrects the overshot at the frequency of bandwidth limitation. Fig 5.8(B) shows the magnitude transfer of the asymptotic gain model when $C_{phz} = 100fF$. Table 5.4 shows the pole-zero tracking that indicates the poles and zeros that have been modified or introduced due to the phantom zero compensation.

5.4 Biasing and summary

Fig 5.9 shows the single-ended transimpedance amplifier with all transistors sized and values of resistors and capacitors. The current biasing sources are based on the original current source designed in Fig 5.9(a), which does not affect the gain and noise performance of the TI stage. The biasing schematic for the CPCS stage in Fig 5.9(C) is a series connection of two voltage shifts. Section 4.5[Implementation of biasing] explains its design principle.

The final simulation results generated from Cadence, which highly match the analysis

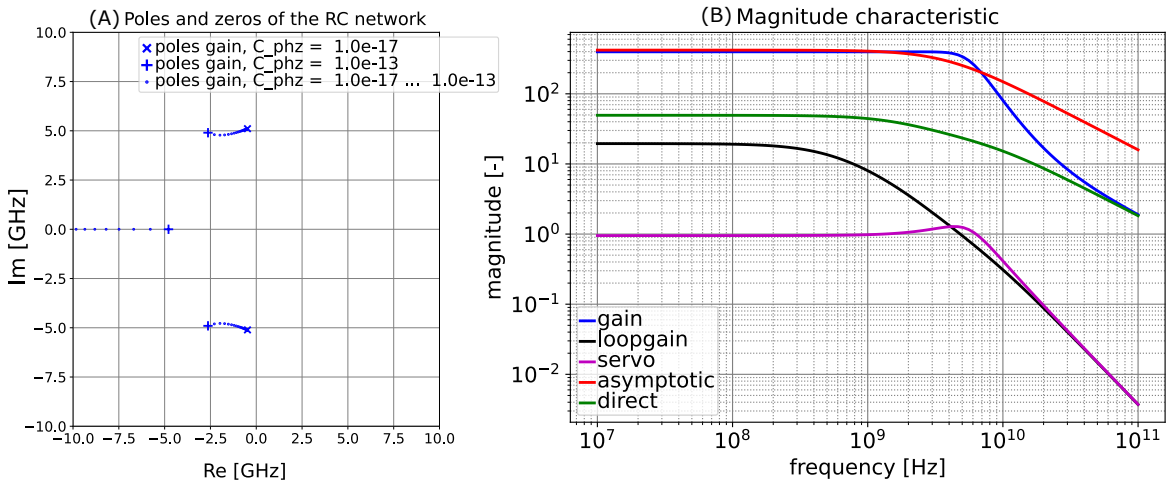


Figure 5.8: (A) Positions of poles vary with the value of C_{phz}. The system gradually becomes a third order MFM system. (B) Magnitude characteristic after the implementation of the phantom zero.

Pole/Zero	**Status**	**Hand Calculation/ Explanation**		**SLICAP**
		Symbolic	**Numeric**	
Feedback pole P_1 [Hz]	modified	Decrease due to the phantom zero (a)		$-1.8G$
Load pole P_2 [Hz]	modified			$-7.2G$
Intermediate pole P_3 [Hz]	Unchanged	$\frac{-1}{2\pi r_{o3}\left(C_{gs4}+C_{gd3}+C_{gb4}\right)}$	$\frac{-1}{2\pi\cdot 200\cdot(1.3+0.16)p} = -545M$	$-514M$
Source Zero Z_1 [Hz]	Unchanged	-	-	$-1392G$
Phantom zero Z_2 [Hz]	new	$\frac{-1}{2\pi R_f C_{phz}}$	$\frac{-1}{2\pi\cdot 420\cdot 100f} = -3.79G$	$-3.79G$

Table 5.4: Loop gain pole-zero tracking of the two-stage TI amplifier after phantom zero compensation. The status indicates the situation(new, modified, or unmodified) of the pole/zero in respect to the previous step. The hand calculation provides symbolic explanations and numeric results for each pole/zero. (a) It is hard to estimate the modified positions of P_1 and P_2 because the value of C_{phz} is very close to the capacitance C_{gg3} and C_{gd3} of the first stage, which makes the first order estimation not accurate.

in SLICAP, are presented as follows:

Noise and bandwidth

Fig 5.10 shows the Output-referred noise and the gain magnitude of the TI amplifier, respectively. In the frequency range of interest, its PSD is lower than the quantization noise caused by ADC (2.08×10^{-16} [V^2/Hz]). The bandwidth of the TI stage is around $3.5GHz$, which is higher than the bandwidth of the TA stage.

Stability

Fig 5.11 shows the loop-gain plot of the TI amplifier. After compensation, the phase margin is enhanced by phantom zero.

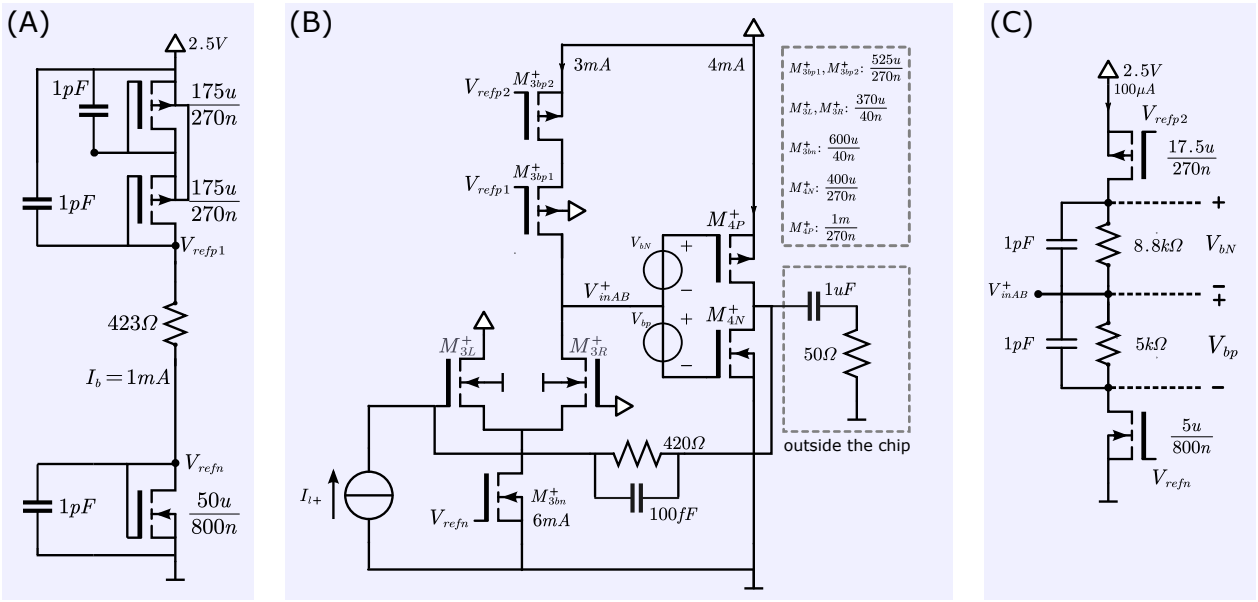


Figure 5.9: (A)The original current source. (B)The biased Single-ended TI amplifier. The negative part of the TI amplifier, which has the same structure, is not shown. (C)The biasing schematic for the CPCS stage.

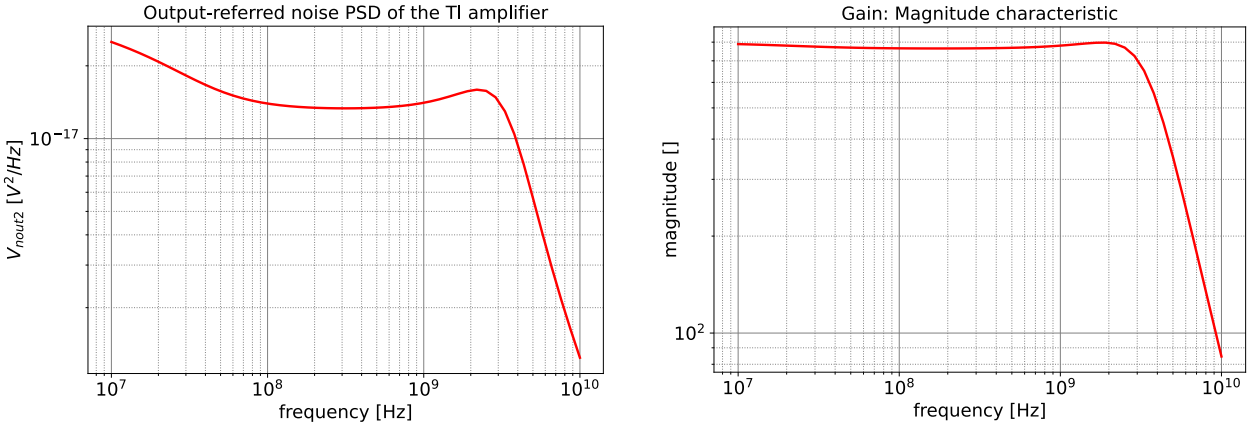


Figure 5.10: Left: Output-referred noise PSD of the TI amplifier. Right: Gain plot(magnitude) of the TI amplifier.

Phase/Frequency error

Fig 5.12 shows the phase plot of the TI amplifier varying with temperature. If the TI stage is connected after the TA stage, the phase error caused by the TI stage in the temperature range from -40 to 100°C, could be transformed to frequency error by Eq 2.1.13. As an estimation, the TI stage result 1.6, 3.4, and 10 ppb frequency error for the base tone, the third overtone, and the fifth overtone, respectively. Table 5.5 summarizes the specifications after the design of the TI amplifier.

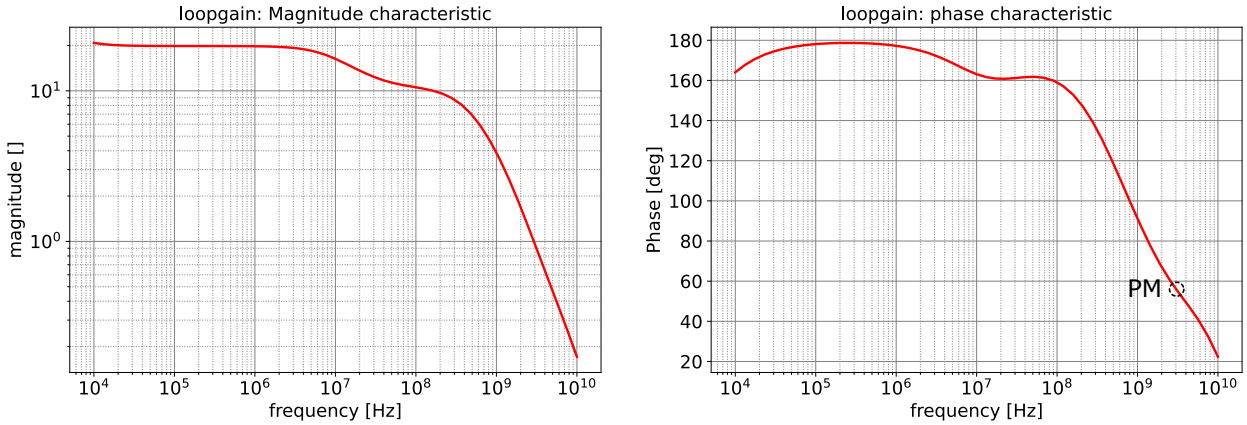


Figure 5.11: loop gain plot of the TI amplifier. The phase margin is 55.38 deg at 2 GHz.

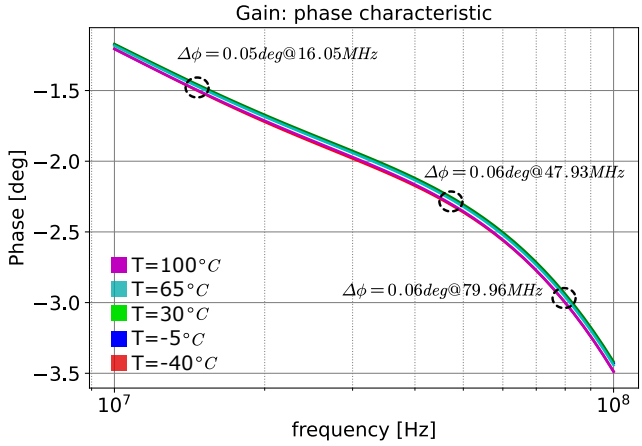


Figure 5.12: Phase error at three resonance frequencies of the TI amplifier. According to Eq 2.1.13, the TI stage result 1.6, 3.4, and 10 ppb frequency error for the base tone, the third overtone, and the fifth overtone, respectively.

Stage	Specifications	Values
TI	Drive capability [mA]	$\geqslant 12.8$ with 50Ω load
	Gain L_{DC}	795
	Bandwidth [GHz]	3.51
	Output-referred noise $[V^2/Hz]$	$< 3 \times 10^{-17}$
	Phase margin [deg]	55.38
	Chip area $[m^2]$	7.70×10^{-9}
	Frequency error @ -40 to 100 °C [ppb]	[1.6, 3.4, 10](a)
	Power consumption $[mW]$	42.1

Table 5.5: Specifications of the transimpedance stage after design. (a) The estimated frequency error contributed by the TI amplifier for the base tone, the third overtone, and the fifth overtone, respectively.

CHAPTER 6

Integration of two stages

After the design of transadmittance stage and the transimpedance stage, we will discuss the integration of the two stages in this chapter. Ideally, the frequency characteristic of the TA stage reflects that of the crystal by a current output. The TI stage behaves like a buffer, which makes the output of the TA stage observable to the ADC. Fig 6.1 shows the single-ended circuity of TA+TI amplifier. It is important to know that the design of the TA stage is without accounting for input impedance of the TI stage. Similarly, the design of the TI stage is without accounting for the output impedance of the TA stage. These assumptions are reasonable due to the functions of feedback. However, slight mismatches before and after the integration are inevitable. The final results are verified by Cadence simulations, which highly match the analysis of SLICAP.

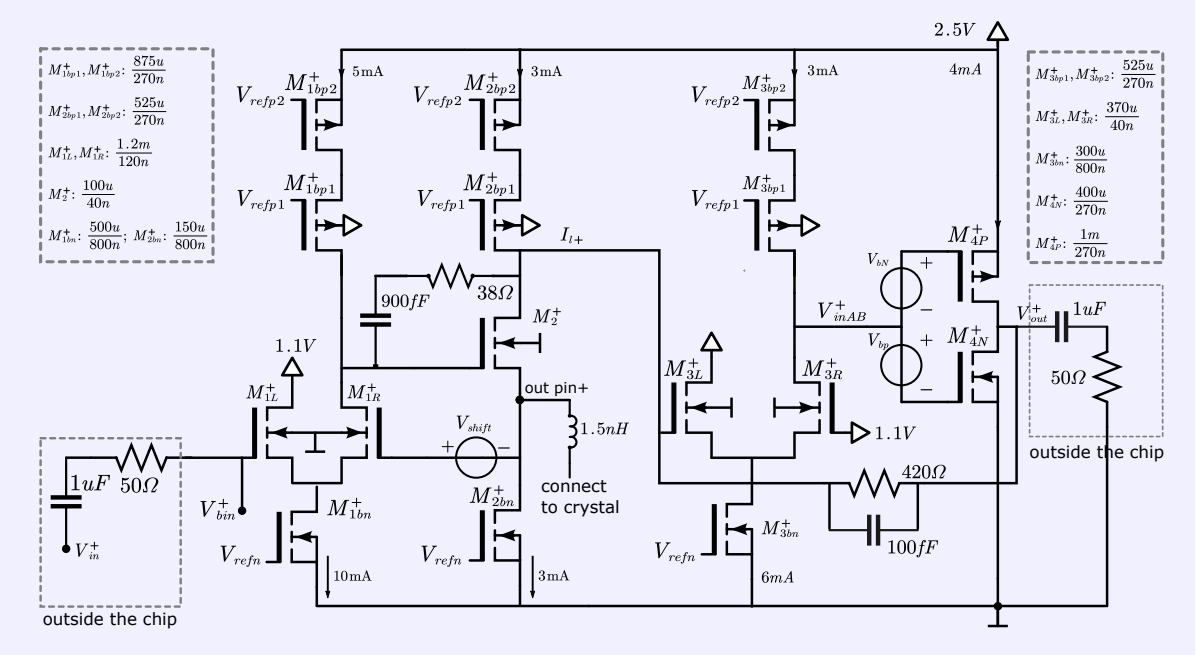


Figure 6.1: The single-ended TA+TI amplifier with all transistors labeled and sized. The biasing implementation of voltage shift networks is presented in Fig 5.9 and 4.26

6.1 Pre-layout

In this section, the results of the pre-layout simulations of the overall system are presented. The following topics highlight the results related to the system specifications.

Frequency response

There are no requirements on the bandwidth. However, the requirements of frequency error could be transformed to that of equivalent bandwidth of the three tones as explained in section 3.3[Frequency response]. Therefore, the equivalent bandwidth should be as large as possible to get a better frequency error. Fig 6.2(B) shows the equivalent bandwidth of the three tones by substituting the crystal with R_n. Fig 6.2(A) shows the AC gain of the whole amplifier from source to load. Around the three resonance frequencies, the gain in Fig 6.2(A) and (B) are exactly equal.

However, the overall bandwidth decreases compared with the results obtained from section 4.6 and 5.4 due to the interaction between the TA and the TI stage is not ideal as we assumed in the former analysis. For example, the input/output impedance of the TI/TA stage may lower the LP product of the TA/TI stage, which can be seen in Fig 6.3(A). Since we have concluded the strategies to enhance the bandwidth for both stages, we think this error is controllable and does not disobey the orthogonal design. If the frequency error is within requirement, there is no need to enhance bandwidth by the trade-off of other parameters.

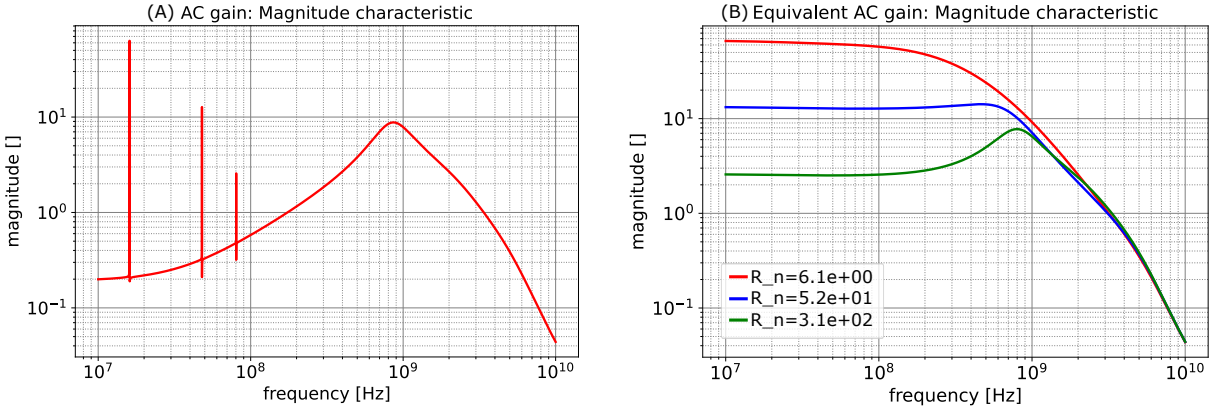


Figure 6.2: (A)The AC gain of the whole amplifier from source to load. At the three resonance frequencies, the ideal gain equals $2R_f/R_n$. (B)The equivalent frequency response of the three tones by substituting the crystal with R_n.

The stability of the overall system could be observed by loop-gain of the TA and the TI stage as shown in Fig 6.3. In addition, table 6.1 shows the phase/gain margin of the system under five typical design corners. Even in the worst case (FS and SF), both TA and TI stages are stable.

Input and output

According to table 3.3, the input RMS voltages are $[2, 16.4, 46.4]\,mV$, with corresponding output RMS voltages $[260.6, 250.0, 119.6]\,mV$ for the base tone, the third overtone, and the

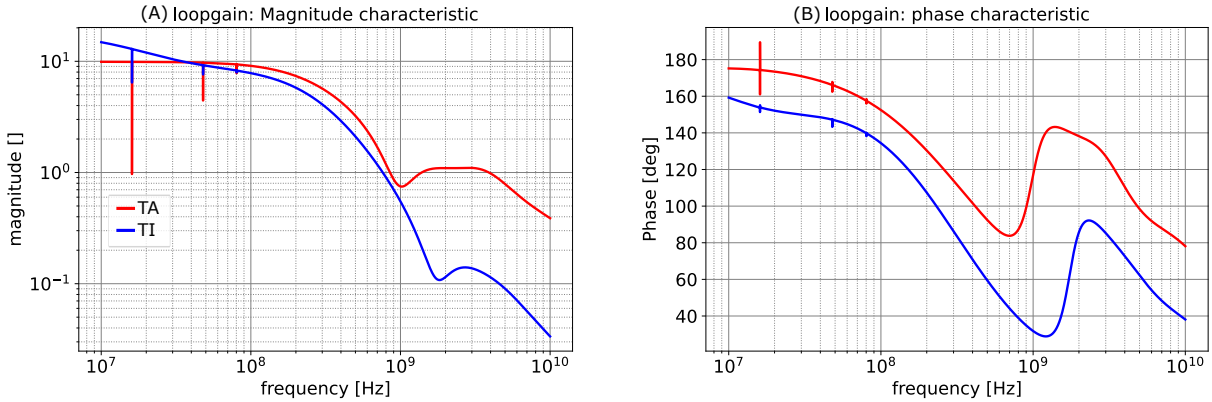


Figure 6.3: Loop-gain magnitude and phase of the TA and TI stage.

Corner		TT	FF	SS	SF	FS
TA	Gain margin [dB]	25.7@ 52.4GHz	24.5@ 53.61GHz	26.61@ 59.9GHz	25.56@ 57.5GHz	25.67@ 55.4GHz
	Phase margin [Deg]	92.08@ 850.6MHz	86.92@ 864.1MHz	114.3@ 3.64GHz	89.5@ 853.5MHz	94.87@ 853.1MHz
TI	Gain margin [dB]	39.5@ 23.8GHz	39.8@ 32.44GHz	39.9@ 13.1GHz	39.0@ 23.26GHz	39.9@ 24.5GHz
	Phase margin [Deg]	40.77@ 761.6MHz	42.1@ 830.6MHz	53.37@ 534.2MHz	37.39@ 782.9MHz	44.82@ 742.3MHz

Table 6.1: Cadence simulations: Gain and phase margin of the TA and the TI stage under typical corners.

fifth overtone, respectively. The gain from input to output is given by $2R_f/R_n$. As explained in section 4.2 and 5.1[Drive capability], both TA and TI amplifier satisfies their output swing with sufficient margin. The distortion caused by non-linearity of the system, which is not a required spec of this project, may propagate to the MMXO system as an offset due to the modulation. Fig 6.4 shows the PSS transient simulations for the third overtone. The distortion occurs when output swing is larger than $3V$. According to the requirements of drive capability, the total output swing of the three tones is around $1.8V$, which would not suffer from serious distortion.

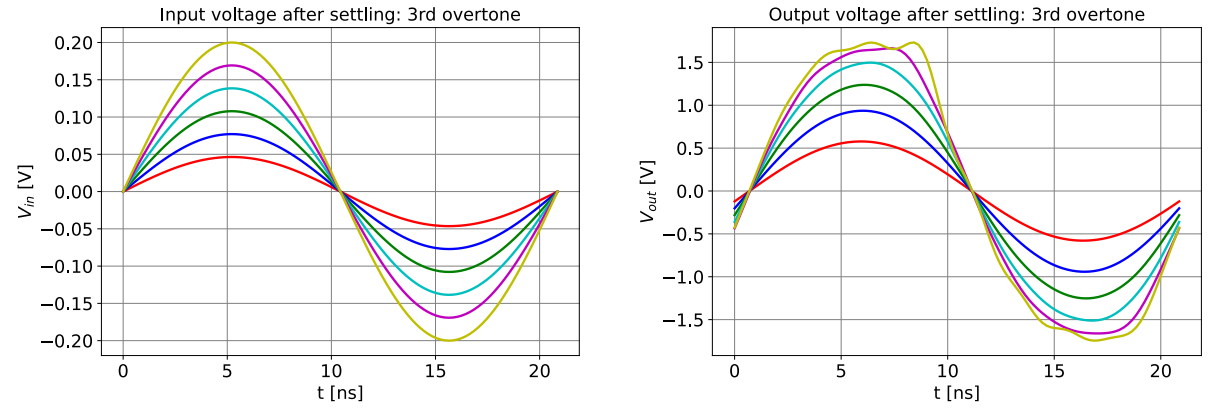


Figure 6.4: The input and output voltage swing when the input signal is the third overtone. PSS simulation is applied to obtain a settled time-domain waveform.

Noise

According to table 3.4, the output-referred noise other than quantization noise should be less than 3.4×10^{-13} and $7.3 \times 10^{-15}\,[\mathrm{V}^2/\mathrm{Hz}]$ at the base tone and the third overtone, respectively. Fig 6.5 shows the final output referred noise PSD. The noise peaking at the base and the third resonance frequency is 4×10^{-14} and $9 \times 10^{-16}\,[\mathrm{V}^2/\mathrm{Hz}]$, respectively. There is almost no noise peaking around the fifth overtone since the output noise floor dominates the noise performance of the fifth overtone, which confirms the analysis in section 3.3[Considerations of noise budgets].

Fig 4.27 shows the output noise floor of the TA stage is above $10^{-21}\,[\mathrm{A}^2/\mathrm{Hz}]$. Ideally, the total output referred noise floor should be above $6.4 \times 10^{-16}\,[\mathrm{V}^2/\mathrm{Hz}]$. However, the final output noise floor in Fig 6.5 is lower than $6.4 \times 10^{-16}\,[\mathrm{V}^2/\mathrm{Hz}]$. This is because the same original current source is applied in the both TA and TI stage. The correlated noise in the two stages generated from biasing sources cancels out to some extent. Therefore, the final output noise would be lower than $10^{-21} \times (2R_f)^2\,[\mathrm{V}^2/\mathrm{Hz}]$

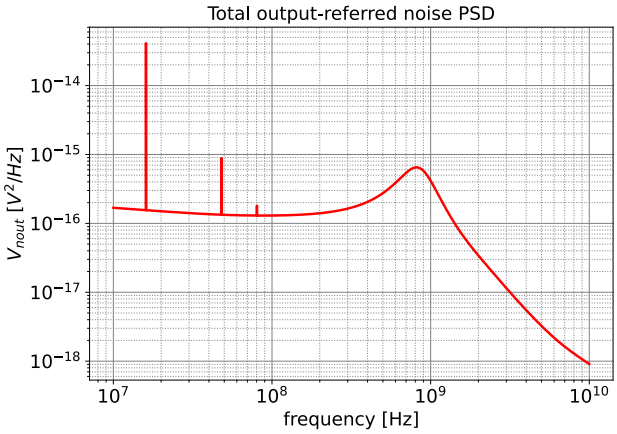


Figure 6.5: Total output-referred noise PSD.

Frequency error

Fig 6.6 shows magnitude and phase plot of transfer function (V_{in+}, V_{in-}) to (V_{out+}, V_{out-}), which reflects the total frequency error over interested temperature range, at the three series resonance frequency. The frequency error of the base tone and the third overtone is within requirement but becomes excessive large for the fifth overtone. Compared with Fig 4.30(b),(d),(f), the frequency error slightly increases after integration of the two amplifiers because of the extra phase shift introduced by the TI stage.

Specifications summary

Table 6.2 summarizes the specifications of the final design. In conclusion, the frequency error of the base tone and the third overtone is close to 10ppb. In order to drive the third overtone with the lowest frequency error, the input frequency should be 80Hz higher than the third resonance frequency. The fifth overtone has a large frequency error around 252ppb due to the high temperature dependent phase shift and low quality factor of the crystal.

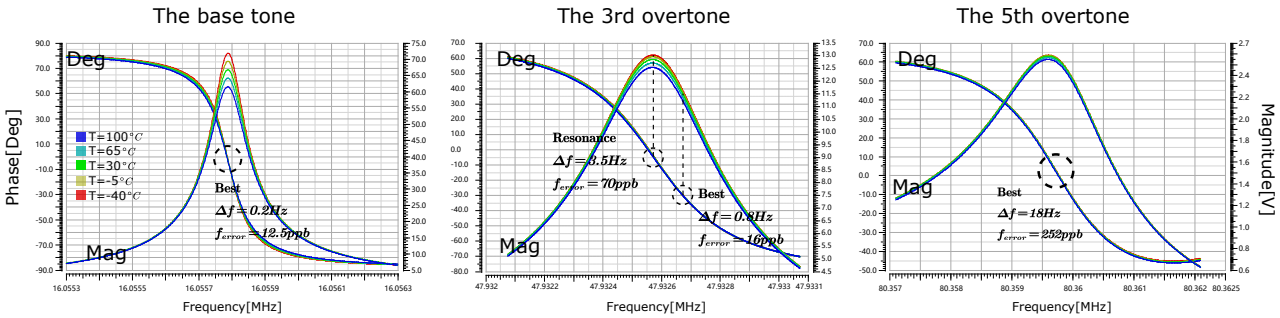


Figure 6.6: Magnitude and phase plot of transfer function (V_{in+}, V_{in-}) to (V_{out+}, V_{out-}).

Specifications	The basetone	The 3rd overtone	The 5th overtone
Drive capability	Output $V_{pp} \geqslant 1.8V$ with 50Ω load		
(a)Output referred noise $[V^2/Hz]$	4×10^{-14} 3.4×10^{-13}	9×10^{-16} 7.3×10^{-15}	1.8×10^{-16} -
Frequency error @ -40 to 100 °C [ppb]	12.5 10	16 10	252 10
Stability	Stable under typical corners		
Chip area $[m^2]$	1.75×10^{-8}		
Power consumption $[mW]$	95.6		

Table 6.2: Specifications of the crystal filter after design. The blue parts indicate the required values. (a)The quantization noise of ADC is not included.

From the perspective of noise performance, the base tone and the third overtone have lower output-referred noise than the required value, which implies a better CNR and phase noise in the overall MMXO system. The output-referred noise of the fifth overtone almost equals to quantization noise of ADC ($2.08 \times 10^{-16} V^2/Hz$). Therefore, the noise floor dominates its output referred noise as our estimation. According to Eq 3.3.7, we can calculate the phase noise caused by the fifth overtone around -136.5[dBc/Hz] at 1KHz offset, which would be even higher if we consider the aliased noise caused by ADC. Since the fifth overtone is not the dominant signal and how the noise of the fifth overtone propagates to the MMXO system is unknown yet, it is hard to get more insights by so far. It could be taken as future research to fully understand its noise mechanism. As a designer, we can offer some solutions and trade-offs to improve its noise performance based on the existing design. We will discuss some feasible improvement methods in the next section.

6.2 Improvement suggestions

Based on the existing design, the following paragraphs highlight important performance that can be improved:

- The frequency error of the fifth overtone is excessively large. The reason has two folds. First, the tested crystal has a low quality factor at the fifth overtone, which cannot be improved since it is decided by the structure of the crystal. Second, the

temperature dependent phase shift is still too high for the fifth overtone. Therefore, the only way to decrease its frequency error is to design a higher equivalent bandwidth according to the analysis in section 3.3[Frequency response]. We have seen that the phantom zero and miller effect terminates the bandwidth of the TA stage in a low frequency. After the integration of the TA and TI stage, there is no significant deterioration of frequency error by comparing Fig 4.30 and 6.6. Hence, improving the frequency compensation of the TA stage may be helpful to suppress frequency error.

- The noise performance of the fifth overtone is limited by quantization noise S_{vADC} of ADC. After aliasing, its noise would be even worse. Since the quantization noise is inevitable, some anti-aliasing techniques need to be applied to avoid excessive deterioration of its noise performance.
- According to table 1.2, the total power consumption of the MMXO is $300mW$. In this project, the total current usage is $47.2mA$. Considering the crystal filter working under 2.5V and 1.1V power supply, its total power consumption is around $94.2mW$, which is almost one-third of the total power consumed by the MMXO. A feasible approach to reduce the power consumed by the crystal filter is to use a lower power supply while keeping the total current unchanged.
- Comparing with the total chip area ($3600 \times 10^{-8}m^2$) of the MMXO, the crystal filter only takes up $1.75 \times 10^{-8}m^2$. It is surprising that the proposed crystal filter still has the potential to shrink chip size if some decoupling capacitors can be reduced or eliminated.

Frequency error

As we explained in section 4.4 and 4.4, the phantom zero introduced by the bondwire inductance terminates the asymptotic gain of the TA stage around 2.27GHz, which limits the frequency stability of the TA stage. an LR branch in series with crystal or a miller capacitor between the first and the second stage of the TA amplifier can improve its stability but not phase shift. Considering size and design difficulty, the pole splitting by miller capacitor C_{ps} is chosen.

During the design of the TA stage, we have seen the system becomes more stable and its bandwidth decreases by increasing the miller capacitor C_{ps}. However, the compensation may be excessive if we consider the influence of the TI stage. In fact, the TI stage may introduce dominant poles into the TA stage and decreases the bandwidth of the TA stage. In other words, C_{ps} may be too large if we consider a decreased bandwidth. Fig 6.7(a),(b) shows the overall frequency response varying with C_{ps}. Fig 6.7(c),(d) and (e),(f) shows the loop-gain plots of the TA and TI stage varying with C_{ps}, respectively. We can clearly see the overall bandwidth is increasing with a lower C_{ps} and stability margin. After C_{ps} is lower than $50fF$, the overall bandwidth barely increases since the bandwidth limitation is no longer the miller effect. Table 6.7 records the frequency error and bandwidth for the three tones at different C_{ps}. Frequency error of the fifth overtone significantly decreases with lower C_{ps}.

When C_{ps} is lower than $50fF$, bandwidth barely increases. The reason has two folds. First, the inductance of bondwire sets the bandwidth upper limit. The overall bandwidth cannot be higher than 2.27 GHz for $L_w = 1.5nH$. Second, the non-ideal interaction between the TI and TA stage may decrease the overall bandwidth below the designed specs

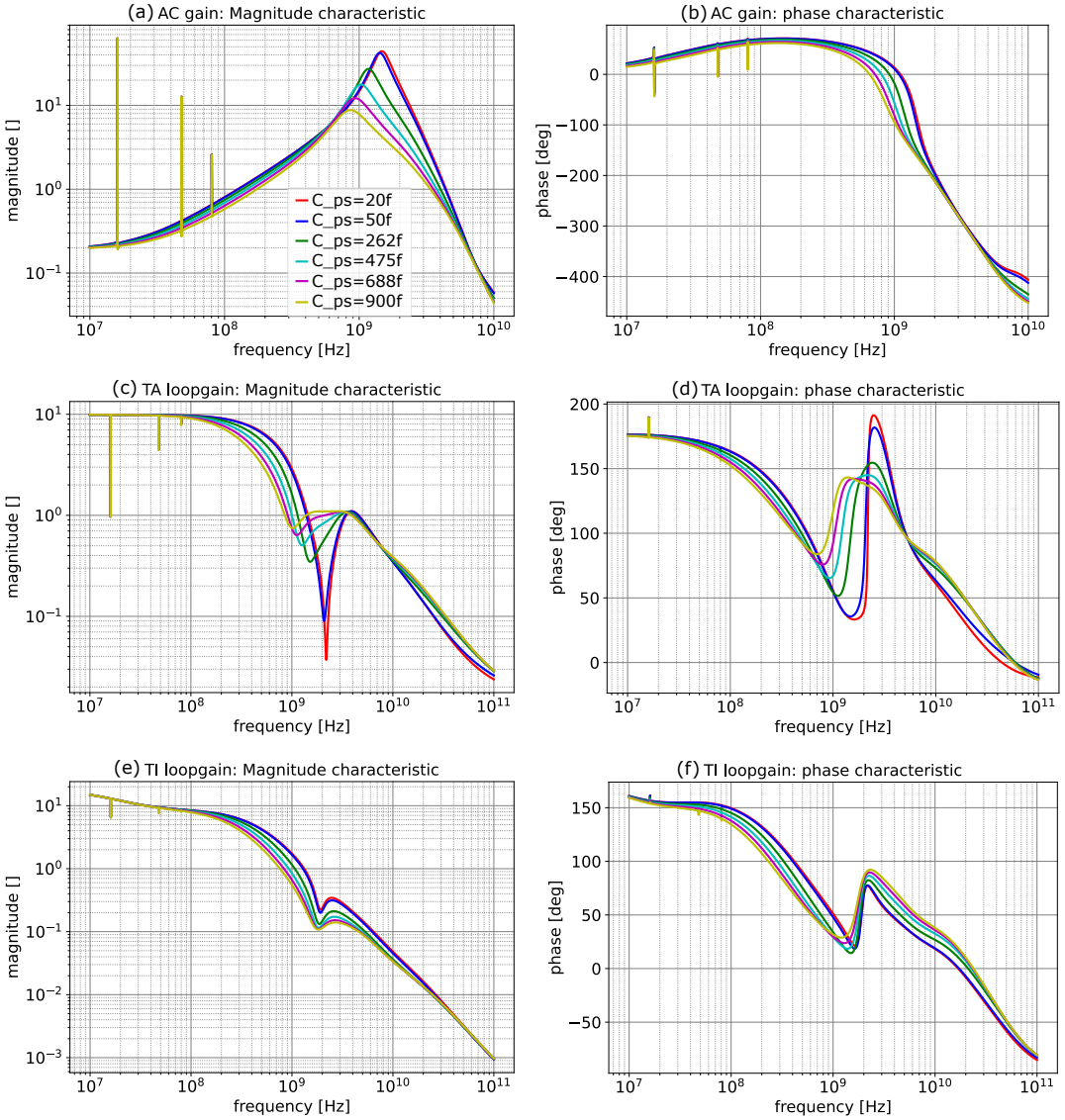


Figure 6.7: (a)(b)Overall frequency response varying with miller capacitor C_{ps}. (c)(d)loop-gain plots of the TA stage varying with C_{ps}. (e)(f)loop-gain plots of the TI stage varying with C_{ps}.

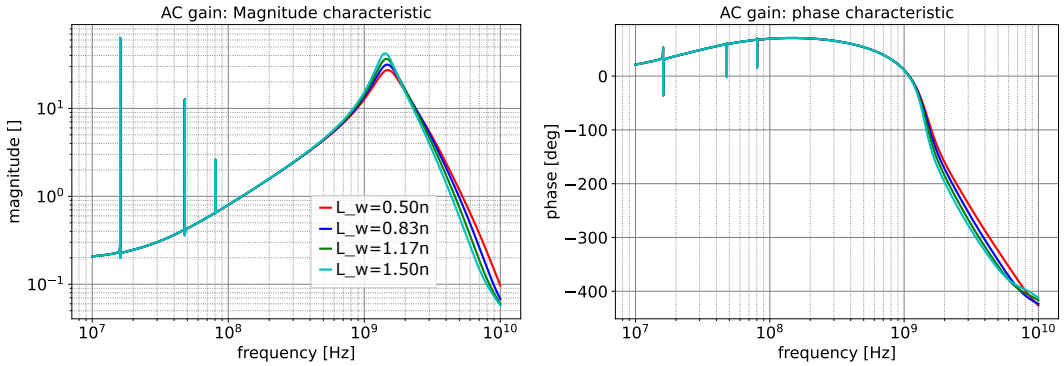


Figure 6.8: Overall frequency response varying with bondwire inductance L_w.

C_{ps} [fF]		900	688	475	263	50
Bandwidth [GHz]		0.86	0.90	1.07	1.19	1.43
f_{error} [ppb]	The base tone	12.5	8.9	7.4	5.3	3.1
	The 3rd overtone	16.0	12.3	10.2	6.3	3.8
	The 5th overtone	252	193	163	137	104

Table 6.3: Frequency error and bandwidth for the three tones at different C_{ps}.

Diameter [μm]	25	50	75	100	125
Analytical [pH]	1034	872	778	713	662
Measurement [pH]	1039	877	783	716	666

Table 6.4: Impact of diameter on partial self-inductance of bond wires.Source[20]

shown in table 5.5 and 4.8. Setting $C_{ps} = 50fF$, fig 6.8 shows the overall frequency response varying with inductance of the bondwires that are directly connected with the tested crystal. Although L_w decreases three times to $0.5nH$, the final bandwidth basically unchanged. Therefore, the phantom zero introduced by bondwire has not yet limited the final bandwidth. In other words, the circuitry still has the potential to get higher bandwidth. This could be achieved, by following the design steps described in chapter 4 and 5, with tradeoffs of more power and area.

For the improvement of the next-generation MMXO products, the low inductance interconnection technique is very important to break the bandwidth limit and achieve lower frequency error. Flip-chip technology and wire bonding are widely employed for interconnection. The former has wider bandwidth due to small parasitics. However, its fabrication process is complex and high-cost. As a traditional technique, wire bonding is a popular choice since it is low cost and simple in most industrial electronics. However, its high impedance limits its broadband application.

Some techniques were reported to improve the bandwidth of a bondwire interconnect. One method to minimize the inductance of bondwire is to increase its radius [20]. By increasing the diameter from $25\mu m$ to $100\mu m$, the partial self-inductance reduces by approximately 30%, from $1039pH$ to $666.1pH$. Using thicker bondwires leads to a significant improvement of the signal transmission properties with lower return and insertion loss. Table 6.4 shows the experimental results presented in paper [20]. Similarly, a bondwire with shorter length also exhibits wider bandwidth, but the minimum length is limited by the chip thickness. In order to short bondwire length effectively, paper [25] proposed a method that a cavity can be etched on the carrier to put a chip inside so that the top of the chip and the carrier can be near at the same horizontal level. To further reduce the bondwire inductance, multiple bondwires can be shunted together in parallel. However, the mutual inductance between bondwires sets a lower bound for the minimum achievable inductance. The operation bandwidth is still limited. Paper [3] proposed another wideband bondwire interconnection technique by forming a five-stage low-pass filter. It requires five elements for a single interconnect realization. The disadvantage is the occupied area is

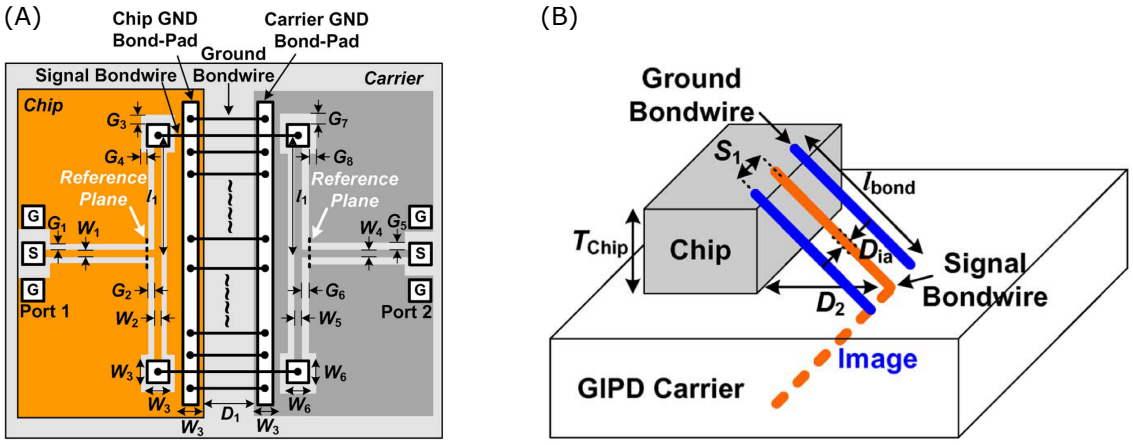


Figure 6.9: (A)The physical structure of the broadband interconnect using the multi-path technique. (B)The lateral view to estimate bondwire inductance. Source[14]

large and the cost is too high.

In 2013, CH Li and his team invented a low-cost bondwire interconnect to achieve broadband operation without any additional high-cost process [14]. Transmission lines are incorporated with bondwires to form a multi-path structure. With properly designing the characteristic impedance and the length of transmission lines, the bondwire effect can be reduced. The proposed the multi-path design for chip-to-carrier communications has around 3.2 times bandwidth of a single bondwire alone. Fig 6.9(a) shows the physical structure of the designed interconnect using the proposed technique, multiple bondwires are bonded between the chip ground and the carrier ground to minimize ground parasitics. In this structure, the ground bondwires adjacent to signal bondwires can also be used to reduce the bondwire inductance by inducing negative mutual coupling to the signal bondwires. Fig 6.9(b) shows the lateral view to estimate bondwire inductance. With two bondwires in parallel with length of $707\mu m$ and spacing of 20 μm, the effective bondwire inductance could be estimated around $0.52nH$, which is verified by the experiment results of return and insertion loss ($S11$ and $S22$ smaller than -16.6 and -13.4 dB, respectively.)

Another feasible solution to decrease frequency error is to use a crystal with higher quality factor. This could be achieved, by changing the cutting method and material of the crystal. Since it is directly related to the performance-to-cost ratio of the MMXO products, we need to further evaluate the commercial value.

Noise

The noise limitation for the 5th overtone due to the quantization noise of ADC implies a higher phase noise than -147[dBc/Hz]. There are two methods to improve its phase noise according to Eq 3.3.14, without changing the structure of existing design.

- Increase the input power of the fifth overtone.
- Increase the gain of the TI stage.

However, the above methods are not very effective since the total power consumed by crystal and the total output swing are both limited. If we want to reduce the noise of the fifth overtone, we have to sacrifice the performance of the base tone and the third overtone.

The main reason of this trade-off is that only one crystal filter is used for three tones. The dynamic range between the three tones limits their performance. If we can decouple the three signals and design three separate crystal filters for them respectively, each tone can acquire excellent performance without the trade-off. However, the price is increasing chip area, power consumption, and design complexity.

In addition, the aliased noise caused by ADC would make the noise performance of the fifth overtone even worse. Fig 6.10 shows the output-referred noise PSD before and after aliasing. With $2GHz$ full input bandwidth and $1.25GHz$ sampling frequency, the phase noise of the fifth overtone will be 4.2dB higher after aliasing. To decrease aliased noise, we need to apply ADC with higher sampling frequency or we allow higher frequency error and decrease the bandwidth of the crystal filter.

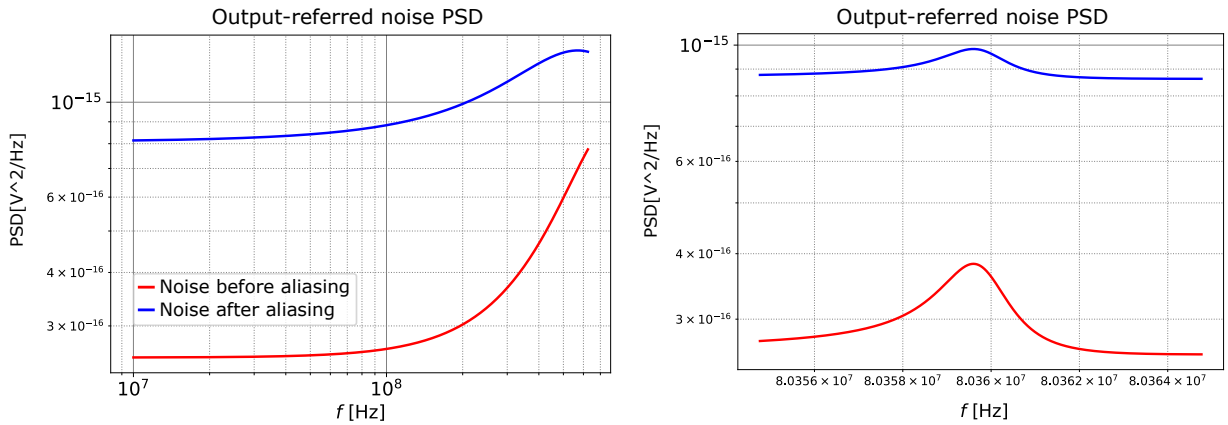


Figure 6.10: Left: Total output-referred noise PSD before and after aliasing over a wide frequency range. Right: Total output-referred noise PSD before and after aliasing around the fifth overtone.

Power consumption and chip area

The design of the crystal filter implements the current source by 2.5V transistors. Thus, The default setting of VDD is 2.5V. A feasible solution to decrease power consumption is to use lower VDD for those transistors, since there are enough saturation margins for M^+_{1bp}, M^+_{2bp}, and M^+_{3bp} as shown in Fig 6.1.

In addition, we can optimize chip area of the TA stage if the signal transistors (M^+_{1L}, M^+_{1R}, and M^+_2) can switch from 1,1V to a higher voltage level. As explained in section 4.5, the voltage shift network V_{shift} provides a voltage difference between the gate of M^+_{1R} and the drain of M^+_2 in DC, which establishes a stable biasing for both stages through negative feedback and avoid M^+_{1R} working under excessive drain voltage. However, the $5p$ capacitor of V_{shift} takes up $9.76 \times 10^{-9} m^2$, which is almost half of the total area and cannot be reduced since it is sensitive to signal quality and noise performance. Therefore, switching to higher voltage transistors, such as 1.8V transistors, is helpful to eliminate the design of V_{shift} and optimize chip area.

CHAPTER 7

Discussion

7.1 Summary

In this thesis project, a microelectronic design of a crystal filter for high accuracy multi-mode crystal oscillator has been presented. The objective of the crystal filter is to accurately reflect the frequency characteristic of the loaded crystal. Any temperature change should not affect the matching accuracy. The target for frequency error versus temperature variation from -40 to 100 °C is below 10[ppb]. The applied design approach in this thesis project is the structure electronic design (SED), which carefully considers the order of design procedures and makes the overall design orthogonal.

In chapter 2 and 3, we study the crystal characteristic and discuss the working principle of the crystal filter. Several optional structures and working modes of the crystal filter are compared and discussed. In order to acquire a relatively balanced performance of the three input tones, a TA+TI structure is chosen for the design. Based on the existing specifications of the MMXO, we calculate and summarize the gain, noise, and bandwidth design targets for the three tones, respectively. In the early-stage of design, we have acquired many useful insights into the crystal filter, which are confirmed by the pre-layout results. The following lines highlight the most important conclusions from the system design:

- The equivalent bandwidth and loop-gain of the crystal filter at the three resonance frequencies determines the frequency error of the three output signals respectively.
- Bondwires connected with crystal set the upper limit of bandwidth of the crystal filter.
- The noise performance of the fifth overtone is limited by the quantization noise and noise aliasing caused by ADC.

In chapter 4 and 5, we realize the derived specifications for the TA and the TI stage, respectively. Following the design approach of SED, the design of the amplifiers is divided into noise, drive capability, bandwidth&accuracy, frequency compensation, and biasing. The TA stage, which directly drives the tested crystal, reflects the frequency characteristic of the crystal by a current output. The TI stage transforms and amplifies the current output from the TA stage to the final voltage output for ADC. The pre-layout results after integration of the two stages are presented in chapter 6, the following paragraphs summarize those important performances achieved by the crystal filter:

The noise specifications of the crystal filter are derived from the phase noise of the current MMXO system. The base tone and the third overtone meet the noise requirements

with enough design margin, while the fifth overtone fails with noise specs due to the quantization noise and aliased noise caused by ADC.

The frequency error over the working temperature range is mainly determined by the equivalent bandwidth and loop-gain at the three resonance frequencies, which has been optimized and designed using symbolic analysis(SLICAP). The final result shows the frequency error of the base tone and the third overtone is close to 10 ppb, while the fifth overtone has a large frequency error around 252 ppb. Without changing the structure of the crystal filter, we can effectively improve the frequency error by weakening frequency compensation and enlarging bandwidth. The price is a lower stability margin. To further decrease the frequency error, we need to not only exchange bandwidth with more power and area consumed but also break the upper limit of bandwidth by low inductance interconnection techniques.

The crystal filter is able to drive the three input tones and provides full input swing for the ADC. In the pre-layout simulations, the amplifier is stable under all typical corners. The power consumed by the crystal is $20\mu W$, which ensures crystal safety during system operation. The amplifier only occupies a small area compared to the overall MMXO system.

7.2 Future work

This thesis design discusses the importance of bandwidth and DC loop gain to frequency stability. To do the best effort, we try to reach the bandwidth limitation set by bondwires while keeping a large DC loop-gain for the three tones. Although the final results are close to our expectations, we did not express and quantify their relationships. To improve the system design and better understand frequency stability versus temperature, we can mimic the small signal characteristic of transistors versus temperature with the EKV model in SLICAP. In this case, we can express and simulate many important performances as a function of temperature. Therefore, we can analyze the relationship between frequency and temperature more analytically and thus get more insights into the mechanism of the crystal filter.

For example, we have seen the phase shift caused by the TA and TI stage influence the final frequency error of the crystal filter together. Suppose the TA and TI stage have negative temperature dependent characteristics. In that case, the phase error caused by TA and TI stage can even cancel out each other in such an amplifier. To design such a TA and TI stage, we should stand on a solid study of the temperature coefficients of transistors.

APPENDIX A

Appendix

Chapter 2. System design

Crystal characteristic

Quality factor analysis

According to equation 2.1.6 and the crystal structure as shown in figure 2.1. Quality factor of crystal in series resonance frequency could be derived from series resonance frequency.

$$Q_s = \frac{\omega_s L_n}{R_n} = \frac{1}{R_n}\sqrt{\frac{L_n}{C_n}} \tag{A.0.1}$$

The quality factor of parallel resonance could be calculated as:

$$Q_p = \frac{2\pi\frac{1}{2}V_p^2\left(\frac{C_n+C_0}{C_n}\right)^2 C_0\frac{C_n}{C_n+C_0}}{\frac{V_p^2}{2\left(R_n^2+\left(\omega_p L_n-\frac{1}{\omega_p C_n}\right)^2\right)}R_n\frac{2\pi}{\omega_p}} \tag{A.0.2}$$

$$\omega_p = \sqrt{\frac{C_n+C_0}{L_n C_0 C_n}} \tag{A.0.3}$$

Substitute ω_p with equation 2.1.5,

$$\begin{aligned} Q_p &= \frac{2\pi\frac{1}{2}V_p^2\left(\frac{C_n+C_0}{C_n}\right)^2 C_0\frac{C_n}{C_n+C_0}}{\frac{V_p^2}{2\left(R_n^2+\left(\sqrt{\frac{C_n+C_0}{L_n C_0 C_n}}L_n-\frac{1}{\sqrt{\frac{C_n+C_0}{L_n C_0 C_n}}C_n}\right)^2\right)}R_n\frac{2\pi}{\sqrt{\frac{C_n+C_0}{L_n C_0 C_n}}}} \\ &= \frac{1}{C_0 C_n^2 L_n R_n}(C_0+C_n)\frac{C_0^2R_n^2+C_nC_0R_n^2+C_nL_n}{\sqrt{\frac{1}{C_0C_nL_n}(C_0+C_n)}} \\ &= \frac{1}{R_nC_n}\sqrt{\frac{C_0+C_n}{L_nC_0C_n}}\left(R_n^2C_0^2+C_nR_n^2C_0+L_nC_n\right) \end{aligned} \tag{A.0.4}$$

$$\begin{aligned}
\frac{Q_p}{Q_s} &= \frac{\frac{1}{R_nC_n}\sqrt{\frac{C_0+C_n}{L_nC_0C_n}}\left(R_n^2C_0^2+C_nR_n^2C_0+L_nC_n\right)}{\frac{1}{R_n}\sqrt{\frac{L_n}{C_n}}} \\
&= \frac{1}{C_n\sqrt{\frac{1}{C_n}L_n}}\left(C_0^2R_n^2+C_nC_0R_n^2+C_nL_n\right)\sqrt{\frac{1}{C_0C_nL_n}\left(C_0+C_n\right)} \\
&= \left(C_0^2R_n^2+C_nC_0R_n^2+C_nL_n\right)\sqrt{\frac{1}{C_0C_nL_n}\left(C_0+C_n\right)\frac{1}{C_nL_n}} \\
&= \sqrt{\frac{C_0+C_n}{C_0}}(1+\frac{C_0R_n^2}{L_n}+\frac{C_0^2R_n^2}{C_nL_n}) \\
&= \sqrt{\frac{C_0+C_n}{C_0}}(1+\frac{C_0R_n^2}{L_n}\frac{C_n+C_0}{C_n}) \qquad \text{(A.0.5)}
\end{aligned}$$

According to the data in 'XTalData 16.05M'. A 16.05MHz crystal for example with series resistance $R_n = 7\Omega$, has a motional inductance $L_n = 17mH$, motional capacitance $C_n = 5.7fF$ and shunt capacitance $C_0 = 1.65pF$. Q_s and Q_p could be obtained as:

$$Q_s = \frac{1}{R_n}\sqrt{\frac{L_n}{C_n}} = 2.4671 \times 10^5 \qquad \text{(A.0.6)}$$

$$\begin{aligned}
Q_p &= \sqrt{\frac{C_0+C_n}{C_0}}(1+\frac{C_0R_n^2}{L_n}\frac{C_n+C_0}{C_n})Q_s \\
&= \sqrt{\frac{C_0+C_n}{C_0}}(Q_s+\frac{1}{R_n}\sqrt{\frac{L_n}{C_n}}\frac{C_0R_n^2}{L_n}\frac{C_n+C_0}{C_n}) \\
&= \sqrt{\frac{C_0+C_n}{C_0}}(Q_s+R_n\sqrt{\frac{C_n}{L_n}}\frac{C_0(C_n+C_0)}{C_n^2}) \\
&= \sqrt{\frac{C_0+C_n}{C_0}}(Q_s+\frac{1}{Q_s}\frac{C_0(C_n+C_0)}{C_n^2}) = 2.4714 \times 10^5 \\
&\approx Q_s+\frac{1}{Q_s}\frac{C_0^2}{C_n^2} = 2.4671 \times 10^5 \qquad \text{(A.0.7)}
\end{aligned}$$

It could be observed that $Q_p > Q_s$ but their values are very close. On the later analysis, We assume that $Q_p = Q_s$ to compare the power consumption of crystal on different resonance frequency.

Power consumption/ R_p analysis

Assuming power P_0 is consumed by crystal, if power supply is working on series resonance frequency, the current I_s through crystal could be calculated as:

$$I_S = \sqrt{\frac{P_0}{R_n}} \qquad \text{(A.0.8)}$$

The total power consumption of circuit must satisfy:

$$P_{total.series} \geq V_{DD} \cdot I_s = V_{DD}\sqrt{\frac{P_0}{R_n}} \tag{A.0.9}$$

For parallel resonance frequency, equation A.0.8 is not applicable. R_n need to be translated into equivalent resistance R_p in parallel resonance frequency. As shown in figure 2.6, L_p and C_p cancel out each other in parallel resonance frequency. R_p behaves as a equivalent resistance to present power loss. Since $Q_s = Q_p$, it can be derived that:

$$\begin{aligned}
&Q_s = Q_p \Rightarrow \omega_p R_p^{'} C_p = \frac{\omega_s L_n}{R_n} \\
&\omega_s \approx \omega_p \\
&R_p^{'} = \frac{L_n}{R_n C_p} \\
&C_p = \frac{C_0 C_n}{C_0 + C_n} \\
&R_p = R_p^{'}\left(\frac{C_n}{C_0 + C_n}\right)^2 \\
&R_p = \frac{L_n C_n}{R_n C_0 \left(C_0 + C_n\right)}
\end{aligned} \tag{A.0.10}$$

$$\begin{aligned}
\frac{V_p^2}{R_p} &= \frac{V_p^2}{\left(R_n^2 + \left(\omega_p L_n - \frac{1}{\omega_p C_n}\right)^2\right)} R_n \\
R_p &= \frac{\left(R_n^2 + \left(\omega_p L_n - \frac{1}{\omega_p C_n}\right)^2\right)}{R_n} \\
&= \frac{\left(R_n^2 + \left(\sqrt{\frac{C_n + C_0}{L_n C_0 C_n}} L_n - \frac{1}{\sqrt{\frac{C_n + C_0}{L_n C_0 C_n}} C_n}\right)^2\right)}{R_n} \\
&= \frac{1}{C_0 R_n \left(C_0 + C_n\right)} \left(C_0^2 R_n^2 + C_n C_0 R_n^2 + C_n L_n\right) \\
&\approx \frac{C_n L_n}{R_n C_0 \left(C_0 + C_n\right)}
\end{aligned} \tag{A.0.11}$$

Assuming the same power P_0 is consumed by crystal in parallel resonance frequency, the voltage V_p across crystal could be calculated as:

$$V_p = \sqrt{P_0 R_p} \tag{A.0.12}$$

Because voltage across crystal must be smaller than power supply voltage,

$$V_p \leq V_{DD} \Rightarrow \sqrt{P_0 R_p} \leq V_{DD} \tag{A.0.13}$$

The power consumption limitation in parallel resonance frequency could be calculated as:

$$P_0 \leq \frac{V_{DD}^2}{R_p} \leq P_{total.parallel} \tag{A.0.14}$$

According to equation A.0.9 and A.0.14, the total power consumption in series resonance frequency should satisfy:

$$P_0 \leq V_{DD}^2 \sqrt{\frac{1}{R_p R_n}} \leq P_{total.series} \tag{A.0.15}$$

According to the data in 'XTalData 16.05M'. A 16.05MHz crystal for example with series resistance $R_n = 7\Omega$, has a motional inductance $L_n = 17mH$, motional capacitance $C_n = 5.7fF$ and shunt capacitance $C_0 = 1.65pF$. The equivalent shunt resistance at parallel resonance frequency have a value of $R_p = 5M\Omega$. Assume that power supply $V_{DD} = 1.8V$. It could be calculated that the limitation value for P_0 is 0.64 μW, which means the power consumption in parallel resonance frequency should satisfy $P_{total.parallel} \geq 0.64\mu W$ and the power consumption in series resonance frequency should satisfy $P_{total.series} \geq 547\mu W$ if crystal in two frequencies consume the same power P_0. It could be observed that parallel resonance frequency has better performance in power consumption.

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