Design of a Boost DC-DC Converter for Energy Harvesting Applications in 40nm CMOS Process

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Design of a Boost DC-DC Converter for Energy Harvesting Applications in 40nm CMOS Process

Master of Science Thesis

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Abstract

DC-DC converters are critical building blocks in energy harvesting systems which are applied to provide the energy for the implantable biomedical devices. They are required to meet very strict specifications and consume as less power as possible. Therefore, their power conversion efficiency and stability of the functionality in the varying environment become the major considerations in this thesis project, the target of which is to design a DC-DC converter for energy harvesting applications.

The conventional PWM control is not usually suitable for the DC-DC converters applied in energy harvesting applications because of its bad stability and low power conversion efficiency over wide input voltage and load current ranges. It is demonstrated that the adaptive on-time/off-time (AOOT) control proposed in this thesis is an excellent alternative to deal with the issue and the zero current switching (ZCS) adjustment technique can be applied to improve further the performance of the DC-DC converter by the fine tuning of the off-time.

In this thesis, a systematic design flow of a boost DC-DC converter has been presented from the design of the power plant, to the selection of the most suitable control technique, then to the transistor-level implementation and finally to the layout design. Moreover, the circuitry of a boost DC-DC converter and the layout of its most parts have been implemented in TSMC 40nm CMOS process. The post-layout simulation results prove that the proposed boost DC-DC converter can generate a stable $1V$ output voltage with very small ripples ($< \sim 10mV$) and achieve more than 90% (maximum about 95%) power conversion efficiency over a wide input voltage range ($0.35V \sim 0.65V$) and a wide load current range ($1mA \sim 10mA$).

Keywords: Boost DC-DC converter, Energy harvesting, Power conversion efficiency, Adaptive on-time/off-time control, Zero current switching adjustment.

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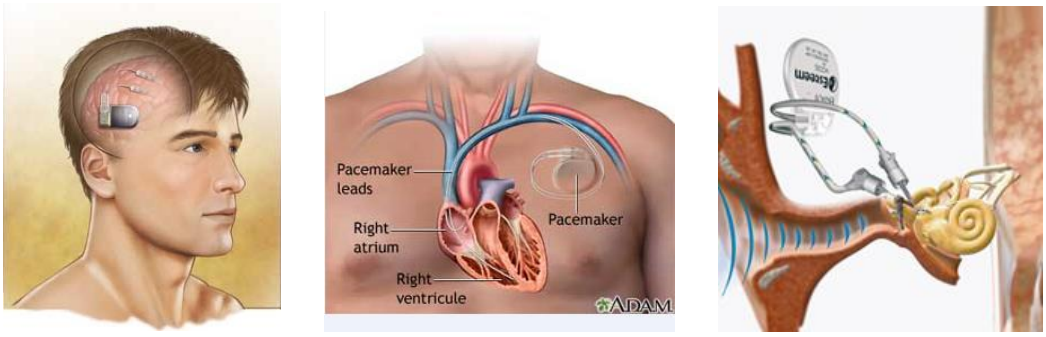
Chapter 1

Introduction

1.1 Background

In the past few decades, due to the explosive growth of the microelectronics industry and semiconductor technology, the electronic products, which are becoming not only smaller and smaller but also more and more complex, have played a very important role in shaping human society. The emergence of many electronic products has changed the lifestyle of the human beings, such as the laptop or the mobile phone. The booming development of electronic devices has promoted a lot to the advance of the biomedical technology, which causes the situation that various kinds of implantable electronic devices are currently being used to monitor, diagnose and treat the diseases for personal healthcare, such as the neurostimulator (Figure 1-1.a) [1], the pacemakers (Figure 1-1.b) [2] and the cochlear implant (Figure 1-1.c) [3].



(a) (b) (c)

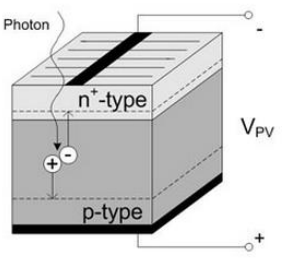
Figure 1-1: Implantable electronic devices in the biomedical application [1] [2] [3].

It is common sense that any electronic device cannot operate without power. Hence, the implantable biomedical devices need to be powered by some power supplies. In the consideration of the volume and convenience, these devices generally use tiny batteries assembled on the devices as the power source. But accordingly, a great challenge occurs,

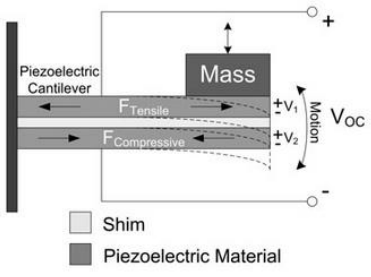
that is how the batteries can be replaced or recharged when the energy is depleted. Obviously, it is quite difficult or even infeasible to replace the batteries of the biomedical devices which have been implanted into the human body. Therefore, many efforts have been made on exploring an efficient method to realize self-powered or self-rechargeable power supplies for the implantable devices.

Energy harvesting technology provides a suitable solution to the issues mentioned above. Although the earliest use of energy harvesting dates back to the windmill and the waterwheel, the energy harvesting discussed afterwards refers to techniques which are based on semiconductor technology and used for low-energy electronics. Energy harvesting systems can capture ambient energy such as solar, thermal, kinetic or radio-frequency (RF) energy and transform the captured energy into the electrical domain so as to charge the battery or directly power the implantable device. A brief introduction to four most common existing harvesting techniques has been proposed in [4]. The four harvesting techniques are solar energy harvesting, thermoelectric energy harvesting, kinetic energy harvesting and RF energy harvesting.

All the energy harvesting techniques can be applied to supply power to implantable biomedical devices. But the specific application will be restricted by some practical limitations. For example, for solar energy harvesting (Figure 1-2.a) [5], the limited area of the solar receiver and the low intensity of the light which can be received by the harvester will make this technique not available for devices deeply implanted into the body or under the skin. For kinetic energy harvesting (Figure 1-2.b) [5], since the motion or activity made by some parts of the human body is weak, this technique is unsuitable for devices which are implanted in a part of the human body without much motion. Moreover, for thermoelectric energy harvesting (Figure 1-2.c) [5], to ensure a sufficient temperature difference between two sides of the harvest, this technique is suitable for devices inlaid on the skin, because one side of which can sense the temperature of human body and the other side of which can sense the temperature of ambient air. Finally, for RF energy harvesting (Figure 1-2.d) [6], since the power density of the RF signal that can be received from a nearby base station is quite low ($-12dBm/m^2$) [7], the feasible solution is to use a dedicated RF source to supply enough power for the RF energy harvesting system in the implantable devices [8]. The principle of this method is similar to that of radio-frequency identification technology (RFID).



(a)



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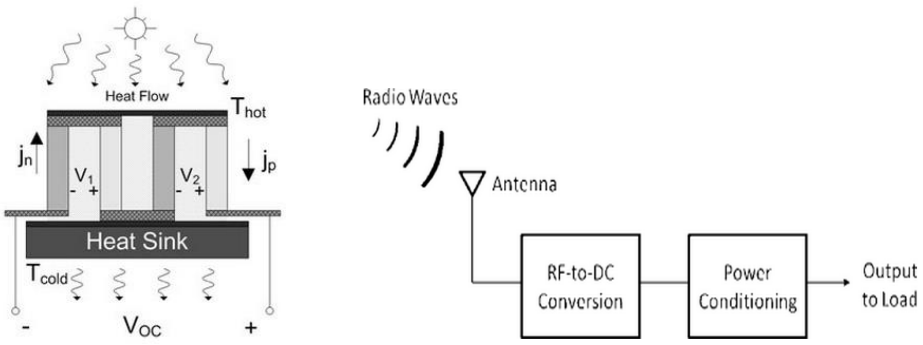

(c) (d)

Figure 1-2: Energy harvesting techniques: (a) solar energy [5]; (b) kinetic energy [5]; (c) thermoelectric energy [5]; (d) RF energy [6].

No matter of which kind of energy harvesting system, there is a common phenomenon, that is, the output voltage of the energy harvester is generally too low to provide the supply voltage for the battery. For current battery technology, it requires a supply voltage at least around $1V$ to charge the battery. But as mentioned in [9] [10], for body-wearable applications, the output voltage can only achieve about $100mV$ for the thermoelectric generators (TEG) and the output voltage of a single solar cell is just about $500mV$ outdoors but becomes lower than $200mV$ in dark office environment. For the RF energy harvesting system with a single stage rectifier (voltage doubler), the results of [11] show that, if the input power is about $0dBm$, the output voltage of the RF energy harvester is just over $100mV$. Although the output voltage of the RF energy harvester can be raised by increasing the number of stages of the rectifier (voltage doubling circuit), according to the conclusion made in [12], the RF-to-DC power conversion efficiency of a multistage configuration will be worse than that of a single stage configuration. Therefore, because of the bad power conversion efficiency, the number of stages of AC-DC converters should be limited. Instead, a DC-DC converter whose efficiency can ideally achieve 100% is applied to boost the small output voltage of the energy harvester to the required level for charging the battery. Figure 1-3 shows a RF energy harvesting system which can be used to charge the battery of implantable devices.

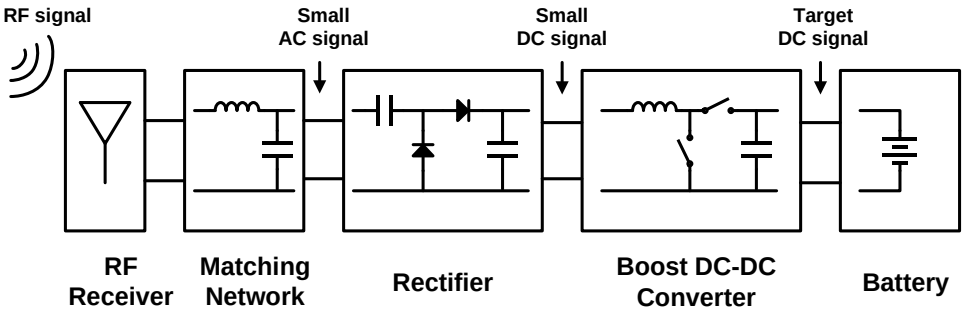

Figure 1-3: RF energy harvesting system used to charge the battery.

1.2 DC-DC Converter

The Direct-Current to Direct-Current (DC-DC) converter is an electronic circuit which can convert a DC voltage into another DC voltage. It has been widely used in current portable electronic devices for regulation of supply voltages. Since the current electronic devices are generally constituted by several sub-circuits, each of which requires its own supply voltage perhaps different from the voltage supplied by the battery or the external supplier, a DC-DC converter can be used to realize the step-up or step-down conversion of the supply voltage. Figure 1-4 shows the function of a DC-DC converter in a battery-operated portable device, in which the battery voltage is converted into different voltages for supplying different blocks in the device.

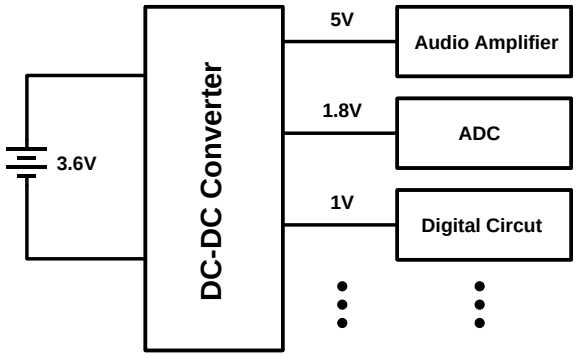

Figure 1-4: General application of a DC-DC converter in portable devices.

In recent years, due to its characteristics, the DC-DC converter has also been widely used in energy harvesting system to convert the voltage generated by the harvester to the stable voltage required by the back-end circuit or battery. For the DC-DC converter in an energy harvesting application, the power conversion efficiency which is equal to the output power over the input power, is generally the most important consideration.

There are three fundamental methods that can be applied to achieve the DC-DC voltage conversion. The first one is using linear voltage conversion on resistive dividers. This kind of DC-DC converter is also named low-dropout regulator (LDO). The basic operating principle of the linear voltage converter can be explained with the aid of an example shown in Figure 1-5. The target voltage is obtained from the resistive divider composed of a variable resistor (R_{series}) and a constant resistor (R_{load}). The control circuit adjusts the value of the variable resistor so as to regulate the output voltage to the desired value. For this kind of DC-DC converter, as the output voltage is generated by a division of the input voltage, it can only achieve step-down voltage conversion. Another drawback of this method is the poor power conversion efficiency. Since the excess power is dissipated on the resistor (R_{series}), this method is inefficient compared to the other two ones which will be introduced afterwards. Moreover, according to Equation 1.1 which is

used to calculate the power conversion efficiency of the linear voltage converter shown in Figure 1-5 [13], the efficiency will get even worse in the condition where the voltage conversion ratio ($V_{\mathrm{out}}/V_{\mathrm{in}}$) is small and the control current (I_{c}) is high. However, because the control circuit is relatively simple and neither any large inductors nor capacitors are required, the implementation of this kind of DC-DC converter is comparatively simple and area-saving. Therefore, the linear voltage convertor is well suitable for applications with low requirements on the power conversion efficiency but high demand on design simplification and area limitation.

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{out}} \cdot I_{\mathrm{o}}}{V_{\mathrm{in}} \cdot (I_{\mathrm{o}} + I_{\mathrm{c}})} \tag{1.1}$$

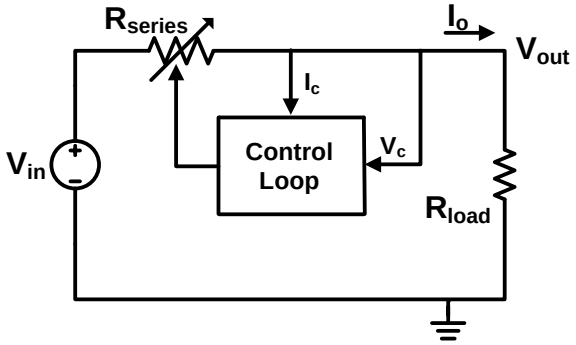

Figure 1-5: Schematic of a linear voltage converter [13].

The second approach to implement a DC-DC converter is using a switch-mode charge-pump circuit to realize the step-up or step-down voltage conversion. In this kind of DC-DC converter, there are some energy-storing capacitors and power switches. By periodically turning on and off the power switches, the topology of the circuit is changed, thus achieving the voltage conversion. Figure 1-6 shows the circuit and the operating principle of a step-up charge-pump DC-DC converter. In the first phase (Φ_1), since the flying capacitor C_1 is connected to the input voltage source, the energy coming from the input is stored in C_1. In the second phase (Φ_2), since the flying capacitor C_1 is connected to the load capacitor C_2, the energy stored in the flying capacitor C_1 is delivered to the load capacitor C_2. The output voltage of this DC-DC converter can be expressed by Equation 1.2 [13].

$$V_{\mathrm{out}} = \frac{2R_{\mathrm{L}}f_{\mathrm{sw}}C_1}{1+R_{\mathrm{L}}f_{\mathrm{sw}}C_1}V_{\mathrm{in}} \tag{1.2}$$

From the expression, it can be concluded that, if the item ($2R_{\mathrm{L}}f_{\mathrm{sw}}C_1$) is larger than 1, this circuit can achieve a step-up voltage conversion. In the ideal case, as no quiescent power dissipation exists in this kind of DC-DC converter (ignore the power consumption of the control circuit), the power conversion efficiency of this converter can achieve approximately 100% in the special case (the output voltage is double of the input voltage).

But in reality, since the static and dynamic power losses of the power switches are in a non-negligible level, and the complex control circuit which is required to control many power switches will consume much power, the efficiency of this kind of converter cannot be as perfect as expected. Although the power conversion efficiency of this kind of DC-DC converter is generally better than that of the first method, in most case, it is worse than that of the third method which will be discussed in the following.

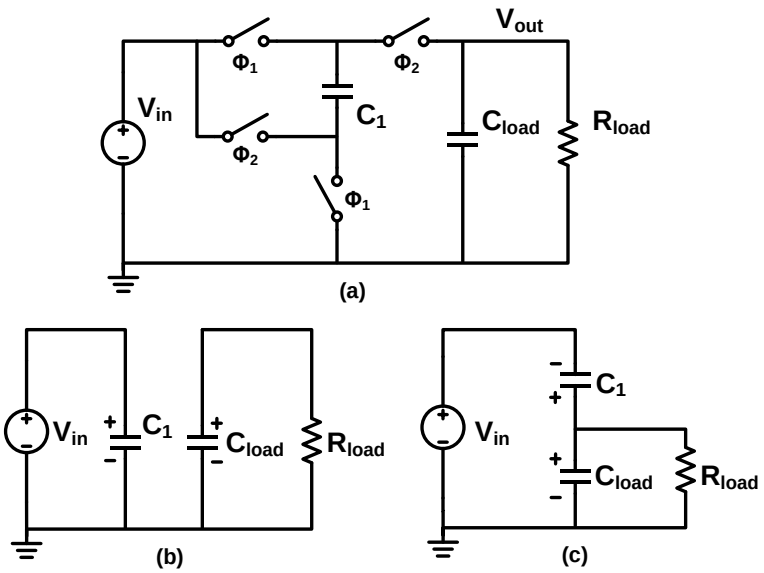

Figure 1-6: Schematic of a charge-pump DC-DC converter [13].

The third method to achieve the DC-DC voltage conversion is by means of a combination of an inductor and a capacitor. This kind of DC-DC converter also belongs to switch-mode DC-DC converters (inductor-based) whose operating principle is similar to the charge-pump DC-DC converter. Through turning on and off the power switches in the converter, the energy coming from the input voltage source is periodically stored in the inductor and delivered to the load capacitor, thus achieving step-up or step-down voltage conversion. Figure 1-7 shows the circuit and working principle of an inductor-based step-up (boost) DC-DC converter. In the first phase, when the power switch S_1 is closed and the power switch S_2 is open, the current is charged in the inductor. In the next phase, the power switch S_1 is open and the power switch S_2 is closed and the energy stored in the inductor is delivered to the load capacitor. A detailed explanation of its operating principle will be given in Section 2.1. As the inductor is a reactive component as the capacitor, the charging and discharging of an ideal inductor also involves no energy loss. Therefore, in the ideal case, the power conversion efficiency of the inductor-based DC-DC converter can achieve 100% as well. However, since the number of the power switches in an inductor-based DC-DC converter is generally half of that in a charge-pump DC-DC converter, the power losses of the third method, which are mainly caused by the

power switches and the control circuit, are less than those of the second method. Hence, the power conversion efficiency of the inductor-based DC-DC converter is normally the best among all the implementation methods. But as a trade-off, due to the use of a large inductor which in most cases cannot be integrated on an IC, this method is more area consuming than the other ones.

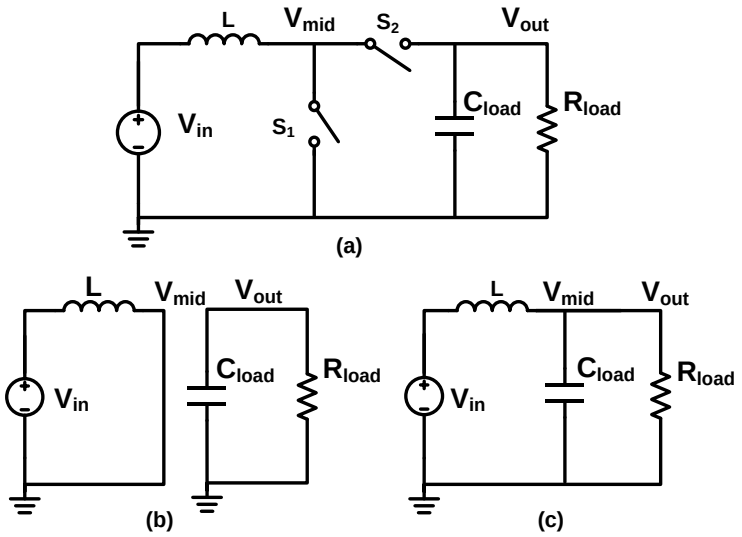

Figure 1-7: Schematic of an inductor-based boost DC-DC converter [13].

After the above brief introduction of the properties of three fundamental methods to implement the DC-DC converter, it can be seen that each method has its own advantages and disadvantages. In order to choose the best one for a specific design of a DC-DC converter, the designer should be well aware of which specification (power conversion efficiency, area consumption, design simplification, etc.) is most important for the target application and make the decision based on this. In this thesis, as the power conversion efficiency is the primary specification, the inductor-based method is chosen for the boost DC-DC converter designed in this work. If without specific notification, all the DC-DC converters mentioned afterwards refer to the inductor-based DC-DC converter.

1.3 Research Objectives

This research was carried out in the Analog IC Design team of the Ultra-Low Power Wireless System group at the Holst Centre/ imec in the Netherlands. The final target of this work is to design a high power conversion efficient boost DC-DC converter which can be used to convert the low voltage generated by the front-end energy harvester to a high voltage for charging the back-end battery. Since the input voltage of the boost DC-DC converter is derived from an energy harvesting system, it will vary in a range

along with the variation of the input power received by the energy harvester. In addition, the load battery requires a $1V$ supply voltage for charging and it can be charged in two modes (fast/slow). In the fast charging mode, the battery can be considered equivalent to a constant $10mA$ load current source. In the slow charging mode, the battery can be equivalent to a constant $1mA$ load current source. According to the requirements provided by our company, the design specifications can be listed in Table 1-1:

Table 1-1: Specifications of this research

	Value
Input voltage (V_{in})	$0.4V \pm 10\%$
Output voltage (V_{out})	$1V$
Output voltage ripple (V_{ripple})	$< 10mV$
Load current (I_{load})	$10mA$ (fast charging mode) 1mA (slow charging mode)
Power conversion efficiency (η)	As high as possible
Chip area (A)	As small as possible

Since this is the first time to design a boost DC-DC converter for energy harvesting application in our team, besides to design a specific circuit which can meet the specifications, another important task of this research was to build up a systematic design flow and analysis method of a DC-DC converter design, the aim of which is to provide a guideline to our team for further design of any other types of DC-DC converters in other applications. Therefore, in the following chapters, there will be a lot of discussion on how to choose the best solution to a specific problem occurring in the entire design process

Although the target application of this boost DC-DC converter is RF energy harvesting, after some slight adjustments of the parameters of the circuit system, this boost DC-DC converter can actually be used for a wide application range.

1.4 Thesis Outline

This thesis is organized as follows. The basic operating principle and the main power loss mechanisms of the boost DC-DC converter are introduced in Chapter 2. The preliminary design of the power plant of the boost DC-DC converter including ways to determine the values of the inductor and load capacitor as well as the sizes of the power switches is also

discussed in Chapter 2. In Chapter 3, general control techniques of the boost DC-DC converter are discussed and the adaptive on-time/off-time (AOOT) control method with zero current switching (ZCS) adjustment which is applied in this design is explained. The detailed transistor-level implementation of the schematic of the boost DC-DC converter is presented in Chapter 4 together with some important design considerations. The layout design of the boost converter is described in Chapter 5, which mainly focuses on two main parts of the circuitry, the MOS transistors used for power switches and the current mirror array applied in the DAC for ZCS adjustment. The post-layout simulation results of the boost DC-DC converter designed in this work are presented and discussed in Chapter 6. Finally, a summary of this thesis project including the contributions, conclusions and recommendations for future works is made in Chapter 7.

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Chapter 2

Basic Principle Analyses and Preliminary Design

2.1 Basic Working Principle of the Boost DC-DC Converter

The boost DC-DC converter is applied to convert a low-level DC voltage into a high-level quasi DC voltage. Quasi DC voltage means that the actual output of the boost converter is a DC voltage along with a small AC voltage ripple. As the AC voltage ripple is quite small compared to the DC voltage, the output of the boost converter is generally considered to be a DC voltage. This is also the reason why it is named a DC to DC converter. Figure 2-1 shows the basic circuit diagram of an inductor-based boost DC-DC converter. In the boost converter, two power switches are alternatively opened and closed, which periodically switches of the inductor between the input terminal and output terminal, thus, achieving the function of boosting the voltage.

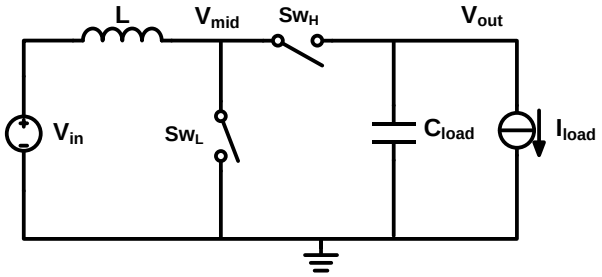

Figure 2-1: Basic Inductor-based boost DC-DC converter.

Based on different waveforms of the inductor current, there are two conduction modes for the boost converter, which are the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM), respectively. In CCM, there is always a positive current existing in the inductor (The positive direction is defined as flowing from the input terminal to the output terminal). In the ideal case of CCM, one of the power switches is immediately turned open when the other one is turned closed, which means

there is not a moment (dead time) when two power switches are simultaneously open. In DCM, the current flowing through the inductor will go down to zero and stay in zero for some while, which means there is a period of time (dead time) when the two power switches will be both open.

Before analyzing the basic working principle of the boost DC-DC converter working in CCM or DCM, some general assumptions should be made first. Based on these assumptions, it will be easy to describe the waveforms of the boost converter. A detailed theoretical analysis of this method has been provided in Erickson's book [1], in which it is named the small-ripple approximation method. The assumptions include:

(1) The converter operates in the steady state. This means that the system parameters including the input voltage, output voltage and the load current are all constant. For the boost converter, it also means that the start-up phase has been passed.

(2) The ripple of the output voltage is very small with respect to the average (DC) value of the output voltage. It means that the output voltage is regarded as a DC voltage.

(3) All the components of the converter are ideal and lossless. It means that the parasitic effects of the inductor, the capacitor and the MOS transistors are all ignored.

(4) The relationship between the voltage and the current for the inductor and the capacitor are all linear. It means that the voltage across the inductor and the current flowing out of the capacitor should always satisfy the basic equations:

$$V_{\mathrm{L}} = L \cdot \frac{di_{\mathrm{L}}}{dt} \tag{2.1}$$

$$I_{\mathrm{C}} = C \cdot \frac{dv_{\mathrm{C}}}{dt} \tag{2.2}$$

Based on these assumptions, the working principle of the boost converter will be explained as follows. When the low-side power switch (Sw_{L}) is closed and the high-side power switch (Sw_{H}) is open, the converter works in the on-time phase. In this phase, the structure and the waveforms of the converter are shown in Figure 2-2. As the middle point of the converter is connected to ground, the voltage at this point (V_{mid}) is zero. According to Equation 2.1, the current flowing through the inductor (i_{L}) increases by a constant ratio, which is:

$$\frac{di_{\mathrm{L}}}{dt} = \frac{V_{\mathrm{in}}}{L} \tag{2.3}$$

As for the output voltage of the converter (V_{out}), since the load capacitor is loaded with a constant current source, the output voltage decreases by a constant ratio, which is:

$$\frac{dv_{\mathrm{out}}}{dt} = \frac{I_{\mathrm{load}}}{C_{\mathrm{load}}} \tag{2.4}$$

After the on-time phase, the boost converter enters into the off-time phase, in which, the low-side power switch (Sw_{L}) is open and the high-side power switch (Sw_{H}) is closed. The structure and the waveforms of the converter in this phase are shown in Figure 2-3. Since the middle point of the converter is connected to the output, the voltage of this point (V_{mid}) is approximately equal to the DC value of the output voltage ($V_{\mathrm{out\_dc}}$). Therefore,

the current flowing through the inductor (i_L) can be regarded as decreasing by a constant ratio, which is

$$\frac{di_L}{dt} = \frac{V_{out\_dc} - V_{in}}{L} \tag{2.5}$$

In this phase, the load capacitor is not only discharged by the constant load current but also charged by the inductor releasing current which is expressed by Equation 2.5. Hence, in the off-time phase, the output voltage satisfies that:

$$\frac{dv_{out}}{dt} = \frac{i_L - I_{load}}{C_{load}} \tag{2.6}$$

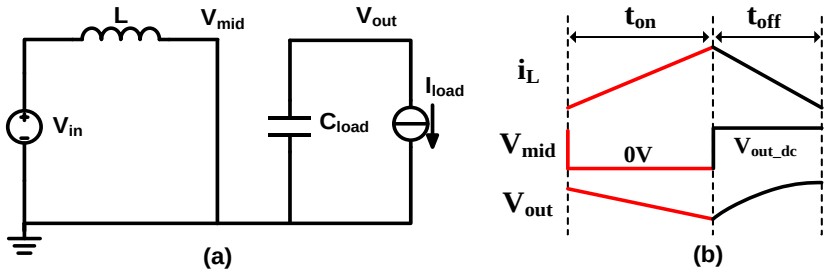

Figure 2-2: Boost DC-DC converter in the on-time phase.

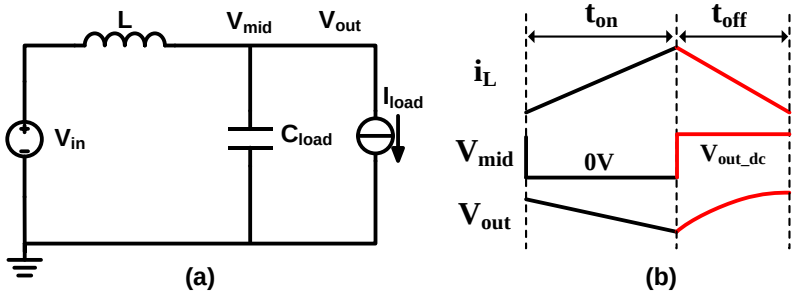

Figure 2-3: Boost DC-DC converter in the off-time phase.

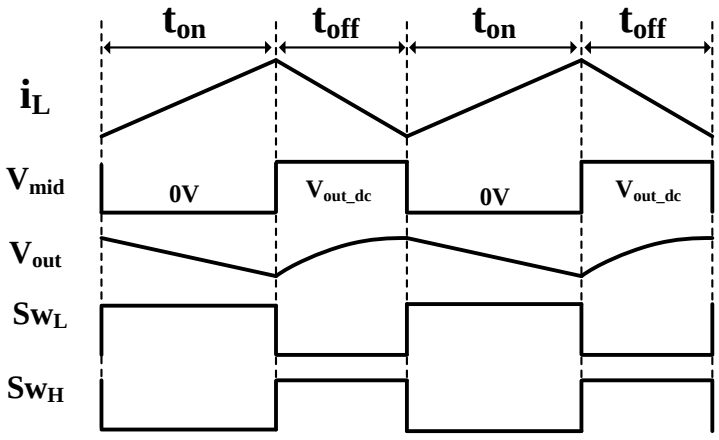

Figure 2-4: Timing diagram of main signals in a CCM boost converter.

For the boost converter working in CCM, there are only two phases, one of which is the on-time phase and the other is the off-time phase. The working principle of a CCM boost DC-DC converter can be illustrated by the timing diagram of the main signals in the converter, which is shown in Figure 2-4. However, for the boost converter working in DCM, since there is a period of time when two power switches are both open, an additional phase which is named the dead-time phase exists in the switching period of the DC-DC converter. In the dead-time phase, the structure and the waveforms of the boost converter are shown in Figure 2-5. Since both switches are open, the voltage of the middle point (V_{mid}) is equal to the input voltage, which means the voltage across the inductor and the current through the inductor are both zero. The output of the converter is in the same condition as during in the on-time phase. Therefore, the output voltage decreases by the ratio which has been expressed in Equation 2.4. The timing diagram of the main signals in the DCM boost DC-DC converter is shown in Figure 2-6.

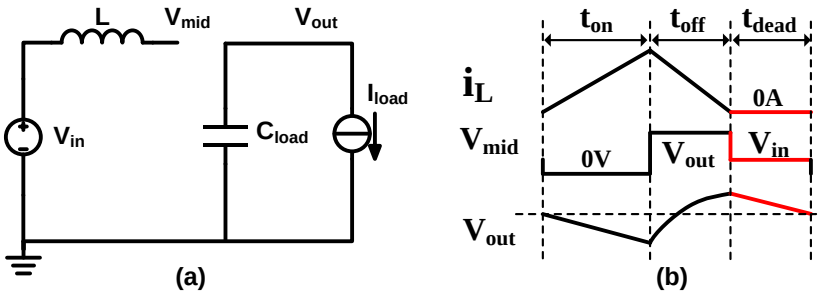

Figure 2-5: Boost DC-DC converter in the dead-time phase.

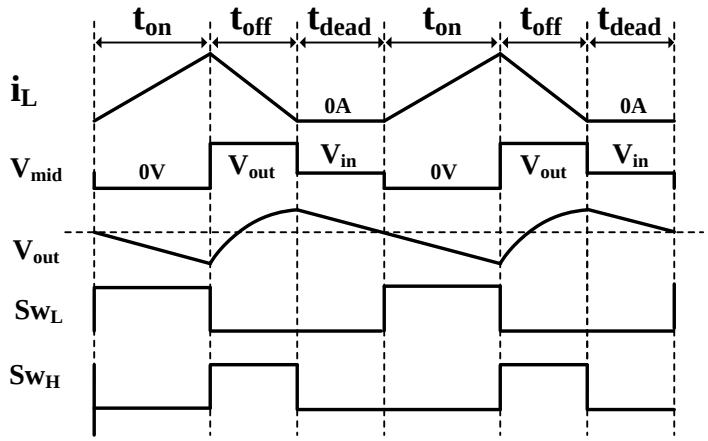

Figure 2-6: Timing diagram of the main signals in a DCM boost converter.

From the discussion above, we can see that the working condition of a DC-DC converter is determined by the power switches. Therefore, in the entire system of a DC-DC converter, apart from the circuit shown in Figure 2-1 (normally named as the

power plant of a DC-DC converter), there should be a control system that is used to automatically control the opening and closing of the power switches alternatively. The detailed discussion on the control system will be given in the next chapter.

The voltage conversion ratio (k) which is the ratio of the output voltage over the input voltage is an important parameter for a DC-DC converter. In a specific application, this value is usually required to be fixed. Therefore, knowing its relationship with other parameters will be very helpful for the design of a DC-DC converter. However, for the converters working in different conduction modes (CCM or DCM), the expressions of this value are quite different. For the converters working in CCM, this value is only related to the duty cycle (D). But for the converters working in DCM, this value depends not only on the duty cycle (D) but also on the inductor value (L) and the load resistor (R_{L}). The derivation of the expressions is normally based on the volt-second balance of the inductor. Since in steady state and regardless of the losses the net energy change in the inductor over a switching period is zero, the volt-second balance of the inductor is also zero [2], which can be expressed:

$$\int_0^T V_{\mathrm{L}}(t)dt = V_{\mathrm{in}} t_{\mathrm{on}} + (V_{\mathrm{in}} - V_{\mathrm{out}})\, t_{\mathrm{on}} = 0 \tag{2.7}$$

Therefore, for the converters working in CCM, it holds

$$k = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{t_{\mathrm{on}}+t_{\mathrm{off}}}{t_{\mathrm{off}}} = \frac{T}{t_{\mathrm{off}}} = \frac{1}{1-D}\ , \tag{2.8}$$

for the converters working in DCM, it holds

$$k = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{1+\sqrt{1+\frac{2R_{\mathrm{L}}}{L(t_{\mathrm{on}}+t_{\mathrm{off}}+t_{\mathrm{dead}})}t_{\mathrm{on}}^2}}{2} = \frac{1+\sqrt{1+\frac{2R_{\mathrm{L}}TD^2}{L}}}{2}\ , \tag{2.9}$$

in which $t_{\mathrm{on}}, t_{\mathrm{off}}$ and t_{dead} represent the durations of the on-time, the off-time and the dead-time, respectively. T is the total switching period. The detailed mathematic derivation of these equations is introduced in [2]. In this thesis, no more discussions about the mathematic derivation will be given. We just want to mention that, according to Equations 2.8 and 2.9, how the parameter variations affect the DC-DC converter can be clearly observed. Therefore, these two expressions are quite useful for the design of a DC-DC converter.

The circuit shown in Figure 2-1 is normally named a synchronous boost DC-DC converter, in which two power switches are applied to control the converter. In some applications, since a diode can implement the same function as the power switch does, the high-side power switch can be replaced by a diode, as shown in Figure 2-7. The DC- DC converter in this structure is also named an asynchronous DC-DC converter. However, due to the high forward voltage drop, it would be inefficient to use a diode for the high-side switch [3], especially in low-voltage electronic circuit design such as this work (the maximum voltage is about 1V). In a DC-DC converter, the voltage drop across the power switch or the diode is expected to be as small as possible, since a high voltage drop will cause a large power loss. For Schottky diodes, the typical forward drop voltage drop

is about 200-300mV [4], which is too high to use in this work. Although there are some techniques which can be used to implement a diode with a low forward voltage drop [4] [5], the circuit implementations are all quite complex and will consumes much extra power. In this work, the synchronous structure is finally used for the DC-DC converter design, which can not only simplify the design work but also achieve a relatively low voltage drop across the high-side switch. The final simulation results (in Chapter 6) show that the maximum value of this voltage is less than 50mV.

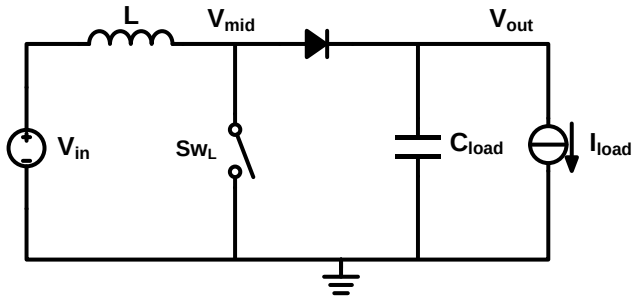

Figure 2-7: Asynchronous boost DC-DC converter.

In the previous discussion about the working principle of the boost DC-DC converter, we have assumed that the boost converter works in the steady state. But before reaching the steady state, the boost converter has to undergo a startup phase. During the startup phase, the output voltage of the converter rises from zero to the steady value.

Since the circuit blocks of the control system require a sufficient supply voltage to work, there should be a high enough voltage that can be used to power the control system. In the buck DC-DC converter, the input voltage is usually high enough to provide the supply voltage for the control system, so the supply voltage can be obtained directly from the input voltage or through a voltage divider. But in the boost DC-DC converter, in some cases, the input voltage is too low to provide the supply voltage for the control system, so the output voltage is used to power the control system when the boost converter works in the steady state. But during the startup phase, as the output voltage starts from zero, there will is some time when the output voltage is not high enough. Therefore, an external circuit is usually required to generate the supply voltage for a while until the output voltage arises to a sufficient value. Then the output voltage is used for the supply voltage, and the external circuit is switched off.

Many startup mechanisms have been proposed in previous studies. For instance, an extra auxiliary voltage [2] or battery [6] is used to charge the output of the converter to the minimum supply voltage during the startup phase; and in [7], a mechanical switch is applied to transform vibration mechanical energy into electrical energy to provide the startup voltage for the converter; in [8], an inductor-based transformer is used to form a positive feedback loop which can amplify the thermal noise to generate the startup voltage; in [9], an RF energy harvester is used with a multi-stage voltage doubler to

generate the startup voltage. Among these methods, the last one which is reported in [9] seems to be a suitable candidate for this work. As mentioned in Section 1.1, since the RF energy harvester with a several-stage voltage doubler rectifier has been utilized to generate the $0.4V$ input voltage for the boost DC-DC converter in this work, we can add some additional stages to create a voltage doubler rectifier. These additional stages of the voltage doubler rectifier are only used for the startup mechanism. After the startup phase, these stages will be switched off.

The specific design of the startup mechanism is not included in this work. From the simulation results shown in Chapter 6, it can be observed that the minimum supply voltage for the control system of the boost DC-DC converter designed in this work is about $0.7V$. Therefore, the whole design of this thesis project is based on the assumption that the load capacitor has had an initial voltage of $0.7V$. The startup mechanism can be studied in future work.

2.2 Power Loss Mechanism

The power conversion efficiency is normally the major consideration for DC-DC converters, especially for those found in portable devices where prolonging the battery life is a key goal [10]. In this design, since the target application of the boost DC-DC converter is in an RF energy harvesting system, the power conversion efficiency is definitely the principal specification. To achieve maximum power conversion efficiency in a DC-DC converter, it is very helpful to understand the power loss mechanisms. If all the main sources of power losses in a DC-DC converter are clearly known, the proper efforts can be made on optimization of the power conversion efficiency.

The power losses of a DC-DC converter system can generally be divided into two categories, which are the conduction losses and the switching losses. The conduction losses are induced by the mean DC current flowing through the parasitic or equivalent resistances. The switching losses are induced by the periodical variations of the current through or the voltage across the components such as the inductor or the power switches of the converter. As mentioned in [11], it is usually easy to calculate the conduction losses, since only the average current and the resistances are required to know. But for the switching losses, because they depend on many variables, any calculations are only a rough approximation and can be far away from the real value found in the actual design, particularly at high switching frequencies [11]. Therefore, only five fundamental power losses are normally considered during the practical analysis of the power loss mechanism of a DC-DC converter. The five power losses are: (1) the conduction loss of the power switches; (2) the switching loss of the power switches; (3) the conduction loss of the inductor DCR (DC resistance); (4) the loss of the load capacitor ESR (equivalent series resistance); (5) the power consumption of the control circuit.

For a synchronous DC-DC converter in CMOS technology, the conduction losses of

the power switches are caused by the turn-on resistances of the MOSFET transistors. When there are currents flowing through the closed power switches, energy will be consumed by the MOSFET turn-on resistances. The conduction losses of the low-side and the high-side MOSFET power switches can be expressed as:

$$P_{\mathrm{C\_lsw}} = \frac{R_{\mathrm{on\_lsw}}}{T}\int_0^{t_{\mathrm{lsw}}} i_{\mathrm{L}}^2(t)\,dt \tag{2.10}$$

$$P_{\mathrm{C\_hsw}} = \frac{R_{\mathrm{on\_hsw}}}{T}\int_0^{t_{\mathrm{hsw}}} i_{\mathrm{L}}^2(t)\,dt\ , \tag{2.11}$$

in which $R_{\mathrm{on\_lsw}}$ and $R_{\mathrm{on\_hsw}}$ are the MOSFET turn-on resistances; t_{lsw} and t_{hsw} represent the durations of the time when the low-side switch and high-side switch are closed, respectively; i_{L} is the inductor current; T is the switching period of the DC-DC converter. According to Equation 2.10 and 2.11, it can be seen that the conduction losses of the power switches are only determined by the inductor current and the MOSFET turn-on resistance. Since the inductor current is related to many other variables such as the switching frequency or input/output voltage, the available method to reduce this loss is to reduce the turn-on resistance of the MOS power switch. The general equation of the MOSFET turn-on resistance (R_{on}) can be expressed as [12]:

$$R_{\mathrm{on}} = \frac{1}{\mu C_{\mathrm{ox}}\frac{W}{L}(V_{\mathrm{gs}}-V_{\mathrm{th}})} \tag{2.12}$$

Assuming the gate driving voltage (V_{gs}) is limited by supply, which means no voltage boosting technique is used, the only variation that can be used to adjust the turn-on resistance is the aspect ratio (W/L). Therefore, using transistors with large aspect ratios is the only way to reduce the turn-on resistances thus reducing the conduction losses of the MOSFET power switches.

Compared to the conduction losses, the switching losses of the power switches are less intuitive. Since the MOSFET power switches require some time to change their on/off states, some energy will be consumed during the transition time. This loss mechanism can be explained with the aid of Figure 2-8. As shown in Figure 2-8, due to the overlap of the non-zero current and the non-zero voltage during the transition time, energy will be lost on the transistor. Figure 2-8a shows the best-case scenario, in which, the voltage across the transistor and the current through the transistor start changing simultaneously and also reach their final values simultaneously. Figure 2-8b shows the worst-case scenario (which is closer to reality) [11], in which, the voltage or the current starts changing until the other one reaches its final value. The switching loss of the power switch in the best case or the worst case can be expressed by Equations 2.13 and 2.14.

$$P_{\mathrm{S\_sw\_b}} = \frac{1}{T}\left(\int_0^{t_{\mathrm{o}}} V_{\mathrm{ds}}I_{\mathrm{ds}}dt + \int_0^{t_{\mathrm{c}}} V_{\mathrm{ds}}I_{\mathrm{ds}}dt\right) \tag{2.13}$$

$$P_{\mathrm{S\_sw\_w}} = \frac{1}{T}\left(\int_0^{t_{\mathrm{cr}}+t_{\mathrm{vf}}} V_{\mathrm{ds}}I_{\mathrm{ds}}dt + \int_0^{t_{\mathrm{vr}}+t_{\mathrm{cf}}} V_{\mathrm{ds}}I_{\mathrm{ds}}dt\right)\ , \tag{2.14}$$

in which T is the switching period of the DC-DC converter. In Equations 2.13 and 2.14, since only the transition times ($t_{\mathrm{o}}, t_{\mathrm{c}}, t_{\mathrm{cr}}, t_{\mathrm{vf}}, t_{\mathrm{vr}}, t_{\mathrm{cf}}$) can be independently adjusted, the

available way to reduce the switching losses of the power switches is to reduce these transition times. However, in order to further reduce the transition times, larger buffers are required to drive the power switches. The larger buffer with stronger driving ability will also consume more energy, which perhaps leads to a result opposite to what is designed. Therefore, the trade-off between the transition time of the power switch and the driving ability of the buffer should be considered when the switching losses of the power switches are improved.

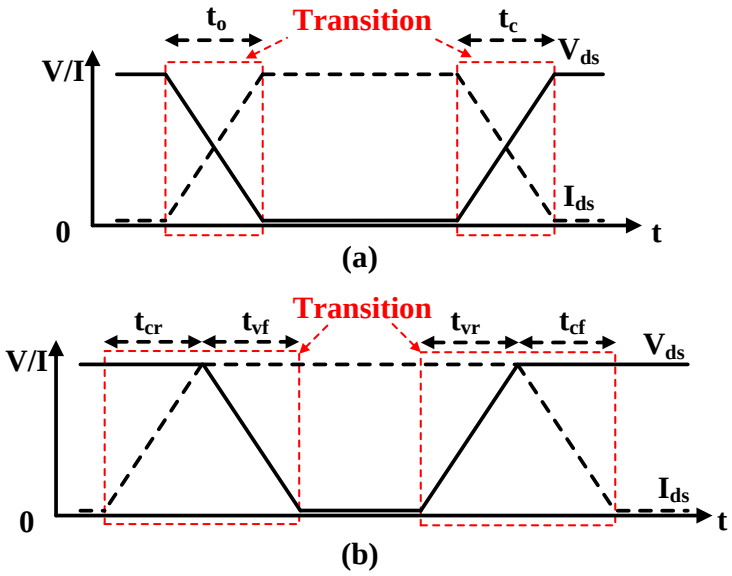

Figure 2-8: Switching waveforms of the transistor
(a) in the best-case scenario; (b) in the worst-case scenario.

The conduction loss of the inductor is caused by the DC resistance (DCR) of the inductor. The inductor DCR is actually the winding resistance which is determined by the size and structure of the inductor. When there is current flowing through the inductor, energy will be consumed on the inductor due to the DCR. This loss can be expressed as:

$$P_{\mathrm{L\_DRC}} = \frac{R_{\mathrm{dc\_L}}}{T}\int_0^T i_L^2(t)\,dt \ , \tag{2.15}$$

in which $R_{\mathrm{dc\_L}}$ is the inductor DCR; i_{L} is the inductor current and T is the switching period of the DC-DC converter. It is obvious that the available way to reduce the conduction loss of the inductor is using an inductor with a low DCR.

The loss mechanisms generated by the load capacitor are complex. As mentioned in [10], for simplifying the loss model, the actual losses including the contact resistance, leakage and dielectric losses are lumped together into an individual power-loss element named “equivalent series resistance” (ESR). The loss of the ESR can represent the overall power losses of the load capacitor, which can be expressed as:

$$P_{\mathrm{C\_ESR}} = \frac{R_{\mathrm{C_{ESR}}}}{T}\int_0^T i_{\mathrm{C}}^2\,(t)dt \tag{2.16}$$

in which $R_{\mathrm{C\_ESR}}$ is the ESR of the load capacitor , T is the switching period of the

DC-DC converter and i_C is the current flowing through the load capacitor ESR. i_C can be expressed as:

$$i_C(t) = i_{load}(t) - i_L(t) \ , \tag{2.17}$$

in which i_{load} is the load current and i_L is the inductor current. Since manufactures usually offer data about ESR values of their capacitors, a capacitor with a low ESR can be used in a DC-DC converter in order to reduce the loss of the load capacitor.

The loss mechanisms mentioned above are all caused by the components (inductor, power switches and load capacitor) in the power plant of the DC-DC converter. Besides, the circuit blocks in the control system such as the comparator, amplifier or digital circuit, will also consume some power to maintain the operation of the DC-DC converter. Normally, the DC-DC converter works in the high load current condition, which means that the load current is much higher than the driving current of the control system. In this case, the power consumption of the control system is generally neglected. But when the load current of the DC-DC converter becomes very low, the power consumption of the control system will take a great part of the total loss. In this case, ultra-low power technology should be used for the circuit design of the control system.

After the analyses of the five fundamental loss mechanisms of the DC-DC converter, the total power loss of the converter can be approximated by the sum of these losses:

$$P_{loss} = P_{C\_hsw} + P_{C\_lsw} + P_{S\_hsw} + P_{S\_lsw} + P_{DCR\_L} + P_{ESR\_C} + P_{control} \tag{2.18}$$

Moreover, the output power (P_{out}) is usually easy to obtain by the product of the output voltage and the load current. Therefore, the power conversion efficiency (η) of the DC-DC converter can be expressed as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out}+P_{loss}} \tag{2.19}$$

2.3 Preliminary Design of the Power Plant

For the design of a DC-DC converter, the first step is normally to determine the parameters of the components in the power plant, which include the sizes of the power switches, the inductance of the inductor and the capacitance of the load capacitor. Compared to the design of the control system, the importance of this step seems to be often neglected by designers, as few discussions about this step have been reported [13] [14]. In fact, since the majority of the power loss of a DC-DC converter stems from the components in the power plant rather than the circuit of the control system, an elaborate design of the power plant will make much contribution to achieving a high efficient DC-DC converter design. In this section, the preliminary design of the power plant of the boost DC-DC converter for this project will be described.

The design specifications of this work have been listed in Table 1.1 in Section 1.3. The design of the power plant should be based on these system parameters including the

input voltage (V_{in}), the output voltage (V_{out}), the output voltage ripple ($V_{\text{o\_ripple}}$) and the load current (I_{load}). At first, let us analyze and roughly calculate the waveform of the inductor current. Since the pulse frequency modulation (PFM) adaptive on-time/off-time (AOOT) control technique is applied in this work, the boost converter will work in DCM and the switching period of the boost converter will be changed with the variation of the load current. If the input voltage and the output voltage are fixed, the on-time and the off-time will be constant. When the boost converter works in the maximum load current, the switching period will be shortest due to the minimum dead time. When the boost converter works in the light load current, then the switching period will be increased by increasing the dead time. The detailed working principle of the control technique will be explained in Section 3.4.

For high power efficiency, the duration of the dead-time is expected to be as short as possible when the boost converter works with the maximum load current. In this work, the maximum load current is $10mA$. Therefore, when the boost converter works with a $10mA$ load current, in the ideal case, the dead-time should be zero. At this moment, the boost converter works at the boundary of DCM and CCM. The waveform of the inductor current is shown in Figure 2-9. Then the average value and the peak value of the inductor current can be calculated as follows.

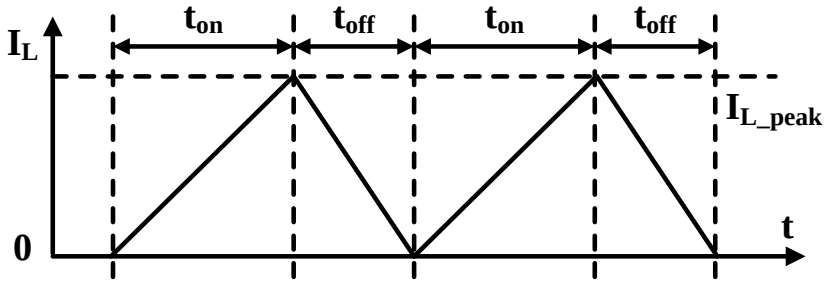

Figure 2-9: Waveform of the inductor current for the boost converter working in the boundary of CCM and DCM.

The output power of the boost converter can be derived from Equation 2.20.

$$P_{\text{out}} = V_{\text{out}} \cdot I_{\text{load}} = 1V \cdot 10mA = 10mW \tag{2.20}$$

If we assume the power conversion efficiency (η) is 95%, then the input power of the boost converter is:

$$P_{\text{in}} = \frac{P_{\text{out}}}{\eta} = \frac{10mW}{0.95} \approx 10.53mW \tag{2.21}$$

Meanwhile, the input power is also equal to the product of the input voltage and the average input current. For a boost DC-DC converter, since the inductor is always connected to the input terminal, the average inductor current is equal to the average input current. Hence, the average value of the inductor current ($i_{\text{L\_ave}}$) is:

$$i_{\text{L\_ave}} = i_{\text{in\_ave}} = \frac{P_{\text{in}}}{V_{\text{in}}} = \frac{10.53mW}{0.4V} = 26.325mA \tag{2.22}$$

If the waveform of the inductor current is triangular, as shown in Figure 2-9, the relationship between the average value of the inductor current ($i_{\text{L\_ave}}$) and the peak value of the inductor current ($I_{\text{L\_peak}}$) can be expressed by Equation 2.23.

$$i_{\text{L\_ave}} = \int_0^T i_L(t) \cdot dt = \frac{1}{2} I_{\text{L\_peak}} \tag{2.23}$$

So, the peak value of the inductor current is:

$$I_{\text{L\_peak}} = 2 \cdot i_{\text{L\_ave}} = 52.65mA \tag{2.24}$$

This result is obtained by the mathematical calculation based on many ideal assumptions. In reality, due to the un-ideal factors such as the voltage drops over the inductor and the power switches, the peak value of the inductor current should be a little higher than the calculation result.

The sizes of the MOSFET power switches can be determined from the peak value of the inductor current and the acceptable voltage drops across over the power switches. Apart from Equation 2.12, the turn-on resistance of the MOSFET power switches can also be expressed by:

$$R_{\text{on}} = \frac{V_{\text{ds}}}{I_{\text{ds}}} \tag{2.25}$$

Therefore, if we know the maximum current flowing through the switch transistor and its acceptable maximum crossover voltage drop, the aspect ratio (W/L) of the transistor can be obtained. For the power switches of the DC-DC converter, the maximum current is equal to the peak value of the inductor current. In this work, the calculation result of the peak value of the inductor current is $52.65mA$. But in consideration of the un-ideal factors, this value can be roughly approximated as $60mA$. The acceptable maximum voltage drop across over the power switch ($V_{\text{ds\_max}}$) is expected to be 20mV in this work. Then, the aspect ratios of the NMOS and the PMOS power switch transistors can be obtained by Equations 2.26 and 2.27.

$$\left(\frac{W}{L}\right)_n = \frac{I_{\text{L\_peak}}}{\mu_n C_{\text{ox}}(V_{\text{gsn}} - V_{\text{thn}}) V_{\text{ds\_max}}} \tag{2.26}$$

$$\left(\frac{W}{L}\right)_p = \frac{I_{\text{L\_peak}}}{\mu_p C_{\text{ox}}(V_{\text{gsp}} - V_{\text{thp}}) V_{\text{ds\_max}}} \ , \tag{2.27}$$

in which V_{gsn} and V_{gsp} are the gate voltages of the power switches, which are both equal to $1V$ in this design; μ_n, μ_p, C_{ox}, V_{thn} and V_{thp} are the technological parameters, which can be found in the technical files. After a rough calculation, the aspect ratios of the power switches are:

$$\left(\frac{W}{L}\right)_n \approx \frac{60mA}{200\mu A/V^2 \cdot (1V - 0.55V) \cdot 20mV} \approx 3.3 \times 10^4 \tag{2.28}$$

$$\left(\frac{W}{L}\right)_p \approx \frac{60mA}{70\mu A/V^2 \cdot (1V - 0.55V) \cdot 20mV} \approx 11 \times 10^4 \tag{2.29}$$

The mathematic derivation only provides an elementary estimation in order to simplify the design work. The final decision of the aspect ratios of the power switches should be made on the base of the simulation results and some other considerations. In this work, based on the simulation results of a parameter sweep and under the consideration of layout simplification, the sizes of the low-side NMOS power switch and the high-side PMOS power switch are determined. The parameters of the power switches are listed in Table 2-1.

Table 2-1: Parameters of the MOSFET power switches

	Width (W)	Length (L)	Aspect ratio (W/L)
Low-side NMOS power switch	$3.584mm$	$100nm$	3.584×10^4
High-side PMOS power switch	$7.168mm$	$100nm$	7.168×10^4

The inductance of the inductor in the power plant is generally related to the switching frequency of the DC-DC converter. In general, increasing the inductance of the inductor can reduce the switching frequency of the DC-DC converter. Therefore, during the selection of an inductor for the DC-DC converter, the issue of the switching frequency should be taken into consideration. The relationship between the inductance of the inductor (L) and the switching frequency (f_{sw}) of the boost DC-DC converter designed in this work can be obtained from the following derivation.

According to Equation 2.1, we can get Equation 2.30 and 2.31 which express the voltage and current conditions of the inductor during the on-time phase (2.30) and off-time phase (2.31).

$$V_{\mathrm{in}} = L \cdot \frac{I_{\mathrm{L\_peak}}}{t_{\mathrm{on}}} \tag{2.30}$$

$$V_{\mathrm{out}} - V_{\mathrm{in}} = L \cdot \frac{I_{\mathrm{L\_peak}}}{t_{\mathrm{off}}} \tag{2.31}$$

Since the input and output voltage of the boost converter are known, the ratio of the on-time (t_{on}) and the off- time (t_{off}) can be determined.

$$\frac{t_{\mathrm{on}}}{t_{\mathrm{off}}} = \frac{V_{\mathrm{out}} - V_{\mathrm{in}}}{V_{\mathrm{in}}} = \frac{1V - 0.4V}{0.4V} = \frac{3}{2} \tag{2.32}$$

When the boost converter works at the boundary of DCM and CCM, the switching period (T) of the boost converter is equal to the sum of the on-time and the off-time ($T = t_{\mathrm{on}} + t_{\mathrm{off}}$). So we can get:

$$t_{\mathrm{on}} = \frac{3}{5}T \tag{2.33}$$

$$t_{\mathrm{off}} = \frac{2}{5}T \tag{2.34}$$

According to Equations 2.30 and 2.33, we can obtain:

$$L \cdot f_{\mathrm{sw}} = \frac{3 \cdot 0.4V}{5 \cdot 60mA} = 4\ \mu H/MHz\ , \tag{2.35}$$

in which f_{sw} is the switching frequency, which is equal to the reciprocal of the switching period ($f_{\mathrm{sw}} = 1/T$). Hence, Equation 2.35 shows the relationship between the inductor inductance (L) and the switching frequency (f_{sw}) in this work. It means if a $1\mu H$ inductor is used in the boost DC-DC converter, the maximum switching frequency of the boost converter will be about $4MHz$; if a $10\mu H$ inductor is used, the maximum switching frequency will be about $400kHz$.

In this work, since there is not any specific requirement or limitation on the switching frequency, the determination of the inductor inductance and the switching frequency will be made in consideration of the power conversion efficiency. As discussed in Section 2.2, the inductor inductance and the switching frequency will affect the power conversion efficiency mainly through changing the conduction loss of the inductor DCR and the switching losses of the power switches. Therefore, the inductor inductance will be determined in order to achieve the minimum power losses mentioned above.

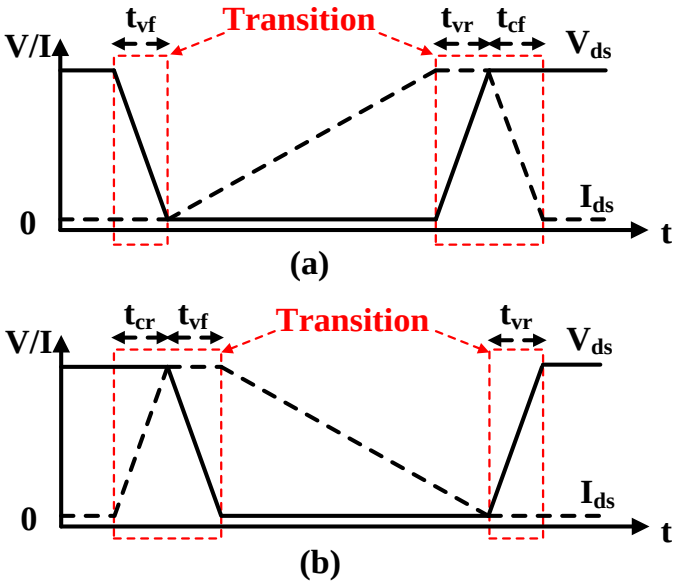

Figure 2-10: Switching waveforms of the transistor
(a) in the best-case scenario; (b) in the worst-case scenario.

The conduction loss of the inductor DCR and the switching loss of the power switch are expressed by Equations 2.15 and 2.14 (assuming the worst-case scenario). But for the boost DC-DC converter designed in this work, the voltage and current waveforms of the two power switches are not similar to what was shown in Figure 2-8b. For the low-side NMOS power switch, the initial current through the switch is close to zero at the moment when it is turned on. At the moment when the switch is turned off, the initial current

through the switch is equal to the peak current of the inductor which is about $60mA$ given by a previous calculation. For the high-side PMOS power switch, the initial current through the switch is equal to the peak current of the inductor (60mA) when it is turned on. And the initial current through the switch is about zero when it is turned off. Therefore, the waveforms of the two power switches are shown in Figure 2-10. According to Equation 2.16, the switching losses of the low-side NMOS power switch and the high-side PMOS power switch can be expressed as:

$$P_{\text{S\_nsw}} = \frac{1}{T}\left(\int_0^{t_{\text{cr}}+t_{\text{vf}}} V_{\text{ds}} I_{\text{ds}} dt + \int_0^{t_{\text{vr}}+t_{\text{cf}}} V_{\text{ds}} I_{\text{ds}} dt\right)$$

$$= \frac{1}{2} V_{\text{ds}} I_{\text{ds}} (t_{\text{vr}} + t_{\text{cf}}) \cdot f_{\text{sw}} \tag{2.36}$$

$$P_{\text{S\_psw}} = \frac{1}{T}\left(\int_0^{t_{\text{cr}}+t_{\text{vf}}} V_{\text{ds}} I_{\text{ds}} dt + \int_0^{t_{\text{vr}}+t_{\text{cf}}} V_{\text{ds}} I_{\text{ds}} dt\right)$$

$$= \frac{1}{2} V_{\text{ds}} I_{\text{ds}} (t_{\text{cr}} + t_{\text{vf}}) \cdot f_{\text{sw}} \tag{2.37}$$

Table 2-2: Candidates of the inductors for the comparison

Production No.	L	R_{dc} (Max.)
CLF6045T-100M	$10\mu H$	$45.6m\Omega$
CLF7045T-1R0N	$1\mu H$	$12.48m\Omega$
VLB7050HT-R11M	$110nH$	$0.286m\Omega$

Table 2-3: Calculation results of the power losses with different inductors

Production No.	$P_{\text{DCR\_L}}$	$P_{\text{S\_nsw}}$	$P_{\text{S\_psw}}$	P_{sum}
CLF6045T-100M	$30.83\mu W$	$0.48uW$	$0.72uW$	$32.03uW$
CLF7045T-1R0N	$8.4\mu W$	$4.8uW$	$7.2uW$	$20.4uW$
VLB7050HT-R11M	$0.19\mu W$	$43.2uW$	$64.8uW$	$108.19uW$

Based on Equation 2.15, 2.36 and 2.37, a comparison can be made to determine which value is the best choice for the inductance of the inductor. The candidates of the comparison are three inductors of TDK Company [15]. The production number and their parameters are shown in Table 2-2. After substituting these parameters into Equations 2.15, 2.36 and 2.47, we can get the calculation results that are shown in Table 2-3. In this design, V_{ds} of the low-side NMOS transistor is about $0.4V$ and V_{ds} of the high-side

PMOS transistor is about $0.6V$. I_{ds} of these two transistors are both equal to $60mA$. The sum of t_{vr} and t_{cf} for the low-side NMOS transistor and the sum of t_{cr} and t_{vf} of the high-side NMOS transistor are both set to be about 100ps.

From the calculation results, it can be concluded that the inductor with a $1\mu H$ inductance is relatively the best choice in this design. Although a larger inductor will effectively reduce the switching losses of the power switches, the conduction loss of the inductor will be seriously increased. A smaller inductor can dramatically decrease the conduction loss of the inductor, but the switching losses of the power switches will badly arise as well. Therefore, in this work, we finally choose "*CLF7045T-1R0N"* [16] as the inductor in the boost DC-DC converter. According to the SPICE netlist provided from the TDK website, the equivalent schematic model of the inductor is shown in Figure 2-11.

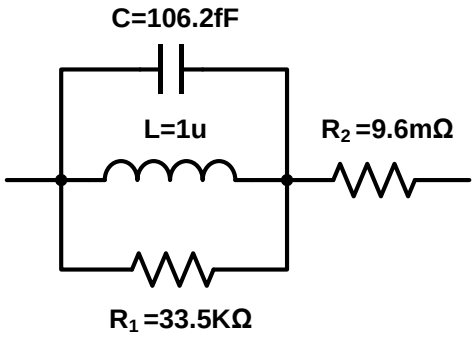

Figure 2-11: Equivalent schematic model of the inductor "CLF7045T-1R0N".

When the inductance of the inductor is decided to be $1\mu H$, according to Equation 2.33, 2.34 and 2.35, we can obtain that the ideal values of the switching period, the on-time and the off-time of the boost converter should be:

$$T = \frac{1}{f_{\mathrm{sw}}} = \frac{L}{4\ \mu H/MHz} = 250ns \tag{2.38}$$

$$t_{\mathrm{on}} = \frac{3}{5}T = 150ns \tag{2.39}$$

$$t_{\mathrm{off}} = \frac{2}{5}T = 100ns \tag{2.40}$$

For the boost DC-DC converter designed in this work, the selection of the load capacitor is only determined by the limitation on the output voltage ripple. When the boost DC-DC converter works in DCM or at the boundary of DCM and CCM, the output voltage ripple ($V_{\mathrm{o\_ripple}}$) can be written as:

$$V_{\mathrm{o\_ripple}} = \frac{i_{\mathrm{load}} \cdot (t_{\mathrm{on}} + t_{\mathrm{dead}})}{C_{\mathrm{load}}} \tag{2.41}$$

In this work, when the load current of the boost converter is $10mA$, the maximum output voltage ripple is expected to be lower than 10mV, ($V_{\mathrm{o\_ripple}} < 10mV$). Moreover, in the

ideal case, the converter works at the boundary of DCM and CCM, which means the dead time (t_{dead}) is zero. Therefore, we can derive:

$$C_{\text{load}} > \frac{t_{\text{on}} \cdot i_{\text{load}}}{V_{\text{o\_ripple}}} > 150nF \tag{2.42}$$

But in the real implementation of the control technique of the boost converter, the dead-time is larger than zero when the load current is $10mA$. (The detailed explanation of the control technique applied in this design will be given in the next chapter.) As a result, to guarantee the requested output voltage ripple, a little larger capacitor should be selected for the load capacitor. Finally, the capacitance of the load capacitor is determined to be $220nF$. Since the equivalent schematic model of a capacitor is like what will be shown in Figure 2-12, the parasitic inductance of the load capacitor will introduce some spikes to the output of the DC-DC converter. Therefore, to reduce this effect, some small capacitors in parallel can be used to implement the load capacitor. In this work, ten $22nF$ capacitors are used to achieve the total capacitance of the load capacitor(s) is $220nF$. To reduce the power loss of the load capacitor ESR, a capacitor with a low ESR should be chosen. Finally, the capacitor *"C0603JB0J223K030BC"* [17] with a $22nF$ capacitance is applied in this work. Based on the SPICE netlist provided by TDK, the equivalent schematic model of the capacitor is shown in Figure 2-12.

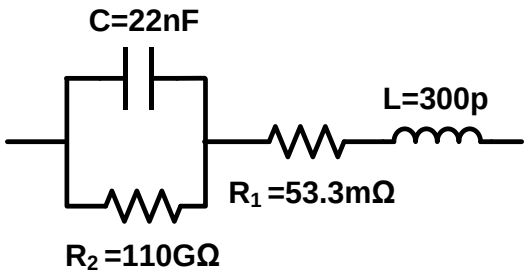

Figure 2-12: Equivalent schematic model of the capacitor "C0603JB0J223K030BC".

So far, the preliminary design of the power plant of the boost DC-DC converter has been finished. Based on the conclusions made above, the control system of the boost DC-DC converter can be designed in the next step. The discussion on the design of the control system will be given in following chapters.

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[16] URL: http://product.tdk.com/inductor/ind/detailed_information.php?lang=en&ref=jp&part_no=CLF7045T-1R0N

[17] URL: http://product.tdk.com/capacitor/mlcc/detailed_information.php?lang=en&ref=jp&part_no=C0603JB0J223K030BC

Chapter 3

Control System

3.1 Introduction to This Chapter

In a DC-DC converter system, the power switches in the power plant play very important roles. Due to their dynamic switching (alternatively open and close), the topology of the components (inductors or capacitors) in the power plant is periodically changed thus making the DC-DC converter realize its functionality (step-up or step-down voltage conversion). The working principle of an inductive DC-DC converter has been described in Section 2.1. As mentioned before, an inductor is controlled by two power switches to be connected to the input and output terminal. Hence the energy coming from the input source is periodically stored in the inductor and then released to the load. In the ideal case when all system parameters including the input voltage, the output voltage and the load current are fixed, two pulse signals with a constant frequency and a fixed duty cycle can be used to drive the power switches. But in reality, since the system parameters are always be changed by some effects, a control system is required to automatically adjust the duty cycles or the frequencies of the drive signals.

How to design a robust control system with lower power consumption has always been the crucial issue for the research in this field. Until now, many kinds of control methodologies have been proposed, each of which focus on solving different problems in different applications and have corresponding advantages and disadvantages. If we make a general classification of these methods, they can be sorted into two categories. One is the conventional pulse width modulation (PWM) control which includes the voltage-mode control (VMC) and the current-mode control (CMC). The other one is the pulse frequency modulation (PFM) control in which the frequencies of the drive signals are dependent on the system parameters and the propagation delays [1]. Since most PFM control methods utilize the output ripple voltage of the converter for pulse modulation, the PFM control is also named ripple-based control.

Later in Section 3.2, a short introduction to VMC and CMC as well as their characteristics and limitations will be given. The PFM control technique and some general implementation methods will be described in Section 3.3. The specific control

technique applied in this work will be presented in Section 3.4 along with the explanation about some improvement techniques. The approaches which can be used to generate and control the on-time and the off-time signals will be introduced in Section 3.5. Finally, an advanced technique which is applied to achieve the zero-current switching (ZCS) for improving the efficiency of the DC-DC converter will be discussed in Section 3.6. If there is not any specific notification, all the control methods will be discussed for the boost DC-DC converter.

3.2 PWM Control

Voltage-mode control (VMC) and current-mode control (CMC) are two kinds of conventional PWM control methods which have been widely used for controlling DC-DC converters. VMC was first proposed and was applied on the first IC switching controller by Silicon General (later LinFinity, then Microsemi) in 1976 [2]. The basic operating principle of the VMC is that the duty cycles of the drive signals to control the power switches are proportional to the "control voltage" which is actually the difference between the output voltage of the converter and the regulated (reference) voltage. Figure 3-1 shows a typical implementation of a VMC boost DC-DC converter. Therein, the error amplifier (EA) is used to provide a control voltage V_c to the PWM comparator (Comp). The PWM comparator generates the drive signals to the power switches (Sw_L and Sw_H) via the gate drive logic circuit by comparing the control voltage (V_c) with a fixed voltage ramp (V_{ramp}) generated from an extra clock. The part in the dashed box is a Type 3 (PID) compensation circuit for the frequency compensation. The resistor R_{f2} works together with R_{f1} for biasing the input of the error amplifier.

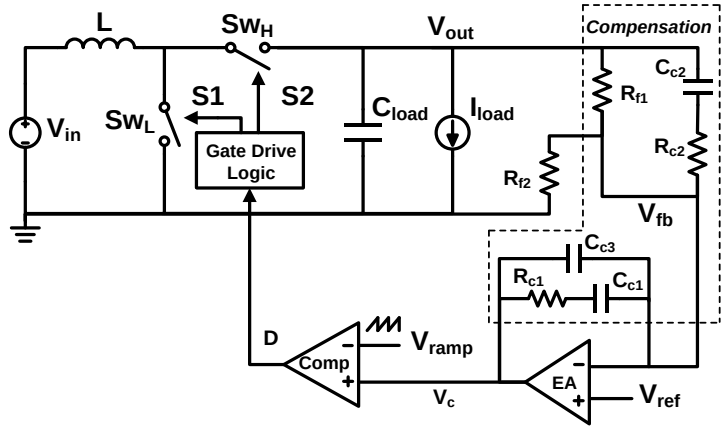

Figure 3-1: Boost DC-DC converter with a typical CCM VMC control.

The generation and control of the PWM signal can be illustrated by the waveforms shown in Figure 3-2. If the output voltage (V_{out}) drops for some reason, the control

voltage (V_c) generated by the error amplifier will be increased due to the larger difference between the feedback voltage (V_{fb}) and the reference voltage (V_{ref}). The increment of V_c will lead to a larger duty cycle. Due to Equation 2.8, the ratio of the input voltage over the output voltage is equal to $(1-D)$ for a boost converter working in the continuous- conduction mode (CCM). Hence, when the input voltage is fixed, the output voltage of the boost converter will be pulled up by the increment of the duty cycle. If the output voltage rises, the opposite operation will occur. This mechanism ensures the output voltage is always close to the reference voltage thus achieving a good output voltage regulation for the boost DC-DC converter.

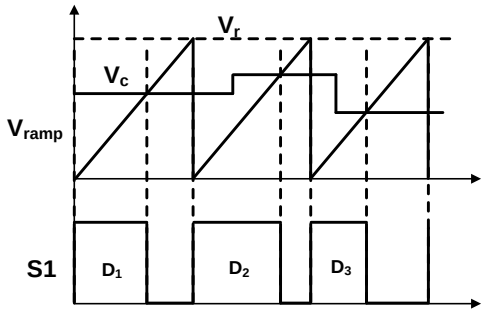

Figure 3-2: PWM signal generation by the PWM comparator.

The small-signal transfer function, which is typically defined by the state-space averaging method, is widely used to analyze the dynamic behavior, frequency response and loop stability of a DC-DC converter [3]. A lot of studies have been done on the mathematical analysis [4] [5] [6] [7]. In this work, the complex formula derivations and mathematical analyses will not be studied. We just cite some conclusions from previous studies and use them to discuss the characters of different control methods.

When doing small-signal analysis on a DC-DC converter, the entire converter system is usually divided into some parts and the total transfer function of the entire system is equal to the product of all the transfer functions of each part. For the CCM VMC boost converter shown in Figure 3-1, the entire converter system can be divided into three parts, which are consecutively the PWM signal generator, the power plant and the compensation block. According to the waveforms shown in Figure 3-2, the transfer function of the PWM signal generator becomes:

$$\frac{\hat{d}}{\hat{v}_c} = \frac{1}{V_r} \tag{3.1}$$

It means the small-signal transfer function of this part is independent of the frequency. So it can be ignored during the dynamic analysis of the frequency response.

The transfer function of the power plant which is also named as duty-cycle-to-output transfer function can be expressed as:

$$\frac{\hat{V}_{out}}{\hat{d}} = \frac{V_{out}^2}{V_{in}} \frac{\left(1+\frac{s}{\omega_{z1}}\right)+\left(1-\frac{s}{\omega_{RHP\_z}}\right)}{1+\frac{s}{\omega_0 \cdot Q}+\frac{s^2}{\omega_0^2}} \tag{3.2}$$

in which,

$$\omega_{z1} = \frac{1}{C \cdot R_{ESR\_C}} \tag{3.3}$$

$$\omega_{RHP\_z} = \frac{R_{load}}{L} \cdot \left(\frac{V_{in}}{V_{out}}\right)^2 \tag{3.4}$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C_{load}}} \cdot \frac{V_{in}}{V_{out}} \tag{3.5}$$

$$Q = \omega_0 \cdot C_{load} \cdot R_{ESR\_C} \tag{3.6}$$

The detailed mathematical derivation of these equations can be found in other literatures such as [6] [7]. Here, we just choose the most classical expressions in which some parasitic resistances and capacitances, such as the inductor parasitic resistance, the inductor parasitic capacitance, power switch MOS transistor parasitic resistance, etc., have been ignored due to their relatively small value compared to the dominant resistances (load resistor) and capacitances (load capacitor) in the entire system. From the small-signal transfer function of the power plant (Equation 3.2), we can see a double-pole ω_0 (Equation 3.5), a zero ω_{z1} caused by the ESR of the load capacitor (Equation 3.3) and a Right-Half Plane (RHP) zero ω_{RHP_z} (Equation 3.4).

The RHP zero exists in any kinds of fixed frequency CCM boost DC-DC converter. It is an unexpected zero, because in a mathematical explanation, the phase decreases with increasing gain at this point, which makes it is very difficult to compensate the entire control loop with adequate phase margin [8]. The effect of the RHP zero can also be intuitively explained as below. If the output of the converter suddenly drops down which means more energy is required to charge the load, the duty cycle will be increased thus providing a longer on-time for the inductor to store more energy. But for a boost converter, the energy is delivered to the load during the off-time. Although more energy has been stored in the inductor during the on-time, there is now a smaller off-time available for the inductor to deliver stored energy to the output. Therefore, the output of the converter may even drop further. It is difficult to cancel the RHP zero in a boost converter system. The only way to eliminate its effect is to move the RHP zero far away from the switching frequency [2]. According to Equation 3.4, in a specific application, in which V_{in}, V_{out} and R_{load} are fixed, the only way to increase the value of the RHP zero is to reduce the inductor. But in most cases, a smaller inductor means higher switching frequency. So the effect of the RHP zero gives much trouble to a design of a fixed frequency boost converter.

The last part of the entire converter system is the compensation block. This part is used to compensate the entire control loop for loop stability. The general criterion for stabilizing the loop of any DC-DC converter is to set the crossover frequency ($\text{Gain} = 0$) at about $1/10$ to $1/5$ of the switching frequency and to ensure a straight line (on a “log Gain” versus “log Frequency” plot) in “-20db” slope at the crossover frequency with enough phase margin. For this purpose, a Type 3 (PID) compensation circuit is applied

and its Bode diagram (magnitude only) is shown in Figure 3-3. This compensation circuit can provide a low frequency zero to compensate the double-pole existing in the power plant. Figure 3-3 also exhibits the bode-diagram of the entire converter system. It can be seen that, the loop stability of this kind of DC-DC converter can be guaranteed by a correct setting of the parameters of the power plant and the compensation block.

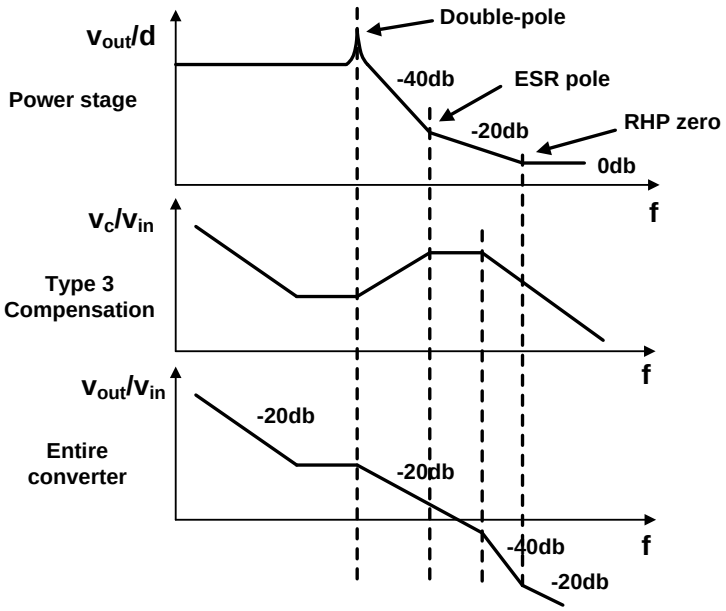

Figure 3-3: Compensation for the loop stability of a VMC boost DC-DC converter.

In a VMC DC-DC converter system, the ramp signal used for the PWM comparator is generated by an extra block which will consumes additional energy. Then, an idea came, that is, whether an intrinsic signal in the DC-DC converter could be used to replace the ramp signal. Accordingly, CMC technique was proposed around 1980 and subsequently widely used [2]. A typical implementation of a CMC boost DC-DC converter is shown in Figure 3-4. The basic working principle of CMC is quite similar to VMC except that the ramp signal used for the PWM comparator is generated by a current sensor which senses the current of the inductor or the power switches. It is just because of this inner current loop that the transfer function of the PWM generation part is dependent on frequency and, as a result, the transfer function of the power plant together with the PWM generation has only a single-pole at the resonant frequency of the load resister and the load capacitor. A detailed expression for the duty-cycle-to-output transfer function is:

$$\frac{\hat{V}_{out}}{\hat{V}_c} = \frac{R_{\text{load}}(1-D)}{2\times R_{\text{ramp}}} \frac{\left(1+\frac{s}{\omega_{z1}}\right)+\left(1-\frac{s}{\omega_{\text{RHP\_z}}}\right)}{1+\frac{s}{\omega_0}} \quad , \tag{3.7}$$

in which,

$$\omega_{z1} = \frac{1}{C\cdot R_{\text{ESR\_C}}} \tag{3.8}$$

$$\omega_{\mathrm{RHP\_z}} = \frac{R_{load}}{L} \cdot \left(\frac{V_{\mathrm{in}}}{V_{\mathrm{out}}}\right)^2 \tag{3.9}$$

$$\omega_0 = \frac{2}{R_{load} \cdot C_{load}} \tag{3.10}$$

From the equations, we can see the RHP zero also exits in this kind of boost converter. So CMC technique does not give any contribution to eliminate the effect of the RHP zero. But because the double-pole in VMC has been replaced by a single-pole in CMC, the compensation block will become simpler. The Type 2 compensation is enough for a CMC DC-DC converter. The Bode diagram (magnitude only) of the entire converter system is shown in Figure 3-5.

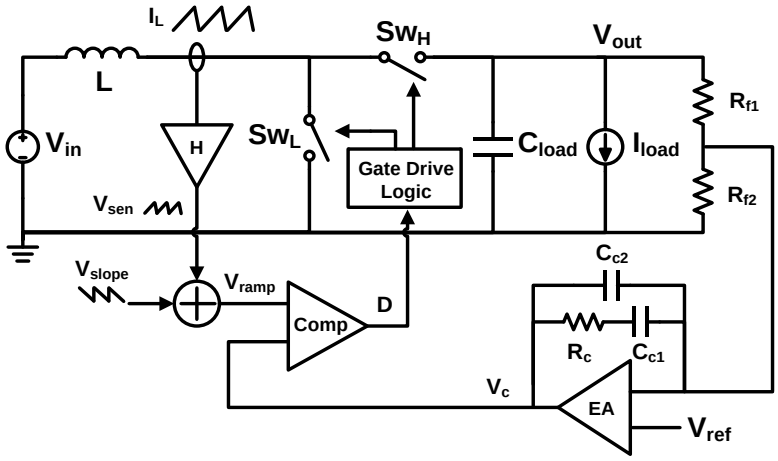

Figure 3-4: Boost DC-DC converter with a typical CCM CMC control.

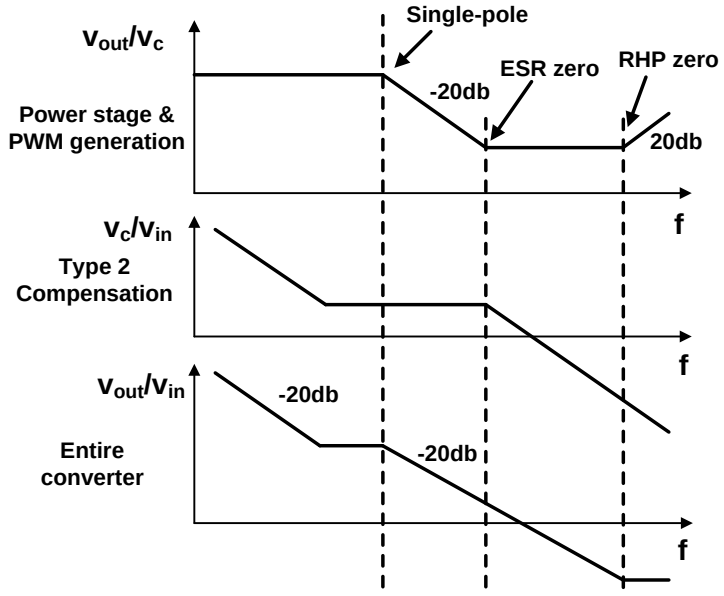

Figure 3-5: Compensation for the loop stability of a CMC boost DC-DC converter.

Besides the RHP zero effect, the CCM CMC DC-DC converter also suffers from Subharmonic Oscillation when the duty cycle exceeds 50%. As shown in Figure 3-6, when the duty cycle is greater than 50% ($D > 50\%$), if the inductor current is suddenly increased by Δi_{L0} due to an unexpected disturbance, this current increment will be magnified after a cycle (grows to Δi_{L1} and Δi_{L2}) thus causing large variation of the duty cycle. In Figure 3-6, D_0 is the duty cycle of a stable DC-DC converter and D_1 is the duty cycle of a DC-DC converter in Subharmonic Oscillation. A traditional method to solve this problem is named "slope compensation", that is adding a fixed slope current onto the sensed ramp current. The circuit implementation of this method has been shown in Figure 3-4 and its theory can be illustrated by Figure 3-7. It should be noted that, the theory illustrated in Figure 3-7 is in current domain but in the implementation circuit shown in Figure 3-4, all current signals are transformed to voltage signals by resistors and then used for the comparison. As shown in Figure 3-7, it can be seen that, any disturbance of the inductor current (Δi_{L0}) will be damped (drops to Δi_{L1} and Δi_{L2}) and the inductor current will finally return to the steady-state condition after several cycles.

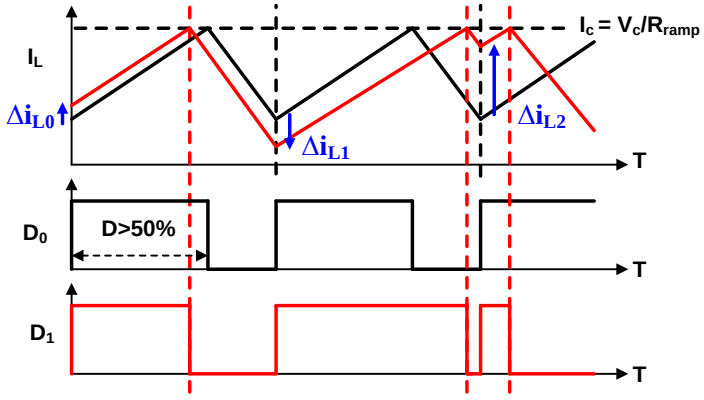

Figure 3-6: Subharmonic oscillation when duty cycle exceeds 50%.

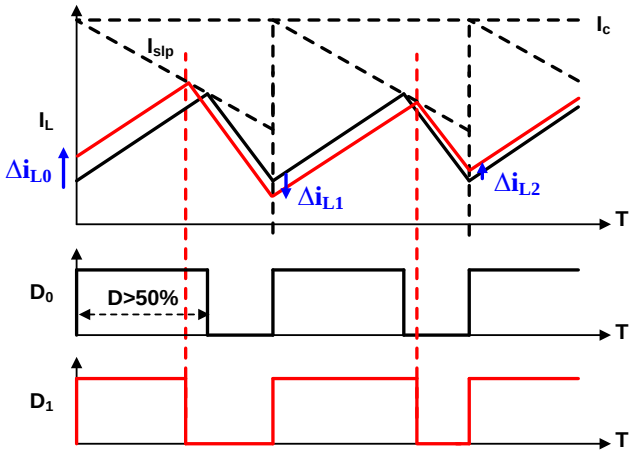

Figure 3-7: Slope compensation to eliminate the subharmonic oscillation.

Although the current-mode control technique can simplify the compensation and make it easier to stabilize the DC-DC converter, there are still some drawbacks of this method. For example, the power consumption cannot be effectively reduced due to the slope compensation current generation block. Moreover, the RHP zero problem also exits in this control technique the same as in the VMC control technique. An effective method to eliminate the RHP zero effect is making the fixed frequency PWM DC-DC converter work in the discontinuous-conduction mode (DCM) (for both VMC and CMC). This conclusion has been demonstrated by many other studies such as [5] [8]. As mentioned in [8], when a DC-DC converter works in DCM, due to a relatively smaller inductor, the RHP zero will be extended to a high frequency which is beyond the switching frequency. Therefore, the RHP zero effect can be neglected in a DCM boost DC-DC converter.

In a DCM DC-DC converter system, the main difference from a CCM DC-DC converter is that one more signal is required to terminate the off-time and start the dead-time. In a CCM converter, the external clock signal is used to synchronously terminate the off-time in the last cycle and start the on-time in the next cycle. The termination of the on-time will be determined by the PWM comparator and meanwhile the off-time will be started. Hence, a CCM converter only needs two signals (the clock signal and the output signal of the PWM comparator) to control the two power switches. But in a DCM converter, the termination of the off-time is no longer determined by the external clock signal. The high-side power switch should be turned off when the inductor current falls down to zero. Therefore, the DCM DC-DC converter needs three signals, in addition to the clock signal and the output signal of the PWM comparator, an extra block is required to sense the inductor current and generate a control signal to terminate the off-time when the sensed inductor current reaches zero. An implementation of the DCM VMC boost DC-DC converter with zero inductor current sensing is proposed in [9]. The schematic of the circuit system is exhibited in Figure 3-8. We can see that except an additional current sensor for the off-time control, all the other blocks are the same as the CCM VMC boost converter system.

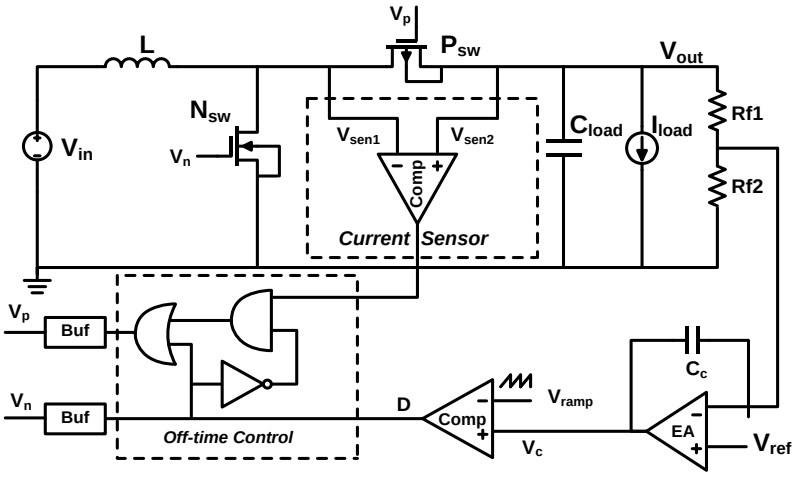

Figure 3-8: DCM VMC boost DC-DC converter system [9].

Comparing Figure 3-8 with Figure 3-1, we can find another difference between a DCM VCM boost converter and a CCM VCM boost converter that is the compensation circuit. Since the transfer function of a boost converter working in DCM (no matter in VMC or CMC) has only a single-pole [10], Type 1 or Type 2 compensation is enough for the loop stability. As shown in Figure 3-8, Type 1 compensation is applied in the control loop.

Making the fixed frequency PWM boost DC-DC converter working in DCM can effectively cancel the effects of the RHP zero and the double-pole thus enhancing the loop stability. But this method also has its weakness. If the load current varies over a large range, the power conversion efficiency of the DC-DC converter will change a lot. The efficiency of the converter working in a light load condition can be much worse than that in a high load condition. This can be qualitatively explained as follows. Since the working frequency of the DC-DC converter is always the same, the switching losses are almost in the same value for both high and light load conditions. But in the light load condition, because the power delivered to the load in each cycle is smaller, the switching losses will take a larger proportion of the total power thus reducing the total power conversion efficiency. In order to optimize the power conversion efficiency of the DC-DC converter in both high and light load condition, another kind of control method has been widely used for the low-power and high-efficiency applications. Because the working frequency is changed according to different load currents, this method is named pulse frequency modulation (PFM) control. Detailed discussion on this control method will be given in the next Section.

3.3 PFM Control

As mentioned in the last Section, for the PWM control method, the regulation of the output voltage of the converter under different load current conditions is achieved by adjusting the duty cycle or the on-time of the drive signal with a fixed frequency. However, in terms of the PFM control method, the regulation of the output under different load current conditions is achieved by changing the frequency. In the light load condition, since the frequency of the PFM control is much lower than that in the high load condition, the switching losses will be reduced thus significantly improving the power conversion efficiency. Because the output ripple voltage of a DC-DC converter is dependent on the load current, the PFM control generally utilizes this voltage for pulse modulation. As a result, the PFM control method is also named the ripple-based control [1]. There are two basic PFM ripple-based control techniques which have widely been used in recent years. One of them is the hysteretic control and the other is the constant on-time/off-time (COOT) control. Although [1] mentioned these methods are more suitable for the buck converter, after some modification, they can actually be used for the boost converter as well.

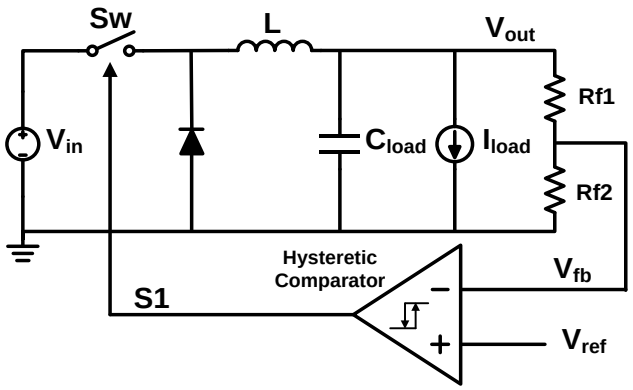

Figure 3-9: Buck DC-DC converter with hysteretic control [1].

Figure 3-9 shows a buck converter with hysteretic control [1]. In here, the hysteretic comparator is the core of the entire control system. This comparator is used to not only regulate the output voltage but also generate the pulse signal. The asynchronous structure is used for design simplification which means only one drive signal is required for the main power switch. The basic operation of the buck converter is illustrated in Figure 3-10. When the switch *Sw* is on, the buck converter works in the on-time phase. The energy coming from the input terminal is being stored in the inductor and used to charge the load. Both the inductor current and the output voltage increase. When the output voltage rises up to the upper boundary of the hysteretic band ($V_{\mathrm{ref}} + 0.5V_{\mathrm{H}}$), the hysteretic comparator will send a signal to open Switch *Sw*. Then, the buck converter works in the off-time phase and the dead time phase. The inductor current will fall down to zero (in the off-time) and stay zero (in the dead-time). The output voltage will continuously fall down to the lower boundary of the hysteretic band ($V_{\mathrm{ref}} - 0.5V_{\mathrm{H}}$), at this moment, the switch *Sw* will be turned on and a new cycle will start again.

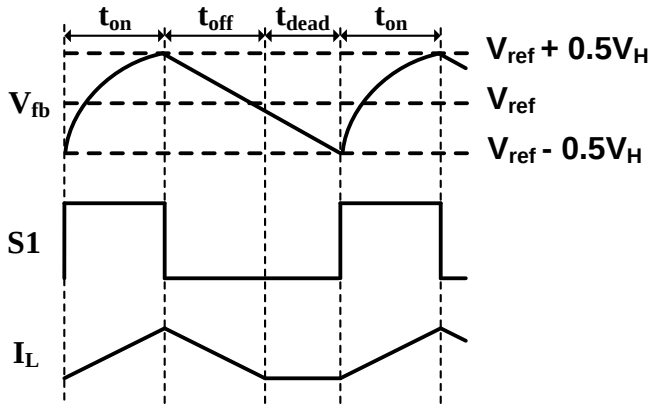

Figure 3-10: Timing diagram of the buck converter with hysteretic control.

Figure 3-11 exhibits a buck converter with constant-on-time/off-time control [1]. In here, the general comparator is used to monitor the output voltage and send the timer an

active signal to start the on-time (constant on-time) or the off-time (constant off-time). The duration of the on-time (constant on-time) or the off-time (constant off-time) is set as a constant value by the timer. The detailed operation can be understood by the aid of the timing diagram which is shown in Figure 3-12. In terms of the constant on-time control, the comparator sends an active signal to start the on-time when the output voltage falls down to the reference voltage (Figure 3-12 (a)). In terms of the constant off-time control, the comparator sends an active signal to start the off-time when the output voltage rises up to the reference voltage (Figure 3-12 (b)).

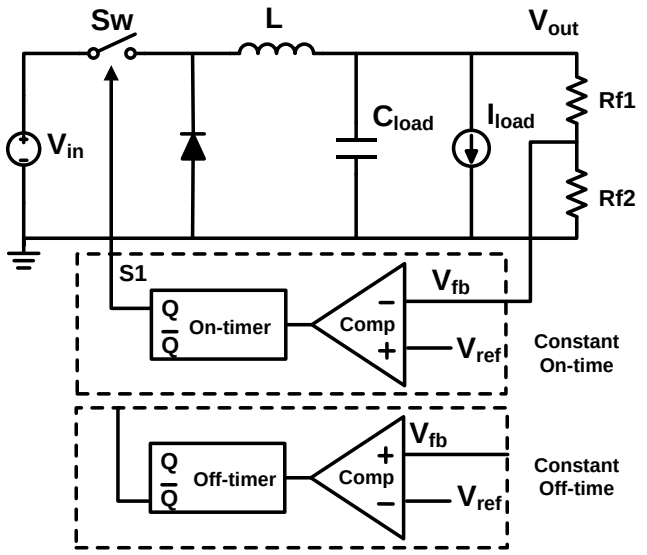

Figure 3-11: Buck DC-DC converter with COOT control [1].

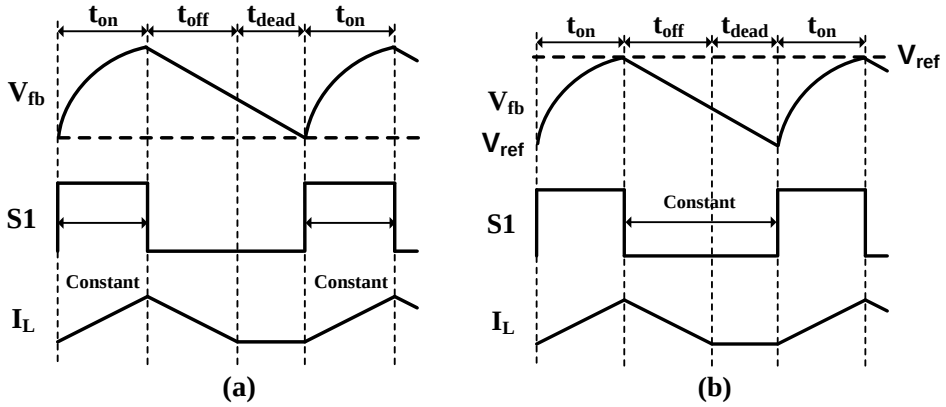

Figure 3-12: Timing diagram of the buck converter with (a) constant on-time (b) constant off-time control.

For the buck converter, the output voltage rises up during the on-time and falls down during the off-time and the dead-time. But for the boost converter, the output voltage rises

up during the off-time and falls down during the on-time and the dead-time. Because of a similar behavior of the output voltage during the on-time and the dead-time, the general PFM control methods such as those mentioned before cannot be applied for the boost converter. That is the reason why [1] mentioned ripple-based control is more suitable for buck converters. However, after making some improvement, the hysteretic control and the COOT control can also be used for the design of a boost DC-DC converter. For example, [11] provided an implementation method of the boost DC-DC converter with hysteretic control, and [12] designed a boost DC-DC converter with constant on-time control. In this thesis, the detailed explanation of these methods will not be given. The control method finally applied in this work belongs to an enhanced method of the COOT control. Its operating principle will be discussed in detail in the next section.

Because the PFM control system does neither require an error amplifier nor a clock signal generation, it can further improve the power conversion efficiency of the DC-DC converter, besides reducing the switching losses in the light load current condition. Due to its good performance in terms of power conversion efficiency and loop stability, the PFM (ripple-based) control technique is extremely attractive for low-power high-efficiency required applications such as portable or energy harvesting electronic devices. However, this method also suffers from some practical limitations or problems. Detailed discussions about these issues have been given in [1]. In summary, there are three dominant drawbacks of the ripple-based PFM technique, which are respectively (1) poorly defined switching frequency, (2) sensitivity to external noises, (3) inadequate DC regulation. The poorly defined switching frequency means the working frequency has a strong dependency on the system parameters (input and output voltage, load current) and some other non-ideal effects (parasitic effects and propagation delays). The sensitivity to external disturbances means that if there is some noise at the feedback node (V_{fb}), the noise may be sensed by the comparator and injected into the control loop thus interfering with the functionality. The inadequate DC regulation means the output voltage cannot be too close to the reference voltage due to some propagation delays or parasitic effects. Relevant improvement methods which can be used to eliminate the problem have also been proposed in [1]. In this thesis, we will not describe all of them in detail. We will just introduce the methods which have been applied in this work in the next section.

3.4 Control Technique Applied in This Work

Almost all kinds of general methods which can be used to control the DC-DC converter have been discussed in the previous sections. As mentioned before, each method has its own merits and limitations. Consequently, it has widely been acknowledged that no one method is optimal for all applications. It should be determined by the design requirements or specifications which control method is the best choice for controlling the DC-DC converter. In this design, because the boost DC-DC converter is used to transfer the

energy coming from the energy harvesting front-end to charge the load battery, the power conversion efficiency is the most important specification. Besides, since the input DC voltage of the boost DC-DC converter comes from a rectifier which rectifies an AC signal into a DC signal, the value of the rectified DC voltage is not stable. Hence, the loop stability is also a very important specification for this design. As for the frequency variation and the inadequate output DC regulation, there are not any specific requirements on them in this work.

Based on the analysis of the design specifications and the characteristics of different control techniques, the COOT control is finally applied in this work. As a kind of PFM ripple-based control technique, COOT control can provide not only perfect power conversion efficiency but also sufficient loop stability, which is undoubtedly the most suitable choice for this design. But as mentioned before, the basic COOT control circuit shown in Figure 3-12 cannot be directly used for a boost converter. Some improvements and adjustments should be made in order to achieve a boost DC-DC converter with COOT control. Figure 3-13 shows a simplified circuit model of the boost DC-DC converter with an enhanced COOT control technique which is used in this design. Its operation will be explained later by the aim of the timing diagram shown in Figure 3-14.

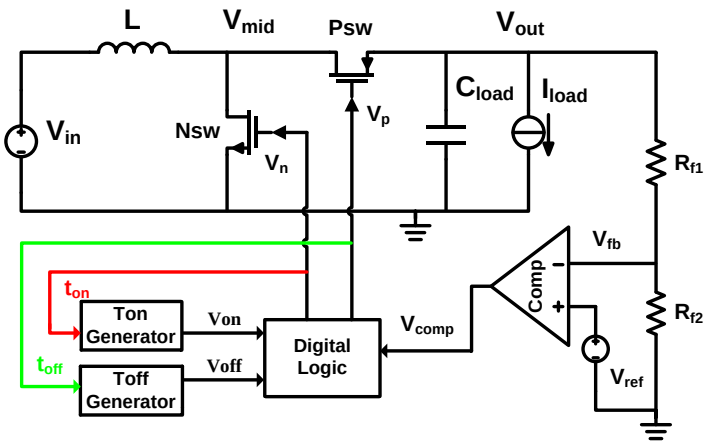

Figure 3-13: Boost DC-DC converter with an enhanced COOT control.

From Figure 3-14, we can see that the rising edge of the comparator output signal (V_{comp}) is used to activate a new cycle. During the dead-time in last cycle, since both the NMOS power switch (N_{sw}) and the PMOS power switch (P_{sw}) are open, the output voltage of the boost converter (V_{out}) falls down due to the load current. When the feedback voltage V_{fb} drops down to the reference voltage (V_{ref}), the rising of V_{comp} will start a new cycle. In a cycle, the on-time and the off-time is set to be constant values by two time generators. These two time generators utilize a specific mechanism to generate the proper on-time and off-time. (The proper on-time and off-time means the energy charged in the inductor during the on-time is equal to the energy discharged from the inductor to the load capacitor during the off-time.) After the on-time and off-time, the

boost converter works in the dead-time. The duration of the dead-time will be determined by when the feedback voltage falls down to the reference voltage.

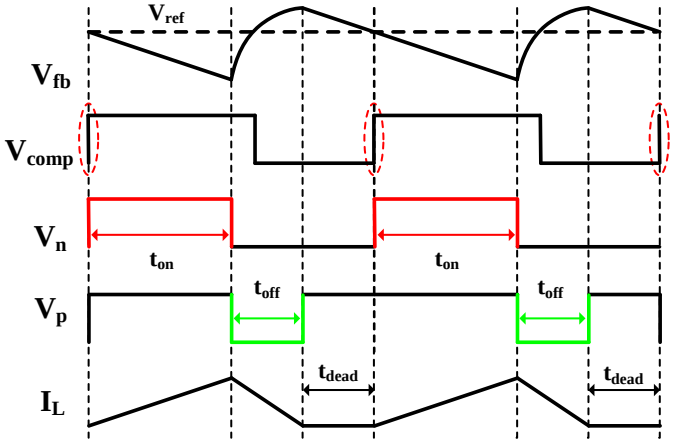

Figure 3-14: Timing diagram of the boost converter with an enhanced COOT control.

By using this enhanced method, COOT control has been achieved on a boost DC-DC converter design. But the general limitations of the PFM ripple-based control techniques which have been mentioned in previous section ((1) poorly defined switching frequency, (2) sensitivity to external noise, (3) inadequate DC regulation) also occur in this control system. Some improvements should be made to eliminate their effects. At first, since it is exactly our target to change the switching frequency under different load current conditions for high power conversion efficiency, there is no specific requirement on a fixed switching frequency. Hence, the first limitation will not be considered in this design. Moreover, as it is not necessary to charge the load battery with an accurate $1V$ voltage in this work, a little deviation (tens mV) between the output voltage and the reference voltage will not affect the charging action. Therefore, the third problem will also be ignored in this design. The only problem required to be considered in this work is the second one which is that the control system is sensitive to external noise.

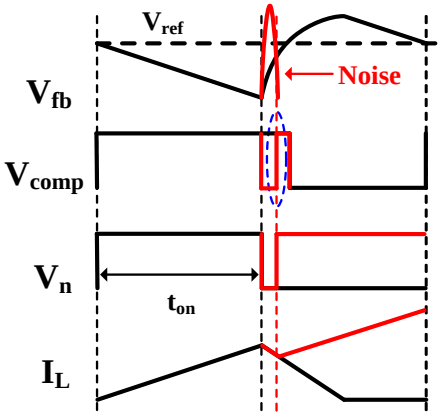

Figure 3-15: Control system is sensitivity to the noise at the node V_{fb}.

This problem is illustrated in Figure 3-15. We can see, if there is a spike (red curve) occurring at the feedback node V_{fb}, this spike will be sensed by the comparator and imported into the control system thus breaking the right functionality. Some effective solutions to eliminate this problem have been discussed in [1]. In this work, we choose a simple method proposed in [1] which is to add a small capacitor (C_{f}) across the upper resistor (R_{f1}) of the feedback divider. The small parallel capacitor works as a high-pass to improve noise immunity by increasing the PWM ramp. If the capacitor is chosen to satisfy the inequality

$$C_{\mathrm{f}}\frac{R_{\mathrm{f1}}\cdot R_{\mathrm{f2}}}{R_{\mathrm{f1}}+R_{\mathrm{f2}}} \gg T \ , \tag{3.11}$$

in which T is the switching period, then the ripple of the output voltage will reach the input of the comparator without further attenuation. But we should also pay attention to another issue which is the value of this high-pass filter capacitor should not be too much, because the step response of the boost converter with a large C_{f} will be very slow. Based on the simulation results, the value of this filter capacitor is finally set to be $200fC$. Figure 3-16 shows the boost DC-DC converter system with this improvement. However, during the research, we found that the performance of this improvement method is not very good. In future works, more effective methods should be studied and proposed.

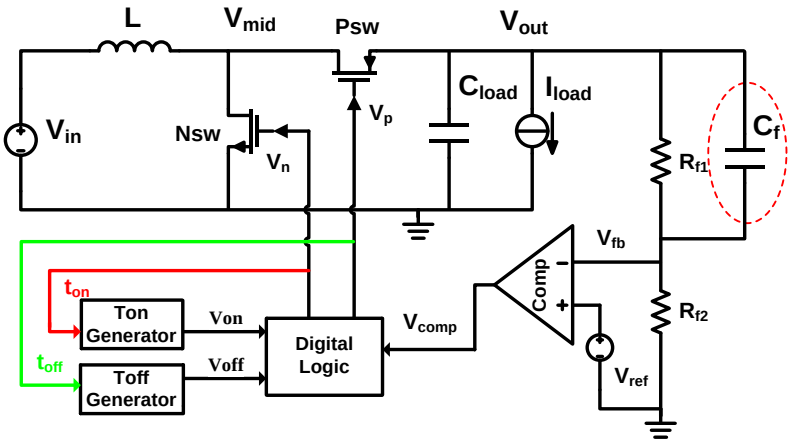

Figure 3-16: Boost DC-DC converter system with the filter cap

Until now, COOT control with relevant improvement techniques to eliminate its limitations has been described. But in order to achieve the proper setting of the on-time and off-time as mentioned before, an adaptive on-time/off-time (AOOT) control is applied to replace the general COOT control in this work. AOOT control is almost the same as the COOT except that the on-time and off-time are no more a constant value. In AOOT control, the values of the on-time and the off-time will be dependent on one or more system parameters (input voltage, output voltage, load current, etc.). In this work, we set the on-time and the off-time related to the input voltage and the output voltage. Let us review the equations in Section 2.1. Equations 2.3 and 2.5 express the charging and

discharging of the inductor current. According to these two equations, we can obtain that:

$$i_{\text{rise}} = \frac{V_{\text{in}} \cdot t_{\text{on}}}{L} \tag{3.12}$$

$$i_{\text{fall}} = \frac{(V_{\text{out}} - V_{\text{in}}) \cdot t_{\text{off}}}{L} \tag{3.13}$$

For high efficiency, we expect that i_{rise} is equal to i_{fall}, which means the current charged in the inductor is fully delivered to the load battery without any waste. But in COOT control, if there is a variation on the input voltage, because the output voltage is always fixed close to the reference voltage, the current balance will be broken. In AOOT control, if we set the on-time proportional to $(V_{\text{out}} - V_{\text{in}})$ and the off-time proportional to V_{in}, no matter what value the input voltage or output voltage is, the current balance will always be satisfied. The conclusion can be demonstrated by following equations. If we set:

$$t_{\text{on}} = k_1 \cdot (V_{\text{out}} - V_{\text{in}}) \tag{3.14}$$

$$t_{\text{off}} = k_2 \cdot V_{\text{in}} \tag{3.15}$$

And we make $k_1 = k_2$, there will always be:

$$i_{\text{rise}} = \frac{V_{\text{in}} \cdot t_{\text{on}}}{L} = i_{\text{fall}} = \frac{(V_{\text{out}} - V_{\text{in}}) \cdot t_{\text{off}}}{L} \tag{3.16}$$

Hence, by using AOOT control, the on-time and the off-time can be automatically adjusted according to different values of the input voltage and the output voltage thus always guaranteeing that the charging current of the inductor during the on-time is equal to the discharging current of the inductor during the off-time. Now the only problem is how to generate the on-time and the off-time which satisfy Equations 3.14 and 3.15. The mechanism of the time signal generation will be introduced in the next section.

3.5 Time Signal Generation

In a boost DC-DC converter with AOOT control, the generation and control of the on-time and the off-time is a crucial task. Actually, the on-time is the high-level pulse width of the drive signal V_{n} to the NMOS power switch, and the off-time is the low- level pulse width of the drive signal V_{p} to the PMOS power switch. Usually, these two time signals are generated and controlled by time generators.

There have been many implementation methods for time generators which have been proposed in previous works. Recently, two kinds of approaches have been widely applied in other studies. The first one is using an oscillator to generate a square-wave pulse signal for one power switch, and using a controlled delay line with a simple digital circuit to generate the signal for the other power switch [13], [14], [15], [16], [17]. One instance of the first approach is shown in Figure 3-17 [14]. A tunable ring oscillator with some frequency dividers can generate a pulse signal V_1 with 50% duty cycle for the on-time, of

which the pulse width (t_{on}) can be controlled by the bias current. A digital controlled delay line and an AND gate are used for the off-time generation. According to the timing diagram of the main signals shown in Figure 3-18, the off-time (t_{off}) is equal to the delay time (t_{delay}) which can be tuned by a digital control code.

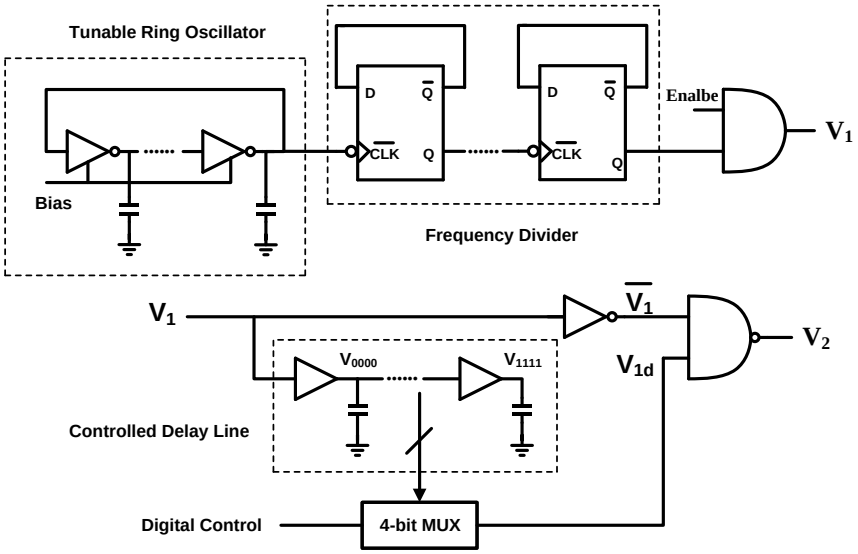

Figure 3-17: One approach to implement the time generators. [14]

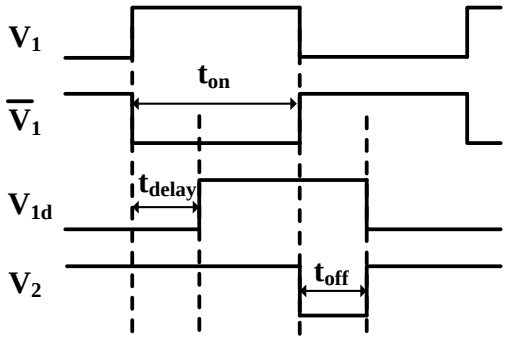

Figure 3-18: Timing diagram of main signals in the time generator. [14]

The other approach which has been widely employed to generate pulse signals in a DC-DC converter is charging a capacitor by a current source and comparing the voltage with a reference [18], [19], [20], [21], [22], [23]. Based on the charging and discharging equation of a capacitor (Equations 3.17 and 3.18) any desired time can be obtained by a proper setting of the values of *C*, *V* and *I*.

$$I = C \cdot \frac{dV}{dt} \tag{3.17}$$

$$t = C \cdot \frac{V}{t} \tag{3.18}$$

The working principle can be viewed clearly through an example [21], in which, a

pulse generator with a DAC pulse width modulator and a sleep mode control was proposed. Its schematic is shown in Figure 3-19. The MOSFET P_s works as a current mirror to generate a reference current for charging the capacitor array. The capacitance of the capacitor array in shunt structure is digitally controlled by the switch D_4-D_0 and their compliments. An analog comparator compares the voltage of the node V_{charge} with the reference voltage V_{ref}, and then outputs a pulse signal with the desired pulse width. The timing diagram of the main signals is shown in Figure 3-20.

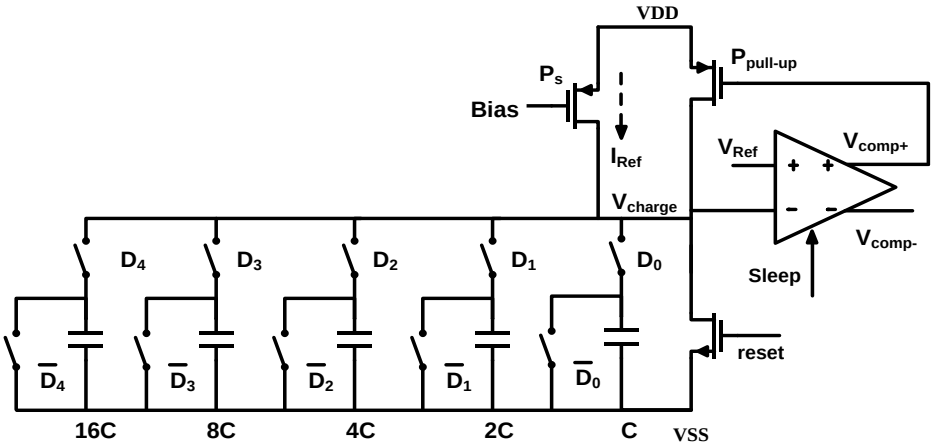

Figure 3-19: I-C time generator with DAC and sleep mode control [21].

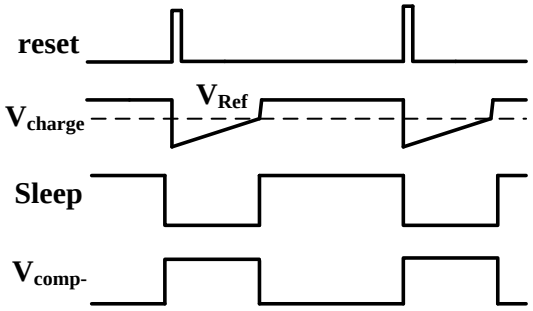

Figure 3-20: Timing diagram of main signals in the time generator [21].

Comparing these two methods, the second one is less power-efficient due to the constant DC current in the comparator, but it is more area-efficient and easy implemented as the circuits only include a ramp generator and an analog comparator [21]. In addition, in order to achieve AOOT control, the time signals should satisfy Equation 3.14 and 3.15. The second method can easily achieve this function by setting the charging current or the comparison voltage related to the input voltage and output voltage. Based on these benefits, the second method is used for the design of the time generators in this work. Figure 3-21 shows the on-time generator and its working principle. A constant current I_{on} is used to discharge the capacitor C_{on} from the initial voltage V_{out} to the reference voltage V_{in}, the generation time t_{on} satisfies the equation:

$$t_{\text{on}} = \frac{C_{\text{on}}}{I_{\text{on}}} \cdot (V_{\text{out}} - V_{\text{in}}) \tag{3.19}$$

Figure 3-22 shows the off-time generator and its working principle. A constant current I_{off} is used to charge the capacitor C_{off} from the initial zero to the reference voltage V_{in}, the generation time t_{off} satisfies the equation:

$$t_{\text{off}} = \frac{C_{\text{off}}}{I_{\text{off}}} \cdot V_{\text{in}} \tag{3.20}$$

If we make k_1 in Equation 3.14 is equal to ($C_{\text{on}}/I_{\text{on}}$), and k_2 in Equation 3.15 equal to ($C_{\text{off}}/ I_{\text{off}}$), Equations 3.19 and 3.20 are exactly the same as Equation 3.14 and 3.15. Then, the timing balance of the on-time and the off-time mentioned in Section 3.4 can be achieved by just making $C_{\text{on}}/I_{\text{on}}$= $C_{\text{off}}/ I_{\text{off}}$.

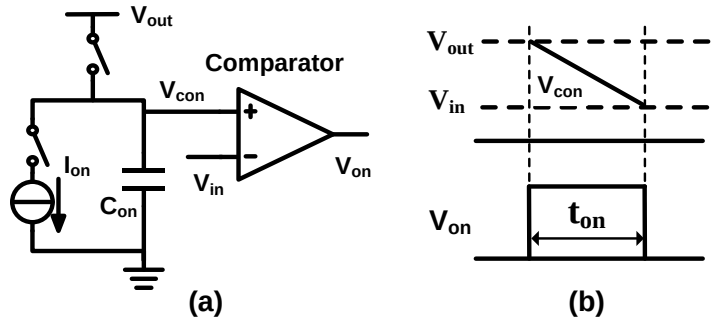

Figure 3-21: On-time generator and its working principle.

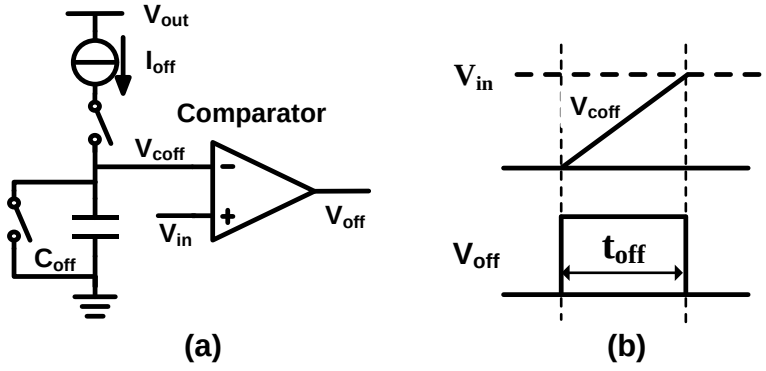

Figure 3-22: Off-time generator and its working principle.

3.6 Zero Current Switching Adjustment

According to the analysis in Section 3.4, the adaptive on-time control can theoretically ensure the current stored in the inductor during the on-time equals the current released from the inductor during the off-time. However, many non-ideal effects are not taken into account during the formula derivation. For example, the voltage across the inductor during the on-time should actually be ($V_{\text{in}} - V_{\text{ds\_nsw}}$) rather than V_{in} ($V_{\text{ds\_nsw}}$ is the

drain-source voltage of the NMOS power switch transistor), hence a precise expression of the inductor charging equation should be:

$$i_{\text{rise}} = (V_{\text{in}} - V_{\text{ds\_nsw}}) \cdot \frac{t_{\text{on}}}{L} \tag{3.15}$$

The same non-ideal effect also occurs during the off-time, a more precise expression of the inductor discharging equation would be:

$$i_{\text{fall}} = (V_{\text{in}} - V_{\text{out}} - V_{\text{ds\_psw}}) \cdot \frac{t_{\text{off}}}{L} \tag{3.16}$$

The non-ideal effects in the time generator will also break the timing balance between the on-time and the off-time. In terms of the time generators applied in this work, non-ideal effects include capacitor mismatch (ΔC_{mis}), current mismatch (Δi_{mis}) and the inaccuracy of the comparator (V_{err}). A more precise expression of the time generating equation would be:

$$t = (C \pm \Delta C_{\text{mis}}) \cdot \frac{(V_{\text{ref}} \pm V_{\text{err}})}{(i_{\text{c}} \pm \Delta i_{\text{mis}})} \tag{3.17}$$

Due to these non-ideal effects, an extra block is required to slightly adjust the off-time thus guaranteeing the timing balance. As mentioned in Section 2.1, the boost converter operates in DCM, which means the DC current flowing through the inductor is zero. Hence, the inductor current should rise from zero at the beginning of the on-time and fall down to zero at the end of the off-time. This mechanism is named zero current switching (ZCS).

To achieve ZCS adjustment, an energy efficient method which is nearly free of static current dissipation has been proposed and widely used in recent studies [13] [16] [20] [24]. According to the condition of the drain voltage (V_{mid}) of the high-side power switch (PMOS) at the end of the off-time phase, whether the off-time is overly short or overly long can be judged.

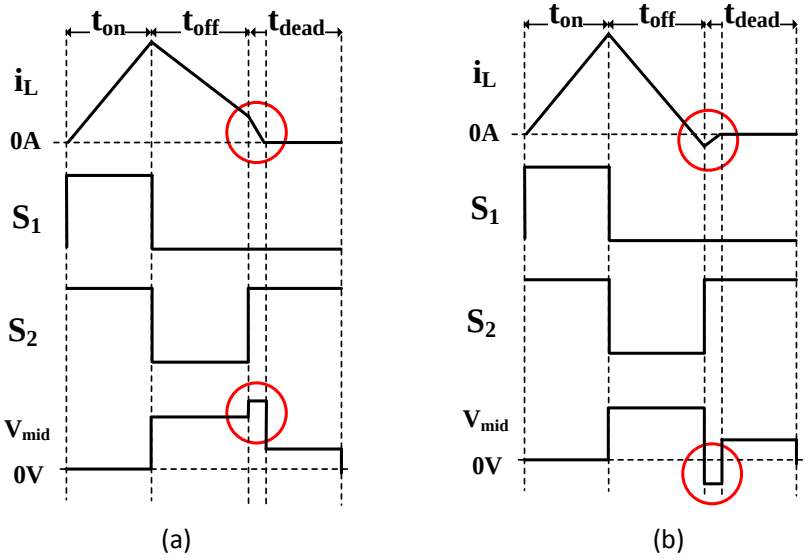

Figure 3-23: Boost converter with overly short off-time (a) and overly long off-time (b)

The operating principle can be explained by means of Figure 3-23. In the off-time period, because the high-side power switch is closed, its drain voltage (V_{mid}) is nearly equal to its source voltage which is exactly the output voltage (V_{out}) of the boost converter. At the end of the off-time period, if the off-time is overly short which means the inductor current has not fallen down to zero (Figure 3-23 (a)), V_{mid} will have a positive voltage jump. The reason for the positive jump is the remaining positive inductor current will continue flowing through the high-side PMOS power switch which has a large crossover resistance when it is switched off. The positive direction of the current is defined as flowing from the input to the output of the boost converter. On the other hand, at the end of the off-time period, if the off-time is overly long which means the inductor current has fallen to a negative value (Figure 3-23 (b)), V_{mid} will have a negative voltage jump. The reason for the negative jump is that, at this moment, there is a negative current flowing through the high-side PMOS power switch which has a large crossover resistance. Therefore, by detecting the high or low state of V_{mid} at the end of the off-time, we can obtain whether the off-time should be increased or decreased for ZCS.

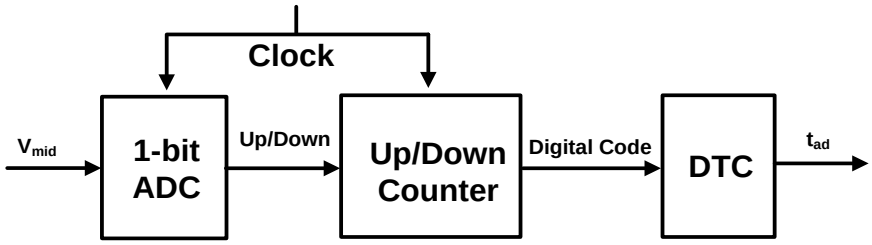

Figure 3-24: Mechanism of the ZCS adjustment.

The ZCS adjustment can be achieved by the control system shown in Figure 3-24. A 1-bit analog-to-digital converter (ADC) is used to detect the high/low state of the node V_{mid} and provide the information to the control system about whether the off-time should be increased or decreased in next cycle. According to the ADC's information, an up/down counter adjusts the digital code which carries the information about how much the off-time should be corrected for ZCS. A digital-to-time converter (DTC) is applied to receive the digital code, and based on the digital code, to generate an additional time to correct the off-time for ZCS. This ZCS adjustment system detects the off-time condition (overly short or long) in a period, and makes correction on the off-time in the next period. In steady state, the digital code should be 1-bit up and down around a definite value.

In this work, regardless of the effects of the non-ideal factors, the off-time should be *100ns* if the on-time is *150ns*. Since the non-ideal effects do not change the timing balance drastically, a *±15%* adjustment of the off-time is sufficient to overcome these non-ideal effects, which means the off-time is tuned in a range of *85ns~115ns*. Under the consideration of the design simplification and allowable tuning accuracy, the resolution of the ZCS adjustment in time is determined as *1ns* per bit. According to the inductor

discharging equation, we can obtain that *1ns* off-time variation can cause the inductor current to change a value of:

$$i_{\mathrm{L\_V}} = 0.6V \cdot \frac{1ns}{1uH} = 600\mu A \tag{3.18}$$

It means the resolution of the ZCS adjustment in current is about 600μA, which is accurate enough for this work. Therefore, a 5-bit binary code is applied in the ZCS adjustment system.

Finally, Figure 3-25 shows the model of the entire boost DC-DC converter system with AOOT control and ZCS adjustment that has been designed in this work.

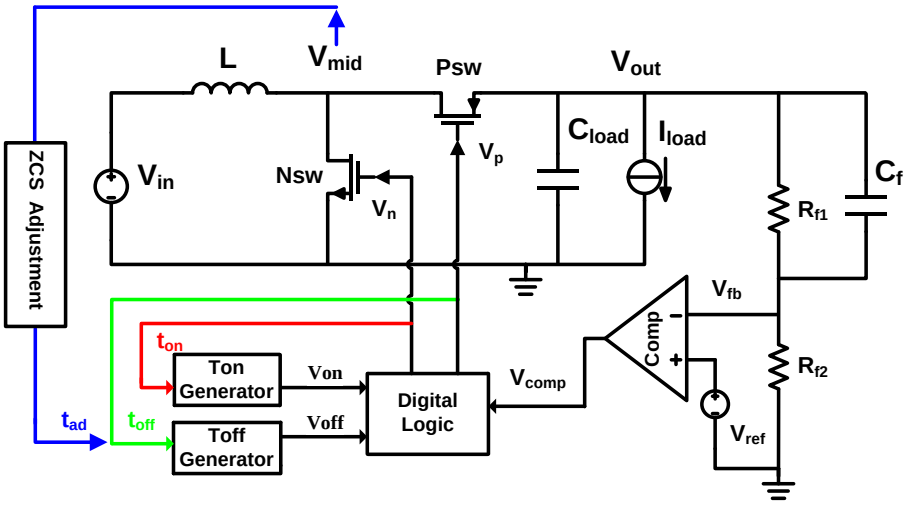

Figure 3-25: Entire boost DC-DC converter with AOOT control and ZCS adjustment.

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Chapter 4

Circuit Implementation

4.1 Overview of This Chapter

The basic functionality of the boost DC-DC converter system designed in this work has been introduced in previous chapters. In Chapter 2, the power plant of the boost converter has been designed based on the target specifications. In Chapter 3, the most suitable control technique has been selected after detailed analyses of all candidates. Figure 4-1 shows the system-level schematic of the entire boost DC-DC converter system designed in this research. In this chapter, the circuit implementation of each block in transistor level will be introduced. The Digital Logic block used to control the sequence of all signals in the control loop is introduced in Section 4.2. The time generators applied to control the durations of the on-time and off-time are described in Section 4.3. The circuit implementation of the ZCS adjustment is presented in Section 4.4. In Sections 4.5 and 4.6, the circuit design of the comparator and the reference current generator are discussed.

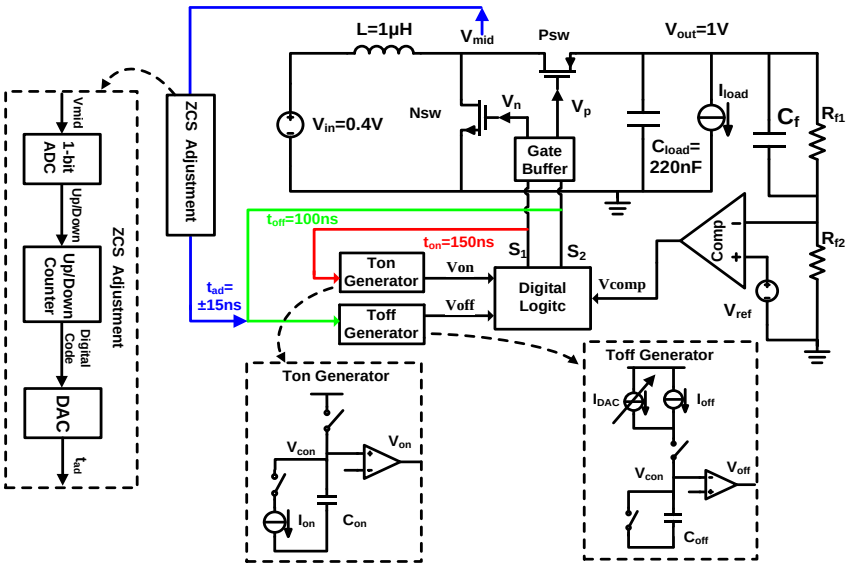

Figure 4-1: Entire boost DC-DC converter system designed in this work.

4.2 Digital Logic Block

The Digital Logic block is the only digital circuit in the entire system of the boost DC-DC converter. It plays a crucial role, namely to control the sequence of all signals in the control system thus making the converter operate in the right functionality. Its specific working principle in steady state will be explained by means of Figure 4-1 and the following flow chart (Figure 4-2).

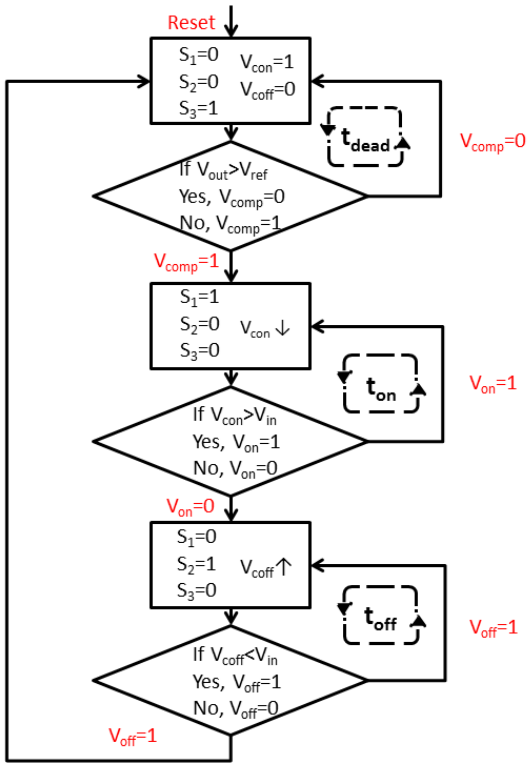

Figure 4-2: Operation flow chart of the boost DC-DC converter.

At first, a "Reset" signal ($\overline{Re} = 0$) comes and resets the Digital Logic block to the initial phase. In this phase, there are $S_1 = 0$, $S_2 = 0$ and $S_3 = 1$. S_1 is the signal that carries the on-time information. As shown in Figure 4-1, after a gate buffer, S_1 is turned to V_n. S_2 is the signal that carries the off-time information. As shown in Figure 4-1, after an inverter and a gate buffer, S_2 is turned to V_p. S_3 is the signal that carries the dead-time information. The reset signal also resets the T_{on} Generator and T_{off} Generator to the initial phase where there are $V_{con} = 1$ and $V_{coff} = 0$. Then the "Reset" signal is turned off ($\overline{Re} = 1$) and the boost converter starts working in the dead-time phase. The dead-time phase will be maintained until the output voltage of the boost converter drops below the reference voltage ($V_{out} < V_{ref}$). When $V_{out} < V_{ref}$, S_1 is activated to 1 and the boost converter steps into the on-time phase. The duration of the on-time phase is controlled by the T_{on} Generator. After a specific time, the T_{on} Generator will send a signal to switch S_1

from 1 to 0 and S_2 from 0 to 1 which means to terminate the on-time phase and start the off-time phase. The duration of the off-time phase is determined by the T_{off} Generator which will send a signal to shift the boost converter from the off-time phase into the dead-time phase. When the boost converter enters the dead-time phase, it will face an operating model selection which will be further explained later in this section. If the output voltage is still lower than the reference voltage ($V_{\text{out}} < V_{\text{ref}}$) after a cycle, S_1 will be immediately turned to 1, which means a new on-time phase starts. In this case, the boost converter works in quasi-CCM. If the output voltage is higher than the reference voltage after a cycle, the dead-time will be maintained until the voltage output drops below the reference voltage. In this case, the boost converter works in DCM. The timing diagram of main signals in the control system is shown in Figure 4-3 where $\overline{Re} = -Re$.

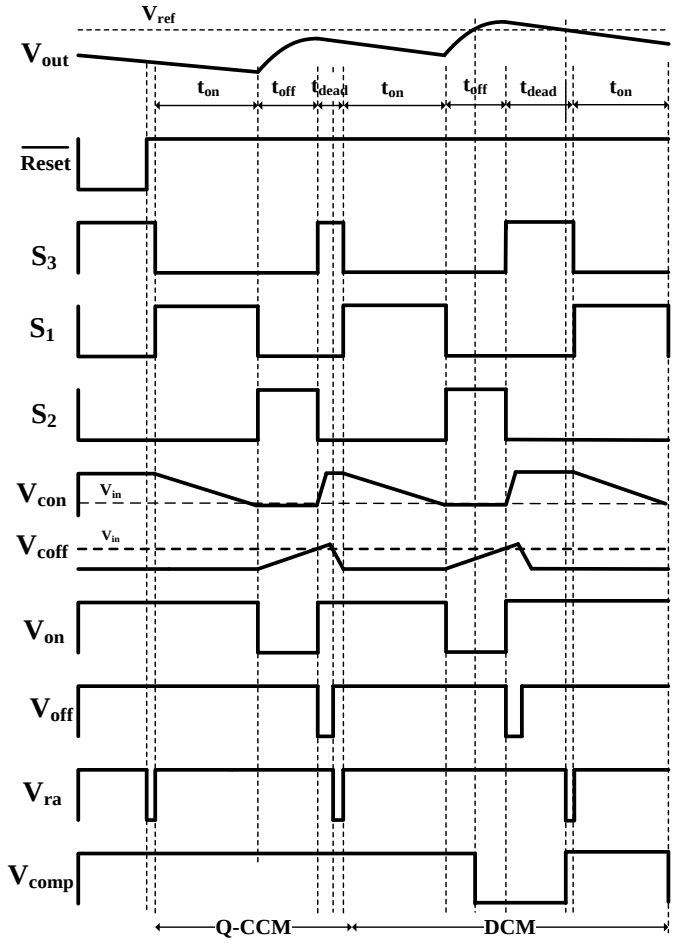

Figure 4-3: Timing diagram of all signals.

In order to achieve the logic function mentioned above, the Digital Logic block is built by some digital cells such as D flip-flops and logic gates. Its detailed schematic is shown in Figure 4-4. During the design of this block, some issues should be considered, otherwise the performance or even the functionality of the converter will be destroyed.

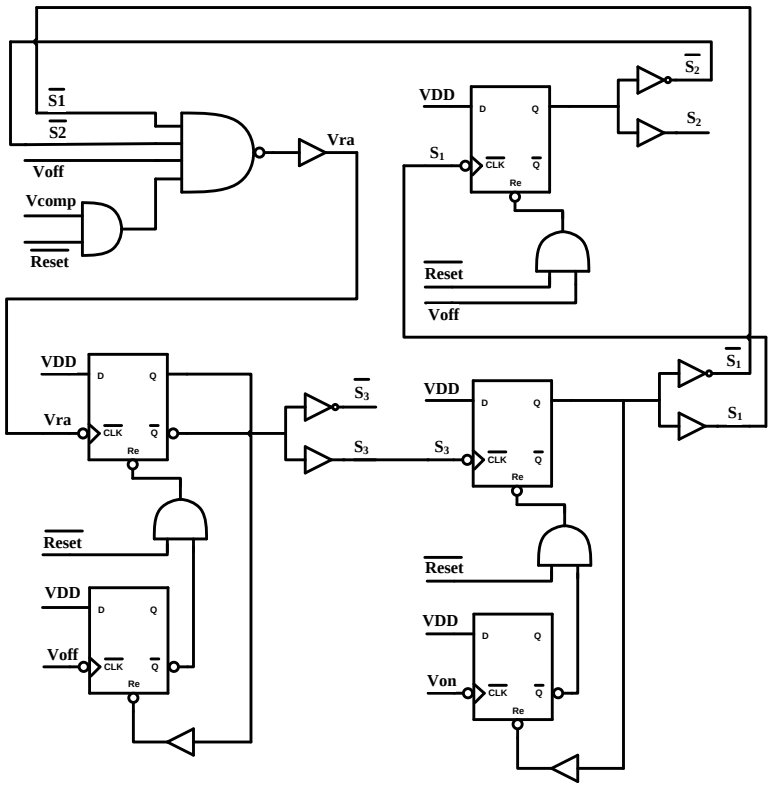

Figure 4-4: Schematic of the Digital Logic block.

The first issue also the most important one is which signal should be used to trigger S_3. S_3 is the control signal for the dead-time. According to the working principle of the control method discussed in Section 3.4, the dead-time will be maintained until the output voltage of the boost converter drops below the reference voltage ($V_{\text{out}} < V_{\text{ref}}$). But if S_3 is directly triggered by the output signal of the comparator (V_{comp}), there will be a mistake if the output voltage of the boost converter is still lower than the reference voltage ($V_{\text{out}} < V_{\text{ref}}$) after the off-time. The failure mechanism is shown in Figure 4-5.

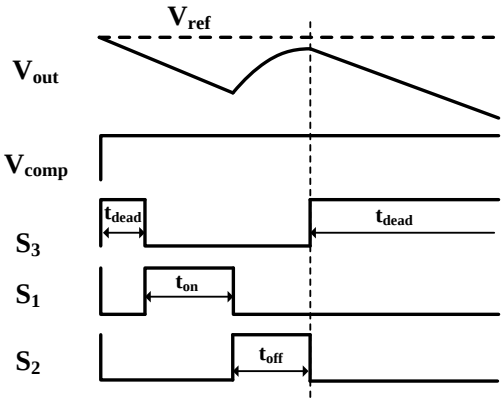

Figure 4-5: First failure mechanism of the control system.

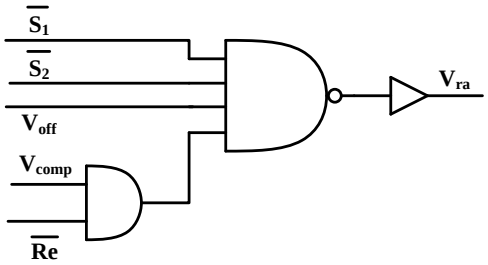

Figure 4-6: Operating model selection circuit.

To avoid this failure, an operating model selection circuit shown in Figure 4-6 can be used to solve this problem. The signal V_{ra} is used to control the dead-time instead of the signal V_{comp}. V_{ra} is controlled by $V_{\mathrm{comp}}, V_{\mathrm{off}}$, $\overline{S_1}$, $\overline{S_2}$ and $\overline{Re}$. When the boost converter steps from the off-time phase into the dead-time phase, two models will be selected:

(1) $V_{\mathrm{comp}} = 1$ which means V_{out} is still lower than V_{ref} ($V_{\mathrm{out}} < V_{\mathrm{ref}}$) after an off-time. At this moment, V_{comp}, V_{off}, $\overline{S_1}$, $\overline{S_2}$ and $\overline{Re}$ are all equal to 1 and V_{ra} will be only controlled by V_{off}. In Figure 4-7, we can see V_{coff} will quickly fall below V_{in} in the dead-time phase thus causing V_{off} rising to 1. Accordingly, V_{ra} will be turned to 0 and then S_3 will be turned to 0 by the falling edge of V_{ra}. S_1 will be turned to 1 by the falling edge of S_3 which means a new cycle starts. In this case, because the dead-time is very short, the boost converter works in the quasi-CCM mode.

(2) $V_{\mathrm{comp}} = 0$ which means V_{out} is higher than V_{ref} ($V_{\mathrm{out}} > V_{\mathrm{ref}}$) after an off-time. At this moment, V_{ra} is controlled by V_{comp}. From Figure 4-7, we can see that, after some time, V_{comp} will rise to 1 because the output voltage falls below the reference voltage. Then V_{ra} will become 0 due to the falling edge of V_{comp} and a new cycle begins. In this case, due to a relatively long dead-time, the boost converter works in the DCM mode.

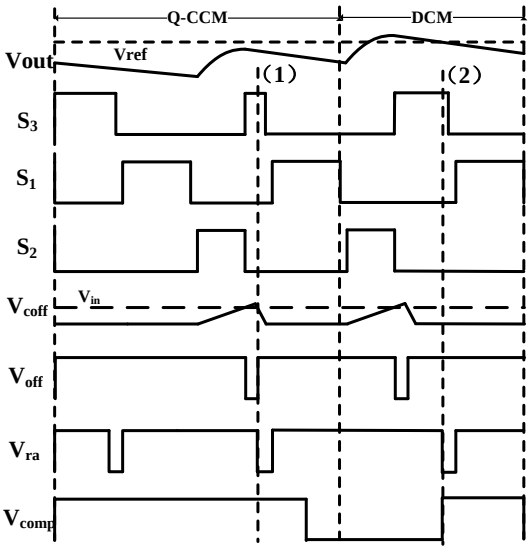

Figure 4-7: Timing diagram of quasi-CCM and DCM.

From the above analyses, it becomes clear that, by using the operation model selection circuit, automatic model selection can be really achieved thus ensuring the converter to work properly. Moreover, the model selection circuit can also ensure a new cycle starting after the previous cycle ending. The reason is that V_{ra} can only be turned to 0 when both $\overline{S_1}$ and $\overline{S_2}$ are 1, which means the boost converter is not working in the on-time or the off-time phase.

The second issue which should be considered occurs in the S_1 and S_3 generation. The signal S_3 should be reset to 1 by the falling edge of V_{off} rather than the low level of V_{off}. According to the working principle, Signal S_3 is switched from 1 to 0 to terminate the dead-time and start the on-time by the falling edge of Signal V_{ra}. But at the falling edge of V_{ra}, V_{off} may be low due to system delay. If S_3 is reset by the low level of V_{off}, it may miss the activated signal (the falling edge of V_{ra}). If this happens, the boost converter will not work correctly. The timing diagram of this problem is shown in Figure 4-8.

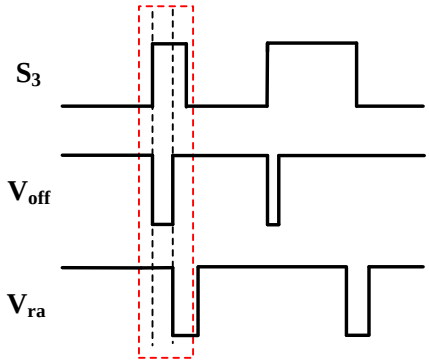

Figure 4-8: Timing diagram of S_3 triggering and resetting.

An extra D flip-flop can be used to reset S_3 on the falling edge of V_{off}. The detailed circuit implementation is shown in Figure 4-9. The same problem also occurs in the generation of S_1. So the same circuit is applied for S_1 generation as well.

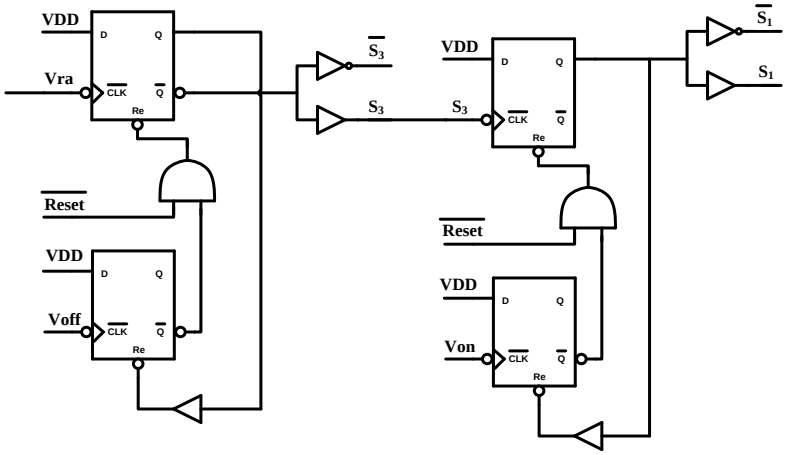

Figure 4-9: S_1 and S_3 generating circuits.

The third issue which should be paid attention to is the overlap of Signals S_1 and S_2. From Figure 4-10, we can see that if the two power switches are closed simultaneously, the output of the DC-DC convertor will be shorted to ground. Not only the energy stored in the load capacitor will be lost, but also the output voltage ripple will be affected by the short. Therefore, the overlap of S_1 and S_2 should be avoided at all times. As shown in Figure 4-4, the S_2 is triggered by the falling edge of S_1 in this design. Hence, this problem does not occur any more.

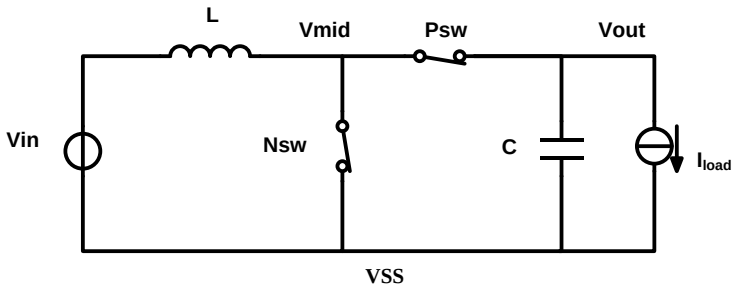

Figure 4-10: Output of the boost converter short to the ground.

4.3 On-Time and Off-Time Generators

In Section 3.5, we have discussed the selection of the implementation method for the time generators in this work, and their basic schematics have been shown in Figure 3-21 and Figure 3-22. In this section, the transistor-level circuit implementation will be described. Figure 4-11 shows the transistor-level circuit of the on-time and off-time generators. The parameters of all transistors are shown in Table 4-1. Figure 4-11 (a) is the circuitry of the on-time generator, and Figure 4-11 (b) is the circuitry of the off-time generator. In the circuits, the transistors M1, M2, M5, M6, M8 and M9 work as current mirrors which provide charging and discharging currents, Transistors M3, M4, M7, M10 and M11 are applied as switches which are controlled by S_1, S_2 and S_3.

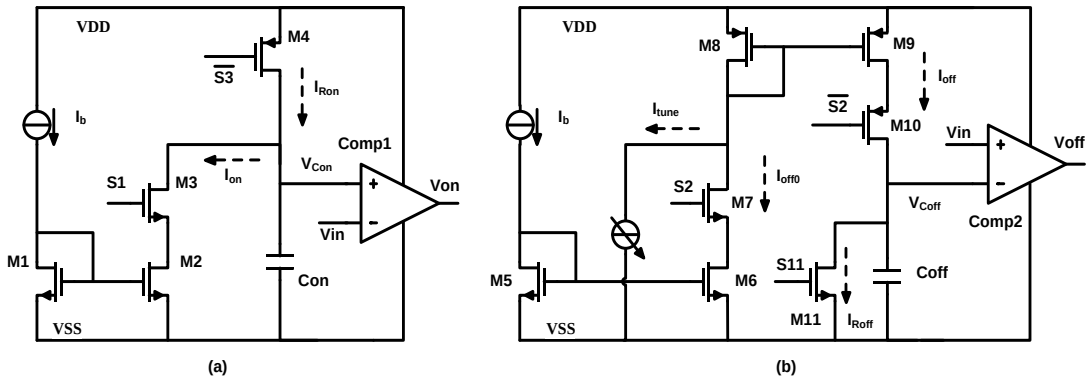

Figure 4-11: Circuit implementation of the on-time and off-time generators.

Table 4-1: Parameters of the transistors in the on-time and off-time generators

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11
L (µm)	*2*	*2*	*0.1*	*0.04*	*2*	*2*	*0.1*	*2*	*2*	*0.1*	*0.04*
W (µm)	*0.2*	*0.8*	*0.6*	*2.4*	*0.2*	*0.2*	*0.6*	*5*	*5*	*0.9*	*1.2*
F (µm)	*1*	*1*	*2*	*7*	*1*	*1*	*2*	*2*	*2*	*2*	*7*
M (µm)	*10*	*100*	*1*	*2*	*10*	*80*	*1*	*2*	*2*	*1*	*1*

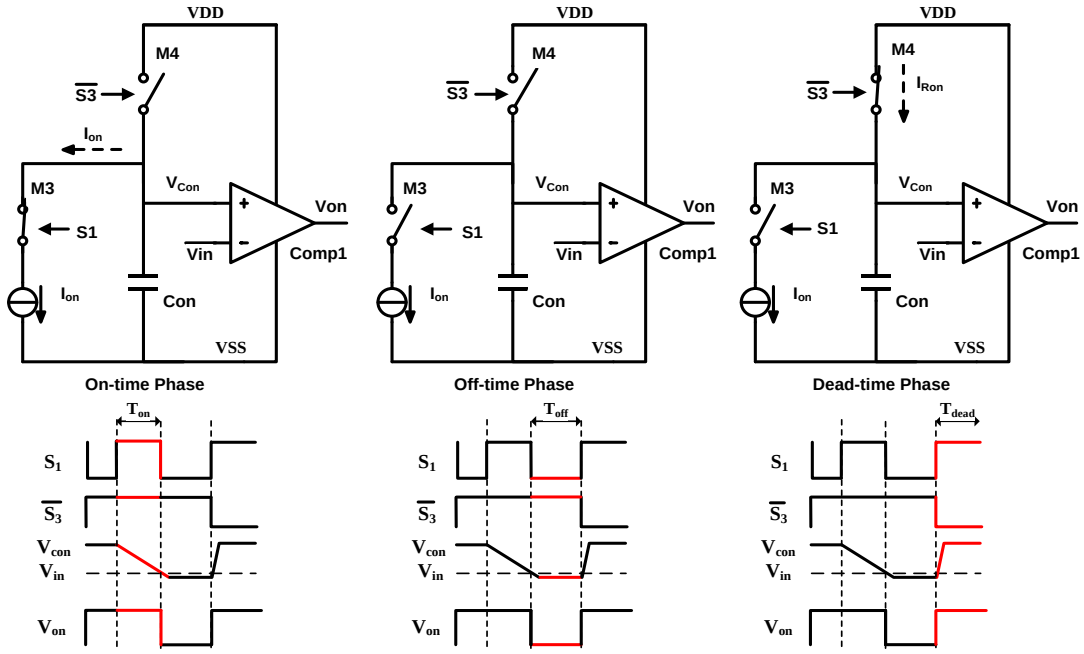

Figure 4-12: Different working phases of the on-time generator.

Figure 4-12 shows the working conditions of the on-time generator in different phases. In the on-time phase, switch M3 is close and switch M4 is open. The capacitor C_{on} with an initial voltage V_{DD} is discharged by a constant current I_{on}. The voltage of node V_{con} drops down on a rate of,

$$\frac{dV_{con}}{dt} = \frac{I_{on}}{C_{on}} \tag{4.3}$$

When V_{con} drops to the value V_{in}, i.e., the same voltage as appeared at the other input of the comparator, the comparator will output an active signal (falling edge) to the Digital Logic block. This signal will shift the boost converter from the on-time phase to the off-time phase. In the off-time phase, switch M3 and M4 are both open. The voltage of node V_{con} will remain at a value which is slightly lower than V_{in} and the output of the comparator will stay low. In the dead-time phase, the switch M3 is open and the switch M4 is closed. The capacitor is quickly charged to V_{dd}. In this phase, the output of the comparator will return to the high level.

From the analysis in Chapter 2, we know V_{in}, V_{dd} and t_{on} is $0.4V$, $1V$ and $150ns$, respectively. According to Equation 4.3, we can get:

$$\frac{C_{on}}{I_{on}} = \frac{t_{on}}{V_{out}-V_{in}} = \frac{150ns}{1V-0.4V} = 250nF/A \tag{4.4}$$

Under the consideration of acceptable power consumption, the discharging current (I_{on}) is set to be $10\mu A$ in this work. Hence the capacitor C_{on} becomes

$$C_{\text{on}} = 250nF/A \times I_{\text{on}} = 2.5pF \tag{4.5}$$

For lower power consumption, the discharging current can be further reduced. As a result, capacitor C_{on} should be decreased as well. Table 4-2 shows the simulation results of the power consumption of the on-time generator with different discharging currents.

In Table 4-2, we can see that the decrement of the discharging current makes little contribution to reducing the power consumption. This demonstrates that it is a reasonable decision to set the discharging current and the capacitor as $10\mu A$ and $2.5pF$ in this work.

Table 4-2: Power consumption of the on-time generator for different discharging currents

Discharging current I_{on}	10µA	1µA
$P_{ton\_generator}$ at high load condition (10mA)	9.6µW	4.3µW
$P_{ton\_generator}$ / P_{in} at high load condition (10mA)	0.093%	0.091%
$P_{ton\_generator}$ at low load condition (0.1mA)	3µW	2.9µW
$P_{ton\_generator}$ / P_{in} at low load condition (0.1mA)	2.471%	2.45%

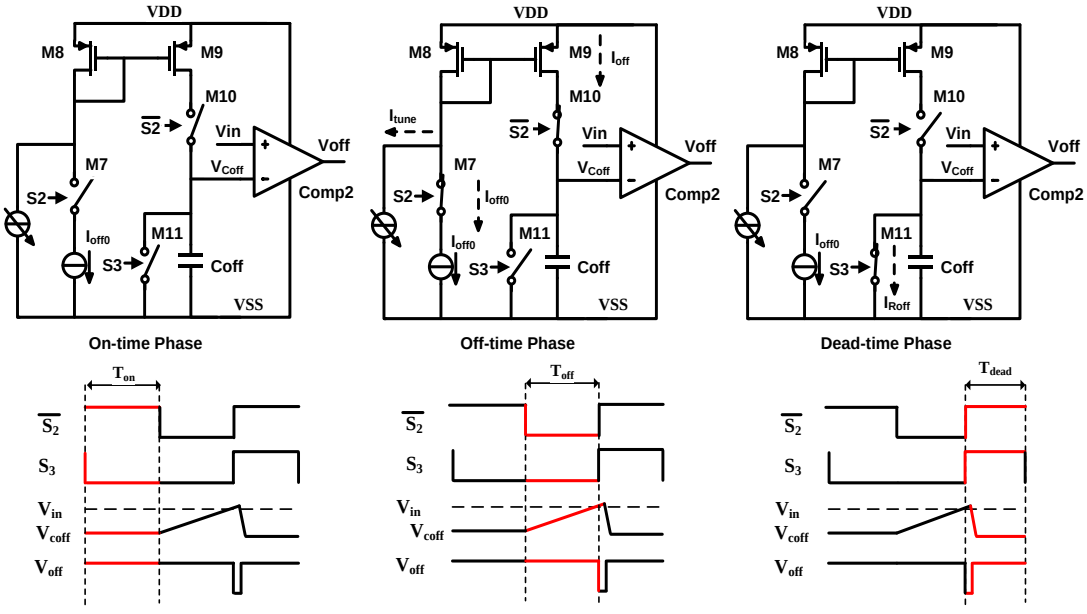

Figure 4-13: Different working phases of the off-time generator.

Figure 4-13 exhibits the working conditions of the off-time generator working in different phases. In the on-time phase, switches M7, M10 and M11 are all open. The voltage of node V_{off} will remain the same value as it is in the dead-time phase, and the output of the comparator will stay high. In the off-time phase, switch M11 is open and switches M7 and M10 are closed. The capacitor is charged by a constant current I_{off}. The voltage of node V_{coff} rises at a rate of,

$$\frac{dV_{\text{coff}}}{dt} = \frac{\text{I}_{\text{off}}}{C_{\text{off}}} \tag{4.6}$$

When V_{coff} rises to the same value (V_{in}) as present at the other input of the comparator, the comparator will output an active signal (falling edge) to the Digital Logic blocks which will terminate the off-time phase and turn the boost convertor to the dead-time phase. In the dead-time phase, switches M7 and M10 are both open and the switch M11 is closed. The capacitor is fast discharged to $0V$. The output of the comparator will return to the high level during this phase.

According to Equation 2.32, if the on-time is $150ns,$ the off-time is required to be $100ns$ for the timing balance. In order to generate a $100ns$ off-time, based on Equation 4.3, it follows:

$$\frac{C_{\text{off}}}{I_{\text{off}}} = \frac{t_{\text{off}}}{C_{\text{coff}}} = \frac{100ns}{0.4V} = 250nF/A \tag{4.7}$$

Since the charging current I_{off} in the off-time generator should be tuned in a range so as to adjust the off-time for achieving the ZCS adjustment (the detailed operating principle will be presented in the next section). Under the consideration of the ZCS adjustment resolution, this current cannot be too small. Therefore, the value of the charging current I_{off} is finally set to be $10\mu A$, and C_{off} becomes

$$C_{\text{off}} = 250nF/A \times I_{\text{off}} = 2.5pF \tag{4.8}$$

As mentioned above, transistors M1, M2, M5, M6, M8 and M9 work as current mirrors in the time generators. In general, it is better to use a transistor with larger size for the current mirror application due to the better performance on mismatch and noise. But since the charging and the discharging currents in the time generators are relatively small (in microampere level), the transistors with too large size will lead to a longer setting time which will reduce the accuracy of the time generators or even break down the functionality of the boost converter. From the simulation results shown in Figure 4-14, this issue can be seen clearly.

Figure 4-14 (a) is the simulation results of the time generators in which the channel lengths (L) of the transistor M1, M2, M5, M6, M8 and M9 are $2\mu m$. Figure 4-14 (b) is the simulation results of the time generators in which the channel lengths (L) of the transistor M1, M2, M5, M6, M8 and M9 are $3\mu m$. The *W/L* ratios of the transistors are the same on these two conditions. But in Figure 4-14 (b), the larger L leads to a bigger parasitic capacitor, thus causing a longer settling time. If in this case, the average currents during the on-time and the off-time will be far away from the desired value. As a result, the

generated time based on Equations 4.2 and 4.3 will not be accurate. In this work, the channel lengths of the transistors M1, M2, M5, M6, M8 and M9 are determined as $2\mu m$.

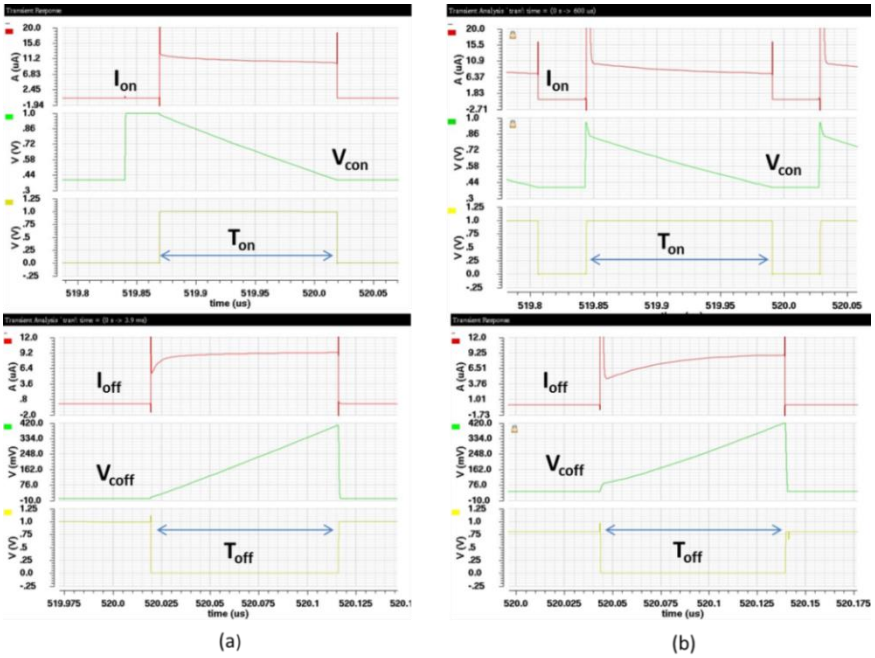

Figure 4-14: Simulation results of the time generators with different channel length.

In the circuitry of the time generators (Figure 4-11), transistors M3, M4, M7, M10 and M11 are applied as switches. Among these transistor-based switches, M4 and M11 should have a very large *W/L*, because the voltage of node V_{con} need be immediately charged to V_{dd} and the voltage of node V_{coff} need to be immediately discharged to V_{ss} in the dead-time phase, especially when the boost converter works in the quasi-CCM mode (the dead-time is very short). In this work, the *W/L* of M4 is chosen to be 840 and the *W/L* of M11 is chosen to be 200. The simulation results are shown in Figure 4-15. The reset time of nodes V_{con} and V_{coff} are approximately $600ps$. The maximum current passing through the transistors during the reset process is about $5mA$.

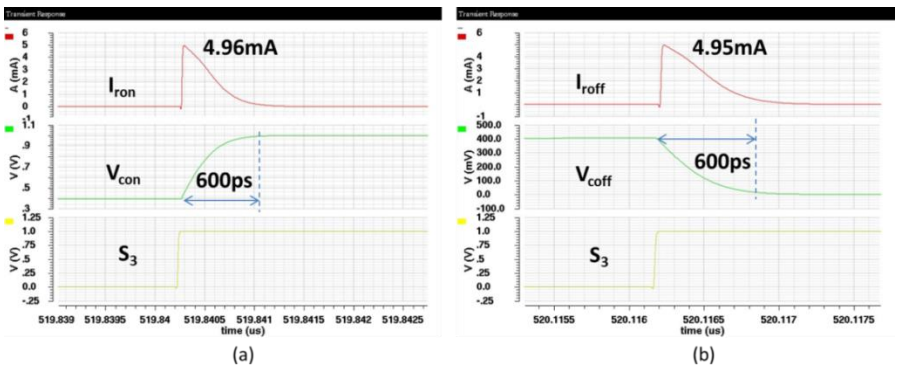

Figure 4-15: Reset of nodes V_{con} and V_{coff} in the dead-time phase.

4.4 Zero Current Switching Adjustment Blocks

The operating principle of the zero current switching (ZCS) adjustment has been described in Section 3.6. The transistor-level circuit implementation will be introduced in this section. Figure 3-24 showed the system-level diagram of the ZCS adjustment block. In this block, a 1-bit ADC is applied to detect the high/low state of node V_{mid} at the end of the off-time phase. A simple digital block (up/down counter) receives the ADC's information and adjusts the digital code which carries the information about how much the off-time should be corrected. A DTC is controlled by the digital code and generates additional time to correct the off-time. The tuning range of this block is $-15ns\sim+15ns$. The minimum tuning step is $1ns$.

Since only the high/low state of V_{mid} need to be detected, the 1-bit ADC can be implemented by a CMOS D flip-flop. Compared with an analog ADC, this method is more power efficient. The circuit of the 1-bit ADC is illustrated in Figure 4-16. V_{p} is the drive signal of the PMOS power switch transistor. When V_{p} turns from low to high, the high-side power switch is turned open which means the off-time ends and the dead-time starts. At this moment, the drain voltage of the PMOS power switch transistor V_{mid} will have a positive voltage jump or a negative voltage jump according to the state (positive/negative) of the inductor current. The working principle has been explained in Section 3.6 by Figure 3-23. Hence, V_{mid} is connected to the D terminal and V_{p} is used as the clocking signal for the D flip-flop. In addition, the D flip-flop will be reset by V_{n} in the on-time phase. V_{n} is the drive signal of the low-side NMOS power switch transistor.

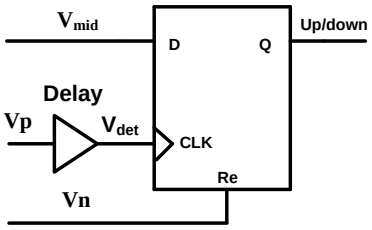

Figure 4-16: A D flip-flop 1-bit ADC.

However from the simulation result, an unexpected ringing is seen at node V_{mid} when the boost converter is switched from the off-time phase to the dead-time phase (as shown in Figure 4-17). Because node V_{mid} is also connected to the large inductor, the ringing is perhaps caused by the effect of the inductor and some other parasitic capacitors. The specific reason of this ringing will be studied further in future works. The ringing will perhaps cause a false reading of the inductor current at the end of the off-time and result in an opposite ZCS adjustment. Comparing Figures 4-17 and 3-23, we can find the reason of the false reading. For instance, to compare Figure 4-17a with 3-23a, if the voltage detection happens on the top half-wave position, the off-time will be further increased thus making an opposite adjustment.

In this work, the problem is solved by adding a short delay between the clocking

terminal of the D flip-flop and the signal V_p. Figure 4-17 shows this solution. The state (positive/negative) of the inductor current at the beginning of the dead-time can be illustrated by the original direction of the ringing waveform. If the inductor current has dropped below zero at the end of the off-time, the starting direction of the ringing waveform will be negative (Figure 4-17a). On the contrary, if the inductor current is still higher than zero when the off-time ends, the starting direction of the ringing will be positive (Figure 4-17b). Therefore a careful setting of the delay time can guarantee the correct reading of the inductor current state (positive/negative) at the end of the off-time thus guaranteeing the function of the ZCS adjustment block.

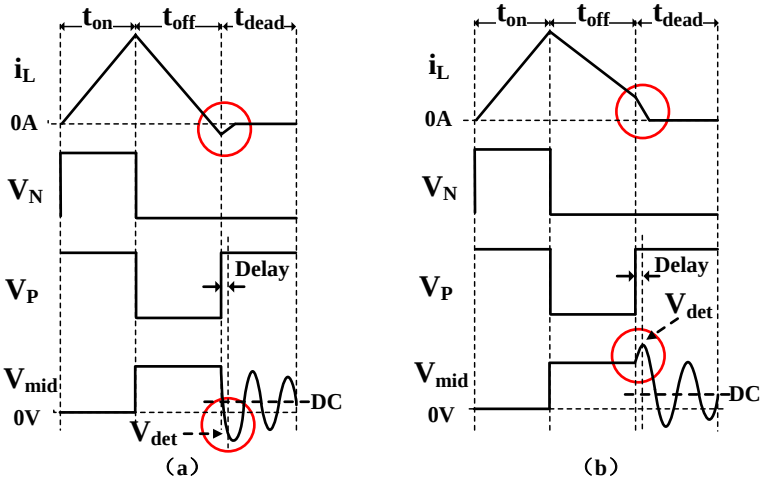

Figure 4-17: Voltage detection for an overlong or insufficient off-time.

The output signal of the 1-bit ADC presents the state of the inductor current at the end of the off-time. If the output is high, it means the inductor current at the end of the off-time is positive, thus the duration of the off-time should be increased in the next cycle. If the output is low, it means the inductor current at the end of the off-time is negative and the off-time should be decreased in the next cycle. An up/down counter can be applied to read the output signal of the 1-bit ADC and to adjust the off-time. According to the analysis in Section 3.6, the up/down counter will output a 5-bit binary code to control the DTC. A general up/down counter is applied in this work. When it is reset, the initial state of the output signal is 10000. If the output signal of the counter exceeds the range (11111), the counter will be automatically reset to the initial state.

The digital code output from the up/down counter is applied to control a DTC to calibrate the off-time for ZCS adjustment. From the discussion in last section, we know the off-time is generated by applying a current (i_{off}) to charge a capacitor (C_{off}) (Figure 3-a1). Hence, the ZCS adjustment block can adjust either the charging current i_{off} (current mode) or the charged capacitor C_{off} (capacitor mode) to achieve the off-time calibration. Then the off-time generating equation will be changed to:

$$\text{Current mode:} \qquad t_{\text{off}} \pm t_{\text{ad}} = \frac{C_{\text{off}}}{i_{\text{off}} \pm i_{\text{ad}}} \times V_{\text{in}} \tag{4.9}$$

$$\text{Capacitor mode:} \qquad t_{\text{off}} \pm t_{\text{ad}} = \frac{C_{\text{off}} \pm C_{\text{ad}}}{i_{\text{off}}} \times V_{\text{in}} \tag{4.10}$$

To achieve 1*ns* minimum tuning step for the ZCS adjustment ($t_{ad\_lsb} = 1ns$), 1 LSB of the DTC should be $100nA$ ($i_{ad\_lsb} = 100nA$) in current-mode or $25fF$ ($C_{ad\_lsb} = 25fF$) in capacitor mode. A comparison of these two methods on accuracy can be made dependent on the matching formulas in TSMC-40nm technology files. By hand calculation, the accuracies of 1 LSB adjustment for the current mode ($\partial(\Delta I_{\text{off\_lsb}})/\partial(I_{\text{off\_lsb}})$) and for the capacitor mode ($\partial(\Delta C_{\text{off\_lsb}})/\partial(C_{\text{off\_lsb}})$) are both about 1%. Although the results show the capacitor mode is a little better (about 0.2%) than the current mode, the difference is rather small. In terms of area, a 1 LSB tuning capacitor (25*fF*) occupies about $20\mu m^2$ area, but a 1 LSB tuning current source (100*nA*) just needs less than $0.5\mu m^2$ area. So the current-mode DTC is much better than the capacitor-mode DTC with respect to area. The power consumption of the capacitor-mode DTC should be undoubtedly less than the current-mode DTC because it is theoretically free of static current. But the power consumption of the current-mode DTC is also relatively small compared with the total power loss of the whole converter system (its maximum static current is just 1.5μA). A comparison chart of these two methods is listed in Table 4.3. Under the consideration of accuracy, area and power consumption, the current-mode DTC is finally employed in this work. Figure 4-18 illustrates the schematic of a current-mode DTC which is implemented by adding a current-steering DAC in the off-time generator. The current-steering DAC is applied to generate the additional time for the off-time calibration. The current-steering DAC is based on an array of matched current sources which are unity code or binary weighted.

Table 4.3: Comparison between the current-mode DTC and the capacitor-mode DTC

	Accuracy	**Area**	**Power consumption**
Current mode	*A little worse*	*Much smaller*	*Larger but acceptable*
Capacitor mode	*A little better*	*Much larger*	*Smaller*

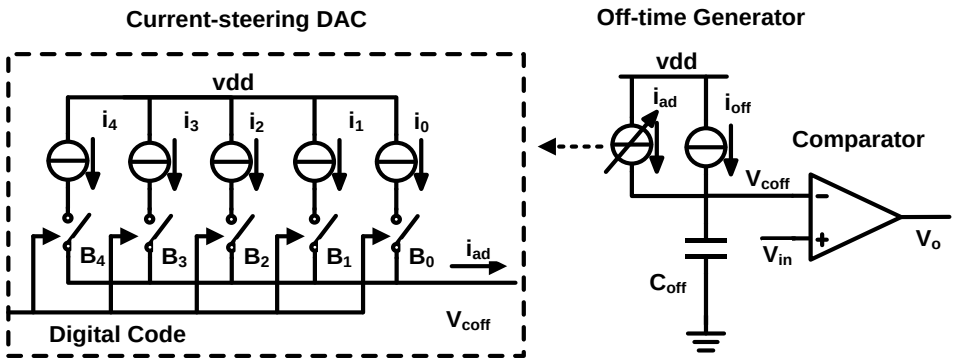

Figure 4-18: Current-mode DTC for the off-time calibration.

As discussed before, the up/down counter outputs a 5-bit binary code to control the DAC. However, there will be some problems existing in a fully binary-controlled DAC. As mentioned in [1], the monotonicity cannot be guaranteed, the DNL errors and the glitch energy are both large. By contract, a thermometer-controlled DAC with only unit elements can have better performance at a time. Since the thermometer-controlled DAC only changes one bit in each reaction, the monotonicity can be guaranteed. Moreover, for a binary-controlled DAC, the current branch controlled by high-order digital codes requires to generate large current which will cause large glitch energy and DNL error. But for a thermometer-controlled DAC, because each current branch produces an equal amount of current, which is not large, the glitch energy and DNL error will be smaller than for a binary-controlled DAC. However, this implementation also has its drawbacks such as the requirements on more control signals and more area. Hence, in order to take the advantages of two structures, a segmented structure is applied to implement the current-steering DAC.

The n-bit input digital code is segmented into *m* less significant bits (LSBs) and (*n*-*m*) most significant bits (MSBs). The m-bit LSBs are used to control the binary weighted current branches and the (n-m)-bit MSBs are decoded from binary to thermometer to control the unary current branches. By applying this structure, not only the problem of non-monotonicity, large glitch energy and large DNL error can be solved by the high-order code thermometer control, but also the number of control signals and area can be effectively reduced by low-order code binary control. The ratio of the number of MSBs (n-m) over the number of LSBs (m) is named segmentation. For conventional designs, optimum segmentation is 75% [2]. In [1], a segmentation of 90% is used for good performance in high-speed design. In this work, the 5-bit binary output of the up/down counter can be segmented to 3/2 (60%) or 4/1 (80%) to control the DAC. Under consideration of simple implementation and acceptable performance, the segmentation is finally determined as 60%, which means the high-order 3 bits is decoded to thermometer and the low-order 2 bits are remained in binary. Figure 4-19 illustrates the final implementation of the ZCS adjustment block in system level.

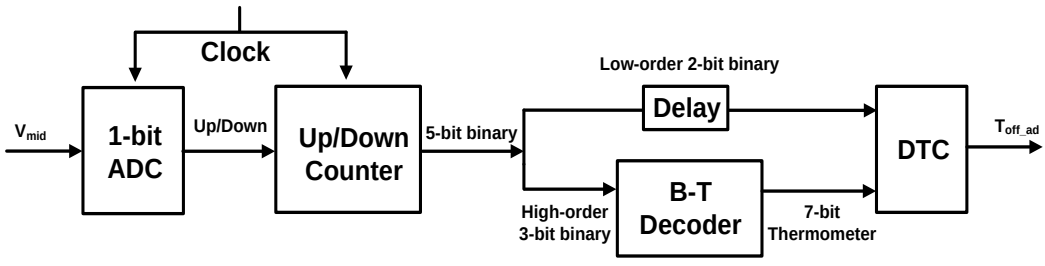

Figure 4-19: System-level diagram of the ZCS adjustment block

Due to the segmentation mechanism, the input signal of the DAC is 2-bit binary

weighed and 7-bit unary weighed. The schematic of the two current branches controlled by the 2-bit binary is shown in Figure 4-20. In here, two NMOS transistors M_{b1} and M_{b2} are used as current mirrors to generate $100nA$ (1 LSB) and $200nA$ (2 LSBs) current in each branch. Since these two branches generate the two minimum current signals in the DAC, the accuracy of these two current mirrors is the most important specification. The accuracy of a MOS transistor-based current mirror is mainly determined by three parameters of the copying transistor: generated current, overdrive voltage and area. There have been a lot of studies on their relationship. The detailed equations are not described here. In general, the larger these three parameters are, the better the current mirror's accuracy is. In this work, since the target currents have been determined, the controllable parameters are only the overdrive voltage and the area. But due to the quite small generated currents (hundreds of nAs), a large overdrive voltage means a small width to length ratio (*W/L*), and the parasitic capacitors caused by large area will affect the performance of the current mirror in high-speed operating condition (several MHz). Therefore, in the trade-off, the overdrive voltage is set to about $80mV$ and transistors with relatively small size are used for M_{b1} and M_{b2} in the end. The detailed parameters are listed in Table 4.3.

As shown in Figure 4-20, differential pairs of NMOS transistors are used as the switches to control each current branch connected to the output of the DAC (V_{coff}) or not. By applying this method, a constant current occurs in every current branch, but the current flows to different places under the control of two complementary switches. The drain voltage of each current mirror transistor (V_x, V_y) is fixed, thus cancelling the effect of V_{ds} variation on the generated current. Because these two current branches generate the minimum current signals, the additional power consumption due to the constant current can be ignored. The accuracy is more important than the power consumption for these two current branches. The size of these switch transistors should be small so as to reduce the parasitic capacitors for high-speed application. The detailed parameters of these transistors are listed in Table 4-5.

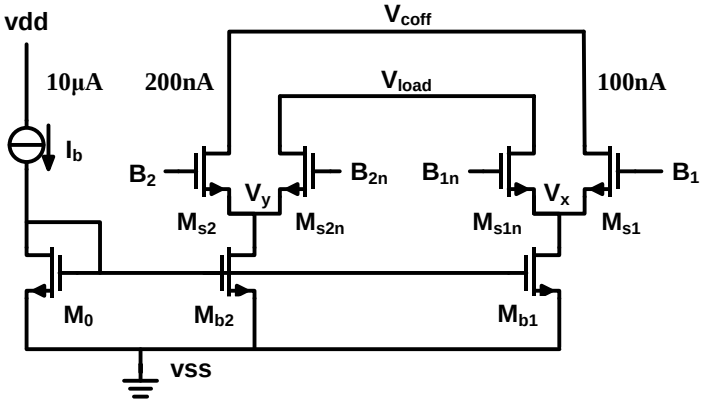

Figure 4-20: Two current branches controlled by 2-bit binary digital code in the DAC.

The schematic of the other seven unary current branches is shown in Figure 4-21. Each branch generates the same current ($400nA$) which represents 1 MSB in the DAC. All branches use the same structure and transistors. Because the currents in these branches are relatively large, for a high efficient, a single transistor is used as the switch in each branch rather than the complementary structure applied in the binary-controlled branches. The detailed parameters of the transistors are listed in Table 4-4.

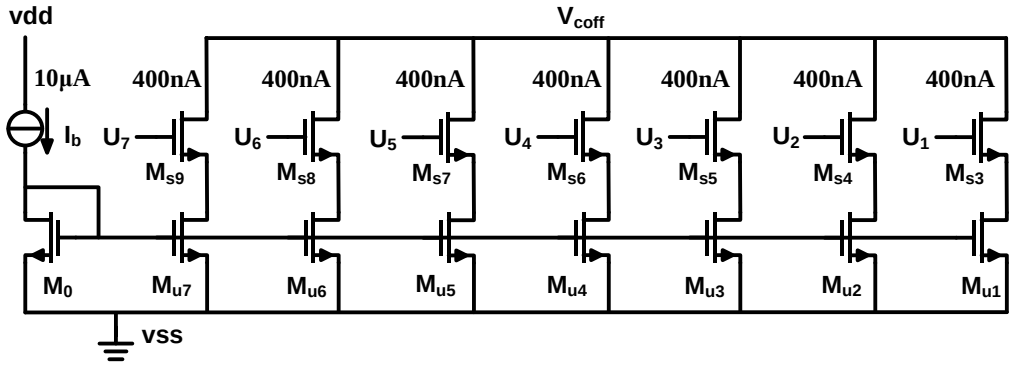

Figure 4-21: Seven current branches controlled by 7-bit unary digital code in the DAC.

Table 4-4: Parameters of the transistors in the DAC

	M_0	M_{b1}	M_{s1}	M_{s1n}	M_{b2}	M_{s2}	M_{s2n}	M_{u1}~ M_{u7}	M_{s3}~ M_{s10}
L	*2μ*	*2μ*	*0.1μ*	*0.1μ*	*2μ*	*0.1μ*	*0.1μ*	*2μ*	*0.1μ*
W	*0.2μ*	*0.2μ*	*0.6μ*	*0.6μ*	*0.2μ*	*0.6μ*	*0.6μ*	*0.2μ*	*0.6μ*
M	*100*	*1*	*1*	*1*	*2*	*1*	*1*	*4*	*1*

4.5 Comparator

No matter which kind of control technique, there will necessarily be a comparator in the control system of a DC-DC converter. For instance, as mentioned in Section 3.2, in the voltage-mode control or the current-mode control system, a comparator is used to compare the output of the error amplifier with a ramp signal, and then outputs a signal to adjust the duty cycle of the PWM signals which control the power switches. In a PFM ripple-based control system, the comparator plays a more important role since it replaces the function of the error amplifier to regulate the output voltage of the DC-DC converter. A comparator continuously monitors the output of the DC-DC converter. If the output voltage of the converter drops or rises across the reference voltage, the comparator will send an active signal to the Digital Logic blocks and then shift the operating phase (on-time, off-time or dead-time) of the DC-DC converter. The specific working principle

has been described in Section 3.4 and Section 4.1.

In this work, since the PFM ripple-based control technique is applied, no error amplifier exits in the control system. The output voltage of the boost converter is regulated by a comparator. For the comparator in this application, some characteristics should be considered during the design. The most important one is the propagation delay. Figure 4-22 illustrates the effect of the comparator delay on the performance of the boost converter. A large comparator delay will make the triggering point far away from the comparison point thus increasing the dead-time. When the boost converter works at a light load condition, a large comparator delay will not give much trouble to the boost converter, since the additional dead-time caused by comparator delay is a small portion of the whole dead-time. In this case, only the DC (average) value of the output voltage of the boost converter will be slightly decreased as shown in Figure 4-22 (a). So it means that just the output regulating accuracy of the boost converter is impaired by the large comparator delay at light load condition. However, when the boost converter works with a high load, if the comparator delay is too large, besides the regulating accuracy, even the functionality of the boost converter will be destroyed. As shown in Figure 4-22 (b), if the dead-time is too long such that the energy discharging in the dead-time and the on-time has been larger than the energy charging in the off-time, the output of the boost converter cannot stay in a steady state, which means the stability of the converter has been interfered by the large comparator delay. Therefore, the propagation delay of the comparator should be designed to be a small value.

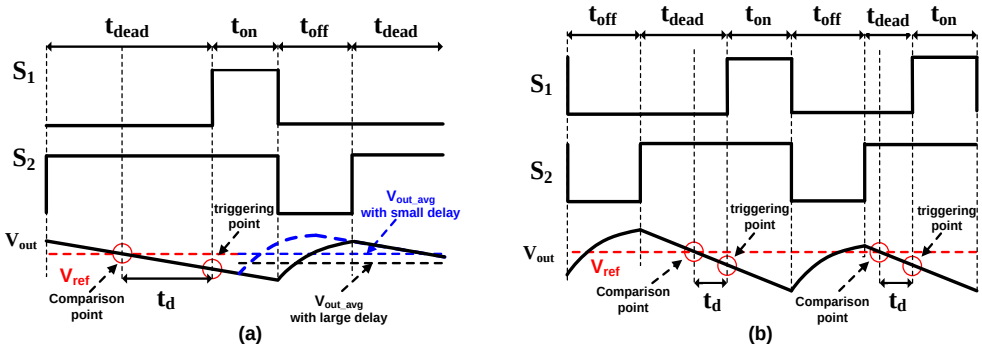

Figure 4-22: Comparator delay effect under (a) low load and (b) low load.

Apart from the propagation delay, the uncertain transition region of the comparator which is determined by the noise level should be controlled in a safe range. In this design, the comparator is applied to compare the small output ripple of the boost converter with a reference DC voltage, and the minimum output ripple is only about *10*mV. Therefore, the detection range of the comparator should be much smaller than 10mV. In addition, since in this design, the comparator is the only block which needs to constantly operate in the whole control system besides the biasing block, its power consumption takes up a large portion of the total power consumption. In order to design a boost converter with very high power conversion efficiency, after ensuring the functionality of the comparator, its

power consumption should be optimized as much as possible.

In this work, besides the comparator used for the output regulation, there are still two comparators existing in the time generators to control the duration of the on-time and the off-time. Their working principle has been described in Section 4.3. For these two comparators, due to their different application, the functionality and the performance are less sensitive to the propagation delay and the noise compared to the other comparator. Hence, the static current in these two comparators could be set at a smaller value to reduce the power consumption. As a consequence, the propagation delays will be larger.

In this work, a two-stage, open loop comparator is applied in the control system of the boost converter. The schematic of the comparator is shown in Figure 4-23. For the comparators applied in the time generators, since the comparison point is about $0.4V$, a differential pair of PMOS transistors can be used as the input stage. For the comparator applied for the output voltage regulating, as the output voltage of the boost converter can be dropped down by a voltage divider, the comparison point can also be set at about $0.4V$. For simplification, the comparator in the two applications can use the same structure (shown in Figure 4-23) but with different bias currents for different propagation delays.

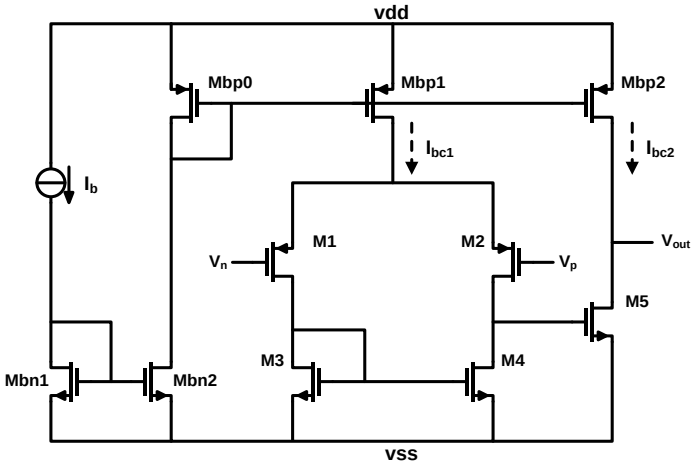

Figure 4-23: Schematic of the comparator.

In the schematic of the comparator, transistors M1 and M2 are the differential input pairs of the first stage. Due to a low bias current, these two transistors work in the subthreshold region. Transistor M5 is the input of the second stage. It works in the saturation region. The poles of the comparator caused by two stages can be expressed as:

$$p_1 = \frac{g_{ds\_M2}+g_{ds\_M4}}{C_1} \tag{4.11}$$

$$p_2 = \frac{g_{ds\_M5}+g_{ds\_Mbp2}}{C_2} \tag{4.12}$$

In which C_1 is the sum of the capacitors connected to the output of the first stage and C_2 is the sum of the capacitors connected to the output of the second stage. As a general knowledge, the open loop amplifier which works as a comparator should have a large

bandwidth. Hence, poles p_1 and p_2 should be at high frequency.

As mentioned above, for different applications, due to the different limitation for the propagation delay, the bias currents are set at a different value. For a short propagation delay, the bias currents (I_{bc1}, I_{bc2}) of the comparator which is used for the output regulation are set at $2\mu A$. As a result, the effect of the comparator delay to the accuracy of the output voltage regulation is very weak. After a trade-off between the acceptable propagation delay and power consumption, the bias current (I_{bc1}, I_{bc2}) of the comparators which are used in the time generators are set at $0.2\mu A$.

4.6 Reference Current Generator

In the control system of the boost DC-DC converter designed in this work, a precise and stable current reference is indispensable, not only for the time generators to generate pulse signals with desired duty cycles to drive the power switches (Section 4.2), but also for the current-mode DAC in the ZCS adjustment block to slightly calibrate the off-time (Section 4.4). As we know, many external factors can affect the accuracy of the generating current, of which temperature and the supply voltage (V_{dd}) variation are two dominant ones. Hence, to design a low power reference current generator which is in sensitive to temperature and supply voltage (V_{dd}) variations becomes a crucial task.

In order to suppress the temperature effect on the generating current, the general idea which has been widely applied is adding a positively scaled (PTAT) current to a negatively scaled (CTAT) current [3]. By setting these two temperature compensating currents in a proper ratio, the temperature effect can be canceled and the total current will be, to a first order, independent of temperature.

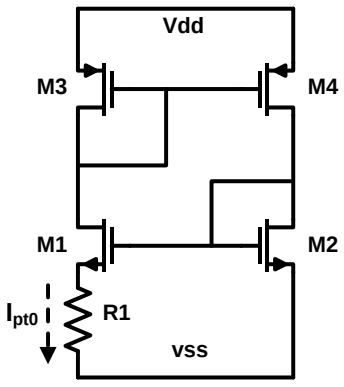

Figure 4-24: PTAT current source.

The PTAT current can be generated by the circuit shown in Figure 4-24. The transistors M1 and M2 work in the subthreshold saturation region, and the transistors M3

and M4 work in strong inversion saturation region as current mirrors. For a subthreshold MOS transistor, there is:

$$I_D = I_0 exp\frac{V_{GS}}{\zeta V_T} \tag{4.13}$$

Accordingly, for M1 and M2, there are:

$$V_{GS1} = \zeta V_T \ln(\frac{I_{D1}}{I_{0\_M1}}) \tag{4.14a}$$

$$V_{GS2} = \zeta V_T \ln(\frac{I_{D2}}{I_{0\_M2}}) \tag{4.14b}$$

Since M1 and M2 compose a current mirror, their source currents are in a ratio of:

$$\frac{I_{D2}}{I_{D1}} = \frac{I_{S4}}{I_{S3}} = \frac{S4}{S3} \tag{4.15}$$

in which, S3 and S4 are the aspect ratios of the transistor M3 and M4. Then, the current flowing through the resistor R1 can be expressed as:

$$I_{pt0} = \frac{V_{GS2} - V_{GS1}}{R_1} = \frac{KT}{q}\ln(\frac{S1}{S2}\cdot\frac{S4}{S3}) \tag{4.16}$$

Therefore, the current I_{pt0} generated in this part is a PTAT current.

The CTAT current can be generated based on the conclusion proposed in [3]. It says that, after biasing a constant drain current, the gate-source voltage of a MOSFET which works in subthreshold region, decreases linearly with temperature. An approximation equation between the gate-source voltage (V_{GS}) and temperature (T) is obtained in [3]:

$$V_{GS}(T) \approx V_{GS}(T_0) + K_G(\frac{T}{T_0} - 1) \ , \tag{4.17}$$

where

$$K_G \cong K_T + V_{GS}(T_0) - V_{TH}(T_0) - V_{OFF} \tag{4.18}$$

For typical values of K_T and V_{OFF} which are BSIM3v3 model parameters, K_G is a negative quantity [3] thus causing the voltage V_{GS} to decrease with temperature. Therefore, a CTAT current I_{nt0} can be obtained by applying the CTAT voltage V_{GS} on a resistor, which can be expressed as:

$$I_{nt0} = \frac{V_{GS}(T)}{R} = \frac{V_{GS}(T_0)}{R} + \frac{K_G}{R}(\frac{T}{T_0} - 1) \tag{4.19}$$

A simple circuit to combine the PTAT current and the CTAT current for getting a temperature independent current is shown in Figure 4-25, which was proposed in [4]. This implementation method is much simpler than the circuit proposed in [3]. In this circuitry, M1, M2, M3 and M4 compose the PTAT current generator, and the generating PTAT current I_{pt0} is copied to the output by the current mirror composed of M3 and M9. In addition, M5, M6, M7 and M8 compose the CTAT current generator and the generating CTAT current I_{nt0} is copied to the output by the current mirror composed of M8 and M9. Then, the output current I_b can be expressed as:

$$I_b = \frac{S9}{S3}I_{pt0} + \frac{S10}{S8}I_{nt0} = K_1(T) + K_2(T) \tag{4.20}$$

If the derivative of the output current I_b with respect to temperature T is zero ($\partial I_b/\partial T = 0$), the output current I_b is independent of temperature. This can be done by a proper setting of the ratio of the PTAT current I_{pt0} and the CTAT current I_{nt0} .

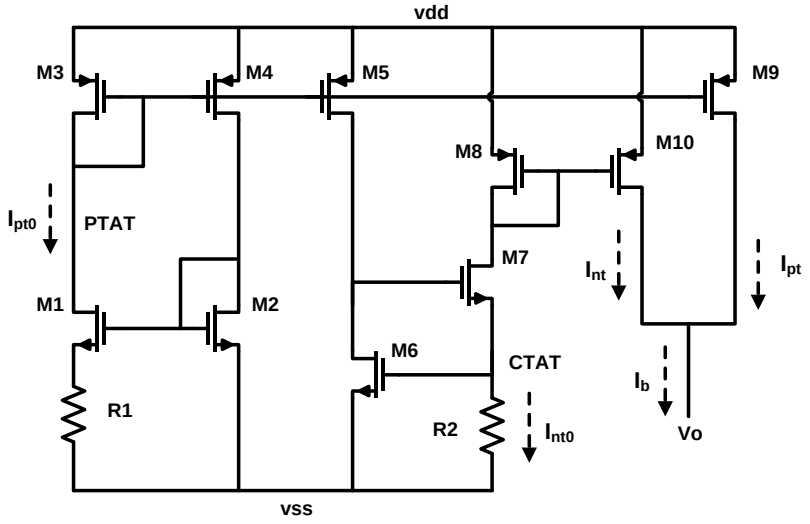

Figure 4-25: Combination of a PTAT current source and a CTAT current source [4].

Another factor that can affect the accuracy of the generating current is the supply voltage (V_{dd}) variation. Due to the channel-length modulation effect, if the source-drain voltage on a transistor is changed, the drain current of this transistor will also be different. The supply voltage (V_{dd}) variation can lead the PTAT current generator and CTAT current generator to make a positive response, which means, if there is an increment on the supply voltage (V_{dd}), both the PTAT and CTAT currents will be increased, and vice versa.

The supply voltage (V_{dd}) variation effect can be suppressed by just adding an N-time of the PTAT current to the CTAT current generator [4]. The detailed implementation is shown in Figure 4-26. The transistor M11 composes a current mirror with the transistor M3, which adds an N-time of the PTAT current I_{pt1} ($I_{pt1} = N \cdot I_{pt0}$) to the CTAT current generator. After adding this block, the current flowing through the transistor M8 is the sum of the CTAT current I_{nt0} and the N-time of the PTAT current I_{pt1}. The expression of the final output current I_b (equation 4.20) will be modified to:

$$I_b = \frac{S9}{S3} I_{pt0} + \frac{S10}{S8}\left(\frac{V_{GS6}}{R2} - N I_{pt0}\right) \tag{4.21}$$

By taking the derivative of equation (4.21) with respect to V_{dd}, there is:

$$\frac{\partial I_b}{\partial Vdd} = \left(\frac{S9}{S3} - \frac{S10}{S8} N + \frac{\partial (V_{GS6}/R2)}{\partial Vdd}\right) \times \frac{\partial I_{pt0}}{\partial Vdd} \tag{4.22}$$

Due to equation 4.14, the derivation of $(V_{GS6}/R2)$ with respect to Vdd is:

$$\frac{\partial (V_{GS6}/R2)}{\partial Vdd} = \frac{\zeta V_T}{I_{D6} R2} \frac{\partial I_{D6}}{\partial Vdd} = \frac{\zeta V_T}{I_{D6} R2} \frac{S5}{S3} \frac{\partial I_{pt0}}{\partial Vdd} \tag{4.23}$$

Finally, we can obtain that:

$$\frac{\partial I_b}{\partial Vdd} = \left(\frac{S9}{S3} - \frac{S10}{S8}N + \frac{S10}{S8}\frac{S5}{S3}\frac{\zeta V_T}{I_{D6}R2}\right) \times \frac{\partial I_{pt0}}{\partial Vdd} \tag{4.24}$$

The negative item in Equation 4.24 can make that the expression in the bracket becomes equal to zero, thus causing the derivative of the output current with respect to the supply voltage variation to zero ($\partial I_b/\partial Vdd = 0$). Therefore, the supply voltage variation effect on the output current I_b can be suppressed by this method.

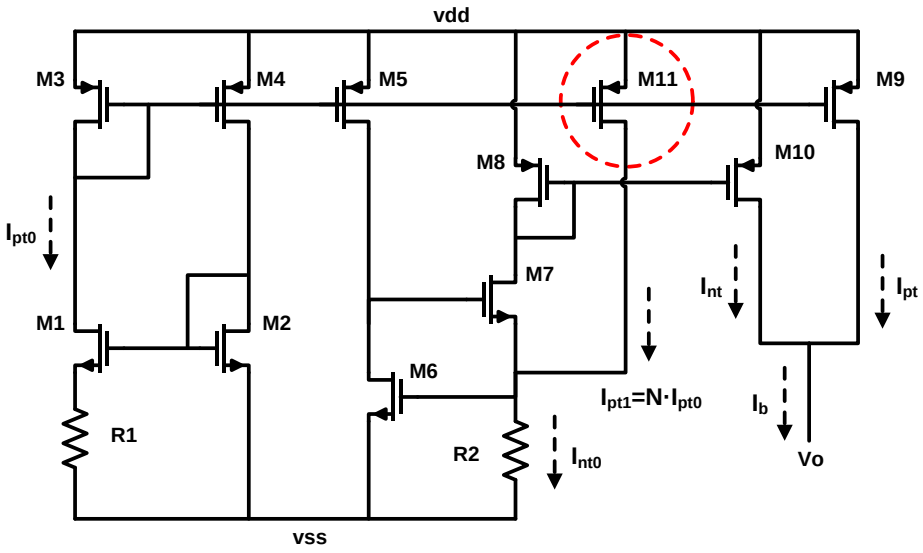

Figure 4-26: Final schematic of the reference current generator.

Based on Equations 4.20 and 4.21, the output current I_b can theoretically be independent of temperature and supply voltage variation. But in real work, since many parameters in the circuit are correlative to each other, it is different to find out the balance. For example, a larger N for the additional current I_{pt1} is good to suppress the supply voltage variation effect, but as a result, it will lead to a bad temperature compensation behavior.

According to the result given in [4], if the target reference current is 1μA, the effect of the supply voltage variation on the reference current should be about 0.009μA/V and the temperature effect on the reference current should be 0.027μA peak-to-peak for temperature variation from -20 °to 120 °. But in this research, due to time limitation, the circuit was not set in an optimal condition. The simulation results show that the supply voltage variation on the reference current is about 0.07μA/V, and the temperature effect on the reference current is about 0.29μA peak-to-peak for temperature variation from -20 ° to 120 °. An easy method to properly set the parameters in the circuit should be studied in future work. The parameters of the transistors used in the work are shown in Table 4.5.

Table 4-5: Parameters of the transistors in this block.

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11
L (µm)	*4*	*4*	*4*	*4*	*4*	*4*	*4*	*4*	*4*	*4*	*2*
W (µm)	*160*	*4*	*4*	*4*	*3*	*125*	*125*	*2*	*3.2*	*2.3*	*1*
R1 = *160kΩ*						R2 = *300kΩ*					

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Chapter 5

Layout Design

5.1 Overview of the Layout Design

Due to the technology limitation and design consideration, not all components of the boost DC-DC converter are integrated on-chip in this work. At first, the $1\mu H$ inductor and the $220nF$ load capacitor are applied off-chip. The reason is that on-chip inductors or capacitors with such a large inductances or capacitances have large area and poor series resistance which will seriously reduce the efficiency of the boost converter. Secondly, for easy output voltage control, the voltage reference and the output voltage divider of the boost converter are implemented outside the chip as well, which means any required output voltage can be obtained by just changing the off-chip parameters. Moreover, the capacitor C_f applied to improve the noise immunity of the boost converter (discussed in Section 3.4) is also placed outside of the chip. As shown in Figure 5-1, the layout design just involves the circuits in the red square.

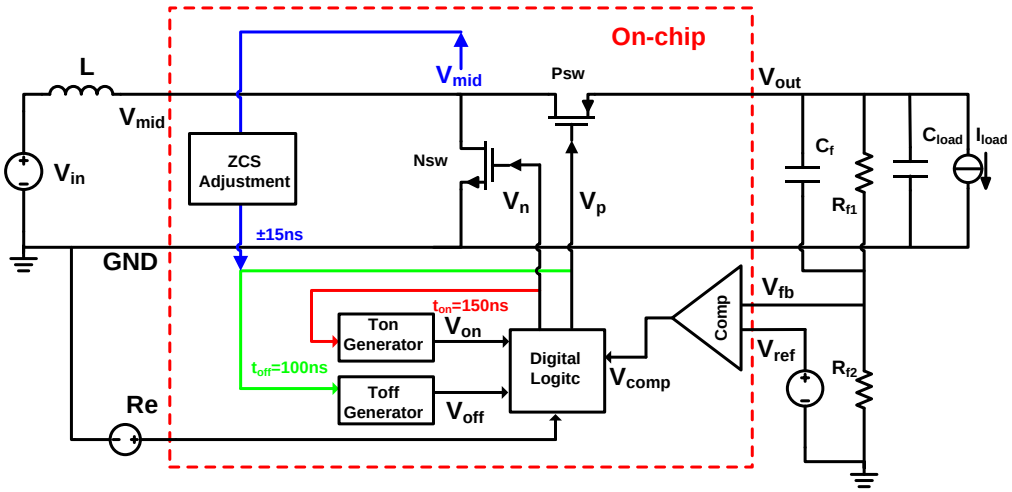


Figure 5-1: On-chip and off-chip parts of the boost DC-DC converter.

The final layout of the entire on-chip system of the boost DC-DC converter is shown in Figure 5-2. It includes two large power switch MOS transistors with buffers, three comparators, two time generators, a current mirror array, a reference and bias current generator, a ZCS adjustment block, a digital logic control block and some decoupling capacitors. During the whole layout work, only two parts of the boost converter require elaborate design because the functionality and the performance of the converter are very sensitive to their effects. One of them are the MOS transistors used as the power switches, and the other one is the current mirror array which includes the current-steering DAC applied in the current-mode DTC for the ZCS adjustment. Later in this chapter, detailed discussions will be given on the layout design of these two parts. As for the layout design of the other blocks, because no special skills are applied, no detailed description will be mentioned in the thesis.

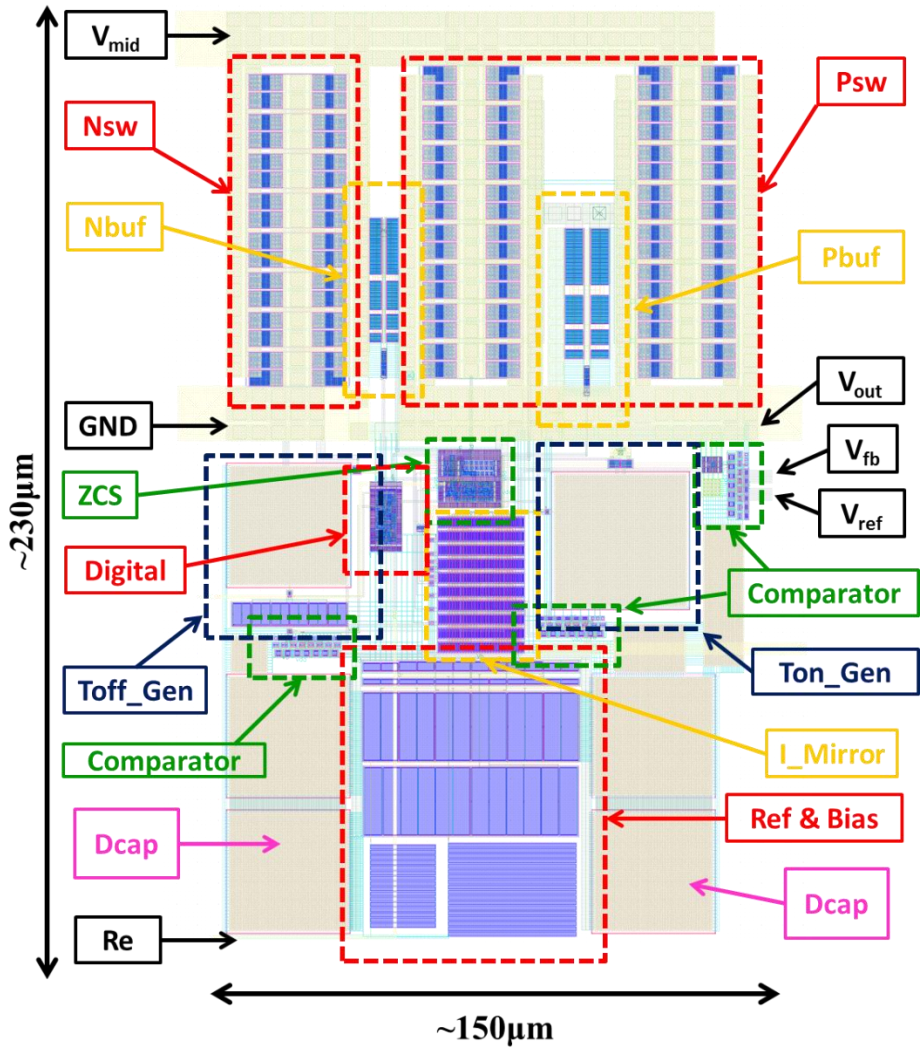


Figure 5-2: Layout of the entire on-chip part of the boost DC-DC converter.

5.2 Layout Design of the Power Switches

In Chapter 2, we have discussed the size of the MOS transistors used for the power switches in the boost converter. To achieve a very low turn-on resistance, the aspect ratios (W/L) of these MOS transistors should be very large. In this work, the final aspect ratios of the two MOS transistors used as power switches in the boost DC-DC converter have been shown in Table 2-1. So there are:

$$(\frac{W}{L})_n = 35840 \tag{5.1}$$

$$(\frac{W}{L})_p = 71680 \tag{5.2}$$

From the equations, we can find that the aspect ratios of the power switch transistors are extremely large. A problem consequently appears, that is, how to reasonably design the layout of the transistors with such high aspect ratios. Obviously, it is impossible to make it in the simplest structure as shown in Figure 5.3. Then, the finger structure can be applied to reduce the aspect ratio of each transistor unit. In the finger structure, a single transistor with an extremely high aspect ratio can be divided into many unit cells which connect with each other. But as shown in Figure 5.4, we can find that, if the aspect ratio of each unit cell is in a reasonable value, the number of the fingers will be very large. It means this structure is still unreasonable in terms of the space. Therefore, more advanced methods should be used to design the layout of the power switch transistors.

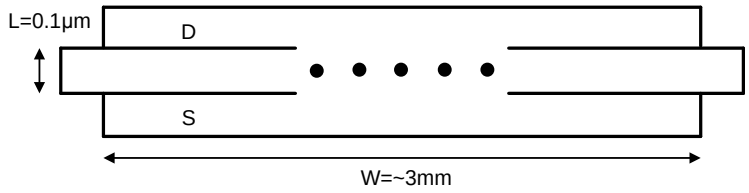


Figure 5-3: Transistor with a large W/L in the simplest structure.

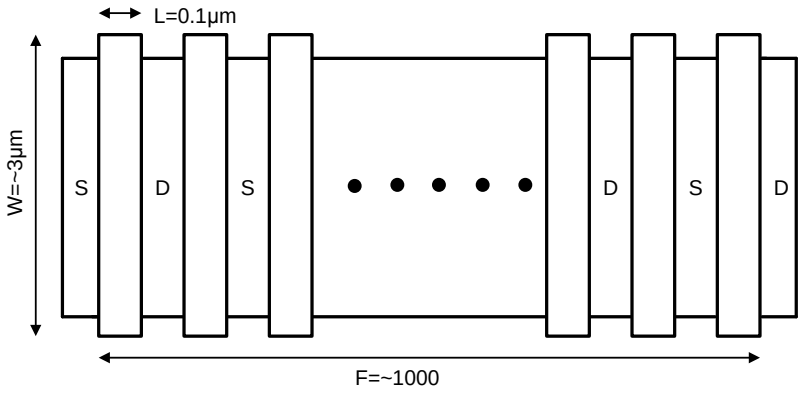


Figure 5-4: Transistor with a smaller W/L in the finger structure.

In this work, we segment the large power switch transistors into several independent small cells and place them in parallel (as shown in Figure 5.5). By using this approach, the layout design for the power switch transistors will be easily implemented. The reason is the transistor with a high aspect ratio has been segmented to N independent cells and the aspect ratio of each unit cell will be $1/N$ smaller. For example, N is set to be 32 in this work. For a unit cell of the NMOS power switch transistor, we only need to draw the layout of a transistor with an aspect ratio of $112\mu m/0.1\mu m$. By applying the finger structure, it is easy to design the layout of such a unit cell. The layout implementation of a unit cell is exhibited in Figure 5.6. In addition, an extra benefit can be obtained by using this structure, that is, the turn-on resistance of the power switch transistor will be reduced by the parallel structure. As mentioned in Section 2.2, since the static loss caused by the power switch transistor's turn-on resistance is a dominant factor in the loss mechanism, this approach can effectively improve the efficiency of the boost converter.

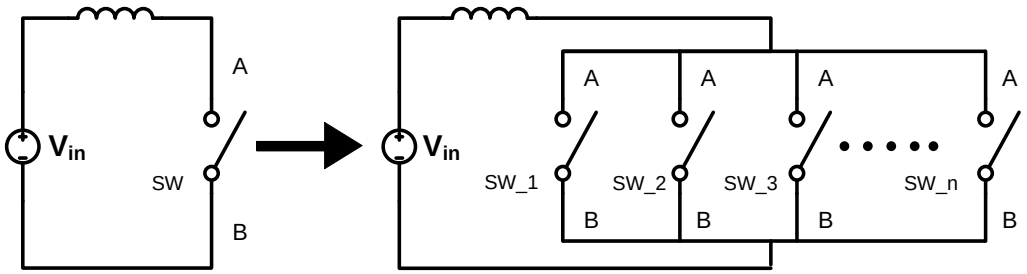


Figure 5-5: Segmentation of the large power switch transistor.

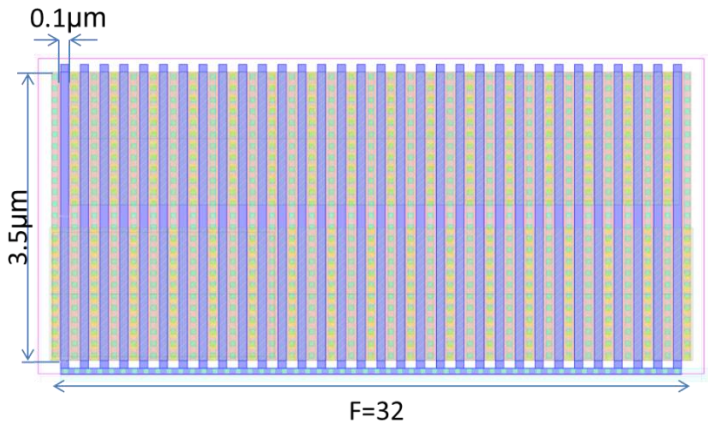


Figure 5-6: Unit cell of the power switch transistor.

After determining the size of each unit cell, the next step is to join the 32 unit cells together and connect them to the two terminals of the power switch. Since, in this design, the current flowing through the power switches is relatively large (about $60mA$), the relationship between the maximum tolerable current and the width of the Copper metal

wire is required to be considered in order to prevent the failure in terms of reliability. The equations of this relationship can be derived from the technical documents of TSMC 40nm technology [1]. For metal x ($x = 1\sim6$), there is:

$$I_{\max\_Mx} = 1.329 \times (W \times 0.9 - 0.008) \tag{5.3}$$

For metal y ($y = 7\sim8$), there is:

$$I_{\max\_My} = 3.04 \times (W \times 0.9 - 0.2) \tag{5.4}$$

The maximum current ($I_{\max}$) is defined as the maximum DC current allowed for metal lines, vias, or contacts. It is based on 0.1% point of measurement data at a 10% resistance increase after $100K$ hours of continuous operation at 110℃ [1]. As the currents flowing through the power switch transistors are in pulse wave, the effective DC current is equal to the average current which can be calculated as:

$$I_{avg} = \frac{1}{\tau} \times \int_0^{\tau} I(t)dt \tag{5.5}$$

For a current in a pulsed wave, the rules of the effective DC current (I_{avg}) are identical to the rules of the maximum current ($I_{\max}$) [1], which means the item $I_{\max}$ in Equations 5.3 and 5.4 can be replaced by I_{avg}.

According to the rules mentioned above, the widths of the wires used to connect the power switch transistor can be determined. In this work, for simplification, apply the same structure to implement the layout of the PMOS and NMOS power switch transistors. Since its size of the PMOS power switch transistor is two times of the NMOS power switch transistor, two identical cells in parallel are applied to implement its layout design. Therefore, we will just discuss the layout design for the NMOS power switch transistor.

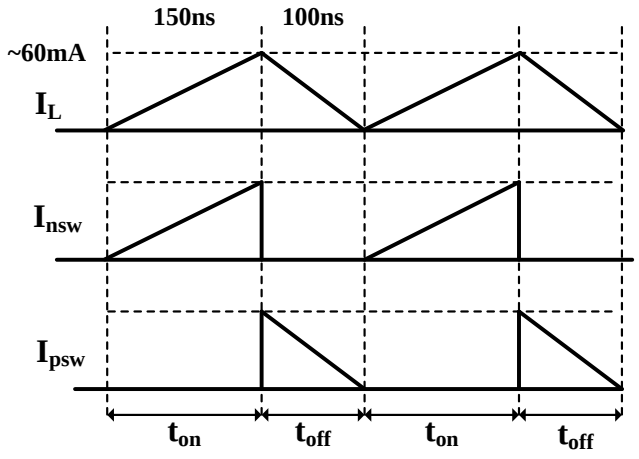


Figure 5-7: Currents flowing through the inductor and power switch transistors.

As we know, the current flowing through the NMOS power switch transistor is equal to the current flowing through the inductor during the on-time and the maximum duty cycle of the current pulse exits when the boost converter works in the boundary of CCM and DCM. As shown in Figure 5.7, the effective DC current flowing through the NMOS

power switch can be roughly calculated as:

$$I_{avg\_nsw} = \frac{1}{\tau} \times \int_0^{\tau} I_{nsw}(t)dt \approx 40mA \tag{5.6}$$

As discussion before, the NMOS power switch transistor with a high aspect ratio has been segmented into 32 unit cells. For each cell shown in Figure 5-6, the effective DC current should be:

$$I_{avg\_unsw} = \frac{I_{avg\_nsw}}{32} \approx 1.25mA \tag{5.7}$$

According to Equation 5.3, to tolerate a $1.25mA$ current, the width of the wire (metal x) should be more than $1.1um$. In this work, two metal wires with a width of $1.4um$ are used to connect the source and drain area of the transistor to the two terminals (A and B in Figure 5-5) of the power switch. In order to save area and increase the contact area, these two metal wires can be placed above the transistor as shown in Figure 5-8. By using this method, not only the area but also the resistance caused by the metal contacts can be effectively reduced.

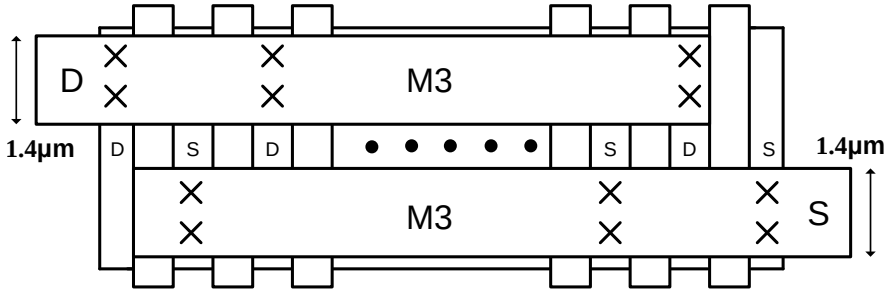


Figure 5-8: Source and drain connection of a unit transistor.

Two main power lines are required to connect the 32 unit cells together, one of which is used to connect all the drain terminals of the unit transistors with the inductor, and the other one is used to connect all the source terminals of the unit transistors to ground. The current tolerance of these two power lines have been calculated by using Equation 5.6, which should be more than $40mA$. But as the maximum width of the metal x wire is $4.95\mu m$ and the maximum width of the metal y wire is $13.2\mu m$ in this technology, according to Equations 5.3 and 5.4, we can obtain that the maximum tolerable current though a single-layer metal wire is:

$$I_{\max\_Mx} = 1.329 \times (4.95 \times 0.9 - 0.008) \approx 5.9mA \tag{5.8}$$

$$I_{\max\_My} = 3.04 \times (13.2 \times 0.9 - 0.2) \approx 35mA \tag{5.9}$$

It is obvious that only a single-layer metal wire cannot tolerate the current flowing through the power switches. Therefore, multiple-layer metal wires in parallel can be used to solve the problem. In this work, not only to increase the maximum tolerable current,

but also to reduce the resistance caused by the wide metal wires, five-layer metal wires are used for the power switch transistor. The structure of the five-layer metal wires is shown in Figure 5-9. Since the metal contact areas are very large, the resistances of the vias can be ignored. As shown in Figure 5-9 (a), a Metal 7 wire and a Metal 8 wire both having a width of $13\mu m$ are placed on two vertically parallel layers. Below these two metal wires, metal 4, 5 and 6 wires are separately placed on three vertically parallel layers. On each layer, three wires in the same metal and in the same width of $4\mu m$ are placed in horizontally parallel as shown in Figure 5-9 (b) (the area with dashed line). In this structure, the maximum tolerable current of the total wires is:

$$I_{\max\_total} = 3 \times \left(I_{\max\_M4}(4\mu m) + I_{\max\_M5}(4\mu m) + I_{\max\_M6}(4\mu m)\right) + I_{\max\_M8}(13\mu m) + I_{\max\_M7}(13\mu m) \approx 110mA \quad (5.10)$$

It is much larger than the maximum effective current flowing through the power switch transistor. Hence, the reliability of the metal wires can be guaranteed even the flowing current becomes larger.

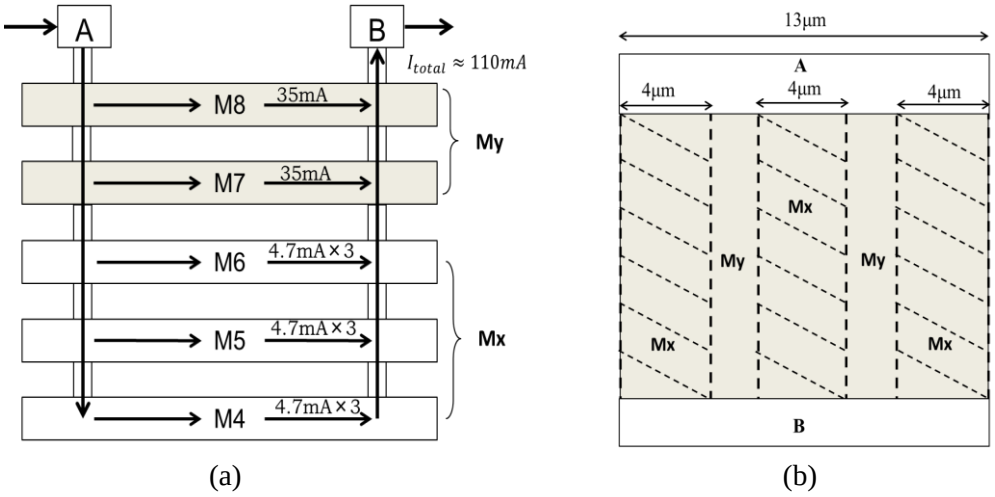
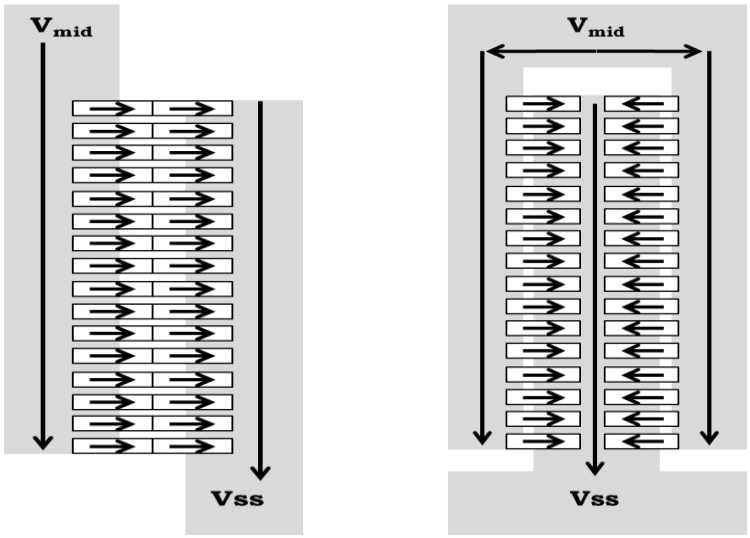


Figure 5-9: 5-layer metal wire, (a) cross-section view, (a) top view.

Figure 5-10 shows two topologies of the final layout implementation of the NMOS power switch transistor composed by 32 unit cells. Figure 5-10 (a) shows a general structure, in which, two power lines V_{mid} and V_{ss} are placed on two sides of the unit transistors. Figure 5-10 (b) shows an advanced structure which is similar with the finger structure. In the second structure, the two power lines V_{mid} and V_{ss} are closer to each other compared with the first one, which means the parasitic resistance will be lower and the area will be smaller. A comparison experiment between these two structures has been done. The simulation results show that the parasitic resistance caused by the metal connection wires for the first structure is about $70m\Omega$; and the parasitic resistance caused by the metal connection wires for the second structure is about $60m\Omega$. Since the

lower parasitic resistance can reduce the static power consumption thus improving the power efficiency for the boost converter, the final layout implementation of the power switch transistor in this work uses the structure shown in Figure 5-10 (b).



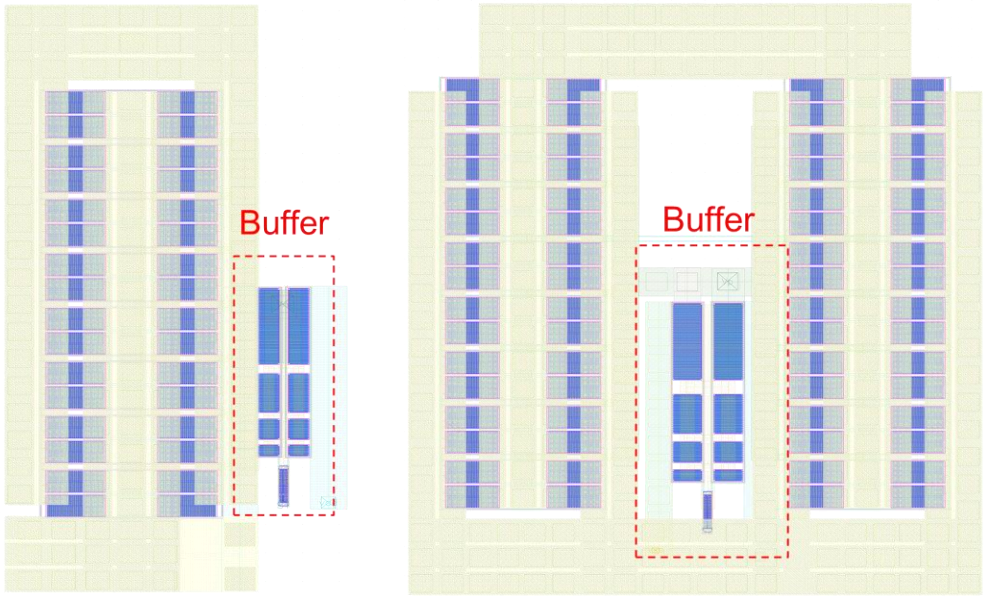
(a) (b)

Figure 5-10: Two topologies of the NMOS power switch transistor's layout.

For the transistor with a very high aspect ratio, the parasitic capacitance on the gate is also very large. From the simulation results, we can obtain that, in this design, the gate parasitic capacitance of the NMOS power switch transistor ($3584\mu m/0.1\mu m$) is about $1pF$, and the parasitic capacitance induced by the metal wires (shown in Figure 5-10 (b)) is about $1.5pF$. Thus, it means the signal used to turn the power switch on and off need to drive a $2.5pF$ load capacitor. In addition, the transition time of the power switch should be short, as much energy will be lost on the switch during the transition time. Therefore, a large buffer is required to drive the power switch. In this work, the transition time of the NMOS power switch (shown in Figure 2-10) is controlled within $100ps$, so according to the charging/dis-charging equation of a capacitor, the average driving current of the buffer should be about $25mA$. Although the driving current is quite large, since the buffer works in the high current condition only for a short while, the effective DC current of the buffer calculated by Equation 5.6 is quite small. Based on Equations 5.1 and 5.2, in which the item $I_{\max}$ is replaced by I_{avg}, the width (W) of the metal wire connecting the buffer and the gate of the power switch need not to be very large.

In this work, for design simplification, the size of the PMOS power switch transistor is determined as two times of the size of the NMOS power switch transistor. The layout implementation of the PMOS power switch transistor is to connect two identical unit cells in parallel, each of which is in the same structure as the NMOS power switch transistor. The final layouts of the NMOS and PMOS power switch transistors with buffers are

exhibited in Figure 5-11.



(a) (b)

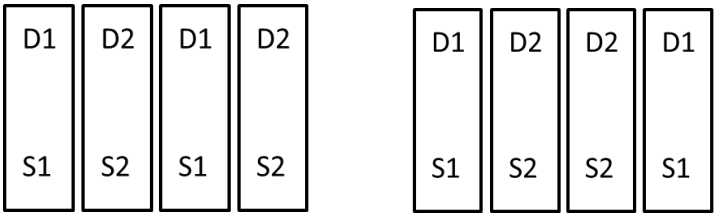
Figure 5-11: Final layout of the NMOS (a) and PMOS (b) power switches with buffers.

5.3 Layout Design of the Current Mirror Array

As discussed in Section 4.2, a $1\mu A$ current is required for the on-time generator to discharge the capacitor at a specific rate, and for the same purpose, a $10\mu A$ current is required for the off-time generator. As discussed in Section 4.3, since a current-mode DAC is used to calibrate the off-time, an accurate $0.1\mu A$ current is required for 1 LSB adjustment and an accurate $0.4\mu A$ current is required for 1 MSB adjustment. All these accurate currents required in the boost converter are generated by the current mirrors which scale up/down the $1\mu A$ reference current generated by the reference current generator. Therefore, to design current mirrors with high accuracy is a crucial mission for this work.

The accuracy of a transistor-based current mirror can be improved by using large transistors or increasing the overdrive voltage ($V_{GS} - V_{TH}$). Besides, a good layout can guarantee the matching characteristic of a current mirror thus improving the accuracy as well. A general layout technique for current mirrors is shown in Figure 5-12. Based on this technique, the layout topology for the current mirrors in this work is shown in Figure 5-13. The reference branch of the current mirror which has $1\mu A$ current is segmented to ten unit cells. These unit cells are placed in the middle of the structure. The minimum mirroring currents which are $0.1\mu A$ for 1 LSB of the DAC and $0.2\mu A$ for 2 LSB of the DAC (shown in Figure 4-20) are placed close to the center at the yellow squares in Figure

5-13. The mirroring currents which are $0.4\mu A$ for 1 MSB of the DAC (shown in Figure 4-21) are placed at the red squares in Figure 5-13. Because the accuracy level of the currents used for the DAC is superior, the current mirrors to generate these currents are placed in the center. For the currents used for the on-time generator (at the blue squares in Figure 5-13) and the off-time generator (at the purple squares in Figure 5-13), the accuracy is less important. The current mirrors to generate these currents can be placed farther away from the center.



(a) (b)

Figure 5-12: General layout techniques for current mirrors.

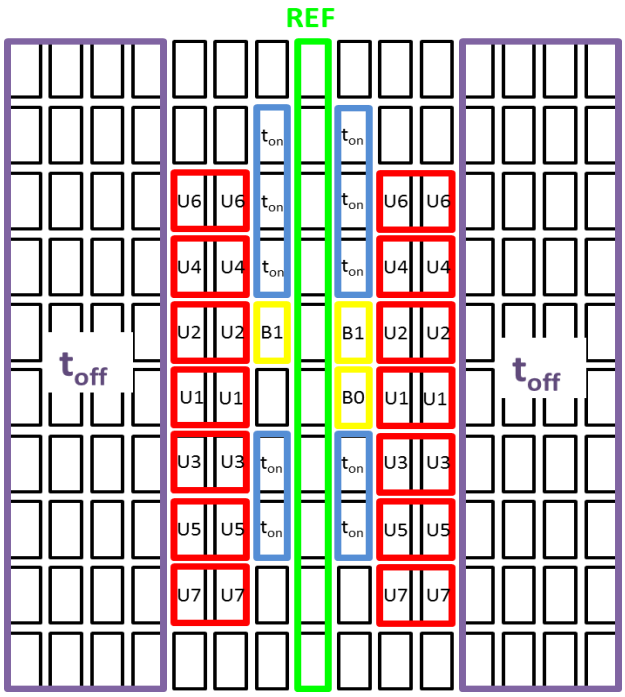


Figure 5-13: Layout topology for the current mirrors in this work.

The final layout of the current mirror array is shown in Figure 5-14. Besides the current mirrors mentioned before, there are still some other additional current mirrors to generate the bias current for the comparators in the boost converter circuit system. Because the accuracy of the bias current is not important, these current mirrors can be

placed at anywhere.

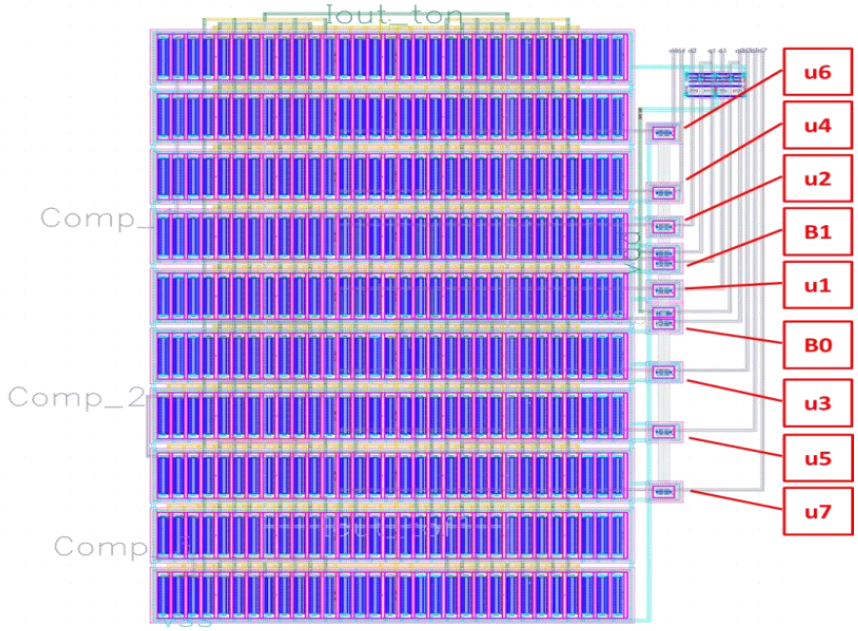


Figure 5-14: General layout techniques for current mirrors.

5.4 Conclusions of the Layout Design

Since the power switch transistors play a very crucial role in a DC-DC converter circuit system, usually transistors with very large aspect ratios and extremely wide connection metal wires are employed in the circuit in order to not only reduce the parasitic resistance for high efficiency but also increase the maximum current tolerance. As a consequence, much area is consumed by these parts (power switch, connection wires and driving buffers). The highlight of this layout design compared to other studies is that by using the method mentioned in Section 5.2, less area is used to implement power switches but also making the DC-DC converter with good performance.

A comparison of this design with some other outstanding low-power DC-DC converters published during recent years is shown in Table 5-1. For the boost DC-DC converter designed in this work, although the required maximum load current is $10mA$ (to charge the load battery), the simulation results demonstrate that this boost converter can also achieve an approximate 95% power conversion efficiency when it is loaded with a $12mA$ current. In order to evaluate these designs, we can use a figure of merit (FOM) which is expressed by Equation 5.11.

$$FOM = \frac{\eta_{\max} \times I_{\text{load\_max}}}{A} \tag{5.11}$$

Although the FOM of "Saurav [3]" is close to this design, its power conversion efficiency which is generally the most importance consideration for a DC-DC converter is relatively

low. Therefore, it can be concluded that this design is the best one.

Table 5-1: Comparison table of several low-power boost DC-DC converters

	This work	**Tzu-Chi [2]**	**Saurav [3]**	**Po-Hsiang [4]**
Technology	**40nm**	**0.25µm**	**45nm**	**0.35µm**
Consuming area (*A*) (Power switches, metal wires and buffers)	$\sim 100 \times 150\ \mu m^2$	$\sim 450 \times 550\ \mu m^2$	$\sim 200 \times 600\ \mu m^2$	$\sim 800 \times 1000\ \mu m^2$
Max. load current (I_{load_max})	12mA	50mA	100mA	450mA
Max. power conversion efficiency (η_{max})	95% *(Post-layout)*	95%	87%	95%
Figure of merit (FOM)	*0.76*	*0.2*	*0.73*	*0.53*

Bibliography

[1] TSMC 45/40 NM CMOS LOGIC AND MS_RF DESIGN RULE (Confidential).

[2] Tzu-Chi Huang; Chun-Yu Hsieh; Yao-Yi Yang; Yu-Huei Lee; Yu-Chai Kang; Ke-Horng Chen; Chen-Chih Huang; Ying-Hsi Lin; Ming-Wei Lee, "A Battery-Free 217 nW Static Control Power Buck Converter for Wireless RF Energy Harvesting With α -Calibrated Dynamic On/Off Time and Adaptive Phase Lead Control," *Solid-State Circuits, IEEE Journal of*, vol.47, no.4, pp.852,862, April 2012.

[3] Bandyopadhyay, S.; Ramadass, Y.K.; Chandrakasan, A.P., "20 μA to 100 mA DC–DC Converter With 2.8-4.2 V Battery Supply for Portable Applications in 45 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol.46, no.12, pp.2807,2820, Dec. 2011.

[4] Po-Hsiang Lan; Po-Chiun Huang, "A High Efficiency FLL-Assisted Current-Controlled DC-DC Converter Over Light-Loaded Range," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.59, no.10, pp.2468,2476, Oct. 2012.

Chapter 6

Simulation Results

6.1 Simulation Environment

The post-layout simulation results of the boost DC-DC converter designed in this project are presented in this chapter. Because this project missed the tape-out of our company, the designed boost DC-DC converter was not turned into a real production although the layout of the circuit had been implemented in TSMC 40nm CMOS process as shown in Figure 5.2. The functionalities and performances of this boost DC-DC converter are verified through the post-layout simulations which are made in Cadence Virtuoso.

The schematic of the test bench is shown in Figure 6-1. In here, an ideal voltage source is used to provide the input voltage for the boost DC-DC converter. Besides, as discussed in Section 3.5, the input voltage source is also connected to the time generators to determine the on-time and off-time for achieving the AOOT control. The load battery which is charged by the boost converter is modeled as a constant current source. When the battery is charged in the fast charging mode, the current of the equivalent constant current source is $10mA$. When the battery is charged in the slow charging mode, the current of the constant current source is $1mA$. The boost DC-DC converter is composed of an on-chip part and some off-chip parts. The on-chip part uses the extraction of the circuit layout shown in Figure 5.2. The off-chip parts include the voltage divider, the inductor and the load capacitor. According to the discussion in Section 3.4, the voltage divider consists of a $200fF$ capacitor (C_{f}), a $600k\Omega$ resistor (R_{f1}) and a $400k\Omega$ resistor (R_{f2}). Based on the selections of the inductor and the load capacitor explained in Section 2.3, the Spice models of the inductor "*CLF7045T-1R0N"* and the capacitor "*C0603JB0J223K030BC*" provided by TDK Company are used in the test bench. The values of the parameters of the inductor are shown in Figure 2-11. The values of the parameters of the capacitor are shown in Figure 2-12. Hereby, it should be emphasized that, as mentioned in Section 2.3, the load capacitor consists of ten separate capacitors connected in parallel. Finally, except for the input voltage source, another two voltage sources are used for the test. One of them is used to provide the reference voltage (V_{ref}) for the output voltage regulation and the other one is used for the initial reset of the

digital circuit. In order to make the simulation results closer to the real measurement results, the connection such as bond wires or bond pads can be added to the test bench. In this work, these parts are not taken into account. In future work, an improvement of the test bench can be made in this respect.

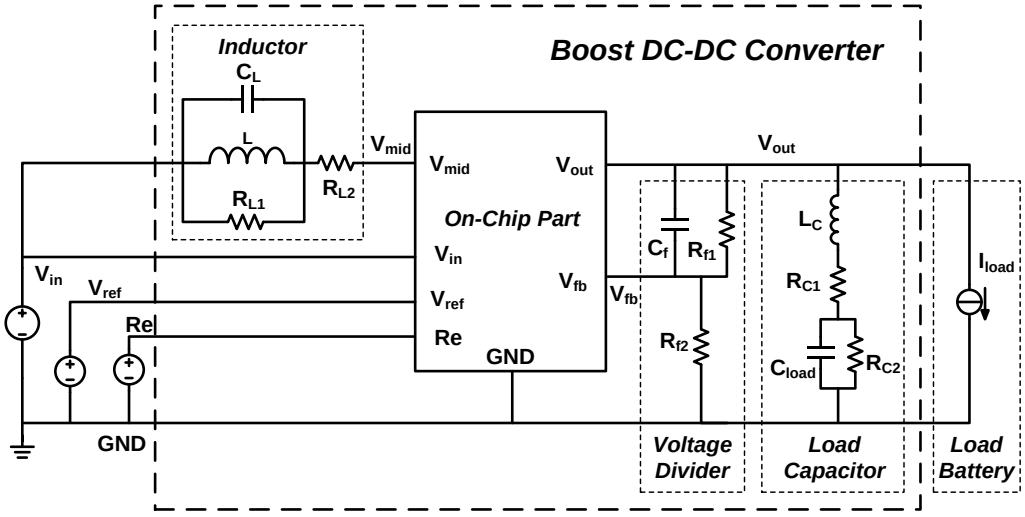


Figure 6-1: The schematic of the test bench.

The post-layout simulations of the boost DC-DC converter are carried out using the test bench introduced above. The functionalities and performances of the boost DC- DC converter will be presented in the following sections. The minimum supply voltage for the control system and the operation of the boost converter in the startup phase will be shown in Section 6.2. Section 6.3 will discuss the waveforms and the performance of the boost converter which is operating in the steady state under two different load current conditions ($I_{\mathrm{load}} = 10mA$ or $1mA$). The responses of the boost converter to the input voltage or load current variations will be presented in Section 6.4.

6.2 Operation of the Converter in the Startup Phase

The startup phase mentioned here is different from what has been introduced in Section 2.1. The startup phase discussed in Section 2.1 means the phase during which the output voltage of the boost DC-DC converter rises from zero to the steady state value. In fact, the startup phase can be divided into two sub-phases for the boost DC-DC converter designed in this project. In the first sub-phase, since the output voltage of the boost converter is not high enough to provide the supply voltage for the control system, an external mechanism is required to generate a supply voltage to power the control system or pre-charge the load capacitor at the output of the boost converter. After the voltage of

the load capacitor (the output voltage of the boost converter) reaches a sufficient value, the boost converter enters the second startup sub-phase. In this phase, the output voltage is used to provide the supply voltage for the control system and the output voltage will finally rise to the steady state value. The study of the first startup sub-phase is not included in this research. The startup phase discussed in this section just refers to the second startup sub-phase. Therefore, in the test bench shown in Figure 6-1, the load capacitor (C_{load}) is given an initial voltage which is equal to the minimum voltage that can ensure the control system operating correctly.

In most cases, the boost DC-DC converter is only applied in the steady state. Hence, in the startup phase, the boost converter can be without any load, which means the load current is equal to zero. In addition, the power conversion efficiency is no longer an important consideration for the boost converter working in the startup phase. In contrast, the minimum supply voltage for the control system is the most significant, because the lower this value is, the easier it will be for the external startup voltage generation mechanism such as the thermoelectric or RF energy harvesting.

In this design, the minimum voltage for the control system is about $0.7V$. If the load capacitor has an initial voltage of $0.7V$, the boost DC-DC converter can automatically raise its output voltage to the steady state value ($1V$). The startup behavior of the boost DC-DC converter designed in this research is shown in Figure 6-2. It can be seen that, before the boost converter reaches the steady state, it operates in CCM (to be more precise, quasi-CCM as mentioned in Section 4.2). When the boost converter reaches the steady state, it starts to operate in DCM. The lowest value of the initial voltage is mainly determined by the analog circuits in the control system. For example, in this design, if the initial voltage is lower than $0.7V$, the overly long propagation delays of the comparators (Section 4.5) and the unsufficient biasing current generated by the reference current generator (Section 4.6) will cause the boost DC-DC converter to break down.

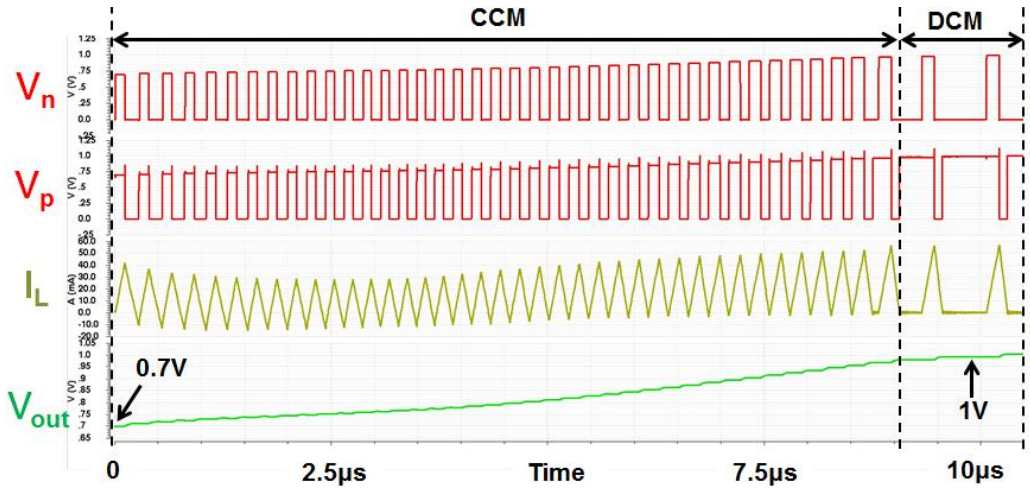


Figure 6-2: Startup phase of the boost DC-DC converter.

6.3 Operation of the Converter in the Steady State

When the boost DC-DC converter is used to charge the load battery, it should operate in the steady state. For the boost DC-DC converter designed in this work, it should achieve the specifications listed in Table 1-1 (Section 1.3) when it operates in the steady state. The post-layout simulations are carried out to verify its functionality and performance under two load conditions ($I_{\text{load}} = 10mA$ or $1mA$). Firstly, the post-layout simulation results of the boost converter loaded with a $10mA$ constant current source ($I_{\text{load}} = 10mA$) are shown.

Figure 6-3 shows the waveforms of the boost converter working in the steady state. In here, UD is the "up/ down" signal in the Zero Current Switching (ZCS) adjustment blocks (Figure 4-19). UD is a binary signal. When UD is low, the off-time will be decreased in the next cycle. When UD is high, the off-time will be increased in the next cycle. The detailed control principle has been introduced in Sections 3.6 and 4.4. Moreover, V_{n} and V_{p} are the signals used to control the MOSFET power switches (Figure 4-1). Furthermore, I_{L} represents the inductor current and V_{out} is the output voltage of the boost converter. From Figure 6-3, it can be seen that, the boost converter works without any load ($I_{\text{load}} = 0$) at the beginning time ($< 50\mu s$). When the load current is changed to $10mA$, the boost converter starts working in the high load condition. After a short response time, its output voltage will be stable close to $1V$(988~$996mV$). The peak value of the inductor current (I_{L}) is about $57mA$.

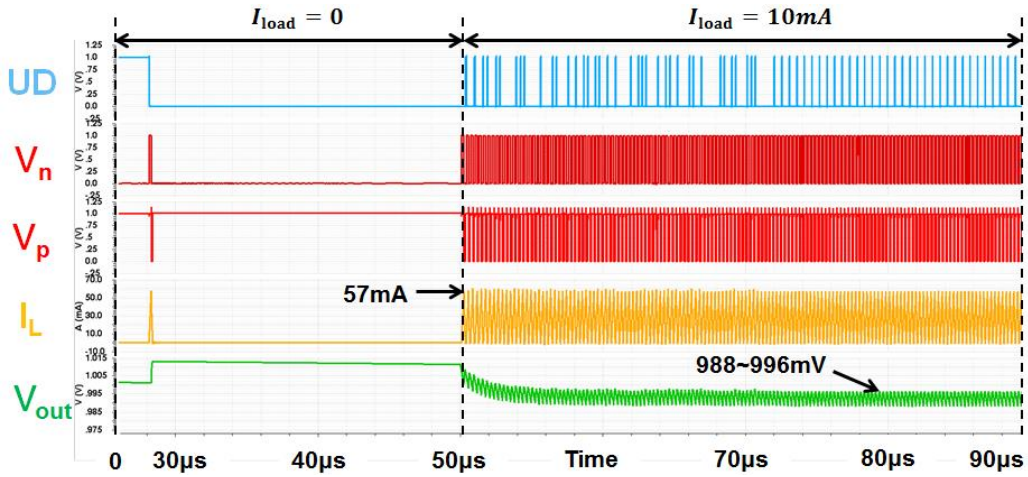


Figure 6-3: Waveforms of the boost DC-DC converter ($I_{\text{load}} = 10mA$).

Zooming in on Figure 6-3, Figure 6-4 is obtained. In here, we can see that, the on-time is a constant value of $151.1ns$ in each cycle and the off-time is alternatively changed from $92.7ns$ to $93.9ns$ and vice versa because of the ZCS adjustment. The ripple of the output voltage is $8mV$ ($996mV - 988mV = 8mV$).

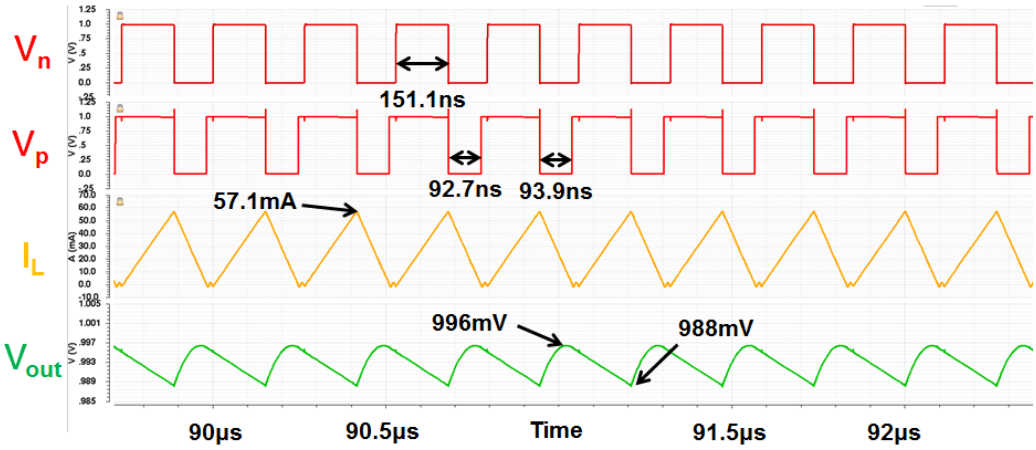
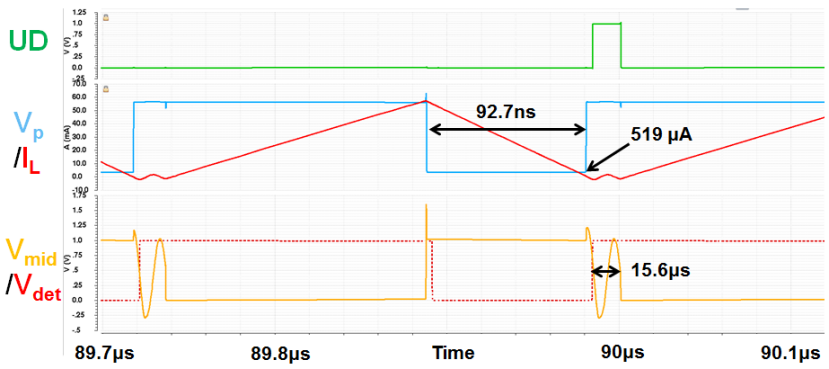
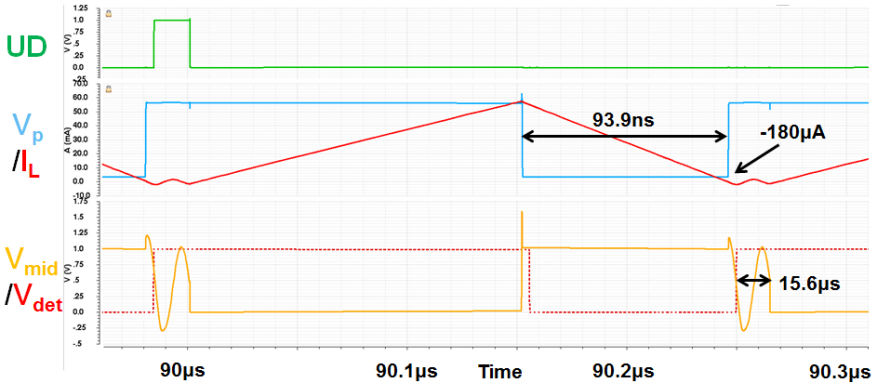


Figure 6-4: Zoom-in waveforms of the boost DC-DC converter ($I_{\mathrm{load}} = 10mA$).

The ZCS adjustment technique is applied in this boost converter system in order to achieve the accurate time balance between the on-time and the off-time (see Section 3.6). Its functionality and performance are verified by the simulation results shown in Figure 6-5. Figure 6-5 displays the waveforms of the boost converter in two adjacent cycles. From Figure 6-5a, we can see that, by detecting the voltage V_{mid} at the end of the off-time, whether the off-time is overly long or overly short can be determined by the ZCS adjustment blocks. The residual current ($519\mu A$) in the inductor at the end of the off-time leads the "up/down" signal UD to the high level, which will increase the off-time by one LSB in the next cycle. In Figure 6-5b, the off-time in the next cycle is increased from $92.7ns$ to $93.9ns$ (one LSB is about $1.2ns$) and as a result the residual current in the inductor at the end of the next off-time is changed to -$180\mu A$. This leads the signal UD staying in the low level, which will accordingly decrease the off-time by one LSB in the following cycle. Therefore, the off-time will be toggled between these two values and the residual current in the inductor at the end of each off-time will be controlled in the range of -$180\mu A$~ $519\mu A$. The ringing problem mentioned in Section 4.4 can be clearly seen in the post-layout simulation results. This issue will reduce the accuracy of the ZCS adjustment by one LSB. An improvement will be made in future work.



(a)



(b)

Figure 6-5: Verification of the ZCS adjustment technique ($I_{\mathrm{load}} = 10mA$).

Finally, the power conversion efficiency of the boost converter can be obtained from the post-layout simulation results by using Calculator in Cadence Virtuoso. Because the power consumptions of the reference voltage source (V_{ref}) and the reset voltage source (Re) is extremely small compared with that of the input voltage source (V_{in}), the calculation formula can be approximately written as:

$$\eta = \frac{\int (V_{\mathrm{out}} \cdot I_{\mathrm{load}}) dt}{\int (V_{\mathrm{in}} \cdot I(V_{\mathrm{in}})) dt} \tag{6.1}$$

in which $I(V_{\mathrm{in}})$ is the current flowing through the input voltage source (V_{in}). The calculation result shows that the power conversion efficiency can achieve 94.8% for the boost DC-DC converter working with a $10mA$ load current.

The same post-layout simulations are made for the boost DC-DC converter loaded with a $1mA$ constant current source ($I_{\mathrm{load}} = 1mA$) as well. The simulation results are displayed in the following:

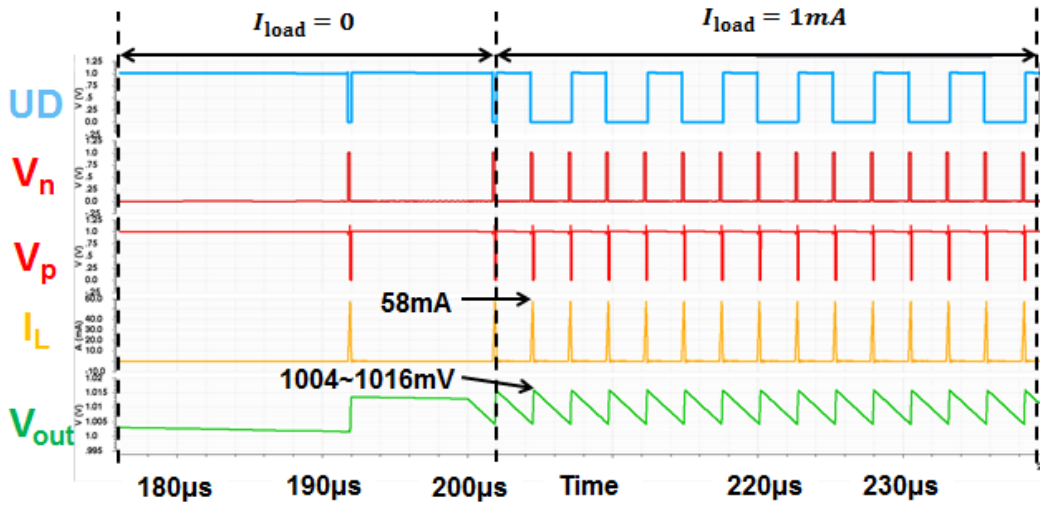


Figure 6-6: Waveforms of the boost DC-DC converter ($I_{\mathrm{load}} = 1mA$).

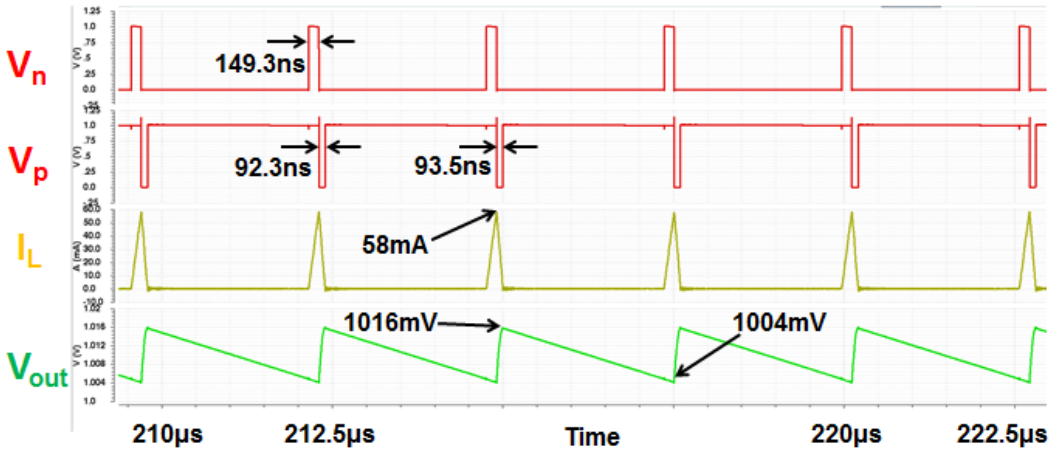
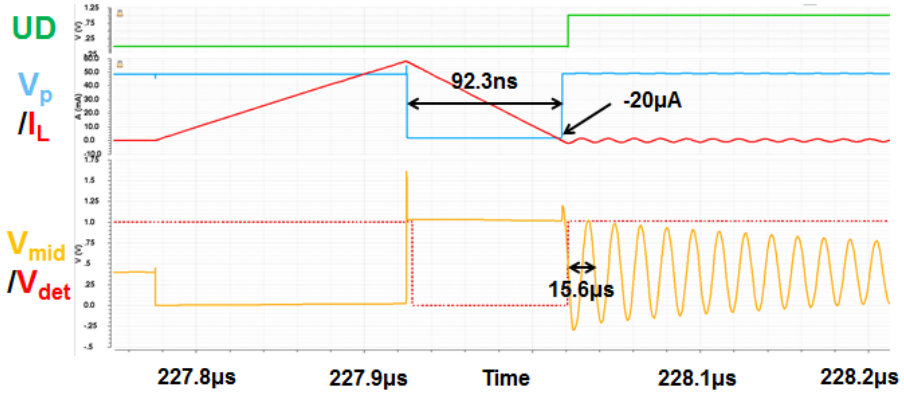
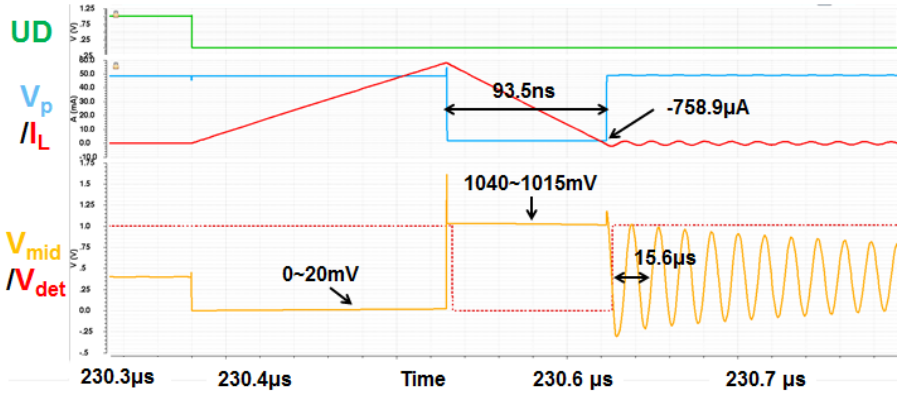


Figure 6-7: Zoom-in waveforms of the boost DC-DC converter ($I_{\mathrm{load}} = 1mA$).



(a)



(b)

Figure 6-8: Verification of the ZCS adjustment technique ($I_{\mathrm{load}} = 1mA$).

By using Calculator in Cadence Virtuoso, we obtain that the power conversion efficiency of the boost DC-DC working with a $1mA$ load current can achieve 93.3%.

6.4 Responses of the Converter to Input Voltage and Load Current Variations

For the boost DC-DC converter applied in an energy harvesting system, the input voltage will be affected by the front-end circuit. For instance, in an RF energy harvesting system, the variation of the input power received by the RF energy harvester (antenna and rectifier) will change the input voltage of the boot converter. Besides, the load current of the boost converter will often be changed according to different load conditions. As a consequence, a well-designed boost DC-DC converter should always generate a stable output voltage no matter what variations are encountered. In this design, the AOOT control technique is applied to control the boost converter in order to achieve the target. According to the explanation about AOOT control given in Section 3.4, we know that: (1) the boost converter will adjust the on-time and the off-time based on Equation 3.13 and 3.14 in response to the input voltage variation; (2) the boost converter will change the switching frequency by increasing or decreasing the dead-time in response to the load current variation.

The post-layout simulation results of the responses of the boost DC-DC converter to an input voltage variation is shown in Figure 6-9. We can see that, in this extreme condition, when the input voltage rises from $350mV$ to $650mV$, the on-time is adjusted from $163.5ns$ to $90.1ns$. Accordingly, the off-time is also changed. As shown in the black ellipses in Figure 6-9, in order to achieve Zero Current Switching, the ZCS adjustment block is fine tuning the off-time after a changing of the on-time and the off-time. Based on the simulation results, it can be concluded that the boost DC-DC converter designed in this research can quickly respond to an input voltage variation and generate a very stable output voltage despite any variation of the input voltage.

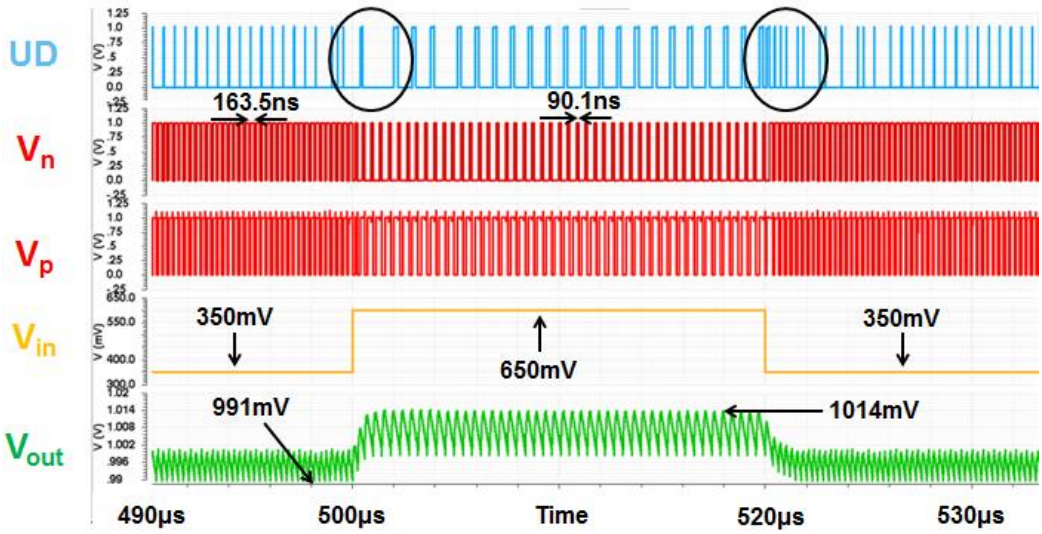


Figure 6-9: Responses of the boost converter to an input voltage variation.

The responses of the boost DC-DC converter to a load current variation can be seen in Figures 6-3 and 6-6. For instance, Figure 6-6 shows the responses of the boost converter on a load current variation from 0 to $1mA$. The on-time and the off-time are almost maintained at the same values. Only the dead-time is decreased as the load current is increaed. Figure 6-10 presents the responses of the boost converter when the load current is changed from $10mA$ to $1mA$. According to the simulation results, a similar conclusion can be made, that is, the boost DC-DC converter designed in this work can quickly respond to a load current variation and generate a very stable output voltage.

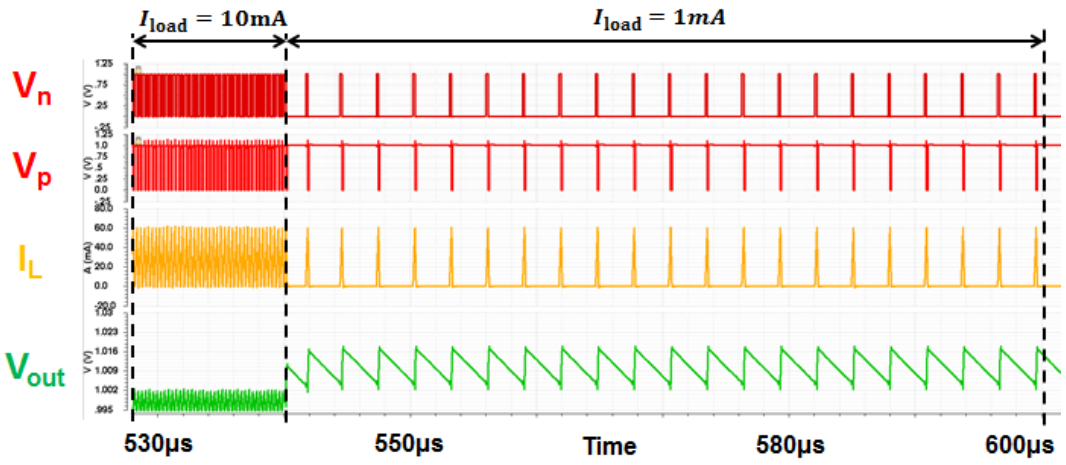


Figure 6-10: Responses of the boost converter to a load current variation.

Chapter 7

Conclusions

7.1 Summary

This thesis presents the design of a switch-mode inductor-based boost DC-DC converter which can be applied for power management in energy harvesting systems. By using the adaptive on-time/off-time (AOOT) control and zero current switching (ZCS) adjustment, the proposed boost converter can generate a stable $1V$ output voltage and achieve very high power conversion efficiency over wide input voltage and load current ranges. The circuit implementation and the layout design of the on-chip part have been done in TSMC 40nm CMOS technology. With the post-layout simulation results, the functionality and performance of the circuit system have been demonstrated to achieve the design targets.

7.2 Contributions

The main contributions of this work include:

- *A systematic design flow of a boost DC-DC converter has been proposed from the initial system-level design to the final layout implementation.*

  Since this is the first time to design a boost DC-DC converter for energy harvesting applications in our team at Holst Centre/imec, this work is not only to design a circuit that can meet the specifications but also to provide a guideline for further design of any other types of DC-DC converters in other applications. In this thesis, a detailed design flow has been presented from (1) the design of the power plant, to (2) the selection of the most suitable control technique, then to (3) the transistor-level implementation and finally to (4) the layout design. Based on this flow, if the application or requirement is changed, it will be easy to make a modification of this boost DC-DC converter or to design a new DC-DC converter.

- *An advanced control method with the combination of AOOT control and ZCS adjustment has been applied in the boost DC-DC converter to achieve high power conversion efficiency and a stable output voltage over wide input voltage and load current ranges.*

  Due to large variations of the input voltage and load current, the general PWM control techniques are usually not suitable for the boost DC-DC converter used for energy harvesting. A boost DC-DC converter in AOOT control can quickly respond to an input voltage variation and achieve high power conversion efficiency over a wide load current range. Moreover, by using the ZCS adjustment technique, the performance of the boost DC- DC converter will be improved because of the fine tuning of the off-time. Therefore, AOOT control with ZCS adjustment has been demonstrated to be very appropriate for a boost DC-DC converter in energy harvesting applications.

- *A novel method to implement the layout of the MOSFET power switches has been presented which can not only save area but also reduce the parasitic resistance thus improving the performance of the boost DC-DC converter.*

  In general, the power switches are the most area-consuming components in a DC-DC converter except the inductor and the capacitor. As a result, the large parasitic resistances caused by the big transistors will reduce the power conversion efficiency. By using the structure proposed in this thesis to implement the layout of the MOSFET power switches, much area can be saved and the power conversion efficiency can be improved due to the reduction of the parasitic resistance.

- *A boost DC-DC converter with very high power conversion efficiency targeted for energy harvesting has been designed.*

  The simulation results have demonstrated that the proposed boost DC-DC converter can achieve more than 90% (maximum about 95%) power conversion efficiency over a wide input voltage range ($0.35V \sim 0.65V$) and a wide load current range ($1mA \sim 10mA$). In fact, according to the application requirements, after a little modification of the circuit, this boost DC-DC converter can also fulfil the same performance under other working conditions such as loaded with a much higher or lower current.

7.3 Future Works

Due to the time constraint, this project missed the tape-out of our company. As a result, the designed boost DC-DC converter cannot be tested by real measurements. As a next step, this circuit should be manufactured and assembled in a printed circuit board (PCB). The effects of the pond wires, pond pads and some other practical factors on the functionality and performance of the boost DC-DC converter will be tested and analyzed.

Moreover, some improvements should be made for solving the problems mentioned in this thesis. For example, as mentioned in Section 4.4, because of the ringing occurring on the drain of the PMOS power switch at the end of each off-time, the accuracy of the ZCS adjustment may be degraded by one-LSB. In future, a good solution should be worked out after doing a further analysis on the causes of this ringing. In addition, the temperature behavior of the reference current generator should be improved in order to generate a more stable reference current over a wider temperature range.