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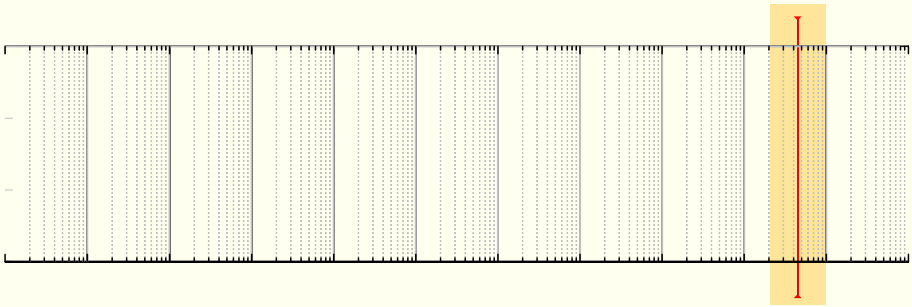

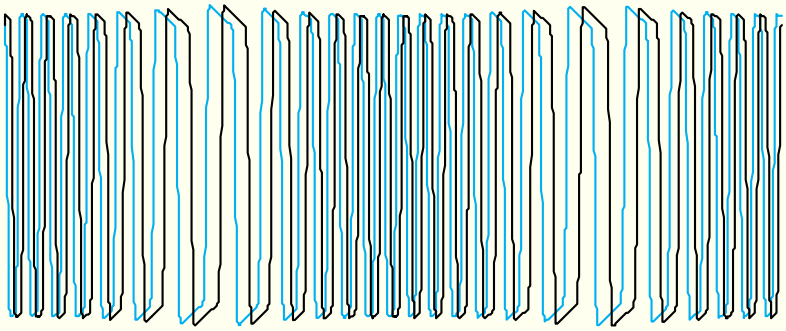

The Design of Integrated Frequency Sources and their Application to Wideband FM Demodulation

Akshay Visweswaran

The Design of Integrated Frequency Sources and their Application to Wideband FM Demodulation

Proefschrift

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Thesis Summary

Wideband data transmission can increase the throughput of a wireless system. In theory, scaling the carrier frequency facilitates the use of wider bandwidths without increase in the fractional bandwidth at radio frequency (RF). Given that transit frequencies as high as 300 GHz can be obtained with minimum feature sizes on the order of 10 nm on chip today, integrated-circuit technology is poised to remain the most amenable and likely platform for implementation of mm-wave and sub mm-wave systems in the coming years. However, at present the performance and power-efficiency of the RF front-end at these frequencies is limited by technology when compared to the thumping success of wireless communication in GSM and ISM bands in the low-GHz range. From an implementation point of view, one of the bigger challenges remains demodulation, which is curtailed by the lack of circuit techniques for handling and processing signals occupying multi-GHz of bandwidth.

The design and study of autonomous frequency sources during the course of this research shows that phase-stable oscillators, such as those with resonant loads, are less responsive to forced external stimuli when compared to ring oscillators with first-order loads that demonstrate phase stability orders-of-magnitude lower in comparison. As a consequence, injection-locked ring oscillators can linearly track wideband frequency modulation for rates as high as one-fifth the carrier frequency with ease. The first part of this thesis presents the design, analysis and characterization of an injection-locking, wideband FM demodulator for application in heterodyne receivers. The low-power FM demodulator operates across 2-10 GHz of intermediate-frequency (IF) bandwidth, and comprises a four-stage ring oscillator that injection-locks to the input FM and reduces the carrier frequency and FM deviation by a factor of four. Correlating the quadrature-phased outputs inherent to a four-stage ring topology enables and simplifies power-efficient, wideband FM demodulation for large fractional bandwidths approaching unity.

Stand-alone characterization of the oscillator shows that it is capable of locking to at

least a modulating frequency of 400 MHz (i.e., a carrier- to modulation-frequency ratio of ~10), and further testing is limited by the FM source. Linear demodulation of the quadrature-phased outputs of the locked-in oscillator is realized using a low-power folded-CMOS implementation of a Gilbert-cell mixer. The design, analysis and stand-alone characterization of a differential class-AB amplifier developed in this work are also detailed in the thesis. The amplifier designed for low distortion and low-impedance drive interfaces the demodulated output to the 50-Ω measurement environment. The inductorless demodulator prototyped in 65-nm bulk CMOS occupies 0.17 mm^2 and dissipates 3.2 mW from 1.2 V at quiescent point. The SNR sensitivity is 8 dB, and demodulator measures a 0.1% BER at 10 Mbps for a 45-mV_{pp} input signal at IF.

The transmission of an FM signal through an injection locked oscillator is explained analytically and verified via simulation and experimental characterization of a stand-alone ring oscillator. Expressions for time-instantaneous I/Q phases and the demodulator's output characteristic are also developed that verify wideband operation. In addition, experimental characterization of the oscillator's response to external noise and FM reveal physical trends such as noise-induced frequency shifts, onset of chaos, and hysteresis, which lie beyond the scope conventional theory. These observations are discussed in context of the locked-in demodulator's sensitivity to noise and interference.

The second part of the thesis examines phase stability in integrated oscillators and addresses the mechanisms that lead to conversion of noise into fluctuations in phase. In the low-noise technique developed in this thesis, hard-limiting the oscillator output with transformer-coupled gate overdrive creates phase insensitivity to noise. Coupled transformers reduce loading in the loop, and phase-noise conversion from not just the transistor pair, but the tank is reduced as well. The principle of phase insensitivity described in this work eliminates the tail-current source, which becomes a significant noise contributor at high power levels. It is known that maximum phase-noise conversion of channel noise occurs when the two switching transistors conduct simultaneously. The cyclo-stationary, time-dependent oscillator

phase-noise expression developed in this thesis shows this. Rise and fall transient times are therefore minimized using transformer-coupled gate overdrive to improve phase stability. An embodiment of the proposed oscillator concept optimized for high-power consumption was prototyped in 65-nm bulk CMOS and characterized extensively for comparison of phase noise performance theory. Measurements show that the phase noise is within 2-dB reach of the challenging -147 dBc/Hz GSM base-station phase-noise specification for a 915 MHz carrier at an 800-kHz offset. Findings from the oscillator study presented in this research have triggered further innovation in the field, which are discussed in this thesis.

Chapter 1 – Introduction

Built on fundamentals developed over more than a century, the experiment of wireless communication has evolved into a field of engineering science and varied application. Ranging from broadcasts, mobile telephony, personal and local-area networks, to advances in medical diagnostics, imaging, and space exploration, wireless electronic systems are among the major estates that currently shape man's progress and thinking.

Radio communication between a transmitter and a receiver establishes a wireless link. Key blocks of the transmitter are a modulator and power-amplifier (PA) as shown in Fig. 1.1a. The high-frequency carrier (at f_c) is modulated at a rate, f_m, and transmitted via the PA. The characteristics of a propagating RF wave are frequency, phase and amplitude – any of which may be modulated with information, depending on the system-type and standard. The receiver's RF-front-end that is comprised of an LNA, mixer and local-oscillator down-converts the modulated RF-input to an intermediate frequency (IF), after which data recovery is accomplished through a demodulator, as shown in Fig. 1.1b. Super-heterodyne receivers operate at a non-zero IF, whereas in the specialized case of zero-IF in homodyne receivers, the same LO frequency (f_c) is applied in the transmit- and receive-paths.

Research in the design of power-efficient transceivers is mandated by the count of wireless devices in operation, which runs into billions as wireless technology finds itself at the heart of workplace and social infrastructure worldwide. The relevance of energy-efficient links stands to grow as the internet of things (IoT) envisioned for the near future will see a plurality of interconnected wireless devices communicating information in real time. The heightened efficiency and automation of routine activities is fuelling the dream of smart cities, among others. Since the entire transmitted RF-power is drawn from the voltage supply, the transmitter with limited efficiency dominates energy consumption during operation. Receivers are typically powered-on continuously, since time of reception is unknown while transmission is deterministic. In general, power-optimization of the transmitter and receiver are

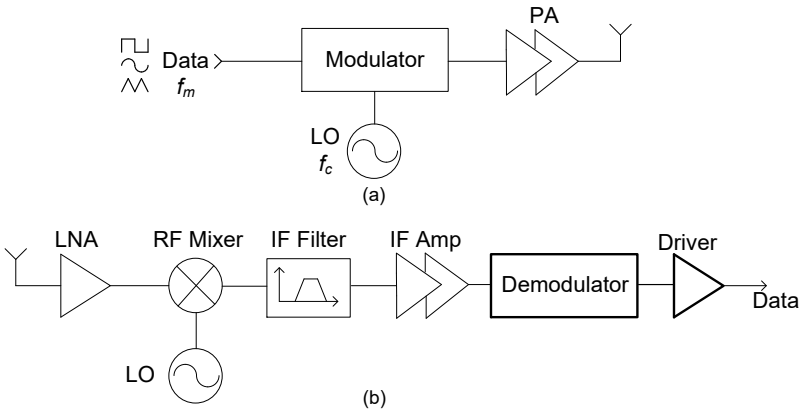

Fig. 1.1: Block diagrams of an (a) RF transmitter, and (b) RF receiver.

equally important when realizing energy efficient wireless links.

The pursuit of multi-gigabits per second throughput, while maintaining range and connectivity, is driving the next phase of innovation in wireless technology into mm-wave from 30–300 GHz, and optical communication in the visible-light spectrum. Untapped bands beyond 100 GHz have potential for spectroscopy, wireless sensing, and high data-rate (~10 Gbps) space-borne telemetric systems and links. Long-range communication is not possible in the vicinity of 60, 120 and 180 GHz, due to peaks in the atmospheric O_2 absorption of RF energy in these bands [1.1]. However, efforts to commercialize these bands for directive, short-range communication are underway for applications such as video streaming, broadband internet access, virtual reality, gesture recognition and automotive radars. The availability of unlicensed bandwidth for use worldwide (e.g., 59-64 GHz) creates a lucrative prospect for wideband communication. On the other hand, the ubiquitous acceptance of smartphones and the increased use of mobile data have created unprecedented challenges for licensed wireless service providers. Performance is limited by the carrier frequency spectrum that ranges between 700 MHz and 2.6 GHz, amidst demands for greater capacity in mobile broadband communication. Ongoing studies at 28 and 38 GHz show reduced atmospheric and rainfall absorption [1.2], thereby opening avenues for a shift in mobile communication into the mm-wave range within the emerging 5G standard. The designated bandwidths

between 27.5–29.5 GHz and 36–40 GHz [1.3] are being commercially surveyed for communication at data rates ranging from 200–500 Mbps [1.4], [1.5].

The implementation of wideband radios, however, throws up design challenges along the transmit- and receive-chain that require research and innovation in circuit blocks, and parallel advances in IC technology for provision of transistors and back-end metallization amenable to these objectives. Wideband receiver performance is typically limited by power consumption, which increases in proportion to the data rate. Demodulation of wideband signals is further restricted by the challenge and complexity of designing interface circuits and delay networks (at RF and IF), despite the availability of sub-micron transistors having transit frequencies in excess of 250 GHz. While a trade-off between bandwidth and power consumption is encountered in circuit design routinely, the phase-linearity of conventional passive delays or phase-shift networks necessary for demodulation remains bandlimited [1.6]. At present, there have been few demonstrations of integrated wideband circuits that verify the feasibility of energy-efficient communication links, e.g., the 3-5 GHz UWB-FM transceiver in [1.7].

1.1 Wideband FM demodulation at IF

Portable receivers for low-cost, high-speed wireless links should be compact, fully-integrated and consume minimal DC power. Co-optimization of systems and circuits is necessary to achieve energy-efficient, low-power communication links [1.8]. Simple modulation schemes such as wideband frequency-shift keying (FSK) are currently of interest for wireless local- and personal-area communication, because they require low-complexity transceivers. However, power-efficient data transfers at rates up to 1 Gbit/s are required for applications such as video streaming [1.9]. Demodulation at an intermediate frequency (IF) in a low-complexity heterodyne receiver (Fig. 1.1a) enables greater bandwidth handling and mitigates the impact of receiver flicker noise, limited port isolation, and signal interference often encountered in homodyne receivers. Circuit operation at a reduced fractional bandwidth ($\Delta f/f_c$) through appropriate choice of an IF can potentially simplify the implementation of a wideband receiver, thereby saving power and chip area.

In theory, scaling the carrier frequency facilitates the use of wider bandwidths (without increase in fractional bandwidth at RF), however, the performance and efficiency of the RF-front end at high frequencies is limited by IC technology. In contrast, wideband demodulation at IF in heterodyne receivers is limited by the lack of circuit techniques. The first part of this thesis presents the design and analysis of an injection-locking, wideband FM demodulator for heterodyne receivers [1.10]. This is the first demonstration of a fully-integrated, multi-GHz, low-power IF-demodulator capable of operating at fractional bandwidths approaching unity. The work presents detailed analysis and experimental characterization of the propagation of an FM signal through a locked-in ring oscillator, and its properties that enable power-efficient wideband demodulation. Division of FM deviation and scaling of Bessel-function coefficients are derived analytically and experimentally verified through a 65-nm prototype demodulator. The demodulator operates across 2-10 GHz IF ($\Delta f/fc$=1.4), while consuming 0.32 nJ/bit at a 10-Mbps data rate. Measurements verify that the oscillator is capable of locking to a modulation rate of at least 400 MHz (0.8 Gbps). Low-power circuits developed in the work are evaluated using mathematical analysis and simulation. These include a ring oscillator with wideband sensitivity, a folded CMOS mixer with Q-point control, and a fully-differential, 3-stage class-AB amplifier with common-mode feedback stabilization. The prototype IC is characterized extensively using a wide range of experiments to study division of FM deviation, wideband demodulation, noise sensitivity, bit-error rates and response to in-band and out-of-band interference.

1.2 Differential class-AB driver

A fully-differential class-AB amplifier capable of operation at rates of 100 MHz [1.11] interfaces the demodulator to the 50-Ω measurement environment. The high loop gain and differential operation ensure low-distortion. Common-mode feedback is applied to increase output drive capability and reduce crossover distortion when operating in class-AB from a low supply voltage. The pre-amplifier stage is a gain-boosted folded cascode amplifier. Analysis of the gain-boosted amplifier presented in this thesis shows for the first time that there exist two, as opposed to the generally

perceived single pole-zero doublet, in the transfer function. Doublets result from the individual frequency responses of each auxiliary amplifier added to enhance the output impedances of the NMOS and PMOS cascode branches, respectively. The impact that the two sets of doublets have on the settling behavior is examined along with simple design guidelines to optimize the amplifier's performance. A detailed analysis of the amplifier design and characterization of a 65-nm CMOS prototype is presented in Chapter 5.

1.3 Low noise oscillator design for GSM base-stations

The second part of the thesis presents the design and analysis of a power-efficient, low-phase-noise local-oscillator (LO) intended for GSM base-station (BTS) receivers [1.12]. One of the challenges in the implementation of these narrowband receivers is the 200-kHz spacing between adjacent channels [1.13]. Base-station receivers handle multiple channels simultaneously, and as a consequence, stringent dynamic-range, noise-floor and in-band blocking requirements exist for a specified minimum sensitivity of -104 dBm [1.13]. The receiver's in-band blocking specification dominates the phase noise requirement of the BTS receiver's LO. In-band interferers desensitize the receiver to the signal of interest through reciprocal mixing with the LO-spillover at offset frequencies, as shown in Fig. 1.2a. Fig. 1.2b shows the in-band blocking profile for the GSM-900 base-station standard. It can be seen that the receiver is required to operate in the presence of an 88-dB stronger interferer at a relatively close, 800-kHz offset from the carrier frequency. This translates into a very stringent phase-noise requirement, one that has proven difficult to implement in bulk-CMOS IC technologies. The limited quality-factor (Q) of on-chip passives and the constraint on output swing set by device breakdown determine the lowest attainable phase noise, while selectivity of practical RF filters isn't sufficient to eliminate strong in-band blockers and alleviate the constraint on LO phase noise. As will be shown in Chapter 2, when scaling existing IC oscillator designs to meet aggressive phase-noise specifications for applications such as base stations, the dwindling trade-off between phase noise and power consumption leads to excessive dissipation. The oscillator's phase-noise re-

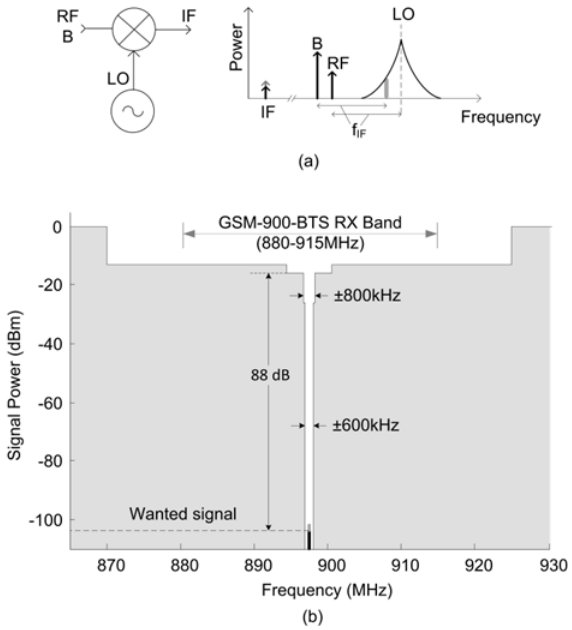

Fig. 1.2: (a) A depiction of reciprocal mixing with interference, and (b) the GSM-900-BTS-Normal in-band blocker profile.

-quirements between 600-kHz and 3-MHz offsets are listed in Table I, and derived in the next sub-section. At an 800-kHz offset, the GSM-900-BTS and the DCS-1800-BTS specifications are -147 dBc/Hz and -138 dBc/Hz, respectively. In GSM mobile handsets, by comparison, the transmit- and receive-bands being 20-MHz apart set a more relaxed requirement on the transmitter phase noise of -162 dBc/Hz at a 20-MHz offset.

High-power offers a challenging design space where low transistor output impedances, effect of interconnect parastics, and transistor non-linearities limit phase noise performance. In this work, phase desensitization through hard-limiting (and subsequent filtering of harmonics) is implemented in the design of a low-phase-noise oscillator for GSM-BTS receivers. The high-power, low-noise oscillator achieves a phase-noise efficiency that is comparable to designs targeting mobile handsets. While hard limiting the output and operation in triode are counter-intuitive to oscillator design, as will be shown, the oscillator's insensitivity to noise under these conditions overcomes the apparent drawbacks. Predictions of the oscillator's

phase noise from theory and circuit simulation are verified through extensive characterization of an 8-GHz prototype in 65-nm bulk CMOS as proof of concept. Consuming 32 mA from a 1.5-V supply, the oscillator prototype designed for a moderate tuning range of 10% trades tuning range for phase noise performance, and is within 1.5-dB reach of the stringent GSM-900 BTS specification.

1.4 RF link analysis

Propagation of an EM wave through space is accompanied by a drop in power spectral density, which is referred to as path loss. Free-space propagation loss occurs due to the outward expansion of the wave-front from the transmitting antenna, and is one of the major factors affecting the link budget analysis of a wireless system. The frequency dependent free-space path loss over a distance, *d*, is captured by Friis' equation [1.14]:

$$\frac{P_r}{P_t} = \phi_p G_t G_r \left(\frac{c}{4\pi f d}\right)^2, \quad \text{where the freespace path loss } = 20\,log\left(\frac{c}{4\pi f d}\right) in\ dB. \tag{1.1}$$

The ratio between transmitted power, P_t, and received power, P_r, depends the transmit- and receive-antenna gains, G_t and G_r, respectively, the polarization loss ϕ_p, and the free-space path loss, where c is the speed of light and f is the frequency. Antenna gains G_t and G_r represent a ratio of the power transmitted within an infinitesimally small solid angle in a given direction (typically that of peak radiation) to that of an isotropic source. Similar to other passives, reciprocity in an antenna dictates that its transmit- and receive-properties are identical [1.15]. Gain is related to directivity via radiation efficiency. The factor ϕ_p represents the polarization loss between the transmit- and receive-antenna. The link budget of a wireless system is typically calculated assuming polarization-matched, lossless antennas with unity gain – typified by a set of isotropic antennas having directivity, radiation efficiency and gain equal to one. The minimum detectable signal, P_{mds} (in dBm) is written as [1.16]:

$$P_{mds} = kTB|_{dBm} + NF|_{dB} + SNR|_{dB} + 10\log(n), \tag{1.2}$$

Table I: In-band blocker and phase noise requirements for GSM base-stations

	GSM-900-BTS Normal (870-925MHz)		GSM-1800-BTS Normal (1690-1805MHz)	
Frequency offset	In-band blocker (dBm)	Phase noise (dBc/Hz)	In-band blocker (dBm)	Phase noise (dBc/Hz)
600kHz – 800kHz	-26	-137	-35	-128
800kHz – 1.6MHz	-16	-147	-25	-138
1.6MHz – 3MHz	-16	-147	-25	-138
>3MHz	-13	-150	-25	-138

where *kTB* is the maximum available noise power from a matched antenna (*B* is the bandwidth, *T* is temperature and *k* is Boltzmann's constant), *n* is the number of antennas, *NF* is the receiver noise-figure, and *SNR* is the signal to noise ratio required by the demodulator at IF to satisfy its BER requirement. Coherent detection of a binary FSK signal with β=1 has a probability of error, P_b, given by [1.17]:

$$P_b = \frac{1}{2} erfc\left(\frac{SNR}{2}\right)^{0.5}. \quad (1.3)$$

The difference between the received-power calculated from eqn. 1.1 and the minimum detectable signal from eqn. 1.2 gives the link margin.

Under the assumption that the receiver's noise-figure doesn't suffer from gain-compression and that the thermal-noise floor of the receiver is significantly lower than the noise obtained from reciprocal mixing, the phase-noise specifications for GSM-BTS receivers can be calculated using eqn. 1.2. When the signal in the channel of interest is 3-dB higher than the minimum sensitivity of -104 dBm and the carrier-to-interference (C /I) ratio is specified at 9 dB [1.13], the oscillator's phase-noise requirement is:

$$\mathcal{L}(\Delta f) = P_{mds} - P_{int}(\Delta f) - \left[\frac{C}{I}\right] - 10 \cdot \log B. \quad (1.4)$$

In eqn. 1.4 the minimum detectable signal, P_{mds}, is -101 dBm for GSM base-stations, P_{int} is the power of the in-band interferer at an offset Δf from the carrier, and *B* is the GSM channel bandwidth of 200 kHz. The specified interference power and corresponding oscillator phase-noise targets at frequency offsets ranging between

600 kHz to 3 MHz are listed in Table I for the GSM-900-BTS and DCS-1800-BTS standards.

1.5 A note on IC technology

The analysis and circuit operation described in this thesis are verified via experiments on prototype circuits implemented in 65-nm bulk CMOS. Submicron integrated circuit (IC) technology has enabled the design and integration of complete transceiver chains on a single platform, popularized by the acronym SoC (system on chip). Precise and repeatable processing steps enable feature sizes on the orders of 10 nm on chip today, and an amenable Cu/Al back-end metallization stack for interconnects and passives has enabled the design and large-scale manufacture of wireless transceivers in the low-GHz range on a 10-Ω-cm silicon substrate (e.g., GSM, Bluetooth, WiFi).

CMOS technology is driven by the mass consumer market for digitally intensive hardware and memory, making it a more cost-effective solution for large-scale manufacturing compared to SiGe and GaAs. These applications continue to drive CMOS towards further miniaturization, with integration levels doubling every 18 months in accordance with Moore's Law. Shrinking gate lengths ensure a high packaging density and lower device parasitic capacitance. However, reduced intrinsic gain[1] and headroom limitations due to a reduced V_{DD}/V_{th} ratio outweigh the benefits of scaling from an analog/RF design perspective. In addition, since the back-end metallization does not scale as aggressively as transistor sizes, the relatively unchanged dimensions of passives keep the RF circuit footprint on a chip largely unchanged.

A product-line 65-nm CMOS process with an 8-metal back-end stack comprising a 1.4-um thick top aluminum layer, and 0.9-um thick first- and second-from top copper layers (i.e., no thick-metal option for high-Q passives) was used in the design of the prototype demodulator, its sub-circuits and the base-station oscillator.

[1] Increasing the gate length in a lower technology node can provide higher intrinsic gain, but the lower oxide thickness results in a reduced f_t. This may be a suitable for trade-off when designing circuits in the 1-2 GHz range.

1.6 Thesis outline

The two main subjects of this thesis, namely, wideband demodulation and low-phase-noise oscillator design are presented in sequence. Chapter 2 is a discussion of background knowledge and literature survey leading up to the work in this thesis. Design of the injection-locking, wideband demodulator and its sub-circuits is described in Chapter 3, and measurement results characterizing the 65-nm prototype and its sub-circuits are presented in Chapter 4. The design, analysis and characterization of the fully differential, Class-AB amplifier designed for the demodulator interface is described in Chapter 5. Design, analysis and measurements characterizing the hard-limiting oscillator prototype developed in this thesis are described in Chapter 6, and the work of the thesis is summarized in Chapter 7.

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Chapter 2 – Background theory and literature

This chapter briefly summarizes some of the background knowledge and literature survey leading up to the research presented in this thesis. Basic principles of frequency modulation (FM) and a literature survey of FM demodulators are presented. This is followed by a summary of oscillator phase noise models and existing low phase noise oscillators, and an in-depth overview of the LC oscillator.

2.1 Fundamentals of FM

In frequency modulation, the instantaneous phase of a carrier is varied by modulating its instantaneous frequency with the information-containing baseband signal. The FM-wave takes the following mathematical form:

$$v_{FM}(t) = X_c cos\big(\omega_c t + \varphi(t)\big). \tag{2.1}$$

In eqn. 2.1, X_c and ω_c are the carrier amplitude and frequency, respectively, and the instantaneous frequency is determined by the modulation:

$$\omega_i(t) = \omega_C + \Delta\omega f(t). \tag{2.2}$$

The frequency deviation, $\Delta\omega$, describes the maximum excursion the instantaneous frequency takes about the carrier. The modulating function, $f(t)$, is periodic with an angular frequency ω_m. The instantaneous phase equals the time-integral of frequency, and is written as:

$$\phi(t) = \int_0^t \omega_i(t)\ \mathrm{dt} = \omega_c t + \Delta\omega \int_0^t f(t)dt. \tag{2.3}$$

In the case of a single-tone modulation, the modulating signal $f(t)$ equals $cos\,\omega_m t$ and the resulting FM signal may be written as:

$$v_{FM}(t) = X_c cos\left[\omega_c t + \Delta\omega \int_0^t f(t)dt\right], \tag{2.4}$$

$$v_{FM}(t) = X_c cos[\omega_C t + \beta sin(\omega_m t)]. \tag{2.5}$$

The ratio ($\Delta\omega/\omega_m$) is defined as the modulation index (β in eqn. 2.5), and the ratio $\Delta\omega/\omega_c$ is called the deviation ratio, D_r. Expanding eqn. 2.5 yields:

$$v_{FM}(t) = X_c cos(\omega_c t) cos\big(\beta sin(\omega_m t)\big) - X_c sin(\omega_c t) sin\big(\beta sin(\omega_m t)\big). \quad (2.6)$$

From eqn. 2.6 it's seen that an FM signal can be expressed as the sum of two AM signals. Evaluation of eqn. 2.6 using Bessel functions of the first kind defines the spectral components of the FM signal and its bandwidth [2.1]. Coefficients of higher-order harmonics decay rapidly, thus bringing a sharp roll-off at the edges of the spectrum. As per Carson's rule, 98.6% of the FM signal's power is concentrated in a bandwidth equal to $2(\beta+1)(\omega_m/2\pi)$. The decomposition of eqn. 2.6 into its spectral components yields [2.2]:

$$cos(\beta \sin(\omega_m t)) \; = J_0(\beta) + 2 \sum_{n=0}^{\infty} J_{2n} \cos(2n\omega_m t), \quad (2.7)$$

$$\sin(\beta \sin(\omega_m t)) \; = \; 2 \sum_{n=0}^{\infty} J_{(2n+1)}(\beta) \sin\big((2n+1)\omega_m t\big), \quad (2.8)$$

Substituting eqns. 2.7 and 2.8 in eqn. 2.6, after simplification, yields:

$$\begin{aligned} v_{FM}(t) = J_0(\beta) cos(\omega_c t) + J_1(\beta)[cos(\omega_c + \omega_m)t - cos(\omega_c - \omega_m)t] \\ + J_2(\beta)[cos(\omega_c + 2\omega_m)t + cos(\omega_c - 2\omega_m)t] + \cdots \; , \end{aligned} \quad (2.9)$$

$$where \; J_n(\beta) = \frac{1}{2\pi} \int_{-\pi}^{\pi} e^{j(\beta sinx - nx)} dx. \quad (2.10)$$

Eqn. 2.9 shows that each coefficient, $J_n(\beta)$, defines the power of the n^{th} spectral-tone, and that the spectrum is symmetric around ω_c. The spacing between consecutive spectral tones equals the modulating signal-frequency, ω_m. The integral in eqn. 2.10 yields a real value, and a tabulation of J_n for different modulation indices can be found in [2.2]. Transmission of an FM signal through an injection-locked oscillator and division of FM deviation demonstrated in this thesis (Chapter 3) are explained using Bessel function coefficients defined by eqn. 2.10.

2.1.1 FM Bandwidth and Noise

The output of an FM demodulator, as will be seen in the next sub-section, is proportional to the frequency deviation corresponding to $\varphi(t)$ in eqns. 2.1 and 2.5, and may be written as:

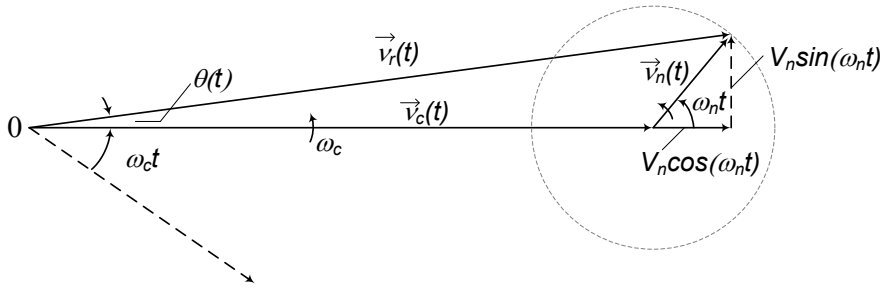

Fig. 2.1: Amplitude and phase modulation created by noise.

$$v_o(t) \propto \left[\frac{1}{2\pi}\frac{d\varphi(t)}{dt}\right] \Rightarrow \; v_o(t) = [k \cdot \Delta f \cdot sin(\omega_m t)], \tag{2.11}$$

where k is a constant of proportionality (V/Hz) and $\Delta f = \Delta\omega/2\pi$. The average power, P_o, delivered to a load resistance R_L at the demodulator output is:

$$P_o = \left[\frac{1}{R_L T}\int_0^T {v_o}^2(t)\,dt\right] = \left[\frac{k^2\Delta f^2}{2R_L}\right], \qquad where\ T = \frac{\omega_m}{2\pi}. \tag{2.12}$$

Each noise frequency component beats with the carrier wave to produce amplitude and phase modulation, as illustrated for a single frequency component of noise, $\vec{v}_n(t)$, in Fig. 2.1. Representing the moduli of the carrier and noise vectors as $|\vec{v}_c|$ and $|\vec{v}_n|$, respectively, the resulting modulation seen from Fig. 2.1 is:

$$\vec{v}_r(t) = \big(|\vec{v}_c| + |\vec{v}_n| cos(\omega_n t)\big) + j|\vec{v}_n| sin(\omega_n t). \tag{2.13}$$

In eqn. 2.13, the magnitude of the noise component is much smaller than the carrier amplitude X_c, i.e., $|\vec{v}_n| \ll |\vec{v}_c|$. Eqn. 2.13 simplifies to:

$$\vec{v}_r(t) = |\vec{v}_c| sin\big(\omega_c t + \theta(t)\big), \text{ where} \tag{2.14}$$

$$\theta(t) = arctan\left[\frac{|\vec{v}_n| sin(\omega_n t)}{|\vec{v}_c| + |\vec{v}_n| cos(\omega_n t)}\right] \approx \left[\frac{|\vec{v}_n|}{|\vec{v}_c|} sin(\omega_n t)\right]. \tag{2.15}$$

Similar to eqn. 2.11, the noise voltage produced at the output of the demodulator by the noise modulation of eqn. 2.14 is:

$$v_n(t) \propto \left[\frac{1}{2\pi}\frac{d\theta(t)}{dt}\right] \Rightarrow \; v_n(t) = \left[k \cdot \frac{|\vec{v}_n|}{|\vec{v}_c|} f_n \cdot sin(\omega_n t)\right], \tag{2.16}$$

where k is a constant of proportionality. The analysis thus far has assumed a single frequency-component of noise at f_n. The average noise power delivered to the load at

the demodulator output, P_{fn}, is written as:

$$P_{fn} = \left[\frac{1}{R_L T}\int_0^T {v_n}^2(t)\,dt\right] = \left[\frac{k^2 f_n^2}{|\vec{v}_c|^2}\cdot\frac{|\vec{v}_n|^2}{2R_L}\right]. \tag{2.17}$$

Assuming that the input noise has a flat power spectral density, S_n, the noise frequency components within a bandwidth *df* can be treated as a single frequency component at the center of the band with the same total noise power [2.3]. That is, the noise power in a bandwidth *df* associated with the single frequency component, f_n, can be related to S_n as follows:

$$S_n df = \frac{|\vec{v}_n|^2}{2R_L}. \tag{2.18a}$$

Substituting eqn. 2.18a in eqn. 2.17 yields:

$$P_{fn} = \left[\frac{k^2 f_n^2}{|\vec{v}_c|^2} S_n df\right] = \left[\frac{k^2 f_n^2}{2R_s P_c} S_n df\right], \qquad where\ P_c = \frac{|\vec{v}_c|^2}{2R_s}. \tag{2.18b}$$

In eqn. 2.18b, P_c is the average carrier power delivered to a resistance R_s. Assuming an IF bandwidth of $2f_m$, the total integrated noise power at the demodulator output is:

$$P_n = \int_{-f_m}^{f_m} P_{fn} = \left[\frac{k^2 S_n}{|\vec{v}_c|^2}\int_{-f_m}^{f_m} f_n^2 df\right] = \left[\frac{1}{3}\frac{k^2 S_n}{R_s P_c}(f_m)^3\right]. \tag{2.19}$$

Using eqns. 2.12 and 2.19, and assuming $R_s = R_L$, the signal-to-noise ratio (SNR_{FM}) at the demodulator output may be written as:

$$SNR_{FM} = \left[\frac{P_o}{P_n}\right] = \left[3\left(\frac{\Delta f}{f_m}\right)^2 \frac{P_c}{2S_n f_m}\right] = \left[\frac{3\beta^2}{2}\frac{P_c}{S_n f_m}\right]. \tag{2.20}$$

The SNR at the output of an AM demodulator receiving the same average power (at a modulation index *m*) and subject to the same noise power spectral density is calculated in [2.3] and shown to be:

$$SNR_{AM} = \left[\frac{m^2}{2}\frac{P_c}{S_n f_m}\right], \qquad where\ 0 \le m \le 1. \tag{2.21}$$

Eqn. 2.20 shows that the SNR increases with the modulation index. Compared to amplitude demodulation in eqn. 2.21, there is an SNR improvement of $3\beta^2$, which can be maximized with greater bandwidth occupation (e.g., doubling β results in a 10-dB improvement in SNR).

Digital modulation is comprehensively benchmarked on the basis of spectral efficiency and the signal-to-noise ratio requirement to meet a target BER [2.4]. Bandwidth-efficient schemes such as OFDM and QAM can maximize throughput in crowded ISM bands. However, they require a larger SNR to meet the same target BER when compared to FSK and PSK schemes [2.4], and require more complicated circuits to implement pre-distortion and other forms of DSP. Higher-order MPSK schemes show improved spectral efficiency at the expense of SNR performance and increased complexity. PSK systems appear most suited for high data-rate applications, but require linear amplifiers to preserve bandwidth and are more sensitive to noise, group delays and multipath reflections [2.5].

FSK systems tend to occupy more bandwidth, but are comparatively low in complexity (e.g., a dynamically tuned VCO is a fair narrowband modulator), they can operate at extremely low SNR values, provide the best BER performance under added Gaussian noise, and are not sensitive to phase and amplitude fluctuations. The design of wideband systems are, however, synonymous with circuit design challenges and increased power dissipation as discussed in Chapter 1. At present, there have been few demonstrations of integrated wideband circuits that verify the feasibility of energy-efficient communication links, e.g., the 3-5 GHz UWB-FM transceiver in [2.6]. Chapters 3 and 4 of this thesis detail the design and experimental characterization of a low-power multi-GHz FM demodulator suitable for wideband heterodyne applications.

2.2 FM demodulation: overview and architectures

Recovering the modulating signal from the received FM signal is known as demodulation or discrimination. Clarke and Hess [2.1] have identified that an overwhelming majority of existing FM demodulators fall within two classes of implementation. The first uses a phase-locked loop to track the FM modulation. The bandwidth of PLL demodulators is limited by the tuning range of the VCO and PLL settling time. The block diagram of the second and more widely used principle is shown in Fig. 2.2, where demodulation results from envelope detection of the differentiated input FM signal. The derivative of an FM signal (see eqn. 2.4) is:

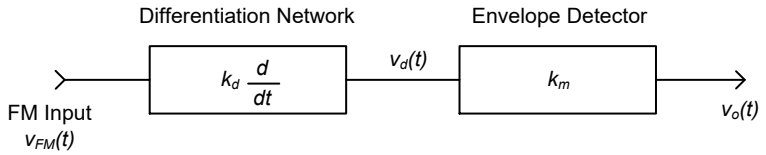

Fig. 2.2: Block diagram of a model frequency demodulator.

$$v_d(t) = X_c k_d [\omega_c + \Delta\omega f(t)] \cdot sin\left[\omega_c t + \Delta\omega \int_0^t f(t)dt\right]. \quad (2.22)$$

The highlighted term in the first parenthesis is the envelope that is proportional to the instantaneous frequency shown in eqn. 2.3, and is the output of the envelope detector. The signal term at the output is:

$$v_d(t) = X_c k_d k_m [\Delta\omega f(t)] = k[\Delta f \cdot f(t)]. \quad (2.23)$$

The result of equation 2.23 that captures the demodulated output was previously used in equation 2.11.

2.2.1 A note on synchronous detection

Multiplication of the differentiated output with an undifferentiated reference FM signal accomplishes synchronous detection. The resulting high-frequency component is centered at $2f_c$ and therefore permits detection of larger deviation ratios with negligible distortion when compared to asynchronous detection wherein the high frequency ripple is centered at f_c. A reference signal bearing a phase difference of ϕ_o with respect to an incoming FM signal described by eqn. 2.4 is:

$$v_{ref}(t) = X_r cos\left[\omega_c t + \Delta\omega \int_0^t f(t)dt + \phi_0\right]. \quad (2.24)$$

Multiplication of eqn. 2.24 with eqn. 2.22 yields a low-frequency output that depends on the phase difference of the two signals, i.e., ϕ_o:

$$v_d(t) \propto sin(\phi_o) \cdot [\Delta f\ f(t)]. \quad (2.25)$$

It is therefore desired to keep the reference signal quadrature-phased with respect to the incoming FM. Further, since the phase of the incoming FM can be arbitrary, the

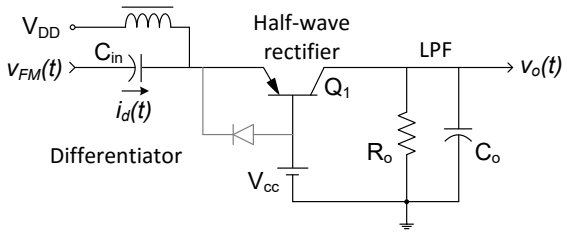

Fig. 2.3: Direct differentiation based demodulator.

quadrature-phased reference required for synchronous detection is best generated using it.

2.2.2 A brief synopsis of FM demodulators

The differentiation operation in the block diagram of Fig. 2.2 may be implemented in the frequency domain or as a time-delay. A classical direct differentiation demodulator is shown in Fig. 2.3. In this circuit, the capacitor current implements the differentiator. The current $i_d(t) \approx C\ dV_{FM}(t)/dt$ if the transistor and diode are ideal, and the entire input FM drops across the input capacitor, C_{in}. The half-wave rectifier and low-pass filer form the envelope detector. The circuit is sensitive to generator and transistor impedance that greatly limit its performance in practice.

An alternate direct differentiation based demodulator is presented by Darabi in [2.7]. A block diagram of the IF-demodulator is shown in Fig. 2.4. It operates at 1-MHz IF and is designed to demodulate down-converted IQ streams in an image-reject receiver. Differentiation is accomplished using op-amp stages in feedback and is therefore not suitable for wideband or high data-rate applications.

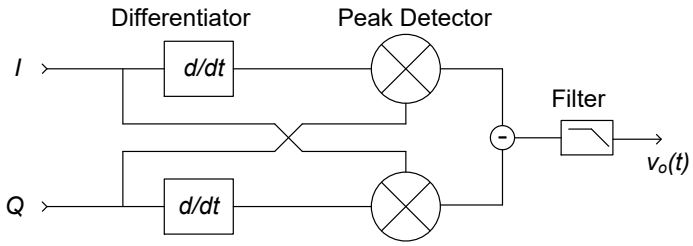

Fig. 2.4: Direct differentiation based IF-demodulator [2.8].

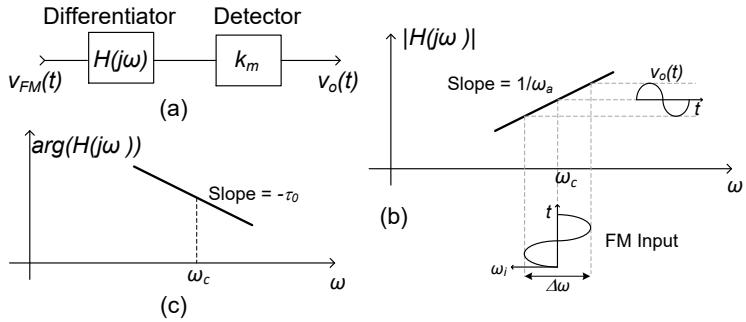

Fig. 2.5: (a) Frequency-domain differentiation based demodulator, frequency response of the network (b) Magnitude response, and (c) Phase response.

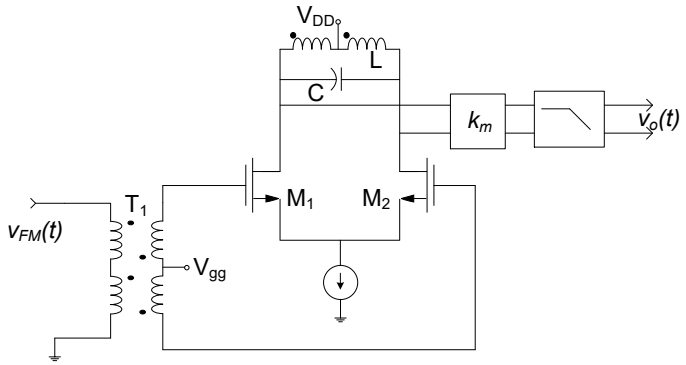

Fig. 2.6: FM demodulator using a frequency-domain LC differentiator.

Frequency-domain differentiators are networks whose magnitude response increases linearly around the FM-carrier frequency over the entire FM deviation with a constant slope, as shown in Fig. 2.5. The network converts the input frequency variation to amplitude variation at its output (illustrated in Fig. 2.5b). The output takes the form described by eqn. 2.22. The linear phase response shown in Fig. 2.5c ensures a constant group delay over the FM deviation. A practical implementation of the filter characteristics shown in Fig. 2.5 is an RLC tank [2.8]. It is evident that demodulators relying on linear phase characteristics of passive networks are better suited for narrowband applications. The single-slope and dual-slope demodulators belong to this category [2.1]. One possible embodiment of the block-diagram of Fig. 2.5 comprising an RF-amplifier (tuned to an offset from f_c) followed by asynchronous phase detection is shown in Fig. 2.6.

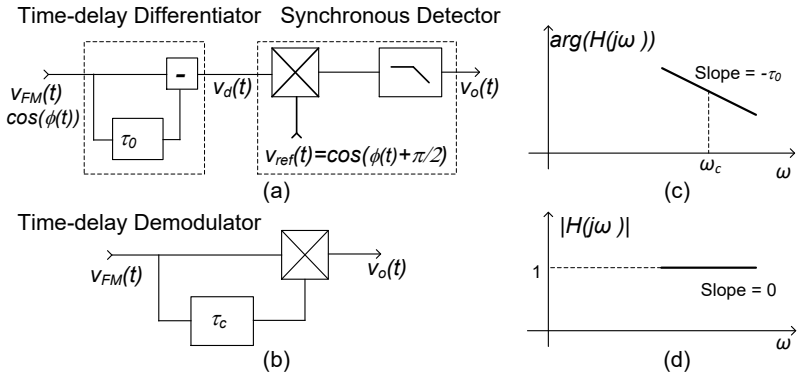

Fig. 2.7: Block diagrams of (a) a time-delay demodulator, and (b) a simplified version. Response of the delay-network: (a) Phase, and (b) Magnitude.

Time-delay differentiators implement the definition of a derivative:

$$f'(t) = \lim_{\tau \to 0} \frac{f(t) - f(t-\tau)}{\tau}. \tag{2.26}$$

Fig. 2.7a shows the block diagram of a time-delay differentiator. The delay, τ_o, may be implemented with a filter having a linear magnitude and phase response as shown in Figs. 2.7c and 2.7d. In section 2.2.1 it was shown that a phase difference of 90^o between the incoming FM and reference signal enables synchronous detection. This is noted in Fig. 2.7a. It can be shown analytically that the phase-shift can be transferred to the delay-path, leading to the simplified block diagram shown in Fig. 2.7b. A detail often missed in literature is that a 90-degree phase lag in a modulated signal is equivalent to introducing a quarter-time-period ($\tau_c = T_c/4$) delay in the carrier term only. This isolation isn't feasible in practice, when processing the received RF. For instance, in the case of a sinusoidally modulated FM signal described by eqn. 2.5, what is required ideally, and what can be implemented with any ideal delay/filter are:

$$v_{ref}(t) = X_c cos[\omega_C(t-\tau_c) + \beta sin(\omega_m t)] \text{ and} \tag{2.27}$$

$$v_{ref}(t) = X_c cos\big[\omega_C(t-\tau_c) + \beta sin\big(\omega_m(t-\tau_c)\big)\big], \text{ respectively.} \tag{2.28}$$

Eqn. 2.28 closely approximates eqn. 2.27 for narrowband applications ($\omega_c >> \omega_m$), however, the difference results in increased baseband distortion as the bandwidth of

the input FM increases. Using the definition of a derivative from eqn. 2.26 on the multiplication-result of eqns. 2.5 and 2.28, the low-pass-filtered demodulator output equals:

$$v_o(t) = k_{td} sin[\Delta\omega\tau_c \cdot cos(\omega_m t)] \approx k_{td}\Delta\omega\tau_c \cdot cos(\omega_m t), \quad (2.29)$$

In eqn. 2.29, k_{td} is a constant of proportionality, which captures the total transfer gain of all the circuit blocks. The demodulated output contains the modulating signal, and is proportional to the frequency deviation in the input FM.

The delay-network implementation using LC filters published by Bilotti in 1968 [2.9] is a widely used time-delay demodulator. Other examples include LC implementations of delay lines [2.10], and phase shift networks [2.11]. However, the narrowband linearity of the LC-tank load restricts wideband performance. Variation in magnitude response around the resonant frequency produces baseband distortion and the requirement for large signal-drive and high mixer gain raise the power consumption. The active Bessel filters based discriminator in [2.12] shows wideband performance in the MHz range ($\Delta f/f_c=0.5$). However, the need for high-order filters increases power consumption (12.6 mW), while g_m/C bandwidth restricts efficient detection to lower data rates (~1 Mbps).

2.3 Closing remarks on FM-demodulator theory

Basic principles of frequency modulation and a literature survey of demodulators have been presented. Bessel function coefficients characterizing the spectrum of an FM signal are introduced, which are used to characterize the propagation of an FM signal through an injection locked stage in the wideband FM demodulator presented in Chapter 3. Literature survey shows that direct-differentiation, filter-domain and time-delay demodulators implement the same general form of demodulation, which includes differentiation of the input FM followed by envelope detection. Their operating bandwidth is typically limited by the narrowband phase linearity of on chip passives. Analysis of SNR due to frequency modulation from noise will be used to augment the discussion on oscillator phase-noise analysis, which is discussed in detail in the remainder of this chapter.

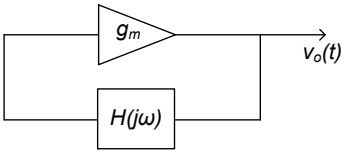

Fig. 2.7: Oscillator positive feedback model.

2.4 Oscillator Fundamentals

An oscillator is an autonomous circuit that converts DC-power to (ideally) a single-frequency tone at its output. It is central to phase-locked loops that generate the LO signal in RF transceivers (Fig. 1.1). An oscillator is modelled as a positive-feedback system as shown in Fig. 2.7, comprising a gain stage and a frequency-selective filter. The two minimum requirements for oscillation at a given frequency, f_c, known as Barkhausen's criteria, are: 1) magnitude of the loop-gain >1, and 2) phase around the loop is a multiple of $2n\pi$. When these are satisfied, the circuit amplifies its noise components at f_c incrementally, building up to stable oscillation. Amplitude limiting is inherent to any practical implementation of a gain stage that operates from a finite voltage supply.

2.4.1 Phase noise

The phase instability of an oscillator's output is expressed as the single-side-band noise power in a 1-Hz bandwidth at a certain frequency-offset from the carrier relative to the power of the carrier frequency. It is specified in decibels-below-the-carrier per Hertz (dBc/Hz). Noise generated by the active devices, passive networks and biasing sources modulate the carrier, which results in power transmission in bands offset from the desired frequency. The output of an oscillator takes the form of eqn. 2.1, where the time-varying phase, $\varphi(t)$, is an outcome of noise modulation.

A MOS transistor's channel-noise has two major components: white noise arising from random motion of charge carriers due to thermal excitation, and flicker noise arising from surface-trapping of charge carriers at the semiconductor-oxide interface. Thermal noise generated in the transistor-channel (and passives) has a flat power spectral density in RF bands, and appears with a -20dB/dec roll-off in a phase

noise plot versus offset frequency [2.13]. The flicker noise varies inversely with frequency (1/f roll-off) and is prevalent at low frequencies. It gets up-converted to the frequency of oscillation and appears with a 30-dB/dec roll-off in a phase noise plot versus frequency-offset. A review of phase noise models for circuit analysis is presented in Section 2.4, along with a discussion of the physical mechanisms that convert circuit noise to phase noise.

2.4.2 Injection locking

Synchronization of the operating frequency of an autonomous system with that of an external stimulus is known as injection locking. An oscillator at f_0 can be forced to track the phase and frequency characteristics of an uncorrelated external signal in the vicinity of its natural frequency ($f_0 \pm \Delta f$). The frequency band, Δf, over which the oscillator locks, depends on the strength of the applied signal and inversely on the phase stability of the oscillator. Phase-stable systems are less sensitive, and only lock over a narrow frequency range. Static locking to single frequencies in LC oscillators is explained in [2.14] using vector algebra, and provides valuable design insight for the application of injection locking. The phenomenon of locking was first observed 350 years ago in pendulum clocks by Huygens, and the quest for analytical models capturing the phenomenon continues to intrigue the scientific community [2.15]. In this thesis, we successfully demonstrate injection locking to modulated signals over a wide bandwidth and investigate its merits for low-power, low-complexity demodulation. Experimental characterization reveals time-dependencies and hysteresis accompanying injection locking, along with the impact of external noise on the locking-process. These results are presented in Chapter 4.

2.5 Ring oscillators

Ring oscillators are formed by placing a number of series-connected gain stages in a closed loop. Each stage is typically associated with a voltage gain $-A_0$ (negative sign for phase inversion of a MOS amplifier) and a single pole frequency, ω_0, that is associated with a first-order RC load. Considering that each pole effects a maximum phase-shift of 90 degrees, a minimum of three inverting stages are required to form a

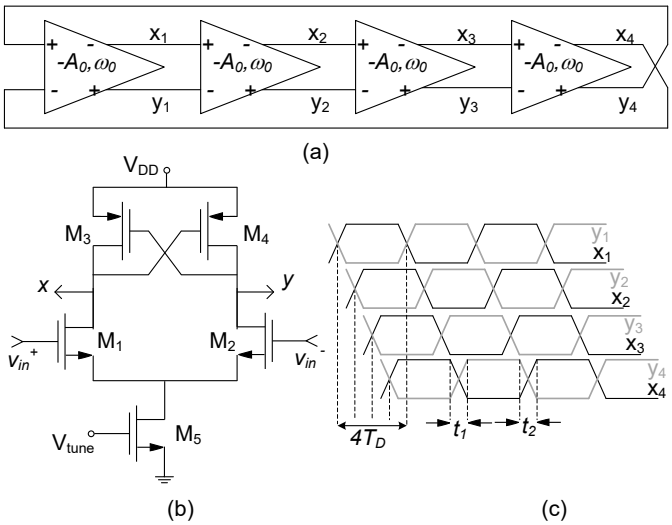

Fig. 2.8: (a) 4-stage differential ring oscillator and (b) circuit implementation of each stage, and (c) output voltage waveforms.

ring oscillator. A four-stage ring oscillator is shown in Fig. 2.8a, comprising differential gain stages. The cross-connection at the output of the 4th-stage interface adds a 180-degree phase shift, resulting in a 45-degree phase lag between successive stages. As a result, the frequency of oscillation for a 4-stage ring oscillator coincides with ω_0. Node-pairs a_1-a_3 and a_2-a_4 shown in Fig. 2.8a are quadrature-phased. Neglecting loading of the stages, the linear transfer-function of the loop comprising the 4-stage cascade can be written as:

$$T(j\omega) = -\left[\frac{A_0}{(1 + j(\omega/\omega_0))}\right]^4. \tag{2.30}$$

To satisfy the second Barkhausen criterion for oscillation, the magnitude of $T(j\omega)$ from eqn. 2.30 is equated to one for ω equal to ω_0. This results in a minimum voltage gain requirement of $\sqrt{2}$ per stage.

One possible implementation of a gain stage is shown in Fig. 2.8b. The cross-coupled PMOS load provides regenerative gain that ensures faster transients at the output compared to an NMOS differential amplifier with resistor loads, i.e., shorter switching durations noted in Fig. 2.8c as '*t1'* and '*t2*'. It is also important to note that the oscillator draws current chiefly during t_1 and t_2, when the nodes x and y

discharge via transistors M_3 and M_4, respectively. Frequency tuning is implemented via a variable resistor at the tail node, where M_5 is operated in triode and controlled by V_{tune}. The time-domain waveforms of the internal oscillator nodes are shown in Fig. 2.8c. The 45-degree phase-lag per stage translates to an oscillation period of $8T_D$. As discussed in [2.16] in the context of a 3-stage ring oscillator, a difference exists in the large-signal period and frequency of oscillation derived from eqn. 2.30. In practice, it is not necessary that $1/8T_D$ equals ω_0 since the large-signal behavior of transistors veers from Q-point performance due to non-linear transfer characteristics. The oscillator start-up (e.g., from noise), in the absence of loading, begins at ω_0, and as the amplitude grows the system frequency shifts and stabilizes at $1/8T_D$.

An injection-locked, 4-stage differential ring oscillator is used in the implementation of an FM-demodulator in this thesis. The weak selectivity of the circuit makes it sensitive to external stimuli, allowing it to lock over a wide frequency range [2.17]. It will be shown later in Chapter 3 that the quadrature-phased signals inherent to the circuit both facilitate and simplify wideband demodulation.

2.6 LC oscillators

Integrated LC oscillators have a resonant tank comprised of a spiral inductor (L) and a tuning capacitor (C) that sets the oscillation frequency to $1/2\pi\sqrt{LC}$. Sheet resistance of the on-chip metallization introduces conductor losses in the spiral inductors and parallel-plate capacitors. Finite conductivity of the substrate results in eddy and displacement current losses that lower the inductor's quality factor (Q). Eddy-current losses reduce with increasing substrate resistivity, while uncertainty of the substrate-potential beneath the windings makes the precise calculation of displacement-current losses difficult using simulators like EMX™ and ADS-Momentum™ [2.16]. The schematic of a cross-coupled LC oscillator is shown in Fig. 2.9a. The series loss components of the passives L and C can be modeled by a parallel equivalent resistance, shown as 'R_p' in Fig. 2.9b, where $R_p \approx (Q\omega L)$ [2.1].

The cross-coupled transistor pair is the equivalent of a differential pair placed in positive feedback. The impedance looking into the FET-pair, noted as 'Z_{in}' in

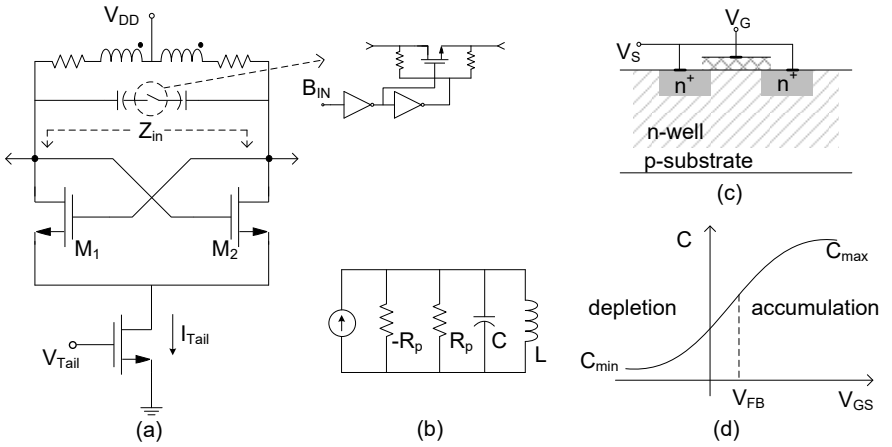

Fig. 2.9: (a) Cross-coupled LC oscillator, (b) equivalent representation at resonance, (c) cross-section of an accumulation-mode varactor, and (d) its C-V characteristic versus gate-source voltage.

Fig. 2.9a is $-2/g_m$, where g_m is the small-signal transconductance of each transistor. This negative resistance offsets the losses R_p, resulting in oscillation when $g_m R_p \geq 1$.

During large-signal steady-state operation the conductance offered by the cross-coupled pair varies between 0 and more than $-g_m/2$ with time. The effective transconductance over one period of oscillation, $-G_m$, during steady-state operation is $\sim 1/R_p$ assuming it perfectly offsets the tank loss [2.19]. The oscillator's operation is approximated by the tail current switching between either transistor-arm within one time-period. At the fundamental frequency, the square-wave decomposition results in a differential output voltage swing of $(4/\pi)I_{Tail}R_p$ [2.18]. The approximation doesn't take into account simultaneous conduction in M_1 and M_2, transistor operating modes, and tank-loading due to the finite, non-linear transistor output impedance. This is why a direct relationship between the output swing and tail-current is not observed over a wide range of I_{Tail}.

Two points of note that arise within the framework of the above approximation are: 1) as the tail current is increased for a given tank R_p, the effective large-signal $-G_m$ remains constant and equal to $1/R_p$. The excursions of $g_m(t)$ increase, but the average value remains constant, and 2) given that $-G_m$ remains constant, it can be assumed

that the phase noise contributed by the transistors in the $1/f^2$ region is independent of their aspect ratio and transconductance [2.19].

2.6.1 Frequency tuning

Frequency tuning is accomplished on chip using varactors or digitally-switched capacitor banks as shown in Fig. 2.9a. On-chip varactors are constructed either with PN junctions, or using the capacitance between the gate terminal and the shorted drain and source terminals of a MOSFET. An accumulation mode varactor is constructed by placing N^+ diffusions in an n-well, as shown in Fig.2.9c, and its C-V characteristic is shown in Fig. 2.9c. Increase in V_{GB} beyond the flat-band voltage (V_{FB}) results in accumulation of majority carrier electrons at the semiconductor-oxide interface resulting in maximum capacitance. When V_{GB} is reduced, repulsion of electrons from the interface results in a series depletion capacitance that reduces overall capacitance [2.20]. When compared to the pn-junction varactor, the MOS varactor is better suited for low V_{DD} operation and can handle positive and negative voltages. The Q-factor of the MOS-varactor depends on the drain-source resistance, and typically drops as C_{GS} increases since the relative increase in capacitance is larger than the relative drop in accumulation-resistance [2.16]. Discrete tuning using switched, parallel-plate metal-oxide-metal capacitor banks implements higher quality factor capacitors, and circumvents MOS-capacitor non-linearity at the cost of fine frequency tuning and increased complexity. In the low-noise oscillator presented in Chapter 5, digital frequency tuning is implemented, and the switch implementation shown in Fig. 2.9a is described in greater detail.

2.6.2 LC tank design

The LC tank of an oscillator should be designed to minimize phase noise for a specified power budget and tuning range. For low-power designs with a target output swing (if not specified, it is best designed for a swing that results in the lowest phase noise), an inductor having the required R_p at f_0 with maximum Q is often selected. The inductor design requires a few simulation iterations that involve an optimization of width, turns, spacing and shielding [2.21]. Inductor Q typically

dominates the tank's quality factor in the low-GHz frequency range. In general, the optimal tank is determined by accounting for the quality factor of the fixed capacitance required to bridge the frequency gap between f_0 and the inductor's self-resonance frequency. In designs targeting extremely low phase noise with no limit on the power budget, the aim is to deliver maximum power to the load (R_p), while keeping the output swing at a maximum. Following the qualitative discussion in [2.22], increasing the bias current beyond an accompanying increment in output swing degrades phase noise in a cross-coupled LC oscillator. Neglecting the effect of loading[1], a reduction in phase noise can be obtained without loss of phase-noise efficiency by iteratively reducing R_p (assuming tank-Q remains constant) and compensating the drop in output swing with increase in I_{TAIL}. Down-scaling of inductance is accompanied by drop in self-coupling[2] and reduction in substrate losses. Though the latter results in a higher inductor-Q, the overall tank-Q is degraded by the impact of parasitic via resistances on-chip. A tank with a lower inductance requires a larger fixed capacitance to resonate at the same f_0, which affects tuning range and tuning sensitivity as well. In conclusion, optimization of an oscillator's resonator depends on the circuit specifications and can be used to

[1] This optimistic first-order assumption is surveyed in Section 2.7.5 where mathematical analysis and simulation are compared.

[2] In a multi-turn inductor the total inductance is the sum of partial self-inductances of each segment, and positive and negative mutual inductances [2.23], [2.24]. The coupling between orthogonal segments is negligible (assuming the magnetic field produced by one conductor has a constant gradient across the width of the other, i.e., $\oint B.ds = 0$). Segments along which current flows in the same direction couple positively, and those with opposite currents couple negatively. The simplification in [2.23] shows that the mutual inductance between any two parallel segments is approximately proportional to $2l\cdot[log(2l/d)-1]$, where l is the conductor-length and d is the spacing between them. Calculating the coupling between mutually angled segments in hexagonal and octagonal coils is computationally intensive and detailed in [2.25]. Multi-turn inductors commonly used on chip (resembling auto-transformers) show improved area efficiency because of the dominant positive mutual coupling between the closely spaced segments carrying currents in the same direction. The differential inductance $L_D=2\cdot L_0(1+k_{mm})$ and the common-mode inductance $L_{CM}=0.5\cdot L_0(1-k_{mm})$, where L_0 is the inductance of the unwound coil, and k_{mm} is the net coefficient of self-coupling [2.26]. Small inductances on the order of ~100 pH require just a single turn, for which k_{mm} diminishes and results in a lower ratio of inductance and conductor loss (L/r_{cond}).

balance priorities between power consumption, phase noise and tuning range for a target operating frequency based on the constraints of the technology.

2.7 A review of phase noise models

This section briefly discusses oscillator phase-noise models. Phase-noise models have typically revolved around their application to LC oscillators, and over time the gradual increase in knowledge of phase noise mechanisms has opened doors for innovation in low-noise oscillator design. All phase noise models assume that additive noise in the signal loop does not alter the frequency of oscillation.

2.7.1 Leeson's phase noise model

D.B. Leeson presented a simplified, empirical model for the phase noise of a tuned oscillator in 1966 [2.27] based on experiments that stated:

$$L(\Delta\omega) = 10 \cdot log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right\}\left\{1+\frac{\Delta\omega_{1/f}}{|\Delta\omega|}\right\}\right]. \quad (2.31)$$

In eqn. 2.31, Q is the quality factor of the tank, ω_c and $\Delta\omega$ are the carrier and angular offset frequencies, respectively, and the fitting-parameter F is the excess noise factor of the oscillator. Boltzmann's constant is denoted by k, T is the temperature, P_{sig} is the peak signal power at ω_c, and $\Delta\omega_{1/f^3}$ is the flicker-noise corner-frequency. Neglecting *1/f* noise and assuming $\omega_c >> \Delta\omega$, the equation simplifies to:

$$L(\Delta\omega) = 10 \cdot log\left[\frac{2FkT}{P_{sig}}\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right]. \quad (2.32)$$

Leeson's paper provides little detail on phase-noise mechanisms but insights from the eqns. 2.31 and 2.32 have proven valuable for oscillator design. Namely, maximizing tank-Q and the signal power of an oscillator improves its phase-noise performance. The model asserts that $\Delta\omega_{1/f^3}$in the PN plot equals the device *1/f*-corner frequency, however, measurements show otherwise. Therefore, similar to *F*, this too is a fitting parameter. Leeson's model of eqn. 2.31 accounts for the four regions seen in a phase noise measurement: 1) -30dB/dec roll-off due to *1/f* noise, 2) -20dB/dec roll-off due to thermal noise, 3) -10 dB/dec roll-off due to 1/f noise from the buffer interfacing the oscillator under test and the measurement setup, and 4) a

noise floor due to the thermal noise of the buffer. The two latter regions are represented by the inclusion of '1' in the two curly brackets of eqn. 2.31. Leeson postulated that when Q is very large, the 30-dB/dec can predominate out to a frequency offset of $\omega_0/2Q$, in which case there is no 20-dB/dec region in the phase noise curve.

Along the timeline there have been several phase-noise analyses that confirm Leeson's empirical form of eqn. 2.31. The analysis by Craninckx in [2.28] – based on a linear-feedback model applied to an LC oscillator in steady-state oscillation – agrees with Leeson's conclusion that phase noise is inversely proportional to the signal-to-noise ratio and the square of the tank quality factor. However, the analysis does not converge on a solution for Leeson's noise factor, *F,* in eqn. 2.31. A similar outcome is reached using the comparatively simpler filter-based analysis described in the next sub-section.

2.7.2 Filter-based noise shaping

The noise-shaping analysis for an LC load is eloquently paraphrased in [2.29]. The impedance of an LC tank in the vicinity ($\Delta\omega$) of its center-frequency, ω_0, is approximately:

$$Z(\omega_0 + \Delta\omega) \approx \left[j\frac{\omega_0^2 L}{2\Delta\omega} \right], \\ \Rightarrow |Z(\omega_0 + \Delta\omega)| = \left[\frac{1}{G}\frac{\omega_0}{2Q \cdot \Delta\omega} \right]. \tag{2.33}$$

In eqn. 2.33, G is the conductance of the tank. The mean-square noise spectral density of the tank conductance equals:

$$i_n^2/\Delta f = 4KTG. \tag{2.34}$$

The spectral density of the mean-squared noise voltage equals:

$$(i_n^2/\Delta f) \cdot |Z|^2 = 4kTR\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2. \tag{2.35}$$

The mean-square noise voltage contributes equally to amplitude and phase modulation sidebands. This orthogonality neglects phase modulation produced by the non-linear response of device capacitance and conductance to the amplitude

modulation sidebands. Pure AM is rejected by amplitude limiting inherent to the oscillator[3], and the phase noise is expressed as the ratio between the root-mean-squared noise and differential signal voltage (V_{rms_d}) contained in a 1-Hz bandwidth:

$$L(\Delta\omega) = 10 \cdot log\left[\frac{2kTR}{V_{rms\_d}^2}\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right] = 10 \cdot log\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right]. \quad (2.36)$$

Note: the differential mean-square signal power equals the peak single-ended power (P_{sig}) in an LC oscillator. Including a noise factor F to account for transistor noise yields the result obtained by Leeson given by 2.32.

2.7.3 Phasor based LTV analysis

The ambiguous noise factor, F, in Leeson's model fails to throw light on phase-noise contribution mechanisms of active circuits. The phasor-based approach described by Samori in [2.19] evaluates phase and amplitude sidebands produced by additive noise in cross-coupled LC oscillators. It is shown that large-signal periodic switching of the transistor-pair in a current-limited oscillator results in negligible phase-noise contribution from amplitude sidebands and noise around harmonics folds back to the carrier. The second observation of note, as discussed in Section 2.5, states that the effective transconductance over one period of oscillation, $-G_m$, during steady-state is approximately $\sim 1/R_p$. Building on this approach, Rael compares the large-signal operation of the cross-coupled pair to a mixer in [2.22], to obtain valuable insight on phase-noise mechanisms in a cross-coupled LC oscillator. Three prominent noise sources in the oscillator are the tank resistance, FETs and the tail-current source. Time-invariant thermal noise from the tank affects phase noise directly, as seen from eqn. 2.36.

The tail-current noise around DC, dominated by *1/f* noise, is up-converted to RF via the switching action of the cross-coupled FETs and the noise around the second-harmonic is down-converted to f_0. The down-converted noise contributes to phase noise, which is calculated in Section 2.7.3. The up-converted *1/f* noise

[3] This is further discussed in the next sub-section.

predominantly produces AM, which translates to phase noise through non-linearity of varactors or the switching FETs themselves. An explanation is that the slow varying *1/f* noise modulates the DC current, which in turn modulates the output amplitude over time. However, the analysis in [2.30] does show that the output frequency first increases with bias current and as the harmonic in the transistor's output current begin to increase, the frequency drops in accordance with Groszkowski's observation[4] to maintain the energy balance between L and C [2.31]. The analysis in [2.30] also shows that the dependence of output frequency on the tail-current diminishes when the tank capacitance is much larger than the parasitic capacitance on the common-source node of the oscillator, which is often the case with oscillators designed for low phase noise (see section 2.5.2). This backs the intuition that the dominant consequence of tail-current *1/f* noise is amplitude modulation.

The mean-square current noise spectral density from the switching FETs is $4kT\gamma g_m$ (the excess noise factor, γ, is a bias-dependent fitting parameter), at the zero-crossing time window when both transistors are in saturation. As per the approximations discussed in Section 2.5, this equals a noise contribution of $4kT\gamma/R_p$ over one cycle, leading to the conclusion that as a first-order approximation, the device noise contribution is unrelated to its dimension or transconductance. The complete phase noise equation for the LC VCO circuit calculated in [2.22] for a tail-current transconductance (g_{mT}) equals (each contribution is derived individually in section 2.5, along with a discussion on the underlying assumptions):

$$L(\Delta\omega) = 10 \cdot log\left[\frac{2kT\{1+\gamma(1+(4/9)g_{mT}R_p)\}}{P_{sig}}\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right]. \quad (2.37)$$

In eqn. 2.37, the noise factor F is given by:

$$F = 1 + \gamma + \gamma\alpha g_{mT}R_p. \quad (2.38)$$

For a g_m-core switching with a conduction angle equal to π (i.e., 50% duty-cycle),

[4] Harmonic components of the transistor's current flow into the lower-impedance capacitor and increase the reactive energy in it. The frequency of oscillation shifts down until the reactive energy in the inductor increases to equal that of the capacitor for steady-state balance.

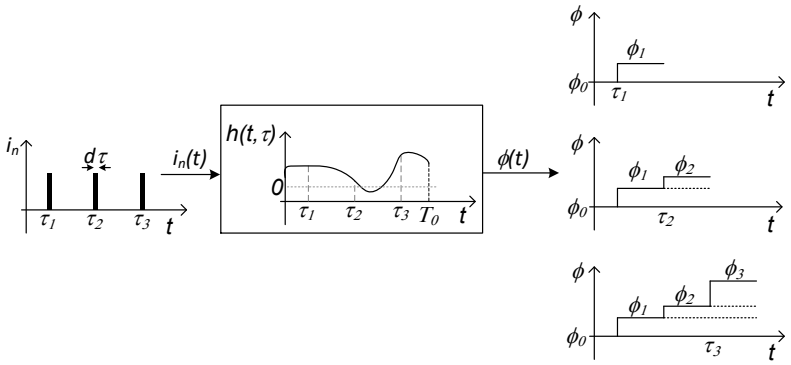

Fig. 2.10: Example of a linear phase system typified by eqn. 2.39.

the corrected value of α (4/9 in eqn. 2.38) is shown to be ~0.085 via simulation in [2.32]. Eqn. 2.36 takes the form of Leeson's model, however, the insight on noise mechanisms lead to the concept of tail filtering [2.18]. The tail-current noise at $2f_0$ may be filtered via a capacitor from its drain (drain of M_3 in Fig. 2.9a) to ground, and a high-impedance to isolate the tail current noise at $2f_0$ is realized using a parallel resonant tank between the common-source node of the g_m-pair and the drain of the tail current source. High impedance at the tail net has two important impacts when one transistor is on and the other is cut off: 1) it reduces loading of the tank due to triode operation of the switching FETs, and 2) the noise of the cross-coupled transistors appearing at the output is reduced by the high source impedance in the common-mode path.

2.7.4 Hajimiri's LTV phase noise model

The pursuit of a linear, time-varying (LTV) phase-noise model started as early as 1966 [2.33], [2.34], and is presented in a simple closed-form by Hajimiri and Lee in [2.29], [2.35]. The theory describes an impulse sensitivity function (ISF), which quantifies the phase sensitivity of the oscillating waveform to perturbations at different time instances within one cycle. The ISF is used to obtain a more accurate representation of noise modulation in the noise-to-signal ratio, which is phase noise. From eqn. 2.15 it's seen that: 1) the output phase is actually a non-linear, inverse-tan function of the magnitudes of the signal and noise voltages, 2) assuming that the

noise amplitude is negligible in comparison with the signal amplitude, a linear relationship can be established between output phase and the noise amplitude, and 3) amplitude modulation is disregarded for simplicity since oscillators are typically self-limiting and demonstrate an amplitude response that damps out amplitude irregularities over time[5] [2.1]. As discussed in Section 2.6.3, the contribution of AM sidebands to phase noise is negligible when the oscillation amplitude increases. However, a correlation between amplitude- and phase-modulation sidebands exists via non-linear transfer characteristics of varactors, transistor overlap capacitances, and output conductance. These are ignored in our application of the LTV model.

The conversion of noise amplitude to signal phase depends on the oscillator type, and within the bounds of a linear approximation, it is captured in the impulse sensitivity function described in [2.35]:

$$\phi(t) = \int_{-\infty}^{\infty} h(t,\tau) i_n(\tau)\, d\tau \tag{2.39}$$

The implication of eqn. 2.39 is simple. Hinged on a linear approximation, it suggests that the phase error at any given time, $\phi(t)$, is an aggregate of phase shifts produced by noise impulses, $i_n(\tau)$, at varying times instances, τ, and of duration $d\tau$[6]. The term $h(t,\tau)$ in eqn. 2.39 captures the impulse-response of the oscillator with respect to phase, and is the ISF. It is a normalized function that varies between -1 and +1. A graphical illustration of eqn. 2.39 is shown in Fig. 2.10. The ISF is periodic with a time period, T_0, and differs at instances τ_1, τ_2 and τ_3. The phase shift is an aggregate of the individual phase shifts produced by the three noise impulses in this example. In most cases, the ISF is closely related to the output voltage waveform of an oscillator. The phase noise expression assumes a cyclostationary random noise process, i.e., the statistical properties of noise sources are time-varying and periodic, and that phase noise can be captured with knowledge of signal and noise powers and the ISF within one oscillation period. Unlike Rael's mixer-based approach tailored for the cross-coupled LC oscillator, the LTV model can be used to predict the phase

[5] The impact of amplitude modulation on phase noise is calculated in [2.35].

[6] Current impulses imply instantaneous charge-injection into the tank.

noise of any practical oscillator provided the phase noise conversion of each individual noise source can be captured analytically. The sources of error discussed above are summarized as: 1) a linear approximation of the amplitude-to-phase transfer, and 2) disregarding the correlation between amplitude and phase modulation.

Another assumption made in development of the theory that is evident from the illustration of Fig. 2.10 is that the phase shift in the signal output, $\phi(t)$, is not reflected in the sensitivity function, which ideally should overlap with the phase of the output waveform[7]. However, this can be justified as follows: phase fluctuations induced by noise are negligible compared to the period of oscillation, and therefore so is the resulting shift in ISF. The closed-form phase-noise expression (that includes noise-folding coefficients from harmonics) for an oscillator comprising a load where the output swing is seen across a capacitor is derived in [2.35]:

$$L(\Delta\omega) = 10\ log\ \left[\frac{\sum_i S_i}{2q_{max}^2\Delta\omega^2}\right], where \tag{2.40}$$

$$S_i = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_i^2(\phi)\overline{i_i^2}(\phi)\, d\phi. \tag{2.41}$$

In eqn. 2.40 S_i is the phase noise contribution of the i^{th} noise source, q_{max}^2 is the maximum charge displaced in the filter capacitance, and $\Delta\omega$ is the frequency offset in radians/s. In the r.m.s-integral, $\Gamma_i(\phi)$ is the ISF of the i^{th} noise source. By knowing $\Gamma_i(\phi)$ for every noise contributor, Leeson's noise factor, F, can be calculated for any oscillator circuit with a load comprising a capacitor in parallel with an effective resistance or inductance. Though it is not as rigorous as the mathematically intensive studies in [2.36], [2.37], the ISF-approach has gained a lot of traction because it is intuitive and fairly accurate against simulation and measurement when applied correctly.

[7] A brilliant criticism of all LTV approaches made in [2.36] is that the assumption of cyclostationarity in the treatment of oscillator phase noise, by definition, implies the availability of a precise time reference, while the purpose of the phase noise analysis is to quantify the lack of it.

An important point of note is that when the ISF equals zero, no phase shift is induced in the oscillating waveform by noise. Therefore, one would like to design a low-noise oscillator where noise is injected at ISF zero crossings. An alternate approach to low phase noise design would be to maximize the region of phase insensitivity where the ISF equals zero and inject signal and noise currents therein. As a result, reduction in phase-noise conversion of noise generated by the transistors and the resonator can be accomplished. Proposal of this notion and experimental study of a prototype oscillator that embodies the approach forms a part of this thesis. The design concept of phase desensitization of an oscillator via hard limiting presented in this thesis [2.38] is analyzed using Hajimiri's LTV theory in Chapter 6.

2.8 Detailed analysis of noise in cross-coupled LC oscillators

In this section, the phase-noise performance of the cross-coupled oscillator of Fig. 2.9a is analyzed in detail. The contribution of each noise source in the circuit, namely, the LC tank, pair of switching transistors and tail-current source are examined in detail. Comparisons between theory and simulation are presented, which highlight phase-noise limitations of on-chip oscillators and the challenge of achieving the GSM base-station specification.

In the following analysis, differential operation is treated as a summation of single-ended signal and noise powers, and therefore, the parameters of tank impedance (R_p), peak voltage swing (V_0) and tank capacitance (C_o) and inductance (L) correspond to half-circuit or single-ended values. Using the substitutions specific to a 2nd order LC tank of $q_{max} = CV_0$, $C_o^2 = \omega^4 L_o^2$ and $Q = R_p/\omega L_o$ the phase noise expression from eqn. 2.40 simplifies to:

$$L(\Delta\omega) = 10 \cdot log\left[\left(\frac{R_p}{2P_{sig}}\right)\left(\frac{\omega_c}{Q\Delta\omega}\right)^2 \sum_i S_i\right], \qquad (2.42)$$

$where\ P_{sig} = V_0^2/R_p.$

In eqn. 2.42, the phase-noise contribution of individual noise sources, S_i, is calculated using eqn. 2.41 that contains the impulse sensitivity of each individual noise contributor.

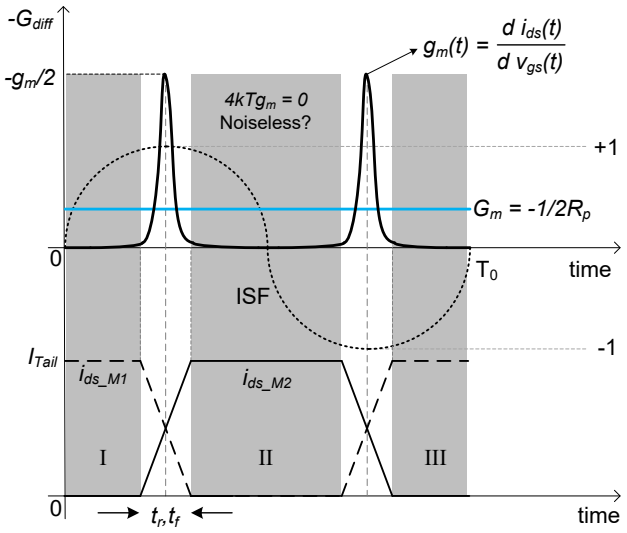

Fig. 2.11: Periodic large-signal transconductance of the cross-coupled devices.

2.8.1 LC tank noise

The resonator's thermal noise expressed as a current spectral density equals $4kT/R_p$, and from [2.25] $\Gamma(\phi) = -sin(\phi)$[8]. Therefore, S_{tank} can be written as:

$$S_{Tank} = \frac{1}{2\pi}\frac{4KT}{R_p}\int_0^{2\pi} sin^2(\phi)d\phi = \frac{2KT}{R_p}. \tag{2.43}$$

When N tanks are connected in a loop, the effective filtering increases by a factor of N^2, and the number of noise sources increases by N. This results in an improvement in phase noise by a factor of N [2.16], [2.39]. The phase-noise contribution of the tank in a differential oscillator is calculated by setting N = 2 in eqns. 2.42 and 2.43:

$$L(\Delta\omega)_{tank} = 10 \cdot log\left[\frac{N}{N^2}\left(\frac{R_p}{2P_{sig}}\right)\left(\frac{\omega_c}{Q\Delta\omega}\right)^2\frac{2KT}{R_p}\right],$$
$$\Rightarrow L(\Delta\omega)_{tank} = 10 \cdot log\left[\left(\frac{2KT}{P_{sig}}\right)\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right]. \tag{2.44}$$

[8] $\Gamma(\phi) = -sin\phi$ for an LC oscillator whose output is described by $cos\phi$. In this case $\Gamma(\phi)$ is quadrature-phased with respect to the tank voltage. In most oscillators the ISF can be approximated by the derivative of the output voltage waveform.

The result of eqn. 2.44 is identical to the phase-noise contribution of the tank predicted by the approaches described in sections 2.6.1 – 2.6.3 (see eqns. 2.32, 2.36 and 2.37).

For sake of completeness, the result of eqn. 2.44 is obtained directly for the differential LC oscillator. The load equals $2R_p$ and the resonator's current-noise spectral density equals $4kT/2R_p$. Therefore, S_{tank} equals:

$$S_{Tank\_diff} = \frac{1}{2\pi}\frac{4kT}{2R_p}\int_0^{2\pi} sin^2(\phi)d\phi = \frac{kT}{R_p}. \tag{2.45}$$

The impulse sensitivity function, which is a function varying between ±1 does not change in the case of differential operation. The maximum charge displaced in the differential resonator ($C{\cdot}V_0$) equals that in the single-ended case (w.r.t eqn. 2.40) because the differential capacitance is half the single-ended capacitance, and the peak fundamental output swing doubles for a differential output. The phase-noise contribution of the differential tank is, therefore, calculated using eqns. 2.42 and 2.45 as:

$$\begin{aligned} L(\Delta\omega)_{tank} &= 10 \cdot log\left[\left(\frac{(2R_p)}{2P_{sig\_diff}}\right)\left(\frac{\omega_c}{Q\Delta\omega}\right)^2\frac{KT}{R_p}\right], \\ \Rightarrow L(\Delta\omega)_{tank} &= 10 \cdot log\left[\left(\frac{2KT}{P_{sig}}\right)\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right] \end{aligned} \tag{2.46}$$

In the above simplification, a factor '2' is incorporated in the squared term, and the differential signal power, P_{sig_diff}, is replaced with the single-ended signal power, P_{sig}, to remain consistent with eqn. 2.44.

2.8.2 Cross-coupled transistor pair noise

The cross-coupled transistors are typically treated as current switches during large-signal operation. Each transistor (M_1 and M_2) conducts during one-half of the time period when the other is cut-off. Fig. 2.11 is an illustration of differential transconductance resulting from individual transistor drain currents. The time varying transconductance, $g_m(t)$, is the derivative of drain current with respect to the

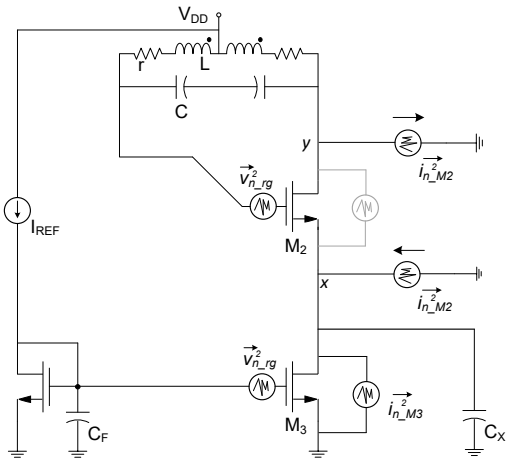

Fig. 2.12: Periodic large-signal conduction state of one cross-coupled device.

driving gate-source voltage. During rise and fall transients (t_r and t_f in Fig. 2.11), $g_m(t)$ first increases with gate drive and attenuates with the accompanying drop in drain-source potential as the transistor enters triode. The non-linear characteristics of the output current versus the sinusoidal gate-drive voltage result in amplitude control during steady-state operation. The output swing and Q-point transconductance, g_m, increase with bias current, which results in reduced rise and fall times t_r and t_f. The transconductance drops to a very low value in deep-triode when the output current reaches its limit (see regions I, II and III highlighted in Fig. 2.11). It takes very little to surmise from Fig. 2.11 that $4kT\gamma g_m(t)$ is a poor approximation for transistor noise, for it implies a noiseless on-state.

Consider Fig. 2.12 that shows the oscillator state when one of the cross-coupled transistors (M_1) is cut off, and the second transistor (M_2) conducts. As shown in Fig. 2.12 the channel noise[9] of M_2 can be decomposed into two equal contributions: from, and to ground [2.40]. If the impedance looking into the tail-current source, M_3, at node-x is much higher than the impedance looking into M_2, the two channel-noise components at nodes x and y compensate each other, and the noise current reaching

[9] The channel noise is not constant during the half-period when M_2 conducts, since both V_{GS} and V_{DS} vary sinusoidally with time, thereby affecting the channel-noise spectral density even in saturation.

the tank is negligible in regions I, II and III in Fig. 2.11. In this ideal scenario, the noise contribution of the transistors is limited to time intervals t_r and t_f in Fig. 2.11, when M_1 and M_2 conduct simultaneously. The noise currents of the two transistors find a path to the tank via the low impedance source nets. During this time, one transistor transitions from triode to cut-off via saturation and the other from cut-off to triode via saturation, respectively.

The above approximation is an unlikely one, given the finite and often low output impedance of the tail-current source in sub-micron CMOS, and the presence of parasitic capacitance C_X (see Fig. 2.12) at node *x*. The analysis in [2.32] is built around the assumption of an ideal tail-current source, however, the result best describes Hegazi's tail-filtering oscillator [2.18], in which a resonant network presents a high impedance at node *x*. Assuming a perfect implementation of Hegazi's concept of tail filtering to minimize phase noise contribution of the cross-coupled transistors, it is clear from Fig. 2.11 that the period of simultaneous conduction (transition times t_r and t_f) should be minimized. There is no doubt that an oscillator's phase noise is a function of t_r and t_f. However, the analysis of a cross-coupled oscillator in [2.32] represents t_r and t_f by an equivalent conduction angle and states that oscillator phase noise can be computed with acceptable error when the transconductance when averaged over one time-period (G_m) is assumed to exactly compensate tank loss during stable oscillation. As shown in Fig. 2.10, G_m is approximated as $-1/2R_p$ [2.19]. The transistor's current-noise spectral density of $4kT\gamma g_m$ in saturation (at Q-point V_{DS}) is then equated to $4kT\gamma/R_p$, and from [2.35] $\Gamma(\phi) = -sin(\phi)$. Therefore, S_{MOS} simplifies to:

$$S_{MOS} = \frac{1}{2\pi}\frac{4kT\gamma}{R_p}\int_0^{2\pi} sin^2(\phi)d\phi = \frac{2kT\gamma}{R_p}. \tag{2.47}$$

The phase-noise contribution of the MOS transistor's channel noise, for a differential circuit with $N = 2$, is calculated using eqns. 2.42 and 2.47 as:

$$L(\Delta\omega)_{MOS} = 10 \cdot log\left[\frac{1}{N}\left(\frac{R_p}{2P_{sig}}\right)\left(\frac{\omega_c}{Q\Delta\omega}\right)^2\frac{2KT\gamma}{R_p}\right], \tag{2.48}$$

$$\Rightarrow L(\Delta\omega)_{MOS} = 10 \cdot log\left[\left(\frac{2KT\gamma}{P_{sig}}\right)\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right].$$

The noise contribution S_{MOS} in eqn. 2.48 is calculated over an entire cycle with an average resistance equal to R_p. This is a significant approximation that assumes:

1. The effective noise spectral density of the time-varying transfer shown in Fig. 2.10 can be captured by an average resistance.
2. The transistors remain in saturation, and the impedance shunting the resonator is solely an outcome of transconductance.
3. The rise and fall transients that describe simultaneous conduction are lumped into the expression of an average resistance.

2.8.3 Tail current noise

As described in section 2.6.3, the phase-noise contribution of the tail-current source involves up-conversion of *1/f* noise and downconversion of noise at $2f_0$ with respect to the oscillator switching frequency, f_0. Calculating the ISF of the tail current source is non-trivial, and its phase-noise contribution is calculated here using the filtering approach described in Section 2.6.2. The switching cross-coupled transistors can be likened to a single-balanced Gilbert-cell mixer (with a single-ended load = R_p) that is driven by an input noise-current i_{in} at the tail node. The differential output voltage at IF arising from mixing pairs of f_0 & $2f_0$, and $2f_0$ & $3f_0$ is given by [2.16], [2.41][10]:

$$\begin{aligned} v_o &= \left[\frac{1}{\pi} i_{in} 2R_L - \frac{1}{3\pi} i_{in} 2R_L\right], \\ \frac{v_o}{2R_L} &= \left[\frac{2}{3\pi} i_{in}\right] \Rightarrow i_0 = \left[\frac{2}{3\pi} i_{in}\right]. \end{aligned} \tag{2.49}$$

The transfer function of the tail-current noise source ($i_n^2/\Delta f = 4kT\gamma g_{mT}$) through the switching core is given by eqn. 2.49. Therefore, the mean-square current-noise spectral density appearing at the output equals:

$$\frac{i_n^2}{\Delta f} = \frac{4}{9\pi^2} 4kT\gamma g_{mT}. \tag{2.50}$$

[10] Components at f_0 due to mixing of higher-order terms are not included. These are calculated and shown in [2.42].

Using eqn. 2.35, the spectral density of the mean-square voltage equals:

$$(i_n^2/\Delta f)\cdot|Z|^2=\left[\frac{4}{9\pi^2}i_n^2\cdot R_{pd}^2\left(\frac{\omega_0}{2Q\cdot\Delta\omega}\right)^2\right]. \tag{2.51}$$

In eqn. 2.51, R_{Pd} is the differential tank impedance at resonance and equals twice R_p. Like the assumption in eqn. 2.35, the mean-squared noise voltage contributes equally to amplitude- and phase-modulation sidebands. The phase noise is expressed as the ratio between the root-mean-squared noise and signal power contained in a 1-Hz bandwidth:

$$\begin{aligned}10^{L(\Delta\omega)}&=\left[\frac{2}{9\pi^2}\frac{i_n^2R_{pd}}{P_{sig}}\left(\frac{\omega_0}{2Q\cdot\Delta\omega}\right)^2\right]=\left[\frac{4}{9\pi^2}\frac{i_n^2R_p}{P_{sig}}\left(\frac{\omega_0}{2Q\cdot\Delta\omega}\right)^2\right],\\ L(\Delta\omega)&=10\cdot log\left[2kT\left(\alpha_T\frac{\gamma g_{m_T}R_p}{P_{sig}}\right)\left(\frac{\omega_0}{2Q\cdot\Delta\omega}\right)^2\right].\end{aligned} \tag{2.52}$$

Note from eqn. 2.52, that the mean-squared differential signal power equals the peak single-ended power. The value of $8/9\pi^2$ in eqn. 2.52 (denoted by α_T) equals 0.09, and explains the value of ~0.085 reported via simulation in [2.32]. The value α_T according to [2.32] is a function of the conduction angle of transistors M_1 and M_2 (assumed to be π in the above analysis, where the transistors are on for one-half of the period). It is a fitting parameter that is applicable when all transistors operate in saturation, where their noise may be approximated as $4kTg_m\gamma$. In the next section, the analysis is compared to simulation. It is shown that its applicability holds only for a relatively small range of oscillation amplitudes in low-power designs.

The phase noise in the $1/f^2$ region of the cross-coupled LC oscillator is obtained by combining eqns. 2.44, 2.48 and 2.52:

$$L(\Delta\omega)=10\cdot log\left[\frac{2kT}{P_{sig}}\left(1+\gamma+\frac{8}{9\pi^2}g_{mT}R_p\gamma\right)\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right]. \tag{2.53}$$

2.8.4 Studying the impact of gate-resistance noise

Fig. 2.12 shows that the voltage-noise source due to the gate resistance, r_g, of the cross-coupled transistors (M_2 in this case) sees a high impedance at resonance (akin to an open circuit) via the tank load and off transistor, M_1. Its phase-noise con-

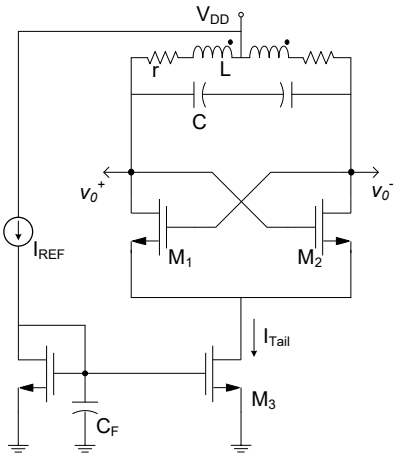

Fig. 2.13: Circuit schematics of the cross-coupled LC oscillator.

-tribution is therefore negligible in most cases.

Unlike transistors M_1 and M_2 (see Fig. 2.11), whose gate resistance noise-voltage source sees an obviating high impedance, the tail-current's gate resistance (transistor M_3) is terminated by a large capacitance, C_F (see Fig. 2.11) that filters out noise from the current-mirror diode, M_4, and current source feeding it. The AC ground created by C_F ensures that the entire noise voltage appears across the gate-source terminals and gets converted to a noise current through the transconductance of the tail current source, which increases significantly in high-power designs. The noise components of the gate resistance, r_g, in the vicinity $2f_0$ that down-convert to f_0 are written using eqn. 2.49 as:

$$\frac{i_n^2}{\Delta f} = \frac{4}{9\pi^2}\left(4KTr_g\right) \cdot g_{mT}^2 \,. \tag{2.54}$$

Using eqn. 2.35, the spectral density of the mean-square voltage equals:

$$(i_n^2/\Delta f) \cdot |Z|^2 = \left[\frac{4}{9\pi^2} i_n^2 \cdot R_{pd}^2 \left(\frac{\omega_0}{2Q \cdot \Delta\omega}\right)^2\right]. \tag{2.55}$$

The phase noise, similar to eqn. 2.50, is expressed as the ratio of the root-mean-square noise and signal powers contained in a 1-Hz bandwidth:

$$L(\Delta\omega) = 10 \cdot log\left[\left(2kT\frac{8}{9\pi^2}\frac{r_g R_p \cdot g_{mT}^2}{P_{sig}}\right)\left(\frac{\omega_0}{2Q \cdot \Delta\omega}\right)^2\right]. \tag{2.56}$$

The overall phase noise of a cross-coupled LC oscillator that results from thermal noise sources in the circuit is thus obtained by combining eqns. 2.53 and 2.56, and equals:

$$L(\Delta\omega) = 10 \cdot log\left[\frac{2KT}{P_{sig}}\left(1 + \gamma + \frac{8}{9\pi^2} g_{m_T} R_p\left(\gamma + r_g g_{mT}\right)\right)\left(\frac{\omega_c}{2Q\Delta\omega}\right)^2\right]. \quad (2.57)$$

It is worth mentioning again that eqn. 2.57 predicts the phase noise in the $1/f^2$ region, neglecting the effect of parasitic capacitance C_X (see Fig. 2.11) at the common-source node of the differential pair, and assumes a large output impedance of the tail current source. It also assumes that all transistors operate in saturation and load the tank negligibly, that noise is independent of channel-current variation, and that a linear relationship between channel current and input voltage (via g_m) characterizes the transistors' large-signal transfer characteristics.

2.8.5 Comparison of theory and simulation

The phase noise of the 8-GHz LC oscillator of Fig. 2.13 simulated at 3-MHz offset is plotted in Fig. 2.14. Figs. 2.14a and 2.14b show the phase noise of two oscillator designs targeting low and high power consumption, respectively. The oscillators are powered by a 1.2-V supply. The simulation uses inductors having a Q-factor of ~25 at 8 GHz from the TSMC 65-nm library developed for the back-end metallization option that includes a 3-um thick Cu layer[11].

For the high- and low-power designs, the differential tank inductance equal 0.96 nH and 147 pH, respectively. The aspect ratios of transistors M_1 and M_2 equals [1µm/60nm]×8_{fingers} and [2.5µm/60nm]×32_{fingers}, respectively, and aspect ratios of transistors M_3 and M_4 equal [3µm/120nm]×12_{fingers} and [3µm/120nm]×32_{fingers}, respectively. The aspect ratios are optimized for phase noise performance. The tail-transistor size affects phase noise considerably for high power consumption and is therefore optimized for maximum impedance in the common-mode path. The differential tank capacitance in the low-power design equals 400 fF, and equals 2.9 pF in the high-power design.

[11] The actual oscillator implemented in this work is in a metallization option that does not contain this thick-metal option (20% lower Q), as described in Section 1.2.

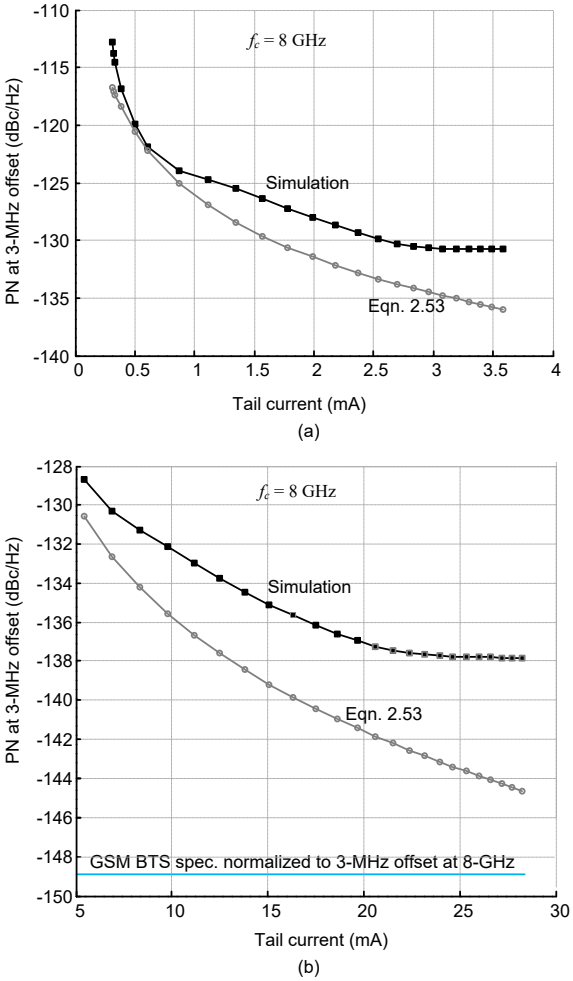

Fig. 2.14: Phase noise simulated at 3-MHz for the 8-GHz oscillator in Fig. 2.12 designed for (a) low power consumption, and (b) high power consumption.

The phase noise predicted by theory is plotted for comparison in Fig. 2.14. It is seen from Fig. 2.14a that as power consumption increases the deviation from theory increases. This is due to: 1) increased tank loading as the cross-coupled transistors enter triode, 2) a drop in the impedance of the tail-current source results in an increased noise contribution from the cross-coupled pair, and 3) increased noise contribution from the tail-current source. The discrepancy is further aggravated in

high-power designs, where differences between theory and simulation for low-phase noise oscillator designs can be as high as 6-7 dB.

2.9 The low-noise design challenge

The GSM-900 BTS specification at 800 kHz (-147 dBc/Hz, see Table 1.1) when normalized to an 8-GHz carrier and 3-MHz offset is shown in Fig 2.14b. The challenge for a base-station design is visible, as a 10-dB difference exists for an oscillator operating at 20-mA bias (~24 mW). The simplified simulation does not take into account layout parasitic resistances that significantly reduce the tank-Q for diminishing inductor sizes.

When the oscillator is designed for an unrestrained power budget (e.g., base station applications) the mitigation of transistor noise due to high tail-current impedance reduces significantly, while the channel noise and gate noise contribution of the tail-current source itself increases due to its increased g_m. As a consequence, the tail-current source is a major limiting factor when scaling the cross-coupled oscillator for high-power operation (on the 100-mV order). In the oscillator design presented in Chapter 5 of this thesis [2.38], hard-limiting the output waveform creates phase insensitivity, which permits the elimination of the tail-current source without the penalty in increased noise contribution from the cross-coupled transistors as predicted for the LC VCO of Fig. 2.13. Increased gate-drive generated in the oscillator using coupled transformers reduces rise and fall times of transients, which minimizes phase-noise contribution of the core transistors. Hard limiting leads to a reduction in the phase-noise contribution of the resonator as well, and results in extremely low phase noise (within 1.5 dB of the BTS specification, for a moderate, but sufficient, tuning range of 10%) at a phase-noise efficiency comparable to low-power oscillator designs.

2.10 Summary

This chapter summarizes some of the background knowledge and literature survey leading up to the research presented in this thesis. Basic principles of frequency modulation (FM), analysis of demodulator noise, and a literature survey of FM

demodulators are presented in the first part of the chapter. The theory behind direct-differentiation, filter-domain and time-domain FM demodulators are described, along with bandwidth limitations of conventional demodulation methods. This lays the platform for the FM demodulator based on injection-locking developed in this thesis (described in chapters 3 and 4) for power-efficient demodulation of wideband FM signals.

This is followed by a summary of oscillator theory, that includes ring and LC based oscillators, their design and frequency tuning. Oscillator phase noise models, that include Leeson's model, filter-based noise shaping, phasor based analysis, and the linear time-varying model are reviewed in depth. The noise mechanisms in LC oscillators are analytically surveyed, and compared to simulation. Phase-noise limitations in on-chip oscillator implementations are described, and introductory aspects behind the principle of phase desensitization proposed in this thesis for low-noise oscillator design (chapter 6) have been presented to the reader.

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Chapter 3 – Injection-locked FM demodulation

This chapter describes the design and operation of the FM demodulator and its sub-blocks developed for wideband operation between 2-10 GHz at IF. The transmission of an FM signal through an injection-locked oscillator and division of FM deviation are explained analytically and verified via simulations that show translation of Bessel function coefficients at the output of the locked-in oscillator. Expressions for time instantaneous I/Q signals and the demodulator's output characteristic are developed that verify wideband operation.

3.1 Demodulator overview

Injection-locked ring oscillators (ILOs) perform frequency division, and multi-phase signal injection is known to widen the locking range of these dividers [3.1]. Four-stage oscillators requiring anti-phase signals fit seamlessly into differential circuit chains, and inductorless implementations are widely used for quadrature-phased frequency division of an LO signal. These circuits are inherently compact in die area, require a lower input drive compared to dynamic CMOS frequency dividers (e.g., [3.2]), and can operate across nearly two octaves in the low-GHz region [3.3], [3.4]. Since the output discharges entirely during each cycle, the oscillator doesn't retain information from the previous cycle and is memoryless. This allows the oscillator to lock to a wide range of input frequencies (compared to tuned oscillators [3.5]), and track the modulation of a wideband FM signal with ease. The remarkable ability of these circuits to lock to FM signals and divide the frequency is the subject of this study. It has remained an unexplored circuit technique for wideband demodulation.

It is important to note that while the locked-in oscillator reduces FM deviation by virtue of division, the modulation frequency remains unaltered. This effect was observed by Beers in 1944 [3.6], and is studied in detail in this chapter. The operating bandwidth is therefore reduced by the division factor (assumed to be 4 here), which eases the bandwidth/power consumption trade-off in the stages that follow. Time-instantaneous quadrature signals produced by the locked-in ring can be

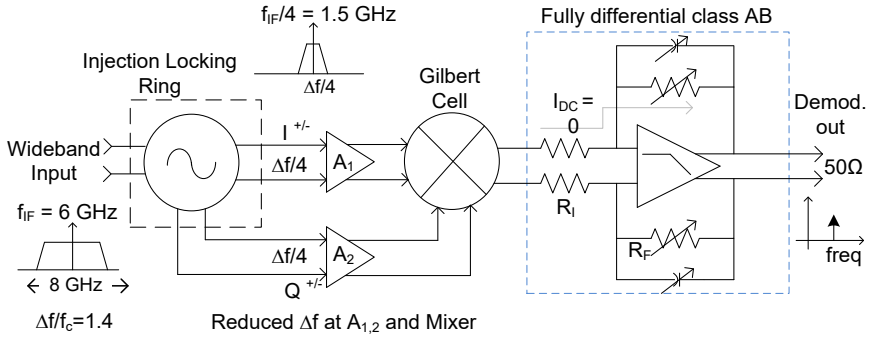

Fig. 3.1: Block diagram of the injection-locked, wideband IF demodulator developed in this work.

utilized for FM detection, thereby avoiding the need for wideband, true-time delays, and complex frequency plans for quadrature-phase generation. Other benefits of this approach to demodulation are: 1) data-rate independent power consumption, 2) wideband operation, 3) insensitivity to noise and additive amplitude modulation of the input RF, 4) a requirement for low distortion is not imposed on the IF amplifier, and 5) operation of the ring-oscillator at $1/4^{th}$ the intermediate frequency enables a higher IF and a lower fractional bandwidth. The minimum signal amplitude required for injection locking, and its susceptibility to in-band interferers are alleviated by applying the technique at IF rather than RF, because potential blockers can be filtered by the preceding stages. A wideband IF pre-amplifier is required in the chain (Fig. 1a), which is not implemented in the 65-nm CMOS prototype demodulator developed in this work.

Fig. 3.1 shows a block diagram of the proposed IF demodulator for the heterodyne receiver of Fig. 1.1b. Quadrature outputs from the injection-locked input stage are interfaced through buffers $A_{1,2}$ to a Gilbert mixer. The power consumption of the interface buffers and the mixer are reduced considerably by the rail-to-rail output provided by the ring oscillator, and reduction of the signal bandwidth by FM division (illustrated in Fig. 3.1). The low-frequency demodulated output from the mixer is buffered for 50-Ω measurement using a differential class-AB operational amplifier developed in this thesis [3.7] that is configured in shunt feedback.

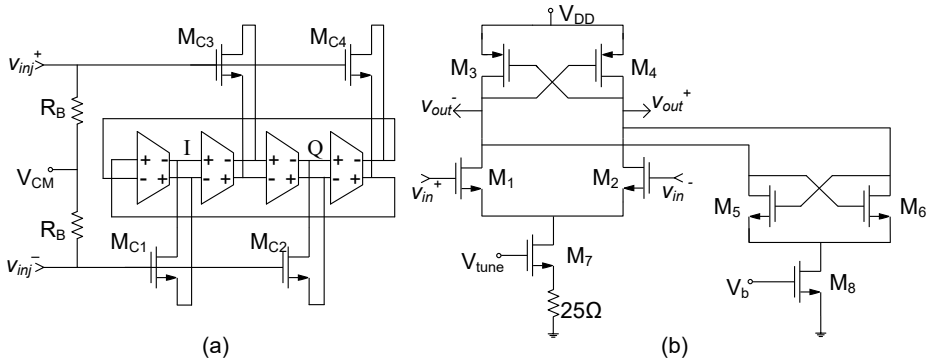

Fig. 3.2: **(a) Injection-locked, four-stage ring oscillator, (b) implementation of each stage.**

3.2 Locked-in oscillator design and operation

The four-stage ring oscillator shown in Fig. 3.2a constitutes the input stage. It is differentially injection locked to the wideband input signal through gain stages $M_{C1\text{-}4}$. Each stage consists of a differential pair loaded by a cross-coupled PMOS pair (shown in Fig. 3.2b), which provides local positive feedback to ensure that the outputs charge and discharge rapidly. Cross-coupled transistors $M_{5,6}$ (controlled by V_b) provide additional regenerative gain in case of start-up failure. A frequency tuning range from 0.8–1.9 GHz is implemented via a variable resistor at the tail node, where M_7 is operated in triode and controlled by V_{tune}. The oscillator stages draw between 350 and 500 μA, depending on V_{tune}. The DC voltage V_{CM} (Fig. 3.2a) ensures that transistors $M_{C1\text{-}4}$ operate in saturation, and provide sufficient gain to prevent the oscillator from falling out of lock and distorting the demodulated waveform. Its optimal value cannot be determined *a priori* and is therefore obtained iteratively. All measurements have been performed with V_{CM} and V_b set to 0.6 V and 0 V, respectively (V_{DD} = 1.2 V).

Fig. 3.3 shows the large-signal operation of one of the stages, and the associated voltage and current waveforms. The triode resistance of M_7 is shown as '$\underline{R_{ss}}$' Fig. 3.2b. Consider node 'x' and voltage v_x in Fig. 3.3a. The impulse-like discharge current sunk by M_1 is sourced by transistor M_3, after which it cuts-off (annotated in Fig. 3.3c as '$i_{M3\text{-}1}$'). The peak output swing appears across the drain-source of M_{C1}, which operates in saturation conducting a DC current (I_Q) sourced by M_4 and sunk

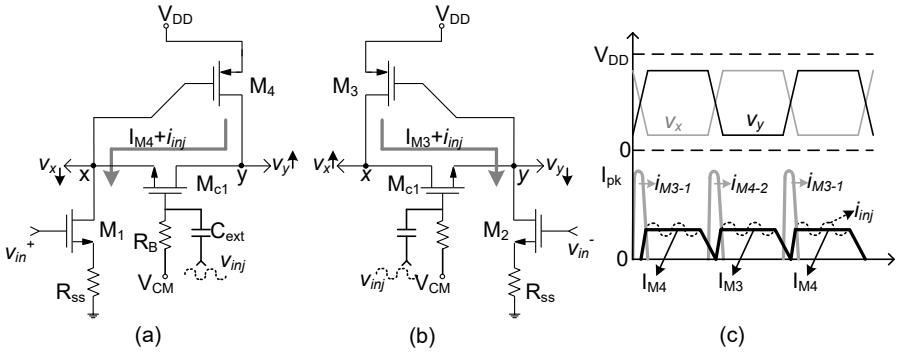

Fig. 3.3: Single-stage circuit during large signal operation. (a) M_3 and M_2 are cut-off, and current flows from node y to *x*, (b) M_1 and M_4 are cut-off, and current flows from node *x* to *y*, (c) an illustration showing current waveforms during large-signal operation.

by M_1, noted as 'I_{M4}' in Figs. 3.3a & 3.3c. Voltage V_{CM} biasing the gate of M_{C1} determines I_Q, and the Q-point transconductance of M_{C1}. In the second half of the cycle, node 'y' is discharged via M_2 ('$i_{M4\text{-}2}$' in Fig.3.3c), resulting in a swap of drain and source terminals for M_{C1}. Transistor M_{C1} conducts I_Q sourced by M_3 (now biased on) and sunk by M_2 – noted as 'I_{M3}' in Figs. 3.3b & 3.3c. The drain-source overdrive (of $M_{1\text{-}4}$) required to conduct the steady-state value of I_Q determines the peak-to-peak swing at nodes 'x' and 'y', i.e., v_x and v_y.

When an AC signal rides the bias voltage at the gate of the coupling transistors (e.g., M_{C1}), it drives a signal current into the oscillator loop, which drops across triode impedances loading its drain/source terminals (e.g., nodes 'x' and 'y'). The resulting envelope (see Fig. 3.4) on the output triggers the charging and discharging of the subsequent stage, and thereby draws the oscillator into lock. The envelope signal is eliminated by hard-limiting interface buffers. Fig. 3.4 shows the simulated time-domain response of the oscillator (f_0 = 1.88 GHz, V_{CM} = 0.6 V) when 100-mV_{pp} locking signals with static frequencies of 7 and 9 GHz, respectively, are applied at a time of 100 ns. Due to the absence of memory in the loop, the oscillator locks to the frequency tones at wide offsets from its free-running frequency almost instantaneously (2 cycles in this example), suggesting the ability to lock binary FSK at rates in the gigabit-per-second range. The binary FSK modulation rate is typically orders of magnitude below the carrier (f_c), and does not affect the tracking ability of

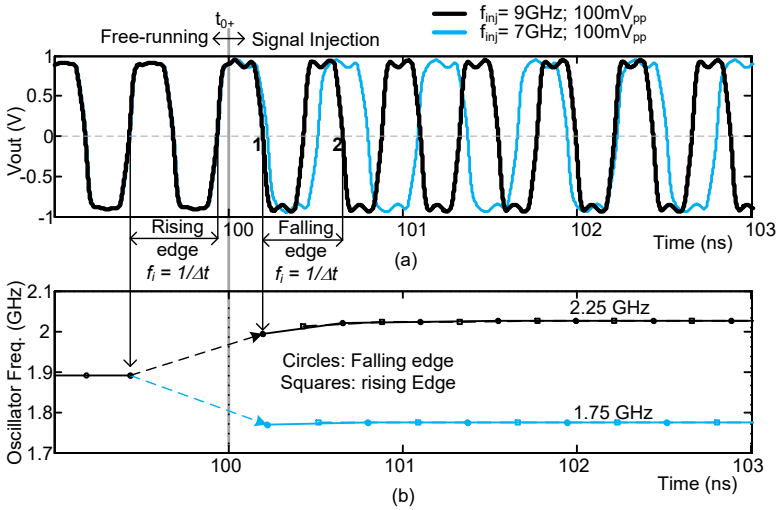

Fig. 3.4: Simulated locking response for f_{inj} of 9 and 7 GHz applied at 100 ns (a) time-domain simulation of the output voltage, and (b) instantaneous frequency vs. time.

the locked-in ring oscillator. Simulations suggest that the demodulator detects FM coherently when the carrier is typically one order of magnitude higher in frequency than the modulating signal. This limits the maximum data-rate to ~400 Mbps at the 2 GHz band edge, and ~2 Gbit/s between 8 and 10 GHz.

3.2.1 Transformation of the FM Modulation Index

It was shown in Section 2.1 that Bessel function coefficients (BFCs) fingerprint the signal spectrum at offsets from the carrier frequency for a given FM modulation index. These are evaluated via simulation of the locked-in oscillator to verify the FM transmission characteristics predicted by the analytical form of the expected output. A typical FM signal modulated by a single tone $cos\ \omega_m t$, is given by eqn. 2.5:

$$v_{FM}(t) = X_o \cos[3.\omega_C t + \beta \sin(\omega_m t)]\,. \tag{3.1}$$

From eqn. 2.4, the ratio $\Delta\omega/\omega_c$ is the deviation ratio – D_r, and twice its value is the signal's fractional bandwidth. When an FM signal is passed through a factor 'n' frequency divider, the resulting division of FM deviation and the carrier frequency is obtained by dividing $V_{FM}(t)$ from eqn. 3.1 by 'n':

$$v_o(t) = X_c \cos\left[\frac{\omega_C}{n} t + \frac{\beta}{n}\sin(\omega_m t)\right], \tag{3.2}$$

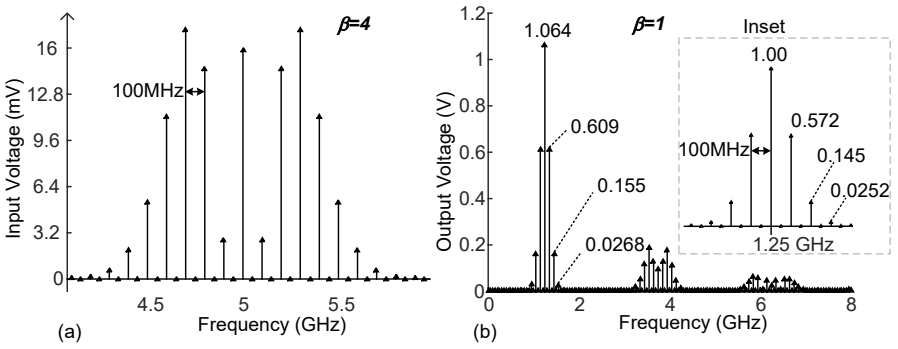

Fig. 3.5: Transformation of modulation index. (a) Input 80mV$_{pp}$ FM signal with f_c= 5 GHz, f_m= 100 MHz and β=4, and (b) differential output of the locked-in oscillator. FM deviation is divided by 4, and the input β of 4 is translated to 1.

where X_c is the signal amplitude at the oscillator's output. A key observation from eqn. 3.2 is that the division of FM deviation is brought about by the transformation of the modulation index (now β/n), and the retention of the modulating signal. This is confirmed via Spectre-RF^{TM} simulation of the locked-in oscillator. Fig. 3.5 shows a simulation example of division of FM deviation. The 80 mV$_{pp}$ input FM signal applied to the oscillator shown in Fig. 3.5a has f_c = 5 GHz, f_m = 100 MHz, and β = 4. The BFCs for modulation indices of 1, 0.25 and 4 are listed in Table 4.1 (Chapter 4, Section 4.3), along with their ratio with the carrier-specific coefficient, J_0. The spectrum of the differential voltage at the output of the locked-in oscillator is shown in Fig. 3.5b, and the inset zooms in on the X-axis around the scaled-down carrier of 1.25 GHz. It is seen that the offset tones normalized to the carrier tone in Fig. 3.5b agree well with the theoretical values listen in Table 4.1. The harmonics seen in Fig. 3.5b are characteristic of FM distortion, where the deviation around harmonics of the carrier increases by a factor equal to the harmonic in question. Experimental results that validate theory and simulation are presented in Chapter 4.

3.2.2 Quadrature Signals and FM Demodulation

Generally, envelope detection of the derivative of an FM signal accomplishes FM demodulation [3.8]. Both filter-domain (e.g, [3.9], [3.10]), and delay-line implementations (e.g., [3.11], [3.12], [3.13]) comprised of differentiators, are band-

limited to a narrow window in frequency where the phase gradient ($d\phi/df$) of the central passive network remains constant. For wideband operation, the realization of a controllable pure time delay entails complexity that often results in relatively high power consumption and large chip area [3.14], [3.15], [3.16]. It will be shown that the quadrature-phased outputs inherent to the locked-in ring oscillator simplify demodulation by circumventing the need for an auxiliary wideband true-time delay. In this section, a simple analytical prediction of the locked-in oscillator's quadrature-path delay is verified via simulation. It is then used to derive the demodulator's wideband characteristic. Under perfect lock, the Q and I signals (see Fig. 3.2a) are expected to be shifted in time by one-fourth of the instantaneous time period. For the FM input signal represented by eqn. 3.1 and the output of the locked-in oscillator represented by eqn. 3.2, the I and Q signals may be written as:

$$v_{FM_I}(t) = X_c \cos\left[\frac{\omega_C}{n}t + \frac{\beta}{n}\sin(\omega_m t)\right] = X_c \cos[\omega_c' t + \beta' \sin(\omega_m t)], \tag{3.3}$$

$$v_{FM_Q}(t) = X_c cos\left[\omega_c'\left(t - \tau_d(t)\right) + \beta' \sin\{\omega_m\left(t - \tau_d(t)\right)\}\right], \tag{3.4}$$

where ω_c', and β' are the scaled down carrier frequency and modulation index, respectively. The delay between the two branches, τ_d, determines the demodulator characteristic, and is calculated using $\omega(t)$ defined by eqn. 2.2. It can be expressed as the sum of a fixed delay at f_c, and a time-varying function of the modulating signal:

$$\begin{aligned} \tau_d(t) &= \frac{2\pi}{4\omega(t)} = \frac{1}{4}\left[\frac{1}{\{\beta' f_m \cos(\omega_m t) + f_c'\}}\right], \\ \tau_d(t) &= \frac{1}{4f_c'}\left[1 + \frac{-\cos(\omega_m t)}{\{\cos(\omega_m t) + 1/D_r\}}\right]. \end{aligned} \tag{3.5}$$

The ring oscillator's output interface consists of a series of hard-limiting inverters (Fig. 3.1) switching between 0 and V_{DD}. In the midst of harmonics that comprise the square wave, the frequency modulation is 'sampled' at the zero crossings of the hard-limited FM signal. Fig. 3.6 shows a Spectre-RF™ simulation of the voltages on the Q and I branches of the locked oscillator. The input signal has f_c = 5 GHz, f_m = 100 MHz, β = 25, Δf = 2.5 GHz, and fractional bandwidth $\Delta f/f_c$ equals 1. The delay

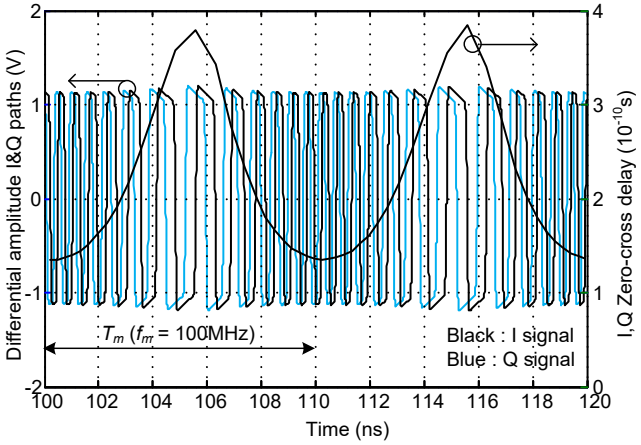

Fig. 3.6: Simulated transient I and Q signals and the delay between their zero-crossings for a fractional bandwidth $\Delta f/f_c = 1$, f_c =5 GHz, f_m =100 MHz, β =25.

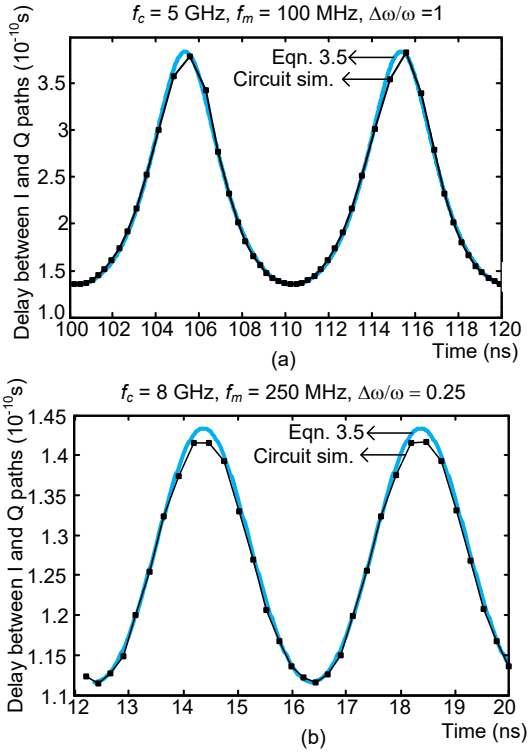

Fig. 3.7: Simulated delay between the Q and I signal paths recorded at zero-crossings, compared to the delay predicted by eqn. 3.6 for (a) f_c = 5 GHz, f_m = 100 MHz, and β = 25, and (b) f_c = 8 GHz, f_m = 250 MHz, and FM deviation of 1 GHz (β = 4).

between the zero-crossings of the Q and I signals is also plotted on Fig. 3.6 against the right-hand Y-ordinate. The delay predicted by eqn. 3.5 compares well with simulation, as seen from their comparison in Fig. 3.7a. A superposition of theoretical and simulated delay for a lower modulation index ($\beta = 4$) where f_c = 8 GHz, f_m = 250 MHz and $\Delta f/f_c$ equals 0.25 is shown in Fig. 3.7b. A theoretical minimum ratio of ω_c/ω_m of 8 is reached when applying Shannon's sampling limit to the scaling down of f_c by a factor of 4. The Gilbert mixer driven by large signals at either port behaves like a phase detector. Its low-pass-filtered output current that describes the FM demodulator's characteristic is proportional to the difference between the phases of eqns. 3.3 and 3.4, and may be expressed as [3.8], [3.17]:

$$i_O(t)\ \alpha\ [\omega_c' \tau_d(t) + \beta'\{\sin(\omega_m t) - \sin(\omega_m(t - \tau_d(t)))\}]. \tag{3.6}$$

Evaluating eqn. 3.6 for the limit $\tau_d \to 0$ (assuming $\omega_c >> \omega_m$ and that τ_d equals $\pi/2\omega_c$) and using the simplification used in [3.18] for the evaluation of delay-line demodulators, results in an approximation that sheds light on the recovery of the modulating signal:

$$\lim_{\tau_d \to 0} i_O(t) = \beta' \tau_d \frac{\left[\sin(\omega_m t) - sin\left(\omega_m (t - \tau_d)\right)\right]}{\tau_d},$$
$$\lim_{\tau_d \to 0} i_O(t) = \beta' \tau_d \frac{d(\sin(\omega_m t))}{dt} = \frac{\pi}{2} D_r \cos(\omega_m t). \tag{3.7}$$

Eqn. 3.7 predicts undistorted detection of the modulating signal. However,
Fourier coefficients of eqn. 3.6 depend on ω_m and the deviation ratio, D_r. The normalized form of $i_0(t)$ from eqn. 3.6 is simulated using Matlab™ to evaluate the output characteristic and baseband distortion assuming a constant of proportionality equal to one. The delay, τ_d, is described by eqn. 3.5. Harmonic distortion components (HD_2 – HD_5) are plotted in Fig. 3.8 for a 5-GHz carrier modulated at 10 and 250 MHz. Baseband distortion increases with D_r, resulting in stringent filtering requirements.

However, in the case of FSK demodulation, the data can be reconstructed easily via hard-limiting inverter stages. The demodulator's characteristic obtained from Spectre™ simulation of the entire circuit (i.e., components of Fig. 3.1) is shown in

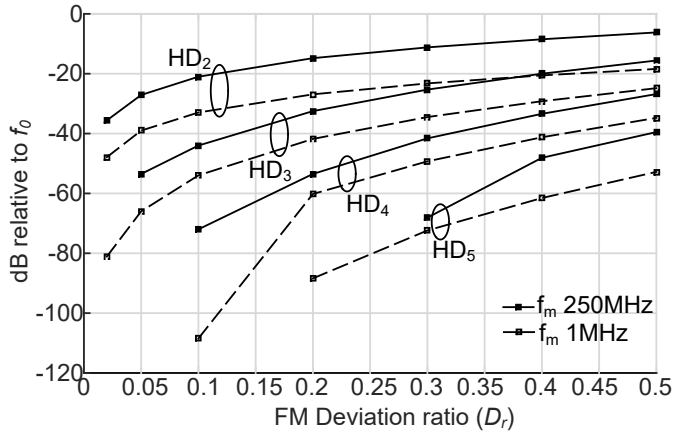

Fig. 3.8: Harmonic distortion of eqn. 3.6 versus deviation ratio for f_m equal to 1 and 250 MHz, and f_c equal to 5 GHz.

Fig. 3.9. The normalized fundamental component of the mixer's output current is plotted against D_r, and compared to the normalized theoretical prediction from eqn. 3.6. A good correlation is seen between theory and simulation, while the demodulator's wideband capabilities are clearly visible, as the mixer's output current varies almost linearly even as the fractional bandwidth approaches unity. Characterization data for the demodulator prototyped in 65-nm CMOS is presented in Chapter 4.

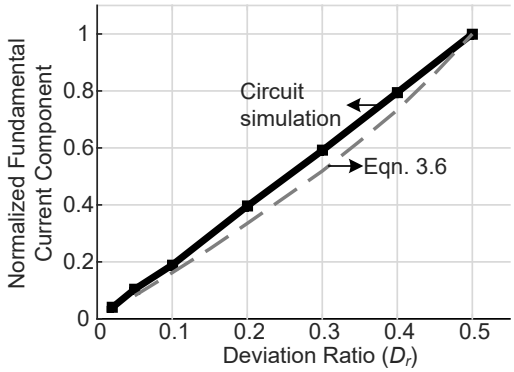

Fig. 3.9: Normalized plot of the mixer's fundamental output current component vs. deviation ratio, for f_c = 5 GHz and f_m = 10 MHz, compared to the characteristic predicted by eqn. 3.6.

3.3 A comparative view on demodulator non-linearity

FM discrimination is a non-linear process. In ideal delay-line demodulators the modulation is recovered in the form of signal phase, which leads to odd harmonics as shown by Gerrits in [3.18]. The third harmonic distortion (HD_3) can be as high as -18dB for a deviation ratio of 0.5, and this does not include any non-ideality in the magnitude and phase response of a practical filter. It is further shown in [3.18] that an offset in the transmit and demodulator center frequencies in such a system increases even-order distortion. This can be as high as a second-harmonic distortion component (HD_2) of -7 dB, and HD_3 of -21 dB for a deviation ratio of 0.25.

A more realistic derivation for transfer characteristic is presented in the widely used classical demodulator described by Bilotti in [3.19] and uses a 90-degree phase shift filter. This demodulator is implemented in [3.20] for wideband demodulation at 1 Gbps at IF. The transfer characteristic of the demodulator using a second-order LC phase-shift filter (with a selectivity Q and 90-degree phase shift at the carrier frequency) derived in [3.19] is subject to a narrowband approximation of phase and magnitude response. The result shows a characteristic independent of modulation rate and carrier frequency. The normalized output current varies as function of the frequency offset according to the relation:

$$I_0 = \frac{2a}{1+a^2}, where\ a = 2QD_r. \tag{3.8}$$

Bilotti in [3.19] shows excellent correlation between measurement and theory for variations in 'a' from -4 to +4. The symmetric transfer function supplies odd harmonics. For a best case example, a filter Q-factor of 10 whose response lies on the borderline acceptance of approximations leading to eqn. 3.8 is considered. The harmonic distortion components at the demodulator's output for sinusoidal modulation are calculated using Matlab™ and listed below in Table 3.1.

The wideband limitation of this traditional demodulator can be gauged by the increased distortion. It is important to note that the demodulator distortion obtained from eqn. 3.6 captures the exact cycle-to-cycle variation of the delay, τ_d, as function of modulation rate and carrier frequency, and is not subject to approximation. The

Table 3.1: HD components of an LC phase-shift demodulator (eqn. 3.8)

D_r	a	HD_3 [dB]	HD_5 [dB]	HD_7 [dB]	HD_9 [dB]	THD [dB]
0.05	[-1,1]	-16	-31	-46		-13.95
0.10	[-2,2]	-8	-16	-26	-33	-4.03

Table 3.2: HD components of the locked-in demod. at 250MHz (Fig.3.8/eqn 3.6)

Dr	THD
0.25	-12.5
0.4	-6.5
0.5	-4.5

THD of the injection-locked demodulator for the more distorted 250-MHz data-rate case shown in Fig. 3.8 is listed table 3.2. When compared to the LC phase-shift based demodulator, the presented injection-locked demodulator shows a times-5 increment on the operating deviation ratio (and bandwidth) for the same distortion when compared to a scenario where the phase-shift demodulator marginally enters its non-linear regime; i.e., where $a \in [-2,2]$. More importantly, in a practical wideband RF/IF scenario, when compared to the phase-shift demodulator operation in its linear region described within the bounds $a \in [-1,1]$, the FM deviation covered by the injection locking prototype, for the same distortion, is also 5-times more (see D_r of 0.05 vs. 0.25), with a THD of -13 dB.

In terms of distortion, the performance of the locked-in demodulator over a wide bandwidth is as good as the LC phase-shift demodulator's performance over a narrow bandwidth. It is however true that distortion of the locked-in demodulator is lower at lower FM bandwidths, which is the case with any demodulator. For FSK demodulators the data can easily be reconstructed via hard limiting through inverter stages, and may therefore not be a critical problem to address.

3.4 Folded Gilbert mixer and interface buffers

Mixers operating from low supply voltages encounter headroom limitations, and the tail current source is often sacrificed at the expense of bias regulation and common-

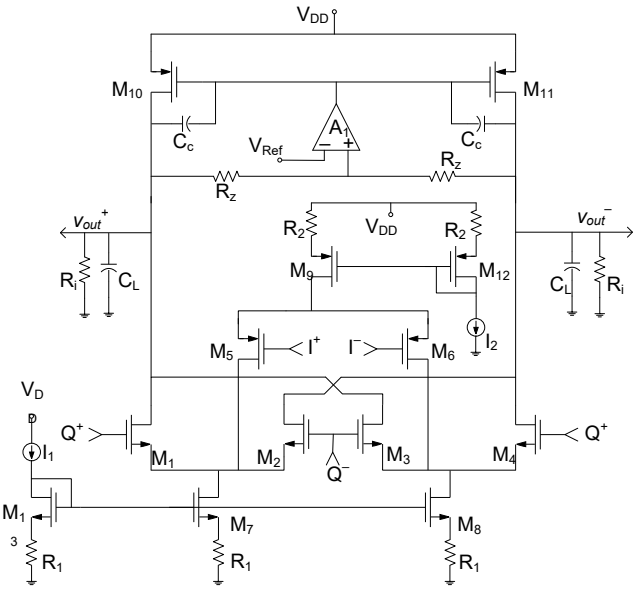

Fig. 3.10: The folded CMOS Gilbert mixer.

mode performance. The folded implementation of the 4-quadrant Gilbert mixer (shown in Fig. 3.10) uses complimentary transistors at its ports that allow accurate bias regulation, while the fully-balanced implementation minimizes feedthrough. The switching quad consists of NMOS transistors $M_{1\text{-}4}$, while PMOS transistors $M_{5,6}$ form the RF port. The PMOS device widths are twice that of the NMOS quad to ensure equal input loading. The injection-locked stage provides a rail-to-rail swing that allows the mixer to be designed for low power consumption. Current source I_2 biases transistors $M_{5,6}$, and the DC current difference between I_1 and I_2 is equally distributed between transistors $M_{1\text{-}4}$ of the switching quad. This allows accurate bias control to tailor the current in the RF and quad transistors for large-signal drive at either port, where it operates as a phase detector [3.21]. Measurements are made with I_1 varied between 125 and 600 μA, while maintaining 25 μA in each of transistors $M_{1\text{-}4}$. The simulated common-mode suppression from 0.5 to 2.5 GHz (since the 2-10 GHz input is divided by four) varies from 40-50 dB at either port. The mixer conversion gain is limited by the output impedance of tail current sources $M_{7,8,9}$, which is improved using 75-Ω degeneration resistance at each source node.

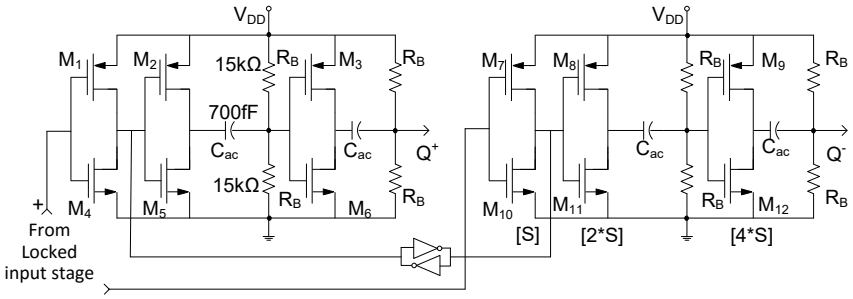

Fig. 3.11: Interface amplifiers.

The DC bias voltage at the output is set using common-mode feedback (CMFB). The CMFB amplifier is a standard NMOS folded-cascode amplifier that consumes 30 μA. The compensation capacitance (C_c) stabilizes the CMFB loop, while the minimum current to ensure a stable CMFB loop is 25 μA in each of transistors $M_{1\text{-}4}$.Interface buffers $A_{1,2}$ (Fig. 3.1) are shown in Fig. 3.11. They consist of a 3-inverter cascade. Cross-coupling inverters between the paths preserve the desired 180^o phase difference. The output DC is set to mid-supply using a resistive divider, and the inter-stage coupling network has a 40-MHz high-pass cut-off frequency that does not attenuate the propagating signal.

3.5 Summary

In this chapter the design and operation of the injection-locked, wideband demodulator and its circuit blocks were described. Analysis of Bessel-function coefficients establishes transmission characteristics of an FM signal through an injection locked oscillator. Division of FM deviation is verified via simulations, confirming the theory developed in this chapter. Expressions for time instantaneous I/Q-phases and the demodulator's output characteristic were developed that verify wideband operation. Extensive experimental characterization of the wideband demodulator prototyped in 65-nm CMOS is presented in the next chapter.

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Chapter 4 – Experimental characterization of the FM demodulator

Extensive laboratory-measurements characterizing the IF demodulator prototyped in 65-nm CMOS are detailed in this chapter. Stand-alone characterization of the four-stage ring oscillator and its response to external noise and FM, along are also described and discussed. The chapter ends with a summary of the work and conclusions drawn from it.

4.1 Demodulator characterization

A micrograph of the 624×277-μm^2 demodulator prototype (core area) implemented in 65-nm CMOS is shown in Fig. 4.1a. The chip is mounted on a custom test board (PCB) for measurement. All bias nodes and the output are wire-bonded to the PCB, while the RF input is probed on-die. Fig. 4.1b shows a micrograph of the ring oscillator characterized stand-alone.

Measured spectra of the oscillator at band edges of 900 MHz (-13.4 dBm output) and 1.8 GHz (-14.8 dBm output) are shown in Fig. 4.2. The ring oscillator has a free-running tuning range of 67% centered at 1.35 GHz.

The 2-10 GHz input bandwidth has been measured in sub-bands of 1 GHz (see setup in Fig. 4.3a). National Instruments arbitrary-waveform generator cards synthesize

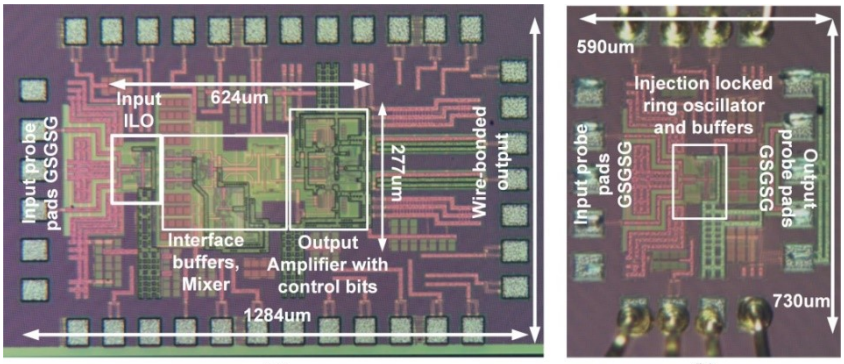


Fig. 4.1: 65nm CMOS chip micrograph of: (a) the IF demodulator with 624×277 μm^2 core area, and (b) the stand-alone injection-locking oscillator.

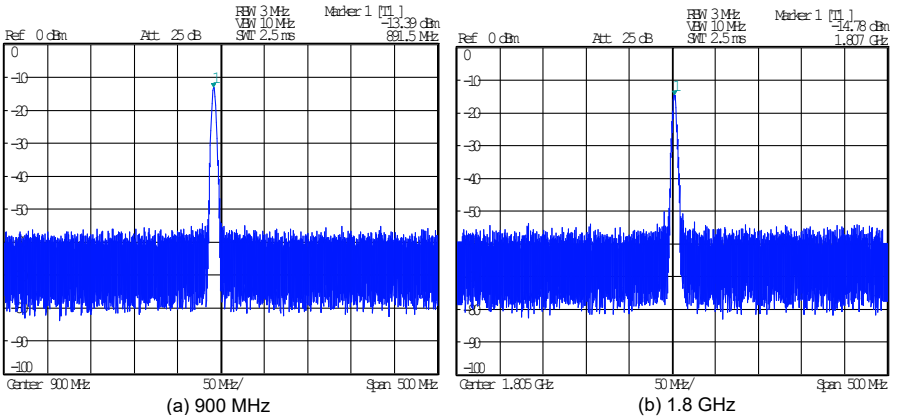


Fig. 4.2: Frequency spectra of the free-running oscillators at band edges (a) 900MHz and (b) 1.8 GHz. The tuning range is 900 MHz centered at 1.35 GHz (i.e., 66.7%).

linearly-modulated analog FM signals of 1 GHz bandwidth that drive (off-chip) up-conversion I/Q modulators to produce a wideband signal at the desired f_c. Programmable DC-offset correction and I/Q-phase correction minimizes carrier feedthrough and power in the image band, respectively. The digital modulation frequency range of the AWG is 200 kbps to 2 Mbps.

The measurement set-up shown in Fig. 4.3b combines noise and the input signal. Attenuators in both signal paths provide gain control, and a bandpass filter sets the noise bandwidth to 4.34-6.75 GHz (insertion loss <3 dB). Signal and noise power is measured at reference plane 'Y' (i.e., the probe head) using the HP-E4419A power meter and calibrated sensor head.

A 1-GHz bandwidth analog FM signal applied to the demodulator input is divided down by a factor of 4 to 250 MHz. For example, the 4-5 GHz bandwidth input signal of Fig. 4.4a is reduced to 1-1.25 GHz at the output of the locked-in oscillator (Fig. 4.4b). Fig. 4.4b shows the spectrum over a frequency range wide enough to include FM harmonics. The suppression of harmonics is better than 20 dB, which indicates that the oscillator is operating within its locking range. As seen from the measured output on Fig. 4.4b, the bandwidths of FM harmonics scale with the harmonic in question (as predicted in Section 3.2.1).

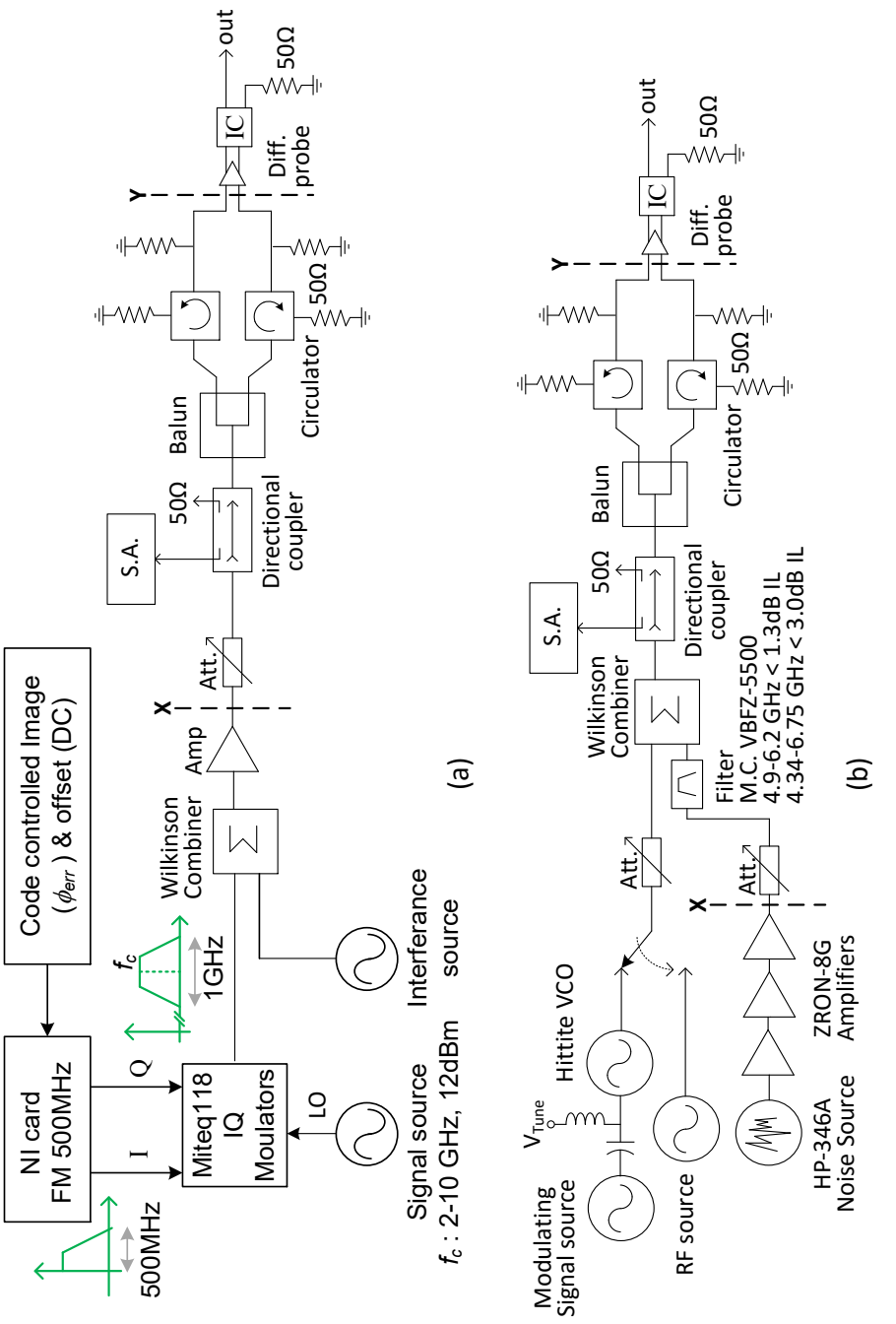
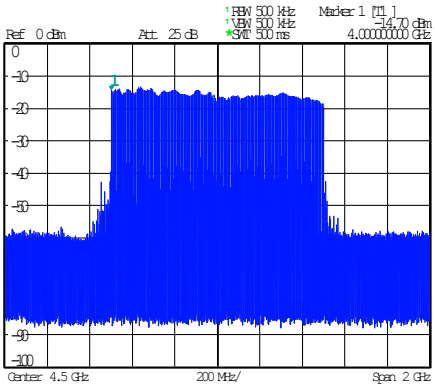
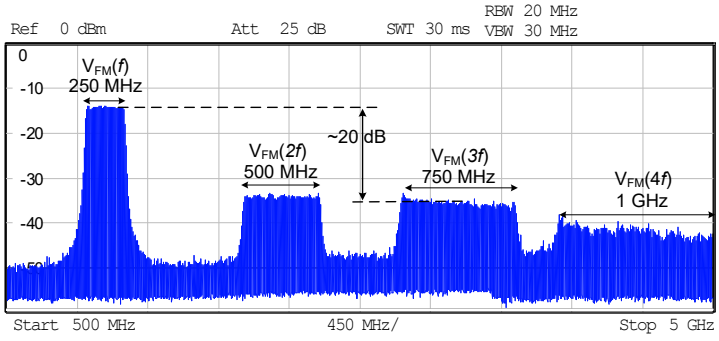


Fig. 4.3: Block diagram of (a) the wideband FM source set-up, and (b) set-up for injection locking and noise analysis.



(a) Wide-band input 4 – 5GHz (Mid-band)



(b) S.E. Injection-locked stage output divided by 4 to 1 – 1.25GHz

Fig. 4.4: Division of FM deviation. (a) 4–5 GHz bandwidth input FM, (b) Input bandwidth is divided down by a factor of 4 (1.00–1.25 GHz).

The measured division of FM deviation and translation of modulation index predicted by theory and simulation are compared in Figs. 4.5 & 4.6. The FM input is generated by modulating a wideband VCO [Hittite HMC586LC4B] using a laboratory signal source as shown in Fig. 4.3b. The 4-8 GHz VCO has a near-constant sensitivity of ~0.4 GHz/V between 4.5 to 6 GHz. Figs. 4.5a shows the measured input waveform (simulated in Fig. 3.5) for a f_c = 5-GHz, f_m = 100 MHz and β=4. Fig. 4.5b shows the spectrum of the fundamental FM output. The modulation index and bandwidth scale by a factor of 4 as predicted by theory. The experiment was repeated with a distorted input generated using overdriven back-to-back ZRON-8G amps. The unaltered output confirms a low distortion requirement is not imposed on the IF amplifier.

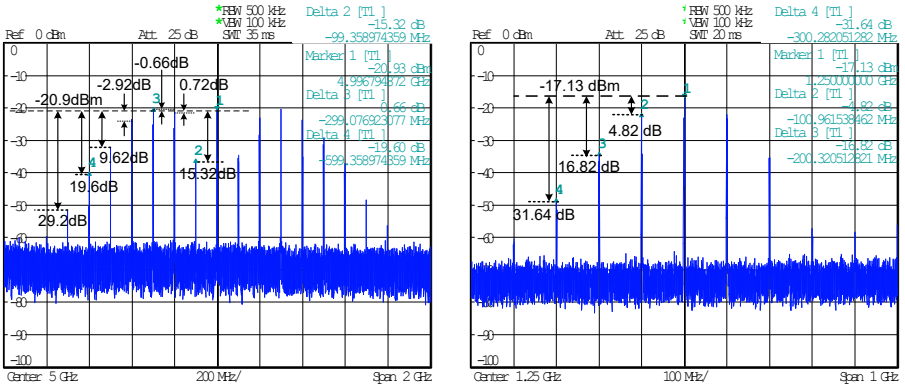


Fig. 4.5: Measured verification of theory and simulation predicting scaling of modulation index (a) Spectrum of the input signal used for simulation in Fig. 3.5, generated and applied to the oscillator f_c = 5GHz, f_m = 100MHz, β = 4. (b) BFC scaling at the divided fundamental output having β = 1 confirms theory.

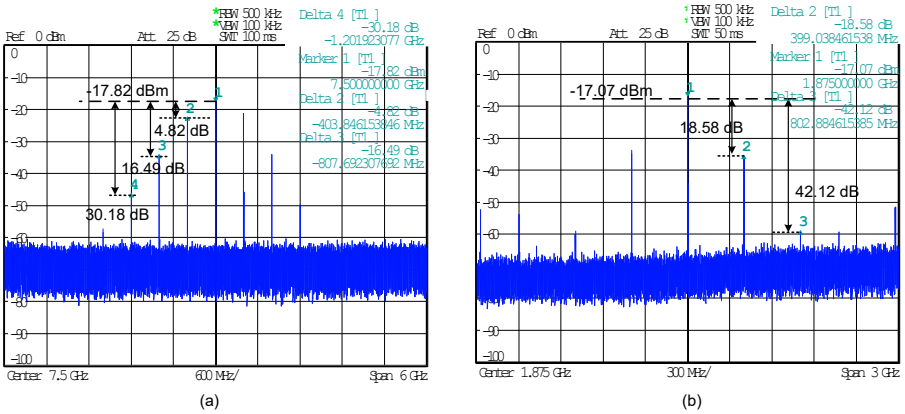


Fig. 4.6: Measured verification of division of modulation index for higher modulation rate. (a) Wideband FM input, f_c = 5GHz, f_m = 400MHz, β = 1, (b) BFC scaling at the divided fundamental output having β = 0.25.

Verification of the scaling of the modulation index at higher modulation rates is shown in Fig. 4.6, where a 7.5-GHz carrier is modulated at 400 MHz. The modulation index of 1 is scaled at the output to 0.25. The input impedance at the tuning port of the off-chip Hittite VCO limits the FM index, β, to less than 0.3 for modulating frequencies > 450 MHz. BFC ratios obtained from the spectra in Fig. 4.5 and 4.6 are tabulated in Table 4.1 and show good comparison with theory.

Table 4.1: Bessel function coefficients for different modulation indices

Theory								
β	J_0	J_1, $\lvert J_0/J_1\rvert$	J_2, $\lvert J_0/J_2\rvert$	J_3, $\lvert J_0/J_3\rvert$	J_4, $\lvert J_0/J_4\rvert$	J_5, $\lvert J_0/J_5\rvert$	J_6, $\lvert J_0/J_6\rvert$	J_7, $\lvert J_0/J_7\rvert$
0.25	0.9848	0.0077 18dB	0.0070 42.1dB					
1	0.765	0.44, 4.8dB	0.1149, 16.5dB	0.0195, 31.9dB				
4	-0.40	-0.066, 15.58dB	0.3641, 0.75dB	0.4301, -0.7dB	0.2811, 3dB	0.1320, 9.56dB	0.0345, 21.22dB	0.0151, 28.4dB
Measurement								
	β	$\lvert J_0/J_1\rvert$	$\lvert J_0/J_2\rvert$	$\lvert J_0/J_3\rvert$	$\lvert J_0/J_4\rvert$	$\lvert J_0/J_5\rvert$	$\lvert J_0/J_6\rvert$	$\lvert J_0/J_7\rvert$
Fig. 4.5a	4	15.32dB	0.72dB	-0.66dB	2.9dB	9.62dB	19.60dB	29.2dB
Fig. 4.5b	1	4.82dB	16.82dB	31.64dB				
Fig. 4.6a	1	4.82dB	16.49dB	30.18dB				
Fig. 4.6b	0.25	18.58dB	42.12dB					

The oscillator's locking profile measured with V_{CM} (see Fig. 3.2a) set to 0.6 V is shown in Fig. 4.7, for free-running frequency (f_0) values of 1.25, 1.5, and 1.75 GHz (see test-setup in Fig. 4.3b). For this measurement, the noise source is disconnected. The locking sensitivity is measured at each input frequency, with the oscillator first reset to f_0. The signal path and source are calibrated for losses and errors, res-

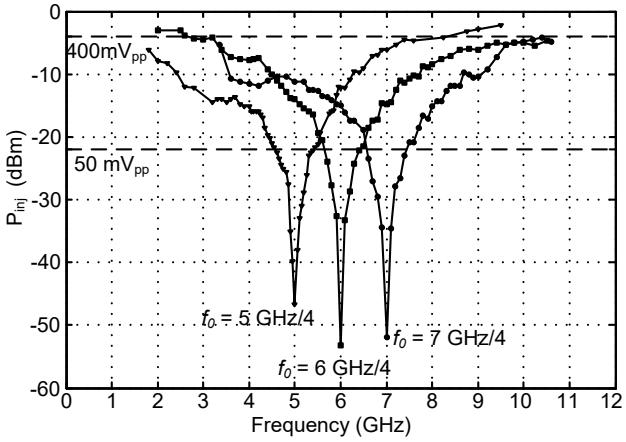


Fig. 4.7: Free-running injection-locking profile measured with the oscillator reset to f_0 each time. Measurement sets at f_0 = 1.25, 1.5, 1.75 GHz.

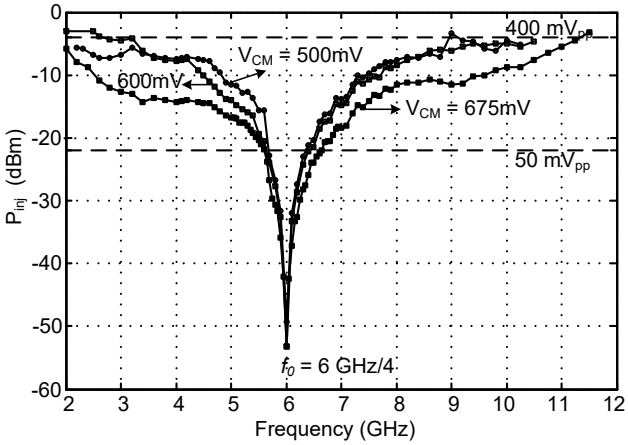


Fig. 4.8: Effect of V_{CM} seen on the locking range and sensitivity of the free-running locking profile.

-pectively. The locking sensitivity reduces as the offset from $4f_0$ increases. However, V_{CM}, can be optimized for gain (i.e., increase current I_Q as described in Section 3.2). The locking range and sensitivity at a given frequency increase with V_{CM} as seen from the measurements in Fig. 4.8. Increasing V_{CM} increases the g_m of the coupling transistors ($M_{C1\text{-}4}$ in Fi. 3.2a) resulting in larger signal- injection in the oscillator. The entire 2-10 GHz band can be covered without frequency tuning with V_{CM} set constant at 0.6 V at 400 $mV_{p\text{-}p}$ input swing. The locking profiles shown in Figs. 4.7

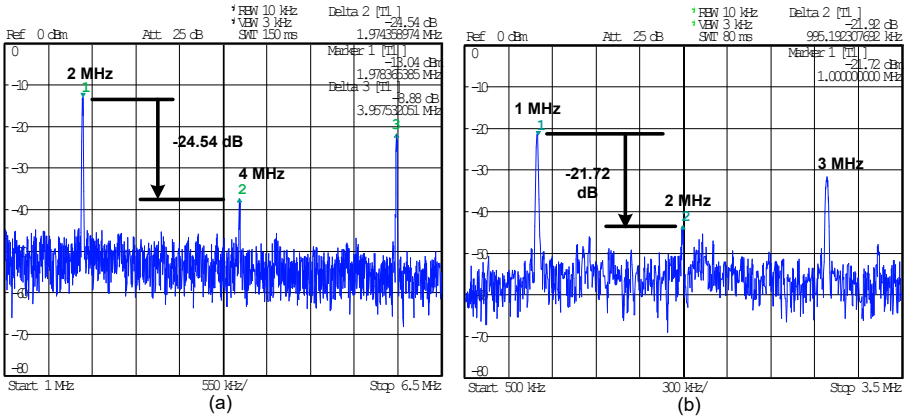


Fig. 4.9: Demodulated output spectrum (a) 4-5 GHz input modulated by a 2-MHz triangular signal, (b) 2-3 GHz input with 1-MHz modulation.

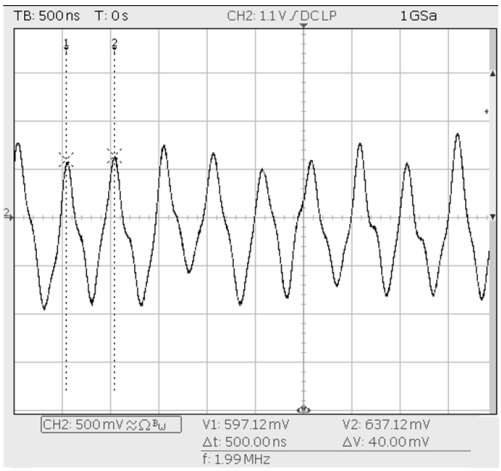


Fig. 4.10: Oscilloscope capture of the 2-MHz demodulated triangular-wave.

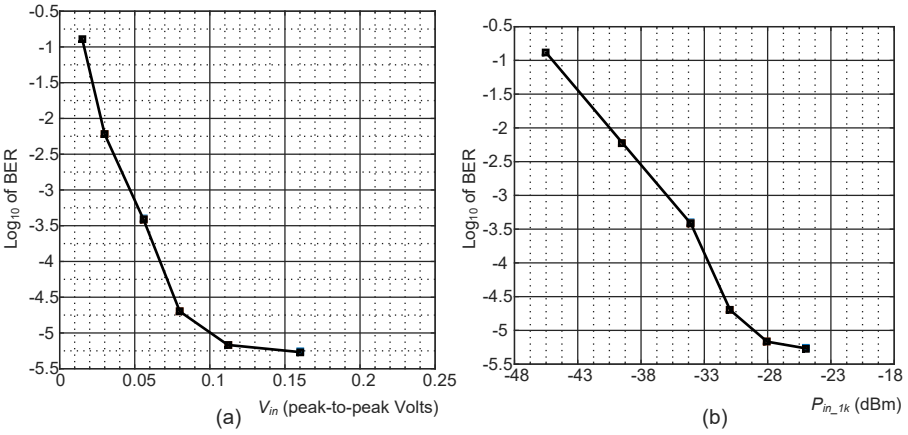


Fig. 4.11: Measured BER for the demodulator at a 10 Mbps data rate versus: (a) input amplitude, (b) Power delivered to 1-kΩ IF impedance.

and 4.8 are measured with the oscillator reset to f_0 after each locking measurement is completed at a particular frequency offset. The demodulated output for the test setup of Fig. 4.3a is shown in Fig. 4.9. The input RF band is 4–5 GHz, V_{CM} is 0.6 V, and f_0 is 1.5 GHz. The modulating signal is set to 2 MHz (limit of the wideband AWG), and a triangular waveshape is used to obtain a flat RF power spectrum. The demodulated output is a differential 1-V_{pp} 2-MHz triangular wave, with a second-harmonic suppression of ~24 dBc (see Fig. 4.9a). The oscilloscope capture of the

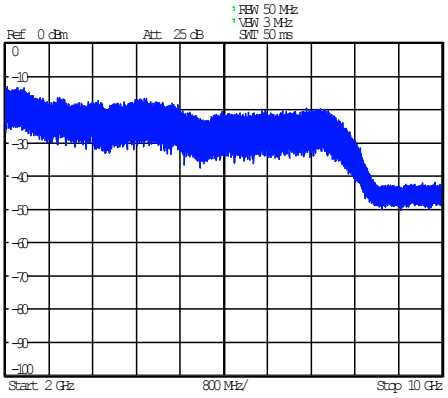


Fig. 4.12: Spectrum of the amplified noise-source captured with a 50-MHz resolution bandwidth at reference-plane 'X' in Fig. 17b, shows the variation from an ideal white-noise source (noise-coloring).

demodulated waveform is shown in Fig. 4.10. The output spectrum for the low-band case of 2–3 GHz and f_m = 1 MHz is shown in Fig. 4.9b. Note that the output power at frequencies lower than 10 MHz is attenuated by AC coupling at the spectrum analyzer input.

The bit-error-rate (BER) of the demodulator is measured using 3.75 – 6.25 V pulses at a rate of 5 MHz from an HP-3762A data generator. The input stream (PRBS 2^{10}-1) consists of pseudo-random-binary sequences of length equal to 1023 with 1 error-bit per 1000 patterns. The data modulates a Hittite VCO [4.HMC586LC4B] to generate the input FSK signal having a 1-GHz FM bandwidth around a 5-GHz carrier. Figs. 4.11a and 4.11b show the BER versus the input voltage and input power (delivered to 1 kΩ), respectively, measured using an HP-3763A error detector. A back-to-back connection of the data generator and error detector yields a BER of 9.8×10^{-7}. During measurement, the oscillator's f_0 was maintained at 1.25 GHz, and V_{CM} equals 0.62 V. The BER degrades rapidly with decreasing input power since the oscillator's locking-range shrinks for diminishing inputs (Fig. 4.7). The BER measured for a 100-mV_{pp} input signal is 6.8×10^{-6}, and it drops to 1×10^{-3} for a 45-mV_{pp} input.

Fig. 4.12 shows the noise spectrum at plane 'X' on Fig. 4.3b. The filtered noise is

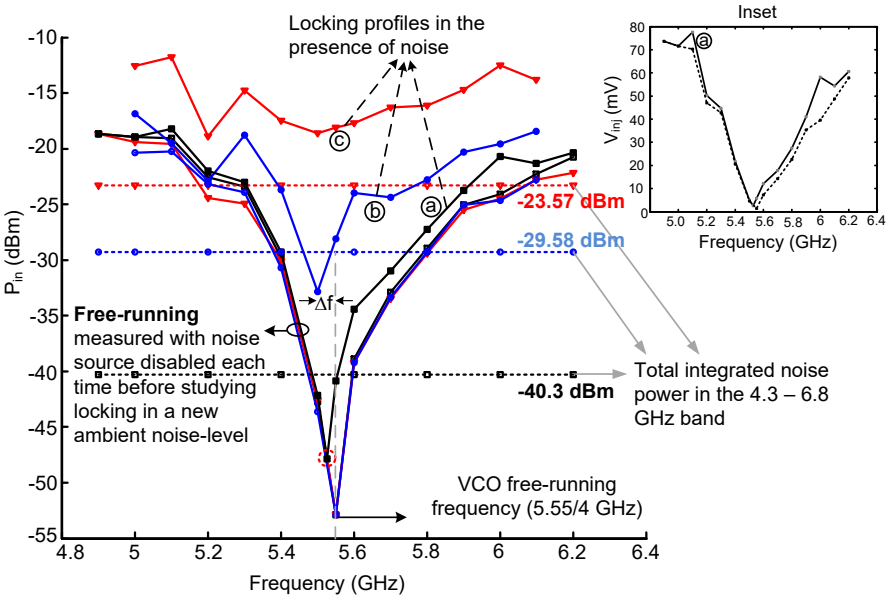


Fig. 4.13: Locking profile measured before and after applying different levels of integrated noise power to the locking signal. The oscillator's f_0 is set mid-band at 5.55 GHz/4. The free-running profile and curve 'a' are shown in mV scale in the inset.

colored (not white with a flat spectral density). Similar to measurements in Figs. 4.7 and 4.8, the curves marked 'free-running' in Fig. 4.13 show the oscillator's locking profile when the noise source is disabled. Each point on the figure is an average of 5 readings. The three measurement sets show a maximum spread of ~7 mV (at 5.2 GHz) and an average spread of ~2.5 mV. Sensitivity of the demodulator is limited by the oscillator's locking behavior in the presence of noise, which is analyzed via measurement. Noise is typically small-signal compared to the signal for BER<10^{-3}, and locking is a large-signal process. The evaluation of sensitivity limits requires comparable signal and noise levels (i.e., SNR≈1). Large-signal noise alters the properties of the free-running oscillator and its locking sensitivity. Our experimental study of the oscillator's response to varying noise levels using the test-setup of Fig. 3b ($4f_0$ set mid-band to 5.5 GHz, V_{CM} = 0.6V) reveals three distinct modes of operation:

In the first mode, the oscillator is driven by extremely low noise levels (i.e., high SNR). The interconnect losses are compensated using a ZRON-8G amplifier and

trimmed to within 1 dB using attenuators. The integrated noise power (4.33–6.75 GHz) applied at the probe head is measured using the HP-E4419A power meter, and equals -79.4 dBm. The noise induces a small shift in the frequency of oscillation (~kHz range) along with a phase-noise degradation of less than 0.6 dB. The observed frequency shift to a lower value agrees with theoretical predictions of an oscillator's response to white and colored noise [4.1], [4.2], [4.3]. In this mode, the locking sensitivity in the presence of noise does not vary discernibly in comparison with the free-running profile since the SNR remains high. For -79.4 dBm noise, when the oscillator locks, the SNR is ~60 dB at the band-edges and ~40 dB at $4f_0$ (as seen from Fig. 4.13a).

In the second mode, increased input-noise continues to shift the oscillation frequency to a lower value. A measured example is shown in Fig. 4.13, where the black-curve labelled 'a' represents the oscillator's locking profile in the presence of -40.3 dBm of integrated noise. A phase noise degradation of 9 dB and a noise-induced free-running frequency shift of ~6 MHz (24 MHz at $4f_0$) are observed at the output. As a result, the frequency for maximum sensitivity changes compared to the free-running case. The sensitivity change is better visible in the amplitude scale of the inset of Fig. 4.13. Measurements show that the oscillator is capable of locking to negative SNR values (between 5.49 to 5.56 GHz) in the vicinity of its newly established f_0, as seen from Fig. 4.13. The ability to lock to negative SNR values over a narrow frequency range is characteristic of this mode.

In the third mode, the excess noise destabilizes the oscillator, exciting chaotic behavior. The red curve labeled 'c' in Fig. 4.13 shows the locking profile in this mode when the noise power equals -23.57 dBm. The oscillator can still be locked to an input signal, although at an increased input drive (approx. -15 dBm). The absence of a stable oscillating frequency is reflected in the flat locking profile, along with the inability to lock to negative SNR inputs compared to mode-2. A transitional state between modes-2 and -3 is captured by the blue curve labeled 'b', when the oscillator is driven with -29.58-dBm of integrated noise. The oscillator shows a weak preference for a single frequency compared to mode-1.

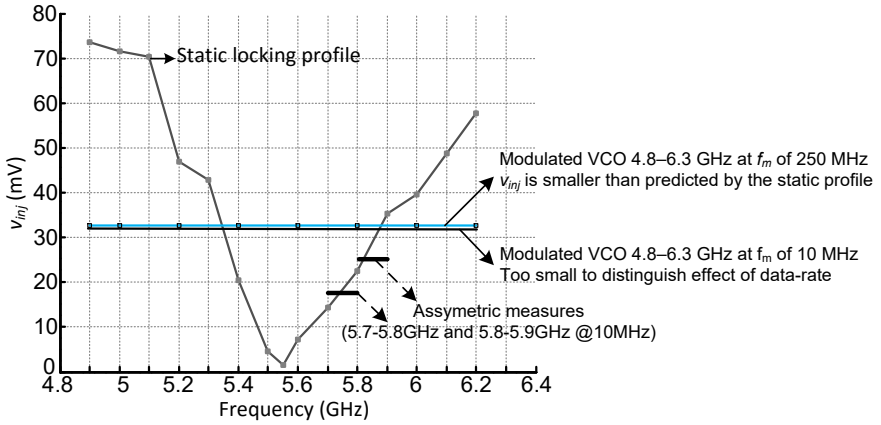


Fig. 4.14: Locking sensitivity to modulated signals (horizontal lines) differs from the static locking profile. Effect of data rate on locking signal strength between f_m = 10 MHz and 250 MHz is negligible.

The free-running oscillator's static locking profile (Figs. 4.7 and 4.8), does not accurately predict its response to a wideband signal. Fig. 4.14 shows the locking profile obtained from single-tone tests when the oscillator's f_0 is 5.55 GHz/4. Appended to the static profile is the minimum detectable wideband signal level, P_{mds}, for which the oscillator locks to a 4.8-6.3-GHz wideband FM signal having f_c = 5.55 GHz, f_m = 250 MHz and β = 1. The power of the wideband signal required

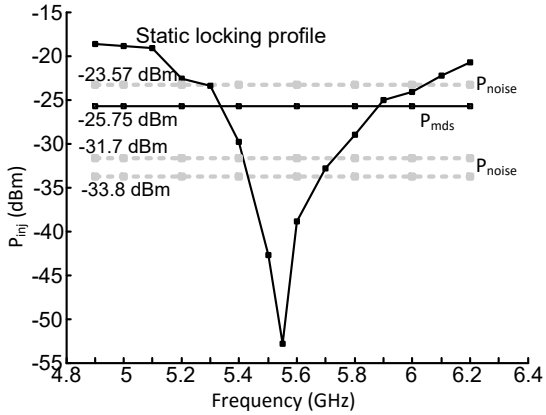


Fig. 4.15: Static locking profile and minimum input power (P_{mds}) for locking to f_c=5.55 GHz f_m=250 MHz and β=1. The integrated noise levels applied are annotated.

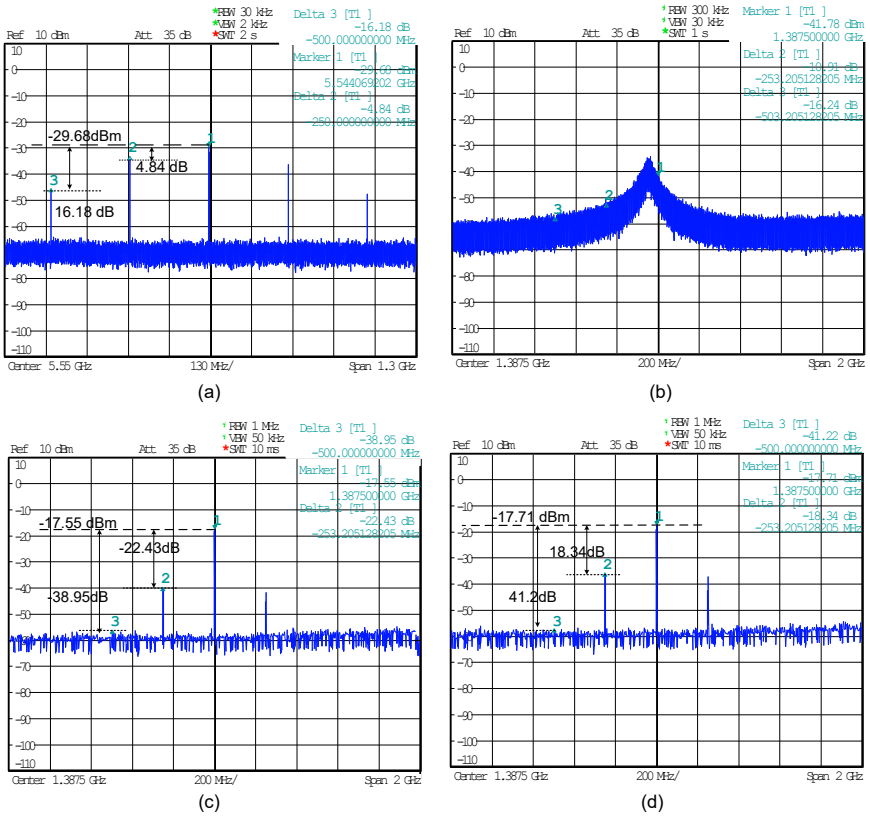


Fig. 4.16: Spectra of the locked-in oscillator for varying levels of SNR for a 5.55 GHz input (f_0 = 1.3875 GHz). (a) Input signal spectrum (β =1, fm = 250 MHz). The output spectra for integrated noise levels of Fig. 26b (b) SNR = -2.18 dB, (c) SNR = +5.95 dB and (d) +8.05 dB.

for locking, is less than what is predicted at the band-edges of the free-running locking profile, and similar for a 10- and 250-MHz modulation rate. Bessel-function transformation at the output characterizes FM-signal transmission through the locked-in ring (see Section 3.2.1), and is used to identify the minimum detectable signal. P_{mds} is measured at reference-plane 'Y' on Fig. 4.3b and is -25.75 dBm.

The input signal (P_{mds} at plane 'Y' in Fig. 4.3b) having β = 1, and f_m = 250 MHz is shown in Fig. 4.16a. The integrated noise levels indicated on Fig. 4.15 are then applied to the input. The integrated noise of -23.57 dBm results in complete loss of lock and the output is shown in Fig. 4.16b. The oscillator begins to partially lock to

the input signal at 6-dB SNR for a -31.7 dBm integrated noise input. This is evident from Fig. 4.16c, where the sideband attenuation corresponds to a modulation index lower than the expected 0.25. A drop in power of the FM sideband spectral tones is indicative that the oscillator has not locked over the entire bandwidth. At 8-dB SNR, the oscillator locks to the entire bandwidth as seen from Fig. 4.16d, with BFCs aligning with those for β = 0.25. Under the assumption that the oscillator tracks the same FM deviation at the same input drive levels, the SNR sensitivity for a 250-MHz signal can be expected to approximate that of a 500-Mbps signal. With the knowledge that: a) an 8-dB SNR input can be demodulated successfully, and b) the locking amplitude is independent of the modulation rate for f_c/f_m >10 (as seen from Fig. 4.14); referencing P_{mds} of -25.75 dBm (32.62 mV_{pp}) against the FSK detection curve of Fig. 4.11a gives an approximate of BER of $10^{-2.25}$ (5.62×10^{-3}). Coherent detection of a binary FSK signal with β=1 has a probability of error P_b that's given by [4.31]:

$$P_b = \frac{1}{2} erfc\left(\frac{SNR}{2}\right)^{0.5} = 6\times10^{-3} \quad (12)$$

For the same SNR, the ball-park estimate for BER of a high-data-rate binary FSK signal using the results in Fig. 4.16d, Fig. 4.15 and Fig. 4.11a shows less than 6.5% deviation from the theoretical estimate for a coherent FSK detector.

During the course of measurements shown in Figs. 4.13-4.16 it was observed that the oscillator consistently returns to its original free-running frequency and phase noise performance upon withdrawal of the external noise and signal stimuli.

Interference in mm-wave links is typically negligible. High antenna directivity enables line-of-sight wireless links, and attenuation due to path-loss reduces any potential interference. The response of the demodulator to in-band and out-of-band interference is studied using the setup shown in Fig. 4.3. The oscillator is tuned to its lower band edge of 900 MHz. In the presence of a wideband input from 2-3 GHz, the power of the interference signal (out-of-band at 1.95 GHz, i.e., 50 MHz spacing from the band-edge, and in-band at f_c = 2.5 GHz) is ramped up and sequentially ramped down. Spectrum captures of the wideband input and interference tones (at

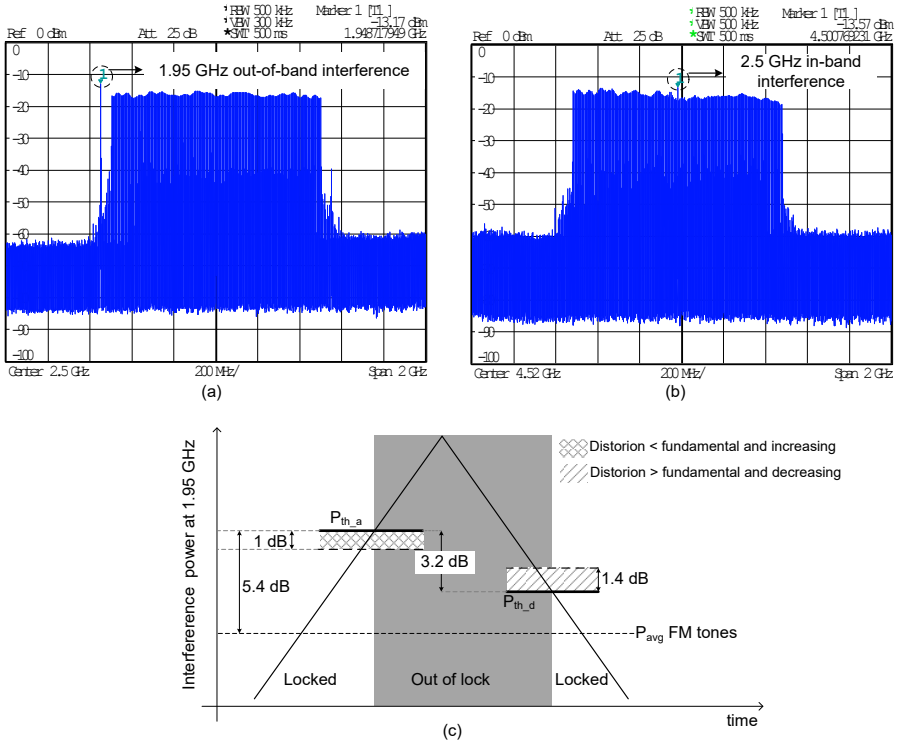


Fig. 4.17: Interference tests for a 2-3 GHz FM input (a) out-of-band (1.95 GHz), (b) in-band (2.5 GHz). (c) Impact of interference levels on the demodulator, and hysteresis.

reference place 'X' in Fig. 4.3a) are shown in Figs. 4.17a and 4.17b. As the power of the out-of-band interference surpasses the power of the FM spectral tones (by ~5.4 dB) it scrambles the demodulator output, which causes a rapid increase in harmonic content and beat notes. The observations from the experiment are illustrated in Fig. 4.17c. During the ramp's descent, the interferer threshold for restoration of normal operation (noted as P_{th_d}) drops compared to the value in ascent (P_{th_a}). Three important characteristics of the lock-in oscillator's response to interference are observed: 1. the time-based dependence of the response on its previous state reiterates the hysteresis accompanying injection locking that differentiates the oscillator's response to static frequencies and modulation over the same frequency band (Fig. 4.14), and 2. A thresholding effect is observed. Performance of the demodulator degrades rapidly beyond a certain interference level

and 3. Similar behavior is observed for in-band and out-of-band interference. The difference observed in this experiment is a ~6-dB lower interference tolerance level (P_{th_a}) and a ~5-dB separation between P_{th_a} and P_{th_d} for the in-band interferer.

4.2 Demodulator performance summary and comparison

Table 4.2 summarizes the performance of IF demodulators based on delay lines [4.7], injection locking [4.8], and phase shift networks [4.9], [4.10]. The IF demodulator developed in this work achieves excellent low-power wideband performance. The QVCO based design in [4.8] has a comparable data-rate capability. However, the narrowband phase linearity of the LC tank load, and limited locking range restrict its narrowband phase linearity of the LC tank load, and limited locking range restrict its wideband performance ($\Delta f/f_c$=0.08). The 7-mW power dissipation accounts only for the demodulator core. The 0.13-μm SiGe demodulator in [4.9] employs an LC phase-shift filter ($\Delta f/f_c$=*0.22*) that limits sensitivity at wide offsets from the carrier. Large signal drive and high mixer gain in

Table 4.2: Performance summary of recently published IF demodulators

[4.Ref.]	Tech.	V_{DD} (V)	Mod.	BW (Δf) (GHz)	$\Delta f/f_c$	Data Rate (Mb/s)	Q_{point} $P_{diss.}$ (mW)	Energy per bit (nJ)	P_{in} at $1e^{-3}$ BER (dBm)	Output Power (dBm)
[4.15]	0.18um CMOS	1.8	GFSK	0.44-0.54	0.2	1	3.6*	3.6	n/a**	n/a
[4.32]	0.13um CMOS	1.2	FM/FSK	19.2-21.8	0.08	1500	7.2*	0.005	-16	+1
[4.33]	0.13um SiGe	2.7	FSK	8-10	0.22	2000	32.4x	0.016	n/a	+1
[4.34]	0.18um CMOS	1.8	GFSK	.015-.025	0.50	1	12.6 x	12.6	n/a**	-13
This work	65nm CMOS	1.2	FM/FSK	2 – 10	1.34	10 800+	3.2	0.32	-36	+10•

*Demod. core power (no IF or baseband amplifier)
** Rail-to-rail input drive
x Includes IF Limiter but not baseband amplifier
+ Stand-alone oscillator characterization for high-data rate inputs
•Q-point power diss. does not include power for delivering 10dBm into the 50 Ohm load

wideband operation. In addition, as is the case with the LC delay in [4.7], the variation in magnitude response around the resonant frequency produces baseband distortion and limits [4.9] raises the power consumption to 34 mW. The active Bessel filters based quadrature discriminator in [4.10] shows wideband performance in the MHz range ($\Delta f/f_c=0.5$). However, the need for high-order filters increases power consumption (12.6 mW), while g_m/C bandwidth restricts efficient detection to lower data rates (~1 Mbps). Quadrature phased division of FM deviation demonstrated in this work reinforces the factors that underpin efficient demodulation, namely, reduction of the signal bandwidth (via reformation of β), provision of wideband quadrature phases at no additional power expense, and large signal drive delivered by the regenerative oscillator gain. When operating across 2-10 GHz ($\Delta f/f_c$=1.34), the entire demodulator dissipates just 3.2 mW from 1.2 V. The IF pre-amplifier required to drive the demodulator can be optimized for non-linear gain for a high IF impedance using, for instance, a ~17-mW distributed amplifier (extrapolated for 30-dB gain for 200 Ω from results of the 90-nm prototype in [4.11]) or a ~12-mW shunt-peaking driver [4.12] simulated in 65-nm CMOS for 35-dB gain from 2-10 GHz.

4.3 Summary and discussion

In Chapters 3 and 4, an FM demodulator is presented in which a 4-stage ring oscillator locks to a wideband input and divides the FM deviation by 4. Phase correlation of the locked-in oscillator's quadrature outputs allows simplified low-power demodulation, with a linear characteristic at baseband for a fractional bandwidth greater than one. Additional benefits of the injection locked demodulator are: data-rate independent power consumption, insensitivity to noise and AM interference, a requirement for low distortion is not imposed on the IF amplifier, and operation of the oscillator at $1/4^{th}$ the intermediate frequency enables a higher IF and a lower fractional bandwidth.

The propagation of an FM signal through an injection-locked oscillator is analyzed in depth. Division of frequency deviation and scaling of Bessel function coefficients derived analytically are verified via simulation and measured for a 65-nm prototype

demodulator. Through simulation and analysis, low-power circuits developed in the work are evaluated, namely, a ring oscillator with wideband sensitivity, a folded CMOS mixer with Q-point control, and a 3-stage differential class-AB amplifier (presented in Chapter 5). The prototype IC is characterized extensively using a wide range of test-benches to study division of FM deviation, wideband demodulation, noise sensitivity, and bit-error rates. Stand-alone characterization of the input oscillator showing its response to external noise and high modulation rate (up to 400 MHz) FM signals is presented, along with stand-alone characterization of the output Class-AB amplifier. The demodulator operation is measured over 2-10 GHz ($\Delta f/f_c$ = 1.34). Energy consumption is just 0.32 nJ/bit with an SNR sensitivity of 8 dB, and 0.1% BER at 10 Mbps observed for a 45-mV_{pp} input IF signal.

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Chapter 5 – Differential class-AB amplifier

A wideband, fully-differential, 3-stage class-AB amplifier capable of operation at rates of 100 MHz is described in this chapter [5.1]. The high loop gain and low impedance drive capability ensure a low-distortion interface to the 50-Ω measurement environment. Common-mode feedback is applied to increase output drive capability and reduce crossover distortion when operating in class-AB from a low supply voltage. Detailed analyses of gain-boosting doublets and the frequency response of the class-AB Monticelli bias are presented along with simulation and measurement results. Drawing between 800 μA and 3.9 mA from a nominal V_{DD} of 1.2 V in 65-nm CMOS, the 0.052-mm^2 amplifier delivers a 1.6-V_{pp} swing across a 50-Ω load with a THD+N of -82.6 dB at 150 kHz, in the unity-gain configuration.

5.1 Differential 3-stage Class-AB Amplifier: topology and design

The fully-differential class-AB amplifier developed for the prototype IF demodulator [5.2] is configured in shunt-feedback as shown in Fig. 3.1. It interfaces the demodulated output to a 50-Ω load for measurement. The amplifier is biased for low current consumption at 800 μA, and is compensated for a 60^o phase margin when driving a 10-pF load. In this configuration, the amplifier's open-loop DC gain is 83 dB and it has a 70-MHz unity-gain bandwidth.

CMOS amplifiers typically suffer a headroom limitation that worsens with technology and voltage scaling (e.g., below 1-V V_{DD}), as the transistor threshold voltage remains relatively constant. Operating the output class-AB stage from a higher voltage compared to preceding stages [5.3] maximizes output power for a given MOS threshold, but requires multiple supplies. Crossover distortion is an important aspect of class-AB operation, and even-order terms can be reduced but not eliminated in a complementary topology via device sizing and bias control [5.4]. Fully-differential operation maximizes the output swing from a given V_{DD} (1.8 V_{pp} from 1.2 V), suppresses even-order distortion, and rejects noise and interference arising from co-integration with other sub-circuits.

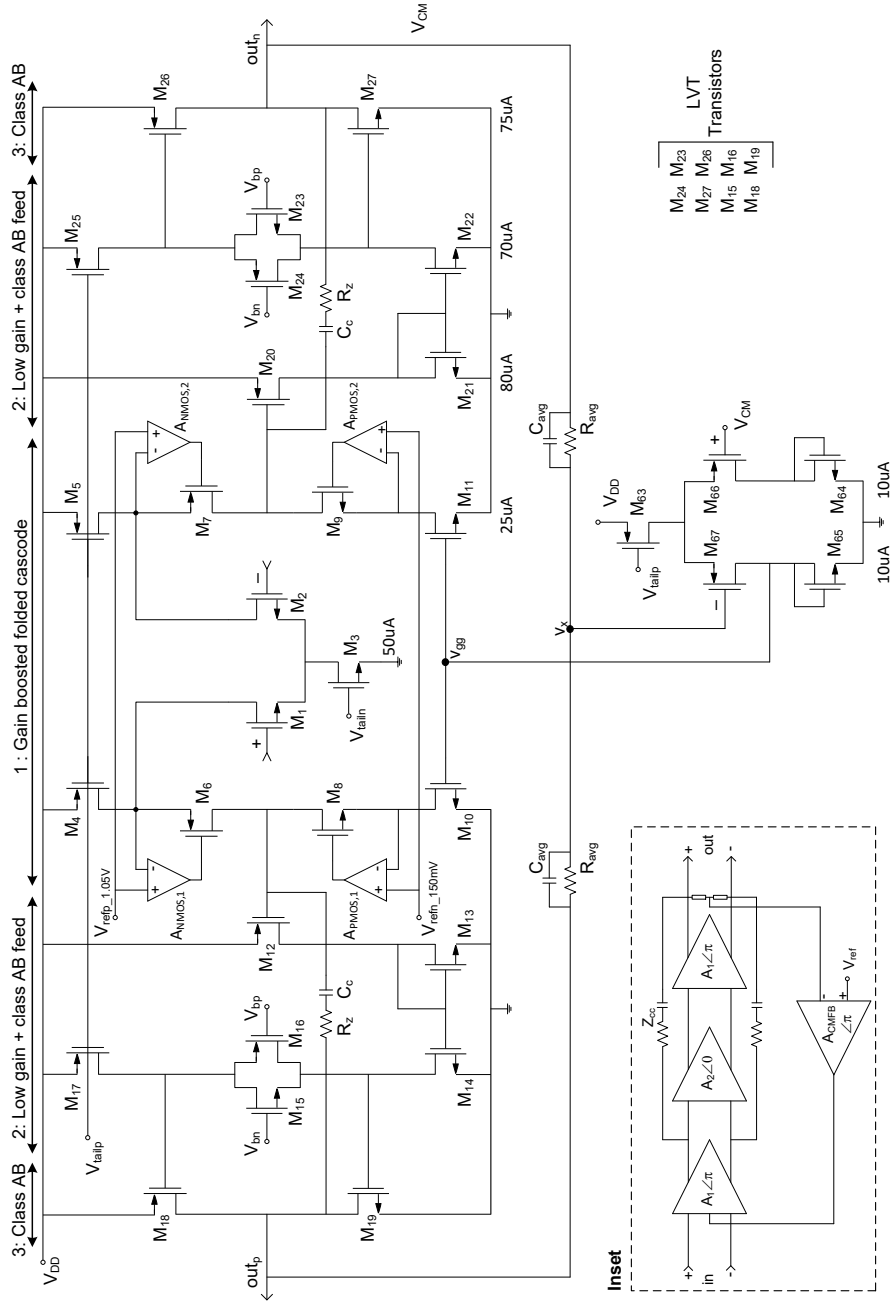

Fig. 5.1: Circuit diagrams of the differential 3-stage Class-AB amplifier, a simplified block diagram of the three stages and CMFB is shown in the inset.

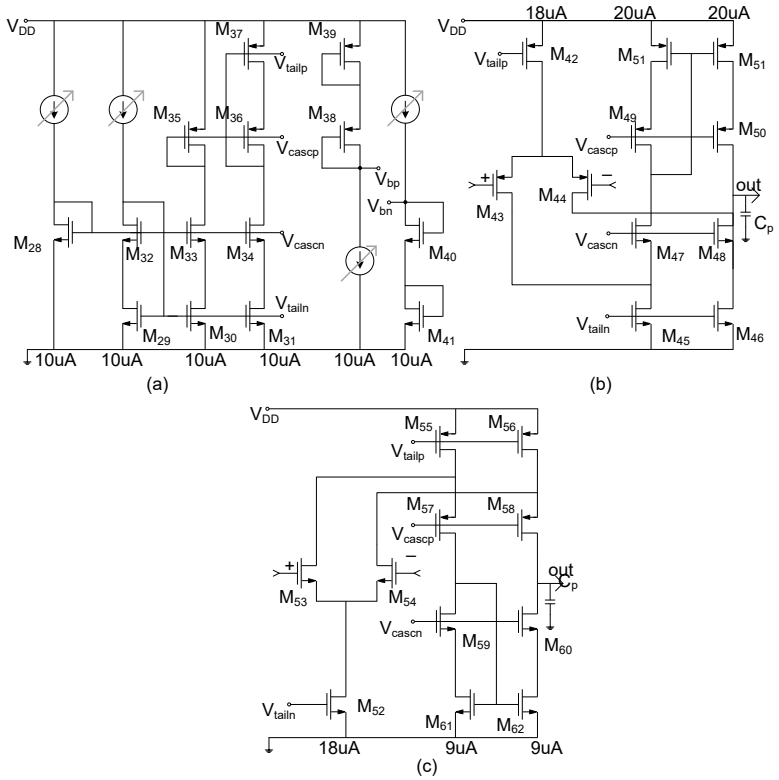

Fig. 5.2: Circuit diagrams of: (a) the bias block and amplifiers (b) A_{PMOS} and (c) A_{NMOS} from Fig. 5.1.

The amplifier schematic, annotated with branch currents, is shown in Fig. 5.1. The inset shows a simplified block diagram of the three-stage amplifier outlining the differential and common-mode signal paths. Schematics of the amplifier's sub-cells are shown in Figs. 5.2a- 5.2c. The first stage is a fully-differential gain-boosted, folded-cascode (FC) amplifier. The negative feedback loop applied to transistors $M_{6\text{-}9}$ increases the output impedance of the cascode arm by a factor of the auxiliary amplifier's gain (A_{NMOS} and A_{PMOS} in Fig. 5.1), resulting in an increase in DC gain without impact on the unity-gain bandwidth of the amplifier. It is therefore possible to achieve fast settling and high gain at the same time. The DC voltage at the source terminals of transistors $M_{6,9}$ is regulated using reference voltages V_{refp} and V_{refn}, allowing a 150-mV gate overdrive for transistors $M_{4,5}$ and $M_{10,11}$. The gates of $M_{10,11}$, typically at AC ground, are used for common-mode bias control. Differential

operation of the first stage eliminates a pole/zero pair produced by the current mirror required for single-ended implementation. Looking at the 2nd stage half-circuit, low-gain inversions from M_{20} and M_{22} drive the Monticelli CMOS pair $M_{23,24}$ [5.5] biasing the third class-AB stage. The diode-connected transistor M_{21} is a wideband load at the drain of M_{20}, however, a significant 2nd stage pole is seen at the output of M_{22}. When the CMFB loop is operating, DC voltage at the first-stage output is determined by the V_{SG} requirement of M_{20} (and M_{12}) to conduct current sourced by M_{25} (and M_{17}), as determined by the mirrors-ratio between $M_{21,22}$ and $M_{13,14}$ [5.6], [5.7]. Trimming C_p controls the bandwidth of the gain-boost loop, and the doublet seen in the frequency response.

5.2 Small signal analysis

The uncompensated amplifier has 4 important poles [5.1], which are evaluated in detail here. The dominant pole is located at the output of the first gain-boosted, FC amplifier stage. Time constants of the third and second stages, account for the second and third poles, respectively. The 4th pole is determined by the time constant associated with the source nodes of $M_{6,7}$. The doublets arising due to the frequency response of the gain enhancement loop, analyzed in this section, are placed between the unity-gain frequency and the second pole of the amplifier [5.8].

5.2.1 Gain boost amplifier

Neglecting body-effect, the output impedances of the cascode arm (e.g., $M_9 - M_{11}$) before and after gain boosting are derived in references [5.8] and [5.9], respectively, and equal[1,2]:

$$r_{casc} = r_{ds11}(g_{m11}r_{ds9} + 1) + r_{ds9}, and \tag{5.1}$$

[1] An approximation of eqn. 5.1 is reached by noting that the loop-gain of the current-sense voltage-feedback loop equals ($g_{m11}r_{ds9}$). Therefore, $r_{o\_casc} \approx r_{ds11}(1+ g_{m11}r_{ds9})$.

[2] With the inverting amplifier added to the loop, an approximation of eqn. 5.2 is reached by noting that the two feedback components at the source net ($g_{m11}r_{ds9}$), and at the gate net ($-g_{m11}r_{ds9}A_{aux}$), respectively, result in a total negative loop-gain equal to $g_{m11}r_{ds9}(1+A_{aux})$. Therefore $r_{o\_GB} \approx r_{ds11}(g_{m11}r_{ds9}(1+A_{aux})+1)$.

$$r_{o\_GB} = r_{ds11}(g_{m9}r_{ds9}(1 + A_{aux}) + 1) + r_{ds9} \\ = r_{ds9} + r_{ds11} + r_{ds11}g_{m9}r_{ds9}(1 + A_{aux}). \tag{5.2}$$

Assuming a single pole roll-off for the gain-boost amplifier $A_{PMOS1,2}$ at ω_p, and an open-loop gain of A_p, eqn. 5.2 can be written as:

$$r_{GB\_n} = r_{ds9} + r_{ds11} + r_{ds11}g_{m9}r_{ds9}\left[1 + \frac{A_p}{\left(1 + j\frac{\omega}{\omega_p}\right)}\right], \tag{5.3}$$

$$r_{GB\_n} = \Sigma r_{ds} + r_{ds11}g_{m9}r_{ds9}(1 + A_n)\left[\frac{1 + j\frac{\omega}{(1 + A_p)\omega_p}}{\left(1 + j\frac{\omega}{\omega_p}\right)}\right], \tag{5.4}$$

$$r_{GB\_n} \approx r_{casc}(1 + A_n)\left[\frac{\left(1 + j\frac{\omega}{(1 + A_p)\omega_p}\right)}{\left(1 + j\frac{\omega}{\omega_p}\right)}\right]. \tag{5.5}$$

It is seen from eqn. 5.5 that the gain-boosted output resistance is frequency dependent. The roll-off at ω_n is -20-dB/dec, and it flattens out to its original value of the cascode impedance[3] on encountering the zero in its transfer function at $(1+A_n)\omega_n$. Both NMOS and PMOS cascode branches of the first stage in Fig. 5.1 are gain-boosted. Enhancing the output impedance of just one section can at best provide a 6-dB increase in the open-loop voltage gain. Denoting the DC gain of auxiliary amplifiers $A_{NMOS1,2}$ as A_n and the pole frequency as ω_n in eqn. 5.5, the output impedance of PMOS cascode branch (e.g., $M_7 - M_5$) may be written as[4]:

$$r_{GB\_p} \approx r_{casc}\left(1 + A_p\right)\left[\frac{1 + j\frac{\omega}{(1 + A_n)\omega_n}}{\left(1 + j\frac{\omega}{\omega_n}\right)}\right]. \tag{5.6}$$

The total output resistance, r_o, is the parallel combination of NMOS and PMOS cascode-arm impedances described by eqns. 5.5 and 5.6:

[3] It is assumed that the second pole of the loop located at the source of M_{11} lies at a higher frequency, and therefore, doesn't interfere with the frequency response.

[4] For ease of analysis, the cascode impedance of the PMOS branch prior to gain boosting is assumed equal to that of the NMOS branch (r_{0_casc}).

$$r_o = (1+A_n)(1+A_p)r_{casc} \cdot \left[\frac{\left[\frac{1+j\frac{\omega}{(1+A_n)\omega_n}}{\left(1+j\frac{\omega}{\omega_n}\right)}\right]\left[\frac{1+j\frac{\omega}{(1+A_p)\omega_p}}{\left(1+j\frac{\omega}{\omega_p}\right)}\right]}{(1+A_n)\left[\frac{1+j\frac{\omega}{(1+A_n)\omega_n}}{\left(1+j\frac{\omega}{\omega_n}\right)}\right]+(1+A_p)\left[\frac{1+j\frac{\omega}{(1+A_p)\omega_p}}{\left(1+j\frac{\omega}{\omega_p}\right)}\right]}\right]. \quad (5.7)$$

$$r_o = \frac{(1+A_n)(1+A_p)}{(2+A_p+A_n)} r_{casc} \cdot \left[\frac{\left(1+j\frac{\omega}{(1+A_n)\omega_n}\right)\left(1+j\frac{\omega}{(1+A_p)\omega_p}\right)}{\left[(j\omega)^2\frac{2}{(2+A_p+A_n)\omega_n\omega_p}+j\omega\frac{\left(\omega_n(2+A_n)+\omega_p(2+A_p)\right)}{(2+A_p+A_n)\omega_n\omega_p}+1\right]}\right], \quad (5.8)$$

$$r_o = A_{eff} r_{casc} \cdot \left[\frac{\left(1+j\frac{\omega}{\omega_{zn}}\right)\left(1+j\frac{\omega}{\omega_{zp}}\right)}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2}}\right)}\right]. \quad (5.9)$$

It is clear from eqn. 5.8 that there are two zeros in the output resistance and their location remains unaltered from that in the individual feedback loops.

The denominator of eqn. 5.8 is a second-order polynomial that can be cast into the form of eqn. 5.9. It will be shown that the parallel connection of two gain-boosted loops results in a set of frequency doublets when loaded with a capacitance in parallel. The low-frequency pole in the denominator of eqn. 5.8 determines the 20-dB/dec roll-off of the effective output resistance, r_0, and the second high-frequency pole compensates the phase-shift produced by the additional zero present in eqn. 5.8 when compared with eqns. 5.5 and 5.6. Solving eqn. 5.8 yields:

$$\omega_{zn} = (1+A_n)\omega_n, \quad (5.10)$$

$$\omega_{zp} = (1+A_p)\omega_p, \quad (5.11)$$

$$\omega_{p1} = \frac{1}{4}\left(\omega_n(2+A_n)+\omega_p(2+A_p)\right)(1-k_0) \text{ and} \quad (5.12)$$

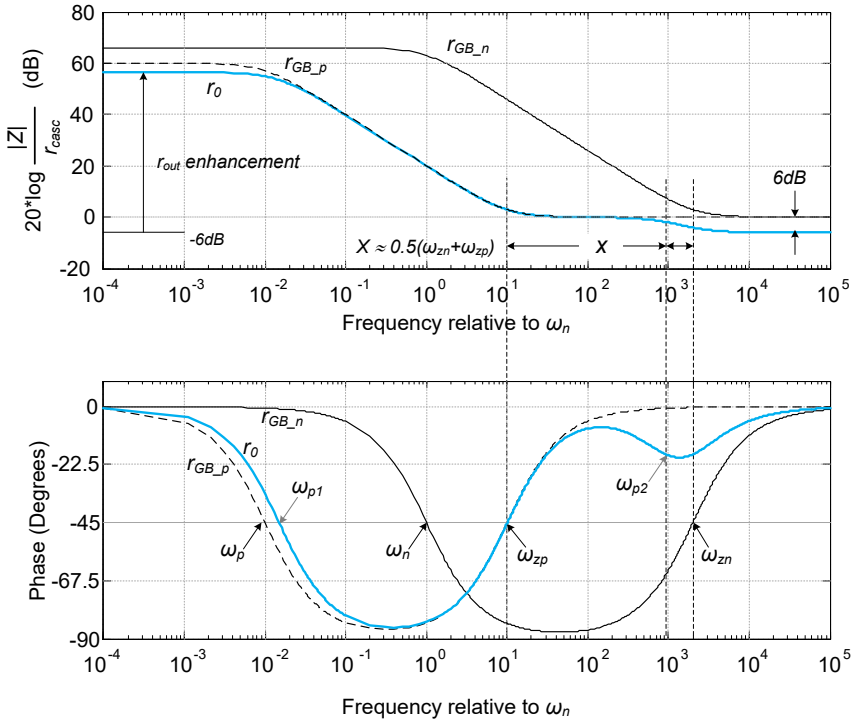

Fig. 5.3: Matlab™-simulated magnitude- and phase-responses of the gain-boosted impedances r_{GB_n}, r_{GB_p} (eqn. 5.5 and eqn. 5.6, respectively), and their parallel combination described by eqn. 5.8 (A_n = 60 dB, A_p = 66 dB).

$$\omega_{p2} = \frac{1}{4}\Big(\omega_n(2+A_n) + \omega_p\big(2+A_p\big)\Big)(1+k_0), \tag{5.13}$$

$$where\ k_0 = \sqrt{1 - \frac{2\omega_n\omega_p\big(4A_n + 4A_p + 8\big)}{\Big(\omega_n(2+A_n) + \omega_p\big(2+A_p\big)\Big)^2}}. \tag{5.14}$$

$$\lim_{k_0 \to 1} \omega_{p2} \approx \left[\frac{\big(\omega_{zn} + \omega_{pn}\big) + \big(\omega_n + \omega_p\big)}{2}\right] \approx \left[\frac{\big(\omega_{zn} + \omega_{pn}\big)}{2}\right]. \tag{5.15}$$

Fig. 5.3 shows the frequency response of the gain-boosted output impedance (i.e., eqns. 5.5, 5.6 and 5.8) simulated using Matlab™. In this example the gains A_n and A_p are 60 and 66 dB, respectively, and angular frequencies ω_n and ω_p correspond to frequencies of 100 kHz and 10 kHz, respectively. The curves corresponding to eqns. 5.5 and 5.6 are labeled 'r_{GB_n}' and 'r_{GB_p}', respectively, and the blue curve

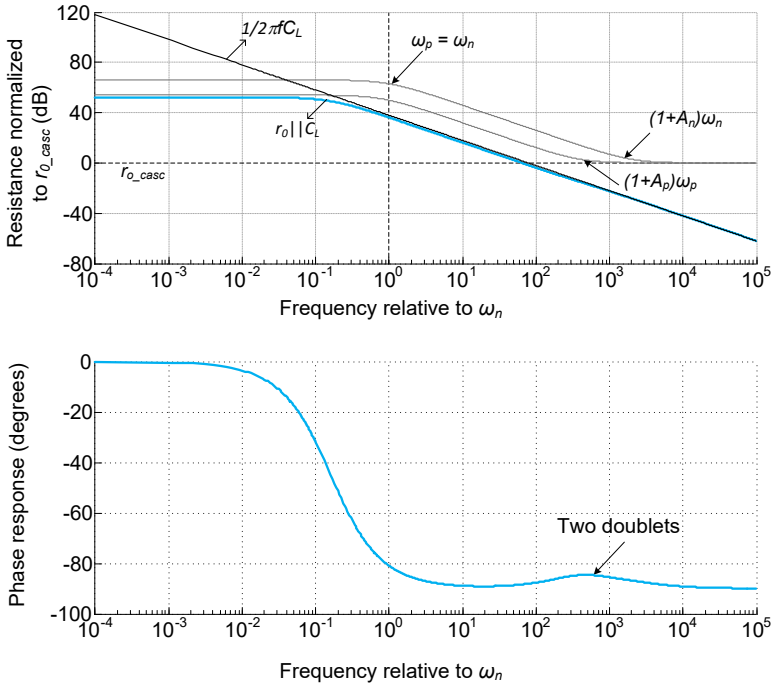

Fig. 5.4: Matlab™-simulated magnitude- and phase-response showing two frequency doublets obtained from the parallel combination of gain-boosted resistances r_{GB_n} and r_{GB_p}, with a load capacitance, C_L.

corresponding to eqn. 5.8 is labeled 'r_0'. The ordinate is normalized to the cascode impedance prior to gain-boosting (r_{casc}), and the multiplication of the output impedance by a factor of $A_{eff} = (1+A_n)(1+A_p)/(2+A_n+A_p)$, as seen from eqn. 5.8, is visible in the magnitude response shown in Fig. 5.3 at low frequencies. The enhancement is recorded from -6 dB, which corresponds to the parallel combination of the cascode impedances prior to gain boosting. The total output resistance, r_0, rolls-off at 20-dB/dec after encountering ω_{p1} and tends to flatten at ω_{zp}. The second pole ω_{p2} (see eqn. 5.13), lies between the two zeros described by eqns. 5.10 and 5.11[5], and Fig. 5.3 shows its impact on the frequency response. The impedance

[5] ω_{p2} lies almost mid-way between ω_{zn} and ω_{zp}, with less than 2% variation from the mean location for a moderate 40-dB DC gain ascribed to A_n and A_p. The simplification is captured in eqn. 5.15.

ultimately levels-off at $r_{casc}/2$ after ω_{zn} when both loop gains are less than one.

The frequency response of the parallel combination of r_0 and the load capacitance (1.75 pF in this example) is shown in Fig. 5.4. A 90-degree phase-shift is seen at the output when compared to Fig. 5.3 due to the additional pole seen at the output due to the load-capacitance. This pole is located in the close vicinity of the higher zero – ω_{zn} in this example. Contrary to common understanding, there is a set of doublets, as opposed to a single doublet, in the frequency response of gain-boosted FC amplifier.

Unlike the exaggerated examples shown in Figs. 5.3 and 5.4, doublets are hard to discern from the frequency response of the amplifier, and their presence is better visible in the settling response of the amplifier. Doublets in the frequency response produce a slow-settling component [5.10]. The heuristic approach in [5.8] assumes a single gain-boosted loop with an ideal current source and concludes that an acceptable frequency range for à pole-zero doublet is:

$$\beta\omega_{ug} < \omega_z < \omega_2. \tag{5.16}$$

In eqn. 5.14, ω_{ug} is the unity-gain frequency of the overall amplifier, $1/\beta$ is the gain when the amplifier is configured in negative feedback, and ω_z is the unity-gain frequency of the gain-boost amplifier (ω_{zn} defined by eqns. 5.10). The second pole of the amplifier is denoted as ω_2 (note: clearly, ω_2 of the amplifier and ω_{p2} in the gain-boosted output-impedance described by eqn. 5.14 are different and not to be confused). The design scope narrows down to placing the doublets between the unity-gain frequency of the amplifier and its second pole when designed for use as a unity-gain buffer.

Trimming capacitance C_p at the output of gain-boost amplifiers (see Fig. 5.2) controls the bandwidth of the gain-boost loop, and therefore the doublets seen in the frequency response shown in Fig. 5.4. The design freedom is constrained by having to first optimize C_p to ensure stability of the loop such that the phase-margin is greater than 60 degrees. The impact of doublets on the step-response is presented after a discussion on frequency compensation of the amplifier in section 5.2, where the frequency range available for positioning the doublets is also outlined.

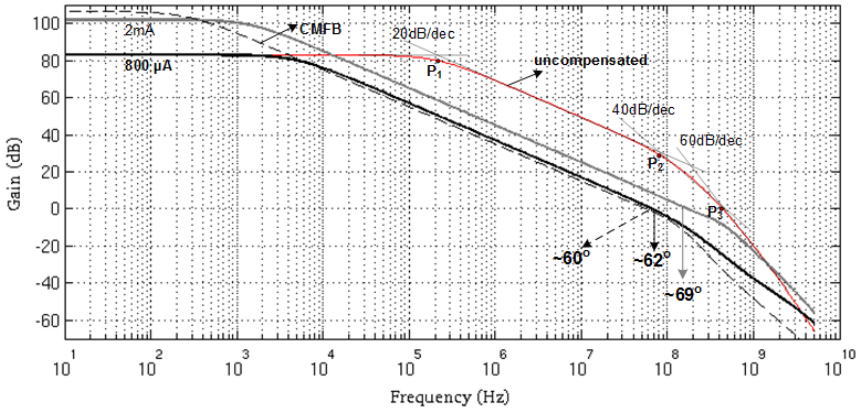

Fig. 5.5: Simulated differential and common-mode small-signal response of the amplifier of Fig. 5.1, with phase margins annotated on the figure.

5.2.2 Three-stage amplifier model

As described earlier, the uncompensated amplifier has 4 important poles [5.1]. The dominant pole is located at the output of the first stage. Time constants of the third and second stages, account for the second and third poles, respectively. The 4th pole is determined by the time constant associated with the source nodes of $M_{6,7}$. A small-signal simulation of the amplifier's differential and common-mode response for a 50 Ω || 10 pF load is shown in Fig. 5.5, for a total bias current of 800 µA drawn from V_{DD}.

The poles of a Miller-compensated 3-stage amplifier assuming 1 pole per stage are derived in [5.11], for the small-signal equivalent model shown in Fig. 5.6. The poles

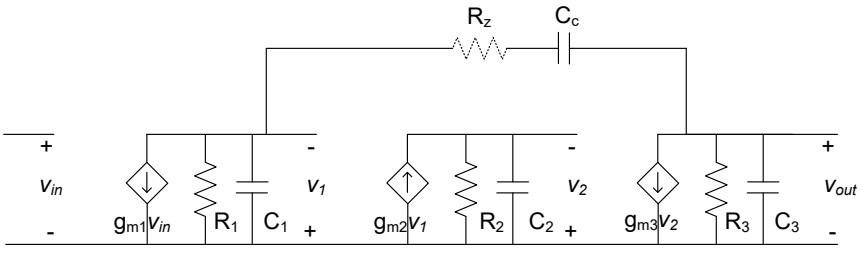

Fig. 5.6: Simplified small-signal circuit used for analysis.

and zeroes of the transfer function are:

$$P_1 = \frac{1}{(R_1 C_c)(g_{m2} R_2)(g_{m3} R_3)}, \tag{5.16}$$

$$P_3 = \frac{1}{(R_2 C_2)}, \tag{5.17}$$

$$P_2 = \frac{g_{m3}}{C_3} g_{m2} R_2, \tag{5.18}$$

$$Z_1 = -\left(\frac{\sqrt{b^2 + 4a} - b}{2a}\right) \; and \tag{5.19}$$

$$Z_2 = \left(\frac{b + \sqrt{b^2 + 4a}}{2a}\right), \tag{5.20}$$

$$where \; a = \left(\frac{C_c C_2}{g_{m2} g_{m3}}\right) \; and \; b = \frac{1}{g_{m2} R_2}\left(\frac{C_c}{g_{m3}}\right). \tag{5.21}$$

From eqns. 5.16 to 5.18 it can be seen that gain-boosting increases the output impedance and therefore permits a lower value for the miller capacitance C_c. Increasing g_{m3} increases gain, and aids pole splitting (see 2-mA example in Fig. 5.5).

As a first-order approximation, the second stage's time constant is independent of networks loading other stages, and the Miller capacitance, C_c. It is interesting to note that the gain of the second stage, $g_{m2}R_2$, aids pole-splitting by lowering P_1 and increasing P_2. However, the second stage is optimized for minimizing the time-constant R_2C_2. Placing the second stage's pole, P_3, outside the unity-gain bandwidth obtained after pole-splitting avoids the need for nested Miller compensation.

The transfer function of the small-signal model of Fig. 5.6 contains two zeroes, Z_1 and Z_2, which are described by eqns. 5.19 and 5.20, respectively. The high-frequency LHP-zero, Z_2, can be neglected since it lies more than an order of magnitude beyond the amplifier's unity-gain bandwidth. The low-frequency right-half-plane (RHP) zero, Z_1, due to C_c is transformed to a LHP zero using a nulling resistor R_z [5.12] to offset P_3. The pole created by R_z and C_1 does not significantly degrade the phase margin. In this design C_c is a 520-fF MOM capacitor and R_z is a 900-Ω polysilicon resistor with an option for trimming implemented

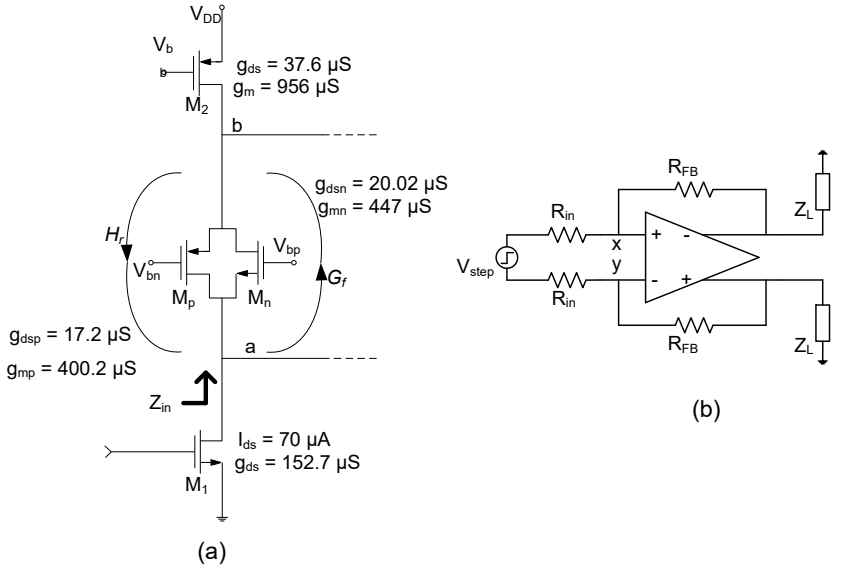

Fig. 5.7: Monticelli-cell analysis and operating point values used to evaluate eqns. 5.22 to 5.24, and (b) fully differential shunt-feedback configuration.

with parallel resistors and switches (3 bits).

5.2.3 Class-AB driver and Monticelli bias pair

The complimentary Monticelli bias cell transistors form a feedback loop indicated in Fig. 5.7. Signal paths G_f and H_r are the forward and reverse gains at DC, respectively. Solving for the input impedance [5.13] yields:

$$Z_{in} = \left[\frac{Z_{0\_in}}{1 - G_f H_r}\right], where\ Z_{0\_in} = \left[\frac{1}{g_{mn}} \parallel r_{ds1} \parallel r_{ds\_n}\right], \tag{5.22}$$

$$G_f = \left[\left\{\frac{\left(\frac{1}{g_{mp}} \parallel r_{ds2}\right)}{\left(\frac{1}{g_{mp}} \parallel r_{ds2} + r_{ds_{np}}\right)}\right\} + g_{mn}\left\{\frac{1}{g_{mp}} \parallel r_{ds2} \parallel r_{ds_{np}}\right\}\right] and \tag{5.23}$$

$$H_r = \left[\left\{\frac{\left(\frac{1}{g_{mn}} \parallel r_{ds1}\right)}{\left(\frac{1}{g_{mn}} \parallel r_{ds1} + r_{ds\_np}\right)}\right\} + g_{mp}\left\{\frac{1}{g_{mn}} \parallel r_{ds1} \parallel r_{ds\_np}\right\}\right]. \tag{5.24}$$

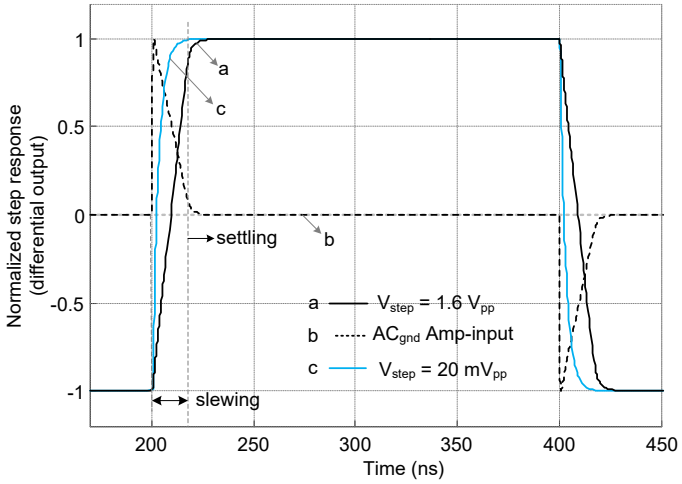

Fig. 5.8: Differential small-signal and large signal step-response of the amplifier configured in unity-gain shunt-feedback (R_{FB}, R_{in} = 10 kΩ, Z_L = 50 Ω || 10 pF). Output-slewing and settling are annotated on the figure.

Z_{0_in} is the open-loop DC impedance loading node '*a*', and g_{mn} and g_{mp} are the trans-conductances of M_n and M_p, respectively. The output resistances (r_{out}) of M_1 and M_2 are r_{ds1} and r_{ds1}, respectively, and r_{ds_np} is the parallel combination of the r_{out} of M_n and M_p. Keeping $g_{mn} \approx g_{mp}$ in the presence of the passive transfer (first terms in eqns. 5.23 and 5.24) ensures that the loop gain, $G_f H_r$, is less than one to ensure stability. From Fig. 5.7, Z_{in} is 5.38 kΩ, the loop gain is 0.70, and the capacitance (C_L) loading node 'a' is ~90 fF. The second-stage pole ($Z_{in}C_L$) predicted at 354 MHz is in close proximity to P_3 at 385 MHz (see Fig. 5.5), validating the analysis. A measurement sum--mary of the amplifier's stand-alone performance and comparison with recently reported Class-AB amplifiers is presented in Section 5.4.

5.3 Step response and noise

The Spectre™-simulated transient response of the amplifier to a small-signal (20 mV_{pp}) and large-signal (1.6 V_{pp}) differential input voltage-step is shown in Fig. 5.8. In this example, the amplifier is configured in unity-gain shunt-feedback as shown in Fig. 5.7b and drives a 50-Ω || 10-pF load, and is biased at 800 µA (see AC response in Fig. 5.5). The 1.6-V_{pp} response is slew-rate limited and the regions of

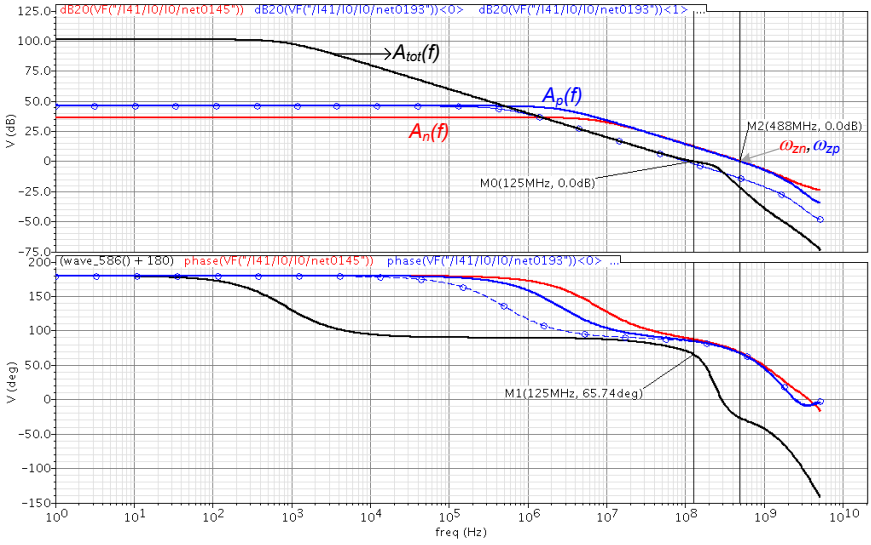

Fig. 5.9: Frequency response of the compensated amplifier and the NMOS and PMOS gain-boost loops of the first cascode stage (Z_L = 50 Ω || 50 pF).

slewing and settling are annotated on Fig 5.8. The simulated slew-rate is 88 V/µs (44 V/µs single-ended). The settling transient on the differential input nets, nodes '*x*' and '*y*', is also shown in Fig. 5.8. A ratio of the differential output and input voltage is approximately equal to the open-loop gain of the amplifier and determines the settling accuracy. This also reveals slow-settling components produced by doublets in the frequency response.

The amplifier's frequency response for a 50-Ω || 50-pF load is shown in Fig. 5.9, and represents the maximum capacitance for which the amplifier has a 60-degree phase margin. The single-pole approximation used in eqns. 5.5 and 5.6 is implemented with gain-boost loops having a 70-degree phase margin, as seen from Fig. 5.9. The amplifiers ANMOS and APMOS (see Fig. 5.2) are designed for equal unity-gain frequencies; this is also seen from Fig. 5.9, where $\omega_{zn} = \omega_{zp}$. According to [5.10] the time-constant of the slow-settling component varies inversely with the frequency at which the doublet occurs, and its relative magnitude is directly proportional to the spacing between the pole and zero and inversely proportional to the amplifier's unity

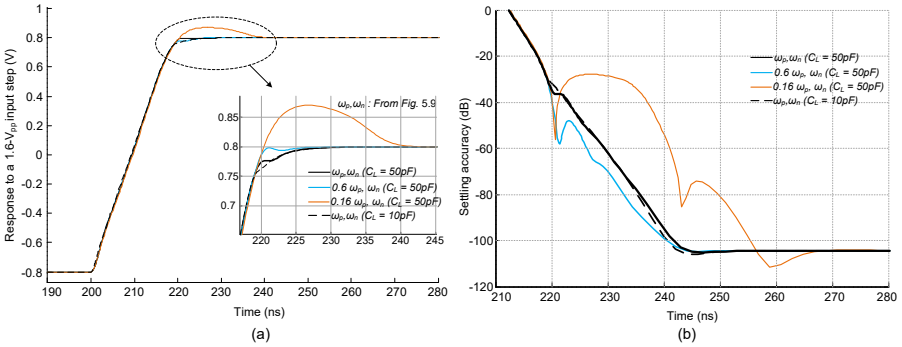

Fig. 5.10: Step-response showing the effect of the slow settling component for varying loop-bandwidths when the load equals 50 Ω || 50 pF.

gain frequency. It is therefore desirable to minimize the double spacing. In this amplifier there exist three instances of a closely placed pole and zero. As shown for the first time in section 5.2.1, a pair of doublets is encountered in the open-loop transfer of the gain-boosted stage. In the scenario where $\omega_{zn} = \omega_{zp}$ the first doublet-spacing equals zero and the transfer function represents that of a single gain-boosted stage loaded with an ideal current source. The second doublet can therefore be placed according to eqn. 5.16 by trimming the bandwidth of the gain-boost loop. The third closely spaced pole-zero pair is the zero produced via R_z and C_C that, as explained in Section 5.2.2, offsets P_3 arising from the second stage. Designing P_3 to lie beyond the unity gain frequency mitigates the impact of this doublet on the settling performance.

The effect of the twin-doublets arising from complementary gain-boosting is shown via simulation. Consider the step-responses shown in Fig. 5.10. The black curve corresponds to the implemented amplifier having the frequency response shown in Fig. 5.9. The onset of the slow-settling component is seen at 220ns, in Fig. 5.10b. The effect of the slow-settling component on the total settling time is truly small. When the load capacitance is reduced from 50 pF to 10 pF, the slow-settling component further diminishes as seen from the dotted-black curve due to the increase in the amplifier's unity-gain bandwidth. The settling accuracy in either case equals the amplifiers open-loop gain of ~100 dB. The effect of the slow-settling

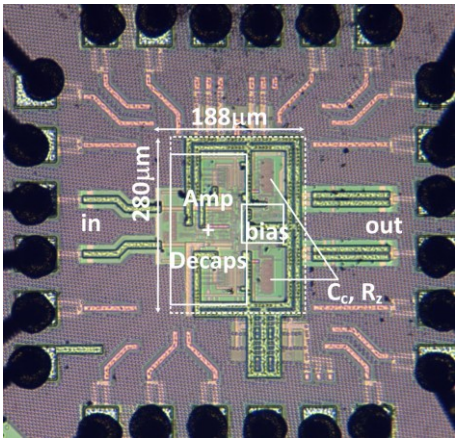

Fig. 5.11: Chip micrograph of the prototype amplifier. The amplifier occupies an active area of 0.052mm^2.

components magnify when the doublets shift to a lower frequency. The orange curve in Fig. 5.10 corresponds to reduction in ω_{zp} by a factor of 0.16 (6x increase of C_p on APMOS of Fig. 5.2). The blue curve with circles in Fig. 5.9 shows the small-signal transfer of the PMOS gain-boost loop with the reduced gain-boost bandwidth. The zero in the boosted impedance is now introduced prior to the unity-gain bandwidth. Since ω_{zp} and ω_{zn} no longer correspond to the same frequency, the first doublet comes into play as well. The 6x increase in capacitance is an exaggerated example that shows the severe impact a low-frequency doublet can have on the frequency response. However, the amplifier's sensitivity to variation in the gain-boost loop bandwidth is fairly low, as is seen from the blue curve of Fig. 5.10a and 5.10b, wherein a 30% change in capacitance produces a negligible difference in the settling time.

5.4 Stand-alone characterization of the class-AB amplifier

Measurements characterizing large-signal operation, stability, noise and distortion of the amplifier when configured for unity gain are presented in this section. The annotated chip micrograph of the 0.052-mm^2 prototype is shown in Fig. 5.11. The die is mounted on a custom designed test board and configured for unity voltage

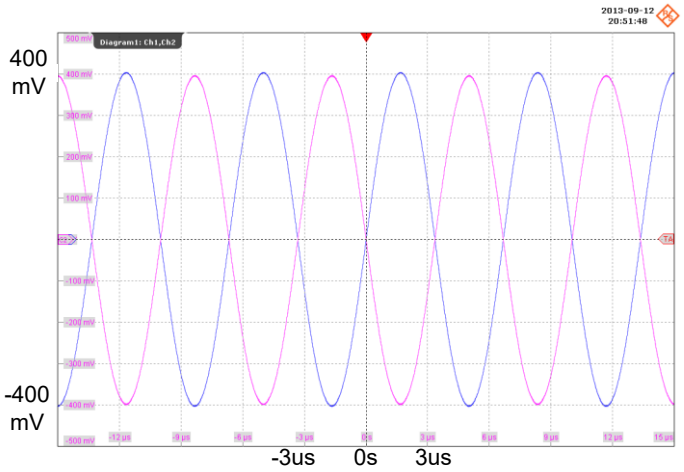

Fig. 5.12: Large-signal response for an 800mV$_{pp}$ input at 150 kHz.

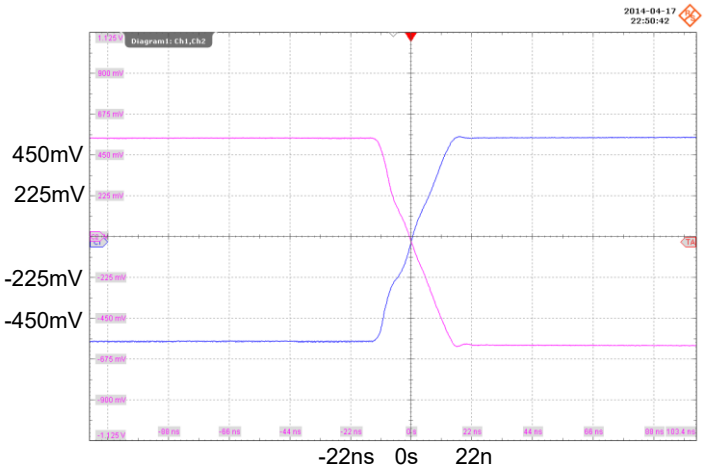

Fig. 5.13: Response to 1.2V input step (Y_{load} = 0.02 + jω50e^{-12}S).

gain initially (i.e., worst-case stability) using input and shunt feedback resistances of 10 kΩ (see Fig. 5.7b). No feedback capacitance is added.

The differential, large-signal response to a 1.6 V_{pp} input at 150 kHz applied via a balun is shown in Fig. 5.12. The output is measured on a 50-Ω oscilloscope. A 50-pF capacitor loads each output in addition to loading by 0.3m of interconnect cable and the oscilloscope's input capacitance. Each output swings symmetrically about the 600-mV_{DC} operating point set by the CMFB loop (V_{DD}=1.2V).

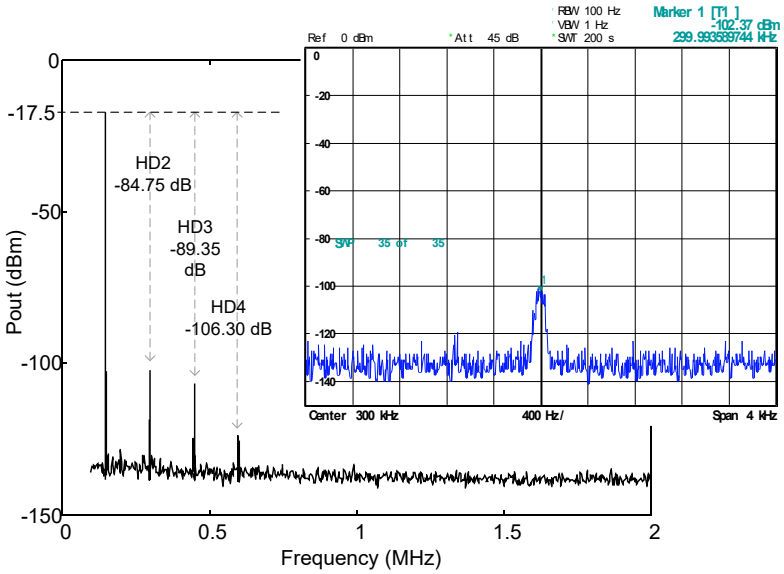

Fig. 5.14: Output distortion and noise for Y_{load} of 0.02 + jω50e^{-12} S at 150 kHz.

The amplifier response to a 1.2-V (differential) input step sourced from two arbitrary waveform generators for a load admittance of 0.02+jω50e^{-12} S is shown in Fig. 5.13. The response has an overshoot of 1.1%, which corresponds to a damping factor of 0.82 assuming a two-pole system. Slewing characteristics are limited by the second stage in this design. The slew-rate is 42 V/μs (rising) and 44 V/μs (falling), and does not vary with Q-point current in the class-AB arm and C_{load}. A stable step response is observed for loads as low as 8 Ω at each output. However, output distortion increases with the reduction in load impedance.

The output distortion for a 1.6- V_{pp} input at 150 kHz, and the measured driver noise floor (input shorted) are shown in Fig. 5.14. The distortion is measured with a balun at the output. Even-order harmonics are suppressed by differential operation, however, they arise at the output due to: 1) phase inaccuracies of the input and output baluns, and 2) g_m mismatch between the signal paths. The THD+N when each output swings to 70% of V_{DD} is -82.6dB for Y_{load} = 0.02+ jω50e^{-12}S. The THD for a 16-Ω load (same load capacitance) drops to 77 dB due to the lower loop gain and increased current drive required from the output stage with a reduced load.

Table 5.1: Measurement summary of the fully differential Class-AB amplifier

65-nm CMOS Amp.	V_{DD} (V)	R_L/C_L (Ω/F)	R_z, C_c (Ω, pF)	UGB (MHz)	Q_{point} I_{DC} (mA)	V_{out} (V_{pp})	S.R. (V/μs)	THD+N/freq (dB/kHz)	Overshoot, Damping fact.
High Power*	1.2	50-8/50p	850, 0.52	110	3.9	1.6	42	-82.6/150	1.1%, 0.82
Low Power*	1.2	50/10p	850, 0.52	75	0.8	1.6	42	-74/150	1.4%, 0.80
*The difference b/w the high and low power configurations is the current in the Class-AB arm, and load drive ability.									

Table 5.2: Comparison of class-AB driver amplifiers

Ref, CMOS technology	V_{DD} (V)	R_L / C_L (Ω/F)	C_{comp} (pF)	Q_{point} P_{diss} (mW)	V_{out} (V_{pp})	S.R. (V/μs)	THD+N/freq (dB/kHz)
[5.3], 130nm	1.2/2	16/1n	14	1.2§	1.6	0.4	-84/1
[5.14], 65nm	2.5	16/12n	35	12.5§	1.85	n/a	-68/1
[5.15], 0.18μm	1.8	–/0.24p	n/a	3.6*	2.4*	6k+	n/a
This work, 65nm	1.2	50/50p	0.52	4.7*	1.6*	42	-82.6/150
§ Single ended * Differential +Mentioned spec.							

When the amplifier is biased at 800 μA (using V_{bn} and V_{bp}) the THD drops to 74 dB. The drop in loop gain is explained from the curves in Fig. 5.5 that show dependence of gain on current consuption. Distortion tones are measured from multiple sweeps at a 75-kHz (f_0/2) spacing around a 5-kHz span (sweep time of 200 s at 100-Hz resolution and an average of 35 sweeps each) using a R&S FSUP spectrum analyzer up to the 10th harmonic. A fundamental frequency of 150 kHz was chosen to minimize the resolution requirement (for dynamic range) and time of measurement. An attenuation of 25 dB added in the signal path minimizes distortion contributed by the analyzer. The signal source distortion is suppressed using a custom designed 10th-order Chebychev LC filter. Characterization of the on-board filter implemented using discrete components show an 80-dB suppression of the second harmonic at 300 kHz.

The measurement summary of the amplifier for high-power and low- power settings is given in Table 5.1. The difference between the two settings is the power

dissipated in the Class-AB arm, and therefore the low-impedance drive capability. The slew rate is limited by the second stage and remains relatively unchanged when the current-bias of the Class-AB arm is changed. In Table 4.2 the amplifier's performance is compared with low-impedance class-AB audio drivers [5.3] and [5.14], and a switch-mode fully-differential class-AB amplifier designed for a 50-Ms/s ADC [5.15]. Owing to differential operation and the wide bandwidth requirement, it consumes more power than the audio amplifier example in [5.3]. This results in a higher slew rate and comparable distortion at an increment of two frequency decades. The single-ended design in [5.3] uses level shifting, while this work is a fully-differential low-impedance driver operating from a 1.2-V supply. An output swing in excess of the operating supply voltage is obtained through differential operation.

5.5 Summary and conclusions

A wideband, fully-differential class-AB baseband amplifier capable of driving low impedance loads is presented. The operating point is stabilized by a continuous-time common-mode feedback loop. The 3-stage amplifier when operated from a 1.2-V supply (nominal for 65-nm CMOS) delivers an output swing comparable to other published works operating from higher supply voltages with a 42-V/μs slew rate, while differential operation suppresses cross-over distortion arising from Class-AB operation. In this chapter, a detailed small-signal analysis of the amplifier stages was presented, and calculations verified against simulation. Insight into the presence of an additional doublet in a complimentary gain-boosted folded cascode amplifier is presented, and design measures to overcome degradation in settling behavior described. The Monticelli bias cell was analyzed for feedback gain and its impact on the frequency response was studied and verified against simulation. The amplifier topology was prototyped in 65-nm CMOS and measurements confirmed stability and operation over varying load conditions.

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Chapter 6 – Transformer-coupled hard-limiting oscillator

In this chapter, the design, analysis and measurement of the hard-limiting oscillator prototype in 65-nm CMOS [6.1], [6.2] is described. It is shown that phase insensitivity to noise created via transformer-coupled hard-limiting enables the design of a high-power, low-phase-noise oscillator for the GSM-BTS specification (derived in Section 1.2), with a power efficiency that's comparable with state-of-the-art designs for GSM handsets.

6.1 The oscillator concept

A simplified schematic of the proposed hard-limiting oscillator [6.1], [6.2] is shown in Fig. 6.1, where C_2 and C_3 model the average non-linear capacitances seen at the respective ports during large-signal operation. Positive feedback is realized between the drain and gate terminals of M_1 and M_2 using 1:2 step-up transformers T_1 and T_2. Separate, wideband transformers provide greater common-mode rejection, and ensure that the voltage gain needed to overdrive the transistors for hard-limiting the output is adequate. The transformers also control the impedances seen by the transistors at the drain and gate interfaces, and promote greater frequency stability in the loop than an LC tank equivalent. Before discussing circuit design details and operation, the concept is evaluated for its potential as a low-phase-noise oscillator and to define limitations on the phase noise imposed by the circuit in practice.

The linear time-variant phase noise model [6.3] detailed in Section 2.6.4 describes an impulse sensitivity function (ISF) that quantifies the sensitivity of the oscillating waveform to perturbations at different time instances within one cycle. It is used to analyze the phase noise of the oscillator design concept in this section. The ISF (Γ), periodic with the same frequency as the time-domain voltage across the tank, has regions of maximum and minimum sensitivity. This knowledge motivates the consideration of waveshape as a potential design degree of freedom to optimize the trade-off between phase noise and power consumption.

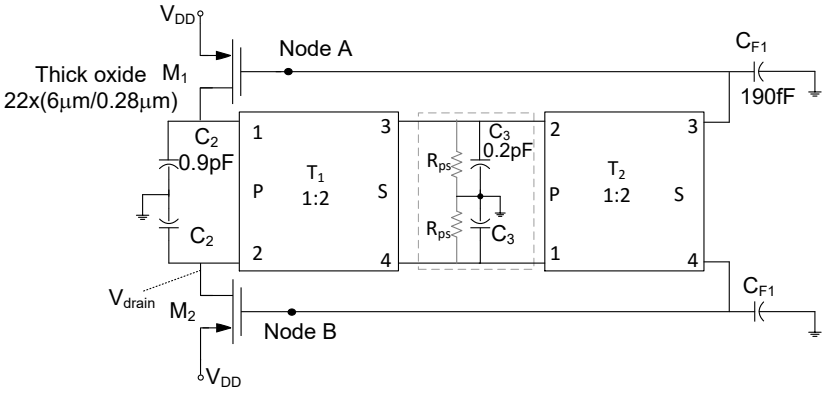


Fig. 6.1: Simplified oscillator schematic. Design values of the implemented step-up transformers T_1 and T_2 are shown in Fig. 6.4.

The impact of waveshape on the conversion of circuit noise to phase noise is exploited in this work. It has been explored previously in a single-ended common-base oscillator designed for the DCS-1800-BTS specification presented in [6.4], where BJT devices are voltage-biased to steepen the slope around waveform zero-crossings. Steepening of the slope implies that the approach to – and departure from – the point of maximum noise sensitivity is faster. Phase noise generated in the vicinity of this point is therefore reduced. Increasing the output amplitude of the cross-coupled oscillator within the current-limited region of operation also achieves this goal to some extent. The tank in [6.5] is designed for dual resonance at the fundamental and third harmonic, while in [6.6] an auxiliary circuit tuned to the 3rd harmonic increases the slope around the zero-crossing to lower the phase noise.

6.2 Theoretical analysis

Following the theory developed in [6.3] and [6.7], the phase noise of an oscillator is determined by the periodic phase-noise conversion of individual noise contributions. In the following analysis each noise source is approximated with a constant power-spectral density during one oscillation period. This assumption is valid for passive networks; however, transistors in non-linear oscillators traverse different operating modes, which force a time-varying treatment of noise-sources that is cumbersome. The approximation is qualified during the analysis of the proposed oscillator, as it

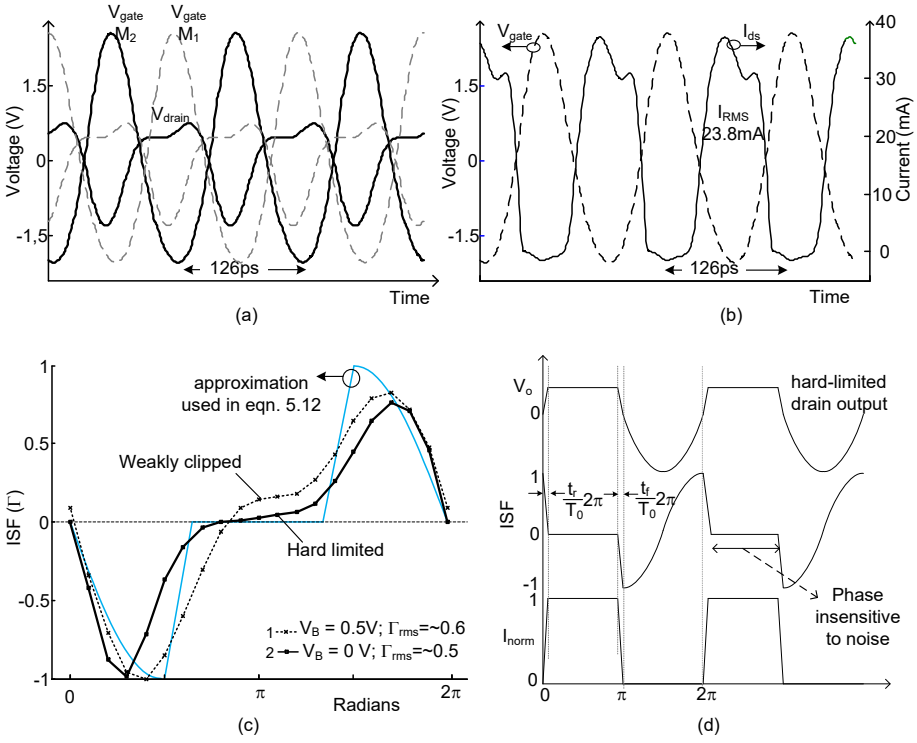


Fig. 6.2: (a) Transient simulation results at 8 GHz for V_B = 0 V and V_{DD} = 1.5 V at the gate and drain of $M_{1,2}$, for the circuit of Fig. 6a (b) transient gate voltage and drain current of M_1 for V_B=0 V, (c) ISF simulated by injecting a 100uA current impulse for V_B=0.5 V and 0 V, and (d) approximations of the transient waveforms and the ISF.

will be shown that the transistors operate largely between triode and cut-off. The phase noise contribution of each noise source is approximated by its ISF that is obtained via the phase-shift induced by an infinitesimal impulse of charge injected at different instances within one cycle. The oscillator's phase noise $L(\Delta\omega)$ from Section 2.6.4 equals:

$$L(\Delta\omega) = 10\ log\left[N\frac{\sum_i S_i}{2q_{max}^2\Delta\omega^2}\right], where \tag{6.1}$$

$$S_i = \frac{1}{2\pi N^2}\int_0^{2\pi} \Gamma_i^2(\phi)\overline{i_i^2}(\phi)\,d\phi. \tag{6.2}$$

In eqn. 6.1 S_i is the contribution of the i^{th} noise source, q_{max}^2 is the maximum charge

in the resonator, and $\Delta\omega$ is the frequency offset in radians/s. N, the number of stages, equals 2 for a differential circuit.

Results showing the amplified gate drive and clipped drain voltage swing from Spectre-RF^{TM} transient simulations of the oscillator prototype are shown in Fig. 6.2a for a 0-V gate bias voltage, V_B (detailed in Fig 6.5). The corresponding square-wave current flowing through the transistor is shown in Fig. 6.2b, and the impulse sensitivity function (ISF) of the prototype circuit is shown in Fig. 6.2c. The ISF was simulated through 100-uA impulse injection for V_B equal to 0.5 V and 0 V. Overdriving the gate ensures that the output is hard limited, thereby creating a region of insensitivity to all circuit noise sources close to π radians in duration where the ISF is approximately zero. Since the ISF is related to the time-domain voltage, the freewheeling tank waveform when the transistors are cut-off is the source of the sinusoidal portions seen in the ISF, while imperfect switching of the transistors causes slewing that characterizes the remaining portions of the ISF cycle. It will be seen from the following analysis that circuit noise is more likely to be converted to oscillator phase noise during these transitions than at any other part of the oscillation cycle. Minimizing these transition times is therefore important to the realization of an oscillator with low phase-noise performance.
For the brief fractions of the oscillation period (T_0) when the output is slewing with finite rise and fall times t_r and t_f, the variation of the impulse sensitivity function can be approximated as a linear relationship. The ISF, $\Gamma(\phi)$, is further approximated by a cosine function in interval $[\pi<\phi<2\pi]$ when the transistors are switched off. In the interval $[0<\phi<\pi]$ when the transistors are switched on, the output is clipped and the ISF approaches zero.

Based on the above description the ISF is decomposed into three components that are characterized by the freewheeling tank-waveform when the transistors remain cut off (cosine), output slewing during transitions from cut-off to triode and vice versa (linear), and phase insensitivity created by hard-limiting the drain waveform (flat). The approximation and the ISFs obtained from circuit simulation are compared in Fig. 6.2c. It is clear that varying the boundaries between the three

regimes for the approximation can give a satisfactory fit to the simulated ISF. The mathematical approximation is used to develop an expression for the oscillator's phase noise. Equations describing the regimes captured by the approximate ISF are given by:

$$\Gamma(\phi) = \begin{cases} 1 - \dfrac{\phi}{(t_r/T_0)2\pi} & ; \quad 0 < \phi < \dfrac{t_r}{T_0}2\pi \\ 0 & ; \quad \dfrac{t_r}{T_0}2\pi < \phi < \pi - \dfrac{t_f}{T_0}2\pi \\ \dfrac{\pi - \phi}{(t_f/T_0)2\pi} - 1 & ; \quad \pi - \dfrac{t_f}{T_0}2\pi < \phi < \pi \\ \cos(\phi) & ; \ \pi < \phi < 2\pi \end{cases} \tag{6.3}$$

The noise contribution of the tank in a 1Hz bandwidth is:

$$\overline{i_{n,tank}^2} = \frac{4kT}{R}, \tag{6.4}$$

where R is the equivalent resistance shunting the tank at resonance. Substituting eqns. 6.3 and 6.4 in eqn. 6.2 gives the tank-noise-contribution:

$$S_{tank} = \frac{1}{2\pi N^2}\frac{4kT}{R}\left[\int_0^{\frac{t_r}{T_0}2\pi}\left\{1 - \frac{\phi}{(t_r/T_0)2\pi}\right\}^2 d\phi + \int_{\pi-\frac{t_f}{T_0}2\pi}^{\pi}\left\{\frac{\pi - \phi}{(t_f/T_0)2\pi} - 1\right\}^2 d\phi + \int_{\pi}^{2\pi} cos^2(\phi)d\phi\right], \tag{6.5}$$

$$S_{tank} = \frac{kT}{R}\left[\frac{t_r + t_f}{3T_0} + \frac{1}{4}\right]. \tag{6.6}$$

During the transients (rise and fall) the transistors transition from cut-off, through saturation, to the onset of the triode region. In the analysis of transistor noise during t_r and t_f the maximum noise in triode is assumed:

$$\overline{i_{n,MOS}^2} = 4kT\gamma g_{d0}, \tag{6.7}$$

where γ equals the excess noise factor of a single MOS transistor and g_{d0} is the output conductance of the transistor when V_{ds} equals zero. Since the source of the PMOS transistors is grounded (i.e., no tail current source), the impulse sensitivity function in eqn. 6.3 can also be used to determine the ISF of the MOS transistors, Γ_{MOS}, [6.3]:

$$\Gamma_{MOS} = \Gamma(\phi) \cdot \alpha(\phi). \tag{6.8}$$

The function $\alpha(\phi)$ defines the periodicity of the noise source determined by transistor switching (since the transistors add current and noise only in the on-state). It can be approximated closely by:

$$\alpha(\phi) = \begin{cases} 0\ ; & 0 < \phi < \pi \\ 1\ ; & \pi < \phi < 2\pi \end{cases} \tag{6.9}$$

Using eqns. 6.2, 6.3 and 6.9, the phase-noise contribution from transistors can be written as:

$$S_{MOS} = \frac{4KT\gamma g_{d0}}{2\pi N^2}\left[\int_0^{\frac{t_r}{T_0}2\pi}\left\{1 - \frac{\phi}{(t_r/T_0)2\pi}\right\}^2 d\phi + \int_{\pi-\frac{t_f}{T_0}2\pi}^{\pi}\left\{\frac{\pi-\phi}{(t_f/T_0)2\pi} - 1\right\}^2 d\phi\right], \tag{6.10}$$

$$S_{MOS} = KT\gamma g_{d0}\left[\frac{t_r + t_f}{3T_0}\right]. \tag{6.11}$$

For N=2, the total phase noise of the oscillator is obtained by substituting eqns. 6.6 and 6.11 into eqn. 6.1 and equals:

$$L(\Delta\omega) = 10 \cdot log\left[\frac{KT}{C^2V_o^2\Delta\omega^2}\left\{\frac{1}{R}\left(\frac{t_r + t_f}{3T_0} + \frac{1}{4}\right) + \gamma g_{d0}\left(\frac{t_r + t_f}{3T_0}\right)\right\}\right]. \tag{6.12}$$

The maximum charge is represented as a product of capacitance (C) and peak single-ended fundamental swing V_0. Eqn. 12 reveals that the phase noise is a strong function of the transistor switching times. Assuming that the rise and fall time (t_r and t_f) of the current transient as well as the clipped drain voltage are negligible so that the transistors switch instantaneously between on (triode) and off-state with $t_r = t_f$ equal to zero, the oscillator phase noise from eqn. 6.12 simplifies to:

$$L(\Delta\omega) = 10 \cdot log\left[\frac{KT}{4C^2V_o^2\Delta\omega^2R}\right]. \tag{6.13}$$

The result of eqn.6.13 suggests that the transistors are eliminated entirely as sources of phase noise as their switching times diminish to zero, leaving the effective phase noise of the oscillator dependent only upon feedback network losses. It is important to note in the treatment of eqns. 12 and 13 that the output swing cannot be replaced simply by the product of transistor current and R, since the low output impedance of the transistor loads the tank during the on-state (i.e., when $0<\phi<\pi$). However, the

potential penalty in phase noise from the transistor being in triode is negated because the ISF is zero in this interval (as seen from Fig. 6.2c and 3d). As a result, noise generated by the transistor outside of the switching transitions does not contribute to the oscillator phase noise, as seen from comparison of eqns. 6.12 and 6.13. While hard-limiting the output and operation in triode is counter-intuitive to oscillator design, the oscillator insensitivity to noise under these conditions overcomes the apparent drawbacks. However, ideal switching cannot occur in practice. The dramatic gate over-drive generated by the two-transformer feedback, in this regard, plays an important role in minimizing the rise and fall times, thereby reducing oscillator phase noise. The phase noise predicted by eqn. 6.12 is verified against simulation results in the next section of this chapter.

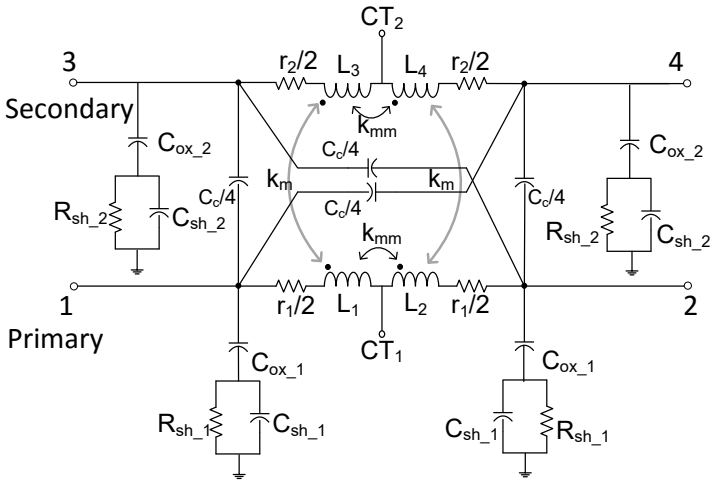
6.3 Circuit design and operation

The operating frequency (7.8 GHz) is chosen to minimize the area associated with the 2-transformer layout, as the target bands of 1.8 GHz and 900 MHz can be easily reached using inductorless frequency dividers. PMOS devices are preferred for their approximately 15% lower *1/f*-corner at the same g_m in the 65-nm CMOS process.

6.3.1 Transformer feedback network

Common-mode rejection in the feedback path of the oscillator is ensured through tight magnetic coupling between the primary and secondary windings of each transformer (i.e., high k_m), which minimizes the transformer leakage inductance [6.8]. A low-impedance path to ground at the center-taps of the 1:2 turns ratio planar transformers is also added to shunt common-mode signals away from the differential signal path. This ensures minimum gain in the common-mode, while differential start-up and operation prevail. A stack of the top and second (from the top) 0.9-um thick Cu metals and the 1.4-um thick Al-cap layer are used to construct the transformers. Self-inductances of the primary and secondary are 0.5 nH and 1.25 nH, respectively, and k_m equals 0.748.

A lumped-element circuit model of each 1:2 transformer used in the oscillator circuit of Fig. 6.1 is shown Fig. 6.3. The component values listed in Fig. 6.3 are obtained



Component	Value	Component	Value
L_1, L_2	250pH	C_{sh_1}	17.75 fF
L_3, L_4	612.5pH	C_{sh_2}	25.75 fF
k_m	0.748	C_{ox_1}	48 fF
k_{mm}	0.0175	C_{ox_2}	80 fF
r_1	1.34 Ω	C_c	19.8 fF
r_2	2.82 Ω	R_{Sh_1}, R_{sh_2}	16 Ω

Fig. 6.3: Lumped equivalent model of the 1:2 feedback transformers shown in Fig. 6.1.

by fitting 4-port parameters of the model to full-wave EM simulation data for the transformer layout. Transmission peaks in the frequency response of the two-transformer cascade used in the feedback network are spread farther apart by maximizing primary-to-secondary coupling, k_m. Stagger tuning of the transformers (i.e., tuning the secondary lower than the primary, such that $\omega_{secondary}/\omega_{primary}<0.8$) is also used to suppress the loop-gain at the non-dominant frequency peak and ensure a stable oscillation at the desired frequency. The magnitude response of the feedback network stand-alone (from the drain side) is shown in Fig. 6.4a, and has a dominant peak at 10.3 GHz with an impedance of 205 Ω. Good agreement is seen between the response of the feedback network predicted from EM simulation and the lumped-element equivalent circuit of Fig. 6.3.

Transistor parasitics and the switched-capacitor tuning network (see Fig. 6.5a) shift the resonant frequency down to 8 GHz in the final oscillator prototype. Seen from

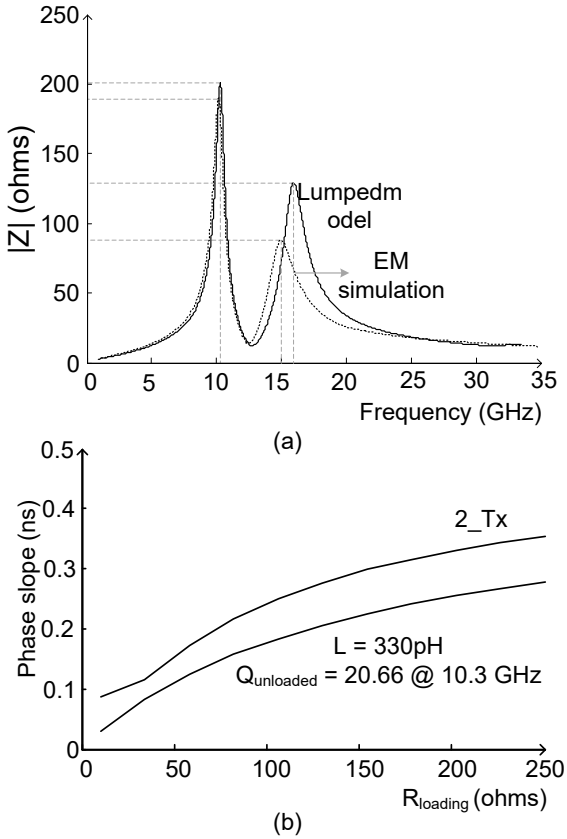


Fig. 6.4: (a) Magnitude response seen from the drain side of the lumped model and EM simulation of the two transformer cascade, when loaded with the capacitor values indicated in Fig. 6.1, (b) Slope of the phase response at resonance for varying loads (2-Tx vs. inductor equivalent from EM simulation for the CMOS technology).

the transistor drain side, the effective capacitance loading the tank is ~1.2 pF. A shunt loading of 1 kΩ is assumed across the T_1-T_2 interface to model switch losses (see Fig. 6.1). The magnetizing inductance seen at the input of the two transformer cascade is 330 pH. The real part of the shunt equivalent impedance seen between the drain terminals at 8 GHz resonance is 130 Ω for the implementation of Fig. 6a. The single-ended load seen at each drain is therefore one-half of this impedance, or R of 65 Ω and C of 2.4 pF as defined previously for eqn. 12 in Section 6.1.

In an oscillator designed for a high output swing, transistor operation in triode across a part of each cycle and consequent loading of the feedback network is inevitable.

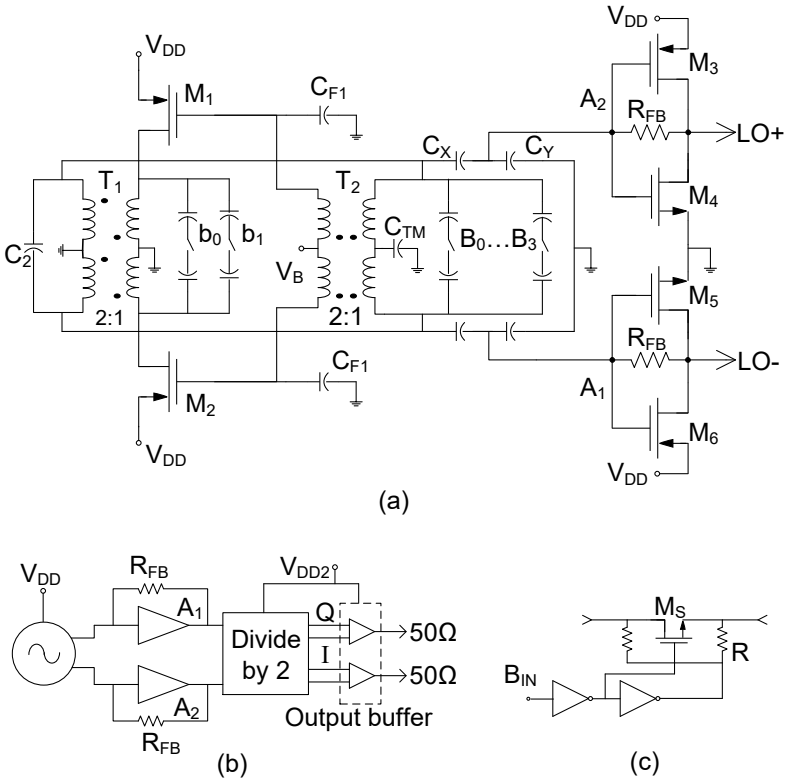


Fig. 6.5: (a) Detailed circuit diagram of the implemented oscillator and interface buffers $A_{1,2}$, (b) block diagram of the test IC, and (c) the digital switch.

Tank loading affects the selectivity of the feedback network in an oscillator resulting in lower output amplitude, and the phase noise seen at the oscillator's output necessarily increases with greater loading. Selectivity of the 2-transformer feedback network can be gauged easily by observing the rate of change in phase with respect to frequency (i.e., the phase slope). Similarly, the slope of the phase response at resonance for a parallel LC resonator increases with increasing tank Q-factor [6.9]. The phase slope of the impedance at resonance when the transformer feedback loop is broken at the gate (nodes A and B indicated in Fig. 6.1) and loading at the drain is varied between 10 Ω and 250 Ω in 10 equal steps is plotted in Fig. 6.4b from simulation. A single-LC tank at resonance is also simulated for comparison. The inductance assumed is equal to the magnetizing `inductance of the cascaded

transformer network (i.e., L_{tank} =330 pH), with loading due to tuning switch losses (1-kΩ shunt resistor) for a fair comparison. The unloaded inductor has a Q of 20.66 at 10.3 GHz and is resonated using an ideal 1.2 pF capacitor. For a loading of 150 Ω at the drain side (Fig. 6.4b), the Q factor of an inductor that would give the same phase slope with frequency as the 2-transformer cascade is 10.7 compared to 7.64. The two-transformer cascade has a greater slope in the phase response – and hence higher frequency selectivity – than an equivalent LC tank at resonance for all loading values simulated (see Fig. 6.4b). The increase in impedance seen from drain to gate is therefore expected to reduce the loading effect on frequency selectivity of the feedback network when the transistor enters the triode regime (i.e., in the *on* state) in the oscillator prototype. Thus, the two transformer cascade provides a large-signal voltage gain of ~3 that overdrives the transistor output into clipping, with better selectivity than a conventional tank.

6.3.2 Design details and circuit operation

The oscillator is prototyped in a production 7-metal 65-nm bulk-CMOS process with no thick-metal option [6.10]. A detailed schematic of the oscillator is shown in Fig. 6.5a, and a block diagram of the implemented IC in Fig. 6.5b. The DC bias of $M_{1,2}$ (V_B at center-tap of T_2 in Fig. 6.1) sets the bias current at start-up, which determines the amount of resonator charge during stable oscillation. The fundamental tone excites the secondary winding of T_1, while harmonics are shunted to ground through MOM capacitors C_2. The gates of $M_{1,2}$ are driven from T_2, which steps-up the filtered waveform for a peak-to-peak swing as high as $3.5V_{DD}$ at each gate. Transistors $M_{1,2}$ are 22×(6 µm/0.28 µm) thick-oxide devices that withstand the large gate swing without breakdown and reduced parasitic overlap capacitances compared to thin-oxide equivalents. Lower gate-to-drain capacitance (C_{gd}) during large-signal operation is beneficial, as loading seen at the transistor drain is approximately $(1+n^2)C_{gd}$ due to signal attenuation from gate to drain, where n is the turns ratio of a single transformer.

The output from the oscillator core is taken via a capacitive tap (C_X, C_Y) to minimize loading of the buffers $A_{1,2}$ interfacing the oscillator to a dynamic frequency divider.

Their power consumption and feedback resistance can be traded for gain, bandwidth and reverse isolation. The divider output is interfaced to the single-ended 50-Ω measurement equipment using a differential pair with a transformer-balun load. Separate analog and digital supplies (V_{DD} and V_{DD2}, respectively) maximize isolation between the circuit blocks. Separate on-chip meshes for analog and digital ground provide additional isolation.

Four switched MOM-capacitors (B_0-B_3) provide simplified frequency tuning at the interface of T_1 and T_2 (Fig. 6.5a). Control bits b_0-b_1 fine tune the impedance at the secondary of T_1, as the change in impedance is reflected at the output attenuated by a square of the turns ratio. The resistance of the switching element determines the Q of the capacitor bank, and a trade-off between parasitic capacitance and on-resistance (r_{on}) is encountered with respect to its sizing, as described in [6.11]. In the switch (shown schematically in Fig. 6.5c), biasing via the resistors ensures a negative gate-source voltage in the off-state, and minimum r_{on} when on. The drain bias during the off-state is set to V_{DD}, which provides better control over the reverse biased drain-bulk junction capacitance, while reducing signal leakage through the drain-bulk junction [6.12]. The inverters do not consume static power and occupy little area.

Fig. 6.2a shows the simulated transient response at the transistor drain and gate for V_B equal to 0 V, where the total steady-state current consumption is 33.65 mA from 1.5 V. Tuning bits b_0, b_1, B_1 and B_2 are set to 1. The output is clipped, and the rise and fall transients cumulatively occupy ~15% of the oscillation period. The fundamental component appearing at the drain is 0.85 V_{peak}. The result of a transient simulation showing i_{ds} and the gate-voltage swing of M_1 is shown in Fig. 6.2b. The large gate-drive obtained through cascaded transformers T_1 and T_2 (~3 V_{DD} peak-to-peak) forces the transistors to switch rapidly between triode and cut-off. This is a key attribute of the switching hypothesis discussed in Section 5.1. The electric field at the drain drops with decreasing V_{sd} (for the PMOS transistor), and the drain output voltage is clipped when the channel cannot conduct more current. Gate overdrive causes sharp transients at the drain (i.e., small t_r from Fig. 6.2a), and it ensures that

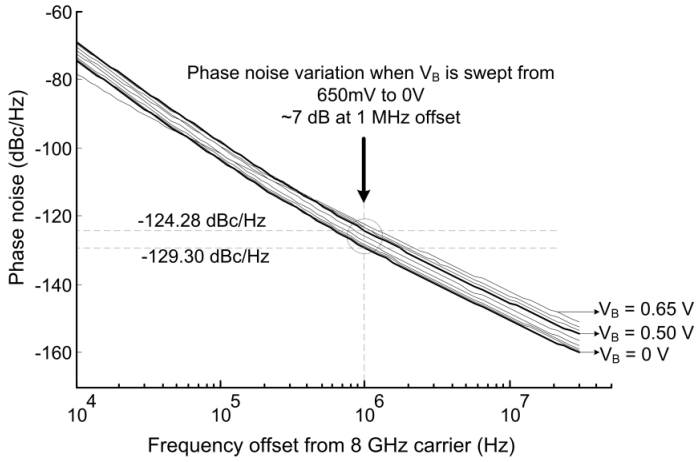


Fig. 6.6: Spectre-RF^{TM} simulation of PN at 8 GHz, for V_B varied from 650 mV to 0 V. Phase noise improves by 5.1 dB at 1 MHz offset for V_B = 500 mV (23.4 mA) and 0 V (33.5 mA).

the devices remain cut-off while the drain swings to a minimum approaching -1.3 V ($-V_{DD}$ approximately) during the remainder of the oscillation cycle. Eliminating the tail current bias source is a deliberate design choice, as rise and fall transients accompanying hard limiting are not slew-rate limited. The transistors provide max-

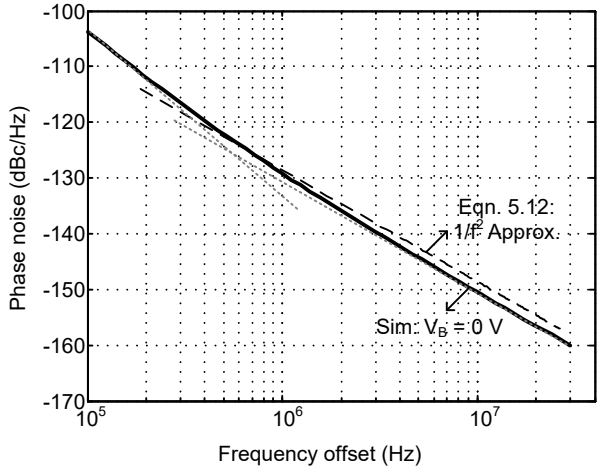


Fig. 6.7: 1/f ^{2} phase noise extrapolation vs. offset frequency using eqn. 12 (V_0 = 0.85 V_p, R = 65, C = 2.4pF and γ = 1.04), and Spectre-RF^{TM} simulation of PN for V_B = 0 V (from Fig.6.6).

-imum current during their on state, which coincides with the region where the output clips, as seen from Fig. 6.2a and Fig. 6.2b. This is necessary for low-phase-noise performance since the transistor noise contribution increases in triode [6.13]. The signal amplitude is reduced by the low output impedance in triode, but mismatch gain via transformers T_1 and T_2 restores it as described previously, yielding approximately 4.5-V_{pp} gate swing when V_B equals 0 V.

The evolution of phase noise obtained by varying V_B for the circuit shown in Fig, 6.6 when operated from a 1.5-V supply is shown in Fig. 6.6. V_B is varied from 650 mV to 0 V, and the corresponding steady-state power consumption increases from 13.65 mW (9.1 mA) to 50.5 mW (33.65 mA). The start-up current in the respective bias settings are 5.05 mA and 27.82 mA[1]. The combination of a rise in signal amplitude and noise reduction through hard limiting, contribute to a 7-dB improvement in phase noise. Of these curves, the phase noise performances for V_B set to 500 mV and 0 V (indicated in Fig. 6.6) have been analyzed comparatively. A 5-dB phase noise improvement at 1-MHz offset (-124.3 dBc/Hz to -129.3 dBc/Hz) is obtained when the current drawn by the oscillator is raised from 23.4 mA (35.1 mW) to 33.5 mA (50.5 mW). The fundamental components seen at the drain in the two cases are 0.62 V_{peak} and 0.85 V_{peak}, respectively.

6.4 Phase noise analysis vs. simulation

The phase noise predicted in the $1/f^2$-region from eqn. 6.12 is plotted in Fig. 6.7 for $V_B = 0$ along with the simulated phase noise from Fig. 6.6. The parameters derived for the oscillator prototype are: C[2] = 2.4 pF, V_0 = 0.85 V, R = 65 Ω, g_{d0} = 18.18 mS and γ = 1.04 (obtained from circuit simulation). For a given gate-amplitude, the oscillator phase noise improves as t_r and t_f are reduced, as expected. Switching time improves with technology scaling as device parasitics are reduced and the transistor

[1] In the absence of current regulation, the steady-state current consumption increases when compared to the start-up current. However, for a given bias condition and resonator losses, the maximum current consumption is determined (and limited) by the transistors' aspect ratio.

[2] The capacitance is distributed across the coupled-transformer network to optimize the impedances in the loop for maximum voltage gain. The effective capacitance of 2.4pF resonates with the 165-nH magnetizing inductance.

large-signal transconductance increases. Therefore, a further reduction in phase noise is anticipated from improvements in device technology.

The phase noise of the prototype oscillator at a 3-MHz offset (for $V_B = 0$ V) obtained from Spectre-RF^{TM} simulation is -139.6 dBc/Hz. As obtained from Fig. 6.2a and 3c, t_r and t_f occupy ~15% of the waveform period (T_0). The phase noise in the $1/f^2$ region predicted by the eqn. 6.12 in this condition is -138.2 dBc/Hz, which is 1.4 dB more than the value predicted from a simulation of the complete circuit (seen from Fig. 6.7). The difference can be attributed to the approximations made in the development of the theoretical expression of eqn. 6.12. While assuming a linear rise and fall of the drain current does underestimate transistor noise by a small margin, as stated in Section 6.2, transistor noise contribution during the rise and fall transients was assumed to be constant with a worst case value of triode noise. The coarse approximation of the cosine portion of the ISF in the interval $[\pi<\phi<2\pi]$ overestimates tank noise as is evident from Fig. 6.2c.

Recall that hard limiting creates a time window where sensitivity to noise is considerably reduced and the ISF approaches zero (as seen in the simulated ISFs of Fig. 6.2c). Reducing the voltage swing at the gate nodes results in milder output clipping, as illustrated for a gate bias V_B of 0.5 V, where t_r and t_f occupy ~32% of T_0 and V_0 equals 0.62 V_p (compared to 0.85 V_p for $V_B = 0$ V, where t_r and t_f occupy ~15% of T_0). In the 0-V case, the total noise power appearing at the output drops

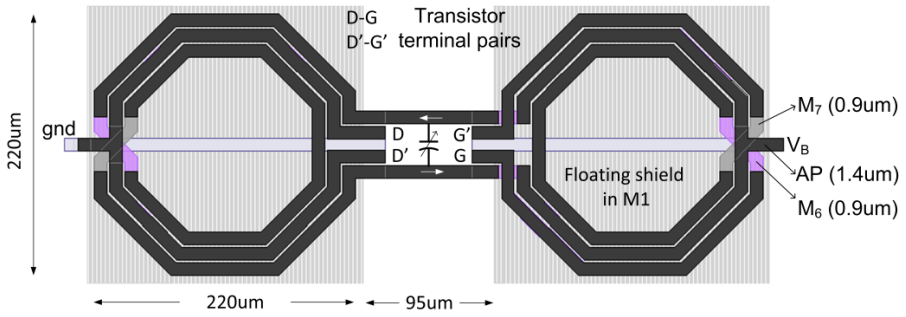


Fig. 6.8: Layout view of the two-transformer core.

with the advent of hard limiting and contributes to approximately 42% of the 5 dB improvement in phase noise, while the remaining is obtained through the increase in fundamental power.

For the phase-noise values indicated in Fig. 6.7 showing the 0-V and 0.5-V biasing cases, the rms noise powers contained in a 1-Hz bandwidth obtained via a Spectre P-Noise simulation are 4.48×10^{-14} V^2/Hz and 6.35×10^{-14} V^2/Hz, respectively. This is the rms noise power appearing between the drain of one transistor and ground. The noise contribution of the passives (half-circuit) in either case are 1.9×10^{-14} V^2/Hz and 2.8×10^{-14} V^2/Hz, respectively. For the values of t_r and t_f mentioned in the beginning of this section, the noise contribution in the 0-V and 0.5-V bias case obtained from theory are 2.1×10^{-14} V^2/Hz and 2.5×10^{-14} V^2/Hz, respectively, with a ~10%-error in either case.

6.5 Layout, frequency pushing, divider and buffer

Fig. 6.8 shows the transformer layout with frequency tuning indicated at the interface nodes between them. Each transformer is 220x220 um^2 in size. A stack of the top and second (from the top) 0.9-um thick Cu metals and the 1.4-um thick Al-cap layer are used to construct the transformers. A floating shield in metal-1 reduces substrate loss [6.14]. Transistors $M_{1,2}$ forming the oscillator core are laid out along the line of electrical symmetry.

Removing the tail current source increases the oscillator's sensitivity to supply voltage variations, resulting in frequency pushing. Fixed capacitors C_{F1} placed at the gate of each transistor reduce frequency pushing. They are 190 fF (see Fig. 6.1) each and dominate over the bias-dependent transistor parasitic capacitances at the node.

Fig. 6.9a shows the dynamic rail-to-rail digital frequency-divider producing quadrature outputs [6.15] and its transistor level implementation. Compared to source-coupled-logic (SCL) dividers, dynamic dividers can be designed to consume less power and have a lower noise floor. The circuit needs to be driven symmetrically with an amplitude that is large enough to prevent self-oscillation in

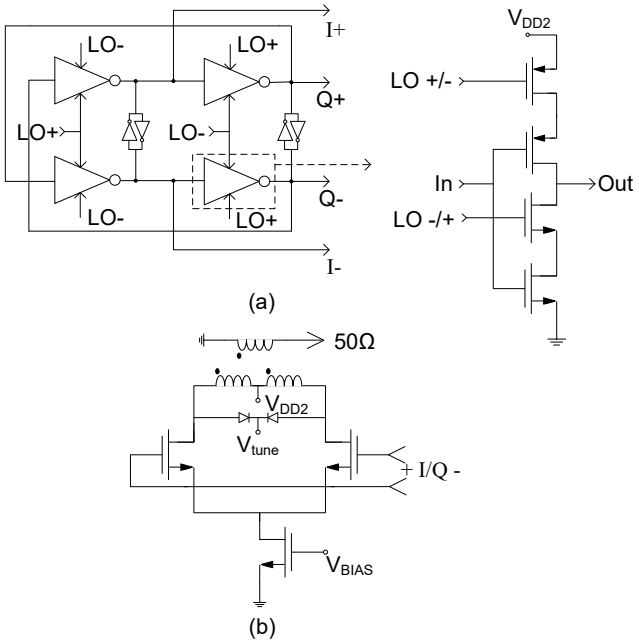


Fig. 6.9: (a) Digital frequency divider and implementation of the clocked inverter, and (b) The output buffer driving the 50Ω measurement load.

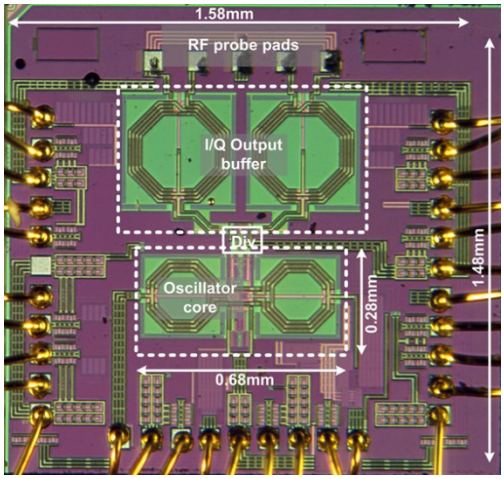


Fig. 6.10: Chip micrograph. The oscillator dimension is 0.19 mm^2 (0.68 mm by 0.28 mm). DC inputs are wire-bonded and the RF output is probed on die.

positive feedback loop. Cross-coupled inverters are used to ensure opposite polarity at the respective nodes they connect, and their gain can be designed to trade noise performance for the ability to correct phase imbalance in the input signal. The divider consumes 5 mA from 1.2 V and 6.8 mA from 1.5 V during steady-state operation. The output buffer is shown in Fig. 9b. V_{BIAS} is used to adjust the gain. The transformer provides impedance matching over a wide bandwidth, and can be tuned by via V_{TUNE}.

6.6 Measurement results

The chip is mounted and wire-bonded on a customized test board. The RF outputs are probed on die. The annotated chip micrograph is shown in Fig. 6.10, where the oscillator core (highlighted) is 0.19 mm^2.

The phase noise measured at 3.92 GHz (i.e., at the divide-by-2 output) for power consumptions of 25.8 mW and 19.2 mW from 1.2 V is shown in Fig. 6.11. The phase noise measurements taken at 1.5 V for power consumptions of 35.4, 41, 44 and 48 mW are shown in Figs. 6.12a –d. Bias voltage V_B is swept from 500 mV to 0 V, as in the simulation presented previously in Section IV. The phase noise at an offset frequency of 1 MHz improves from -129.4 to -135 dBc/Hz as the power consumption varies from 35.4 mW to 48 mW. The measured *1/f*-noise corner frequency lies between 650-700 kHz. This measurement validates simulation results and is discussed further with respect to Fig. 6.13. The new oscillator design alleviates the power consumption/phase noise trade-off significantly, especially at higher power, where the returns for an increase in power consumption are less satisfactory, since the accompanying improvement in phase noise performance diminishes. At 48-mW power consumption, the DCS-1800-BTS-Normal specification is met with 1-dB margin, while the most stringent GSM-900-BTS spec. is ~2-dB away from being satisfied. This is amongst the lowest phase noise for integrated VCOs from reports in the recent literature, as discussed in the comparison later in this section.

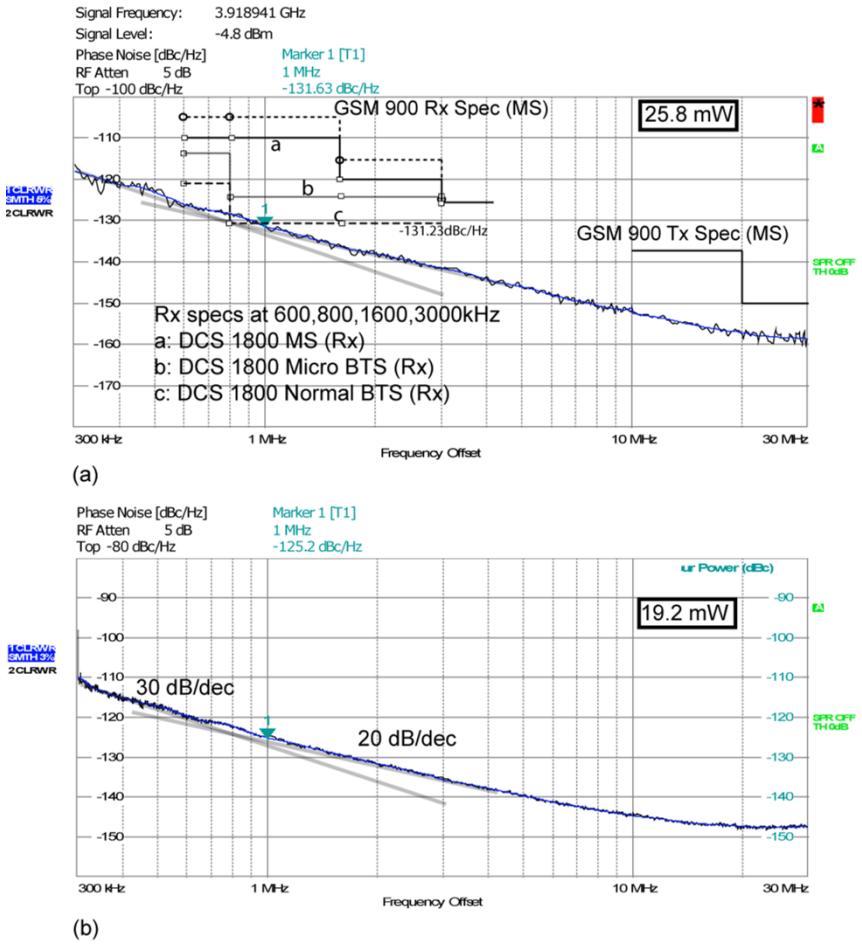
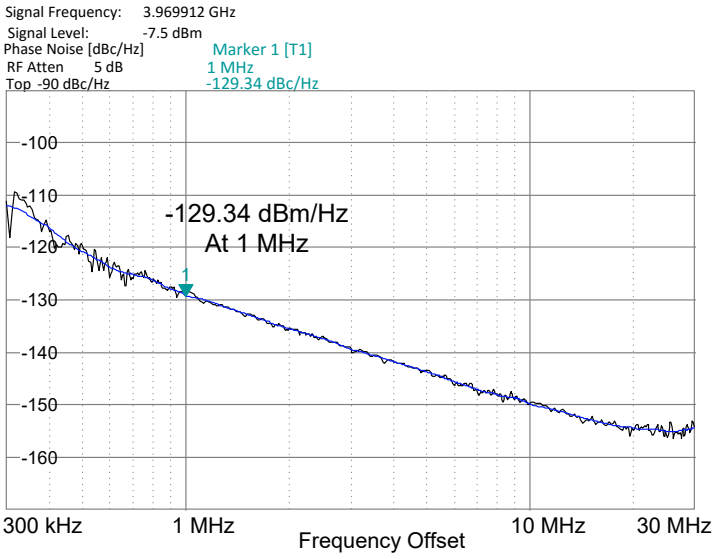
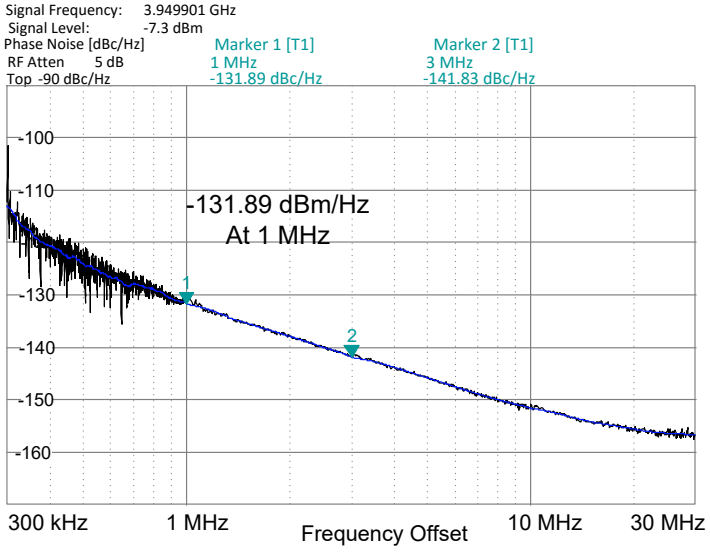


Fig. 6.11: Phase noise measured at 25.8 plot (a) and 19.2mW (b), when operated from 1.2V. The GSM/DCS Mobile (MS) and Base station (BTS) specifications are normalized to the 3.92 GHz carrier frequency.

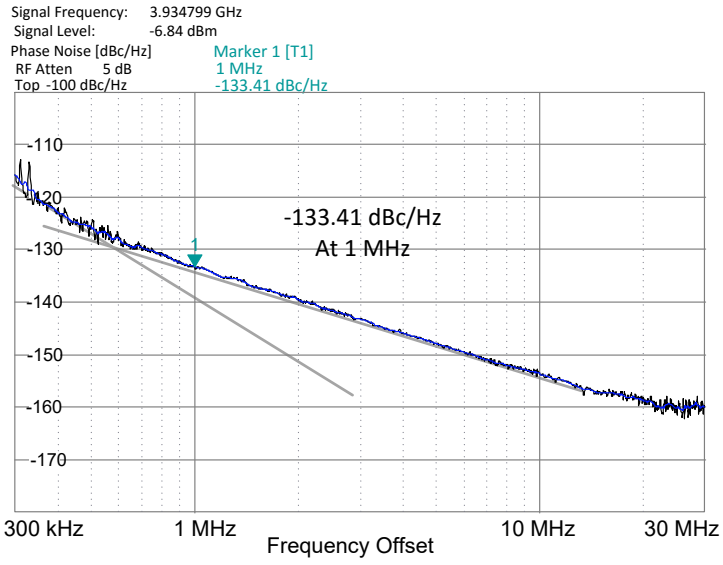


(a) V_B = 0.5 V

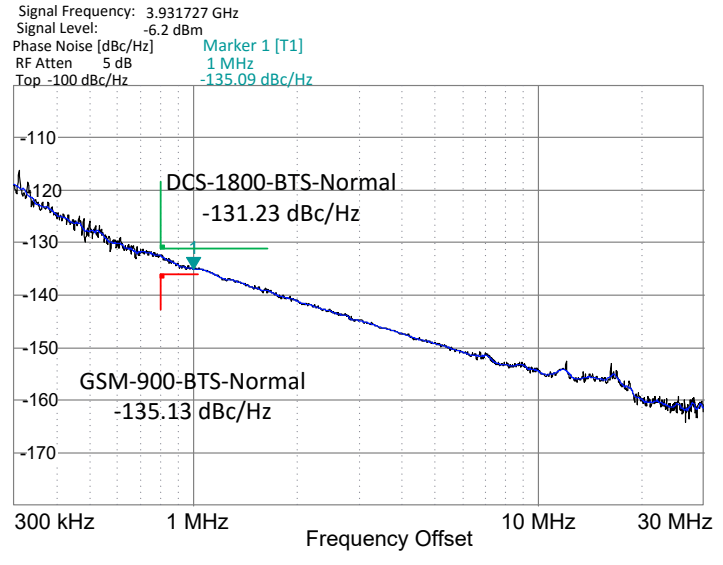


(b) V_B = 0.4 V

Fig. 6.12- first part: Phase noise measured at 1.5V for V_B equal to (a) 500 mV (35.4 mW), (b) 400 mV (41 mW).



(c) V_B = 0.15 V



(d) V_B = 0 V

Fig. 6.12 – second part: Phase noise measured at 1.5V for V_B equal (a) 150 mV (44 mW), and (b) 0 V (48 mW). At 0 V bias, the DCS-1800-BTS-Normal spec. is met with ~1-dB margin, while phase noise is ~1.5-dB higher than the GSM-900-BTS spec. at 1-MHz offset.

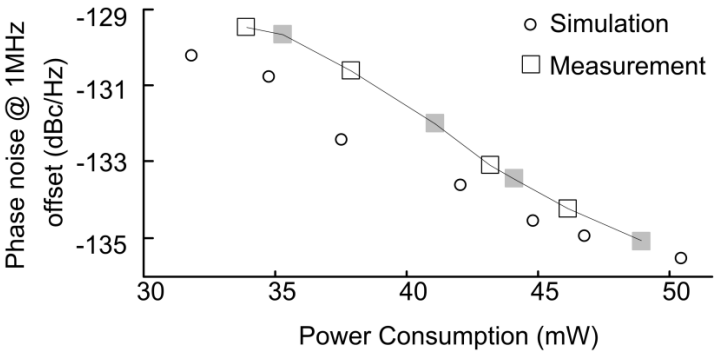


Fig. 6.13: Phase noise at 1MHz offset vs. power consumption for V_{DD} equal to 1.5 V. Simulation results from Fig. 6 (V_B varied from 0.6 V to 0 V) are included to validate the phase noise trend. The shaded squares correspond to measurements shown in Fig. 6.12.

Fig. 6.13 shows the phase noise of the developed hard limiting oscillator at 1-MHz offset vs. power consumption from a 1.5-V supply. Measurement results compare well with simulation and the phase noise predicted by eqn. 6.12 in Section 6.2. Simulation results from Fig. 6.6 are added to the plot. The shaded squares corres-

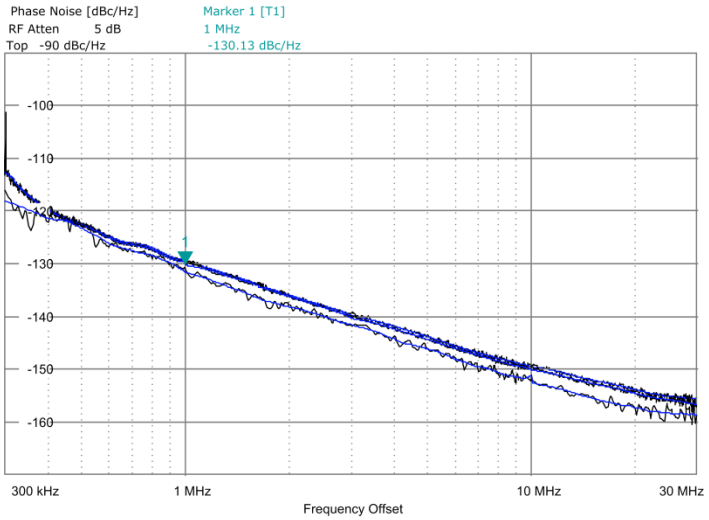


Fig. 6.14: Phase noise measured at mid-band and tuning range extremes. The variation across the tuning range at 1 MHz offset is ~1.6 dB.

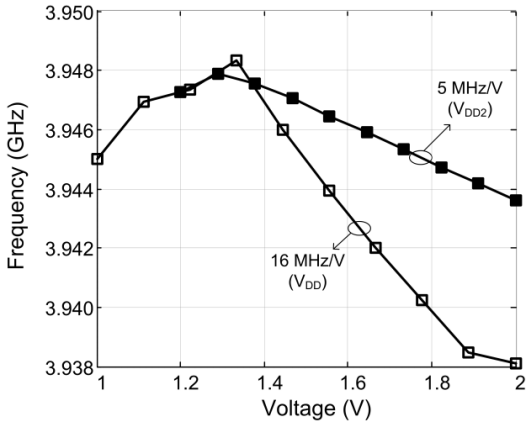


Figure 15: Frequency pushing measured due to supply voltage variation.

-pond to the phase noise measurements shown in Fig. 6.12a–d. Measurement results show a similar trend to simulations, where a combination of increase in fundamental power and phase desensitization through hard limiting provide a rapid improvement in phase noise with respect to power consumption. Gate overdrive that is not limited by the supply clearly improves the phase noise performance. Phase noise measurements at low power are limited by the divider's sensitivity.

The hard-limiting prototype oscillator has a 10.2% tuning range (7.28 – 8.06 GHz) that can be increased by switching more capacitors in parallel to the existing 4-bit tuning scheme. The phase noise variation at the tuning range edges is 1.6 dB at a 1-MHz offset. Phase-noise curves measured at 1.2 V for 25.8-mW of power consumption at the tuning range edges and the middle of the band are shown in Fig. 6.14. The divided output frequency versus supply voltage variation is shown in Fig. 6.15. At the highest frequency, where the oscillator is most sensitive to pushing, it is lower than 16 MHz/V and 5.75 MHz/V at V_{DD} and V_{DD2}, respectively. The output frequency varies by just 1.8 MHz for ±10% variation from the nominal 1.2 V.

6.7 Comparison with prior-art and impact of this work

Table 6.1 compares measured results with state-of-the-art oscillator topologies implemented in IC technologies. The phase noise is normalized to a 915-MHz

Table 6.1: Measurement summary and comparison with published work

	This Work 2012	Ref. LC 2012	[6.4] 2000	[6.20] 2001	[6.15] 2006	[6.16] 2007	[6.21] 2008	[6.17] 2011	[6.18] 2011	[6.19] 2012	[6.22] 2013	[6.23] 2013	[6.24] 2013	[6.25] 2015	[6.26] 2016
Technology	65nm CMOS	65nm CMOS	0.25um Bi CMOS	0.35um CMOS	90nm CMOS	130nm CMOS	130nm CMOS	65nm CMOS	90nm CMOS	55nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	55nm CMOS	28nm CMOS
Supply [V]	1.5 1.2[+]	1.2	1.9	2.5	1.4	3.3	1	1.2	1.2	1.5	2.15	1.25	0.4	1.5	0.7
Measured Freq. [GHz]	3.92 (7.84 ÷2)	7.7	1.5	1.2	0.915 (3.6 ÷4)	1.56	5.2	12.6	3.7	3.35	4.07	3.7	3	7.9	5
Tuning Range [6.GHz]	3.64 – 4.03 10.2%	7.6 – 8.2 8%	1.49 – 1.56 4.7%	1 – 1.2 18%	3.21 – 4.10 24%	1.5 – 1.65 9.6%	4.8 – 5.65 14%	10.8 – 14.8 31.3%	2.44 – 4 22.1%	6.7 – 9.2 31%	4.07-4.91 18.6%	3.24-4.2 25%	3-4.8 46%	7.4 – 8.4 13%	4.7-5.4 13.8%
PN norm. to 915MHz [dBc/Hz] **1-MHz offset**	-147.7 -144.3[+]	-135.8	-140	-146.5	-139.5	-144.6	-136.6	-138.3	-138.6	-143.8	-149.6	-144.8	-139.3	-142.3	-132.2
DC Power [mW]	48 25.8[+]	18	38	9.25	25.2	290.4	1.4	22.5	22.8	27	126.8	15	6.8	6.3	0.5
Oscillator-core area [mm^2]	0.19	0.065	N/A	N/A	N/A	N/A	0.11	0.212	N/A	0.49	0.37	0.22	0.12	0.19	0.18
FOM [dB]	189.9 189.3[+]	182.2	183.4	196	184.8	178.6	194.3	184.1	184.2	188.8	187.8	192.2	190.2	193.5	194.4
Circuit description	Transformer coupled hard limiting	Cross-coupled LC	Common-base oscillator	Cross-coupled LC with I_{tail} Inductor (Low power)	Cross-coupled LC with I_{tail} Inductor (High power)	Colpitts oscillator	Class C oscillator	Power combining using 4-port Inductor	Cross-coupled LC	Class C/B oscillator	combining two high-swing class-C stages	Class-F oscillator	Class-D oscillator	Complementary Class-B with transformer based tail filtering	Transformer coupled CM termination

$$FOM = abs\left[\mathcal{L}(\Delta\omega) + 20 \cdot log10\left(\frac{\Delta\omega}{\omega_0}\right) + \log\left(\frac{P_{diss}}{1mW}\right)\right]$$

[+] 1.2-V measurement

carrier for comparison. At 1.5 V, the phase noise at 1-MHz offset (-147.7 dBc/Hz) is lower than oscillators published prior to 2012, with an FOM of ~189 dB. As discussed in Chapter 1, scaling existing oscillator topologies for increased power consumption in order to meet aggressive phase noise specifications results in reduced phase-noise efficiency. This is evident in the low-noise designs presented in [6.15] and [6.16], wherein the Colpitts oscillator and the tail-filtering technique, respectively, are adapted for high power consumption. The dual-core oscillator implemented in [6.22] combines the merit of Class-C operation presented [6.21] by scaling the supply voltage to 2.15 V with the power-combining principle of [6.17], to achieves a 1.9-dB lower normalized phase noise of -149.6 dBc/Hz at an FOM of 187.8 dB.

The phase noise mechanisms in a cross-coupled oscillator were discussed in in Chapter 2 (Section 2.7). The fundamental phase-noise limit of the cross-coupled oscillator is reached when the tail-current source is noiseless. This limit is described by eqn. 2.53 when the tail-current's noise contribution is set to zero. Hegazi's technique of inductive degeneration and tail-filtering [6.15] approaches this limit in principle, wherein transistors contribute to phase noise only when they simultaneously conduct (explained in Section 2.7, w.r.t Figs. 2.10 and 2.11). The Class-C oscillator [6.21] also approaches this limit by operating all transistors in saturation. Operation in Class-C results in a higher DC-RF current conversion efficiency when compared to the Class-B operation often ascribed to the cross-coupled oscillator during analysis. This results in an increased phase noise FOM of 194.3 dB. Operation in saturation limits the swing of Class-C oscillators when operated from voltage supplies on the order of 1.2-1.5 V, and therefore their phase noise capability. Hegazi's tail-filtering principle on the other hand, does not face this constraint; however, high power designs (e.g., [6.15]) do not demonstrate the same efficiency and performance of the original low-power prototype [6.20]. It is important to note, that in both these oscillator concepts (i.e., tail-filtering and Class-C), the tank contributes noise throughout the oscillation period.

The hard-limiting principle described in this chapter addresses all known factors that

contribute to phase noise in the $1/f^2$ region: 1) Hard-limiting the output creates a region of phase-noise insensitivity, and therefore permits eliminating the tail-current without penalty of increased noise contribution from the switching pair, 2) the over-driven gate ensures the period of simultaneous conduction of the switching pair is minimized (~2x) compared to a cross-coupled oscillator which results in reduced phase noise contribution, 3) it is observed that the phase insensitivity created by hard-limiting is applicable to transistor as well as tank-noise, and lastly 4) the transformer coupled interface minimizes loading in the oscillator loop that arises from triode operation. This is not a trivial calculation as seen from the analyses in [6.27]-[6.30], and therefore in the analysis of section 6.1 this effect is lumped into the amplitude of the fundamental component that is obtained from simulation. The oscillator is designed for a moderate tuning range of 10% (adequate for the ~6% tuning range requirement from 870-925 MHz for a GSM-BTS receiver) to maximize phase noise performance.

The merits of hard-limiting and exploring waveshape to tailor phase noise performance for high power applications are clear from the above discussion of the hard-limiting prototype and its comparison with the tail-filtering and Class-C designs. Since the publication of the concept in 2012, subsequent oscillator designs have incorporated its key principles. The Class-F oscillator [6.23] reinterprets third-harmonic tuning proposed in [6.6] in the Zero-ISF context described in this work. It applies the premise that a region of constant-amplitude in the waveshape of a resonant harmonic oscillator results in Zero-ISF, which coincides, beneficially, with the transistor's on-time. The Class-D oscillator in [6.24] directly invokes hard-limiting induced impulse insensitivity in an LC oscillator to sacrifice the tail-current source in order to approach Hegazi's noise-limit for a cross-coupled oscillator, while [6.26] follows suit with additional filtering in the common-mode path for improved performance in the $1/f^3$ region. As an aside, the highlighted text in section 6.2.1 is quoted from the journal publication of this work [6.2], where a focus on common-mode design was described in 2014. The transformer-based tail-filtering design in [6.25] also benefits from the flat-ISF that is an outcome of voltage-limited operation.

These low and moderate power designs show a very high figure of merit of 192-194 dB (see Table 6.1).

6.8 Summary

Phase desensitization through hard limiting (in contrast to conventional design methodology) is explored to achieve ultra-low phase noise. The circuit topology and operation ensure that the energy compensation through the active devices coincides with the clipped peak output voltage, thereby minimizing the conversion of circuit noise from active and passive devices to phase noise. The main contribution towards low phase noise lies in the elimination of the tail current source for high power designs, without incurring the penalty of increased noise contribution from the switching transistors. The circuit alleviates the phase noise/power consumption trade-off, and provides a substantial improvement in performance due to a combination of hard limiting and increase in fundamental power. Both these aspects are manifested via mismatched gain obtained from a cascade of two transformers. An 8-GHz prototyped in 65 nm CMOS provides measurement proof of the concept. At 32 mA drawn from a 1.5-V supply and a tuning range of 10%, the oscillator is within 1.5 dB reach of the GSM-900 base-station specification of -147 dBc/Hz at an 800-kHz offset.

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Chapter 7

Wideband FM demodulation at IF based on injection locking a multi-stage ring oscillator is described in this thesis, along with the use of hard-limiting for phase desensitization in low-noise oscillators. The conclusions drawn from the theory developed in this work, and experiments validating them are presented in this chapter, which closes the thesis with recommendations for future work.

7.1 Injection-locked FM demodulation

From stand-alone characterization of a 65-nm CMOS prototype, it is observed that a locked-in ring oscillator tracks wideband frequency modulation linearly. Since the output discharges entirely over each period, the operation of the free-running oscillator is often described as being memoryless and consequently susceptible to external stimulus. The oscillator locks over a wide range of input frequencies, and the main reason is that the exponential current buildup that characterizes the charging and discharging phases is easily triggered by an external input.

The transmission of an FM signal through a locked-in oscillator is characterized by scaling of the modulation index and FM deviation. This is best demonstrated via Bessel function coefficients that characterize the FM spectrum for varying modulation indices. Measurements confirm translation of Bessel function coefficients at the output of the locked-in ring oscillator and show excellent correlation to theory. While the FM bandwidth is scaled down via injection locking, correlating the quadrature-phased outputs inherent to the four-stage ring topology enables and simplifies power-efficient wideband FM demodulation. This circumvents the need for controllable auxiliary true-time delays. The demodulator characteristic shows a liner performance for fractional bandwidths approaching unity. Other benefits of this approach to demodulation include: 1) data-rate independent power consumption, 2) wideband operation, 3) insensitivity to noise and additive amplitude modulation of the input RF, 4) a requirement for low distortion is not imposed on the IF amplifier, and 5) operation of the ring-oscillator at $1/4^{th}$ the intermediate frequency enables a higher IF and a lower fractional

bandwidth for improved efficiency.

A 65-nm CMOS prototype demodulator occupies 0.17 mm^2 and dissipates just 3.2 mW from 1.2 V at quiescent point. The SNR sensitivity is 8 dB, and demodulator measures a 0.1% BER at 10 Mbps for a 45 mV_{pp} input signal at IF. Verification of injection locking is limited by the test-equipment to rates up to 420 MHz (0.84 Gbps), while simulation predict the oscillator can track modulation rates on the order of $1/5^{th}$ the carrier frequency.

Additional measurements conducted to study the response of the oscillator to external noise and FM show physical trends not reported to date. Experimental characterization of the oscillator's response to FM shows increased sensitivity compared to static frequencies over the same frequency band. This demonstration of hysteresis lies beyond the scope of existing mathematical models that explain injection locking. However, the lower locking threshold for modulated signals reduces the amplification requirement at IF for injection locking. A similar effect is observed when the locking threshold increases during interference ramp-down when followed sequentially by a ramp-up of the interference applied to a locked-in oscillator. Experimental study of a ring oscillator's response to colored noise reveals degradation in phase stability accompanied by a noise-induced frequency shift. This noise-induced frequency shift increases with the external noise injected in the oscillator loop. Excess noise induces chaotic behavior, during which the oscillator is still capable of locking to external stimulus, but at increased input-power levels. With increasing SNR levels it is observed that the oscillator transitions from instability to complete injection-lock via transient states of partial lock. When partially locked, the oscillator is seen to lock to part of the FM deviation before falling out of lock, resulting in a lower modulation index at the output than expected. The partial locked states in the presence of excess noise resemble the oscillator’s response to insufficient signal drive to lock over the total FM bandwidth. Therefore, though the SNR sensitivity for a perfect lock is measured to be 8 dB, operation does not cease at lower values of input SNR.

7.2 Low noise oscillator design

In this thesis phase noise models developed over past few decades are reviewed for insights on phase noise conversion mechanisms in oscillators. In this work a hard-limiting oscillator prototype was proposed that minimizes phase noise conversion of thermal noise contributors in an oscillator. The theoretical phase noise expression developed in this work is based on Hajimiri's linear time-varying phase-noise model, and compare closely with simulation and measurements.

The tail-current source in a cross-coupled oscillator mitigates noise contribution and loading from the switching pair, however, its contribution to phase noise can be substantially more while targeting stringent phase noise specifications at the expense of power dissipation. Hard limiting the output with transformer-coupled gate overdrive creates phase insensitivity that rejects noise from not just the transistor pair, but the tank as well, while the transformers reduce loading in the loop. The circuit is suitable for high-power consumption and the principle of operation alleviates the phase noise/power consumption trade-off, and provides a substantial improvement in performance due to a combination of hard limiting and increase in fundamental power. Maximum phase-noise conversion of channel noise occurs when the switching transistors simultaneously conduct. A cyclostationary, time-dependent phase-noise expression developed in this thesis shows this. Rise and fall transient times are therefore minimized using transformer-coupled gate-overdrive. The theoretical phase noise model developed in this thesis is verified against simulation and measurement with a reasonable accuracy of less than 2 dB. The GSM 900-MHz base-station specification of -147 dBc/Hz at an 800-kHz offset is among the most challenging receiver phase noise requirements. The 65-nm CMOS prototype oscillator developed in this work has a moderate tuning range of 10% and is within 2-dB reach of this specification at room temperature and dissipates 48-mW from a 1.5-V supply. Key principles of phase noise reduction proposed in this work have been incorporated in subsequent oscillator designs from other research groups.

7.3 Future work and recommendations

The frequency axis extends in one direction and it must be pursued. Innovations in circuit techniques are necessary to realize the potential of envisioned wideband and high data-rate systems at mm-wave and sub mm-wave frequencies, as well as to experiment with unexplored bands for applications yet to be discovered. A key aspect moving forward will be the demonstration of electrical sources in these bands, bringing the antenna on chip, and designing receivers capable of handling wideband modulation at reduced signal to noise ratios.

At present we find ourselves at cross-roads with technology and technique, where the construction of the high-frequency RF front-end is limited to a few transistors with a strong emphasis on negating their parasitic reactances for unilateral operation. There may still be a few generations of CMOS scaling to come that might aid the performance trade-off against power consumption. Demodulation of wideband data is poised to be a significant challenge. The IF demodulator developed in this work benefits from wideband locking capabilities, low SNR sensitivity, and from the fact that the locked-in ring needs to be designed at a quarter of the IF frequency. A greater reduction in operating frequency can be accomplished with a greater number of stages (for e.g., an 8-stage ring oscillator at 10 GHz, can demodulate an IF signal at 80 GHz). However, in the context of the FM demodulator developed in this work, and in general, a future challenge would be the design of power-efficient, wideband amplifier stages operating over fractional bandwidths on the order of one.

Aside from the implementation details of wideband radios is the advancement of theoretical studies. Oscillators, their application and characterization form the core of this thesis. Findings presented here from experimental study of the oscillator's response to external noise and FM lie beyond the scope of present mathematical models and require dedicated study. Analytical studies on frequency shifts and chaos induced by external noise will provide a better insight on these processes, and can even lead to improvements in phase noise models. On the other hand, injection locking is a phenomenon that is treated in the frequency domain with vector representation, though experiments reveal time-dependencies that are developed within the locked-in state. The analytical treatment and explanation of harmonic

injection locking is a difficult problem. However, a solution that parameterizes the non-linear processes and state dependencies that characterize injection locking will add significantly to the understanding of autonomous systems.

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Collaborative research:

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