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Microelectronics

A Compact Resistor-Based Temperature Sensor

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In partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering
at Delft University of Technology,
Faculty of Electrical Engineering, Mathematics and Computer Science
To be defended on Friday June 21st, 2019

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Abstract

Smart temperature sensors can be used for the temperature compensation of micro-electromechanical (MEMS) frequency references. From the different types of CMOS temperature sensors, resistor-based sensors are currently the most energy-efficient. However, compared with bipolar transistor (BJT)-based temperature sensors, resistors suffer from higher nonlinearity and spread of their temperature dependencies which require multi-point calibration to achieve similar accuracy. Given that a new design direction should attempt to combine the best features of both types of sensors, the target of this work is to develop a resistor-based temperature sensor that should be more energy-efficient than BJT-based sensors, but with a competitive area.

This thesis investigates circuit techniques to obtain a design of a compact resistor-based temperature sensor (area $< 0.1mm^2$) which is energy-efficient, while achieving high resolution ($sub - mK$) and high accuracy (inaccuracy $< 0.1°C$).

To achieve the target specifications, a frequency-locked-loop (FLL) is implemented around the sensing element. Design directions were presented, consisting of a continuous-time readout and a discrete-time readout together with their limitations and performance. Based on the simulation results, it can be stated that the combination between the FLL readout and the Wien-bridge sensing element enables the design of a compact sensor which achieves the target specifications.

Acknowledgments

Firstly, I would like to express my sincere gratitude to my advisor, Professor Kofi Makinwa, for his guidance during the time of research and writing of this thesis. I would like to thank him for giving me this great project from which I had to learn a lot and for sharing his knowledge with me.

Secondly, I would like to thank Professor Michiel Pertjis and Professor Fabio Sebastiano for being part of my thesis committee and for all the knowledge I gained while I was attending their courses.

Thirdly, my special thanks are extended to my collegues from the Electronic Instrumentation Laboratory for their help and assistance.

Last but not least, I would like to thank my husband, Cristian, and our family for the continuous support and motivation they gave me. I want to thank Cristian for being my partner, my friend and collegue, my best critic yet my strongest supporter.

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Chapter 1 Introduction

1.1 Motivation

All electronic systems exhibit a certain temperature dependence, and so temperature sensors play an important role in most complex systems. Numerous devices (laptop computers, LCDs, batteries) need to monitor, control or compensate for changes of temperature so that their intended functionality is preserved over a wide temperature range. Common ways of sensing temperature involve the use of resistive temperature detectors (RTDs), thermistors, thermocouples, and silicon temperature sensors. Silicon temperature sensors can also include signal processing circuitry in the same package, in which case the ensemble is called a *smart temperature sensor* [5].

Since there are numerous applications that require temperature sensing, the exact requirements for a smart temperature sensor can only be defined in the context of a particular application. In the case of *micro-electro-mechanical (MEMS) frequency references*, temperature sensors are used to compensate for the temperature dependence of a MEMS resonator. To have a full understanding of why this compensation is necessary and how it works, a short description of such systems will be provided in the next section.

1.2 Overview of Target Application

Until recently, most clocked systems relied on frequency references based on quartz resonators, however, these occupy a large area, are unsuitable for batch processing and difficult to integrate on silicon chips. A better alternative is to use MEMS resonators since these are CMOS compatible, thus leading to thin, cheap and low power timing solutions [6].

While easier integration was the main driver for the transition from quartz crystals to MEMS resonators, achieving high stability, frequency and relia-

bility is not that straightforward for MEMS resonators. Temperature-stable operation is difficult to achieve since the frequency of a moderately doped silicon micromechanical resonator has a temperature coefficient of approximately 31 ppm/°C [7]. Uncompensated, this leads to an output frequency variation of 4000 ppm from 40°C to 85°C [8]; in comparison, uncompensated quartz crystals exhibit a variation of 25 ppm over the same temperature range [9]. As a consequence, a consistent goal of silicon MEMS resonator research has been to reduce this intrinsic temperature dependence through different compensation techniques [10–13].

One way to reduce this temperature dependence is to combine a MEMS resonator with a fractional-N synthesizer and a precision temperature sensor, as shown in Figure 1.1 ([8], [14]). The high-resolution control provided by the fractional-N synthesizer enables a simple method for temperature compensation with the help of the information provided by the temperature sensor [1]. The charge pump and the sustaining oscillator circuit maintain the resonant oscillation of the MEMS device, while the temperature sensor monitors the chip temperature and drives the digital logic block. This block calculates the control word which serves as an input to the fractional-N synthesizer. The output frequency is given by the programmable frequency divider, which generates an output signal whose frequency is a multiple of the MEMS resonator frequency and, more importantly, which is stable over the operating temperature range. With this architecture, programmable MEMS-based oscillators are able to achieve frequency stability of less than 0.5-ppm [8], similar to that of high-end quartz references [15]. Further improvements in temperature stability will depend on advances in the performance of temperature sensors. On that premise, *this thesis investigates circuit-techniques which can be used to design a smart temperature sensor for the temperature compensation of MEMS-based oscillators.*

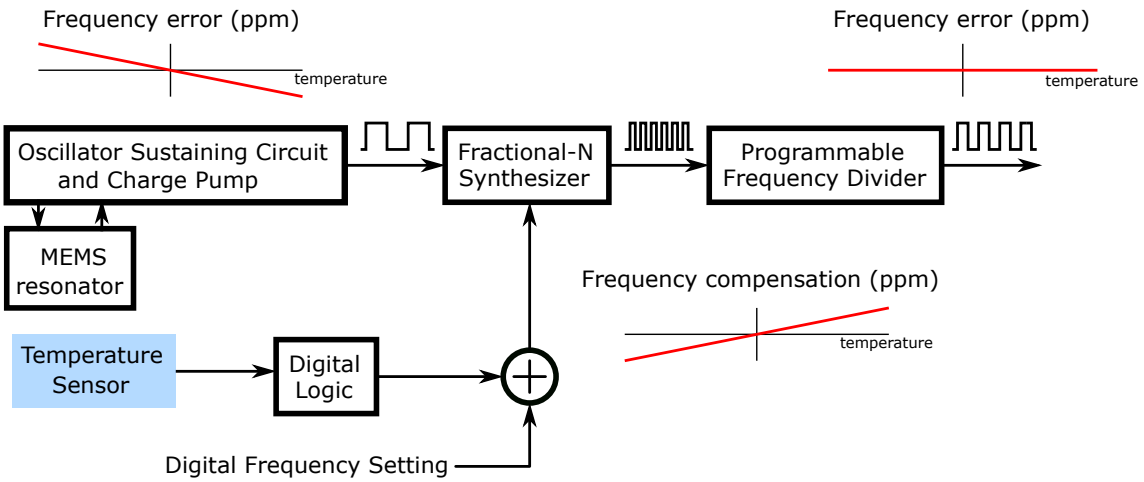


Figure 1.1: Block diagram of a programmable MEMS-based oscillator

1.3 Temperature Sensor's Target Specifications

The temperature information can be extracted via various signals: current, voltage, frequency, phase, etc., so different readout circuits can be implemented. The following section starts with describing existing temperature sensors used for the compensation of MEMS-based oscillators. This is followed by the derivation of target specifications for a new temperature sensor based on the performance of state-of-the-art (SOTA) designs.

One way to extract the temperature information is to implement a voltage divider with the use of a temperature-dependent MEMS-resistor, R_{MEMS}, and a tunable temperature independent reference impedance, R_{ref} (shown in Figure 1.2). The amplifier is comparing the output voltage of the divider with a reference voltage V_{ref}, and the error signal is fed to a quantizer which digitally balances the reference impedance so as to minimize the error signal. This implementation enables a MEMS-based programmable oscillator with frequency stability smaller than $\pm 0.5ppm$. The temperature sensor occupies 0.15 mm^2, consumes 2.8mA from a 3.3V supply and achieves 0.1mK resolution in 100ms conversion time.

Another design of a temperature sensor used for the compensation of MEMS-based frequency references employs a bipolar transistor (BJT) -based sensing element followed by a switched-capacitor (SC) Sigma-Delta ($\Sigma\Delta$)

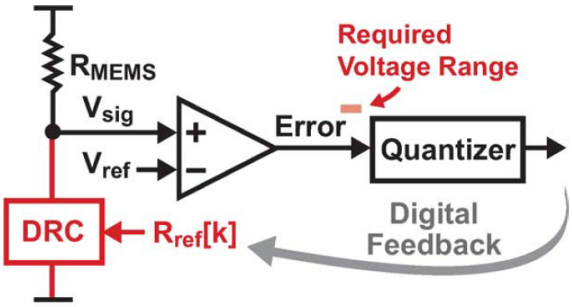


Figure 1.2: Block diagram of the temperature sensor from design [1]

modulator (Figure 1.3). The base-emitter voltage, V_{BE1}, has a negative temperature coefficient of approximately $-2mV/°C$ (with a complementary-to-absolute-temperature characteristic, known as CTAT,), whereas the difference between the two BJT base-emitter voltages, ΔV_{BE}, is proportional-to-absolute-temperature (PTAT) and it is given by:

$$\Delta V_{BE} = n \cdot \frac{k_B \cdot T}{q} \cdot \ln(p), \tag{1.1}$$

where p is the ratio of the two collector currents, n is a process dependent non-ideality factor, k_B is Boltzmann constant, T is temperature and q is the electron charge. The linear combination of V_{BE} and ΔV_{BE} generates a band-gap voltage V_{BG} equal to:

$$V_{BG} = V_{BE1} + \alpha \cdot \Delta V_{BE}, \tag{1.2}$$

where α is a gain factor.

V_{BE} and ΔV_{BE} are applied to a charge-balancing second order $\Sigma\Delta$ modulator which outputs a bit-stream whose average value is proportional to $(\alpha \cdot \Delta V_{BE}) / V_{BG}$. To improve its accuracy and stability, several dynamic correction techniques are applied: correlated double sampling (CDS), chopping and dynamic element matching (DEM). This compensation scheme enables frequency stability of $\pm 3ppm$ over the [-40, 85] °C temperature range. The temperature sensor occupies $0.085mm^2$, draws 4.5uA from a 1.5 to 3.3V

supply and achieves a resolution of 25mK in a conversion time of 6ms.

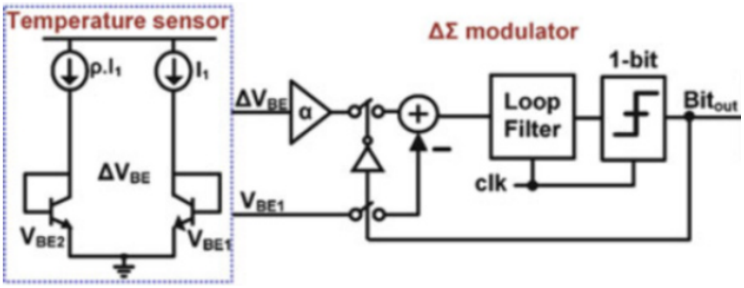


Figure 1.3: Block diagram of the temperature sensor from design [2]

The applications in which frequency references are used are very different, each with their own set of requirements. For timekeeping in mobile or battery-powered devices, a frequency reference needs to occupy a small area and have low power consumption [16]. That means that the associated temperature sensor should be also compact and energy efficient since its energy consumption will be part of the total energy budget. Moreover, tight control of the frequency stability requires high-temperature resolution. In order to achieve sub-ppm stability over the operating range, this should be at the mK-level. These general requirements will be further discussed in the context of SOTA temperature sensors.

Many CMOS compatible devices have been used to fabricate smart temperature sensors: metal-oxide-semiconductor field-effect-transistors (MOSFETs), bipolar junction transistors (BJTs) [17], [18] and resistors [3, 4, 8, 19]. Based on a survey of performance data published over the last 30 years [20], resistor-based temperature sensors are currently the most energy efficient. They can simultaneously achieve sub-mK resolution and compact sizes (below $0.1mm^2$). However, compared with BJTs, resistors suffer from higher nonlinearity and spread of their temperature dependencies which require multi-point calibration to achieve similar accuracy. This can dramatically increase their manufacturing costs. In the case of a MEMS frequency reference, however, this is not a big drawback since calibration is already used to compensate for the initial frequency offset caused by the process variations inherent to the resonator's fabrication [16]. In conclusion, a resistor-based temperature sensor matches the application.

From the survey [20], BJT-based temperature sensors are the most accurate. Thus the target specifications of a new temperature sensor should also be compatible with those of existing BJT-based temperature sensors. Table 1.1 shows a performance summary of state-of-the-art BJT and resistor-based temperature sensors. One can see that the sensing part is implemented using different structures: Wien bridge (WB) resistors, Wheatstone bridge (WhB) resistors, and Poly-phase filter (PPF) resistors. The readout circuits can consist of Frequency-locked loop (FLL) circuits, Sigma-Delta ($\Sigma\Delta$) modulators and Continuous time Analog-to-digital converters (CT ADCs).

	[18]	[21]	[3]	[22]	[23]	[4]
Sensor type	BJT	BJT	Res.(WB)	Res.(WB)	Res.(WhB)	Res.(PPF)
Readout type	$\Sigma\Delta$	$\Sigma\Delta$	FLL	CT ADC	CT ADC	FLL
Tech. node $[nm]$	65	160	180	180	180	65
Area $[mm^2]$	0.1	0.16	0.09	0.12	0.12	0.007
Power $[\mu W]$	10	6.9	31	52	79	68
Temp. range $[^\circ C]$	-70 - 125	-70 - 125	-40 - 85	-40 - 180	-55 - 125	-40 - 85
Inaccuracy $[^\circ C]$	$\pm$0.2	$\pm$0.06	$\pm$0.12	$\pm$0.11	$\pm$0.14	$\pm$0.12
Trim method	1	1	3	2	2	2
Resolution [mK]	30	15	2.8	0.46	0.16	2.5
Conv. time [ms]	455	5	32	10	10	1
Res. FOM $[pJK^2]$	4100	7.8	8	0.11	0.02	0.43

Table 1.1: Performance summary and comparison of state-of-the-art BJT-based and resistor-based temperature sensors

Table (1.1) provides a good starting point for possible target specifications of a new resistor-based temperature sensor. Designs [18] and [21] highlight the high accuracy that BJT-based sensors can achieve with one point trim, with [21] being the most accurate BJT-based temperature-to-digital converter (TDC) ever reported [20]. Another important characteristic of these designs is the small area they occupy: $0.1mm^2$ and $0.16mm^2$, respectively. On the other hand, designs [22] and [23] are the most energy-efficient resistor-based temperature sensors ever reported [20], while [3] and [4] are the smallest designs that obtain reasonable energy-efficiency. Given that a new design direction should attempt to combine the best features of both types of sensors, the target of this work is to develop a resistor-based temperature

sensor that should be more energy-efficient than BJT-based sensors, but with a competitive area.

It is easy to see that when striving for a lower area, both bipolar transistors temperature sensors and resistor-based temperature sensors can be made smaller than $0.1mm^2$. The design in [4] takes advantage of a more digital-oriented architecture in a smaller technology node, but at the expense of resolution. Since the resistor-based temperature sensors in [22] and [23] can easily achieve sub-mK resolution, the target for the current design is set for a $0.1mm^2$ area and a resolution below 1mK. In terms of inaccuracy, the design in [3] shows that with a 2-point trim an inaccuracy of $0.12°C$ over the [-40, 85]$°C$ range can be expected. When considering a power budget, the delimitation between the different sensing elements and readout circuits is not that straightforward, so the desired maximum could be the minimum one reported for a resistor-based temperature sensor ([3]), around $30\mu W$. Table 1.2 summarises the set of derived target specifications for the proposed design (Table 1.2).

Specification	Value	Motivation
Tech. node [nm]	0.18	
Area [mm^2]	<0.1	BJT-based SOTA
Power [μW]	<30	R -based SOTA
Temp. range [$°C$]	-40 - 85	R -based SOTA
Inaccuracy [$°C$]	±0.12	R -based SOTA
Trim method	3	R -based SOTA
Resolution [mK]	<1	BJT-based SOTA
Conv. time [ms]	30	BJT-based SOTA
Res. FOM [pJK^2]	<0.21	R -based SOTA

Table 1.2: Target specifications for the proposed design

Based on the previous analysis, the main *goal of this project* can be fully established: *the design of a compact resistor-based temperature sensor which is energy-efficient, while achieving high resolution (sub − mK) and high accuracy (inaccuracy* $< 0.1°C$*).*

1.4 Previous Implementations

While reviewing the target specifications and the performance summary of SOTA temperature sensors (Table 1.1), one can observe that the performance of the designs in [3] and [4] approaches the target specifications. Both temperature sensors are using a frequency-locked-loop (FLL) readout [24–26], but they have different implementations. The first design builds the FLL around a voltage-control oscillator (VCO), a current buffer, a chopper demodulator and a Wien-bridge filter (Figure 1.4), while the other design uses a comparator directly after an RC filter, simplifying the loop but at the expense of resolution (Figure 1.5)

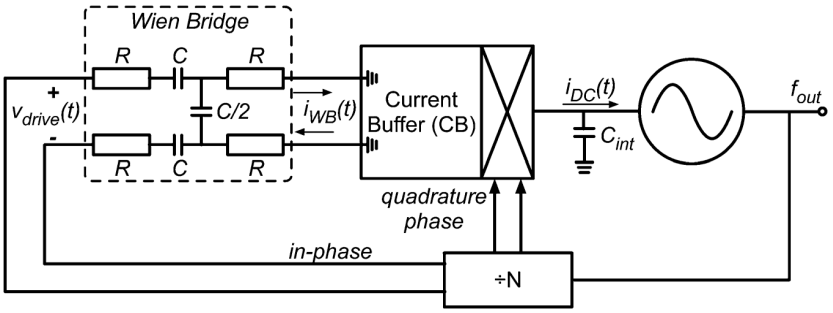


Figure 1.4: Block diagram of the temperature sensor from design [3]

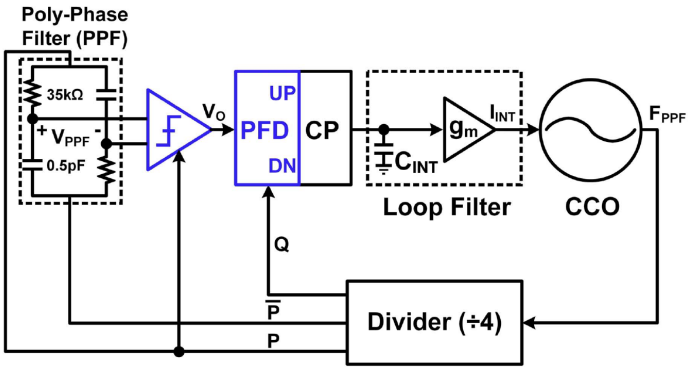


Figure 1.5: Block diagram of the temperature sensor from design [4]

Nonetheless, both designs prove that, in principle, the use of an FLL results in a design with high power efficiency and, simultaneously small area.

Based on these results, the work described in this thesis will begin from this basic concept and investigate how its performance can be improved.

1.5 Thesis Overview

The thesis is organized as follows: Chapter 2 illustrates the working principle of a frequency-locked-loop type of readout and how can it be applied in the context of a resistor-based temperature sensor. A system level analysis of this type of architecture is performed in order to determine the system-level considerations. Chapter 3 discusses the circuit-level implementation of the temperature sensor, supported by simulation results. Two approaches are considered: a continuous-time readout and a discrete-time readout. Chapter 4 describes two of the possible implementations for digitizing the output of the FLL. Chapter 5 presents the main conclusions of the project, emphasizing the limitations of each implementation and the trade-offs one needs to consider when trying to achieve the target specifications.

Chapter 2 System Analysis

This chapter describes the proposed resistor-based temperature sensor, which, together with a frequency-locked-loop (FLL) readout circuit, aims to achieve the target specifications derived in the previous chapter (Table 1.2). First, the choice of the sensing element is discussed. This is followed by a system-level analysis, which gives an overview of critical design concepts.

2.1 Choice of the Temperature Sensing Element

The sensing element can be treated as a black box, which has temperature as the input. The output signal needs to be either frequency or phase in order to be compatible with the FLL readout. A simple implementation of this system is an RC-filter, where the resistor is temperature dependent. It is essential for the filter to have a well-defined temperature dependency (i.e., only due to the resistor) in order to limit sources of spread and non-linearity. In standard CMOS processes, this can be easily achieved by using metal-insulator-metal (MiM) capacitors, which are almost stable with temperature. Based on this information, an RC filter is suitable to be used as a sensing element.

Figure 2.1 shows the frequency and phase response of a low-pass (LPF), high-pass (HPF) and band-pass (BPF) RC-filter (also known as a Wien-bridge) with the same cut-off/center frequencies. By looking at the phase response, a critical property of the BPF arises: the phase response of a BPF has a larger slope than the LPF or HPF. Moreover, at the center frequency, the phase equals 0 °, and the phase response is almost linear. These two properties make the BPF the best candidate for the sensing element because it provides the highest change in phase for a change in input frequency.

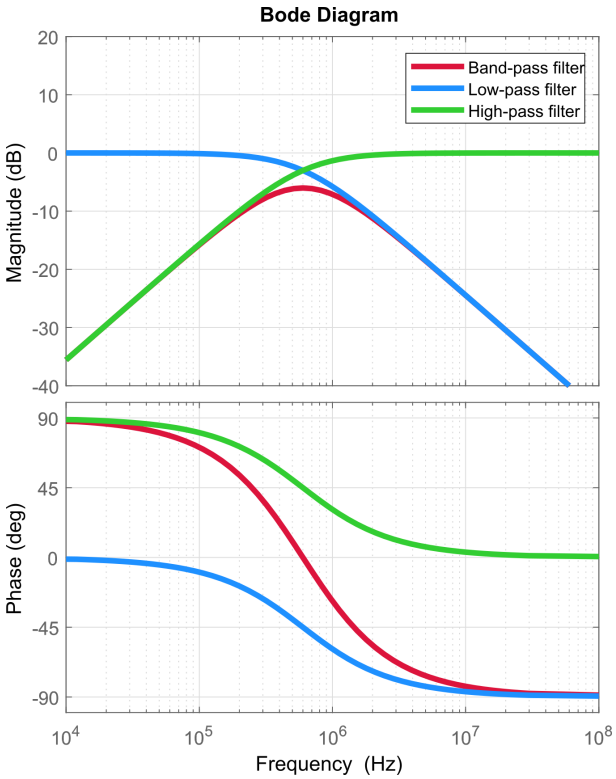


Figure 2.1: Transfer function of a HPF, LPF and BPF

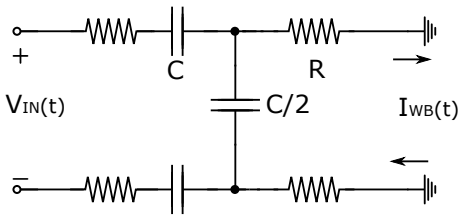


Figure 2.2: Schematic of the Wien-bridge

In the case of a Wien-bridge (WB) RC filter (Figure 2.2), the relationship between the input voltage and the output current of the filter is:

$$H_{WB}(j\omega) = \frac{I_{WB}(j\omega)}{V_{IN}(j\omega)} = \frac{j\omega C}{-\omega^2 R^2 C^2 + 3j\omega RC + 1} \tag{2.1}$$

The phase response of the Wien-bridge is given by:

$$\phi_{WB}(\omega) = -\tan^{-1}\left(\frac{R^2C^2\omega^2 - 1}{3RC\omega}\right) \tag{2.2}$$

The center frequency of the bridge can be expressed as:

$$f_{\text{center}}(\omega) \simeq \frac{1}{2\pi RC} \tag{2.3}$$

These three equations describe the sensing element and serve as a basis for the next section's analysis, where an FLL readout is employed around the sensing element to extract the temperature information.

2.2 Architecture

2.2.1 FLL Readout Principle

When the Wien-bridge is driven by a frequency signal, its output will exhibit a certain phase shift. For the moment, it is enough to think about the FLL as a feedback loop that looks at the output phase of the bridge and changes its driving frequency until the phase-response of the WB is 0 °. When the loop has settled, the driving frequency will be equal to the center frequency of the WB:

$$f_{\text{out,FLL}} = N \cdot f_{\text{center}}(\omega) \simeq N \cdot \frac{1}{2\pi R(T)C}, \tag{2.4}$$

where $R(T)$ is the resistance of the temperature dependent resistor, C is the capacitance value of the MiM capacitor and N is the ratio between the output frequency of the FLL and the bridge's center frequency.

Since the FLL controls the WB phase to 0 °, it is relevant to define the phase to frequency sensitivity at this point:

$$S_{\phi_{WB},\omega} = \left.\frac{d\phi_{WB}(\omega)}{d\omega}\right|_{\omega o=1/(RC)} = -\frac{2}{3} \cdot RC \tag{2.5}$$

2.2.2 Sensing Temperature Principle

The FLL requires a phase detector in order to lock the WB phase to 0 °. The combination of a multiplier and a low-pass filter can serve as a phase detector [27], see Figure 2.3. The two rectangular signals ϕ_{drive} and ϕ_{chop}

have the same frequency, but are 90° phase shifted:

$$\phi_{drive}(\omega) = \frac{4}{\pi} \cdot A \cdot \sin\left(\omega_{drive} t + \varphi_0\right) + \frac{4}{3\pi} \cdot A \cdot \sin\left(3\omega_{drive} t + \varphi_0\right) + \ldots \tag{2.6}$$

$$\phi_{\text{ chop }}(\omega) = \frac{4}{\pi} \sin\left(\omega_{\text{ chop }} t + \varphi_{90}\right) + \frac{4}{3\pi} \sin\left(3\omega_{\text{drive}} t + \varphi_{90}\right) + \ldots \tag{2.7}$$

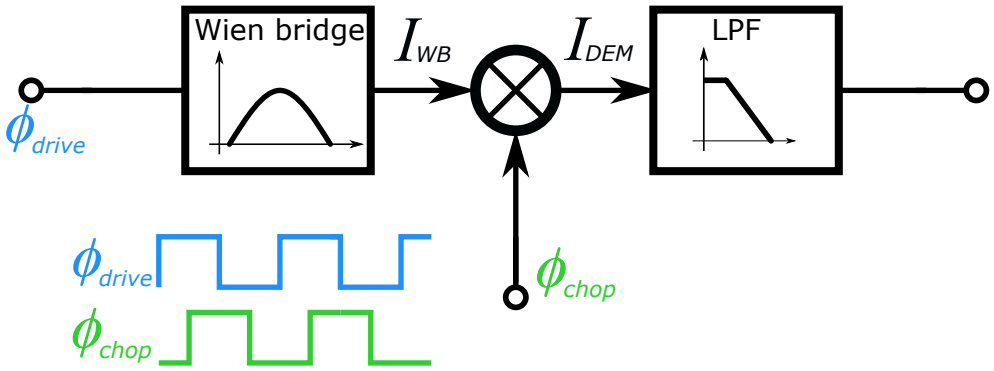


Figure 2.3: Phase detection principle

If only the first three harmonics of the driving signal ϕ_{drive} are considered, the output current of the WB filter can be written as:

$$\begin{aligned} I_{WB}(\omega) = & \frac{4}{\pi} \cdot A \cdot |H_{WB}(j\omega)| \cdot \sin\left(\omega_{drive} t + \varphi_0 + \varphi_{WB(\omega)}\right) + \\ & \frac{4}{3\pi} \cdot A \cdot |H_{WB}(3j\omega)| \cdot \sin\left(3\omega_{drive} t + \varphi_0 + \varphi_{WB(3\omega)}\right) + \ldots \end{aligned} \tag{2.8}$$

This output current is multiplied by the control signal and results in a DC component:

$$\begin{aligned} I_{DEM\_DC} \approx & \frac{8A}{\pi^2} \cdot \left[|H_{WB}(\omega)| \cdot \cos\left(\varphi_0 - \varphi_{90} + \varphi_{WB(\omega)}\right)\right] + \\ & \frac{8A}{\pi^2} \cdot \frac{1}{9} \left[|H_{WB}(3\omega)| \cdot \cos\left(\varphi_0 - \varphi_{90} + \varphi_{WB(3\omega)}\right)\right] + \ldots \end{aligned} \tag{2.9}$$

together with some additional components at even harmonics of the driving frequency.

When ϕ_{drive} and ϕ_{chop} are perfectly 90° shifted, the value of I_{DEM_DC}

will be mostly defined by the phase shift of the Wien bridge ($I_{DEM\_DC} \sim \cos\left(\varphi_{WB(\omega)}\right)$). This phase detection scheme can be easily implemented with the help of a polarity reversing switch (known as a chopper, [28]), which is driven by the rectangular signal ϕ_{chop} .

2.2.3 System-Level Diagram

After describing a temperature sensing principle that is compatible with the FLL readout, the next step is to discuss exactly how the readout circuit extracts temperature information from the sensing element (Wien bridge). Figure 2.4 illustrates the block diagram of the proposed system. Before diving into its operation, some of its key features are worth mentioning. It is a fully-differential structure, which helps minimize common-mode errors. Furthermore, the VCO is driven by the integrator output and not directly by the power supply ([29]). This reduces supply noise coupling, which can drastically degrade the system's performance.

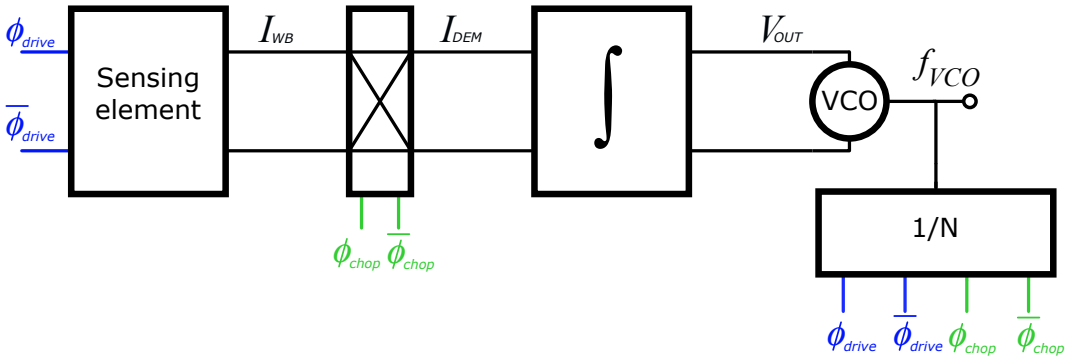


Figure 2.4: Block diagram of the proposed architecture

The operation of the system can be briefly described as follows: the output current of the phase detector is integrated and applied to the VCO. As a result, the output frequency of the VCO is adjusted such that it drives the Wien bridge to its center frequency.

The timing of the system is shown in Figure 2.5. The VCO's output is divided by an N-integer frequency divider which generates the bridge's driving signals (ϕ_{drive}), and the 90° phase shifted signals (ϕ_{chop}), which are required for the phase detector. The phase detector output current (I_{DEM})

is applied to the integrator, and the resulting voltage (V_{OUT}) controls the input of the VCO.

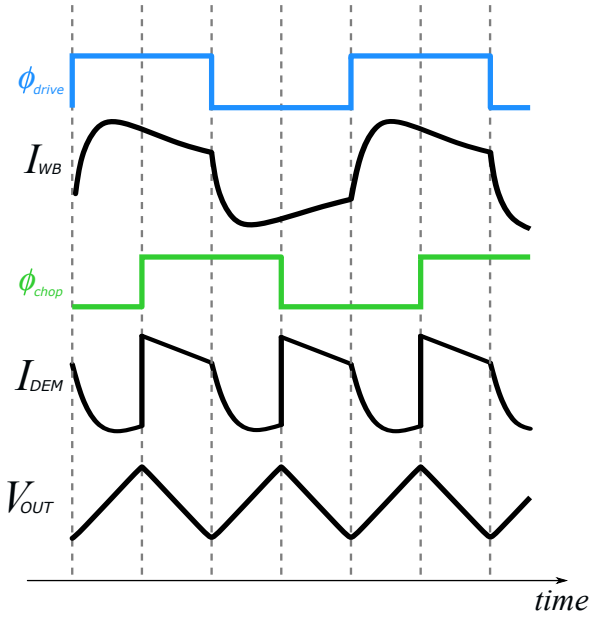


Figure 2.5: Timing diagram of the system

As previously discussed, besides the DC component, the demodulated current has components at even harmonics of the driving frequency. Of these harmonics, the one at $2 \cdot f_{drive}$ contributes the most to the ripple of the output voltage of the FLL. After integration, this ripple translates via the VCO's gain, into a variation in the output frequency. This will cause a spur in the output spectrum of the FLL, which limits its resolution. Fortunately, there are a number of ways to solve this problem. Firstly, the integration capacitor size can be increased in order to better suppress the ripple; however, this comes at the cost of the area. Another option is to add an extra first-order RC filter after the integrator. But, in order to reduce the ripple to sub-mV level, large components are required, which also costs area and the extra phase-shift can even lead to loop instability. Another option is to add a Zero-Order-Hold (ZOH) filter designed so that its notches are located at the frequencies of the ripple signal [30]. This solution not only filters out all the unwanted harmonics, it also adapts to any change in frequency. Considering these arguments, a ZOH filter is implemented to filter out the ripple signal.

The ZOH filter requires control signals which are derived from the frequency divider, as shown in Figure 2.6.

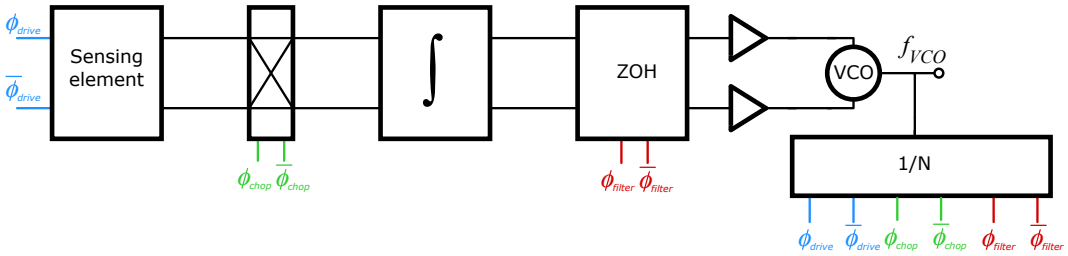


Figure 2.6: Block diagram of the proposed architecture with ZOH filter

2.3 System-Level Modeling

In an FLL the signal of interest moves through multiple domains: it is translated from frequency to phase, to current, to voltage and back again to the frequency domain. Without clearly identifying the transfer functions of the system, one cannot properly investigate the limits of the design. This section provides a simplified model, which will help the reader to identify critical parameters in the proposed system.

2.3.1 Small-Signal Model of the Temperature Sensor with the FLL Readout

The small-signal model (Figure 2.7) assumes that the loop is tightly locked to the center frequency of the Wien-bridge. Two observations can be made based on this model. Firstly, the signal transfer function (STF) from the input of the WB (Δf) to the output of the FLL is bandlimited. Secondly, any unwanted perturbation coming from the VCO is high-pass filtered by a noise transfer function (NTF) (Figure 2.8). Note that the STF and NTF are scaled to the bridge's center frequency, which was chosen to be 600kHz ($R_{WB} = 125k\Omega, C_{WB} = 2.12pF$). For the proposed design, a division factor of N=4 was used, while having a 20pF integration capacitor. More details about the chosen values will be presented in the next chapter.

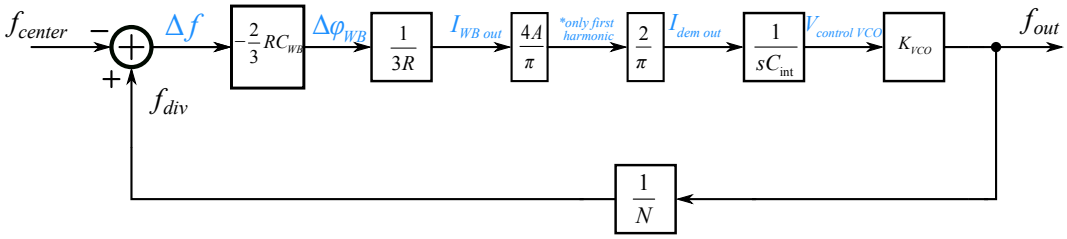


Figure 2.7: Small-signal model of the system

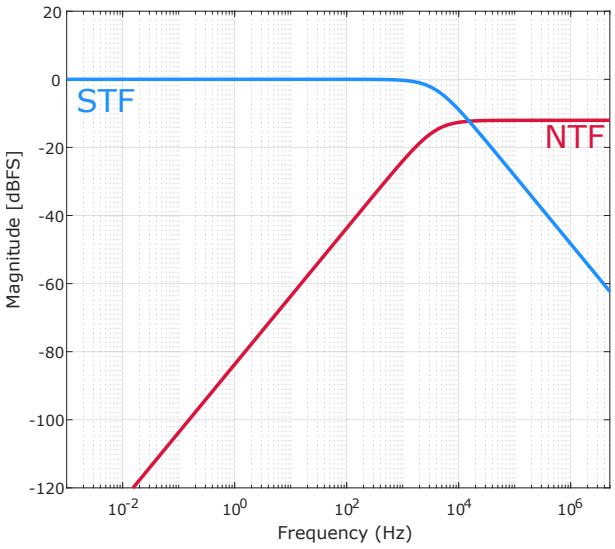


Figure 2.8: STF and NTF in the FLL

Based on the same small-signal model, the NTF from the bridge's output (or integrator's input) reveals that the noise coming from this point is low-pass filtered by the FLL. This means that a small bandwidth is desired to filter out the thermal noise generated by the bridge. However, this will increase the contribution of the VCO's noise to the output of the FLL. Since the VCO's noise is high-pass filtered by the loop, a large bandwidth will suppress the non-idealities coming from the VCO. The choice of the closed loop bandwidth is one of the most critical design parameters which impacts the performance of the system and involves a trade-off that the designer needs to take into account. Assuming that the sensor and the VCO are the dominant noise sources, it is essential to establish which of these two noise sources needs to be more aggressively suppressed. When the bridge's thermal noise is the dominant source, the loop bandwidth should be reduced. On the

contrary, if the VCO noise is dominating, the loop bandwidth needs to be increased. In this design, a small loop bandwidth to filter the thermal noise coming from the bridge was chosen, while keeping the integration capacitor size as small as possible, as it will be presented in the circuit implementation chapter (Chapter 3).

The resolution limit is set by the noise coming from the sensor and the noise coming from the readout. The equivalent output impedance of the bridge at the center frequency can be calculated as:

$$\mathrm{Re}\left\{Z_{out,WB}\right\} = \frac{12 \cdot R_{WB}}{5} \tag{2.10}$$

Based on this result, the power spectral density (PSD) of the WB's output current noise is given by:

$$S_{in,out,WB} = \frac{4 \cdot k_B \cdot T}{\mathrm{Re}\left\{Z_{out,WB}\right\}} = \frac{5 \cdot k_B \cdot T}{3 \cdot R_{WB}}, \tag{2.11}$$

where k_B is Boltzmann's constant and T is temperature. The bridge resistance value, R_{WB}, is equal to 125 $k\Omega$ for reasons that will be explained in the next chapter. Based on the small-signal model of the system (Figure 2.9), the NTF from the input of the integrator (output of the bridge) to the output of the FLL can be calculated as:

$$\frac{f_{\mathrm{out},FLL}(s)}{I_{\mathrm{noise}}(s)} = \frac{9 \cdot N \cdot \pi}{32 \cdot A \cdot C_{WB}}, \tag{2.12}$$

where N is the frequency divider value (N=4), C_{WB} is the capacitor from the Wien-bridge and A is the amplitude of the driving signal at the bridge's input.

To ensure that the readout's thermal noise contributes only 10% to the overall noise budget, a ratio of 3:1 is considered between the bridge's thermal noise and the readout's thermal noise. The PSD at the output of the FLL, S_{fout}, can be calculated by taking the total noise PSD from the input of the integrator and multiply it with the squared absolute value of the NTF (2.12).

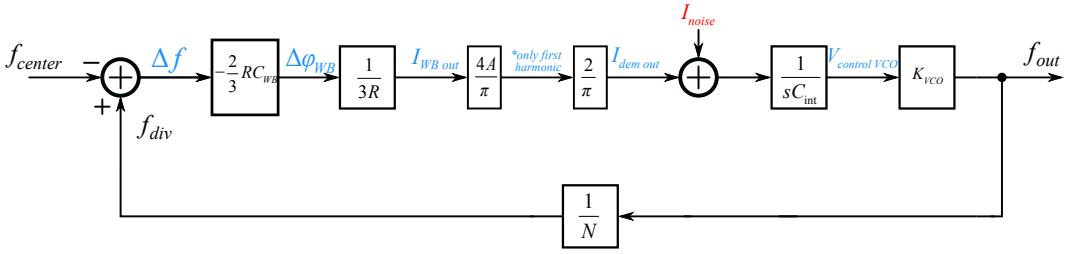


Figure 2.9: Small-signal model of the system with noise included

2.4 Source of Errors

Like any other feedback system, there are some errors which may limit the FLL's overall performance. In this section, these errors will be discussed, together with solutions to minimize their effect.

2.4.1 Integrator

$1/f$ Noise

The input referred $1/f$ noise of the OTA will change the control voltage of the VCO, therefore changing its output frequency and limiting the resolution of the system.

A solution to this problem is to use dynamic compensation techniques ([31]) such as chopping, which can be easily implemented in this design since it only requires adding 2 choppers (same polarity reversing switch used as the phase detector previously described) to the inputs and outputs of the amplifier. A brief explanation of the chopping principle is done with the help of Figure 2.10. The input signal is modulated by the chopping control signal ϕ_{chop}, amplified and then demodulated at the output of the amplifier. The $1/f$ noise of the amplifier (and its offset voltage) is modulated only once, which enables its filtering at the output of the amplifier.

Figure 2.11 illustrates how the chopping principle is applied in the proposed architecture. As shown in Figure 2.11, the bridge demodulator (A) and the input chopping switches (B) can be combined so as to avoid errors caused by the addition of extra resistance in series with the Wien-bridge [32].

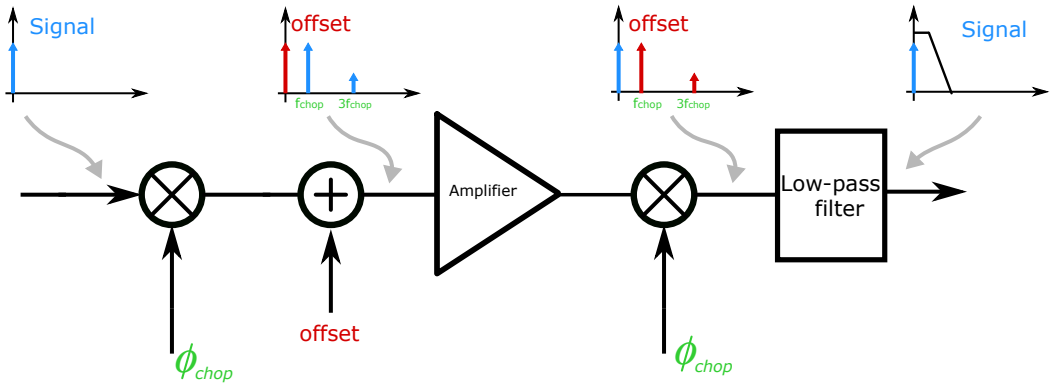


Figure 2.10: Chopping principle

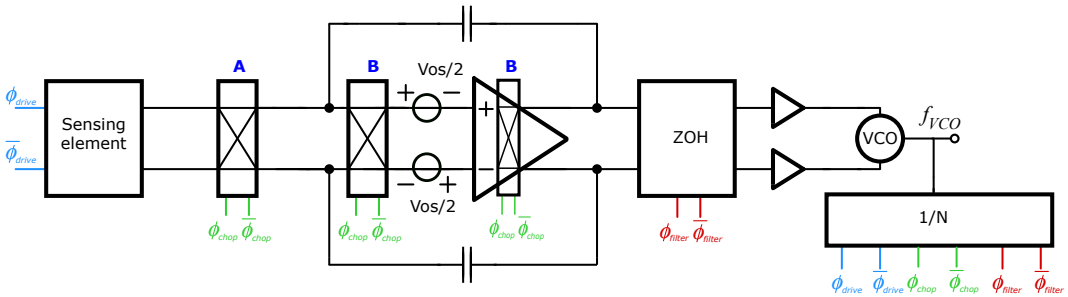


Figure 2.11: Chopping the amplifier's offset

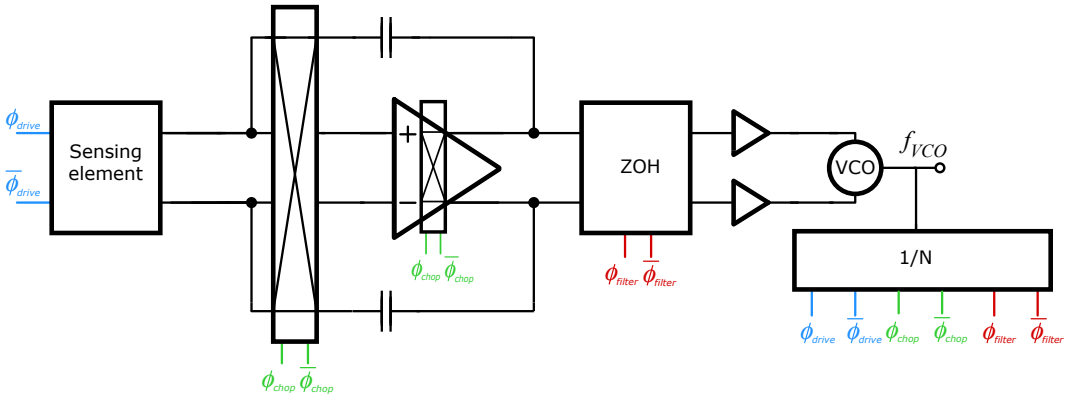


Figure 2.12: Merging the input chopper with the demodulator

In section 2.2.3, the choice of a ZOH after the integrator was motivated. However, additional care must be taken when considering an amplifier with offset. Figure (Figure 2.13) shows the output voltage of the integrator in the case of a zero-offset voltage (Vout offset-free) and in the case with finite

offset (Vout with offset). This behavior appears due to the fact that the offset voltage appears as a square-wave at the output of the integrator, and the chopping signal and the driving signal are 90° phase shifted.

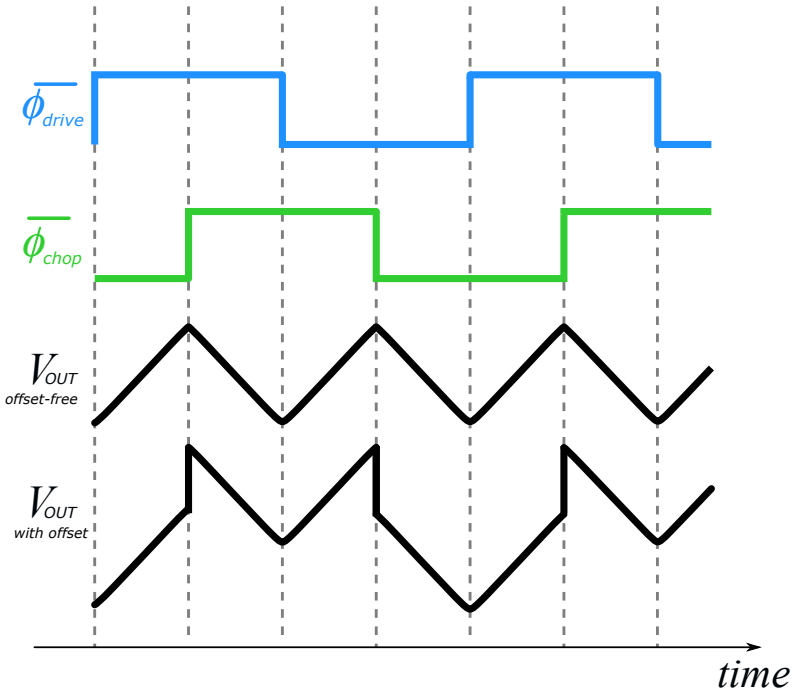


Figure 2.13: Offset effect at the output of the integrator

This could be a problem since the control voltage of the VCO should be as constant as possible. The sampling signal of the ZOH filter should be designed to avoid the fast transition moments (when the polarity reversal of the choppers causes an abrupt change in the output voltage of the integrator which is correlated with the offset). Figure 2.14 shows the implementation of the SC ZOH filter [30].

The input of the VCO, Vin VCO, is connected to Vout SH up or Vout SH down, depending on the value of the sampling signal of the SC filter, ϕ_{filter}. The sampling moment of the SC filter can be found by visual inspection of the waveforms (Figure 2.15). In order to have the input voltage of the VCO as constant as possible, ϕ_{filter} has to be equal to $\phi_{chop}/2$.

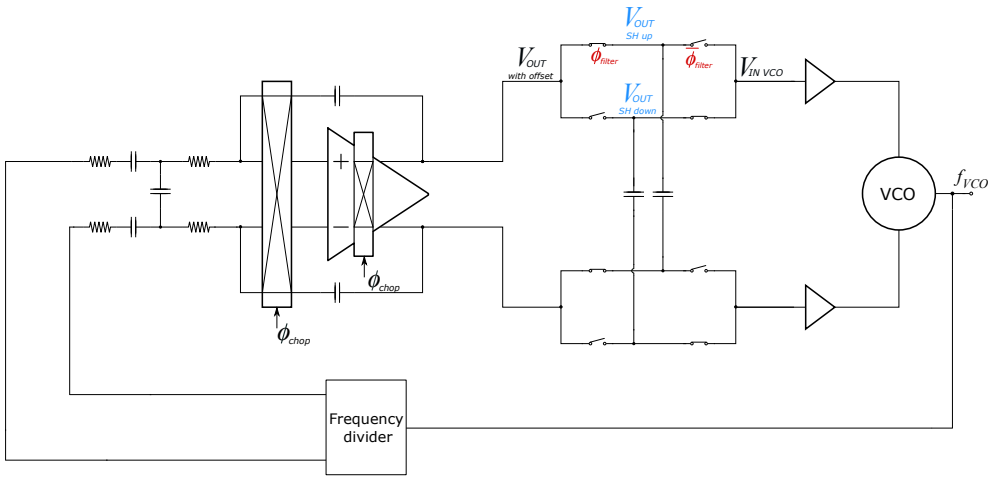


Figure 2.14: Block diagram of the proposed architecture with ZOH implemented

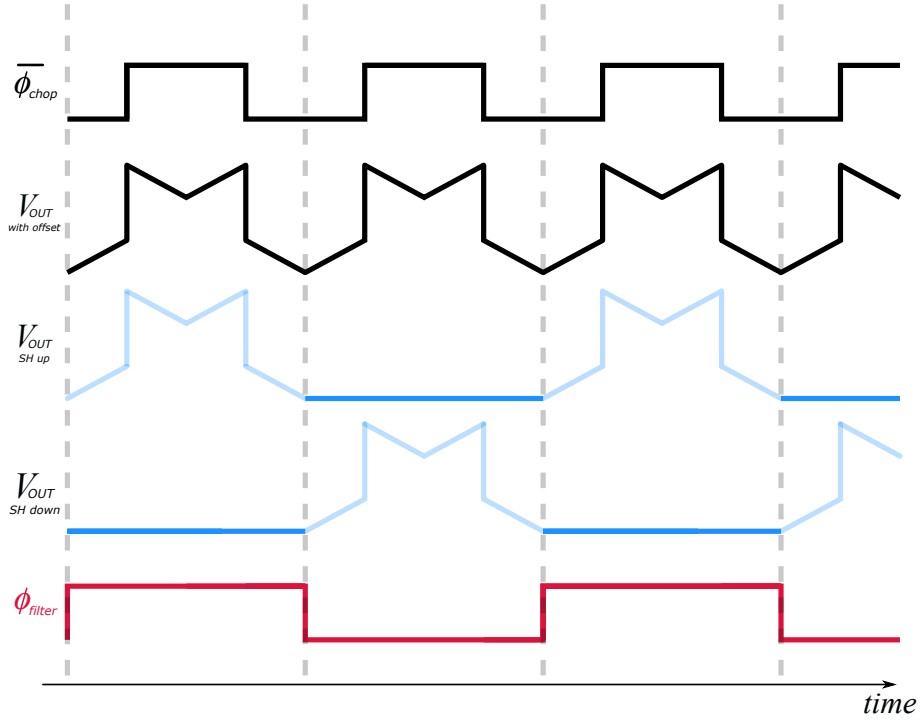


Figure 2.15: Choice of the sampling signal

Finite Gain

Another nonideality that must be taken into account is the finite gain of the integrator. As in any feedback system, the finite gain of the integrator

results in a steady-state error. However, since the spread of the Wien bridge resistors will be mitigated by calibration, this effect can also be minimized. On the other hand, this will only work well if the gain of the amplifier does not vary significantly over temperature and process corners, so care must be taken when designing the amplifier.

The finite gain effect can be analysed with the small-signal model shown in 2.7, where the integrator's transfer function is replaced by:

$$\frac{V_{\text{out}}(s)}{I_{\text{in}}(s)} = -\frac{\left(R + \frac{1}{sC_{\text{int}}}\right) \cdot A_o}{1 + sRC_{\text{int}} + A_0 \cdot (1 + sRC_{\text{int}})}, \tag{2.13}$$

where A_0 is the OTA finite gain.

Figure 2.16 illustrates the effect of finite gain on the NTF, showing minimal change in the STF. From this it can be concluded that a higher gain is desired in order to suppress any nonideality of the loop effectively.

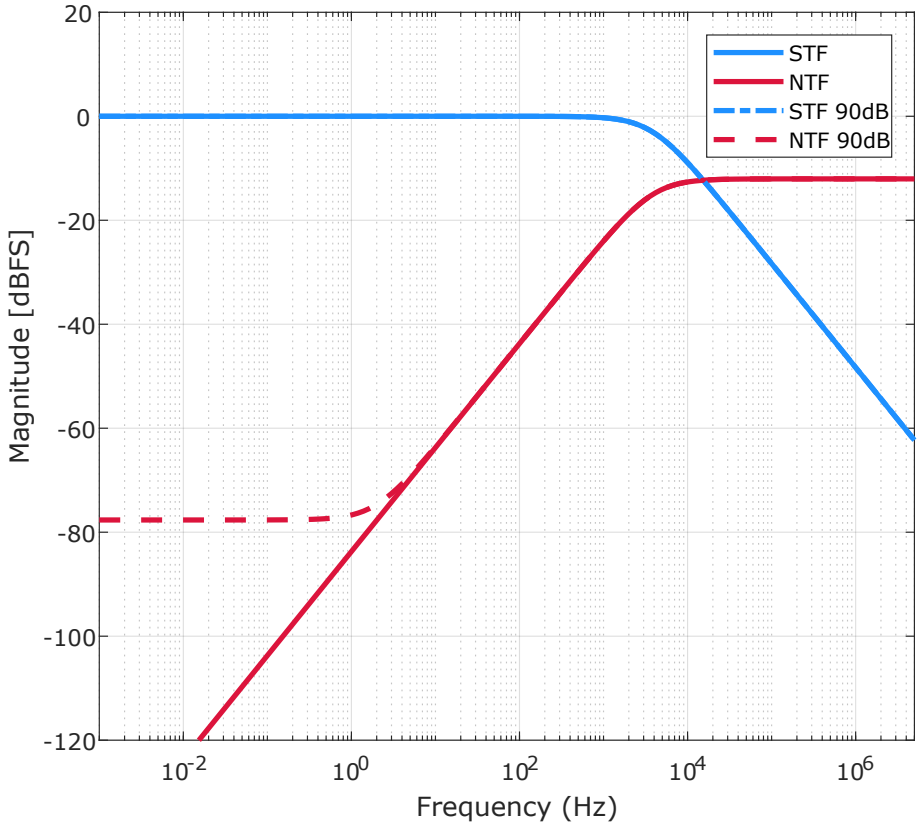


Figure 2.16: Finite gain effect seen in the NTF and STF

The same effect is apparent from the output spectrum (Figure 2.17), where it can be seen that the STF remains relatively unchanged for different gain values.

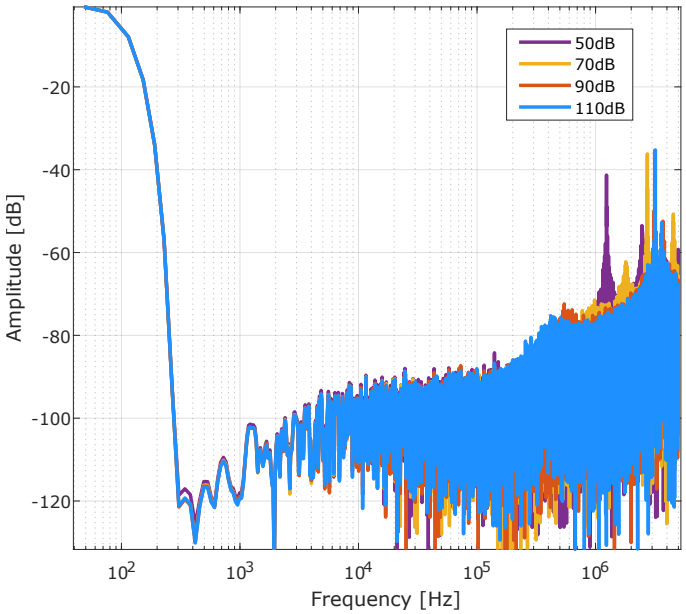


Figure 2.17: Finite gain effect seen in the output spectrum

2.4.2 FLL Operation and Concluding Remarks

This chapter concludes with the description of the proposed temperature sensor, illustrated in Figure 2.18. An FLL is built around a Wien-bridge, whose resistors are used as temperature sensing elements. A Wien-bridge is a band-pass filter with a phase almost linear around 0°, where its center frequency is defined. This inspires the idea of using the phase as an error signal to determine the difference between the center frequency of the bridge and the frequency driving the bridge. The FLL acts as a negative feedback loop that changes the driving frequency of the bridge such that the phase-response of the WB is 0°. After the loop has settled, the lock-frequency is equal to the center frequency of the bridge. The output of the FLL is then providing an N times higher frequency, where N is given by the frequency divider block.

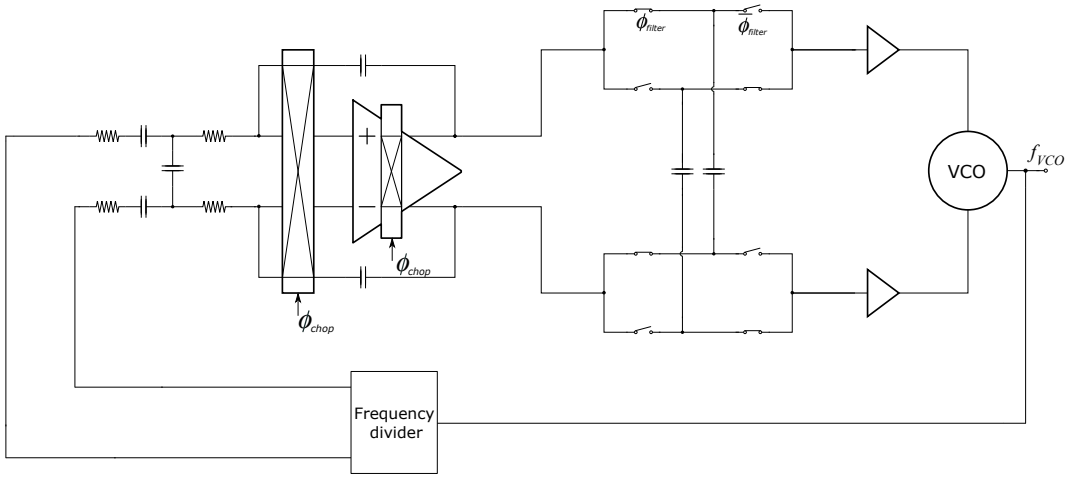


Figure 2.18: Block diagram of the proposed temperature sensor

Based on the analysis performed in this chapter, some design directions can be established. First, the Wien-bridge has to be designed while considering mainly its size and power; afterward, care must be taken not to limit its resolution with the amount of noise generated by the resistors. The readout circuitry should be designed to be as transparent as possible with respect to the properties of the sensor while investing a minimum amount of power and occupying a small area.

Chapter 3 Circuit Implementation

3.1 Sensor Circuit Design

The temperature sensor is the core of the entire system; therefore it needs to be carefully chosen when a set of performance specifications (Table 1.2) needs to be achieved. For convenience, the table will be added below so as to serve as a guideline for the design choices.

Specification	Value
Tech. node [nm]	0.18
Area [mm^2]	<0.1
Power [μW]	<30
Temp. range [$^\circ C$]	-40 - 85
Inaccuracy [$^\circ C$]	$\pm$0.12
Trim method	3
Resolution [mK]	<1
Conv. time [ms]	30
Res. FOM [pJK^2]	<0.21

Table 3.1: Target specifications for the proposed design

3.1.1 Resistor and Capacitor Types

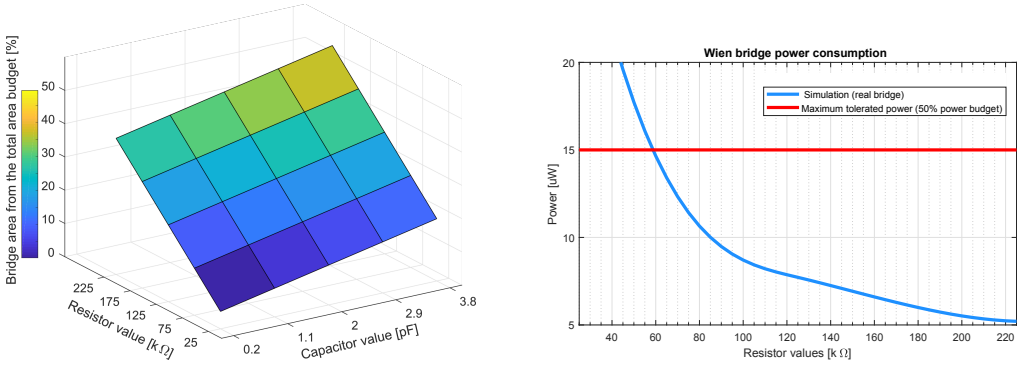
To maximize its sensitivity, the resistor used in an R-based temperature sensor should have a large temperature coefficient (TC). In CMOS technology, the n-well and the silicide resistors have the highest TC, so they are a valid design option from this point of view. In addition to their temperature dependency, resistors are also voltage dependent. This dependency should be as low as possible (below 0.1°C) in order to minimize their sensitivity to power supply variations.

Another important aspect is the possibility of compensating for process spread and the non-linear temperature dependence by calibration. Based on previous measurements [33], the silicided p-poly resistors achieve the highest accuracy after calibration. As explained in Chapter 2, the bridge capacitors were realized with metal-insulator-metal (MiM) capacitors since they are almost stable with temperature.

3.1.2 Power and Area Constraints

In the previous paragraph, the advantages of the silicided p-poly resistor were emphasized. However, this type of resistor suffers from a significant drawback: its sheet resistance is quite low compared to other resistors ($7.9\Omega s/square$). To minimize the area occupied by the resistors, minimum-width silicided p-poly resistors are used ($0.42\mu m$). In the case of the MiM capacitor, its density is equal to $2fF/\mu m^2$. In addition to this, especially for a compact design, it is imperative to find a good trade-off between the area occupied by the bridge and the one filled by the readout. A good starting point would be to split the entire area budget ($0.1mm^2$) into two, to give equal weight to the sensor and to the readout circuitry. Figure 3.1(a) illustrates some of the possible combinations for the Wien-bridge components which fit in half of the total area budget. The area estimation was done by using the Virtuoso Layout Generator tool to extract the layout of the resistors and the capacitors. For a first-order estimation, at least 1/3 of the area occupied by the resistors and the capacitors was reserved for routing and spacing.

The total power budget ($30\mu W$) is another factor that will be used to rule out some of the component sizings. As done with the area budget, the power budget can be split equally to the bridge and the readout 3.1. Figure 3.2 illustrates the setup used for simulating the Wien-bridge power. This setup assumes that an ideal readout is implemented so that the outputs of the bridge are connected to a virtual ground node. The inputs of the bridge are driven with square waves switching between 0V and 1.8V with a frequency equal to the Wien-bridge center frequency.



(a) Area (b) Power

Figure 3.1: Wien bridge area and power

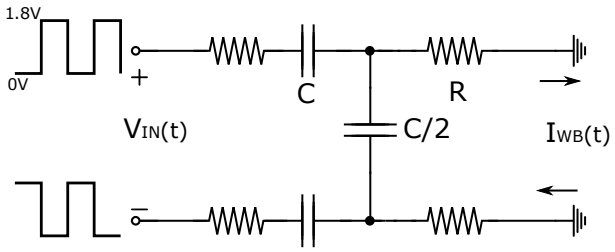


Figure 3.2: Testbench for simulating the Wien-bridge power

From Figure 3.1(b), a resistor value below 60 kΩ would lead to higher power consumption than the maximum tolerated value; consequently it can not be chosen.

3.1.3 Effect of Parasitic Resistances and Capacitances

A significant limitation in the choice of the Wien-bridge components sizing is the influence of parasitic effects on the filter's transfer function. Figure 3.3 shows the center frequency of the bridge as a function of resistor and capacitor values. The dashed lines correspond to the center frequency of an ideal bridge, whereas the solid ones represent the simulated center frequency of the real bridge, with parasitic resistors and capacitors included from the layout extraction (first-order estimation). From this graph, it can be seen that the difference between each of the two frequencies (ideal versus real bridge) decreases as the resistor is reduced or/and the capacitor is increased, as expected. Another limitation on the frequency value comes from the

fact that the center frequency of the bridge needs to be higher than the flicker-noise corner frequency from the readout circuit; so that this can be suppressed by chopping. In CMOS technology, MOS devices have a corner frequency of about 100kHz, setting the lower boundary for the frequency of the bridge. Simulation results showed that the upper limit for the Wien-bridge frequency is around 600kHz and a minimum capacitor value of 2pF has to be chosen so as to avoid high degradation of the filter's phase response due to parasitic effects. After the finalization of the design for this project, a new SOTA design [22] has been published recently, which proves that a Wien-bridge with a center frequency of 500kHz (R=64kΩ and C=5pF) can achieve a resolution of 0.46mK in 10ms. The design consumes 52uA and has a total area of 0.12 mm^2, from which the Wien-bridge occupies 25% 1.1. This is in good agreement with the presented analysis.

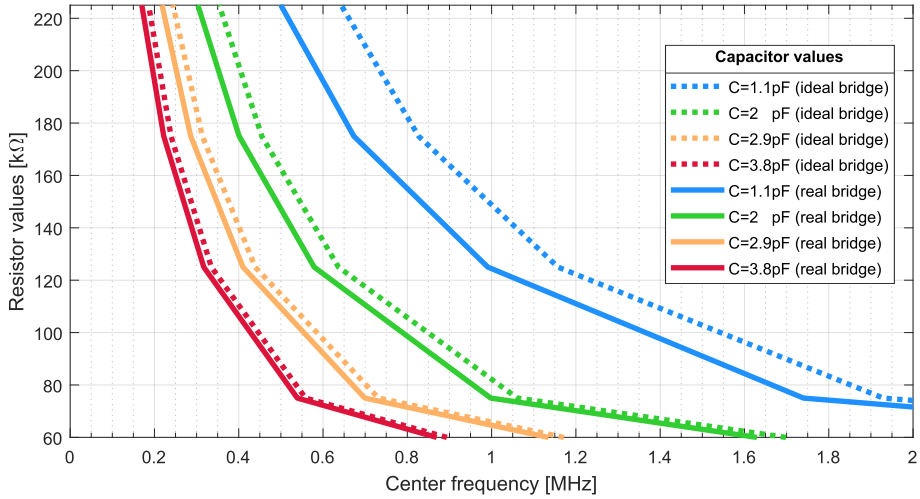


Figure 3.3: Center frequency of the Wien bridge for different resistor (min. width silicided p-poly) and capacitor (MiM) values

3.1.4 Resolution

The output referred current noise of the bridge should be the limiting factor of the resolution in specific given conversion time. Design [3] achieved a resolution of 2.8mK in 32ms conversion time. Since this design has the lowest power consumption from Table 1.1, one of the targets of the proposed

design is to achieve lower resolution (<1mK) in the same or even shorter conversion time with similar power consumption. Since the TC of the 135 kΩ resistor used in [3] is half of the TC of a silicided p-poly resistor, the expected resolution for this design should be at least 2 times better if the resistor has a similar value based on the fact that the FLL's sensitivity, given by 3.1, is two times higher.

$$S_{WB} = \frac{df}{dT} = \frac{df}{dR} \cdot \frac{dR}{dT} = -\frac{TC \cdot N}{2\pi R_{WB} C_{WB}}, \tag{3.1}$$

with N being the frequency divider ratio and it is equal to 4 for both designs.

3.1.5 Sensor Design Concluding Remarks

By taking into account all the constraints presented in this section, the resistor value chosen is 125 kΩ, and the capacitor value is equal to 2.12pF.

The center frequency was chosen to be the maximum value for which parasitic influence can be considered acceptable. The motivation for pushing the center frequency to the highest value possible is linked with the ripple present on the integrator's output as a consequence of the phase detection operation. Since the ripple has a frequency equal to double the bridge's frequency, a higher value of the center frequency results in a lower integration capacitor size and/or a relaxation of the ZOH filter requirements. One last step in the characterization of the bridge is to link its frequency with temperature, as shown in the Figure 3.4.

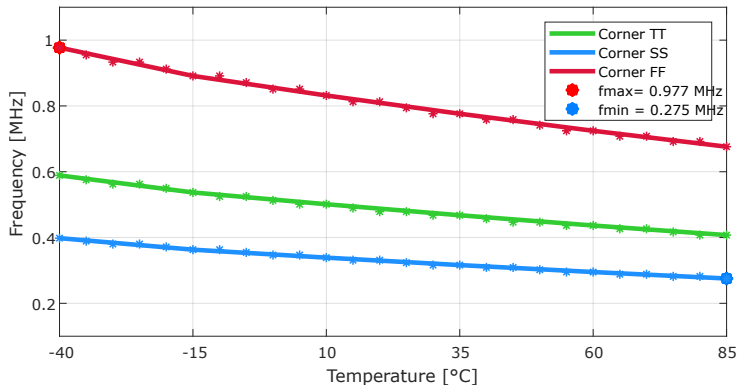


Figure 3.4: Center frequency of the Wien-bridge as a function of temperature

3.2 Continuous-Time Readout Circuit Design

In this section, the FLL's blocks will be described at the circuit level, while emphasizing some of the design parameters which were considered.

3.2.1 Voltage-Controlled Oscillator

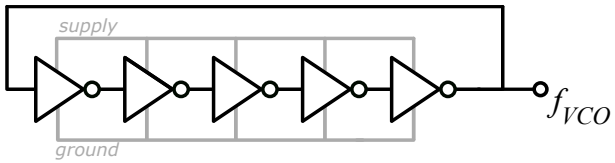


Figure 3.5: VCO circuit diagram

The System Analysis chapter (Chapter 2) revealed that the VCO's non-linearity and noise are, to a certain degree, suppressed by the loop, so the main focus of this design is to keep the VCO's power consumption to a minimum level. A ring-oscillator type of VCO with 5 inverter stages (Figure 3.5) was chosen because it can perform the function of a voltage-to-frequency converter with low power consumption and within a small area. Besides, being based on inverters, its area can be further reduced in more advanced technologies. There are numerous design parameters that can influence the performance of the VCO, some of which are reviewed next.

Tuning frequency range

One of the key specifications of a VCO is its tuning range, meaning the range of frequencies that the VCO needs to cover. In this application, the VCO's output frequency needs to be four times (the frequency divider value) higher than the center frequency of the bridge over all corners and temperatures. Linking this information with (Figure 3.4), $f_{VCO\_MAX} > 4MHz$ and $f_{VCO\_MIN} < 1.1MHz$. Figure 3.6 shows that in order to cover the desired frequency range, the VCO was designed so as the control voltage lies between 600mV and 1.2V.

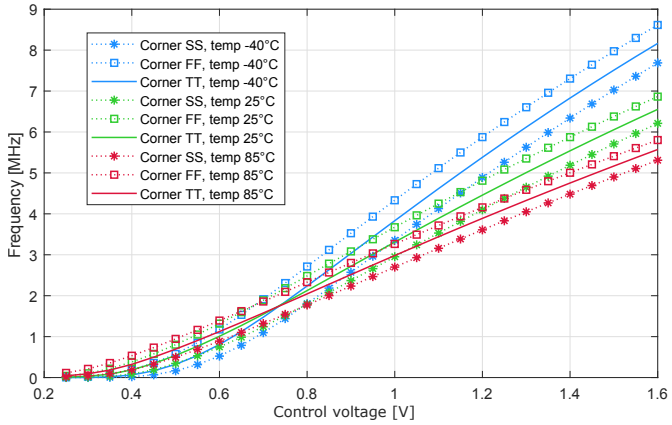


Figure 3.6: VCO's tunning frequency

VCO Gain Non-linearity

The VCO gain, K_{VCO}, defines how much the output frequency f_{VCO} changes for a change in the input voltage V_{TUNE}:

$$K_{VCO} = \frac{df_{VCO}}{dV_{IN}} \approx \frac{f_{VCO\_MAX} - f_{VCO\_MIN}}{V_{TUNE\_MAX} - V_{TUNE\_MIN}} \tag{3.2}$$

The VCO gain should be as constant as possible over the tunning range and over temperature and corner variations. From Figure 3.7 it can be seen that K_{VCO} changes less than 2 times its value over temperatures and has similar behaviour over corners.

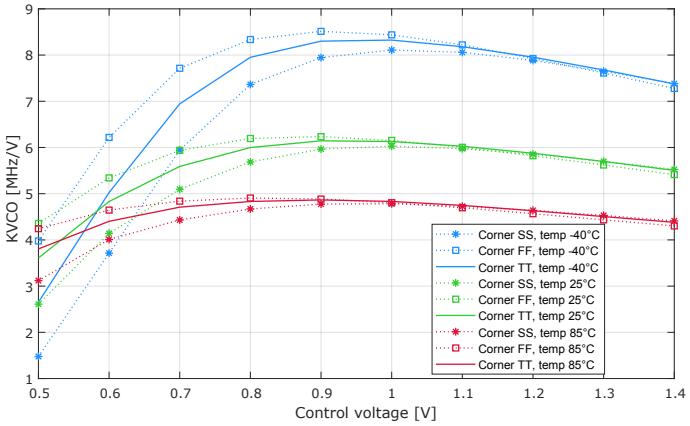


Figure 3.7: VCO's gain nonlinearity

Supply Voltage Effect

A single ended ring-oscillator implementation suffers from bad PSRR. Driving the VCO in a fully-differential approach could provide, to a certain extent, a reduction in noise coming from the supply lines. Based on these observations, the VCO is driven by using a current-steering type of implementation, as shown in Figure 3.8. The loop filter changes its output in order to steer more/less current into the VCO. The current mirrors were implemented with a cascode-type of structure, so as to reduce even more the effect of the supply noise. Furthermore, in order to minimize noise coupling from the substrate, deep n-well MOS transistors available in this technology were used for which the bulk of the nMOS transistor can be tied directly to the transistor's source.

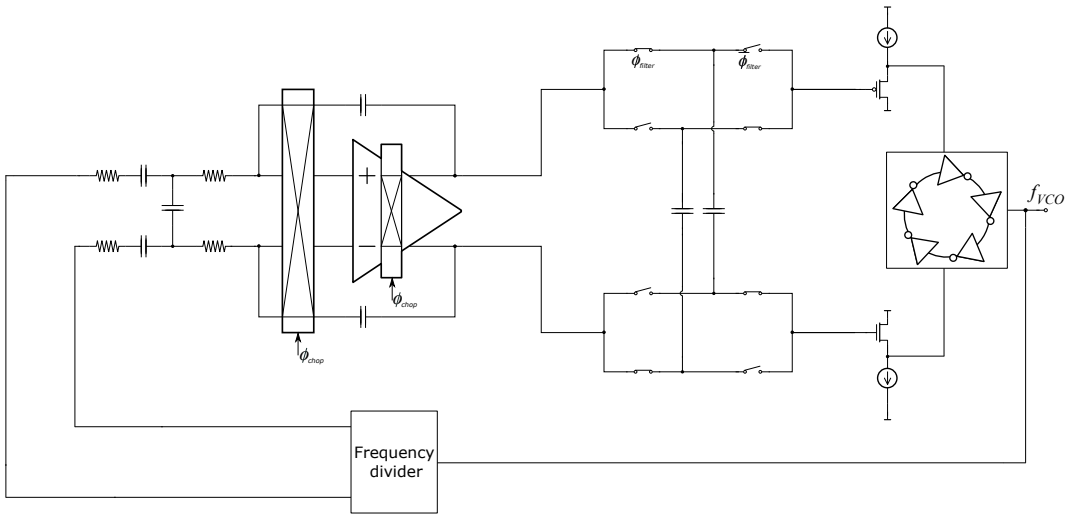


Figure 3.8: FLL circuit implementation

3.2.2 Integrator Implementation

As it was shown in the previous section, the **output swing** of the integrator should be high enough to accommodate the ring-oscillator. In addition to this, the System Analysis Chapter (Chapter 2) revealed that the gain of the amplifier defines the aggressivity of the FLL's NTF, so a **high gain** is desired. These two observations can be used as an indication of the amplifier's

topology choice: a two-stage Miller amplifier fulfills both these requirements [34].

The power budget of the amplifier is divided as follows: the second stage has to provide an output current equal to the one coming from the Wien-bridge, while the first stage is designed based on **noise** considerations. In this design, the ratio between the sensor's noise and the noise of the readout circuitry was kept at a value equal to 3. To keep the **power** as low as possible, a current re-use topology [35] is implemented (Figure 3.9).

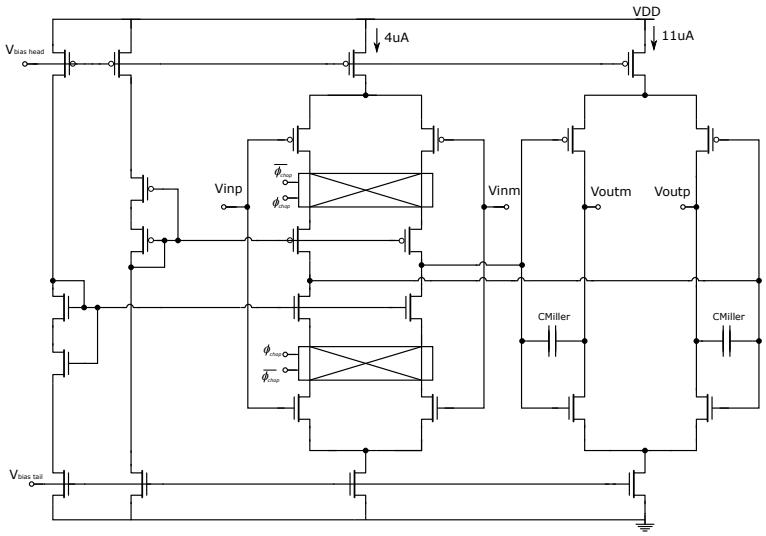


Figure 3.9: Circuit implementation of the amplifier

When the sensor is connected to the readout, the phase response of the Wien-bridge has to remain unchanged. However, the **finite input impedance** of the amplifier can change the transfer function of the bridge. In order to keep this effect at a minimum value, a ratio of at least 100 should be maintained between the output impedance of the bridge and the input impedance of the integrator [36]. As discussed in Chapter 2, the output impedance of the bridge is given by:

$$\mathrm{Re}\left\{Z_{OUT,WB}\right\} = 12R/5 \tag{3.3}$$

In this design, the input impedance of the integrator has a value of $\simeq 1.4k\Omega$, maintaining a ratio of more than 200 between the two impedances

(figure 3.10).

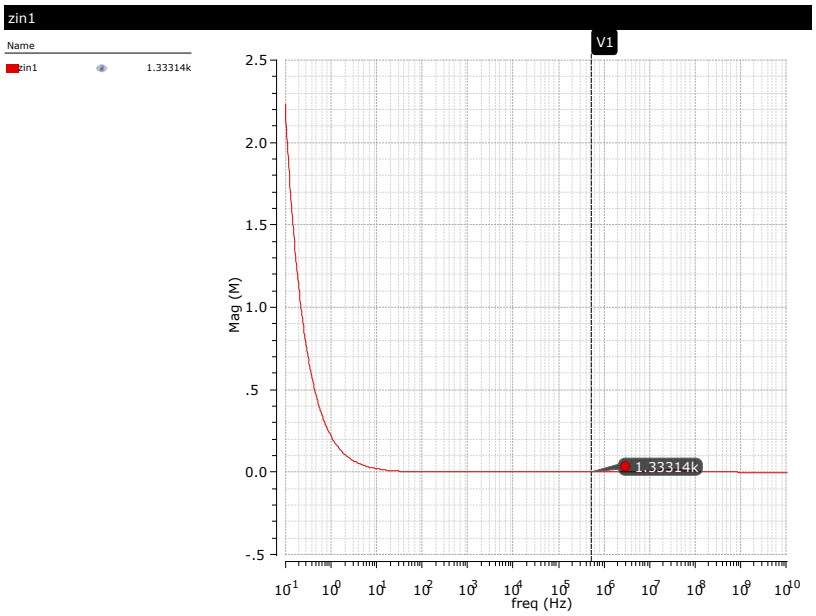


Figure 3.10: Input impedance of the amplifier

As it can be deduced from the above-mentioned requirements, the transconductance value is a critical design variable that can determine the performance of the amplifier. This motivates the use of a **contant-gm biasing** circuit (Figure 3.11) to bias the transistors with minimum dependency on temperature, process or supply variation [34].

Figure 3.12 shows the amplifier's gain variation over the temperature range in all process corners.

3.2.3 Integration Capacitor Size

From the system analysis presented in the previous chapter, the major challenge regarding the FLL design is to achieve a small noise bandwidth. This translates into large time constants for the integrator. However, if the integration capacitor is increased, it becomes the major area contributor. In this design, the integration capacitor size was set to be the minimum size for which the FLL locks to the frequency corresponding to the temperature

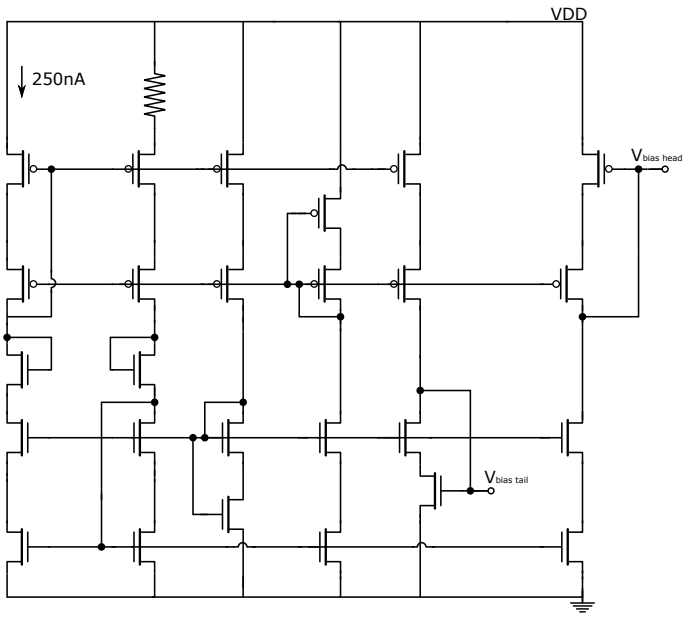


Figure 3.11: Circuit implementation of the constant-gm biasing

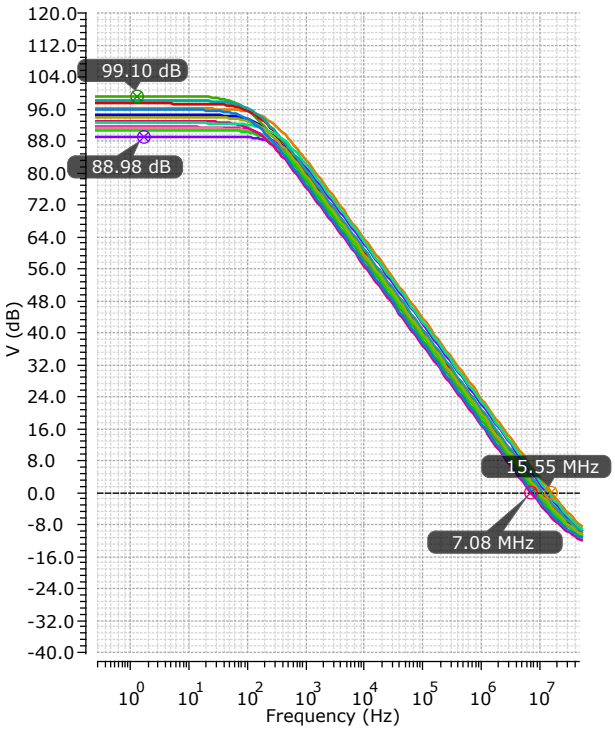


Figure 3.12: Amplifier's gain over corners and temperatures

information. Figure 3.13 shows the FLL's output frequency when a voltage step is applied at the input of the VCO, for different values of the integration capacitor. Since for $C_{int} = 10pF$ the loop exhibits a small overshoot which is exacerbated over temperatures and corners, a value of 20pF was chosen so as to guarantee that the loop locks over the entire operating range.

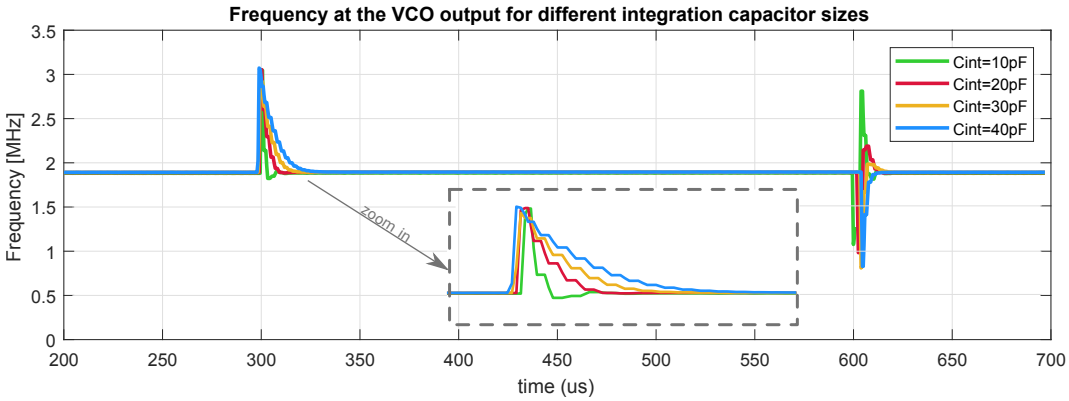


Figure 3.13: FLL step response for different integration capacitor values

3.2.4 Level Shifter and Frequency Divider

A level shifter is needed at the output of the VCO to perform the voltage level transition between the ring oscillator's output voltage and the supply voltage. The implementation displayed in Figure 3.14 is used because both the local supply and ground of the VCO are different from the voltage supply or ground of the system. The circuit is based on a sense amplifier type of read-out where the stored latch value is over-written by the input comparators.

The frequency divider, as the name suggests, implements the division of the output frequency of the VCO by N times so that the output frequency of the FLL can be compared with the bridge's center frequency. However, since the SC filter samples at half the filter's frequency, an additional division factor is added. In order to reduce the timing errors between all the loop's control signals, D flip-flops are used to implement the frequency divider.

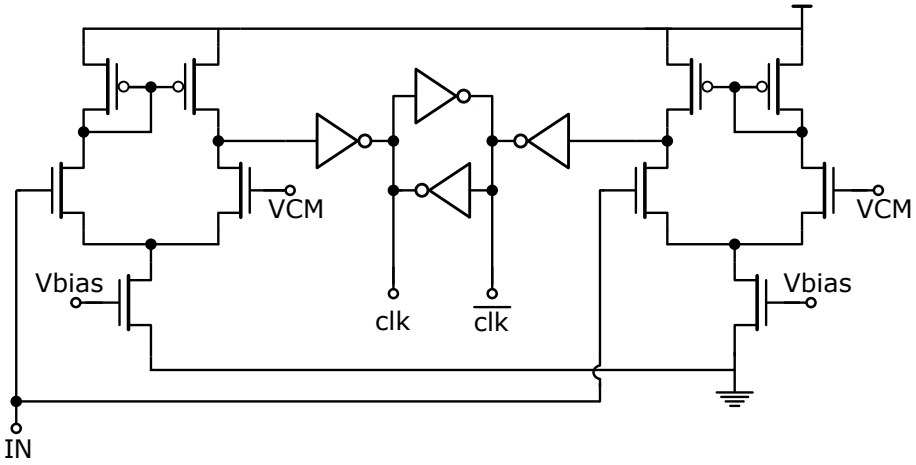


Figure 3.14: Level shifter schematic

3.3 Continuous-Time Readout Simulation Results

3.3.1 Transient Behavior and Sensitivity

The transient behaviour of the loop over corners and temperatures is illustrated in Figure 3.15:

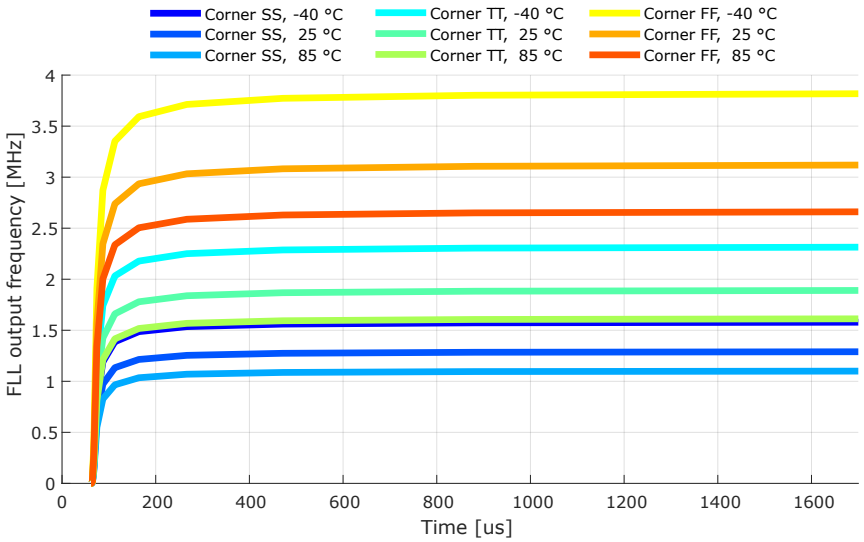


Figure 3.15: FLL output frequency vs. time

From Figure 3.16, the sensitivity of the output frequency can be calculated, which is in accordance with the one derived when the stand-alone Wien-

bridge was analyzed (Figure 3.4).

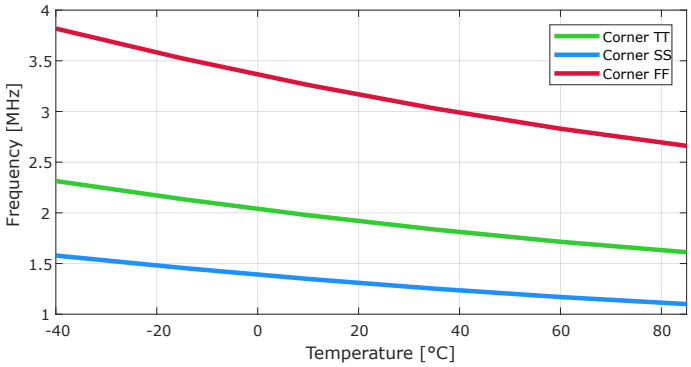


Figure 3.16: FLL output sensitivity

3.3.2 Resolution

Figure 3.17 shows the output spectrum of the FLL extracted from transient simulations with and without noise. Since the simulation time is very long for this type of circuit, the output spectrum was extracted so as to give an estimation of the performance and to provide information about the limitations of the design. The output spectrum reveals that there was no notable difference between the output of the noise-free FLL and the one when noise was introduced, meaning that the design is still quantization noise limited for the simulated time. A longer simulation time would be needed in order to achieve a thermal-noise limited resolution. Unfortunately, only a limited amount of data points were stored due to the long simulation time required for a noise simulation. In this case, for a bandwidth of 10kHz, an Effective-Number of Bits (ENOB) equal to 16.5 was achieved. Moreover, the output spectrum shows a first-order noise shaped characteristic caused by the frequency-to-digital converter (FDC), as it will be described in the next chapter.

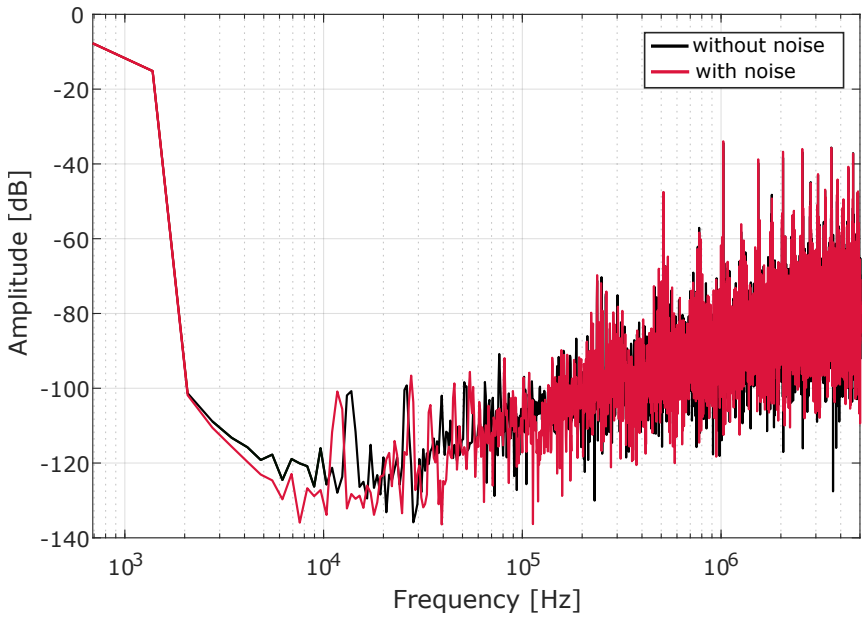


Figure 3.17: Output spectrum with and without noise

3.3.3 Inaccuracy

The accuracy of the temperature sensor was estimated based on Monte-Carlo simulations. The high simulation time limits the number of runs that can be simulated, so a number of 5 runs was chosen. Figure 3.18 shows the output of the FLL versus temperature for the simulated runs.

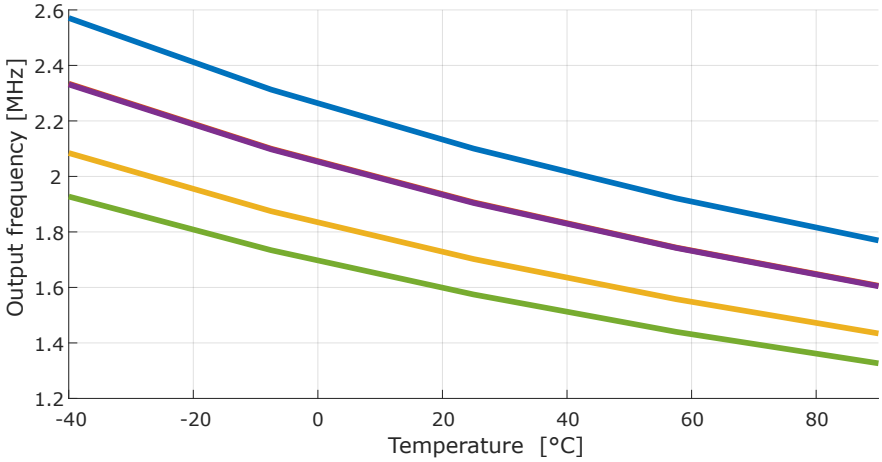
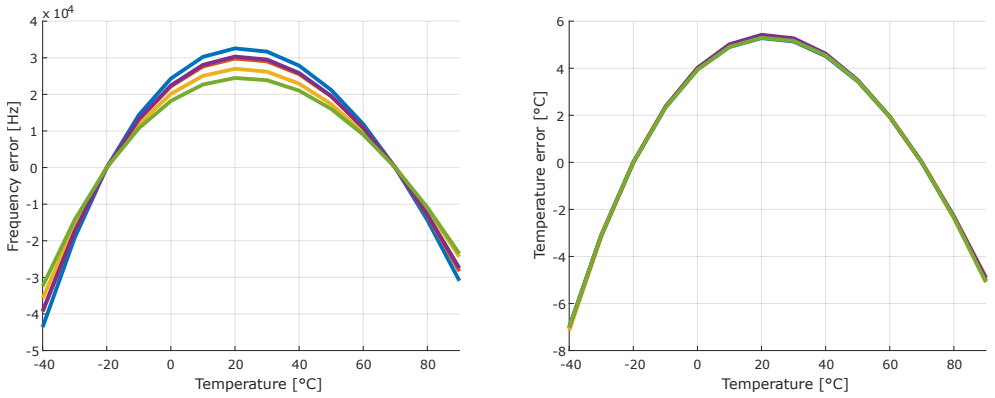


Figure 3.18: FLL output frequency MC (5runs)

A first-order polynomial fit (based on a least-squares method) is assigned to each curve. By making the difference between the simulated characteristic and its polynomial fit curve, the frequency error is obtained (Figure 3.19 (a)). The frequency-to-temperature sensitivity translates the frequency error into temperature error (Figure 3.19 (b)).



(a) Frequency error (b) Temperature error

Figure 3.19: Frequency error and temperature error after 2-point trim

After a systematic error removal, the simulated inaccuracy has a value of 0.12°C (Figure 3.20).

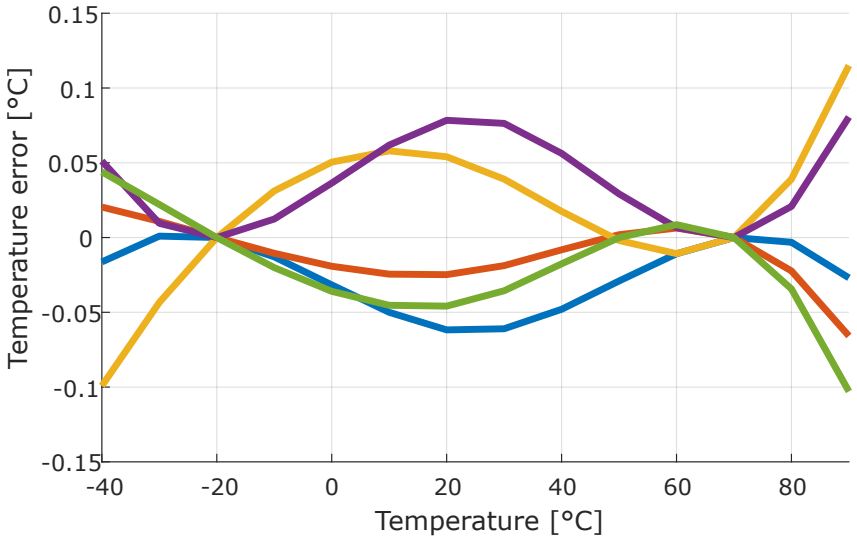
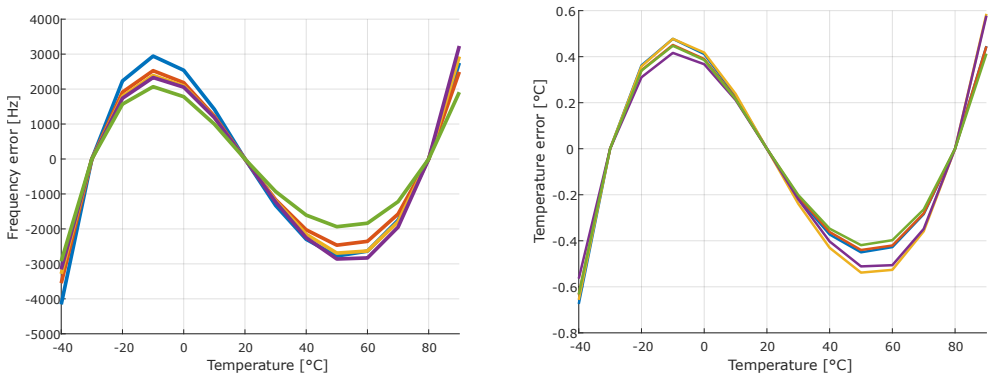


Figure 3.20: Temperature error after 2-point trim and systematic error removal

If a second order polynomial fit is performed (equivalent to a 3-point trim, 3.21), the inaccuracy value is reduced to below 0.1°C (Figure 3.22).



(a) Frequency error (b) Temperature error

Figure 3.21: Frequency error and temperature error after 3-point trim

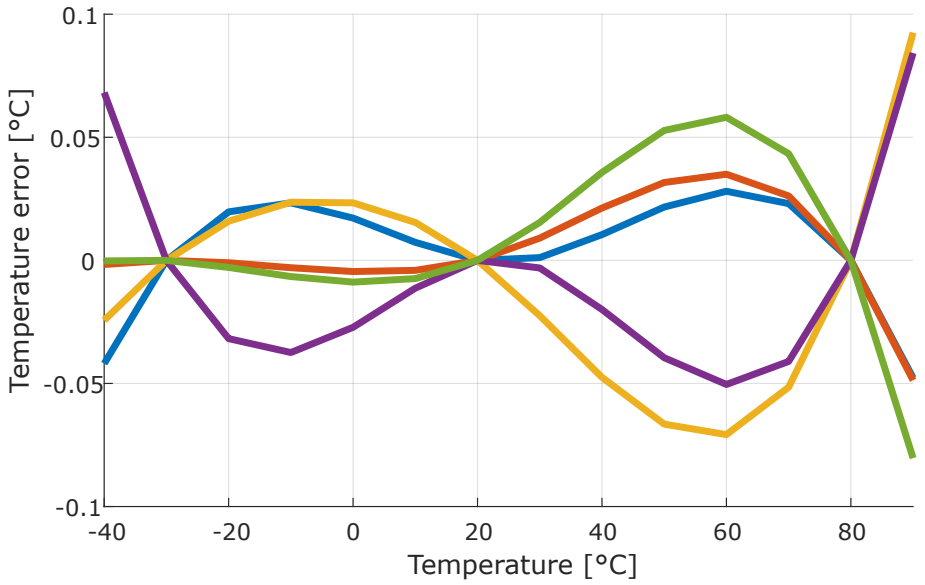


Figure 3.22: Temperature error after 3-point trim and systematic error removal

3.3.4 Supply Sensitivity

The supply sensitivity of the sensor was analysed by applying a sinusoid of amplitude 100mV and 100kHz frequency on the supply. At this design step, an issue with this type of circuit was discovered. Figure 3.23 reveals that the supply variation can significantly degrade the performance of the design.

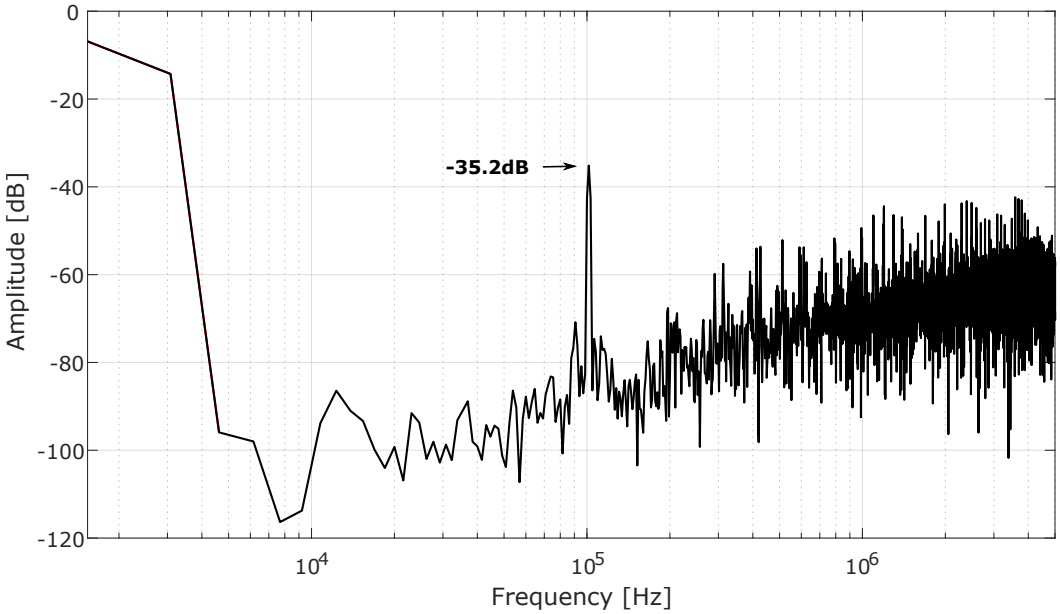


Figure 3.23: Output spectrum of the FLL with supply variation (100kHz)

The great impact of the supply variation is mainly caused by the mismatch in the current-steering driving circuit of the VCO, so a solution is required in order to overcome this limitation. Another possibility to drive the VCO was investigated, and it is presented in Figure 3.24. Here, a flip-around amplifier was used to perform the same function as the current-steering driving circuit and the SC passive filter. The same amount of current was used in the flip-around amplifier (single stage, current re-use topology with $8\mu A$ in total). The VCO acts as a resistive load for the OTA, which degrades its gain and performance; however, all the nonidealities are suppressed by the gain of the integrator. This implementation still uses a double sampling procedure at a frequency equal to half of the chopping frequency so that the ripple is effectively removed.

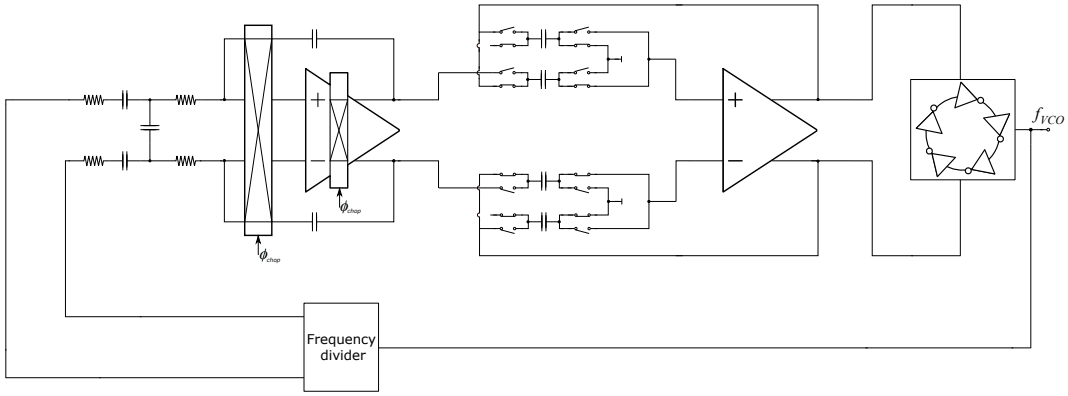


Figure 3.24: Improving the supply sensitivity: the flip-around amplifier

Simulations showed that indeed, with the flip-around amplifier the impact of the supply variation decreases (Figure 3.25).

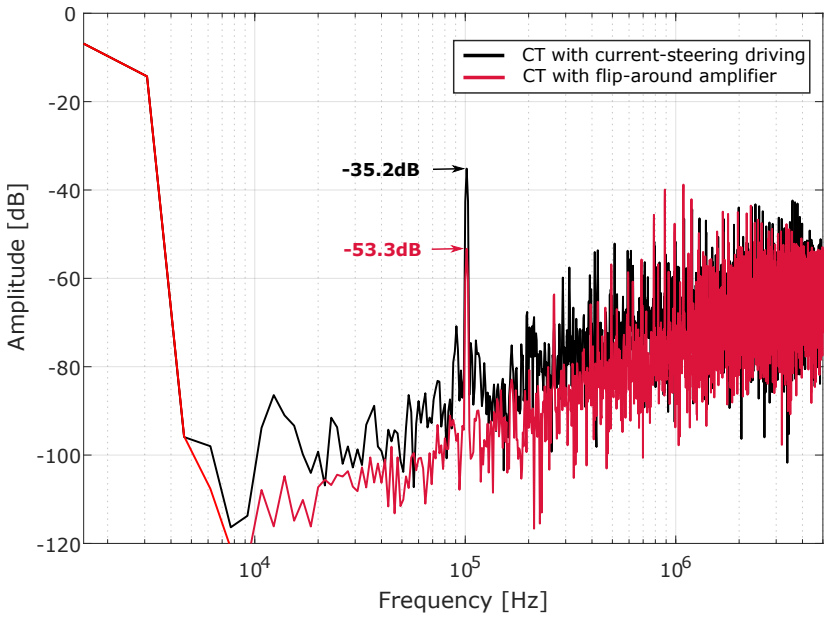


Figure 3.25: Output spectrum with supply variation (100kHz)

3.3.5 Power and Area Concluding Remarks

Figure 3.26 presents the power and area breakdown of the implemented design extracted from simulations. The area estimation is done with the help of the Layout Generation option provided by Virtuoso XL Layout Editor; a layout extraction of the blocks is performed while leaving some margin for routing and spacing between the components. For the main area contributors, the Wien-bridge and the integration capacitors, at minimum 1/3 of their area is left for routing and spacing.

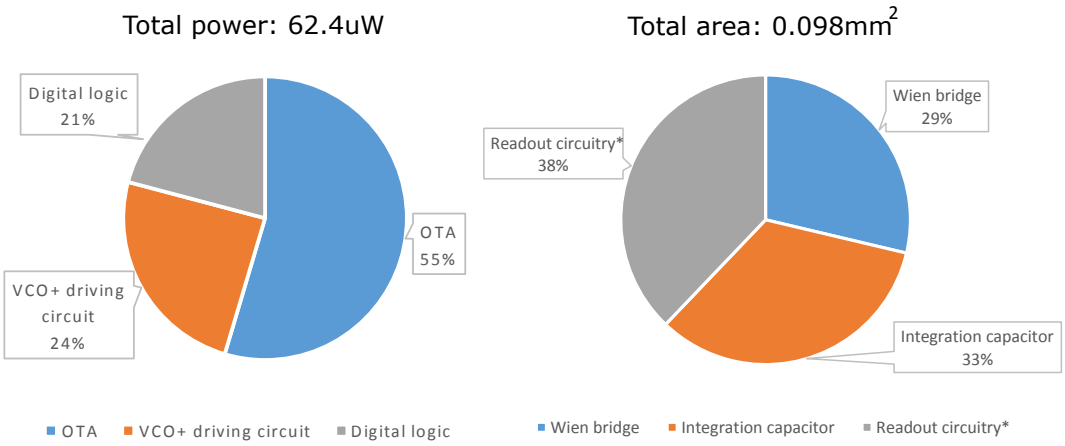


Figure 3.26: Power and area breakdown (1)

The estimated area budget is below the targeted one ($0.1mm^2$), with its main contributors still being the readout circuitry with the integration capacitors included. Since the power budget achieved was double the targeted value ($30\mu W$), some comments about the main power contributors are required. Simulations showed that the current coming from the bridge has a maximum value of 5.5µA over corners and temperatures. Assuming that the noise of the amplifier is dominated by the first stage, in order to keep a ratio of 3:1 between the sensor's noise and the readout's noise rms values, the amplifier needs a power allocation of $30\mu W$, which is a compromise for the targeted specifications. The only way to reduce this power with the same architecture is to use a higher resistor value so that the noise limitation comes only from the sensing element, but with an impact on the resolution of the application.

3.4 Switched-Capacitor Readout Circuit Design

While looking at the area breakdown of the previous implementation, one can observe that the integration capacitors occupy the same area as the sensing element. This is not an optimum design, since, as stated at the beginning of this chapter a good design should aim to have half of the area reserved for the sensor and half for the readout. The next question is what can be done to reduce the area occupied by the integration capacitors? In the System Analysis chapter, the reason for using high capacitor values was motivated: in order to filter out the noise coming from the sensor; the FLL has to have a small loop bandwidth, so large RC constants for the integrator are required. While the previous section was exploiting the proper sizing of the integration capacitor, this section will explore the other possibility: implementing a resistor with a higher value, therefore a higher time constant for the integrator.

3.4.1 Changing the Sensor-readout Interface

A method of implementing high resistors on a chip is by using a switched-capacitor (SC) resistor implementation (Figure 3.27). The operation can be briefly explained as follows: the capacitor C is charged and discharged by opening and closing of the switches which are driven by a signal with a sampling period of T. The average current can be calculated, and it is equivalent to the one passing through the resistor. This implies that the capacitor basically replaces the resistor. The resistance value depends on the sampling period of the signal that drives the switches and the capacitance value. The lower the sampling frequency or, the lower C is, the higher the equivalent resistance is.

The System Analysis Chapter began with the motivation to use a BPF as the sensing element. However, a BPF is the combination of an LPF and an HPF. Starting again from this point, one can change the Wien bridge filter (Figure 3.28 (a)) to the one from Figure 3.28 (b). From that, the resistor R_2 can be replaced by an equivalent SC resistor, effectively increasing the resistance value. Since resistors were used to sense the temperature, in order

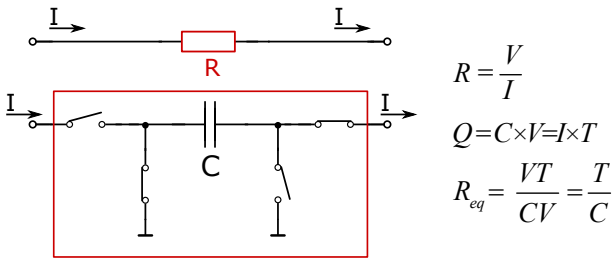
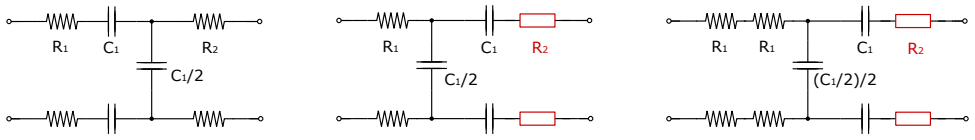


Figure 3.27: SC equivalent resistor

not to reduce the sensing area, the resistor R_2 is shifted in series with R_1. The capacitor value is sized so as to keep the same cut-off frequency.



(a) Step 1 (b) Step 2 (c) Step 3

Figure 3.28: Changing the sensor's implementation

It is necessary to analyze if the modified structure of the sensing element has the same behavior in temperature as the Wien-bridge. This can be done by looking at Figure 3.29 and following the reasoning described next. If the temperature increases, the value of R_1 increases, so the cut-off frequency of the LPF decreases. If this happens, the loop will lock to a lower frequency. The sampling signal which drives the SC resistor is derived from the loop so that it will follow the same direction as the FLL's frequency. A lower sampling frequency leads to a higher equivalent resistance value. This implies that the cut-off frequency of the HPF formed by C_1 and R_2 will decrease and that the FLL will still lock to a lower frequency when the temperature is increased.

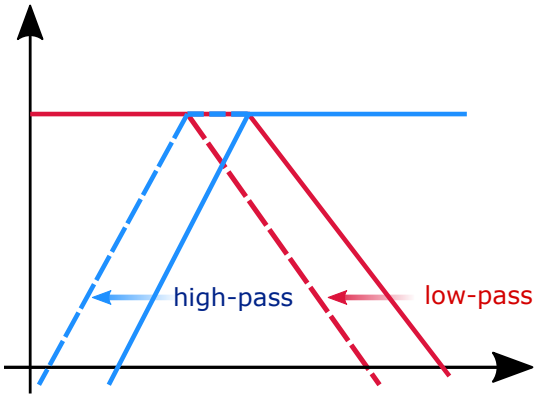


Figure 3.29: Shifting of the low-pass and high-pass frequencies when increasing temperature

3.4.2 Circuit Implementation

In order to make a proper comparison between the continuous time bridge and the discrete time bridge, the same integrator, flip around and VCO were used (3.30). The great advantage of this architecture is the fact that the VCO generates the clocking signal which enables a combination of very useful control signals. Figure 3.31 shows a part of the timing diagram of the SC implementation.

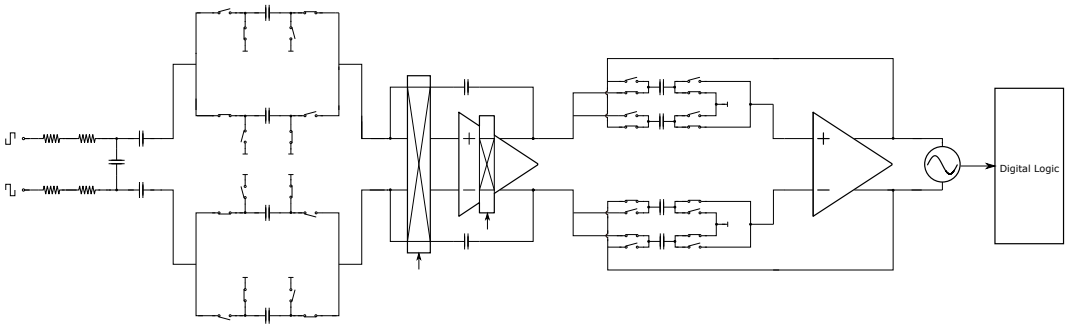


Figure 3.30: FLL SC implementation

For the case of the continuous time read-out, the finite input impedance and any non-ideality of the integrator will translate into the bridge's frequency response. Basically, in order to have great accuracy, the sensor should be independent of the readout, which is not the case since the virtual ground of the integrator will always settle around the desired common mode volt-

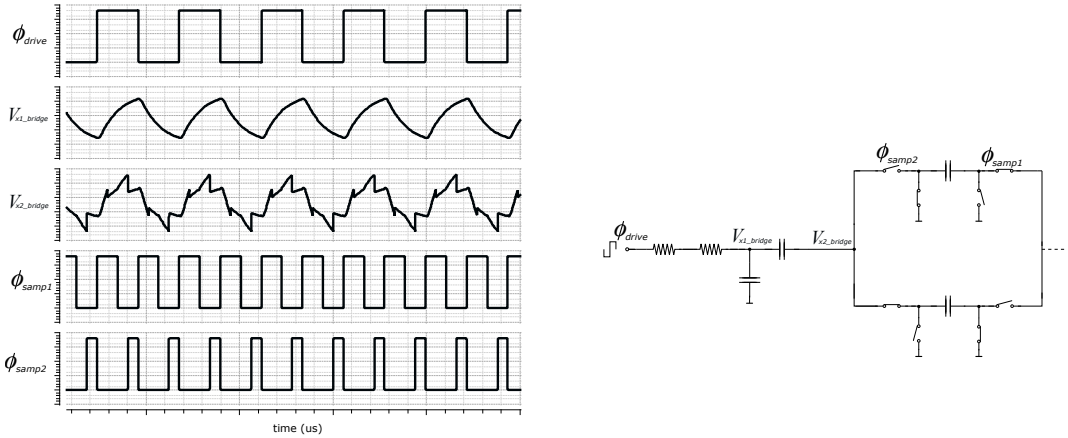


Figure 3.31: FLL SC implementation timing sensor interface

age. For the case of the switched capacitor it is a different story: after transfering the charge from the capacitor to the main feedback capacitor of the integrator, the sampling capacitors are reset with 2 additional switches to the common mode value; therefore, there will be no charge due to the nonidealities of the OTA. (Figure 3.32).

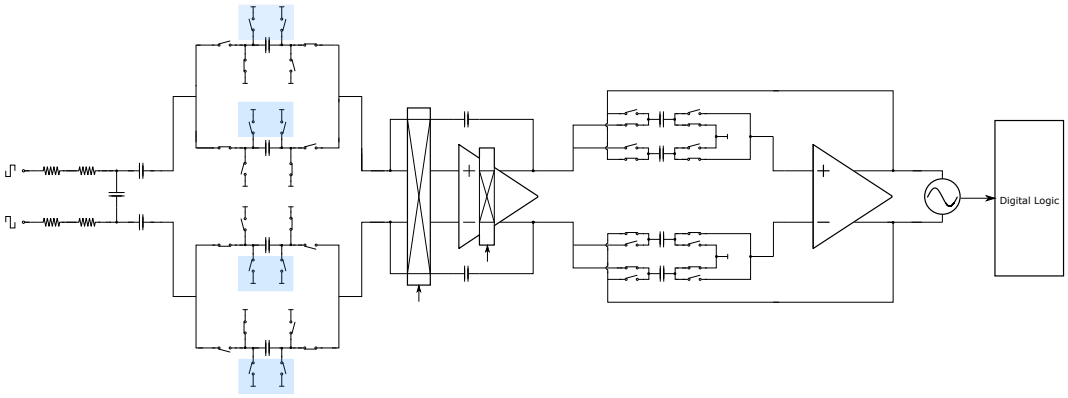


Figure 3.32: FLL SC implementation: adding reset-switches

3.5 Switched- Capacitor Readout Simulation Results

3.5.1 Transient Behavior and Sensitivity

The transient behavior of the FLL over corners and temperatures is shown in Figure 3.33 together with the FLL's sensitivity 3.34.

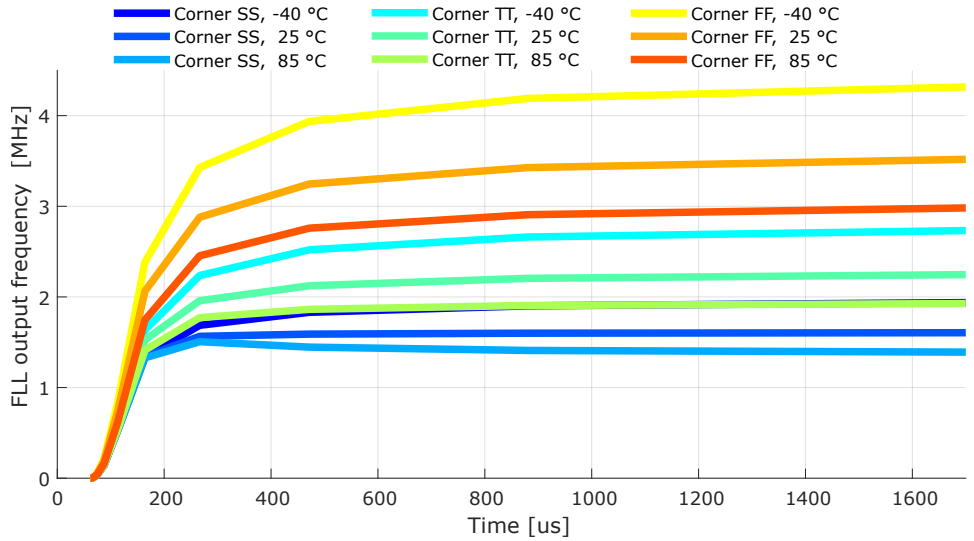


Figure 3.33: FLL output frequency versus time

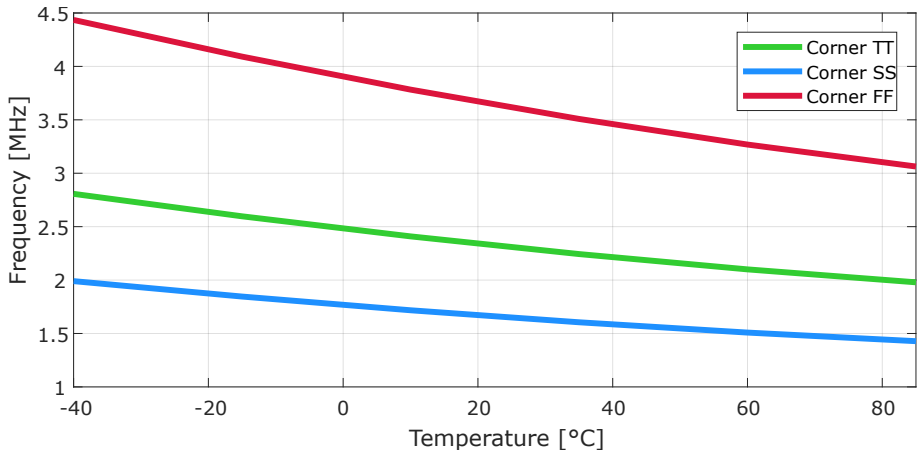


Figure 3.34: FLL output sensitivity

3.5.2 Resolution

Figure 3.35 shows the output spectrum of the FLL with the SC resistor implementation extracted from a transient noise simulation and one noise-free simulation. From the output spectrum, it can be seen that the design is thermal noise limited, achieving only an ENOB=11.91 bits in a 10kHz bandwidth.

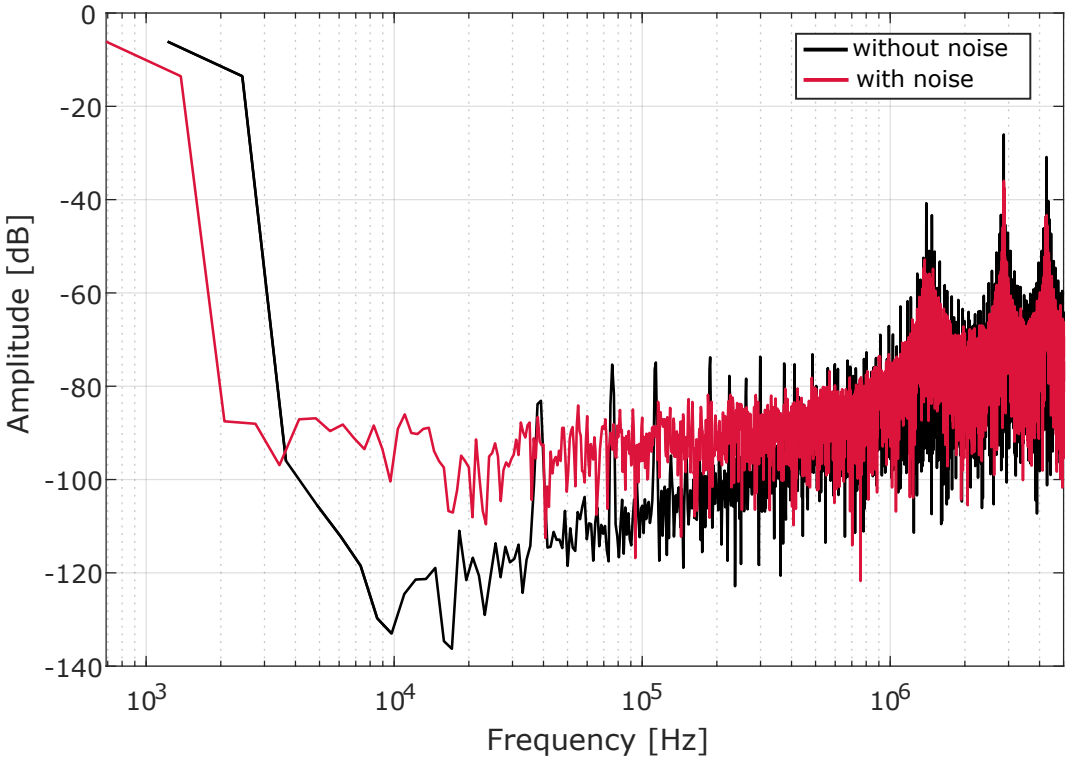


Figure 3.35: Output spectrum with and without noise

3.5.3 Inaccuracy

Following a similar method as described in section 3.3.3, after a 2-point trim and systematic error removal, the obtained inaccuracy is lower than 0.08°C (Figure 3.40), whereas for a 3-point trim and systematic error removal, the inaccuracy becomes lower than 0.05°C (Figure 3.36).

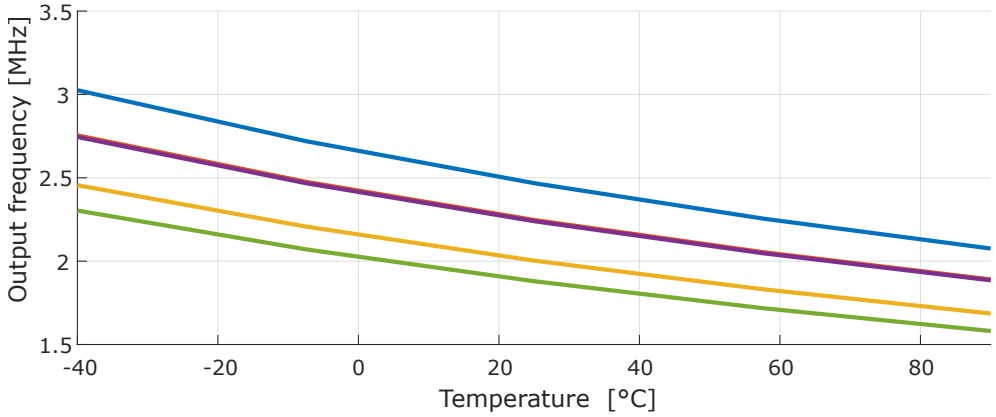
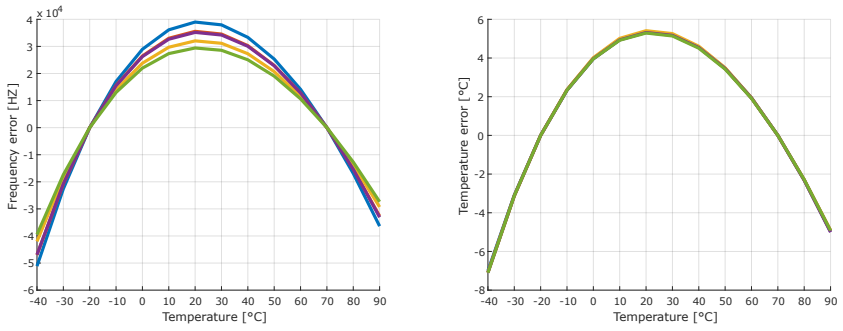


Figure 3.36: FLL output frequency Monte-Carlo Simulation (5 runs)



(a) Frequency error (b) Temperature error

Figure 3.37: Frequency error and temperature error after 2-point trim

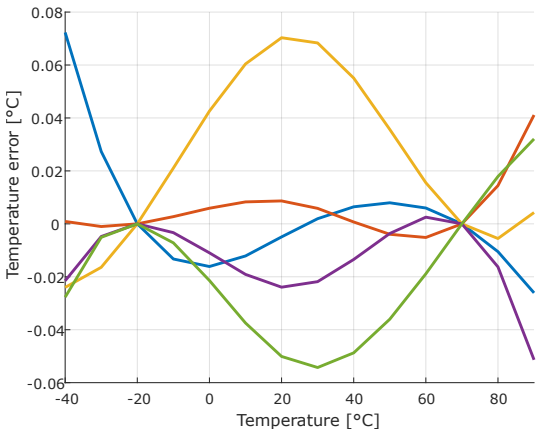
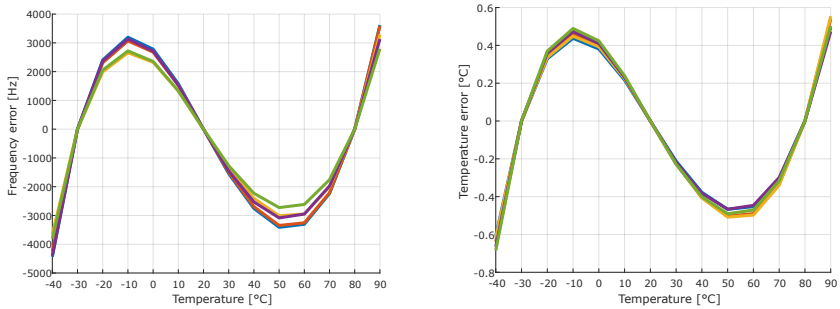


Figure 3.38: FLL output frequency Monte-Carlo Simulation (5 runs)



(a) Frequency error (b) Temperature error

Figure 3.39: Frequency error and temperature error after 3-point trim

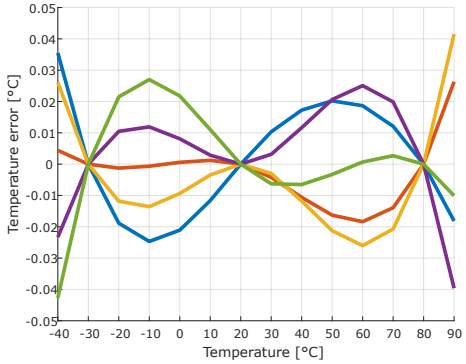


Figure 3.40: FLL output frequency Monte-Carlo Simulation (5 runs)

3.5.4 Power and Area Concluding Remarks

As previously stated, the idea of this implementation was to explore another design direction: increasing the resistor, rather than increasing the integration capacitor size. Some additional control signals are required for the SC resistor switches and the reset switches, however, since the resistor was doubled, less power was consumed to drive the filter, so there is not a large amount of additional power.

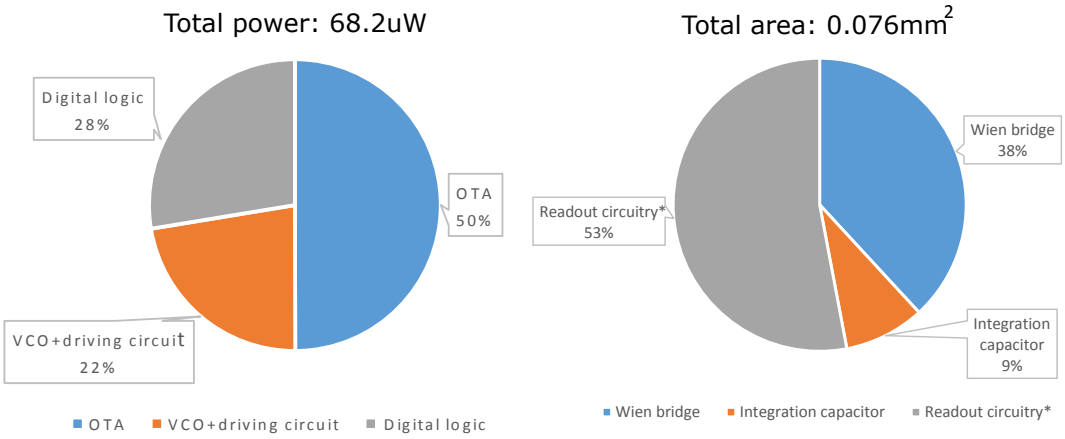


Figure 3.41: Power and area breakdown

Chapter 4 Digitizing the Output of the FLL

The digital temperature compensation of most MEMS-based oscillators requires temperature sensors with a digital output. The system-level analysis of the FLL can then be extended to include the circuitry needed to digitize its output frequency. Discretizing the output signal implies adding quantization noise and care must be taken to ensure that this does not limit sensor resolution. Given that the output signal is generated by a voltage-control oscillator, the discussion about what type of circuit can be used to digitize the output signal will start with a short description of this block.

4.1 VCO and its Domains

In general terms, a VCO translates the variation of an input signal $Vin(t)$ into an output signal $Vout(t)$ whose frequency is determined by the input signal (Figure 4.1).

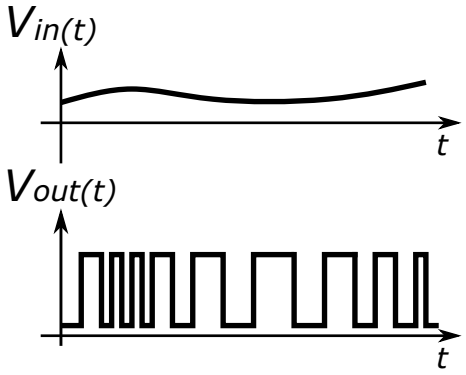


Figure 4.1: Ideal VCO input and output voltage

There is also another important relation between the frequency and the phase of a VCO. Figure 4.2 shows the output transient (voltage) and the phase, $\varphi(t)$, of an ideal free-running VCO. The slope of the phase is proportional to the frequency, i.e., the phase is the integral of the frequency.

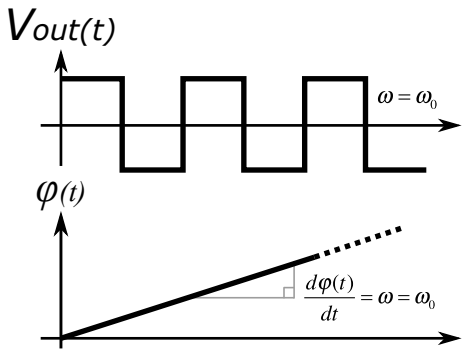


Figure 4.2: Ideal VCO output voltage and phase

Due to these characteristics, there are many ways of extracting the information contained at the VCO's output since both frequency and phase can be read-out. In addition to this, as the buffered output of the VCO toggles between two levels (low and high voltage), it can be used to drive digital blocks efficiently. In the next sections, two readout methods will be discussed: the edge-counting-based readout and the phase-sampling-readout. The analysis starts with a theoretical description of each type of readout circuit, followed by a comparison between them.

4.2 Edge-Counting-Based Readout

A previous FLL-based temperature sensor [3] employs a 20-bit counter to determine the number of output pulses generated in a fixed gating period. The gating pulse was generated by a programmable divider driven by a 131kHz reference oscillator (Figure 4.4). For increased resolution, an edge-combining circuit [37] (Figure 4.4) generates an M times higher output frequency, where M equals the number of inverters in the VCO (M=9 in the previous design). Each NAND gate generates pulses obtained from two consecutive outputs of the VCO. The combination of these pulses results in nine times higher output frequency.

Digitizing the output of the FLL with an edge-counting-based readout is equivalent with filtering the output frequency with a sinc 1 filter [3] of length equal to $T_{conversion}$. The equivalent noise bandwidth is:

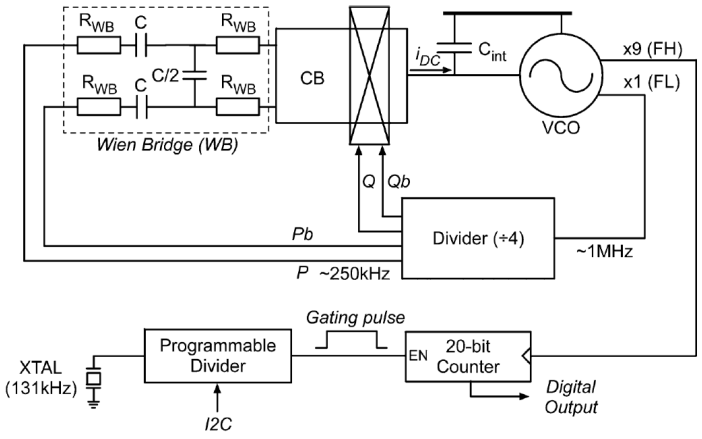


Figure 4.3: Edge-counting-based readout: the edge-combining implementation from previous design [3]

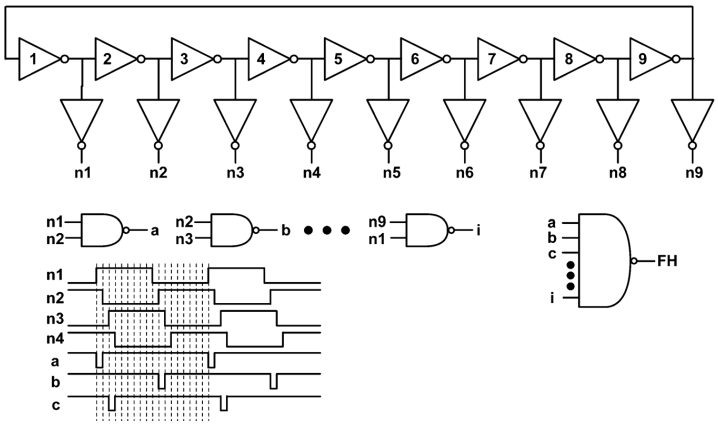


Figure 4.4: Edge-counting-based readout: the edge-combining implementation from previous design [3]

$$ENBW = \frac{1}{2 \cdot T_{conv}} \tag{4.1}$$

Digitizing the output adds quantization noise. The digital representation of the output frequency can be written as:

$$f_{\text{out, dig}} = \frac{M}{T_{\text{conv}}} + \frac{q}{T_{\text{conv}}}, \tag{4.2}$$

where M is the output of the counter and q is the quantization noise which

has a variance $\sigma_q^2 = 2/12$. Following a similar analysis to the one in [3], for a multiplied output with a factor of K, the rms variation of the output frequency is given by:

$$\Delta f_{\text{out},rms} = \sqrt{S_{\text{fout}}(f) \cdot \frac{1}{2 \cdot T_{\text{conv}}} \cdot K^2 + \frac{\sigma_q^2}{(T_{conv})^2}} \tag{4.3}$$

The resolution can be calculated by dividing the total rms variation of the output frequency by the multiplication factor, K, and the frequency-to-temperature sensitivity of the resistor given by 3.1.

Based on this calculation, figure 4.5 illustrates that as the multiplication factor of the output frequency increases, the conversion time for which the design is thermal noise limited decreases. Since the target of this design is to achieve a thermal-noise-limited resolution <1mK in a conversion time of 30ms (Table 1.2), an edge-combining circuit with a multiplication factor of at least 9 should be implemented.

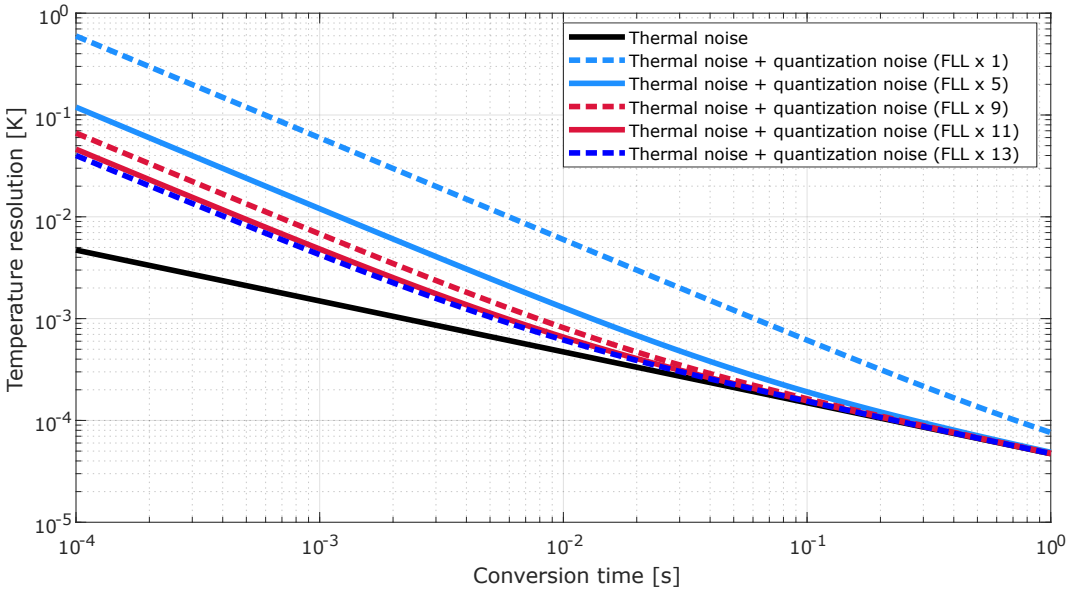


Figure 4.5: Estimated resolution versus conversion time

4.3 Phase-Sampling-Based Readout

The implementation of a phase-sampling digitizer is illustrated in Figure 4.6. The waveforms from Figure 4.6 illustrate the operation of the FDC while looking only at one output of the ring oscillator ($out1$). When $out1$ is changing its value from 1 to 0 (for simplification, one can consider only logic levels 0 and 1 for all the signals), at the next rising edge of the clock signal (CLK), the output of the first flip-flop, Q_1, changes to 0. The second flip-flop's output, Q_2, will take the previous value of signal Q_1, before the rising clock edge. The output of XOR gate, FDC_{out1}, will follow various patterns: if the transitions at the input are faster, the output would produce more 1's, whereas if the transitions are slower, the output will produce more 0's.

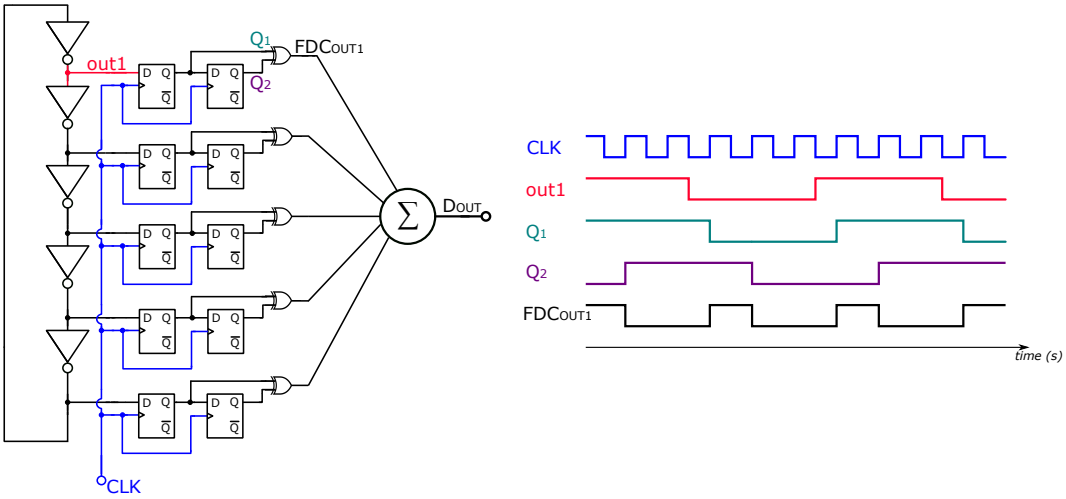


Figure 4.6: Frequency-to-digital converter block and timing diagram

As seen in Figure 4.6 the frequency-to-digital converter uses a 1 bit counter attached to each VCO-inverter output and a higher frequency reference clock to track the phases of the VCO. The clock frequency should be at least two times higher than the maximum VCO frequency over all corners and temperatures, for reasons that will be explained in this section. Since for this design, the VCO's frequency needs to have a maximum value over corners and temperatures of approximately 4MHz to cover the bridge's center frequency range (Chapter Circuit Implementation), a clock frequency of 10MHz needs to be chosen such as to leave some margin. Considering a 5-stage ring

oscillator, the output phases of each stage can be combined to generate $2 \cdot 5$ different states, as shown in Figure 4.7.

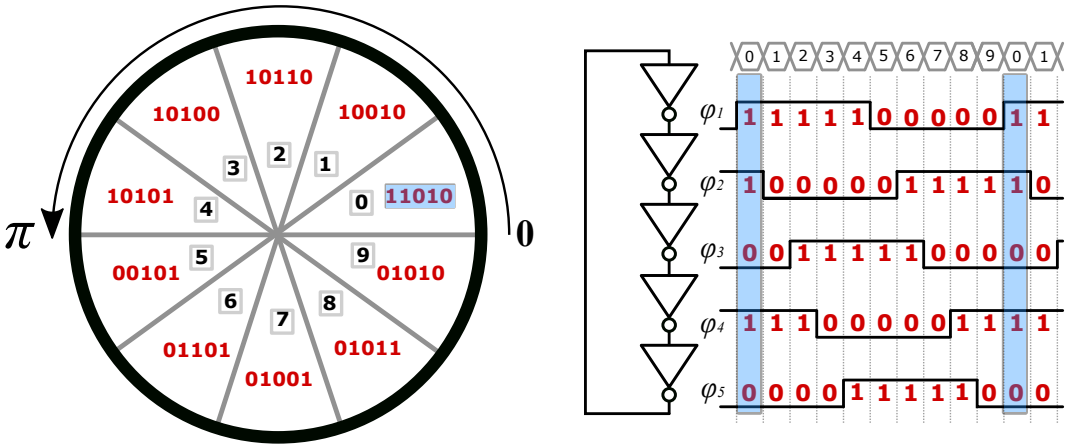


Figure 4.7: Phase sampling and accumulation

Since the output phase accumulates infinitely, it is useful to unwrap the phase around 2π, corresponding to the period of the VCO, as shown in Figure 4.8. The concept of phase quantization will be explained next. Looking at Figure 4.8, the phase LSB step is defined by:

$$LSB_{\varphi} = \frac{\pi}{M}, \tag{4.4}$$

where M is the number of inverters in the ring-oscillator.

Following a similar analysis as the one from [38], and by looking at Figure 4.8, a digital representation of the change in the output phase is given by:

$$D_{OUT}(n) = \frac{(\varphi(n) - \varphi(n-1)) - (\Delta\varphi(n-1) - \Delta\varphi(n))}{LSB_{\varphi}} \tag{4.5}$$

where $\varphi(n-1)$ and $\varphi(n)$ are the phase values corresponding to the sampling moments, whereas $\Delta\varphi(n-1)$ and $\Delta\varphi(n)$ are the quantization errors corresponding to the difference between the phase at the sampling moment and the nearest quantization level corresponding to one of the 2M transitions of the VCO.

Even if an XOR gate misses one transition of the VCO, due to the fact

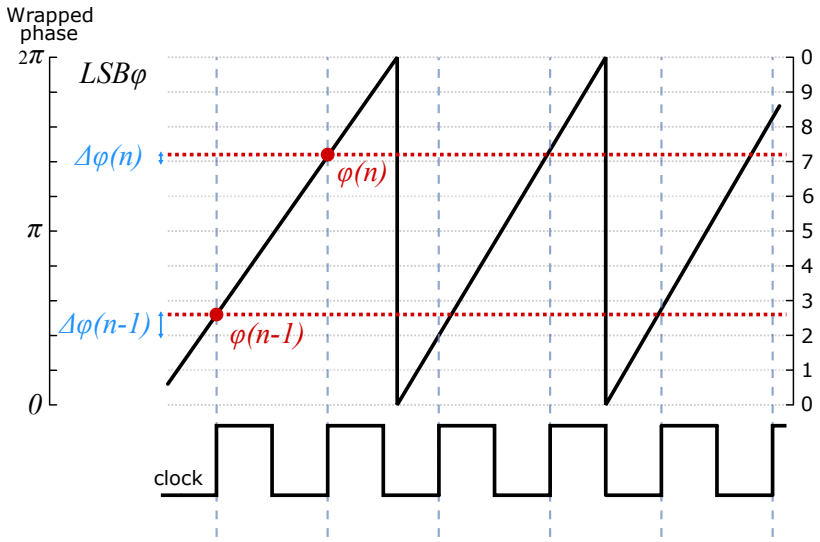


Figure 4.8: Quantization of the VCO's phase

that the clock is 2x higher than the maximum transition rate of any of the VCO outputs, the phase information is not lost and it will add up to the next cycle.

One interesting property of this implementation is apparent when the digital output is represented in the frequency domain. By using the Z-transformation of equation 4.5, one can find the NTF and STF of the digital output:

$$STF = 2M\frac{1}{f_s}K_{VCO} \tag{4.6}$$

$$NTF = \frac{M}{\pi}\left(1 - z^{-1}\right), \tag{4.7}$$

where f_s is the sampling frequency and K_{VCO} is the VCO's gain.

From the previous equations, some observations can be made. The input signal of the FDC is scaled by a known factor, while the quantization error is first-order shaped by the NTF. This result enables the full analysis of the noise transfer function by combining the FLL with the FDC readout. Figure 4.9 illustrates the noise coming from the VCO high-pass filtered by the FLL (as previously shown in Figure 2.8). Following, the noise at the input of the VCO is integrated into phase noise. After adding the quantization error

due to sampling, at the output of the FDC, D_{OUT}, the noise sources are differentiated, resulting in a first-order noise shaping operation.

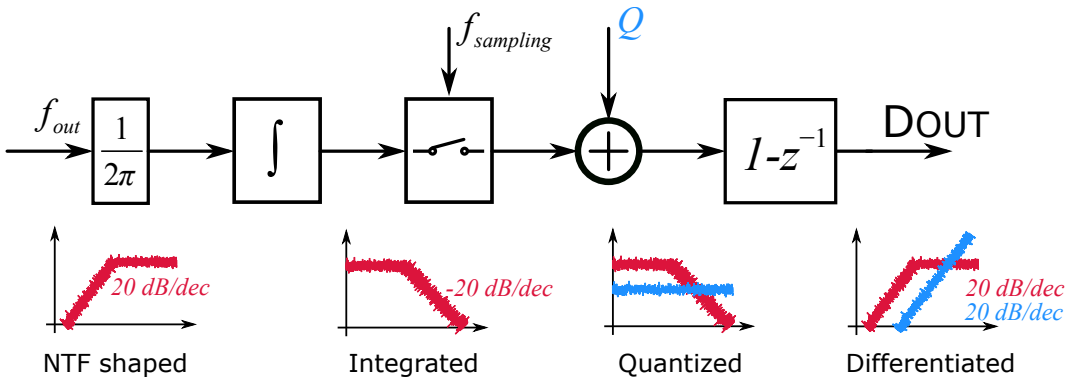


Figure 4.9: FDC block diagram components and their associated noise transfer functions

To derive the SNR, the power of the signal and the power of the noise at the output of the FDC need to be calculated. If the input of the VCO is a sine wave with amplitude A_m and frequency f_m, the signal power is:

$$P_{\text{signal}} = \left(\frac{2 \cdot M \cdot T_{\text{clock}} \cdot K_{VCO} \cdot A_m}{\sqrt{2}} \right)^2, \tag{4.8}$$

where K_{VCO} is the VCO's gain.

It has been shown in [38] that the inband power given a bandwidth f_b is:

$$P_{noise} = 8 \cdot \frac{\pi^2 \cdot (f_b)^3}{36 \cdot (f_{clock})^3} = \frac{\pi^2}{36 \cdot OSR^3}, \tag{4.9}$$

where OSR is the oversampling ratio.

Based on 4.8 and 4.9 the SQNR can be calculated:

$$SQNR = 10 \cdot \lg \left(\frac{9 \cdot f_{\text{clock}} \cdot (2 \cdot M \cdot K_{VCO} \cdot A_m)^2}{4 \cdot \pi^2 \cdot (f_b)^3} \right) \tag{4.10}$$

Based on this result, the SQNR value depends on the number of inverters (M), the sampling frequency (fclock) and the chosen bandwidth. This shows that a more aggressive noise shaping is obtained if the sampling frequency is much higher than the bandwidth (fb).

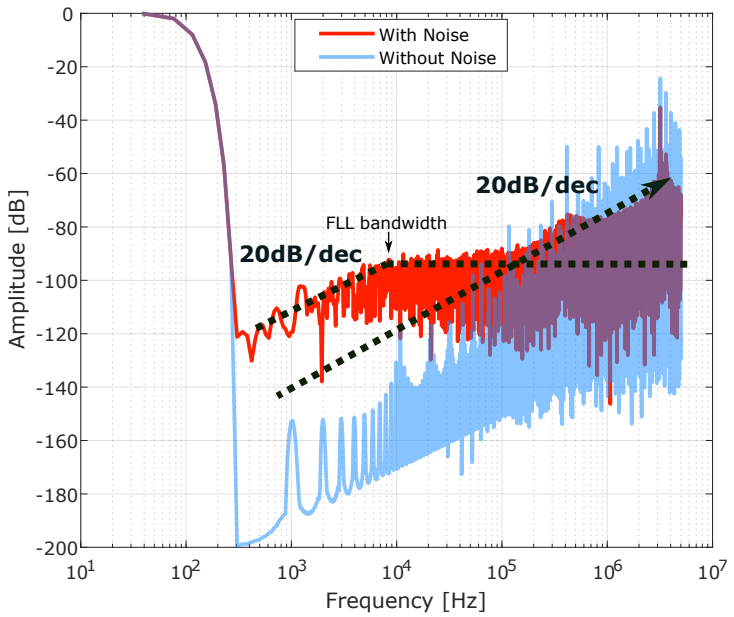


Figure 4.10: Output spectrum extracted from the system model

Figure 4.10 shows the output spectrum of the FLL together with the FDC described above. The blue spectrum represents the output of the system when only quantization noise is taken into account, while the red spectrum includes noise from the VCO. As previously described in section 2.3, the VCO's noise is high-pass filtered by the loop. By looking at both Figure 2.8 and Figure 4.10, one can identify the value of the FLL's closed-loop bandwidth to be $\simeq 8kHz$. The differentiation caused by the FDC results in a first-order noise shaping, in accordance with the analysis shown above.
Simulations are provided in the next section in order to compare the quantization effects of both digitizers and the advantage of using a phase sampling readout instead of a counter based readout.

4.4 Comparison Edge-Counting Readout vs. Phase-Sampling Readout

4.4.1 Resolution vs. Conversion Time

Figure 4.11 illustrates the implementation of the edge-counting-based readout, while Figure 4.12 illustrates the implemention of the phase-sampling-based readout in Simulink.

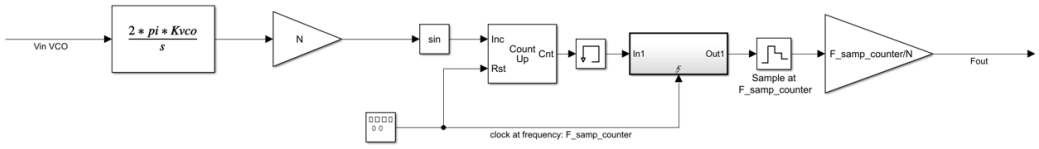


Figure 4.11: Simulink model of digitizing the VCO's output with a counter-based readout

Figure 4.12: Simulink model of digitizing the VCO's output with a phase-sampling-based readout

Figure 4.13 shows the transient response of both types of readout. While the counter seems to accurately reach a steady state (locking frequency of 2.4 MHz), it still requires a certain amount of conversion time until the total in-band quantization noise is less than the sensor's inherent inband thermal noise. The counter can be considered to be a decimation filter (sinc1) which samples the number of VCO transitions between each reset event given by a 25kHz reset signal.

Moreover, the phase sampling readout does not include an inherent decimation effect and therefore it's filtering can be implemented separately based

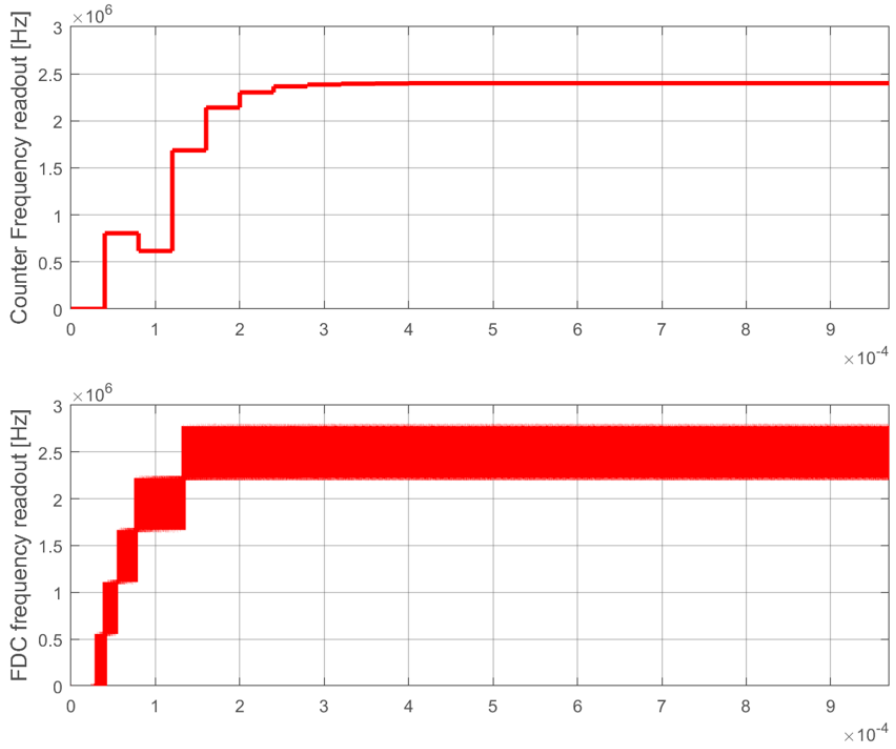


Figure 4.13: Transient response of the FLL with counter-based readout (up) and with phase-sampling readout (down)

on optimizations of power, area and efficiency in downsampling the digital data without inband fold-over. A common filter that is used in both incremental ADCs [39] and temperature sensors [21] is the sinc2 decimation filter with a transfer function given as:

$$H(z) = \frac{1}{D^2} \cdot \left(\frac{1 - z^{-D}}{1 - z^{-1}} \right)^2 \tag{4.11}$$

where D is the decimation ratio. This type of filtering allows a suppression of periodic noise such as the power line noise (50Hz) by configuring it such that its notches are at the multiples of Fs/D[39].

Based on simulations performed in Simulink, the resolution vs. conversion time for both type of readouts are illustrated in Figure 4.14.

It can be seen that the FDC with 5 inverters can achieve the best resolution for given conversion time. Furthermore, the counter based readout requires

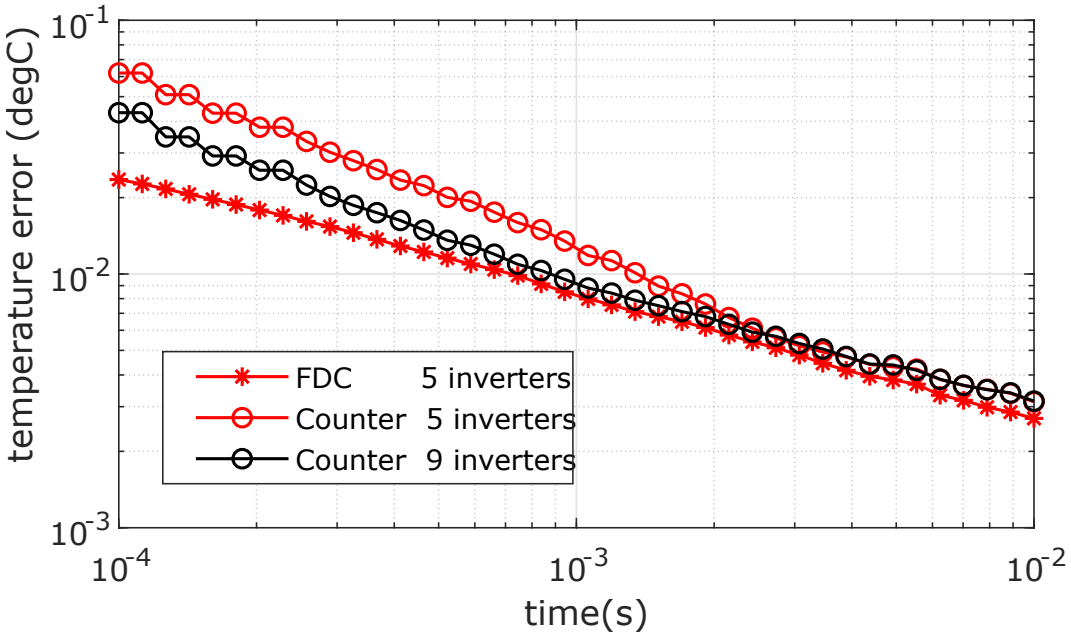


Figure 4.14: Resolution vs. conversion time for edge-counting-based readout and phase-sampling-based readout

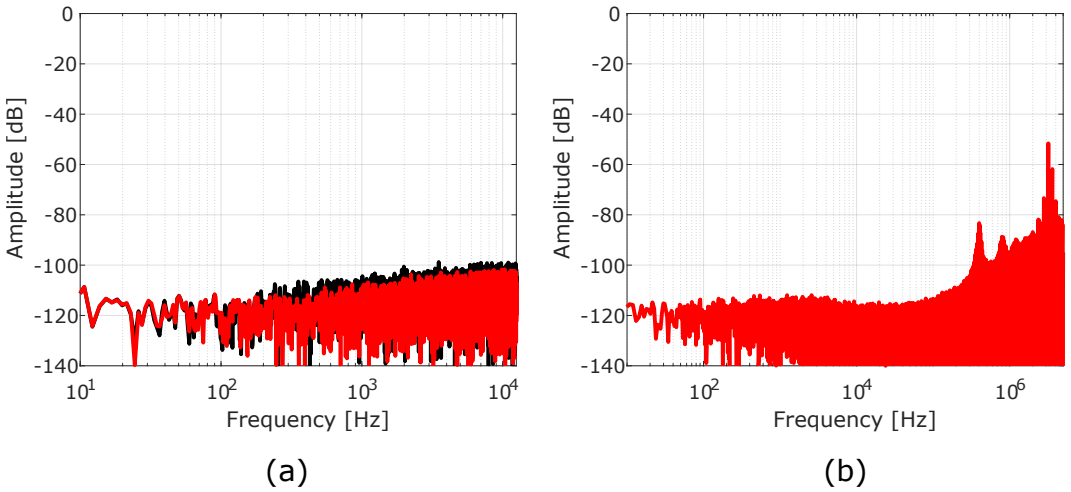


Figure 4.15: Spectrum of: (a) Counter based readout (5 inverters - red and 9 inverters - black) (b) Phase sampling based readout (5 inverters)

even more than 9 inverters in order to lower the in-band quantization noise and to be limited only by the thermal noise of the system. Figure 4.15 shows the Simulink based simulations for the FLL, when both readouts are used.

4.4.2 Circuit Implementation of the Edge-Counting Readout

Since the lowest power consumption design, [3] from Table 1.1 was implementing an edge-counting-based readout (as described in the previous section), further analysis is needed to check if the same type of readout can be implemented in the proposed design. While both designs implement a ring oscillator, there is a fundamental difference in how these two ring oscillators are driven. In the previous design, the ring oscillator's current is controlled by another transistor, making the oscillator a current-controlled oscillator (CCO) (Figure 4.16 and Figure 4.17), where the pMOS transistor is controlled by the voltage Vc. As it can be seen from Figure 4.4, Vc is given by the integration of the current buffer's (CB) output into the integration capacitor.

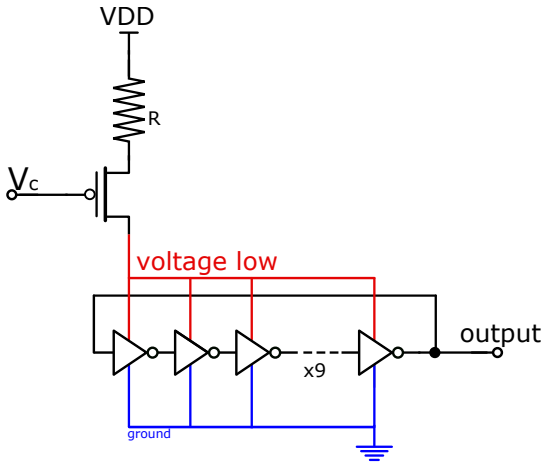


Figure 4.16: Previous design's driving stage for the ring oscillator

However, since in the proposed design the ring oscillator is driven fully differentially, care must be taken so that the buffers following the ZOH filter can provide enough current to the VCO to cover its range over temperatures and corners. Since the proposed design is implemented in the same technology (0.18 µm, TSMC) as the previous one ([3]), table 4.1 can be used as an estimation of the current drawn by the edge-combining circuit together with a 9-stage ring oscillator operating at 1MHz.

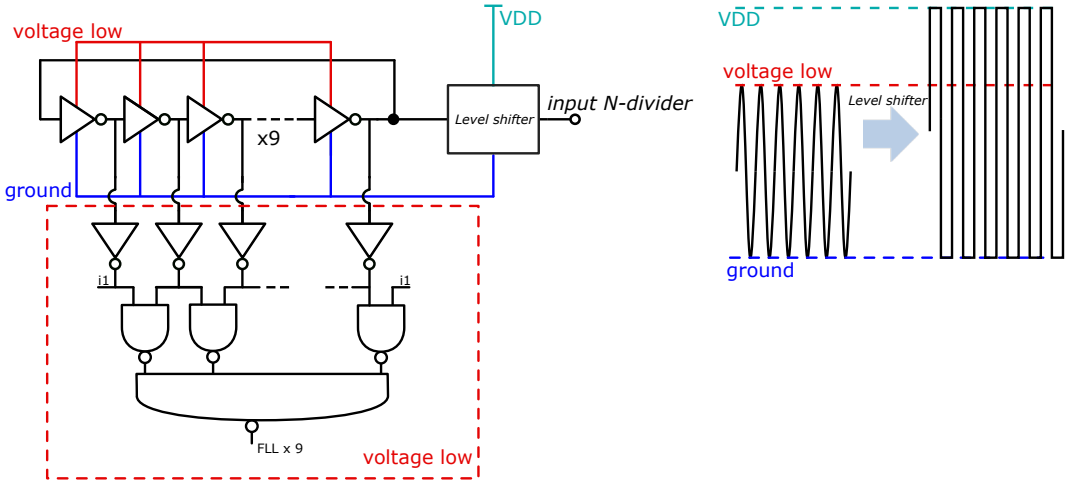


Figure 4.17: Frequency-to-digital converter: design [3]

Technology corner	Typical			Slow			Fast		
Temperature [° C]	-40	25	85	-40	25	85	-40	25	85
VCO current [µA]	2.9	5	7.2	1.4	2.6	3.5	7.2	10.3	13.3

Table 4.1: Maximum power consumption of the ring oscillator and the edge-combining circuit from design [3] over corners and temperatures

Since the theoretical analysis showed that in order to achieve sub mK resolution in 30ms at least a multiplication with 9 is needed 4.5, the buffers should be designed to support a current of minimum 13.3uA for an output frequency of 1MHz. Furthermore, since the proposed design is based on a fully-differential stage which drives the VCO directly (limited driving capability compared to a CCO connected directly to the supply), adding an edge-combiner circuit implies an increase in the necessary load current. Therefore, level shifters at the output of each inverter would be necessary in order to unload the fully differential structure, as shown in Figure 4.18.

Such a level shifter is used for the digital feedback signal (Figure 4.19). It will consume static power in order to bias the comparators which overwrite a latch according to the comparison of the VCO output with the common mode voltage.

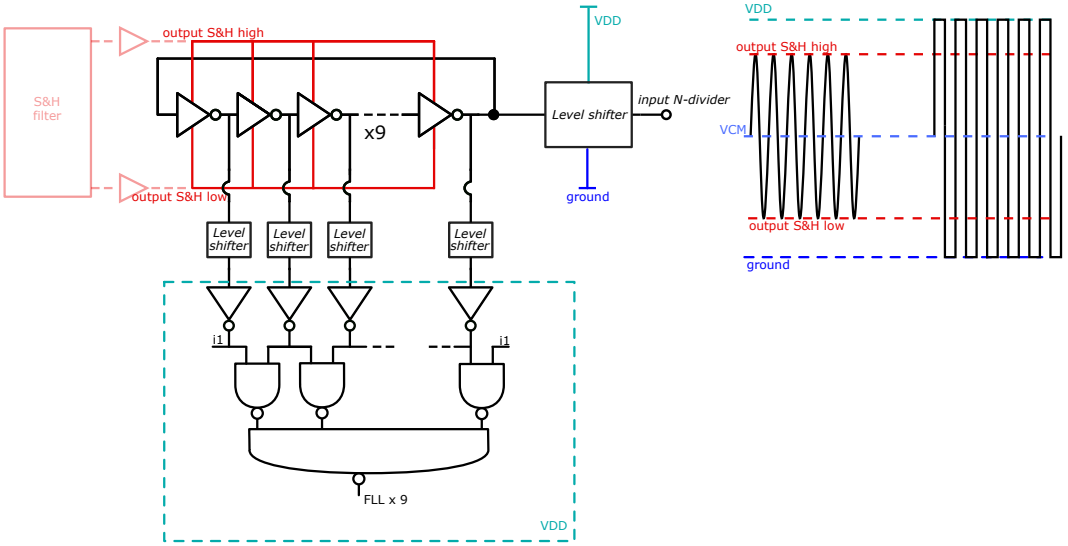


Figure 4.18: Frequency-to-digital converter: proposed design

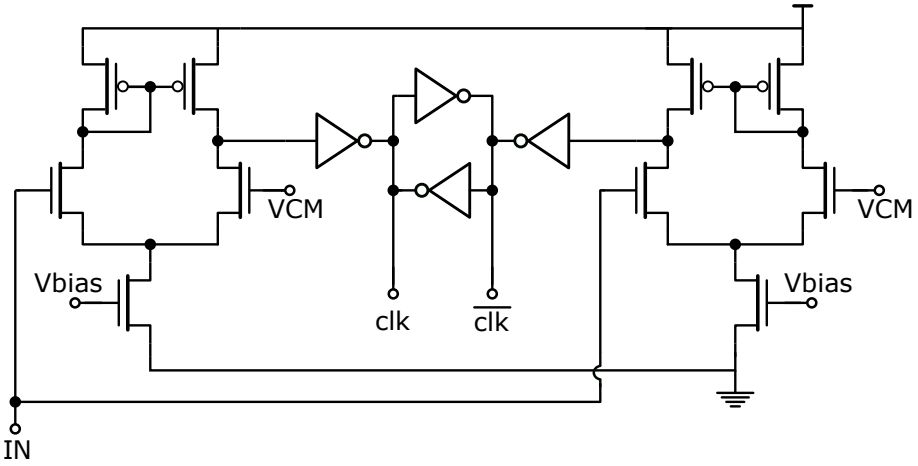
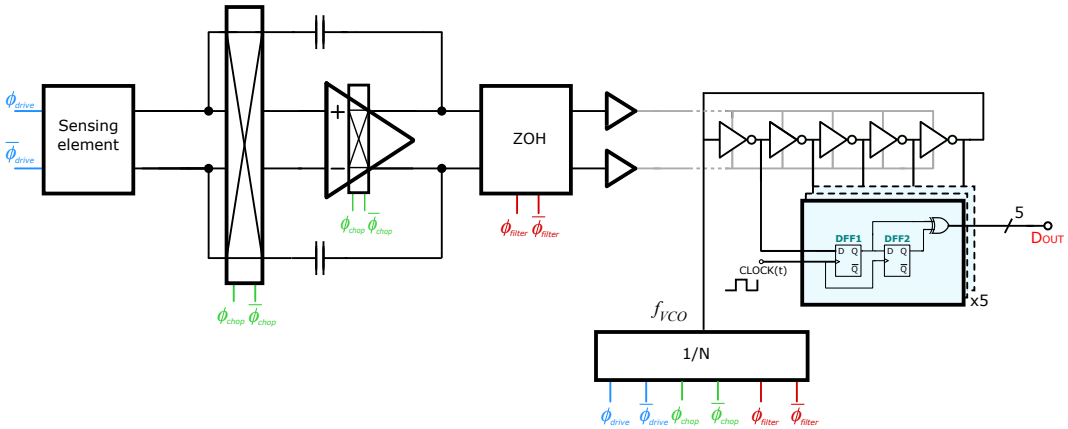


Figure 4.19: Level shifter schematic

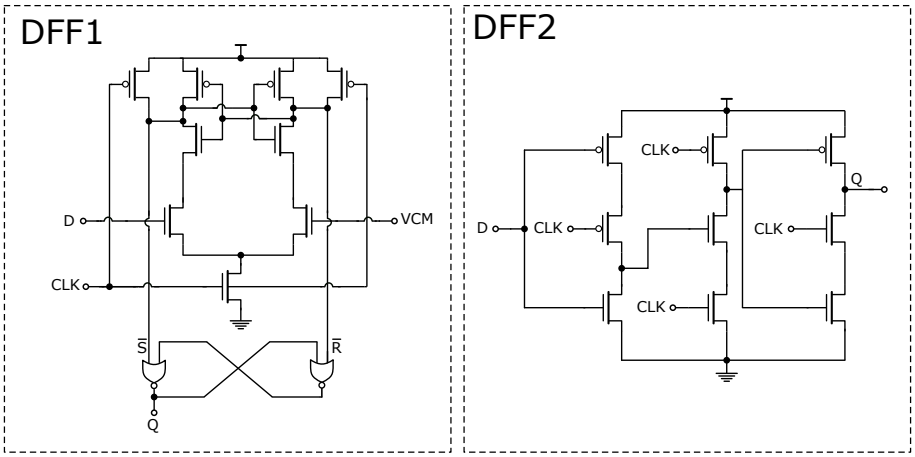
4.4.3 Circuit Implementation of the Phase-Sampling Readout

The final implementation of the design is illustrated in Figure 4.20 (a). The clock has a dual purpose: to reset the latch of the sensing amplifier(Figure 4.20 (b)) and to trigger the storage of the latch inputs. Together with the XOR logic gate, the use of the 1 bit counter will result in a 1st order differentiation of the quantization noise. The inherent advantage of this im-

plementation is the fact that level shifters are not required and therefore no additional static power consumption.



(a) System-level block diagram



(b) D-flip-flops implementation

Figure 4.20: System-level block diagram with the digitization of the output frequency included

Chapter 5 Conclusions

The main focus of this thesis was to investigate how the performance of a resistor-based temperature sensor merged with a frequency-locked-loop readout can be improved.

In the first place, the design procedure was conducted so as to reduce the integration capacitors size to its minimum value in order to achieve a compact sensor. The analysis revealed that there are some options that can be used to minimize the unwanted effects in the loop (chopping, ZOH filter, flip-around amplifier). It resulted in a design with a total power of 62µW, while occupying an estimated area of 0.098mm^2. After a 2-point trim, the expected inaccuracy is around 0.12 °C, with an ENOB of 16.5 bits in a 10kHz bandwidth.

However, the integration capacitor still occupies a similar area with the sensing element, which is not an optimum design. This observation triggered the analysis in another direction of investigation: instead of using a continuous-time readout, a switched-capacitor readout can be used. While this implies some modifications on the sensing element, it is interesting to note that with almost the same amount of power (68 µW), similar performance can be achieved, while occupying a lower area (0.076mm^2). Moreover, the estimated inaccuracy after a 2-point trim is lower than 0.08 °C. However, the ENOB has only a value of 11.91 bits in a 10kHz bandwidth, confirming that kT/C noise can degrade the performance of the sensor. This is an inherent disadvantage of switched capacitor circuits. Despite this reduction in resolution due to the increase in thermal noise, the circuit will provide higher accuracy than its continuous-time counterpart, while occupying a lower area.

The previous chapter presented two possible implementations of the circuit needed to digitize the output of the FLL: the edge-counting-based readout and the phase-sampling-based readout. For this design, the second implementation was preferred motivated by the circuit constraints imposed by the

fully-differential driving of the VCO.

Future work can be done on the discrete-time readout, since the small area and high accuracy that it can provide are strong arguments for motivating its implementation. The power breakdown and area estimation are showing a more balanced design than the continuous-time one. Further improvements on the performance of the system sub-blocks would lead to an even better design. One direction of investigation could be to find a more suitable architecture for the flip-around amplifier as well as for the integrator.

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