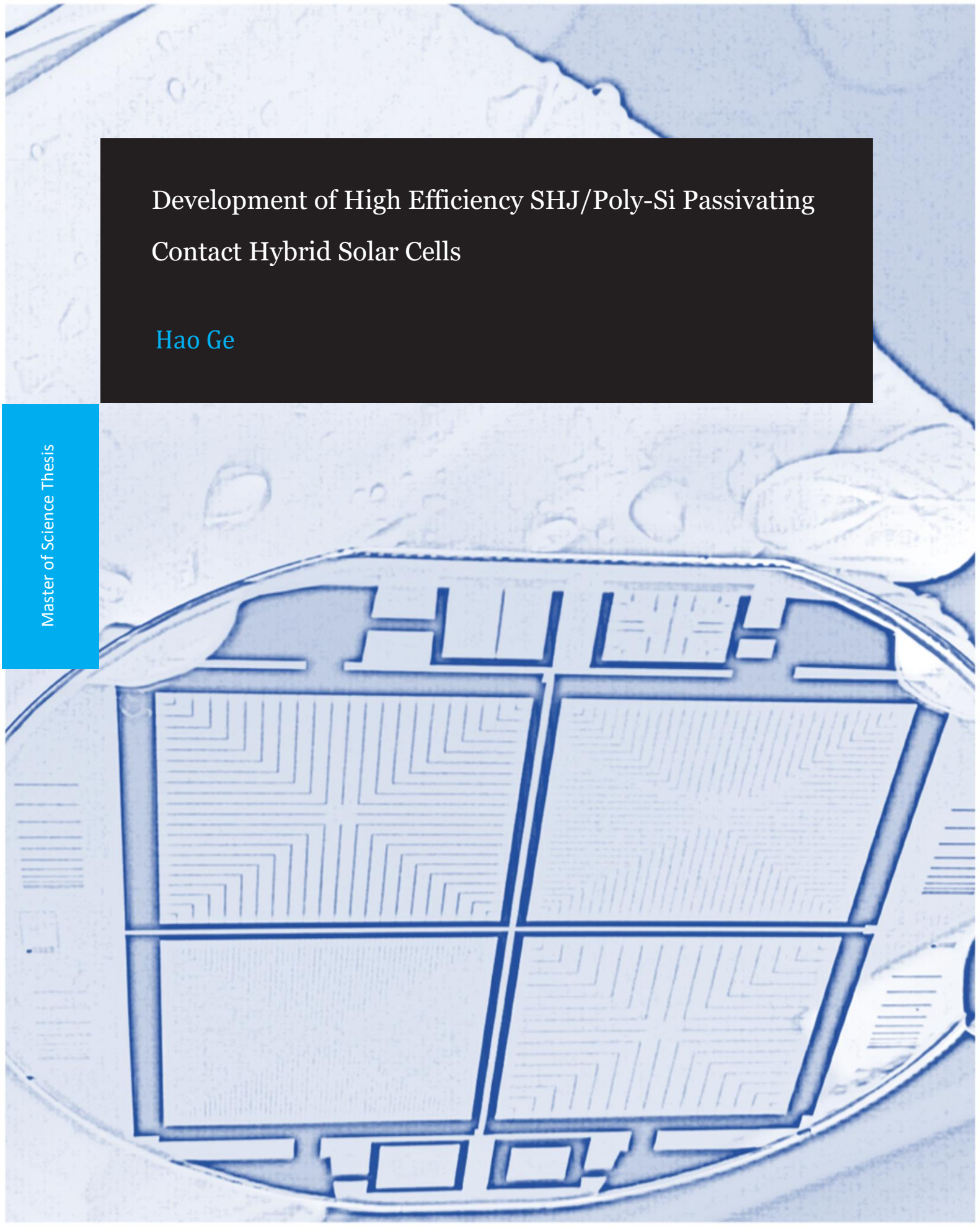
Development of High Efficiency SHJ/Poly-Si Passivating Contact Hybrid Solar Cells

Hao Ge

Master of Science Thesis



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Development of High Efficiency SHJ/Poly-Si Passivating Contact Hybrid Solar Cells

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Abstract

To improve the conversion efficiency of c-Si solar cells, it is crucial to quench the recombination losses at c-Si/metal interface. Such recombination losses are able to be reduced by using carrier-selective passivating contacts by means of hydrogenated amorphous silicon (a-Si:H) and poly-crystalline silicon (poly-Si)/tunneling silicon oxide (SiO_x).

In this thesis, a novel hybrid solar cell concept is presented. The novel structure combines the advantages of silicon heterojunction (SHJ) as front surface field (FSF) and poly-Si passivating contact as rear emitter. This project aims to improve the passivation quality of FSF composed of intrinsic & n-type (i/n) a-Si:H stacks and evaluate transparent conductive oxide (TCO) layer.

Considering FSF optimization, effective cleaning pre-treatment has been developed to provide ultra-clean surface and prevent cross-contamination. Lifetime measurements has shown that three cycles of NAOC improves effective lifetime significantly to 12.6 ms on symmetric structure. Plasma cleaning of chamber and plasma deposition on substrate holder decreases saturation current density (J_0) by 10.9 fA/cm². Comparing to post-deposition annealing in air, H_2 environment annealing shows more appealing passivation quality which improves effective lifetime to 4.7 ms and reduces J_0 to 28.7 fA/cm² on solar cell precursors. V_{OC} demonstrates improvements for thicker i a-Si:H films, but leading to more parasitic absorption losses. This effect results in a trade-off between V_{OC} and J_{SC}. Furthermore, thicker i a-Si:H layer degrades the carrier transport by means of FF.

In terms of TCO optimization, novel hydrogen-doped indium oxide (IO:H)/indium tin oxide (ITO) stacks is presented as an attractive alternative to replace conventional single ITO layer. Hall effect measurements have shown that post-annealing in vacuum is an effective method to decrease carrier density and increase mobility of IO:H/ITO stacks. Accordingly, the opto-electrical properties of IO:H/ITO stacks, single ITO layer and single IO:H layer are compared. 180 °C annealed sample shows optimal performance with high mobility of 117 cm²/(V·s) and low carrier density of 1.07×10^{20} cm^{-3}. Either IO:H/ITO stacks or IO:H single layer shows nearly 4 times higher mobility and half carrier density compared to single ITO film after post-deposition annealing. Spectra measurements reveal that the parasitic absorption of IO:H/ITO stacks is lower than that of ITO film over the complete spectral range. Before post-deposition annealing, it was observed that TCO sputtering decreases passivation quality, but it is less pronounced for IO:H than ITO deposition. However, after post-deposition annealing, passivation degradation is able to be nearly fully recovered for both sputtering: IO:H and ITO.

Based on aforementioned optimization, the highest conversion efficiency of 20.5% was achieved (V_{OC} = 704 mV, J_{SC} = 39.5 mA/cm^2 and FF = 73.8%).

Keywords: Amorphous silicon, passivating contact, transparent conductive oxide, high mobility, hydrogen-doped indium oxide, indium tin oxide

Contents

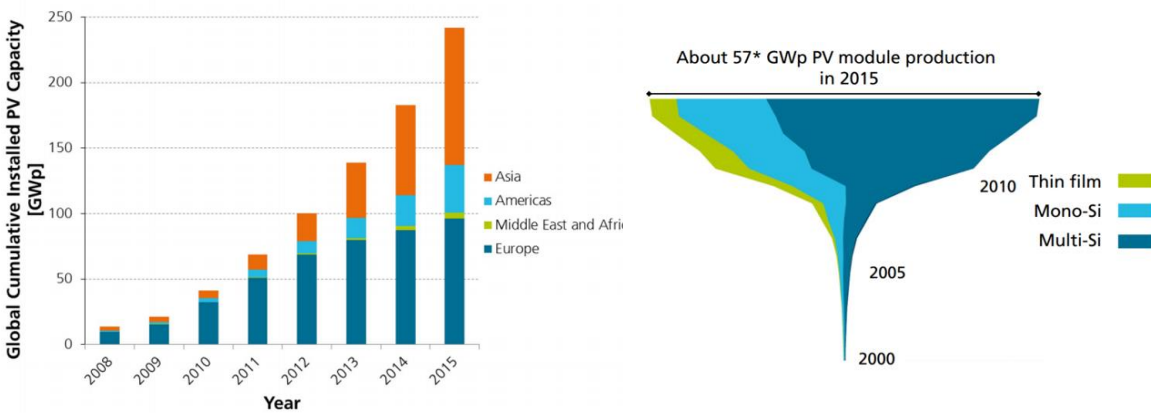
1

Introduction

1.1 Photovoltaic technology: wafer-based crystalline silicon solar cells

With world population and energy demand increase, the traditional energy supplies from fossil fuels as coal, oil and natural gas cannot meet the growing demand alone [1]–[3]. Besides, the incredible amount of fossil fuel consumption causes serious environmental issues, such as air pollution and CO_2 emission. Renewable energies provide more promising and environmentally-friendly alternatives. Among these renewable energies, solar energy becomes more and more appealing due to the infinite resource, convenient application, decentralized system and dramatically decreasing cost.

In the last few years, the cumulative installation of PV modules grew up to 220 GW_p. Moreover, the prominent boom mainly comes from the increase production of crystalline silicon (c-Si) based modules, which consists of monocrystalline silicon (mono-Si) and multicrystalline silicon (multi-Si). Compared to thin film solar cells, the advantages of c-Si cells include high efficiency, high stability, ease of fabrication and longevity.



(a) (b)

Figure 1.1: (a) Global cumulative PV installation until 2015; (b) Annual PV production worldwide (in GWp). 2015 production numbers reported by different analysts vary from between 50 and 65 GWp [4].

1.2 Recombination mechanisms and passivation

1.2.1 Recombination mechanisms

Recombination processes describe the annihilation of generated electrons and holes in the bulk region and surface (or interface), which prohibit the carrier transport and decrease the carrier lifetime, thus are detrimental for achieving high-efficiency solar cells with decreasing the V_{OC} and *FF* of the devices. The recombination mechanisms consist of two main parts [5]:

(i). Bulk recombination
- Radiative recombination
- Auger recombination
- Shockley-Read-Hall (SRH) recombination

(ii). Surface recombination

Radiative and Auger recombination occur in the defect-free semiconductors, while SRH recombination happens in the existence of the impurities or crystal defects in the semiconductors [6].

Radiative recombination

Radiative recombination is a direct recombination process of electrons at valence band with holes at conduction band, which releases the excess energy, corresponding to the bandgap, as photons. It is the

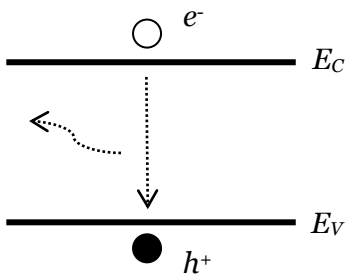


Figure 1.2: Radiative recombination in bulk semiconductors.

opposite direction of the radiative generation, the main generation process, which refers to the generation of electron-hole pairs due to the absorption of photons with sufficient energy to break the bonds. Radiative recombination mostly happens in the direct bandgap materials, so it is not the dominating recombination mechanism for indirect bandgap materials, such as crystalline silicon, as a phonon is required to conserve energy and momentum simultaneously [7].

Auger recombination

Auger recombination describes electron-hole recombination process which transfers the energy and momentum to a third free charge carrier (hole or electron), as illustrated in Figure 1.3. The hole (electron), obtained the energy and momentum, becomes active and jumps to lower (higher) energy

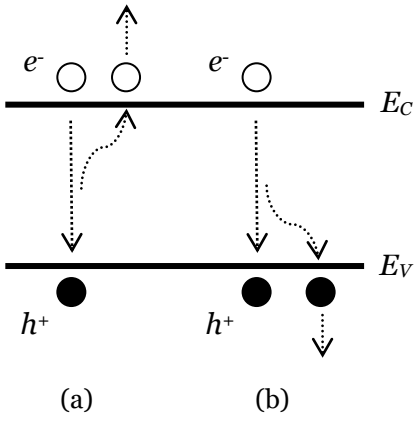


Figure 1.3 : Auger recombination in the bulk: (a) eeh interaction and (b) ehh interaction.

level in valence (conduction) band. Finally, the energy and momentum thermalize when the carrier returns back to the most stable state (valence band top for hole and conduction band bottom for electron). So it is a three-particle-involving process: electron-electron-hole (eeh) or electron-hole-hole (ehh) interaction. In indirect semiconductors, Auger recombination is the main recombination process.

SRH recombination

When there exist impurity atoms (such as iron/copper) or lattice defects in the semiconductors, these defects act as the recombination centers and induce electrons and holes to recombine. The excess energy is then dissipated in the form of heat. It is commonly known as Shockley-Read-Hall (SRH) recombination. These recombination centers introduce allowed energy level within the forbidden gap, named trap states. It is also the dominant recombination process in semiconductors as semiconductor devices for solar cell fabrication can hardly be totally pure without any defects.

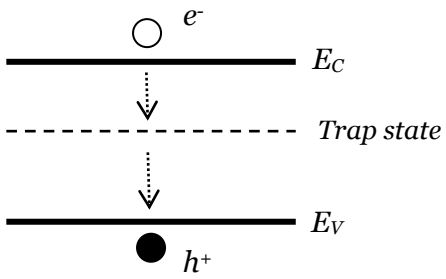
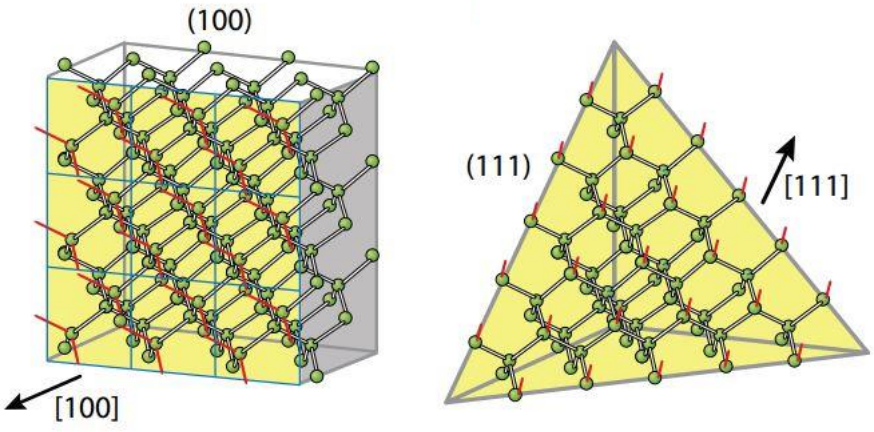


Figure 1.4: SRH recombination induced by trap state in the bulk.

Surface recombination

In the research aim, the high-quality float-zone (FZ) wafers are commonly used, therefore the bulk recombination is negligible in most cases. Only the recombination induced by imperfect surface state is of great importance due to dangling bonds (DB) present on the surface. Crystalline silicon has a diamond cubic crystal structure in which the silicon atom repeats itself in long range order. In the bulk region normally the Si atom is bonded with four neighboring atoms, while in the surface, the termination of the crystal lattice, four valence electrons in Si atom do not fully form bonds. Figure 1.5 shows two common planes in c-Si structure, (100) surface and (111) surface respectively. The three integers in (100) and (111) are so-called Miller indices [8]. As shown in Figure 1.5 (a), the Si atom in (100) plane surface has two dangling bonds while in Figure 1.5 (b), only one unbonded valence electron or dangling bond is presented in (111) plane.



(a) (b)

Figure 1.5: Lattice planes of (a) (100) surface, and (b) (111) surface in crystalline silicon [5]. *The yellow planes are (100) and (111) surfaces respectively and the red lines stand for dangling bonds in the surface.*

The surface recombination rate U_s, via a single-level surface state E_t within the forbidden gap, is then defined by [9], [10]

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{1.1}$$

where n_s (p_s) is the electrons (holes) concentration at the surface; n_i is the intrinsic carrier concentration; n_1 (p_1) is the electrons (holes) density when the Fermi level coincides with the trap state E_t; S_{no} (S_{po}) is the surface recombination velocity of electrons (holes).
Besides the effective surface recombination velocity (SRV) S_{eff} at the edge of surface space charge region (in $x = d$) can be determined by

$$S_{eff} = \frac{U_s}{\Delta n(x=d)} \tag{1.2}$$

where Δn is the excess minority carrier density. The surface recombination velocity gives some indication of the surface characteristics. If there is no recombination happened in surface, the movement of carriers towards to the surface is zero, thus the surface recombination velocity is zero as well.

To conclude, since high-quality FZ wafers are used for research in the lab, the bulk region has a

very low defect density therefore three types of bulk recombination are negligible. On the other hand, the existence of the dangling bonds in the surface makes the surface recombination an importance issue for further improvement of V_{OC} and FF of c-Si solar cells.

1.2.2 Indicators for recombination losses

To evaluate the recombination losses there are two indicators: effective minority carrier lifetime τ_{eff} and saturation current density J_o, which can be measured from WCT-120 Sinton Lifetime Tester.

Effective minority carrier lifetime

The average time which the excess minority carriers survive before recombination, described as effective minority carrier lifetime τ_{eff}, is given by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_s} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_s} \tag{1.3}$$

where τ_{bulk}, τ_{rad}, τ_{Aug}, τ_{SRH} and τ_s are minority carrier lifetime due to bulk, radiative, Auger, SRH and surface recombination respectively.
If the front and rear surface are assumed equal and the photogenerated carriers are uniform, the minority carrier lifetime from surface recombination can be simplified to

$$\frac{1}{\tau_s} = \frac{2S_{eff}}{d} \tag{1.4}$$

where S_{eff} refers to the effective surface recombination velocity and d is the thickness of substrate. The effective surface recombination velocity is an important indicator for recombination loss as well.
High lifetime (normally several milliseconds) is essential for fabricating high-efficiency c-Si solar cell. Typically, τ_{eff} is in the range of hundred microseconds to several milliseconds for c-Si solar cells.

Saturation current density

Saturation current density, J_o , also known as dark current density, is a part of the reverse current in a pn jucntion caused by minority carriers diffusion from the neutral regions to the depletion region [8], which is given by

$$J_0 = qn_i^2\left(\frac{D_n}{L_n N_a} + \frac{D_p}{L_p N_d}\right) \quad (1.5)$$

where q and n_i are the elementary charge and intrinsic carrier concentration; D_n (D_p) is diffusion coefficient of minority carrier electrons (holes); L_n (L_p) is the diffusion length of electrons (holes); N_a and N_d are minority carrier electrons concentration in p-type semiconductor and hole concentration in n-type semiconductor respectively.

Saturation current density should be as low as possible to improve the effective passivation quality. The typical unit is [fA/cm^2] and normally it ranges from 1 fA/cm^2 to several hundred fA/cm^2 for c-Si solar cells.

1.2.3 Surface passivation mechanisms

To suppress the surface recombination, two fundamental methods are applied:

(i). the reduction of surface defect density D_{it} (known as chemical passivation);

(ii). the reduction of electrons or holes concentration at the surface (defined as field-effect passivation).

which are so-called surface passivation techniques.

Chemical passivation

Using other atoms to passivate the dangling bonds of the Si surface, which eliminates (or partially) the surface defect density, is called chemical passivation. Common techniques are forming Si-H bonds or Si-O bonds to saturate the dangling bonds by growing ultra-thin layers, such as hydrogenated amorphous silicon (a-Si:H) or silicon dioxide (SiO_2) layers.

Chemical vapour deposition (CVD) is one of the methods to produce high-quality thin layers. Precursor gasses are brought into the reaction chamber, and then react with the substrate, finally a solid phase material is formed and passivates the dangling bonds. Besides, acid cleaning such as nitric acid (HNO_3) or hydrofluoric acid (HF) also can form Si-O bonds or Si-H bonds to terminate the dangling bonds.

Field-effect passivation

According to the equation 1.1, the highest surface recombination rate happens at the point where the electrons and holes concentration are approximately equal at the surface. Therefore, decreasing one of the two carriers concentration at the surface can effectively limit recombination rate and provides good passivation effect. To separate the electrons and holes, the internal electric field across the surface, known as field-effect passivation, can be achieved by (i) introducing a doping profile within the semiconductor, such as p^+/n^+-doped region

(known as surface field), or (ii) applying highly charged dielectric which has high density charges itself, such as positively-charged SiO_2 and negatively-charged Al_2O_3.

The introduction of a doping profile can be achieved by adding dopant atoms into a narrow surface region or depositing other layers by means of thermal diffusion, ion implantation or chemical vapour deposition methods. Regarding heavily doped region, the high-low junction with the same doping type (p^+-p or n^+-n junction) or p-n junction with the opposite doping can be formed. The field-effect passivation also can be introduced by depositing or growing a thin insulator in order to form a carrier-selective layer. Thus charges storing in the dielectric films induce an internal electric field which hinders the accumulation of one specific carrier at the interface.

1.2.4 Main passivating contacts

The main passivation materials include thermal silicon dioxide (SiO_2) with relatively low positive charges, hydrogenated amorphous silicon nitride (a-SiN_x:H) with high positive charge density, aluminum oxide (Al_2O_3) with negative fixed charges and hydrogenated amorphous silicon (a-Si:H). Besides, the incorporation of different stacks enhance passivation effect further, including SiN_x/SiO_2 [11], [12], SiN_x/Al_2O_3 [13], SiN_x/a-Si:H stacks [10].

Silicon dioxide provides good passivation quality mainly due to the chemical passivation by decreasing the defect density at the interface [10]. Although there are positive fixed charges within the SiO_2 dielectric in the range of 10^{10} – several 10^{11} cm^{-2} [15], [16], it is not enough to trigger the effective field-effect passivation. Therefore, chemical passivation plays a primary role on the c-Si/SiO_2 interface. Furthermore, SiO_2 can provide an excellent antireflection effect thanks to suitable refractive index of around 1.5. Thermal oxidation is a common technique to form high quality and dense SiO_2, which can be achieved by exposing the Si wafer to an oxidizing environment at high temperature. Dry thermal or wet thermal approaches then can be divided according to O_2 or H_2O-vapor environment in thermal annealing furnaces. The record high lifetimes of 29 ms and 32 ms were measured for n-type (resistivity 90 Ω·cm) and p-type (150 Ω·cm) float zone wafers passivated by alnealed (evaporate Al onto the oxide, then anneal at 400 °C in forming gas environment) silicon oxide, with extremely low S_{eff} less than 1 cm s^{-1} [17].

Silicon nitride is a widely used material in industry which also has excellent surface passivation and antireflection effect. Good chemical passivation can be achieved since a large amount of hydrogen is generated during the formation of SiN_x film. Hydrogenation process can terminate dangling bonds at the interface. Besides, SiN_x can induce effective field-effect passivation in N-rich structure on account of high positive fixed charge density of the order of 10^{11} - 10^{12} cm^{-2} [18]. Antireflection properties of SiN_x layer can reduce light reflection significantly due to the optimal value of refractive index around 2.0. Silicon nitride can be produced by direct or remote PECVD with the precursor gasses of SiH_4 and NH_3 [19], [20], which can control the goal

thickness precisely. The structure of a-SiN_x:H consists of two main types: Si-rich film, which exhibits similar amorphous-silicon properties; N-rich film with high positive fixed charge density [21]. The record low S_{eff} of 4 and 20 cm/s on 1.5 and 0.7 Ω·cm low-resistivity polished p-type FZ wafers has been achieved by remote PECVD silicon nitride [19].

Compared with aforementioned positive charge films, aluminum oxide has been proven to be an effective passivation contact with negative fixed charge in the range of 10^{12} – 10^{13} cm^{-2} [22], [23], which is quite high to provide excellent field-effect passivation on c-Si wafers. Best passivation quality of Al_2O_3 layer can be mainly obtained by thermal or plasma-assisted atomic layer deposition (ALD) with a limiting growth rate of 2 nm/min [22]. Surface recombination velocity (SRV) can be less than 10 cm/s on low-resistivity n- and p-type FZ wafers passivated by high-rate spatial ALD Al_2O_3 film [22].

Another emerging outstanding passivation material is hydrogenated amorphous silicon, which provides excellent chemical passivation by intrinsic layer and field-effect passivation by doped films. Phosphine (PH_3) or diborane (B_2H_6), as doping precursor gasses, can be added to form n-type or p-type a-Si:H layers combined with gas silane (SiH_4), sometimes hydrogen (H_2) as well. PECVD is a typical deposition technique to form homogeneous and high-quality a-Si:H films. Good result was obtained on n-type FZ <100> wafer covered by 50 nm-thick rf PECVD intrinsic a-Si:H layers on both sides [24]. The lifetime is as high as 10.3 ms after prolonged annealing (for 100 h) at 200 °C in N_2 ambient with outstanding SRV of 1.32 cm/s assuming infinite bulk c-Si lifetime [24].

Since passivating contacts are of significantly importance of achieving high-efficiency solar cells, in this thesis, two outstanding structures containing SiO_x and a-Si:H contacts are integrated to provide excellent passivation for back emitter and front surface field.

1.3 Motivation for SHJ/poly-Si passivating contact hybrid solar cells

1.3.1 Silicon heterojunction (SHJ) solar cells

Silicon heterojunction solar cells (SHJ) have attracted much attention in research since Sanyo first fabricated HIT® (Heterojunction with Intrinsic Thin layer) solar cell with conversion efficiency of 20.0% on 1 cm^2 CZ n-type c-Si wafer in 1994 [25]. It proved that this sandwiched-device, c-Si wafer between the front and rear doped a-Si:H layers, can be a promising structure with inserting intrinsic a-Si:H as passivation layers. Later on, many research groups and institutions devoted to pushing the record higher by improving surface passivation with more effective cleaning process and low-damage plasma process [26], decreasing parasitic absorption in a-Si:H and TCO layers [27], [28], and lowering the resistivity of TCO layer and electrode materials [29], [30]. The state-of-the-art research record on standard

HIT solar cells was 24.7% on n-type CZ wafer of 98 μm thickness and 101.8 cm² practical size, achieved by Panasonic Corporation in 2013 [31]. To reduce optical loss from front grid electrode further, interdigitated back contact (HIT-IBC) structure hit the record of 25.6% with extremely high J_{SC} of 41.8 mA/cm² in 2014 [32], and even over 26% in 2017 by Kaneka corporation [33]. The detailed parameters are shown in Table 1.1.

Table 1.1: Records of high-efficiency HIT® solar cells [27], [31]

	HIT solar cell	HIT-IBC solar cell
Area (cm²)	101.8	143.7
Thickness (μm)	98	150
V_{OC} (mV)	750	740
J_{SC} (mA/cm²)	39.5	41.8
FF (%)	83.2	82.7
η (%)	24.7	25.6
Year	2013	2014

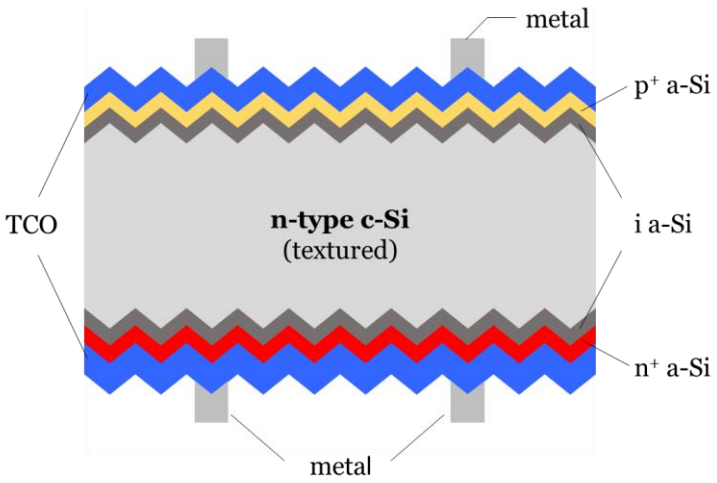


Figure 1.6: A schematic sturcture of n-type SHJ solar cell.

As illustrated in Figure 1.6, normally n-type c-Si wafers are used as the substrates. As-cut wafer is first textured in aqueous alkaline solution and wet-chemically cleaned afterwards combining

with HF dip to remove the local oxide at the wafer surface. A few-nanometer intrinsic a-Si:H layer is then deposited at the front surface with subsequent p-type a-Si layer to form the front emitter by PECVD method. Regarding BSF on the rear side, symmetric structure is fabricated by depositing intrinsic and n-type a-Si films. In this sandwiched-structure, the intrinsic a-Si:H layers provide an excellent chemical passivation of c-Si surface, which can boost the V_{OC} up to 700 mV compared to the structure without intrinsic layers [25]. The doped a-Si:H layers can induce field-effect passivation to repel the minority carrier from accumulating around the surface, which can lower the carrier recombination possibility further. Since the lateral conductivity of the doped layers are rather poor, TCO layers are sputtered at both sides to help the lateral transport of carriers to external electrodes [21]. Besides, front TCO acts as antireflective coating to reduce the front reflectance loss. Back TCO behaves as an effective back reflector to ensure that most not absorbed light (in the NIR region) is reflected into the absorber again. Indium tin oxide (ITO) is a commonly used TCO material. The cell is finalized by simple screen printing technology of grid electrodes at both sides. Highly conductive silver paste was printed and sintered under the temperature of 200 °C.

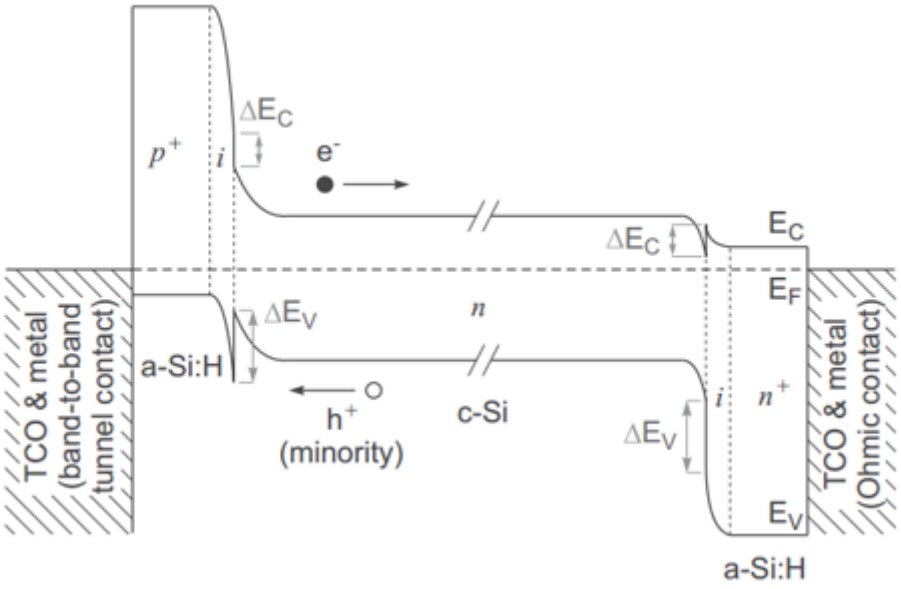


Figure 1.7: Schematic band diagram of SHJ solar cell [34].

The carrier transport mechanism in n-type SHJ solar cell can be explained with the help of band diagram in Figure 1.7. Since c-Si has an indirect bandgap of 1.12 eV and a-Si:H has a direct bandgap of around 1.7 eV, which can be fine-tuned by hydrogen contents, a heterojunction can be formed when they connect. Band offsets of ΔE_C and ΔE_V are introduced in the conduction band and valence band respectively, which are independent of c-Si substrate and a-Si film

doping, with the values of approximately 0.15 eV and 0.45 eV [34], [35]. At the front junction (p-type emitter), holes transport to the interface between p-type a-Si and c-Si substrate, and could be trapped due to the valence band offset ΔE_V. However, with the aid of tunneling and hopping, holes can overcome the energy barrier and transport to the p-type a-Si:H layer and finally be collected at the front electrodes. While for electrons, they are rejected and can hardly pass through the interface because of the large energy barrier induced by p-type a-Si layer. This effect is also called field-effect passivation. The same mechanism happens for electrons in n-type rear emitter. Only electrons can pass through the rear junction and be collected at rear metal.
The advantages of SHJ solar cells can be attributed to four parts: (1) high efficiency over 24% owing to the extremely high V_{OC} exceeding 740 mV after few nanometers intrinsic amorphous silicon layers passivation; (2) excellent temperature coefficient ensures more power output at higher temperature compared to traditional solar cells; (3) simple and low-temperature process cut the production cost further; (4) symmetric structure is less stressed that can pursue thinner wafer thickness, and can be fabricated as bifacial module.

1.3.2 Poly-Si passivating contact solar cells

Another effective carrier-selective passivating contacts structure consists of an ultra-thin silicon oxide layer and a heavily-doped silicon layer having a phase of polycrystalline, amorphous or mixture. The pioneer structure of semi-insulating polycrystalline silicon (SIPOS) developed in 1985 boosts the open circuit voltage up to 720 mV [36]. Afterwards Fraunhofer ISE achieved 19.4% conversion efficiency based on the application of front/rear poly-Si/SiO_x passivating contacts on p-type FZ wafers, which improves the V_{OC} values exceeding 700 mV [37]. The highest conversion efficiency was 25.1% achieved by implementing a tunnel oxide combined with doped silicon film approach [38], called TOPCon (Tunneling Oxide Passivating Contacts), also developed by Fraunhofer ISE, which proves this structure very promising.
Two main poly-Si/SiO_x passivating contacts solar cell structures are shown and compared as followed in Figure 1.8 (a) and (b) respectively. They both include the stack of ultra-thin tunneling oxide layers and doped silicon layers in the form of polycrystalline [37], [39] or mixture of polycrystalline and amorphous [38] by CVD techniques. Wet-chemical cleaning, thermal oxidation and UV/O_3 methods are effective techniques to form an ultra-thin oxide layer around 1.4 - 1.5 nm. Doped amorphous silicon layer can be formed by either depositing intrinsic amorphous silicon layer first by LPCVD combined with ex-situ doping process of ion implantation then or direct in-situ doped amorphous silicon layer by PECVD. Afterwards, a high-temperature annealing is carried out to transform the amorphous silicon to crystalline structure and activate and drive in the dopants to form effective energy barriers for certain carrier at the interface. The biggest difference of structure between top/rear contacted solar cell

and TOPCon solar cell lies in that symmetric layers of poly-Si/SiO_x are applied to top structure of the first solar cell to provide excellent passivation quality, while the latter employs the Al_2O_3-passivated boron-diffused p-type emitter to decrease the parasitic absorption of front layers happened to the former, which benefits the J_{SC} dramatically. The respective electrical parameters are shown in Table 1.2.

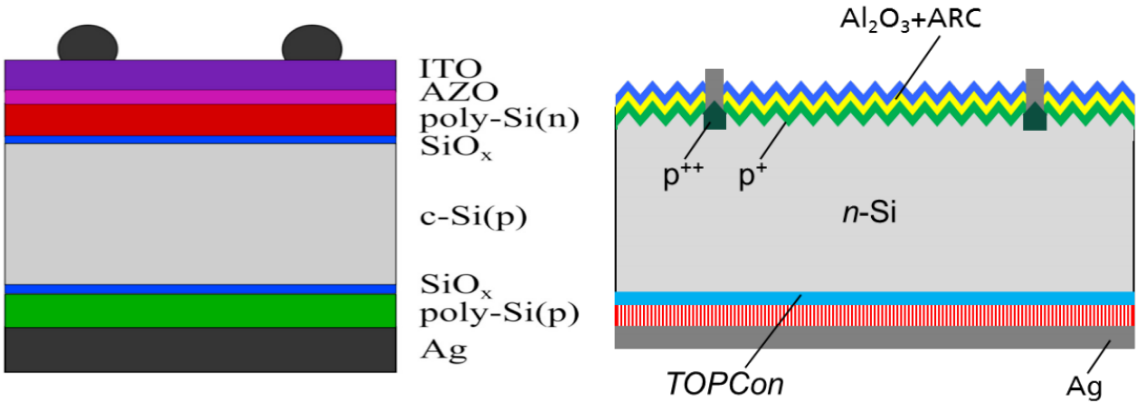


Figure 1.8: Schematic sketches of (a) top/rear poly-Si/SiO_x contacts solar cell; (b) TOPCon solar cell.

Table 1.2: Electrical parameters of poly-Si passivating contacts solar cells [37], [38]

	Top/rear contacted solar cell	TOPCon solar cell
Area (cm^2)	4	4
V_{OC} (mV)	700	718
J_{SC} (mA/cm^2)	33.4	42.1
FF (%)	83	83.2
η (%)	19.4	25.1

An ultra-thin oxide layer plays an important role in surface passivation. It provides outstanding chemical passivation by saturating the dangling bonds in the c-Si surface. Besides, it performs good carrier selectivity with 4.5 eV energy barrier for holes and 3.1 eV for electrons to tunnel [40]. The tunneling is considered as the main working principle for electrons/holes passing through the thin oxide layer, especially when the thickness is less than 2 nm [36], [41]. Recent studies introduced also pinhole-based mechanism for carrier transport when SiO_2 thickness is greater than 2 nm and oxide temperature formation is higher than 1000 °C [41]. Furthermore, heavily-doped poly-Si layer induces an accumulation layer at the interface due to the different

quasi-Fermi level between c-Si absorber and doped poly-Si layer itself, which creates band bending to prevent certain kind of carriers from passing through. As illustrated in Figure 1.9, a phosphorus-doped poly-Si layer forms electron selective barrier and only allows the electrons to pass through tunnel oxide and itself while the holes are rejected. This is also called field-effect passivation.

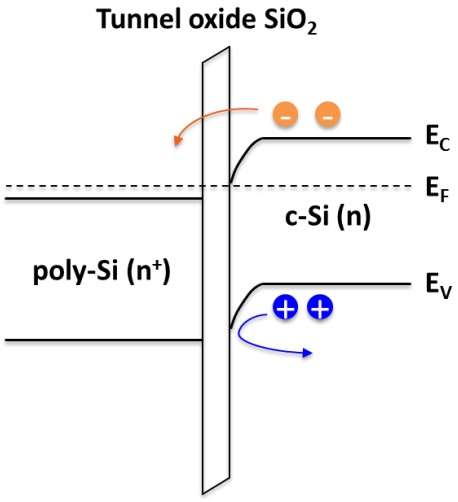


Figure 1.9: Schematic band diagram of n^+ poly-Si/SiO_x passivating contact.

1.3.3 Motivation for developing hybrid solar cells

To achieve high-efficiency silicon heterojunction solar cells, passivation quality of intrinsic/p-type a-Si:H layer stacks are of great importance as n-type counterparts. Nevertheless, it is much more difficult to obtain excellent passivation quality of boron-doped a-Si:H/c-Si structure in the lab, even with an extra intrinsic a-Si:H layer to form chemical passivation [42]–[44]. In terms of intrinsic/phosphorus-doped a-Si:H layer stacks, high minority carrier lifetime as 13.3 ms was reported on symmetric a-Si:H (n^+)/a-Si:H (i)/c-Si (n)/ a-Si:H (i)/ a-Si:H (n^+) planar sample with 20 nm and 5 nm n^+/i a-Si:H respectively after 255 °C post-deposition annealing [43]. In our lab, excellent passivation quality was obtained on same symmetric structure with even thin a-Si:H layer stacks of 4.5 nm i a-Si:H and 6 nm n^+ layer on textured n-type FZ wafers. The minority carrier lifetime of 12.6 ms after 190 °C post-deposition annealing and 4.8 ms as-deposited were measured at an injection level of 1.0×10^{15} cm^{-3}. Regarding symmetric structure of i/p-type a-Si:H stacks, passivation quality measured is not comparable and hard to control. Around 1 ms lifetime was reported in research groups after careful optimization [42], [43]. And in our lab, the average τ_{eff} is around 600 µs with high J_o of 54 fA/cm^2 for i/p^+ a-Si:H stacks, which deteriorates the performance of silicon heterojunction

dramatically and leads to around 17% conversion efficiency. Several explanations may be attributed to this i/p layers degradation: boron contamination at the interface between the p and i layers induces serious carrier recombination [44]; H_2 effusion from thin intrinsic a-Si:H film after depositing boron-doped a-Si:H film. This phenomenon is even worse after post-deposition annealing [42], [43]; phosphorus contamination to i/p bilayers from depositing n-type film due to fabrication order.

On the other hand, poly-Si/SiO_x passivating contacts show promising potential in achieving high-efficiency solar cells. The phosphorus-doped n-type poly-Si with tunneling oxide layers typically present a low recombination current of about 4 - 10 fA/cm², while as for boron-doped p-type poly-Si/SiO_x passivating contacts, typically the values range from to 5 - 20 fA/cm² [38], [40], [45]–[47]. In our lab, the n-type poly-Si/SiO_x stacks achieved low J_o value of 4.5 fA/cm² after a high temperature thermal annealing. And passivation quality of p-type poly-Si is less excellent but still satisfactory with J_o around 12 fA/cm².

Passivation quality of symmetric samples on 1 - 5 Ω·cm resistivity, 280 μm-thick n-type FZ c-Si wafers were shown in Table 1.3. Symmetric samples were prepared by depositing passivating layers on both sides of c-Si substrate, such as a-Si:H (n^+)/a-Si:H (i)/c-Si/a-Si:H (i)/a-Si:H (n^+) or poly-Si (p^+)/SiO_x/c-Si/SiO_x/poly-Si (p^+). The tunnelling oxide was formed wet-chemically with the thickness around 1.5 nm. These passivation properties were measured after post-deposition annealing and saturation current density J_o refers to the value of half symmetric structure.

Table 1.3: Passivation properties of symmetric samples on n-type FZ c-Si wafers

	Bulk Si	Layer thickness (nm)	τ_{eff} (ms)	iV_{OC} (mV)	J_o (fA/cm²)
n^+/i a-Si:H	Textured	6/6	1.7	688	17.2
p^+/i a-Si:H	Textured	5/9	0.6	661	54
n^+ poly-Si/SiO_x	Planar	250	15	733	4.5
p^+ poly-Si/SiO_x	Planar	250	4.5	711	14.2

Since passivation of p-type/intrinsic a-Si:H films is the limiting factor for achieving high-efficiency solar cells, p-type poly-Si passivating contact behaves as a good candidate to provide excellent passivation quality with J_o as low as 14.2 fA/cm². Based on these J_o values, high V_{OC} exceeding 700 mV can be expected. Besides, it is of great importance to provide insight into the carrier transport mechanism and fabrication process on high-efficiency c-Si solar cells.

To obtain better performance, monocrystalline FZ wafers are used. Compared to n-type wafers, p-type bulks suffer from light-induced degradation which forms boron-oxygen defects under the

light exposure [5]. Besides, p-type substrates are more sensitive for impurities. Regarding these problems, n-type FZ wafers were chosen. Two possible hybrid solar cell structures were proposed on n-type substrates based on the i/n^+ a-Si:H stacks and SiO_x/p^+ poly-Si layers, as depicted in Figure 1.10.

Front emitter structure, shown in (a), may benefit the performance with better carrier transport under increased illumination at the emitter, thus higher fill factor [34]. However, the parasitic absorption loss of 250 nm-thick poly-Si layer is more pronounced than approximately 10 nm-thick a-Si:H layers, thus limiting the J_{SC} inevitably for front emitter design [37]. With keeping same level of V_{OC} and FF, higher J_{SC} can be obtained in the rear emitter sturcture. Moreover, the disadvantage of using p-type front poly-Si passivating contact is that it affects holes collection due to current crowding at the front side which will limit the tunnelling mechanism. Therefore the priority is n-type wafer with rear emitter structure in this thesis.

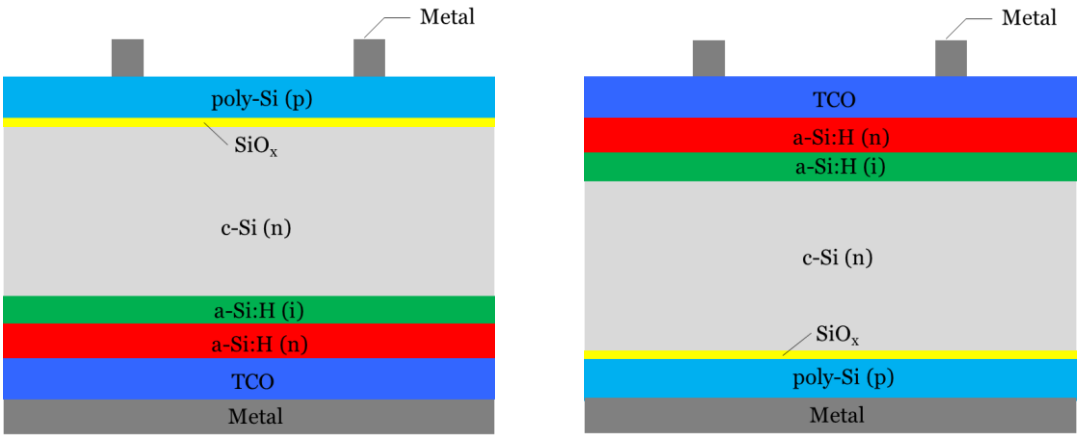


Figure 1.10: Possible structures of hybrid solar cells (not to scale): (a) n-type wafer with front emitter; (b) n-type wafer with rear emitter (priority in this thesis). Textured surface may be used to minimize external reflection and increase internal scattering for hybrid solar cells fabrication.

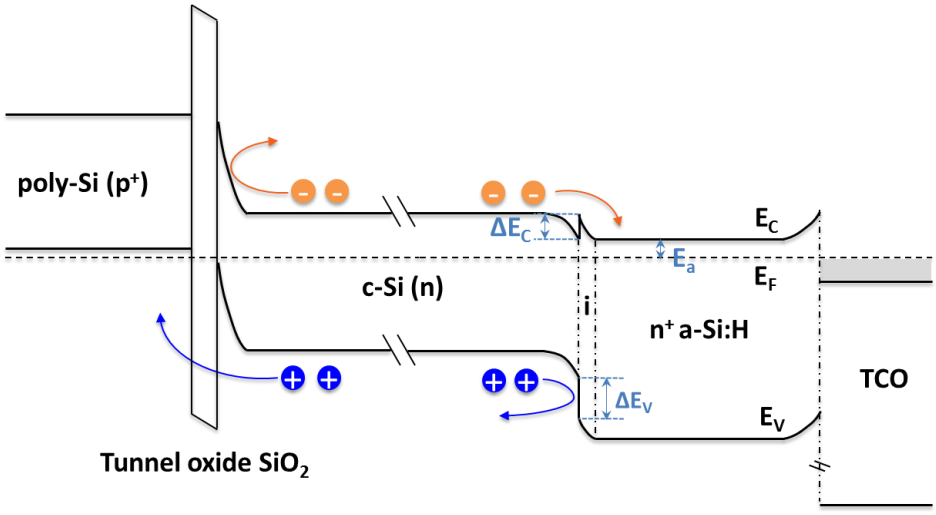


Figure 1.11: Schematic band diagram of poly-Si (p)/SiO_2/c-Si (n)/a-Si:H (i)/a-Si:H (n^+)/TCO structure of hybrid solar cells

1.4 Limiting factors for high efficiency hybrid solar cells

To fabricate high efficiency (η>20%) c-Si solar cells, three predominant parameters should basically meet requirements: J_{SC} > 38 mA/cm², V_{OC} > 700 mV and *FF* > 73%. The limiting factors primarily come from: (i) optical losses from surface reflection and parasitic absorption of non-absorber layers that limits the J_{SC}, (iii) recombination losses caused by pronounced surface recombination which decreases the V_{OC} and (iii) resistance losses due to barrier for carrier transport thus *FF*. These losses will be discussed in detail on different structure parts based on process flow.

1.4.1 Passivation of p-type poly-Si/SiO_x contact

Since B-doped poly-Si layer is placed at the rear side, the parasitic absorption at the long wavelength into this layer is merely pronounced compared to the front parasitic absorption of a-Si:H and TCO layers. Thus, effective passivation quality is the primary task to be considered for rear emitter. Based on the research in our lab, two prerequisites include: (i) thermally-stable tunneling oxide which provides good chemical passivation to c-Si surface and forms effective carrier selectivity; (ii) heavily B-doped poly-Si which creates effective band bending at the poly-Si/c-Si interface and plays an important role in field-effect passivation. The quality of tunneling oxide is critical for passivation quality. If it is too thin, passivation quality deteriorates dramatically while too thicker oxide blocks the majority carriers tunnel through the oxide

interlayer. Normally the thickness keeps around 1.5 nm for effective tunnel mechanism. Besides it should resist to high-temperature annealing and keep stable rather than breaking up when the temperature is up to 1000 °C [48]. The high passivation quality also strongly relies on the formation of heavily-doped poly-Si film where the effective dopants should mostly be confined within poly-Si layer and only a shallow portion diffuses into c-Si bulk [37], [39]. The doping profile at the poly-Si/c-Si interface can be tuned by poly-Si thickness, ion implantation dose, energy, thermal annealing temperature and time.

1.4.2 Wafer front surface texturing and wafer cleaning

Random pyramidal texturing is typically employed in c-Si wafers to minimize reflectance and increase the optical path length in the absorber layer, as so-called light in-coupling and light scattering respectively. Based on anisotropic etching, <100> oriented silicon surface is etched quickly than (111) surface. Therefore, the wafer with (100) planar surface is eventually converted into that of (111) textured surface covered with random upright pyramid in several microns. In our lab, TMAH (tetramethylammonium hydroxide, $(CH_3)_4NOH$) solution is used for etching solution with several mL ALKA-TEX. FREE solution to improve the texturing quality and extend bath lifetime. The size of random pyramids is of vital importance to surface reflection loss and passivation quality, which can be controlled by etching time and additive amount of ALKA-TEX. FREE solution. With smaller size pyramid texturing, higher J_{SC} is obtained until to a certain level due to less reflection loss and enhanced light scattering within the absorber, while V_{OC} also increases because less dangling bonds density on surface but is still not comparable to V_{OC} on planar surface [49]. Typical wafer surface with upright random pyramids is shown in Figure 1.11. Too short etching time causes surface not fully textured, while too long time leads to the large pyramid size up to 10 μm. Besides, more amount of ALKA-TEX. FREE additive accelerates the etching rate thus shorter etching time. For these reasons, optimal etching time is of great significance. Since during the texturing process, the wafers are contaminated by the etching solution and after texturing process the amorphous silicon layers will be deposited on textured silicon surface, which are very sensitive to possible contaminants. Therefore, the surface cleaning is an indispensable process to remove the organic, metallic residues and native oxide on the wafer surface. The effective cleaning may be applied for more than one cycle. The way to provide effective cleaning should be developed.

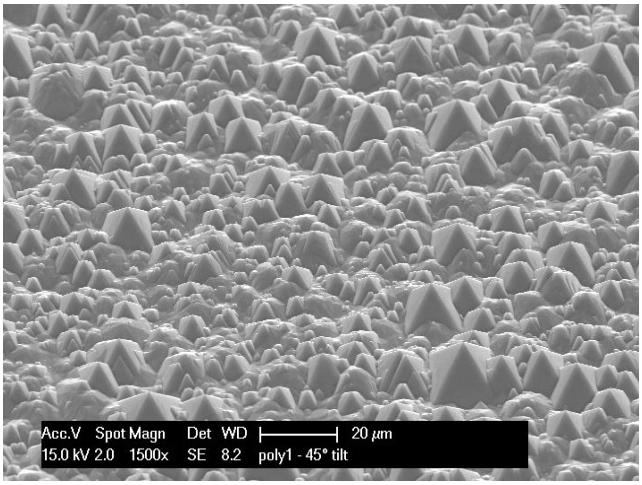


Figure 1.12: Wafer surface morphology after 30 min random pyramidal texturing in a solution of 5% TMAH and 5 mL ALKA-TEX. FREE. Taken in SEM.

1.4.3 Trade-off between V_{OC} and J_{SC} in a-Si:H layers

The variation of thickness on both intrinsic and n-type a-Si:H layers has great impact on the performance of hybrid solar cells. Intrinsic and n-type a-Si:H films provide outstanding passivation, however, as non-absorber layers on the front side, both absorb the incident light and generate parasitic absorption losses. Too thin intrinsic layer does not passivate the dangling bonds effectively, and too thin n-type film cannot form enough band bending at the interface to hinder the transport of minority carriers, which increase the recombination and degrade passivation quality dramatically thus lower $V_{OC.}$ While too thick a-Si:H stacks increase parasitic absorption losses and lead to lower J_{SC} due to the direct bandgap of around 1.7 eV and larger absorption coefficient in short wavelength region compared to c-Si. It has been reported that the collection efficiency of carriers generated in doped a-Si:H layer close to zero and only 30% absorbed light in intrinsic a-Si:H layer contributes to J_{SC} [50]. Moreover, thickness of i/n a-Si:H stacks influence the carrier transport and resistivity loss as well, which leads to an optimal value of *FF*. Suitable post-deposition annealing improves passivation significantly partly because dissociative hydrogen has more chance to diffuse into the interface and passivates the left dangling bonds. While if the annealing temperature or time is too high or long, hydrogen effusion phenomenon happens which will deteriorate passivation quality.

1.4.4 Parasitic absorption and resistivity loss in TCO layer

Since conductivity of doped amorphous silicon is rather poor, TCO layer is deposited on top. A good TCO layer should be conductive enough and concurrently transparent. High carrier concentration (10^{20} - 10^{21} cm^{-3}) and high mobility (90 – 150 $cm^2/V{\cdot}s$) are prerequisites for low resistivity of TCO layer, while low carrier concentration (10^{19} – 10^{20} cm^{-3}) is required to improve the transparency. Therefore, the plausible way is developing a TCO layer with high mobility (> 90 $cm^2/V{\cdot}s$) but low carrier concentration (< 5×10^{20} cm^{-3}). This can be achieved by changing TCO deposition parameters, post-deposition annealing optimization or developing advanced materials, such as IO:H (hydrogen-doped indium oxide). Moreover, the deposition of TCO will influence passivation quality for a-Si:H stacks due to the damage of ion bombardment to a-Si:H layers and possible hydrogen effusion from i a-Si:H/c-Si interface. Post-deposition annealing can partly heal or even fully recover passivation quality. Furthermore, work function of TCO affects the carrier transport from doped a-Si:H layer to metal contact. If work function of TCO is much larger than that of n-type a-Si:H, there will be a high energy barrier at the a-Si:H (n)/TCO interface which will hinder the transport of majority carrier electrons into front metal contacts. The suitable TCO work function should be in the range of 3.5 eV to 4.5 eV to achieve good ohmic contact according to modelling. Finally, as commonly used ARC (antireflective coating), the design of TCO layer should base on Rayleigh film principle and destructive interference to choose optimal refractive index and layer thickness.

1.4.5 Front and rear metal contacts

The front metal pattern design is considerably complex due to the competition between unwelcomed metal shading and finger resistivity. In general, the metal contact area should be as small as possible through decreasing the width of finger to minimize metal shading and benefit J_{SC}. However, to obtain a low resistivity finger design, the metal width and height should be as large as possible to increase the cross area. Moreover, the trade-off between J_{SC} and FF also exist in finger spacing. With a closer finger spacing, it is desirable for a low emitter resistance due to better lateral transport, while it causes more shading and induces more recombination between TCO and metal interface, which are detrimental to J_{SC} and V_{OC} respectively. Therefore, the general design rules are proposed: (i) a high height-to-width aspect ratio with an optimal value of metal width; (ii) optimal finger spacing when the resistance losses equal to shading loss. As for rear metal contacts, since contact recombination between metal and p-type poly-Si is quenched, full rear metal contact design is employed. In order to minimize the transmission through the back of the solar cell, silver (Ag) is used as a back reflector.

1.5 Scientific questions

The aim of this project is to fabricate high efficiency (η>20%) silicon heterojunction/poly-Si passivating contact hybrid solar cells by optimizing front surface field (FSF, consisting of i/n a-Si:H films) and transparent conductive oxide (TCO) layer. The optimal thicknesses of intrinsic and n-type a-Si:H layers should be investigated to minimize the parasitic absorption losses, while maintaining high passivation quality. A novel IO:H/ITO stacks, as an attractive alternative for conventional ITO single layer, should be developed and studied to ensure high transparency to minimize free carrier absorption (FCA) losses, but also high conductivity to guarantee high fill factor (*FF*).

Considering two main experimental parts of FSF and TCO optimizations, following research questions are formulated:

(i). Intrinsic and n-type a-Si:H optimization

- How does the pre-deposition treatment influence passivation quality?
- What are the optimal post-adeposition nnealing conditions to improve passivation quality? Does H_2 flow annealing reduce the defect density further compared to conventional air annealing?
- How do the thicknesses of i/n a-Si:H layers affect hybrid solar cells performance in terms of optical property, recombination and carrier transport?

(ii). TCO optimization

- What is the optimal post-deposition annealing condition for IO:H/ITO stacks to quench free carrier absorption, and concurrently obtain high conductivity?
- What are the differences between IO:H/ITO stacks and ITO single layer in terms of opto-electrical properties and effect on passivation quality?
- How do IO:H/ITO stacks and ITO layer influence the hybrid solar cells performance?

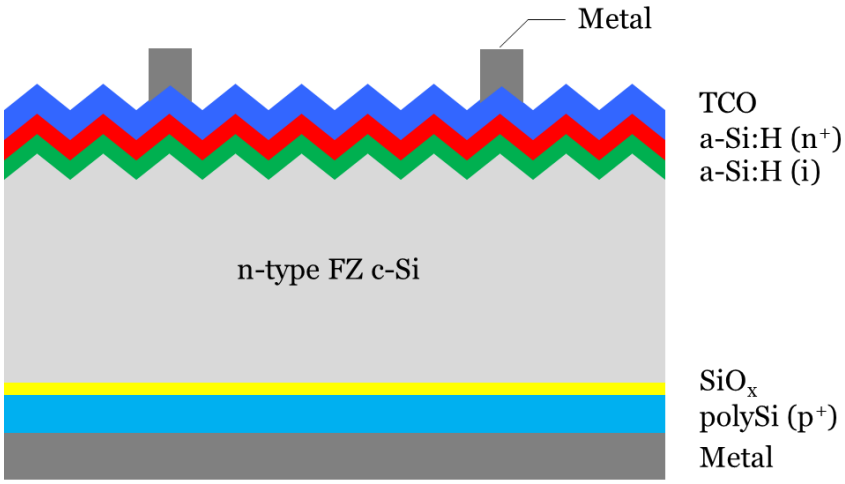


Figure 1.13: 2D schematic structure of hybrid solar cells (not to scale).

1.6 Thesis outline

This thesis consists of five chapters. Chapter 1 is the theoretical background of this project. Main recombination and passivation mechanisms behind solar cells are presented as well as relative indicators for recombination losses. Then the motivation and limiting factors for high efficiency SHJ/poly-Si passivating contact hybrid solar cells are illustrated followed by aim and outline of this thesis.

Chapter 2 offers a detailed overview of the fabrication process of hybrid solar cells and opto-electrical properties characterization techniques of films and devices.

In chapter 3, the importance of cleaning procedures are addressed first. Then post-deposition annealing conditions are investigated to improve surface passivation quality. The thicknesses of i/n a-Si:H stacks are optimized to balance parasitic absorption loss and passivation quality gain.

Chapter 4 presents a novel IO:H/ITO stacks design to improve J_{SC} while keeping *FF*. Post-deposition annealing condition is evaluated first for IO:H/ITO stacks to achieve low carrier density and high mobility. Furthermore, the differences between IO:H/ITO stacks and ITO single layer are investigated to provide hints for different performances on hybrid solar cells.

Finally, chapter 5 summarizes the findings from this project and presents outlook for further improvements on SHJ/poly-Si passivating contact hybrid solar cells.

2

Techniques for Hybrid Solar Cells Fabrication and Characterization

2.1 Fabrication of hybrid solar cells

In this section, the fabrication steps of hybrid solar cells will be introduced. With the term of 'hybrid', it is intended as a solar cell that has a medium thermal budget, in the sense that high temperature approach of poly-Si (T>900 °C) and low temperature process of a-Si:H (T<250 °C) are combined. The carrier-selective passivating rear emitter consisting of ultra-thin tunneling oxide and heavily-doped p-type poly-Si is formed first. After the front surface texturing, few-nanometer thick intrinsic and n-type a-Si:H are deposited by PECVD as front surface field. Transparent conductive oxide is then sputtered on top of a-Si:H layer to help lateral transport of electrons. Finally, front and rear metal contacts are formed by evaporation technique via lift-off method. In this work, high quality n-type FZ c-Si wafers with <100> orientation, resistivity of 1 – 5 Ω·cm and thickness of 280 μm were used as starting materials.

2.1.1 Carrier-selective passivating rear emitter

Rear emitter consists of an ultra-thin tunneling oxide film and a boron-doped poly-Si layer, which are fabricated by a four-step process at the rear planar surface of c-Si wafer. First, the growth of tunneling oxide layer (SiO_2) is optimized by one-step Nitric Acid Oxidation of Silicon (NAOS) cleaning. To remove the native oxide, the c-Si wafer is dipped in 0.55% HF for 4 min. One-step NAOS is then used by 69.5% room temperature HNO_3 immersion for 1 hour to form

stable tunneling oxide approximately 15 Å-thick on both sides of the wafer, followed by 5 min DI water rinse. The second step is the intrinsic amorphous silicon deposition by means of low-pressure chemical vapor deposition (LPCVD) technique. Tempress LPCVD tube furnace in EKL lab is used to deposit 250 nm-thick intrinsic a-Si on top of the SiO_2 layer on both sides of the wafer, with the conditions of temperature of 580 °C, pressure of 150 mTorr and SiH_4 gas flow of 45 sccm. Third, an ex-situ single-side doping process is achieved by ion-implantation step. Varian Implanter E500HP is used to implant B atoms into the a-Si layer to form a doped layer. The implantation energy is 5 keV and dose is 5×10^{15} ion/cm^2. Junction depth in this case is in the order of 10 nm. Finally, 950 °C high-temperature N_2/O_2 atmosphere annealing is used to activate and drive-in the dopants to diffuse into a-Si layer and even form small doping tail within the c-Si bulk which is necessary for an effective carrier transport through the tunneling oxide layer [39]. Moreover, annealing treatment crystallizes a-Si into poly-Si film. Below are B-doping profiles measured by ECV (electrochemical capacitance-voltage) profiling with optimal implantation energy of 5 keV and dose of 5×10^{15} ion/cm^2 and annealing temperature of 190 °C in Figure 2.1.

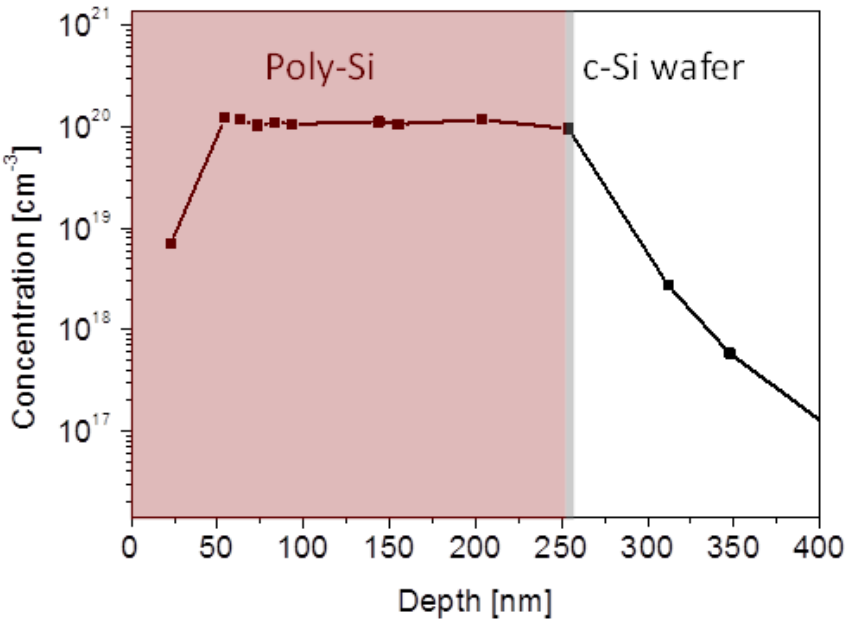


Figure 2.1: B-doping profile on 250 nm poly-Si passivating contacts (5 keV implantation energy, 5×10^{15} ion/cm^2 dose and annealing at 950 °C in N_2/O_2 atmosphere). Measured by ECV.

For p-type poly-Si passivating contacts, the optimal passivation quality is achieved with τ_{eff} = 4.5 ms, J_o = 14.2 fA/cm^2 and iV_{OC} = 711 mV, which is excellent enough for rear emitter. Therefore, further improvement is not the prior task for this thesis.

2.1.2 Heterojunction front surface field

To minimize the front external reflection and improve the light scattering in the absorber, random pyramidal texturing is employed. Based on anisotropic etching, <100> oriented c-Si wafers front surface is preliminary randomly textured by 5% TMAH solution with 120 mL ALKA-TEX. FREE for 20 min, forming <111> oriented upright random pyramidal surface in several microns size (see Figure 2.2). While the rear poly-Si surface is protected by 200 nm-thick SiN_x capping layer which is hardly etched by TMAH solution. Then three-steps Nitric Acid Oxidation Cycle (NAOC) cleaning in EKL cleaning line is used to remove contamination in the wafer surface. 99% room temperature HNO_3 solution is used for 10 min to remove organic contamination, followed by 5 min DI water rinse. Next, 69.5% HNO_3 solution at 110 °C for 10 min followed by 5 min DI water is to clean the metallic residues. Finally, 0.55% HF dip is used to remove chemical oxide layer for 4 min followed by 5 min DI water. The NAOC cleaning is applied for 1-3 times to provide more effective surface cleaning which can avoid any contamination inducing passivation degradation.

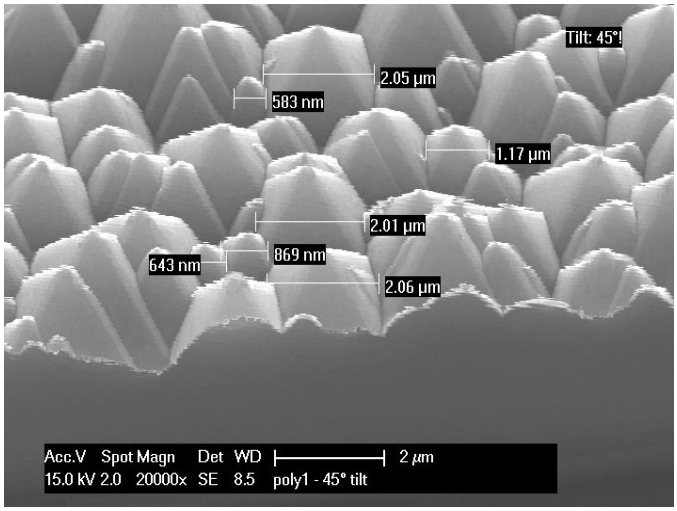


Figure 2.2: Front surface morphology after 20 min random pyramidal texturing in a solution of 5% TMAH with 120 mL ALKA-TEX. FREE. Taken in SEM.

Afterwards, the wafer is transferred swiftly to Amor chamber for depositing intrinsic and n-type a-Si:H films on the textured front side by radio frequency plasma-enhanced chemical vapor deposition (RF-PECVD) technique. To avoid any cross-contamination from deposition chamber, H_2 plasma treatment is used and the substrate holder is covered by 100 nm intrinsic a-Si:H to prevent contamination from the holder. After placing the wafer into Amor chamber, 30 min preheating is used to heat the sample to set temperature value. Pure SiH_4 gas is used to deposit intrinsic a-Si:H film, and together with the precursor gases of hydrogen-diluted PH_3, n-type

a-Si:H layer is formed. Silicon epitaxial growth during intrinsic a-Si:H deposition should be avoided to ensure an atomically sharp interface between c-Si and intrinsic a-Si:H layer [51]. Moreover, low-damage plasma process should be optimized and controlled to obtain a high passivation quality. The deposition conditions (chamber pressure, power of plasma and substrate temperature) and precursor gas properties (precursor gas content and ratio) are of great significance for the opto-electrical properties and passivation quality of a-Si:H layers [52], [53].

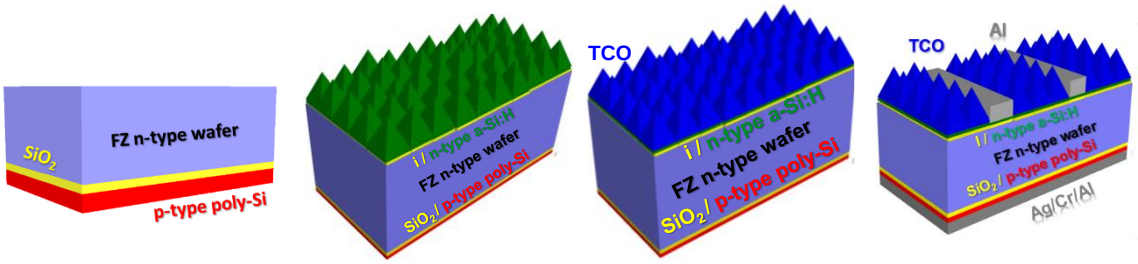
2.1.3 Front transparent conductive oxide

To solve issue with lateral conductivity of electrons to metal electrodes, front transparent conductive oxide (TCO) film is deposited on top of the a-Si:H layer. RF sputtering is used to deposit TCO layers in Zorro instrument. As a physical vapor deposition (PVD) technique, TCO films are deposited on the wafer by the impingement of energetic Ar ions to TCO material targets. Typically, 75 nm TCO layer is sputtered to provide antireflective effect based on destructive interference principle, which can decrease external reflection further in addition to the textured surface design. The most important features of this layer are to ensure high conductivity to improve *FF*, but also high transparency to minimize the parasitic absorption loss thus obtaining high J_{SC}.

2.1.4 Front and rear metal contacts

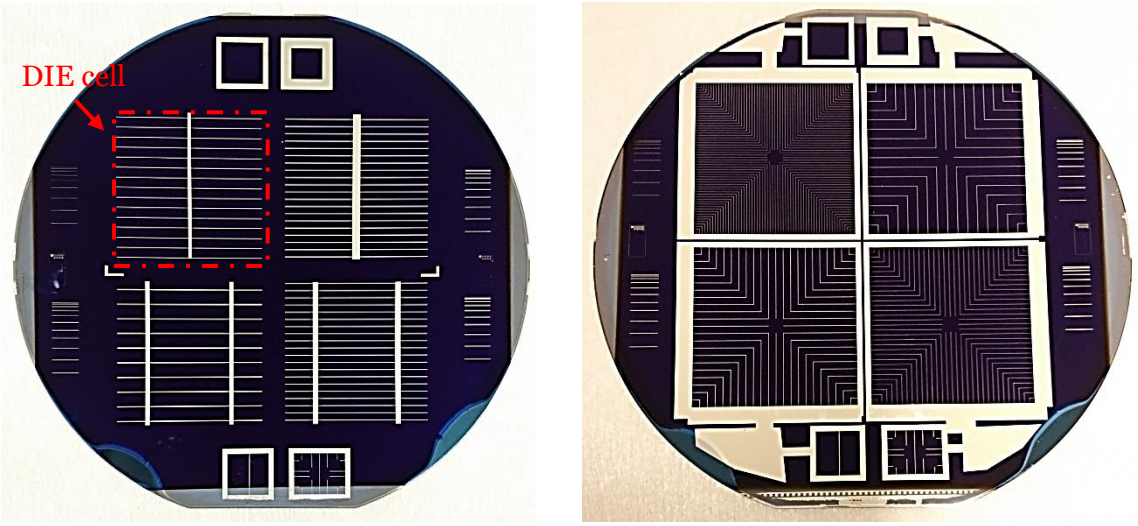
Metallization, as the last process step, is carried out to deposit 6 μm Al at the front textured surface and 200 nm Ag – 30 nm Cr – 2 μm Al at planar rear side. Aluminum (Al) is used as the main conductive layer due to the reasonably high conductivity and cheap price. Silver (Ag), as the most conductive metal, is deposited at the rear side as the first metal layer because of the low contact resistance between poly-Si and Ag interface and back reflection effect. The thin chromium (Cr) film is provide as the intermediate layer to prevent Ag and Al from mixing together during high temperature annealing. As PVD techniques, thermal evaporation and e-beam evaporation are chosen which mainly depends on the melting point of metal. Ag is deposited by thermal evaporation technique that is designed for evaporating relatively low melting point materials. With applying high voltage to a tungsten boat, the temperature increases up to the melting point of 962 °C for Al. Then Ag is evaporated and deposited at the wafer surface. Al and Cr are deposited by e-beam evaporation. The mechanism is that high kinetic energy electron beams impinge the Al or Cr material on the crucible and convert the kinetic energy into thermal energy that melts the Al or Cr to evaporate to the wafers. E-beam

evaporation is primarily designed for evaporating the materials with high melting point, such as Cr with melting point of 1907 °C. Although Al has a rather low melting point of 660 °C, it can form alloy with the tungsten boat that leads to tungsten boat ate by the melted Al if thermal evaporation is used. Thus e-beam evaporation is used for Al deposition. Two hybrid solar cells with different metal patterns are shown in Figure 2.4. Entire process flow is shown in Figure 2.3.



(a) (b) (c) (d)

Figure 2.3: Process flowchart of hybrid solar cells: (a) carrier-selective passivating rear emitter (SiO_2/p poly-Si); (b) heterojunction front surface field (i/n a-Si:H); (c) front transparent conductive oxide (TCO); (d) front and rear metal contacts.



(a) (b)

Figure 2.4: Pictures of hybrid solar cells with two different metal pattens fabricated in the facility of PVMD group at Delft University of Technology. A wafer consists of four DIE cells in the middle. (a) 2.8 cm × 2.8 cm DIE cell with busbas in the middle; (b) 3 cm × 3 cm DIE cell with busbar at the edge.

2.2 Opto-electrical properties of films and devices

In this section, the methods for films and solar cells characterization will be introduced in terms of optical and electrical properties. To evaluate and monitor the passivation quality of wafers and solar cells, Quasi-Steady-State Photoconductance measurement is used. Hall effect measurement and four-point probe method are used to investigate the electrical properties of TCO films. Reflectance and transmittance measurement are used to characterized the optical properties of TCO films and solar cells. For device characterization, illuminate *J-V* and external quantum efficiency are used.

2.2.1 Quasi-Steady-State Photoconductance (QSSPC) measurement

Quasi-Steady-State Photoconductance (QSSPC) measurement is a contactless characterization technique for passivation quality, as a step by step monitoring tool during solar cells fabrication, which is measured by Sinton WCT-120 Lifetime Tester. The principle of QSSPC is by using infrared light flash the excess carriers are created on the sample which increases the conductance of the sample. The photoconductance can be sensed by a contactless coil circuit underneath the instrument stage and the intensity of the flash can be measured by light sensor incorporated in the stage. Considering equal number of electrons and holes generated, the excess photoconductance (σ_L) of a n-type wafer is proportional to excess minority carrier density and mobilities of electrons and holes,

$$\sigma_L = q\Delta p(\mu_n + \mu_p)W \tag{2.1}$$

where q is the elementary charge, Δp is excess minority carrier hole density, μ_n and μ_p are the mobility of electrons and holes respectively and W is the sample thickness.

A measurement of the photoconductance is therefore, a nearly direct way of probing for the excess carrier density.

Minority carrier lifetime can be analyzed according to continuity equation then. Since the uniform distribution of excess carriers is assumed and no external electrical field exists, the transport equation for n-type wafer can be simplified

$$G - \frac{\Delta p}{\tau_{eff}} = \frac{d\Delta p}{dt} \tag{2.2}$$

where G is photogeneration rate of charge carriers. The effective minority carrier lifetime (τ_{eff}) is

$$\tau_{eff} = \frac{\Delta p}{G - \frac{d\Delta p}{dt}} \tag{2.3}$$

Based on the range of minority carrier lifetime, two methods were employed. One is the Quasi-Steady-State (QSS) mode for low lifetime samples of less than 100 µs. Under this condition, $G \gg \frac{d\Delta p}{dt}$, the lifetime in Equation 2.3 can be reduced to

$$\tau_{eff} = \frac{\Delta p}{G} \tag{2.4}$$

When carrier lifetime is larger than 100 µs, the transient mode is used. At this circumstance, as the excess carrier generation rate *G* is less pronounced and assumed to be zero, the lifetime then becomes

$$\tau_{eff} = -\frac{\Delta p}{\frac{d\Delta p}{dt}} \tag{2.5}$$

Since the lifetime of samples fabricated in this thesis exceeds 600 µs, transient model is used. Effective lifetime is a function of the excess minority carrier concentration and a typical graph of FZ n-type c-Si wafer passivated by 20 nm intrinsic a-Si:H layer on both sides was shown in Figure 2.5.

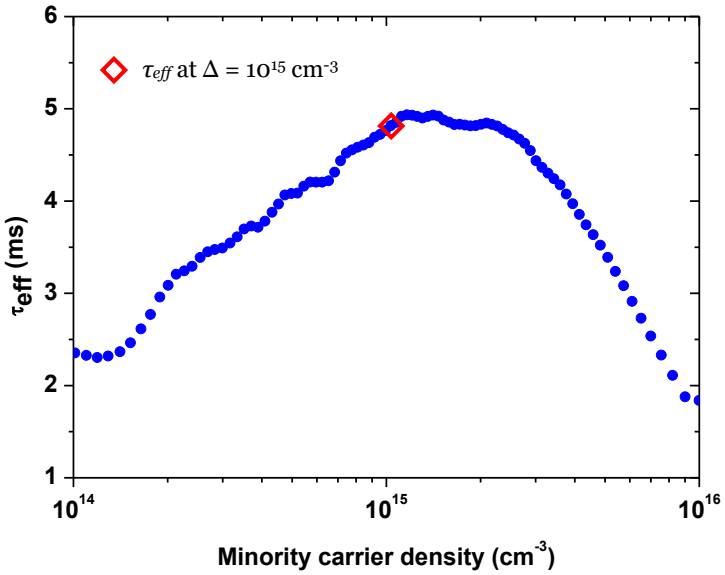


Figure 2.5: Effective minority carrier lifetime of FZ n-type c-Si wafer passivated by 20 nm i a-Si:H on both sides after 190 °C annealing in air for 30 min as a function of excess carrier density.

At high injection levels, the minority carrier lifetime is limited by Auger recombination. Moreover, implied open circuit voltage (iV_{OC}) can be deduced based on the excess carrier density measurement, which is due to the splitting of the quasi-Fermi level depending on the excess charge carrier density [54]. For n-type wafers, the implied open circuit voltage at one-sun illumination can be expressed by

$$iV_{OC} = \frac{k_B T}{q} \ln\left(\frac{\Delta n(N_D+\Delta n)}{n_i^2}\right) \tag{2.6}$$

where k_B is Boltzmann constant, T is temperature, Δn is excess minority carrier electron density, N_D is concentration of donors and n_i is intrinsic concentration of carriers.

2.2.2 Hall effect measurement

Ecopia HMS-5000 Hall Effect setup is the instrument for characterization of carrier density, mobility and resistivity of TCO thin films. The theoretical basis underlying the Hall effect measurement is Lorentz force and Van der Pauw technique. The sample is placed perpendicular to an applied magnetic field on the sample board connecting with four point probes at the corners. When a fixed current flows through the sample, electrons experience a magnetic force and are subject to flow towards to the sample side. The charge difference results in a voltage drop across the sample, so-called Hall voltage (V_H). By measuring the Hall voltage (V_H) and resistivity (ρ) via van der Pauw technique, the carrier density N and mobility μ can be determined by

$$N = \frac{IB}{q\,|V_H|} \tag{2.7}$$

$$\mu = \frac{|V_H|}{IB\rho} \tag{2.8}$$

where I is the fixed current passing through the sample, B is the magnetic field and q is the elementary charge. For best results, the samples should be square in shape and normally 10 mm × 10 mm is preferred in size.

Figure 2.6: Sample mounting fixture: (a) with upper cooling reservoir; (b) zoom-in of sample stage.

2.2.3 Four-point probe

Sheet resistance of TCO films was measured by means of a four-point probe apparatus, which consists of four equally spaced tungsten metal tips. By applying a current flow through two outer probes, the voltage across the inner voltage probes can be measured. The sheet resistance (R_{sheet}) is then determined by

$$R_{sheet} = \frac{\pi}{ln2}\left(\frac{V}{I}\right) \tag{2.9}$$

where V is the voltage across the inner voltage probes, I is the current across two current probes and $\pi/ln\ 2$ is a geometric factor of a semi-infinite thin sheet, which equals to 4.53.

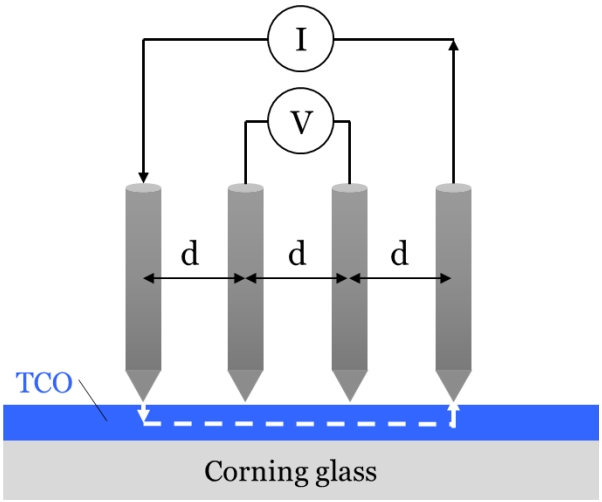


Figure 2.7: Schematic sketch of four-point probe measurement.

2.2.4 Illuminated *J-V*

Illuminated *J-V* measurement is realized by measuring the current of the solar cell with a range of applied voltage under standard test conditions (STC)[1], which is achieved by AAA class Wacom WXS–156S solar simulator. The main external solar cell parameters are obtained from illuminated *J-V* measurement: short circuit current density (J_{SC}), open circuit voltage (V_{OC}), fill factor (*FF*) and conversion efficiency (η). Besides, other important parameters of maximum power (P_{max}), series resistance (R_s) and shunt resistance (R_{sh}) can be determined as well. The typical illuminated *J-V* characteristic of hybrid solar cell is shown in Figure 2.8.

The short circuit current density J_{SC} is defined as current per unit area that flows through the external circuit at short circuit condition, which is also the maximum current density delivered by a solar cell. J_{sc} of a solar cell depends on the photon flux incident on the solar cell, which is determined by the spectrum of the incident light. Therefore, before solar cell measurement, two reference cells of Fraunhofer Institute for Solar Energy Systems were used to calibrate. In hybrid solar cells, J_{SC} strongly relys on the optical properties, such as the absorption in the absorber layer (c-Si bulk) or parasitic absorption losses in the TCO, a-Si:H films and poly-Si layer and surface reflection. The open circuit voltage V_{OC} is the maximum voltage that a solar cell can deliver when no current flows through the external circuit. V_{OC} depends on the photo-generated current density and saturation current density of a solar cell, as described in Equation 2.10,

$$V_{OC} = \frac{k_B T}{q} \ln\left(\frac{J_{ph}}{J_0} + 1\right) \tag{2.10}$$

where J_{ph} is the photo-generated current density and J_o is the saturation current density. Since J_o describes the recombination state in the solar cell, excellent passivation quality gives a low value of J_o thus leading to a high V_{OC}. In hybrid solar cells, V_{OC} is limited by the passivation quality of a-Si:H layers and rear poly-Si although typically a V_{OC} exceeding 700 mV can be measured. The fill factor (*FF*) is the ratio of the maximum power (P_{max}) to the product of V_{OC} and J_{SC}.

$$P_{max} = V_{mpp} J_{mpp} \tag{2.11}$$

$$FF = \frac{P_{max}}{V_{OC}\, J_{SC}} \tag{2.12}$$

[1] Standard test conditions (STC) are defined as the solar irradiation of 1000 W/m² under AM 1.5 spectrum illumination and the constant solar cell temperature of 25 °C.

where V_{mpp} and J_{mpp} are the voltage and current at the maximum power point (MPP) respectively. In practice *FF* is strongly influenced by the series resistance R_s and the shunt resistance $R_{sh.}$ For hybrid solar cells, the series resistance comes from three main parts: (1) the movement of carriers though the a-Si:H layers, TCO and the bulk itself; (2) the contact resistance between the interfaces, such as a-Si:H/TCO and TCO/metal heterointerface; (3) the resistance of the top and rear metal contacts. And the shunt resistance is primarily caused by the leakage across the p-n junction around the edge and the crystal defects, pinholes or impurity precipitates. Lower series resistance and higher shunt resistance lead to higher *FF*. The conversion efficiency η is then defined as the ratio between the maximum power generated and the incident power P_{in}, which is equal to 1000 W/m² at STC.

$$\eta = \frac{V_{OC} J_{SC} FF}{P_{in}} \tag{2.13}$$

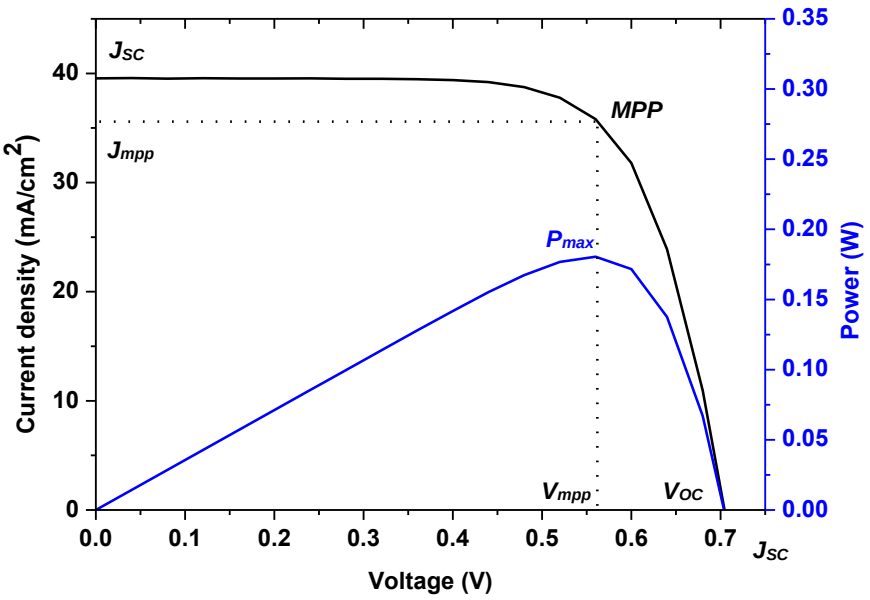


Figure 2.8: Illuminated J-V curve (black) and power output (blue) of 9 cm² hybrid solar cell under AM 1.5 illumination.

2.2.5 Reflectance, transmittance and absorbance

Reflectance (*R*) and transmittance (*T*) of TCO films and solar cells were measured by PerkinElmer Lambda 950 spectrophotometer to provide optical properties of the materials.

With the tungsten-halogen lamp and deuterium light source, a wide range of UV/visible/NIR spectra from 175 nm to 3300 nm is provided. The main component is a 150 mm-diameter integrating sphere (IS) internally coated with Spectralon, which is a highly reflective material. The optical design of 150 mm IS is shown in Figure 2.9. By placing the sample in the transmittance sample holder at the entrance of the sphere or reflectance sample holder at the rear side, either transmitted or reflected light from the sample can be measured by optical detector, which is then compared with the reference beam to obtain the actual transmittance and reflectance respectively. Two optical detectors are used to measure the light intensity and they change the measurement point at the wavelength of 860 nm, therefore there is a small turbulence observed in R and T curves. Before the sample measurement, the calibration consisting of 0% reference signal and 100% reference signal is carried out to rule out any influence from outside light. The absorbance (A) then can be calculated by $1-R-T$.

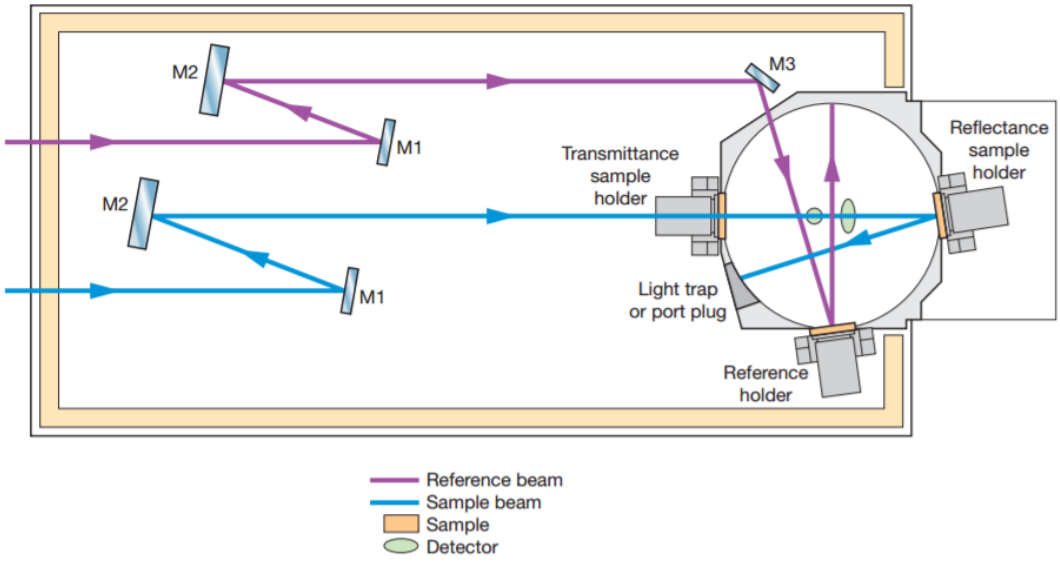


Figure 2.9: Top view of 150 mm integrating sphere (IS) and its optical design [55].

2.2.6 External quantum efficiency

The external quantum efficiency (*EQE*) is the ratio of the number of the charge carriers successfully collected to the number of the photons incident on the solar cell. Since it is wavelength dependent, the monochromatic light of wavelength λ_o is used to illuminate the solar cell and generate the photocurrent I_{ph}. Then *EQE* is determined by

$$EQE(\lambda_0) = \frac{I_{ph}(\lambda_0)}{q\,\Phi_{ph}(\lambda_0)} \tag{2.14}$$

where q is the elementary charge and ϕ_{ph} is the photon flux incident on the solar cell.

An in-house EQE setup is used and shown in Figure 2.10. 300 W Xenon arc lamp is used to emit a broad wavelength spectrum and the light is then pass through the optical chopper to modulate the intensity. Modulated light is send through filters and into an Oriel monochromator to generate a monochromatic light output. The output beam is finally focused by several lenses to a well-defined 3 mm² area on solar cell sample placed in the sample holder. With the metallic probes connected to the solar cell front and rear electrodes, the photo-generated current can be measured. The digital lock-in amplifier is used to isolate the signal from background noise, control the optical chopper. Combining the photon flux ϕ_{ph} at a certain wavelength with the EQE measured, J_{SC} of a hybrid solar cell is then calculated by

$$J_{SC} = q\int_{300}^{1200} EQE(\lambda)\phi(\lambda)d\lambda \tag{2.15}$$

Here only the spectral wavelength range from 300 nm to 1200 nm is chosen because the spectral power density of AM 1.5 is nearly zero below 300 nm and rare photos are absorbed by c-Si after 1200 nm wavelength due to the bandgap. In hybrid solar cells, both optical losses, such as parasitic absorption and reflection, and recombination loss have impact on the EQE spectrum.

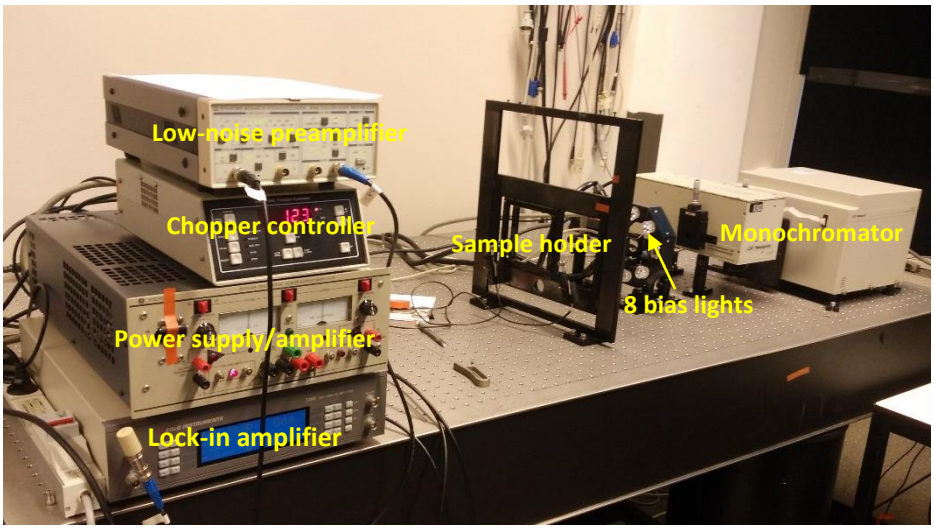


Figure 2.10: In-house EQE steup in PVMD group.

3

Influence of Intrinsic/n-type a-Si:H Layers on Hybrid Solar Cells

3.1 Introduction

In order to suppress the surface recombination of c-Si, intrinsic and n-type hydrogenated amorphous silicon (a-Si:H) layers are used as front surface field (FSF) on hybrid solar cells. Intrinsic a-Si:H provides an excellent chemical passivation to c-Si surface, which improves the V_{OC} well above 700 mV compared to the structure without intrinsic layer [25], [56]. And n-type a-Si:H induces an internal electrical field that creates high band bending at the interface. This provides field-effect passivation to repel the holes away. As the band diagram shown in Figure 3.1, when the electrons transport to the interface, with the aid of tunneling and/or thermionic emission, the band offset of ΔE_C can be overcome and the electrons then flow into n-type a-Si:H layer [57]. While the energy barrier for holes is much larger, they are less likely to pass through the a-Si:H layers. So a-Si:H behaves as a prominent carrier-selective passivating contact. To ensure effective electrons transport into a-Si:H, the activation energy E_a of n-type a-Si:H film should be as low as possible and the suitable value of E_a is around 0.2 eV [58], [59]. However, the drawback for the application of a-Si:H as FSF is that it causes the parasitic absorption in the short wavelength. This is because a-Si:H is a direct bandgap material with the optical bandgap of approximately 1.7 eV, which absorbs the UV and visible light strongly compared to c-Si [39]. The absorption coefficient of a-Si:H is much larger than that of c-Si when the wavelength is less than 700 nm as depicted in Figure 3.2. It also was reported that the collection efficiency of carriers generated in n-type a-Si:H layer is zero and only 30% absorbed light in intrinsic a-Si:H

layer contributes to J_{SC} [50]. The parasitic absorption of a-Si:H limits the J_{SC} to a higher level. Another limitation of the application of a-Si:H passivating contacts is the lack of thermal stability during high-temperature process (such as contact firing after industrial screen printing). Typically, low temperatures below 200 °C are used for processing a-Si:H/c-Si based SHJ solar cells to avoid any thermal damage to a-Si:H layers [31], [34], [43].

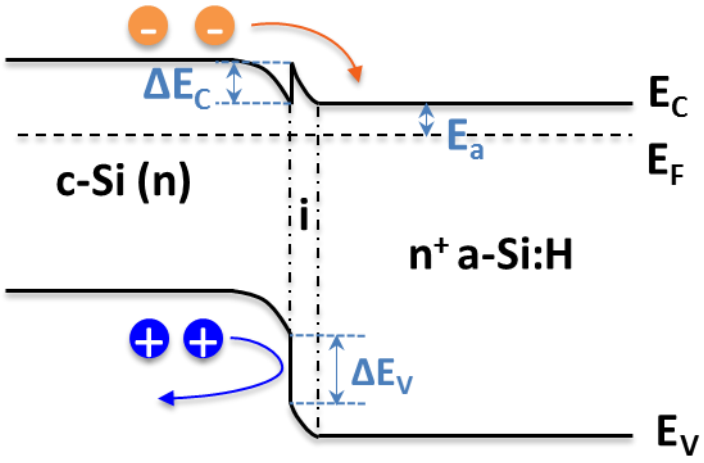


Figure 3.1: Schematic band diagram of a-Si:H (n)/a-Si:H (i)/c-Si (n) structure.

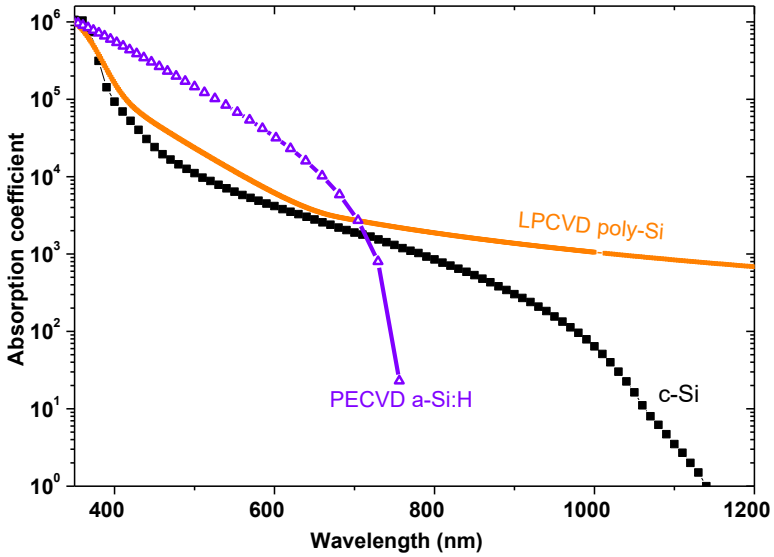


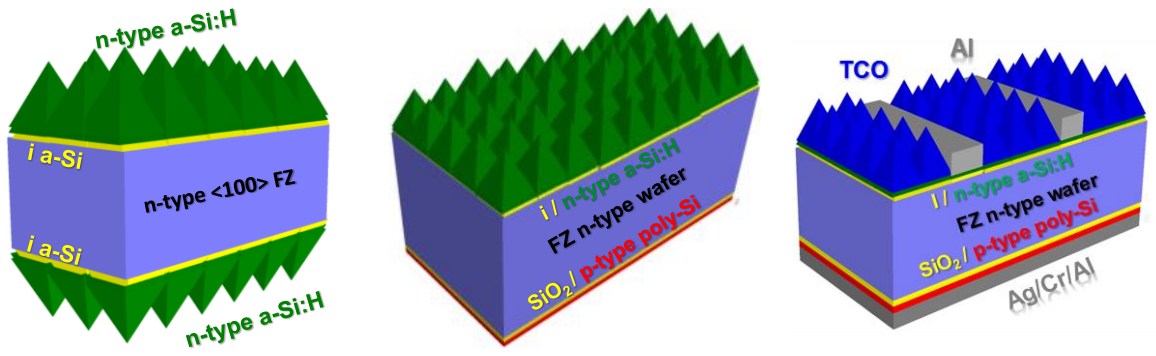
Figure 3.2: Absorption coefficient of PECVD a-Si:H, LPCVD poly-Si and c-Si.

Plasma-enhanced chemical vapor deposition (PECVD) is a mature technique for a-Si:H growth. Silane (SiH_4) is a widely used gas precursor for a-Si:H deposition. By introducing phosphine

(PH_3) or diborane (B_2H_6) gas, intrinsic, n- or p-type a-Si:H can be obtained. The deposition conditions (chamber pressure, power of plasma, substrate temperature and gas flow) and material properties (precursor gas content and ratio) are of great significance to the opto-electrical properties and passivation quality of a-Si:H layers [52], [53], [60], [61]. To obtain a good passivation quality, deposition conditions should be optimized to obtain low-damage plasma deposition process. And silicon epitaxial growth during intrinsic a-Si:H deposition should be avoided to ensure an atomically sharp interface between c-Si and intrinsic a-Si:H layer [51]. Besides, cleaning procedure is of great importance to obtain excellent surface passivation to c-Si wafer [62], [63]. This is usually achieved by wet-chemical process. Moreover post-deposition annealing improves passivation quality dramatically even in air environment, but the moderate temperature is highly preferred [64], [65].

In this chapter, the cleaning procedures were first investigated as an initial but crucial step for passivation quality. Then post-deposition annealing as an effective passivation method was studied in terms of annealing temperature, time and environment. Finally, the effect of intrinsic and n-type a-Si:H layers thickness on the electrical property of symmetric structures were carried out, along with the opto-electrical performance on hybrid solar cells.

3.2 Passivation of i/n a-Si:H stacks and performance on solar cells



(a) (b) (c)

Figure 3.3: Schematic sample structures on n-type c-Si FZ wafer: (a) symmetric structure with i/n a-Si:H layers on both-side textured surfaces; (b) a precursor cell with i/n a-Si:H layers on front textured surface and SiO_x/poly-Si films on rear flat surface; (c) a complete hybrid solar cell.

Figure 3.3 shows three different experiment samples: (a) symmetric structure of a-Si:H(n) /a-Si:H(i)/c-Si/a-Si:H(i)/a-Si:H(n); (b) precursor cell of a-Si:H(n)/a-Si:H(i)/c-Si/SiO_x/poly

-Si(p); and (c) finished hybrid solar cell with front TCO and metal.

High quality n-type FZ wafers with (100) orientation, low resistivity of 1 – 5 Ω·cm and thickness of 280 μm were used to fabricate symmetric passivation test structures and hybrid solar cells. To prepare the symmetric structure as illustrated in Figure 3.3 (a), the following steps were employed:

1. Texturing: 5% TMAH (4 L H_2O and 1 L 25% TMAH) and 120 mL ALKA-TEX. FREE solution for 20 min, then DI water rinse for 5 min and dry in the spin dryer;
2. NAOC (Nitric Acid Oxidation Cycle) cleaning: 99% room temperature (RT) HNO_3 for 10 min followed by 5 min DI water rinse to remove organic contaminants, then 69.5% HNO_3 at 110 °C for 10 min followed by 5 min DI water to clean the metallic residues, finally 0.55% HF dip for 4 min to remove oxide layer. The NAOS cleaning may repeat 1-3 times to provide effective surface cleaning, but after the first time entire NAOS cleaning, the first 99% RT HNO_3 immersion for 10 min and 5 min DI water rinse can be skipped in following NAOS cleaning;
3. RF-PECVD: after NAOS cleaning, the wafers should be transferred swiftly to vacuum environment in Amor chamber to prevent from surface oxidation. After preheating for 30 min, i/n a-Si:H layers were deposited at the same deposition chamber on both sides. The deposition conditions of i/n a-Si:H layers are shown in Table 3.1.

For precursor cells and hybrid solar cells as depicted in Figure 3.3 (b) and (c), the fabrication steps are as follows:

1. Rear emitter (tunneling oxide and p-type poly-Si):
   - Tunneling oxide: 0.55% HF dip for 4 min to remove native oxide; then 69.5% room temperature HNO_3 immersion for 1 h to form around 15 Å tunneling oxide
   - Heavily-doped p-type poly-Si: 250 nm thick intrinsic a-Si layer deposition by Low Pressure Chemical Vapor Deposition (LPCVD); boron implantation with E=5 keV and D=5×10^{15} ion/cm^2 to form doped film; 950 °C high-temperature N_2/O_2 atmosphere annealing to activate, drive-in dopants and crystallize a-Si
   - SiN_x capping on poly-Si side to prevent from etching during texturing process
2. Texturing and front surface field (i/n a-Si:H layers): the same processes as symmetric structures described above (Precursor cells were finished);
3. TCO sputtering: 65 nm IO:H capped by 10 nm ITO deposited by RF-sputtering on textured front surface. The detailed deposition conditions were shown in Table 4.1;
4. Front and rear metal contacts: 6 μm Al evaporated at front textured surface and 200 nm Ag – 30 nm Cr – 2 μm Al evaporated at planar rear side.

Passivation quality was evaluated by Sinton WCT-120 Lifetime Tester based on transient mode. The values of τ_{eff} and iV_{OC} were reported when the minority carrier density (MCD) is 1×10^{15} cm^{-3}

with optical constant of 0.7. The illuminated *J-V* curve of hybrid solar cells was measured by AAA Wacom solar simulator and *pFF* was measured by Sinton Suns-V_{OC} stage. The *EQE* and *R/T* measurement were carried out by an in-house application and Lambda 950 spectrophotometer respectively.

Table 3.1: Deposition conditions of intrinsic and n-type a-Si:H in Amor

	i a-Si:H	n a-Si:H
Amor chamber	2	2
SiH_4 (sccm)	11	11
PH_3 (2% in H_2) (sccm)	-	40
$P_{deposition}$ (mbar)	0.6	0.6
$T_{substrate}$ (°C)	180	180
$T_{hearter}$ (°C)	298	298
$P_{RF,\ measure}$ (W)	2	2

3.2.1 Importance of cleaning procedures

NAOS number of cycles

It is of great importance to ensure effective surface cleaning for c-Si before i/n a-Si:H deposition, especially after the TMAH texturing process since it induces contaminations and micro-roughness on the surface [66]. Passivation measurements were used as main indicators to evaluate the effectiveness of cleaning on symmetric structures with 4.5 nm intrinsic a-Si:H and 6 nm n-type a-Si:H layer deposited on double-side textured c-Si wafers. The only variable is the NAOC cleaning time: ×1 NAOC, ×2 NAOC and ×3 NAOC.

Figure 3.4 shows effective lifetime improves with NAOC cleaning times increasing from 1.3 ms for ×1 NAOC to 4.8 ms for ×3 NAOC on as-deposited samples. After 190 °C 30 min annealing on oven, the lifetime boosts dramatically and this increment is most evident for three-time NAOC cleaning with high lifetime of 12.6 ms. Since the NAOC cleaning is time-consuming which takes at least 40 min for one round, ×1 NAOC was used for all symmetric structure passivation tests and ×3 NAOC is considered to be effective for high-efficiency solar cell fabrication.

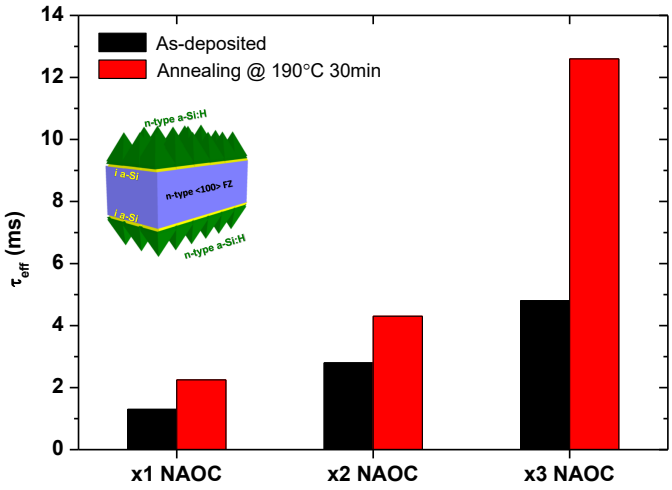


Figure 3.4: Effective minority carrier lifetime ($\Delta=10^{15}$ cm^{-3}) on symmetric structures with different NAOC cleaning times.

Plasma cleaning of chamber and plasma deposition on holder

Two precursor cells were prepared to evaluate the chamber cleaning and holder deposition issues. Tunneling oxide capped with boron-implanted poly-Si of 250 nm thickness was formed as rear emitter. Then 7 nm/6 nm i/n a-Si:H stacks were deposited at the front textured surface as FSF. No chamber cleaning and substrate holder deposition was applied to first sample before PECVD deposition, while for the second sample, 20-minute hydrogen plasma treatment (60 W power plasma with 200 sccm H_2 flow) was used to clean the chamber and the substrate holder was covered by 100 nm intrinsic a-Si:H.

The improved passivation quality, in Figure 3.5, reveals both cleaning processes are inevitable for high quality a-Si:H passivating contacts. The lifetime increases from 3.5 ms to 5.3 ms with iV_{oc} of 709 mV after cleaning. This is due to that boron or phosphorus adhered to the chamber wall or substrate holders can be unintentionally deposited into the subsequent intrinsic or doped layers and induce more recombination centers. This can be even worse when intrinsic and n-type a-Si:H are deposited in the same chamber and the substrate holders are not used separately for different doped layers deposition in available facilities. The same effect was reported in other groups that this cross-contamination would deteriorate passivation quality [44], [67].

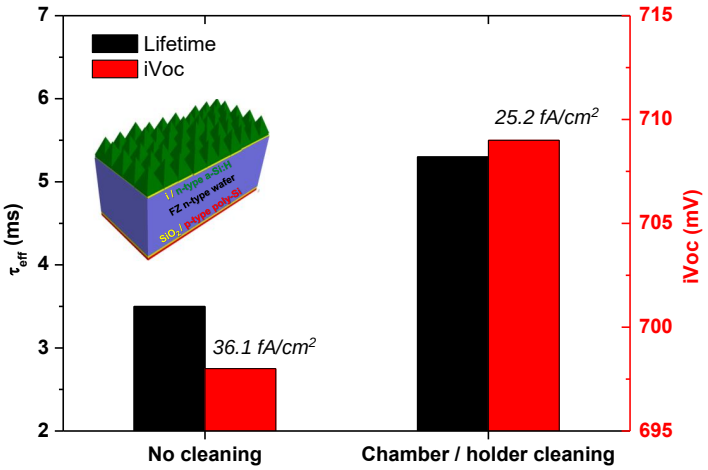


Figure 3.5: Lifetime ($\Delta=10^{15}$ cm^{-3}), iV_{OC} and J_0 measurements on precursor cells (7/6 nm i/n a-Si:H stacks as FSF) without/with chamber cleaning and holder deposition. Measured after 190 °C 30 min annealing on oven.

3.2.2 Effect of post-deposition annealing

Post-deposition annealing is an effective method to improve passivation quality of as-deposited samples with a-Si:H structures, which is considered to reform the structure stability and eliminate the dangling bonds in the structure [43], [64], [68]. Symmetric structures in Figure 3.3 (a) of 4.5/6 nm i/n a-Si:H layers were prepared on double-side textured c-Si wafers after ×1 NAOC cleaning. Passivation quality on three different annealing temperatures of 150 °C, 190 °C and 230 °C were investigated in 1 h annealing periods on oven.

Effect of annealing temperature and time

As revealed in Figure 3.6, post-deposition annealing highly improves passivation quality of i/n a-Si:H stacks compared to as-deposited samples at three different temperatures, no matter the annealing temperature is higher or lower the deposition temperature of 180 °C. This may be due to the hydrogen diffusion in the structure, especially into the a-Si:H/c-Si interface [64], [69], [70]. The annealing may activate diffusion of weakly bonded hydrogen and this dissociative hydrogen passivates the dangling bonds further at the interface and decreases the recombination. The temperature of 230 °C gives the best lifetime of 5.81 ms in 10 min short-period annealing. While if the annealing goes on further, passivation quality deteriorates quickly to 4.15 ms in 50 min, which is much lower than 5.39 ms lifetime measured in 190 °C annealing in the same period. This may relate to the high annealing temperature causes

hydrogen effusion from the heterointerface or amorphous silicon layers and generates more dangling bonds as defective recombination centers [64]. Passivation quality almost saturates for 150 °C and 190 °C annealing after 30 min with 3.6 ms and 5.3 ms respectively, which is good for saving more fabrication time. Moderate temperature may not pose threat on the passivation even for long annealing period because stable structure is already formed and not changed dramatically at this temperature point.

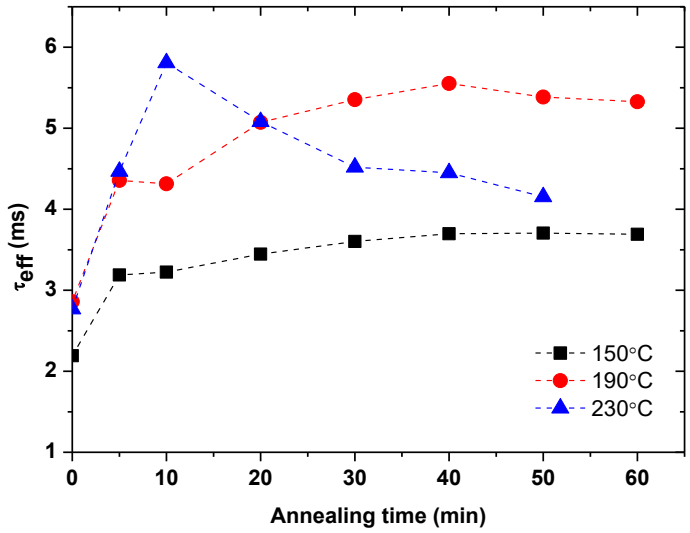


Figure 3.6: Lifetime at $\Delta=10^{15}$ cm^{-3} and implied-V_{OC} as the functions of post-deposition annealing time and temperature on symmetric structures with fixed 4.5/6 nm i/n layers. The annealing was carried out in air environment on oven.

Moreover, passivation stability after post-deposition annealing is of great importance to be investigated since after i/n a-Si:H deposition, the cells are far from finished. Typically, 48 more hours are required to finalize front TCO sputtering, photolithography, metallization and lift-off process, therefore possible degradation after i/n post-deposition annealing should be evaluated. As shown in Figure 3.7, highest lifetime values were obtained after post-deposition annealing with 5.56 ms for 190 °C and 5.80 ms for 230 °C. There is obvious passivation degradation after 48h for both annealing temperatures, which may relate to the hydrogen effusion during the cooling down stage after thermal annealing. However, higher temperature of 230 °C leads to even worse degradation which may be caused by unstable structure and weak Si-H bonds formed during post-deposition annealing. At the initial period within 10 min, hydrogen diffuses fast and passivates the dangling bonds, while due to high temperature, some hydrogen atoms stay active and may dissociate from the bonding state and increase the defect density. High

temperature causes this dynamic balance toward to 'desorption state' and large portion of dangling bonds are formed which deteriorates passivation quality. To obtain a well passivated surface after post-deposition annealing and following cooling down, 190 °C 30 min annealing was chosen as optimal treatment after i/n a-Si:H deposition.

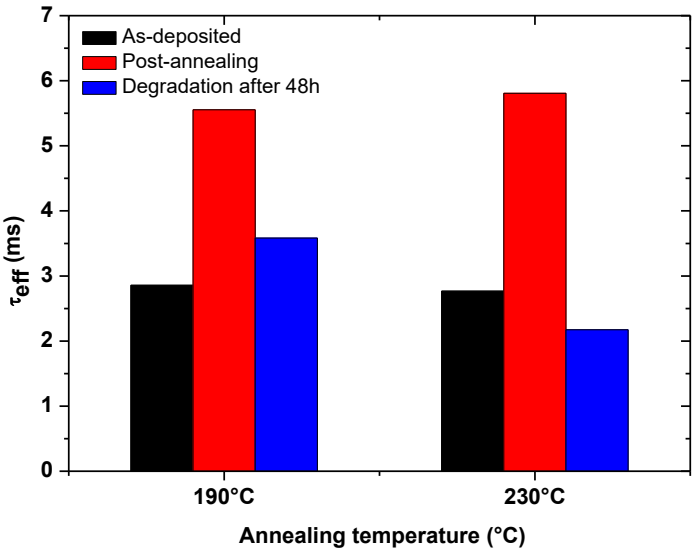


Figure 3.7: Lifetime at an injection level of $\Delta=10^{15}$ cm^{-3} on symmetric structures with 190 °C and 230 °C annealing temperatures at three different stages: as-deposited, post-deposition annealing and degradation after 48h.

Effect of annealing environment: Air or H_2 flow

Post-deposition annealing benefits passivation quality significantly in ambient air environment [52], which was also confirmed in aforementioned experiments. Considering hydrogen plays important role in chemical passivation, one question comes out:

- Does passivation quality improve further if H_2 flow is provided during post-deposition annealing process?

Two experiments were carried out on precursor cells with 3.5 nm i layer and 6 nm n layer as FSF via changing post-deposition annealing environment: one cell was annealed in 190 °C ambient air for 30 min on oven, the other was performed under 200 sccm H_2 flow for 30 min on 180 °C Amor chamber.

The results on precursor cells shows that H_2 flow annealing has better passivation quality which

improves the lifetime by 1.2 ms and reduce J_o dramatically by 12 fA/cm². This is due to more free hydrogen atoms are replenished and can penetrate easily into a-Si:H film or even a-Si:H/c-Si heterointerface to passivate the defects and reduce the defect density.

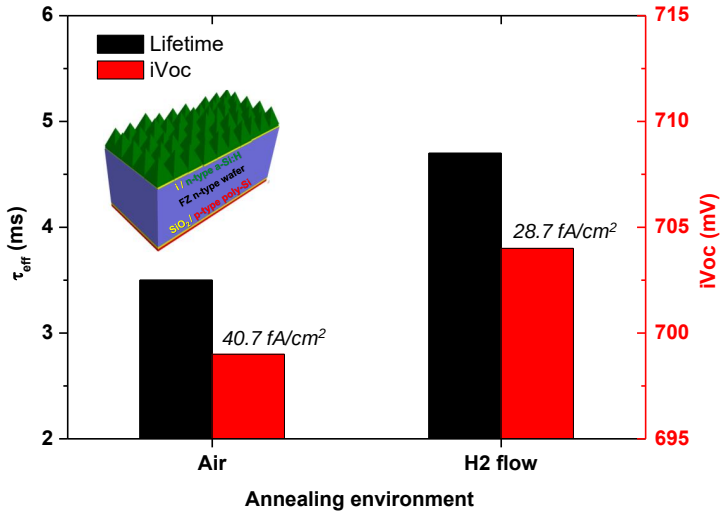


Figure 3.8: Lifetime ($\Delta=10^{15}$ cm^{-3}), iV_{OC} and J_o measurements on precursor cells (3.5/6 nm i/n stacks as FSF) in ambient air and H_2 annealing environment. Air annealing condition is 190 °C ambient air for 30 min on oven and H_2 annealing is 200 sccm H2 flow for 30 min on 180 °C Amor chamber.

3.2.3 Thickness optimization of i/n a-Si:H stacks

To investigate the effect of thickness of intrinsic and n-type a-Si:H, symmetric structures were used first due to the simple process and effective passivation indication for i/n a-Si:H stacks. Then the solar cells were fabricated to analyze the influence on opto-electrical properties.

Effect of n-type a-Si:H layer thickness

Since n-type a-Si:H induces effective band bending at the interface and provides field-effect passivation, it has a significant impact on the performance of solar cells. Under the deposition conditions described in Table 3.1, 40 sccm SiH_4 and 11 sccm PH_3 (2% in H_2 flow) as precursor gases for n-type a-Si:H growth, activation energy of 0.212 eV was obtained with 30 nm n-type a-Si:H layer capped with 300 nm Al film to provide effective conduction on glass sample. This activation energy value corresponds to the ideal reference values reported in other groups to form excellent n-type a-Si:H in terms of the carrier transport [52]. Therefore, the deposition

conditions were kept unchanged for n-type a-Si:H. Figure 3.6 reveals that 6 nm n-type a-Si:H shows excellent lifetime of 5.6 ms and implied-V_{OC} of 707 mV, which is at the same passivation level of 7 nm a-Si:H. The saturation of passivation quality indicates that it has no motivation for a thicker n-type a-Si:H than 6 nm.

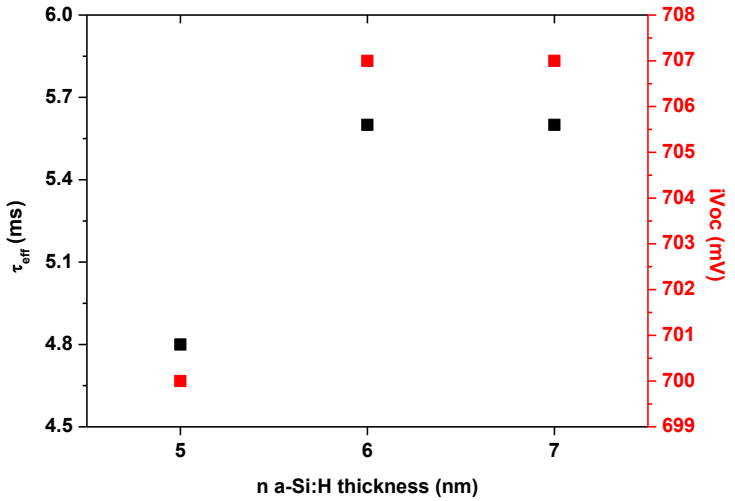
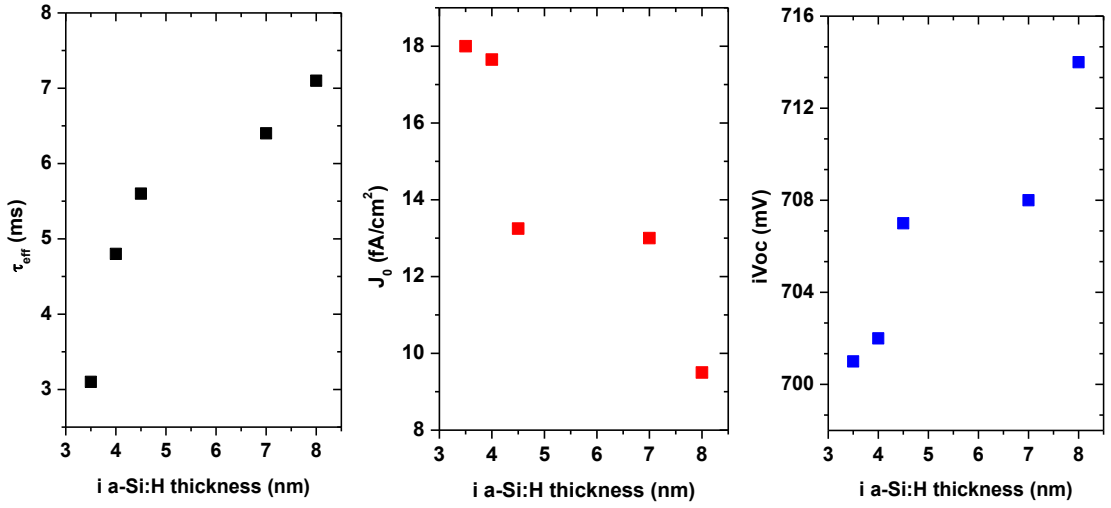


Figure 3.6: Effect of n-type a-Si:H thickness on lifetime ($\Delta=10^{15}$ cm^{-3}) and iV_{OC}. Measured on symmetric structures with fixed 4.5 nm i a-Si:H and different n a-Si:H thickness after 190 °C 30 min annealing on oven.

Effect of intrinsic a-Si:H layer thickness

Figure 3.7 presents the impact of different intrinsic a-Si:H thickness on main passivation indicators τ_{eff}, J_o and iV_{OC} of symmetric structures shown in Figure 3.3 (a). The lifetime and iV_{OC} both increase significantly and J_o decreases dramatically with a thicker i a-Si:H layer. The distinct change happens at the structure with 4.5 nm thick i a-Si:H. At 4 nm-thick intrinsic a-Si:H, J_o is still quite high of 17.65 fA/cm² while it dopes quickly to 13.25 fA/cm² at 4.5 nm thickness and almost keep the same level of 13 fA/cm² at 7 nm-thick i layer. The same trend was also revealed in implied-V_{OC} curve which shows 702 mV, 707 mV and 708 mV for 4 nm, 4.5 nm and 7 nm respectively. The reason of improving passivation can be explained that more dangling bonds are passivated at the interface and lower surface defect density with thicker i a-Si:H layer.



(a) (b) (c)

Figure 3.6: The effect of intrinsic a-Si:H thickness on: (a) minority carrier lifetime τ_{eff}($\Delta=10^{15}$ cm^{-3}); (b) saturation current density J_0 and (c) iV_{OC}. Measured on symmetric structures with a series of thickness of intrinsic a-Si:H: 3.5 nm, 4 nm, 4.5 nm, 7 nm and 8 nm, and fixed 6 nm n-type a-Si:H after 190 °C 30 min annealing on oven.

While there is a trade-off between parasitic absorption and passivation quality in terms of the thickness of intrinsic a-Si:H layer on hybrid solar cells. This contradiction was clearly indicated in Figure 3.7. J_{SC} is lower when the i a-Si:H layer becomes thicker, from 38.81 mA/cm^2 at 3.5 nm i layer to 37.49 mA/cm^2 at 7 nm. The reason may be attributed to more parasitic absorption caused by thicker i a-Si:H layer. When the light travels through the front nonactive layers, intrinsic a-Si:H layer will absorb the photons with higher energy than its bandgap of around 1.7 eV, or wavelength less than 730 nm according to Lambert-Beer law. While only 30% absorbed light in intrinsic layer contributes to J_{SC} [50], this causes parasitic absorption loss. As EQE curve shown in Figure 3.8, at the short wavelength especially less than 700 nm, the parasitic absorption loss increases with a thicker i layer.

On the other hand, V_{OC} improves dramatically from 689 mV to 711 mV with the increasing i layer thickness due to more effective chemical passivation. Moreover, intrinsic a-Si:H layer also influences the carrier transport and resistance, thus has an impact on *FF*. The highest FF of 73.0% was achieved when i a-Si:H is in the intermediate thickness of 4.5 nm. Neither thin nor thick i layer deteriorates the FF compared to 4.5 nm. Thicker intrinsic a-Si:H layer of 7 nm may reduce the electrons tunneling and hopping Probability that leads to a low FF value of 68.8%. If the intrinsic layer is too thin, a slight decrease of FF also can be obtained. Possible explanations are that: serious defect-rich layer is formed at the initial deposition layer mainly due to the unstable

plasma, which is even worse when intrinsic layer is too thin. It was reported that defective SiH_2 interface structure may lead to this degradation [71]; not effective passivation and high surface defect density at the c-Si surface caused by thinner i layer hinder the carrier transport thus lead to low FF.

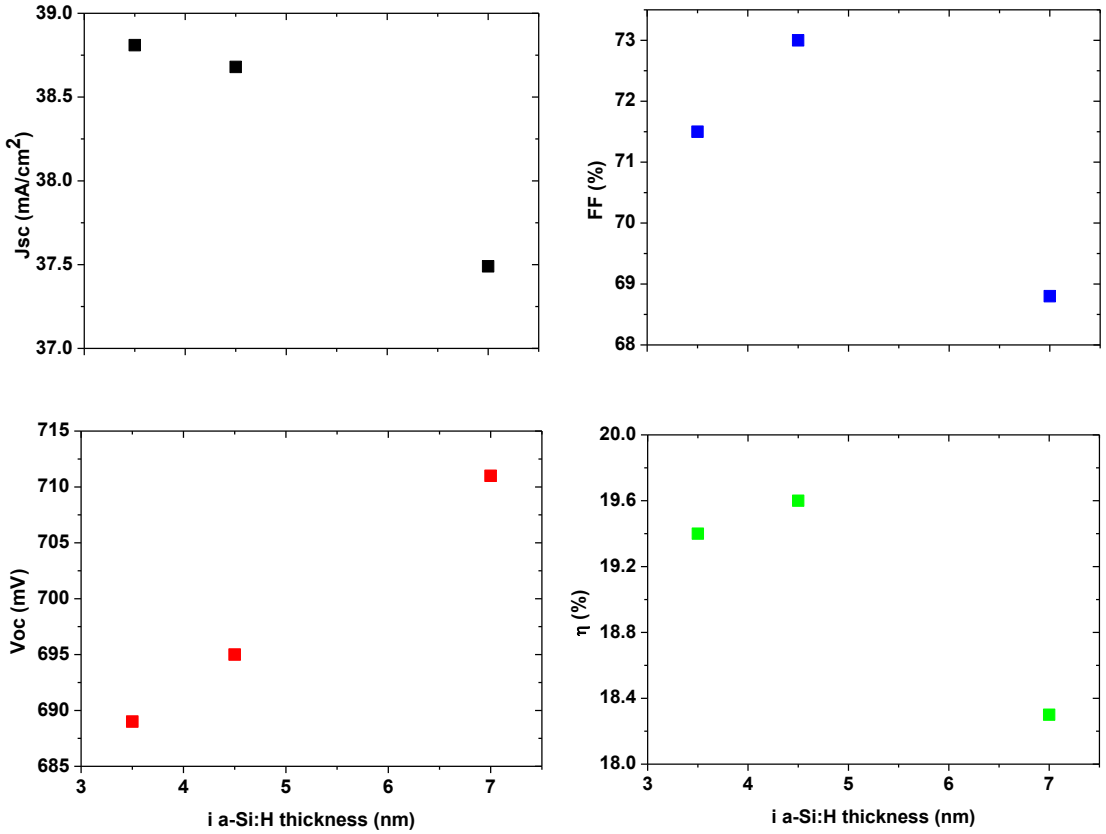


Figure 3.7: Characteristics of hybrid solar cells as a function of intrinsic a-Si:H thickness.

Since the rear side is fully covered by metal, there is no transmission (T) loss for hybrid solar cells. Therefore, 1-R curves show the absorption (A) in hybrid solar cells in Figure 3.8. As an indicator for reflection effect or texturing quality, average reflectance $R_{300\text{-}1200}$ is defined by

$$R_{300-1200} = \frac{\int_{300}^{1200} R(\lambda) d\lambda}{\int_{300}^{1200} d\lambda} \tag{3.1}$$

where R is the reflectance, λ is the wavelength. Average reflectance values are at the same level around 8.19% for three hybrid solar cells with different i layer thickness, which is smaller than the values obtained before in our lab [72], [73].

The loss between the 1-R and EQE refers to the recombination loss and parasitic absorption in Figure 3.8. At short wavelength, the main losses come from the parasitic absorption of front

TCO (IO:H and ITO stacks here) and i/n a-Si:H layers, and part is from the recombination losses. Therefore, a-Si:H/c-Si heterojunction structure has low spectral response in short wavelength range with the EQE value of approximately 0.2 in 300 nm wavelength. At visible wavelength, the recombination loss in c-Si absorber is the main loss mechanism, especially the surface recombination due to the unpassivated dangling bonds. The free carrier absorption (part of parasitic absorption) of rear poly-Si layer and metal contributes to the loss in the long wavelength, as well as recombination. Through quenching these losses, J_{SC} can be improved further. Comparing the three EQE curves in Figure 3.8, the short circuit current density shows a pronounced increment by decreasing the intrinsic a-Si:H thickness from 7 nm i layer to 3.5 nm i film.

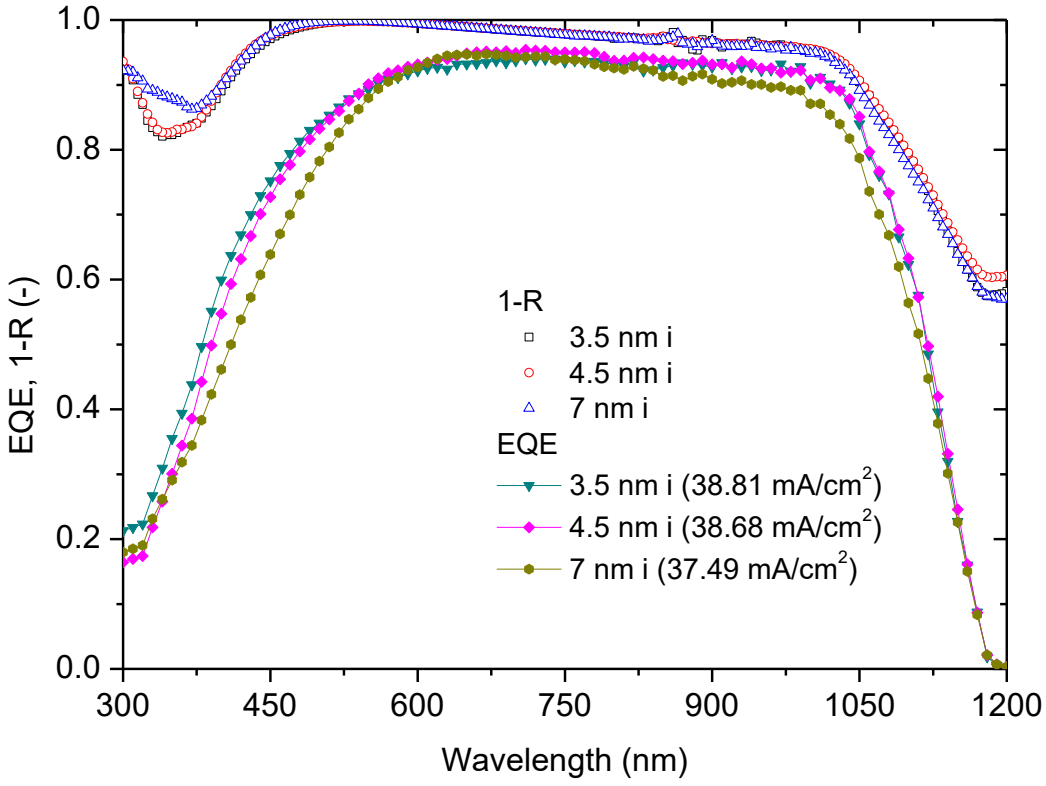


Figure 3.8: 1-R and EQE spectra of hybrid solar cells with different intrinsic a-Si:H thickness.

3.3 Conclusion

In this chapter, passivation quality on intrinsic ad n-type a-Si:H stacks were investigated and relative optimizations were carried out on the hybrid solar cells. First, effective surface cleaning is vital for c-Si/a-Si:H interface. With increasing NAOC cleaning times and plasma cleaning for chamber as well as substrate holder, the lifetime improves significantly. Besides, optimal post-deposition annealing condition of 190 °C 30 min in ambient air was developed. Too high post-deposition annealing temperature as 230 °C causes marked passivation degradation for more than 10 min annealing and after 48 h idle treatment, which may be caused by the formation of unstable structure and effusion of hydrogen from the interface. While low annealing temperature suppresses passivation potential and leads to lower lifetime and implied-V_{OC}. And H_2 flow post-deposition annealing on 180 °C Amor chamber for 30 min shows more appealing passivation performance which improves the lifetime up to 4.7 ms and mainly decreases the J_0 to 28.7 fA/cm² on precursor cell. Furthermore, the thickness of intrinsic a-Si:H has significant impact on passivation quality. Effective lifetime and implied-V_{OC} are strictly related to i a-Si:H thickness since intrinsic layer provides excellent chemical passivation and more dangling bonds are eliminated when thicker i a-Si:H is applied thus lower defect density. Meanwhile, as non-absorber layer, thicker i a-Si:H film has more parasitic absorption losses especially within 700 nm wavelength due to its approximately bandgap of 1.7 eV. There is a trade-off between V_{OC} and J_{SC} regarding the i a-Si:H layer thickness. Moreover, intrinsic layer influences the carrier transport thus *FF*. The hybrid solar cell with 4.5 nm i layer presented highest *FF* of 73%. Thicker i layer of 7 nm prevents the majority carrier electrons from tunneling and hopping into n-type layer which leads to lower *FF* of 68.8%. On the other hand, possible reasons for slightly lower *FF* of 71.5% in 3.5 nm intrinsic layer may be attributed to: (1) serious defect-rich interface is formed, such as defective SiH_2 layer mainly due to the unstable plasma at the initial deposition stage, which is even worse when i layer is too thin; (2) not effective passivation and high surface defect density lead to more recombination centers which hinder the effective carrier transport.

4

Influence of IO:H/ITO stacks on Hybrid Solar Cells

4.1 Introduction

In silicon heterojunction solar cells (SHJ), a-Si:H has a very poor lateral conductivity [18]. In order to suppress any issue with lateral transport of electrons in a-Si:H, a transparent conductive oxide (TCO) layer is usually deposited. The most important features of this layer are to ensure high conductivity to guarantee high FF, but also high transparency to minimize parasitic absorption losses. The commonly used TCO are n-type materials where defects such as oxygen vacancies and impurity behave as electron donors [74], which include Sn- or H-doped indium oxide and Al- or B-doped zinc oxide.

The resistivity ρ, of TCO materials depends on the charge carrier density N and the carrier mobility μ, shown in following Equation 4.1

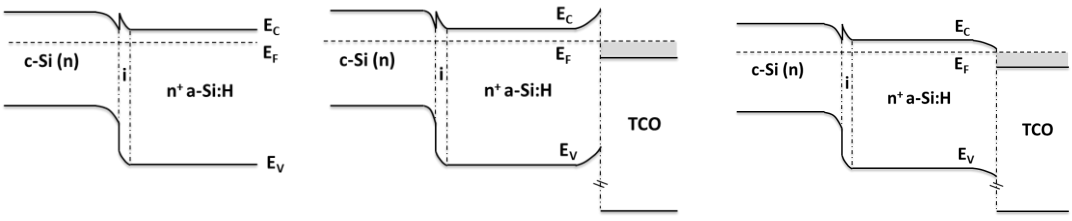
$$\rho = \frac{1}{\sigma} = \frac{1}{eN\mu} \tag{4.1}$$

where σ is the conductivity and e is the electronic charge (e = 1.602 × 10^{19} C). To obtain a highly conductive TCO material (ρ < 10^{-3} Ω·cm), high carrier density (N > 10^{19} cm^{-3}) and mobility (μ > 20 $cm^2 V^{-1} s^{-1}$) are required. While if carrier density increases to reduce the resistivity, the free carrier absorption (FCA) in the near infrared (NIR) region and reflection for incident light that has lower frequency than the plasma frequency increase relevantly, which lead to low transparency for TCO layer. The relation between carrier density N and plasma frequency ω_p is give

$$\omega_p^2 = \frac{Ne^2}{m\varepsilon_0} \tag{4.2}$$

where ω_p is plasma frequency, which refers to the natural frequency of oscillation of the electron gas; m is electron mass and ε_o is the vacuum permittivity. According to this equation, higher plasma frequency is obtained with higher carrier density of TCO, which will lead to higher reflection of incident light which has lower frequency than plasma frequency. Therefore, to balance the low resistivity (high *FF*) and high transparency (high J_{SC}), high mobility (typically > 100 $cm^2 V^{-1} s^{-1}$) offers the only way with moderate or low carrier density.

Solar cell performance depends on not only the properties of TCO layer itself, but also the interface between TCO and doped a-Si:H layer underneath or even metal. Typically sputtering technique is used for TCO deposition and it causes passivation degradation due to sputter-induced ion bombardment and ultraviolet emission from the plasma [75], [76]. Moreover, work function of n-type TCO layer strongly influences the carrier transport at the TCO/a-Si:H interface, and even the a-Si:H/c-Si interface when FSF layer is too thin. The performance of the solar cells, especially the V_{OC} and *FF*, can be influenced significantly [6], [77], [78]. The effect the TCO work function on the band alignment of TCO/a-Si:H (n/i)/c-Si structure is shown in Figure 4.1. TCO with too high work function not only induces lower built-in voltage of a-Si:H/c-Si structure but also forms Schottky barrier at the TCO/a-Si:H (n) interface, which blocks the effective carrier transport and induce the carrier recombination. Ideal TCO work function should be smaller than 4.5 eV to form ohmic contact for a-Si:H (n)/TCO structure according to the simulation.



(a) (b) (c)

Figure 4.1: Schematic band diagram illustrating the effect of TCO work function on band alignment at a-Si:H (n/i)/c-Si (n) structure: (a) without TCO; (b) TCO work function higher than a-Si:H (n); (c) TCO work fucntion lower than a-Si:H (n).

Indium tin oxide (ITO, Sn-doped In_2O_3) is the most used TCO material in silicon heterojunction solar cells due to its low resistivity of 10^{-3} – 10^{-4} Ω·cm [79], [80]. The relatively high carrier

density of $10^{20} – 10^{21}$ cm^{-3}, with rather low mobility of 20 – 40 $cm^2/(V·s)$, however, leads to high FCA and reflection in the NIR region [76], [80], [81]. Meanwhile, the parasitic absorption in near UV makes ITO less transparent due to its energy bandgap of around 4 eV [82]. Hydrogen-doped indium oxide (IO:H, hydrogenated indium oxide) is a quite attractive alternative for replacing ITO because of higher transparency and relatively low resistivity [30], [76], [83]. Typically, low resistivity of $(3 – 5) \times 10^{-4}$ Ω·cm was achieved with high mobility exceeding 100 $cm^2/(V·s)$ and low carrier concentration less than 2×10^{20} cm^{-3} on IO:H samples [30], [79], which reduces the absorption over the complete spectral range, especially in the near IR region [83]. Nevertheless, SHJ solar cells with IO:H perform worse than ITO mainly due to poor contact resistance with metal, which leads to 3% less FF or even more [79]. The specific contact resistivity for ITO/silver interface is approximately 10^{-3} $Ω·cm^2$, and often orders of magnitude higher for IO:H/silver interface of around several $Ω·cm^2$, which is also the case for other less conductive metals, such as copper and aluminum [79]. Therefore, bilayers of IO:H/ITO may be more attractive.

In this chapter, we developed IO:H/ITO stacks using IO:H to replace part of conventional ITO single layer to benefit the short circuit current. The effect of post-deposition annealing on electrical property of IO:H/ITO films were investigated to achieve high mobility and low resistivity. Then ITO single layer and IO:H/ITO bilayers, as two different TCO recipes, were studied and compared in terms of the opto-electrical properties on glass samples and then the performance on hybrid solar cells.

4.2 Opto-electrical properties of IO:H/ITO stacks

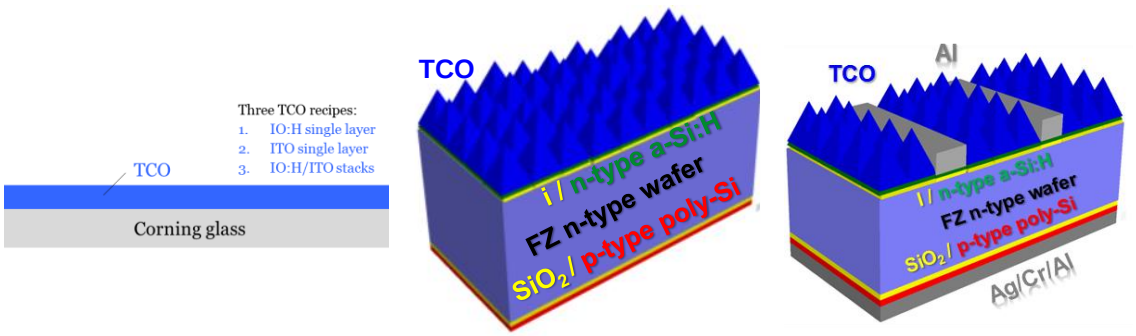
In this part, glass samples were prepared to investigate the opto-electrical properties of TCO films, and precursor cells were fabricated to monitor passivation quality step by step, especially the TCO sputtering and the recovery after post-deposition annealing. Finally, two hybrid solar cells were fabricated to compare the performance with ITO single layer and IO:H/ITO bilayers. Figure 4.2 presents three sample structures respectively: (a) three different kinds of TCO layers on XG corning glass; (2) precursor sample with TCO/a-Si:H (n/i)/c-Si/SiO_x/poly-Si (p) structure; (3) finished solar cell with metal contacts based on precursor cell structure.

To prepare the glass samples as illustrated in Figure 4.2 (a), 10 × 10 cm^2 XG corning glass was used and following steps were performed:

1. Chemical cleaning: 10 min acetone and subsequent 10 min isopropanol (IPA) immersion in ultrasonic bath to remove any organic contaminants on corning glass, then using nitrogen gun to dry;
2. TCO sputtering: load the glass substrates into Zorro chamber, and the sputtering process consists of heating up, target cleaning, deposition and ramping down steps. The detailed sputtering parameters were shown in Table 4.1 – 4.2.
3. Post-deposition annealing: Low temperature post-deposition annealing in air ambient or vacuum environment was used to recover from induced sputtering damage and crystallize the films.

For precursor and finished hybrid solar cells as demonstrated in Figure 4.2 (b) and (c), the fabrication steps were as follows:

1. Rear emitter formation: around 15 Å tunneling oxide was formed by wet-chemically cleaning and heavily-doped p-type poly-Si was grown by LPCVD, ion-implantation and following high-temperature thermal annealing;
2. Texturing and FSF deposition: 5% TMAH solution was used to texture front surface and then 4.5 nm intrinsic and 6 nm n-type a-Si:H were deposited by PECVD in Amor after ×3 NAOC cleaning. To improve passivation quality, H_2 flow post-deposition annealing was performed in 180 °C Amor chamber for 30 min. The detailed deposition conditions were shown in Table 3.1;
3. TCO sputtering and post-deposition annealing: 75 nm TCO was deposited on textured front surface by RF-sputtering in Zorro, and low-temperature post-deposition annealing was used;
4. Front and rear metal contacts: 6 μm Al was evaporated at front textured surface and 200 nm Ag – 30 nm Cr – 2 μm Al at planar rear side.



(a) (b) (c)

Figure 4.2: Schematic sample structures: (a) glass sample with TCO layers; (b) a precursor cell with TCO/a-Si:H (n/i) layers on front textured surface and SiO_x/poly-Si (p) films on rear flat surface; (c) a complete hybrid solar cell.

In order to reduce passivation degradation induced by ion bombardment during TCO sputtering, initial TCO sputtering power was chosen as low as possible after considering the plasma stability, which primarily only sacrifices the deposition rate. Therefore, 25 W initial sputtering power was chosen for IO:H deposition and 20 W initial power for ITO.

Table 4.1: Deposition conditions of 75 nm IO:H/ITO stacks on textured front surface[2]

	IO:H stacks		ITO
Thickness (nm)	10	55	10
$P_{deposition}$ (mbar)	5.7×10^{-3}	5.7×10^{-3}	1.2×10^{-2}
$P_{H2O,\ partial}$ (mbar)	3×10^{-5}	3×10^{-5}	-
$T_{substrate}$ (°C)	25	25	110
$P_{sputtering}$ (W)	25	135	200
Ar (sccm)	40	40	40

Table 4.2: Deposition conditions of 75 nm ITO single layer on textured front surface[3]

	ITO layer	
Thickness (nm)	10	65
$P_{deposition}$ (mbar)	1.2×10^{-2}	1.2×10^{-2}
$T_{substrate}$ (°C)	110	110
$P_{sputtering}$ (W)	20	200
Ar (sccm)	40	40

Table 4.3: Deposition conditions of 75 nm IO:H stacks on textured front surface

	IO:H
Thickness (nm)	75
$P_{deposition}$ (mbar)	5.7×10^{-3}
$P_{H2O,\ partial}$ (mbar)	3×10^{-5}
$T_{substrate}$ (°C)	25
$P_{sputtering}$ (W)	135
Ar (sccm)	40

[2] During IO:H/ITO stacks deposition, 25 W initial sputtering power was used for first 10 nm IO:H film to minimize sputtering damage, then the power jumped to 135 W for fast IO:H deposition of 55 nm. Finally, the samples were transferred to ITO chamber for last 10 nm ITO deposition at 200 W power.

[3] During ITO deposition, initial sputtering power of 20 W was used for first 10 nm thickness to minimize sputtering damage, then jumped to 200 W for next 65 nm.

4.2.1 Effect of post-deposition annealing on IO:H/ITO samples

To recover the TCO sputter-induced passivation degradation and crystallize IO:H film to improve the mobility and decrease the carrier density, post-deposition annealing after TCO sputtering is a mandatory step. Based on previous experiments, it was found that passivation quality deteriorates dramatically if IO:H/ITO stacks are annealed together after deposition. The lifetime declines from 4.86 ms to 3.46 ms and implied-V_{OC} drops from 715 mV to 703 mV on symmetric TCO/a-Si:H (n/i)/c-Si/ a-Si:H (i/n)/TCO structure samples before and after 190 °C 30min post-deposition annealing in oven. Therefore, after IO:H deposition, the samples were transferred to vacuum environment for post-deposition annealing treatment to achieve crystallization of IO:H film. Afterwards, ITO film was sputtered onto the IO:H layer without any further post-deposition annealing to prevent passivation degradation when annealed together. The process flowchart of glass samples as depicted in Figure 4.2 (a) is shown in Figure 4.3. The relative layers thickness for IO:H/ITO stacks are based on the layers thickness on random textured silicon surface multiplying by a theoretical geometric factor of 1.73 [50], [84], which means the thicknesses for 20 W-sputtered IO:H film, 135 W-deposited IO:H layer and 200 W-sputtered ITO are 17 nm, 95 nm and 17 nm respectively on glass samples.

Figure 4.3: Flowchart of glass samples with 129 nm IO:H/ITO stacks. The ratio of the IO:H (20 W)/IO:H (135 W)/ITO (200 W) layers thickness is 1 : 5.5 : 1, the same ratio as on the textured surface.

To optimize post-deposition annealing temperature on IO:H films, 129 nm IO:H bilayers were deposited on glass substrates first, then the samples were transferred to vacuum environment in Amor chamber for different temperature post-deposition annealing for 30 min, afterwards, the last 17 nm ITO films was deposited on top of IO:H films. The electrical properties of mobility, carrier density and resistivity were chosen as main indicators for more transparent (low carrier density) and highly conductive (low resistivity and high mobility) TCO films, as illustrated in Figure 4.4. The sample at 170 °C post-deposition annealing presented lowest resistivity of 4.89×10^{-4} Ω·cm and sheet resistance of 35.82 Ω/□, which, however, mainly stem from highest carrier density of 1.55×10^{20} cm^{-3}. As the annealing temperature rises after 170 °C, the resistivity of IO:H/ITO stacks increases. 180 °C annealed sample showed optimal performance with high

mobility of 117.4 $cm^2/(V \cdot s)$ and low carrier density of 1.07×10^{20} cm^{-3}. Compared to the as-deposited samples without annealing, the mobility of annealed samples is almost doubled and carrier density declines to the half, which increase the resistivity of films slightly. The high mobility is mainly realized by solid-phase crystallization of amorphous IO:H films deposited at room temperature after the post-deposition annealing [30], [83].

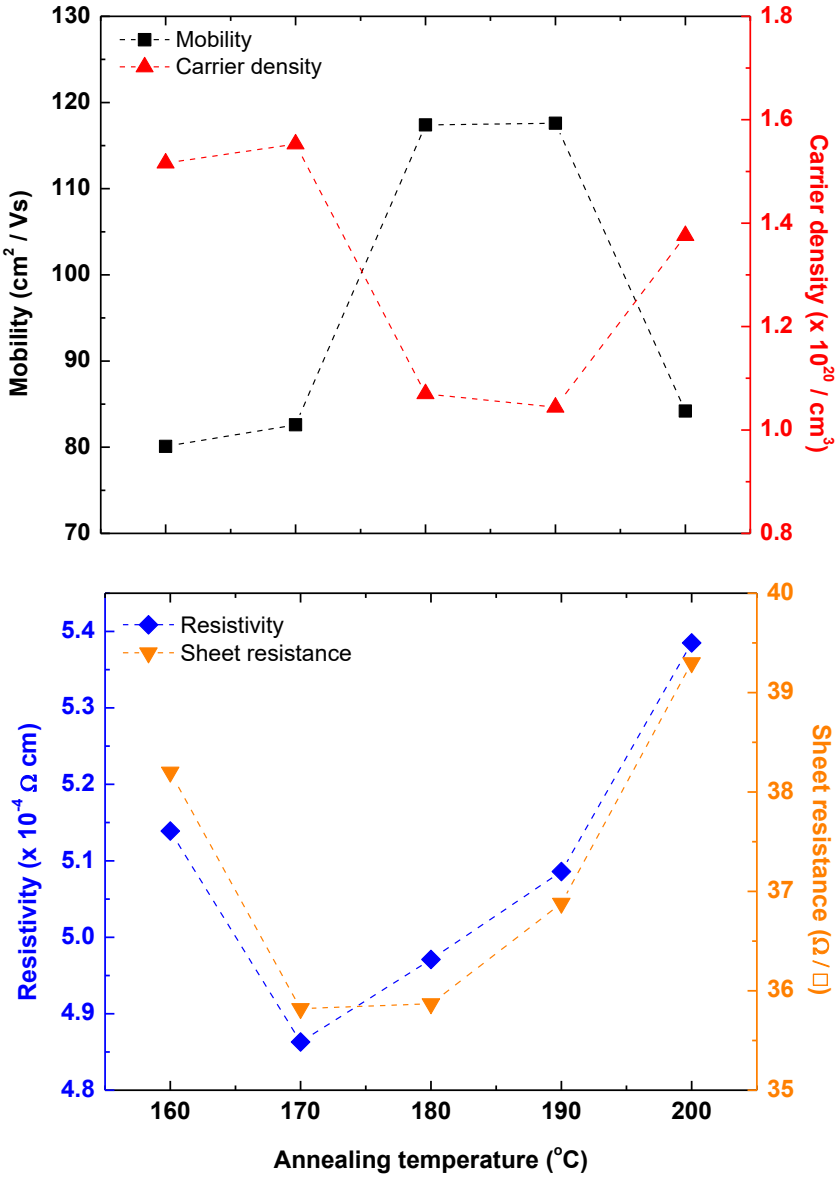


Figure 4.4: Mobility, carrier density, resistivity and sheet resistance of 129 nm IO:H/ITO samples on corning glass as a function of post-deposition annealing temperature for IO:H films in vacuum. The reference values of as-deposited IO:H/ITO samples without post-deposition annealing were measured: μ = 60.24 $cm^2/(V \cdot s)$, N = 2.46×10^{20} cm^{-3}, ρ = 4.2×10^{-4} $\Omega \cdot cm$ and R_{sheet} = 39.8 $\Omega/\square$.

4.2.2 Comparison between ITO layer and IO:H/ITO stacks

In order to deeply investigate how TCO influences the solar cells performance, the electrical properties and optical properties of three different TCO types: ITO, IO:H/ITO and IO:H were investigated. Three different TCO layers with 129 nm thickness were sputtered on glass substrates respectively with the deposition recipes shown in Table 4.1 – 4.3. The 129 nm-thick ITO sample, which consists of 17 nm ITO film sputtered at 20 W power capped with 112 nm ITO deposited at 200 W power, was annealed at 190 °C in air for 30 min. And for IO:H/ITO samples, 25 W sputtering power was used for first 17 nm IO:H and next 95 nm IO:H was deposited at 135 W high power. Then 30 min post-deposition annealing at 180 °C in vacuum was used for IO:H films. Finally, last 17 nm ITO was sputtered at 200 W without any post-deposition annealing. The process for IO:H single layer was much easier that only 135 W high power was used to deposit 129 nm IO:H and then the sample was annealed at 180 °C in vacuum for 30 min.
The electrical properties of ITO, IO:H/ITO and IO:H were shown in Table 4.4. The mobility μ, carrier density N and resistivity ρ were measure by Hall effect, and sheet resistance R_{sheet} was obtained from four-point probe. The contact resistivity $\rho_{contact}$ was measured by transmission line model (TLM) based on hybrid solar cell structure, which mainly comes from TCO/front metal (aluminum) interface. Since TCO layer is conductive enough so that the measurement current mostly flows from contact metal into TCO layer and then flows back to front metal.

Table 4.4: Electrical properties of ITO, IO:H/ITO and IO:H

		μ ($cm^2\,V^{-1}\,s^{-1}$)	N ($\times 10^{20}\,cm^{-3}$)	ρ ($\times 10^{-4}\,\Omega\cdot cm$)	R_{sheet} ($\Omega/\square$)	$\rho_{contact}$ ($\times 10^{-2}\,\Omega\cdot cm^2$)
ITO	As-deposited	28.2	1.27	17.42	109.4	-
	Annealed	24.5	2.01	12.71	92.5	2.88
IO:H/ITO	As-deposited	60.2	2.46	4.20	39.8	-
	Annealed	117.4	1.06	4.92	35.8	2.51
IO:H	As-deposited	60.7	2.37	4.35	30.6	-
	Annealed	90.7	1.48	4.65	33.1	-

The mobility in IO:H films is rather higher than ITO which is realized by H_2O vapor introduced during IO:H deposition. Water vapor during sputtering acts as a source of hydrogen donors, which improves intra- and inter-grain properties remarkably [30]. Besides, water vapor induces an amorphous structure rather than polycrystalline one, which can be transformed into crystalline after post-deposition annealing [30], [79]. Post-deposition annealing is of great importance to achieve low carrier density and high mobility for IO:H films due to the solid-phase crystallization of amorphous IO:H films deposited at room temperature [30]. The

highest mobility was presented in IO:H/ITO sample after post-deposition annealing together with lowest carrier density. Moreover, ITO presents the highest resistivity mainly due to the lowest mobility of approximately four times lower than IO:H films. An issue that might affect performance in terms of series resistance in the solar cells is that the contact resistance between either ITO or IO:H/ITO stacks and aluminum interface is one order magnitude higher than the reference values of around $2 \times 10^{-3}\ \Omega \cdot cm^2$ [79].

The optical properties of ITO, IO:H/ITO and IO:H are shown in Figure 4.5. The absorbance has been calculated by 1-R-T, where R and T are reflectance and transmittance respectively measured by spectrophotometer. The absorbance of IO:H film is lower than that of ITO over the complete spectral range, especially in the UV-visible region. The absorption is rather less in NIR region for all three samples and the absorbance difference between IO:H and ITO film is less pronounced in these wavelength, which is slightly different from the results reported in other groups [30], [79], [83]. This less absorbance in NIR region indicates high-quality ITO and IO:H films were developed.

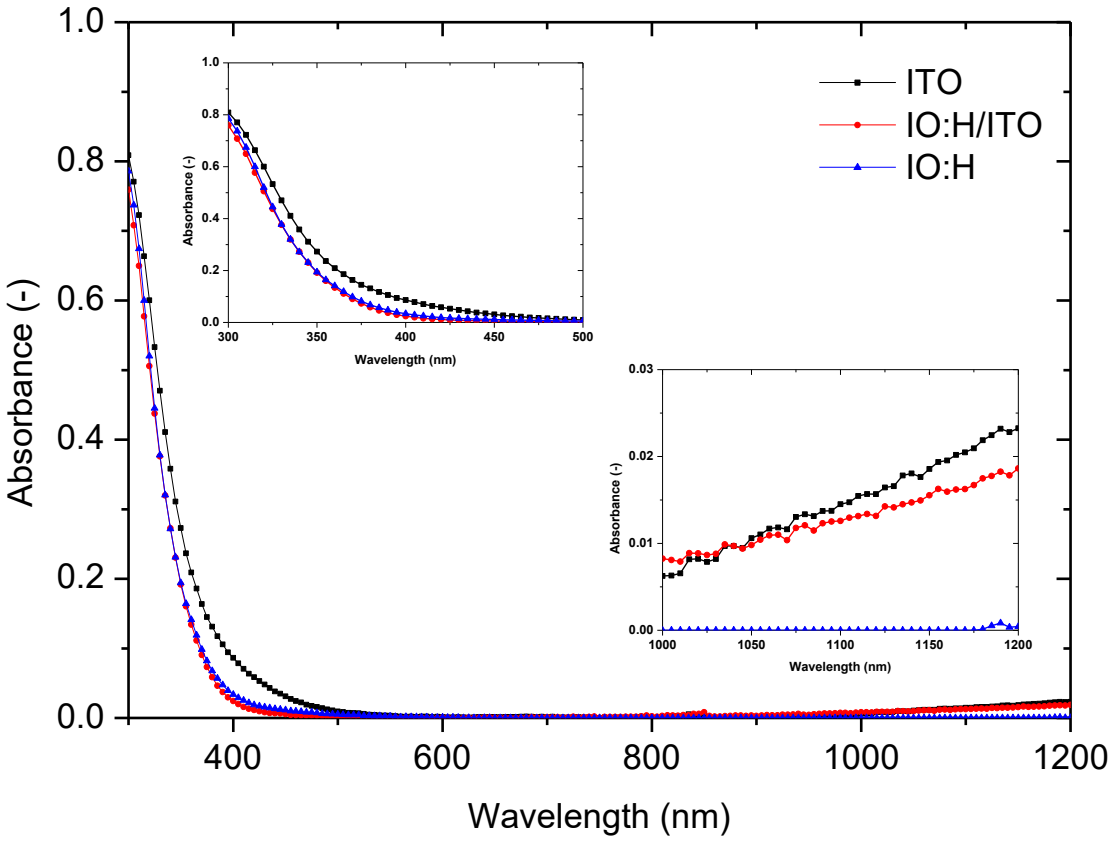
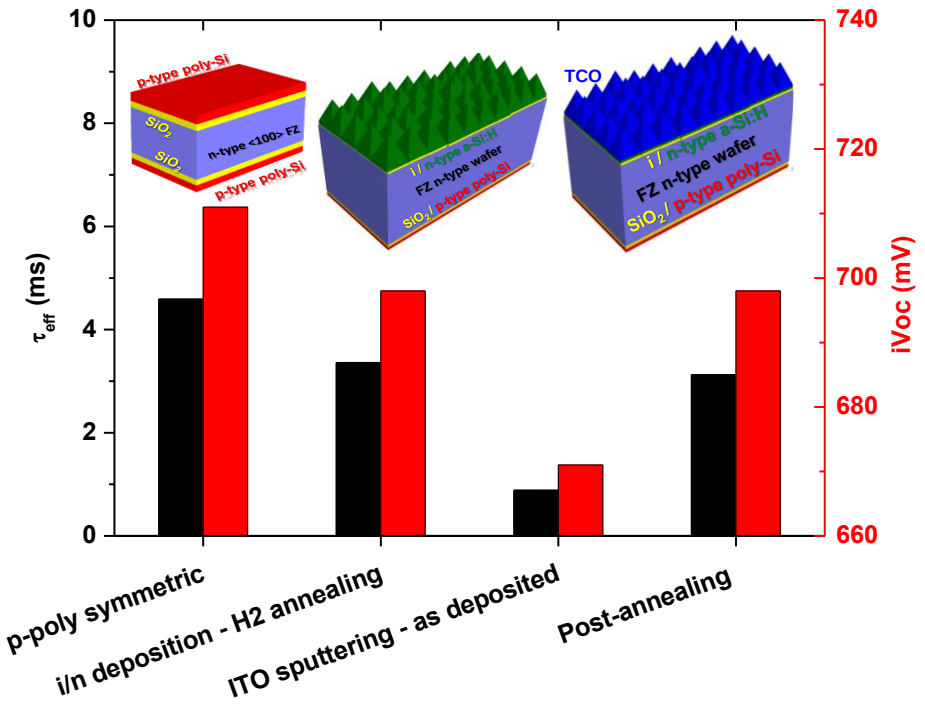


Figure 4.5: Absorption spectra for ITO (annealed 30 min @ 190 °C in air), IO:H/ITO stacks (IO:H film annealed 30 min @ 180 °C in vacuum) and IO:H (annealed 30 min @ 180 °C in vacuum), calculated by 1-R-T. Insets are presented in the plot to highlight the short-wavelength and NIR part os the sprctrum. IO:H was used as a reference.

(a)



(b)

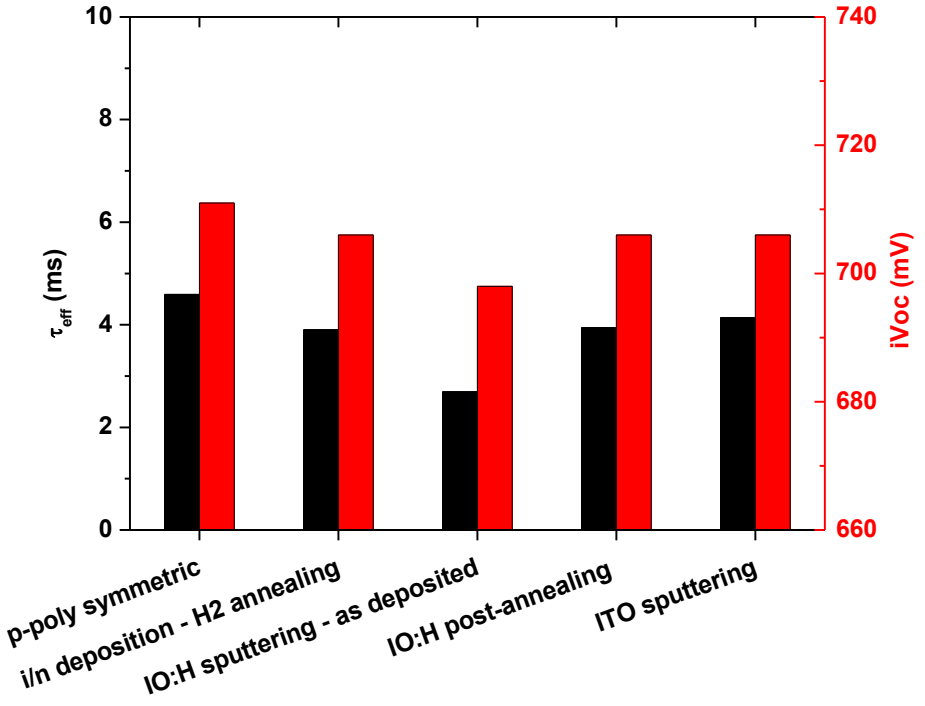


Figure 4.6: Lifetime at $\Delta=10^{15}$ cm^{-3} and iV_{OC} for different process steps during precursor cells fabrication: (a) cell #1 with ITO; (b) cell #2 with IO:H/ITO stacks. Measured in Sinton lifetime tester. Optical constant values were set as 0.7/0.8 for the structures without/with TCO respectively.

It is of significant importance for monitoring passivation quality for every-step process, as shown in Figure 4.6. Damage by TCO sputtering on a-Si:H has been observed on both cell precursors with ITO and IO:H/ITO. Considerable passivation degradation was measured in precursor cell after ITO sputtering. High lifetime of 3.36 ms and iV_{OC} of 698 mV was obtained for precursor cell after i/n deposition and H_2 flow annealing. While after ITO sputtering, a severe decline of 74% in lifetime and a drop of 27 mV in iV_{OC} were observed. This passivation degradation can be mostly recovered by post-deposition annealing after ITO deposition. In literature, permanent microscopic changes have been observed in the a-Si:H network involving Si-H bonds after TCO sputtering and subsequent annealing, which indicates passivation quality may not be directly affected by microstructure of a-Si:H films [75]. This sputter-induced damage is merely pronounced after IO:H sputtering which may be partly due to the gentle room temperature sputtering or IO:H material itself. The post-deposition annealing after IO:H deposition can recover passivation quality and crystallize the IO:H film to reduce the carrier density and improve the mobility. The last 10 nm ITO deposited on textured IO:H layer improves the lifetime further to 4.14 ms, which is slightly higher than that after i/n a-Si:H deposition annealed in H_2 flow. As the sample experienced an extra annealing at 110 °C during the ITO deposition which improves passivation quality further.

With proceeding the precursor cells further, 6 μm Al was evaporated on the front textured surface and 200 nm Ag – 30 nm Cr – 2 μm Al was used as rear metal contacts on two hybrid solar cells #1 and #2 aforementioned. The performance results were shown in Table 4.5 and 1-R/EQE spectra was presented in Figure 4.7.

Table 4.5: Results of hybrid solar cells with two different TCO

Devices	V_{OC} (mV)	J_{SC} (mA/cm²)	R_s (Ω cm²)	R_{sh} (Ω m²)	FF (%)	η (%)	pFF (%)
Cell #1 with ITO	704	39.5	1.84	1.80	73.8	20.5	81
Cell #2 with IO:H/ITO	707	39.7	2.61	0.91	72.0	20.2	81

A subtle difference of V_{OC} between the cell with ITO and cell with IO:H/ITO comes from the process after i/n a-Si:H deposition as shown in Figure 4.6 (a) and (b). Passivation degradation was mostly recovered by post-deposition annealing after TCO sputtering for both cells. There is a slight improvement of J_{SC} for the cell #2 since IO:H layer, as an alternative for 65 nm ITO, has less pronounced parasitic absorption in UV-visible spectra and free carrier absorption in NIR region, which is shown in Figure 4.7. The blue curve stands for the EQE spectra for the cell with

IO:H/ITO and the green curve is for the cell with ITO. In short wavelength region, cell #2 collects better than #1 because of more transparent IO:H/ITO stacks. A negligible gap between the 1-R and EQE was presented in the range from 750 nm to 1000 nm at the cell with ITO yet both 1-R curves are overlapped at the most wavelength ranges. This means the recombination is quenched dramatically which may be achieved by good-quality texturing process (homogeneous pyramid size and shape) and passivation to eliminate the dangling bonds in the c-Si surface. Moreover, a slightly higher *FF* was obtained at the cell with ITO due to the lower series resistance and higher shunt resistance. This decrease of series resistance in #1 is not from the TCO layer since ITO (in cell #1) has higher resistivity and higher contact resistivity at the ITO/aluminum interface compared to IO:H/ITO stacks (in cell #2), as shown in Table 4.4. Therefore, other experimental processes before the TCO sputtering or the difference of the c-Si bulks may lead to the *FF* increase.

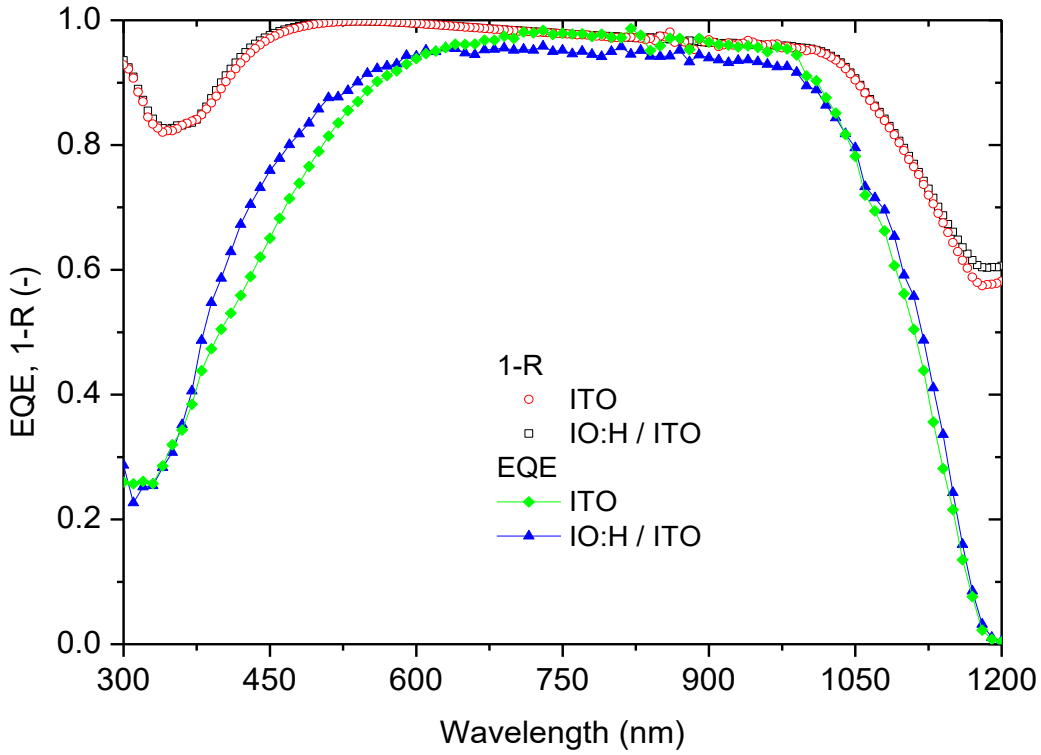


Figure 4.7: 1-R and EQE spectra of hybrid solar cells with two different TCO layers: ITO single layer with lower J_{SC} of 38.64 mA/cm²; IO:H/ITO stacks with slightly higher J_{SC} of 38.96 mA/cm².

4.3 Conclusion

In this chapter, IO:H capped with top ITO stacks, as an attractive alternative to replace conventional ITO single layer, were developed to benefit the J_{SC} while still maintain the *FF*. The post-deposition annealing temperature after IO:H deposition was first optimized in terms of the electrical properties. High mobility of 117.4 $cm^2/(V \cdot s)$ and low carrier density of 1.07×10^{20} cm^{-3} on glass sample with IO:H/ITO stacks have been measured after 180 °C annealing in vacuum for 30 min. Then, the opto-electrical properties of ITO, IO:H/ITO and IO:H films were compared. Either IO:H/ITO stacks or IO:H single layer shows nearly 4 times higher mobility after post-deposition annealing compared to ITO film, which is realized by H_2O vapor introduced during deposition and solid-phase crystallization after post-deposition annealing, thus leading to lower resistivity. After the annealing, the carrier density decreases to the half on IO:H/ITO stacks and IO:H layer compared to nearly doubled on ITO film which shows more optical absorption in the UV-visible region. The TCO sputtering ion bombardment induces damage to a-Si network and causes passivation degradation, which is significantly severe after ITO deposition. A distinct decline of 74% in lifetime and 27 mV in iV_{OC} has been observed after ITO deposition for the solar cell precursor with ITO layer. This passivation degradation is less pronounced after IO:H deposition which may be due to the gentle room temperature deposition. Post-deposition annealing can nearly fully recover passivation degradation for both samples. With proceeding the precursor cells further, two hybrid solar cells were fabricated with IO:H/ITO stacks and ITO single layer. Open circuit voltage is close between two solar cells (704 mV for cell #1 and 707 mV for cell #2). A slight improvement of J_{SC} was obtained in the cell with IO:H/ITO stacks since IO:H layer, as an alternative for 65 nm ITO, has less pronounced parasitic absorption in UV-visible and NIR region. However, the cell with ITO shows excellent spectral response in the visible-NIR range from 640 nm to 1030 nm where the recombination is of rare significance. This may be achieved by good-quality texturing process and passivation to eliminate the dangling bonds at c-Si surface. Furthermore, a slightly higher FF was obtained at the cell with ITO due to the lower series resistance and higher shunt resistance which mainly comes from other process steps. Finally, the highest conversion efficiency of 20.5% was obtained with V_{OC} of 704 mV, J_{SC} of 39.5 mA/cm^2 and *FF* of 73.8% on the cell with ITO.

5

Conclusions and Outlook

5.1 Conclusions

This project aimed at improving SHJ/poly-Si passivating contact hybrid solar cells performance by means of optimizing front surface field of i/n a-Si:H stacks and front TCO layer, including passivation quality improvement of i/n a-Si:H stacks, trade-off between J_{SC} and V_{OC} with different thickness of i a-Si:H layer, comparison between IO:H/ITO stacks and ITO single layer in terms of opto-electrical properties and effect on hybrid solar cells performance.

It was found that effective surface cleaning pretreatment is crucial for obtaining high passivation quality of i/n a-Si:H layers prior to PECVD deposition. With increasing wet cleaning cycle of NAOC, the effective lifetime τ_{eff} improves significantly from 2.1 ms for ×1 NAOC to 12.6 ms for ×3 NAOC. To avoid cross-contamination deteriorating surface passivation, plasma cleaning of chamber and plasma deposition on substrate holder were developed that a decrease of saturation current density J_o of 10.9 fA/cm^2 was obtained.

The passivation quality of i/n a-Si:H stacks benefits from post-deposition annealing. Optimal post-deposition annealing condition of 190 °C 30 min in ambient air has been developed. Annealing at high temperature of 230 °C is not recommended, since lifetime measurement shows that pronounced passivation degradation of 3.6 ms drop was observed after 48 h idle treatment. While low annealing temperature of 150 °C suppresses passivation potential, leading to lower lifetime. Compared to air annealing, H_2 environment post-deposition annealing shows more appealing passivation performance which improves lifetime to 4.7 ms and decreases J_o to

28.7 fA/cm^2 on solar cell precursors.

The influence of front intrinsic a-Si:H passivating layer thickness has been investigated. Effective lifetime and iV_{OC} measured on symmetric structures are strictly related to i a-Si:H thickness since thicker intrinsic layer provides excellent chemical passivation and reduces more defect density. Meanwhile, as non-absorber layer, thicker i a-Si:H leads to more parasitic absorption loss, especially within 700 nm wavelength due to its approximately bandgap of 1.7 eV. There is a trade-off between V_{OC} and J_{SC} regarding i a-Si:H layer thickness. Furthermore, intrinsic layer affects the carrier transport thus *FF*. Hybrid solar cell with 4.5 nm i layer presents highest *FF* of 73.0%, while thicker i layer of 7 nm prohibits the majority carrier electrons from tunneling and hopping into n-type layer which leads to lower *FF* of 68.8%. Moreover, slightly lower *FF* of 71.5% was obtained on hybrid solar cell with 3.5 nm i layer, which may be caused by: (i) serious defect-rich SiH_2 layer is formed due to the unstable plasma at the initial deposition, which is even worse when intrinsic a-Si:H layer is thin; (ii) not effective passivation and high surface defect density lead to more recombination centers which inhibit the effective carrier transport.

IO:H/ITO stacks, as an attractive alternative to replace conventional single ITO layer, have been developed to quench parasitic absorption of TCO layer thus improving J_{SC}. Hall effect measurement on glass samples has shown that post-deposition annealing in vacuum is an effective method to decrease carrier density and increase mobility of IO:H/ITO stacks. 180 °C annealed sample showed optimal performance with high mobility of 117 cm^2/(V·s) and low carrier density of 1.07×10^{20} cm^{-3}.

The opto-electrical properties of IO:H/ITO stacks, ITO single layer and IO:H single layer were compared on glass sample. Either IO:H/ITO stacks or IO:H single layer shows nearly 4 times higher mobility and half carrier density after post-deposition annealing compared to ITO single film, which lead to much lower resistivity of IO:H-related films. Absorption spectra illustrate that the optical absorption of IO:H/ITO stacks is lower than that of ITO film over the complete spectral range, especially in the UV-visible region. In terms of the passivation quality, TCO sputtering ion bombardment induces damage to a-Si network and causes passivation degradation, which is significantly severe for ITO deposition. A distinct decline of 74% in lifetime and 27 mV in iV_{OC} were observed after ITO deposition. This passivation degradation is less pronounced for IO:H deposition which may be due to the gentle room temperature deposition. However, post-deposition annealing can nearly fully recover passivation degradation for both sputtering.

Two hybrid solar cells were fabricated with IO:H/ITO stacks and ITO single layer. Open circuit

voltage is close between two solar cells after the post-deposition annealing treatment. A slight improvement of J_{SC} was measured in the cell with IO:H/ITO stacks which is due to the less parasitic absorption in UV-visible region for IO:H layer. While in the visible range, the cell with ITO has higher EQE due to less recombination. Moreover, owing to low series resistance and high shunt resistance, the cell with ITO layer shows a slightly higher *FF*. This increment of *FF* is not caused by TCO layer since ITO single layer has higher electrical resistivity as well as higher contact resistivity at the TCO/aluminum interface. The highest conversion efficiency of 20.5% was achieved on 9 cm² hybrid solar cell with V_{OC} of 704 mV, J_{SC} of 39.5 mA/cm² and *FF* of 73.8%.

5.2 Outlook

Yoshikawa et al [33] calculated the theoretical efficiency limit for a single-junction c-Si solar cell in 2017 considering recombination, optical and resistance losses in a real solar cell. The theoretical limit of 29.1% is calculated based on a c-Si wafer with the thickness of 165 μm and resistivity of 3 Ω·cm² (V_{OC} = 752 mV, J_{SC} = 43.7 mA/cm² and *FF* = 88.5%). Compared SHJ/poly-Si passivating contact hybrid solar cell with the optimal cell, the losses of 16.6% in *FF*, 11.7% in J_{SC} and 6.4% in V_{OC} are observed respectively. To quench these losses, following feasible improvements can be used.

5.2.1 Fill factor boost

(1) Screen-printing and copper electroplating metallization techniques

Front and rear metal contacts are of great significance for solar cell performance since they contribute to the series resistance and cause the front metal shading. Typically, high conductivity and high height-to-width aspect ratio are two rules for front metal design. The highest *FF* of 73.8% was obtained from evaporation on hybrid solar cells, which is limited by the thickness and conductivity of front aluminum. Silver-paste screen-printing and copper electroplating techniques are two promising alternatives for replacing aluminum evaporation to decrease the metal resistance due to high conductivity of Ag and Cu and thicker metal fingers (> 20 μm) [27], [32]. High *FF* of more than 80% can be obtained after optimization. Besides, Papakonstantinou [85] has successfully applied screen-printing technology to SHJ solar cell fabrication in our group before, which improve *FF* to 78.8% compared to 73.6% obtained from evaporation.

(2) Replacing ITO layer with low work function AZO film

The work function of TCO (W_{TCO}) layer plays a crucial role on the solar cell performance since it influences the carrier transport at the TCO/FSF interface and the total built-in potential of the device [77], [78]. To form a low Schottky barrier contact or even ohmic contact for TCO/a-Si:H (n) contact, the optimal W_{TCO} should be less than 4.5 eV according to our simulation. With the decrease of W_{TCO}, Schottky barrier decreases and the electrons transport much easier, eventually resulting in higher *FF*. Since the work function of ITO is slightly higher which varies from 4.3 eV to 5.1 eV from the literature [86], [87], a lower work function TCO layer is preferred. It was reported that aluminum-doped zinc oxide (AZO) has lower work function in the range of 3.7 – 4.7 eV [88]–[90], which is more promising for replacing ITO layer. However, the disadvantage of AZO film is low carrier mobility of 15 $cm^2/(V{\cdot}s)$ and high carrier concentration of 4.3×10^{20} cm^{-3}, which result in high parasitic absorption, thus low J_{SC} [91].

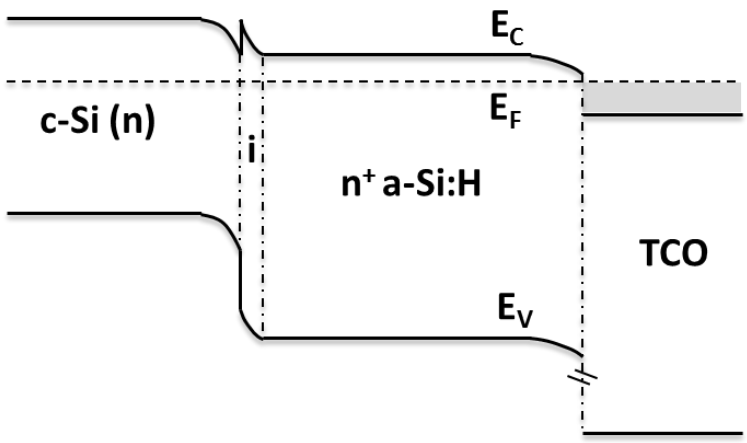


Figure 5.1: Schematic band diagram of c-Si (n)/a-Si:H (i/n)/TCO structure with W_{TCO} lower than n-type a-Si:H.

5.2.2 Current increase

(1) Decrease external reflection: double-layer ARC or black silicon

Reflectance measurement shows there is considerable external reflection of average reflectance of 8.19% on hybrid solar cells, which limits J_{SC} to a higher level. Further optimization should be carried out to decrease external reflection. During this thesis, double-layer antireflection coating design has been tested. According to the simulation from PV Lighthouse, 40 nm ITO capped with 90 nm SiO_2 design was chosen based on the refractive index analysis and reflection

simulation. Then double-layer ARC and conventional single ARC of 55 nm IO:H capped with 10 nm ITO were deposited on front surface of textured wafers. The results show double-layer ARC can decrease the average reflectance to 5.4% compared to 7.1% on IO:H/ITO single-layer ARC design. Moreover, thinner TCO layer (40 nm ITO) is used on double-layer ARC design which decreases the parasitic absorption of TCO thus higher J_{SC}.

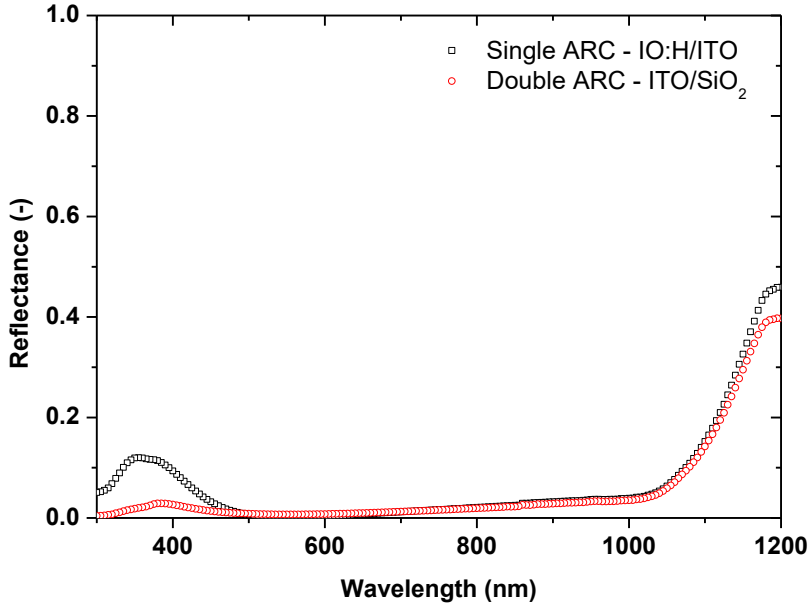


Figure 5.2: The measured reflectance spectra on textured wafers with single-layer ARC (65 nm IO:H/10 nm ITO) and double-layer ARC (40 nm ITO/90 nm SiO_2).

Besides, black silicon project is under investigation in our group, which is a promising approach to eliminate front surface reflection, especially in the visible wavelength [92].

(2) Decrease parasitic absorption

The disadvantage of applying a-Si:H layers at the front side and poly-Si at the rear side is that they cause parasitic absorption in short wavelength and long wavelength respectively. The further optimization can be using other wide bandgap materials to replace a-Si:H, such as a-SiC:H [73], or less absorbance coefficient materials in long wavelength to substitute poly-Si, such as poly-SiO_X [39].

5.2.3 Passivation improvement

(1) Hydrogen plasma treatment for intrinsic a-Si:H

Compared to the excellent V_{OC} of 750 mV on HIT solar cell [31], there is great space for improvement. One possibility is applying hydrogen plasma treatment (HPT) after intrinsic a-Si:H layer deposition to reduce defect density and passivate dangling bonds further [93], [94]. While the problems may be induced by HPT are: (1) high concentration of hydrogen induces serious etching to a-Si:H layer which may damage the c-Si surface [95]; (2) high hydrogen dilution encourages the epitaxial growth of a-Si:H film, which has a detrimental effect on passivation quality and is should be avoided [96].

(2) Hydrogenation treatment for rear poly-Si

Since post-deposition annealing for rear poly-Si is carried out in N_2/O_2 atmosphere, other feasible annealing conditions can be tried. Remote plasma hydrogen passivation (RPHP) treatment is a promising method to improve the passivation quality of poly-Si [37]. Besides, forming gas (N_2 and H_2 atmosphere) annealing (FGA) can be another alternative for providing hydrogen to passivate more dangling bonds at the interface which is tried out in our group before.

Acknowledgements

Ten months ago, with the passion for solar energy, I chose the thesis topic related to solar cells fabrication, which was conducted in a professional group – Photovoltaic Materials and Devices (PVMD). Ten month later, I was proud and satisfied about my choice and what I have done during this meaningful period. Concurrently, I would like to express my sincere appreciation to the people who has helped me on the thesis and in the life, full of gratitude.

First, I would like to thank my supervisors, Olindo, Gianluca and Guangtao for their valuable advices, supports and long-time discussion to inspire me for deep dig in experiments and help me understand the scientific theory. Besides, I would like to express my gratitude to PVMD group members for teaching me to use lab equipments and improving presentation skills, especially Paul for band diagram understanding. Additionally, I would like to thank PVMD and EKL technicians, Martijn, Stefaan, Robert and Mario for training me how to use equipments correctly and safely and shooting the problems.

Furthermore, I would like to thank my roommates and classmates in SET to help me in the life. And Finally, I would like to express my gratitude to my family for their unconditional love and support, from the bottom of my heart.

Last but not least, as the strong voice send from Saudi oil minister three decades ago: “The Stone Age didn’t end for lack of stone, and the oil age will end long before the world runs out of oil.”, this would inspire all the engineers from Sustainable Energy Technology Program to strive for a more sustainable future, for us, for everyone.

Hao Ge

TU Delft library, July 2017

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Appendix

Passivating Rear and Front ConTacts (PeRFeCT) solar cell: An *hybrid* approach

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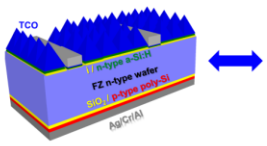
Motivation and challenges

- Contact recombination is the limiting factor in high-η solar cells[1]
- a-Si:H gives very low surface recombination velocity[2]
- Tunneling SiO_2 / implanted poly-Si gives very high passivation quality[3]
- Proposed solar cell is a rear-junction and exhibits i/n a-Si:H at the front side and p-type TOPCon at the rear side

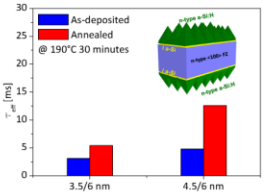


- Thermal budget of the process: 200°C < T < 950°C
- Low temperature metallization and TCO deposition
- Process extremely easy
- High-efficiency concept with industry-relevant process

[1] C.Battaglia, et al., Energy & Environmental Science,(2016); [2] S. Glunz, et al., 31st EUPVSEC, Hamburg, (2015); [3] K. Yamamoto, Asian PVSEC, 2015, Busan, Korea

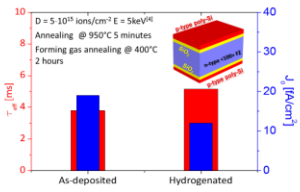
i/n a-Si:H – p-type TOPCon passivation

i/n a-Si:H lifetime symmetric tests



- Increasing i layer thickness -> better chemical passivation
- Annealing makes H^+ diffuse into a-Si/c-Si interface
- Equilibration of the network in the a-Si film[4]

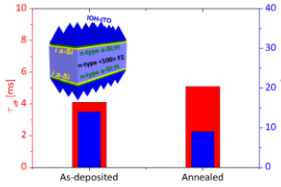
P-type B-implanted TOPCon symmetric tests



- 716 mV as iV_{OC} achieved
- Hydrogenation increases poly-Si mobility[5]
- Post a-Si:H deposition annealing τ_{eff}
- Hydrogenation increases lifetime:
  $J_{0i/n}$ = 7 fA/cm²
  $J_{0,poly}$ = 12 fA/cm²

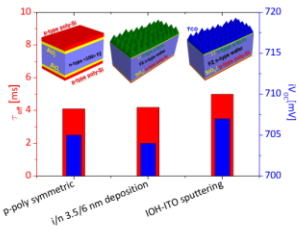
TCO deposition and solar cell precursor tests

IOH-ITO deposition tests



- d_{IOH} = 10 nm low power for minimal sputtering damage
- d_{IOH} = 55 nm for NIR transparency
- d_{ITO} = 10 nm for work function matching with Al

Solar cell precursors lifetime tests



- Monitoring at each step
- Process keeps passivation quality high
- IOH – ITO bilayer to minimize sputtering damage
- Passivation not affected by process

[4] S.De Wolf, et al., Green,(2012); [5] C. Reichel et. al, APL (2015)

Solar cell demonstrators

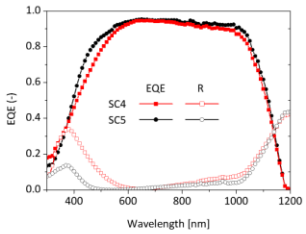
	Front metallization	Area [cm²]	$d_{i/n}$ [nm]	$d_{IOH/ITO}$ [nm]	V_{OC} [mV]	J_{SC-EQE} [mA/cm²]	FF [%]	η [%]	pFF [%]
SC1*	E-beam evaporation	7.84	4.5/6	0/75	695	38.4	71.0	19.0	81.0
SC2	E-beam evaporation	7.84	4.5/6	0/75	703	37.2	71.6	18.7	83.6
SC3	Screen printing + dicing	1.00	4.5/6	0/75	664	36.3	77.9	18.8	83.7
SC4	E-beam evaporation	7.84	7/6	65/10	**712**	37.5	**65.3**	17.4	81.0
SC5	E-beam evaporation	7.84	3.5/6	65/10	703	**38.8**	71.2	19.4	81.0
SC6	E-beam evaporation	9.00	4.5/6	65/10	698	**38.8**	**72.6**	19.7	83.3

Rear metallic stack is evaporated with Ag (200nm) / Cr (30nm) / Al (2µm)

(*) No post deposition annealing

7.84 cm²
H-grid design

9 cm²
squared design



Conclusions

- Both front i/n a-Si:H stack and rear p-type TOPCon achieve low surface recombination velocity
- Annealing after a-Si:H deposition further improves passivation quality
- Combination of thinner a-Si:H and more transparent TCO as IOH increases short-circuit current (J_{SC})
- At cell level, 19.7% efficiency has been achieved

Outlook

	Single cell / best value	Short-term developments	Outlook
V_{OC} [mV]	698 / 712	Texturing, optimized i/n	> 715
J_{SC} [mA/cm²]	38.8 / 38.8	Improving on TCO	> 39.5
FF [%]	72.6 / 77.9	Screen printing / sputtering, Cu-plating, edge isolation, thermally-evaporated Al	> 80
η [%] ($\eta_{combined}$)	19.7 (21.5)		> 22.6