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A CMOS Dual-RC Frequency Reference With ± 200 -ppm Inaccuracy From -45 °C to 85 °C

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Abstract—This paper presents a 7-MHz CMOS RC frequency reference. It consists of a frequency-locked loop in which the output frequency of a digitally controlled oscillator (DCO) is locked to the combined phase shifts of two independent RC (Wien bridge) filters, each employing resistors with complementary temperature coefficients. The filters are driven by the DCO's output frequency and the resulting phase shifts are digitized by high-resolution phase-to-digital converters. Their outputs are then combined in the digital domain to realize a temperature-independent frequency error signal. This digitally assisted temperature compensation scheme achieves an inaccuracy of ± 200 ppm from -45 °C to 85 °C after a two-point trim. The frequency reference draws 430 μ A from a 1.8-V supply, while achieving a supply sensitivity of $0.18\%/V$ and a 330-ppb Allan deviation floor in 3 s of measurement time.

Index Terms—CMOS, digital frequency-locked loop (FLL), digitally controlled oscillator (DCO), integrated frequency reference, RC-based.

I. INTRODUCTION

ELECTRONIC systems rely on accurate frequency references for several functions, such as timing, synchronization, and communication. For almost a century, references based on quartz crystal oscillators have dominated the market because of their excellent accuracy and low jitter [1]. Unfortunately, quartz crystals cannot be directly integrated in standard IC processes and take the form of external and bulky components for most systems-on-chip. Fully integrated frequency references can avoid the use of external components and the related drawbacks in size and costs. The rapid adoption of MEMS frequency references reflects the growing need for more integrated frequency solutions [2].

Integrating a frequency reference in a standard CMOS requires the availability of an on-chip time-constant, i.e., a physical quantity with units of seconds. By using different integrated time constants, various integrated frequency references have been developed, each with different tradeoffs

between their accuracy and power consumption. LC oscillators use lithographically defined on-chip inductors and capacitors to achieve sub-100-ppm inaccuracy over the industrial temperature range [3], [4] but typically operate at GHz frequencies and thus dissipate at least a few milliwatts due to the limited quality factor of their on-chip inductors. References based on the well-defined thermal diffusivity of bulk silicon achieve inaccuracies of about 1000 ppm [5], [6] while those based on the thermal diffusivity of silicon dioxide can achieve about 300 ppm [7] over the military temperature range. However, they typically require a few milliwatts of heating power to achieve reasonable jitter levels [5]–[7].

RC oscillators dissipate much less power, but only achieve moderate accuracy, typically more than 2000 ppm over the industrial temperature range [8]–[13], due to the large temperature coefficients (TCs) of integrated resistors.

First-order TC compensation can be achieved by various combinations of resistors with complementary TCs, resulting in so-called zero-TC (ZTC) resistors [8], [9]. However, the incomplete cancellation of the resistors' higher order TCs limits the resulting accuracy to about 2000 ppm [8]–[13]. Better results can be achieved by digital temperature compensation, in which the output of a temperature sensor is used to perform a polynomial-based correction of the temperature dependence of an on-chip time constant. However, the resulting accuracy is limited by the inaccuracy of the temperature sensor [6].

In addition to the inaccuracy of their time constants, the choice of the oscillator architecture can also limit the inaccuracy of a frequency reference. Non-idealities in the sustaining amplifiers of harmonic oscillators [14] and in the comparators of relaxation oscillators [15] degrade frequency accuracy, and so compensation techniques are required. A better approach is to use a frequency-locked loop (FLL) to lock the frequency of a voltage-controlled oscillator (VCO) to the output of an accurate frequency-to-voltage converter (FVC) [16], thus relaxing the accuracy requirements on the oscillator.

This paper describes an RC-based frequency reference in which high-order temperature compensation is achieved by combining the complementary temperature dependence of two RC networks in the digital domain. After a two-point trim, the result emulates a temperature-independent RC network, which, in turn, forms the basis of a digital FLL (DFLL). Realized in a 0.18 - μ m CMOS process, it generates a 7-MHz output frequency, with an inaccuracy of ± 200 ppm from -45 °C to 85 °C range, 23.8-ps period jitter and an Allan deviation floor of 330 ppb.

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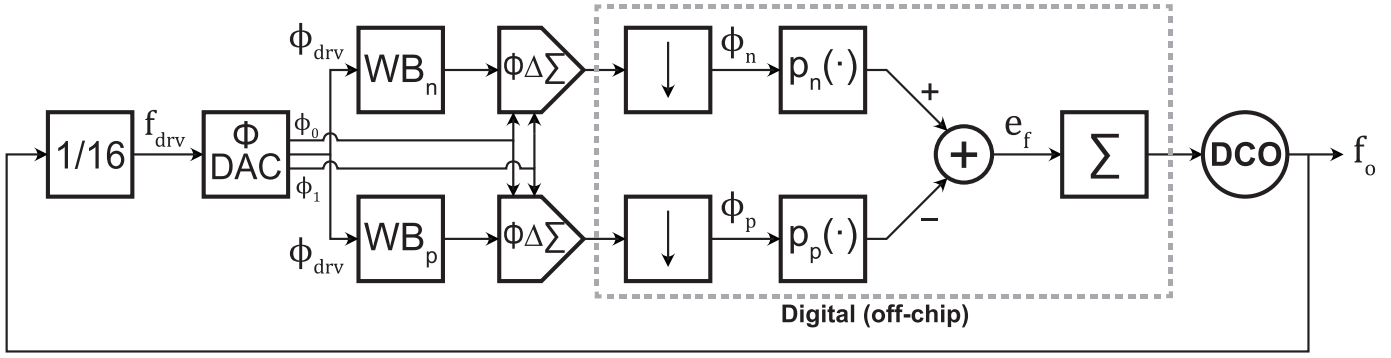


Fig. 1. Block diagram of the dual-RC frequency reference, showing the two-channel digital frequency-locked loop.

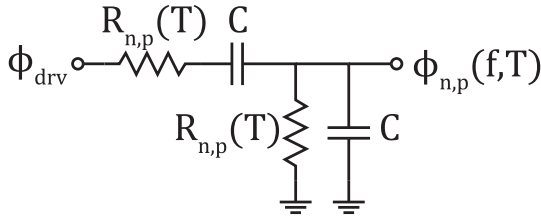


Fig. 2. WB used at the core of the dual-RC frequency reference.

This paper is organized as follows. Section II describes the operating principles of the dual-RC frequency reference. Section III discusses its circuit level implementation. Section IV presents some measurement results and Section V concludes this paper.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the block diagram of the dual-RC DFLL. The digitally controlled oscillator's output frequency, f_o , is applied to two Wien Bridge (WB) filters. Their temperature-dependent phase shifts are then digitized by two phase-domain delta-sigma modulators (PDDSMs) and decimated. After polynomial correction, to compensate for their nonlinear temperature dependencies, the digitized phase shifts are combined to realize a temperature-independent frequency error signal, e_f , which, such as the individual phase shifts, is also a function of f_o . In the steady state, the loop filter forces e_f to be zero, thus fixing the output frequency. In the following, the operating principles of the system will be analyzed in more detail.

A. Temperature-Independent Wien Bridge Phase Readout

As shown in Fig. 2, the WB at the core of the frequency reference is a second-order bandpass filter whose phase shift and center frequency are given by

$$\phi_{n,p}(f, T) = -\tan^{-1}\left(\frac{R_{n,p}(T)^2 C^2 (2\pi f)^2 - 1}{3R_{n,p}(T)C(2\pi f)}\right) \quad (1)$$

$$f_0 = \frac{1}{2\pi R_{n,p}(T)C} \quad (2)$$

where

$$R_{n,p}(T) = R_0(1 + TC_{n,p}(T - T_0) + \dots). \quad (3)$$

T and T_0 are the die temperature and the reference temperature, respectively, and the subscripts p and n refer to each of the two WBs. For clarity, the higher order TCs of the resistors will be ignored for the rest of this analysis.

As the phase shift of each WB is a function of two independent variables, i.e., frequency and temperature, a temperature-independent frequency error cannot be extracted from a single WB filter. Doing this requires two independent WBs, each employing resistors with different TCs. By defining the phase shifts at the center frequency f_0 as a function of temperature T as

$$\psi_{n,p}(T) \triangleq \phi_{n,p}(f_0, T) \quad (4)$$

and $\psi_{n,p}^{-1}$ are the inverses of these functions, where

$$\psi_{n,p}^{-1}(\phi_{n,p}(f_0, T)) = T. \quad (5)$$

We can combine the phase shifts with their respective inverse functions to compute the error signal e_f as

$$e_f(f, T) = \psi_n^{-1}(\phi_n(f, T)) - \psi_p^{-1}(\phi_p(f, T)) \quad (6)$$

where

$$e_f(f_0, T) = 0. \quad (7)$$

In the steady state, the loop drives e_f to 0, and so the DCO's output frequency $f = f_0$.

Fig. 3 shows the simulated phase responses of the two WBs, one employing silicided p-poly resistors ($TC_n = 0.33\%/^\circ\text{C}$) and the other employing unsilicided n-poly resistors ($TC_p = -0.15\%/^\circ\text{C}$) for R_n and R_p , respectively, and the resulting error signal, e_f , after (6) is utilized. In practice, as shown in Fig. 1, the functions $\psi_{n,p}^{-1}$ are implemented by polynomial approximations $p_{n,p}(\cdot)$ to reduce digital complexity. $p_{n,p}(\cdot)$ are obtained by characterizing $\phi_{n,p}$ over temperature, as explained in Section IV-A.

B. Inaccuracy Analysis

The inaccuracy of the dual-RC frequency reference can be estimated from the linear model shown in Fig. 4 (a). Here the errors in each WB due to spread in R_0 and in $TC_{n,p}$ are modeled as additive errors, $\Delta T_{n,p}$. The frequency and

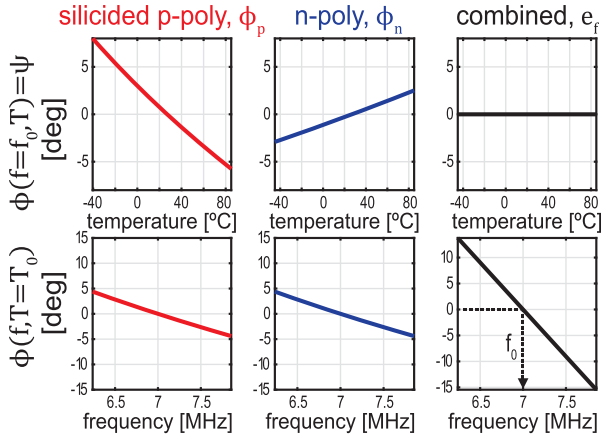


Fig. 3. Top: simulated phase versus temperature responses of the two WB filters and the loop error signal after polynomial correction. Bottom: Simulated phase versus frequency responses of the two WB filters and the loop error signal after polynomial correction.

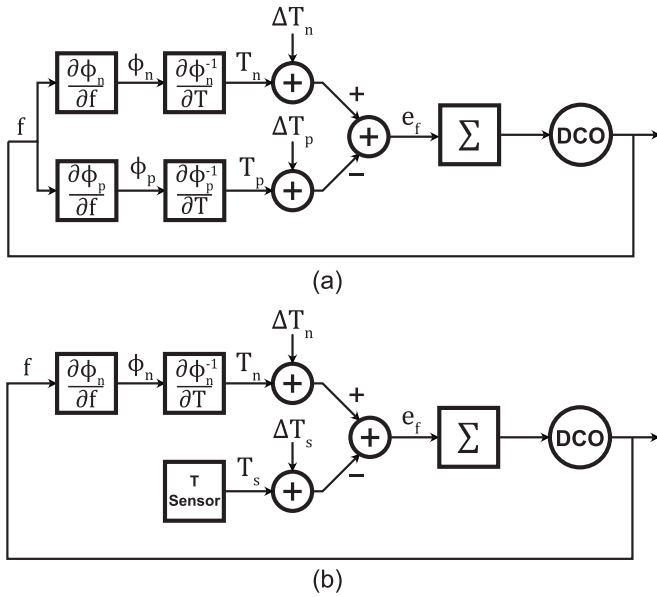


Fig. 4. Linearized model. (a) Dual-channel temperature compensated FLL. (b) Classical temperature compensated FLL.

temperature sensitivities of $\phi_{n,p}$ can be computed from (1) as

$$\left. \frac{\partial \phi_{n,p}}{\partial f} \right|_{f=f_0, T=T_0} = -\frac{2}{3} R_0 C \quad (8)$$

$$\left. \frac{\partial \phi_{n,p}}{\partial T} \right|_{f=f_0} = -\frac{2}{3} TC_{n,p} \quad (9)$$

where the TC of the capacitors has been neglected since it is very small compared with that of the resistors.

This allows the corresponding frequency inaccuracy to be estimated from prior work on WB-based temperature sensors [16]. The error in the output frequency Δf can be computed by exploiting that at the steady state $e_f = 0$. The variance of the frequency error, σ_f^2 , can then be computed

assuming non-correlated errors in the WBs as

$$\sigma_f^2 = (\sigma_{T_n}^2 + \sigma_{T_p}^2) \left(\frac{1}{\frac{\partial \phi_n}{\partial f} \frac{\partial \psi_n}{\partial T} - 1 - \frac{\partial \phi_p}{\partial f} \frac{\partial \psi_p}{\partial T} - 1} \right)^2 \quad (10)$$

where $\sigma_{T_n}^2$ and $\sigma_{T_p}^2$ are the variance of ΔT_n and ΔT_p , respectively. Using (8) and (9) together with (10), we get

$$\frac{\sigma_f}{f_0} = \frac{\sqrt{\sigma_{T_n}^2 + \sigma_{T_p}^2}}{\left| \frac{1}{TC_n} - \frac{1}{TC_p} \right|}. \quad (11)$$

Equation (11) shows that employing resistors with TCs with different signs reduces the overall frequency error. Using the experimental data reported in [17], which was also obtained after a two-point trim, the combination of a silicided p-poly resistor ($TC_n = 0.33\%/^\circ\text{C}$ and $3\sigma_{T_n} = 0.05^\circ\text{C}$) and an unsilicided n-poly resistor ($TC_p = -0.15\%/^\circ\text{C}$ and $3\sigma_{T_p} = 0.2^\circ\text{C}$) yields an expected frequency inaccuracy of 175 ppm (3σ).

It is worth noting that (11) indicates that employing two resistors with TCs of the same polarity will *increase* frequency inaccuracy. As expected, the inaccuracy tends to infinity if the two TCs are exactly the same.

It is interesting to compare the above results with the case of a traditional temperature-compensated FLL, in which a temperature-independent error signal, e_f , is obtained by replacing one of the WB channels with a temperature sensor [6]. The linear model for this case is shown in Fig. 4(b), where the temperature sensor's inaccuracy is modeled by ΔT_s . As before, the relative error on the output frequency can be expressed as

$$\frac{\sigma_f}{f_0} = |TC_n| \sqrt{\sigma_{T_s}^2 + \sigma_{T_n}^2}. \quad (12)$$

Using the silicided p-poly of [17] coupled with a temperature sensor with 0.1°C (3σ) inaccuracy, i.e., [18] and [19] would yield an expected inaccuracy of 334 ppm (3σ).

C. Digital Frequency-Locked Loop

The DFLL can be approximated as a single-pole system [6], with the dominant pole introduced by the integrator implementing the loop filter.

Two noise sources will dominate the output noise of the DFLL: the phase-readout noise and the DCO noise. The phase-readout noise is transferred to the output frequency via a low-pass transfer function, with the passband gain defined by the phase-to-frequency sensitivity of the WB. The DCO noise is high-pass filtered by the loop, with a unity passband gain. Thus, the long-term jitter of the DFLL will be dominated by the phase readout; whereas, the DCO will dominate the short-term jitter of the DFLL. To achieve short-term jitter levels that are compatible with the target accuracy of 500 ppm, the open-loop DCO jitter should be on the order of $10 \text{ ps}_{\text{rms}}$. This requirement ensures that trimming can be performed with the required accuracy in a reasonable measurement time.

To track thermal transients, the bandwidth of the DFLL loop should be larger than the thermal time constant of the die [20]. Thus, the loop bandwidth should be higher than $\sim 10 \text{ Hz}$.

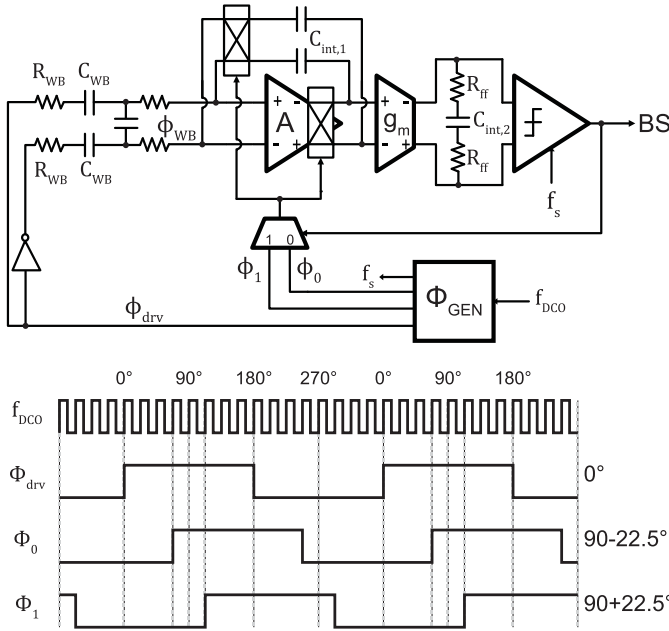


Fig. 5. Schematic of the PDDSM.

However, the existence of nondominant poles in the WB, in the phase-readout and in the DCO places an upper limit on the loop bandwidth required to ensure stability. In this paper, a loop bandwidth of ~ 50 Hz was chosen. Thanks to the highly digital nature of the loop, this can be achieved without using large passive components.

III. CIRCUIT DESIGN

A. Phase-Domain Delta Sigma Modulator

The core of the phase readout consists of a PDDSM in which a synchronous demodulator is embedded in a continuous time delta-sigma ADC [21].

Fig. 5 shows the schematic of the PDDSM [17]. It employs a fully differential version of the WB shown in Fig. 2, with a current output that can be directly connected to the virtual ground of the first integrator stage. In this design, $R_{WB} = 32$ k Ω and $C_{WB} = 10$ pF. The WB is driven at a frequency $f_{drive} = f_{DCO}/16$. The output current is then fed to the input of the PDDSM, where it is applied to a chopper demodulator driven by phase references $\phi_{0,1} = 90^\circ \pm 22.5^\circ$ that are selected by the bitstream output. The demodulator's output is then integrated on the capacitors of the first-stage integrator.

The gain in the delta-sigma loop filter drives the output of the mixer to 0 on average, which ensures that the bitstream average is a function of $\phi_{0,1}$ and the WB phase shift. Although the use of a chopper demodulator results in additional cosine nonlinearity, this can be effectively corrected in the digital domain [22]. The drive signal f_{drive} @ $\phi_{drive} = 0^\circ$, the phase references $\phi_{0,1} = 90^\circ \pm 22.5^\circ$, and the sampling clock with phase $\phi_s = 135^\circ$ for the DSM comparator are all derived from the DCO's 7-MHz output frequency. The values of $\phi_{0,1}$ were chosen to cover the expected phase range over temperature, while allowing for DCO spread after coarse trimming.

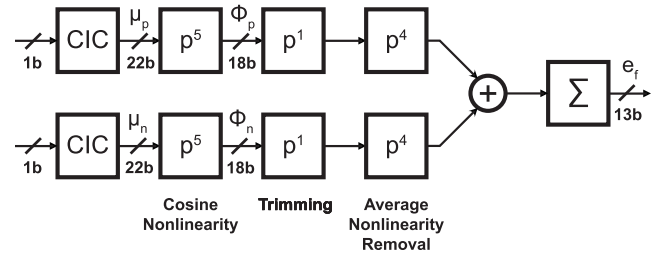


Fig. 6. Schematic of the digital section comprising the temperature compensation and the loop filter.

The exact value of ϕ_s is not critical, as long as sampling does not occur at the transitions of the WB drive or of the phase references.

Chopper switches around the first stage modulate the offset and the $1/f$ noise of the first stage integrator to f_{drive} . They are then filtered by the second-order continuous time loop filter of the PDDSM. The first integrator is built around a two-stage amplifier [17] and a large integration capacitor ($C_{int,1} = 200$ pF). A degenerated transconductance amplifier ($g_m = 2$ μ S) and the integration capacitor ($C_{int,2} = 8$ pF) form the second-stage integrator. The feedforward coefficient required for loop stability is implemented by a series resistor ($R_{ff} = 250$ k Ω) of the same material as the WB resistor to improve the robustness of the DSM loop filter to process spread and temperature.

B. Digital Temperature Compensation and Loop Filter

Digital temperature compensation is accomplished by processing the outputs of the two PDDSMs to produce the temperature-independent loop control signal, e_f , that drives the loop filter. Fig. 6 shows the detailed block diagram of the associated digital blocks.

Two-stage CIC decimation filters [23] remove the over-sampled and shaped quantization noise of the PDDSM outputs prior to polynomial computation. The CIC filters are implemented with a decimation factor of $R = 1024$ and a differential delay of $M = 2$. The chosen parameters achieve a loop sample rate of 427 Hz with 22-bit word length for each phase after decimation.

Polynomials for each channel are implemented as a cascade of three stages. A fifth-order odd polynomial removes cosine nonlinearity originating from the PDDSM. The cancellation of cosine nonlinearity allows the following first-order polynomial (p^1) to implement the two-point trimming directly on the WB phase. The coefficients for p^1 are unique per sample and are extracted after characterizing each sample at two temperatures. Finally, two fourth-order polynomials are used to remove the average nonlinearity of the trimmed sp-poly and n-poly WBs. The coefficients for p^4 are the same for all samples and are extracted by characterizing a statistically significant set. All polynomials have fixed-point 24-bit internal operands and 18-bit output words, which ensures that the quantization errors originating from the polynomials are well below the expected accuracy of the frequency reference.

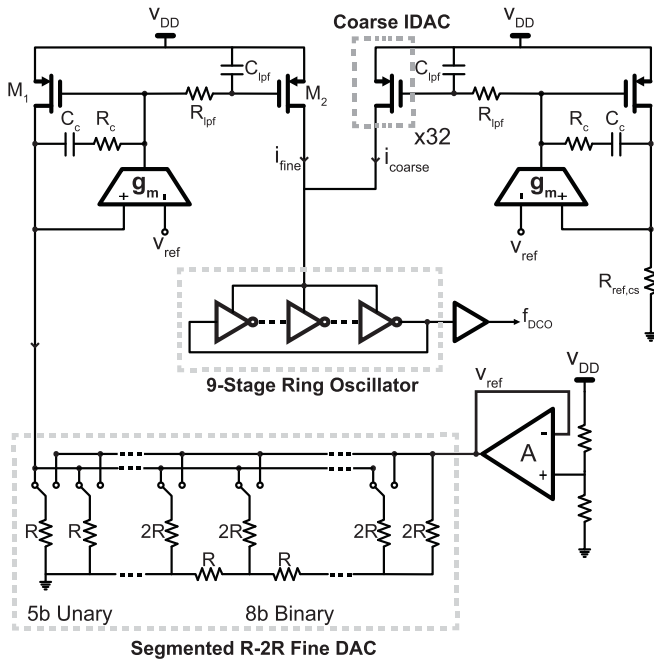


Fig. 7. Schematic of the DCO.

After polynomial correction, the outputs of the two channels are subtracted to achieve the temperature-independent frequency error word, e_f . A 24-bit accumulator running at the loop sample rate integrates e_f and 13-bit MSBs of the accumulator output drive the DCO, closing the loop. A programmable bit shifter following the accumulator allows the loop gain to be adjusted, so that the dominant pole of the loop can be flexibly chosen.

C. Digitally Controlled Oscillator

The DCO provides a digitally programmable output frequency that is the ultimate output of the frequency reference, as well as the feedback signal to the PDDSM.

The DCO must be designed to provide the expected output frequency over PVT. Process variations, which are static after fabrication, will shift the nominal DCO frequency by about $\pm 50\%$, while supply voltage and temperature variations contribute about $\pm 7.5\%$.

In addition, the DCO should have a sufficiently small LSB, because at steady state, the loop output will toggle between two quantization levels. This LSB switching appears directly at the output and, if too large, can degrade the output jitter, which must be low enough to facilitate trimming to the target accuracy in a reasonable measurement time. Moreover, the DCO needs to be monotonic to ensure feedback stability.

Fig. 7 shows the schematic of the DCO. A nine-stage current-starved ring oscillator is controlled by segmented coarse/fine current DACs. A five-bit current-steering DAC (coarse DAC) provides a current i_{coarse} of $180 \mu\text{A}$ and covers the expected $\pm 50\%$ static variation in the DCO center frequency, corresponding to a 125-kHz LSB. A 13-bit current output segmented R-2R DAC (fine DAC) provides a current i_{fine} of $30 \mu\text{A}$ and covers the $\pm 7.5\%$ variation in the

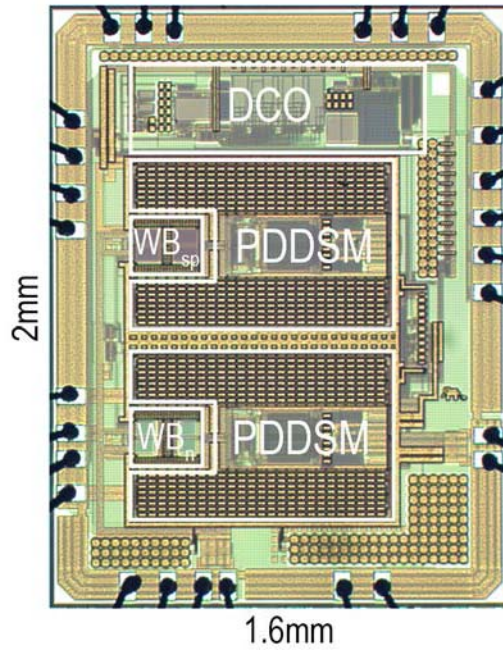


Fig. 8. Chip micrograph for the dual-RC frequency reference.

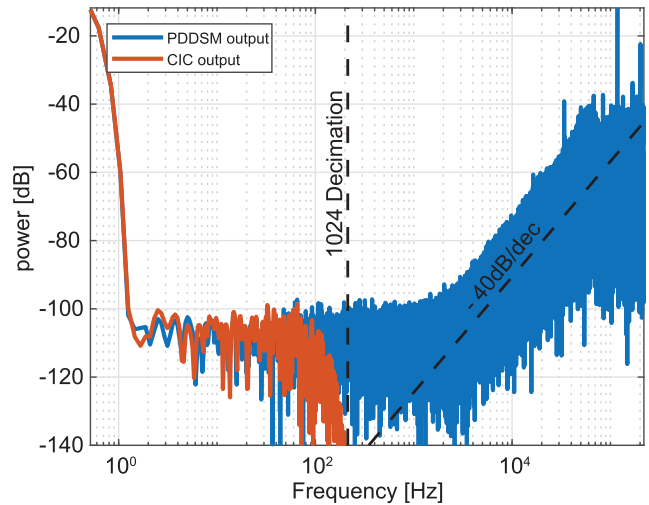


Fig. 9. PSD of the PDDSM output, before and after the decimation filter.

DCO center frequency due to temperature and supply voltage variations. This corresponds to a 120-Hz (17 ppm) LSB step which ensures that the quantization noise of the fine DAC is much lower than the expected DCO jitter of 20 ps (140 ppm). This segmentation allows a large tuning range to be covered, and only the fine DAC needs to be monotonic. A resistive divider can be used to generate the reference voltage V_{ref} , since it does not determine the DFLL's closed-loop accuracy.

To achieve monotonicity, the fine DAC is further segmented into a five-bit unary RDAC and an eight-bit binary R-2R DAC, with high-resistive polysilicon unit resistors. The output current of the fine DAC is applied to the ring oscillator via the regulated current mirror consisting of M_1 , M_2 , and the OTA g_m . The regulated current mirror also maintains the output of the fine R-2R DAC at V_{ref} . It also features an RC low-pass filter (R_{RC} and C_{RC}) to filter wide-band

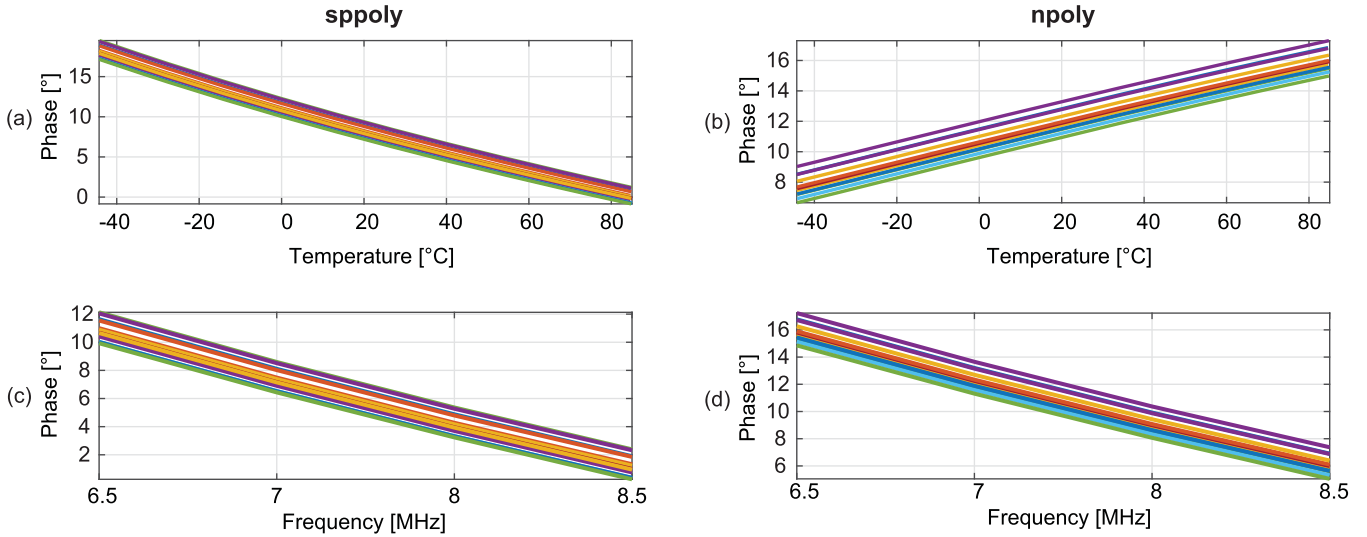


Fig. 10. Phase versus temperature response of silicided (a) p-poly and (b) n-poly WBs and phase versus frequency response of silicided (c) p-poly and (d) n-poly WBs.

noise originating from the DACs and from V_{ref} , so as not to significantly degrade the period jitter of the DCO. A low-pass filter with a cut off 10 times higher than the update rate of the loop ($f_{RC} = 4$ kHz) is chosen so as not to significantly affect loop stability. A similar regulated-mirror structure is used for the coarse DAC to fix the voltage across $R_{ref,cs}$ and generate the reference current for the current-steering coarse DAC.

IV. MEASUREMENT RESULTS

The dual-RC frequency reference (Fig. 8) was implemented in a TSMC $0.18\text{-}\mu\text{m}$ standard CMOS process. The chip has an active area of 1.59 mm^2 , 0.62 mm^2 for each WB and PDDSM combination and 0.35 mm^2 for the DCO. For flexibility, the decimation filter, polynomial computation, and loop filter were realized off-chip in an FPGA. Twelve devices from a single batch were packaged in ceramic DIL28 packages.

Each PDDSM (including its WB) dissipates $162\text{ }\mu\text{W}$. The DCO dissipates $450\text{ }\mu\text{W}$ for a total of $775\text{ }\mu\text{W}$ from a 1.8-V supply. If integrated on chip, synthesis and simulations show that the FPGA logic would consume less than $50\text{ }\mu\text{W}$. The CIC decimators dissipate the largest power, $20\text{ }\mu\text{W}$ each, while running at 437.5 kHz .

A. Open-Loop Temperature Characterization and Trimming

Initially, both WBs were driven by an external reference at the target frequency of 7 MHz , resulting in a WB drive frequency and a sampling frequency of 437.5 kHz . Fig. 9 shows the power spectral density (PSD) of the PDDSM output at room temperature before and after the decimation filter. The second-order-shaped quantization noise and its filtering by the CIC filter can be clearly seen. The decimated phase word has 0.013 m° phase resolution at the loop sampling rate of 427 Hz .

To determine their phase versus temperature characteristics, the chips were placed in a temperature-controlled oven and the temperature was swept over the range from -45 °C to 85 °C with steps of 10 °C. The temperature was determined by a Pt-100 reference resistor mounted in an aluminum block in

thermal contact with the packages. To determine their phase versus frequency characteristics, the WBs were stabilized at a fixed temperature of 27 °C and the drive frequency was varied from 6.5 to 8 MHz .

Fig. 10(a) and (b) shows the phase versus temperature characteristics of the sp-poly and n-poly WBs for all 12 samples. The sp-poly WB shows an average -18° phase shift over temperature. Similarly, the n-poly WB shows an average 8° phase shift. Fig. 10(c) and (d) show the phase versus frequency response for the sp-poly and n-poly WBs. Both WBs show 9° phase shift over the 1.5-MHz range (93.75-kHz range for WB drive.)

From the inverse of the phase to temperature characteristics, two-point trimming polynomials (p^1) were determined for each sample by utilizing the -35 °C and 75 °C measurement points. The residual nonlinear error was averaged over all samples for the sp-poly and n-poly WBs, resulting in two fourth-order fixed polynomials (p^4). Using the linear model of (10), the spread after applying p^4 can be used to estimate the expected contribution of each channel to the total closed-loop frequency inaccuracy. Fig. 11(a) shows that the sp-poly WB contributes ± 50 -ppm inaccuracy, whereas Fig. 11(b) shows that the n-poly WB contributes ± 140 ppm. By combining the two results using (10), the expected total inaccuracy after open-loop characterization is found to be ± 150 ppm and is dominated by the spread of the n-poly WB.

In Section III-C, it was stressed that DCO monotonicity is crucial for loop stability. To verify this, the DCO was characterized by measuring the frequency output as the digital code was swept through the entire control range of the fine DAC. Fig. 12 shows that the DCO achieves 12-bit DNL and 8-bit INL. As discussed earlier, the latter will be corrected by the feedback loop.

B. Closed-Loop Frequency Reference Characterization

Following the extraction of the polynomials p^1 and p^4 , the DFLL loop was closed in the digital domain and the

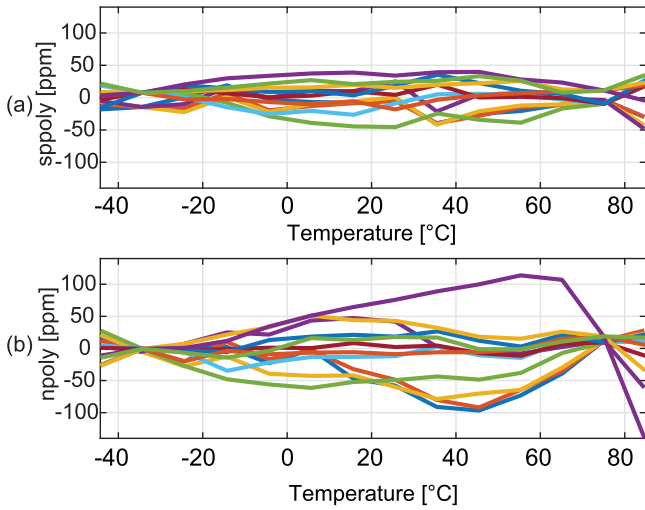


Fig. 11. Inaccuracy contribution of silicided (a) p-poly and (b) n-poly WBs.

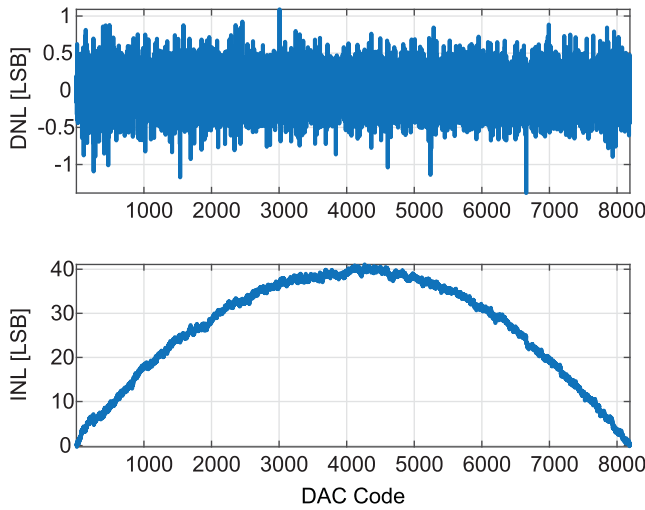


Fig. 12. Measured DNL and INL of the DCO when sweeping the fine DAC in open loop.

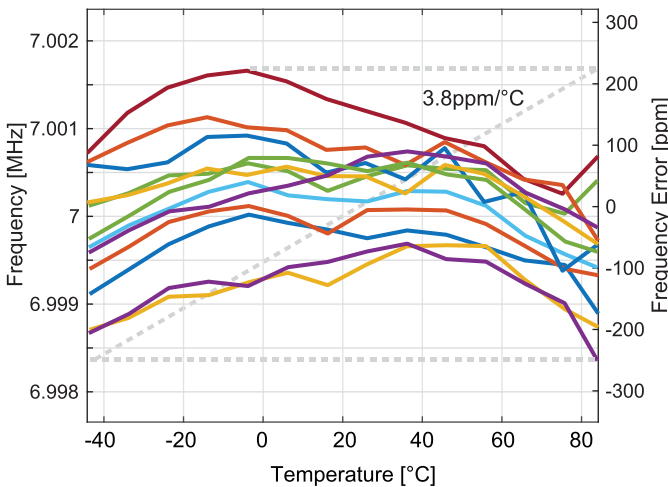


Fig. 13. Inaccuracy of the open-loop compensated frequency reference with temperature variations.

frequency reference was characterized over temperature. Fig. 13 shows that over the target range from $-45\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, the frequency reference achieved ± 250 -ppm frequency

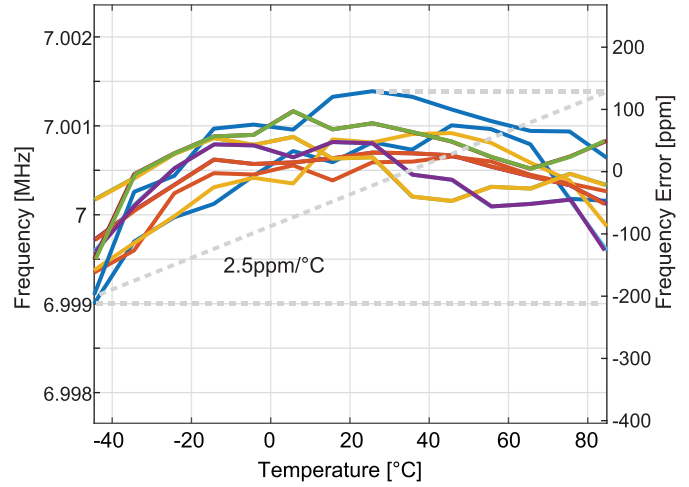


Fig. 14. Inaccuracy of the closed-loop compensated frequency reference with temperature variations.

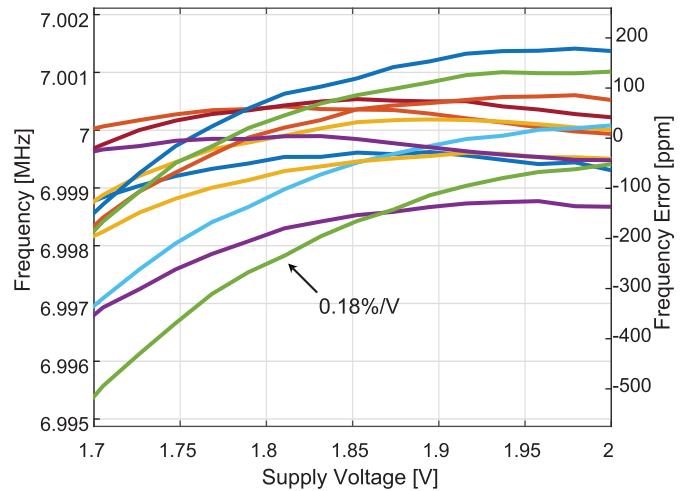


Fig. 15. Inaccuracy of the compensated frequency reference with supply voltage variation.

accuracy (12 samples), resulting in a residual TC of $3.8\text{ ppm}/^{\circ}\text{C}$ (box method).

However, the resulting accuracy is significantly worse than that expected from the open-loop characterization ($\pm 150\text{ ppm}$). The model in (10) assumes that error propagation through the loop is ideal and does not account for extra errors caused, for example, by the use of fixed-point arithmetic. To address this, the coefficients of p^1 were again trimmed at $(-35\text{ }^{\circ}\text{C}$ and $75\text{ }^{\circ}\text{C})$ but with the loop closed. Fig. 14 shows that over the target range from $-45\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, the closed-loop trimmed frequency reference then achieves ± 200 -ppm frequency accuracy (eight samples), resulting in a residual TC of $2.5\text{ ppm}/^{\circ}\text{C}$ (box method). There still remains some residual curvature, since p^4 was determined by an open-loop calibration. In a production scenario, each sample would only require a closed-loop trim at two temperature points.

For the supply sensitivity characterization, the 1.8-V nominal power supply voltages for both the PDDSM and the DCO were varied between 1.7 and 2 V . Fig. 15 shows that the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR ART

	This Work	[24]	[8]	[9]	[10]	[11]	[12]	[13]
Process [nm]	180	180	180	60	180	65	180	65
Frequency [Hz]	7M	24M	3K	32.768K	70.4K	32.768K	11	1.3M
Power [W]	775u	200u	4n	4.48u	99.4u	0.19u	5.8n	0.92u
Area [mm ²]	1.59 ²	0.17	0.5	0.048	0.26	0.015	0.24	0.005
TC [ppm/°C]	3.85 (OL) 2.5 (CL)	18 ¹	13.8	16.67	27.4	38.18	45	96
T Range [°C]	-45 to 85	-40 to 150	-25 to 85	-20 to 100	-40 to 80	-20 to 90	-10 to 90	0 to 150
Voltage [%/V]	0.18	0.03	0.49	0.125	0.5	0.09	1.0	0.49
V Range [V]	1.7 to 2.0	1.8 to 5.0	0.85 to 1.4	1.6 to 3.2	1.2 to 3.0	1.15 to 1.45	1.2 to 2.0	0.9 to 1.9
# of Samples	12 (OL) 8 (CL)	>200 ¹	1	4	1	5	1	2
ADEV [ppm]	0.33	-	63	-	7	4	70	-

¹ Worst case TC computed as $\mu+6\sigma$ from $\mu=3.3\text{ppm}/^\circ\text{C}$ mean and $\sigma=2.45\text{ppm}/^\circ\text{C}$ standard deviation over 200 samples

² Does not include the area of the off-chip digital blocks

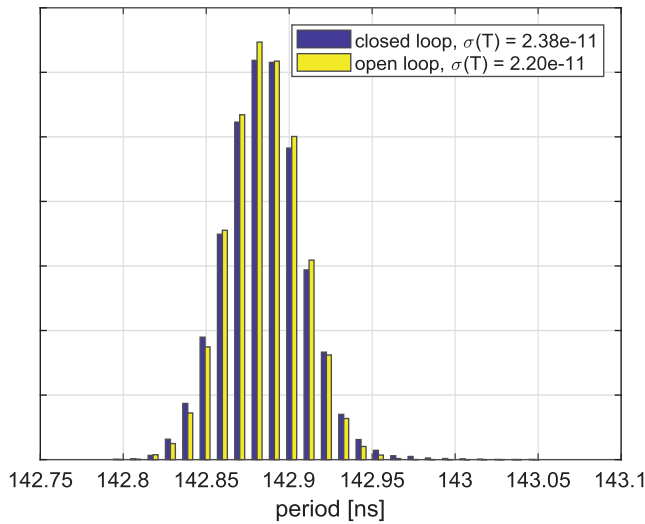


Fig. 16. Period jitter for the closed- and open-loop settings.

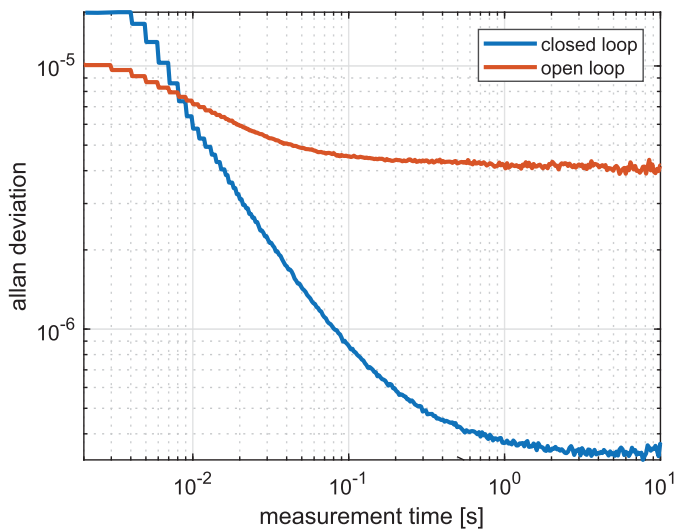


Fig. 17. Allan deviation of the frequency reference for closed- and open-loop operations.

worst case sample has 540-ppm frequency shift, resulting in a voltage coefficient of 0.18%/V.

As shown in Fig. 16, the period jitter of the open-loop DCO is 22 ps, while that of the DFLL is 23.8 ps. This shows that the short-term jitter is dominated by the DCO.

Allan deviation measurements (Fig. 17) show a four-ppm floor for the open-loop DCO, which improves to 330 ppb for the DFLL after 3 s of measurement time, reflecting the much better stability of the on-chip RC time constants.

Table I shows the performance summary of the dual-RC frequency reference and compares it with the state of the art for integrated RC frequency references. The frequency reference in this paper has considerably higher power consumption, primarily due to the DCO, which accounts for over 50% of the power budget. The proposed reference shows a 5.5 times improvement in residual TC over 12 samples compared with the best reported RC reference [7]. Compared with the best reported Allan deviation floor [10], the dual-RC frequency reference shows a 12 times improvement.

V. CONCLUSION

This paper presents a 7-MHz RC frequency reference realized in a standard 0.18- μm CMOS process. The phase responses of two RC networks, each made from resistors with opposite signed TCs, are combined in the digital domain to achieve an accurate time-constant to which the frequency of a DCO is locked. Compared with the state of the art, this digital compensation scheme achieves better accuracy (± 200 ppm from -45 °C to 85 °C, eight samples, and two-point trim). The adoption of high-resolution phase readout allows for an excellent long-term stability (330 ppb at 3 s). The measurement results prove the viability and advantages of RC-based references as fully integrated frequency references in the standard CMOS.

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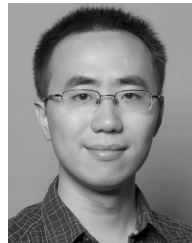
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