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On-Chip Cryogenic Read-Out of Spin Qubit for Quantum Computers

TU Delft

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By

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Abstract

Quantum computing holds the promise to solve problems that are currently intractable by classical computing platforms. Such computing framework relies on the properties of quantum bits (qubits) that operates at cryogenic temperatures well below 1K. Besides a quantum processor, an operational quantum computer needs a classical electronic controller reading out the electrical signals generated by the qubits and the providing electrical control to perform the required operations on the qubits. Since today's quantum processors comprise a low number of qubits (<10), most controlling electronics can operate at room temperature and be connected by bulky interconnects to the cryogenic qubit chamber. However, when scaling up to the thousands of qubits required in a practical quantum algorithm, the classical electronics must be placed at cryogenic temperature to simplify the interconnects and allow a compact, reliable and scalable system. In this work, we propose the fully-integrated implementation in standard CMOS technology of the electronic read-out for spin qubits. Simulations show that the proposed current read-out circuit can achieve a 10MHz bandwidth that is 10X wider than current state-of-the-art read-outs while keeping comparable noise performance and operating at 4.2K. Such results are a promising indication that cryogenic CMOS circuits can provide the building blocks for the integration of the classical electronic controller for future scalable quantum computers.

Acknowledgement

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1 Introduction: The need for cryogenic electronics

Designing electronic circuits that operate at cryogenic temperatures has gained a considerable attention over the recent year. Cryogenic electronics can be extremely useful in applications characterized by a very low operating temperature. For example, the operating temperature in many space missions is considerably lower than the specified operating temperature of electronic devices currently available on the market. As an example, Table 1.1 shows operational temperatures for unheated spacecraft on outer planets (typical surface temperature of different planets). As a result, bulky heating equipment is required to keep the temperature of the electronic units around 20 °C [21]. Designing electronic devices that are directly operational at such cryogenic temperatures will allow removing the heating units, thus resulting in a lighter and smaller spacecraft payload, in lower power consumption, and possibly higher reliability.

Mission	Temperature(℃)
Mars	-20 to –120
Jupiter	-151
Saturn	-183
Uranus	-209
Neptune	-222
Pluto	-229

Table 1.1 Typical operational temperatures for unheated spacecraft [21].

In addition to deep-space application, cryogenic electronics has potential uses in other areas like medical diagnosis, superconducting magnetic energy storage [22], and control electronics for quantum computers. Fig. 1.1 shows a measurement setup for Superconducting Nanowire Single-Photon Detector (SNSPD) in which samples are placed at 1 Kelvin. Moving the electronic readout circuit to lower temperatures is one of the first steps towards on-chip integration of such a quantum optical systems [23]. Another place for use of cryogenic electronics is that of accurate sources or measurement instruments. Fig. 1.2 shows an electron counter, which can be used as a highly precise ampere meter. Some passive (inductor, capacitor, and bidirectional coupler) and active (amplifier) components are already placed at very low temperature (1 to 4 K). Aside from the afore-mentioned advantages of cryogenic applications, cryogenic operation can also lead to performance improvements in electronic circuits in terms of speed and noise, while other performance measures may also improve. Fig. 1.3 shows the variation of some parameters of a Metal-Oxide–Semiconductor Field-Effect Transistor (MOSFET) over temperature. For instance, the maximum oscillation frequency and transconductance of a standard MOS transistor increase at a lower temperature. A more detailed discussion about these parameters is presented in the next sections. Although cryogenic electronics has a wide range of applications, the rest of the thesis will focus on the application of cryogenic electronics in quantum computers that is the object of this work.

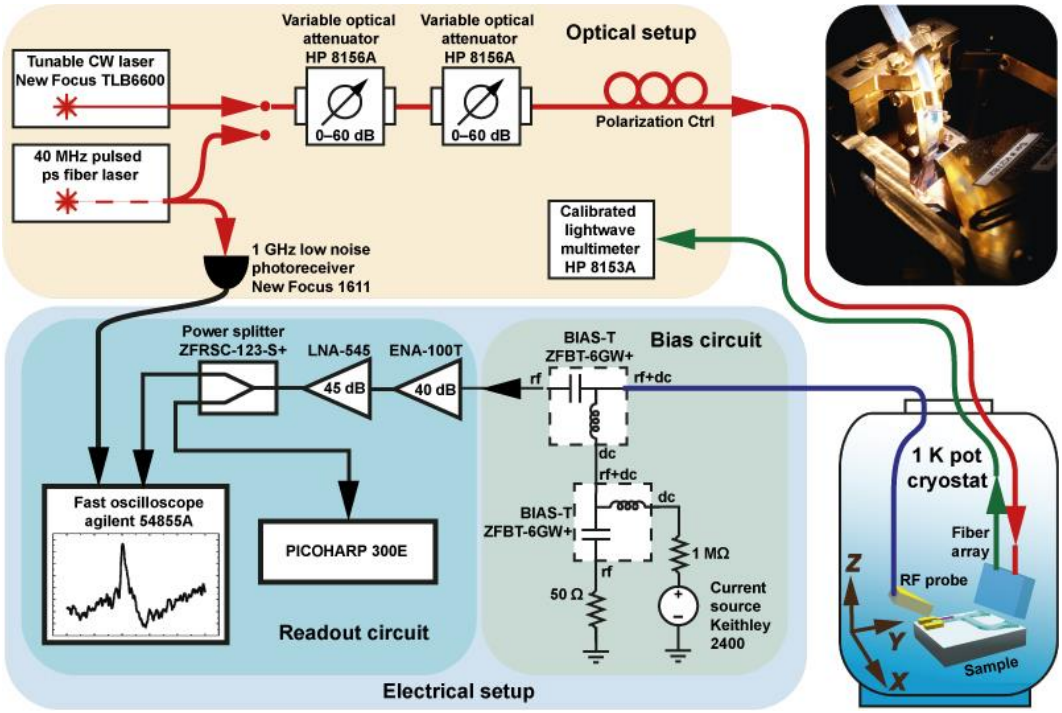


Figure 1.1 The optical setup including laser sources, attenuators and reference detectors. The electrical setup including the bias current source for the SNSPDs and the readout electronics are operating at room temperature [8].

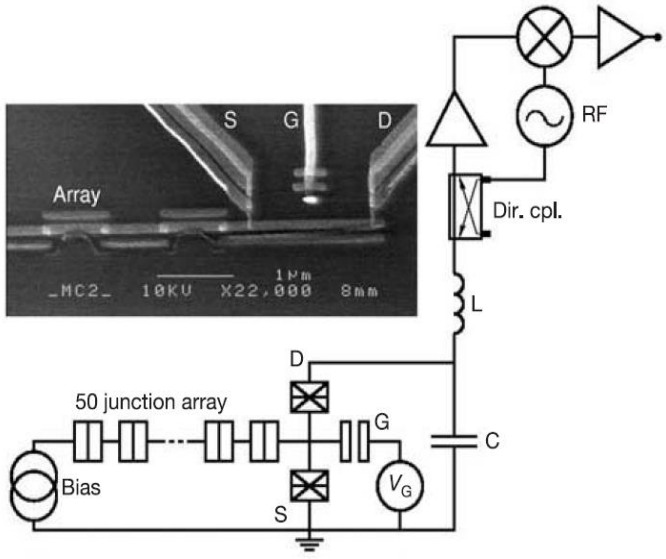


Figure 1.2 Experimental set-up. Scanning electron micrograph of the sample and a schematic layout of the electron counter based on a Single Electron Transistor (SET). Via a directional coupler (dir. cpl.), a radio-frequency signal (f = 358 MHz) is applied to the LC circuit (L is inductance) in which the SET is embedded. The quality factor of the resonator is Q < 15, giving a bandwidth of about 10 MHz. The junction array is placed in a dilution refrigerator at T < 30 mK [17].

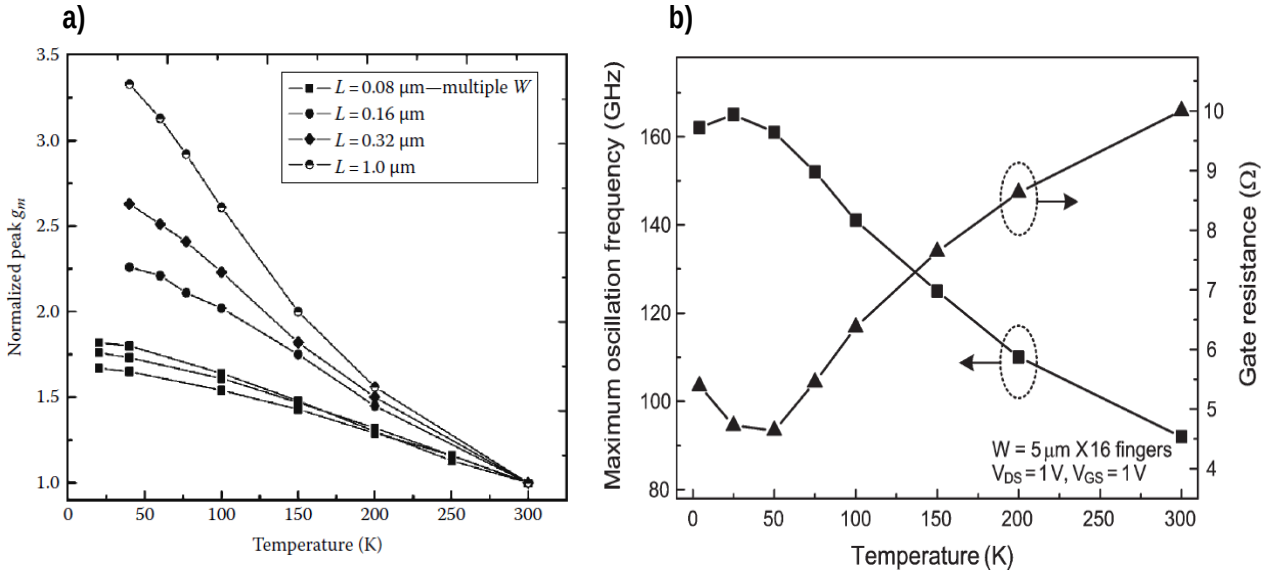


Figure 1.3 a) Normalized peak transconductance as a function of temperature for nMOSFET devices with different gate lengths [4]. b) Dependence of the maximum oscillation frequency and gate resistance on temperature (90nm nMOSFET) [19].

1.1 Quantum Computing

One possible approach to improve computing power (at least in certain applications) is to exploit the quantum properties of matter to create new, non Von Neumann computing paradigms. A quantum bit (qubit) is the counterpart of the classical bit in quantum computing domain [24]. Two important properties of a qubit are ***superposition*** and ***entanglement***. Superposition relates to the fact that in a quantum two-level system, unlike its classical analogue, the state of a qubit can be "0" and "1" simultaneously and the states are follow Dirac's notation $|1\rangle$ and $|0\rangle$. In particular, the state is expressed as $\alpha|0\rangle + \beta|1\rangle$. α and β are probability amplitude of states $|0\rangle$ and $|1\rangle$, respectively so as to satisfy $\alpha^2 + \beta^2 = 1$. The outcome of such a system is apparently not deterministic although the probability coefficients can be determined. Note that after the measurement the output must be either state $|0\rangle$ or $|1\rangle$.

Entanglement relates to the fact that it is possible to connect qubits so that they cannot operate independently. Note that, after a measurement, a two-level qubit should settle to one of the states. Due to the entanglement (strong bond) between two qubits, measuring one qubit influences the state of the other instantaneously.

To understand the superior performance of quantum computers over classical computers, consider an N-qubit system. Unlike classical computers, a quantum processor can theoretically process all 2^N states at the same time. This exponential increase of computation power gives the quantum computer the capability of quickly solving intractable problems.

Although, after the measurement, the N-state qubit will collapse into a single state losing the superposition, quantum algorithms can be designed to properly exploit superposition and entanglement to achieve quantum speed-up, i.e. the ability to solve problems much faster than a classical computer would ever do. For instance, Shor's algorithm compute the integer factorization much faster than any classical factoring algorithms. However, it should be noted that currently only certain types of problems can be solved by quantum computers.

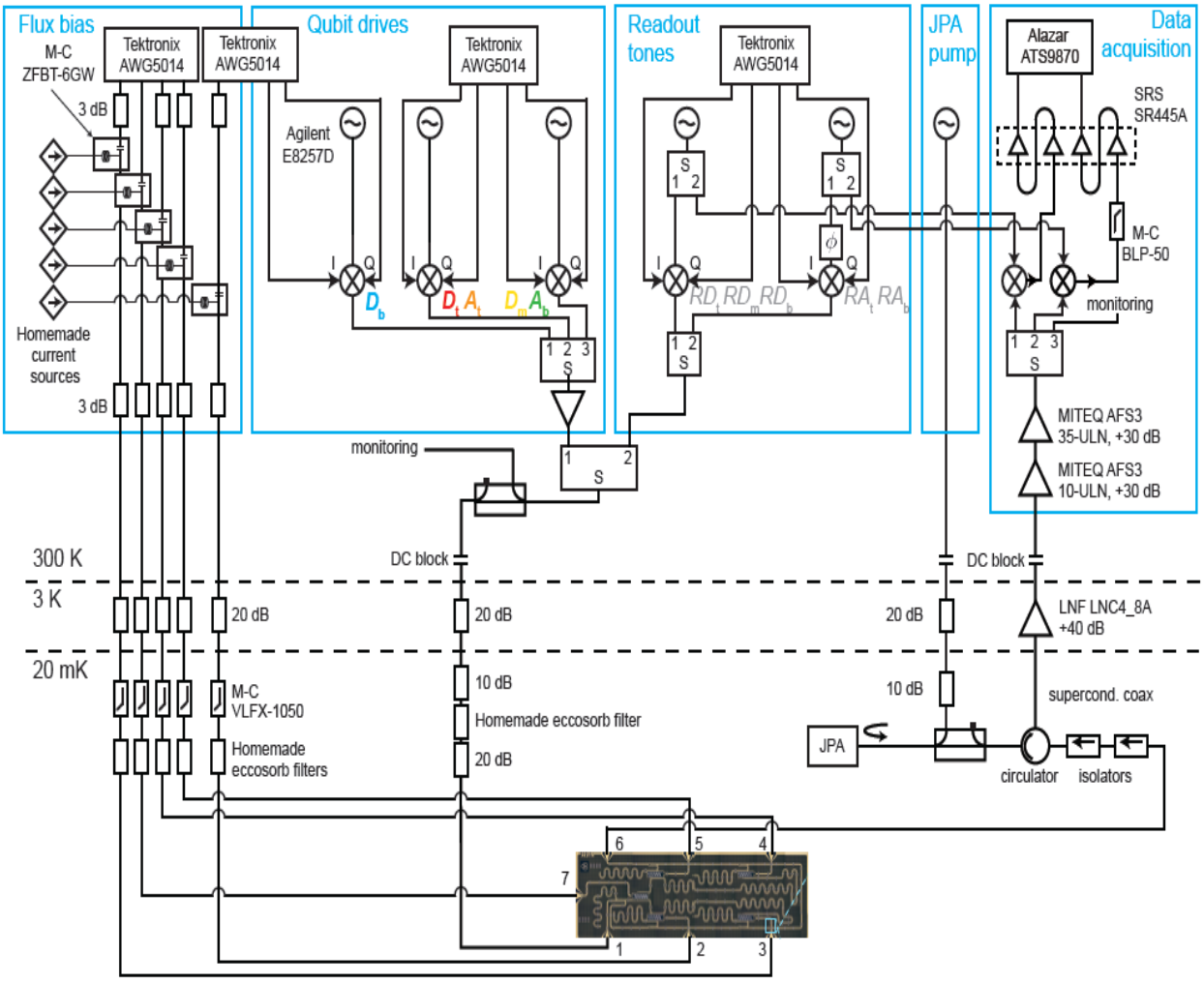


Figure 1.4 Experimental setup and device details. Complete wiring of electronic components outside and inside the dilution refrigerator (Leiden Cryogenics CF-450) [11].

1.2 Practical Quantum Computer

All quantum phenomena exploited by quantum processors are prone to any noise or disturbance from the environment. Any unwanted interaction between qubits and the environment can cause decoherence in the quantum states. If these errors are small enough, they can be detected and corrected through quantum error correction techniques [25]. For proper operation, quantum devices must then be operated at temperatures well below 1 K.

For the sake of understanding the challenges confronting quantum computers' scaling, we need to have a look on a practical architecture of a quantum computer. Fig. 1.4 shows a realistic quantum computer (with 7 qubits) consisting of several temperature stages in order to properly isolate the processor core from ambient disturbance. As it can be seen from Fig. 1.4, there are many passive and active components used to filter out the noise coming from read-out and controlling unit (placed at stages with higher temperature). In order to scale up such a quantum computer, we need to reduce the size of classical electronic sections as well as the core of the processor.

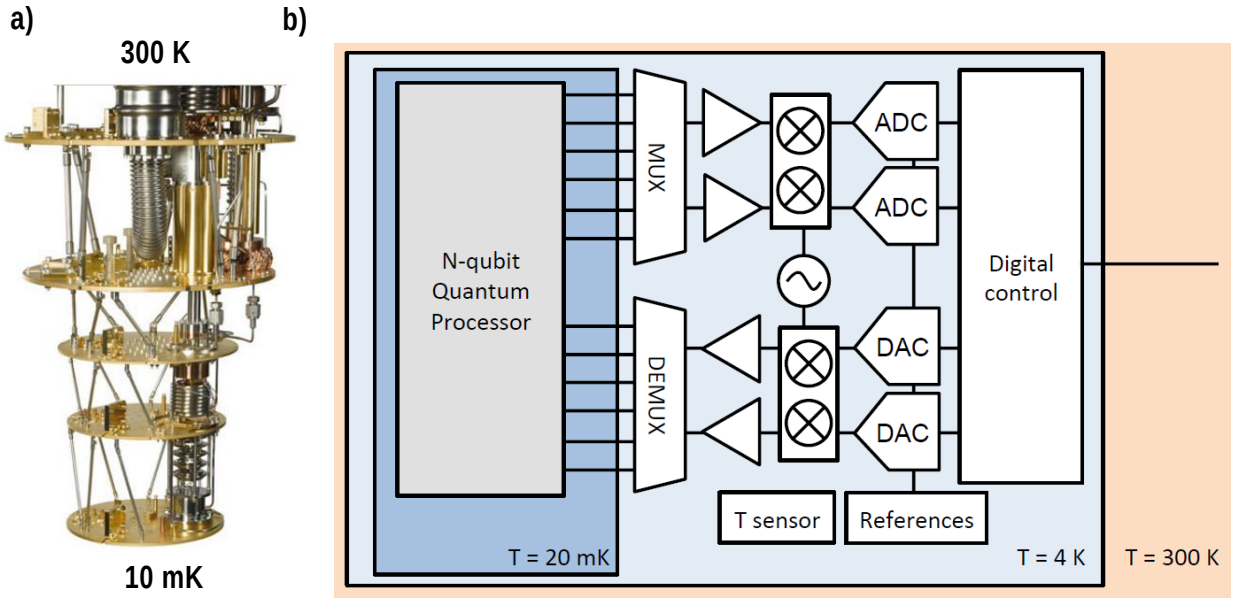


Figure 1.5 a) Dilution refrigerator [2]. b) A scalable quantum computer architecture [5].

Fig. 1.5-a shows a dilution refrigerator constituted by stages form base temperature (< 1 K) to room temperature. The height of the setup can reach up to 2 meters. From 1.5-a it is obvious that these setups

are not capable of handling Hundreds of qubits due to the huge wiring and electronic components required from base to room temperature over a length of a few meters. The idea is to move all the electronic components to cryogenic temperature and do all classical computation at low temperature and, ideally, pull out one data bus as an output of the computer. Fig. 1.5-b shows the concept of scalable quantum computer architecture. There are still discussions about choosing the right temperature (or even several temperature stages) for the operation of classical electronics. A practical quantum computer requires tens of qubits to perform useful computations, although already thirty qubits might be able to perform quantum system simulation [24]. Fig. 1.6 shows an estimation of the number of qubits required for certain applications.

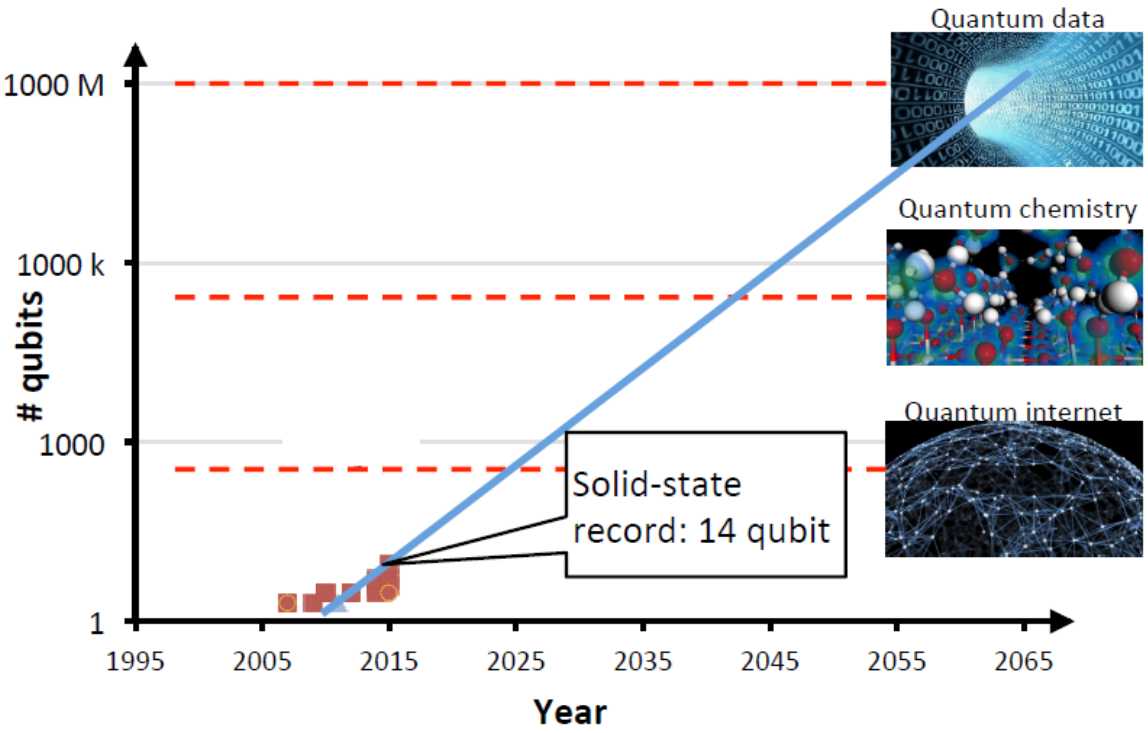


Figure 1.6 Estimated number of qubits for various application [5].

1.3 Cryogenic CMOS

While it is clear that classical controller for the quantum computer must operate at cryogenic temperature, what is the best electronic technology for the controller implementations? There exist several technologies which can be used to design electronic circuits operating at cryogenic temperatures, such as Single Electron Transistor (SET) [6] and superconducting devices like Rapid Single-Flux-Quantum (RSFQ) [26], Reciprocal Quantum Logic (RQL) [27], and Superconducting Quantum Interference Device (SQUID) [28]. However, in terms of scalability, design complexity, cost, and available CAD tools, those technologies still cannot compete with semiconductor devices.

Several cryogenic circuits have been designed using semiconductor devices, such as MOSFETs [29], HEMTs [18], and BJTs [15]. Table 1.2 shows a comparison between different semiconductors' minimum operational temperature. HEMT's high gain, high speed, excellent noise performance, and low power consumption make it a very good candidate for cryogenic electronic circuit design. However, the complexity and integration cost are major drawbacks in using HEMT in highly scalable circuits. On the contrary, BJTs show significant performance degradation below 100 K.

Device	Si BJT	Ge BJT	SiGe HBT	Si JFET	CMOS
Lowest functional temperature	100 K	20 K	4 K	40 K	20 mK
Limit	Low gain	Carrier freeze-out	?	Carrier freeze-out	No major limit

Table 1.2 Minimum operational temperature for different semiconductor devices [7].

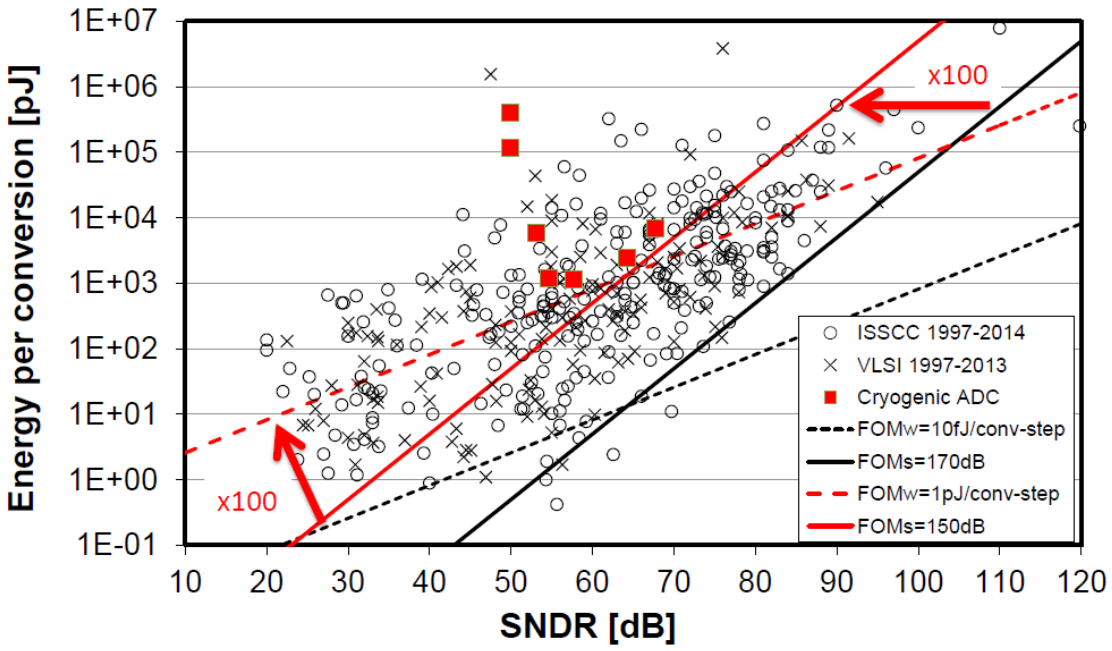


Figure 1.7 State-of-the-art ADCs at room temperature and cryogenic temperature. $FOMw = Energy/2^{(SNDR-1.76)/6.02}$, $FOMs = SNDR - 10\log_{10} 2 \times Energy$ **[7].**

Instead, standard CMOS has demonstrated operation well below 1 K. Moreover, CMOS is the best currently available technology in terms of scalability, being able to offer the integration of billions of devices on the same die. Although there have been some cryogenic CMOS designs, there is still a gap between the performance of those designs and the state-of-the-art at room temperature, which opens an interesting area of research. For instance, Fig. 1.7 compares the Figure-of-Merit (FOM) of different analog-to-digital converters (ADCs) designed for cryogenic application and state-of-the-art ADCs at room temperature.

1.4 Objective of This Work

Thanks to the considerable attention and financial support for developing quantum computers, it may be possible to have several stable qubits on the same chip in the near future; thus, classical electronics will soon be a big impediment against the scaling of quantum computers as mentioned above. With the currently available dilution refrigerators, the cooling power at 4.2 K is around 2.5W. Let us assume that we can use only 40% of the power consumption for reading out of the 1000 qubits. Thus, the maximum power consumption per each read-out channel would be 1mW. The objective of this thesi is to use standard CMOS at cryogenic temperature to design a low-power (<1mW) read-out circuit for a specific type of qubits, i.e. spin qubits.

1.5 Outline of the Thesis

The organization of this thesis is as follows. In chapter 2, the functionality of spin-qubits will be briefly reviewed and the electrical model of the qubit valid for the read-out will be introduced. Currently available read-out schemes will be presented and analyzed in terms of speed, power, and noise performance. Finally, the specifications for the design to be carried out in this thesis will be derived.

Chapter 3 focuses on the design of the proposed spin-qubit read-out circuit. First, the cryogenic behavior of CMOS devices and how to handle it in circuit design will be presented. The chapter continues discussing how to model CMOS devices at cryogenic temperatures. Afterward, analysis of the read-out circuit in terms of noise, power, gain, speed, and operation stability will be presented. Critical problems in the design and possible solutions are explained. The chapter ends by showing the layout of the circuit and the post-layout simulation results.

Since the circuit is going to be characterized at 4.2 K, enough care must be taken in designing the measurement setup. Chapter 4 describes the proposed experimental focusing on possible ways of applying input stimuli.

This thesis concludes with chapter 5, by proposing an outlook of the present work and improvements for the future.

2 Spin Qubit Read-out Techniques

This chapter analyzes spin qubits read-outs and, in particular, a system-level comparison between the two most commonly used techniques will be presented. Other possible read-out topologies will be discussed, and finally, the design specifications will be derived.

2.1 Electron Spin as a Qubit

The high coherence time demonstrated in solid-state spin qubits [24], along with their potential for scalability, make this type of qubits a good candidate for compact quantum processors. The spin of a single electron can be exploited in order to store quantum information (spin up or down). In order to be controlled and manipulated, single electrons need to be trapped in specific structures called “quantum dots”. A quantum dot (QD) implemented in GaAs is shown in Fig. 2.1-a. In such a structure, electrons are confined vertically thanks to the bandgap engineering of the heterostructure (the bandgap difference between GaAs and AlGaAs forms a 2-D electron gas (2-DEG) at their interface). Lateral confinement is achieved by applying negative voltages to the patterned gates on top of the semiconductor heterostructure in order to locally deplete the 2-DEG as shown in Fig. 2.1-a.

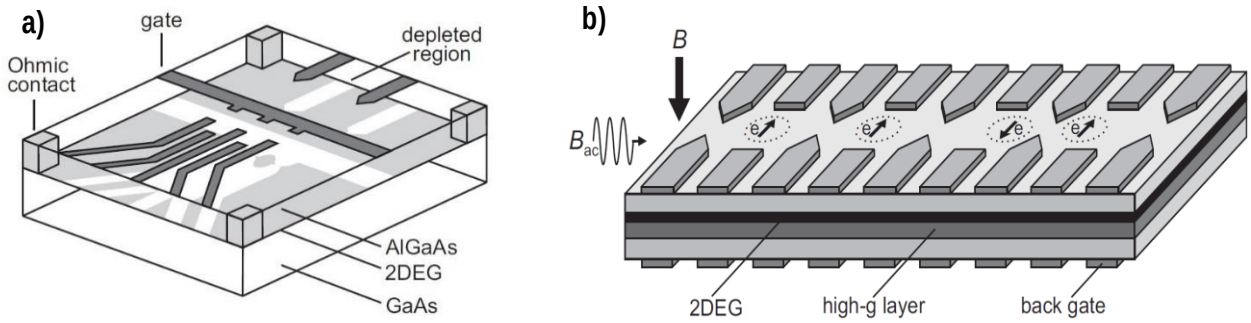


Figure 2.1 a) Schematic view of a lateral quantum dot device defined by metal surface electrodes. Negative voltages applied to metal gate electrodes (dark gray) lead to depleted regions (white) in the 2DEG (light gray). Ohmic contacts (light gray columns) enable bonding wires (not shown) to make electrical contact to the 2DEG reservoirs. b) Schematic picture of the electron spin quantum computer as proposed by Loss and DiVincenzo. The array of metal electrodes on top of a semiconductor heterostructure, containing a two-dimensional electron gas (2DEG) below the surface, defines a number of quantum dots (dotted circles), each holding a single electron spin (arrow). A magnetic field, B, induces a Zeeman splitting between the spin-up and spin-down states of each electron spin. The spin state is controlled either via an oscillating magnetic field or via an oscillating electric field created with the back gates. Coupling between two spins is controlled by changing the voltage on the electrodes between the two dots. Figure adapted from [20].

Since the energy level is extremely low, it is very difficult to differentiate the spin up and spin down states. To do so, by applying an external magnetic field, two sub-energy levels can be reached to host the spin up and spin down states at different energy level as shown in Fig. 2.2. This method is known as Zeeman splitting. It should be noted that the reason to maintain the qubits at a very low temperature (around tens of mK) is to keep the thermal energy of an electron well below of the difference between the energy level of these two sub-energy states, so as to prevent an electron to bounce from one energy level to the other one randomly. In order to control the electron spin, an oscillating magnetic field can be applied as shown in Fig. 2.1-b.

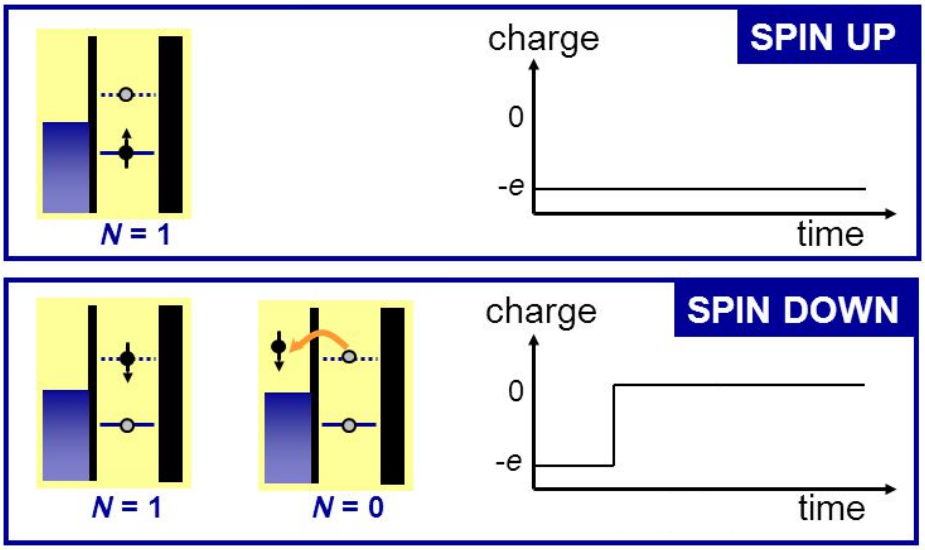
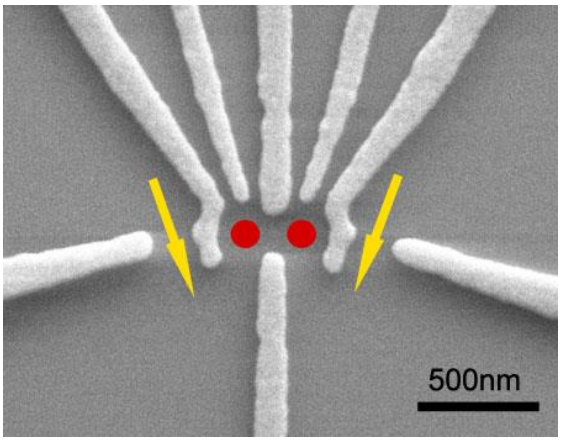


Figure 2.2 Spin to charge conversion. Zeeman splitting between spin up and spin down states. The spin down state doesn't have the enough energy to leave the dot [12].

2.2 Spin QUBIT Read-out

In order to detect the state of a qubit, one must be able to read out the magnetic field generated by the electron spin. By properly biasing the gates of the qubits, one can manipulate the energy levels such that electron with spin up doesn't have enough energy to tunnel through the potential barrier and leave the quantum dot. On the other hand, the electron with spin down can leave the quantum dot and enter the reservoir as it is shown in Fig. 2.2. To detect the charge variation due to the above changes, a quantum point contact (QPC) can be implemented next to the quantum dot as shown in Fig. 2.3-a.

a)



b)

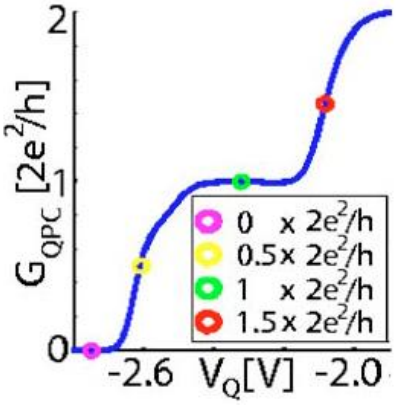


Figure 2.3 a) Double quantum dot structure [1]. b) QPC conductance versus gate voltage [18].

The charge variation can modulate the channel conductance of the QPC through the capacitive coupling, which is modeled as a variable conductance. Among the available measurement setups, RF-Reflectometry and Current-Readout techniques are the two mainly used approaches to reading this variable conductance.

The importance of the biasing of the QPC must not be overlooked; this creates a trade-off between the sensitivity of charge detection (sharpness of transition) and the maximum tolerable noise level on QPC terminals. Fig. 2.3-b shows a plot of the conductance versus gate voltage of QPC (green and pink circles correspond to the biasing points with better noise performance; yellow and red circles correspond to the points with more sensitivity to charge variation). As a result of such tradeoff, the QPC is normally biased with a gate voltage corresponding to the channel conductance that is about 0.7 times that of the quantum conductance [30].

In our setup (Delft spin-qubit), the QPC can be modeled with 25KΩ resistance in parallel with parasitic capacitances around 20pF (mostly due to the wiring from base temperature to 4 K). The variation of resistance is up to 1% due to the charge variation. The fixed bias voltage applied over drain-source of the QPC is around 180 μV; since higher voltage difference can cause a severe change in tunneling rate and causes the instability in dot occupation [18].

The Noise problem is another issue to be considered. As it was mentioned before the current amplitude is very small (in our setup it is 72pA RMS) and it can even be dominated by the noise of the QPC (assuming a noiseless read-out circuit) for higher bandwidths. The shot noise spectral density of the QPC can be derived from Eq. 2.1.

$$S_I = \frac{2e^2}{h} \sum N_i [eV_{QPC} \coth\left(\frac{eV_{QPC}}{2k_B T_e}\right) - 2k_B T_e], \qquad \text{Equation 2.1[18]}$$

where h is Planck constant, e the electron charge, $N_i = T_i\,(1- T_i)$ with T_i the QPC transmission coefficient of mode i (corresponds to the different biasing point of QPC shown in Fig. 2.3-b), V_{QPC} the bias over QPC, k_B the Boltzmann constant, and T_e the electron temperature.

From the Eq. 2.1 the integrated shot noise of the QPC (used in [18]) over 1MHz Bandwidth (which is the bandwidth of the currently available setup) is around 62pA RMS.

As it is mentioned briefly in the previous section, to perform a single-qubit rotation, one way is to apply two static (Zeeman splitting) and rotatory magnetic fields. Considering a spin as a vector in an x-y-z coordinate system shown in Fig. 2.4, under the static magnetic field B_0, the spin of the qubit rotates around the Z-axis with a frequency called Larmor frequency $\omega_0 = -\frac{g\mu}{\hbar}B_0$; where $g, \mu,$ and $\hbar$ are electron g-factor, Bohr magneton, and Dirac constant respectively.

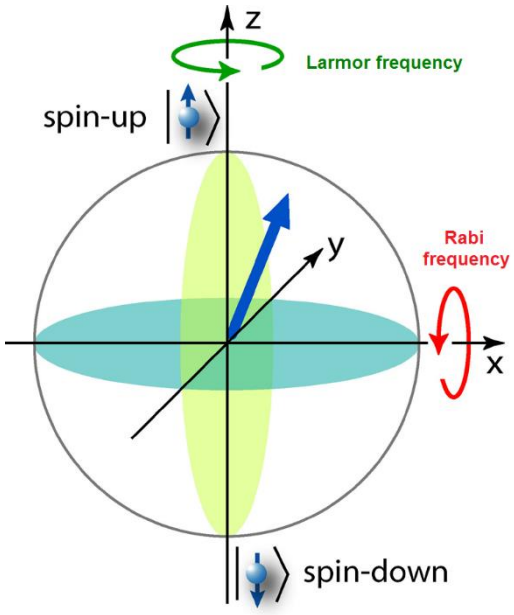


Figure 2.4 The electron spin state is represented by the bold arrow in the Bloch sphere (a geometrical representation of the pure state space of a 2-level quantum system). Pure spin-up and spin-down states are at the north and south poles of the Bloch sphere, respectively. The static magnetic field B_0 causes rotation about the z-axis, while the fast microwave pulse B_1 causes rotation about the x-axis [9].

By applying a rotating magnetic field B_1 (with a frequency ω_{mw}), it is possible to cancel the spin rotation (with Larmor frequency) if $\omega_{mw} = \omega_0$. Consequently, the spin starts to rotate around X- or Y-axis with a considerably lower frequency called Rabi frequency which is proportional to the magnitude of the applied rotating microwave pulse [9]. Table 2.1, and 2.2 show two examples for Rabi frequency and the required accuracy for microwave signal amplitude, frequency, and phase jitter.

The coherence time of the qubit, which defines the minimum speed of measurement can reach up to 100s of microseconds [31]. However, the accuracy requirement for practical purposes requires much faster measurement speed. Therefore, the goal of this design would be to reach 10 MHz bandwidth for the read-out circuit, which is roughly 3 times faster than the required time for the single qubit rotation in our setup which is around 100 ns.

So far, several electrical specifications for the QPC have been investigated. In the following paragraphs, the state-of-the-art implementation to read-out the qubits will be discussed.

	Nominal value	Inaccuracy	Noise
Microwave frequency	10 GHz	3.1 KHz	3.1 KHz_{rms}
Microwave amplitude	1.7 mV	3.4 μV	3.4 μV_{rms}
Microwave time	500 ns	1 ns	1 ns_{rms}

Table 2.1 Specifications for a Rabi Frequency of 1 MHz [9].

	Nominal value	Inaccuracy	Noise
Microwave frequency	10 GHz	3.1 KHz	31 KHz_{rms}
Microwave amplitude	17 mV	34 μV	34 μV_{rms}
Microwave time	50 ns	0.1 ns	0.1 ns_{rms}

Table 2.2 Specifications for a Rabi Frequency of 10 MHz [9].

2.2.1 RF-Reflectometry

In RF-Reflectometry read-out schemes, the QPC resistance is measured by measuring the reflection coefficient at the end of a transmission line connected to the QPC. A matching network is used to convert the impedance of the QPC to that of the coaxial cable used as transmission line (typically 50 Ω), as shown in Fig.2.5. An RF tone is injected into the coaxial cable through a directional coupler and its reflection coefficient is measured by a homodyne receiver. The matching network is designed for best matching for the nominal QPC impedance, i.e. when no electric charge change is detected. This results in a negligible reflected power. When the electron spin is up, the change in electric charge in the quantum dot capacitively coupled to the QPC causes a resistance variation. By measuring the reflected power due to the mismatch (as a result of conductance modulation), state change can be detected. Thanks to upconversion of the baseband signal to higher frequencies in RF-Reflectometry, it is possible to perform the read-out of several qubits using one read-out circuit [32] and applying frequency multiplexing as shown in Fig. 2.6.

The performance of RF-Reflectometry in terms of noise (charge sensitivity of $6 \times 10^{-4} e/\sqrt{Hz}$ at a bandwidth of 10MHz [33]) and bandwidth (tens of MHz [34]) is comparably better that other common

techniques. However, a directional coupler and a matching network per qubit are required, therefore limiting the applicability of the technique to large qubit arrays.

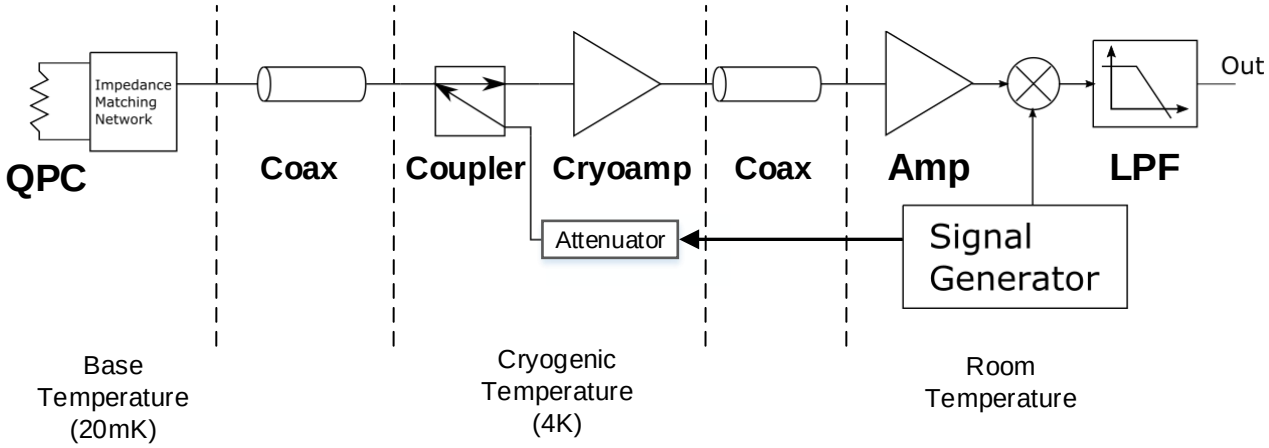


Figure 2.5 RF-Reflectometry read-out setup for spin qubit.

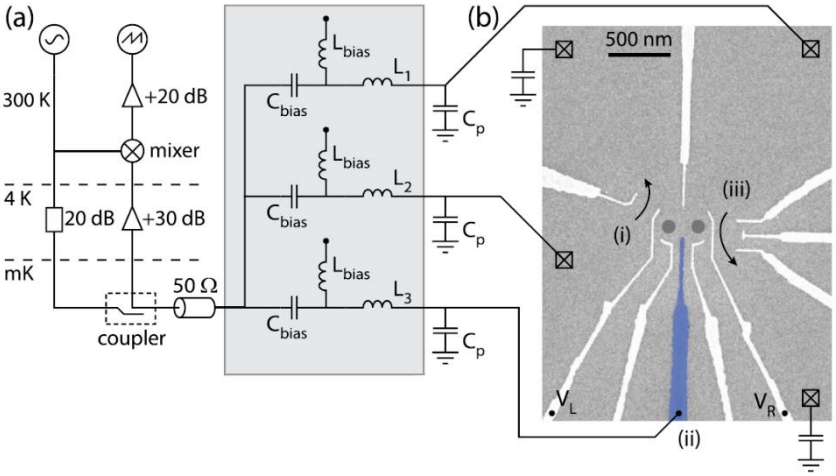


Figure 2.6 a) Three channel frequency multiplexing scheme for spin qubit read-out. b) Micrograph of the GaAs double dot device [16].

2.2.2 Current Read-out

Another commonly used method to perform QPC read-out is based on biasing the QPC with a constant voltage and reading current pulses through the QPC. Fig. 2.7 shows a typical Current-Readout setup being used to measure the QPC variation. In such an implementation there is a long cable from the qubit at base temperature (around 20mK) to room temperature which causes a large parasitic capacitance (up to 300pF [35]). Such a parasitic capacitance majorly degrades the noise performance of the circuit (as will be explained more in detail in chapter 3).

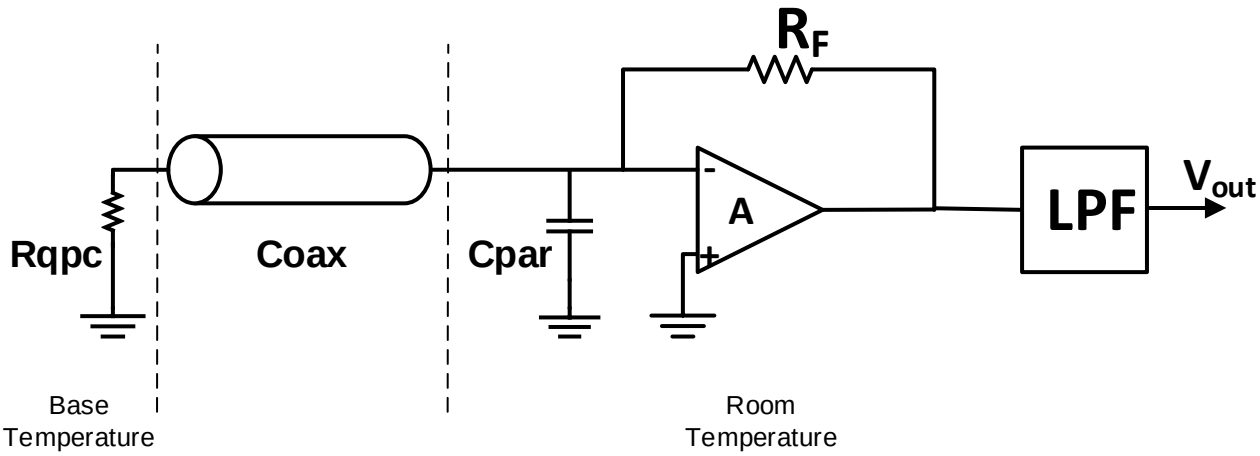


Figure 2.7 Schematic of current readout setup (TIA).

There is also the possibility to convert the current pulse onto a voltage through a resistor and to read out the voltage shown in Fig. 2.8. An example of this technique using a HEMT device as an amplifier is explained in [18]. The possibility of using HEMT at 4K in this implementation gives the opportunity to reduce the parasitic capacitance to 30pF.

The overall input-referred integrated noise of the circuit in this setup (1MHz bandwidth) is 146pA RMS; this confirms the fact that the signal is extremely noisy (in the setup mentioned in [18], for 1MHz bandwidth the RMS value of input current pulse is only 1.5 times higher than the 1-sigma input-referred RMS noise). Fig. 2.9-a shows the measured signal. Some edge detection algorithms (including some digital filtering) can be applied to improve the SNR of the measured signal as shown in Fig. 2.9-b.

In order to have a larger bandwidth in this topology, the resistor in parallel with parasitic capacitance (which defines a pole) must be small enough. On the other hand, voltage (or current) amplification and lesser noise contribution (due to R_i) in this topology requires larger resistance.

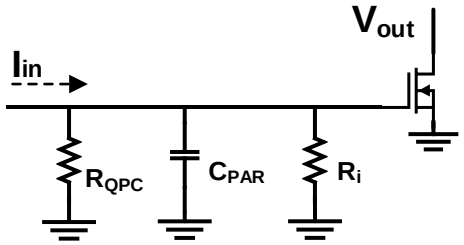


Figure 2.8 Current to voltage conversion readout.

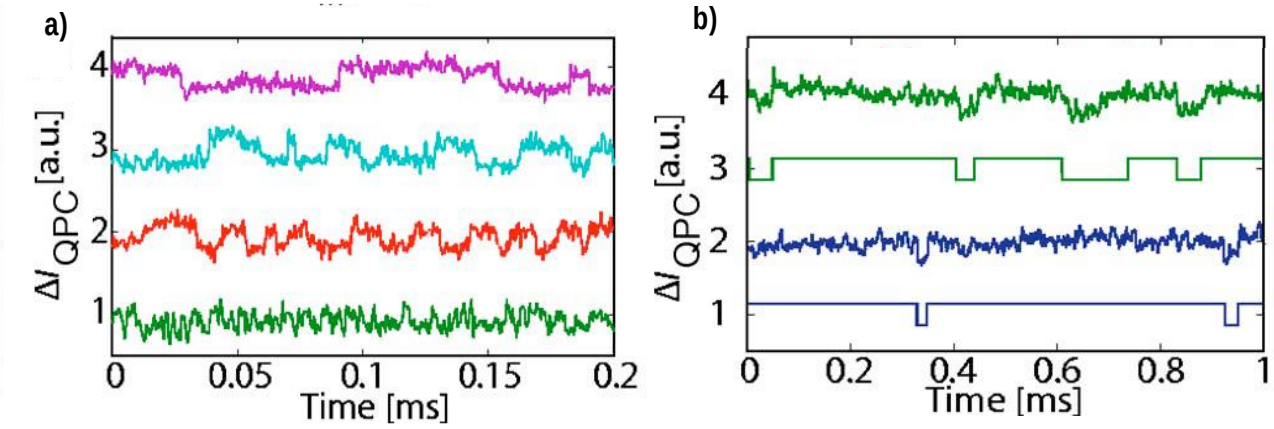
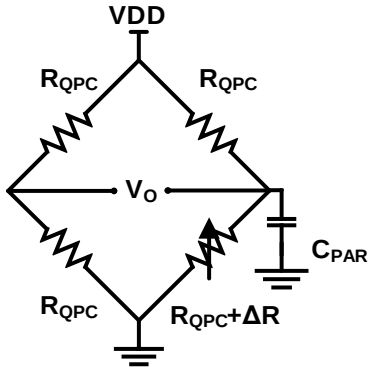


Figure 2.9 a) The tunneling rate is increased from top to bottom by decreasing the negative voltage on the gate of QPC. Here, the signal was band-pass filtered from 3 kHz to 1 MHz. The shortest detectable events are on the order of 400 ns. b) Measured QPC current when increasing the dot potential from top to bottom. An additional band-pass filter (200 Hz–200 kHz) was used for this measurement [18].

Another way is to use the Wheatstone-Bridge configuration as shown in Fig. 2.10. However, due to the large value of the QPC resistance in parallel with the parasitic capacitances (because of the wiring from base temperature to room temperature, parasitic of the following stages, and packaging), the bandwidth is limited.



$$V_O = \frac{VDD}{4} \times \frac{\Delta R}{R_{QPC}+\Delta R/2} \quad \left(f \ll \frac{1}{2\pi R_{QPC} C_{PAR}}\right) \qquad \text{Equation 2.1}$$

Figure 2.10 Wheatstone-Bridge read-out topology.

So far, these setups are made up of discrete components that require large area, which makes these solution unsuitable for measurement of tens of qubits on the same chip. Furthermore, the available setups are not fast enough, thus preventing the read-out of large numbers of qubits within their coherence times. The goal of this thesis is to design an integrated, high bandwidth, and low noise Current-Readout chip operating at cryogenic temperatures.

2.3 Fast, Low Noise Current Read-out

To solve the bandwidth problem, we need a very low input impedance read-out circuit. Fig. 2.7 shows a transimpedance amplifier structure. The input impedance of this circuit is defined by the feedback resistor divided by the gain of the OTA. Therefore, by adopting high OTA gain and a small enough feedback resistor, very low input impedance can be obtained. On the contrary, to have enough output swing and less contribution to the overall noise, large values of R_F are required, which cannot be implemented with a metal resistor because of low sheet resistance. The poly resistor is a possible candidate but it suffers from parasitic capacitance, which makes it difficult to keep the bandwidth of the TIA high.

Let us assume 500 MΩ resistor is adopted for R_F, and 500 Ω input impedance is required. As a result, the gain of the amplifier shown in Fig. 2.7 ("A") must be at least 120 dB, which is hard to achieve. There is a possibility to replace the resistor in the feedback path with a transistor biased in a triode region. There are two main problems with such a solution; first of all, controlling the value of such a resistance is difficult due to the inaccuracy of the applied voltage to the gate and the deviation of transistor parameters over process variation. Another problem is the noise contribution of the externally applied bias voltage to the gate of the transistor in overall noise performance; digitally tuning of the circuit might help the noise issue but it requires a very high-resolution DAC to provide an accurate enough value for the feedback resistor.

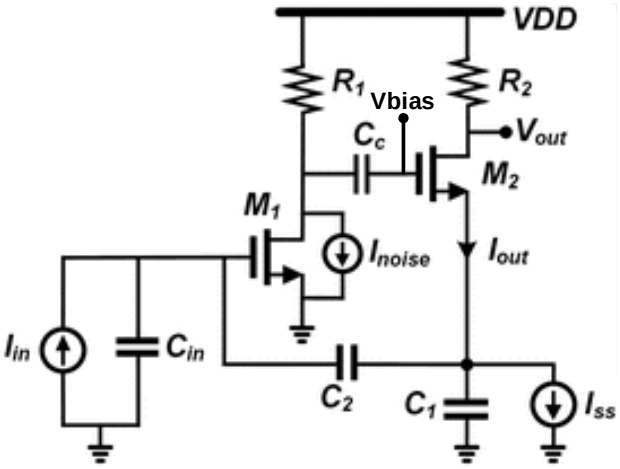


Figure 2.11 Capacitive feedback transimpedance amplifier [10].

$$CTIA\ gain = \frac{V_{out}}{I_{in}} = \frac{R_2 \times \frac{g_{m1}R_1(C_1+C_2)+C_2}{g_{m1}R_1C_2+C_2+C_{in}}}{1+\frac{S(C_1C_{in}+C_1C_2+C_2C_{in})}{g_{m2}(g_{m1}R_1C_2+C_2+C_{in})}} \approx R_2 \times (1+\frac{C_1}{C_2}) \quad \text{(Low frequencies)} \quad \text{Equation 2.2-a}$$

$$f_{-3dB} \approx \frac{(1+g_{m1}R_1)\times g_{m2}}{2\pi \times C_1} \quad \text{Equation 2.2-b}$$

Fig. 2.11 shows a Capacitive Feedback Transimpedance Amplifier (CTIA) topology which is being used for optical communication applications up to 2.5 GHz [10]. Eq. 2.2-a shows that the CTIA gain is defined by the value of R_2 and the ratio of C_1 and C_2; large C_1 can drop the bandwidth of the circuit based on Eq. 2.2-b. For instance, to have 500 MΩ of CTIA gain (assuming C_1=2 pF and C_2=0.5 pF), R_2 must be equal to 100 MΩ. If M_2 is biased with 5 nA (considering g_{M2}=20 $|I_{M2}|$=100 n℧), the bandwidth would be around 200 KHz (considering $g_{M1}R_1$=25). Lack of DC path for the input current is another problem of this structure (adding DC path increases the input parasitics and design complexity).

The topology shown in Fig. 2.12, which can provide high transimpedance gain and bandwidth, and that can be directly connected to the QPC without any extra DC path. The input impedance of this circuit is calculated in Eq. 2.3 and can be designed to be very low, so as to maintain the high bandwidth and to sink all the current from QPC. By biasing the Ibias with low bias current, it can provide large resistive gain. On the other hand, small biasing current in Ibias branch reduces the noise contribution of that branch. More extensive study of the circuit and improvements are presented in the next chapter.

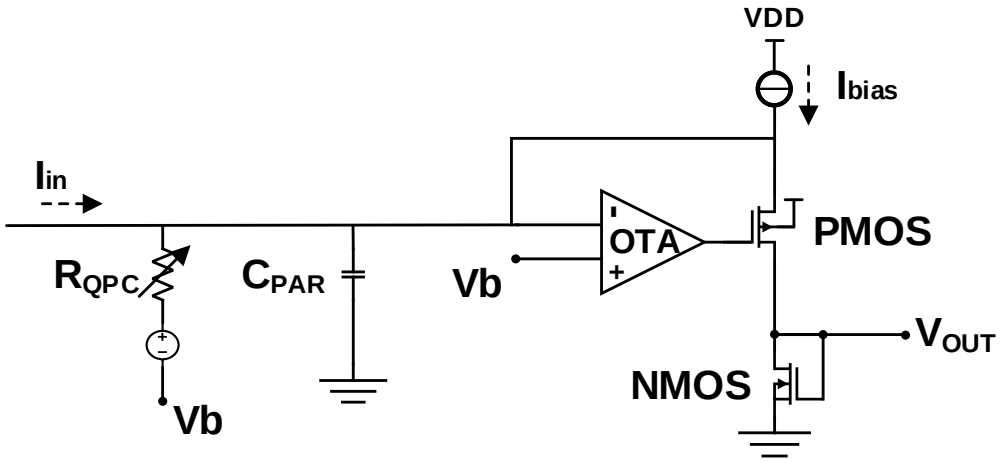


Figure 2.12 g_m-boosted transimpedance amplifier.

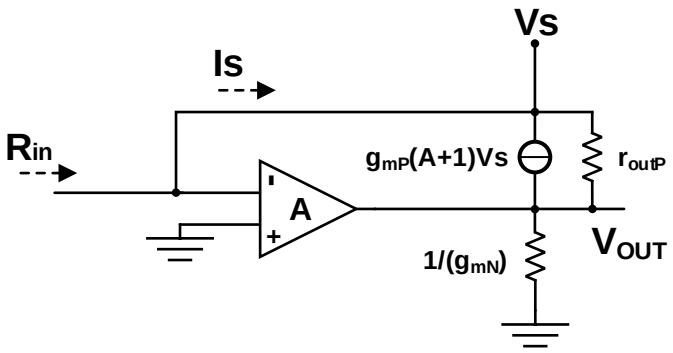


Figure 2.13 Small signal equivalent of g_m-boosted transimpedance amplifier shown in Fig. 2.8.

Kcl @ node V_S : $$\frac{V_s-\frac{I_S}{g_{mN}}}{r_{outP}} + g_{mP} \times (A+1) \times V_s = I_S$$ Equation 2.3-a

$R_{in} = V_S/I_S$: $$R_{in} \approx \frac{1}{g_{mP} \times (A+1)}$$ Equation 2.3-b

A general problem which can be seen in all current read-out topologies, discussed so far, is the effect of the input parasitic capacitances on the noise performance of the circuit [36]. Input parasitic capacitances generate a zero in the input-referred noise transfer function of the OTA and increases the contribution of the integrated noise of the OTA in the overall noise performance of the circuit; this is one of the most important reasons for us to move the read-out circuit to cryogenic temperature (closer to the QPC to reduce the wire parasitic capacitances). More extensive noise analysis is presented in section 3.4.

2.4 Design specifications

Based on the cooling power limitation and what has been discussed so far, we can derive and summarize the specifications of our design.

Regarding the noise specification, as mentioned before, the noise floor of the currently available setup is $0.25 \times 10^{-25}\ {}^{A^2}/_{Hz}$. The goal of this design is to reach the same noise floor while achieving 10 times of higher bandwidth.

In order to measure the noise spectrum of the designed chip, the input-referred noise level of the measurement setup which is mainly due the matching LNA followed by the output stage of the read-out circuit (explained in chapter 4) must be below the input-referred noise floor of the designed circuit itself; otherwise, the noise of the measurement instrument will dominate the noise floor and makes it impossible to characterize the noise performance of the IC. This specification defines a TIA minimum gain (equivalent impedance of the whole TIA) as shown in Eq. 2.4.

$$I_{noise-input-reffered-measurment\ setup} = \frac{V_{noise-measurment-setup}}{TIA\ Gain(impedance)} \qquad \text{Equation 2.4}$$

From the matching LNA datasheet [3] which will be placed in our PCB, we can say the minimum noise level of our measurement setup is 2 $^{nV}/_{\sqrt{Hz}}$. Assuming the input pair transistors of the OTA shown in Fig. 2.8 are the main noise sources (it is explained in section 3.4) and they are biased with 200uA; Eq. 3.5 shows how the noise sources of the OTA appear at the input of the circuit. Now we can divide the integrated noise of the measurement setup over the required bandwidth (10MHz) by the input-referred noise of the OTA and roughly calculate the minimum TIA gain required to prevent the noise of the measurement setup dominates the noise floor of the circuit (an extra factor 10 is considered as safety margin for minimum required TIA gain). The upper limit for TIA gain can be calculated in order to avoid the saturation of the output stages.

As it is mentioned before, the input capacitance degrades the noise performance of the circuit. The final goal of this design is the integration of the read-out circuit and qubit at either 4.2 K or base temperature. However, as a short-term goal, this chip must be able to work with the currently available setup, which requires an interconnection wire from base temperature to 4.2 K, resulting in a large parasitic capacitance at the input of the circuit. Therefore, this chip must be able to handle a range of input capacitances from 2.5 pF to 20 pF maintaining stability. Table 2.1 shows a summary of all the specifications. In the first prototype the operating temperature of the designed chip is 4.2K. Later, we will be able to use more advanced cooling systems to decrease temperature further, if required.

Design specification	Value
Maximum power consumption per channel	1 mW
Minimum bandwidth	10 MHz
Input-referred integrated noise (up to 1 MHz BW , for 20pF input capacitance)	<150 pA RMS
Input parasitic capacitance range	2.5 pF to 20 pF
Amplitude of input signal	72 pA RMS
Minimum TIA gain	> 3 MΩ
Maximum TIA gain (To avoid output saturation)	< 500 MΩ
Voltage fluctuation on QPC terminal (kick-back noise in RMS up to 1GHz)	< 180 µV
Adopted technology	SSMC 0.16-um CMOS

Table 2.3 Design specifications for the cryogenic DC-Readout circuit.

3 Cryogenic Modelling and Circuit Implementation

In the previous chapter, the design specifications have been presented and several read-out topologies have been investigated. This chapter focuses on the circuit level implementation of the proposed read-out. First, the characterization and modeling of standard CMOS at cryogenic temperature for design and simulation purpose will be described. Then, specific design challenges, and possible solutions will be discussed.

3.1 CMOS Characterization at 4.2 K

Before going to the circuit level implementation, a proper model for the transistors is required. The modeling of CMOS transistors at cryogenic temperature was made possible by the availability of cryogenic characterization of several NMOS and PMOS transistors with different sizes (shown in Table 3.1 and Table 3.2) in the technology chosen for the circuit implementation (SSMC 0.16-um CMOS). The modelling of only those transistors would be sufficient because any arbitrary transistor sizes used in the circuit design will be implemented by combining these transistors in series or parallel. To derive the small signal parameters of a transistor, DC characteristic curves of the transistor are required.

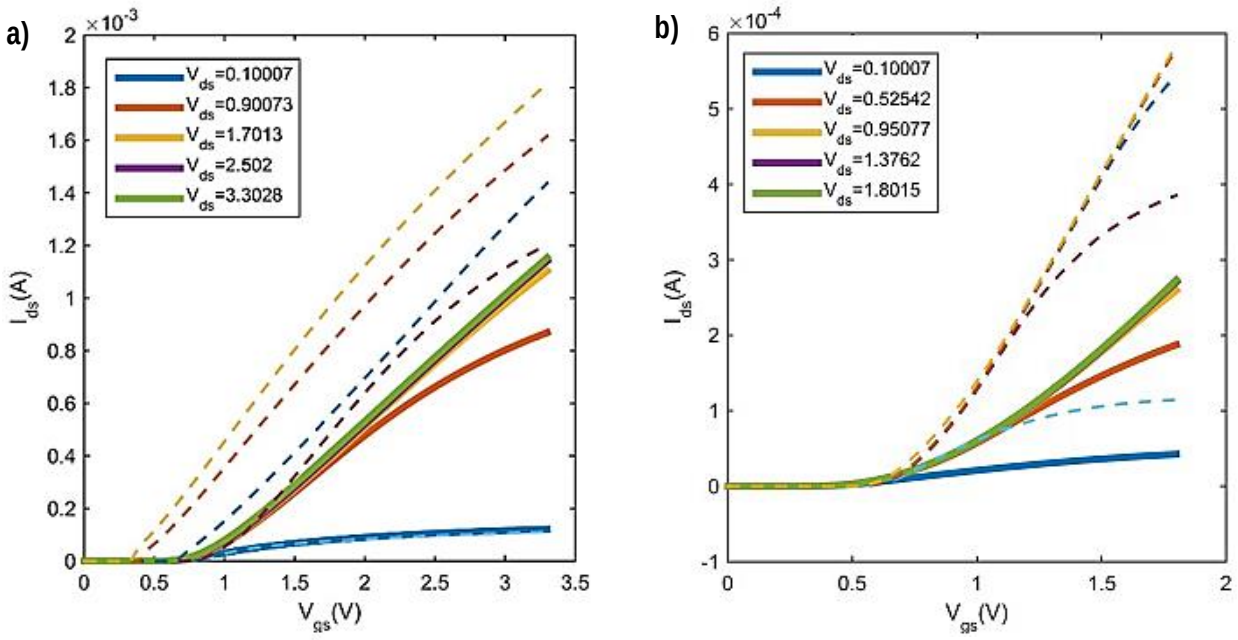


Figure 3.1. $I_{ds} - V_{gs}$ curves for: a) Short-Short thick-oxide NMOS transistor. b) Short-Short thin-oxide NMOS transistor (dashed lines and the solid lines measured @ 4.2 K @ 300 K respectively for 5 different drain-source voltages. The adopted technology is SSMC 0.16-um) [15].

W(um) / L(um)	2.32	0.232
1.6	Long-Long	Long-Short
0.16	Short -Long	Short-Short

Table 3.2 Measured transistors' dimensions (Thin-oxide devices).

W(um) / L(um)	2	0.4
1.61	Long-Long	Long-Short
0.322	Short -Long	Short-Short

Table 3.1 Measured transistors' dimensions (Thick-oxide devices).

Fig. 3.1, and Fig. 3.2 show the DC curves for one transistor at different biasing points measured at room temperature (300 K) and 4.2 K. From Fig. 3.1 the shift in threshold voltage and in transconductance can be seen by comparing the solid lines (measurements at 300 K) and the corresponding dashed lines (measurements at 4.2 K [15]). Fig. 3.2 shows the increase of the current and reduction of the output impedance (for higher drain-source voltages) at 4.2 K.

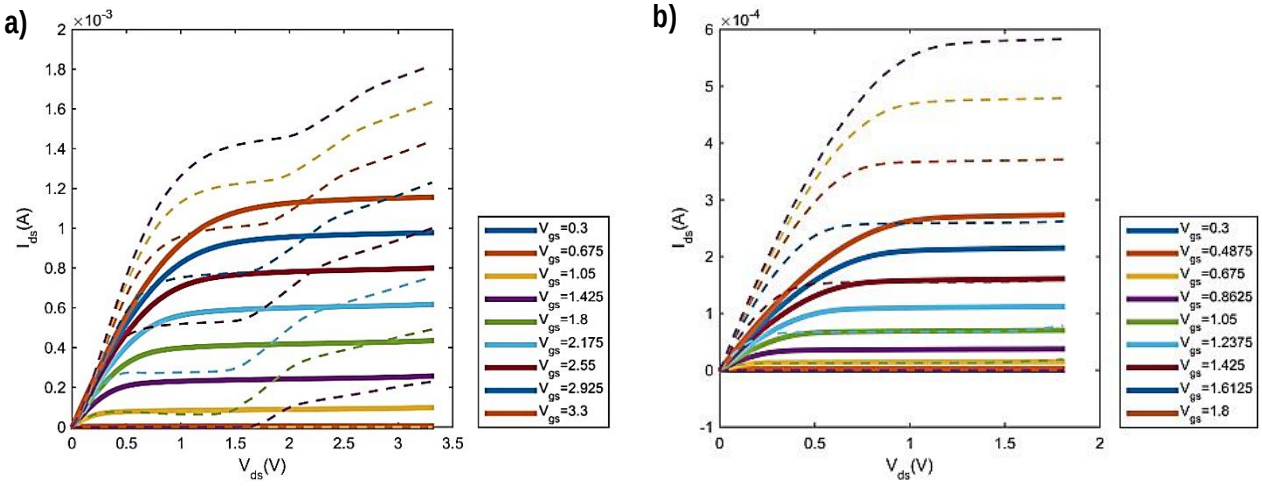


Figure 3.2 $I_{ds} - V_{ds}$ measurement curves for a) Short-Short thick-oxide NMOS transistor, and b) Short-Short thin-oxide NMOS transistor (dashed lines and the solid lines measured @ 4.2K and @ 300K respectively for 5 different drain-source voltages. The adopted technology is SSMC 0.16-um) [15].

3.1.1 Mobility variation over temperature

The carrier mobility is known to be related to scattering mechanisms [37]. Due to the temperature dependence of scattering phenomena, the mobility is also temperature dependent. There are several scattering mechanisms, like phonon scattering due to silicon lattice vibration, surface scattering due to imperfections at Si-SiO2 interface, Coulomb scattering (a similar effect to surface scattering), etc. A more thorough description of these phenomena is outside the scope of this thesis, however Fig. 3.3 shows the temperature dependence of mobility over temperature in which it is dominated by phonon scattering at higher temperature and limited by Coulomb and surface scattering at lower temperature.

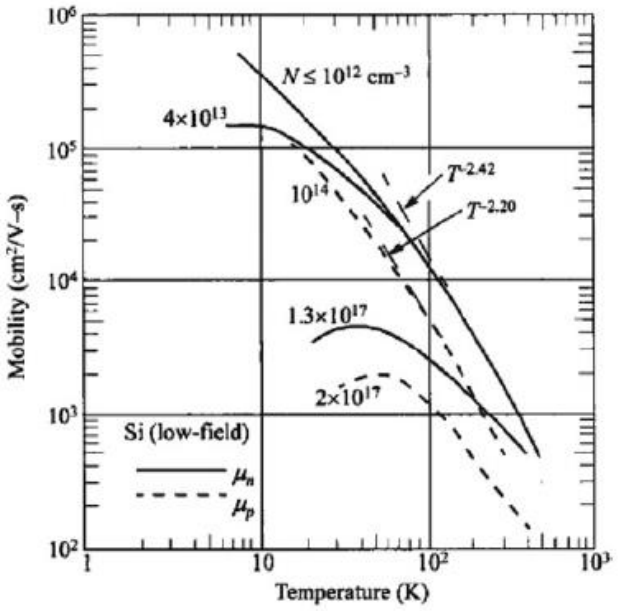


Figure 3.3 Temperature dependance of mobility, the dashed lines represent for holes, and the solid lines represent electrons [13].

3.1.2 Threshold voltage temperature dependency

Another temperature dependent parameter in MOSFET is the threshold. Roughly speaking, carriers must have enough kinetic energy in order to create a channel in MOSFET devices. By reducing temperature we need to apply stronger field to compensate for the reduced kinetic energy of carriers. The temperature dependency of threshold voltage is shown in Fig. 3.4.

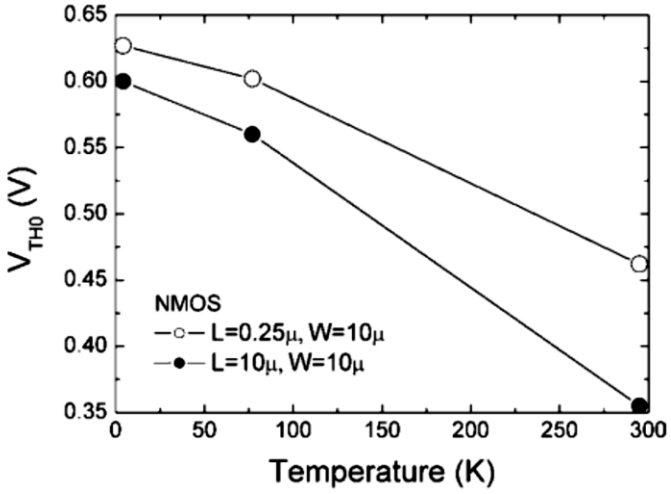


Figure 3.4 Temperature dependence of threshold voltage of NMOS at temperature of 300K, 77K and 4K [14].

3.1.3 Hysteresis and Kink Effect

On top of the increase in transistors current and threshold voltage, transistors at cryogenic temperatures may show hysteresis in their output characteristics, i.e. different current when V_{DS} is increasing or decreasing. The origin of this effect can be related to the different time required for the formation and disappearance of the depletion layer in forward and backward sweep, respectively [38]. If the sweep is done in an infinite amount of time, this effect vanishes. Our models ignore this effect, since it does not appear to be relevant in the adopted technology.

Another effect that emerges at cryogenic temperature is a current kink [39], i.e. the quick increase of the drain current for higher V_{DS} shown in Fig. 3.2. This increase of current has a different cause than the increase in carrier mobility at a lower temperature. A body current is generated at large V_{DS} due to impact ionization. At the same time, due to the freeze-out of the substrate, the substrate resistance increases dramatically. As a result of the body potential increases due to the body current flowing through substrate, the threshold voltage drops and an increase in drain current appears. The body potential continues to increase until the body-source diode turns on and stops the body potential increase and the threshold voltage drop [15]; therefore the drain current will be saturated again. In our circuit design, we are trying to avoid regions with such a high V_{DS} (to skip the kink effect). Moreover, the kink effect is much less evident in thin-oxide devices (which has been exploited in this design) comparing to thick-oxide devices [15].

3.1.4 Transistor Parameters at 4.2 K

Reliable AC circuit simulations require proper modeling of small signal parameters. As it can be seen from Fig. 3.1 and Fig. 3.2, the I_D-V_{GS} and I_D-V_{DS} curves have different slopes at room temperature with respect to a cryogenic temperature which means different transconductance and output resistance. Unfortunately, with the available cryogenic measurement setups and available test structures, it was not feasible to derive information about noise, mismatch, and capacitive parasitics. Therefore, a proper margin must be taken into account in designing for a required noise performance.

According to literature, the parasitic capacitances decreases by a factor from 2x to 4x at 4.2 K compared to room temperature (300 K) [4], [38]. Also, the thermal noise is reducing linearly with absolute temperature. On the contrary, the flicker noise and mismatch (as shown in Fig. 3.5) is getting worse at deep cryogenic temperatures [40], [41]. More detailed noise analysis is presented in section 3.4.

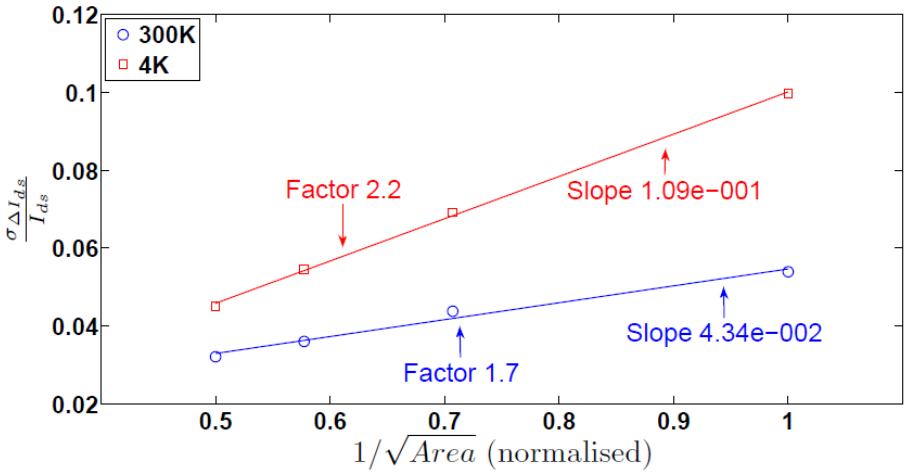


Figure 3.5 NMOS (0.35µm PD-SOI CMOS) drain current mismatch: Ids= 0.5µA, Vds= 0.3V [6].

3.2 Modelling of CMOS for Circuit Simulation at 4.2 K

The change in transistor biasing point and other parameters at 4.2 K degrades the performance of circuits designed for room temperature applications and can even make them non-functional. Therefore, a proper modeling of transistors at 4.2 K is required. Based on the measurement results, several approaches has been exploited to reproduce the same curves in the simulator in order to derive the right values for small signal parameters. The first strategy used to model the transistors was to use the Matlab curve fitting tool and import the characterization data in Cadence Virtuoso as Verilog-A model (Polynomial model for the curves) for each transistor.

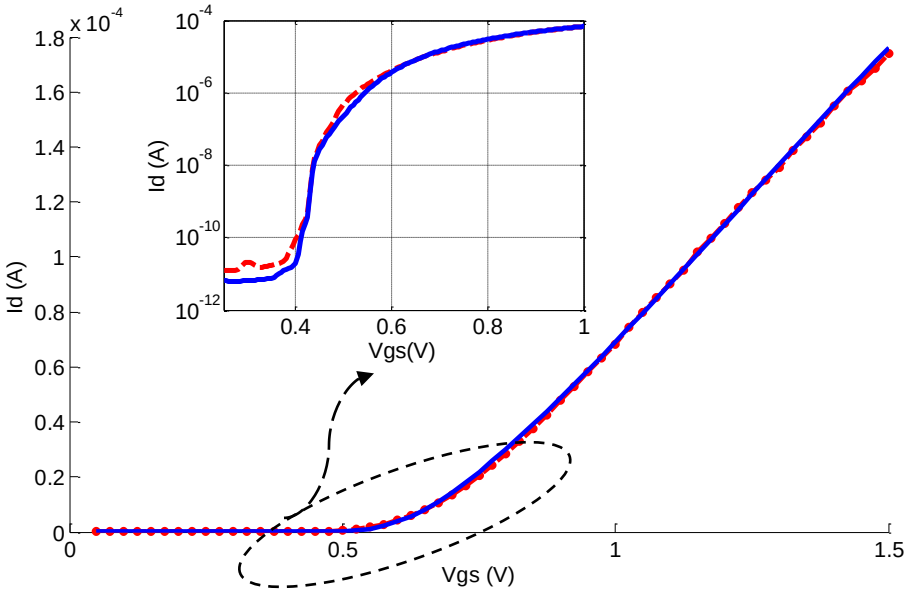


Figure 3.6 Fitted $I_{ds} - V_{gs}$ curves VS measurement data (red dashed line) for Long-Short thin-oxide devices.

The problem of this technique is that still there are some sharp transitions in the simulated curves (due to fitting accuracy and a limited number of measured points), which can create a discontinuity in the derivatives of the curves and cause convergence problems in simulations, especially for larger circuits. Another method is to use IC-CAP device modeling software to extract the new parameter based on the measurements at 4.2 K. However, the resulting curves were not satisfying due to the considerable differences between the measured parameters and the fitted curves.

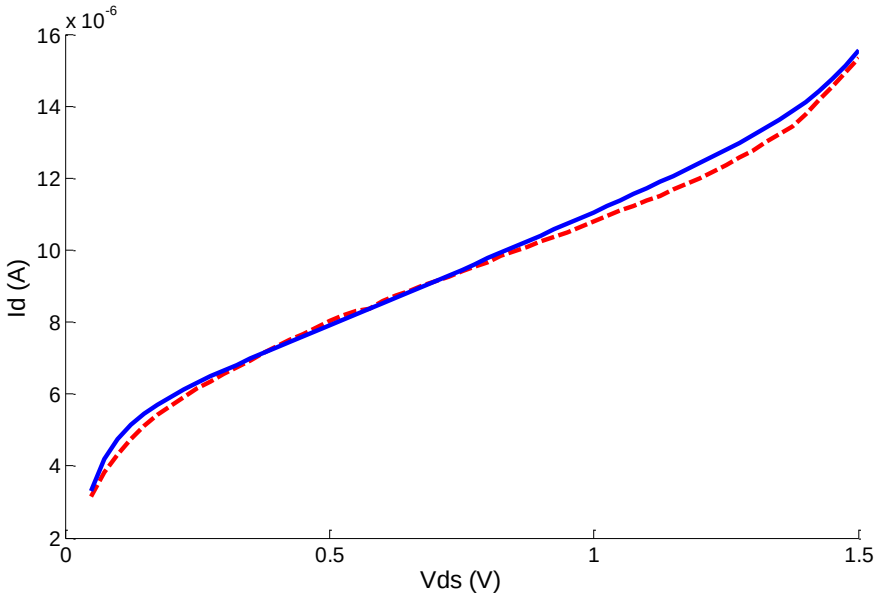


Figure 3.7. Fitted $I_{ds} - V_{ds}$ curves VS measurement data (red dashed line) for Long-Short thin-oxide devices.

An idea to solve the smoothness problem of the curves is to use the original transistors model (MOS model 11 in the adopted 0.16-um technology) and modify them in order to fit them into the measured curves. The parameters including “slphib”, “fbet1”, “betsqr”, “alpr”, “tr”, “vfb”, and “ssfr” have been modified mainly to increase the threshold voltage (V_{TH}), the gm of transistors, and to reduce the output resistance. Fig 3.6, and Fig. 3.7 show the fitted curves for one of the measured transistors. The same procedure has been applied to other transistors mentioned in Table 3.1 in order to use them in circuit design. More detailed information about these parameters can be found in NXP MOS Model 11 manual. To see the values adopted for the above-mentioned parameters in the modified library see the appendix A.

3.3 Circuit Level Implementation of the Read-out

After analyzing several possible techniques for resistance read-out in chapter 2 that can satisfy the specifications in section 2.3, the circuit shown in Fig. 3.8 has been chosen. It is and improved version of the circuit shown in Fig. 2.12 optimized for wider signal bandwidth. Its advantages are its low input impedance (required for high bandwidth), good noise performance (dominated by the OTA), and no need for an extra DC current path at the input.

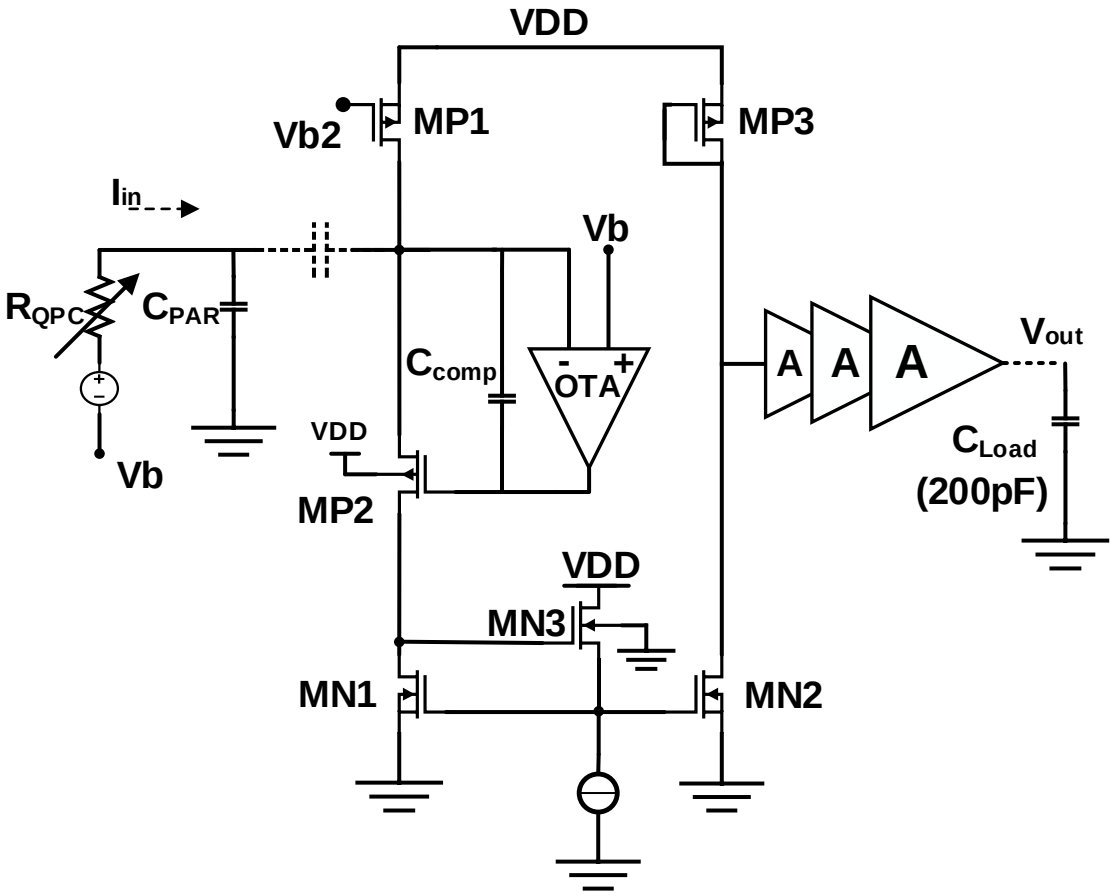


Figure 3.8. Circuit level implementation of the read-out structure.

The first point which must be taken into account in designing of this circuit is to keep the input impedance of the circuit low enough in order to keep the bandwidth high. The input impedance in parallel with the input parasitic (wire, pads, OTA, and etc.) as shown in Fig. 2.13 creates a pole which can limit the bandwidth. The input current sunk by the low input impedance TIA is converted to a voltage through diode connected MN1 (transistor MN3 is added to push the pole at the gate node of MN1 to higher frequencies as explained in Eq. 3.1). To satisfy the specification on the TIA gain, the voltage at the gate of MN3is amplified by MN2 and MP3 and by 9 cascaded stages. Those stages are designed to amplify the voltage and to increase the driving factor of the circuit to be able to drive the 200 pF output load (due to the wire from 4.2 K to 300 K) without losing the significant bandwidth, as explained in section 3.6.

3.3.1 Sizing of Current to Voltage Converter

Eq. 3.1-c shows that by adding the transistor MN3, the pole at gate node of MN1 is moved from $[\, g_{mMN1}/C_{gsMN1}]$ to $[g_{mMN1} \times r_{outMN1} \times g_{mMN3}/C_{gsMN1}]$. On the other hand, transistor MN3 generates a zero (shown in Eq. 3.1-c) in the transfer function of impedance seen from the drain of transistor MN1 which can creates stability issues; therefore, proper sizing and biasing of MN3 is very important. Consequently, to increase the phase margin of the loop (including MN1, and MN3) a capacitor bank is placed in parallel with drain-source of transistor MN1.

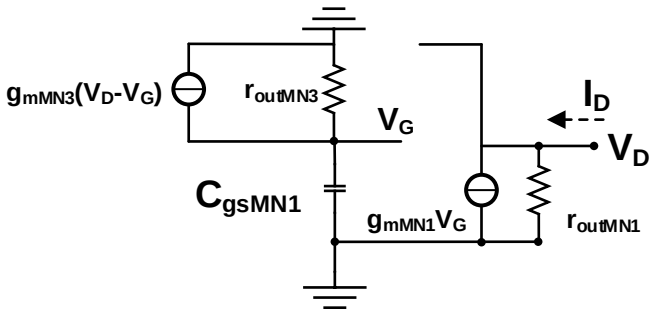


Figure 3.9 Small-signal equivalent of transistors MN1 and MN3 shown in Fig. 3.8 (CgsMN1 includes all the parasitics seen at the gate node of MN1 and MN2).

Kcl @ node V_D: $\frac{V_G}{r_{outMN3}} + C_{gsMN1}sV_G = g_{mMN3} \times (V_D - V_G).$ Equation 3.1-a

Kcl @ node V_G: $I_D = g_{mMN1}V_G + \frac{V_D}{r_{outMN1}}$ Equation 3.1-b

After calculating V_G from Eq. 3.1-a and replacing it in Eq. 3.1-b:

$$R_t = \frac{V_D}{I_D} \approx \frac{r_{outMN3} \times (r_{outMN3} \times g_{mMN3} + sC_{gsMN1} \times r_{outMN3})}{g_{mMN1} \times r_{outMN1} \times g_{mMN3} \times r_{outMN3} + sC_{gsMN1} \times r_{outMN3}}$$

$(r_{outMN1}, r_{outMN3} \gg 1)$; Equation 3.1-c

One more point to be mentioned is the AC coupling capacitor shown with the dashed line at the input of the circuit in Fig. 3.8. When connecting the circuit to a real QPC, as mentioned in chapter 2, there must be a DC current path. However, in our first measurements, we might not be able to use a real QPC. Therefore, we need to generate extremely small current pulses (which is explained in chapter 4) to

characterize the chip. Consequently, this AC coupling capacitor is required to isolate DC and AC signal paths.

The input impedance is defined by the gain of the OTA block and the transconductance of MP2 as explained in Eq. 2.3. The biasing current of MP2 is chosen to be 100nA in order to reduce the noise contribution of MN1 and MP1 (discussed in next section) and to keep the bandwidth above 10MHz; considering the 20pF input capacitance, to maintain a 10MHz bandwidth, the input impedance of the TIA must be less than 796Ω. Therefore, based on Eq. 2.3 (and assuming $g_{MP2} = 10 \times I_{MP2}$) the gain of the OTA must be higher than 62dB.

The second issue is the stability of the OTA-MP2 loop which is discussed in section 3.5. Noise performance is another important matter that imposes stringent limitations on designing the circuit, especially the OTA. The noise performance of the circuit will be explained extensively in the next section.

Despite of the comprehensive noise analysis presented in section 3.4 there is still some uncertainty about the device noise at cryogenic temperature (especially flicker noise at 4.2 K) which led to make the gain of the output stages variable (4 out of 9 cascaded stages mentioned in section 3.6 are variable gain stages) in order to avoid saturation of the TIA due to excessive noise. In the following section, all the above-mentioned issues will be addressed.

3.4 Noise Performance of the Circuit

For the sake of investigating the noise contribution of each component and to compare it with the input signal, the input-referred current noise (RMS) contribution of each transistor is calculated. MN1, MP1 and the OTA shown in Fig. 3.8 are found to be the most dominant noise sources. In order to attenuate the noise contribution of the cascaded gain stages, a large mirroring factor (1:25) is chosen between transistors MN1 and MN2. A larger ratio is not desired because it could reduce the desired bandwidth due to the large gate-source parasitic capacitance of MN2.

The noise sources of MN1, MP1, and MP2 can be modeled as parallel current sources connected to the transistor's drain and source. A simplified circuit for the calculation of the noise due to MP2 is shown in Fig.3.10. The input referred noise is derived in Eq. 3.2, showing that the noise contribution of MP2 is negligible at low frequency. However, at high frequencies it might become significant due to the zero in the transfer function. In order to reduce the noise contribution of MP1 shown in Fig. 3.8, a large length over width (L/W) is chosen to decrease the transconductance of MP1 (current noise spectral density, $S_{In} = 4KT\gamma g_m$). The larger area of MP1 also reduces its flicker noise contribution. Sizing of transistor MN1 is more critical. As it will be discussed in the next section, the flicker noise is the dominant noise source at 4.2 K; considering the fact that, a larger size of MN1 is preferable. On the other hand, the second critical pole which limits the speed of the circuit is located at the gate node of transistor MN1 (the pole is determined by the transconductance and gate-source parasitic capacitance of MN1 and MN2 [Eq. 3.1-c]). Regarding this issue, adding transistor MN3 shown in Fig. 3.8 relaxes the trade-off between speed and noise performance by pushing the pole to higher frequencies.

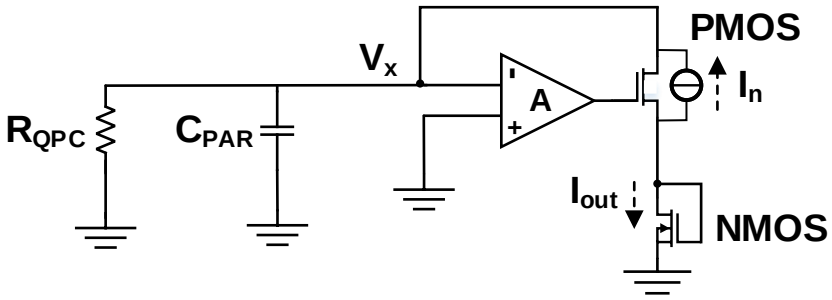


Figure 3.10 Small-signal equivalent of transistors MP2 shown in Fig. 3.8 including its noise source.

$$(\text{Kcl @ node } V_X) \Rightarrow I_{n-in} \approx I_{out} \approx \frac{I_n}{g_{mPMOS} \times (A+1) \times Z_{QPC}} (Z_{QPC} = R_{QPC} || (1/SC_{PAR})). \text{ Equation 3.2}$$

So far it is known that the input-referred noise of the cascaded gain stages will be attenuated due to the large mirror factor between MN1 and MN2; the noise of MP1 would be negligible by proper sizing, and the current noise source of MN1 can be transferred to the input with the gain close to 1. The last but not the least component to be analyzed in terms of noise is the OTA. Fig. 3.11 shows the equivalent voltage noise source of the OTA. This voltage can be translated to input noise source dividing by impedance generated by R_{QPC} parallel with C_{PAR}. This division generates a zero in the OTA input-referred current noise transfer function as it can be derived from in Eq. 3.3 which degrades the integrated noise performance over the bandwidth, as discussed in details in the next section.

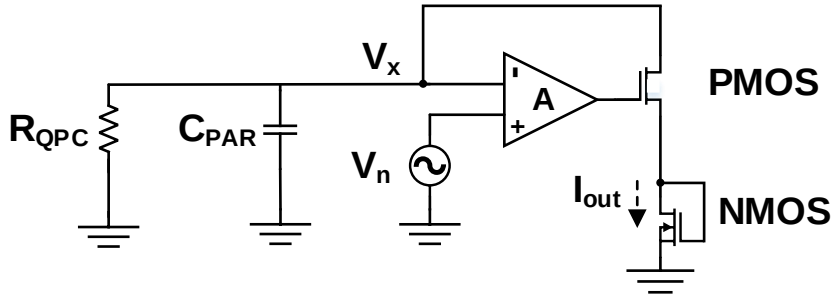


Figure 3.11. Equivalent noise source of OTA.

$$(\text{Kcl @ node } V_X, \text{ and } V_X/Z_{QPC} = I_{OUT}) \Rightarrow I_{out} \approx \frac{g_{mPMOS} \times A \times V_n}{(g_{mPMOS} \times (A+1) \times Z_{QPC}) - 1} \quad \text{Equation 3.3-a}$$

$$S_{Vn-thermal} = \frac{4KT\gamma}{g_m} \left(V^2/Hz\right) \Rightarrow S_{Iout-thermal} \approx \frac{S_{Vn-thermal}}{(Z_{QPC})^2} \left(A^2/Hz\right); \quad \text{Equation 3.3-b}$$

$$(Z_{QPC} = R_{QPC} || (1/SC_{PAR}))$$

3.4.1 Optimization of the Input Pair Size at 4.2 K

This section studies the noise contribution of the OTA in the overall noise performance of the circuit. Among many transistors inside the OTA which can contribute in the noise performance, the input pair are the most critical since they can add to input parasitic capacitance and move the zero in noise transfer function to lower frequencies as it can be seen in Eq. 3.5-a and Fig. 3.12-b; therefore, enough care must be taken in sizing the input pair of the OTA to lower their noise contribution. We are for the moment assuming that by proper sizing of other transistors inside the OTA, their noise contribution will not be dominant. This assumption is supported by the noise simulation results shown in Table 3.3 and Table 3.4.

As it will be discussed later, the flicker noise becomes the dominant noise source at 4.2K; hence, the larger sizes of transistors are preferable since the flicker noise is inversely proportional to the size of the transistors according to Eq. 3.4-b. On the other hand, the larger area of input-pair transistors results in larger C_{PAR} which moves the zero to lower frequencies and increases the integrated noise. Chopping technique is a popular method to reduce low-frequency noise. However, due to the high sensitivity of the QPC terminals, any switching at the input node in undesired.

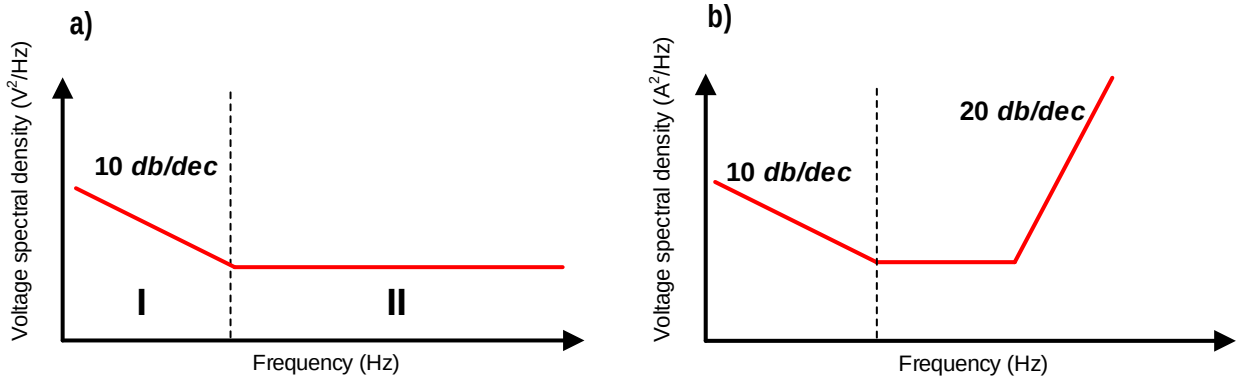


Figure 3.12 a) Typical noise spectrum of a transistor (voltage noise source shown in Fig. 3.11). b) Effect of the zero in the spectrum (input-referred current noise source).

A noise spectrum of a single transistor in standard CMOS for moderate frequencies can be divided into two regions as shown in Fig. 3.12-a; region "I" where the flicker noise is dominant and region "II" where thermal noise is dominant. Thermal noise is the voltage (or current) fluctuation caused by the random Brownian motion of electrons in a resistive medium [42] and in the CMOS it can be calculated as shown in Eq. 3.4-a. The source of the flicker noise is not yet well understood. However, it is believed to be caused by the random trapping and detrapping of the mobile carriers in the traps located at Si-SiO2 interface and within the gate-oxide [42]. Eq. 3.4-b shows one possible way to model flicker noise which is useful for hand calculations.

$$S_{V-thermal-noise} = \frac{4KT\gamma}{g_m} \left(V^2/Hz\right) \qquad \text{Equation 3.4-a}$$

$$S_{V-flicker-noise} = \frac{K_{1/f}}{2\mu C_{ox} WLf} \left(V^2/Hz\right) \qquad \text{Equation 3.4-b}$$

where K is the Boltzmann constant, T the temperature in Kelvin, γ a coefficient usually between 0.67 to 1 (based on the region of operation), g_m the transistors conductance, $K_{1/f}$ the flicker noise coefficient, μ the mobility, C_{ox} the oxide capacitance, and W, L, f transistor width, transistor length, and frequency respectively.

Adding thermal and flicker noise sources together and considering the effect of the C_{PAR} (using Eq. 3.3 and 3.4), one can calculate the optimal size of the input pair for the required input-referred integrated RMS noise (due to the input pair of the OTA) in the required bandwidth (which is 10 MHz in this design) as in Eq. 3.5. The lower frequency band is set to be 200 KHz (the same as available setup [18]).

$$I_n^2 = \int_{200\,KHz}^{10\,MHz} 2 \times \Big[\underbrace{\frac{4KT\gamma}{\alpha \times g_m \times R_{QPC}^2}}_{Thermal\ noise} + \underbrace{\frac{\beta \times K_{1/f}}{2\mu C_{ox} WLf R_{QPC}^2}}_{Flicker\ noise} \Big] \left(|1 + j2\pi R_{QPC} C_{PAR}|^2\right) df \qquad \text{Equation 3.5-a}$$

$$C_{gs} = \begin{cases} W\left(C_{ov} + \frac{2}{3} LC_{ox}\right) & Strong\ inversion \\ WC_{ov} & Weak\ inversion \end{cases}, \quad g_m = \begin{cases} \sqrt{\frac{2\mu_n C_{ox} W I_D}{L}} & Strong\ inversion \\ \frac{qI_D}{nKT} & Weak\ inversion \end{cases} \qquad \text{Equation 3.5-b}$$

where α and β are coefficients added for to account for larger noise at cryogenic temperature, as it will be explained in the following. C_{OV} is the overlap capacitance, I_D the transistor biasing current, n the inversion coefficient (between 1 and 2), and q the electron charge.

The input pair transistors can be designed to operate either in weak inversion or in strong inversion. Depending on the region of operation, based on Eq. 3.5-b, gm, and Cgs can assume different values which modify the result of the Eq. 3.5-a. The summation of input transistor Cgs, package and PCB parasitics, and wire capacitance forms the C_{PAR}. In order to find the optimal size, separate equations are used for each region of operation of the transistor. Since those equations are not consistent, a discontinuity appears in the optimization graph shown in Fig. 3.13.

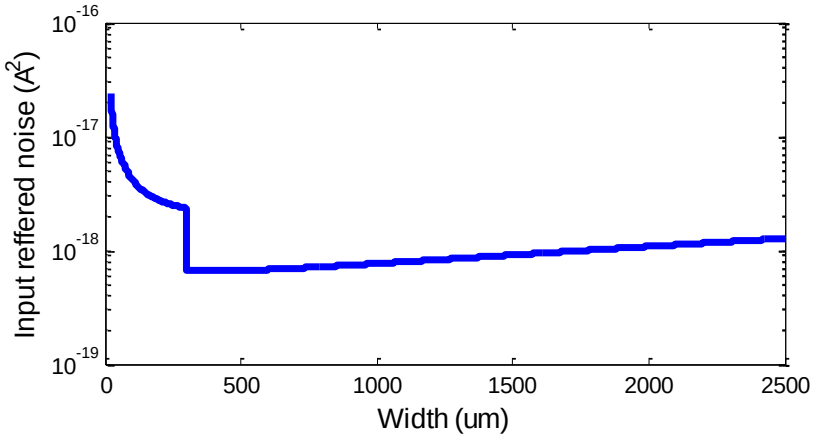


Figure 3.13 Calculated input-referred noise versus the width of the input pair transistors based on Eq. 3.5-a.

To show the optimal point more clearly, separate optimization graphs for each of the regions of operation are shown in Fig. 3.14.

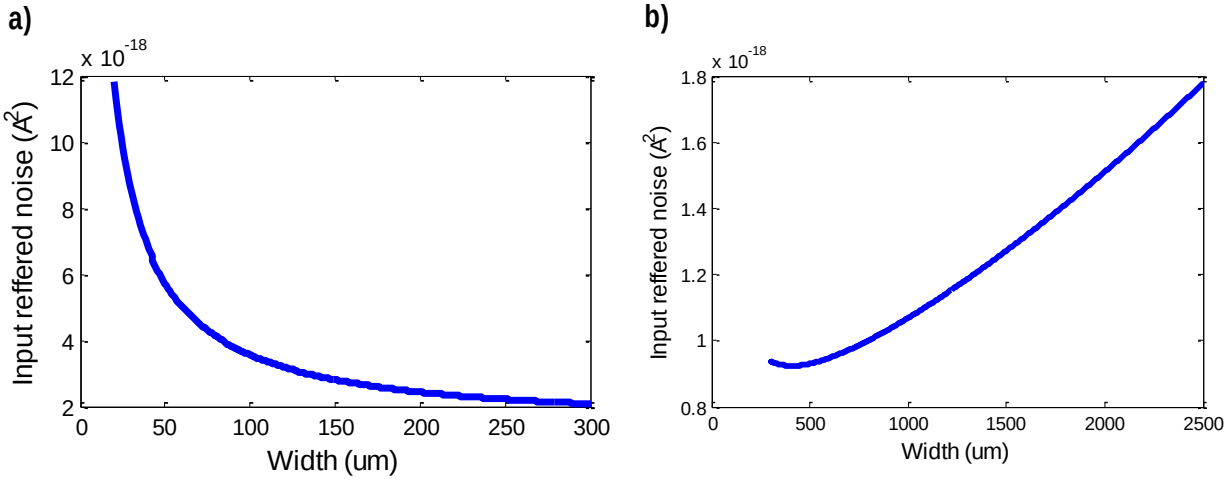


Figure 3.14 Calculated input-referred noise versus the width of the input pair transistors at 300 K based on Eq. 3.5-a; a) Strong inversion. b) Weak inversion.

The optimization of the input pair area has been done for different biasing currents of OTA and for different lengths (for both PMOS and NMOS input pair). The optimal length is found to be 0.8 um (the sweep of the length has been done for three fixed widths, and the current was set to the maximum current). Meanwhile, increasing the current has no significant impact on the flicker noise but it reduces the thermal noise. The maximum current consumption is set by maximum power budget (1 mW). The fraction of CPAR caused by external parasitic sources [C_{PAR} – Cgs] is assumed to be 2.5 pF for this optimization (assuming that QPC and read-out circuit are integrated on the same chip). The first optimization is done for -55℃ (218 K), which is the minimum specified temperature for the device models and their noise models. Fig. 3.15 shows the output noise spectrum simulated at -55℃.

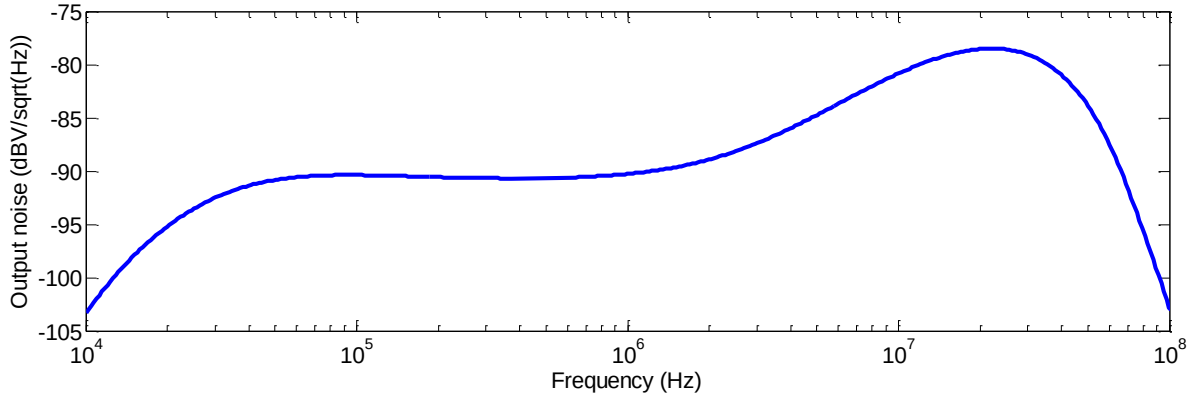


Figure 3.15 Output noise spectrum simulated for the input parasitic capacitance of 2.5 pF at 218 K.

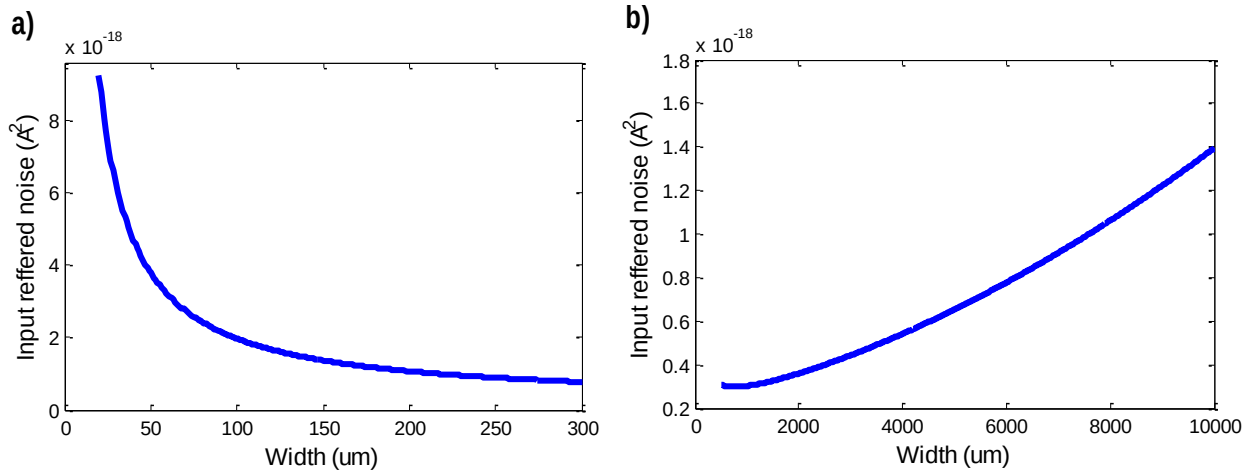


Figure 3.16 a) Calculated input-referred noise versus the width of the input pair transistors at 4.2 K based on Eq. 3.5-a. a) Strong inversion. b) Weak inversion.

Now we need to have a proper assessment of noise performance at 4.2K. According to the literature [40] and our previous measurements at cryogenic temperature [41], we expect the thermal noise to decrease almost linearly with absolute temperature. However, the flicker noise is predicted to get higher by going to very low temperatures [43], [41].

In order to optimize the size of the OTA input pair transistors at that temperature, two extra coefficients have been included (α for thermal noise and β for flicker noise) in Eq. 3.5-a. The factor α is assumed to be 52 considering the fact that the thermal noise is decreasing linearly with temperature (from 218K to 4.2K), and the factor $\beta$is assumed to be 10 (considering the worst case). Fig. 3.16 shows the calculated noise versus width of the input pair transistor at 4.2K. Fig. 3.17 shows the expected noise spectrum of the designed circuit at 4.2 K.

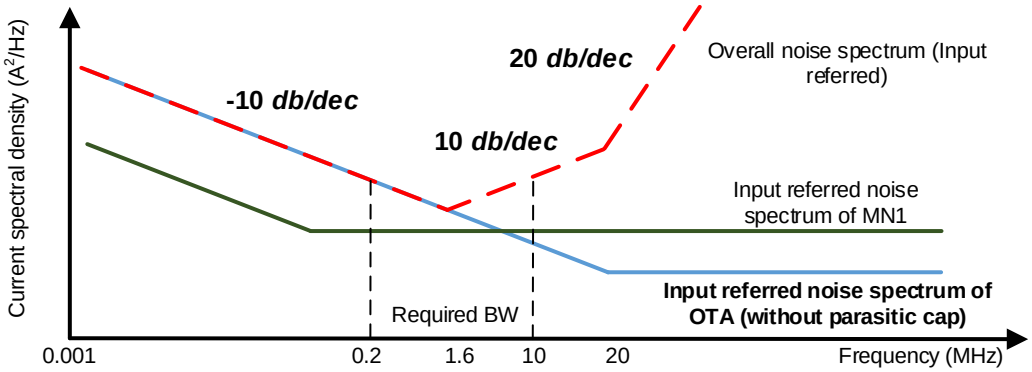


Figure 3.17 Overall calculated input-referred noise spectrum (red dashed line).

Noise type \ Temp (K)	218.15	4.2
Thermal Noise (input referred RMS)	2.12 nA	294.2 pA
Flicker Noise (input referred RMS)	165.8 pA	524 pA

Table 3.3 Input-referred noise for the input parasitic of 2.5 pF (200 kHz-10 MHz BW).

Noise type \ Temp (K)	218.15	4.2
Thermal Noise (input referred RMS)	8.05 nA	1.11 nA
Flicker Noise (input referred RMS)	543.6 pA	1.72 nA

Table 3.4 Input-referred noise for the input parasitic of 20 pF (200 kHz-10 MHz BW).

3.4.2 Kick-back Noise

Since the input node of the circuit is connected to the QPC, any voltage fluctuation due to noise or switching can deteriorate the state of the qubits. The noise generated by the circuit can appear as voltage at the input (thanks to the OTA feedback) and be injected back into the QPC. The specification for voltage fluctuation on the input node imposes that the voltage fluctuation must be less than 180 µV RMS; in our simulation, the integrated noise at the input node of the circuit (integrated up to 10 GHz bandwidth) is less than 20 µV RMS.

3.5 OTA Design

From section 3.3, the minimum required gain of the OTA block (shown in Fig. 3.8) is 62 dB, in order to have low TIA input impedance is calculated. Besides that, it is explained in section 4.4 that in order to lower the noise contribution of MN1 and MP1 (shown in Fig. 3.8), the bias current of MP1 must be as low as possible; therefore, the OTA power consumption is dominant in the whole power budget of 1mW. As it is explained in the previous section, the noise requirement sets the input pair size of the OTA. Despite having more flicker noise, NMOS transistors are chosen over PMOS transistors for the input pair of the OTA; for the same biasing conditions, i.e. for the same transconductance and current, NMOS has 4.9 times less parasitic capacitances than PMOS in NXP SSMC 0.16-um CMOS technology.

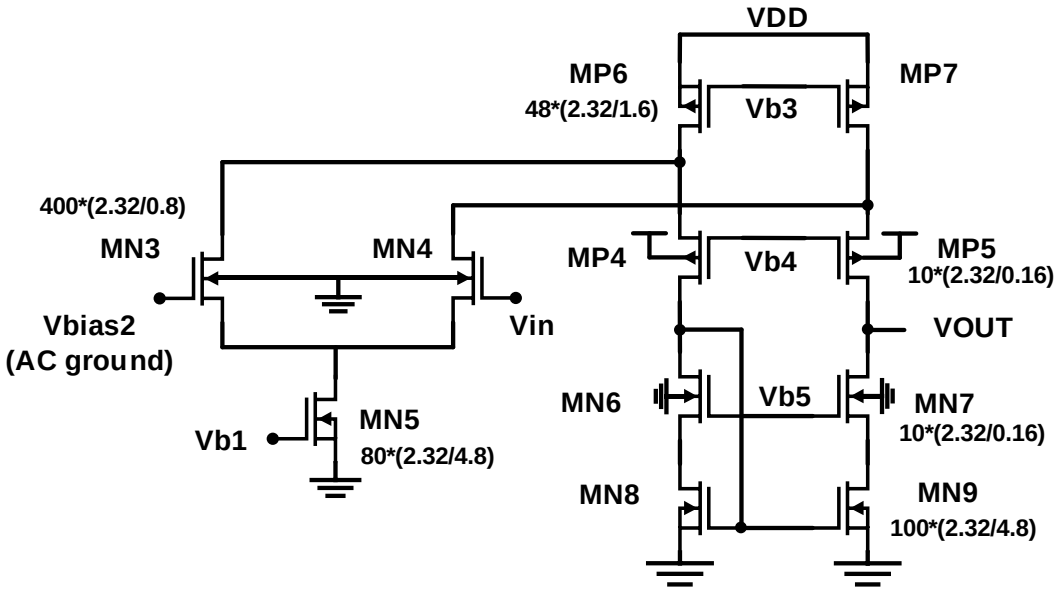


Figure 3.18 Folded-Cascode OTA with NMOS input pair.

The Vgs of MP2 is around 570mV at room temperature for 100nA biasing current. At cryogenic temperature, the required Vgs for the same biasing current becomes even larger (≈ 660mV) due to the increase in threshold voltage of a transistor. This causes large difference between the common-mode input OTA voltage (connected to MP2's source) and the OTA output (connected to MP2's gate). Consequently, the Folded-Cascode OTA with NMOS input pair shown in Fig. 3.18 is a well fit for this read-out structure as it does not need any extra stage or level shifters to compensate for the DC voltage difference and it can provide enough gain to maintain the bandwidth. Knowing the required gain of the OTA, size of the input pair, biasing current of the OTA and applying Eq. 3.6, we can determine the sizing of the other transistors

$$A_{OTA} = g_{mMN4} \times [(g_{mMP5} r_{oMP5} (r_{oMP7} || r_{oMN4})) || (g_{mMN7} r_{oMN7} r_{oMN9})] \qquad \text{Equation 3.6}$$

At cryogenic temperature, the flicker noise is expected to be the dominant noise source as it is mentioned in section 3.4; by reducing the biasing current of the OTA, the input referred thermal noise of the OTA increases while it does not affect the flicker noise (in the first order). Therefore, it can be reduced as long as the thermal noise is comparatively lower than flicker noise. Since we do not have an accurate model of flicker noise at 4.2 K, a digitally tunable current source is implemented to tune the power consumption of the OTA (the biasing current of the input branch and folded branch scale up or down with the same ratio). The output swing of the OTA is very small (in the order of tens of microvolts). Thus, the linearity and slewing are not much of a concern in the required bandwidth (10MHz).

3.5.1 Stability of the Circuit

In order to study the stability of the circuit, the loop-gain is calculated in Eq. 3.7-a using the simplified model of the circuit shown in Fig. 3.19. In order to calculate the loop-gain equation, the loop is cut at the input terminal of the OTA (V_2 is the input of the OTA and V_1 is the input of the circuit which is connected to the source of MP2) Consequently, two left half-plane poles and one left half-plane zero (shown in Eq. 3.7-b) are derived from the simplified loop-gain transfer function.

To increase the loop stability and improve the phase margin, one of the LHP and LHZ can be designed in such a way to cancel each other. Since a proper model of transistor's parasitic is not available, exact cancellation is difficult to implement in practice due to process spread. Therefore, two tuning mechanisms have been introduced; the biasing current of MP1 is digitally controllable to tune gm2 and hence the zero's location.

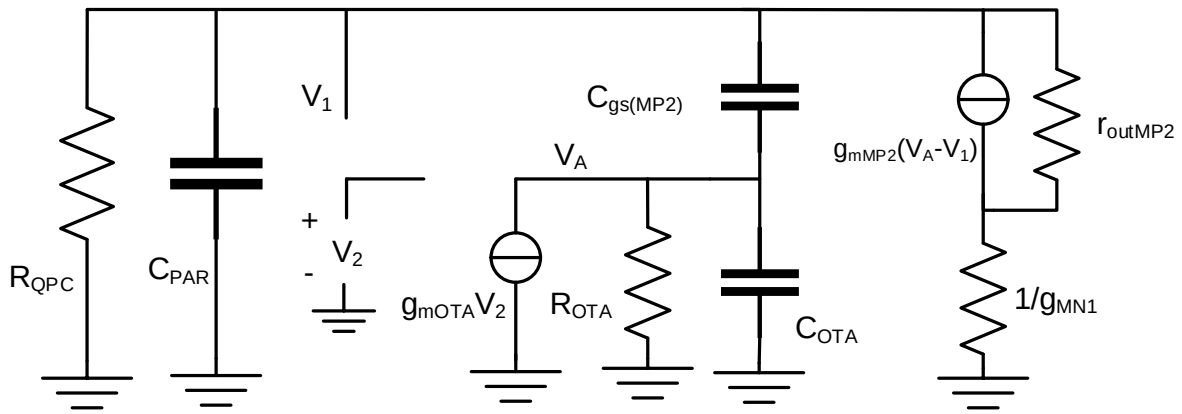


Figure 3.19 Simplified model of the loopgain including the OTA and MP2 transistor.

Equation 3.7-a

$$\frac{V_1}{V_2} \approx \frac{-g_{mOTA}\, R_{OTA}\, R_{QPC}\, (g_{mMP2} + sC_{gsMP2})}{(1+ sC_{OTA}R_{OTA})(g_{mMP2}\, R_{QPC} + 1 + sC_{PAR}R_{QPC} + sC_{gsMP2}R_{QPC}) + sC_{gsMP2}R_{OTA}(1+sC_{PAR}R_{QPC})}$$

assuming $gm_{MP2}R_{QPC}$, and $SC_{gsMP2}R_{QPC}$ are negligible, we have:

$$LH\ Zero\ @\ \frac{g_{MP2}}{C_{gsMP2}}, \qquad LH\ Poles\ @\ \frac{1}{R_{QPC}C_{PAR}},\ \frac{1}{R_{OTA}(C_{gs(MP2)}+C_{OTA})} \qquad \text{Equation 3.7-b}$$

The second mechanism is the tunable capacitor bank placed in parallel to the Cgs of MP2 (Fig. 3.8) to tune the location of zero (assuming that the size of MP2 is chosen in such a way that CgsMP2 << C_{OTA} in order to decrease the sensitivity of the location of the pole to variation of the CgsMP2). It is evident that by adding the capacitor bank the bandwidth will be limited. This is the price to pay for a more reliable and stable circuit. Fig. 3.20 and Fig. 3.21 show the loop-gain and phase for different values of compensation cap corresponding to 14MHz and 1.8MHz bandwidth (bandwidth of the whole circuit from input to output including all the stages) respectively (it should be reminded that the minimum desired bandwidth is 10 MHz).

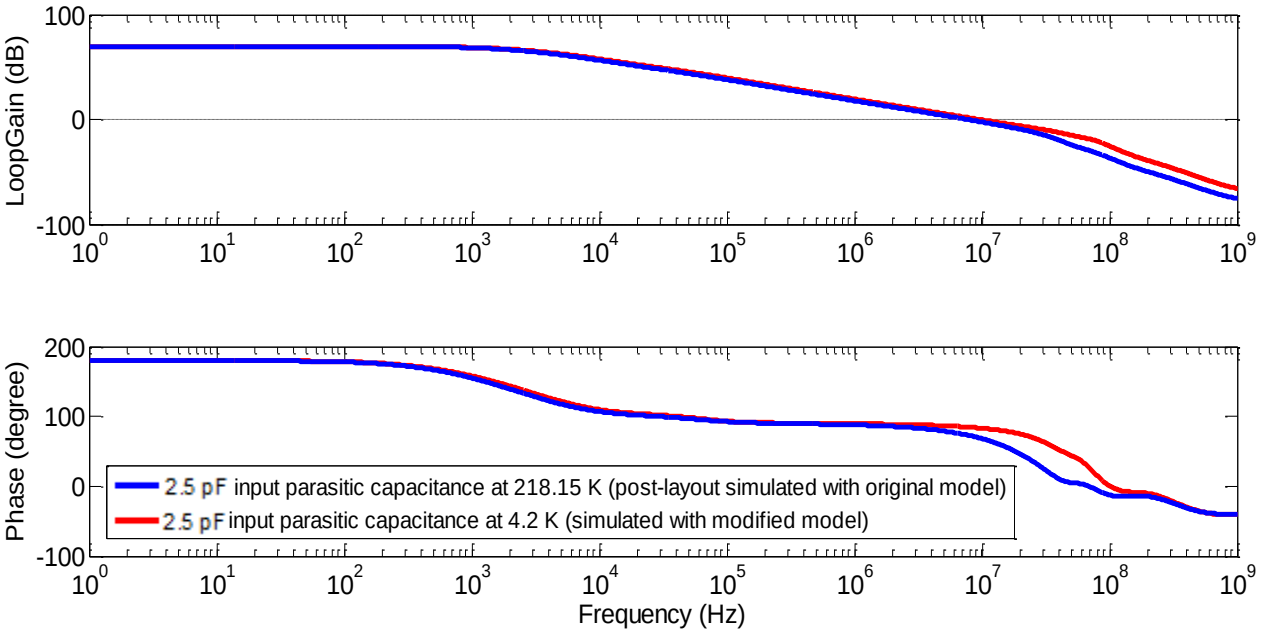


Figure 3.20 Stability analysis for different input parasitic capacitance and over different temperature. Blue and red lines correspond to 12.3MHz and 14MHz bandwidth respectively.

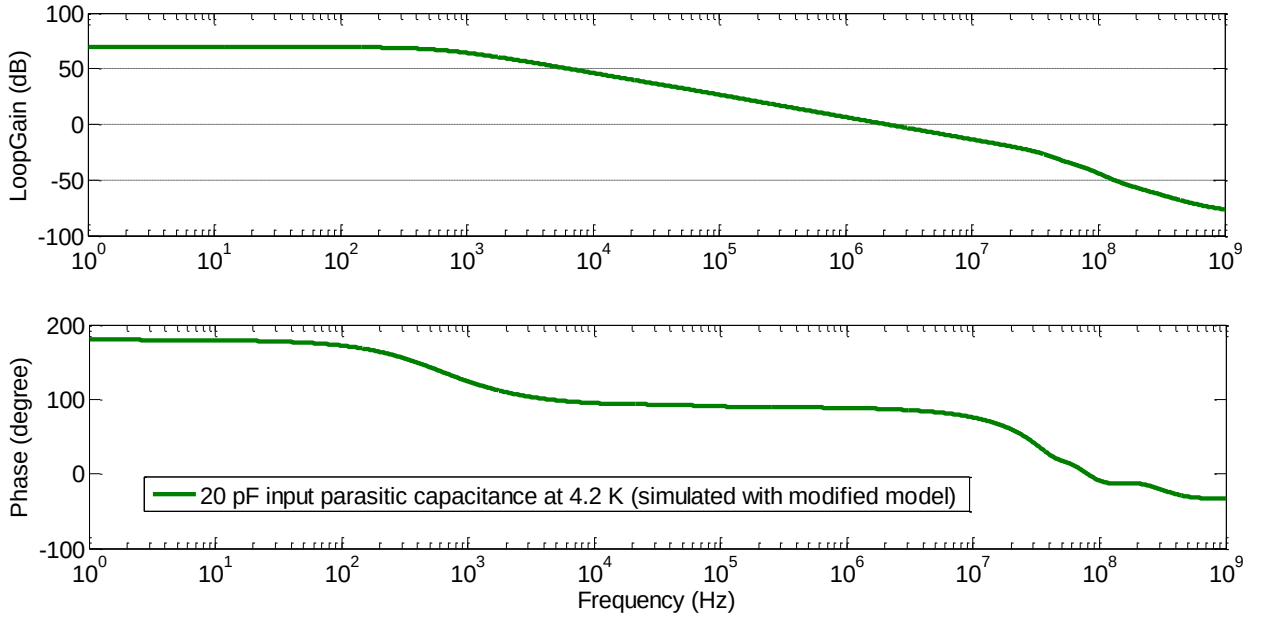


Figure 3.21 Stability analysis with maximum compensation capacitance (All switeches in capacitor bank are on). The bandwidth of the circuit equals to 1.8MHz.

3.6 Intermediate Gain Stages

Since all measurement equipment will be placed at room temperature, the test chip must be able to drive a large capacitive load due to the long wires from the chip at cryo-temperature to the room-temperature equipment. To address this point, nine gm-over-gm gain stages (Fig. 3.22-a) are used (excluding the output stage) to increase the driving strength of the amplifier without significant degradation in circuit bandwidth. For the optimum bandwidth of the amplifier chain, the width-ratio between two successive stages is chosen to be 2.9 which has been confirmed to be optimal by simulation.

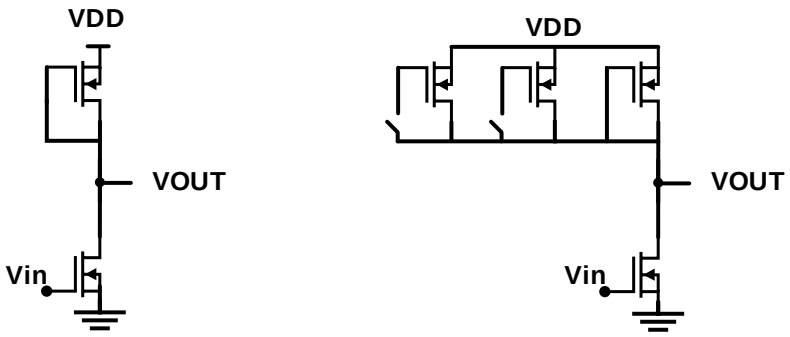


Figure 3.22 a) Intermediate gain stages. b) With variable gain.

Because the input signal is very small (in the order of tens of pA), we need a large amplification to ease the requirements of the measurement equipment. However, due to uncertainty in the noise performance at 4.2 K, a too large amplification can saturate the output transistors. Therefore, the last4 gain stages are designed to have a variable amplification by tuning the active load, as shown in Fig. 3.22-b.

This tunable variable gain gives this opportunity to avoid the saturation of the circuit by lowering the gain. Another problem is that any noise measurement setup has a minimum detectable noise floor. Using tunable gain, one can increase the gain to make the output noise detectable for the measurement setup. Exploiting the tunable gain, the transimpedance ranges from 1MΩ to 130MΩ as shown in Fig. 3.23. It worth to mention that the bandwidth degradation after adding those intermediate stage is around 5% which is negligible.

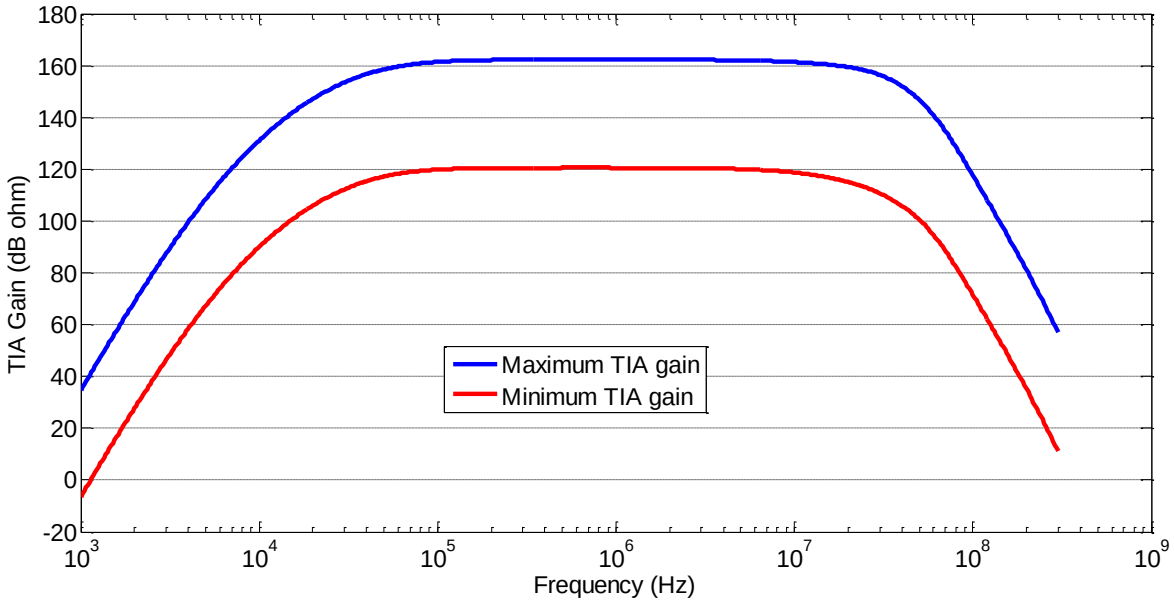


Figure 3.23 Maximum and minimum obtainable gain exploiting variable gain (with modified model at 4.2K).

3.7 Non-ideal Supply and Ground Path

In practice, the VDD and ground nodes are not ideal inside the chip due to the finite impedance of the metal traces and the pads. In addition to that, the lead-frame in the package adds extra impedance. A typical model for a package pin is shown in Fig. 3.24. Table 3.5 shows the electrical characteristics of a typical DIP40 package, which is the package adopted for the proposed test chip. As a result of these non-idealities, especially in the last gain stages, the impedance of the traces becomes comparable to the 1/gm of transistors causing a considerable portion of the signal to be fed back to previous stages as shown in Fig. 3.25, causing unwanted feedback and eventually instability

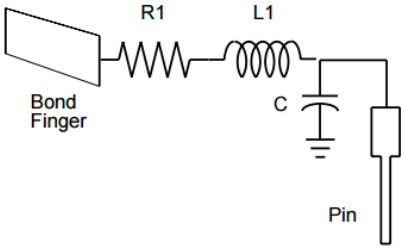


Figure 3.24 Package trace model.

Pin No.	R(Ω)	L(nH)	C(pF)	t_{of}(ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	157
4,17,24,37	0.110	6.48	2.34	123
5,16,25,36	0.103	5.69	2.16	111

Table 3.5 Electrical characteristics of DIP40 pins.

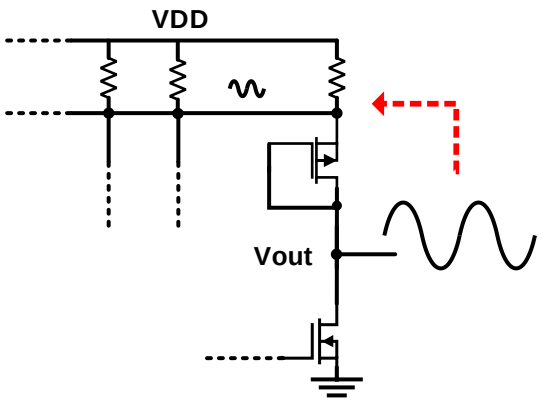


Figure 3.25 Effect of non-ideality in supply path.

For instance, the output stage biasing current is around 22mA corresponding to a gm of 190m℧; the impedance of the trace plus pad (shown in Table 3.5) can easily be up to 10% of 1/gm of the active load of the output stage. Therefore, by sharing the same ground up to 10% of the output signal might be fed back to the input stage; due to the high amplification (TIA gain), this can easily create instability. One solution to solve this problem is to use several VDD and Ground pins to separate the supply of the prior stages from later stages as shown in Fig. 3.26. The effectiveness of the technique is approved with the simulation result shown in Fig. 3.27.

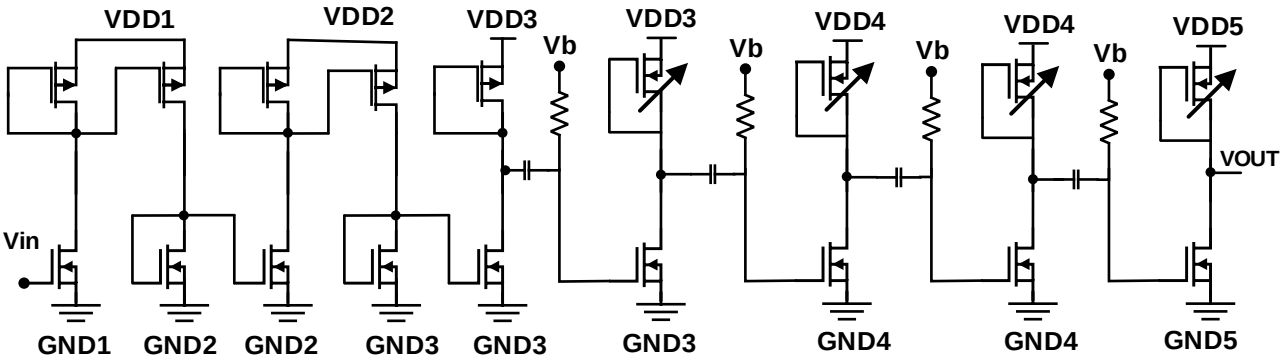


Figure 3.26 Isolating VDDs and GNDs in the 9 output stages to compensate the effects of non-ideal supply and ground path

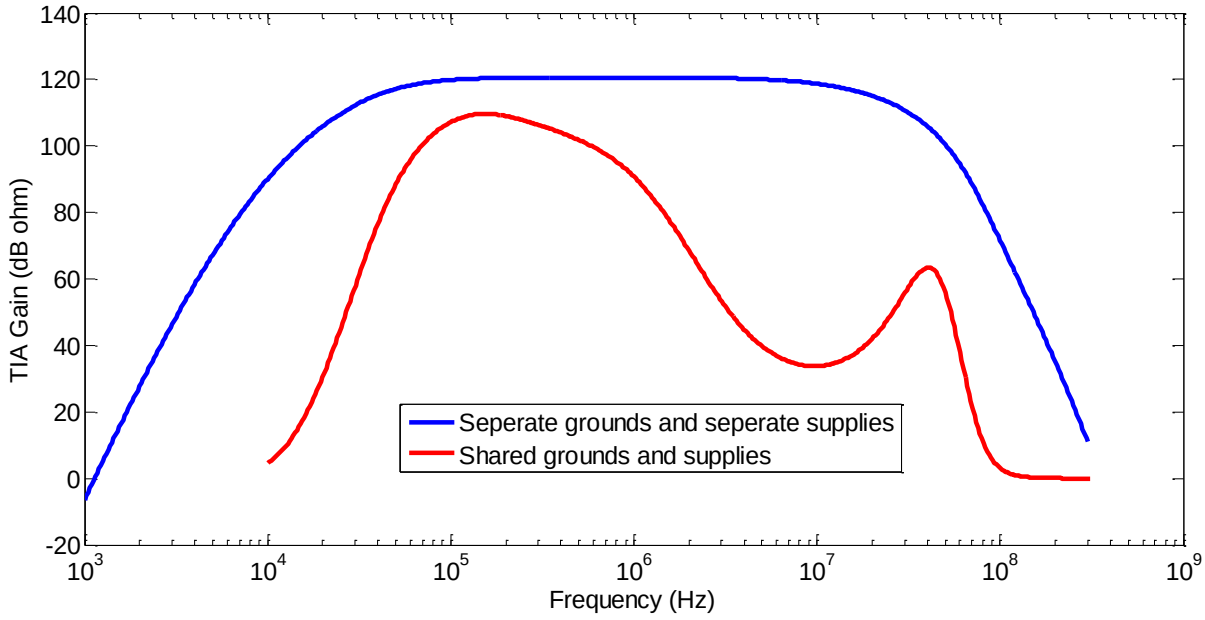


Figure 3.27 Solving the Effect of non-ideality in supply path by separating VDDs and GNDs.

3.8 Improved PSRR

A very important point which must be taken into account is the effect of any fluctuation in supply path and the effect of that on circuit performance. Even the cleanest supply source has some noise and fluctuations; in our circuit, which is aimed to an extremely low-noise application, that effect can be even dominant. Additionally, the circuit is single-ended and is very prone to the noise of the supply.

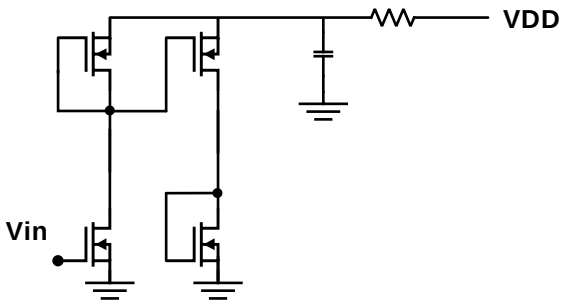


Figure 3.28. Filtering out the noise from supply by adding low-pass filter.

In order to improve the PSRR of the circuit, a simple low pass filter shown in Fig. 3.28 with corner frequency of around 1.5 to 40 KHz (with a resistor in the range of 2 to 10Ω and the capacitor in the range of 2 to 10 µF) is going to be inserted on the PCB in all supply paths to filter out the noise from supply.

According to the simulation (applying 100mV$_{P-P}$ of fluctuation (which is a achievable noise level for a good voltage regulator available in the market) on supply voltage of the first stage), after adding the LPF, the output integrated voltage (over 10GHz of bandwidth) reduces from 5V to 100uV which can be neglected.

3.9 Bias Circuit

Due to the wide range of biasing currents (from 10nA in the first stage to 20mA in the last stage) designing a reference circuit for this chip is challenging. As a reference circuit, a gm-constant circuit shown in Fig. 3.29 with 10µA is designed. Due to process spread in the absolute values of resistor and mismatch of transistors (which are two uncorrelated sources of error), the biasing current can vary up to 30% (3σ) as shown in Fig. 3.30.

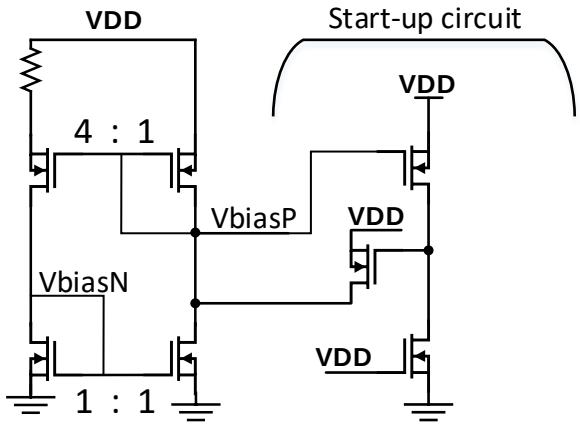


Figure 3.29 gm-constant reference circuit

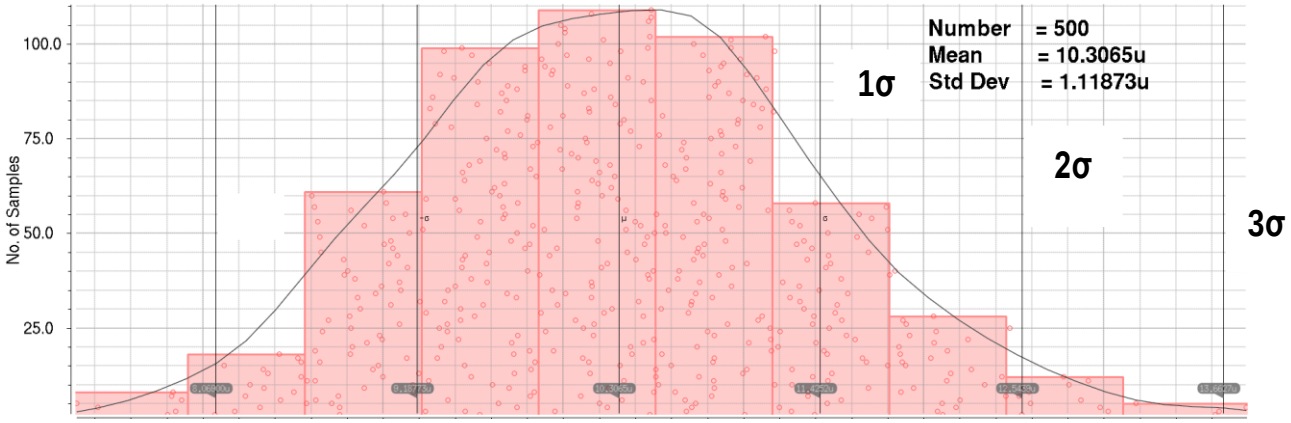


Figure 3.30 Deviation from desired value of the reference due to the process spread and mismatch.

In order to compensate for the effect of process spread in resistor's absolute value, which is the dominant source of error in the reference current, an external current source is also implemented in case more accurate biasing is required. In order to reduce the noise contribution of the external source, it is designed to have 10 times higher current (100 μA); accordingly, the noise will be divided by 10.

3.10 Digital Circuitry

As it is explained in the previous section, in order to guarantee the functionality of the circuit at cryo-temperature, some tunable circuits including the capacitor bank (for OTA compensation and stability of the circuit), tunable current source (controlling the OTA power consumption and OTA stability), switch between external and internal current source, and tunable active load (variable gain) has been implemented. To program all the switches, a 42-bit (in total, 42 switches are used in this circuit) shift register has been implemented that can be programmed using the SPI protocol.

At cryo-temperature, there is this possibility that the shift register will not be functional. To have a backup plan, an extra multiplexer is added for each bit at the output of the shift register. The multiplexer can select a default setting if a default activation signal is activated through one of the pins.

3.11 Layout

In this section the layout of the circuit is presented. Fig. 3.31 shows different blocks such as the OTA, intermediate gain stages, Biasing, and Digital. The input and output pads are placed far away from each other in order to prevent any coupling between one another which can creates stability issues. The digital and analog parts are very well isolated (even the digital and analog ESD protections are separated from each other).

The overall area of the chip including the pad-rings is 2.2 mm^2 (1.812 mm × 1.215 mm).

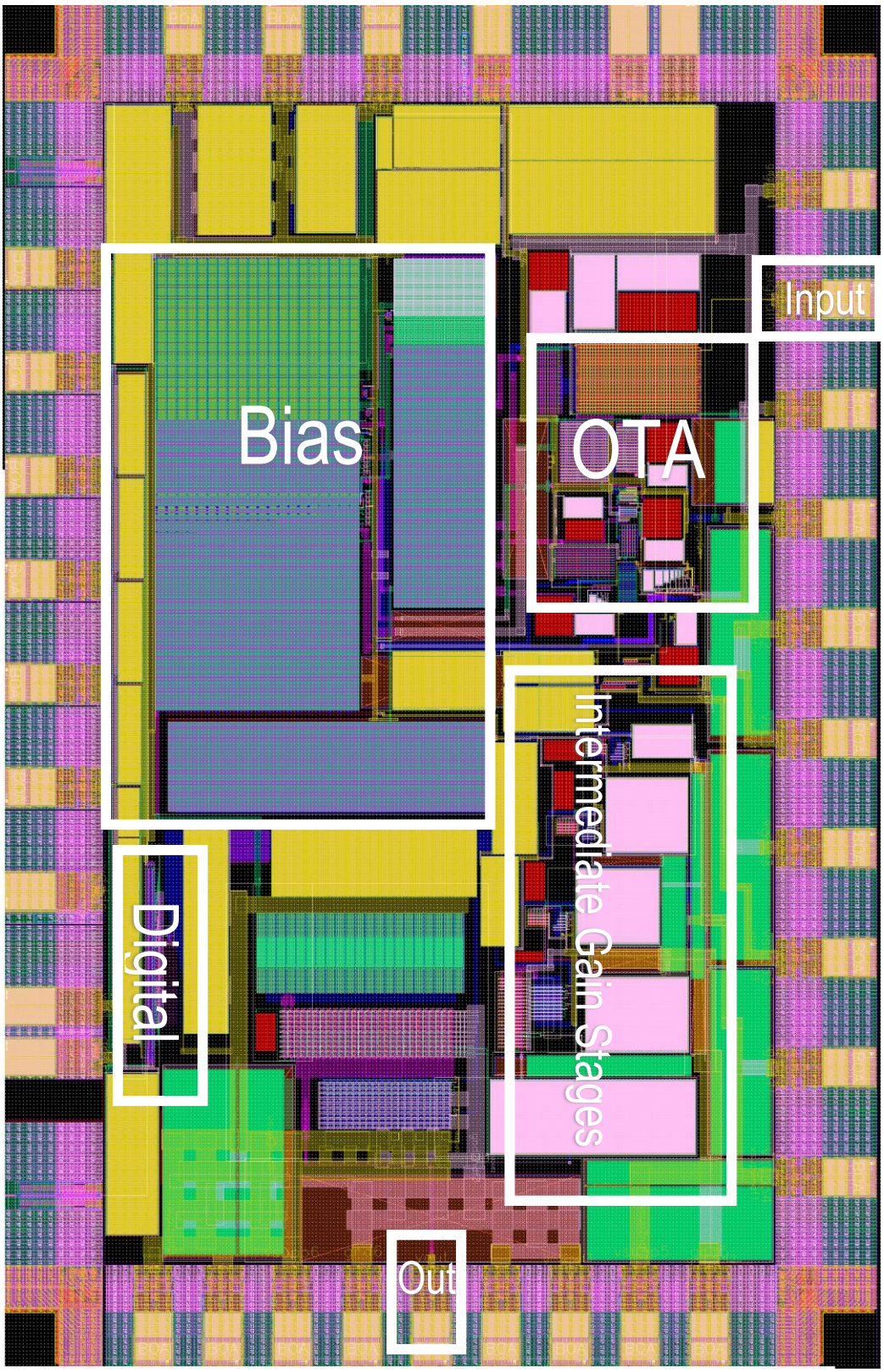


Figure 3.31 Layout of the designed chip including the pad-ring.

3.12 Post-Layout simulation results

As it is shown in Fig. 3.20, Fig 3.21, and Fig. 3.23, the circuit simulated using the modified model (for 4 K simulation) is functional and by properly setting the tunable parameters, similar performance is achievable with respect to the performance at room temperature using the model from the foundry. Fig. 3.32 shows the post-layout simulation of the circuit at -55 ℃ using foundry model. Table 3.6 presents a comparison between this work and State-of-the-art design.

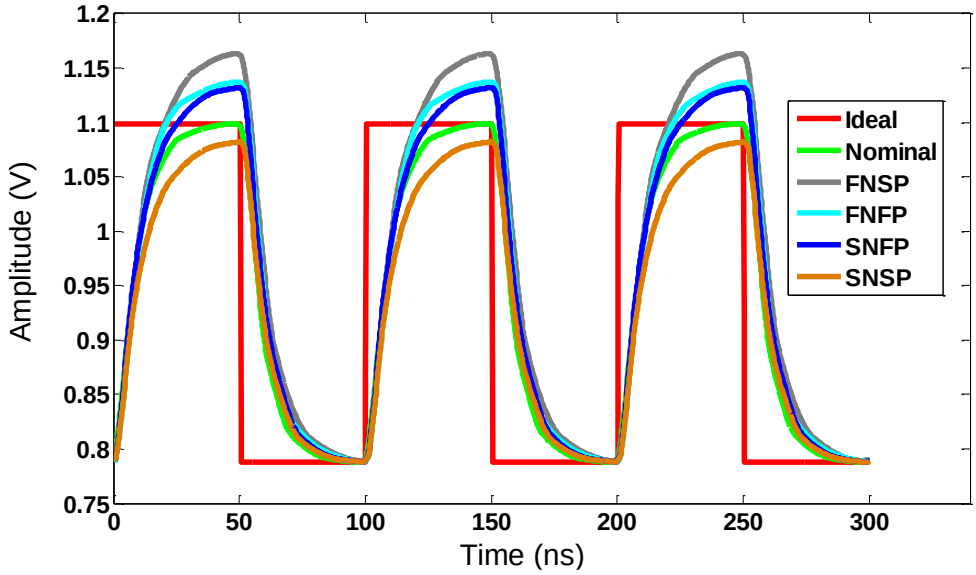


Figure 3.32 Post-layout transient simulation at 218 K over different process corners.

	Desired specification for this work	This work (Simulation)	State-of-the-art [24]
Power consumption	1 mW	400 µW (excluding buffer stages)	340 µW
Bandwidth (MHz)	10	1.6 to 18 (tunable)	1
Input-referred integrated noise (up to 1 MHz BW , for 20pF input capacitance)	< 150 pA RMS	130 pA RMS	148 pA RMS
Input-referred integrated noise (up to 10 MHz BW , for 2.5pF input capacitance)	_	600 pA RMS	_
Input-referred integrated noise (up to 1 MHz BW , for 2.5pF input capacitance)	_	28 pA RMS	_
Input parasitic capacitance range (pF)	2.5 to 20	2.5 to 20	20
Current to voltage gain	3 MΩ < Desired gain < 500 MΩ	1 MΩ to 130 MΩ (tunable)	_
Adopted technology	0.16-um CMOS	0.16-um CMOS	HEMT
Temperature (K)	4.2	4.2	1.8

Table 3.6 Comparison between the desired specifications, simulations, and state-of-the-art.

4 Measurement Plan

This chapter presents a measurement plan for the proposed read-out circuit that can address the challenges of measuring a chip at cryogenic temperature with an extremely low noise level (down to 100 fA/$\sqrt{Hz}$) and a small input current pulse (around 72pA of pulse amplitude). As it is mentioned before, for the first measurements, we might not have access to a real QPC; therefore, in order to model a real QPC and generate such a small current pulse, the circuit shown in Fig. 4.1 to be connected to the input of the chip is proposed. The amplitude of the pulse generator would be 18mV in order to generate a 72pA current pulse at the input of the circuit. While the circuit emulates the small signal impedance of the QPC (25 kΩ), it generates much higher noise than the QPC. To remove the noise contribution of the components shown in Fig. 4.2 (especially from the 25 kΩ source resistance at 4.2 K), a switch (jumper) is placed, so that the noise can be measured at the output of the amplifier without any input signal.

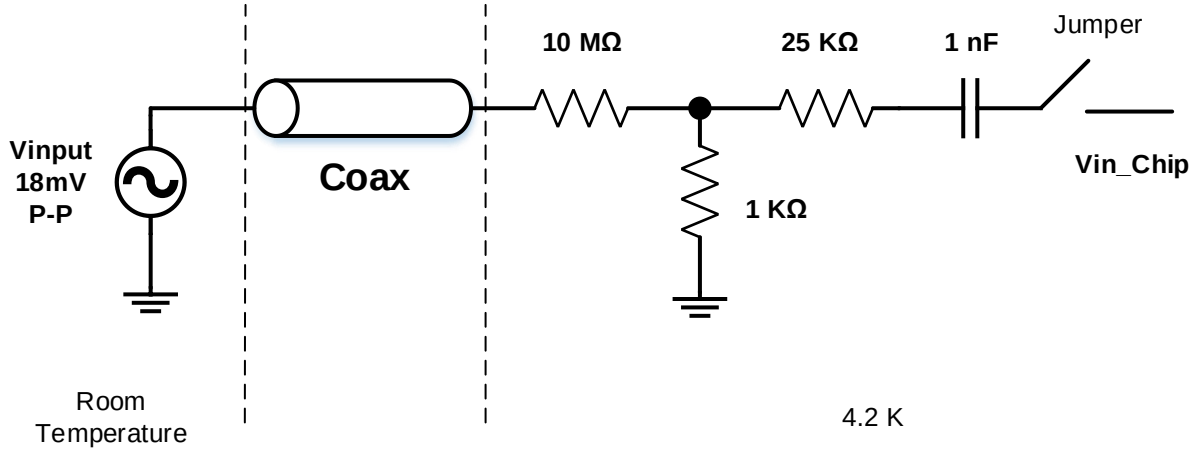


Figure 4.1 A setup to model the Quantum Point Contact (QPC) at the input of the chip.

Another issue is the fact that standard measurement instruments, like a spectrum analyzer, have 50 Ω input impedance (high impedance ports typically show poor noise performance). Therefore, a matching LNA needed to be placed at the output of the chip. For this purpose, the circuit in Fig. 4.2 using a LT1227 opamp has been designed. It should be noticed that the noise floor of the LNA must be below the minimum output noise floor of the chip for a proper noise measurement (the input swing of the LNA is more than 2V).

Features

- **140MHz Bandwidth: A_V = 10**
- **1100V/µs Slew Rate**
- Low Cost
- 30mA Output Drive Current
- High Input Impedance: 14M ohms, 3pF
- Wide Supply Range: ±2V to ±15V
- Shutdown Mode: I_S <250µA
- Low Supply Current: I_S = 10mA
- Inputs Common Mode to Within 1.5V of Supplies
- Outputs Swing Within 0.8V of Supplies

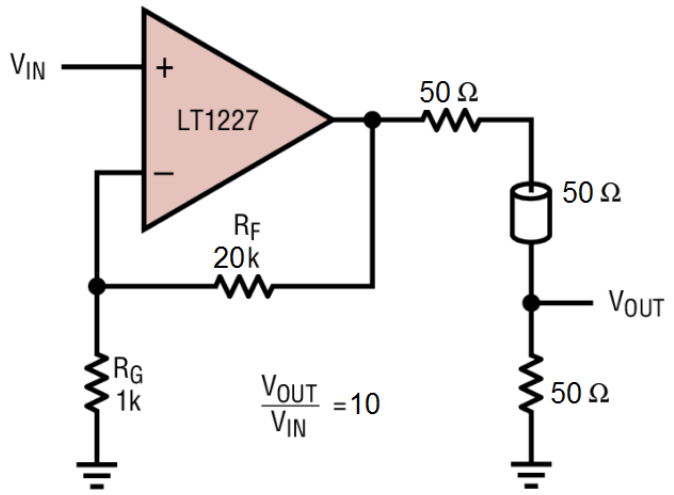


Figure 4.2 The output matching LNA [3].

The last point to be mentioned is the RC(values are mentioned in section 3.8) filters placed in supply paths in order to improve the Power Supply Rejection Ration (PSRR) as it is mentioned in section 3.8. The maximum IR drop due to the resistors in supply path is around 35 mV which can be compensated with the SMU controller using 4-wire sensing [44]. Initial tests will be done at room temperature to verify the functionality of the chip (e.g. biasing of the circuit). Fig. 4.3 shows the proposed setup for the room-temperature measurement.

The chip is designed to have its best performance at 4.2 K which is the boiling temperature of Hilum-4 at one atmosphere [45]. In order to achieve such a temperature the chip will be mounted on a PCB and inserted in a Helium vessel as shown in Fig. 4.4. The PCB will be connected through long cables (~1.5 m) in a steel pipe to the room-temperature equipment.

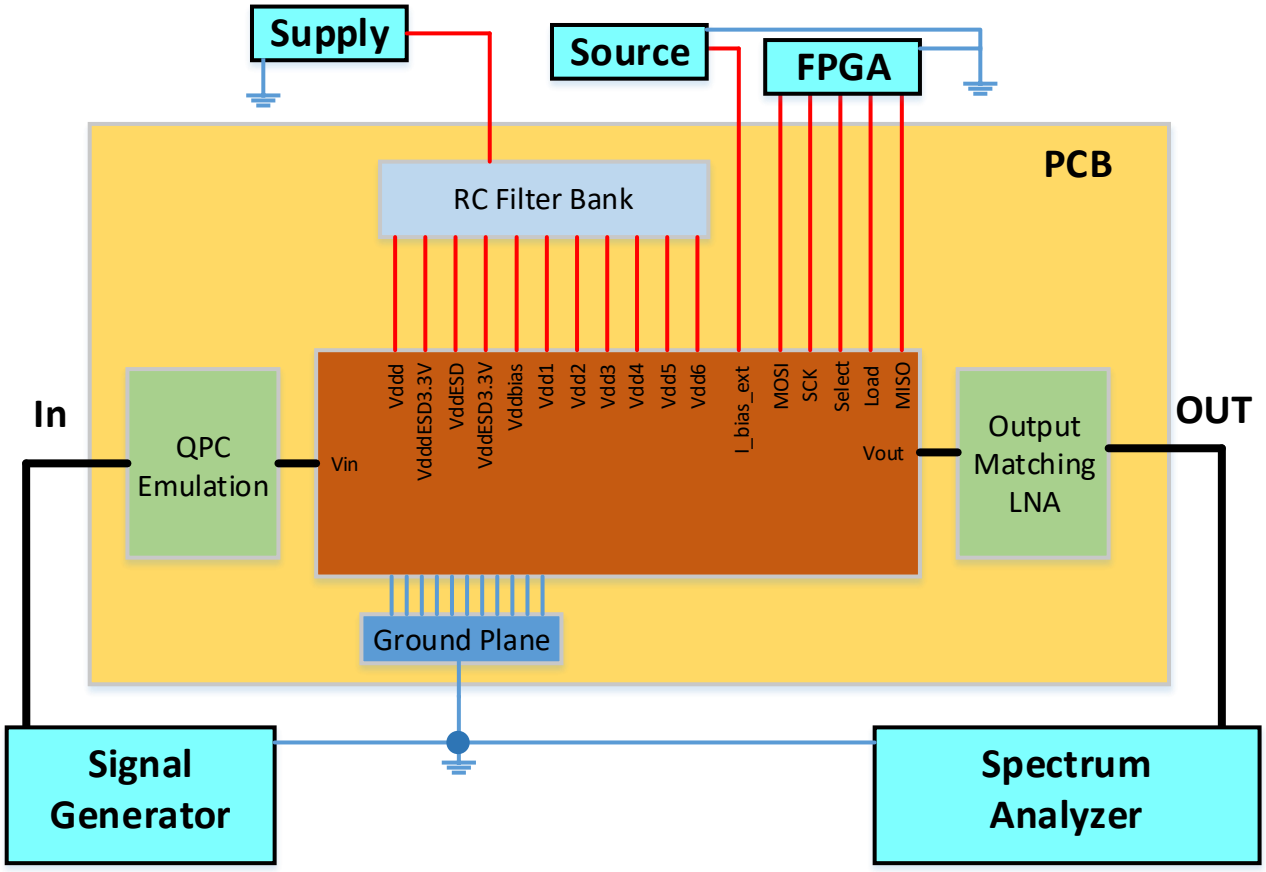


Figure 4.3 Room temperature measurement setup

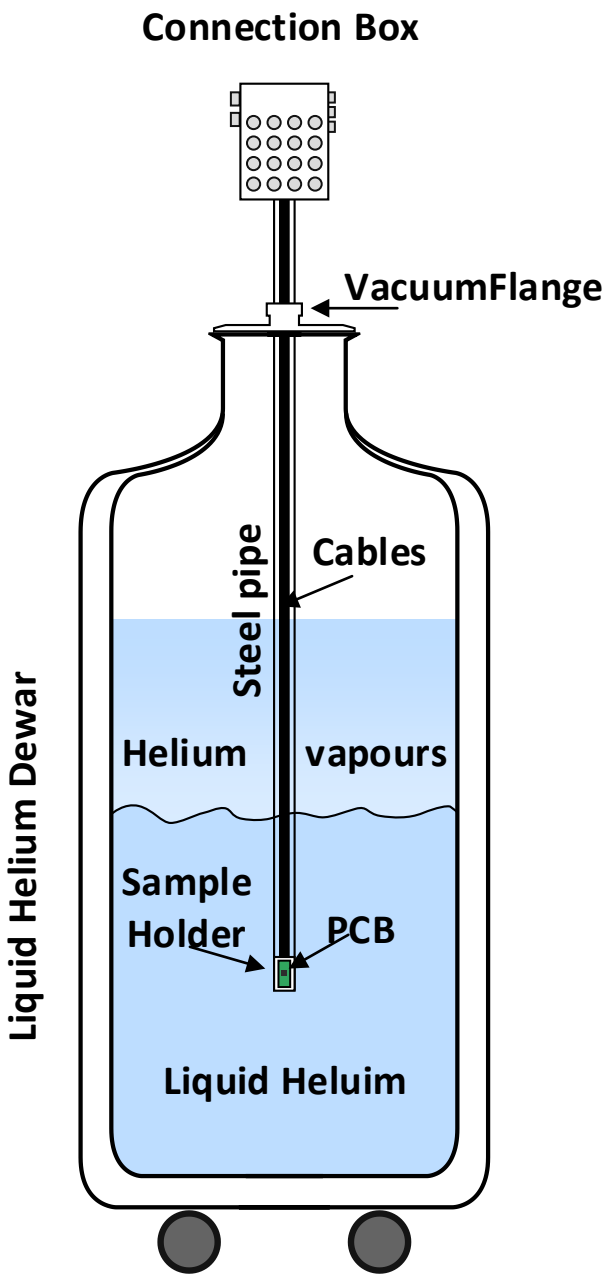


Figure 4.4 Cryogenic measurement setup.

5 Conclusion and future work

5.1 Conclusion

In this thesis, a thorough explanation of current read-out techniques for Quantum Point Contact (QPC) have been presented. A complete design flow of a cryogenic QPC current read-out has been shown, from deriving the specifications to post-layout simulation. This design targets to push the bandwidth of the state-of-the-art QPC readout by 10x within the limited power budget of 1mW and keeping the same noise floor. To summarize, the following results can be mentioned:

- By going down to cryogenic temperature, some critical transistor parameters change. Although some of them will degrade the chip performance (like flicker noise), others bring advantages in circuit performance like lower thermal noise and higher transistor speed. There may also be undesirable effects like hysteresis and kink effect but those are typically negligible in sub-micron CMOS technologies, like the one adopted in this work (SSMC 0.16-um CMOS).

- Modifying some parameters in the foundry CMOS model makes it possible to adapt the simulation model to match the measured transistor characteristics at 4.2 K and to use such new model for circuit design and simulation at that temperature.

- The electrical model of the currently available QPC and the read-out setup has been analyzed and a high bandwidth, low noise read-out circuit has been proposed and laid out. A complete noise, speed, and power budget analysis has been performed. The circuit noise performance has been optimized for a relatively low input capacitance, which is the use case for qubit in close proximity to the readout (or integrated with the readout on the same chip).

- In this design, many critical issues, such as stability, PSRR, kick-back noise and non-ideal supply path, have been addressed considering a relatively large safety margins that reduce risks related to the lack of a very accurate device models at 4.2 K including, for example, transient behavior and noise performance. This has been achieved by careful design and by allowing tunability of some parameters, such as like bias currents, transistor widths (active loads), and compensation capacitor.

- A new measurement setup has been proposed in order to apply an extremely small signal at the input of the circuit and measuring a very low noise level at the output.

Comparing to the currently available setups, this work proposes a potential candidate for replacing all off-chip components used in the currently available read-out setups with a fully integrated prototype. It can then be considered as an initial step toward the realization of a scalable quantum computer comprising a cryogenic quantum processor and a cryo-CMOS classical electronic controller.

5.2 Future work

5.2.1 Short-Term Goal

The chip layout is ready to be sent for the fabrication. As a short term goal, after chip fabrication, several things needs to be done:

- Initial DC and transient measurement at room temperature in order to confirm the functionality of the chip.

- Comparing the measurement and simulation results and validate the accuracy of the models.

- Measuring the critical specifications of the design, such as noise and bandwidth. The results could also be very useful to characterize the flicker noise at cryogenic temperatures.

5.2.2 Long-Term Goal

- As a long-term goal, it would be very interesting to connect the chip to a real QPC to check the functionality of the circuit with a real QPC (in the actual condition of operation it was designed for).

- Using the measurement data, to create a more accurate MOSFET models at cryogenic temperature (including parameters for transient and noise simulation).

- Testing the chip at temperatures lower than 1 K and investigate the possibility of qubit and read-out co-integration and operation at 4K and below.

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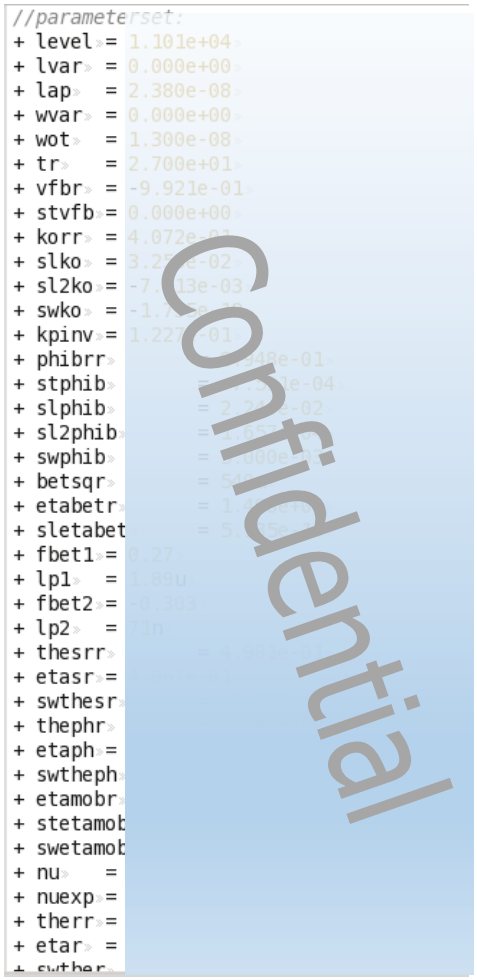
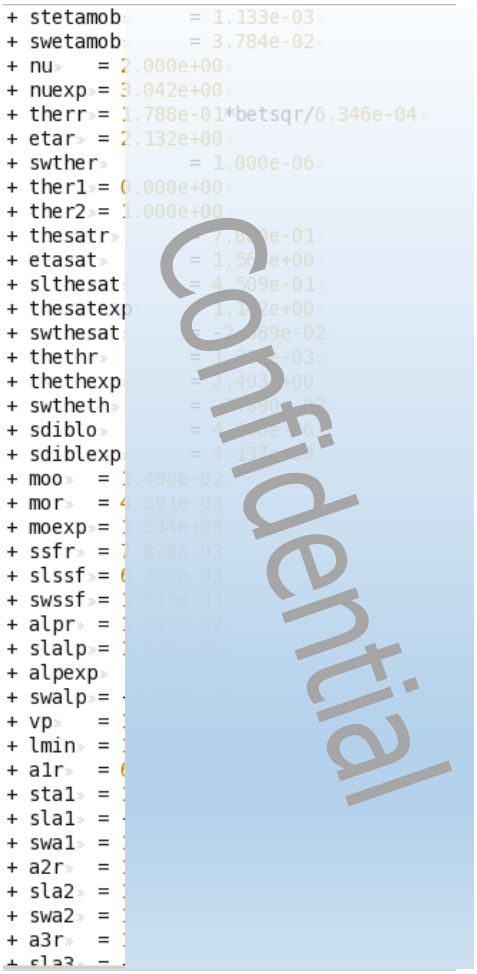
7 Appendix A





Mostly modified parameters in the model**:**

- **UO/MUEO/FBET1:** Mobility related parameters
- **KVTHO:** Threshold shift parameter
- **ALP:** Channel Length Modulation pre-factor