Linearity Research of A CMOS Image Sensor

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Linearity Research of a CMOS Image Sensor

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voorzitter van het College voor Promoties,

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door

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To my beloved families

You’re never too old to set another goal or to dream a new dream.

-*C. S. Lewis*

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Chapter 1 Introduction

Widely used at a global scale, semiconductors play a critical role in pushing the modern society into an electronics era. In the past 50 years, Moore's law has driven wafer size to grow larger in order to sustain cost competitiveness. The quality of lithography, as the costliest process in silicon wafer fabrication, is directly related to the linearity performance of the image sensor used in the mask inspection system. Within this context, an imaging system with excellent linearity performance is needed to meet the resolution and accuracy requirement of the next generation lithography machines. Designing and implementing a CMOS image sensor with high linearity is the primary goal of this thesis.

A short overview of the background is given in Section 1.1. A brief introduction to the imaging systems will be introduced in Section 1.2. Motivation and objects will be presented in Section 1.3. Finally, a summary on the structure of the thesis is given in Section 1.4.

1.1 Background

In 1782, Alessandro Volta, an Italian scientist first used the term "Semiconducting" to describe the properties of same materials that have the combined properties of insulators and conductors [1.1]. Since then, many scientists and engineers have invested on the research of semiconductors. Shockley invented the junction transistor in 1947 [1.2], marking the first milestone in the development of semiconductors technology. The first bipolar integrated circuit (IC) was invented in 1959 by Kilby and Noyce [1.3], which further led to the fabrication of a metal oxide semiconductor (MOS) structure. The course of semiconductors development in the past few decades have arguably an equivalent influence on human history as the Industrial Revolution [1.4]. Semiconductors are key components of all kinds of electronic devices, such as computers, TV, smartphones and other electrical appliances; it has propelled technological advancements which have made life more convenient and intelligent.

Silicon wafers are an essential element in the characterization of integrated circuits [1.4], where the integrated circuits are commonly fabricated on. In the past half-century, Moore's law on: "the number of transistors on integrated circuits double approximately every two years" [1.4] not only increased the transistor density, it also drove the silicon wafer to continuously grow in size. As shown in Figure 1-1, the mainstream wafer size was 100-mm in diameter during the mid-1970's; less than three decades later, most semiconductor manufacturers have upgraded the wafer size to 300-mm in diameter [1.5]. Although the manufacture from 300-mm to 450-mm diameter silicon wafers have been delayed from the anticipated year of 2017 to early 2023 [1.6], semiconductor giants still ambitiously accelerate the conversion, driven by multiple factors including environmental considerations and economic benefits [1.7].

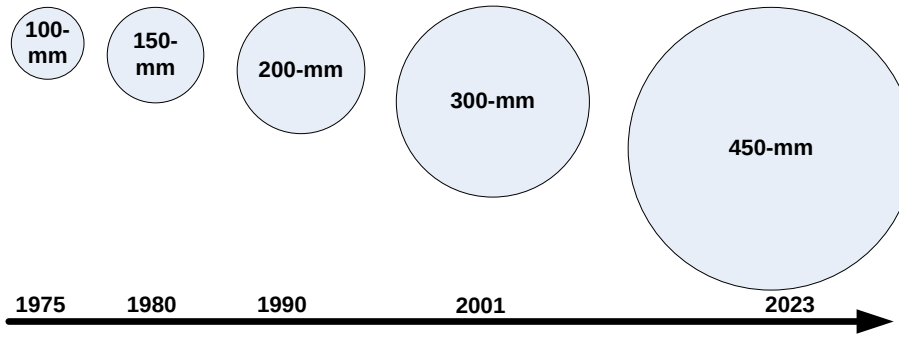

Figure 1-1. The roadmap of silicon wafer size [1.6].

Larger wafers not only increase the utilization efficiency of wafer area but also that of the resources including energy, water [1.7]. Nowadays, a single chip containing millions or billions of transistors is able to perform more complicated functions, thereby inspiring the development of chips with larger size. The Volta GPU chip designed by Nvidia integrates more than 21 billion transistors [1.8]. A larger wafer can also hold more chips, meaning a higher chip throughput can be achieved. As a result, the reduction on the average cost per chip further increases the incentive to make wafer size larger.

Substantial cost savings have intensified the competition of major semiconductor manufacturing companies to develop 450-mm wafer. However, in the transition from 300-mm to 450-mm, there are many technological obstacles on top of financial challenges [1.9]. All equipment from crystal growth to final device testing needs to be upgraded so that it reaches a certain level of precision [1.10]; this requires technological breakthroughs instead of simple linear technological extensions from the existing equipment used in 300-mm wafer fabrication.

For 450-mm wafers, as the most complex and important step in the whole process of the semiconductor manufacturing: lithography, may account for over 60 % of fabrication cost [1.10]. Using a photographic process, lithography "writes" or "prints" precise patterns on a silicon wafer [1.11].

In the lithographic system, a mask inspection system [1.12] is shown in Figure 1-2. Instead of a wafer, a reticle is imaged on a camera system to look for potential defects in the manufacturing process [1.12]. As the wafer manufacturing process is constantly adapting to achieve better resolution and to go beyond size limits, a critical constraint is imposed on the performance of the camera system in the inspection system [1.13]. Notably, the linearity result of the camera is what determines the quality of the inspection system, reflecting the mask errors. In this context, a highly linear imaging system is needed in the lithography machines.

Moreover, linearity is also a crucial property for the image systems in other applications where an accurate relative intensity measurement is essential. In quantitative imaging operations, the nonlinearity of the image sensor must be small enough to perform all types of image analysis including ratio calculations and flat fielding [1.14], [1.15]. In scientific imaging a linearity calibration is usually employed, such as an imaging system used in photoelectron spectroscopy, a substantial deviation from an ideal linear photon response could generate a wrong result in the recorded spectra [1.16].

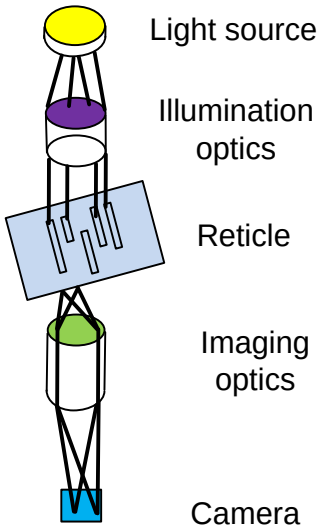

Figure 1-2. Aerial image inspection Tool [1.12].

1.2 Imaging Systems

Silicon-based imaging systems can be categorized as CCD (charge coupled device) and CMOS (complementary metal oxide semiconductor) image sensors system [1.17]. Each imaging system has its own unique strengths and weaknesses depending on how they are applied. Due to the advantages of system-on-chip capability combined with low power consumption and low cost [1.18], as well as the steady improvement on the imaging performances in the past decades, the CMOS image sensors have become the preferred choice.

1.2.1 CCD Image Sensors

CCD and CMOS image sensors share a same fundamental operation principle; they both use a photosensitive element, the photodiode as the primary means to capture photons [1.17]. The main difference lies in the method of conveying the photonic information to the readout circuit [1.17]. For CCDs, the photodiodes convert the incident photons into electrons, which are sequentially shifted from one pixel to the neighboring with MOS capacitors [1.19]. Outside of the pixel array, an amplifier converts the electrons to a voltage which has a linear function with the light intensity. A high-resolution off-chip analog-to-digital converter (ADC) further digitalizes the analog signal.

CCD imagers are able to fully maintain the signal without distortion by adopting particular channel design [1.19] and through obtaining a low noise. The passive principle of charge transfer and the use of a single electronic conversion

chain, including amplifier and ADC, promises excellent uniformity [1.20]. A CCD image sensor also has a higher fill factor and better uniformity than CMOS competitor [1.18]. Due to these advantages, the CCD sensors have dominated the high-end imaging market until recent years, especially for scientific and medical applications.

Nevertheless, the sequential transfer and readout scheme of electrons in the pixel restricts the speed of the CCD sensors [1.21]. To improve charge transfer efficiency of the pixel, a high voltage is used for the control clock of the pixel [1.21]; this process consumes considerable power. More important, being incompatible with CMOS process, CCD image sensor cannot realize system integration as the other circuitry such as a programmable amplifier, ADC and digital process circuitry need to be fabricated on another chip based on a CMOS process [1.17]. Correspondingly, it increases the area of the system as well as the cost. The unique charge transfer mechanism increases the mass production risk that one damaged pixel can ruin the signal capture of the other pixels; thus the yield of CCD sensor is lower, resulting in the higher cost of CCD sensor.

1.2.2 CMOS Image Sensors

The invention of the CMOS sensors occurred around the same time period as the CCD [1.22]. However, the initial poor noise performance restrained its application when it was first introduced in the market. Due to the later technology breakthroughs, in particular with regards to the development of the pinned photodiode (PPD) [1.17], the CMOS sensor became comparable to the CCD sensor in sensitivity and noise performance. Different techniques including the use of the logarithmic pixel [1.23] and dynamic range extension methods [1.24], an even broader dynamic range can be realized from a CMOS image sensor than from a CCD.

Most importantly, it is possible to implement a CMOS image sensor on a single chip [1.17] where pixel array can be integrated together with ADCs, periphery circuits, and digital signal processors, so that the size and the cost of the whole imaging system can be reduced substantially.

Contrary to the CCD sensor, the active pixel of the CMOS image sensors uses an in-pixel amplifier, which increases the readout speed together with the random-access mechanism [1.25]. Currently CMOS image sensors have excellent image quality, comparable to its CCD counterpart; it also has the benefits of system integration ability, low cost, and low power consumption [1.26]. The detailed introduction of the operating principles for a CMOS image sensor will be given in Chapter 2.

1.3 Motivation and Objectives

The ultimate goal of this thesis is to develop a CMOS image sensor with an excellent performance on linearity, which can be used in the next generation of lithography equipment. A small nonlinearity less than 0.1 % is targeted for the image sensor. Different methodologies, from pixel-level to system-level are adopted to linearize the output of the CMOS image sensor.

The primary objectives of this thesis can be summarized as follows: (i) to underline the nonlinearity sources of the CMOS image sensors; (ii) based on the thorough theoretical analysis, to build a behavioral model of the CMOS image sensor on linearity; (iii) to verify the behavioral model through the experimental results of a test chip and (iv) to characterize new types of pixel design aimed for the linearity improvement; (v) to demonstrate different linearity optimization methods from system-level with measurement results of prototypes chip, (vi) to suggest future research directions for this field of work.

1.4 Thesis Outline

This thesis is comprised of eight chapters. The organization of the thesis is arranged as follows.

Chapter 2 gives a literature review. Based on a review of the fundamental principle of photodetection, an overview of the CMOS image sensors is given. Different pixel structures aimed for different applications are introduced. The primary performance indicators of the CIS such as conversion gain, fill factor, linearity and noise are laid out.

Chapter 3 presents a theoretical analysis of the nonlinear errors in the CMOS image sensor based on a 4T pixel structure. A behavioral model of CMOS image sensor's linearity is then proposed; finally, a test chip is used to verify the validity of the linearity model and the theoretical analysis.

In Chapter 4, based on the analysis of Chapter 3, two types of pixel structures are proposed to address the nonlinear errors of the pixel. A prototype image sensor which adopts dual correlated double sampling (CDS) is employed to verify the pixel-level linearity improvement.

In Chapter 5, a digital assistant calibration method is used to compensate the nonlinearity caused by the pixel and readout circuitry. The experimental results fully prove the effectiveness of the calibration method.

Chapter 6 analyses the temperature effect on the pixel performance of a CMOS image sensor. The behavioral model proposed in Chapter 3 is updated with all temperature coefficients of the elements in the pixel. The digital calibration method proposed in Chapter 5 also demonstrates outstanding immunity to the

temperature variation on linearity.

Based on the linearity optimization methods introduced in Chapter 4 and 5, Chapter 7 proposes more techniques to linearize a CMOS image sensor. Several types of pixel structures are presented, especially a novel pixel based on a capacitive transimpedance amplifier (CTIA) structure, which can effectively reduce the nonlinear error caused by the nonlinear integration capacitor. Two other calibration methods are explored to address the drawbacks of the first calibration method employed in Chapter 5.

Chapter 8 concludes the work presented in this thesis and provides a vision for the improvement of the future work.

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Chapter 2 CMOS Image Sensor Overview

This chapter gives an introduction of the CMOS image sensors. The chapter first introduces the principle of photon detection of the CMOS image sensors in Section 2.1. In Section 2.2, the primary pixel's configurations are introduced, such as 3T, 4T, and logarithmic structures. Section 2.3 presents the vital evaluation parameters of the CMOS image sensor such as linearity, noise, dynamic range etc. Finally, a conclusion is outlined in Section 2.4.

2.1 Device Physics of CMOS Image Sensor

The photodiode is the most fundamental photodetector component in the imaging system [2.1], based usually on a simple p-n junction to capture the photogenerated carriers.

When a p-n junction works in the reverse bias condition, with the enhanced internal electric field, the depletion region's width will increase. Without external energy involved, only small leakage current flows in the diode [2.2].

As a photon flux strikes a semiconductor with a sufficient energy value [2.2] higher than the band gap energy of this type of material E_g, electrons will be shifted from a lower energy band (valence band) to a higher energy band (conduction band) [2.2] in the semiconductor. Silicon, gallium arsenide and germanium are three common semiconductor materials, which have a different band gap energy. E_g is also temperature dependent which will be introduced in Chapter 6. In silicon, the minimum E_g to enable a transition of an electron across the band gap at room temperature is around 1.12 eV [2.3].

The energy of the photon E_p is decided by the wavelength of the light λ, which follows Eq. (2-1), where h is Planck's constant; c and v are the speed and frequency of light [2.1].

$$E_p = hv = \frac{hc}{\lambda} \tag{2-1}$$

Figure 2-1 explains the photoelectric effect of the photodiode, where the absorbed photon energy leads to the generation of electron-hole pairs [2.2].

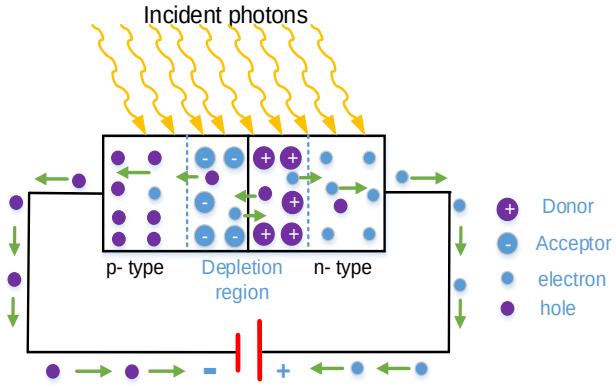

Figure 2-1. The principle of the photodiode [2.2].

The repulsive force due to the internal electric field in the depletion region separates the electrons and holes generated by the photodiode, and accelerates the drifts of the electrons and holes towards the anode and cathode of the p-n diode

[2.2], as shown in Figure 2-1.

In the photodiode, the electric current generated by the absorbed photons is called photocurrent; when an electric current is generated in the absence of light, it is called dark current.

The generated charges are held by the intrinsic capacitance of the photodiode [2.2], and then are converted into a voltage signal with a magnitude proportional to the light intensity [2.2].

There are two typical types of p-n junction diodes shown in Figure 2-2, which are commonly used in the early image sensors with a standard CMOS process.

- n+/ p- sub
- n-well / p- sub

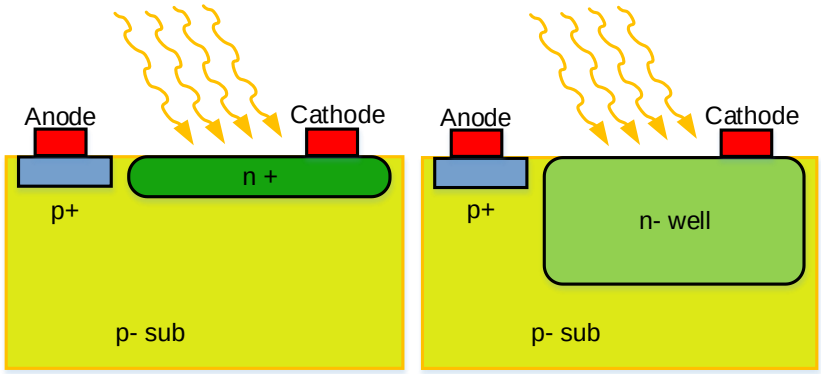

Figure 2-2. The structures of the photodiodes [2.3].

The first structure is the simplest structure, where a high n doping is formed in a p- substrate [2.4]. A high doping concentration leads to a small depletion region width, reducing the collection efficiency and generating a larger junction capacitance.

The second structure still connects the p- substrate to the anode and a lowly doped n- layer to the cathode. The doping of the n layer is relatively lower than the first structure and creates a deeper depletion region where more electrons can be stored [2.4]. However, the minimal spacing from the n-well to the nearby n-wells required by the design rules, also results in a structure with a smaller fill factor.

These two structures cannot realize real CDS with the following readout circuit which will lead to a large kTC noise. Further, the large dark current caused by surface generation also affects the imaging performance. To address these issues that degrade the imaging quality, more complicated structures such as the pinned photodiode structure is currently adopted in the image sensor, which will be explained in the following section.

2.2 Pixel Types

Photodetection in the pixel is realized by the photodiode, while the conveyance of photonic information out of the pixel is carried out by the other components. There are two basic types of pixel structures in a CMOS image sensor: passive pixel and active pixel [2.1].

2.2.1 Passive Pixel

In 1967, Weckler proposed the passive pixel, which laid down a bedrock for the development of the modern image sensor [2.5]. The schematic of the passive pixel is shown in Figure 2-3. The passive pixel includes a photodiode and a switch transistor. The output of the pixels is connected to a transimpedance amplifier placed in the column level or chip level. In Figure 2-3, φ_{RST} is the control signal of the reset transistor and C_{INT} is the integration capacitor of the transimpedance amplifier. In the reset phase, the transistor in the chosen row is activated to reset the photodiode along with the amplifier circuit. In the readout phase, the transistor in the chosen row is activated again to convert the charges accumulated during the integration period. A voltage proportional to the light intensity is achieved by the transimpedance amplifier.

A passive pixel has a high fill factor because it only has one transistor. However, the passive pixel has a large read noise due to the massive capacitive loading [2.5]. The reset switch and integration capacitor C_{INT} also introduce kTC noise [2.6]. The large RC time constant generated by the readout bus restricts the speed of the image sensor. Furthermore, the crosstalk among the pixels also degrades the imaging quality of the sensor [2.1]. These issues halted the development of the passive pixel, which was finally replaced by active pixels.

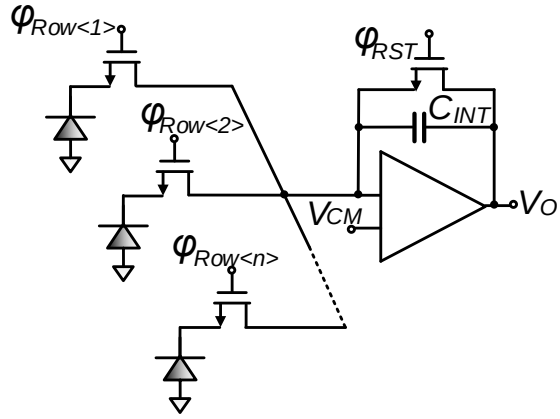

Figure 2-3. Schematic of passive pixel.

2.2.2 Active Pixel

Compared to the passive pixel which has a larger noise, an active pixel employs an in-pixel amplifier and therefore has a better noise and speed performance [2.6]. Due to these advantages, the active pixel has become the primary choice for the CMOS image sensors.

2.2.2.1 3T Pixel

The three transistor pixel structure (3T) is the most straightforward active pixel structure, which is comprised of a photodiode, a reset transistor (RST), a row select transistor (ROW) and a source-follower transistor (SF). The current source for the SF is shared by the pixels in a column. The schematic of this type of pixel is shown in Figure 2-4.

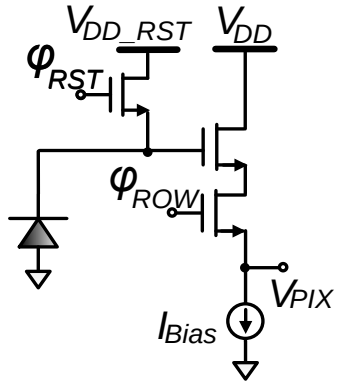

Figure 2-4. 3T pixel schematic.

In a 3T pixel structure, three transistors are employed. Compared to the other pixel's configuration with more transistors, it has a larger fill factor. However, it is difficult to get rid of the reset noise caused by the RST transistor [2.1]. Besides, it is harmful to the performance of the pixel as the direct contact of the photodiode with the silicon-silicon oxide interface, which will generate a large dark current [2.6]. These issues trigger further innovation and improvement on the pixel structures.

2.2.2.2 4T Pixel

In a four transistor pixel structure (4T) shown in Figure 2-5, an additional transfer transistor (TX) is added between the photodiode and the floating diffusion (FD) node. The photodiode in the 3T pixel was replaced by a pinned photodiode.

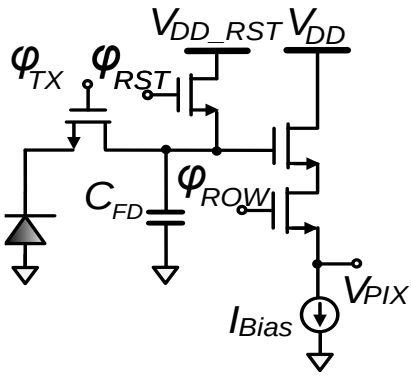

Figure 2-5. 4T pixel schematic.

The pinned photodiode was initially proposed by Teranishi in 1980 adopted in a CCD image sensor to achieve a low image lag performance [2.7]. In 1995, the pinned photodiode was used in the 4T pixel. When the n- layer was placed in between a p- substrate and a highly p+ layer [2.8], a buried structure was created in the form of a fully depleted n layer, demonstrated in Figure 2-6. And the p+ layer and p- sub are both connected to the same bias voltage V_{SUB} which is either a ground voltage or a negative bias voltage. A negative bias voltage can increase the depletion depth and enhance the full-well capacity of the pixel [2.9]. The isolation between n layer and the silicon surface states in the 4T pixel significantly suppressed the dark current.

Furthermore, the integration and transfer process of the generated charges are separated by the TX transistor, thereby enabling real correlated double sampling [2.1]. Thus, the kTC noise can be canceled in the 4T pixel with the assistance of the following CDS circuit.

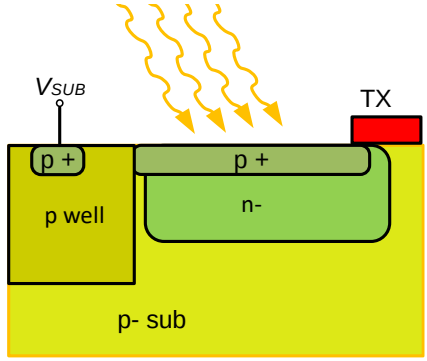

Figure 2-6. The structures of the Pinned photodiode.

A 4T pixel also has a higher electron-to-voltage conversion gain than the 3T pixel, which is determined by the photodiode capacitance. By isolating the FD

node with the photodiode, a 4T pixel attains a small integration capacitor on the FD node C_{FD}, which increases the value of the conversion gain. In general, a 4T pixel has a better noise performance, a larger conversion gain and a smaller dark current at the cost of a complicated process. Some extra masks are required in 4T pixels, which increases the cost of the imager.

2.2.2.3 Logarithmic Pixel

The logarithmic active pixel was introduced in 1984 [2.10], which uses a nonlinear readout technique with the advantage of high dynamic range. This type of pixel is commonly used in applications that require a broad dynamic range, such as the human visual system. The schematic is shown in Figure 2-7.

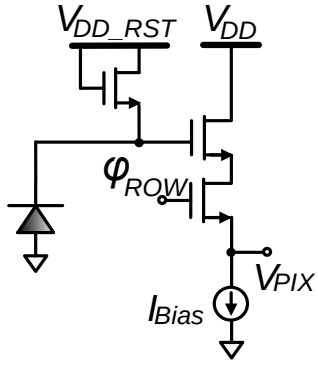

Figure 2-7. The schematic of logarithmic pixel.

This type of pixel does not include a reset transistor and the output response is continuous [2.10]. The small photocurrent I_{ph} in the pixel drives a diode-connected MOS transistor to work within the subthreshold region [2.10], whose current I_d follows Eq. (2-2).

$$I_d = I_{S0}\frac{W}{L}(e^{\frac{V_{PD}}{nU_T}} - 1) \tag{2-2}$$

Where W and L are channel width and length of the transistor; U_T is the thermal voltage; V_{PD} is the voltage on the photodiode; I_{S0} is the drain current when the gate-source voltage of the transistor V_{GS} equals to the threshold voltage V_{th} [2.10]; n is the subthreshold slope factor decided by the capacitance ratio of the depletion layer and the oxide layer [2.11].

The voltage on the PD node is therefore logarithmically proportional to the light intensity [2.11], shown in Eq. (2-3), which further generates a logarithmic output voltage of the pixel.

$$V_{PD} = V_{DD\_RST} - nV_T \ln(I_{ph} / I_{S0}) - |V_{th}| \quad (2\text{-}3)$$

By encoding the photocurrent into a logarithmic function, the logarithmic pixel attains a large dynamic range [2.10]. Compared with other types of pixel, the logarithmic pixel's dynamic range is restrained by the electrical range of transistors, rather than the photodiode's full-well capacity [2.11].

However, when the transistor is working in the subthreshold region, a large in-pixel fixed pattern noise is caused by the high sensitivity of the transistors to variations in threshold voltage [2.12]; and the photodiode current has a strong temperature dependence. Furthermore, the logarithmic pixel also has a considerable image lag and low sensitivity [2.12]. All these drawbacks make it unappealing for wide usage. In [2.12]-[2.13], several pixel structures with combined linear and logarithmic response have been proposed to achieve a compromise between high dynamic range and other pixel's merits.

2.2.2.4 Capacitive Transimpedance Amplifier Pixel

In the passive pixels, a capacitive transimpedance amplifier is usually used to convert the accumulated charges to a voltage at a column-level or chip-level. However, the pixel structure suffers from a considerable read noise and a low sensitivity. In-pixel CTIA is adopted, which can achieve better sensitivity and linearity [2.14], [2.15].

The CTIA pixel consists of a photodiode, an integration capacitor, a transimpedance amplifier and a reset switch. The amplifier can be realized by a simple CMOS inverter structure shown in Figure 2-8 (a), or a differential amplifier shown in Figure 2-8 (b), where C_{PD} is the parasitic capacitor of the photodiode; C_F is the integration capacitor in the feedback loop and the reset transistor is controlled by the signal φ_{RST}.

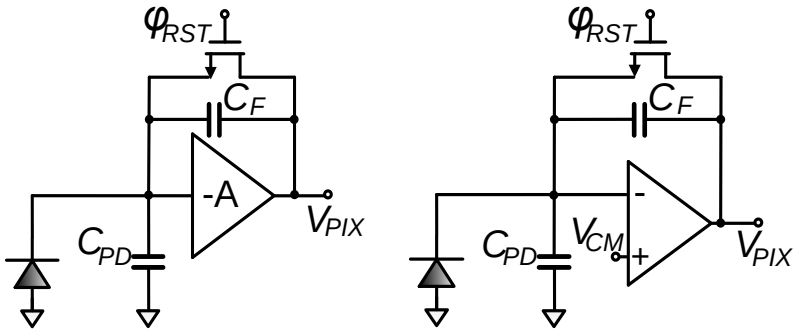

Figure 2-8. CTIA pixel (a) with an inverter structure; (b) with a differential amplifier structure.

In these two-pixel structures, when φ_{RST} is activated, the input and output of the amplifier are connected together [2.15], generating a reset voltage. In Fig 2-8 (a), the reset voltage is decided by the gate-source voltage of the input transistor in the amplifier, which is sensitive to the process variation, while in Fig 2-8 (b) the reset value is equal to the reference voltage V_{CM}.

When the reset transistor is switched off, charges generated by the photodiode are accumulated on the feedback capacitor C_F instead of the photodiode capacitor C_{PD}. With a small C_F, the pixel can achieve a high conversion gain. The feedback capacitor is usually implemented by a metal-insulator-metal (MIM) capacitor or metal-oxide-metal (MOM) capacitor, which has a low voltage coefficient. As a result, this type of pixel achieves an outstanding linearity [2.14]. If the open gain of the amplifier is large enough, the CTIA output is determined by the photodiode current, integration time T_{INT} and C_F, expressed as

$$V_{PIX} = \frac{I_{ph} T_{INT}}{C_F} \tag{2-4}$$

However, the CTIA pixel has a smaller fill factor than the other pixel structures. The small capacitance used in the closed loop of the pixel caused a large mismatch due to the process variation. The fixed-pattern noise (FPN) of the CTIA pixel is worse than the conventional 3T or 4T pixel [2.14]. Furthermore, the switch transistor also generates a larger leakage current which degrades the imaging performance under low illumination.

2.2.2.5 Digital Pixel

To realize high speed, the digital pixel structure is first proposed in the image sensor by the researchers from Stanford University in 1994 [2.16]. The schematic is shown in Figure 2-9, where an ADC is employed inside the pixel.

In digital pixels, the conversion error caused by the column level mismatch is reduced [2.16] when the column readout circuit is absent; correspondingly, a higher SNR is achieved with the digital pixel. It realizes high speed by means of pixel-level digitalization. This type of pixel structure is adopted in some scientific applications which need an extremely large frame rate. However, the small fill factor and larger FPN limit its applications in commercial image systems.

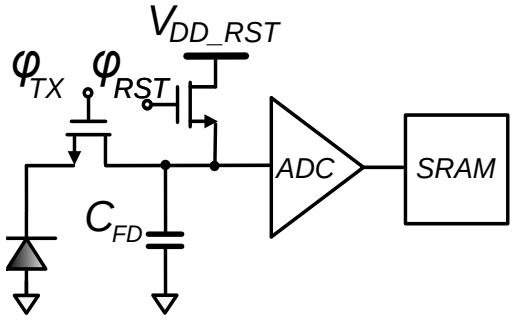

Figure 2-9. The schematic of the digital pixel.

2.2.2.6 Other Types of Pixels

Many other pixel structures have been proposed based on the 3T and 4T pixel design, aimed for different applications.

For some linear image sensors, the pixel adopts the structure of direct injection (DI) [2.17] and gate modulated injection (GMI) [2.18] to improve the linearity. In the mobile phone application, the pixel sharing structures are commonly employed to realize a high fill factor, where the transistors including the RST, SF and ROW transistors are shared with several photodiodes; the number of transistors per photodiode can amount to 2.5T, 1.75T, or 1.5T [2.19], [2.20]. To achieve a high speed, a 5T pixel enables global shutter operation which uses an additional transistor compared to the 4T pixel [2.21]. Pixel structures with more transistors such as 6T and 8T pixels, which combine pixel-CDS with global shutter, have been proposed to improve the noise performance [2.22].

2.3 Performance Metrics

In this section, the most fundamental performance indicators of a CMOS image sensor will be reviewed.

2.3.1 Fill factor (FF)

Pixels are composed of photodiodes and transistors; sometimes capacitors are also added, such as the CTIA pixel and the digital pixel. The fill factor of a pixel quantifies the ratio of the area of the photo-sensitive region A_{PD} over the total pixel size A_{PIXEL}, shown in Eq. (2-5).

$$FF = \frac{A_{PD}}{A_{PIXEL}} \tag{2-5}$$

Within a certain pixel size A_{PIXEL}, the pixel with a larger fill factor tends to have a higher sensitivity as more photons can be collected in a larger photodiode if the value of the integration capacitor is fixed. Shared pixel structures are commonly used in the image sensors that adopt front side-illumination (FSI) technology to optimize the fill factor. Furthermore, micro lenses are employed to focus the light on the photoactive region [2.1], thereby improving the effective fill factor in modern CIS.

Furthermore, high-end imaging systems are widely adopting backside illumination (BSI) technology, where photodiodes are placed on the front side while the other elements such as transistors and metal wires are placed on the backside. With the employment of this technology, the fill factor can be improved to a theoretical value of up to 100 % [2.23].

2.3.2 Conversion Gain (CG)

The amount of voltage variation of one electron is defined as the conversion gain of an image sensor [2.24]. The value of the conversion gain in a CMOS image sensor is decided by the capacitance value of the integration capacitor C_{INT} and in-pixel buffer's gain A (such as the gain of the SF in a 4T pixel).

$$CG = \frac{q}{C_{INT}} A \tag{2-6}$$

For a CMOS image sensor, to realize a higher conversion gain and to achieve a lower noise, more studies have been conducted to reduce the value of the integration capacitor, reported in [2.24], [2.25].

2.2.3 Full-well Capacity (FWC)

An important parameter that decides the dynamic range of the image sensor (see 2.2.9) is the full-well capacity. Without the range limitation of the following amplifier and ADC, full-well capacity is defined as the maximum amount of charge stored in the photodiode [2.26], which follows Eq. (2-7).

$$N_{sat} = \frac{1}{q} \int_{V_{RST}}^{V_{MAX}} C_{PD}(V) \cdot dV \tag{2-7}$$

In Eq. (2-7), N_{sat} is the maximum amount of charge and C_{PD} is the photodiode capacitance, q is the charge of an electron; V_{RST} and V_{MAX} is the reset voltage and the saturation voltage respectively.

There are many factors that affect the value of FWC, such as the photon flux and the low voltage of the TX transistor reported in [2.26], [2.27]. The FWC is

generally directly proportional to the light-sensitive area. Furthermore, the FWC is also temperature related [2.28], the detailed analysis of the temperature dependency on the value of FWC will be discussed in Chapter 6.

2.2.4 Quantum Efficiency (QE)

Quantum efficiency is used to evaluate a pixel's capability to convert the impinging photons to the collected electron-hole pairs [2.1]. The value follows Eq. (2-8).

$$QE = \frac{N_e}{N_p} \cdot 100\% \tag{2-8}$$

In Eq. (2-8), N_p is the amount of the impinging photons while N_e is the corresponding number of the carriers collected by the pixel. As introduced in Section 2.1, the photon energy depends on its wavelength and material. Correspondingly, the value of the quantum efficiency has a spectral dependency. It also relates to the geometrical characteristics of the photodiode [2.29]. The measurement of the QE is a little different with the test setup of the other parameters. A monochromator with a multi-wavelength light source is required to generate a desired wavelength. The detailed optical setup will be introduced in Chapter 4.

2.2.5 Frame Rate (FR)

The frame rate is a parameter to evaluate how many images a sensor can capture in one second [2.1]. The frame rate is commonly related to the architecture and resolution of the CIS. The image sensor that adopts digital pixels usually has the highest frame rate. For an image sensor with a larger pixel array, the image sensor with column-parallel architecture usually attains a higher frame rate than its counterpart with global ADC.

2.3.6 Linearity

Linearity is a parameter that evaluates the level at which the actual measured curve of a function is consistent with the ideal curve; the deviation between both is usually specified in terms of nonlinearity. The definition for the nonlinearity of an image sensor is quite similar to the nonlinearity of an ADC. In the ADCs, differential nonlinearity (DNL) and integral nonlinearity (INL) are two parameters to evaluate the linearity performance of the ADC.

In an ADC, DNL is defined as the deviation of the actual step from the ideal step width [2.30]; in an image sensor, DNL can be regarded as the deviation between the differential value of two consecutive incremental output signal and their

corresponding ideal differential values.

Similar to the definition in an ADC, the INL of the image sensors was defined as the deviation of the output curve from an ideal photon response [2.30]. And INL is usually employed to express the sensor's linearity performance in the image sensors.

There are two methods employed to measure the nonlinearity of the image sensor:

- Varying the intensity of a light source linearly with a fixed exposure time for the image sensor;
- Increasing the exposure time of the sensor at a fixed light condition.

Compared to the complexity in controlling the level of a light intensity increase in a linear way, it is much easier to plot the mean signal value versus a linear increasing exposure time for the image sensor. As shown in Figure 2-10, a linear least-squares regression line is plotted to fit the test data after the offset is removed. The results on the nonlinearity of the CIS system is derived from the deviation of all test data from the fit line. The nonlinearity can be calculated as Eq. (2-9) [2.30],

$$Nonlinearity = \frac{(|\delta_{max}| + |\delta_{min}|)}{2} \cdot 100\% \tag{2-9}$$

where δmax and δmin is the maximum and minimum deviation expressed in percentage, shown in Figure 2-10.

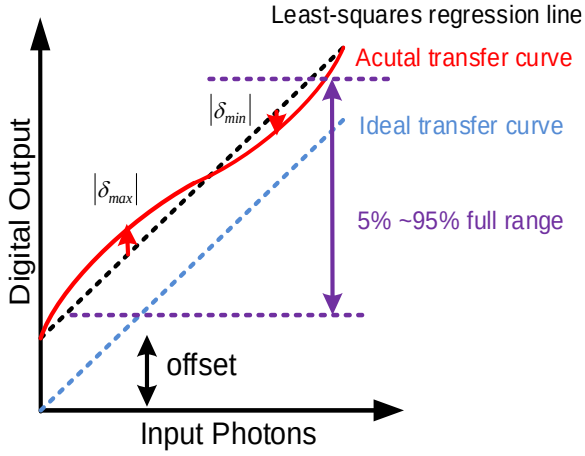

Figure 2-10. The nonlinearity definition [2.30].

In the image sensor, when the pixel is about to reach full-well capacity with generated carriers, the nearly full-well will degrade the linearity performance of the pixel by reducing the probability of electrons captured [2.30]. According to EMAV1288 measurement standard [2.31], a range of 5 % to 95 % of the

saturation capacity is chosen to calculate the nonlinearity. Many factors affect the linearity of the image sensor. A detailed linearity analysis of the image sensor will be given in Chapter 3.

2.2.7 Noise

Noise sources in a photodetector are typically categorized as spatial noise and temporal noise [2.32]. The non-uniform response of the image sensor caused by components' mismatch is defined as spatial noise. Also known as fixed-pattern noise, spatial noise can be found in a fixed position in an image. Human's eyes are especially sensitive to the column FPN which is mainly due to the process variation in a column level circuit. Another type of noise fluctuates over time [2.32], as such it became referred to as temporal noise.

2.2.7.1 Spatial Noise

Spatial noise usually uses two parameters to conduct an evaluation, including dark signal non-uniformity (DSNU) and photon response non-uniformity (PRNU) [2.33]. DSNU is a non-uniform variation in the pixels' output voltage in a dark condition [2.32], which can be regarded as an offset error. The primary sources of the DSNU come from two parts. The first part originates from the mismatch of components in the circuit, which was independent of the exposure time, and could be suppressed by techniques such as CDS or dual CDS. The second part is the dark current of the pixel, which will be explained in a separated subsection.

PRNU is the variation in the pixels' output voltage with illumination. Contrary to the DSNU, PRNU is proportional to the illumination condition, which was referred to as gain error. PRNU mainly comes from the non-uniformity in the conversion of photon-electron and electron-voltage [2.33]. A look-up table can be adopted to attenuate the gain error of the image sensor [2.34].

In general, FPN can be eliminated by further processing in the analog and digital domain.

2.2.7.2 Temporal Noise

The temporal noise cannot be eradicated by digital processing as spatial noise, which becomes paramount in the image sensor. The temporal noise comes from every block of the image sensor: pixel, amplifier and ADC. Temporal noise mainly includes shot noise, reset noise, thermal noise and flicker noise [2.32].

Shot noise is usually caused by the statistical variation of absorbed photons [2.32] as well as by the statistical variation in number of dark-current generated electrons.

Thermal noise caused by the charge carriers' thermal fluctuation [2.1] is the

most primary noise source in the image sensor. All transistors and resistors contribute to thermal noise.

Reset noise in the image sensors is same as kTC noise in analog circuit, which is from the thermal noise of the reset transistor sampled by the integration capacitor [2.32]. In a 4T pixel, kTC noise can be canceled by the following CDS operation; it is also the primary reason why the 3T pixel was finally replaced by 4T pixel.

Flicker noise is also considered as a significant noise source in the CMOS circuit, caused by interface oxide traps [2.32]; flicker noise is also referred to as 1/f noise as the spectral density is inversely proportional to the frequency [2.32]. However, to a large extent, flicker noise is suppressed by CDS circuit.

2.2.8 Dark Current (DC)

Dark current is the current flowing in the photodiode in dark, mainly determined by the fabrication technology [2.32]. The value of the dark current is affected by many factors such as doping concentration, lifetime of the minority and majority carriers [2.35], and the geometrical shapes of the photodiode. Furthermore, the value is strongly temperature-dependent.

Dark current is a critical parameter that decides many other parameters such as signal-to-noise ratio and noise performance. Dark current consists of several components [2.36], such as the thermal generation current created in the depletion region, the diffusion current that comes from the bulk, as well as the leakage current from the surface of the pixel due to the defect states [2.35].

In modern CIS, a 4T pixel is commonly employed where the additional p+ layer efficiently isolates the depletion region and the silicon surface, leading to a significant reduction of the dark current.

2.2.9 Dynamic Range (DR) and Signal-to-Noise Ratio (SNR)

In the image sensors, the dynamic range can be calculated as the ratio of maximum measurable signal V_{max} of a pixel to its minimum measurable signal V_{min} [2.36], limited by the temporal noise of the circuit. Dynamic range affects the performance of the image sensor in distinguishing details under a very bright and dark conditions [2.36].

$$DR = 20log(\frac{V_{max}}{V_{min}}) \tag{2-10}$$

Besides the reduction on the readout noise, increasing the FWC and storing more electrons in the photodiode is another way to increase the DR, which is determined by the size of the photon-sensitive region of the pixel. Within a limited pixel size, many methods are proposed to extend the dynamic range of the image

sensors, such as the logarithmic pixel mentioned in section 2.2.2. However, the large FPN of this type of pixel structure degrades the image quality. Multiple exposure or multiple integration capacitor techniques are applied on a linear pixel which effectively extend the DR range [2.37], [2.38].

The SNR and the DR of the imager are often related. The SNR of the image sensors is the ratio of the output signal at a specific input signal and the corresponding noise signal [2.39], shown in Eq. (2-11), where V_{out} is the output signal of the image sensor while δV_{out} is the noise presented in the V_{out} [2.39].

$$SNR = 20log(\frac{V_{out}}{\delta V_{out}}) \tag{2-11}$$

In Eq. (2-11), the noise of SNR includes signal related noise, for instance, the photon shot noise that is equivalent to the square root of the signal. As such, an image sensor usually achieves a smaller SNR value than the DR. With a strong illumination, the photon shot noise has become the dominant noise source [2.32].

2.4 Conclusion

In this chapter, the main pixel structures of the image sensors and some critical evaluation parameters are introduced. The imaging performance relies on the pixel structure and the detailed application. 4T pixel is one of the most popular pixel structures due to it's outstanding balance among the evaluation parameters. The linearity analysis of the image sensors based on a 4T pixel structure will be presented in the next chapter.

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Chapter 3 Linearity Analysis of a CMOS Image Sensor

This chapter of the thesis is based on the publication :

F. Wang, A. J. P. Theuwissen, "Linearity analysis of a CMOS image sensor," in *Proc. Electronic Imaging*, San Francisco, pp. 84-90, Jan. 30 - Feb. 2, 2017.

In this thesis, linearity is the most critical parameter of a CMOS image sensor. This chapter provides a theoretical analysis on the linearity of the CIS system based on a 4T pixel structure and proposes a behavioral model with MATLAB.

A prototype chip designed in a 0.18 μm, 1-poly and 4-metal CMOS process technology is used to verify the proposed model. The pixel array of the test array is 80 × 160 with a pitch of 15 μm, containing dozens of groups of pixels with different design parameters. The measurement results confirmed the factors affecting the linearity, which can guide future CMOS image sensor designs to achieve a better linearity.

In this chapter, the linearity in a CMOS imaging system is first introduced. The detailed theoretical linearity analysis of a CMOS image sensor and the model of the CIS's linearity are presented in Section 3.2. A test chip with multiple groups of pixels with different pixel parameter designs is presented in Section 3.3. The measurement details are presented in Section 3.4, and finally a conclusion is given in Section 3.5.

3.1 Introduction

In all imaging systems, there is a nonlinearity between the input luminance intensity and the digital output response. For most commercial imaging systems, the linearity requirement is not so stringent. Sometimes, the deviations from a linear response in camera systems are intentionally built to serve different purposes [3.1]. For example, gamma correction is added to code the luminance into a perceptually uniform domain [3.1]. In [3.2], the nonlinear characteristics of the pixel are used to increase the dynamic range of the image sensors.

However, linearity is still a crucial property for image systems in many applications [3.3], in particular with image quality that rely on absolute signal measurements. In quantitative imaging operations, the image sensor must be linear enough to perform an image analysis [3.3], [3.4]. For scientific imaging, the linearity of the image sensor usually constrains the performance of spectral reconstruction.

Due to the advantages of system-on-chip capability with lower power consumption and low cost, as well as the technological breakthroughs in imaging performances in the past decades, the CMOS image sensors have already become the preferred choice in comparison with the CCD competitor.

A CMOS image sensor is a complex, multi-physical heterogeneous system consisting of optical components and electronic blocks. Using photodiodes to convert photons into electrons, an electrical signal is obtained proportional to the light intensity. The electrical signal is then further processed, through amplification and digitization by the readout circuit. Every step introduces a nonlinear error to the image sensor. In the CMOS image sensors, the nonlinear electron-to-voltage conversion is dominant [3.5]. The detailed linearity analysis of a CMOS image sensor is given in the following section.

3.2 Linearity Analysis of a CIS

In this section, the linearity analysis of a CMOS image sensor based on a traditional 4T pixel is presented. A functional block diagram for a typical CMOS image sensor system is depicted in Figure 3-1, represented by five blocks. Photodiodes absorb incident photons and generate a flow of current in the pixel circuit [3.6]. The total capacitance C_{FD} on the floating diffusion node transforms the generated electrons to a voltage. A source follower is used to drive the loading circuit. A column-level or global-level amplifier provides extra gain and noise reduction, especially under low illumination conditions. Finally, an ADC digitalizes the analog output into digital signals to be further processed. The input of the imaging system is an average number of incident photons (P) under unit

exposure time, and the final output is a digital number (DN). Ideally, the transfer function between the incident photon number and the final digital output of the ADC should vary linearly [3.6]. However, each block introduces a nonlinearity; the output signal cannot be simply regarded as a value directly proportional to the photon input.

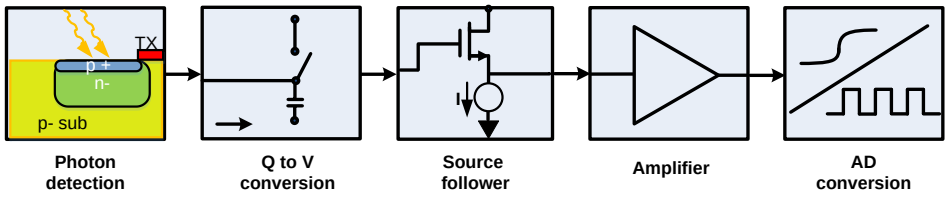

Figure 3-1. The diagram of a CMOS image sensor.

The photocurrent of the photodiode is linear to the incident light level. Pinned photodiodes are now widely used to bring down the dark current and noise, which limit the linearity of the photocurrent in the photodiode developed in the early stage, especially in the weak illumination conditions [3.7]. For this reason, the nonlinearity resulting from the photodiode is ignored. In other words, it is assumed that the conversion from the photons to electrons by the photodiode is linear.

The ADC and the amplifier can achieve excellent linearity with an elaborate circuit design. The nonlinearity of the pixel is mainly caused by the inconsistent source follower's gain and the nonlinear integrating capacitor C_{FD}.

Figure 3-2 shows the schematic of a typical voltage mode 4T pixel. The pixel circuit consists of a pinned photodiode, a charge transfer switch (M1), a reset switch (M2), a source follower (M3) and a row select switch (M4). The current source transistor (M5) is shared by multiple rows of pixels and the current is variable by changing the bias voltage V_{LN}; V_{PIX} is the output voltage of pixel. In the following analysis, the nonlinearity caused by the row select transistor (M4) is omitted to simplify the analysis; V_{DD} is the power supply of the pixel while V_{DD_RST} is the high voltage for the reset switch.

The SF is used to drive the load circuit. The size of the SF is usually designed as small as possible to achieve a higher fill factor. Eq. (3-1) shows the small-signal voltage gain (G_{SF}) of the SF, where $g_{m,SF}$ and $g_{mb,SF}$ are the gate-to-drain and the bulk-to-drain transconductances of the SF transistor; the factor χ is the ratio of $g_{m,SF}$ and $g_{mb,SF}$; R_S is the finite output resistance of the current source; γ represents the body effect; φ_F defines the Fermi potential of the semiconductor and V_{SB} is the source-to-substrate voltage. The nonlinear gain of the SF degrades the linearity of the image sensor, as it changes with the output voltage of the pixel V_{PIX}.

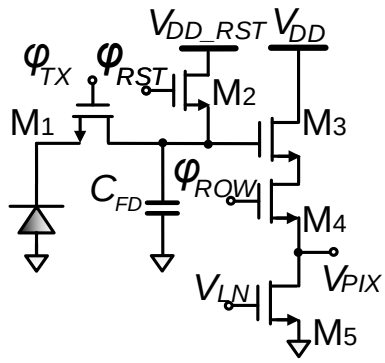

Figure 3-2. The Schematic of the 4T pixel.

Due to the body effect of the SF and finite output resistor of the current source [3.8], the gain of the SF is not a constant value, as shown in Eq. (3-1).

$$G_{SF} = \frac{g_{m,SF} \cdot R_S}{(g_{m,SF} + g_{mb,SF}) \cdot R_S + 1} = \frac{g_{m,SF}}{(g_{m,SF} + \chi \cdot g_{m,SF}) + 1/R_S}$$
$$= \left(1 + \frac{\gamma}{2 \cdot \sqrt{2\varphi_F + V_{SB}}} + \frac{1}{g_{m,SF} \cdot R_S}\right)^{-1} = \left(1 + \frac{\gamma}{2 \cdot \sqrt{2\varphi_F + V_{PIX}}} + \frac{1}{g_{m,SF} \cdot R_S}\right)^{-1} \quad (3\text{-}1)$$

When the transistor is working in saturation, its current follows Eq. (3-2), where λ is the channel-length modulation parameter; C_{ox} is unit oxide capacitance and μ is the field-effect mobility of the transistor; W and L are the transistor's width and length; V_{th} is the transistor's threshold voltage; V_{GS} and V_{DS} are the gate-to-source and the drain-to-source voltages of the transistor.

$$I = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 (1 + \lambda \cdot V_{DS}) \quad (3\text{-}2)$$

The finite output resistance of the current source varies with the bias current I_S and it can be expressed as:

$$R_S \approx \frac{1}{\lambda I_S} \quad (3\text{-}3)$$

Together with Eq. (3-3), we can derive the value of $g_{m,SF} \cdot R_S$, which is shown in Eq. (3-4).

$$g_{m,SF} \cdot R_S = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \left(\frac{W_{SF}}{L_{SF}}\right) \cdot (1 + \lambda \cdot V_{DS})} \cdot \frac{1}{\lambda \cdot \sqrt{I_S}} \quad (3\text{-}4)$$

In Eq. (3-4), W_{SF} and L_{SF} are the width and length of the SF. Combining Eq. (3-2) and Eq. (3-4), results in the gain of the SF follows Eq. (3-5). The value of G_{SF} is determined by the bias current and transistor size, and G_{SF} varies with $V_{PIX.}$

$$G_{SF} = \left(1 + \frac{\gamma}{2 \cdot \sqrt{2\varphi_F + V_{PIX}}} + \frac{\lambda \cdot \sqrt{I_S}}{\sqrt{2 \cdot \mu \cdot C_{ox} \cdot (W_{SF} / L_{SF}) \cdot (1 + \lambda \cdot (V_{DD} - V_{PIX}))}}\right)^{-1} \quad (3\text{-}5)$$

V_{FD} is the voltage on the FD, and it is related to the output voltage of the pixel. The value of V_{FD} can be calculated as Eq. (3-6).

$$V_{FD} = V_{PIX} + \sqrt{\frac{2 \cdot I_S}{\mu \cdot C_{ox} \cdot (W_{SF} / L_{SF}) \cdot (1 + \lambda \cdot (V_{DD} - V_{PIX}))}} + V_{th,SF} \quad (3\text{-}6)$$

The threshold voltage of the SF can be expressed in Eq. (3-7), with V_{th0} being the zero-bias threshold voltage. The value of $V_{th,SF}$ thus has a voltage dependency on V_{PIX}.

$$V_{th,SF} = V_{th0} + \gamma \cdot (\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F}) = V_{th0} + \gamma \cdot (\sqrt{2\varphi_F + V_{PIX}} - \sqrt{2\varphi_F}) \quad (3\text{-}7)$$

In a 4T pixel, another factor affecting the linearity performance of the pixel is the integration capacitance C_{FD}. All transistors in the pixel except the row select transistor are connected to the FD node, which means that the TX, the RST and the SF transistors all contribute parasitic capacitors to the whole value of $C_{FD.}$

First, a review of the capacitance model of a single transistor is introduced to assist the analysis on C_{FD}. Shown in Figure 3-3, between every two of the four terminals of a transistor a capacitor is present [3.8]. There are five capacitances: C_{GS}, C_{GD}, C_{GB}, C_{SB} and C_{DB} among the four terminals.

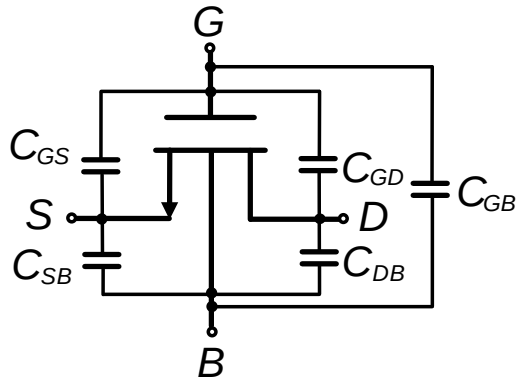

Figure 3-3. The capacitance model of the transistor [3.8].

The overlap capacitances originate from the overlap region between the gate-to-source and gate-to-drain [3.8]. In the transistor, the value of the gate-to-drain and gate-to-source overlap capacitances follow Eq. (3-8), where *Xd* is the channel overlap length and *W* is the width of the transistor.

$$C_{GS\_OV} = C_{GD\_OV} = WXdC_{ox} \tag{3-8}$$

Junction capacitances exist between the source/drain region and the substrate [3.8], consisting of the bottom-plate junction capacitance C_J and sidewall capacitance C_{JSW} [3.9]. The value of C_J follows Eq. (3-9), where C_{J0} is the zero-bias junction capacitance per unit area; φ_B is the built-in potential of the bottom; V_R is the reverse bias voltage and M_J is junction grading coefficient of the bottom area [3.9].

$$C_J = \frac{C_{J0}}{(1+V_R/\varphi_B)^{M_J}} \tag{3-9}$$

C_{J0} can be calculated by Eq. (3-10), where ε_r is the relative permittivity of the silicon while ε_0 is the permittivity of free space [3.8]; q is the electronic charge; N_A and N_D are the doping concentrations of the p- and n- type materials [3.8], respectively.

$$C_{J0} = \left[\frac{\varepsilon_0 \cdot \varepsilon_r \cdot q}{2\varphi_B} \cdot \left(\frac{N_A N_D}{N_A + N_D} \right) \right]^{\frac{1}{2}} \tag{3-10}$$

Similarly, the sidewall capacitance C_{JSW} is given in Eq. (3-11), where C_{JSW0} is the normalized capacitance per unit length; φ_{BSW} is the built-in potential of the sidewalls, and M_{JSW} is the junction grading coefficient of the side-walls capacitance [3.9].

$$C_{JSW} = \frac{C_{JSW0}}{(1+V_R/\varphi_{BSW})^{M_{JSW}}} \tag{3-11}$$

In the junction sidewalls of the transistor, the source/drain regions contact with the regions with a higher p doping density than the substrate [3.9]. The sidewall zero-bias capacitance C_{JSW0} is shown in Eq. (3-12), where $N_{A(sw)}$ is the sidewall doping density and φ_{BSW} is the built-in potential of the side-wall junction [3.9].

$$C_{JSW0} = \left[\frac{\varepsilon_0 \cdot \varepsilon_r \cdot q}{2\varphi_{BSW}} \cdot \left(\frac{N_{A(SW)} N_D}{N_{A(SW)} + N_D} \right) \right]^{\frac{1}{2}} \tag{3-12}$$

As a result, the total capacitances caused by the junction capacitance can be written as in Eq. (3-13), where A is the junction area and while P is the perimeter.

$$C_{DB} = C_{SB} = C_J A + C_{JSW} P \tag{3-13}$$

The value of the intrinsic capacitance relies on the transistor's operation region. When the transistor works in the cutoff region, no carriers flow in the channel, leading to a zero gate-to-channel capacitance [3.10].

$$C_{GS} = C_{GD} = 0; C_{GB} = WLC_{ox} \tag{3-14}$$

When the transistor works in the saturation region, due to the non-uniform electric field, different amount of charges are present at the source and drain, leading to an unequal split gate oxide capacitance between the source and drain [3.10]. Eq. (3-15) gives the estimated value.

$$C_{GS} = \frac{2}{3} WLC_{ox}; C_{GD} = 0; C_{GB} = 0 \tag{3-15}$$

When the transistor works in the linear region, the charge in the channel is uniformly distributed from the source to drain, where the gate-to-channel capacitance is shared equally by the source and drain [3.10], shown in Eq. (3-16).

$$C_{GS} = C_{GD} = \frac{1}{2} WLC_{ox}; C_{GB} = 0 \tag{3-16}$$

After the review of the capacitance model of the single transistor, the capacitance value of C_{FD} can be calculated. A cross-sectional view of the C_{FD} is shown in Figure 3-4. C_{FD} can be categorized into metal capacitance, overlap capacitance, p-n junction capacitance and gate-channel capacitance [3.11], [3.12].

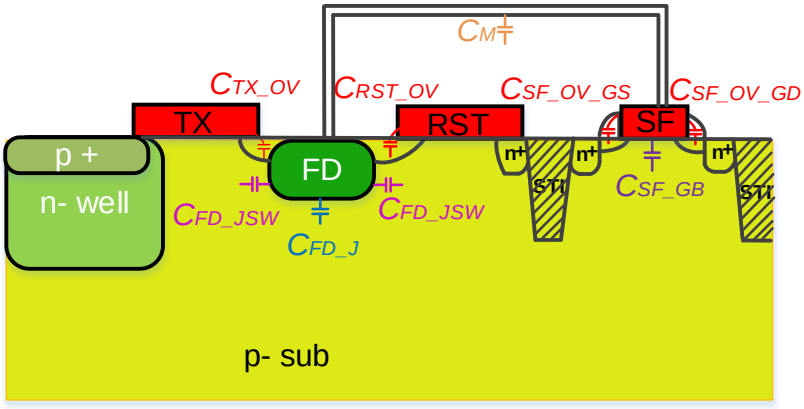

Figure 3-4. A cross-sectional view of C_{FD}.

When the photonic signal of the pixel is read out, the RST and TX transistors are turned off, which contribute to the overlap capacitances, while the source follower transistor works in the saturation region. As shown in Figure 3-4, C_{TX_OV}, C_{RST_OV} and C_{SF_OV} are the overlap capacitances of the TX, the RST and the SF transistors, respectively, while Xd_{TX}, Xd_{RST}, Xd_{SF} and W_{TX}, W_{RST}, W_{SF} are the channel overlap lengths and widths of these transistors, correspondingly. C_{SF_OV} consists of $C_{SF\_OV\_GS}$ and $C_{SF\_OV\_GD}$, which are the gate-to-source and the gate-to-drain overlap capacitances of the SF, and C_{SF_OV} changes with the SF's gain due to the Miller effect.

$$C_{SF\_OV} = C_{SF\_OV\_GS} + C_{SF\_OV\_GD} = W_{SF} \cdot Xd_{SF} \cdot C_{ox} \cdot (1 - G_{SF}) + W_{SF} \cdot Xd_{SF} \cdot C_{ox} \quad (3\text{-}17)$$

C_{SF_GB} is the equivalent gate-to-ground capacitance contributed by the gate-to-source capacitance of the SF, which changes along with the SF's gain due to the Miller effect.

$$C_{SF\_GB} = C_{SF\_GS} \cdot (1 - G_{SF}) = 2/3 \cdot W_{SF} \cdot L_{SF} \cdot C_{ox} \cdot (1 - G_{SF}) \quad (3\text{-}18)$$

In $C_{FD,}$ the junction capacitances mainly result from the FD's depletion region, consisting of the bottom plate capacitance C_{FD_J} and the side wall capacitance C_{FD_SW}. C_{FD_J} and C_{FD_JSW} are directly proportional to the diffusion area A_{FD} and the perimeter of the FD region $P_{FD.}$ Both capacitances are related to the voltage value V_{FD}. Thus, the capacitances also vary with V_{PIX}.

$$C_{FD\_J} = \frac{C_{J0}}{(1+V_{FD}/\varphi_B)^{M_J}} A_{FD}; C_{FD\_JSW} = \frac{C_{JSW0}}{(1+V_{FD}/\varphi_{BSW})^{M_{JSW}}} P_{FD} \quad (3\text{-}19)$$

Finally, C_M represents the parasitic capacitance of the metal wires. It can be regarded as a constant value, which is independent of the variation of V_{PIX}. Table 3-1 gives a detailed summary of C_{FD}.

Based on the summary given in Table 3-1, the total capacitance on the FD node is shown in Eq. (3-20). Undoubtedly, C_{FD} has linear parts while some other parts have a complex dependency on the pixel output voltage, constituting the overall value of C_{FD} nonlinear.

$$C_{FD} = C_{RST\_OV} + C_{TX\_OV} + C_{SF\_OV} + C_{SF\_GB} + C_{FD\_J} + C_{FD\_JSW} + C_M \quad (3\text{-}20)$$

Table 3-1. A summary of the components of C_{FD}.

Components of C_{FD}	Equation
Metal capacitance	C_M
Gate capacitance	$C_{TX\_OV} = Xd_{TX} \cdot W_{TX} \cdot C_{ox}$
	$C_{RST\_OV} = Xd_{RST} \cdot W_{RST} \cdot C_{ox}$
	$C_{SF\_OV} = W_{SF} \cdot Xd_{SF} \cdot C_{ox} \cdot (2 - G_{SF})$
	$C_{SF\_GB} = 2/3 \cdot W_{SF} \cdot L_{SF} \cdot C_{ox} \cdot (1 - G_{SF})$
p-n junction capacitance	$C_{FD\_J} = \frac{C_{J0}}{(1+V_{FD}/\varphi_B)^{M_J}} A_{FD}$
	$C_{FD\_JSW} = \frac{C_{JSW0}}{(1+V_{FD}/\varphi_{BSW})^{M_{JSW}}} P_{FD}$

In the pixel, the accumulated charges of the pixel Q (the maximum value is the full-well capacity of the pixel) within a certain exposure time t, is proportional to the photodiode's area A_{PPD} and quantum efficiency QE, shown in Eq. (3-21). I_{PD} is the photodiode current.

$$Q = P \cdot QE \cdot q \cdot t \cdot A_{PPD} = I_{PD} \cdot t \tag{3-21}$$

G_{SF} and C_{FD} depend on the value of the pixel's output voltage V_{PIX}; it is difficult to analyze the linearity performance of the pixel's whole output range with the large signal analysis. With a small signal model, we can derive the relationship between Q and the pixel's output voltage, which is expressed in Eq. (3-22).

$$\delta Q = -\frac{C_{FD}(V_{PIX})}{G_{SF}(V_{PIX})} \delta V_{PIX} \tag{3-22}$$

By integrating V_{PIX} from V_{PIX_MAX} to V_{PIX_MIN} shown in Eq. (3-23), the curve between the number of the integrated charge and pixel's output voltage can be obtained; the nonlinearity of the pixel can also be characterized. In Eq. (3-23), V_{PIX_MIM} is the minimal value of the pixel's output voltage while V_{PIX_MAX} is the maximum value.

$$Q = -\int_{V_{PIX\_MAX}}^{V_{PIX\_MIN}} \frac{C_{FD}(V_{PIX})}{G_{SF}(V_{PIX})} dV_{PIX} \tag{3-23}$$

After further conversion by the following readout circuitry, the nonlinearity of the image sensor can be characterized.

3.3 Test Chip

A chip with a 0.18μm 1-poly and 4-metal CMOS process technology [3.14] is used to verify the algorithm proposed above. The readout channel and the timing diagram of the chip are shown in Figure 3-5.

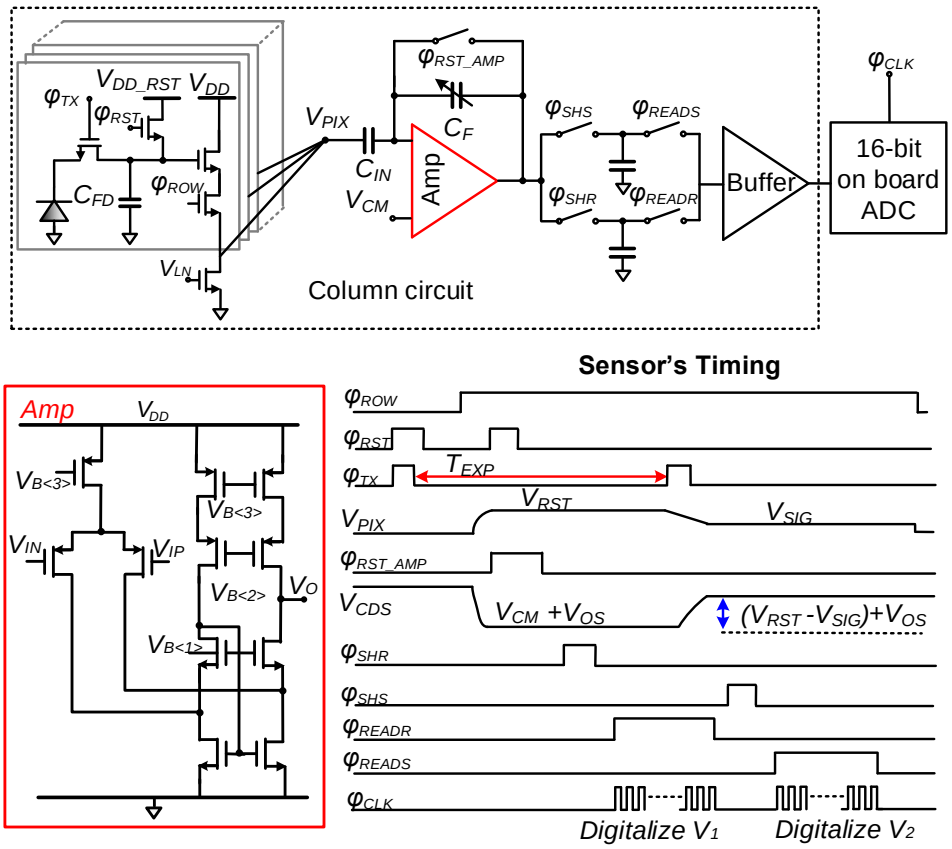

Figure 3-5. The readout channel of the test image sensor (Designed by Yang. X in [3.14]).

The image sensor has a pixel array of 80 (rows) × 160 (columns), which adopts the traditional 4T pixel structure. The pixel array is divided into dozens of groups with different pixel parameters. The variable design parameters include transfer gate width (W_{TX}) and length (L_{TX}), floating diffusion node width (W_{FD}) and length (L_{FD}), and SF's width (W_{SF}) and length (L_{SF}). The gain of the column amplifier is decided by the ratio of the input capacitor C_{IN} and the feedback capacitor C_F. In this design, the gain is fixed to unity gain. A folded operational amplifier (OPA), known for its large voltage swing and shown in Figure 3-5, is used as the column amplifier. φ_{RST_AMP} controls the reset switch of the column amplifier. The reference voltage V_{CM} and the offset of the column amplifier V_{OS} are sampled on

the capacitor C_{SHR} by the control signal φ_{SHR}. The differential voltage between the reset value V_{RST} and the pixel value V_{SIG} is then sampled together with V_{CM} + V_{OS} on the capacitor C_{SHS} by the signal φ_{SHS}. The analog signals stored on these two capacitors, V_1 and V_2, will be read out by φ_{READR} and φ_{READS} column by column. The analog output is then buffered and digitalized by a high-resolution on-board ADC. The ADC performs the second CDS operation, significantly reducing the FPN. The clock of the ADC φ_{CLK} is 50MHz. The ADC's excellent static performance guarantees that it does not restrict the linearity performance of the image sensor.

The size of the chip is 4.62 mm × 3.15 mm. The micrograph of the chip is shown in Figure 3-6. The row and column addressing circuits adopt shift registers [3.14] to scan the pixel array. An onboard FPGA is employed to provide digital control signals and to capture the data digitalized by the ADC.

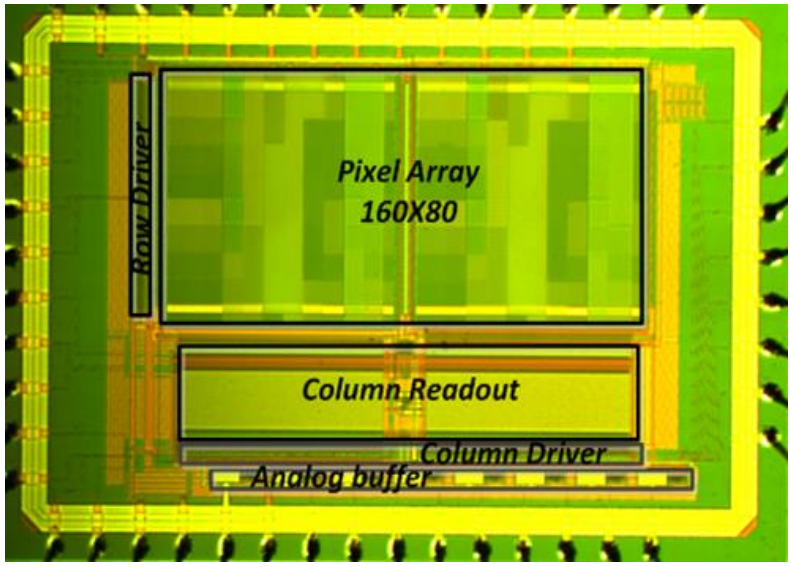

Figure 3-6. The micrograph of the test image sensor.

In this test chip, there are more than 60 types of pixel designs with the purpose to extract the process parameters and to evaluate the pixels' performance [3.14]. Two groups of the pixels are chosen to compare the nonlinearity of the image sensor, based on various pixel parameters shown in Table 3-2. Group A and B have different PPD sizes while each pixel in the same group uses the same PPD size.

Table 3-2. The design parameters of the pixels.

Group	Pixel	TX (W_{TX} / L_{TX}) (μm / μm)	FD (W_{FD} / L_{FD}) (μm / μm)	SF (W_{SF} / L_{SF}) (μm / μm)
GroupA	Pixel1	6.0/0.6	5.7/1.3	0.6/1.0
	Pixel2	6.0/0.6	5.7/1.3	0.7/1.0
	Pixel3	6.0/0.6	5.7/1.3	0.8/1.0
	Pixel4	6.0/0.6	5.7/1.3	0.9/1.0
GroupB	Pixel1	2.0/0.6	1.7/1.3	0.9/0.5
	Pixel2	4.0/0.6	3.7/1.3	0.9/0.5
	Pixel3	8.0/0.6	7.7/1.3	0.9/0.5
	Pixel4	10/0.6	9.7/1.3	0.9/0.5
	Pixel5	12/0.6	11.7/1.3	0.9/0.5

3.4 Measured Results

Based on the algorithm, the modeling results of the C-V characteristic of the C_{FD} for the pixels of Group B are plotted in Figure 3-7. The width of the FD increases from 1.7 μm to 11.7 μm. The wider the FD, the larger the capacitance of the FD. Furthermore, the FD capacitances decrease with the output voltage of the pixel V_{PIX}. These variations are consistent with Eq. (3-20).

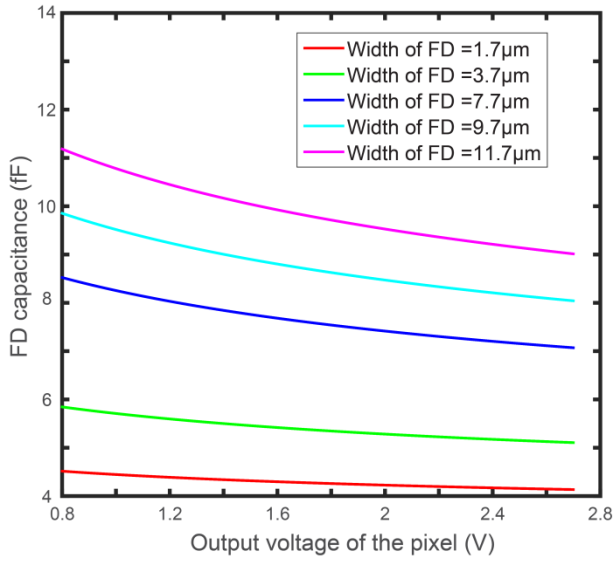

Figure 3-7. *C-V* characteristic of C_{FD}.

The averaged values of the FD capacitance over the whole range of V_{PIX} are chosen as the modeled value of the C_{FD}. The pixels of Group A and B are chosen to compare the test results with the modeling results. Figure 3-8 demonstrates that the photoelectric conversion characteristic of the measurement results align with the modeling results in the image sensor.

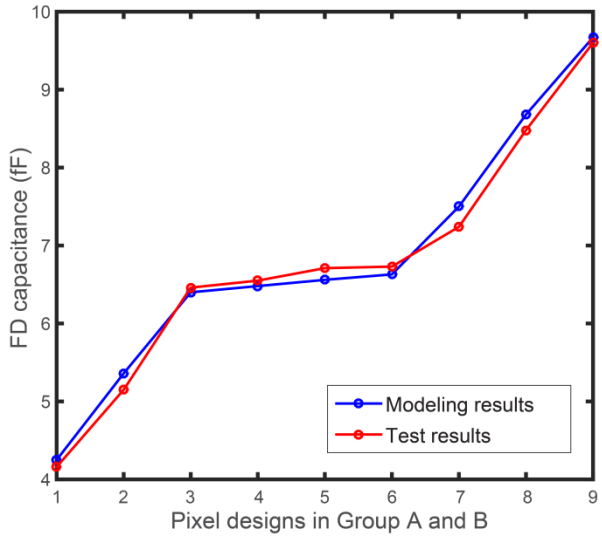

Figure 3-8. Test vs. modeling results of C_{FD}.

According to the analysis mentioned above in section 3.2, the conclusion can be made that the threshold voltage and the gain of the source follower nonlinearly vary with the output voltage of the source follower. A column of pixels without photodiodes are used to test the linearity performance of the source follower independently.

In the measurements of the nonlinearity of the source follower, a voltage is applied on the gate of the source follower. Figure 3-9 shows that V_{GS} of the source follower increases with the output voltage, due to the body effect. In Figure 3-9, the solid lines stand for the simulation results while the asterisk markers represent the test results. The chip is tested with different bias currents of the pixel, ranging from 1 µA to 5 µA.

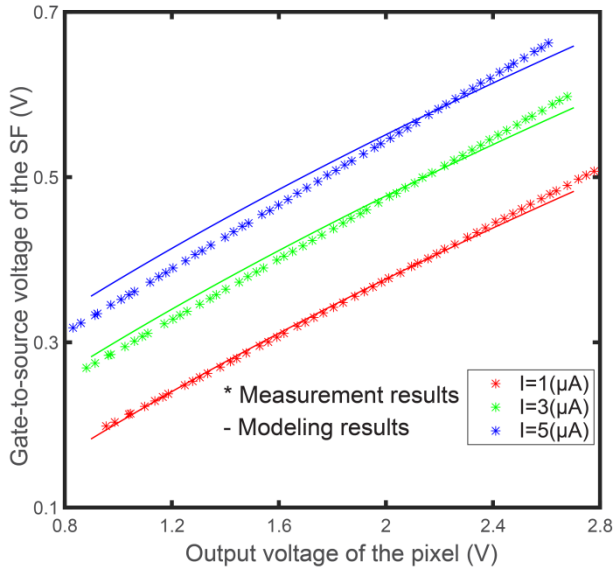

Figure 3-9. V_{GS} of the SF vs. V_{PIX}.

Figure 3-10 plots the relationship between the gain of the SF G_{SF} and the output voltage of the pixel V_{PIX}. A larger bias current leads to a smaller G_{SF}. These conclusions validate Eq. (3-5).

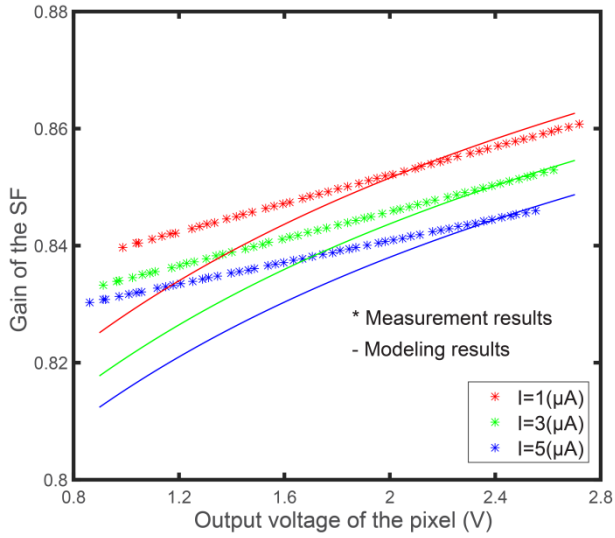

Figure 3-10. Gain of the SF vs. V_{PIX}.

In the nonlinearity measurement of pixels, the exposure time of the image sensor is increasing while a light source provides a constant illumination. The nonlinearity is usually expressed in percentage, as introduced in the EMAV1288

measurement standard [3.13], basing on the deviation between the obtained data points and the calculated best-fit line. Figure 3-11 shows the nonlinearity for the different pixels in Group A, where the width of the SF increases from 0.6 µm to 0.9 µm, the nonlinearity slightly increases. The blue lines represent the simulation results while the red ones provide the test results.

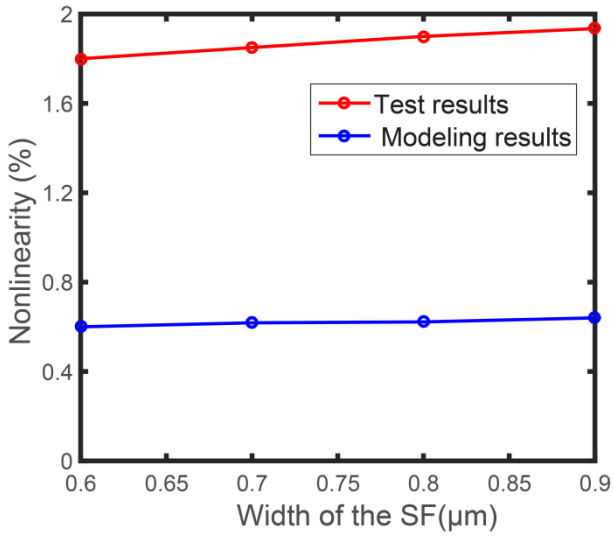

Figure 3-11. The nonlinearity and the noise performances of the pixels in Group A.

Similarly, Figure 3-12 shows the nonlinearity results of Group B. The width of FD changes from 1.7 µm to 11.7 µm while the photodiode design and other parameters keep same; the junction capacitance of the FD increases, resulting in a worsen linearity. In Figure 3-11 and 3-12, the simulation and the test results share the same trend on the nonlinearity for various pixel designs. Theoretically, when the sizes of the SF and the FD increases, the nonlinear capacitance ratio will also increase, thereby bringing down the linearity performance of the whole image sensor. The significant deviations between the simulated and measured results are mainly due to the long exposure time and large dark current of the pixels in the test chip, which affect the linearity results. Chip-level optimization will be carried out in the following design.

Based on these measurement results and the analysis presented in section 3.2, the linearity of the pixel can be improved by choosing suitable design parameters, such as a smaller size of the FD or the SF.

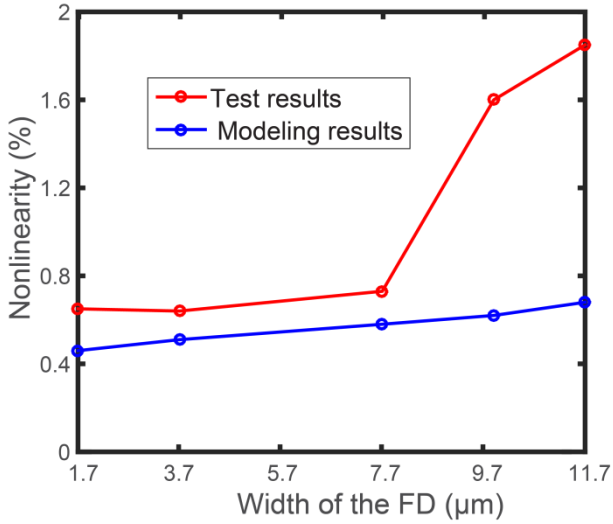

Figure 3-12. The nonlinearity performances of the pixels in Group B.

In addition, a smaller size of the SF can lead to a larger noise while a smaller FD also limits the full-well capacity. Hui Tian showed the evidence that the nonlinearity of an image sensor improves SNR at a high illumination in [3.15]. Besides, Jun Lin analyzed the relationship between the nonlinearity and modulation transfer function (MTF) in [3.5]. Tradeoffs exist among the performances of noise, nonlinearity, and modulation transfer function for image sensors. The procedures mentioned above can serve as a guideline for future pixel designs.

3.5 Conclusion

In this chapter, the nonlinear components of the image sensors based on the 4T pixel structure are analyzed. A behavioral model of the CIS's linearity is proposed. The modeled value of C_{FD}, G_{SF} and linearity are in line with the measurement results of a test chip including multiple groups of pixel designs. The experimental results conclusively prove the effectiveness of the modeling algorithm and the theoretical analysis.

Based on the conclusion of this chapter, a pixel-level linearity optimization will be proposed in Chapter 4.

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Chapter 4 Highly Linear Pixel Designs Embedded in a CIS with Dual CDS

Based on the nonlinearity analysis of a CMOS image sensor presented in Chapter 3, it is clear that the body effect of the source follower transistor and the voltage dependency of the integration capacitor contribute the most to the nonlinearity of the 4T pixel. A type of pixel design using an in-pixel analog buffer is proposed to reduce the nonlinearity by the SF. An additional MIM capacitor adding to the FD node of a 4T pixel also can improve the linearity by reducing the nonlinear ratio of the integration capacitor. Measurement results of a prototype image sensor designed with 0.18-μm CIS technology show that the proposed pixels demonstrate an efficient linearity improvement compared with the traditional 4T pixel. The image sensor also adopts dual CDS to reduce the column FPN.

Section 4.2 introduces the architecture of the prototype CMOS image sensor. Section 4.3 and Section 4.4 discuss the pixel optimization and detailed circuit design of the readout circuit. The setup of the testing and experimental results of the test chip are presented in Section 4.5 and 4.6. Finally, Section 4.7 gives the conclusions.

4.1 Introduction

Linearity is an important parameter for the CMOS imaging systems; many studies have been conducted on linearizing the response of the image sensor. On a software-level, many optimization algorithms such as analytical means and look-up tables (LUTs) [4.1], [4.2], are commonly used to calibrate the digital output and recover the linear response by acquiring and refitting the transfer curve of the image sensor [4.2]. However, the off-chip processing consumes a lot of operation time, power and the linearity improvement is not remarkable. The improvement usually depends on the order of the polynomial and the accuracy of the approximation that the polynomial function can achieve. A commercial camera attains 0.5 % nonlinearity after calibration as reported in [4.2]. A smaller nonlinearity less than 0.1 % is targeted for the application introduced in Chapter 1. Furthermore, with an increase of the resolution and complexity of the sensor, the demands of on-chip image processing capabilities, such as computing and compression capability, trigger the requirement of on-chip linearity improvement capability.

To reduce the off-chip processing time, power consumption as well as improving the system efficiency, chip-level linearity improvement is emphasized. In a CMOS image sensor, the linearity is determined by its pixel design and readout circuitry [4.3]. The previous chapter has already proved that most of the 4T pixel's nonlinearity is a result of the SF's nonlinear gain and the integration capacitor's voltage dependence. In this chapter, two types of pixel designs are proposed to mitigate these two nonlinear error sources, respectively.

4.2 Imager Architecture

Figure 4-1 shows the overall block diagram of the prototype image sensor, based on the column-parallel structure. The sensor uses a rolling shutter readout mechanism comprising of a pixel array (128 × 128), column readout circuits, row decoder/driver, column decoder, low dropout (LDO) regulator, bias/reference generator and digital logic controls. The on-chip LDO regulator provides a stable power supply for the readout circuit. The pixel array consists of 128 × 128 pixels with a pixel pitch of 10μm. Column amplifiers provide a programmable gain from 1× to 8× to suppress the read noise. After sampling by the sample-hold circuits, the analog signal of each column is digitalized by the 10-bit Single-Slope Analog-to-Digital Converter (SS-ADC). An on-chip ramp generator generates a ramp signal for the ADCs. The digitalized output is transferred into in the static random-access memory (SRAM). The contents of the SRAM are read out through sense amplifiers and sent to the FPGA.

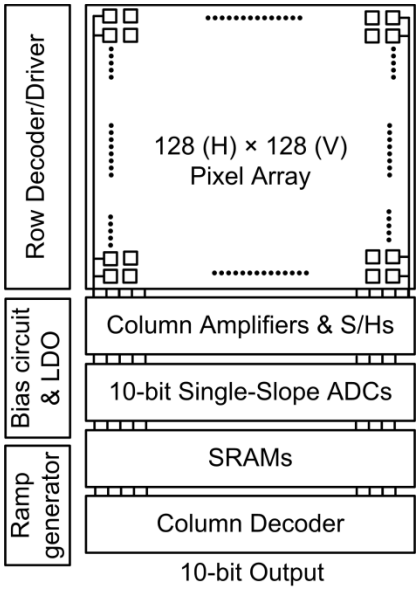


Figure 4-1. The proposed CIS system diagram.

4.3 Pixel Design

Based on the nonlinearity analysis of the 4T pixel in Chapter 3, a type of pixel that mitigates the nonlinear error caused by the SF is first proposed. The schematic of the new pixel V1 is depicted in Figure 4-2, where a single-stage operational amplifier in unity gain configuration is used as an analog buffer to drive the loading circuits instead of the SF. The new structure realizes a constant unity gain which is not related to the output voltage of the pixel.

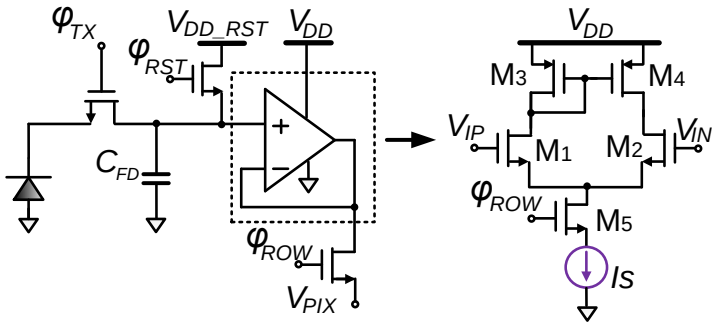


Figure 4-2. The schematic of Pixel V1.

The single-stage OPA structure is selected based on the wide common mode range and low noise performance within a limited pixel size. In the closed-loop configuration, the analog buffer can realize near unity-gain, shown in Eq. (4-1),

where A_{OPA} is the open-loop gain of the OPA; g_{m1} is the transconductance of the input transistor; R is the equivalent output resistance of the OPA and equal to the parallel value of the output resistance of transistor M1 and M3; W_1 and L_1 are the width and length of the input transistor M1; r_{o1} and r_{o3} are the output resistance of transistor M1 and M3; λ_n and λ_p are the channel-length modulation parameters of a nMOS and a pMOS transistor; μ is the carrier mobility and C_{ox} is unit oxide capacitance; I_S is the tail bias current of the OPA.

$$G_{OPA} = \frac{A_{OPA}}{1+A_{OPA}} = \frac{g_{m1}R}{1+g_{m1}R} = (1+\frac{1}{g_{m1}R})^{-1} = (1+\frac{1}{g_{m1}(r_{o1} \,\mathrm{P}\, r_{o3})})^{-1} = (1+\frac{2(\lambda_n+\lambda_p)\sqrt{I_s}}{\sqrt{\mu \cdot C_{ox} \cdot (W_1/L_1)}})^{-1} \quad (4\text{-}1)$$

The negative feedback can reduce the distortion of the amplifier which is related to the input signal. A larger open loop gain of the amplifier can thus better suppress the nonlinearity of the voltage buffer. However, the open loop gain of an amplifier depends on the circuit structure. A telescopic or two-stage amplifier structure can achieve a larger gain at the cost of noise and chip area. It is difficult to adopt a complex amplifier structure within the limited pixel size. In this design, the open loop gain of the adopted single-stage amplifier can reach 44 dB. According to the SPICE simulation, when the input voltage range is 1.7 V~2.7 V, the nonlinearity of the voltage buffer in pixel V1 is 0.12 % while the nonlinearity of the SF is 2.2 % in a reference 4T pixel V2, which is included for a comparison of the linearity performance.

The previous chapter has already introduced the concept that the integration capacitor C_{FD} is nonlinear, consisting of several types of capacitances. In pixel V3, a MIM capacitor with a size of 1.6 μm × 1.7 μm is added to the FD node to reduce the nonlinear ratio of the integration capacitor, shown in Figure 4-3. The MIM capacitance ratio over the total capacitance value on the FD node is around 57%, which increases the linear ratio of the integration capacitance.

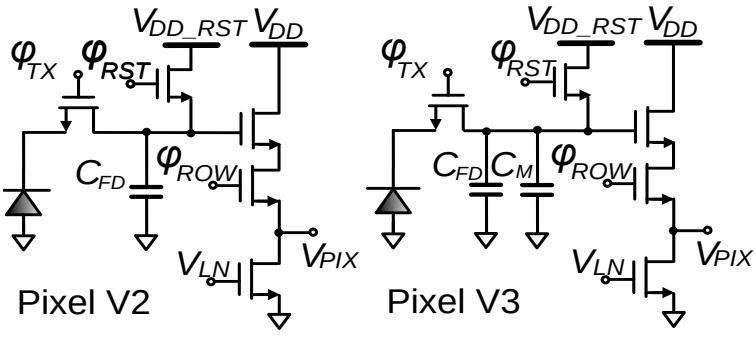
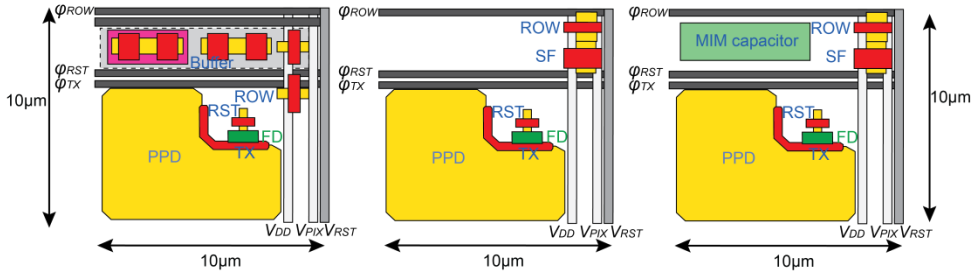


Figure 4-3. The schematic of pixels V2 and V3.

The conceptual layout of the pixels is shown in Figure 4-4. The pixels have a common size of 10 μm × 10 μm. To fairly compare the performance, all pixels use the same photodiode design, while the pixel V2 does not fully use the pixel area. The photodiodes adopt a geometrical L-shaped design [4.4] on the overlapping region with the transfer gate to achieve a large fill factor and to improve charge transfer efficiency. All the pixels achieve a fill factor of 47 %. To improve the linearity, the row select and reset transistors in the pixels adopt low threshold voltage transistors (around 0.1 V) to reduce the value of the switch resistors and have a sufficient settling time. In pixel V2 and V3, the SF also uses the same low threshold voltage transistor to reduce the temporal noise [4.5]. A guard ring is added to isolate the pixel array from substrate noise. The layout of pixels is also optimized to reduce the dark current.



(a) (b) (c)

Figure 4-4. The conceptual layout of pixel (a) V1; (b) V2; (c) V3.

In Figure 4-4, the input and load transistors of the buffer in pixel V1 use a longer length to realize enough gain, while the SF in the pixel V2 and V3 adopts an optimized size to achieve optimized noise performance. The other transistors such as the row select and reset transistors use a minimum length permitted by the process to reduce charge injection.

In the 4T pixel, the pinned photodiode and the following correlated double sampling circuit eliminate the kTC noise. Thus the noise of the source follower dominates the pixel noise. The input equivalent noise of the SF [4.6] is given by Eq. (4-2).

$$\overline{V_{n,in,SF}^2} = 4kT\frac{2}{3}\frac{1}{g_{m,SF}} + \frac{K_N}{W_{SF}L_{SF}C_{ox}f} \tag{4-2}$$

In Eq. (4-2), K_N is the flicker noise constant of the nMOS transistor which is process dependent; f is the frequency; k is the Boltzmann's constant; T is the absolute temperature. The following CDS circuit also eliminates most of the 1/f noise of the SF [4.7]. Therefore, the thermal noise of the source follower has a

significant contribution to the read noise of the CMOS image sensor [4.8]-[4.9].

The input noise of the 5T-OPA in the pixel V1 follows Eq. (4-3), where g_{m3}, K_P is the transconductance and flicker noise coefficient of the pMOS transistors M3, respectively; W_3 and L_3 are the width and length of the PMOS transistor M3 [4.10].

$$\overline{V_{n,in,opa}^2} = 8kT\frac{2}{3}\left(\frac{g_{m3}}{g_{m1}^2}+\frac{1}{g_{m1}}\right)+\frac{2}{C_{ox}f}\left(\frac{K_P g_{m3}^2}{W_3 L_3 g_{m1}^2}+\frac{K_N}{W_1 L_1}\right) \quad (4\text{-}3)$$

From Eq. (4-3), it can be derived that pixel V1 introduces more noise compared with 4T pixel.

4.4 Readout Circuit Design

The readout circuit of this prototype image sensor adopts the column-parallel structure, where the pixels are read out and processed simultaneously in all columns. Compared with the serial structure of the CIS, it achieves a better trade-off between chip size, power consumption, and speed [4.9]. The critical blocks of the readout circuits will be introduced in the following section.

4.4.1 Low Dropout Regulator Design

Usually, the readout circuit is sensitive to the noise of the power supply. Large ripples and ground noise can affect the imaging performance [4.10]. In this design, a low dropout regulator with low quiescent power consumption is employed to provide a stable and low noise DC power to the readout array.

Figure 4-5 shows the schematic of the proposed LDO regulator, consisting of the bias circuit, an error amplifier (EA), a buffer, power stage and current limiting circuit.

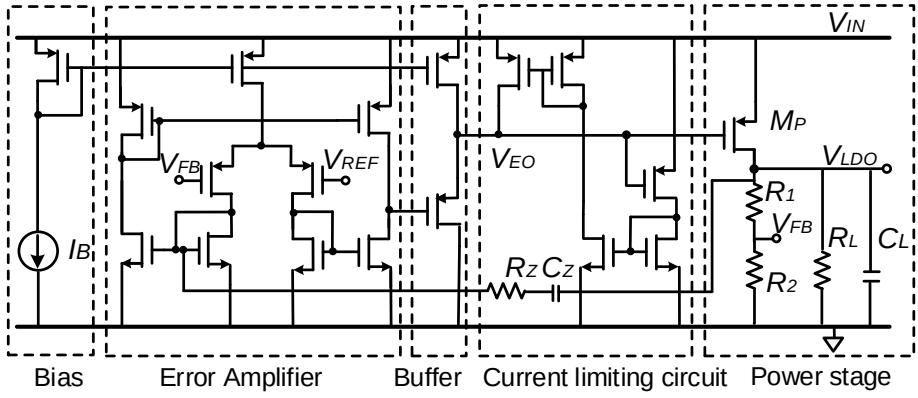


Figure 4-5. The schematic of the LDO regulator.

In Figure 4-5, V_{IN} is the input voltage of the LDO regulator. Generated by an on-chip bandgap, the reference voltage V_{REF} is adjustable from 0.8V~1.3V by programming the switches in the bandgap. An operational transconductance amplifier is employed as the error amplifier to ensure that the LDO regulator operates within a wide load region. The amplifier compares V_{REF} with a feedback voltage V_{FB}. The source follower, functioning as a voltage buffer, is employed to drive the power transistor M_P. The current limiting circuit is used to prevent the overflow of the loading current. Miller resistor R_Z and capacitor C_Z are employed for phase compensation. The feedback network consisting of resistors R_1 and R_2, together with the amplifier, maintains a constant output voltage [4.10], shown in Eq. (4-4).

$$V_{LDO} = (1 + \frac{R_1}{R_2})V_{REF} \tag{4-4}$$

4.4.2 Column Amplifier Design

In a CMOS image sensor, an amplifier is usually adopted either on a column level or global level to realize analog CDS and suppress the read noise. In this design, dual CDS is adopted to reduce the column fixed pattern noise. A switched capacitor amplifier works as the first CDS circuit; then an ADC provides the second CDS operation in the digital domain.

Figure 4-6 shows the schematic of the switch-capacitor CDS column amplifier. The column amplifier provides a programmable gain 1× to 8× by varying the ratio of the input and feedback capacitors of the column amplifier. The input capacitor C_{IN} is fixed at 1 pF while the feedback capacitor C_F can be switched from 0.125 pF to 1 pF. As shown in Figure 4-6, a telescopic cascode OPA with a differential input and single-ended output structure is adopted in the column amplifier design. The differential structure has a high common-mode rejection ratio (CMRR), at the cost of doubling noise and power consumption [4.11]. The telescopic cascode OPA attains a high open-loop gain of 86 dB with wide linear range. The high gain of the OPA guarantees the high linearity of the column amplifier [4.11]. The bias voltages $V_{B<0>}$ to $V_{B<2>}$ generated by the bias circuit, are shared by all columns. The column amplifier with a high closed-loop gain significantly suppressed the temporal noise from the following circuit, especially from the ADC.

The column amplifier also realizes the first analog CDS operation. In the first sampling phase, the signal φ_{AMP_RST} is maintained at a high level. The pixel's reset voltage V_{RST} is sampled on the C_{IN}. In the amplification phase, the signal voltage of the pixel V_{SIG} is sensed on the C_{IN}. The charge variation from the input is

conveyed to the C_F. The output voltage of the column amplifier V_{CDS} can be expressed in Eq. (4-5), where V_{CM} is the common voltage of the amplifier.

$$V_{CDS} = V_{CM} + C_{IN} / C_F (V_{RST} - V_{SIG}) \tag{4-5}$$

The analog CDS operation removes the in-pixel fixed pattern noise, mainly caused by the variation of the threshold voltage of the in-pixel readout circuits. Together with the pinned photodiode, the column amplifier reduces the kTC noise generated by the reset transistor of the pixel. The output voltage of the amplifier V_{CDS} is further sampled by a sample and hold circuit and sent to the following ADC. The sample capacitance C_{SH} is 1pF.

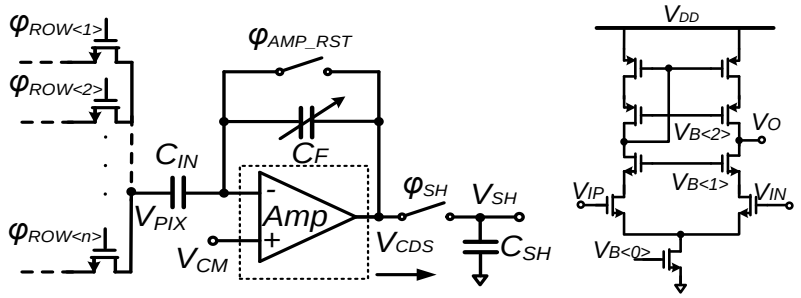


Figure 4-6. (a) The column-parallel amplifier and S/H circuit; (b) OPA used in the amplifier.

The CDS circuit shown in Figure 4-6 induces another FPN caused by the offset voltage V_{OS}, due to the mismatch of the OPA. The output voltage which includes the offset of the amplifier can be expressed in Eq. (4-6).

$$V_{CDS} = V_{CM} + C_{IN} / C_F (V_{RST} - V_{SIG}) + V_{OS} \tag{4-6}$$

To avoid a vertical stripe pattern in the output image, a second digital CDS is carried out in the digital domain by the ADC, which can cancel this type of FPN.

4.4.3 Column-Level Single Slope ADC Design

In CMOS image sensors, column-parallel ADC architectures usually contain SS-ADCs [4.12]-[4.14], Successive Approximation ADCs [4.15]-[4.16], Sigma-Delta ADCs [4.17]-[4.18], or Cyclic ADCs [4.19]-[4.20]. Despite having the disadvantage of low conversion speed, SS-ADC is still a favorite choice due to the benefits of its high resolution, high linearity with a small area and low power [4.12].

The column-parallel SS-ADC in this design consists of an on-chip ramp generator, a comparator, a 10-bit ripple counter and 10-bit data latches. The ramp generator creates a global ramp signal for all the column ADCs. The comparator compares the sampled analog signal with the ramp signal until the comparison

result flips. The counter at each column calculates the trigger time, which is then converted into a digital number.

4.4.3.1 Comparator

The offset of the comparator is detrimental to the linearity performance of the ADC. Two different auto-zeroing techniques: input offset storage (IOS) and output offset storage (OOS) are commonly used to realize a low offset of the comparator [4.21]-[4.22].

In this design, the comparator circuit is shown in Figure 4-7, which is based on the design proposed in [4.23], combining the IOS and OOS techniques to attenuate the offset. A differential architecture is employed in the comparator design, which effectively reduces the charge injected by the switches and common mode noise. Based on the consideration of a reasonable gain and speed, a configuration of three stages of preamplifiers with a dynamic latch is adopted.

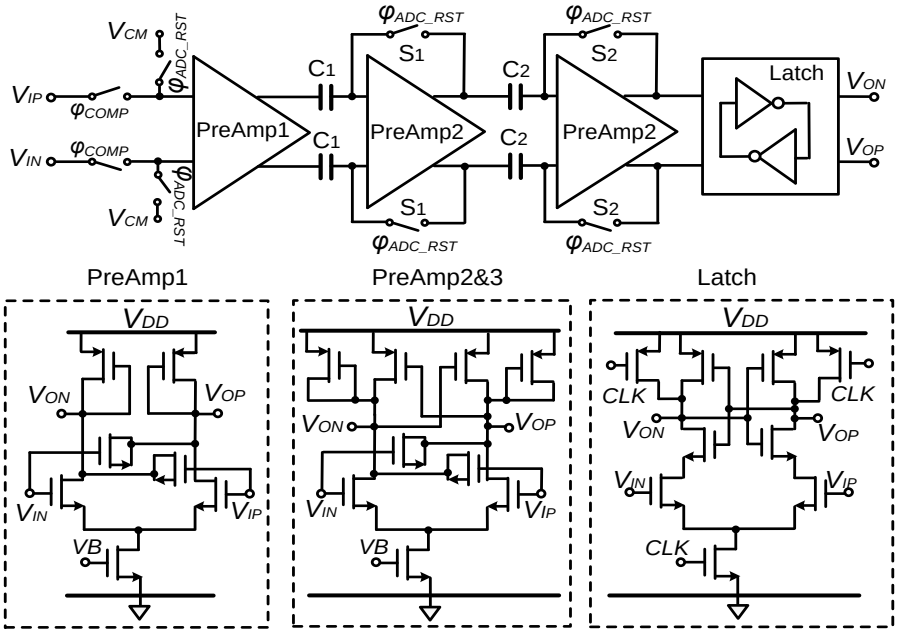


Figure 4-7. The schematic of the comparator (Based on the design introduced in [4.23]).

In the comparator, the first stage preamplifier is designed with a relatively small gain to avoid saturation of the capacitor pair [4.23]. The second and third stage preamplifier that use positive feedback, have a larger gain to suppress the offset. Furthermore, extra transistors are adopted in the preamplifiers to reduce the kickback noise. The control logic necessary to drive the comparator, will be introduced in the following section.

With the combined offset canceling technique, the comparator can achieve an offset less than a half Least Significant Bit (LSB). The offset of the comparator V_{OS} [4.23] follows Eq. (4-7),

$$V_{OS} = \frac{V_{OS\_2}}{A_1(1+A_2)} + \frac{\Delta Q_1}{A_1 C_1} + \frac{V_{OS\_3}}{A_1 A_2 (1+A_3)} + \frac{\Delta Q_2}{A_1 A_2 C_1} + \frac{V_{OS\_LATCH}}{A_1 A_2 A_3} \tag{4-7}$$

where A1, A2 and A3 are the gains of the preamplifiers, respectively; V_{OS_2}, V_{OS_3}, are the offset of the second and third stage preamplifier; V_{OS_LATCH} is the offset of the latch. ΔQ_1 and ΔQ_2 are the charge injected mismatches from the switches S_1 and S_2; C_1 and C_2 are the auto-zeroing capacitors.

4.4.3.2 Ramp Generator

The ramp generator is an important block in the SS-ADC, whose performance decides the accuracy and linearity of the whole ADC circuit [4.24]. A progressively incrementing or decrementing ramp signal is usually generated by a high-resolution Digital-to-Analog converter (DAC) or an integrator circuit [4.24]. The DAC-type based ramp generator usually consumes a large area compared with the integrator type ramp generator.

A bilateral ramp generator used in this CIS is realized by a switched-capacitor integrator. As shown in Figure 4-8, the integrator consists of an operational amplifier OPA_2, a mux and reset switches.

As shown in Figure 4-8, a rail-to-rail input/output OPA structure is adopted in the integrator which realizes a wide linear swing; the class AB output structure is selected while considering the drivability for the large load capacitances of the column ADC array. The mux decides the direction of the mirrored current and the ramp signal, whether it is a progressively incrementing or decrementing ramp signal starting from the DC voltage V_S.

The linearity of the ramp generator depends on the current which is conveyed by a reference current mirror [4.24]. Together with an adjustable onboard resistor R, a folded cascode operational amplifier OPA_1 converts the bandgap reference voltage V_{REF} to a reference current I_{REF}. The value of the reference current is expressed in Eq. (4-8).

$$I_{REF} = V_{REF} / R \tag{4-8}$$

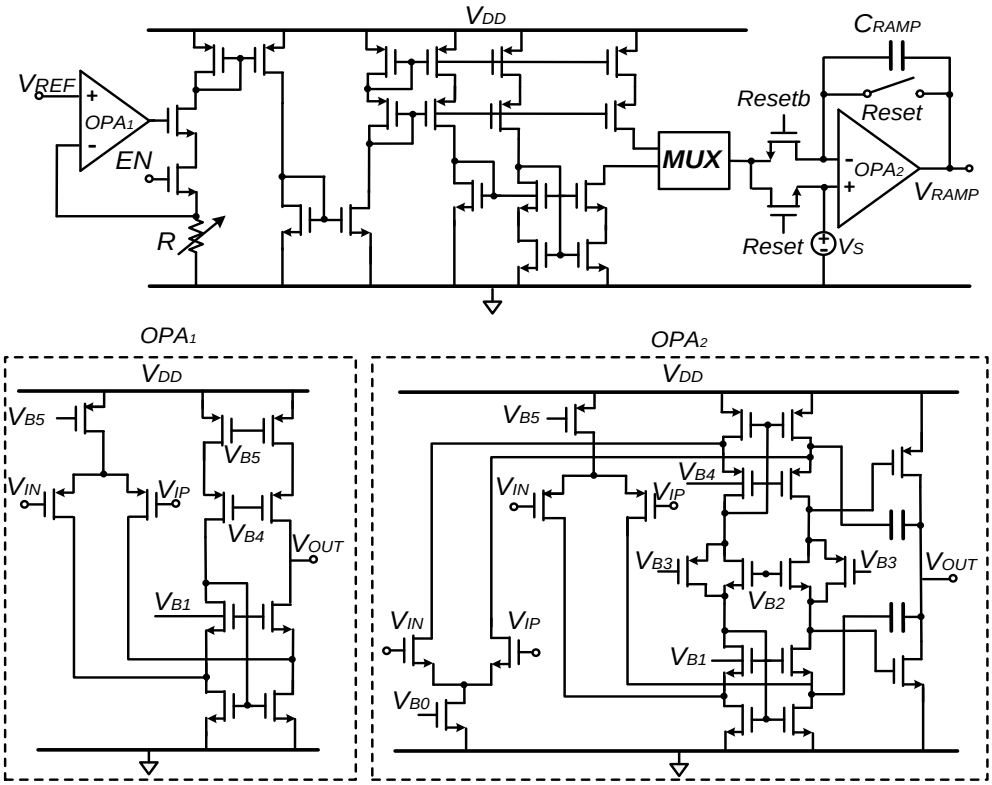


Figure 4-8. The schematic of the ramp generator.

The slope of the ramp signal is decided by the reference current I_{REF}, the integration capacitor of the ramp generator C_{RAMP}, and the period of the reset signal T. The expression of the ramp voltage is shown in Eq. (4-9).

$$V_{RAMP}(t) = \frac{A_{OPA2}}{A_{OPA2}+1}\left(V_S + \frac{1}{C_{RAMP}}\int_0^T I_{REF}(t)dt\right) \tag{4-9}$$

In Eq. (4-9), A_{OPA2} is the gain of the rail-to-rail operational amplifier OPA_2; C_{RAMP} is designed using a MIM capacitor for its excellent linearity performance despite that it has a relatively lower area efficiency [4.24].

4.4.3.3 Up-down Counter

There are two types of counter design usually adopted in the single slope ADC. The synchronous counter is usually shared with all column ADCs to save power consumption [4.25]. In this design, a 10-bit asynchronous up-down counter, which can be operated in a shorter span of time when compared to the synchronous counter, is employed in each column to capture the data from the comparator. The schematic for the counter based on the design reported in [4.26]

is shown in Figure 4-9. Based on the D Flip-Flop blocks, the direction of the counter can be up or down by switching the value of the control signal φ_{UD} through a MUX. The control signal φ_{KEEP} is used to lock the data during the counter direction transition period. φ_{RSTB} is the reset signal of the counter.

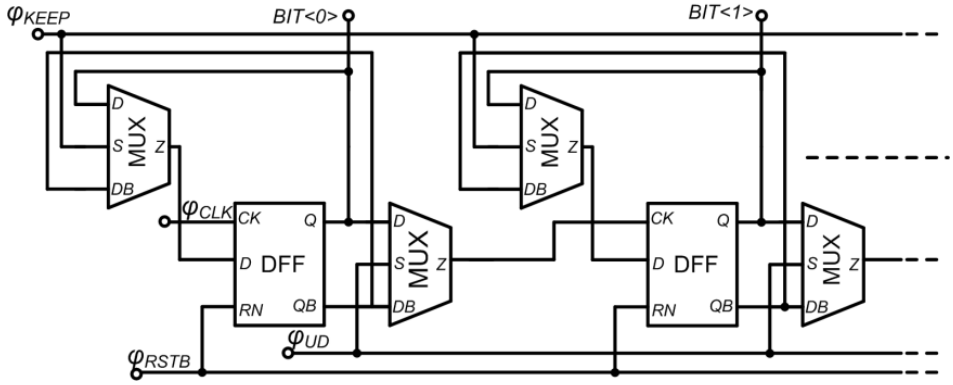


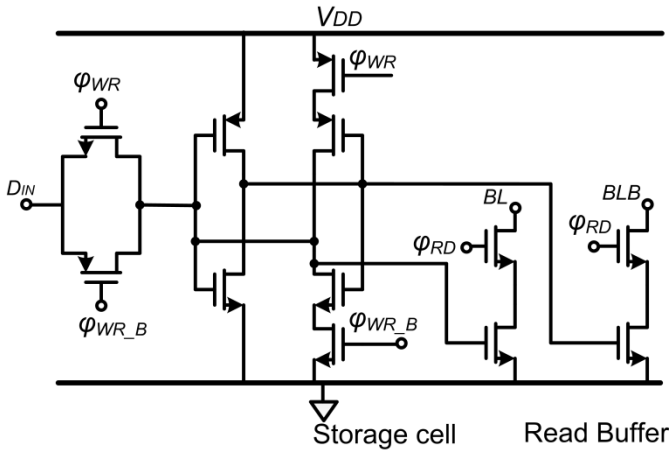
Figure 4-9. Schematic of 10-bit up-down counter [4.26].

Subsequently, a 10-bit latch is used to lock the counter's output. Finally, the latched data are written and stored in the SRAM.

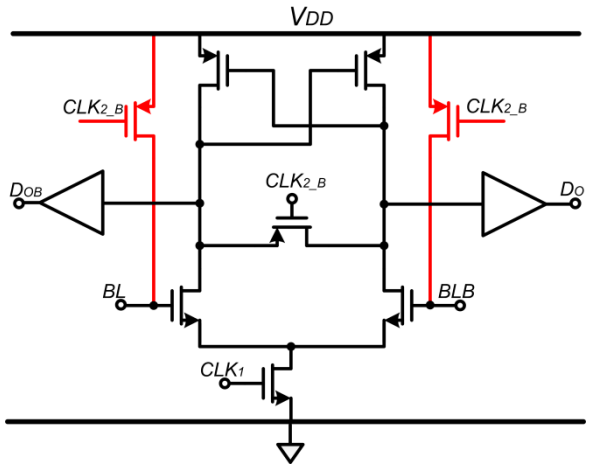
4.4.4 SRAM Design

Compared with the SRAM cell with a single-port, the SRAM cell with multi-ports has the advantage of parallel operation, popular among high-speed communication designs [4.27]. In this design, to improve the static noise margin (SNM), a type of SRAM cell with one-write port and two-read ports based on the design reported in [4.28] is employed, shown in Figure 4-10 (a). *BL* and *BLB* are the bit-line and complement bit-line while D_{IN} is the input digital signal; φ_{WR} and φ_{WR_B} are two opposite signals which control the "write" operation of the SRAM cell and φ_{RD} controls the "read" operation. Compared with the traditional 6T and 8T SRAM cell, the proposed SRAM cell reduces the read-write disturbance and demonstrates to have better performance in static and dynamic noise margin [4.28]-[4.30].

The sense amplifier detects the value of the stored data in the SRAM cell during the read period and further displays the data [4.31]. The sense amplifier used in this design is shown in Figure 4-10 (b).



(a)



(b)

Figure 4-10. Schematic of (a) SRAM cell; (b) sense amplifier [4.28].

The sense amplifier has two control signals: CLK_1 and CLK_{2_B}, which are generated by a non-overlap clock generator circuit shown in Figure 4-11. As shown in Figure 4-10 (b), the transistors in the red lines enable the bit-lines to be pre-charged to the high voltage through the signal CLK_{2_B}. The pre-charge operation is carried out before the read operation, which saves the power consumption and accelerates the speed [4.28].

As shown in Figure 4-11, non-overlap clock generator circuit generates two groups of non-overlap clocks signals. CLK_{2_B} is used to pre-charge the bit-lines, while the other signals are used to recover the stored data together with column decoder circuits.

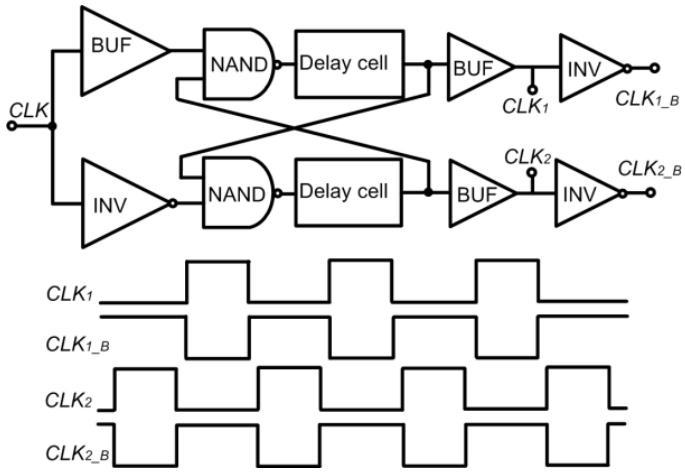


Figure 4-11. Non-overlap clock generator.

4.4.5 Timing Diagram of the CIS

Figure 4-12 shows the timing diagram of the 10-bit CIS with dual CDS. The column amplifier realizes the first analog CDS by subtracting the measured V_{RST} and V_{SIG} of the pixel. The second CDS is carried out by the ADC in the digital domain. The clock signal of the ADC φ_{CLK} operates at 50MHz.

The timing of the CIS is divided into two phases. During the reset phase, the pulse φ_{RST} and φ_{TX} are set high to reset the PPD and FD. Then, the pulse φ_{RST} and φ_{TX} are turned off and the integration phase is started.

The second phase is the readout phase. φ_{RST} is activated again to enable the readout process of the V_{RST} signal, then the column amplifier and the comparator in the ADC realize auto-zeros by setting φ_{CDS_RST} and φ_{ADC_RST} sequentially high. φ_{CDS_RST} is the reset signal of the column amplifier while φ_{ADC_RST} is the reset signal of the comparator. When the φ_{CDS_RST} is high, the output voltage of the column amplifier is set as the common voltage V_{CM} with the offset of the amplifier, sampled by the S/H circuit with the signal φ_{SH}. Afterwards, the pulse φ_{TX} is activated to transfer the charge accumulated in the photodiode to the FD. As shown in Figure 4-12, the period between the two adjacent falling edges of φ_{TX} defines the exposure time T_{EXP}. The signal φ_{SH} is activated again, and the sampled differential signal between the reset value and signal value is sent to the input of the comparator. The analog CDS operation removes the fixed pattern noise, the reset/kTC noise and most of the 1/f noise of the pixel [4.18].

An A/D conversion begins with the signal φ_{COMP}, representing the effective time of the comparator. φ_{RAMP_ENB} is the disable signal of the ramp signal generator. For the 10-bit ADC, a 256 clock cycle is first performed to digitalize

the sampled signal $V_{CM}+V_{OS}$. By varying the value of φ_{UD}, the direction of the counter starts to go up. φ_{KEEP} keeps the data unchanged during the counter direction transition period. A second A/D conversion with a 256 + 1024 clock cycle digitalizes the sampled value $V_{CM}+G\times(V_{RST}-V_{SIG})+V_{OS}$, where G is the closed-loop gain of the column amplifier. In this way, the offset error of the column amplifier is canceled by the digital CDS.

Subsequently, the latches synchronize the digital output with the digital signal φ_{LATCH_ADC}. The data is finally conveyed to SRAM by the signal φ_{WR} and read out by the signal φ_{RD}.

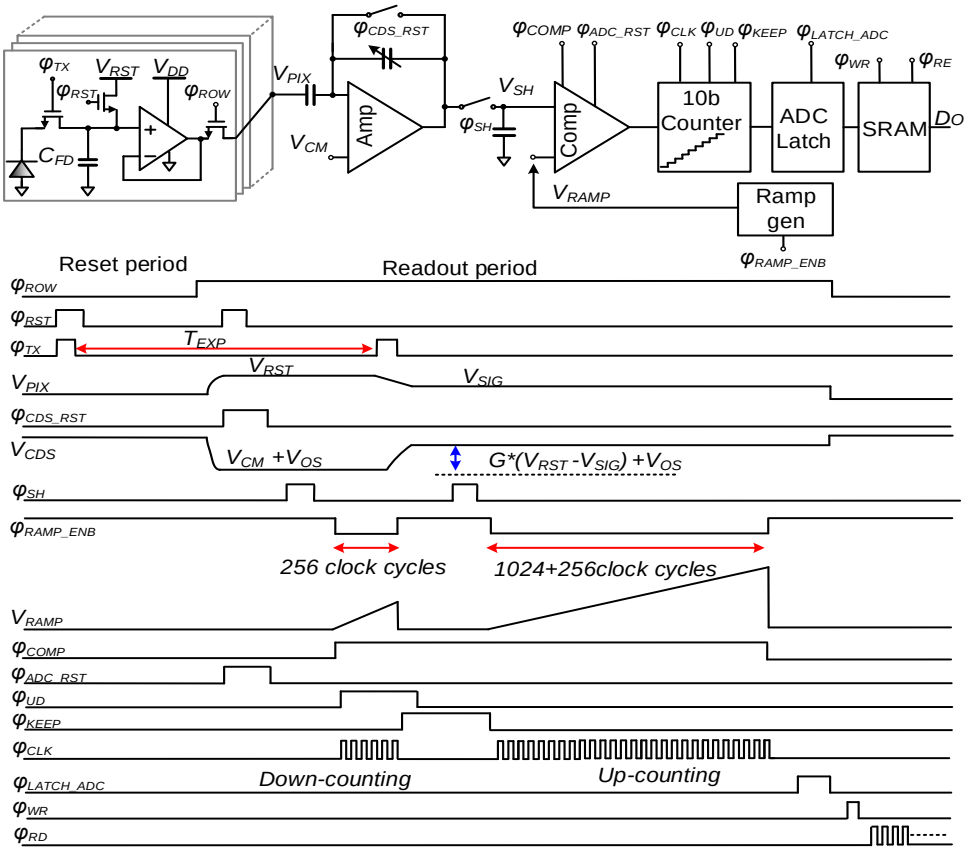


Figure 4-12. Timing diagram of the CIS with dual CDS.

4.5 Camera System

Figure 4-13 shows the die micrograph of the fabricated chip implemented with a 0.18-μm 1-poly and 4-metal CIS process. The chip consists of a 128 × 128 pixel array with a 10 μm pixel pitch. The chip area is 2.6 mm × 5 mm while the core pixel array area is 1.28 mm × 1.28 mm.

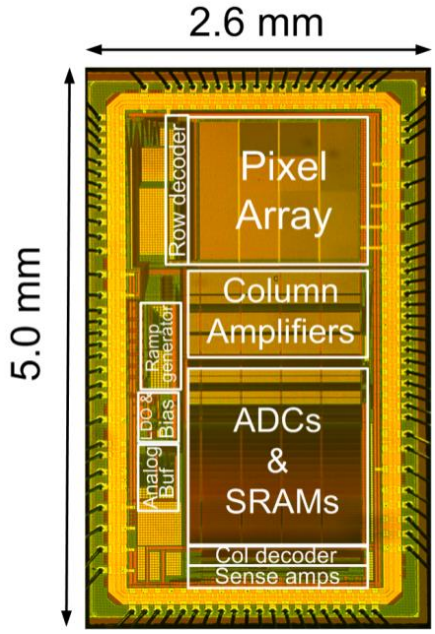


Figure 4-13. Chip microphotograph.

Figure 4-14 shows the test environment of the imaging system. A 4-layer mother-daughter PCB is developed for the digital imaging system. The motherboard hosts an Altera Cyclone II FPGA, generating digital control signals for the CMOS image sensor. The motherboard also generates the power supplies of the chip and itself. The daughter board hosts the image sensor and optical lens. Two boards are connected via stack-up connectors. The image data are transmitted to the FPGA then sent to the computer via a Camera Link interface. LabVIEW is used to capture and analyze the data.

In the test system shown in Figure 4-14, a tungsten-halogen lamp provides a stable illumination. A monochromator provides a desired bandwidth ranging from 350 nm to 950 nm. An integrating sphere provides a uniform monochromatic light beam to the test chip and a reference photodiode [4.32]. This reference photodiode with known sensitivity is employed to calculate the quantum efficiency of the sensor.

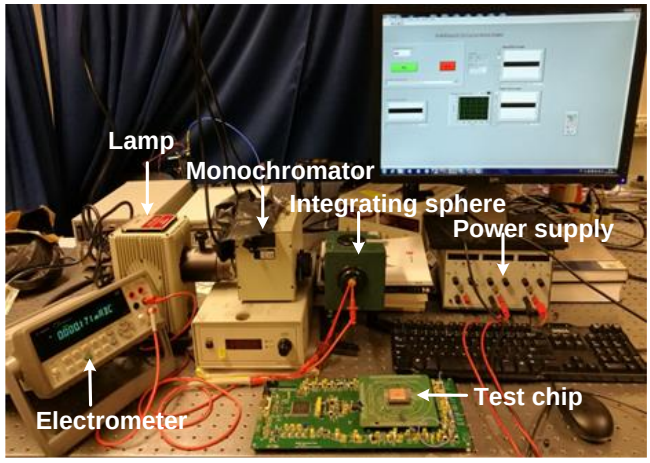


Figure 4-14. Test environment.

4.6 Experimental Results

The measurement results of the test chip will be introduced in the following subsections, which starts with the introduction of the LDO regulator.

4.6.1 LDO Regulator

The LDO regulator proposed in this chip has a core area of 312 × 104 μm^2. The whole area includes the bandgap circuit 500 × 150 μm^2 in dimension, and the chip photo is shown in Figure 4-15.

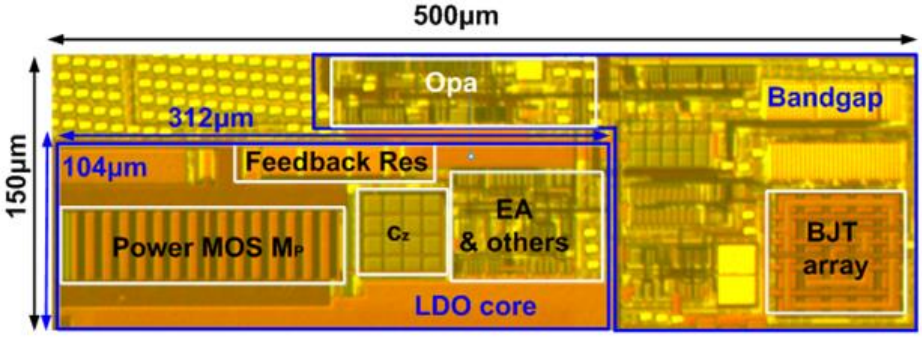


Figure 4-15. Chip photo of the proposed LDO regulator.

With an input voltage V_{IN} range from 3 to 3.8 V, the output voltage of the LDO regulator is between 2.7~2.8 V depending on the current load. The measurement results of the line regulation and load regulation are shown in Figure 4-16. When V_{IN} is 3.3 V, the load current changes from 0.1 to 33 mA, the variation of the output voltage of the LDO regulator V_O is 80 mV. The calculated load regulation

is 2.5 mV/mA. The prototype LDO regulator consumes a quiescent current of 10 μA. The minimum dropout voltage is about 0.37 V and the line regulation is 26 mV/V when the load current is 33 mA. This is mainly due to the voltage drop in the metal wire and bonding wire. A wider metal trace on the chip and a thicker ever multiple bonding wires are considered to employed to reduce the voltage drop in the future design. The readout array consumes a current less than 10 mA, therefore the LDO regulator can be further used in a CMOS image sensor with a larger pixel array.

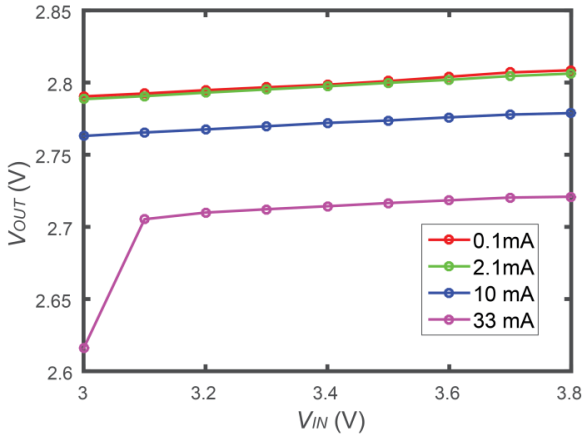


Figure 4-16. Measured line and load regulation.

4.6.2 Ramp Generator

The measured ramp signal generated by the on-chip ramp generator is plotted in Figure 4-17, which shows that the ramp generator can provide a bilateral ramp signal with a large output swing. The yellow signal represents the reset signal of the ramp generator, while the blue one is the generated ramp signal which can reach a range from 0.7 V~2.9 V. The period of the ramp signal is 102.4 μs while the ADC works at a frequency of 12.5 MHz.

Figure 4-17. Measured ramp signal (a) with down direction; (b) with up direction.

By varying the on-chip resistor, the ramp signal realizes a different slope. Figure 4-18 shows the measured ramp signal working in dual CDS mode with a 50 MHz clock. The period of the ramp signal is 40 μs.

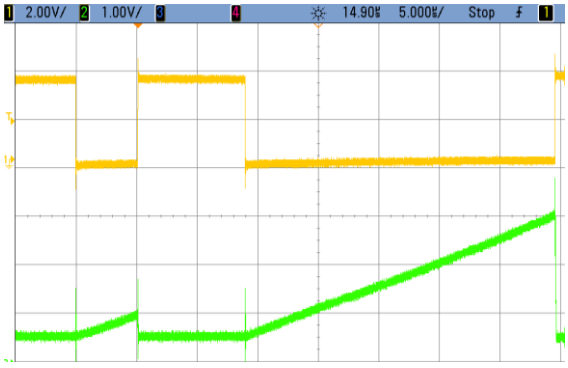


Figure 4-18. Measured ramp signal in dual CDS mode.

4.6.3 Pixels

In this thesis, the linearity performance is the most important index. The new test chip introduced in this chapter adopts optimized pixel and circuit designs. The measured dark current of pixels V1~V3 at room temperature are less than 60 e-/pixel/s at different settings. The values of the pixel's dark current are quite small, which will not affect the pixels' linearity performance within a short exposure time. During the linearity measurement, a tungsten-halogen lamp is used to provide a constant illumination source. The number of photons reaching the image sensor is changed by increasing the exposure time from 1 μs to 1024 μs evenly. According to the EMAV1288 measurement standard [4.33], 5 % to 95 % of the full output range is selected to calculate the nonlinearity of the pixels. Figure 4-19 shows the linearity performances of the proposed pixels. From top to bottom, the vertical axis represent the averaged digital value of the whole pixel array, DNL and INL performance of the image sensor, respectively. Compared with the traditional 4T pixel V2, the pixel with an analog buffer in place of a SF successfully reduces the nonlinear errors caused by the SF. It obtains a nonlinearity of 0.20 % while the 4T pixel has nearly twice as much as 0.38 %; pixel V3 brings down the nonlinear ratio in C_{FD}, and thus achieves a small nonlinearity, merely 0.14 %.

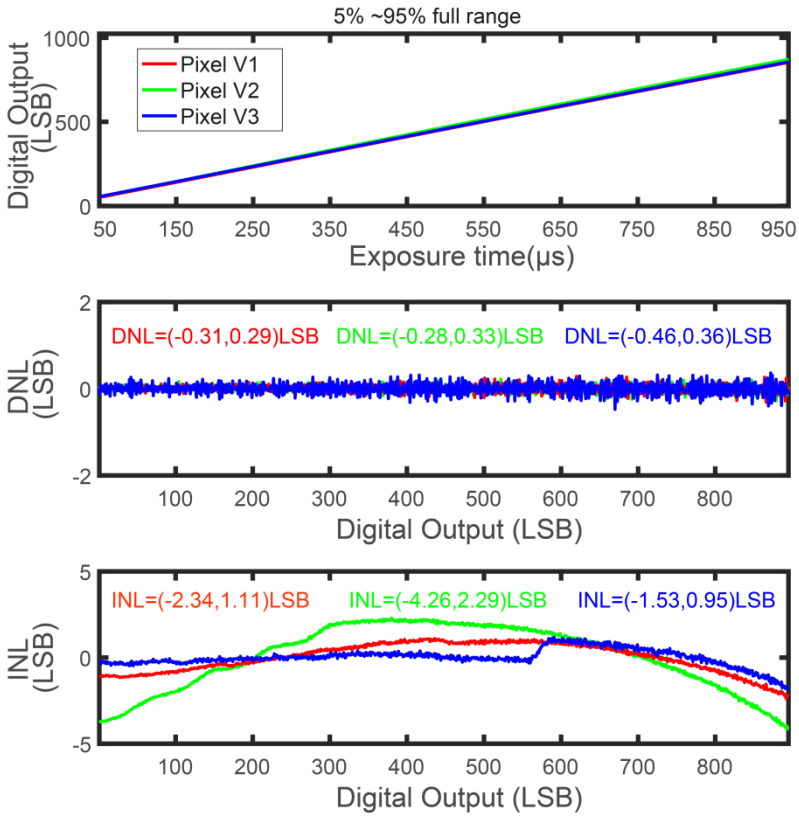


Figure 4-19. Linearity performances of the pixels.

In some application, especially for the scientific image sensors used in space imaging, the sensor's linearity performance at low photon flux level is emphasized. 0.1~10 % of the full well capacity of the pixels are used to evaluate the linearity performance. The corresponding measured nonlinearity of the pixels V1~V3 is 0.12 %, 0.31 % and 0.088 % respectively, which validates the pixel-level linearity improvement even at a low illumination condition.

These results show that pixel V1 not only improves the linearity performance, it also realizes a near unit gain and hence increases the conversion gain of the pixel. Figure 4-20 shows the mean-variance plots of the pixels where the conversion gain and FWC of the pixels can be calculated. The measured conversion gains (= slope of the curves in the mean-variance plots) of the pixels are 56.2 μV/e-, 47.3 μV/e- and 18.7μV/e-, respectively for the pixels V1, V2 and V3.

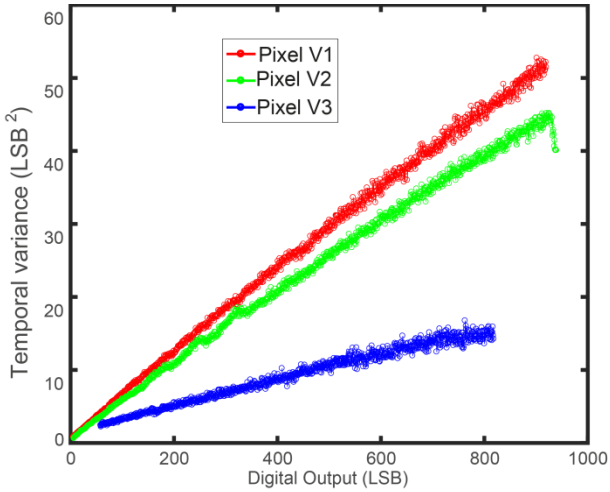


Figure 4-20. Mean-variance plots of the pixels.

By capturing the digital response of the test chip and the reference photodiode at different wavelengths, the quantum efficiency of the pixels can be calculated. The results are shown in Figure 4-21. In pixel V1, the electrons generated by the photodiodes are partly captured by the nearby n-well of the pMOS transistors, leading to a smaller QE when compared with the conventional 4T pixel. The in-pixel MIM capacitor also causes a smaller QE for the pixel V3 due to the light blocking effect of the top metal layer of the MIM capacitor.

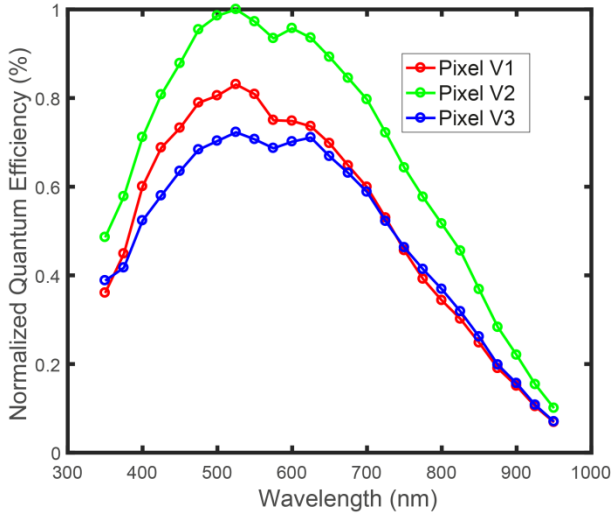
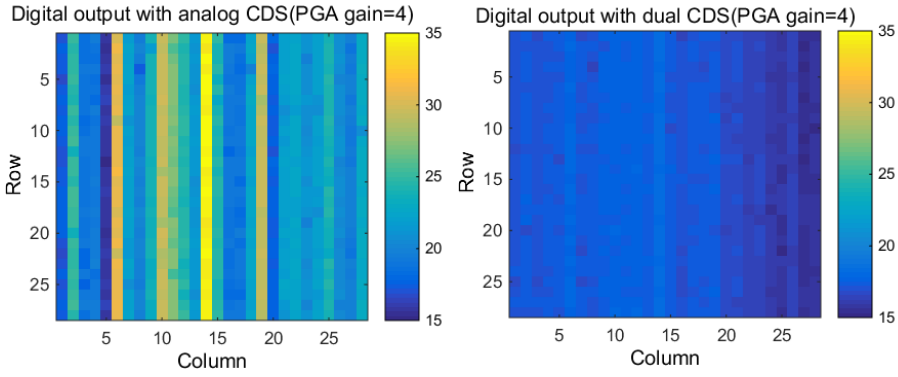


Figure 4-21. Measured quantum efficiency.

With the auto-zeroing technique used in the column ADCs, column FPN is caused by variations of the bias current in the pixel, as well as the offset and gain

errors of the column amplifier. Figure 4-22 (a) shows a captured image of the pixel V1 in dark condition using only analog CDS while Figure 4-22 (b) shows the image using the dual CDS. The PGA with a 4 × gain is used to achieve a better visual comparison. The column fixed pattern noise in Figure 4-22 (a) is mainly due to the offset errors of the column amplifier. With the assistance of the dual CDS, the column FPN of the pixel V1, V2 and V3 can be improved from 0.32 % to 0.046 %, 0.34 % to 0.048 %, 0.30 % to 0.044 %, respectively. The measured row noise for pixels V1~V3 are less than 1e- (pixel array 28 × 28).



(a) (b)

Figure 4-22. Measured digital output of the pixel V1 (a) with analog CDS; (b) with dual CDS.

4.6.4 Imaging Demonstration

Figure 4-23 shows a sample image obtained by the proposed CMOS image sensor, which is taken with 8msec exposure time and 2 × gain of the PGA. The sensor has a frame rate of 160 fps at an input clock of 50 MHz.

Figure 4-23. A sample image.

Table 4-1 shows the results of the proposed CIS compared to previously published works. Pixels V1 and V3 achieve improved linearity results. Especially, pixel V3 achieves the best linearity results and the largest full-well capacity at the cost of a lower conversion gain and larger input referred noise in the electron domain.

Table 4-1. Performance comparison.

		This Work			[4.34] 2015	[4.35] 2014	[4.36] 2017
Process (nm)		180			130	180	180
Array Size		128×128			640×480	920×256	2048×2048
Pitch (μm)		10			5.6	1.85	6.5
Fill factor (%)		47			38	NA	67
ADC Architecture		10-bit SS			10-bit SS	10-bit SAR	12-bit SS
Frame rate (fps)		160			131	9	47
Conversion gain (μV/e-)		V1	V2	V3	43	52	80/20
		56.5	47.7	18.7			
Read Noise	μVrms	310	220	215	350	5300	160
	e-rms	5.4	4.6	11.8	4.6	101	2
Full-well capacity (e-)		17270	23000	42500	23000	4994	45000
Column FPN (%)		0.046	0.048	0.044	0.45	0.5	NA
Row noise (e-)		0.87	0.95	0.94	NA	NA	NA
Nonlinearity (%)		0.20	0.38	0.14	0.18	NA	0.5
Dynamic range (dB)		70.0	73.8	71.1	84	73	87

4.7 Conclusion

In this chapter, based on the 4T pixel structures, new pixel designs featuring a better linearity performance are proposed. The chip is designed with a 180 nm CIS process. Compared to the reference 4T pixel V2, pixel V1 cancels the nonlinearity caused by the SF and shows a better overall linearity performance. Pixel V3 reduces the nonlinear ratio of the integration capacitance, and therefore also attenuates the nonlinear error caused by C_{FD}. A dual CDS technique is employed in this design to reduce the column FPN. With the assistance of the dual CDS, all pixels were able to obtain a small column FPN, less than a half LSB.

Although pixel V1 reduces the nonlinearity caused by the SF, the integration capacitor on the FD node still contributes to the nonlinearity of the pixel. Pixel V3 achieves the best linearity results among three structures at the cost of a lower conversion gain and worsened noise performance.

Furthermore, the readout circuitry also degrades the overall linearity performance of the image sensor. New solutions still need to be considered to further reduce the nonlinearity caused by the pixel and the following readout circuitry, which will be introduced in the next chapter.

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Chapter 5 A Digitally Assisted Linearity-Calibration Targeting High Linearity

This chapter of the thesis is based on the publication :

F. Wang, Qiang. L. H, A. J. P. Theuwissen, "A Highly Linear CMOS Image Sensor with a Digitally Assisted Calibration Method," in *Proc. Int. Image Sensors Workshop*, Japan, pp. 336-339, 2017.

Chapter 4 proposed two types of pixel designs to improve the linearity from different standpoints. However, the nonlinear C_{FD} and following readout circuitry still contribute to the nonlinear errors of the image sensor. In this chapter, a digital assisted calibration method is employed to further improve the linearity of the image sensor. A hybrid behavioral model of the CIS is proposed to verify the effectiveness of the calibration method as well as providing design guidance for the circuit design. Subsequently, TCAD simulation results are used to help explain the spill-back effect of the transfer transistor's channel, which also explains the decreasing linearity performance of the pixel due to the increasing voltage of V_{TXH}. V_{TXH} is the high voltage of the transfer transistor in the pixel. Silicon experimental results show that the on-chip linearity correction efficiently suppressed the sensor's nonlinearity to a value less than 0.06 % for the pixels.

This chapter starts with an introduction. Next, Section 5.2 states the readout chain design of the prototype CMOS image sensor. The calibration method is presented in section 5.3. A hybrid behavioral model used to validate the calibration method is presented in Section 5.4. The measurement results of the fabricated image sensor are presented in 5.5. The conclusions are drawn in Section 5.6.

5.1 Introduction

In the last chapter, two types of pixel designs are proposed to realize pixel-level linearity optimization from different standpoints. Nevertheless, the pixel designs cannot overcome the nonlinearity caused by the nonlinear integration capacitor. Pixel V3 achieves a nonlinearity of 0.14 %, which is still above the nonlinearity requirement for the lithography applications. Further, pixel V3 has a small conversion gain which leads to a large noise in electron domain. The other solutions should be proposed to further improve the linearity of the image sensors.

Some other techniques are also proposed to improve the linearity of the pixel. In [5.1] and [5.2], two types of pixel design based on the capacitive transimpedance amplifier structure are proposed to improve the linearity on pixel-level. However, the pixel that uses the CTIA structure has disadvantages such as a high power consumption and a low fill factor. More importantly, its poorer noise performance has prevented it from being widely used.

Furthermore, the readout circuitry of the image sensor also introduces nonlinear errors to the imaging system. In this chapter, a digitally assisted linearity-calibration method is employed to further improve the linearity based on the design of Chapter 4. The buffer pixel V1 and traditional 4T pixel V2 are employed to verify the calibration method.

An image sensor system is a multi-physical heterogeneous system which includes optical and electronic blocks. A hybrid behavioral model of the CIS using MATLAB and Verilog-A, is proposed to speed up the simulation and validate the linearity-calibration method in this Chapter.

5.2 Chip Design

In this Chapter, a test chip based on the design presented in Chapter 4 is proposed. Digital calibration is employed in this design.

Figure 5-1 shows the schematic and the timing diagram of the readout chain. Similar with the previous chip, the column-parallel chain contains a switched capacitor amplifier, a SS-ADC, and SRAM.

There are several points which are different compared to the chip design introduced in the last chapter.

First, in this design, only analog CDS is adopted. The FPN caused by the offset of the amplifier can be canceled by subtracting a dark reference frame, obtained from the average value of multiple frames to eliminate the temporal noise [5.3]-[5.4].

Second, the sample and hold circuit is bypassed to further reduce the frame time and readout noise.

The third and the most important is the 12-bit onboard current steering DAC used in replacement of the on-chip ramp generator. It is a 12-bit onboard current steering DAC employed to provide a ramp signal V_{RAMP} in relation to the calibration method which will be introduced in the following section. A higher resolution DAC can provide a more linear ramp signal for the ADC. Due to the advantages of high speed and high resolution, the structure of current steering is chosen for the DAC. The schematic of ramp generator is shown in Figure 5-2.

There are two clock signals in this design. Φ_{CLK_A} is the clock of the 10-bit ADC which operates at 12.5MHz while Φ_{CLK_D} is the clock of the 12-bit DAC, which runs at 50 MHz. When the Φ_{DAC_EN} is high, the 12-bit DAC generates the ramp signal V_{RAMP} for the 10-bit ADC. Simultaneously, the column counter calculates the period of the comparator's output. The other digital control signals are the same with the signals shown in Figure 4-12.

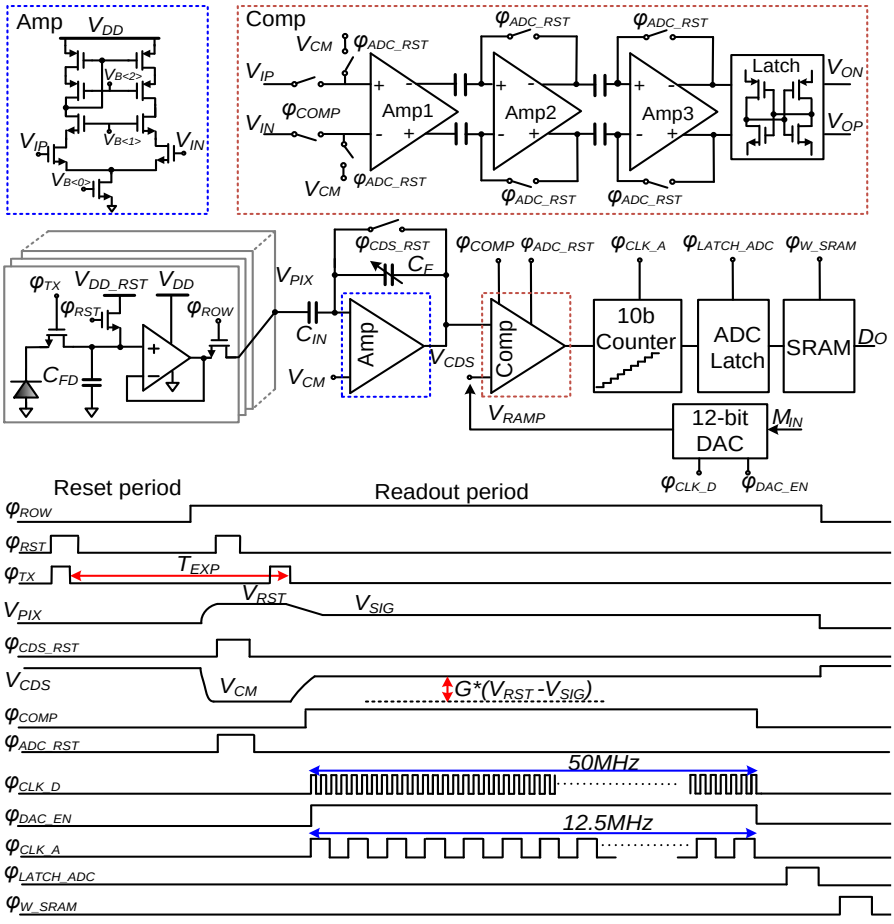


Figure 5-1. The schematic and timing diagram of the readout chain.

As shown in the schematic of Figure 5-2, the 12-bit current steering DAC converts the digital input signal from the FPGA into two differential current outputs. The loading resistors R_{RAMP1} and R_{RAMP2} convey the current outputs to two differential voltage outputs. Then a high bandwidth OPA combined with R_1~R_4, transforms the differential analog voltage to the single-ended ramp signal V_{RAMP}, which is shared by all column ADC.

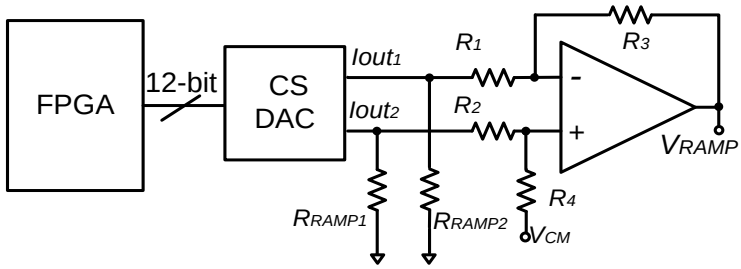


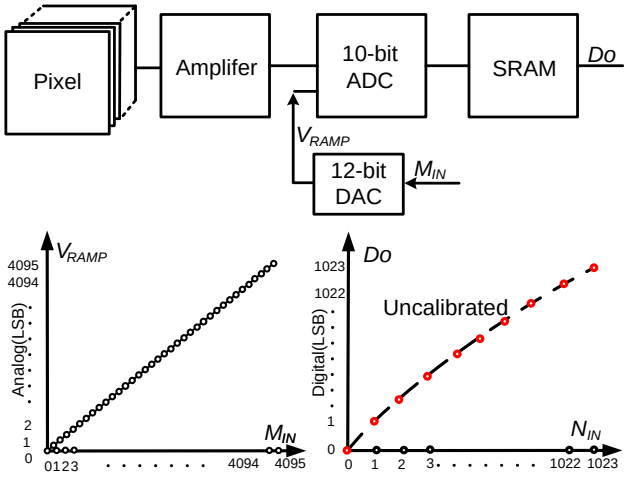
Figure 5-2. The schematic of the ramp generator based in a current steering DAC (CS DAC).

5.3 Calibration Method

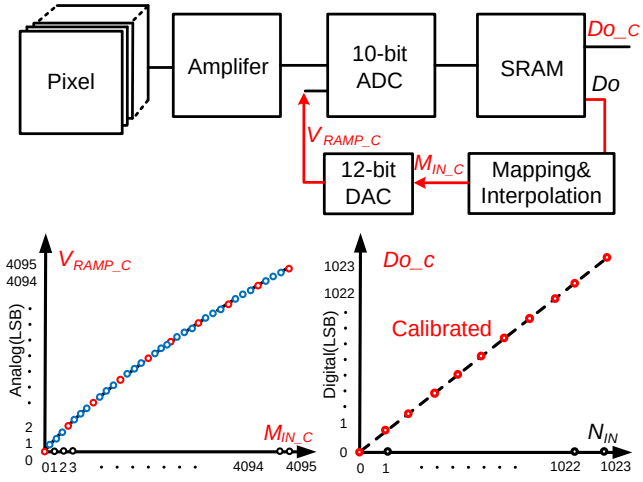
The image sensor discussed in this chapter employs the analog CDS and has two operation modes: normal mode and calibration mode. In normal mode shown in Figure 5-3 (a), the image sensor works conventionally. The operation goes as follows: M_{IN} is the digital input code of the DAC, which increases from 0 to 4095 (2^{12}-1) evenly, with which the 12-bit DAC generates a linear ramp signal V_{RAMP} for the 10-bit ADC. During the linearity measurements, the intensity of the incoming light is fixed. The number of incident photons coming to the sensor is evenly increasing by varying the exposure time from 1 T_{EXP} to 1024 × $T_{EXP.}$ The digital output of the 10-bit ADC is captured and saved into the SRAM within each exposure time. N_{IN} is the exposure sequence. Due to the nonlinearity of the imaging system, the transfer function from the incremental injected photons to the individual digital output (*Do*) is not linear, which could be observed in Figure 5-3 (a).

Based on the nonlinear transfer function of the CIS, the nonlinearities of the whole system can be analyzed. The nonlinear behavior of the CIS is copied into the ADC circuitry and to create a new nonlinear ramp signal for the ADC. In the calibration mode illustrated in Figure 5-3 (b), after the transfer curve of the image sensor has been captured in normal mode, a new ramp signal V_{RAMP_C} is used to realize the calibration. M_{IN_C} is the corresponding output sequence after mapping and interpolation. The mapping process removes the offset and the gain errors of the data collected from the SRAMs. Interpolation is needed for the 12-bit DAC.

After the interpolation, the calibrated ramp signal V_{RAMP_C} contains the information of the nonlinearities of the pixel and of the following readout circuitry. The new ramp signal will cancel out these nonlinearity in the output signal after calibration. In other words, the new ramp signal is deliberately made nonlinear, but in a very controlled way, to compensate the shortcoming of the sensor as far as nonlinearity is concerned.



(a)



(b)

Figure 5-3. (a) Operation in normal mode; (b) Operation in calibration mode of the CIS.

5.4 Behavioral Model

At the architectural level, various behavioral modeling languages, such as MATLAB, Simulink and Verilog-A, are commonly used in the circuit design to speed up the simulation with an acceptable accuracy [5.5], [5.6]. In this section, a hybrid behavioral model of the CIS is built for the validation of the proposed calibration algorithm and performance estimation.

In [5.7], based on the analysis of the nonlinear sources of the image sensor system, a mathematic model of the pixel's response using MATLAB has been presented. The Capacitance-Voltage characteristic of the C_{FD} and the nonlinearity of G_{SF} are well investigated.

Figure 5-4 depicts a behavioral model of the CIS system with the digital calibration mentioned above. Different description languages are used to extract the behavioral models of the optical and electronic components. The input of the signal chain is the number of incident photons which is regarded as linear. The average number of incident photons linearly increases with the exposure time. The photocurrent integrated on C_{FD} and is converted into an analog voltage value. The voltage is read out through the in-pixel voltage buffer either realized by the source follower or by the analog buffer. After the pixel's signal is sent to the column amplifier, the following ADC circuit digitalizes the analog voltage. The final output is the digital number (DN).

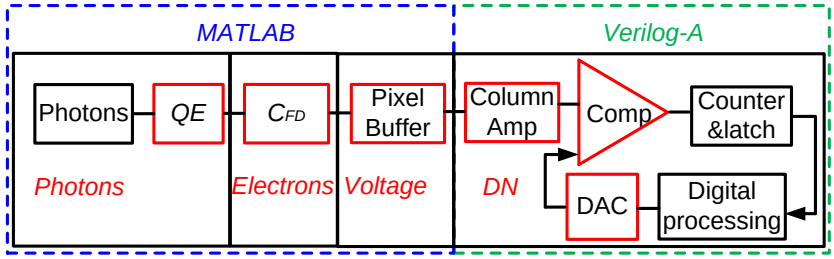


Figure 5-4. The behavioral model of the CIS system.

Using the same technology, based on the proposed model in Chapter 3, the same algorithm is employed to build a compact behavioral model of the pixel V1 and V2 with MATLAB. The next analog, mixed-signal circuits and digital processing circuits are described by Verilog-A. In this heterogeneous system model, the non-ideality factors of the blocks in red line are considered, which have been listed in Table 5-1, with QE being the quantum efficiency of the pixels.

Table 5-1. Non-idealities in the CIS.

Blocks	Non-idealities in the system	Description language
QE	Differences among pixels	MATLAB
Integration capacitor	Dependence of the output voltage, dependence of the buffer's gain, non-uniformity	MATLAB
Pixel Buffer (Pixel V1)	Noise, gain error, non-uniformity	MATLAB
Pixel Buffer (Pixel V2)	Noise, dependence of the output voltage, non-uniformity	MATLAB
Column amplifier	Gain error, offset, non-uniformity of the capacitor	Verilog A
Comparator	Gain error, offset, noise, delay time	Verilog A
DAC	Offset, noise, non-uniformity of the current sources	Verilog A

In Figure 5-5, the primary vertical axis on the left plots the simulation results of the corresponding gain of the voltage buffers in both pixels and with the proposed model in [5.7], whereas the secondary vertical axis on the right side depicts the Capacitance-Voltage characteristics of the C_{FD}. The horizontal axis is the output voltage range of the pixel.

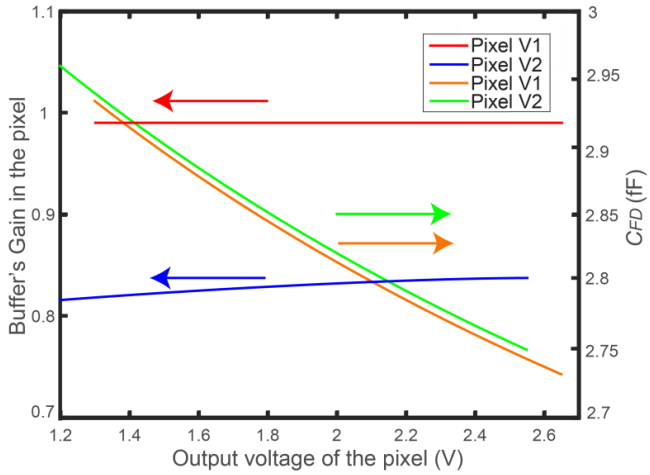


Figure 5-5. Output voltage vs. Gain of the pixel's buffer & *C-V* characteristic of C_{FD}.

In the above simulation, V_{RST_DD} is set as 2.7 V, while the power supply of the pixel V_{DD} in the pixels is 3.3 V. The bias current is 10 μA for both pixels. The red and orange lines represent the modeling results of the pixel V1 while the blue and green lines give that of the pixel V2. Configured in a closed-loop, the pixel V1

realizes a constant nearly unity-gain, whose value is only determined by the open loop gain of the OPA. For the 4T pixel V2, the gain of the source follower is not constant. It increases with the output voltage of the pixel V_{PIX}. The output voltage of the pixel V2 is also lower than that of the pixel V1 due to the SF's threshold voltage.

Figure 5-5 also gives the simulation results of the Capacitance-Voltage characteristics of the C_{FD} in the pixel V1 and V2, where the FD capacitances decrease with the output voltage of the pixel. The average values of the capacitances over the whole range of the output voltage are chosen as the modeled value of the C_{FD}.

This behavioral model of the CIS system not only provides an early validation of the image sensor calibration algorithms, but also gives guidance to the circuit design. The DAC's resolution and linearity performance both affect the nonlinearity of the image sensor and the effectiveness of the calibration method. Figure 5-6 shows the nonlinearity simulation results of the CIS based on the proposed hybrid model.

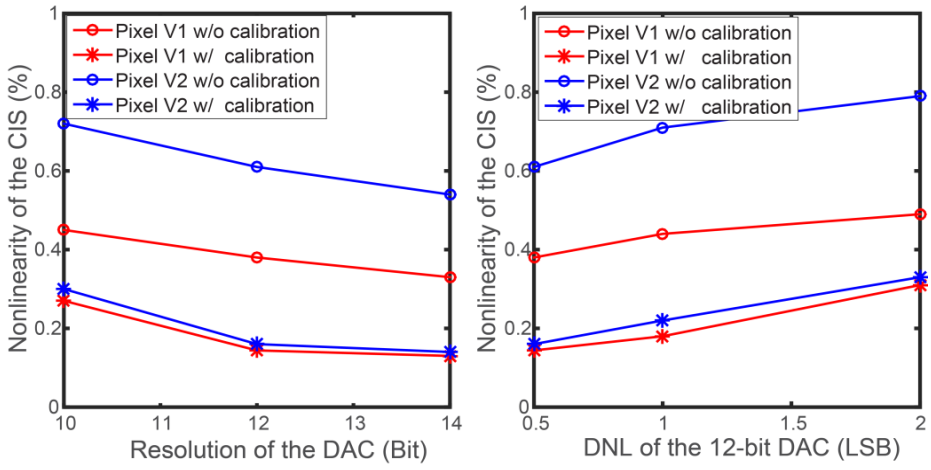


Figure 5-6. The simulation results of the linearity performance. (a) with different resolution of the DAC; (b) with different DNL value of the 12-bit DAC.

In Figure 5-6 (a) it can be seen that when the resolution of the DAC increases from 10-bit to 14-bit and with a DNL value of the DAC always less than half LSB, the linearity of the image sensor system with pixel V1 and V2 is improved, especially with the assistance of the calibration method. When the DAC's resolution increases from 12-bit to 14-bit, the linearity improvement is limited. To reduce the operating time and the complexity of the system, a 12-bit DAC is employed to provide a ramp signal for the 10-bit ADC in this design.

Figure 5-6 (b) plots the modeling results of the CIS's nonlinearity build on a 12-bit DAC with different DNL values. When the DNL of the DAC is less than half LSB, the nonlinearity of the whole CIS system can be improved from 0.38 % to 0.14 %, and 0.61 % to 0.16 % respectively for V1 and V2, with the assistance of the calibration method. However, the improvement is less effective when the linearity performance of DAC deteriorates. So a high-resolution DAC with good linearity performance is needed.

5.5 Measured Results

For the linearity measurement, the light condition is fixed. The number of photons coming to the image sensor is changed by increasing the exposure time from 1 μs to 1024 μs evenly. Figure 5-7 shows the nonlinearity results of the pixel V1 and V2 with different values of V_{TXH}, which is the high voltage of the transfer transistor in the pixel.

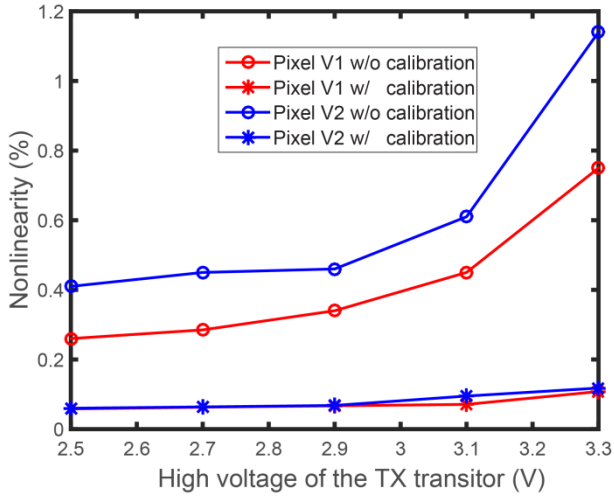


Figure 5-7. Nonlinearity performance of the pixels with different V_{THX}.

In the measurement, V_{RST_DD} is set as 2.7 V as the setting in the simulation, which is lower than the power supply of the pixel. This is a requirement of the linear input range for the analog buffer in the pixel V1 at the cost of a lower full-well capacity. The value of V_{TXH} is related to the characteristics of the pixel, such as the dark current and FPN [5.8]. In the measurement, V_{TXH} is variable from 2.5 V to 3.3 V. The input range of the ADC is set as 1V. All linearity evaluations are done with a window containing 28 × 28 pixels averaged over the 200 frames captured. According to the measurement results, a higher value of V_{TXH} leads to a worse linearity of the CIS. When V_{TXH} equals 2.5 V, the nonlinearity of pixel V1

and V2 is 0.24 % and 0.41 %, respectively. When V_{TXH} equals 3.3 V, the nonlinearity of the pixel V1 is 0.76 % while that of the 4T pixel V2 is 1.14 %.

In [5.9], it is explained that the value of V_{TXH} affects the pixel's performance due to the charge spill-back effect. In Figure 5-8, the transfer curves of the pixel V1 for different V_{TXH} values are plotted.

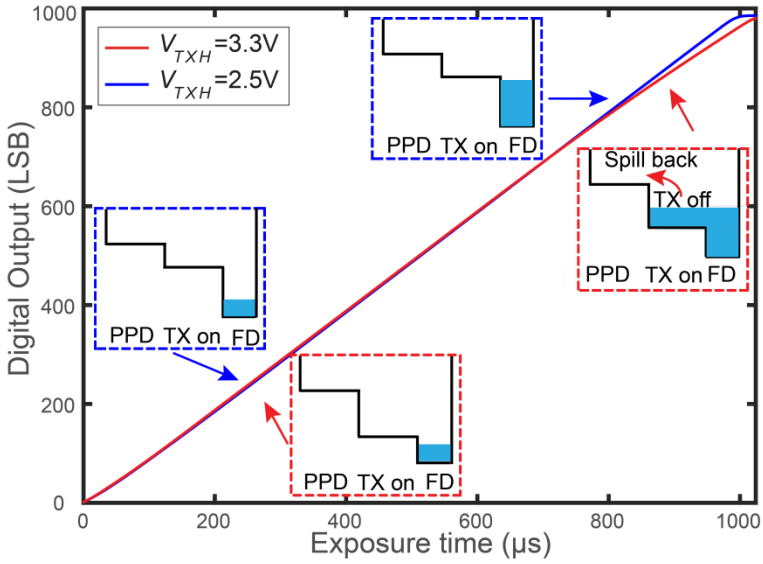


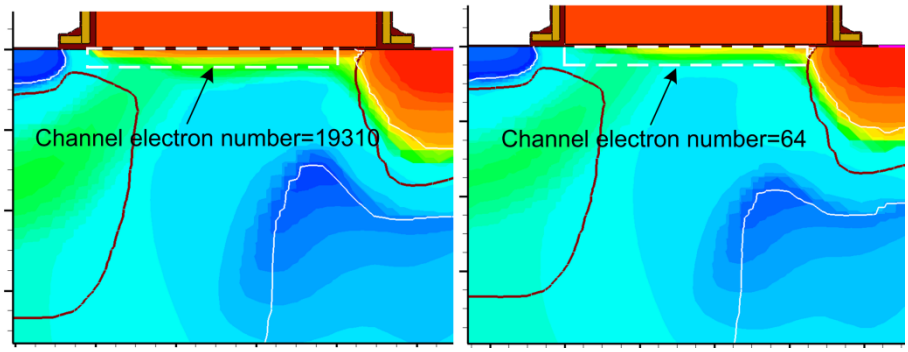
Figure 5-8. Digital output of pixel V1 vs. exposure time.

In the small signal region, the charge transfer channel under the gate of the transfer transistor is always in the depletion mode. When the number of transferred electrons increases, the potential of the FD will become lower. In the large signal region, the charge transfer channel enters into the inversion mode. Electrons can spill back to the PPD when the TX is switched off. A higher V_{TXH} enables the channel to enter the inversion mode earlier. This explains why a pixel with a higher V_{TXH} has a worse linearity performance. So the linearity with lower V_{TXH} is better, if the charge transfer can be completed with this lower values and/or if the transfer time is long enough to avoid image lag [5.10].

The simulation results of Sentaurus TCAD tool are used to verify the above analysis. Plotted in Figure 5-9 is the electron density at the end of the charge transfer phase with high and low light illumination. In Figure 5-9 (a), with highlight illumination, the channel of TX accumulates many electrons and enters to the inversion mode due to the decreasing voltage on FD, while the channel of TX in Figure 5-9 (b) is working in the depleted mode with a few number of accumulated electrons.

As pointed out in [5.10] after the TX is closed，the spill-back effect can

encourage the electrons in the channel to return to the FD, which will worsen the linearity performance of the pixels.



(a) (b)

Figure 5-9. Electron density during the end of charge transfer phase: (a) High illumination; (b) Low illumination.

Similar to the conventional nMOS transistor, a higher voltage on the gate can accumulate more electrons in the channel, it also happens to the TX. Figure 5-10 shows the simulated electron current density underneath the TX, 1ns after the TX is turned off. In the simulation, when V_{TXH} is equal to 3.3 V, the ratio of the electrons flown back to the PPD over the total accumulated charges is 0.6 %. When V_{TXH} reaches 3 V, the ratio becomes smaller (less than 0.1 %) which means fewer electrons return back to the PPD. The linearity in the high illumination region becomes better.

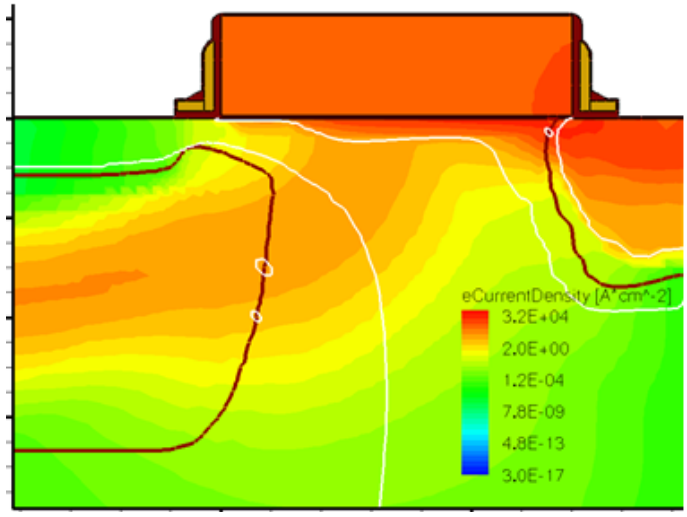


Figure 5-10. Electron current density: 1ns after TX is switched off.

Although a high V_{TXH} leads to a degrading linearity performance, the calibration method proposed improves the pixels' linearity effectively. The pixels have better linearity results after the calibration. When V_{TXH} equals 2.5 V, the nonlinearity of the pixel V1 and V2 is respectively 0.24 % and 0.41 % before calibration. After calibration, the averaged output of both pixel arrays achieves a measured nonlinearity less than 0.06 %, which is shown in Figure 5-7.

Figure 5-11 (a) plots the digital output of the image sensor based on the pixel V1 when V_{THX} equals to 2.5V. According to the EMAV1288, 5 % ~ 95 % of the whole output range is chosen to calculate the nonlinearity. Figure 5-11 (b) and (c) plot the DNL and INL result of the image sensor with pixel V1, respectively. We can calculate the nonlinearity based on the maximum and minimum value of the INL. The blue lines show the measurement results without calibration, and the red lines represent those with calibration. From Figure 5-11, it is clear that the calibration method effectively improves the linearity result of the image sensor.

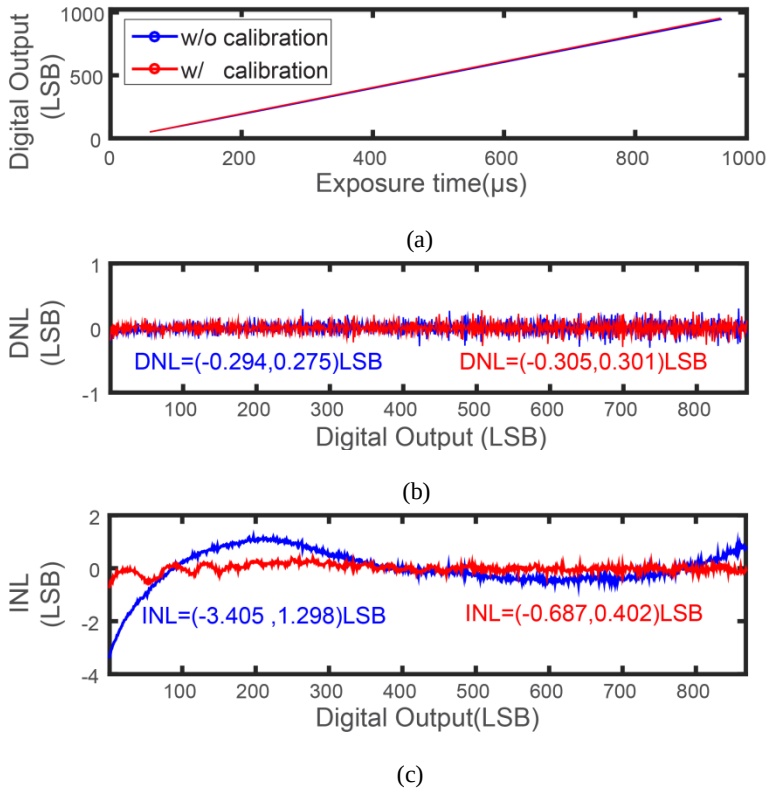


Figure 5-11. The nonlinearity of pixel V1(V_{TXH}=2.5V).

Figure 5-11 shows the nonlinearity improvement within 5 % to 95 % of the output range. In the full output range of the image sensor, the nonlinearity of the pixel V1 and V2 has been improved from 0.28 %, 0.48 % to 0.071 % and 0.062 %

respectively after calibration. The results also verify the effectiveness of the calibration method at low photon flux condition.

Figure 5-12 plots the nonlinearity results for each pixel in the pixel array V1 and V2. We can observe obvious improvement on linearity for each pixel with calibration.

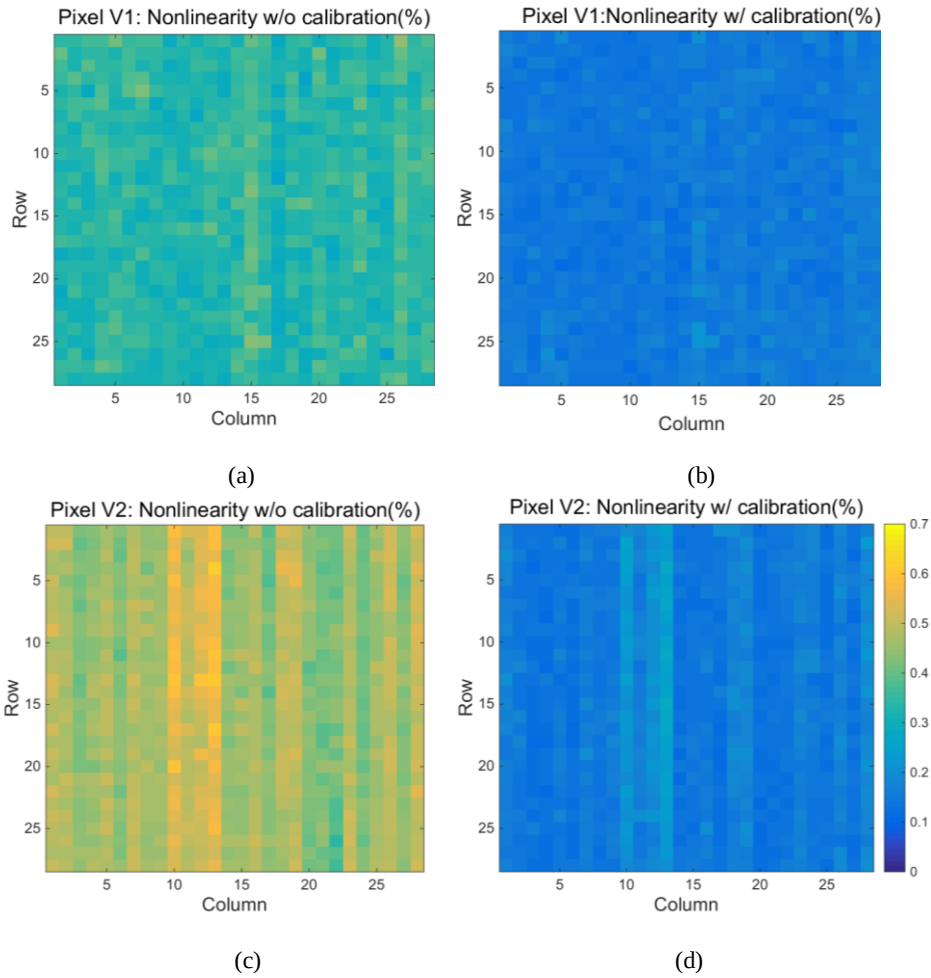
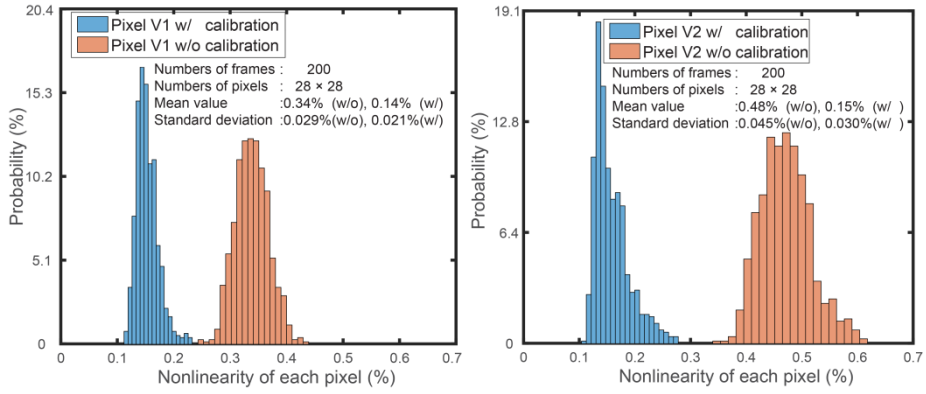


Figure 5-12. Nonlinearity of each pixel (a) Pixel V1 w/o calibration; (b) Pixel V1 w/ calibration; (c) Pixel V2 w/o calibration; (d) Pixel V2 w/ calibration.

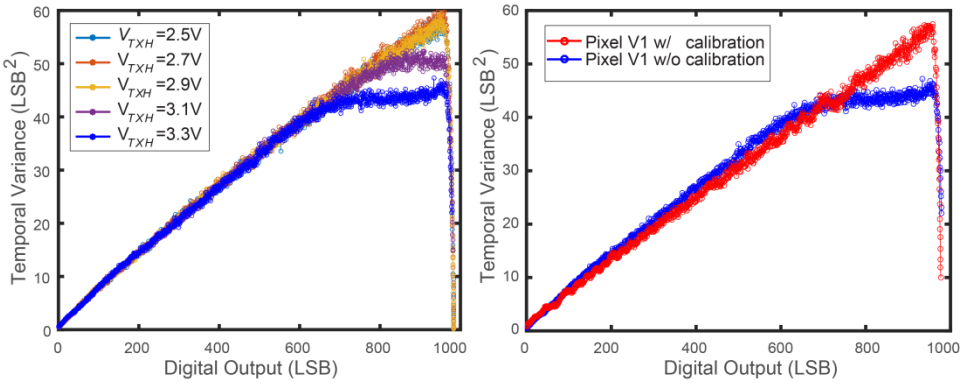
Figure 5-13 shows the corresponding histogram of the nonlinearity results in the pixel array. Mean value of the nonlinearity of single pixel in the pixel array V1 and V2 is respectively 0.34 % and 0.48 % without calibration. With the assistance of the calibration, the value of pixel V1 and V2 becomes 0.14 % and 0.15 % respectively.



(a) (b)

Figure 5-13. Histogram of the nonlinearity in (a) Pixel V1 array; (b) Pixel V2 array.

It is also easy to observe the spill-back effect from the mean-variance curve. Figure 5-14 (a) shows the mean-variance curves of the pixel V1 with different values of the V_{TXH}. When V_{TXH} is higher than 3.0 V, the digital response at the saturation region is very unlinear. Figure 5-14 (b) plots the Mean-Variance curve of the pixel V1 after calibration. When V_{TXH} equals 3.3 V, the Mean-Variance curve which is close to the saturation region becomes normal. Actually, the calibration cannot cancel off the spill-back effect; however, it can calibrate the digital output. This is another way to validate the effectiveness of the calibration method. Pixel V2 has the same trend as pixel V1 at different values of V_{TXH}.



(a) (b)

Figure 5-14. (a) Mean-variance curve of pixel V1 with different V_{THX}; (b) Mean-variance curve of pixel V1with calibration (V_{THX}=3.3V).

The calibration method is also valid for the other settings. Figure 5-15 shows the linearity improvement for the pixel V1 and V2 as a function of the gain of the

column amplifier. When the gain of the column amplifier varies from 1 × to 8 ×, the nonlinearity of the CIS has been improved with the proposed calibration method.

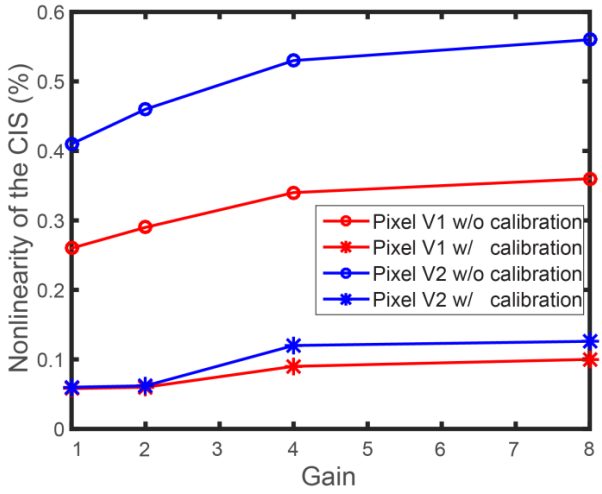


Figure 5-15. Nonlinearity performances of the pixels as a function of the gain.

In the linearity measurement mentioned above, we use a constant illumination and the minimal exposure time is 1μs. To prove the calibration method is useful in different illumination conditions, the same input code of the ramp signal extracted from the measured results with 1μs unit exposure time is used. Then we change the illumination intensity and exposure time, and we finish the nonlinearity measurements with calibration. From Figure 5-16, the conclusion can be drawn that the calibration method is valid under different light intensities.

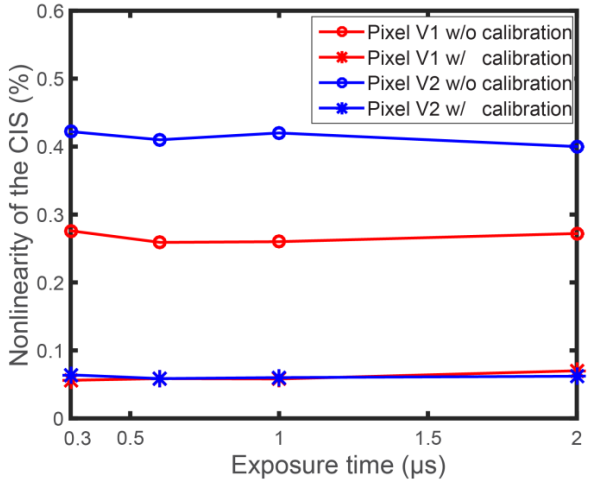


Figure 5-16. Nonlinearity performances of the pixels as a function of the exposure time.

Figure 5-17 plots the nonlinearity performances of the CIS at the different wavelengths. A monochromator ranges from 300 to 1000 nm and a small-size integrating sphere is used to obtain the desired bandwidth of light. By extracting the digital output of the CIS at the wavelength of 460 nm, the same calibration code is used to calibrate the CIS at the other wavelengths. Figure 5-17 shows that the calibration method is valid for the CMOS image sensor at the different wavelengths, which is of great importance to color image sensors.

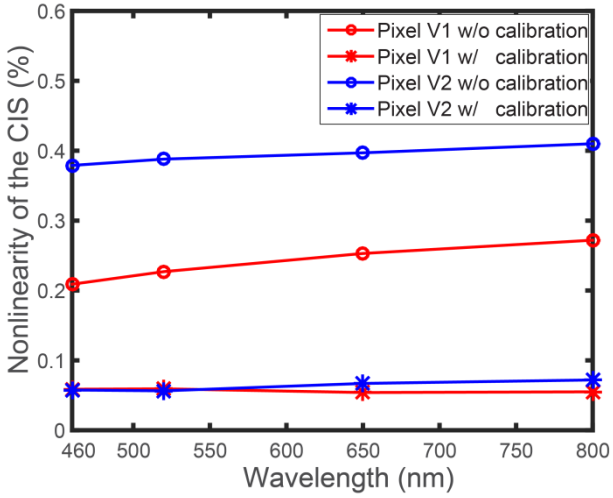


Figure 5-17. Nonlinearity performances of the pixels as a function of the wavelength.

The simulation results of the conversion gain for the pixel V1 is 55.7 μV/e-, while that of the pixel V2 is 46.9 μV/e-. The measured results of the conversion gain are 56.8 μV/e- and 45.3 μV/e- for pixel V1 and pixel V2, respectively. The measured results are in line with the simulation results.

Compared with the standard 4T pixel, the pixel V1 introduces more input referred noise in the voltage domain. Figure 5-18 shows the input-referred noise voltage in dark for the proposed pixels with different amplifier gain setting. Pixel V1 has a slightly higher input-referred noise than that of the 4T pixel V2. The programmable gain of the column amplifier efficiently suppresses the input-referred random noise. The input-referred noise of pixel V1 and V2 is respectively 234 μVrms and 189 μVrms at an analog gain of 8 ×. Nevertheless, the pixel V1 achieves a lower input-referred noise in the electron domain due to the larger conversion gain, compared with 4T pixel V2. When the gain of the column amplifier is 8 ×, the readout noise is 4.12 e- for pixel V1 and 4.17 e- for pixel V2.

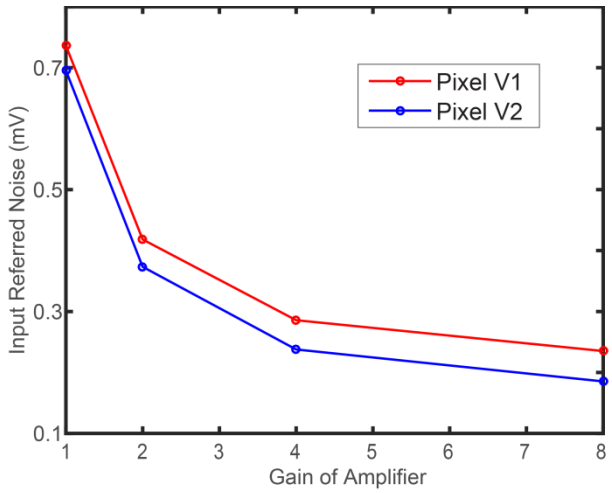
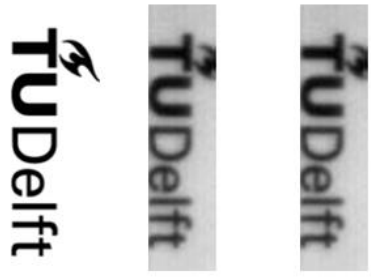


Figure 5-18. Input-referred noise vs. column amplifier gain.

The whole pixel array is 128 × 128 in this design, which contains several different types of pixel designs. In this chapter, pixel V1 and V2 are used to compare and validate the effectiveness of the calibration method. For image sensor demonstration purposes, we choose the images taken by the pixel V1 array whose size is 128 × 32. Figure 5-19 (a) is a sampled picture while (b) and (c) show the captured figure by pixel V1 array at a frame rate of 60 frames/s without and with calibration.



(a) (b) (c)

Figure 5-19. (a) Sample picture; (b) Captured picture (Pixel V1) w/o calibration; (c) Captured picture (Pixel V1) w/ calibration.

From Figure 5-19, it is not easy to observe the linearity improvement from the monochrome photo. In a future design, color filters will be added on the sensor to get a clear visual comparison on the effectiveness of the calibration.

The measurement results of the proposed image sensor are summarized in Table 5-2. Compared with previously published works [5.1], [5.11]-[5.14], this work defines the best performance in linearity. After calibration, both pixels have

a nonlinearity which is less than 0.06 %. In contrast to off-chip calibrations, this method can reduce the following off-chip processing time and improve the system efficiency, as well as attain better linearity results. The proposed calibration method can realize high linearity without adopting a special pixel design.

The linearity performance of the DAC decides the effectiveness of the calibration. A high resolution and highly linear on-chip DAC is preferred. The transfer curve of the CIS captured at low-speed clock can be used to calibrate the digital output where DAC works at high speed. This method can also be applied to the commercial CIS which has a large pixel array.

5.6 Conclusion

In this chapter, based on the circuit design introduced in Chapter 4, an on-chip calibration method is proposed to address the nonlinear errors caused by the pixels and readout circuitry. Without adding any cost on chip area, power consumption and speed, the proposed calibration method realizes excellent linearity improvement of the image sensors. A hybrid behavioral model of the whole image sensor system is proposed to verify the validity of the calibration method. Measured results show that both pixels achieve a nonlinearity of less than 0.06 % with the assistance of the calibration method.

Table 5-2. Performance comparison.

Reference		**This Work**		[5.1]	[5.11]	[5.12]	[5.13]		[5.14]
Linearity improvement techniques		**Pixel optimization & digital calibration**		Pixel optimization	LUT calibration	Feedback mechanism	Pixel optimization		N/A
Array size		**128 × 128**		128 × 160	640 × 480	54 × 60	64 × 128		1032 × 1024
Global/Rolling shutter		**RS**		RS	RS	RS	RS		RS
ADC Architecture		**10-bit SS-ADC**		12-bit SS-ADC	10-bit ADC	Off-chip 14-bit ADC	Off-chip 16-bit ADC		13~19-bit Folding + Cyclic ADC
Process	nm	**180**		180	180	180	180		180
Pixel size	μm^2	**10 × 10**		12 × 10	6.2 × 6.2	25 × 25	11 × 11		7.5 × 7.5
Fill factor	%	**47**		36	49	68	51		52
Frame rate	fps	**60**		40	30	100	N/A		4
Pixel type		**Buffer**	**4T**	CTIA	3T	4T current mode	4T	4T optimized	4T
Conversion gain	µV/e-	**56.8**	**45.3**	40	N/A	N/A	71	122	67
Read Noise	µVrms	**234**	**189**	656	N/A	1560	92	134	80
	e-rms	**4.12 (Gain=8)**	**4.17 (Gain=8)**	16.4 (Gain=8)	50	N/A	1.3 (Gain=16)	1.1 (Gain=16)	1.2
Full well capacity	e-	**17270**	**20960**	30613	N/A	1M	8730	3739	14950
Dynamic range	dB	**72.4**	**74**	65	72	52	77	71	82
Nonlinearity	w/o calibration (%)	**0.24**	**0.42**	0.095	1.8	1.7	0.3	0.2	0.32
	w/ calibration (%)	**0.058**	**0.06**		0.5	0.51			

Acknowledgment

The author would like to thank Dr. Han for his support on the TCAD simulation.

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Chapter 6 Temperature Effect on the Linearity Performance of a CIS

This chapter of the thesis is based on the publication:

F. Wang, A. J. P. Theuwissen, "Temperature effect on the linearity performance of a CMOS image sensor," *IEEE Sensors letter*., vol. 2, no. 3, pp. 1-4, 2018.

This chapter focuses on the analysis of the operating temperature effect on a CMOS image sensor's performance, especially the linearity behavior. As the temperature increases, the value of the integration capacitor C_{FD} on the FD region increases as well. Moreover, the gain of the in-pixel voltage buffer decreases. These two factors lead to a reduced conversion gain of the pixel at a higher temperature. Because of the increase of the nonlinear part of the C_{FD}, the linearity of the CIS at a higher temperature will deteriorate as well. Measurement results conducted on the prototype image sensor which is proposed in Chapter 5, agree well with an updated analytical model of the CIS and demonstrate an efficient linearity improvement at different temperatures with the calibration method.

Section 6.1 emphasizes the importance of the temperature analysis on the CMOS image sensors' performances. A theoretical analysis is presented in section 6.2. The measured linearity temperature dependency based on the fabricated image sensor are presented in Section 6.3. A summary is given in Section 6.4.

6.1 Introduction

The operating temperature of a CIS is an important element that can influence the characteristics of the electronic components. In some applications, such as the image sensors used in autonomous vehicles, the image sensor should be able to withstand harsh temperatures due to the complex driving environment [6.1], [6.2], such as blazing sunlight and temperature variations.

The imaging quality of the image sensors is significantly affected by the temperature. Most notable is the dark current, which is strongly temperature-dependent [6.3], [6.4]. The temperature dependence of the full-well capacity in the image sensor has also been discussed in [6.4]. By using an analytical model of the pinned photodiode, the authors successfully explained the FWC variations on the temperature and verified the conclusion through a test chip. Based on the bias current's temperature characteristics of the pixel, a temperature compensation method is introduced in [6.5] to stabilize the output of the CIS against any temperature variations. However, the temperature effect on the linearity performance of the image sensors has not been well studied.

As introduced in Chapter 3 of this thesis, the linearity of a CIS is mainly constrained by the transfer function of the pixel, where the gain of the voltage buffer and the integration capacitor in the pixel are two determining factors. These two factors have a complicated temperature dependency, which will be discussed in the following section.

In this chapter, the temperature effects on the linearity characteristic of the CIS are analyzed. By adding the temperature model of the elements in the proposed model, it is possible to perform a temperature-dependent linearity modeling of the CIS. The analysis is experimentally verified by using two types of pixels, introduced in Chapter 4. Measurement results are in line with the modeling results with respect to temperature variations. The results also demonstrate an efficient linearity improvement at different temperatures with the assistance of the calibration method proposed in Chapter 5.

6.2 Temperature Dependency Analysis

The operating temperature affects the properties of CMOS transistors. First of all, the temperature changes the value of the band gap energy E_g [6.6], which further affects the other electrical characteristics of the semiconductor device. A higher temperature accelerates the atoms vibration [6.6], the space between atoms will increase, which decreases the value of the band gap energy. Based on this theory, Varshni [6.6] proposed a semi-empirical equation of E_g, shown in Eq. (6-1):

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{6-1}$$

where E_g (0) is the band gap energy at a temperature of absolute zero Kelvin, which is equal to -273.15 degrees Celsius (°C) [6.6], T is the temperature of the semiconductor; α and β are fitting parameters [6.6], which are decided by the material type. Figure 6-1 shows the corresponding band gap energy value of three different materials: silicon, gallium arsenide and germanium at different temperatures [6.7]. As shown in Figure 6-1, the band gap energy values of these materials decrease with an increase of the temperature.

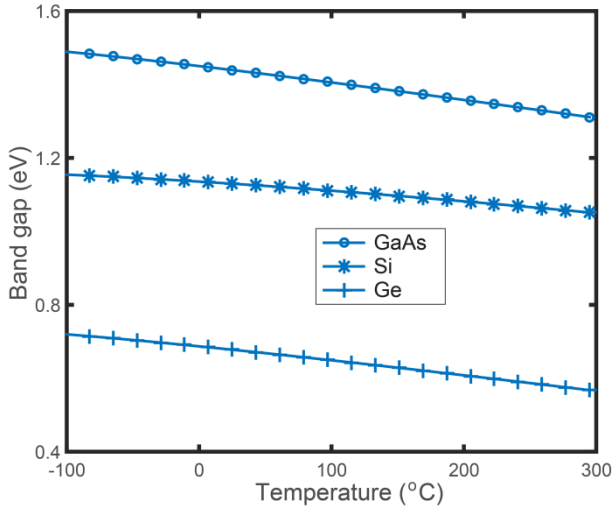


Figure 6-1. The band gap of the semiconductor materials as a function of temperature [6.6].

In CMOS transistors, the carrier mobility μ and the threshold voltage V_{th} are the two most important temperature-dependent physical parameters. Eq. (6-2) shows the value of the transistor's mobility μ as a function of the temperature [6.5].

$$\mu(T) = \mu(T_0)(T / T_0)^{T_{C\mu}} \tag{6-2}$$

Here, $\mu(T_0)$ is the transistor's mobility at room temperature T_0; $T_{C\mu}$ is a negative temperature coefficient (T_C) of the mobility [6.7], which leads to a decreasing μ with a rising temperature.

As shown in Eq. (3-4), the threshold voltage V_{th} is affected by the value of Fermi potential φ_F and V_{th0}. φ_F has a complex temperature dependency as shown in Eq. (6-3); φ_F is directly proportional to the temperature. Furthermore, it is related to the value of the material's intrinsic carrier concentration n_i and the impurity concentration of the substrate N_A [6.7].

$$\varphi_F = kT / q \ln(N_A / n_i) \tag{6-3}$$

The intrinsic carrier concentration n_i also has a strong temperature dependence [6.7], shown in Eq. (6-4).

$$n_i \infty T^{1.5} e^{-E_g(0)/2kT} \tag{6-4}$$

To simplify the analysis, the temperature dependence of V_{th} is modeled with a linear function shown in Eq. (6-5), where $V_{th}(T_0)$ is the threshold voltage value at room temperature and the temperature coefficient T_{CVth} is related to the transistor size [6.8].

$$V_{th}(T) = V_{th}(T_0) + T_{CVth}(T - T_0) \tag{6-5}$$

For the transistor working as the bias current circuit of the pixel, based on a SPICE simulation, V_{th} has a negative temperature coefficient, as shown in Figure 6-2.

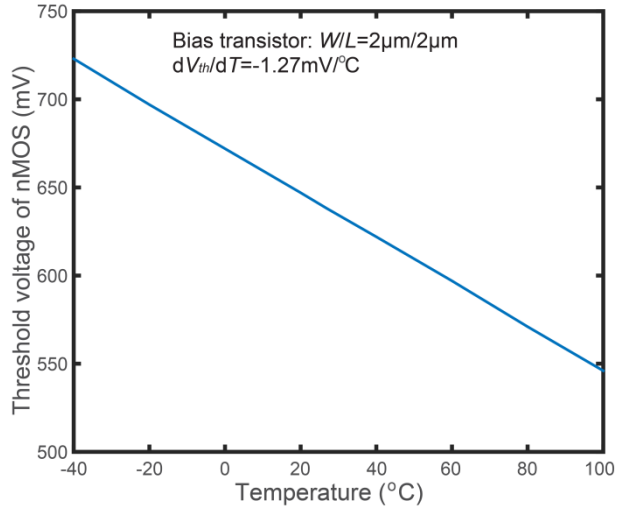


Figure 6-2. The SPICE simulation result of the threshold voltage as a function of temperature.

When the bias transistor is working in saturation, as shown in Eq. (3-2), the pixel's bias current I_s is related to the values of the carrier mobility μ and V_{th}. Both parameters have a temperature dependency. As a result, the variation of the current with the temperature is also complicated. In the pixel circuit, a small value for the bias current is chosen considering the power consumption and output swing. In this situation, the decrease of V_{th} with temperature is more influential than the decrease in mobility with temperature [6.7]. So the current increases with a rising temperature.

Figure 6-3 plots the bias current I_s as a function of the temperature while the bias transistor's size is 2μm/2μm.

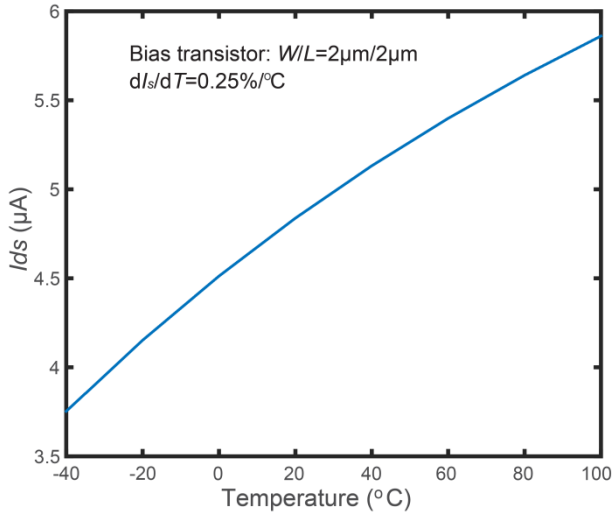


Figure 6-3. The simulation result of the bias current as a function of temperature.

As shown in Figure 6-3, the bias current has a nonlinear relationship with the variation of the temperature. The temperature dependence of bias current I_s can be simplified as Eq. (6-6), where $I_s(T_0)$ is the current value at room temperature while the temperature coefficient T_{CI} is around 0.25 %/°C based on the SPICE simulation.

$$I_s(T) = I_s(T_0)(1 + T_{CI}(T - T_0)) \tag{6-6}$$

In a conventional 4T pixel, the voltage gain of the SF, G_{SF}, varies with the pixel output voltage V_{PIX} shown in Eq. (3-5), which leads to a pixel related nonlinear error. More important, G_{SF} is temperature-dependent due to the temperature effects on carrier mobility μ, voltage threshold V_{th} and bias current I_s.

To simplify the analysis, Eq. (3-5) is replaced by a linear function shown in Eq. (6-7), where $G_{SF}(T_0)$ is the pixel's gain at room temperature and the extracted temperature coefficient T_{CGSF} is -0.029 %/°C based on the SPICE simulation.

$$G_{SF}(T) = G_{SF}(T_0)(1 + T_{CGSF}(T - T_0)) \tag{6-7}$$

On the contrary, the gain of the voltage buffer in pixel V1 G_{OPA} does not vary with V_{PIX}, which is only related to the open loop gain of the amplifier A_{OPA}, modeled in Eq. (4-1).

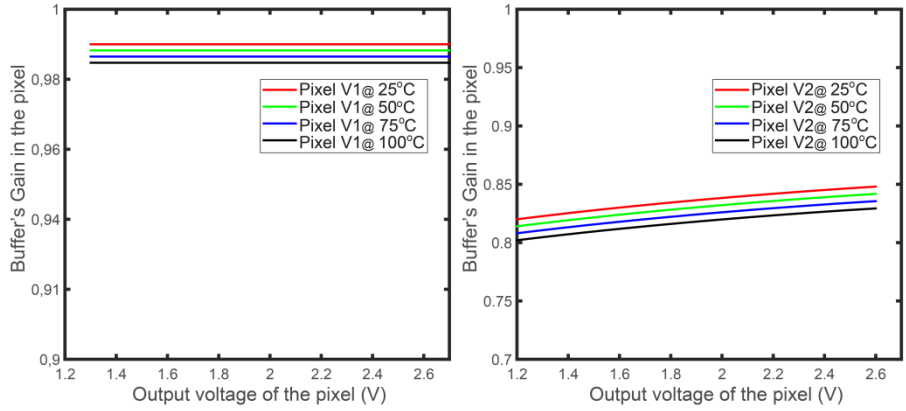
Similarly, the voltage gain of pixel V1 proposed in Chapter 4 decreases with a rise in temperature due to the temperature dependency of the carrier mobility and

bias current. It can be also simplified as Eq. (6-8), where $G_{OPA}(T_0)$ is the pixel's gain at room temperature, and T_{CGOPA} is the extracted temperature coefficient.

$$G_{OPA}(T) = G_{OPA}(T_0)(1 + T_{CGOPA}(T - T_0)) \tag{6-8}$$

In this chapter, a temperature range from 25 °C to 100 °C is chosen due to the temperature range of the oven used in the measurement. The gain deviation between the modeled results by Eq. (6-7), (6-8) and the SPICE simulation results over the whole temperature range, is less than 4 % for both pixel structures.

For pixel V1, T_{CGOPA} is -0.0075 %/°C which is smaller than T_{CGSF} in the 4T pixel. The modeling results of the voltage buffer's gain in pixel V1 and V2 are shown in Figure 6-4. Pixel V1 attains a constant gain regardless of the variation of the pixel's output voltage. The output voltage of pixel V2 is lower than pixel V1 due to the SF's threshold voltage, while the power supply of the RST transistor V_{DD_RST} is set as 2.7 V. Furthermore, the gain variation of pixel V1 at different temperatures is also smaller than the 4T pixel V2.



(a) (b)

Figure 6-4. V_{PIX} vs. Buffer's gain at different temperatures.(a) Pixel V1; (b) Pixel V2.

Subsequently, the temperature effects on the integration capacitor C_{FD} are discussed. The 4T pixel V2 is used to illustrate the temperature effect. As introduced in Chapter 3, the integration capacitor C_{FD} shown in Figure 3-4 consists of several types of capacitances from different transistors [6.9]-[6.10].

From the analysis presented in Section 3.2, C_{FD} consists of linear and nonlinear parts; the nonlinear parts vary with V_{PIX}. More important, C_{FD} has a strong temperature coefficient due to the temperature dependency on G_{SF}, φ_F, V_{th} and other parameters. To simplify the analysis, the linear polynomial functions are used to describe the temperature dependency of each component in C_{FD} shown in Table 6-1.

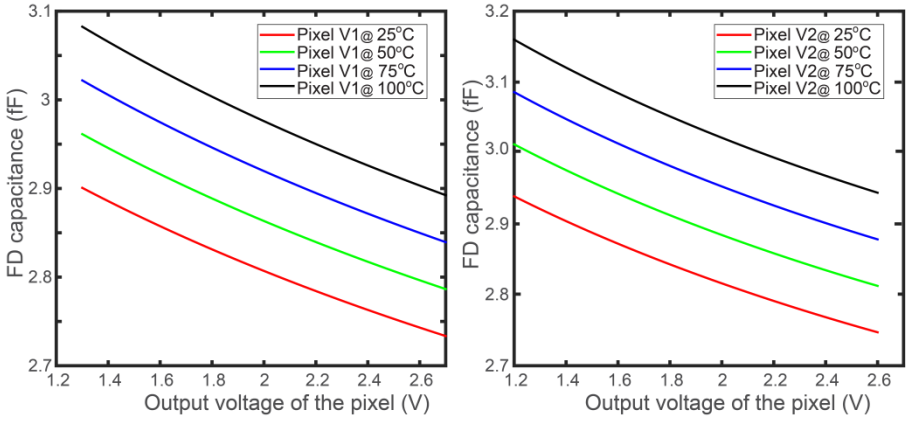
Table 6-1. Temperature dependency on C_{FD}

Components of C_{FD}	Equation	Temperature dependency	Explanation
Metal capacitance	C_M	C_M	Temperature independent
Gate capacitance	$C_{TX\_OV} = Xd_{TX} \cdot W_{TX} \cdot C_{ox}$	$C_{TX\_OV}(T) = C_{TX\_OV}(T_0)(1 + T_{CCOV}(T - T_0))$	T_{CCOV}, $C_{TX\_OV}(T_0)$ are the T_C and room temperature capacitance of the overlap capacitor of the TX
	$C_{RST\_OV} = Xd_{RST} \cdot W_{RST} \cdot C_{ox}$	$C_{RST\_OV}(T) = C_{RST\_OV}(T_0)(1 + T_{CCOV}(T - T_0))$	$C_{RST\_OV}(T_0)$ is room temperature capacitance of the overlap capacitor of the RST
	$C_{SF\_OV} = Xd_{SF} \cdot W_{SF} \cdot C_{ox} \cdot (2 - G_{SF})$	$C_{SF\_OV}(T) = C_{SF\_OV}(T_0)(1 + T_{CCOVSF}(T - T_0))$	T_{CCOVSF}, $C_{SF\_OV}(T_0)$ are the T_C and room temperature capacitance of the overlap capacitor of the SF
	$C_{SF\_GB} = 2 / 3 \cdot W_{SF} \cdot L_{SF} \cdot C_{ox} \cdot (1 - G_{SF})$	$C_{SF\_GB}(T) = C_{SF\_GB}(T_0)(1 + T_{CCGBSF}(T - T_0))$	T_{CCGBSF}, $C_{TX\_SA}(T_0)$ are the T_C and room temperature capacitance of the gate capacitor of the SF
p-n junction capacitance	$C_{FD\_J} = \frac{C_{J0}}{(1+V_{PD}/\varphi_B)^{M_J}} A_{FD}$	$C_{FD\_J}(T) = C_{FD\_J}(T_0)(1 + T_{CCJ}(T - T_0))$	T_{CCJ}, $C_{FD\_J}(T_0)$ are the T_C and room temperature capacitance of the vertical junction capacitor on the FD
	$C_{FD\_JSW} = \frac{C_{J0}}{(1+V_{PD}/\varphi_{BSW})^{M_{JSW}}} P_{FD}$	$C_{FD\_JSW}(T) = C_{FD\_JSW}(T_0)(1 + T_{CCJSW}(T - T_0))$	T_{CCJSW}, $C_{FD\_J\_SW}(T_0)$ are the T_C and room temperature capacitance of the lateral junction capacitor on the FD

In the simplified analytical model, the metal capacitance has a low temperature coefficient, which could be regarded as independent of the temperature and voltage variation. The SPICE simulation shows that C_{SF_GB} has a negative

temperature coefficient T_{CCGBSF}. The overlap capacitance usually has a small temperature coefficient T_{CCOV}, while the junction capacitances have a larger temperature coefficient, which is around 0.25 %/ºC, extracted from the measurement results of several groups of 4T pixels with different FD size. Having the largest capacitance value and temperature coefficient, the junction capacitance is dominant in the temperature variation of C_{FD}.

The modeling of C_{FD} in pixel V1 is similar to the 4T pixel. The modeling results of C_{FD} for both pixels are shown in Figure 6-5, where C_{FD} decreases with the output voltage of the pixel. The average values of the capacitance are chosen as the modeled value of the C_{FD} to calculate the final value of conversion gain. In both pixels, C_{FD} has a positive temperature coefficient.



(a) (b)

Figure 6-5. C_{FD} vs. V_{PIX} at different temperatures. (a) Pixel V1; (b) Pixel V2.

Dark current is the leakage current in the photodiode, which is mainly caused by thermal generation [6.11] and is detrimental to the imaging performance. The value of the dark current depends on many factors such as doping concentrations, band gap, but especially also on the temperature. The model of the dark current proposed in [6.11] is expressed as Eq. (6-9), where V_{PD} is the voltage across the diode and A_D is the size of the photodiode; D_N and D_P are the diffusivities of electrons and holes, while L_N, L_P are the diffusion lengths of electrons and holes, respectively [6.11]; N_A and N_D are the densities of the acceptor and donor in the technology we use [6.11].

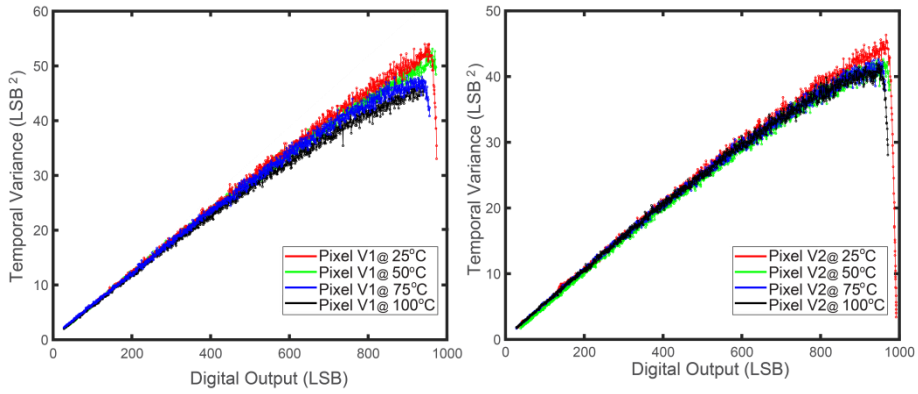
$$I_{dark} = I_S(e^{qV_{PD}/kT} - 1) = qA_D n_i^2 \left(\frac{D_P}{N_D L_P} + \frac{D_N}{N_A L_N}\right)(e^{qV_{PD}/kT} - 1) \tag{6-9}$$

The dark current modeling of the pixel is quite complicated, which is out of the scope in this thesis. The measured results of the pixels' dark current are included.

6.3 Measured Results

By adding the temperature model of the transistors and the capacitors in the CIS model proposed in Chapter 3, the modeling of CIS with its temperature characteristic is included.

Through the mean-variance plots, the corresponding pixel information, such as full-well capacity and conversion gain can be obtained. The mean-variance plots of pixel V1 and V2 at different temperatures are depicted in Figure 6-6, where it is clearly seen that the slope of the curves starts to decline with the increase of the temperature.



(a) (b)

Figure 6-6. Mean-variance plots at different temperatures of (a) pixel V1; (b) pixel V2.

In unity-gain configuration, pixel V1 realizes a larger conversion gain than the traditional 4T pixel, as shown in Figure 6-7, where the lines with star marks represent the modeled results and the lines with circle marks give the measured results over the temperature from 25 ^{o}C to 100 ^{o}C. When the temperature goes up, both pixels have a declined conversion gain mainly due to the increasing value of C_{FD} and the decreasing value of the voltage buffer's gain. As shown in Figure 6-7, the measured results of the conversion gain agree well with the modeled results.

In the prototype chip, the FD region determines the FWC value of the pixel. The voltage range of the ADC remains the same for all temperatures considered. The value of the FWC increases with temperature due to the decreasing CG. The modeling results demonstrate a good agreement with the measured results, which are shown in Figure 6-8. In [6.4], the authors also came to the same conclusion, which was explained from the standpoint of the increasing pinning voltage at a higher temperature.

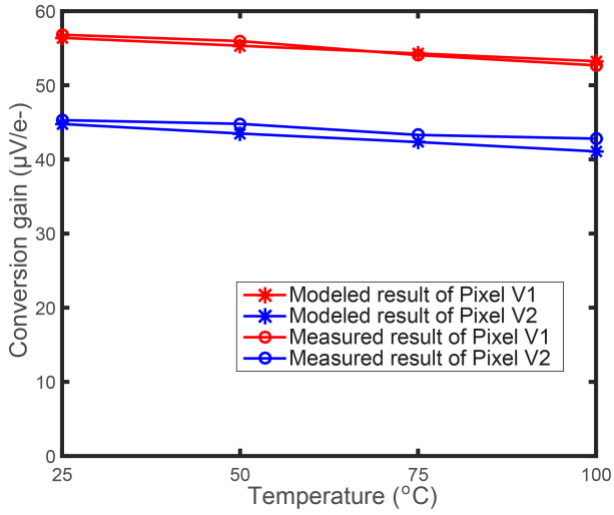


Figure 6-7. The conversion gain as a function of temperature.

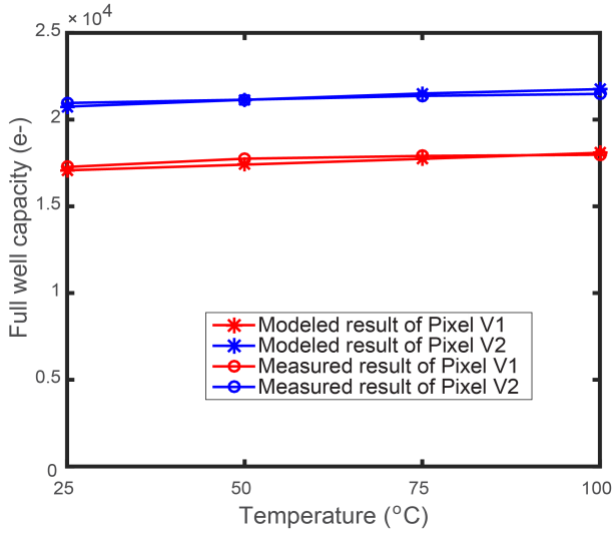


Figure 6-8. The FWC as a function of temperature.

Figure 6-9 shows the corresponding digital output of the pixel V1 in dark with a linear increasing integration time at different temperatures. The dark signal of pixel V1 rises exponentially with temperature. At 100 °C, the digital output of the pixel V1 is already saturated at a long exposure time.

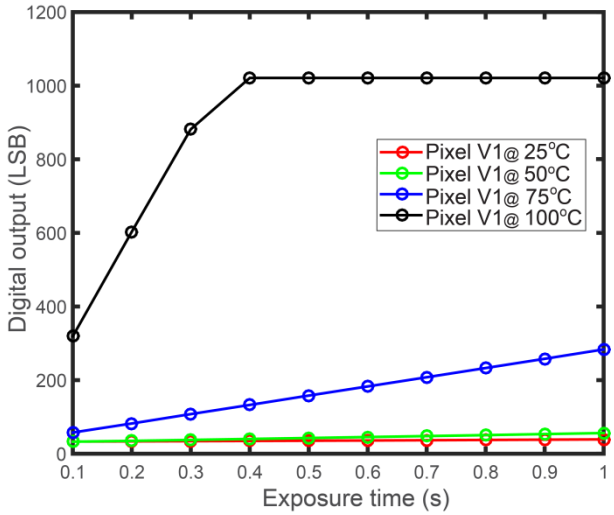


Figure 6-9. Digital output vs. Exposure time at different temperatures of pixel V1.

The dark current can be obtained by calculating the slope of the dark signal over the integration time. The measured dark current of the pixels is shown in Figure 6-10. The dark current of the pixels V1 and V2 rise exponentially with temperature. The doubling temperature is approximately 7~8 ºC, which is similar to the results observed in other publications [6.12], [6.13]. Therefore, a cooling system is commonly implemented to reduce dark current of the sensor.

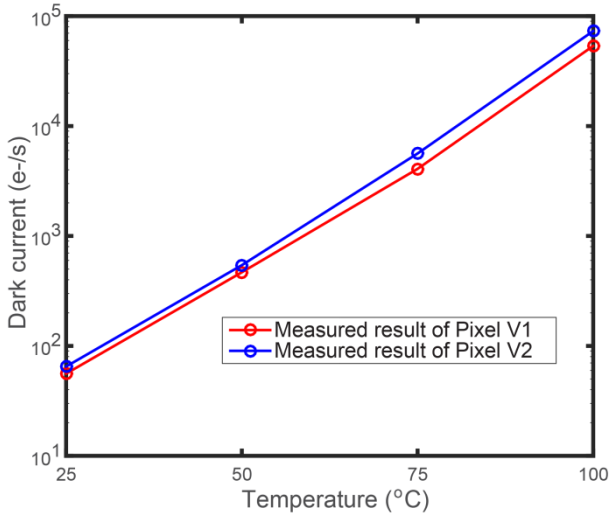


Figure 6-10. The dark current as a function of temperature.

With an increasing value of the C_{FD} at higher temperatures, especially the junction capacitance and thus the nonlinear part of C_{FD} increases, and this further

deteriorates the linearity performance of the pixel [6.10]. The nonlinearity performance of the pixels is shown in Figure 6-11, for both type of pixels the nonlinearity deteriorates with increasing temperature. In the measurement, the light intensity is fixed while the exposure time of the CIS increases evenly. After capturing the transfer curve of the image sensor from the injected photons to the final digital number, the deviation of the measured output curve from an ideal photon response can be attained which leads to a value of the nonlinearity. The nonlinearity measurement results at different temperatures share the same trend with that of the modeling results. Pixel V1 shows a superior linearity compared with the 4T pixel V2 for all temperatures. The measured results are obtained with a maximum exposure time of 0.5 ms, where the dark current has not destroyed CIS's linearity performance even at 100 ^{o}C.

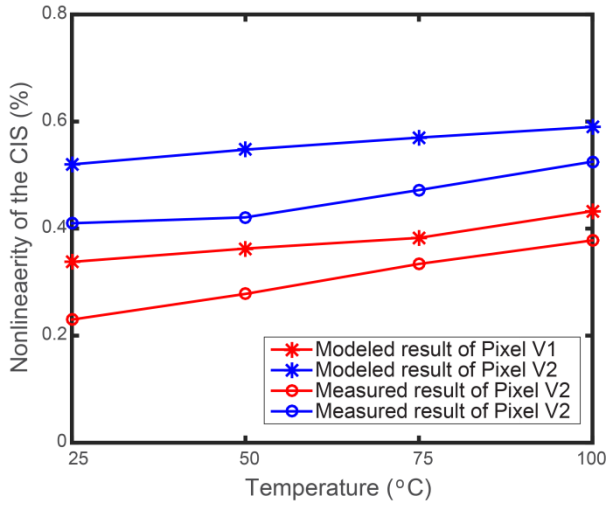


Figure 6-11. Nonlinearity of the pixels at different temperatures w/o calibration.

In Chapter 5, a digital calibration method is proposed to improve the linearity on system-level. In this chapter, the effectiveness of the proposed calibration method at different temperatures is presented.

Firstly, the transfer curve of the image sensor, from the incident photons to the final digital output at a temperature of 25 ^{o}C is captured. By calibrating the ramp signal of the ADC to compensate the nonlinearity of the system, as shown in Figure 6-12, both pixels achieve a nonlinearity of less than 0.06 % at 25 ^{o}C after calibration. The same calibrated ramp code is used to calibrate the CIS at all temperatures; this is indicated as a "uniform calibration". However, when the temperature rises, especially above 75 ^{o}C, the improvements are not as effective as the results at room temperature due to the fact that, the extracted information of the Capacitance-Voltage characteristics of the C_{FD} at 25 ^{o}C is different compared

to what will be extracted at a higher temperature.

Another group of measurements is carried out, where the corresponding transfer curve of the CIS at each specific temperature is used to calibrate the output of the image sensor at that specific temperature. This is called "separated calibration". In Figure 6-12, the measurement results plotted in star marks show that with this specific temperature-depending calibration code, the proposed digital calibration achieves excellent linearity results, even over the whole range of the temperatures.

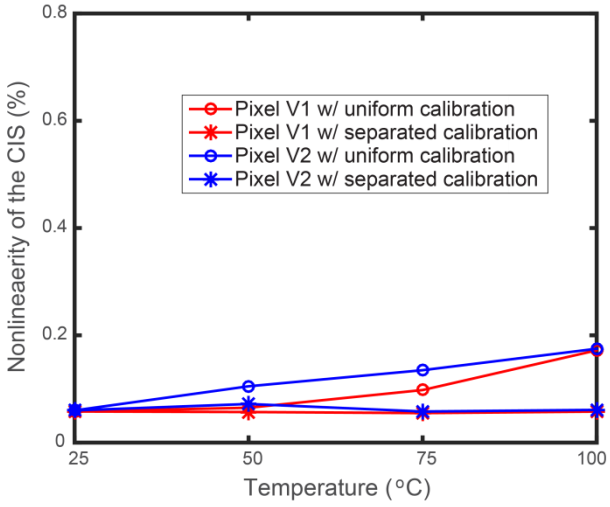


Figure 6-12. Nonlinearity of the pixels at different temperatures w/ calibration.

In a future design, a temperature sensor would be implemented on-chip to realize a fully automatic linearity calibration by choosing the corresponding calibration code according to the measured temperature result.

6.4 Conclusion

Based on an updated analytical CIS model including temperature dependency, we explore the pixels' behavior at different temperatures in this chapter. The measured results of a prototyped CIS agree well with the theoretical analysis. Furthermore, the digital linearity-calibration method proposed in Chapter 5 proves the validity of the linearity improvement while the temperature varies.

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Chapter 7 Pixel Optimizations and 3 Digitally Assisted Linearity-Calibration Methods

This chapter of the thesis is based on the publication :

F. Wang, A. J. P. Theuwissen, "Pixel optimizations and digital calibration methods of a CMOS image sensor aimed for high linearity," accepted by *IEEE transaction on Circuits and Systems.*

F. Wang, A. J. P. Theuwissen, "Two calibration methods to improve the linearity of a CMOS image sensor," in *Proc. Electronic Imaging*, San Francisco, USA, 2018.

In Chapter 4 and 5 respectively, pixel-level and system-level linearity optimization of a CMOS image sensor are introduced. However, these methods have their own deficiencies. The buffer pixel still suffers from the nonlinear errors caused by the nonlinear C_{FD}; and the calibration method needs to capture the transfer curve of the CIS in a constant light condition, which is sometimes hard to realize.

In this chapter, more linearity improvement techniques of the CIS are introduced. Based on an image sensor with an improved digital resolution presented in Section 7.2, several types of pixel designs including a novel buffered CTIA pixel are introduced in Section 7.3. According to the deficiency of the proposed calibration method in Chapter 5, two other types of calibration methods are developed in Section 7.4 to overcome its shortcoming. The measurement results of the proposed image sensor and conclusions are presented in Section 7.5 and 7.6.

7.1 Introduction

In Chapter 4, a novel buffer pixel which utilizing an in-pixel analog buffer efficiently improves the linearity to some extent at the cost of a lower fill factor and worse noise performance. The digital calibration method proposed in Chapter 5, drastically reduces the nonlinearities of all pixel structures, to a value of less than 0.06 %. However, a calibrated ramp signal of the image sensor needs to be first captured with a constant illumination condition. Sometimes, it is not convenient to capture the imager's transfer curve with a fixed illumination.

In this chapter, more linearity improvement techniques of the CIS are introduced. Several types of pixel structure aimed for linearity optimization are first explored. Similar to the buffer pixel structure proposed in Chapter 4, a type of 4T pixel using a pMOS source follower transistor with connected source and bulk, cancels the body factor of the source follower; thus this type of pixel attains a better linearity without employing more transistors. Furthermore, a pixel design based on a capacitive transimpedance amplifier is introduced, achieving an outstanding linearity result while maintaining a relatively high fill factor by sharing most transistors in a column.

Then based on the calibration method presented in Chapter 5 which we call as pixel mode (PM), two other calibration methods, voltage mode (VM) and current mode (CM) are proposed to improve the sensor's linearity without the needs for a constant illumination. Notably, current mode calibration can further suppress the nonlinearity caused by the integration capacitor C_{FD} on the floating diffusion node, which is remnant in voltage mode calibration.

The pixel optimizations and the digital calibration methods are experimentally verified with a prototype CIS fabricated in the same 0.18 μm commercial CMOS image sensor technology used in the other chapters.

7.2 Sensor Architecture

In this design, a prototype CMOS image sensor containing different pixel structures is presented. Figure 7-1 shows the overall architecture of the image sensor. The pixel array consists of 128 × 160 pixels with a pitch of 12 μm. The shared parts of the CTIA pixel circuits and the circuits of the calibration current source are placed between the pixel array and readout circuits. Different from the design presented in the previous chapters, the resolution of the ADC in the column-parallel analog chain is upgraded from 10-bit to 12-bit. The column amplifier still provides a programmable gain from 1 × to 8 × to suppress the read noise. An off-chip dual 14-bit DAC is employed to provide a ramp signal V_{RAMP1} for the ADCs as well as a periodic ramp signal V_{RAMP2} as the in-pixel reset

transistor's power supply (V_{DD_RST}) for voltage mode calibration. In the other modes, V_{DD_RST} is constant and provided by the onboard power supply.

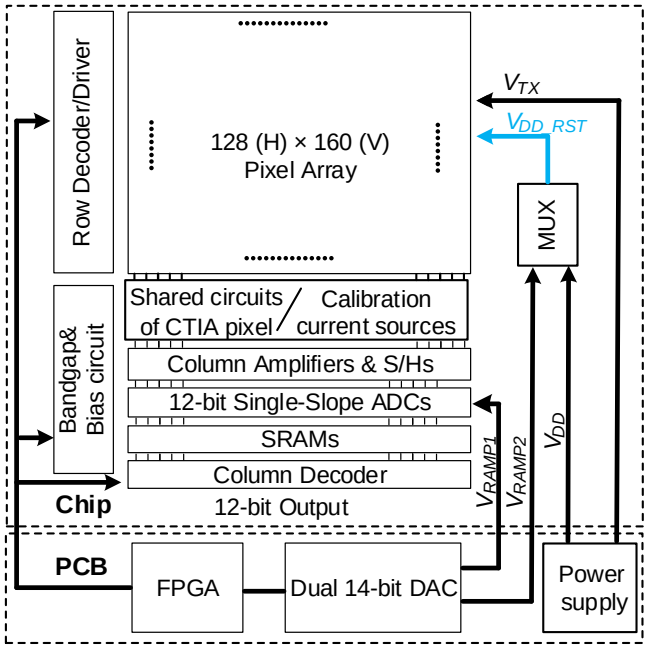


Figure 7-1. The proposed CIS system diagram.

As shown in Figure 7-2, the 14-bit current steering DAC converts the digital signals from the FPGA into two groups of differential current outputs. Similar to the ramp signal generator presented in Figure 5-2, the load resistors R_{RAMP1} and R_{RAMP2} convey the current outputs to two differential voltage outputs. Subsequently, the OPA converts the differential voltage to a single-ended ramp signal V_{RAMP1}. V_{RAMP2} is generated in the same way.

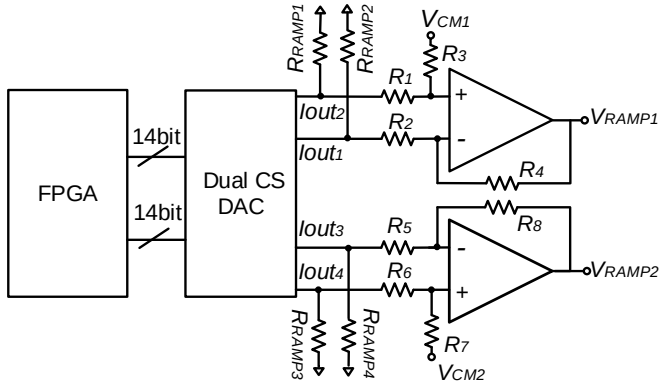


Figure 7-2. The schematic of ramp generator based in a dual current steering DAC.

7.3 Pixel Design

In Chapter 3, we have already reached a conclusion that the gain of the source follower and the nonlinear capacitance on the floating diffusion node C_{FD} introduce most of the nonlinearity to the pixel. To alleviate the nonlinear effects caused by the SF in the 4T pixel, a type of buffer pixel has been proposed in Chapter 4. The schematics of the 4T pixel and buffer pixel are shown in Figure 7-3. To better illustrate the gradual linearity improvement at pixel-level in this chapter, we use pixel V1 to represent the normal 4T pixel while pixel V2 acts as the buffer pixel. Pixel V2 uses a single-stage operational amplifier in unity gain configuration as an analog buffer to drive the loading circuits. In a closed loop configuration, the body effect is canceled, and the linearity is improved at the cost of a smaller fill factor and a larger noise.

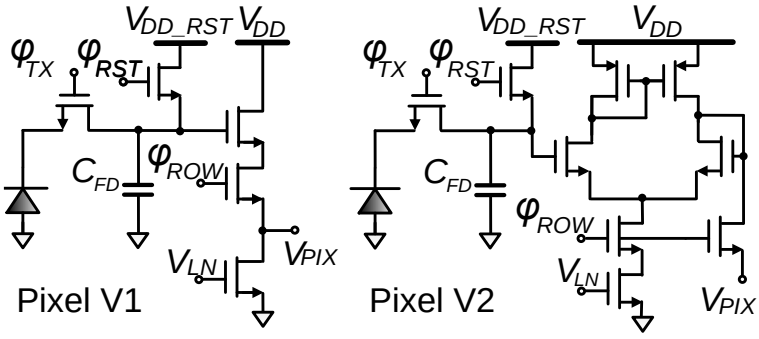


Figure 7-3. The schematic of the pixel V1 and V2.

In this chapter, more pixel structures targeting a better linearity are presented while pixels V1 and V2 are still included to make a comparison. First, two pixel structures V3 and V4 using a pMOS SF transistor are introduced, as shown in Figure 7-4. In pixel V3, the bulks of the SF and row select transistors are connected to the power supply, so the body effect of the pMOS SF is still present. In pixel V4, the bulk of the pMOS SF is tied to the source in a separated n-well, which cancels the body-effect of the pMOS SF. Without using a complicated analog buffer design, pixel V4 realizes a unity gain with one transistor. Thus this type of pixel could realize a higher conversion gain without a noise penalty; However, the row select and source follower transistors of the pixel V4 use separated n-wells; the minimal distance between different n-wells is constrained by the design rules, which limits the fill factor. Pixel V3 has a fill factor of 60 % while that of pixel V4 is 48 %. Compared with the traditional 4T pixel employing the nMOS type SF, the pixels V3 and V4 using pMOS type SF achieve a lower

noise especially its flicker noise. As show in Figure 7-4, the bias current of the pixels is variable by changing the bias voltage V_{LP}.

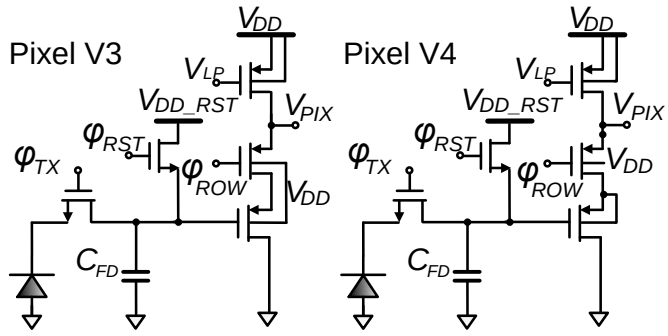


Figure 7-4. The schematic of the pixel V3 and V4.

Although pixels V2 and V4 can mitigate the nonlinearity caused by the SF and thus achieve better linearity result, the nonlinear C_{FD} still contributes to the nonlinear behavior of the pixel. Further solutions can be used to reduce the pixel's nonlinear errors due to the inconstant capacitance.

A new pixel based on a CTIA structure is employed to further reduce the nonlinearity caused by the C_{FD}. Figure 7-5 shows the schematic of the CTIA pixel V5, which consists of an operational amplifier, a feedback capacitor, a reset switch and an analog buffer. A single-ended input telescopic cascade amplifier structure is adopted for the OPA to achieve a high gain on a small area due to the limited pixel size [7.1]. Compared with the differential-input amplifier structure, this single-ended structure has the advantage of a higher fill factor and low noise. The OPA has a voltage gain of 82dB and consumes 1μA. The feedback capacitor in the pixel is implemented by a MIM capacitor C_{INT} (about 4fF), which has an ultra-low voltage coefficient. With the amplifier achieving a high voltage gain, the closed loop forces the integration of the photocurrent on C_{INT}. A highly linear output of the CTIA pixel is thus obtained. The cascode output stage of the amplifier has a higher output impedance than the source follower in the traditional 4T pixel. Therefore, an analog buffer is added after the trans-impedance amplifier. The output of the pixel can be written as Eq. (7-1), where I_{PD} is the photocurrent and A_{OPA} is the open-loop gain of the analog buffer.

$$V_{PIX} = -\frac{1}{C_{INT}} \int I_{PD} dt \cdot \frac{A_{OPA}}{1 + A_{OPA}} \tag{7-1}$$

As shown in Figure 7-5, the whole pixel consists of seven nMOS transistors, while the pMOS and other nMOS transistors inside the dotted line are shared by all pixels in a column; this leads to a fill factor of 36 % with a pixel size of 12 μm

× 10 µm. The bias voltages V_{B1}~V_{B3}, V_{LN} are generated outside the pixel. The reset voltage of the pixel is decided by the gate-source voltage of the amplifier's input transistor, which is sensitive to the process variation. However, the following CDS circuit can reduce this type of noise [7.1].

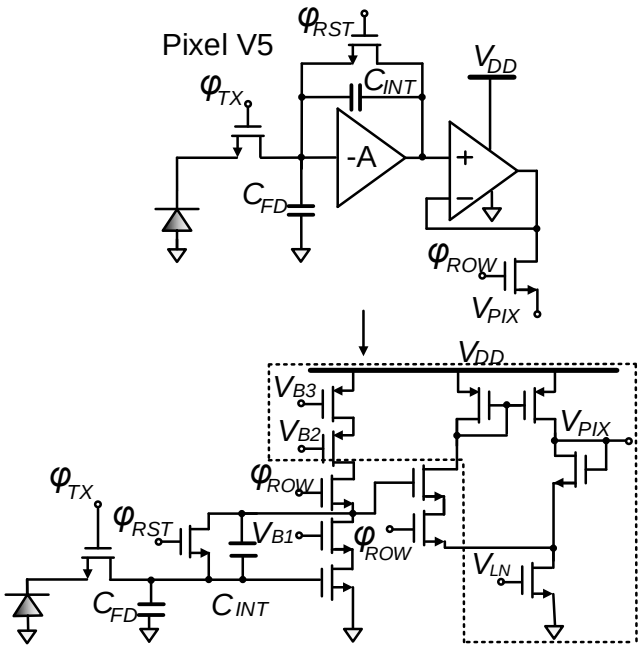


Figure 7-5. The schematic of the pixel V5.

To illustrate and verify the current mode calibration method proposed in the following Section 7.4, two further pixels V6 and V7 are specially adapted in this design based on the 4T pixel structures V1 and V3. These pixels are shown in Figure 7-6.

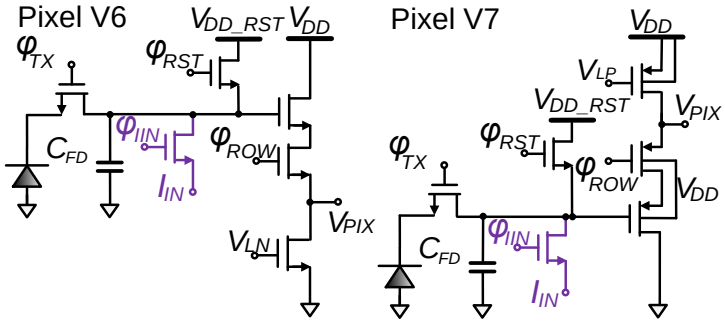


Figure 7-6. The schematic of the pixel V6 and V7.

Compared with the 4T pixels V1 and V3, an extra transistor is added on the FD node of the pixel V6 and V7. The source of that extra transistor is connected to a

calibration current sink circuit and the gate of the transistor is control by a signal $\varphi_{IIN.}$ When the signal φ_{IIN} is turned on, the FD discharges into the out-pixel current sink, where an ultra-low current I_{IN} imitates the photocurrent converted by the photodiode. I_{IN} can be used to capture the electron-voltage transfer curve of the image sensor and further to calibrate the image sensor.

7.4 Calibration Methods

In the proposed pixel structures especially the CTIA, pixel-level linearity optimizations strongly improve the linearity performance of the pixel. However, the readout circuit still contributes to the nonlinear errors of the image sensor.

The pixel mode calibration is first proposed in Chapter 5 to calibrate the nonlinear errors of the image sensor. In the new prototype chip, the resolution of the ADC has been upgraded from 10-bit to 12-bit to achieve a better calibration effectiveness. Furthermore, an additional two calibration methods are explored and proposed to further overcome the first method's deficiency.

The 4T pixel V3 is employed to illustrate the operating principles of the first calibration method. As shown in Figure 7-7, V_{DD_RST} is constant, the photodiode is first reset by pulsing φ_{TX} and φ_{RST}, then the pixel is read out conventionally; the signal φ_{RST} is activated to enable the readout of the V_{RST} signal; at the same time, the control signals φ_{AMP_RST} and φ_{ADC_RST} are sequentially activated, the column amplifier and ADC realize auto-zeros. Afterward, the signal φ_{TX} is activated, the accumulated electrons of the photodiode during the integration phase will be transferred to the FD. The differential value of the pixel's reset and signal value is sampled on the capacitor C_{SH} by the digital signal φ_{SH} and further digitalized by the column ADC.

In Chapter 5, we have already reached a conclusion that the resolution and linearity performance of the DAC decides the effectiveness of the calibration method. The resolution of the DAC is upgraded to 14-bit since the resolution of the ADC employed in this design is 12-bit.

During the pixel mode calibration, the exposure time is increased from a $1 \times T_{EXP}$ to $4096 \times T_{EXP}$ with a fixed light intensity. The digital input code of the DAC M_{IN} increases from 0 to 16383(2^{14}-1) and generates a linear ramp signal V_{RAMP1}. The digital output of the ADC is captured and stored in the SRAM for each exposure time. The mapping process removes the offset and gain errors from the data. The data is then interpolated from 12-bit to 14-bit to match the resolution of the DAC. The final data sequence $M_{IN\_C\_PM}$ is sent to the input of the DAC to generate a calibrated ramp signal $V_{RAMP1\_C\_PM}$, containing the information of the nonlinearities of the pixel and the readout circuit. By applying the nonlinear ramp signal, the original nonlinearities of the image sensor are canceled out.

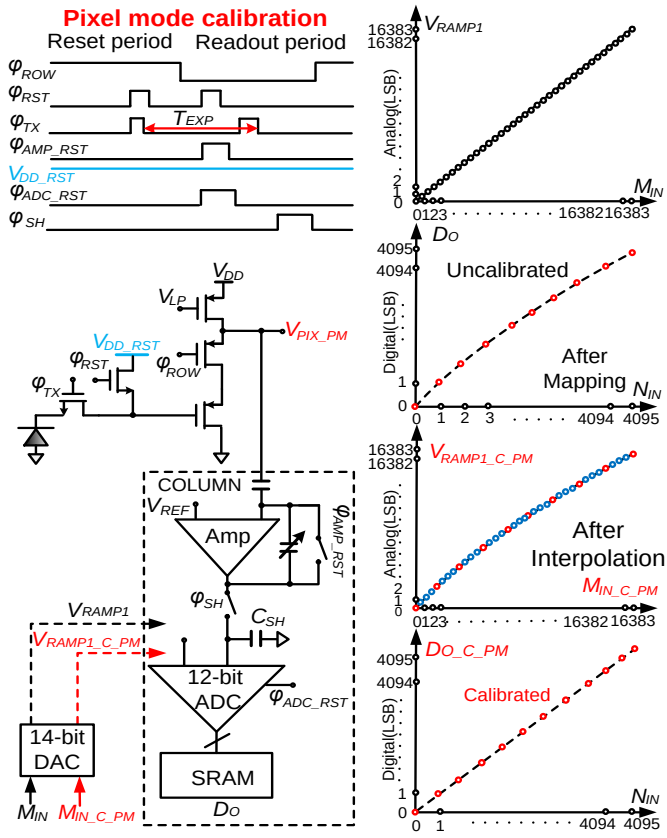


Figure 7-7. Pixel mode calibration operation and its timing diagram.

Pixel mode calibration can calibrate the nonlinearity caused by the readout circuitry as well as the pixel circuit; thus it drastically improves the linearity performance of the image sensor without extra penalty on power consumption, chip size or speed. However, the transfer function of the image sensor needs to be first achieved to change the input of the ADC and further to compensate the nonlinearity of the sensor. All the data should be captured with a constant illumination.

In this chapter, another two calibration methods are proposed to eliminate the dependency on the light condition, which are voltage mode and current mode calibration, respectively.

Figure 7-8 introduces voltage calibration method, where the TX transistor remains off and the photodiode is not used. The transfer curve of the image sensor is measured in a dark environment. Instead of increasing the exposure time, a decremental periodic ramp signal V_{RAMP2} is applied to the drain of the RST transistor. V_{RAMP2} generated by the DAC imitates the voltage on the floating diffusion node in pixel mode. V_{RAMP2} has two values, representing the two

different phases of a conventional pixel operation. A monotonic increasing output signal is achieved by means of the subsequent CDS circuit. Digitized by the on-chip ADC, the final digital output contains the nonlinear information of the SF and readout circuit. Similarly, based on the voltage transfer function between the input ramp signal V_{RAMP2} and the final digital output, the voltage mode calibration records the nonlinear information of the SF and readout circuitry. After mapping and interpolation, the incremental sequence $M_{IN\_C\_VM}$ is converted by the DAC into a new ramp signal $V_{RAMP1\_C\_VM}$, which will be used to compensate the original nonlinearities of the SF and readout circuit.

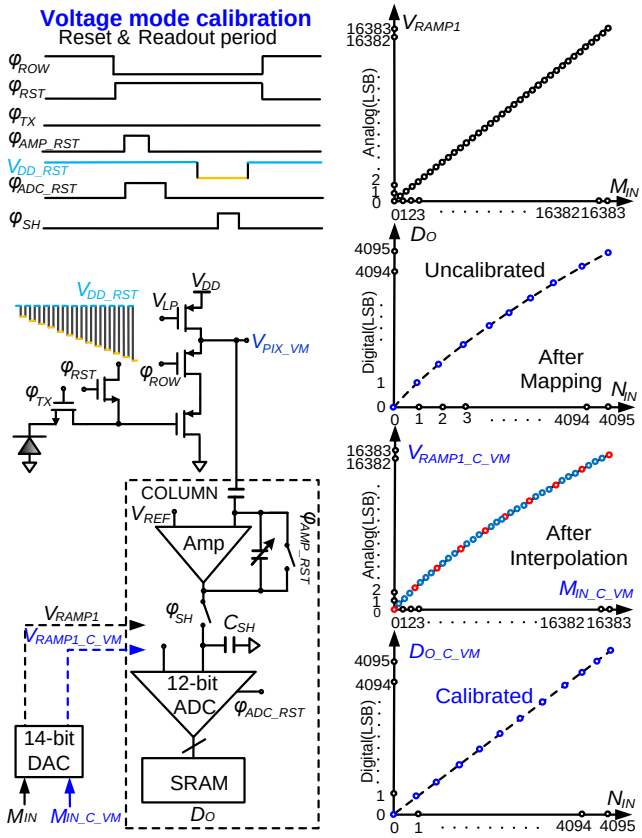


Figure 7-8. Voltage mode calibration operation and its timing diagram.

Compared with the PM calibration method, the power consumption and size of the system will increase with the VM method since the second DAC is needed to generate the periodic ramp signal V_{RAMP2} for the pixel. Furthermore, the voltage mode calibration is unable to obtain the information of the photodiode and the Capacitance-Voltage characteristics of the C_{FD}; as such, the nonlinearity caused by C_{FD} cannot be calibrated and the improvement is less effective when compared

to the PM calibration. The third type of calibration method: current mode calibration is thus proposed. The process of the CM calibration is illustrated with pixel V7, where the extra calibration transistor is used to convey the calibration current, as shown in Figure 7-9.

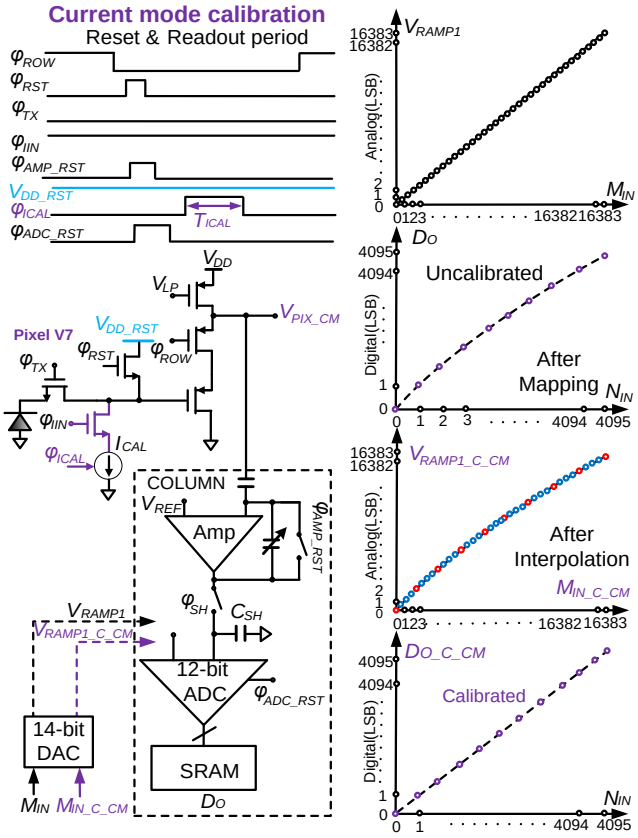


Figure 7-9. Current mode calibration operation and its timing diagram.

During the CM calibration, the photodiode is also disabled. The added transistor avoids the influence on the other group of pixels with different pixel structure in the same column. Signal φ_{ICAL} controls the operation time T_{ICAL} of the calibration current. The calibration current is maintained constant while the period of T_{ICAL} is changed incrementally. The output voltage of the pixel is proportional to the period of T_{ICAL}. If the nonlinearity caused by the transformation of photons to electrons is negligible, this method should calibrate the nonlinearity caused by the pixel and readout circuit. The basic operation of the CM is the same as the operation in pixel mode. By increasing the operation time of φ_{ICAL}, the transfer curve between the calibration charge and the final digital output can be obtained. Like other calibration modes, the updated ramp signal is employed to calibrate the

nonlinearity of the image sensor.

CM calibration can improve the calibration effect compared with VM calibration. The most prominent challenge of the current mode calibration is the design of a small calibration current source. The current of the photodiode is usually in the range of fA~pA, depending on the intensity and wavelength of the light source [7.3]-[7.4]. It is difficult to design such a small current source to imitate the photocurrent generated by the photodiode. In this design, all 64 pixels in one column share one generated calibration current. There are two types of structures to realize a stable current reference. The first type of current reference is based on a β multiplier [7.5]-[7.6], while another type employs a reference voltage and a resistor [7.7]-[7.8].

In this test chip, a reference current generated by a conventional voltage-to-current converter is mirrored to feed the FDs in the pixels shown in Figure 7-10. A folded cascode OPA is used in the voltage-to-current circuit. A negative feedback loop forces the current flow through the nMOS transistor which is equivalent to the input voltage V_{REF} divided by the resistor R_{IN}. V_{REF} is the output voltage of a programmable bandgap circuit. The current through the resistor R_{IN} is mirrored to generate 32 calibration currents. To achieve a sub-nA current, the resistor must be in the order of GΩ, which would cover a large chip area. In [7.9], the resistor is realized by a switched capacitor. In this thesis, an off-chip resistor R_{IN} is selected to save chip area and to facilitate the adjustment of the current. The reference current is adjustable by changing the voltage value of V_{REF} or the resistor value of R_{IN}.

The absolute value of the calibration current is not so critical as far as the calibration current is stable. By lengthening the operation time of T_{ICAL}, a decremental output of the pixel can be attained. The value of the R_{IN} follows Eq. (7-2), where I_{ICAL} is the calibration current; T_{ICAL_MAX} is the maximum operating time of calibration current; N_{ROW} is the number of the shared pixels in a column and ΔV_{FD} is the voltage range on the FD.

$$C_{FD}\Delta V_{FD} = I_{ICAL} \cdot T_{ICAL\_MAX} = \frac{V_{REF}}{R_{IN}} / N_{ROW} \cdot T_{ICAL\_MAX} \qquad (7\text{-}2)$$

The switch leakage current [7.10] can be detrimental to the calibration scheme. Dummy switches, driven by φ_{ICALB} which being the inverted control signal of φ_{ICAL}, are added to the circuit to reduce the charge injection and clock feedthrough. Based on simulation, the dummy switches can reduce the corresponding errors from 2.9 mV to 0.51 mV.

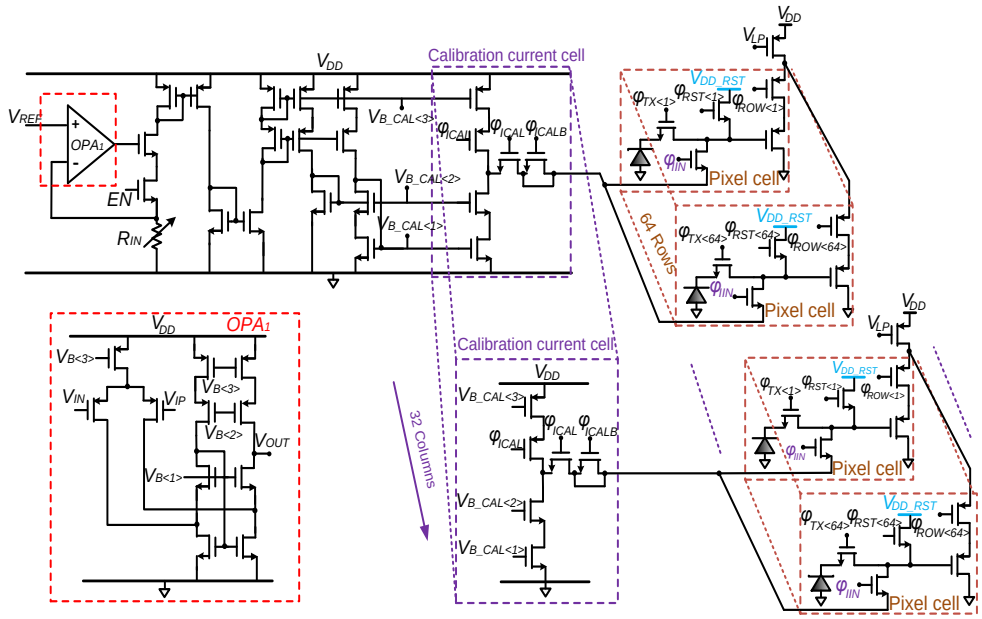


Figure 7-10. Calibration current generator.

7.5 Measured Results

The proposed CMOS image sensor has been fabricated in the same 0.18-µm CIS process technology used in other chapters. Figure 7-11 shows the micrograph of the fabricated chip. The chip size is 3.1 mm × 5.0 mm while the core area of the pixel array is 1.54 mm × 1.60 mm. An Altera Cyclone FPGA is used to provide the digital control signals and to capture the output data of the image sensor.

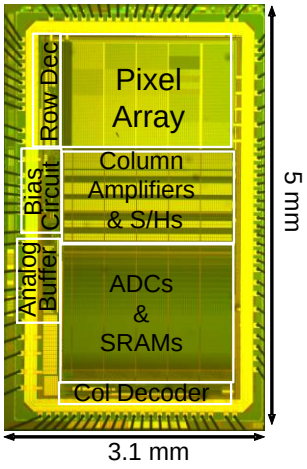


Figure 7-11. Chip microphotograph.

The nonlinearity of the column ADC is an important nonlinear error source of the readout circuitry. There are several methods to measure the nonlinearity of the ADC [7.11]-[7.13]. The histogram test method is the most popular one. By applying a ramp voltage signal generated by a higher resolution DAC or a low-frequency sinusoidal wave to the input of the ADC, the static performance of the ADC can be characterized. In this design and in accordance with the calibration method that is adopted, a linear voltage ramp generated by the same DAC is used to measure the nonlinearity of the column ADC. The measured nonlinearity results contain the nonlinearity of the ADC as well as the DAC. In this design, the employed DAC device (DA5672) has an excellent linearity performance (DNL<0.7 LSB and INL <1.1 LSB). The clock frequency of the 14-bit DAC is 100MHz while that of the 12-bit ADC is 25MHz.

For a typical column ADC, the DNL errors are -0.36/+0.37 LSB and the INL errors are -0.88/+1.97 LSB, which is shown in Figure 7-12, corresponding to a nonlinearity of 0.034 %.

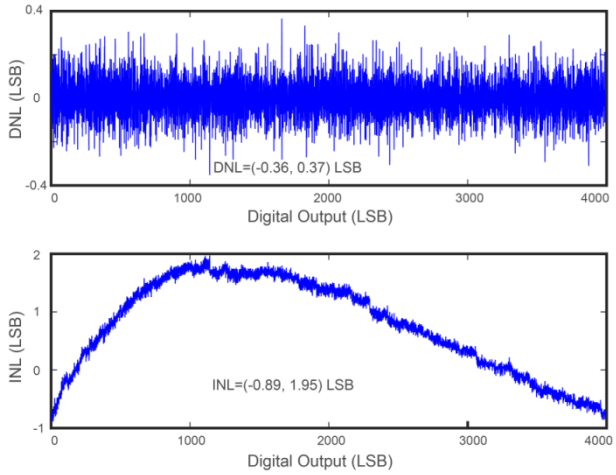


Figure 7-12. Measured nonlinearity performance of one channel SS-ADC.

The nonlinearity performance of all column ADCs is plotted in Figure 7-13, all ADCs have a nonlinearity of less than 0.051 %.

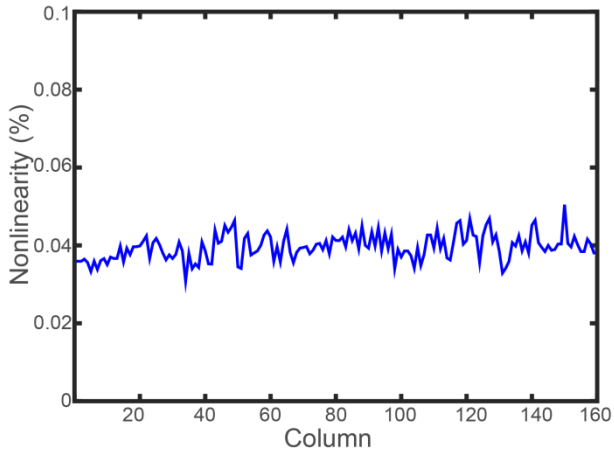


Figure 7-13. Measured nonlinearity performance of SS-ADC array.

The CTIA pixel is the most important pixel structure proposed in this chapter. The green signal in Figure 7-14 shows the measured output signal of the CTIA pixel monitored by an oscilloscope, while the yellow signal represents the reset signal φ_{RST}. By enabling the signal φ_{RST}, the FD node is first reset to a voltage decided by the threshold voltage of the input transistor of the transimpedance amplifier, which is around 0.8V. When the reset switch opens, the charges generated by the photodiode will be integrated on the integration capacitor C_{INT}. As shown in Figure 7-14, the CTIA pixel has a large linear output swing from 0.8 V~3 V.

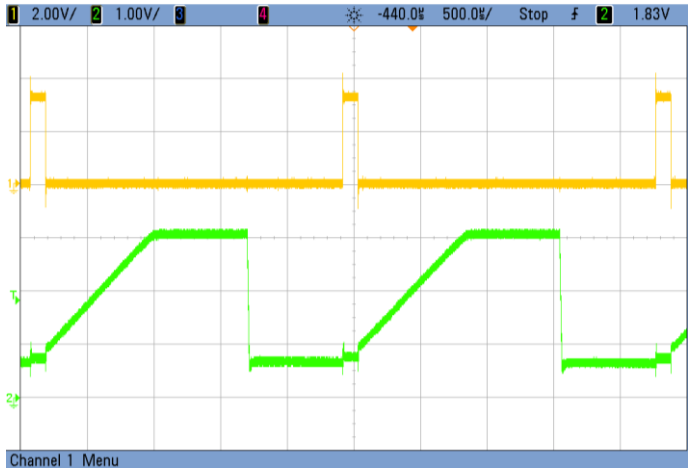


Figure 7-14. The measure output waveform of CTIA pixel.

In the linearity measurement, the exposure time increases from 0.1 μs to 409.6 μs evenly. All linearity curves are measured with 8×30 pixels and averaged over

200 frames captured while the gain of the column amplifier is set to unity. In the measurement, for the pixel V3, V4 and V7 where pMOS transistors are used as the SF, V_{DD_RST} is set as 2 V. For the other pixel structures, the value of V_{DD_RST} is 2.8V. The high voltage of the transfer transistor in the pixel V_{TXH} affects the pixel's characteristics, including the dark current and FPN [7.14]. The value of V_{TXH} is separately set according to each pixel structures.

Table 7-1 shows the nonlinearity results for all type of pixel structures. The other key characteristics of the image sensor, such as fill factor, noise and dark current measured at room temperature are also given in Table 7-1.

Table 7-1. The characteristics of the pixels

Pixel	Fill factor (%)	GC (μV/e-)	FWC (e-)	Noise (e-)	Dark current (e-)	DR (%)	PRNU (%)	Nonlinearity w/o calibration (%)
V1	46.4	54	22070	3.7	26	75.5	0.26	0.41
V2	46.4	60	21000	4.5	19.7	73.4	0.55	0.24
V3	60	40	23100	3.6	60	76.0	0.76	0.68
V4	48	70	13000	2.9	36	73.0	0.89	0.35
V5	36.3	40	30610	16.3	453	65.5	0.99	0.095
V6	45	43.2	24000	4.8	32	73.9	0.30	0.45
V7	42	50	14460	2.8	58	74.2	0.80	0.75

Without employing any calibration method, the 4T pixel V1 has a nonlinearity of 0.41 % while pixel V2 reduces the nonlinearity of the SF, which achieves a nonlinearity of 0.24 %. Furthermore, pixel V2 realizes a larger conversion gain than the 4T pixel V1 by employing the unity gain analog buffer. To fairly compare the linearity performance, pixels V1 and V2 use the same photodiode design, thus achieving the same fill factor.

Pixels V3 and V4 use the pMOS SF, whereby V4 employs the separated n-well to optimize the linearity. Pixel V3 has a nonlinearity of 0.68 % while pixel V4 improves the nonlinearity to 0.35 % by canceling the body effect of the pMOS SF. Pixel V4 also achieves a larger conversion gain and better noise in the electron domain. However, the distance between the different n-wells leads to a smaller fill factor in pixel V4.

The CTIA pixel V5 further reduces the nonlinearity caused by the nonlinear C_{FD}; it achieves the best linearity result among all types of pixels, of less than 0.1 % before calibration. Nevertheless, a small value of the MIM capacitance used in the CTIA will generate a large mismatch which leads to a larger photon response non-uniformity. According to the capacitance model provided by the process files, a standard deviation of the MIM capacitance (1.6μm × 1.7μm) is around 0.91 %.

The measured PRNU of CTIA pixel is 0.99 %. Furthermore, it has worse noise performance and fill factor. Most prominently, the noise contributed by the transimpedence amplifier is dominant in the CTIA pixel.

Pixels V6 and V7 have a nonlinearity of 0.45 % and 0.75 %, respectively.

As shown in Table 7-1, the linearity of the image sensor can be improved by the pixel-level linearity optimization. However, compared with the fundamental 4T pixel V1, pixels V2 and V5 sacrifice the other key characteristics of the image sensor including PRNU and noise. Pixels V3 and V4 employ a pMOS SF and have a smaller output swing than the traditional 4T pixel with nMOS SF. Furthermore, the readout circuit including the amplifier and ADC also contributes to nonlinear errors, which needs extra methods to improve the linearity.

The verification of the calibration methods starts with the pixel mode calibration. As shown in Figure 7-15, without adding any cost on the chip size or power, the pixel mode calibration method efficiently improves the nonlinearity of the image sensor. All pixel structures achieve a nonlinearity less than 0.05% after calibration.

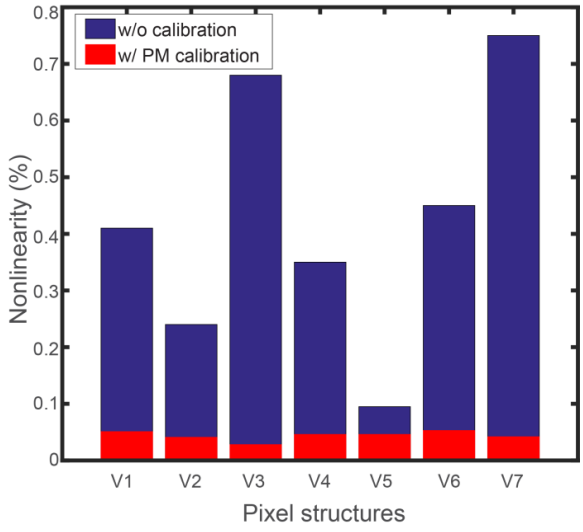
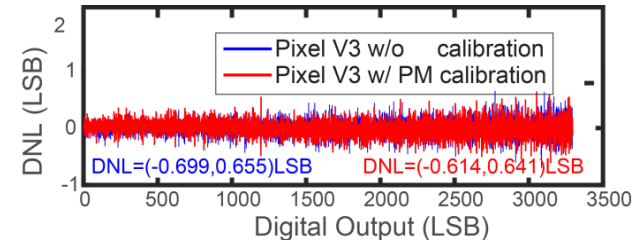
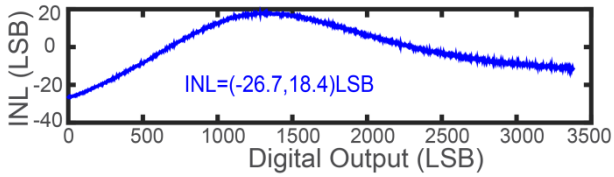


Figure 7-15. Measured nonlinearity performance of all pixel structures.

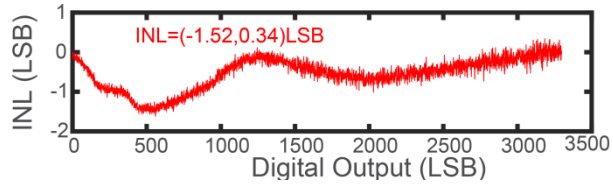
In particular, pixel V3 achieves an excellent nonlinearity with the assistance of the PM calibration, which is 0.028 %. Figure 7-16 (a) plots the DNL results of the image sensor with pixel V3 while Figure 7-16 (b) and (c) show the INL results. The blue lines show the measurement results without calibration, and the red lines represent those with pixel mode calibration. As shown in Figure7-16, the calibration method effectively improves the linearity result of the image sensor.



(a)



(b)



(c)

Figure 7-16. The nonlinearity of pixel V3 (a) DNL; (b) INL (w/o calibration); (c) INL (w/ PM calibration).

Figure 7-17 shows the corresponding histogram of the nonlinearity results in the pixel V3 array. Without calibration, the mean value of the nonlinearity in the pixel array V3 is 0.75 %. With the assistance of the PM calibration, the mean value is improved to 0.12 %, which proves its effectiveness for each pixel.

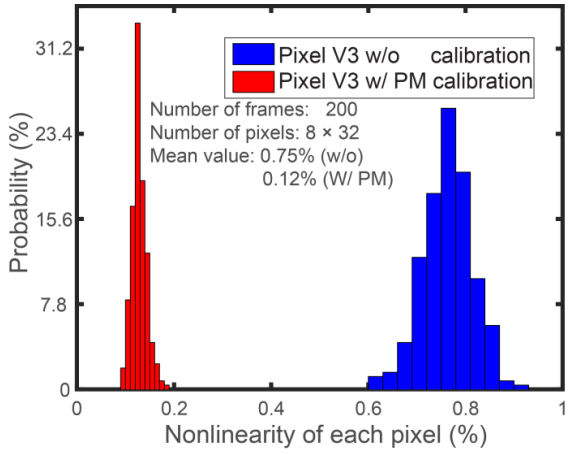


Figure 7-17. Histogram of the nonlinearity in Pixel V3 array.

Next pixels V1 and V3 are used to verify the voltage mode calibration method, which could cancel the nonlinearity of the SF transistor and the following readout circuitry. However, the missing information of the integration capacitance in the electron-voltage conversion of the pixel limits the effectiveness of the calibration method. The measured results show that the voltage mode calibration improves the linearity performance of the pixels V1 and V3. With voltage mode calibration, the nonlinearity of the pixels V1 and pixel V3 improve from 0.41 % to 0.30 % and 0.68 % to 0.43 %, respectively.

Figure 7-18 shows the linearity improvement for each pixel with the proposed VM calibration method in the array of pixel V3.

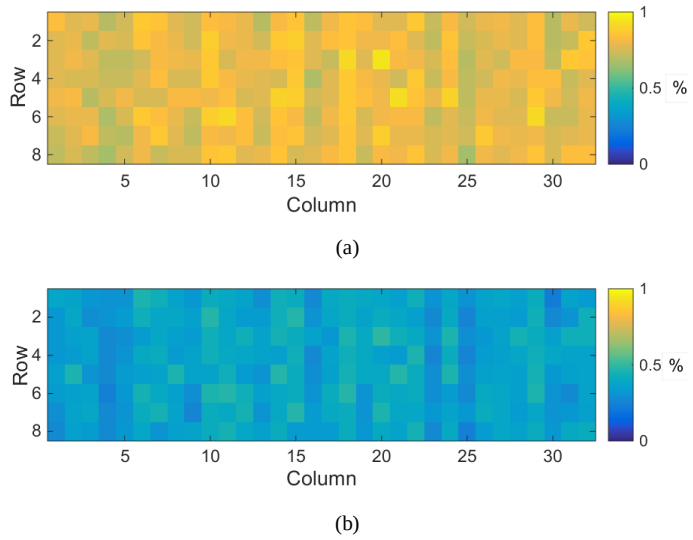


Figure 7-18. The nonlinearity of pixel V3 (for each pixel). (a) w/o calibration; (b) w/ VM calibration.

Finally, the validity of the third calibration method is verified through the pixels V6 and V7. Figure 7-19 plots the output voltage of the pixel V7 in current mode calibration, where the period of φ_{ICAL} increases from $1 \times T_{ICAL\_unit}$ to $20 \times T_{ICAL\_unit}$ evenly in steps of 50 µs, and the signal value of the pixel V_{SIG} decreases from 2.7 V to 1.8 V.

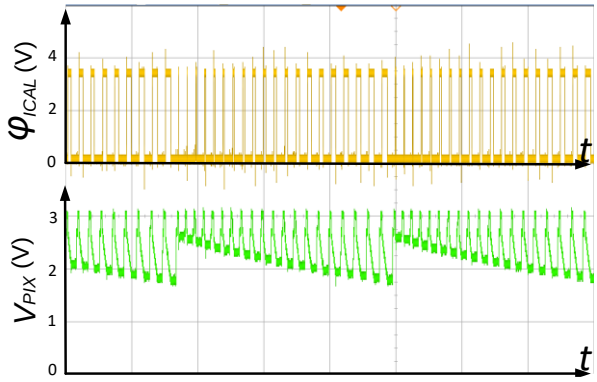


Figure 7-19. Measured output voltage of the pixel V7 in current mode calibration.

By zooming into the waveform, the details of the signals can be seen as shown in Figure 7-20. First, the FD is reset to V_{RST} of around 3V, then the signal value of the pixel V_{SIG} decreases with the width of the T_{ICAL}.

In full calibration operation, the unit integration time of the calibration current T_{CAL_unit} is set as 60 ns. The integration time T_{ICAL} increases evenly from 60 ns to 4096 × 60 ns in steps of 60ns.

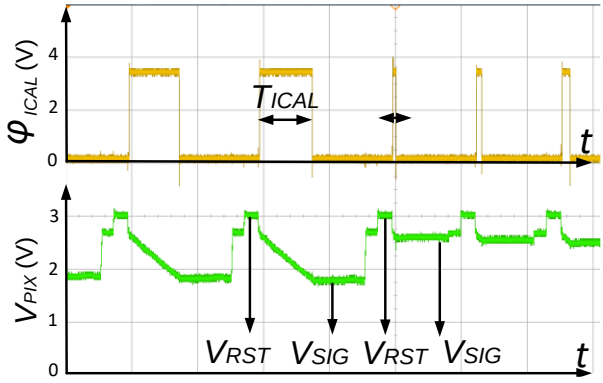


Figure 7-20. Measured output voltage of the pixel V7 in current mode calibration (zoomed in).

Figure 7-21 shows the measured digital output values of pixel V7 in full current mode calibration. From top to bottom, the curves represent the mean value of all pixels in the array, the mean value of all pixels in the same row, and the mean value of all pixels in the same column, respectively.

Due to the small value of the bias current used in the current source, the mismatch of the current source transistors from column to column leads to a considerable variation of the calibration currents between the columns. So here, different to the pixel mode and voltage mode calibration, the transfer curve extracted from the pixels in one column is used to calibrate all the pixels of the whole array.

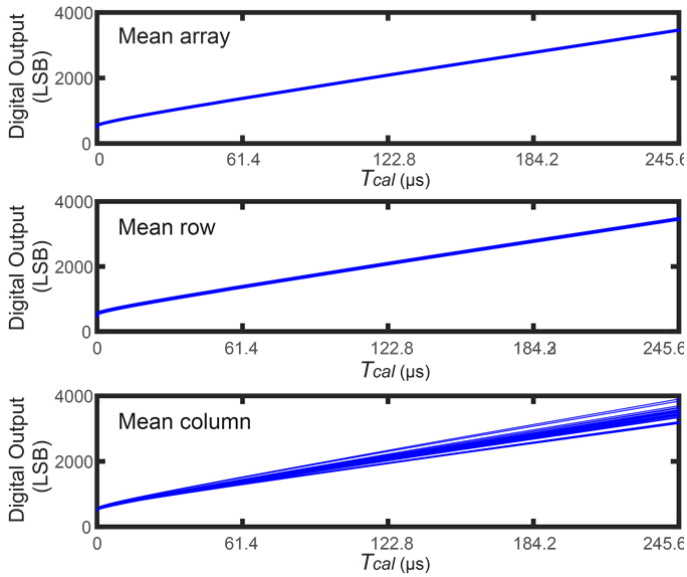


Figure 7-21. Measured digital output of the pixel V7 in current mode calibration.

The measured results show that the current calibration can improve the nonlinearity of pixel V6 and V7 from 0.45 % and 0.75 % to respectively 0.15 % and 0.16 %, which is better than the voltage mode calibration. It is mainly because the information of the Capacitance-Voltage characteristics of the C_{FD} has been contained in the updated ramp signal to calibrate the nonlinear errors during the pixel's electron-voltage conversion.

Figure 7-22 shows an image captured with this test chip. There are various groups with different pixel structures, which have different conversion gains and noise performances. The test chip has a non-uniform photon response due to all these variations.

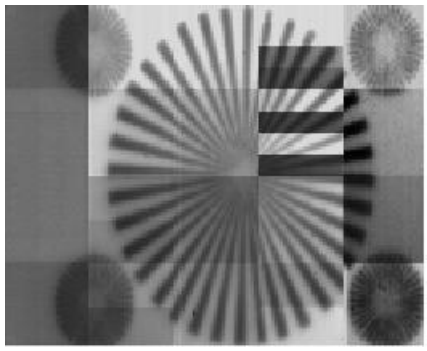


Figure 7-22. Captured image.

The measurement results of the proposed pixels are summarized and compared with previous designs in Table 7-2. The measured results show that the CTIA pixel achieves an outstanding tradeoff between linearity and other significant pixel's merits. other publications [7.1], [7.2], [7.15]-[7.17]. Furthermore, the proposed digital calibration methods improve the linearity of the image sensor. Most notably, pixel V3 achieves a nonlinearity of 0.028 %, which is two times better than the state-of-the-art.

Table 7-2. Performance comparison.

		[7.2]	[7.1]	[7.15	[7.16]	[7.17]	This work				
Process (nm)		180	500	350	180	65	180				
Array size		128 × 128	124 × 132	144 × 144	1620 × 1228	4 × 4	128 × 160				
Pixel size(μm^2)		10 × 10	20.1 × 20.1	9.5 × 9.5	2.6 × 2.6	22 × 22	12 × 10				
Frame rate		60	70	60	NA	NA	40				
Structure		Buf	CTIA	CTIA	CTIA	CTIA	n-SF pixel V1	Buf pixel V2	p-SF pixel V3	CTIA pixel V5	p-SF pixel V7
Fill factor (%)		47	42	26	NA	14	46.4	46.4	60	36. 3	42.0
Conversion gain (μV/e-)		56.3	NA	76	88.2	16	54	60	40	40	50
Peak SNR (dB)		NA	NA	49	41	NA	43.4	43.3	43.6	44.2	41
DR (dB)		74	48	61	47	62	75.5	73.4	76	65.5	74.2
Read Noise (mV)		0.187	0.82	1.90	5.2	0.98	0.20	0.27	0.144	0.65	0.14
Read Noise (e-)		4.17	NA	25	59	61	3.7	4.5	3.6	16.3	2.8
Dark current at room temperature (pA/cm^2)		NA	142	1540	490	NA	7.4	5.6	12.7	166.3	18
Full-Well capacity (e-)		20960	NA	32000	13800	77500	22070	21040	23100	30610	14460
Pixel PRNU at Sat (%)		NA	0.99	1.8	1.8	0.73	0.26	0.55	0.76	0.99	0.8
Non-linearity (%)	w/ o calibration	0.24	NA	NA	NA	0.57	0.41	0.24	0.68	0.095	0.75
	w/ PM calibration	0.058					0.0 50	0.042	0.028	0.048	0.04
	w/ VM calibration	NA					0. 30	NA	0.43	NA	0.46
	w/ CM calibration	NA					NA	NA	NA	NA	0.16

7.6 Conclusion

In this chapter, several different pixel structures, including a buffered CTIA pixel architecture, are proposed to realize a high linearity at the pixel-level. Three calibration methods further exhibit their advantages and disadvantages. The measured results of a proof-of-concept chip fabricated in a commercial 0.18-µm signal CIS process validate the techniques used. The CTIA pixel achieves the best linearity result out of all pixel structures. The pixel mode calibration method attains the best linearity results for all types of pixels. The voltage mode calibration method demonstrates the advantage of working without constant illumination while maintaining linearity improvements. Current calibration mode has the advantage of the voltage mode method and achieves a linearity improvement approaching that of the pixel mode method.

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Chapter 8 Conclusions

In this thesis, the linearity characteristics as well as possible improvement of the linearity of CMOS image sensors are explored. The linearity improvements have focused on two aspects: pixel-level optimization and system-level calibration, both are verified by means of experimental results of several test chips. In this final chapter, based on a summary of the main findings and contributions of this thesis, suggestions for future improvement of the CMOS image sensors are presented.

8.1 Main Contribution

In this thesis, the major achievements are listed as follows:

Regarding contributions to the nonlinearities of the CMOS image sensors.

- In Chapter 3, parameters deciding the linearity performance of a CMOS image sensor are discussed. A behavioral model is used to assist the theoretical analysis. The measurement results of a test chip involving different pixel's parameters prove the theoretical analysis.

- In Chapter 4, two types of pixel designs are proposed to reduce the nonlinear errors of a traditional 4T pixel. Measurement results of a prototype image sensor verify the conclusions of Chapter 3.

- The temperature effect on the linearity of the image sensors is discussed in Chapter 6. The measured results of the test chip are well in line with an updated linearity model.

Regarding the pixel-level linearity optimization of the CMOS image sensors.

- Chapter 4 proposes two types of pixel designs to reduce the nonlinear errors of the image sensors. Measurement results verify the linearity improvements of the pixels compared to the 4T pixel.

- More pixel structures targeting high linearity are presented in Chapter 7, especially a type of CTIA pixel achieving the best linearity result by canceling the nonlinearity caused by the gain of the source follower G_{SF} and integration capacitor C_{FD}.

Regarding the system-level linearity optimization of the CMOS image sensors.

- A digital calibration method is proposed in Chapter 5 to address the nonlinear errors caused by the pixel as well as by the readout circuitry. The simulation results of a hybrid behavioral model verify the calibration method. Measured results of a test chip thoroughly validate the effectiveness of the calibration method in multiple conditions.

- In Chapter 6, the experimental results of the test chip also prove the effectiveness of the calibration method against temperature variations.

- Based on the calibration method proposed in Chapter 5, two other types of calibration methods are presented in Chapter 7 to overcome the deficiency of the first calibration method. These two methods get rid of the requirement of a

constant illumination during the calibration operation, which greatly simplifies the calibration process, while maintaining the linearity improvement.

8.2 Future Work

This thesis has focused on the studies of the linearity of a CMOS image sensor from different standpoints of view. Different techniques are proposed to mitigate the nonlinear errors of a CMOS image sensor. There are still many related topics worth further investigating in future work.

Study of the performance improvement of the CTIA pixel

In this work, several test chips with different pixel structures have been investigated. Compared with the 4T pixel, the optimized pixels reduce the nonlinear errors of the pixel from different aspects. A CTIA pixel achieves the best linearity result without calibration: a nonlinearity less than 0.1 % is measured. However, a CTIA pixel has a larger dark current and poorer noise performance. It is worthwhile to further investigate the improvement of the other merits on the CTIA pixel while maintaining its high linearity.

Optimization of the third calibration method: current mode calibration

Chapter 7 proposed a calibration method which uses a current source to imitate the photocurrent of the pixel and furthermore to calibrate the photon response of the image sensor. Nevertheless, there is a large variation among the calibration current in the column array due to the small current value. It is better to use one calibration current to feed on the FD node of the pixels in each column sequentially by varying the switches in the column decoder circuit. The more accurate the transfer curve can be measured, the more superior the linearity improvement of the image sensor will be.

Application of the calibration methods on current mode pixels

Compared to the voltage mode pixels introduced in this thesis, current mode pixels usually achieve a larger dynamic range and are especially suitable for image computation; however, in general the current mode pixels have a poor linearity performance. It would be of great academic interest to apply the calibration methods on current mode pixels, which will combine these advantages.

Application of the color filter on the image sensor

In this work, all test image sensors are fabricated without a color filter. It is not easy to observe the linearity difference in or from a monochrome photo. In a future

design, color filters could be added on the sensors to get a clear visual comparison on the effectiveness of the calibration methods.

Summary

This thesis provides a thorough analysis of the linearity characteristics of a CMOS image sensor. Firstly, this thesis analyzes the factors that cause the nonlinearity of the image sensors. These factors are then verified by simulation results of a proposed behavioral model and the measurements in a prototype chip. Secondly, different techniques are presented to improve the linearity of the whole imaging system; and the effectiveness of these techniques is further confirmed by measurement results of several test chips.

Chapter 1 introduces the background, motivation and outline of this thesis. The reasons for the necessity of a highly linear imaging system for the next generation photography equipment are explained. Two types of silicon-based image sensors: Charged Coupled Device (CCD) and Complementary Metal-Oxide Semiconductor (CMOS) are introduced and compared, based on their fundamental working mechanisms, as well as their advantages and disadvantages. In this thesis, the research topic is focused on CMOS image sensors because of their benefits of low cost, low power and system integration capability.

Chapter 2 starts with an overview of the fundamental photodetection principles of photodiodes, and then goes to an introduction of typical pixel structures. Because of the excellent balance among the critical parameters of the image sensor such as noise, fill factor and dark current, the 4T pixel structure has become the most popular pixel structure for the CMOS image sensor.

In Chapter 3, a theoretical analysis of the nonlinear errors in a CMOS image sensor based on the 4T pixel structure, is presented. A behavioral model of a CMOS image sensor focused on nonlinearity and described with MATLAB, is then proposed. In a CMOS image sensor, the voltage gain of the source follower (G_{SF}) and the integration capacitance (C_{FD}) are influenced by the value of the pixel's output voltage. Therefore the inconstant G_{SF} and C_{FD} can be considered as the main nonlinearity sources in the image sensor. These two factors are further verified by means of the measurement results of a test chip, fabricated in a commercial 0.18-μm 1P4M CIS process.

Based on the conclusion of Chapter 3, two types of new pixel structures are introduced to reduce the nonlinearity of the pixel in Chapter 4. The first pixel type: the buffer pixel mitigates the nonlinearity of the source follower present in a

traditional 4T pixel. And the additional metal-insulator-metal (MIM) capacitor on the floating diffusion node of the second 4T pixel type brings down the nonlinear ratio of the integration capacitor and thus improves the linearity. Measurements conducted on a prototype image sensor adopting a dual correlated double sampling (CDS) show the linearity improvement on a pixel-level.

Chapter 5 proposes a digital assisted calibration method to further minimize the nonlinearity caused by the pixel and readout circuitry. A hybrid behavioral model described by MATLAB and Verilog-A is used to verify the calibration method. The linearity of the image sensor deteriorates when the high voltage of the transfer transistor in the pixel (V_{TXH}) increases. This is explained by the spill-back effect in the transfer transistor's channel observed in TCAD simulation results and further verified by measured results. The test results of the chip measured at different V_{TXH} values, exposure times, column gains and wavelengths of the light source, sufficiently validate the calibration method, which efficiently suppresses the nonlinearity of the image sensor.

Chapter 6 explores the effect of the temperature on the pixel performance in CMOS image sensors. It is of great importance to conduct such studies since there are a lot of applications where the image sensors need to withstand substantial temperature variations. The behavioral model proposed in Chapter 3 is updated with temperature characteristics. The measured results of the test chip agree well with the simulation results of the model. The digital calibration method proposed in Chapter 5 also demonstrates its excellent immunity to temperature variation.

Based on the linearity optimization methods proposed in Chapter 4 and 5, more techniques are employed to linearize a CMOS image sensor in Chapter 7. Several types of pixels are proposed. In particular, one type of CTIA pixel minimizes the nonlinear errors of the pixel caused by the gain of the source follower G_{SF} and integration capacitor C_{FD}, thus achieves the best linearity results among the proposed pixel structures at the cost of a lower fill factor, a larger noise and dark current. Subsequently, two other types of calibration methods are explored to address the limitations of the calibration method employed in Chapter 5.

A prototype image sensor with a pixel array of 128 × 160 is implemented in the same technology as used in Chapter 3 and 4, and is used to verify the improvement of the linearity with the proposed techniques. The test chip with an enhanced digital resolution has a column pitch of 12μm. One type of 4T pixel working in pixel mode calibration has a nonlinearity of 0.028 %, which is 2 times better than that of the previous state-of-the-art. Voltage mode and current mode calibration methods demonstrate the advantage of working without constant illumination while maintaining linearity improvements.

Chapter 8 summarizes and concludes the work presented in this thesis and

provides advice for future research.

Samenvatting

Dit proefschrift verschaft een uitvoerige analyse van de lineariteit eigenschappen van CMOS beeldsensoren. Allereerst is een analyse gemaakt van de factoren die de niet-lineariteit in beeldsensoren veroorzaken. Deze factoren zijn vervolgens geverifieerd in een simulatie met een voorgesteld gedragsmodel en getest met een prototype sensor. Ten tweede zijn verschillende technieken voorgesteld om de lineariteit van het gehele beeldvormingssysteem te verbeteren, waarvan de effectiviteit vervolgens is bevestigd door de meetresultaten van verschillende testchips.

Hoofdstuk 1 beschrijft de achtergrond, beweegredenen en kaders van dit proefschrift. Uitgelegd wordt waarom een sterk lineair beeldvormingssysteem nodig is voor de volgende generatie lithotografie apparatuur. Twee op silicium gebaseerde typen beeldvormingssystemen, de CCD en CMOS-beeldsensors, worden geïntroduceerd en vergeleken op basis van hun werkingsmechanisme alsmede hun voor- en nadelen. Het onderzoek in dit proefschrift richtte zich op CMOS-beeldsensors, vanwege hun lage kosten, laag benodigd vermogen en de mogelijkheid tot systeemintegratie.

Hoofdstuk 2 begint met een overzicht van de fundamentele fotodetectie principes van fotodiodes en vervolgt dan met een introductie op typische pixelstructuren. Dankzij de uitstekende balans tussen de belangrijkste eigenschappen van de beeldsensor zoals ruis, vulfactor en donkerstroom, is de 4T-pixelstructuur inmiddels de populairste pixelstructuur voor CMOS beeldsensoren.

In Hoofdstuk 3 wordt een theoretische analyse gespresenteerd van niet-lineaire fouten in de CMOS-beeldsensor gebaseerd op de 4T-pixelstructuur. Een gedragsmodel van de CMOS beeldsensor, gefocusseerd op lineariteit en geschreven in MATLAB, wordt vervolgens voorgesteld. In een CMOS-beeldsensor worden de spanningsversterkering van de bronvolger (G_{SF}) en de integratiecondensator (C_{FD}) beïnvloed door de uitstuurspanning van de pixel. De niet-constante G_{SF} en C_{FD} kunnen daarom beschouwd worden als de belangrijkste bronnen van niet-lineariteit in de beeldsensor. Deze twee factoren worden verder geverifieerd middels de meetresultaten van een testchip, vervaardigd in een commercieel 0.18-µm 1P4M CIS-proces.

Op basis van de conclusie uit Hoofdstuk 3 worden in Hoofdstuk 4 twee nieuwe

soorten pixelstructuren gepresenteerd die de niet-lineariteit van de pixel verminderen. De eerste pixel, de bufferpixel, vermindert de niet-lineariteit van de bronvolger in een traditionele 4T-pixel, terwijl een extra metaal-isolator-metaal-condensator (MIM-condensator) op de floating diffusion node van de tweede 4T-pixel de niet-lineariteitsratio van de integratiecondensator verlaagt en daardoor de lineariteit verbetert. Metingen uitgevoerd met een prototype van de beeldsensor, die gebruikt maakt van dubbel gecorreleerde bemonstering laten verbetering zien van de lineariteit op pixelniveau.

Hoofdstuk 5 introduceert een nieuwe digitale kalibratiemethode om de niet-lineariteit, veroorzaakt door de pixels en de uitleescircuits, verder te minimaliseren. Een hybride gedragsmodel, geschreven in MATLAB en Verilog-A, wordt ingezet om de kalibratiemethode te verifiëren. De lineariteit van de beeldsensor vermindert wanneer de hoge spanning van de transfer transistor van de pixel (V_{THX}) toeneemt. Dit wordt verklaard door het spill-back-effect in de transistortunnel, dat werd waargenomen in een TCAD-simulatie en verder is geverifieerd door metingen. De resultaten van tests met de chip, uitgevoerd met verschillende V_{THX} waardes, sluitertijden, kolomversterkingsfactoren en golflengtes van de lichtbron, valideren de kalibratiemethode, die de niet-lineariteit van de beeldsensor adequaat onderdrukt.

Hoofdstuk 6 onderzoekt het effect van temperatuur op de prestatie van de pixel in CMOS-beeldsensors. Het is belangrijk dergelijke studies uit te voeren, daar er veel toepassingen zijn waarin beeldsensoren grote temperatuurschommelingen moeten doorstaan. Het in Hoofdstuk 3 voorgestelde gedragsmodel is bijgewerkt met de temperatuurkarakteristieken. De resultaten uit de simulatie komen goed overeen met de meetresultaten. De in Hoofdstuk 5 geïntroduceerde digitale kalibratiemethode laat tevens een uitmuntende ongevoeligheid voor temperatuurwisselingen zien.

Meer technieken, gebaseerd op de optimaliseermethodes in Hoofdstuk 4 en 5, worden in Hoofdstuk 7 ingezet om de CMOS-beeldsensor lineair te maken. Verschillende soorten pixels worden voorgesteld. In het bijzonder één type CTIA-pixel verkleint de niet-lineaire fouten van de pixel, veroorzaakt door de versterkingswaarde van de bronvolger G_{SF} en de integratiecondensator C_{FD}, en behaalt van de voorgestelde pixelstructuren de beste lineariteitsresultaten, tegen de prijs van een lagere vulfactor, meer ruis en meer donkerstroom. Vervolgens worden twee andere kalibratiemethodes onderzocht om de nadelen van de kalibratiemethode uit Hoofdstuk 5 te verhelpen.

Een prototype van de beeldsensor met een pixelmatrix van 128 bij 160 werd geïmplementeerd in dezelfde fabricagetechniek als in Hoofdstuk 3 en 4, en wordt gebruikt ter verificatie van de lineariteitsverbetering met behulp van de

voorgestelde technieken. De testchip met de uitgebreide digitale resolutie heeft een kolomafstand van 12 µm. Eén soort 4T-pixel bereikte in de pixelkalibratiemodus een niet-lineariteit van 0.028 %, hetgeen twee keer beter is als eerder aangetoond in literatuur. De methodes met spanning- en stroomkalibratie laten het voordeel zien van een kalibratie zonder een constante belichting, terwijl lineariteitsverbeteringen behouden blijven.

Hoofdstuk 8 vat het gepresenteerde werk in dit proefschrift samen, formuleert conclusies en doet aanbevelingen voor verder toekomstig onderzoek.

List of Abbreviations

List of acronyms

ADC Analog-to-digital converter

BSI Back side illumination

CCD Charge-coupled device

CDS Correlated double sampling

CG Conversion gain

CIS CMOS image sensor

CMOS Complementary metal-oxide-semiconductor

CMRR Common-mode rejection ratio

CTIA Capacitive transimpedance amplifier

CS Current steering

DAC Digital-to-Analog converter

DC Dark current

DFF D-flip-flop

DI Direct injection

DN Digital number

DNL Differential nonlinearity

DR Dynamic range

DSNU Dark signal non-uniformity

EA Error amplifier

FD Floating diffusion

FF	Fill factor
FR	Frame Rate
FSI	Front side-illumination
FWC	Full-well capacity
GMI	Gate modulated injection
IC	Integrated circuit
INL	Integral nonlinearity
IOS	Input offset storage
LDO	Low dropout regulator
LSB	Least Significant Bit
LUT	Look-up table
MIM	Metal-insulator-metal
MOM	Metal-oxide-metal
MOS	Metal oxide semiconductor
MTF	Modulation transfer function
OOS	Output offset storage
OPA	Operational amplifier
PD	Photodiode
PPD	Pinned photodiode
PRNU	Photon response non-uniformity
QE	Quantum efficiency
ROW	Row select transistor
RST	Reset transistor
SF	Source follower transistor
SNR	Signal-to-noise ratio

SRAM Static random-access memory

SS-ADC Single-Slope Analog-to-Digital Converter

TX Transfer gate transistor

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Fei Wang
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List of Publications

Journal Papers

F. Wang, L. Q. Han, A. J. P. Theuwissen, "Development and evaluation of a highly linear CMOS image sensor with a digitally assisted linearity-calibration," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 2970-2981, 2018.

F. Wang, A. J. P. Theuwissen, "Temperature effect on the linearity performance of a CMOS image sensor," *IEEE Sensors letter*, vol. 2, no. 3, pp.1-4, 2018.

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Conference Proceedings

F. Wang, A. J. P. Theuwissen, "Two calibration methods to improve the linearity of a CMOS image sensor," in *Proc. Electronic Imaging*, San Francisco, USA, pp. 1-6, 2018. **(Best Paper Award)**

F. Wang, A. J. P. Theuwissen, "Techniques for pixel-level linearity optimization," presented at *Workshop of CMOS Image Sensors for high performance applications*, Toulouse, France, pp.1-20, 2017.

F. Wang, A. J. P. Theuwissen, "Linearity analysis of a CMOS image sensor," in *Proc. Electronic Imaging*, San Francisco, USA, pp. 84-90, 2017.

F. Wang, L. Q. Han, A. J. P. Theuwissen, "A Highly Linear CMOS Image Sensor with a Digitally Assisted Calibration Method," in *Proc. Int. Image Sensors Workshop*, Hiroshima, Japan, pp. 336-339, 2017.

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