Fabrication of Silicon Heterojunction Interdigitated Back-contacted (SHJ-IBC) solar cells

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Fabrication of Silicon Heterojunction Interdigitated Back-contacted (SHJ-IBC) solar cells

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Abstract

Silicon heterojunction (SHJ) solar cell featuring a-Si:H/c-Si structure is a promising candidate to reach high efficiency within single junction solar cells. Despite the standard front/rear contacted SHJ solar cell has an outstanding performance as 25.1%(V_{OC}=738mV, J_{SC}=40.8mA/cm^2, and FF=83.5%)[1], it is still limited by the front grid optical shading, parasitic absorption and lateral transport in front layers: amorphous silicon and TCO. To overcome these limitations, the Silicon heterojunction interdigitated back-contacted (SHJ-IBC) solar cell concept is designed by combining Heterojunction and interdigitated back-contacted structure together. It is an advantageous concept attracting R&D interest, providing the high V_{OC} of SHJ solar cells and the high J_{SC} of IBC solar cells. However, compared to the SHJ front/rear contacted solar cell, SHJ-IBC solar cell demands a relatively complicated patterning process implying more sensitivity to the induced contamination during the fabrication process.

In this work, to achieve the high efficiency of such SHJ-IBC solar cells, the fabrication process based on different patterning approaches was designed and optimized. Among these proposed processes, the approach based on lift-off patterning technique is quite promising, in which only one photolithography step is needed for the patterning of a-Si:H layers. The first run of SHJ-IBC cells were successfully fabricated based on such patterning technique. 15.6% efficiency was achieved after certain annealing time with V_{OC}=576mV, J_{SC}=38.4mA/cm^2, and FF=70%. The solar cell is analysed and several limiting factors are found out, such as emitter passivation, shunt paths, and parasitic absorption. Based on these factors, several recommendations are put forward, such as double SiO_2 as etching barrier, application of TCO and optimization of the emitter properties.

List of Figures

List of Tables

Contents

1

Introduction

1.1. Solar energy

In December 2015, a historic landmark agreement in the 21st session of the Conference of the Parties (COP21) to keep a curb on the global rising temperature was agreed by 195 nations, aiming at the maximum average temperature rise by 1.5°C. [2] This agreement added more support and credit to the shift in energy investment towards the renewable Energy, which is the future solution to the decarbonised society.

Among all the renewable energy candidates, solar energy, the most abundant energy resource on this planet (*Figure 1.1*), is regarded as one of the best options. The great advantage of solar energy lies in that it cannot be monopolized by some countries. It is almost available everywhere and, with certain devices, every individual can harness it successfully. Without concerns about the scarcity, solar energy together with other renewable resources can provide a stable price in the future and even gradually decreasing price because of the learning curve[3].

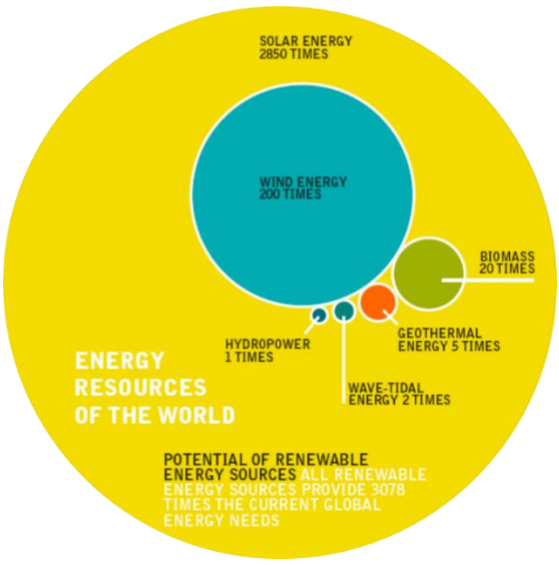


Figure 1.1: Energy resources of the world[4]

1.2. Photovoltaic technology

The technology employed in the utilization of solar energy can be mainly divided into two sectors: Solar Photovoltaics (PV) and Concentrating Solar Thermal Power (CSP). In the last several years, Solar PV experienced a historical boost, from annual 29.5GW$_P$ installation in 2012 to annual 53.7 GW$_P$ installation in 2015 (*Figure 1.2*).

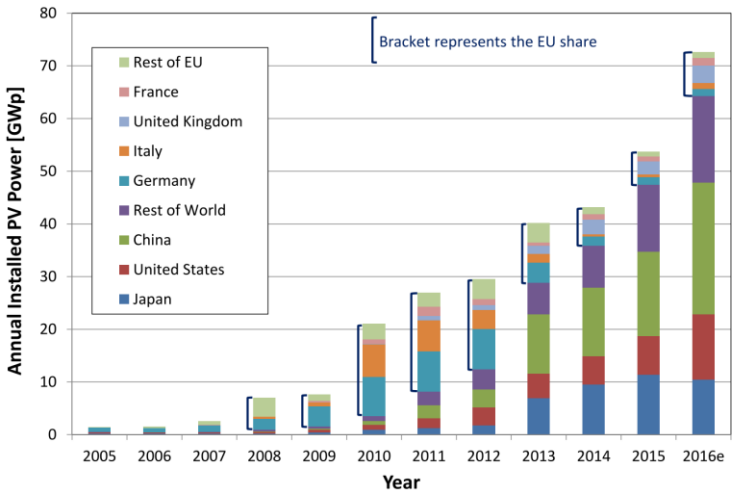


Figure 1.2: Annual PV system installations from 2005 to 2016[2]

The fundamental principles behind this technology is Photovoltaic Effect, in which the sunlight is directly converted into electricity. Based on this, lots of research and development have been involved to improve the technology during the last decades. Solar cells now can be classified into three generations[5]. The first-generation technology is represented by crystalline silicon solar cells. Its technology and knowledge learning have been developed for many years and still dominates the market. Thin-film technology is the second-generation technology. It features the low-cost due to the reduced material consumption. The third-generation technology is referred to all the emerging technologies, aiming achieving low cost without the sacrifice of efficiency. They are still under development. Multi-junction solar cells, multi-exciton generation solar cells[6], and intermediate solar cells are examples of such an arising technology.

1.3. Advanced crystalline silicon solar cell structures

The largely increasing installation in the last decades was mainly based on the crystalline silicon(c-Si) technology. According to the report given by Fraunhofer Institute for Solar Energy Systems, c-Si technology has accounted for 93% of the total market share in 2015. [7] In the forthcoming years, it can be safely estimated that c-Si technology will continue dominate the market because of its durability, stability, and higher efficiency. In this work, SHJ-IBC (Silicon Heterojunction Interdigitated Back Contacted) solar cells combines the advantages of two advanced silicon solar cell structures: Silicon Heterojunction(SHJ) and Interdigitated Back Contacted(IBC) structures.

1.3.1. Interdigitated back-contact (IBC) solar cell

The Interdigitated Back Contacted solar cell, as its name suggests, the emitter, which is moved to the back surface, together with the base contact, forms an interdigitated structure to separate with each other. The sketch of such a structure is presented in *Figure 1.3* with a comparison to the conventional structure. With no emitter contact at the front side, more light can penetrate into the absorption. This is realized by the removal of the shading caused by emitter contact. What's more, the original emitter contact area at the front can be treated by some light absorption enhancement techniques, leading to further increase of the photon generated current.

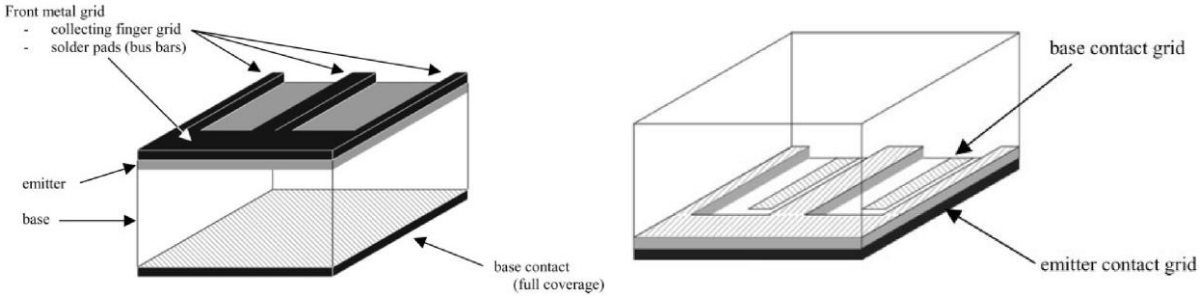


Figure 1.3: Comparison between a conventional solar cell and an IBC solar cell[8]

Because of its superior performance in light management, such a structure is very promising in the future. For the mass production manufacture in Industry, SunPower has been the market leader for couples of years. Its renowned IBC solar cell have already experienced three generations so far and the conversion efficiency have achieved 21.5% in 2004 and 23% in 2012 [9] and 25% in 2014 [10]*Figure 1.4*.

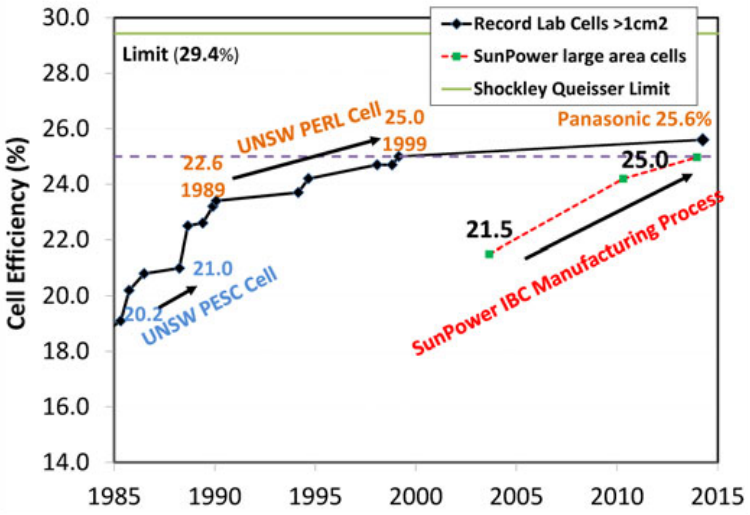


Figure 1.4: Single junction silicon solar cell conversion efficiency results: lab versus Industry(SunPower)[10]

Such a superior structure brings lots of complexities and expenditures to the fabrication process. As a result, the levelized cost of electricity (LCOE) is not that competitive compared to other simple structures[11].

1.3.2. Silicon heterojunction (SHJ) solar cell

In conventional solar cells, to separate the photon-generated electron-hole pairs, two contacts should be applied on both sides of the absorber[12]. Such a separation can be improved by the introduction of a membrane contact with a larger band gap, namely, heterojunction. With the help of heterojunction, two barriers caused by band offsets at the surface of the absorber makes the membrane semi-permeable for respective carriers, as shown in *Figure 1.5*. To be mentioned here is that, for the practical heterojunctions, band offsets exist on both conduction band and valence band, in which tunnel effect can help.

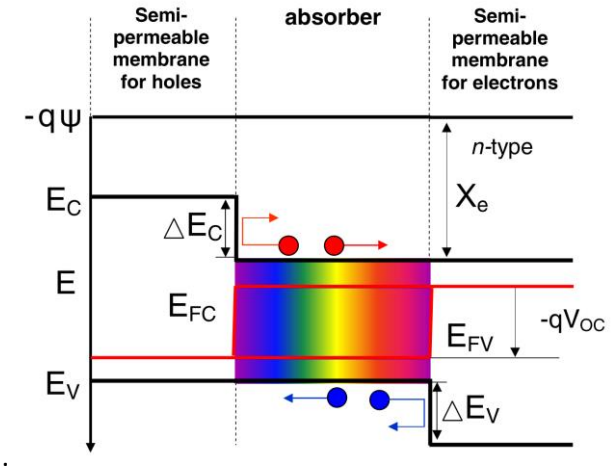


Figure 1.5: Schematic band diagram of heterojunction solar cell (open-circuit condition) [13]

1.3.2.1.Comparison between c-Si homojunction and heterojunction solar cells

Compared to the homojunction structure, silicon heterojunction solar cells have several advantages in terms of fabrication process. For example, lower thermal budget and less fabrication time because of the application of amorphous silicon hydrogenated(a-Si:H) layers, as shown in *Figure 1.6*. Thanks to such a low temperature process, lots of potential damage caused by high temperature to other component can also be avoided. What's more, given that the applied a-Si:H layers are very thin, the material cost can be even lowered down[14]. As for the cell performance, silicon heterojunction solar cells provide increased open-circuit voltage (V_{OC}) because of the improved passivation. In addition, SHJ solar cells provide a revised dependence of temperature[15] [16].

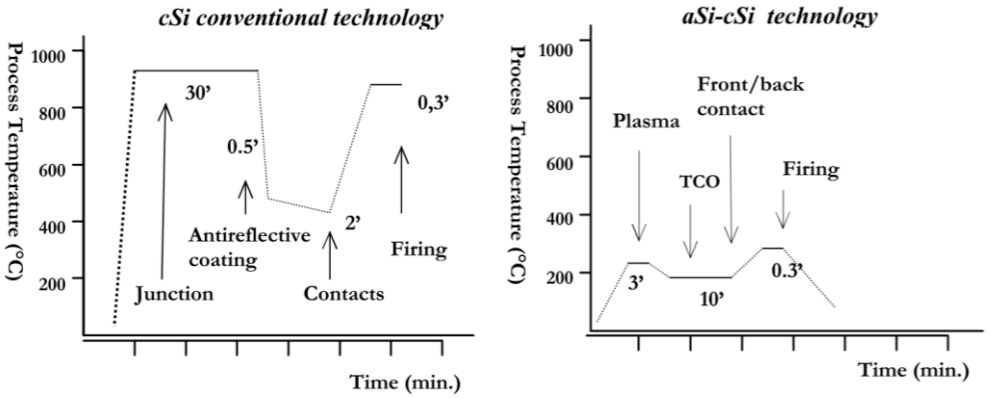


Figure 1.6: Comparison of fabrication processing temperature and time between c-Si conventional solar cells and Silicon Heterojunction solar cells [17]

1.3.2.2.Surface passivation techniques in SHJ solar cells

The silicon heterojunction structure suffers a lot from the a-Si:H/c-Si defects when comparing to conventional homojunction structure. However, such a problem can be fixed by surface passivation techniques. When the a-Si:H layer is deposited onto the c-Si surface, not all the dangling bonds at the surface can be bonded because the a-Si:H network configuration does not always fit for bonding. As a result, these unpassivated dangling bonds leads to defects at the surface. Such a problem can be fixed by passivating those dangling bonds with hydrogen, which is the so-called chemical passivation. It is normally achieved by depositing a thin intrinsic a-Si:H layer. In addition, the passivation quality can be further improved by field-effect passivation, which is achieved by deposition of the doped a-Si:H layer. Because of the fixed charge in the a-Si:H layer, the electric field is formed to force and accelerate the electron/hole separation to minimize recombination.

1.3.2.3.Disadvantages

Even though SHJ solar cells have a very great performance with highest efficiency amounting to 25.1% (V_{OC}=738mV, J_{SC}=40.8mA/cm^2, and FF=83.5%)[1], it still have some disadvantages. The main one comes from the front grid shading and parasitic absorption of front emitter layers which lead to the decrease of J_{SC}. What's more, the front TCO is limited by a trade-off between series resistance (R_S) and anti-reflection (AR) properties.

1.4. SHJ-IBC solar cell

Silicon heterojunction interdigitated back-contacted (SHJ-IBC) solar cell is a superior structure of lots of interest. It provides the high V_{OC} of SHJ solar cell and the high J_{SC} of IBC solar cell, by combining these two structures together[18] [19]. The typical structure is shown in *Figure 1.7*, comprised of back surface field(BSF), emitter, and metal at the rear side, and certain passivation layers and AR coating at the front side.

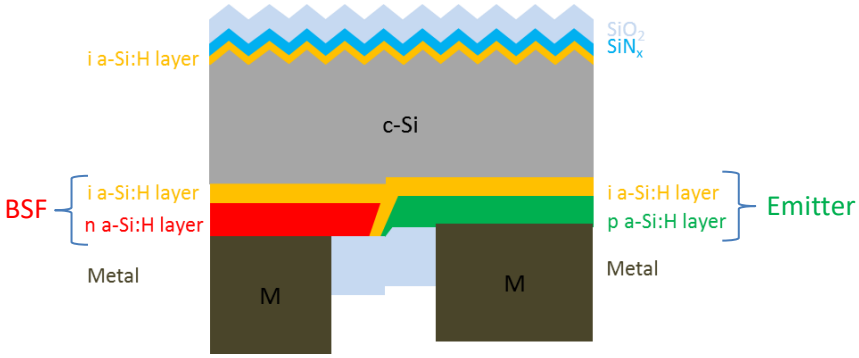


Figure 1.7: Schematic structure of SHJ-IBC solar cells

The theoretical efficiency limit for crystalline silicon based single junction is calculated to be 29.4% [20]. SHJ-IBC solar cells is the most promising one to approach this theoretical limit, as shown in *Figure 1.8*. It is reported that Kaneka has recently achieved a SHJ-IBC solar cell with efficiency of 26.6%[21], before which they held the word record 26.3% of such a structure[22].

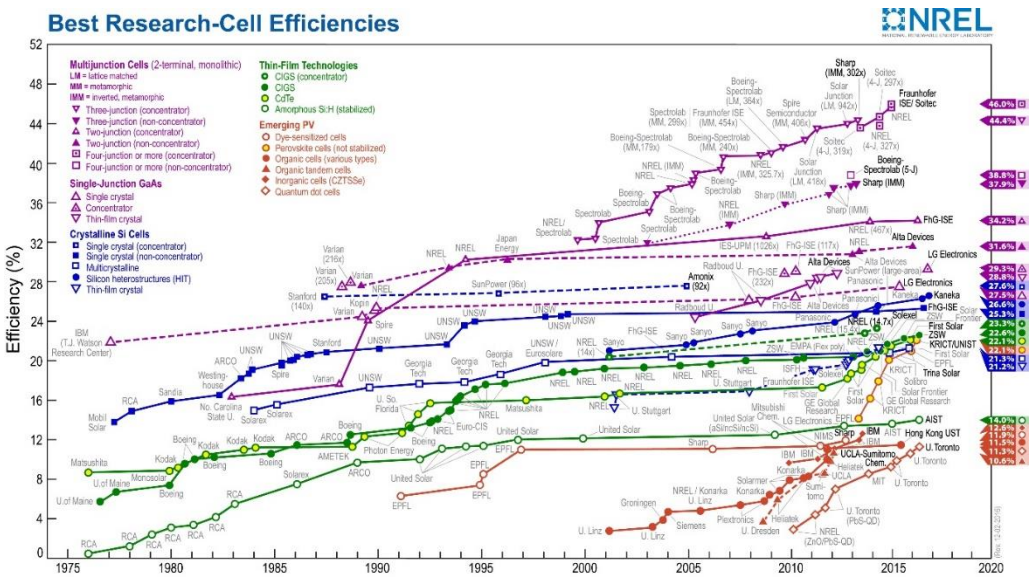


Figure 1.8:Best research-cell efficiencies[21]

However, compared to the SHJ solar cell, SHJ-IBC solar cell scarifies the FF a little bit to achieve the back contacted structure for higher J_{SC}. This is attributed to the induced contamination during the fabrication process. First, the need to break the vacuum in between the layers deposition induces contamination to the interfaces of different layers; Second, the patterning steps for the back interdigitated structure also contributes to the higher chance of contamination.

1.5. Motivation and outline of this work

As mentioned before, the latest world record conversion efficiency of SHJ-IBC solar cells is held by Kaneka, however, no details about this fabrication process have been disclosed so far. Many other research teams have reported their different fabrication processes and achieved nice devices with good performance. In this work, to achieve the high efficiency for such solar cells, the fabrication process based on different patterning approaches was designed and optimized. Among these proposed processes, the approach based on lift-off is quite promising, in which only one photolithography step is needed for the patterning of a-Si:H layers. According to the published fabrication process of SHJ-IBC solar cells with the efficiency of 25.6%[16], the former world record, two photolithography steps were employed for the patterning of the rear side. Normally, two photolithography steps are inevitable because the a-Si:H(i)/a-Si:H(p) layers (emitter) should be separated from the a-Si:H(i)/a-Si:H(n) layers (BSF) shown in *Figure 1.9* step 2 and step 4.

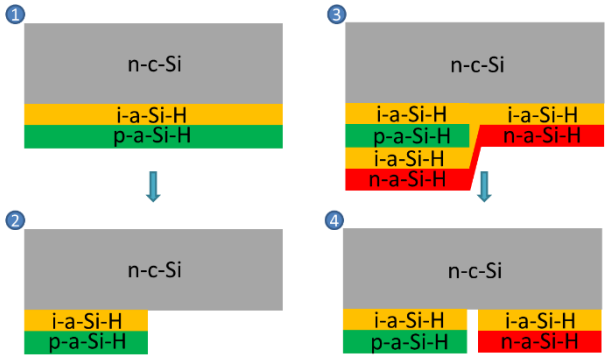


Figure 1.9 Sketch of conventional patterning process

This thesis is comprised of five chapters. Chapter 1 introduces the background of this thesis. First, the solar industry is described, and then, IBC and SHJ structures are discussed respectively, followed by a introduction of SHJ-IBC solar cells. Chapter 2 involves the main experiment instruments and techniques. Chapter 3 present five proposed approaches and their respective testing results and analysis. Lift-off process is considered to be the promising one because of its good testing results and simpler fabrication process. Chapter 4 focuses on the validation of lift-off process and the analysis of the performance of the fabricated solar cell. Some possible optimization methods are also put forward in this chapter. Chapter 5 gives a conclusion to this work.

2

Experimental Setup

In this chapter, the instruments and techniques involved in the fabrication of SHJ-IBC solar cells are introduced first. For example, the Plasma-enhanced Chemical Vapor Deposition(PECVD) technique and Metal evaporation. Then several measurement techniques are described, including Spectroscopic Ellipsometry(SE), Scanning Electron Microscope (SEM) and Quasi-Steady-State Photoconductance (QSSPC). After that, characterization parameters for solar cells are included, such Current density-Voltage (J-V) curve, External Quantum Efficiency (EQE) curve, and Transmittance/Reflectance(R/T) curve.

2.1. Fabrication Instruments and techniques

The a-Si:H layers and SiO_2 layers of the SHJ-IBC solar cells in this work are deposited with the help of Plasma-enhanced Chemical Vapor Deposition(PECVD). For the rear metal contact, it is realized by metal evaporation. They are shown in *Figure 2.1*.

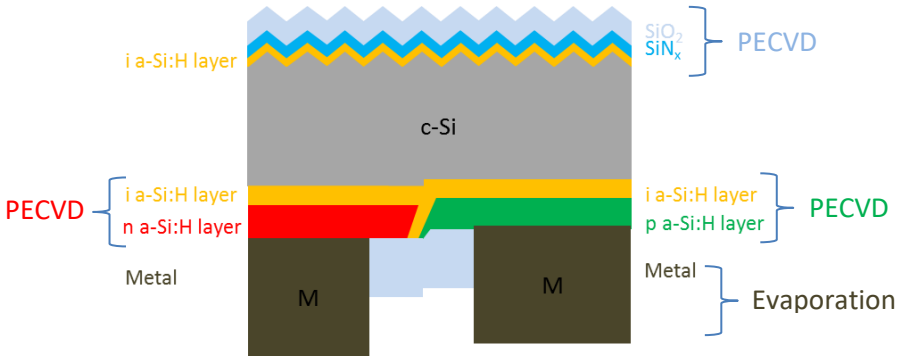


Figure 2.1: Schematic fabricated techniques involved in SHJ-IBC solar cells

2.1.1. Plasma-enhanced Chemical Vapor Deposition(PECVD)

The a-Si:H layers in emitter and BSF of the SHJ-IBC solar cells in this work are deposited with the help of Plasma-enhanced Chemical Vapor Deposition(PECVD). It was realized in Amor, Cleanroom 10000(CR10000), Else Kooi Lab(EKL), TU Delft. For the the SiO_2 layer at the front surface and the SiO_2 layers used as etching barriers during the process, PECVD is also used for the deposition. It was realized in Oxford Plasmasystem 100, Kavli Nanolab, TU Delft. *Figure 2.2* shows the schematic Plasma-Enhanced Chemical Vapor Deposition (PECVD) systems. It consists of a Radio Frequency (RF)

power generator, a substrate, a heater, reaction chamber gas system and pump system. In the reaction chamber, the RF power, provided by RF power generator, creates a plasma between electrodes in the deposition gas provided by gas system. The pressure of the chamber is maintained by pump system and the temperature is maintained by the heater. When the power is applied, the electrons get accelerated and become highly energetic. The deposition happens when the radicals, generated by collision between electrons and gas precursors, are attached to the sample surface in the substrate holder.

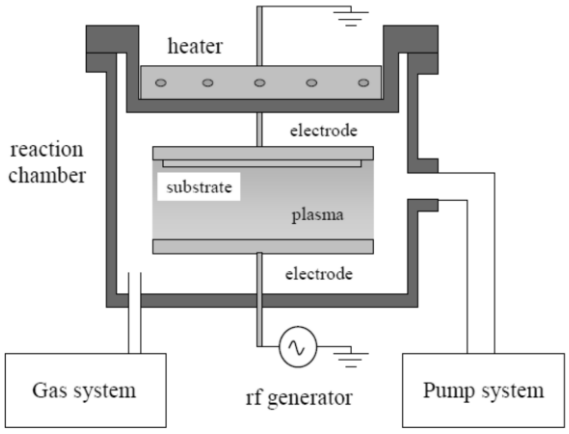


Figure 2.2 Schematic Plasma-Enhanced Chemical Vapor Deposition (PECVD) system[23]

2.1.2. Metal evapouation

In this work, 4 µm aluminium as a back-metal contact is made with Provoc Pro500s by metal evaporation. As is shown in *Figure 2.3*, the metal evaporation system consists of substrate, Tungsten boat, vacuum system and power supply. In general, the metal is put inside the tungsten boat. When the power is supplied, the tungsten boat is heated. As a result, metal gets evaporated and then deposited onto the surface of the sample in substrate.

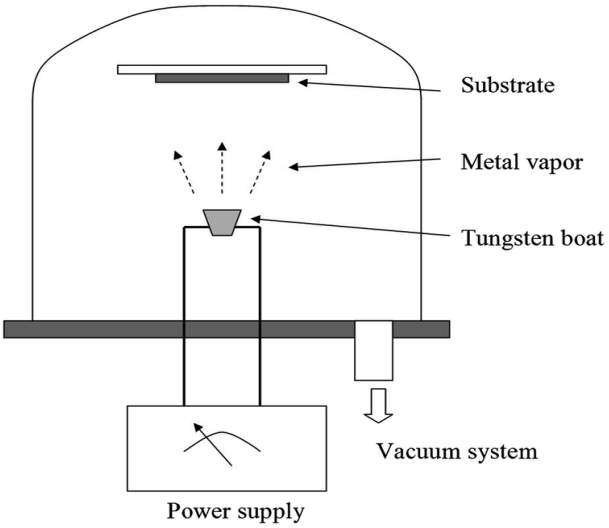


Figure 2.3 Schematic metal evaporation system[24]

2.2. Characterization instruments and techniques

In this section, several measurement techniques are described, including Spectroscopic Ellipsometry(SE), Scanning Electron Microscope (SEM) and Quasi-Steady-State Photoconductance (QSSPC). After that, characterization parameters for solar cells are included, such Current density - Voltage (J-V) curve, External Quantum Efficiency (EQE) curve, and Transmittance/Reflectance(R/T) curve.

2.2.1. Spectroscopic Ellipsometry

In this work, thickness measurement is performed mainly to calculate the etching rate and deposition rate of various layers, such as a-Si:H layers and SiO_2 layers. It is also used to check the uniformity of those etching and deposition processes. Thickness measurement is carried out by the Spectroscopic Ellipsometry (SE). Spectroscopic Ellipsometry (SE) is an optical technique based on the acquisition and analysis of the optical parameters.

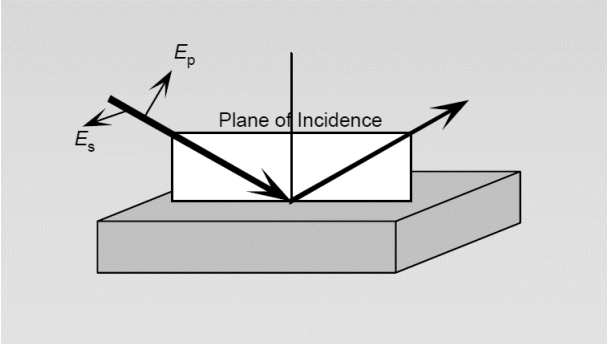


Figure 2.4 Schematic measurement of Spectroscopic Ellipsometry (SE)[25]

As is shown in *Figure 2.4*, a light is projected onto the sample and the reflected off beam is collected and analysed. By comparing the projected beam and reflected beam, some interesting results can be achieved. During this process, what Spectroscopic Ellipsometry (SE) measures are Psi (Ψ) and Delta (Δ). The desired parameters, such as thickness and reflective index, can be derived through certain model in which the interaction between light and sample are analysed. The whole process can be found in the following.

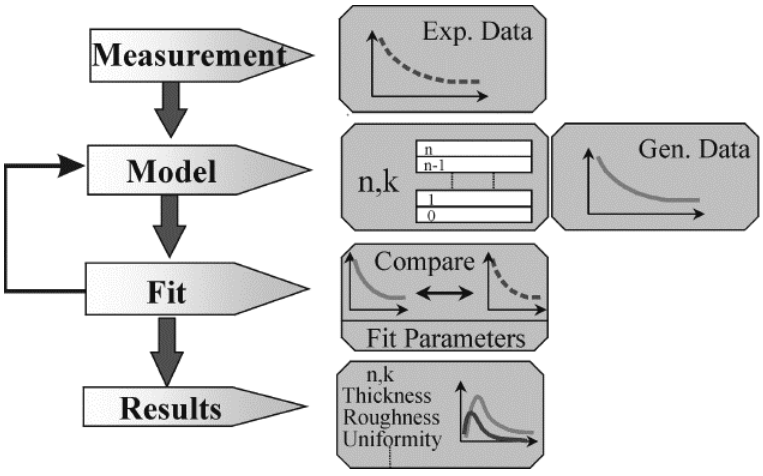


Figure 2.5 Schematic measurement of Spectroscopic Ellipsometry (SE) [25]

2.2.2. Scanning Electron Microscope (SEM)

In this work, Scanning Electron Microscope (SEM) is employed to detect the topology of the back surface of SHJ-IBC solar cell. *Figure 2.6* shows the basics of a Scanning Electron Microscope (SEM) system. It consists of an electron gun, condenser lens, objective lens, substrate, secondary electron detector and a display unit. The electron gun, as an electron source, produces the electron beam that will be focused and accelerated by the lens, and finally projected to the sample. The sample will then emit different numbers of secondary electron depending on the topology of the sample surface. These secondary electrons will then be collected by the secondary electron detector. By analysing the change in the number of electrons, the surface topology can be determined. In addition, X-ray emitted by the sample can be used to determine the elementary composition of the sample.

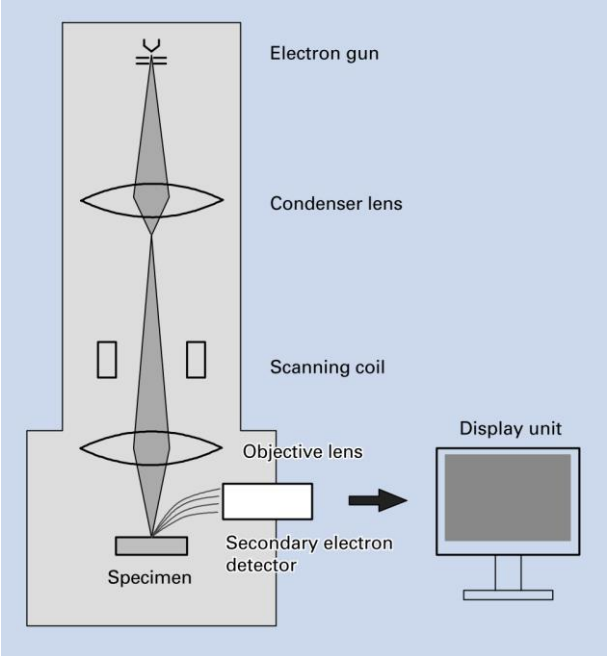


Figure 2.6 Schematic construction of a Scanning Electron Microscope (SEM) system [26]

2.2.3. Quasi-Steady-State Photoconductance (QSSPC)

In this work, the passivation quality of the a-Si:H/c-Si surface is evaluated by measuring the lifetime, which is realized with Sinton WCT-120 Lifetime Tester. A infrared light flash is pulsed onto the sample and excess carriers are then generated in the sample. The conductance of the sample, which is then so-called photoconductance, is brought up because of the excess carriers. The coil inside the stage of Sinton can generate electromagnetic waves to sense the difference of the photoconductance of the sample. By analysing the photoconductance, the excess carrier density can be derived. Then the effective minority carrier liftetime can be deducted based on different modes[27]. For example, Quasi-Steady-State (QSS) mode is used for samples with lifetime less than 200µs and Transient mode is for samples with lifetime over 200µs. Besides, situation current density (J_O) and implied Open-circuited voltage (iV_{OC}) can also be determined based on the measurements.

2.2.4. Illuminated J-V

The solar cell in the dark has a same J-V curve as a diode. When the cell is under illumination, the photo generated current will shift the original curve in accordance with the illumination intensity, which becomes the so-called the illuminated J-V curve[28], as shown in *Figure 2.7*. In this work, the illuminated J-V curve is achieved with Wacom AXS-156S solar simulator. The main parameters of the

SHJ-IBC solar cells for the performance analysis is obtained from the illuminated J-V curve, such as short circuit current(J_{SC}), open circuit current(V_{OC}), Fill factor(FF), series resistance(R_S) and shunt resistance(R_{SH}).

Open circuit current(V_{OC}) is the maximum voltage that s working solar cell can reach. It happens when the solar cell is open circuited where no current flows in the external circuit. V_{OC} is the function of J_0 which represents the recombination in the solar cell. In SHJ-IBC solar cell, V_{OC} is limited by the passivation of emitter/bulk interface, BSF/bulk interface, and front surface.

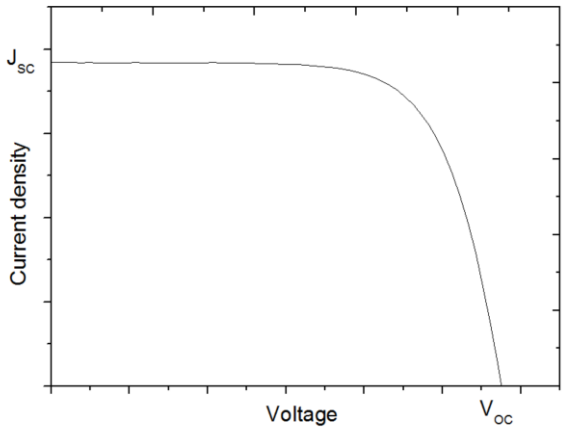


Figure 2.7 Typical J-V curve

Short circuit current density (J_{SC}) is the current density when the solar cell is short circuited. Since the current of the solar cell due to the collection of the photon generated carriers, which involves the absorption of the light and collection of the carriers. So, J_{SC} is mainly dependant on the optical properties and collection probability of the solar cell.

The Fill Factor(FF) is defined by the maximum power point of the solar cell. It can be calculated out by dividing the maximum power by the product of J_{SC} and V_{OC}. It mainly depends on the resistive loss and recombination of the solar cell.

Parasitic Resistivity is one of the loss accounting for the decrease of the power because of the dissipation. It consists of series resistance(R_S) and shunt resistance(R_{SH}). R_S can be evaluated from the slope of the V_{OC} point on the J-V curve while R_{SH} can be evaluated from the slope of the J_{SC} point on the J-V curve.

2.2.5. EQE

In this work, External Quantum Efficiency (EQE) curve is used to analyse the optical property and passivation quality. EQE is defined by the ratio of the incident photons that generate the successfully collected electron-hole pairs to the total incident photons. It is dependent of the optical loss and electrical loss. The optical loss includes reflection and transmission while the electrical loss mainly refers to the collection loss caused by recombination.

2.2.6. Transmittance/ reflectance

In this work, transmittance and reflection of SHJ-IBC solar cells are analysed to determine the optical loss of the SHJ-IBC solar cell. The measurement is achieved with Perkin Elmer Lambda 950 spectrophotometer, of which integration sphere is the core component. *Figure 2.8* shows schematic

construction of an integrating sphere. It consists of transmittance sample holder, reflectance sample holder, reference holder and light trap. The general working principle is that the transmittance or reflectance is calculated by comparison between the detected light beam after transmitting or reflected and the reference beam. Compared to the standard spectrometer with conventional detector arrangement, the integrating sphere performs better because of the less loss before the light arrives at the detector.

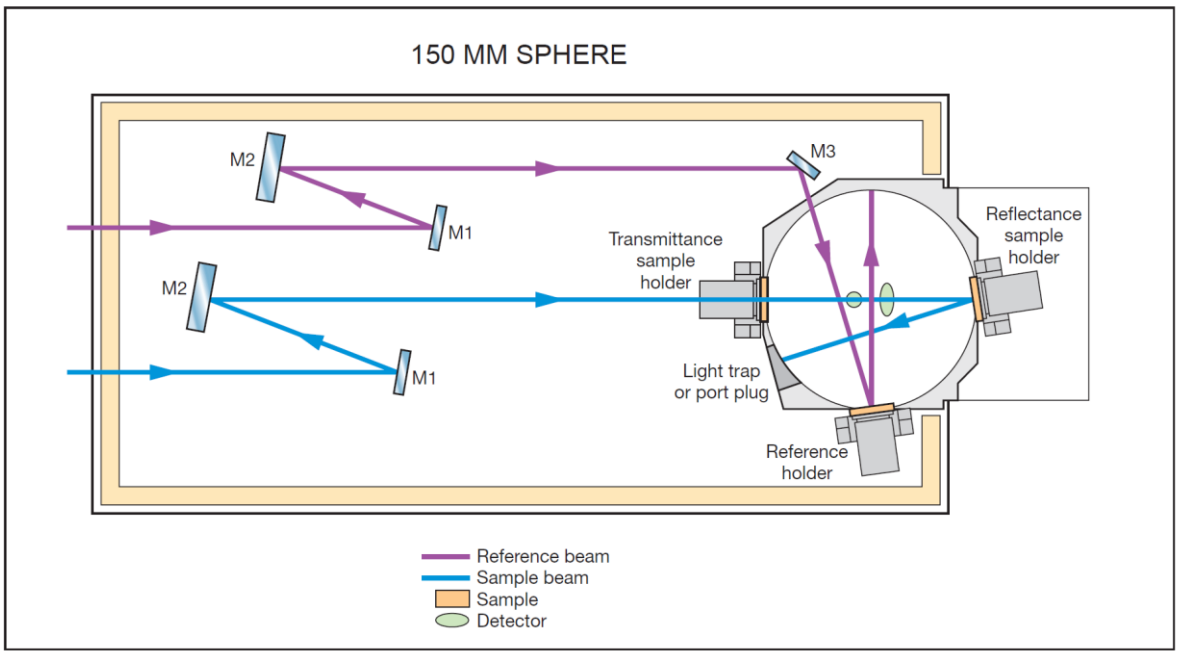


Figure 2.8 Schematic design of 150 mm integrating sphere[29]

3

Designed Fabrication Approaches

In this chapter, photolithography as a patterning technique is first introduced. Five approaches designed in this work based on photolithography technique are then illustrated. From the process point of view, all of them could give a successful patterning of the a-Si:H layers, but some of them still need more improvements from the passivation point of view. The flowcharts and corresponding description of different approaches will be discussed in different sections.

3.1. Patterning process of SHJ-IBC solar cells

Among all the involved processes of an SHJ-IBC solar cell fabrication approach, the patterning process is exclusively treated as the most imperative steps, in which the rear-side polarizations of the (doped) a-Si:H thin layers are patterned as is shown in *Figure 3.1*[30]

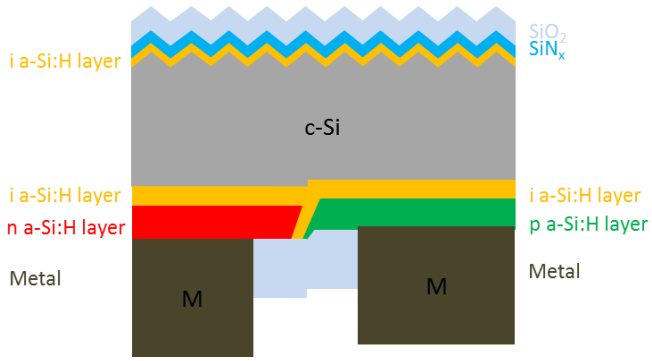


Figure 3.1: Schematic structure of SHJ-IBC solar cell

The traditional patterning process of IBC homo-junction solar cells is based on the diffusion doping, which needs a very high-temperature working environment. However, for amorphous silicon materials, higher temperature more than 200 °C is totally intolerable due to the themal stability of the a-Si:H layers. As a result, more restrictions and complexities are enclosed to the process to maintain the passivation properties of the amorphous silicon. This is also one of the reasons for the fact that patterning process holds the dominated cost of the SHJ-IBC solar cell device.

Due to such a great intricacy of the patterning process, any inaccuracy or contamination would have a certain impact on the performance of the solar cell. Even more, the stability of the performance of

SHJ-IBC in the long term, regardless of whether or not the cell is under illumination, is also influenced by the patterning process[31]. So, the quality of patterning should be ensured. To achieve this, several fundamental requirements should be meet[30]:

- Perfect accuracy and alignment of the pattern
- Maintaining of the passivation quality of SHJ structure
- No induced optical loss
- No induced resistive loss

Based on these imperative requirements, patterning techniques can be developed and several of them have been reported by different research teams recently. All these techniques can be generally divided into four categories: photolithography, ink-jet resist printing, shadow masking[32] and laser[33]. According to four criteria: Equipment cost, process equipment, typical resolution, and scalability, they are compared to each other and summarized in *Table 3.1*.

	Technology			
	Photo-lithography	Inkjet	Shadow-masking	LIFT/ LDW
Equipment costs	⊖⊖ (Contact-) Mask aligner	⊕ Printing tool	⊕⊕ Masking PECVD	⊖ Laser scribing tool
Process costs	⊖⊖ Wet-chemical, resist strip, and lift-off	⊖ Wet-chemical, lift-off	⊕⊕ Mask renewal, cleaning	⊕ Donor sub-strate prepara-tion
Typical feature-size	⊕⊕ $F \leq 1\,\mu m$	⊖ $F \leq 50\,\mu m$	⊖⊖ $F \leq 100\,\mu m$	⊕ $F \leq 10\,\mu m$
Mass-production/ Scalability	⊖ Parallel pattern-ing, mask overlay alignment	⊕ Serial pat-terning, print tool align-ment	⊖⊖ Parallel pattern-ing, mask overlay alignment during PECVD	⊕⊕ Serial process, no align-ment required

Table 3.1: Approximate comparison of the prevailing patterning techniques for SHJ-IBC solar cells (Double green plus corresponds superior competitiveness while double red minus means inferior competitiveness)[33]

Although the disadvantages of photolithography are evident considering its cost, this doesn't hinder its development at all. It can be found from the *Table 3.1* that photolithography technique has the smallest typical feature size, which is smaller than 1 µm. This means, with this technique, the accuracy of the whole process can be improved a lot and so does the final performance of the solar cell as well.

Given this big advantage and the equipment availability in TU Delft's Else Kooi Lab (EKL), we designed several potential fabrication processes via photolithography as a patterning technique for SHJ-IBC

solar cells. from the process point of view, all of them could give a successful patterning of the a-Si:H layers, but some of them still need more improvements from the passivation point of view. The corresponding flowchart and description of different approaches will be discussed in the following sections.

3.2. Approach 1- a-Si:H layer patterning with TMAH (1%) dip

In this approach, several techniques have been designed to ensure a high performance:

First, for the front side of the SHJ-IBC solar cells, random pyramids are introduced onto the front surface, which is a state-of-the-art technique to achieve light in-coupling and light scattering[34]. As a result, light enhancement is achieved by reducing the front surface reflection and increasing the light path length in the c-Si bulk. To further decrease the reflection at the front side, applying anti-reflection coating (ARC) to the surface is necessary[35]. As a result, SiN_X is deposited onto the textured surface, at the same time, the SiNx layer also acts as a passivation layer for the front surface. Before the SiNx layer deposition, an intrinsic a-Si:H layer is used to improve the front surface passivation[36]. The detailed passivation test result of this layer can be found in the appendix. The optimum J_0 value of the a-Si:H/SiNx layer passivation to the textured c-Si Surface is 10.5fA/cm^2.

Secondly, for the rear side of the solar cell in this approach, flat surface is kept to avoid the deterioration of the passivation induced by higher dangling bonds density of the textured surface. because of the different etching behaviours of emitter(a-Si:H(i)/a-Si:H(p)) and BSF(a-Si:H(i)/a-Si:H(n)), wet etching and dry etching are respectively employed to achieve the corresponding patterning of the emitter side and the BSF side on the back surface. To be specific, TMAH (1%) is used as a wet etchant to get rid of the a-Si:H(i)/a-Si:H(n) layers where the emitter locates and hydrogen plasma dry etching is used to etch away the a-Si:H(i)/a-Si:H(p) layers where the BSF locates. It is worthwhile to mention that, to protect the a-Si:H(i)/a-Si:H(p) layers on the emitter side from being etched, an intrinsic a-Si:H layer is deposited on top of the p-type a-Si:H layer as an etching barrier.

3.2.1. Fabrication flowchart of approach 1

About the fabrication flowcharts shown in this thesis, some points should be clarified in advance to smooth the recognition and understanding. First, all the structures shown in the flowchart are upside down so that more attention can be paid to the rear-side surface treatment. This means that the bottom of these structures is where the front side of the cell locates. The top of these structures is the rear side of the solar cells. Secondly, the solid rectangle represents the main step while the transparent rectangle represents the auxiliary step, like cleaning step.

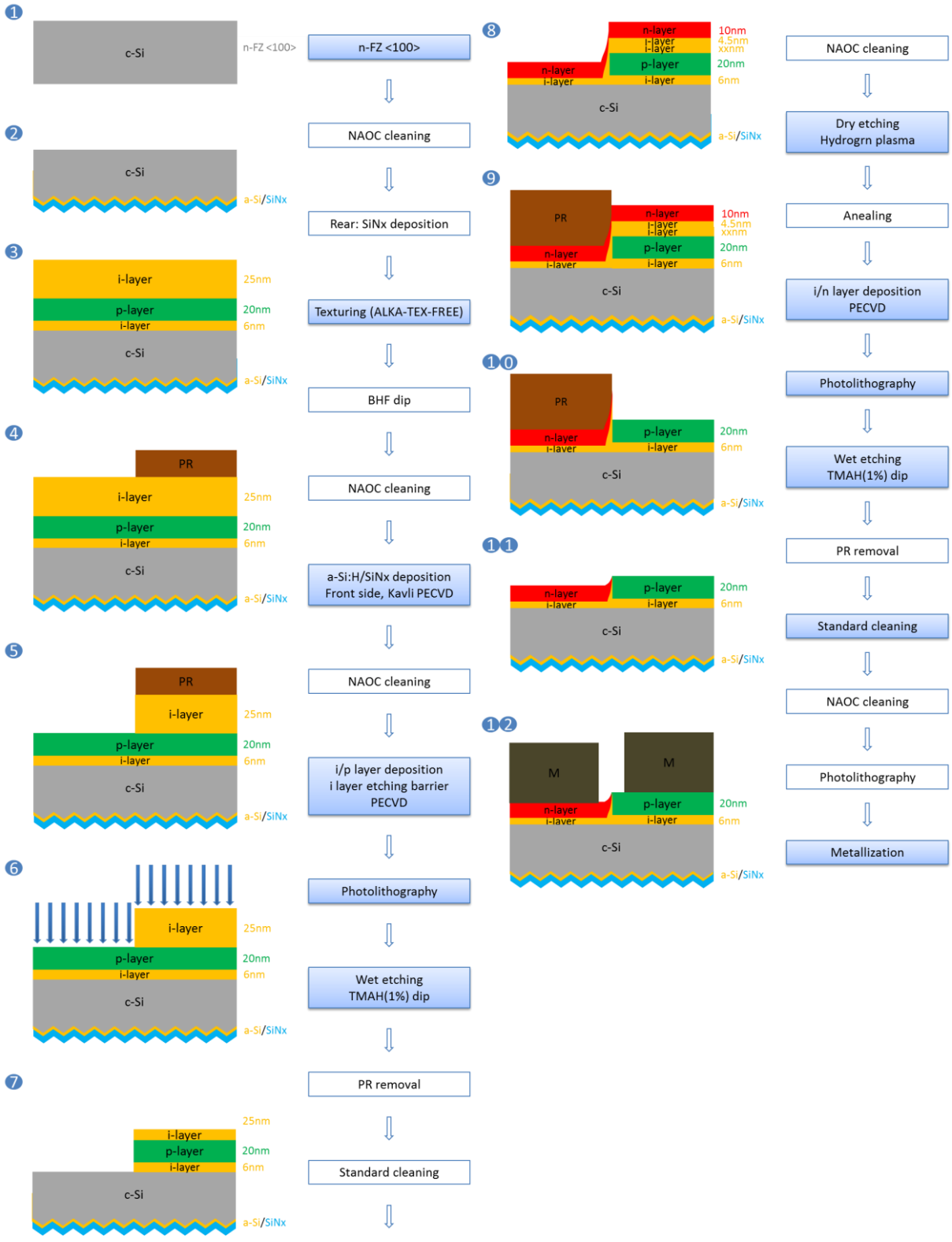


Figure 3.2 Fabrication flowchart of Approach 1: intrinsic a-Si:H as dry etching barrier

Figure 3.2 shows the fabrication procedures of Approach 1. Step 1, the Float Zone (FZ), n-type, <100> oriented, 285µm monocrystalline silicon wafer is prepared as a substrate, and then, NAOC cleaning is performed to remove the possible organic and metal contamination on the wafer. The back surface is then covered by SiN_X to prevent itself from being textured in the following texturing step. The

texturing step is realized in the TMAH (5%, 80°C, ALKA-TEX-FREE) solution. After that, the texturing protection layer SiN_X on the back surface is removed by being dipped into the BHF solution. Step 2, a-Si:H(i)/SiN_x layers are deposited onto the front side as passivation and anti-reflection layers, after the previously mentioned cleaning steps. It's worthwhile to mention that this a-Si:H/SiN_x layer should be deposited at the beginning of the process because of the high-temperature requirement deposition. Otherwise, the passivation properties of the pre-deposited a-Si:H layers on rear side in the emitter and BSF would suffer a lot from this high temperature. Later, NAOC cleaning is performed again as a pre-treatment cleaning step before the a-Si:H deposition. Step 3, a-Si:H(i)/a-Si:H(p)/a-Si:H(i) layers are deposited consecutively on the back surface by PECVD, in which the last deposited a-Si:H(i) layer works as an etching barrier to the later dry etching.

Step 4-5, the first photolithography step and subsequent wet etching (TMAH, 1%) are performed to etch the top a-Si:H(i) layer where the BSF locates. The etching stop mechanism is applied here, where the TMAH(1%) solution, as an alkaline etchant, has a very low etching rates for a-Si:H(p) layer[30]. This will be illustrated later in the next section. Now, a-Si:H(i)/a-Si:H(p) layer stack at the BSF side is exposed and ready for the dry etching. Step 6-7, after the removal of photoresist and cleaning steps, hydrogen plasma dry etching can be used to remove the exposed part of a-Si:H(i)/a-Si:H(p) layer. due to a thicker a-Si:H etching barrier on top of the emitter area, the thickness of emitter is not affected. It is then followed by an annealing step in the same PECVD chamber without breaking the vacuum. Step 8, BSF is formed by the a-Si:H(i)/a-Si:H(n) layers deposition, being achieved as well by PECVD. Step 9-10, in order to remove the a-Si:H(i)/a-Si:H(n) layers and the rest of the a-Si:H(i) etching barrier layer on top of the emitter, another photolithography step and the subsequent wet etching (TMAH, 1%) step are needed. Due to the etching selectivity of TMAH to p-type a-Si:H layer, the etching is landed on the p-type a-Si:H emitter.

Step 11, the photoresist is removed and standard cleaning is performed to ensure a clean back surface before the metallization. Step 12, finally, the photolithography lift-off technique is also adopted here for the metallization of the solar cell.

3.2.2. Etching techniques and their influence on the passivation

It can be easily observed that, during the whole process of this approach, several kinds of etching techniques are employed to achieve the patterning, for example in step 5 and step 10, TMAH (1%) is employed to etch a-Si:H(i)/a-Si:H(n) layers and in step 6, hydrogen plasma is used to etch a-Si:H(i)/a-Si:H(p) layers. So, the investigations were done on their etching behaviours and the influences on the passivation properties of the BSF and emitter.

3.2.2.1. Wet etching via TMAH

In this approach, wet etching via TMAH is used to etch a-Si:H(i)/a-Si:H(n) layers while p-type a-Si:H layer stays unetched (Step 5 and Step 9). Because of such an etching behavior, the patterning of the emitter (step 10) can be realized. In this subsection, we first tested the etching rate of TMAH (1%) and then the feasibility of alternative etchant: developer MF322. At the end, the influence of TMAH on passivation is tested.

Etching rate and selectivity test

As mentioned before, TMAH(1%) as an alkaline etchant, has a good selectivity for a-Si:H(p) layer[37]. To control the dipping time of etching, the accurate etching rate of TMAH (1%) to intrinsic and n-type

a-Si:H layers should be tested. Also, the selectivity p-type a-Si:H should be investigated. So, the following experiment was doped out: intrinsic a-Si:H, n-type a-Si:H and p-type a-Si:H with certain thickness were deposited on the test wafer. All of them were dipped into TMAH (1%) solution for 2 min. The thickness before etching and after etching was measured with Spectroscopic Ellipsometry so that the respective etching rate can be calculated out. The results are presented in *Table 3.2*.

Table 3.2 Etching rate of p-type, intrinsic, and n-type a-Si:H layers in TMAH (1%)

Sample	Thickness before etching [nm]	Thickness after etching [nm]	Etching time [min]	etching rate [nm/min]
p-type	33.5	32.2	2	0.65
intrinsic	19.8	13.04	2	3.38
n-type	33.91	25.86	2	4.025

The etching time used in the etching process, shown in Fig. 3.2, now can be calculated according to the thickness of a-Si:H(i)/a-Si:H(n) layers. Due to the remains of etching barrier layer, the etching time can be extended slightly to make sure all the layers on top of the a-Si:H(p) layer are removed. From the table, it can also be observed that TMAH (1%) does have a good selectivity for p-type a-Si:H layer because of the quite lower etching rate due to its lowly doping, compared to those of intrinsic and n-type a-Si:H layers.

Developer MF322

During the photolithography step, it was found that the developer MF322 is made up of TMAH. So, it can be expected that the developer MF322 can also be used to etch away the i/n layer as long as the dipping time is optimized. This means no additional etching step is needed only if the wafer is dipped longer during the development step of photolithography. So, the same experiments were performed to get the etching rate of intrinsic and n-type a-Si:H layers in developer MF322.

Table 3.3 Etching rate of intrinsic and n-type a-Si:H layers in developer MF322

a-Si:H	Thickness before etching [nm]	Thickness after etching [nm]	Etching time [min]	etching rate [nm/min]
Intrinsic	35.30	25.27	4	2.5
n-type	35.48	25.48	4	2.5

Table 3.3 shows that the etching rate of intrinsic and n-type a-Si:H layers are the same, 2.5nm/ min, which is applicable for wet etching. However, another issue worth considering is that, due to the longer development time, the unexposed part of the photoresist (positive) may not be able to bear with the developer anymore and even start falling off. Consequently, the finger formation of IBC is deteriorated because of the absence of top photoresist as a protection layer during the etching process. The microscopic image *Figure 3.3* provides the evidence for such damage to the photoresist.

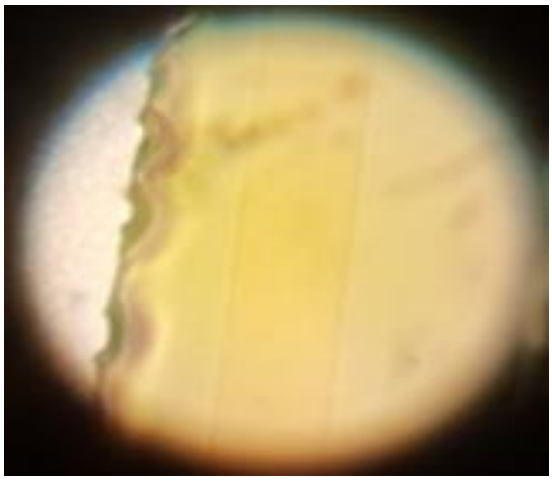


Figure 3.3 microscope picture of Finger of the photoresist after over development.

However, it was found that longer baking before the development can help the wanted part of photoresist stand longer in the developer.

Passivation property of a-Si:H layers after TMAH (1%) dip

In order to investigate the passivation quality, the lifetime of the a-Si:H layers after the patterning process should be measured. In this work, the symmetric test samples were measured by Sinton WCT-120 Lifetime Tester to get the lifetime. For example, in Step 10, to investigate the influence of the extra dip in TMAH (1%) on the a-Si:H(p) layer surface passivation after the removal of top a-Si:H(i)/a-Si:H(n) layers, a stack of Si:H(i)/a-Si:H(p) layer with the same respective thickness as that of the emitter in solar cell was deposited on both sides of a c-Si surface. Then it was dipped into TMAH (1%) solution for a certain short time to simulate the extra dip condition. The lifetime before and after the dip was measured as shown in *Table 3.4*. It was decreased drastically. However, according to the report by some research team[32], TMAH(1%) they employed didn't cause such a passivation problem. This means that more improvements should be figured out since etching is a very complicated process involving several factors: temperature, concentration and etching time.

Table 3.4 Lifetime change of a-Si:H(i)/a-Si:H(n) and a-Si:H(i)/a-Si:H(p) layers after TMAH (1%) dip

Sample	Lifetime before etching [μs]	Lifetime after etching [μs]
a-Si:H(i) 6nm /a-Si:H(p) 6nm	1047	64
a-Si:H(i) 6nm /a-Si:H(n) 10nm	2614	123

3.2.2.2.Dry etching (a-Si:H(i)/ a-Si:H(p) layers etching)

In this approach, Given the fact that TMAH cannot get rid of a-Si:H(i)/a-Si:H(p) layers, dry etching via hydrogen plasma is used to etch a-Si:H(i)/a-Si:H(p) layers in step 6. Because of this, the patterning of the BSF (step 6-10) can be realized. Actually, dry etching is one of the most prevailing techniques to etch semiconductor surface in the industry[38]. The basic idea behind this is that lots of hydrogen atoms provided by plasma have many complex reactions with the a-Si:H surface, such as Addition, Abstraction, Insertion and Etching, leading into the breaking and formation of bonds. The etching happens when the etching reaction dominates [39]. In this subsection, we first tested the etching rate of hydrogen plasma dry etching and then the influence of dry etching on passivation is tested.

Etching rate

Under certain conditions with fixed parameters, like RF power, temperature, and pressure, the etching rate of a-Si:H by hydrogen plasma is constant and nearly independent of etching time[40]. This property gives the advantage that this dry etching process can be controlled by controlling the etching time. So, it's important to test this etching rate under the certain plasma condition so that the precise etching time of Si:H(i)/a-Si:H(p) layers at the BSF side can be achieved by calculation. Also, according to this etching time and the etching rate of intrinsic a-Si:H layer, the thickness of the etching barrier in step 3 at the emitter side can be determined.

The etching rate test experiment went as follows. Intrinsic a-Si:H and p-type a-Si:H layers with thickness around 20-30 nm were deposited on the test wafer. These samples subsequently went through the hydrogen plasma exposure under different conditions. The accurate thickness before etching and after etching of these samples was measured. At the end, the most applicable etching rate was selected out and the plasma condition of this etching rate was adopted. These selected etching rates and plasma conditions can be found in*Table 3.5* and more testing results can be found in Appendix.

Table 3.5 Selected etching rate of intrinsic and p-type a-Si:H layers

Sample	H_2 [sccm]	Pressure [mbar]	RF Power [W]	Etching rate [nm/min]
Intrinsic	200	2.5	6	2.32
p-type	200	2.5	6	1.21

Uniformity

Another important characteristic parameter of the etching process is its uniformity. A good uniformity can guarantee a better uniform formation of IBC patterning on the rear. The testing experiment was performed as follows. The a-Si:H layer with thickness around 16 nm was deposited onto a glass substrate, and then, the hydrogen plasma etching was performed. The thickness before and after etching on the substrate was measured. The measurements were taken on 9 different positions of the sample, 10x10 cm^2 in area see *Figure 3.4*. By comparing the etched thickness of these locations, one can easily get the uniformity of this etching process.

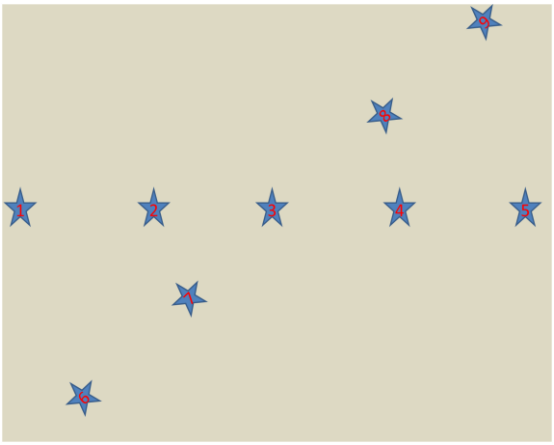


Figure 3.4 thickness measurment locations on the 10x10 cm^2 glass substrate

The testing results show a decent uniformity with the standard deviation of 0.57nm for the average etched thickness of 5.8nm. The detailed experimental data can be found in the appendix.

Passivation Si:H(i) 6nm /a-Si:H(p) layers after dry etching

However, hydrogen plasma etching may bring damage to the passivation of the a-Si:H/c-Si inter surface because of the ion bombardment[41]. So, the passivation test was performed. The Si:H(i)/a-Si:H(p) layers were deposited onto the both sides of the test wafer. Part of the p layer was etched away by 2 min hydrogen plasma etching. Then one hour of annealing was followed in the same chamber under the same condition without hydrogen plasma. The lifetime before etching, after etching, and after annealing were measured and shown in *Table 3.8Table 3.6*.

Table 3.6 Lifetime before etching, after etching and after annealing

Sample	Lifetime [μs]	Jo [FA/m2]	iVoc [V]
Si:H(i) 6nm /a-Si:H(p) layer 8nm	802	16.4	0.682
Hydrogen plasma etching 2min	200	15	616
Annealing 1 hour	503.13	20.3	0.671

It can be observed that the hydrogen plasma etching does bring damage to the passivation of a-Si:H/c-Si intersurface. However, it seems that 1 hour annealing under the same condition without hydrogen plasma can partly restore this damage. What's more, compared to the original lifetime, the loss of the lifetime after the 1 hour annealing under the same condition without hydrogen plasma may also be partly attributed to the result of the decreasing thickness of the a-Si:H(p) layer, which leads to the decrease of field effect passivation. So, the real value of the damage brought by hydrogen plasma is even less.

3.2.3. Summary

In this approach, it is found that TMAH shows good selectivity for a-Si:H(p) layer, but a lower lifetime for the passivation of emitter was found after TMAH dip. The dry-etching seems to be a good solution for the a-Si:H(p) layer etching for its decent etching rate (around 2 nm/min) and uniformity. The damage caused by hydrogen plasma is decreased a lot after 1 hour annealing under the same condition without hydrogen plasma. In Approach 3, when dry etching is applied again, an SiO_2 layer is applied as an etching barrier to minimize the induced damage.

3.3. Approach 2 - a-Si:H layer patterning with NAOC etching

In the last approach, a lower lifetime for the passivation of emitter was found after TMAH dip. To achieve a better passivation quality in this approach, some other wet etching methods should be applied to replace the TMAH. In addition, to simplify the process and minimize the induced process contamination, the possibility of cancelling the photolithography step for BSF patterning should be researched. Based on these ideas, Approach 2 is put forward. Some of the new methods are illustrated as follows:

First, instead of using TMAH (1%) solution as an etchant for the Si:H(i)/a-Si:H(n) layers, NAOC was adopted in this approach, and also, only the top n-type a-Si:H layer needs to be removed, while the bottom intrinsic a-Si:H layers is kept to be shared with the p-type a-Si:H layer at the emitter side.

Secondly, the Tunnel Recombination junction (TRJ) technique from multijunction solar cells[42] is applied here at the BSF side. This will be illustrated in detail in the next section.

Thirdly, interdigitated textured back surface is applied here to expect the increase of scattering of the reflected light at the back surface. An interdigitated textured wafer is made by rinsing the sample into the TMAH (5%, 80°C, ALKA-TEX-FREE) solution with emitter/BSF side covered by SiN_X as a protection layer. As a result, the surface of the sample except the covered area get textured.

Last, the SiO_2 as an etching barrier here was employed to prevent the underneath Si:H(i)/a-Si:H(n) layers from being etched.

3.3.1. Fabrication flowchart of Approach 2

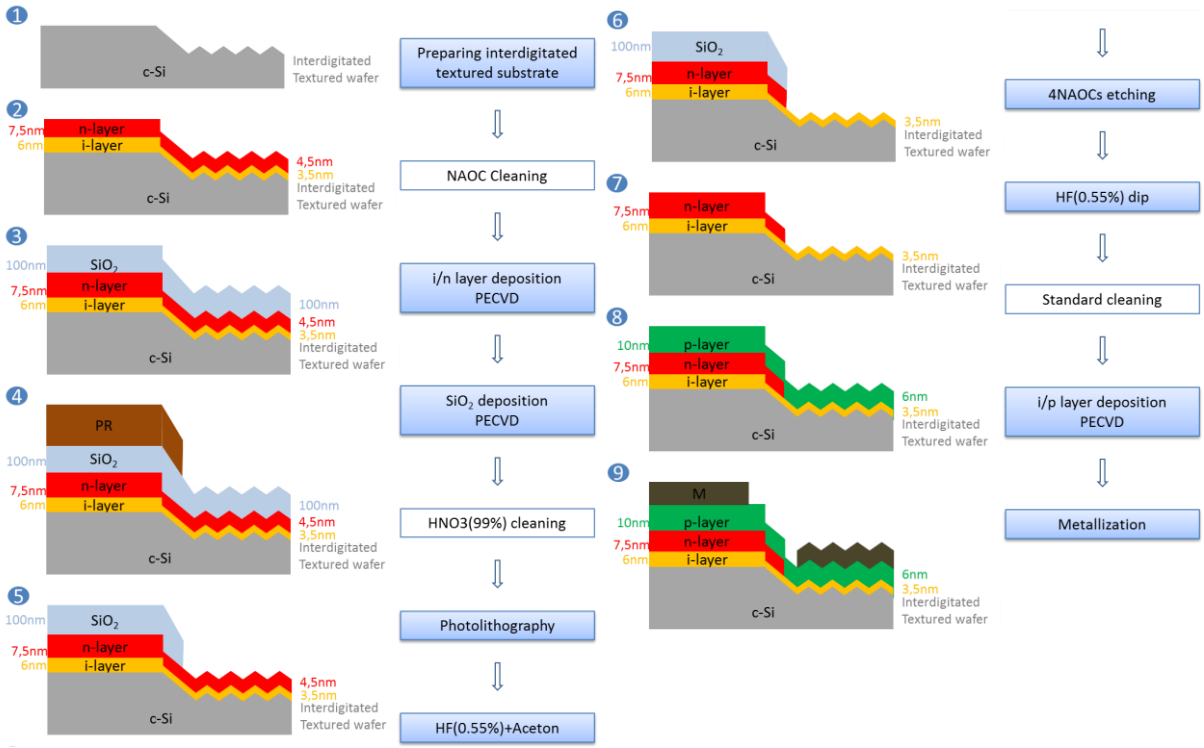


Figure 3.5 Fabrication flowchart of Approach 2

Figure 3.5 shows the fabrication procedures of Approach 2. Step 1, the Float Zone (FZ), n-type, <100> oriented, 285µm monocrystalline silicon interdigitated textured wafer is prepared as a substrate, and

then, NAOC cleaning is performed to remove the possible organic or metal contamination on the wafer as a pretreatment cleaning step before deposition. Step 2-3, a-Si:H(i)/a-Si:H(n) layers are deposited onto the back surface, followed by the deposition of the SiO_2 layer as an etching barrier.

The SiO_2 layer here is very important. Photoresist is normally used as a cover to protect the layers underneath. However, the photoresist, as an organic material, cannot bear with the high temperature in PECVD. The introduction of the SiO_2 layer can solve this problem. With the help of SiO_2, the lower deposition temperature restriction which is imposed by the photoresist can be avoided here.

Step 4-5, the photolithography step was performed and the SiO_2 at the emitter side is removed by HF (0.55%) dip. Step 6, the n-type a-Si:H layer at the emitter side is etched by several NAOCs after the removal of photoresist. Step 7-8, p-type a-Si:H layer is deposited after the removal of SiO_2 layer by HF (0.55%) dip. Now, the emitter (Si:H(i)/Si:H(p) layers) is formed. At the same time, a Tunnel Recombination junction (TRJ), a-Si:H(i)/Si:H(n)/Si:H(p) triple layers stack at the BSF side, is also formed. Step 9, at the end, the fabrication process is finalized by metallization.

3.3.2. Testing of involved techniques

In the flowchart of this approach, several techniques are employed to achieve the patterning; (1) in Step 6, the application of low temperature PECVD SiO_2 etching barrier layer (2) in step 7, NAOC as an etchant for the n-type a-Si:H layer (3) in Step 8, the application of Tunnel Recombination junction (TRJ). So, the corresponding investigations should be done to validate this approach: (1) the influence of SiO_2 layer deposition on the passivation properties of the BSF, (2) the etching rate of NAOC etching and its influence on the c-Si/a-Si:H interface passivation properties.

3.3.2.1. Test the influence of SiO_2 as an etching barrier

The SiO_2 layer is applied in this approach as an etching barrier in step 6. However, the influence of the SiO_2 layer on the surface passivation of underlying a-Si:H(i)/a-Si:H(n) layers needs to be tested. in order to obtain this information: first, a-Si:H(i)/a-Si:H(n) layers were deposited onto the wafer on both sides. A layer of SiO_2 was then deposited onto the both sides as well. Last, they were removed by the HF (0.55%) solution to simulate the same procedures in the real solar cell fabrication process. The lifetime of the sample was measured after each of the previous step. The results are shown in *Table 3.7*. The measurement shows that adding SiO_2 and then removing it with HF doesn't induce any damage to the surface passivation. The good passivation result in *Table 3.7* with SiO_2 on top of a-Si:H(i)/a-Si:H(n) layer also proves that SiO_2 can work as a good passivation layer[43].

Table 3.7 Lifetime change during the SiO_2 deposition and removal

Sample	Lifetime [µs]	Jo [FA/m2]	iVoc [V]
a-Si:H(i)/a-Si:H(n) layer	2803.96	25.5	0.689
a-Si:H(i)/a-Si:H(n) layer + SiO_2	3326.04	22.1	0.697
a-Si:H(i)/a-Si:H(n) layer + SiO_2 + HF dip	2726.31	25.5	0.689

3.3.2.2. NAOC

Nitric Acid Oxidation Circle(NAOC), as a wet cleaning method, has been widely used in PVMD group to treat the c-Si substrate. The NAOC procedures are developed based on the Nitric Acid Oxidation

of Silicon (NAOS) [44]. First, HNO_3(99%) at the room temperature is used to get rid of the organic contamination as a preparation step. Then, the sample is dipped into the HNO_3 (69%) at 110 °C to remove the metal contamination, followed by the removal of the generated silicon oxide layer which is realized with the HF (0.55%) solution at room temperature. This is one circle so far. in order to simplify the process, the next circle starts right from the HNO_3 (69%) at 110 °C and then the removal of oxides are repeated [45]. The whole procedures can be found in *Figure 3.6* (2 NAOC circles). This cleaning method can also be used as an etching technique because the silicon on the surface is etched away around 1.1 nm for each circle. The NAOC is a self-limiting process, with each NAOC, a 1.5nm thick SiO2 is formed which consumes around 1.1nm c-Si material[45].As a result, the NAOC method can provide a precise etching process.

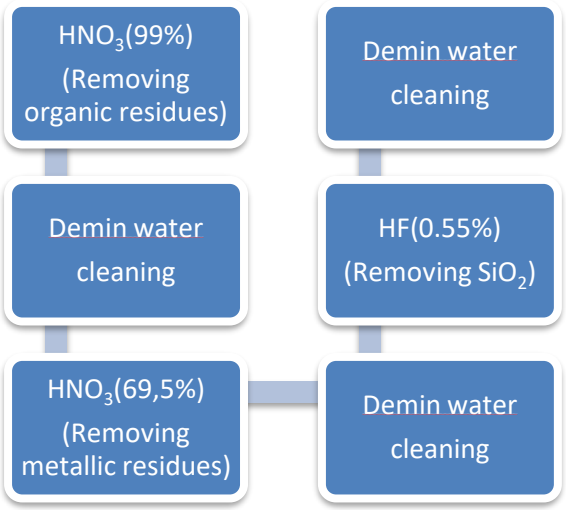


Figure 3.6 Nitric Acid Oxidation Circle procedures

Etching rate of n-type a-Si:H with NAOC

As illustrated in the flowchart, NAOC etching is employed in this work (Step 7). The etching rate was tested by the following experiment: n-type a-Si:H layer with certain thickness was deposited on the test wafer. Three NAOCs were implemented on the sample. The Thickness before and after the NAOC etching was measured. The etching rate can be calculated out, which is 1.3nm/circle. The detailed experimental data can be found in Appendix-3 .

Passivation of the formed emitter by NAOC etching

In the real cell structure, the p-type a-Si:H layer will be deposited after the removal of the n-type a-Si:H layer on the emitter area (Step 8). The passivation of the formed a-Si:H(i)/a-Si:H(p) stack(emitter) will be investigated in this subsection. The testing experiment was done as follows. The a-Si:H(i)/a-Si:H(n) layers with the same respective thickness (3.5nm for intrinsic a-Si:H layer and 4.4 nm for n-type a-Si:H layer) as the real solar cell was deposited onto the double sides of the test wafer to do a symmetric test. 4 NAOCs were performed to ensure that the whole n-type a-Si:H layer，4.4nm thick on textured surface， was etched away. Then, the same p-type a-Si:H layer as those of the real solar cells (6nm p-type a-Si:H layer) were deposited onto the both sides of this sample. The lifetime before etching and after p-type a-Si:H layer deposition were measured. The results are shown in *Table 3.8*.

Table 3.8 Lifetime before NAOC etching and after p-type a-Si:H layer deposition

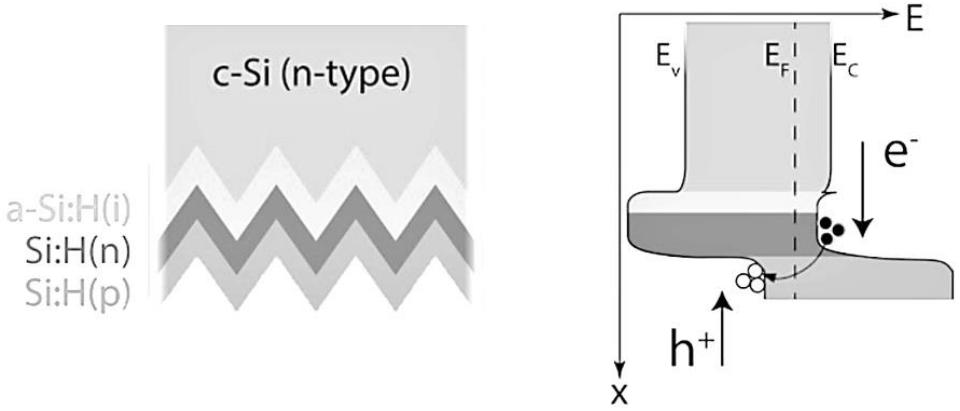
Sample	Lifetime [μs]
a-Si:H(i, 3.5nm)/a-Si:H(n, 4.4nm) layer	1411
a-Si:H(i, 3.5nm)/a-Si:H(n, 4.4nm) layer+4NAOCs+ a-Si:H(p, 6nm) layer	49

The passivation drops after the above-mentioned processes may come from a few possible aspects: (1) The previous SiO_2 deposition and removal steps would do damage to the surface passivation. However, this has been ruled out in the previous section. (2) The passivation of a-Si:H(i)/a-Si:H(p) layers are inherently not good compared to a-Si:H(i)/a-Si:H(n) layers. However, such a low passivation property is unacceptable for a solar cell process. This indicates that some kinds of defects must have been caused by the NAOC etching.

3.3.2.3. Tunnel Recombination junction (TRJ)

In this approach, after the step 8, deposition of p-type a-Si:H layer, the Tunnel Recombination junction (a-Si:H(i)/a-Si:H(n)/ a-Si:H(p) stack) will be formed in the BSF area. The working principle of this junction can be illustrated by the band diagram shown in *Figure 3.7*. Tunnel Recombination junction (TRJ) has been largely researched and exploited in the regime of multijunction solar cells. Examples can be found from other research in PVMD group[42]. This technology was applied to SHJ-IBC solar cell for the first time by the research team from KAUST Solar Centre (KSC) [46].

To realize the efficient TRJ in the SHJ-IBC, several requirements should be fulfilled, such as low resistance tunnel junction at the interface of a-Si:H(n)/a-Si:H(p) layers and high passivation to the c-Si surface. Also, in this approach, to prevent the shunt happening in the p-type a-Si:H layer between BSF and emitter, the lateral conductance of the p-layer should be kept low.



(a) (b)

Figure 3.7 (a) Schematic structure of tunnel recombination junction (b)band diagram of tunnel recombination junction[46]

3.3.3. Summary

To sum up, it is proven that SiO_2 as an etching barrier does not induce any damage to the surface passivation of a-Si:H(i)/a-Si:H(n) layers. The lifetime before deposition of the SiO_2 (2804 μs) and after removal of the SiO_2 (2726 μs) are almost the same. However, the passivation quality of NAOC etching in this approach still needs more investigation, with an decrease of lifetime from 1411 μs to 49 μs. In

addition, to finish this approach, more research should be done on the application of the *tunnel recombination junction*.

3.4. Approach 3 - a-Si:H layer patterning with NAOC etching

In the last two approaches, a lower lifetime for the passivation of emitter was found after TMAH dip and NAOC etching. To achieve a better passivation quality in this approach, some other etching methods should be applied. Based on this idea, Approach 2 is put forward. Some of the new methods are illustrated as follows:

First, instead of using TMAH (1%) solution as an etchant for the Si:H(i)/a-Si:H(n) layers, poly etch (HNO_3 (69%): HF (40%) = 70:1) is introduced in this approach.

Secondly, double side textured wafer surfaces are used for both emitter and BSF in this approach. As a result, the double side textured substrate can further imcrease the scattering of reflected light at the back surface.

Thirdly, dry etching is employed again to etch a-Si:H(i)/a-Si:H(p) layers. However, unlike what we did in approach 1, SiO_2 is selected as an etching barrier to dry etching according to its good passivation performance observed in Approach 2.

3.4.1. Fabrication flowchart of Approach 3

Figure 3.8 shows the fabrication procedures of Approach 3. Step 1-2, Float Zone (FZ), n-type, <100> oriented, 285µm monocrystalline silicon wafer is double side textured to be prepared as a substrate, before which the alignment marker for photolithography should be made and protected by SiN_X layer at the rear side of the substrate. Step 3, NAOC cleaning is performed to remove the possible organic or metal contamination on the wafer as a pretreatment cleaning step for a-Si:H/SiN_x deposition. Step 4, after this front passivation and antireflection layers deposition, the substrate experiences a-Si:H(i)/a-Si:H(n) layers deposition. The standard cleaning steps should be performed in between. Step 5, SiO_2 is deposited onto the a-Si:H(i)/a-Si:H(n) stack as an etching barrier to protect part of the a-Si:H(i)/a-Si:H(n) layers at the BSF side. Step 6-7, photolithography and HF (0.55%) dip are performed to expose the a-Si:H(i)/a-Si:H(n) layers at the emitter side, followed by the removal of photoresist. Step 8, the exposed part of a-Si:H(i)/a-Si:H(n) layers are etched away by poly etch, followed by standard cleaning and NAOC cleaning. Step 9-10, a-Si:H(i)/a-Si:H(p) layers and SiO_2 are deposited one after another. Step 11-12, after the HNO_3 (99%) cleaning to remove the possible contamination during the transport, another photolithography step and HF (0.55%) dip are performed to expose part of the a-Si:H(i)/a-Si:H(p) layers at the BSF side, while the other part of a-Si:H(i)/a-Si:H(p) layers, working as an emitter, are still protected by SiO_2. The photoresist is then removed. Step 13-14, hydrogen plasma is performed to remove the exposed part of a-Si:H(i)/a-Si:H(p) layers, followed by HF (5.5%) dip to remove the SiO_2 protection layer. Step 15, Metallization is finally implemented at the back surface.

Figure 3.8 Fabrication flowchart of Approach 3

3.4.2. Testing of involved techniques

In the flowchart of this approach, several new techniques are employed to achieve the patterning. So, the corresponding investigations should be done to validate this approach.

3.4.2.1.Poly etch

In this approach, poly etch is employed to etch away a-Si:H(i)/a-Si:H(n) layers (Step 8). Poly etch is actually a mix of HNO_3 (69%) and HF (40%) with the ratio of 70:1. HNO_3 (69%) provides the oxidation reaction, while HF(40%) provides oxide dissolution reaction. As a result, the combined reaction rate depends on the concentration ratio of each acting reactant[47]. This is illustrated in *Figure 3.9*, where Area 1 represents the oxidation-limiting area and Area 2 represents dissolution area. As to poly etch, it is located in the extreme dissolution area, where the reaction rate is far slower, around 1 nanometre per second (the testing experimental data can be found in the Appendix). Such a low etching rate brings the controllable and less defects-induced process.

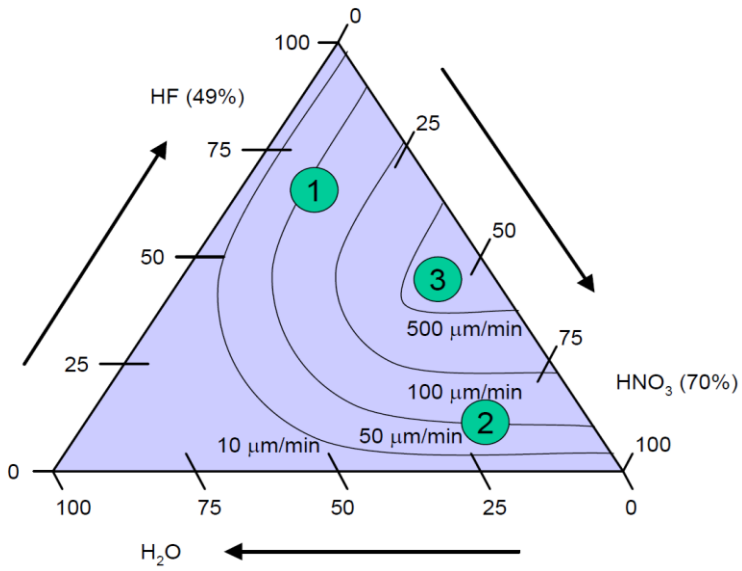


Figure 3.9 Etching rate of the etchant combination: HNO_3+HF+H_2O

Passivation of the formed emitter by poly etch

In Step 8, instead of using TMAH (1%) solution as an etchant for the Si:H(i)/a-Si:H(n) layers, poly etch was adopted and expected to solve the passivation problem. So, the following experiment was implemented to totally simulate the situation in the real solar cell fabrication process. After NAOC cleaning, the same a-Si:H(i)/a-Si:H(n) layers (4.5nm intrinsic a-Si:H and 10 nm n-type a-Si:H) as that of the real solar cell was deposited onto the both sides of the test wafer. Then, the sample was dipped into the poly etch solution for 3 min to make sure that all the a-Si:H layers could be removed. Then, NAOC cleaning steps were performed again. After that, the sample experienced another deposition of a-Si:H(i)/a-Si:H(p) layers on both sides (6nm intrinsic a-Si:H and 8 nm n-type a-Si:H). Again, they are identical to the real ones in the solar cell. The lifetime after this deposition was measured and compared to the reference sample, where a stack of a-Si:H(i)/a-Si:H(p) layers was directly deposited onto the sample wafer without any extra step. In addition, the same experiment was done for TMAH (1%) etching for comparison. These results have been presented in *Table 3.9*. Here, to be mentioned is that the passivation of a-Si:H(i)/a-Si:H(p) layers here was not good due to the maintenance of the Amor.

Table 3.9 Passivation of formed emitter by poly etch and TMAH

Sample	Procedure	Lifetime [µs]	J_o [FA/m2]	iVoc [V]
Poly etch	a-Si:H(i) /a-Si:H(n) + poly etch + a-Si:H(i) /a-Si:H(p)	235.4	226	0.636
TMAH	a-Si:H(i) /a-Si:H(n) + TMAH + a-Si:H(i) /a-Si:H(p)	60.83	990	0.605
Reference	a-Si:H(i) /a-Si:H(p)	236	132	0.638

It can be observed in *Table 3.9* that the sample experienced Poly etch dip exhibits a far better passivation quality than the one with TMAH dip. Even compared to the passivation quality of the reference sample, the poly etch sample shows a similar performance. The increase of the J_o may come from the too long dip of Poly etch, which results in damage to the c-Si substrate surfaces. This can be further illustrated by the appearance of Nanoroughness on the surface observed by SEM, shown in *Figure 3.10*.

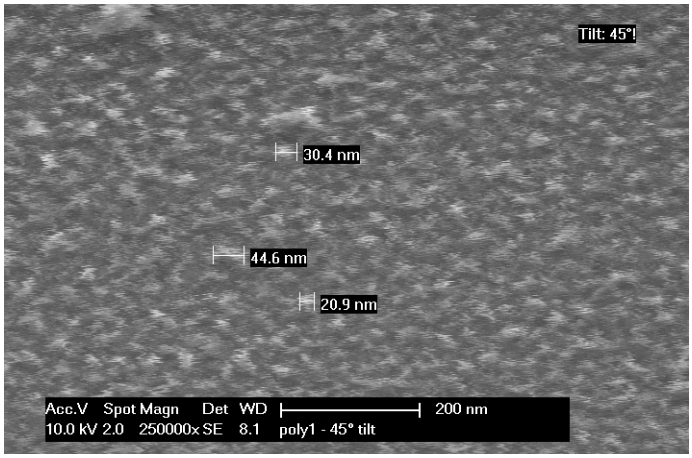


Figure 3.10 Appearance of Nanoroughness after long poly etch dip

3.4.2.2.SiO_2 as an etching barrier to the dry etching of a-Si:H layers

In this approach, dry etching is employed again to get rid of the a-Si:H(i)/a-Si:H(p) layers on top of the SiO_2 in Step 12. To test if the SiO_2 layer can protect the underneath BSF (a-Si:H(i)/a-Si:H(p) layers) and its passivation, the following experiment was done: after the NAOC cleaning, the same a-Si:H(i)/a-Si:H(n) layers (4.5nm intrinsic a-Si:H and 10 nm n-type a-Si:H) as that of the real solar cell was deposited onto both sides of the test wafer. Then, 500 nm SiO_2 and a-Si:H(i)/a-Si:H(p) layers (6 nm intrinsic a-Si:H and 10 nm n-type a-Si:H) were deposited. Next, hydrogen plasma dry etching was performed to remove the just deposited a-Si:H(i)/a-Si:H(p) layers. In the end, the SiO_2 was removed by HF (0.55%) dip. The lifetime before the SiO_2 deposition and after the removal of the SiO_2 layer was measured and compared, as is shown in *Table 3.10*.

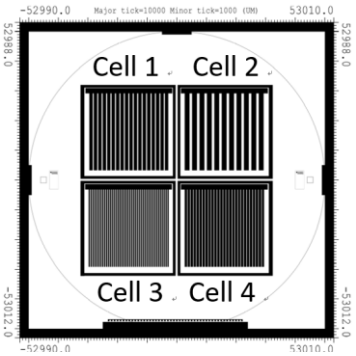
Table 3.10 Lifetime change of a-Si:H(i) /a-Si:H(n) layers during the dry etching (SiO_2 as etching barrier to dry etching)

Sample	Lifetime [µs]	J_o [FA/m2]	iVoc [V]
a-Si:H(i) /a-Si:H(n)	2371.30	26.67	0.69
a-Si:H(i) /a-Si:H(n)+ SiO_2+ a-Si:H(i)/a-Si:H(p)+Dry etching+HF dip	3338.61	24.3	0.697

The lifetime increased after the series treatment of deposition and etching. This means SiO_2 works perfectly as an etching barrier. Even more, it presumably restores the defects on the interface of a-Si:H layers when the sample is under the condition of hydrogen plasma with high temperature. This may be the explanation of the increase of lifetime.

3.4.3. Summary

In this approach, all the techniques have been proved feasible. However, in the fabrication process, when it came to the photolithography step before metallization, lots of contamination was introduced during the process. The passivation before the metallization was measured and shown in*Figure 3.11*. Due to the low lifetime the wafers were not finished with a solar cell.



Cell	Lifetime(us)	J_o(FA/cm^2)	iVoc(V)
1	162,02	156	0,628
2	129,09	190	0,62
3	99,37	122	0,610
4	59,48	275	0,595

Figure 3.11 Passivation results before the metallization

3.5. Approach 4 -patterning with lift-off

Based on the tests done in Approach 3, poly etch is adopted in this approach. Besides, a new approach is proposed with the new technique to achieve the patterning: the Lift-off process. For the emitter side, poly etch is adopted with SiO_2 as etching barrier layer to obtain the patterned emitter fingers. The SiO_2 layer here also serves as a sacrificial layer in the lift-off process for obtaining the BSF fingers. In this approach, all back surface is kept as flat to ensure the optimum surface passivation. The approach with the textured back surface is also developed and shown in the next section. As for the front surface, it is textured and also pre-passivated with a-Si:H/SiNx layers, which is the same as used in Approach 1.

3.5.1. Fabrication flowchart of Approach 4

Figure 3.12 shows the fabrication of Approach 4. Step 1, Float Zone (FZ), n-type, <100> oriented, 285µm monocrystalline silicon flat wafer is prepared as a substrate, and then, NAOC cleaning is performed to remove the possible organic or metal contamination on the wafer. Step 2, the back surface is then covered by SiN_X to prevent itself from being textured in the following texturing step. Step 3, the texturing step is realized in the TMAH (5%,80°C, ALKA-TEX-FREE) solution with a spinner. Step 4, the texturing protection layer SiN_X on the back surface is removed by being dipped into the BHF solution. Step 5, a-Si:H(i)/SiN_x layers are deposited onto the front side as a passivation layer and anti-reflection layer respectively, before which NAOC cleaning step is also performed.

Also, SiO_2 is deposited on the SiN_x layer at the front surface. This is a very important step because the SiO_2 can protect the SiN_x layer in the following steps against the chemical etchants. Also, it can increase the light-incoupling and light scattering. This will be fully explained in Section 4.2, Chapter 4.

Later, NAOC cleaning is performed as a pre-treatment cleaning step before the a-Si:H deposition. Step 7, a-Si:H(i)/a-Si:H(n)/ SiO_2 layers are deposited consecutively on the back surface by PECVD. Step 8-9, after the HNO_3 (99%) dip to remove possible contamination during wafers transport, the photolithography step and following HF (0.55%) dip is performed to expose the part of a-Si:H(i)/a-Si:H(n) layers at the emitter side. The BSF side is protected by the top SiO_2 layer. Step 10, the photoresist is removed by acetone and the sample is then dipped in the HNO_3 (99%) to ensure no photoresist being attached. Step 11, poly etch is used to get rid of the exposed part of a-Si:H(i)/a-Si:H(n) layers. Step 12, after NAOC cleaning, a-Si:H(i)/a-Si:H(p) layers are deposited onto the back surface. Step 13, the sample is dipped into the HF (0.55%) solution to achieve lift-off. Step 14-16, the SiO_2 layer is deposited again on the back surface with a corresponding photolithography step to passivate the gap between emitter and BSF, if it exists. Step 16, interdigitated metal electrodes are deposited onto the back surface by evaporation with the help of photolithography.

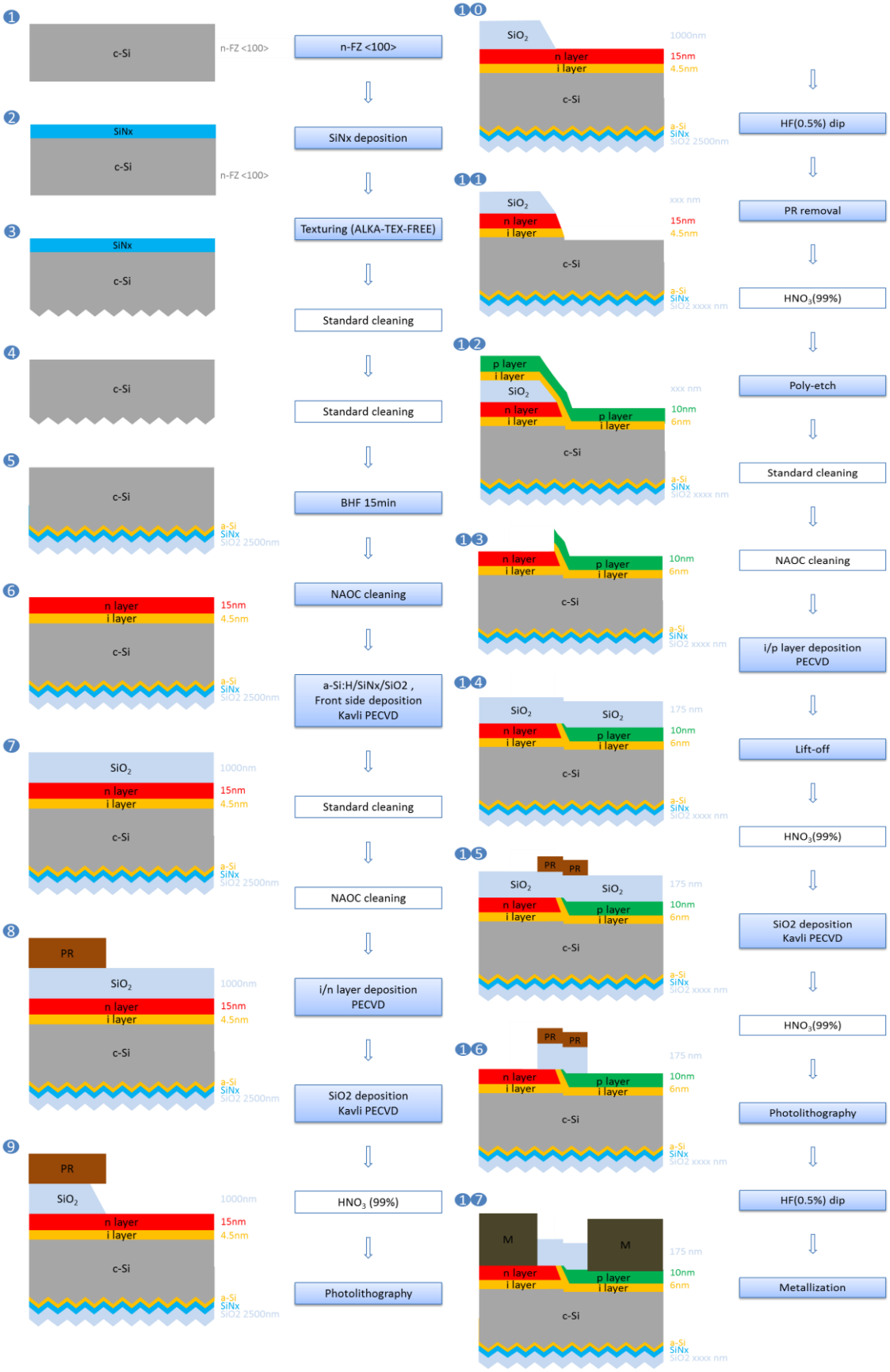


Figure 3.12 Fabrication flowchart of liftoff process used in Approach 4

3.5.2. Testing of involved technique: Lift-off

In this approach, lift-off is applied to achieve the BSF patterning. It is a prevailing application in the regime of thin film technology [48]. As illustrated in *Figure 3.13*, four steps are involved in the lift-off step: sacrificial layer deposition, the pattern defining on the sacrificial layer, target layer deposition, and sacrificial layer removal[49][50].

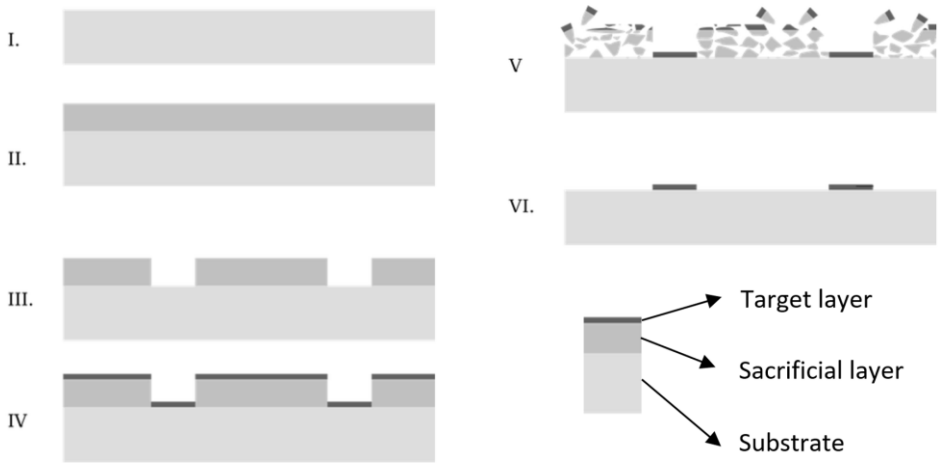
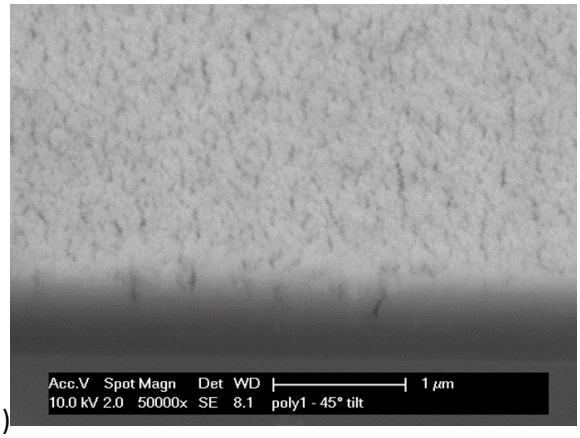


Figure 3.13 Schematic process of Lift-off [51]

In this work, pre-patterned SiO_2 layer works as a sacrificial layer and the emitter and a-Si:H(i)/a-Si:H(p) stack is the target layer, as illustrated in step 11-13. The reason why the a-Si:H layers can be easily lift-off here is attributed to a couple of reasons.

First, the formation of lots of pin holes at the surface of SiO_2, as shown in *Figure 3.14*, plays an important role. These pinholes are the results of the etching in poly etch solution where the i/n layer at the emitter side is removed, as shown in step 10-11. So, when the a-Si:H(i)/a-Si:H(p) layers are deposited onto such a surface, they become loose and porous because of the low deposition temperature, which is a big advantage for the HF (0.55%) solution to reach the SiO_2 layer underneath.

(a) 

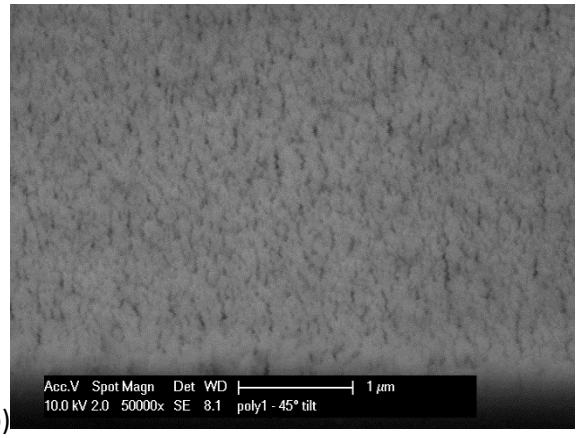
(b) 

Figure 3.14 SEM pictures of SiO2 after poly etch. (a) presents the thickness and the cross-sectional image of the SiO2 layer. (b) presents the surface of the SiO2 layer. all photos were taken with at 45° tilted

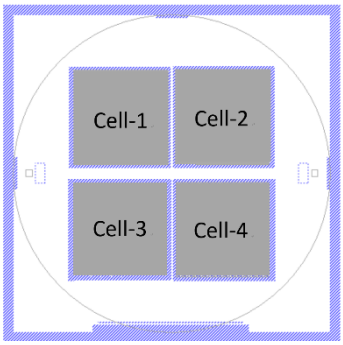
Secondly, as shown in the *Figure 3.14*, the thickness of the SiO_2 here is around 1000nm which is far more than the distance between the neighbor pinholes (around 50nm - 100nm). As a result, when

being rinsed in the HF (0.55%), the a-Si:H(i)/a-Si:H(p) layers on top of the SiO_2 can be easily lift-off, while the etchant doesn't even reach the bottom of the SiO_2 layer.

3.5.3. Summary

To sum up, the Lift-off technique employed in this work has been proved feasible. It even avoids the common problem in lift-off technology, the retention of the sacrificial layer [38]. This is due to the fact that the lift-off process here happens only at the top of the SiO_2 layer and the remaining SiO_2 layer can be easily removed by further HF (0.55%) dip. In addition, because of the introduction of Lift-off process, the last step of photolithography for the BSF patterning is not necessary. As a result, the whole process of this approach is simplified and minimized the additional interface contamination.

Following the approach 4, the patterning structure of SHJ-IBC solar cells have been fabricated successfully. Here are the passivation results before the metallization (*Figure 3.15*). Some contamination was induced in the cell 1 area. According to the passivation of other cell areas, this approach indicates great potential.



Cell	Lifetime(us)	J_o(FA/cm^2)	iVoc(V)
1	268,4	885	0,637
2	821,06	20,7	0,686
3	705,3	41,1	0,684
4	673,98	29	0,678

Figure 3.15 Passivation results before the metallization

In the next chapter, some optimization is made for this fabrication process, in terms of the thickness of SiO_2, etching time of poly etch, and photolithography step. The I-V characterization and relevant parameters of the final solar cell are treated in the next chapter.

3.6. Approach 5 - combination of texturing and patterning

Based on the approach 4, a new approach is proposed with two improvements. First, the patterning of emitter and texturing are combined together in this approach. This is achieved by rinsing the interdigitated prepared wafer into the TMAH (5%, 80°C, ALKA-TEX-FREE) solution. Second, the front surface field (FSF) is adopted.

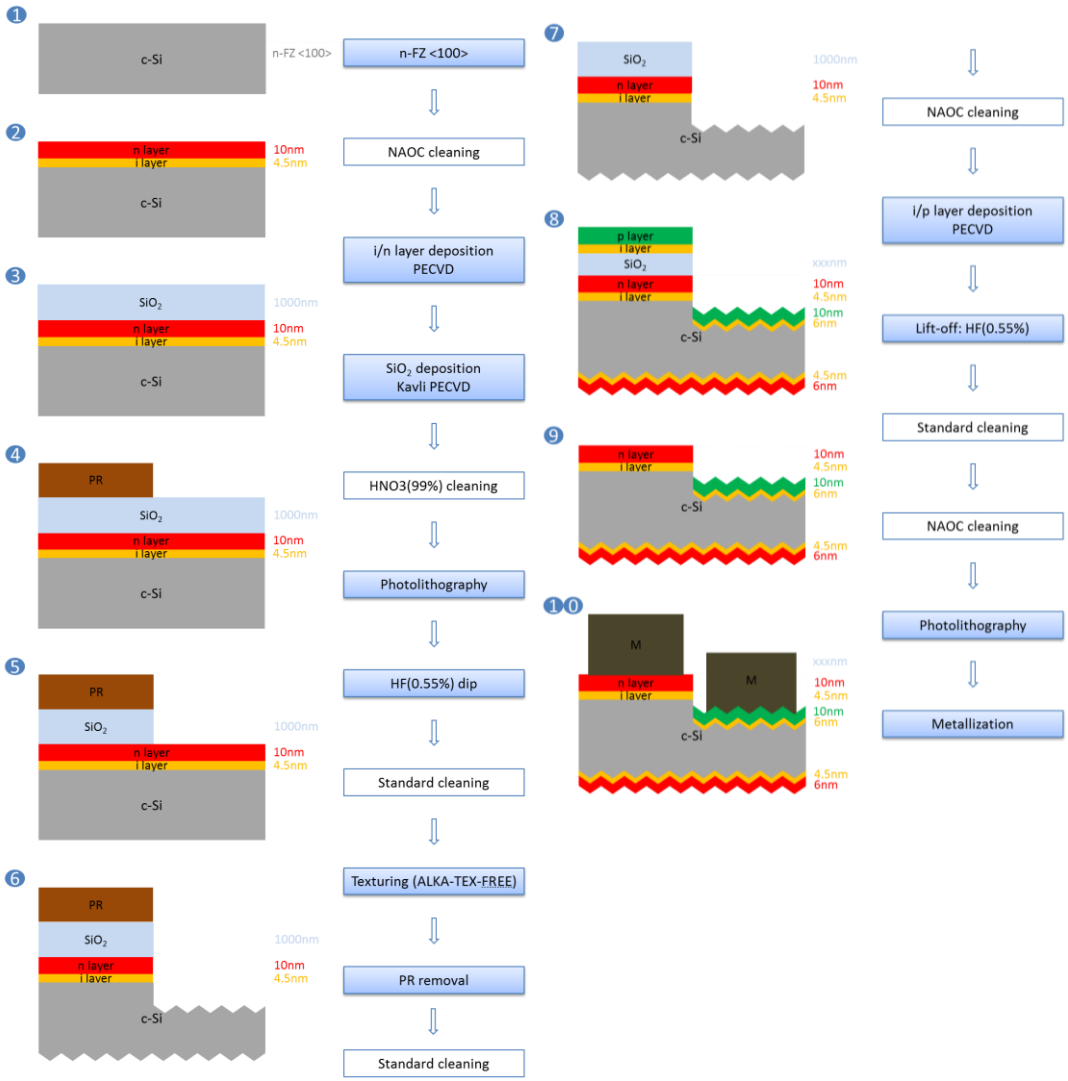


Figure 3.16 Fabrication flowchart of Approach 5

Figure 3.16 shows the fabrication process of Approach 5. Step 1, Float Zone (FZ), n-type, <100> oriented, 285µm monocrystalline silicon wafer is prepared as a substrate, and then, NAOC cleaning is performed to remove the possible organic or metal contamination on the wafer. Step 2, the back surface is then covered by a-Si:H(i)/a-Si:H(n) layers. Step 3, SiO_2 layer is deposited later as an etching barrier and also a sacrificial layer for lift-off. Step 4-5, the photolithography and HF (0.55%) dip are implemented to expose the emitter part of the a-Si:H(i)/a-Si:H(n) layers. Step 6, the whole sample is rinsed in the TMAH (5%, 80°C, ALKA-TEX-FREE) solution for around 15 min to achieve the texture on the front surface and emitter on the back surface. Step 7, the photoresist is removed. Step 8, front a-Si:H(i)/a-Si:H(n) layers (FSF) and back a-Si:H(i)/a-Si:H(p) layers are deposited. Step 9, lift-off is achieved by HF(0.55%) dip and the ultrasonic may help to accelerate the process. Step 10,

interdigitated metal electrodes are deposited onto the back surface by evaporation with the help of photolithography.

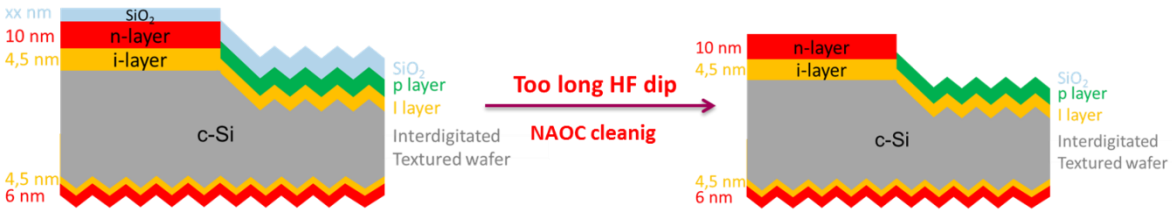
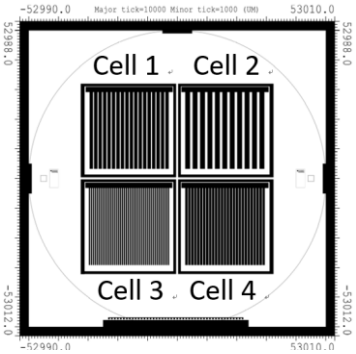


Figure 3.17 Too long HF dip in the NAOC cleaning

In the fabrication of this approach, when the necessary NAOC cleaning is performed as a preparation for the a-Si:H(i)/a-Si:H(p) deposition. The HF (0.55%) dip in the NAOC was too long that the SiO_2 etching barrier layer is even partly removed (*Figure 3.17*). However, the process is continued and stopped before the metallization. The passivation quality was measured just for reference, as is shown in *Figure 3.18*. Without the SiO_2 layer, the a-Si:H(i)/a-Si:H(p) layers cannot be removed and will do great damage to the passivation of the BSF. However, the cell 1 and cell 2 still have a decent performance which indicates that this approach is feasible. More investigation should be done on this approach for a simplified process to obtain a patterned BSF and emitter fingers.



Cell	Lifetime(us)	J_o(FA/cm^2)	iVoc(V)
1	897,73	102	0,673
2	562,47	117	0,665

Figure 3.18 Passivation of the cell1 and cell 2

4

Solar Cell Fabrication and Characterization

As is stated before, among all the approaches presented in the Chapter 3, Approach 4, the lift-off process, gives the most promising passivation results, therefore it was selected for solar cell fabrication. In this chapter, first, the results of the investigations performed based on the SEM image of the fabrication process are presented. Then the parameters of the fabricated solar cell are analysed for further optimization.

4.1. Optimization of the fabrication process

In this section, some investigations were performed to optimize the fabrication process with the help of SEM. The whole fabrication process followed here is shown in *Figure 3.12*. SEM and optical microscopic images were introduced to investigate certain steps to validate the flowchart and find possibilities of improvements.

4.1.1. SEM-1,2

The back surface of the wafer after step 8 (photolithography step) was investigated. Two SEM images, SEM-1 and SEM-2, were taken at the location shown in *Figure 4.1*. One is at the boundary of emitter and BSF, and the other one is at the emitter side for the investigation on the surface of SiO_2.

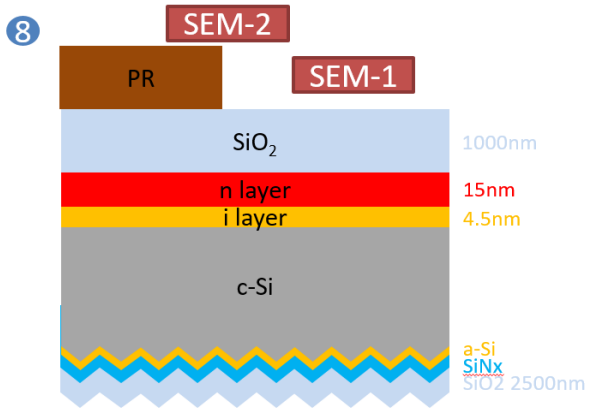
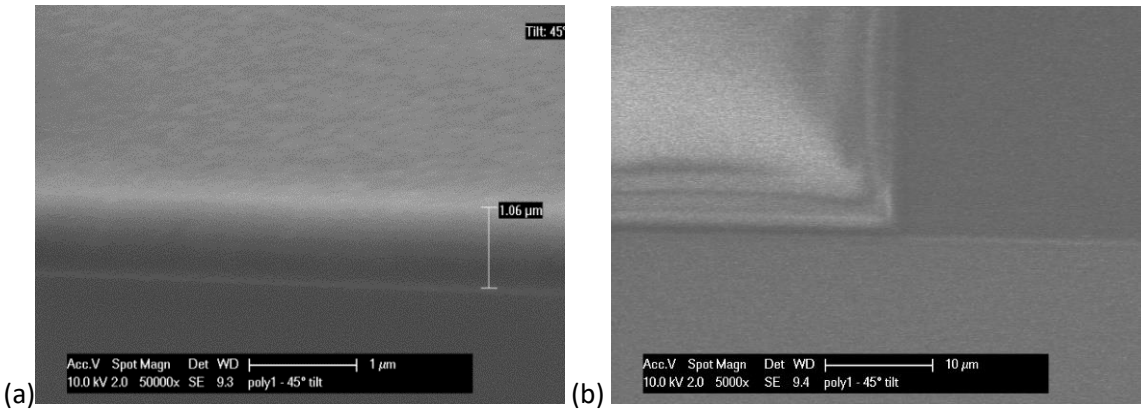


Figure 4.1The sketch picture of the solar cell process shown in Step 8,Figure 3.12 , Approach 4, Chapter 3. The image acquisition location of SEM-1 indicates the surface of SiO_2 layer. The image acquisition location of SEM-2 indicates the emitter/BSF area.

It can be observed from SEM-1 (*Figure 4.2*) that the surface of the SiO_2 layer is relatively flat and no pinholes can be observed. This proves the assumption that the pinholes are the result of the

subsequent poly etch dip. As for SEM-2 (*Figure 4.2*), the boundary is very clear and sharp on the emitter/BSF area at the resolution of 10 µm, which means the photolithography step employed can provide the good separation. The stair-stepping stripes at the edge are the result of the reaction between the surface and the electron beam in SEM, which is irrelevant to this work.

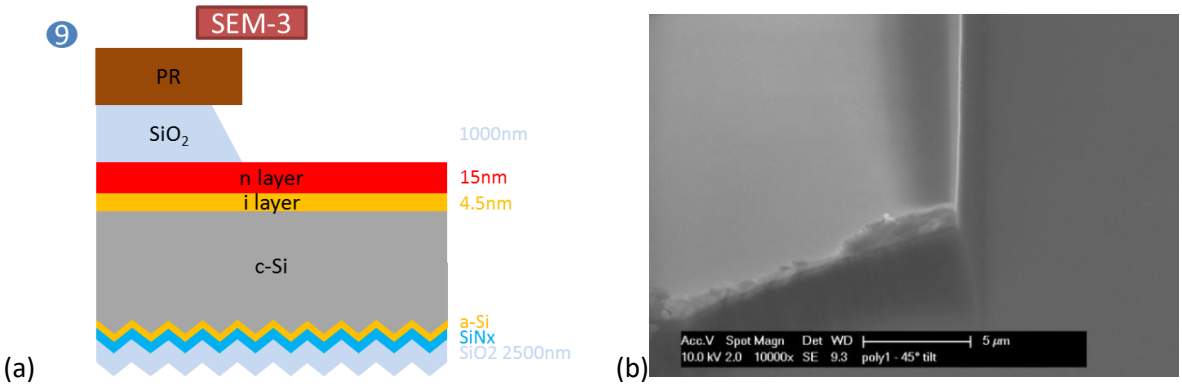


(a) (b)

Figure 4.2 SEM pictures of wafer at process Step 8 shown in Figure 3.12, Approach 4, Chapter 3. (a) SEM-1 presents the surface of SiO_2 layer. (b) SEM-2 presents the emitter/BSF area. All photos were taken at 45° tilted

4.1.2. SEM-3

The back surface of the sample after step 9 (HF (0.55%) dip step) was investigated. SEM-3 was taken at the boundary of emitter and BSF to observe the expected slope (*Figure 4.3 a*). Such a slope is the result of the end etch by HF. This is an undesirable result because it has an impact on the lift-off and the separation between emitter and BSF. Its influence will be treated in the following analysis.



(a) (b)

Figure 4.3 a. the sketch picture of the solar cell process shown in Step 9, Figure 3.12, Approach 4, Chapter 3, The image acquisition location of SEM-3 indicates the emitter/BSF area. (b) SEM-3 image, presenting the emitter/BSF area, taken at 45° tilted

From SEM-3(*Figure 4.3 b*), it seems difficult to identify the slope SiO_2 on the emitter/BSF area. However, with help of the optical microscope, the slope of the SiO_2 layer can be easily observed because of its typical optical property: color evolution by thickness (*Figure 4.4*).

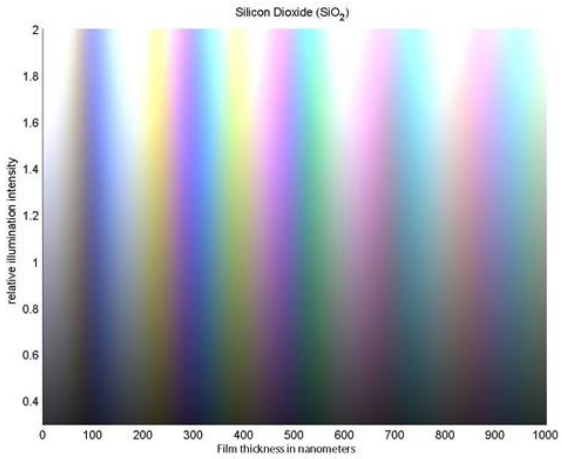


Figure 4.4 Color evolution by thickness of SiO_2 layer on c-Si substrate[52]

According to the image observed by optical microscope (*Figure 4.5*), the changing color at the emitter-BSF boundary indicates the slope of the SiO_2 layer.

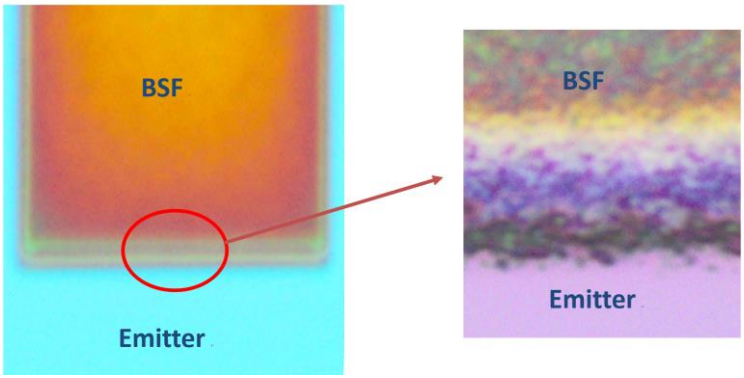


Figure 4.5 Optical microscopic image of SEM-3

4.1.3. SEM-4,5,6

The back surface of the sample after step 11 (poly etch step) was investigated. Three SEM images, SEM-4, SEM-5, and SEM-6 were taken at the location shown in *Figure 4.6*. One is at the boundary of emitter and BSF, one is at the BSF side for the investigation on the surface of SiO_2, and one is at the emitter side to check the influence of poly etch on the c-Si surface.

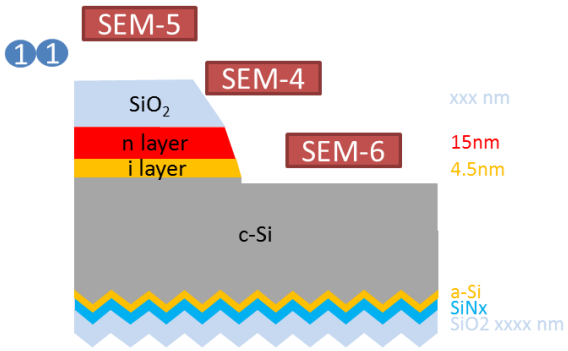
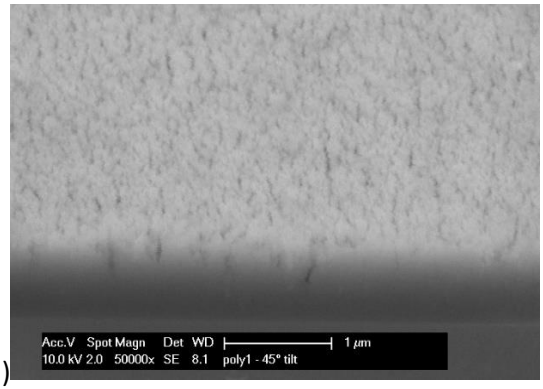


Figure 4.6 The sketch picture of the solar cell process shown in Step 11, Figure 3.12, Approach 4, Chapter 3. The image acquisition location of SEM-5 indicates the surface of SiO_2 layer. The image acquisition location of SEM-4 indicates the emitter/BSF area. The image acquisition location of SEM-6 indicates the c-Si substrate on BSF area.

SEM-5 (*Figure 4.7*) shows the surface of SiO_2 layer after poly etch. Compared to the previous SEM image, lots of pinholes can be found here. This is the reason why the lift-off can be easily achieved. However, attention also needs to be paid on the depth of these pinholes. If they are deep enough to reach the surface of the c-Si substrate, these pinholes will then act as transporting tubes for poly etch solution. As a result, the underlying a-Si:H(i)/a-Si:H(n) layers will be exposed and etched away. After the subsequent a-Si:H(i)/a-Si:H(p) layers deposition into these pinholes, shunt happens. The deepest pinhole that we observed is 463nm as shown in *Figure 4.7 b*. This depth looks safe enough for the BSF finger. However, 463 nm is just the observed maximum depth and there is a great depth distribution of the pinhole. So, in order to make sure that the underlying a-Si:H(i)/a-Si:H(n) layers don't suffer from the pinhole, the SiO_2 etching barrier layer here should be thicker.

(a) 

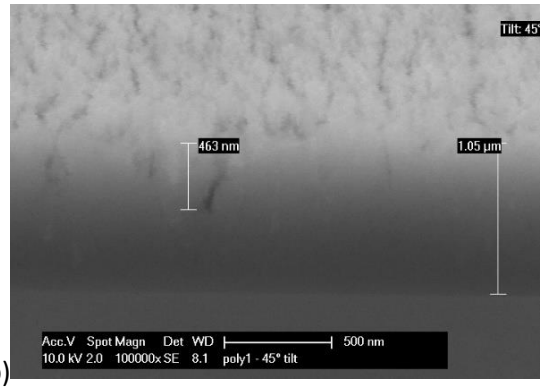
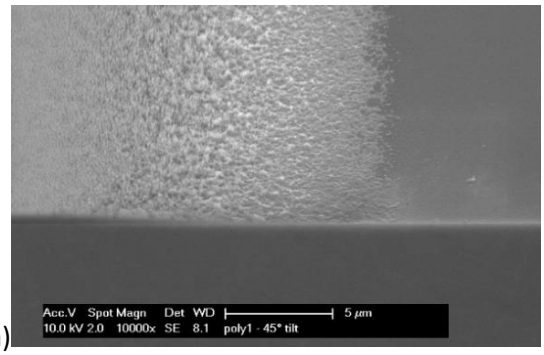
(b) 

Figure 4.7 SEM pictures of wafer at process Step 11 shown inFigure 3.12, Approach 4, Chapter 3. (a) SEM-5a, presents the surface of SiO_2 layer, 1µm resolution. (b) SEM-5b presents the emitter/BSF area, 500 nm resolution. All photos were taken at 45° tilted

However, for the near boundary area in the BSF finger, thicker SiO_2 etching barrier layer cannot help a lot because of the existence of the slope in the SiO_2 edges. SEM-4 (*Figure 4.8*) shows the boundary image. It can be observed from the *Figure 4.8 a*, the boundary here is 10-15 µm wide. The similar slope described previously can be observed in *Figure 4.8 b*. The thinnest SiO_2 layer here is just 189nm, which is far less than the observed maximum pinhole depth, 463nm. The consequence of such a problem will be discussed in the SEM-7 analysis.

(a) 

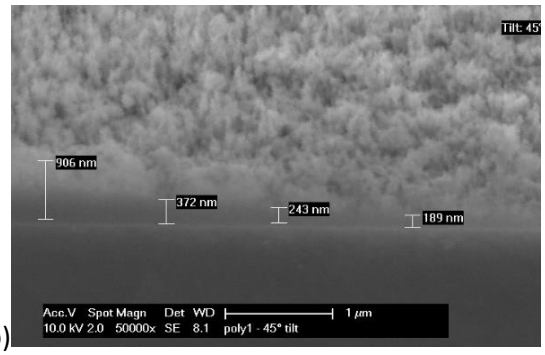
(b) 

Figure 4.8 SEM pictures of wafer at process Step 11 shown in Figure 3.12, Approach 4, Chapter 3. (a) SEM-4a, presents the surface of SiO_2 layer, 5 µm resolution. (b) SEM-4b presents the emitter/BSF area, 1 µm resolution. All photos were taken at 45° tilted

As for SEM-6 (*Figure 4.9*), the Nanoroughness is observed on the surface of the c-Si, which will decrease the passivation quality when the a-Si:H(i)/a-Si:H(p) layers are deposited on its surface. This is the result of too long poly etch. So, the etching time for the poly etch should be further optimized.

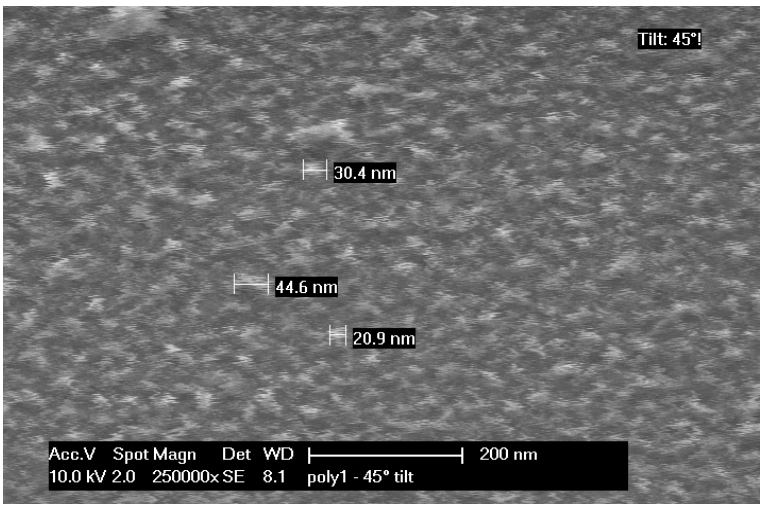


Figure 4.9 SEM picture of wafer at process Step 11 shown in Figure 3.12, Approach 4, Chapter 3. SEM-6 presents c-Si substrate on BSF area, 200 nm resolution, 45° tilted.

4.1.4.SEM-7

The back surface of the sample after step 12 (a-Si:H(i)/a-Si:H(p) layers deposition) was investigated. SEM-7 was taken at the location shown in *Figure 4.10*, the boundary between emitter and BSF.

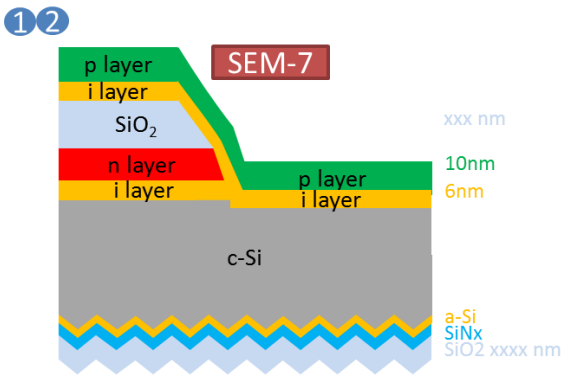


Figure 4.10 The sketch picture of the solar cell process shown in Step 12, Figure 3.12, Approach 4, Chapter 3. The image acquisition location of SEM-7 indicates the emitter/BSF area.

SEM-7 (*Figure 4.11*) shows the boundary image. To avoid confusion, it's worth mentioning that the left part is emitter which is the right part in *Figure 4.10* and the right part is BSF which is the left part in *Figure 4.10*. It can be observed from *Figure 4.11* that the boundary close to the emitter has many craters. This is because of the pinholes at the slope area, described in SEM-4. These pinholes are deeper than the thickness of the SiO_2 layer, so, the poly etch solution can penetrate and reach the a-Si:H(i)/a-Si:H(n) layers. Even more, the underneath substrate is also etched. As a result, those craters are formed.

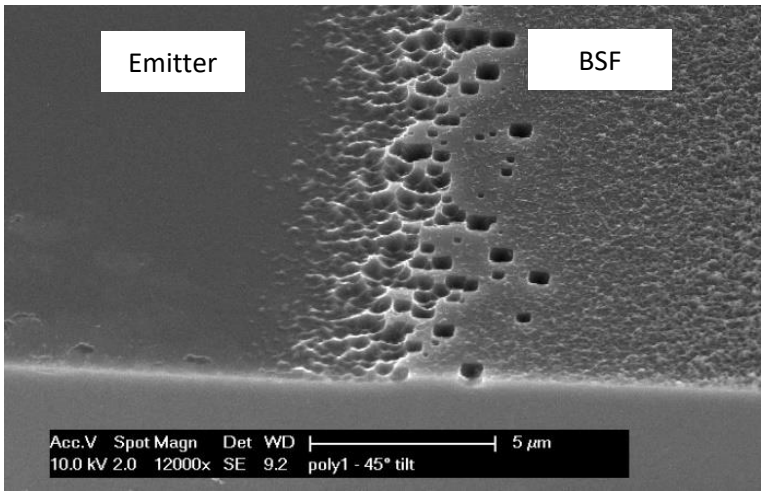


Figure 4.11 SEM picture of wafer at process Step 12 shown in Figure 3.12, Approach 4, Chapter 3. SEM-7 presents emitter/BSF area, 5 µm resolution, 45° tilted.

4.1.5. SEM-8

The back surface of the sample after step 13 (lift-off step) was investigated. SEM-8 was taken at the location shown in *Figure 4.12*, the boundary between emitter and BSF.

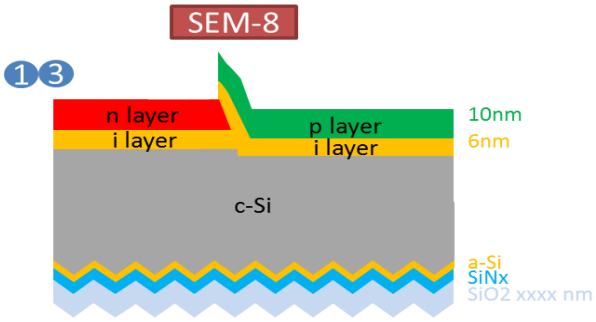


Figure 4.12 The sketch picture of the solar cell process shown in Step 13, Figure 3.12, Approach 4, Chapter 3. The image acquisition location of SEM-8 indicates the emitter/BSF area.

SEM-8 (*Figure 4.13 a*) shows the boundary image after lift-off process. The width of the boundary observed from *Figure 4.13 b* is almost the same as the one of SEM-4 (*Figure 4.8 a*), which means all the other parts were lifted off, and only the slope area was left because of the thinner SiO_2 in this area . *Figure 4.13 c* shows the craters at the emitter side which have been explained in SEM-7. *Figure 4.13 d* shows a layer of crust at the BSF side. This can be explained as follows. Because of the end etch, the thickness of the SiO_2 layer here is very small. When the a-Si:H(i)/a-Si:H(p) layers are deposited, it can be totally covered. As a result, it cannot be lifted off anymore.

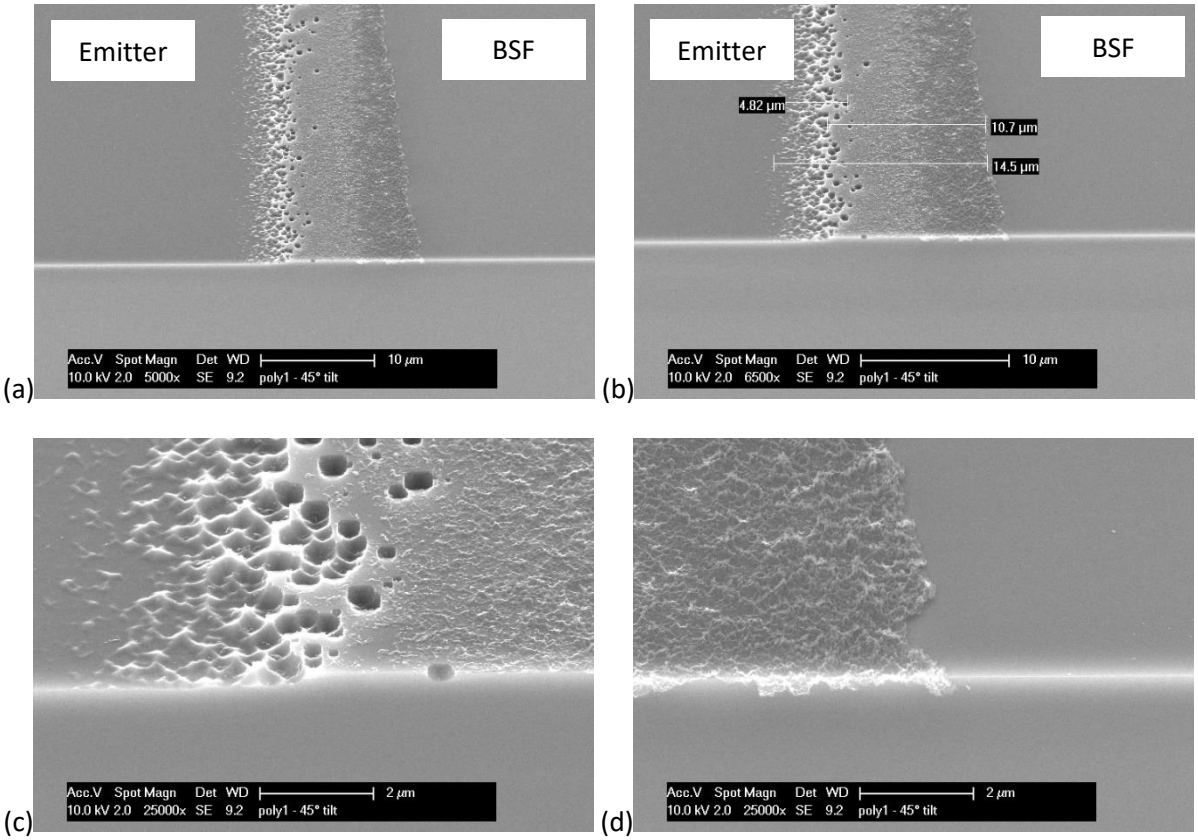


Figure 4.13 SEM pictures of wafer at process Step 13 shown in Figure 3.12, Approach 4, Chapter 3. (a) SEM-8a, presents the emitter/BSF area, 10 µm resolution. (b) SEM-8b presents the emitter/BSF area with measurements, 10 µm resolution. (c) SEM-8c presents the emitter side of the emitter/BSF area, 2 µm resolution. (d) SEM-8d presents the BSF side of the emitter/BSF area, 2 µm resolution. All photos were taken at 45° tilted

4.2. Solar cell results-loss analysis

Based on the SEM results, some optimization is made for the fabrication process: the thickness of the SiO_2 sacrificial layer at rear side is increased to 1500nm, etching time of poly etch is decreased to 15s, and the thickness of SiO_2 layer at front side is also increased, in order to stand longer in HF (0.55%), so that the underneath SiN_x can be protected. The SHJ-IBC solar cell is finally fabricated successfully, with an efficiency of 15.6% (*Table 4.1*). The J-V characterization and relevant parameters of the solar cell are discussed in the following sections.

Table 4.1 I-V parameters of the SHJ-IBC solar cell obtained via lift-off process

J_{SC} [mA/cm^2]	V_{OC} [mV]	FF [%]	η [%]
38.5	576	70.3	15.6

4.2.1. EQE

The J_{sc} of this solar cell before annealing is 39.6 mA/cm^2, which indicates a decent performance of the light management and front surface recombination controlling. However, for a typical IBC solar cell with superior performance, the J_{SC} should overpass 40 mA/cm^2[53]. As a result, some analysis was done on its reflectance, transmittance, and EQE, as depicted in *Figure 4.14*.

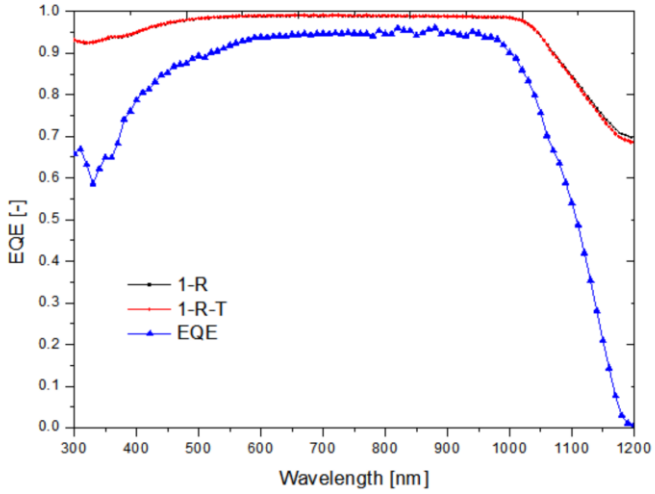


Figure 4.14 Measured EQE, reflectance and transmittance of the solar cell

For the reflectance, it can be observed that the loss stays at a relatively low level in the region of short wavelength. This is attributed to the double ARC (SiN_x +SiO_2 layers) and the Nano textures on the surface of SiO_2 layer caused by pinholes (*Figure 4.7*). As for the long wavelength area, the reflection may be attributed to two parts: one is the first reflection loss at the front surface, and the other one comes from internal reflection at the back surface.

As for the transmission, almost no loss is found in the short wavelength region because most of the light in this region cannot penetrate to that deep in the c-Si bulk to the back surface[54]. In the long wavelength region, there is a tiny portion of transmission because of the gaps between the emitter and BSF, which are not covered by metal.

Optical loss and recombination loss are the two main reasons for the EQE loss of the solar cell. The analysis of EQE here can be divided into three areas: short wavelength area, visible light area, and near infra-red area.

In the short wavelength area, because of the shallow penetration of the light, most of the loss of EQE happens near the front surface. The optical loss here is dominated by the parasitic absorption from front passivation layer (a-Si:H layer). However, since the front passivation layer is very thin in this solar cell, the optical loss is not that severe, compared to the recombination loss.

In the visible light region, the recombination dominates the loss, which mainly comes from the recombination at the bulk-emitter interface and the shunt area at the bulk-BSF interface.

In the near infra-red region, the recombination at the back interface plays less role while the optical loss becomes the main factor[53]. Especially, the parasitic absorption in the aluminum, namely plasmonic absorption[55], accounts for the dramatic EQE loss.

4.2.2. J-V curve

The main parameters of the SHJ-IBC solar cells for the performance analysis are obtained from the illuminated J-V curve, such as short circuit current(J_{SC}), open circuit current(V_{OC}), Fill factor(FF), series resistance(R_S) and shunt resistance(R_{SH}). The measured J-V curve together with other parameters of the solar cell has been presented in *Figure 4.15*.

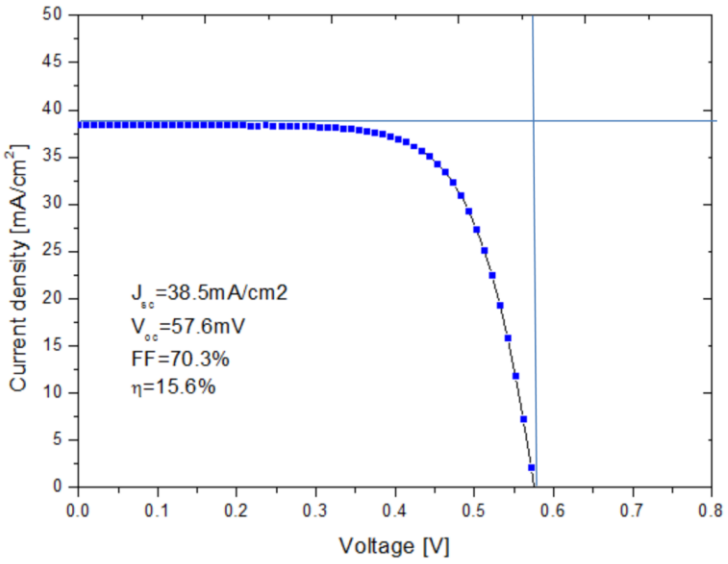


Figure 4.15 Measured J-V curve of the solar cell

V_{OC}

V_{OC} of the solar cell can be deducted from the J_0, which represents the passivation quality of the solar cell. J_0 of this cell can be roughly calculated using the following formula:

$$J_{0(cell)} = J_{0(front)} + a \times J_{0(BSF)} + b \times J_{0(emitter)} + c \times J_{0(gap)}$$

Where a, b and c represents the corresponding pitch ratio of the BSF, emitter and gap.

First, the implied V_{OC} of the solar cell is analysed. *Figure 3.15* in the last chapter shows the highest implied V_{OC}, 686 mV. Compared to the superior SHJ-IBC solar cell with an implied V_{OC} higher than 700mV, this solar cell suffers a lot from the low passivation quality of the emitter (a-Si:H(i)/a-Si:H(p) layers and the front surface passivation. However, the cell V_{OC} here is 576mV which is far less than the implied V_{OC} (maximum 686mV, in *Figure 3.15*) in the passivation test before the final metallization. Two main reasons may account for such a problem. The first one is that the shunt happens in the BSF((a-Si:H(i)/a-Si:H(n) layers)) area caused by pinholes (illustrated in *Figure 4.7*). If these pinholes are covered by the metal as shown in *Figure 4.16*, it becomes even severer because the conductive metal provides a "highway" for the electron to transport, and then, more recombination happens at the circled area in *Figure 4.16*. The second reason is the insufficient band bending, with which the sample can still provide a decent lifetime as long as the c-Si surface is well passivated. However, the calculated implied V_{OC} from such a measurement can never be finally converted to the cell V_{OC} because of the insufficient band bending[53]. As a result, a-Si:H(p) layer with lower activation energy should be developed in the future.

Figure 4.16 Shunt caused by pinholes in the BSF(yellow circle area)

FF

According to research done by Adachi [1], the theoretical maximum FF for the c-Si solar cell is 89%, based on certain conditions. Even though the thickness of the wafer and the doping level of the solar cell in this thesis is different, the FF of this cell, 70.3%, is still too low. The possible reasons of the FF loss must be researched.

Compared to SHJ front/rear contacted solar cells, SHJ-IBC solar cells normally performs better in terms of FF[19]. As we all know, the factors responsible for the decrease of FF is hard to explicitly interpret because of their diversities, correlations, and interactions. However, among all of them, two principal components can be drawn out: recombination loss and resistive loss.

Let's deal with the resistive loss first. Resistive can be divided into two parts: series resistance (R_S) and shunt resistance(R_{SH}). In this case, the series resistance of this solar cell can be roughly observed from the J-V curve. The slope at the open-circuit point is deflected from the one of the ideal solar cell, in which the curve should be almost vertically upward. The measured R_S here is 0.179 $m\Omega/m^2$. The contribution to the FF loss of such an R_S can be evaluated by the pseudo-FF from the Suns-V_{OC} measurement, in which the series resistance is not included. The measured 75.9% pseudo-FF means around 6% loss of the FF is caused by R_S. Normally, the series resistance is mainly comprised of the doped layers resistance, contact resistance and the grid resistance[56]. In this cell, the dominated factors should be the contact resistance and the grid resistance. As for the shunt resistance, the pinholes filled with a-Si:H(i)/a-Si:H(p) layers in the BSF fingers should be the main factor, which has been discussed in *Figure 4.16*.

Besides the resistive losses discussed above, another aspect that influence the FF is the carriers recombination. The patterning steps involve certain photolithography procedures, which brings some surface defects despite those cleaning steps. As a result, the recombination rate increases a lot [57]. Also, these induced contaminations may do harm to the band alignment at the c-Si/a-Si:H interface,

which leads to the further FF loss[18]. According to the research done by Lulu Zhang et al. [19], in which the SHJ solar cell was fabricated intentionally with the same photolithography steps as those for SHJ-IBC solar cell, the FF was decreased by 4% because of the induced surface contamination and defects.

Annealing

The solar cell was annealed at 180°C after the fabrication finished. J-V curve was measured every 2 min during the annealing. The efficiency arrived at the maximum efficiency 15.6% after 6min annealing. The solar cell parameters (J_{SC}, V_{OC}, $R_{S,}$ and FF) as a function of the annealing time are shown in *Figure 4.17* and depicted as follows.

Figure 4.17 shows the J_{SC} and V_{OC} versus annealing time. It can be observed that V_{OC} goes up until 4 min and then goes down with the increasing annealing time. This is attributed to the hydrogen diffusion from the a-Si:H layers into the substrate, during which the dangling bonds can be passivated and the Nanostructure is restored. However, longer annealing time bring the opposite effect, the desorption of the hydrogen[43]. As for J_{SC}, it decreases as time goes by and arrives at the minimum at 4 min and then goes up again. Such a variation is assumed to be relevant to plasmonic absorption at the back metal surface, which is still unknown.

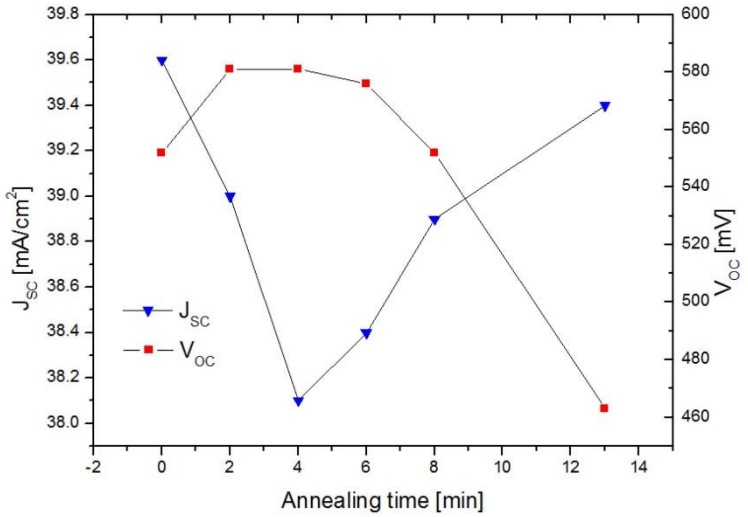


Figure 4.17 Annealing effects on the J_{SC} and V_{OC}

Figure 4.18 shows the R_S and FF vary over annealing time. It can be observed that FF goes up until arriving at the maximum at 4 min and the maintains at this level. R_S is the other way around, goes down and stays at the minimum level. Such a transition proves the relationship between these two parameters, the increase of the FF during the annealing comes from the decrease of R_S. The reason here for the decrease of R_S is the lower contact resistance due to a better ohmic contact after annealing

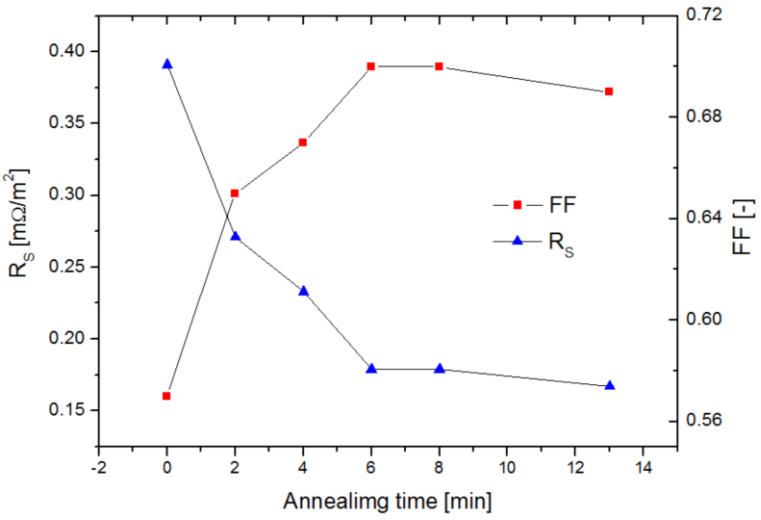


Figure 4.18 Annealing effects on the R_S and FF

5

Conclusion and Outlook

5.1. Conclusion

The focus of this project is to design the patterning approach for SHJ-IBC solar cells. Commonly, the fabrication of a SHJ-IBC solar cell involves several processes, among which the patterning process of a-Si:H layers is exclusively imperative. Photolithography technique is applied for the patterning in this work because of its inherent accuracy. Accordingly, five fabrication approaches were designed to pattern the a-Si:H layers for SHJ-IBC solar cells.

In Approach 1, because of the different etching behaviours of emitter(a-Si:H(i)/a-Si:H(p)) and BSF(a-Si:H(i)/a-Si:H(n)), wet etching and dry etching are respectively employed. TMAH (1%) is used as a wet etchant to etch the a-Si:H(i)/a-Si:H(n) layers to obtain the patterned emitter fingers. Hydrogen plasma dry etching is used to etch away the a-Si:H(i)/a-Si:H(p) layers in the area where the BSF locates. An intrinsic a-Si:H layer is used as an etching barrier to hydrogen plasma.

In Approach 2, intrinsic a-Si:H layer at the back surface is shared by emitter and BSF. As a result, only n-type a-Si:H in the emitter fingers area is removed to achieve patterning for emitter. This is performed by the wet etching: NAOC etching. For the BSF, no patterning action is deployed because of the application of Tunnel Recombination Junction (TRJ).

In Approach 3, poly etch (HNO_3 (69%): HF (40%) = 70:1) is used as a wet etchant to get rid of the a-Si:H(i)/a-Si:H(n) layers for emitter patterning, while hydrogen plasma is used to etch the a-Si:H(i)/a-Si:H(p) layers to obtain the patterned BSF fingers. In this case, an SiO_2 layer is used as an etching barrier for the BSF fingers against hydrogen plasma.

In Approach 4, for the emitter side, poly etch (HNO_3 (69%): HF(40%) = 70:1) is adopted with SiO_2 as etching barrier layer to obtain the patterned emitter fingers. The SiO_2 layer here also serves as a sacrificial layer in the lift-off process for obtaining the BSF fingers.

In Approach 5, for the emitter side, the finger formation and texturing step is combined. This is performed by rinsing the exposed a-Si:H(i)/a-Si:H(n) layers into the TMAH (5%,80^{o}C, ALKA-TEX-FREE) solution. the lift-off process for Approach 4 is still followed to obtain the BSF fingers.

From the process point of view, all of these approaches potentially give a successful patterning of the a-Si:H layers, but some of them still need more improvements from the passivation point of view. Approach 4, the lift-off process, gives the most promising passivation results, therefore it is selected for further investigation, where SEM images were taken for analysis. Based on the SEM images, some optimization is made for the fabrication process to solve the shunt problem including increasing the

thickness of the SiO_2 sacrificial layer and decreasing the poly etch etching time. The SHJ-IBC solar cell is finally fabricated successfully. 15.6% efficiency was achieved after certain annealing time with V_{OC}=576mV, J_{SC}=38.4mA/cm^2, and FF=70%. Based on Transmittance/Reflectance/EQE curve and J-V curve, the main loss comes from the shunt in the BSF and bad passivation quality of the emitter.

5.2. Outlook

Based on the analysis in Chapter 4, there is still large room for optimizations in terms of V_{OC}, $J_{SC,}$ and FF to increase the solar cell efficiency. Several optimization methods have been designed and presented as follows.

5.2.1. Passivation strips of BSF-emitter boundary.

The solar cell suffers from the shunt happening near the BSF-emitter boundary. A possible solution is that passivation layers can be deposited at the beginning of the fabrication process, say step 5 in *Figure 3.12*. The a-Si:H/SiN_x layers are deposited on both sides of the substrate. The front side is used as the passivation/antireflection layers as before. The rear side, after certain photolithography steps using the mask for metallization, can form strips on the BSF-emitter boundaries. This will decrease the influence of the problem happening in the vicinity of the BSF-emitter boundary.

5.2.2. Double SiO_2 layer as etching barrier layer

It was found that the SiO_2 deposited at a higher temperature has a denser structure, which means those pinholes cannot penetrate that deep in such a layer. So, we can combine this two SiO_2 layers together. The loose SiO_2 is deposited on top, responsible for lift-off, while the dense SiO_2 is deposited at the bottom as an etching barrier. In this case, the shunting problem can be solved. Whether the SiO_2 deposited at a higher temperature does harm to the surface passivation or not should be tested in advance.

5.2.3. Front surface field should be introduced

Since the a-Si:H(i)/a-Si:H(p) layers applied in this solar cell cannot provide a good passivation, the recombination rate at the bulk/emitter surface is quite high. In this case, to prevent the electron from being recombined before arriving at the BSF, a front surface field should be included to provide a 'highway' for the electron transport.

5.2.4. Bifacially textured or at least the emitter side textured as Approach 4

The half textured back surface Approach 4 or even a new approach with totally textured back surface should be developed to increase the light incoupling and scattering. However, such an adjustment may increase the parasitic absorption of the metal. More investigations should be done.

5.2.5. TCO between emitter/BSF and metal

TCO should be employed to increase the internal reflection of the metal and even decrease the plasmonic absorption[58].

5.2.6. Optimization of the emitter/BSF ratio and pitch size

The mask now employed for patterning photolithography is the one designed especially for the homojunction IBC solar cells with FSF. When it comes to SHJ-IBC solar cells, because of the differences in carrier transport properties and the material properties, the ratio of the emitter and even the pitch size should be optimized.

5.2.7. Optimization of the pre-treatment and post-treatment of the a-Si:H layers

As mentioned before, contamination and defects during the process bring damage to the surface passivation[19]. Several Pre-treatment and post-treatment actions should be done. For example, more NAOCs and chamber cleaning should be employed before deposition and annealing in the hydrogen atmosphere after deposition can also be used to restore the passivaton.

5.2.8. The proposed double reflection layer (Thickness of the SiO_2 and SiN_x)

In this solar cell, the SiO_2 at the front surface is mainly used to protect the underlying SiN_x. By controlling the thickness of the SiO_2, the so-called double antireflection coating can be made together with SiN_x,

5.2.9. Optimization according to the band diagram

Several optimizations can be designed according to the band diagram. For example, decreasing the activation energy of the doped layer help to lower down the barrier that hinders the minority carrier transport. This need the optimization of the deposition conditions, including the controlling the RF power, pressure, temperature, and gas flow.

Bibliography

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Jiali Zhou

Delft, July 2017

Appendix-1 Dry etching rate of *intrinsic and p-type a-Si:H layers*

Table 0.1 Optimized etching rate of intrinsic a-Si:H layers

Sample	Thickness before etching [nm]	H_2 [sccm]	Pressure [mbar]	RF P [W]	Thickness after etching [nm]	Etching time [min]	Etching rate [nm/min]
1	19.45	200	2.5	6/6	7.8	5	0.03883
2	19.21	200	2.5	3,7	9.02	5	0.03397
3	18.97	200	2.5	1,6	14.4	5	0.01523

Table 0.2 Optimized etching rate of p-type a-Si:H layers

Sample	Thickness before etching [nm]	H_2 [sccm]	Pressure [mbar]	RF P [W]	Thickness after etching [nm]	Etching time [min]	Etching rate [nm/min]
1	26.21	200	2.5	7/7.2	20.79	4	0.02258
2	17.28	200	2.5	6/6	11.2	5	0.02027
3	17.97	200	2.5	4/3,7	12.91	5	0.01687
4	18.64	200	2.5	2,2/1,6	18	5	0.00213

Appendix-2 Uniformity test of dry etching

Table 0.3 Uniformity test of dry etching

Location	Thickness before etching [nm]	Thickness after etching [nm]	Etching time [min]	Etched thickness [nm]
1	17.28	12.23	2.5	5.05
2	16.58	10.25	2.5	6.33
3	16.65	11.2	2.5	5.45
4	16.63	11.55	2.5	5.08
5	17.13	10.74	2.5	6.39
6	16.56	10.08	2.5	6.48
7	16.72	10.51	2.5	6.21
8	16.21	11.03	2.5	5.18
9	15.47	9.33	2.5	6.14

Appendix-3 NAOC etching test

Table 0.4 NAOC etching test

Location	Thickness before etching [nm]	Thickness after etching [nm]	NAOC [-]	Etched thickness [nm]
1	12.51	8.48	3	4.03
2	12.58	8.46	3	4.12
3	12.25	7.79	3	4.46
4	11.77	7.57	3	4.20
5	12.2	8.17	3	4.03
6	11.9	7.65	3	4.25

Appendix-4 Poly etch test

Table 0.5 Etching rate of i/n layer by poly etch

Location	Thickness before etching [nm]	Thickness after etching [nm]	Etching time [s]	Etched thickness [nm]
1	16.52	7.86	8	1.0825
2	17.33	5.18	12	1.0125

Appendix-5 Data acquisition point during thickness measurement on wafer

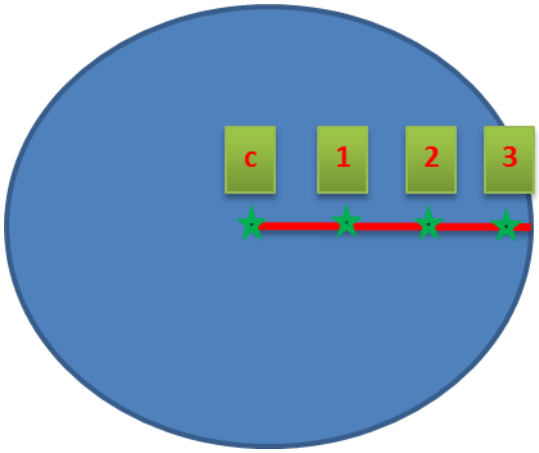

Figure 0.1 Points measured on the wafer with SE