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A Study of Graphene Nanoribbon-based Gate Performance Robustness under Temperature Variations

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***Abstract*—As CMOS scaling is reaching its limits, high power density and leakage, low reliability, and increasing IC production costs are prompting for developing new materials, devices, architectures, and computation paradigms. Additionally, temperature variations have a significant impact on devices and circuits reliability and performance. Graphene's remarkable properties make it a promising post Silicon front-runner for carbon-based nanoelectronics. While for CMOS gates temperature effects have been largely investigated, for gates implemented with atomic-level Graphene Nanoribbons (GNRs), such effects have not been explored. This paper presents the results of such an analysis performed on a set of GNR-based Boolean gates by varying the operation temperature within the military range, i.e., $-55°C$ to $125°C$, and evaluating by means of SPICE simulations gate output signal integrity, propagation delay, and power consumption. Our simulation results reveal that GNR-based gates are robust with respect to temperature variation, e.g., 5.2% and 5.3% maximum variations of NAND output logic "1" (V_{OH}) and logic "0" (V_{OL}) voltage levels, respectively. Moreover, even in the worst condition GNR-based gates outperform CMOS FinFET 7nm counterparts, e.g., $1.6\times$ smaller delay and $185\times$ less power consumption for the INV case, which is strengthening their great potential as basic building blocks for future reliable, low-power, nanoscale carbon-based electronics.**

***Index Terms*—Graphene, GNR, Boolean Gates, NEGF, Phonon Scattering, Carbon Nanoelectronics, Reliability, Temperature Effects.**

I. Introduction

As CMOS technology is going to reach its scaling limits due to high power density, high gate oxide tunneling current, increasing circuit sensitivity to soft errors from radiation, increasing variability issues of line edge control and roughness, and increasing IC production costs [1], [2], alternative technological avenues are considered by developing new materials, devices, architectures, and computation paradigms. Graphene, as one of the promising post Silicon front-runners, has unique and remarkable properties, such as high electron mobility at room temperature ($10\times$ higher than Si), ultimate thinness, ballistic carrier transport with long mean-free paths, and high thermal conductivity, making it attractive for future carbon-based nanoelectronics, and for a wide range of graphene-based applications, e.g., spintronics, photonics and optoelectronics, sensors, energy storage and conversion, flexible electronics, and biomedical devices [3], [4], [5], [6], [7]. Due to its excellent properties, graphene has been used for transistor-based logic, which follows the traditional CMOS design style, e.g., in [8], [9], while alternative approaches towards gate realizations departing from the switch-based mainstream have been introduced in, e.g., [10], [11].

As CMOS dimensions are down-scaling to sub-$10\,\text{nm}$ range, temperature variations have a significant impact on device and circuits reliability and performance [12]. While for CMOS gates temperature effects have been largely investigated [13], for gates implemented with atomic-level Graphene Nanoribbon (GNR), such effects have not been explored. In this paper, we present the results of such an analysis performed on a set of 1- and 2-input GNR-based Boolean gates, i.e., {INV, BUF, AND2, NAND2, OR2, NOR2, XOR2} . We vary the operation temperature within the military range, i.e., $-55°C$ to $125°C$, and evaluate by means of SPICE simulations gate's output signal integrity, propagation delay, and power consumption. The obtained results suggest that the GNR-based gates are robust with respect to temperature variation, e.g., 5.2% and 5.3% maximum variations for NAND for logic "1" (V_{OH}) and logic "0" (V_{OL}) output voltage level, respectively. Additionally, even in the worst case condition they outperform CMOS FinFET 7nm counterparts, e.g., $1.6\times$ smaler delay and $185\times$ less power consumption for the INV case, suggesting that the GNR-based gates have great potential as basic building blocks for future reliable, low-power, carbon-based nanoelectronics.

The remaining of this paper is structured as follows: Section II entails an overview of the simulation framework. Section III presents the simulation results and comments on gates robustness with respect to temperature variation. Finally, some concluding remarks are given in Section IV.

II. Simulation framework

In this section, we present a phonon limited GNR transport computation model based on Non-Equilibrium Green's Function (NEGF) approach which takes into account electron-phonon interaction, for deriving GNR's electrical properties (e.g., current and conductance). Further, we describe the GNR-based complementary Boolean gates SPICE simulation under temperature variations.

A. Phonon Limited GNR Transport Computation Model

In order to model the electronic carrier transport, we make use of the NEGF-Landauer formalism, where NEGF

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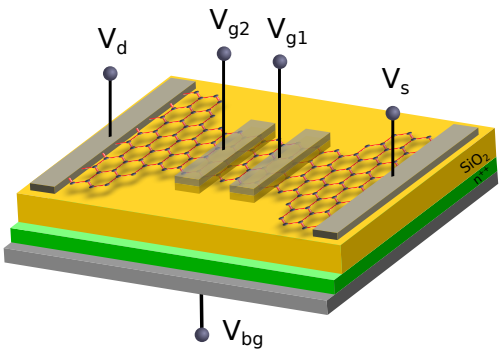

Fig. 1: GNR Basic Building Block.

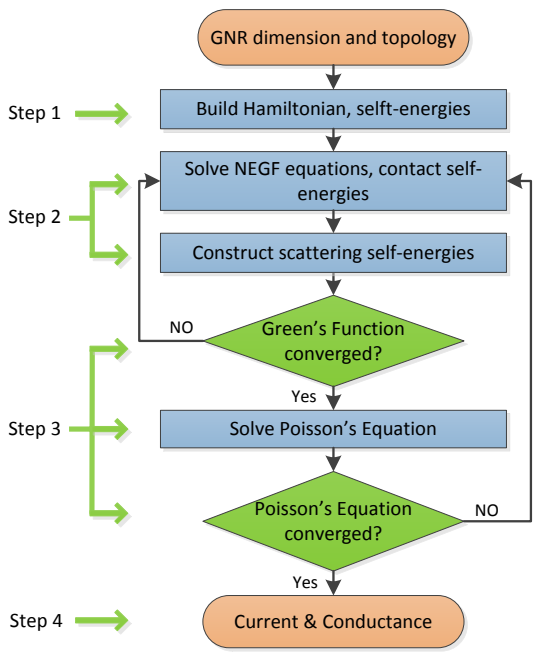

Fig. 2: GNR Simulation Flow based on NEGF-Landauer Formalism with Phonon Scattering.

calculations describe the electron-electron interaction and the Landauer formula gives the GNR current and conductance [14]. To account for the temperature-induced phenomena, i.e., electron-phonon interactions for both optical and acoustic phonons, we extended the NEGF-Landauer simulation framework with the self-consistent Born approximation [15].

The evaluated gates are constructed from basic structures as the one depicted in Figure 1, which includes a trapezoidal graphene Quantum Point Contact (QPC) with zigzag edges carved into a butterfly GNR shape in order to meet the desired gate functionality [16]. This GNR is utilized as conduction channel between the source and drain contacts, which are biased by a potential $V_{\mathrm{d}} - V_{\mathrm{s}}$. Top gates ($V_{\mathrm{g1}}$, V_{g2}) and one back gate (V_{bg}) are utilized to modulate the GNR device conductance and current.

The simulation flow Depicted in Figure 2 consists of 4 steps, as follows.

In **Step 1**, we use semi-empirical Tight Binding (TB) computations to construct the GNR Hamiltonian matrix H with respect to GNR's dimension and gate contact topology, which incorporates all internal and external potentials such as top gate voltages and back gate voltage. H is constructed as:

$$H = \sum_{i,j} t_{i,j} \left|i\right\rangle \left\langle j\right|, \tag{1}$$

$$\text{where } t_{i,j} = \begin{cases} 0, & \text{if atoms } i \text{ and } j \text{ are not adjacent} \\ \tau, & \text{otherwise} \end{cases} \tag{2}$$

and $\tau = -2.7\,\mathrm{eV}$. The drain and source contacts are applied on GNR's end sides with different electrochemical potentials, and the drain and source contact-channel interactions are modelled by the contact self-energy functions Σ_D and Σ_S, respectively.

In **Step 2**, after deriving H, Σ_D, and Σ_S, we proceed to solve NEGF equations in order to obtain the electrical properties. The most important equations to be solved are the energy dependent retarded Green's function (G^r) and the electron and hole correlation functions (G^n and G^p), [14], denoted as:

$$G^r(E) = [(E + i\eta^+)I - H - \Sigma_S - \Sigma_D - \Sigma_{el-ph}]^{-1}, \tag{3}$$

$$G^n(E) = G^r * (\Sigma_S^{in} + \Sigma_D^{in} + \Sigma_{el-ph}^{in}) * G^a, \tag{4}$$

$$G^p(E) = G^r * (\Sigma_S^{out} + \Sigma_D^{out} + \Sigma_{el-ph}^{out}) * G^a, \tag{5}$$

where I is the identity matrix, η^+ is an infinitesimal positive value, and Σ_{el-ph} denotes the scattering function, which corresponds to electron-phonon interactions. $G^a = [G^r]^\dagger$ is the advanced Green's function, Σ_{el-ph}^{in} and Σ_{el-ph}^{out} are in-scattering and out-scattering functions corresponding to electron-phonon interactions. $\Sigma_{S(D)}^{in}$ and $\Sigma_{S(D)}^{out}$ are the source (drain) lesser (in) self-energies function and advanced (out) self-energies function, respectively, computed as:

$$\Sigma_{S(D)}^{in}(E) = \Gamma_{S(D)}(E) * f_{S(D)}(E), \tag{6}$$

$$\Sigma_{S(D)}^{out}(E) = \Gamma_{S(D)}(E) * [1 - f_{S(D)}(E)], \tag{7}$$

where $f(E)$ denotes the Fermi-Dirac distribution function at temperature T and $\Gamma_{S(D)}$ the broadening function computed as:

$$\Gamma_{S(D)}(E) = i[\Sigma_{S(D)}(E) - \Sigma_{S(D)}^{\dagger}(E)]. \tag{8}$$

The electron-phonon scattering function Σ_{el-ph} incorporates all scattering mechanism self-energies related to Acoustic Phonon (AP) and Optical Phonon (OP) [15] (Σ_{el-ph}^{in} and Σ_{el-ph}^{out} are constructed in a similar way), denoted as:

$$\Sigma_{el-ph} = \Sigma_{AP} + \Sigma_{OP}, \tag{9}$$

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where Σ_{AP} and Σ_{OP} are the AP and OP self-energies, respectively, which can be computed as:

$$\Sigma^{in}_{AP}(i,i,E) = D_{AP} * G^n(i,i,E), \tag{10}$$

$$\Sigma^{out}_{AP}(i,i,E) = D_{AP} * G^p(i,i,E), \tag{11}$$

$$\Sigma_{AP}(i,i,E) = D_{AP} * G(i,i,E), \tag{12}$$

$$\begin{aligned}\Sigma^{in}_{OP}(i,i,E) =& D_{OP} * [(n_\omega + 1) * G^n(i,i,E+\hbar\omega) \\ &+ n_\omega * G^n(i,i,E-\hbar\omega)],\end{aligned} \tag{13}$$

$$\begin{aligned}\Sigma^{out}_{OP}(i,i,E) =& D_{OP} * [(n_\omega + 1) * G^p(i,i,E+\hbar\omega) \\ &+ n_\omega * G^p(i,i,E-\hbar\omega)].\end{aligned} \tag{14}$$

For AP scattering and OP scattering, in this study, the two coupling constant are set as $D_{AP} = 0.01\,\mathrm{eV}^2$ and $D_{OP} = 0.07\,\mathrm{eV}^2$. The phonon energy is set as $\hbar\omega = 180\,\mathrm{meV}$. The Bose-Einstein distribution function is defined as:

$$n_\omega = 1/\exp\left(\frac{\hbar\omega}{K_B T} - 1\right), \tag{15}$$

where $\hbar$ is the reduced Planck constant and ω the mode frequency.

In order to simplify the OP scattering self-energy computations, the real part of OP scattering self-energy is neglected ([17] suggests that it has a small impact on phonon scattering) and its imaginary part is computed as:

$$\Sigma_{OP}(E) = -\frac{i}{2}\left(\Sigma^{in}_{OP}(E) + \Sigma^{out}_{OP}(E)\right). \tag{16}$$

In **Step 3**, after building the phonon scattering self-energies, the GNR transport computation model checks G^r change between current iteration and previous iteration. If the variation is bigger than 1%, then go back to Step 2, otherwise, the Poisson's equation is solved (by a 3D Poisson solver) to compute the graphene potential self-consistently [18], [19].

In **Step 4**, after the Poisson's solver has converged, the transmission function T(E), which models the probability of one electron being transmitted from the source contact to the drain contact, is computed as a function of energy as:

$$T(E) = \mathrm{Trace}\left[\Gamma_S(E)\, G^r(E)\, \Gamma_D(E)\, G^a(E)\right]. \tag{17}$$

Finally, the Landauer-Büttiker formalism is utilized to derive GNR's current and conductance as:

$$I = \frac{q}{h}\int_{-\infty}^{+\infty} T(E)\cdot\left(f_0(E-\mu_1) - f_0(E-\mu_2)\right)\,\mathrm{d}E. \tag{18}$$

$$G = \frac{I}{V_d - V_s}. \tag{19}$$

where $f_0(E)$ denotes the Fermi-Dirac distribution function at temperature T, μ_1/μ_2 source/drain contact Fermi energy, and h Planck's constant.

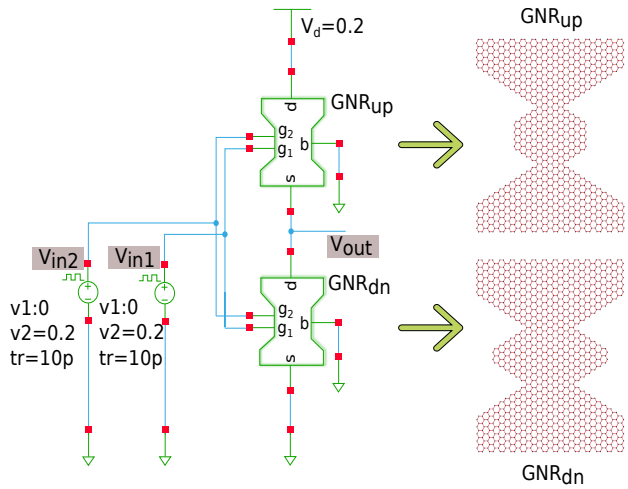

Fig. 3: Generic GNR Gate SPICE Circuit (left) and NAND2 GNRs Dimensions (right).

B. GNR Gate SPICE Simulation

To evaluate the considered GNR-based Boolean gates behavior under temperature variations, we make use of SPICE simulation in Cadence, with a simulation setup exemplified in Figure 3 for a graphene NAND gate. Two GNR devices are employed to construct a complementary style GNR-based Boolean gate, e.g., for a NAND gate, the $\mathrm{GNR_{up}}$ device captures the NAND Boolean function, while the $\mathrm{GNR_{dn}}$ device reflects the AND function [20]. We denote by V_{in1} and V_{in2} the gate inputs and by V_{out} the gate output. The back gate is connected to ground (0 V) and V_{d} is set to 0.2 V, which means that in terms of gate output voltage 0.2 V means logic "1" and 0 V logic "0". Gate inputs rise and fall times are set to 10 ps. We vary the temperature from $-55°C$ to $125°C$, which covers commercial, industrial, and military ranges, and measure for each considered gate , i.e., INV, BUFF, AND2, NAND2, OR2, NOR2 and XOR2, output signal integrity, propagation delay, and power consumption.

III. Simulation Results

In this section, we present the GNR dimensions and topologies of the GNR-based gates, and evaluate their output signal integrity, propagation delay and power consumption under temperature variations by means of the proposed SPICE simulation.

A. GNR Dimensions and Topologies of Boolean Gates

Figure 4 depicts the generic GNR's topology parameters: (i) nanoribbon geometry (i.e., width W and length L, constriction width W_{c} and length L_{c}), bump width W_{b} and length L_{b}, (ii) top gate contacts topology (i.e., contact width $W_{V_{\mathrm{g}}}$ and position relative to the drain and source contacts $P_{V_{\mathrm{g}}}$). Table I summarizes the complementary Boolean gates' GNR dimensions and topologies expressed in terms of the unit value a (0.142 nm).

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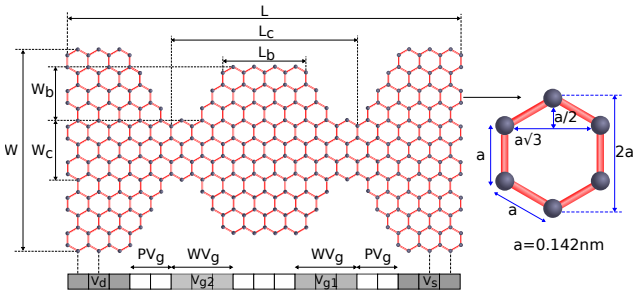

Fig. 4: GNR Dimension and Topology Parameters.

TABLE I: Complementary Boolean gates GNR dimensions and topologies.

		(W, L)	(W_c, L_c)	(W_b, L_b)	(P_{V_g}, W_{V_g})
INV	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(10\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(6\sqrt{3}, 6\sqrt{3})$
BUFF	GNR_{up}	$(47, 25\sqrt{3})$	$(11, 4\sqrt{3})$	$(0, 0)$	$(12\sqrt{3}, 6\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(12\sqrt{3}, 6\sqrt{3})$
AND2	GNR_{up}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(2, 2\sqrt{3})$	$(2\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(4\sqrt{3}, 6\sqrt{3})$
NAND2	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(3\sqrt{3}, 6\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(3\sqrt{3}, 6\sqrt{3})$
OR2	GNR_{up}	$(47, 25\sqrt{3})$	$(11, 4\sqrt{3})$	$(0, 0)$	$(1\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(5, 4\sqrt{3})$	$(4\sqrt{3}, 3\sqrt{3})$
NOR2	GNR_{up}	$(41, 27\sqrt{3})$	$(14, 6\sqrt{3})$	$(2, 2\sqrt{3})$	$(2\sqrt{3}, 6\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(4\sqrt{3}, 3\sqrt{3})$
XOR2	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(5, 4\sqrt{3})$	$(3\sqrt{3}, 6\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(8, 2\sqrt{3})$	$(4\sqrt{3}, 6\sqrt{3})$

B. GNR Gates Performance Robustness under Temperature Variations

Table II summarizes our simulation results in terms of percentage variation of gate output level for logic "1" (V_{OH}) and logic "0" (V_{OL}), propagation delay (τ_{pd}), and power consumption (P). All reported percentages are relative to the values obtained at room temperature $27°C$ (listed in Table II right bottom inset). One can observe that, for all gates, starting from a certain threshold temperature (inbetween $0°C$ and $27°C$), with temperature decrease the following trends are in place: (i) output signal levels get closer to the supply rails voltages - for logic "1" (from -0.48% to -2.29% closer) and for logic "0" (from -0.34% to -1.94% closer), (ii) power consumption decreases (from -22.8% to -85.1%), while (iii) propagation delay gets worse (from 3.2% to 147.1% increase). When increasing T above the temperature threshold, the trend reverses: (i) output signal levels deteriorate from 1.11% to 5.32% for logic "1" and from 1.11% to 4.26% for logic "0", (ii) power consumption increases from 52.1% to 397.4%, while (iii) propagation delay decreases from 3.3% to 58.4%. Overall, across the considered temperature range ($-55°C$ to $125°C$) the following observations are in place: (i) V_{OH} and V_{OL} worst degradation is 5.32% for INV and 4.26% for OR2, respectively, which suggests robustness of GNR-based gates with respect to temperature variation, (ii) gates switch up to $2.47\times$ slower for INV (but still $1.61\times$ faster than CMOS FinFET 7nm at $27°C$), and (iii) gates consume up to $5\times$ more power for OR2 (but still $395\times$ less power than CMOS FinFET 7nm counterpart at $27°C$).

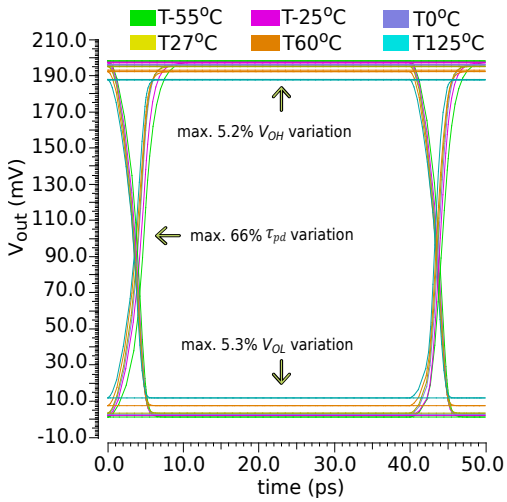

Fig. 5: GNR NAND2 Gate Eye Diagram (% variations are between min and max values).

The eye diagram for the 2-input GNR NAND gate output voltages depicted in Figure 5, reveals that the maximum variations for V_{OH} and V_{OL} are 5.2% and 5.3%, respectively, while the maximum propagation delay variation is 66%. Table III summarizes the worst case delay (at $-55°C$) and power consumption (at $125°C$) for all GNR gates vs. CMOS FinFET 7nm counterparts at room temperature $27°C$, and indicates that even in the worst case temperature conditions GNR gates can still outperform CMOS equivalent counterparts operating at room temperature, e.g., $8.7\times$ smaler delay for XOR2 and $185\times$ less power consumption for INV. These results clearly indicate that GNR-based gates exhibit performance robustness with respect to temperature variations.

IV. Conclusions

In this paper, we performed an evaluation of temperature variations impact on the reliability and performance (output signal integrity, propagation delay, and power consumption) of GNR-based complementary Boolean gates, while taking into account phonon scattering effects on carrier transport. Our results suggest that GNR-based gates are robust with respect to temperature variations and even in the worst case condition potentially outperform room temperature operating CMOS FinFET 7nm counterparts. Our results are suggesting that GNR-based complementary gates have potential as basic building blocks for future reliable, low-power, nanoscale carbon-based electronics.

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TABLE II: GNR gates output voltage levels, delay, and power consumption variation (%) vs. temperature.

	$T[^\circ C]$	$V_{OH}[\%]$	$V_{OL}[\%]$	$\tau_{pd}[\%]$	$P[\%]$		$T[^\circ C]$	$V_{OH}[\%]$	$V_{OL}[\%]$	$\tau_{pd}[\%]$	$P[\%]$
	-55	-1.56%	-1.54%	147.1%	-85.1%		-55	-2.27%	-1.94%	22.1%	-81.3%
	-25	-1.04%	-0.94%	69.2%	-65.3%		-25	-1.66%	-1.51%	14.4%	-58.3%
INV	0	-0.80%	-0.56%	39.0%	-42.7%	BUF	0	-0.95%	-1.10%	7.8%	-43.4%
	60	2.18%	1.68%	-12.5%	112.9%		60	1.73%	1.13%	-17.3%	52.1%
	125	5.32%	4.18%	-14.2%	275.2%		125	3.52%	2.61%	-24.1%	83.7%
	-55	-2.29%	-1.72%	139.2%	-73.8%		-55	-1.54%	-1.07%	63.8%	-73.2%
	-25	-1.63%	-1.16%	57.0%	-52.4%		-25	-1.08%	-0.67%	30.2%	-34.3%
AND2	0	-1.07%	-0.52%	32.1%	-29.8%	NAND2	0	-0.48%	-0.34%	3.2%	-22.8%
	60	1.47%	1.11%	-15.8%	59.3%		60	1.37%	2.07%	-3.3%	87.9%
	125	2.57%	3.27%	-39.3%	188.0%		125	3.67%	4.21%	-44.4%	374.2%
	-55	-1.47%	-1.55%	33.1%	-74.1%		-55	-1.43%	-1.55%	119.5%	-73.6%
	-25	-0.91%	-0.96%	23.1%	-57.1%		-25	-1.08%	-1.13%	39.0%	-54.4%
OR2	0	-0.55%	-0.51%	11.0%	-33.3%	NOR2	0	-0.66%	-0.60%	5.7%	-27.9%
	60	1.67%	1.48%	-38.8%	149.5%		60	1.11%	1.85%	-37.2%	105.8%
	125	3.78%	4.26%	-58.4%	397.4%		125	2.73%	3.48%	-48.9%	250.3%
	-55	-1.52%	-1.73%	59.3%	-72.2%						
	-25	-1.04%	-1.21%	30.2%	-53.8%						
XOR2	0	-0.51%	-0.72%	13.7%	-28.0%						
	60	2.13%	1.92%	-32.1%	168.8%						
	125	4.44%	3.96%	-47.2%	367.6%						

		$V_{OH}[mV]$	$V_{OL}[mV]$	$\tau_{pd}[ps]$	$P[nW]$
$T = 27^\circ C$ Reference	INV	194.27	5.34	0.28	0.670
	BUF	193.60	5.90	0.48	0.459
	AND2	193.34	5.61	0.62	0.357
	NAND2	195.16	3.60	0.67	0.263
	OR2	195.26	4.95	0.77	0.291
	NOR2	195.25	4.96	0.64	0.316
	XOR2	195.23	5.00	0.67	0.280

TABLE III: GNR gates worst case propagation delay (at $-55^\circ C$) and power consumption (at $125^\circ C$) vs. room temperature CMOS FinFET $7\,\mathrm{nm}$ counterparts.

		INV	BUF	AND2	NAND2	OR2	NOR2	XOR2
τ_{pd}	GNR	0.69	0.58	1.48	1.09	1.02	1.40	1.06
$[ps]$	CMOS	1.11	2.04	9.62	7.56	8.31	9.18	9.17
P	GNR	2.5	0.8	1.0	1.2	1.4	1.1	1.3
$[nW]$	CMOS	462.1	470.4	588.6	541.5	553.5	452.8	592.3

REFERENCES

[1] Dennard, R. H., Cai, J., and Kumar, A., *A perspective on todays scaling challenges and possible future directions.* William Andrew Publishing, 2018.

[2] Iwai, H., "Future of nano CMOS technology." in *Solid-State Electronics*, vol. 112, 2015, pp. 56–67.

[3] Matsumoto, K., *Frontiers of graphene and carbon nanotubes - devices and applications.* Springer Japan, 2015.

[4] Yang, Z., et al., "Carbon nanotube- and graphene-based nanomaterials and applications in high-voltage supercapacitor: A review." in *Carbon*, vol. 141, 2019, pp. 467–480.

[5] Ferrari, A. C., et al., "Science and technology roadmap for graphene related 2D crystals, and hybrid systems." in *Nanoscale*, vol. 7, no. 11, 2015, pp. 4587–5062.

[6] Marmolejo, M. J., and Velasco-Medina, J., "Review on graphene nanoribbon devices for logic applications." in *Microelectronics Journal*, vol. 48, 2016, pp. 18–38.

[7] Wang, T., et al., "A review on graphene-based gas/vapor sensors with unique properties and potential applications." in *Nano-Micro Letters*, vol. 8, no. 2, 2016, pp. 95–119.

[8] Chen, Y. Y., et al., "Schottky-barrier-type graphene nano-ribbon field-effect transistors: a study on compact modeling, process variation, and circuit performance." in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2013, pp. 82–88.

[9] Yang, X., et al., "Graphene tunneling FET and its applications in low-power circuit design." in *Proceedings of the 20th symposium on Great lakes symposium on VLSI*, 2010, pp. 263–268.

[10] Moysidis, S., Karafyllidis, I. G., and Dimitrakis, P., "Graphene logic gates." in *IEEE Transactions on Nanotechnology*, vol. 17, no. 4, 2018, pp. 852–859.

[11] Jiang, Y., et al., "Graphene nanoribbon based complementary logic gates and circuits." in *IEEE Transactions on Nanotechnology*, vol. 18, 2019, pp. 287–298.

[12] Silva, F. G. R. G., Meinhardt, C., and Reis, R., "Impact of near-threshold and variability on 7nm FinFET XOR circuits." in *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2018, pp. 573–576.

[13] Igarashi, M., et al., "Study of local BTI variation and its impact on logic circuit and SRAM in 7 nm Fin-FET process," in *IEEE International Reliability Physics Symposium (IRPS)*, 2019, pp. 1–6.

[14] Datta, S., *Quantum transport: Atom to transistor.* Cambridge University Press, 2005.

[15] Akhavan, N. D., et al., "Phonon limited transport in graphene nanoribbon field effect transistors using full three dimensional quantum mechanical simulation." in *Journal of Applied Physics*, vol. 112, no. 9, 2012, p. 094505.

[16] Jiang, Y., Cucu Laurenciu, N., and Cotofana, S. D., "On carving basic Boolean functions on graphene nanoribbons conduction maps." in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5.

[17] Koswatta, S. O., et al., "Nonequilibrium green's function treatment of phonon scattering in carbon-nanotube transistors." in *IEEE Transactions on Electron Devices*, 2007, pp. 2339–2351.

[18] Wang, H., et al., "Atomistic-level hysteresis-aware graphene structures electron transport model." in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–5.

[19] Nagel, J. R., et al., "Solving the generalized poisson equation using the Finite-Difference Method (FDM)." in *Lecture Notes, Dept. of Electrical and Computer Engineering,University of Utah)*, 2012, pp. 1–18.

[20] Jiang, Y., Cucu Laurenciu, N., and Cotofana, S. D., "Complementary arranged graphene nanoribbon-based Boolean gates." in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, vol. 17, 2018, pp. 1–7.

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