A 12-bit 500MS/s PIPELINE SPLIT-ADC

by

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A thesis submitted in partial fulfillment for the degree of Master of Science

in the

Electronics Research Laboratory
Faculty of Electrical Engineering, Mathematics and Computer Science
DELFT UNIVERSITY OF TECHNOLOGY

August 2010

Declaration of Authorship

I, ROHAN SEHGAL, declare that this thesis titled, "A 12-bit 500MS/s pipeline split-ADC" and the work presented in it is my own. I confirm that:

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Abstract

Faculty of Electrical Engineering, Mathematics and Computer Science
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"Split-ADC" calibration is a digital background calibration architecture, recently proposed in [11]. It requires a much lower number of cycles to calibrate the ADC errors due to its deterministic nature, without placing any additional analog complexity. While new error estimation techniques are being explored using this architecture through simulations, a hardware platform flexible in terms of performance and power consumption is much more desirable.

A 12-bit, 500MS/s pipeline "Split-ADC" is designed in TSMC 65nm CMOS. The stage amplifiers of the pipeline ADC are designed to be power scalable so that their settling time varies linearly over a wide range of bias current. A higher power efficiency is achieved in the ADC by using the current-mirror opamp topology in the MDACs operating at 1V supply, and by removing the sample-and-hold amplifier.

The overall pipeline ADC displays a peak SNDR of 66dB at a sampling frequency of 312.5 MS/s, with the analog core of each half-ADC consuming 77.3mW. This translates into a peak figure of merit of 0.3pJ/conversion for the designed split-ADC.

Acknowledgements

Research is about exploring and looking in unknown directions. And as I try to condense my past one year's research into this thesis, I realize I could look so far because I was "standing on the shoulders of giants." While this year was filled with challenges and long working hours, it was also dotted with new learning experiences from a lot of people. And I would like to acknowledge all these people who helped me through this internship and whose contributions are reflected in every chapter of this thesis.

First and foremost, I would like to thank my supervisor, Dr. Klaas Bult for providing me this wonderful opportunity to work at Broadcom amongst an outstanding group of engineers. His knowledge and experience in analog design and his vision for this entire project was a source of inspiration and this internship would not have been possible without him. It was really a pleasure to work under his guidance.

I would like to thank my promoter, Prof. John Long for providing support and feedback on my thesis, and taking care of all the administrative tasks involved in doing a masters thesis.

I would also like to acknowledge Frank van der Goes, Jan Westra, Jan Mulder and Chris Ward for all the technical guidance and ideas they provided. Despite their own respective busy schedules, they were always forthcoming and took a lot of interest in my thesis, and I am really grateful for that. A special mention for Jan Westra without whose excellent mentorship, the layout, something I had no prior experience with, would not have seen daylight. He was a constant source of motivation and humour, and his contribution to this project is invaluable.

I would also like to thank all the other engineers at Broadcom Bunnik, in particular Erol Arslan, Xiaodong Liu, Davide Vecchi, Hakan Ilgaz, Emre Ayranci,

Johan van der Tang and Emmanuele Lopelli, for the numerous technical discussions and advice.

Els was always there for helping me out with all the administrative tasks, assisting with things ranging from residence permit to housing to helping me move. Thanks for making my life a lot easier!

I would like to thank Prof. Wouter Serdijn and Prof. Kofi Makinwa for serving on my thesis committee. I am also indebted to Prof Serdijn for everything he has done for me. The time spent working under him at the Biomedical Electronics group was a valuable learning experience.

I am grateful to all my friends in Netherlands and India who provided company and encouragement during frequent bouts of home-sickness, and some great memories to be cherished for life.

Leaving my family to come to the Netherlands was not an easy move, and I express my heart-felt gratitude to my sister and parents without whose support and sacrifices, my dream of pursuing graduate studies at TU Delft would not have been realized.

Finally I'd like to dedicate this thesis to my both sets of grandparents who, though were peripheral figures in my upbringing, still touched my life in countless little ways. I wish I had more time with you ...

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Chapter 1

Introduction

The past 40 years have seen a coordinated effort by the semiconductor industry to move towards smaller feature sizes on silicon leading to more densely integrated circuits. This aggresive realization of Moore's law has made available powerful digital computing at smaller costs. However, the digital processing blocks still depend on analog interface circuitry to convert the real world signals into digital and vice versa, hence, increasing the requirements from analog interface circuits and data converters. Coupled with the fact that analog circuits only partially benefit from technology scaling, attaining higher speeds while facing other constraints due to lower supply voltages, the performance of data converters has always been the bottleneck for the entire chip. This has spurred on large-scale research on design of high-performance data converters without an excessive amount of power consumption.

1.1 Digital Calibration

While analog performance has improved in deep submicron technology in terms of speed, lower intrinsic gain and voltage swings limit the precision of the analog circuits. These limits can be alleviated by exploiting the low cost digital processing available, to correct for any errors arising from insufficient gain, linearity or

component mismatch. This digital calibration can be implemented through standard digital blocks at only a fraction of the power and area and hence making the system much more energy efficient.

Calibration algorithms can broadly be classified into two categories - statistical and deterministic. Statistical methods rely on modulating the input signal with a pseudo-random (PR) number sequence, and then retrieving it at the end by correlating the output with the same sequence [7, 22, 24]. The majority of the calibration algorithms published in literature are based on this principle, as the use of PR signals allows the calibration to run in background without interrupting the conversion. The PR sequence normally used is made small in order to conserve the dynamic range at the input. However, this increases the averaging time required to extract the PR sequence from the ADC output. For instance, in [17], the number of conversion cycles required for achieving an N-bit linearity was emperically shown to be 2^{2N} cycles, making production testing problematic at lower resolutions to impossible for high resolution ADCs.

Deterministic calibration techniques don't require a long averaging as they operate on the error signal directly, and hence take much less time. Most of the deterministic techniques published are either foreground as they involve taking the ADC offline and using a known analog calibration signal as input [8] or use a smaller and more precise ADC [4], increasing the analog complexity multifold.

1.2 Split ADC Calibration

In [11, 15, 17], a new calibration architecture was proposed which was both deterministic and background in nature. In this architecture, the ADC is split into two identical halves, as shown in fig 1.1, with each slice consuming half the total power and area. The two half ADCs work on the same input signal and by averaging their outputs, the original thermal noise floor and resolution is achieved without

any extra power or complexity. Since the two ADC halfs are designed to be identical, their outputs should also be identical. Any non-zero difference of the two half ADC outputs represents the non-idealities in the ADC paths, and hence can be used by the calibration as the error signal. By taking the difference, the input signal is cancelled out, making the error signal directly available to the calibration engine, allowing it to converge much faster.

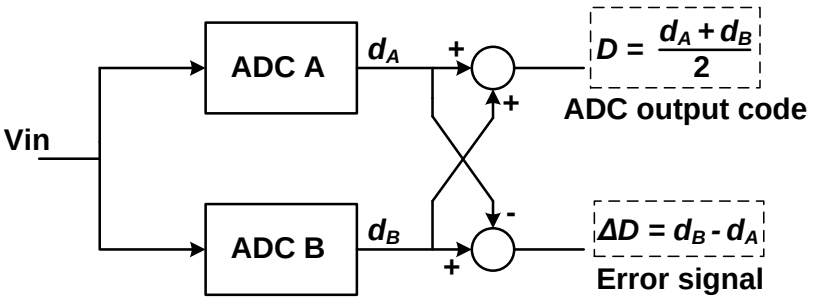


FIGURE 1.1: Split ADC architecture

While taking the difference cancels out the input signal, it also suppresses any identical errors made by the two ADC halfs. Hence, it is necessary to add some kind of asymmetry between the two half ADCs. This can be done by adding offset by either shifting the input signal for one of the ADC halves [15, 17], or shifting the decision levels for the coarse ADC [11]. As this calibration method is still relatively new, investigations are going on towards utilising this architecture in a more efficient way without sacrificing input dynamic range or overrange. It is alse being applied to correct for different kinds of non-idealities and promises much faster and elegant solutions for calibrating ADCs.

1.3 Motivation

The effectiveness of any calibration scheme can be gauged from the calibration time required and the power savings achieved through relaxation of the analog performance. While the excessive time taken by top level transient simulation

of the whole ADC could itself make the entire power optimization process prohibitive, the simulations also don't accurately reflect many non-ideal effects which affect the ADC performance. Hence, to test and compare calibration algorithms, a flexible hardware platform is required which not only presents a much more accurate reflection of the ADC performance but also gives the output in real time, making testing much less time consuming.

In this dissertation, a high speed 12-bit pipeline split-ADC sampling at 500MSamples/s is presented. The ADC was designed to be programmable in terms of performance of analog blocks and is aimed at being a good platform for testing calibration algorithms based on split-ADC architecture. While the calibration itself is aimed at being the major power saver, a few other features and design choices have been implemented in order to design a high-performance, energy efficient pipeline ADC. The ADC was designed in 65nm CMOS technology to highlight the challenges and design trade-offs faced in analog design in deep submicron technology and techniques to deal with them.

1.4 Organization

Chapter 2 briefly describes the important ADC performance parameters and reviews the pipeline ADC architecture. Chapter 3 presents an analysis of the building blocks for a pipeline ADC and their design issues. Chapters 4-5 cover the design of the pipeline split-ADC. Chapter 4 is devoted to the design details and simulation results of the multiplying digital-to-analog converter (MDAC), one of the key blocks of pipeline ADC. The design and simulation results of the remaining ADC blocks and top-level implementation of the pipeline split-ADC are presented in chapter 5. Chapter 6 concludes this dissertation and talks about the future scope of work.

Chapter 2

Background

This chapter begins with an overview of some of the important performance parameters used for characterizing data converters. The second section discusses the pipeline ADC architecture, covering system level design and error correction through 1.5bit/stage topology.

2.1 A/D converter performance metrics

Differential non-linearity (DNL) is defined as the deviation of the step size in a non-ideal data converter from the ideal size. If X_k is the transition point between successive codes k-1 and k, then the DNL of the ADC can be expressed as -

$$DNL(k) = ((X_{k+1} – X_k) - LSB)/LSB \tag{2.1}$$

where LSB is the ideal step for that particular ADC.

The input-output transfer characteristic for a 3-bit ADC is shown in fig 2.1. A positive or negative DNL implies a wide or narrow code, respectively. For DNL less than -1 LSB, the corresponding digital code is skipped, and the ADC is said to have a missing code. For most applications, maximum DNL of an ADC is desired

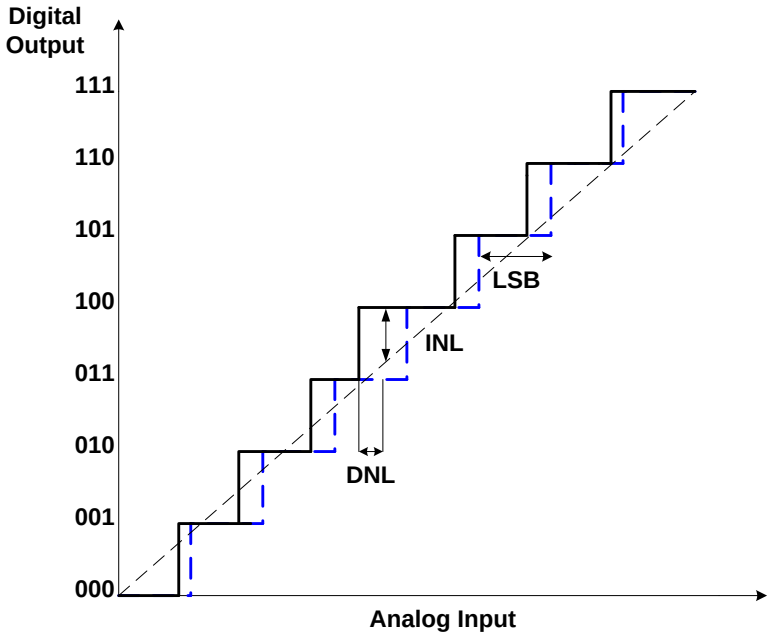


FIGURE 2.1: Transfer function for a 3-bit ADC

to be smaller than 0.5LSB.

Integral non-linearity (INL) is defined as the deviation of the actual transfer function from the straight line passing through the mid-points of the ideal input-output characteristic. The INL can be expressed as

$$INL(k) = \sum_{l=0}^{k} DNL(l) \tag{2.2}$$

However, usually it is measured as the deviation with respect to a best-fit line. The use of best-fit line corrects for any gain and offset errors, which are acceptable in many applications, and gives more information about harmonic distortion. [18]

Signal-to-noise ratio (SNR) is the ratio of the signal power to the total noise power at the output. It is normally expressed as -

$$SNR = 10 \log \left(\frac{\text{signal power}}{\text{total noise power}} \right) \text{ dB} \tag{2.3}$$

SNR is usually measured for a sinusoidal input and is limited by the quantization and thermal noise of the ADC. The ADC quantization noise is given as -

$$SNR = 6.02N + 1.76\,\text{dB} \tag{2.4}$$

where N is the resolution of the ADC.

Spurious free dynamic range (SFDR) is the ratio of the power of the signal to that of the largest spurious component. It is heavily dependent on the input signal. For large input signals the dominant spurious tone is caused by the harmonics of the signal, while for small inputs, tones generated by the DNL-type non-idealities of the ADC become dominant.[19]

Total Harmonic Distortion (THD) is defined as the ratio of the root-mean-square (RMS) sum of all the harmonic components to the amplitude of the fundamental in a certain frequency band.

$$THD = 20\log\frac{\sqrt{\sum_{i=2}^{j} A^2(kf_{in})}}{A(f_{in})} \tag{2.5}$$

where $A(kfin)$ is the amplitude of the harmonic tone present at k-th multiple of input frequency fin.

Intermodulation distortion (IMD) appears for a multi-tone input signal, as the non-linearity of the ADC results in the mixing of the spectral components, generating tones at sum and difference of integer multiples of the input frequencies. It is calculated as the ratio of the rms sum of these tones to the fundamental.

Signal-to-noise and distortion ratio (SNDR) is the ratio of the power of the fundamental to the total noise and distortion power within a certain frequency

band, and can be written as

$$SNDR = 10\log\left(\frac{\text{signal power}}{\text{total noise and distortion power}}\right)\text{ dB} \tag{2.6}$$

SNDR is dependent on both the amplitude and the frequency of the signal. At low input levels, SNDR is limited by noise, while distortion dominates for higher signal levels.

Effective number of bits (ENOB) of an ADC is a measure determined from the SNDR

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.7}$$

Effective Resolution Bandwidth (ERBW) is defined as the input frequency where the SNDR has dropped by 3dB (or 0.5 bit ENOB). ERBW provides a measure for the signal bandwidth that can be handled by the ADC. Usually, the input signal frequency must be lower than the Nyquist frequency to avoid aliasing. However, for sub-sampling ADCs, the effective bandwidth can be well above Nyquist frequency.

Figure of Merit (FoM) is a simple metric used to measure the energy efficiency of an ADC. While a number of FoMs have been proposed, the most popular one [25] takes into account the power consumption, signal bandwidth and the effective resolution of the ADC in the following way

$$FoM = \frac{\text{Power Consumption}}{2^{ENOB}.(2 \times f_{in})} \tag{2.8}$$

where f_{in} is the minimum of ERBW and Nyquist frequency.

Though FoM provides a quick and easy way to compare ADCs, it doesnt present a complete picture of the performance and hence should not be used as the sole

criterion for judging the ADC performance.

2.2 Pipeline ADC

There are several ADC architectures which are suitable for at least one or more performance specifications described in the previous section. In this dissertation, pipeline ADC is chosen as the architecture because of its high scope for application of elaborate error correction techniques. This section presents a system-level review of the pipeline ADC architecture.

2.2.1 Overview

Pipeline ADCs are amongst the most popular architectures for high-speed applications. In a pipeline A/D converter, quantization is broken down in multiple steps performed by a cascade of similar stages. By inserting a sample-and-hold operation at the beginning of each stage, all the stages can be made to operate concurrently. This enables a conversion throughput equal to that of a flash ADC, though with increased latency. The block diagram of a pipeline ADC is shown in fig 2.2.

The input signal is captured by the Sample-and-Hold amplifier (SHA) and quantized by a low-resolution coarse ADC. This digital input is then converted back to an analog signal by a sub-DAC and subtracted from the input signal. The resulting residue is basically the quantization error of that stage, ε_{qi}, which is then passed onto subsequent stages for further digitization. In order to keep the dynamic range of the input signal for each stage identical, the residue at each stage is amplified by a precision gain amplifier with a gain of A_i (nominally equal to 2^{n_i} where n_i is the resolution of the coarse ADC of i-th stage) to increase the residue to full-scale. The transfer characteristic of a pipeline stage with a 2-bit coarse ADC is shown in fig 2.3.

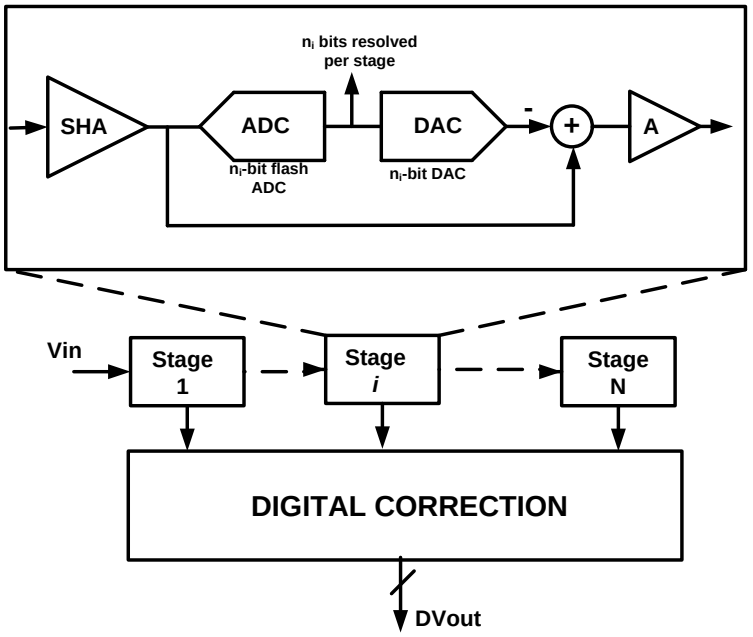


FIGURE 2.2: Pipeline ADC block diagram

The ADC is operated on a two-phase clock, with the sampling and conversion operations performed in the two phases. The stages operate in a complementary fashion, as shown in Fig 2.4. This ensures maximum throughput as new data is available at the output at every clock cycle. However, with every stage a latency

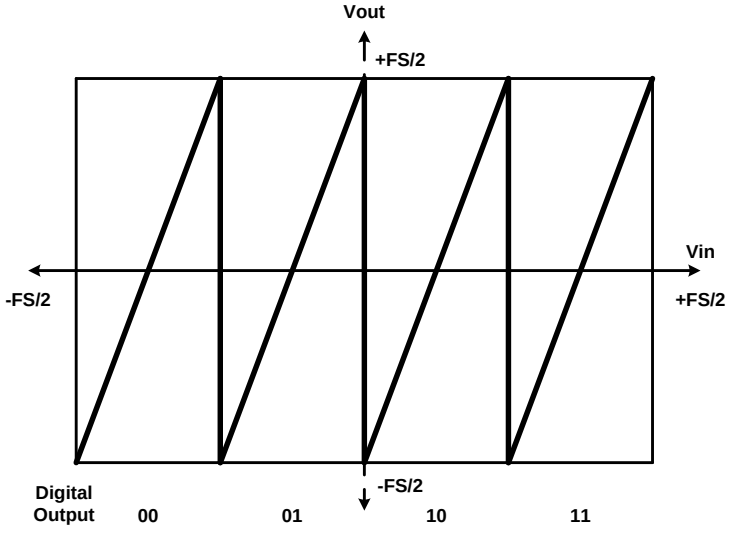


FIGURE 2.3: Stage Transfer Characteristic

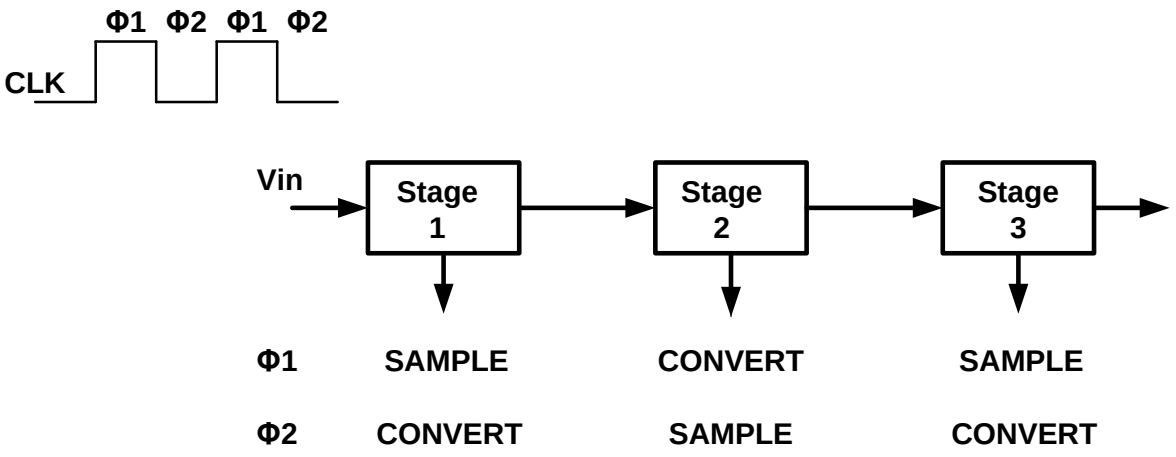


FIGURE 2.4: Concurrent Stage Operation

of 1/2 clock cycle is introduced. The digital bits can be aligned using a shift register.

The overall resolution of the pipeline ADC is given by the sum of effective resolutions of the individual stages. The number of bits left to be resolved is maximum at the input of the first stage and decreases with every stage down the pipeline. Since the dynamic range of the input signal for each stage remains the same, the precision requirements reduce with every passing stage. Hence, while the first stage needs to work at full resolution, the accuracy of the remaining stages can be scaled according to the gain in the pipeline chain to save power [6].

2.2.2 Error Correction

Non-idealities in the pipeline stage arising from comparator offset in the course ADC can lead to incorrect output codes. Fig 2.5 shows the coarse ADC and the transfer characteristic of a 1-bit stage. The reference levels for the sub-DAC are placed at the middle of each subrange, $\pm$Vref/2 and the threshold of the comparator is set in the middle of this range at 0V. Hence, the input signal is either added or subtracted by Vref/2, depending on the output of the comparator. The residue

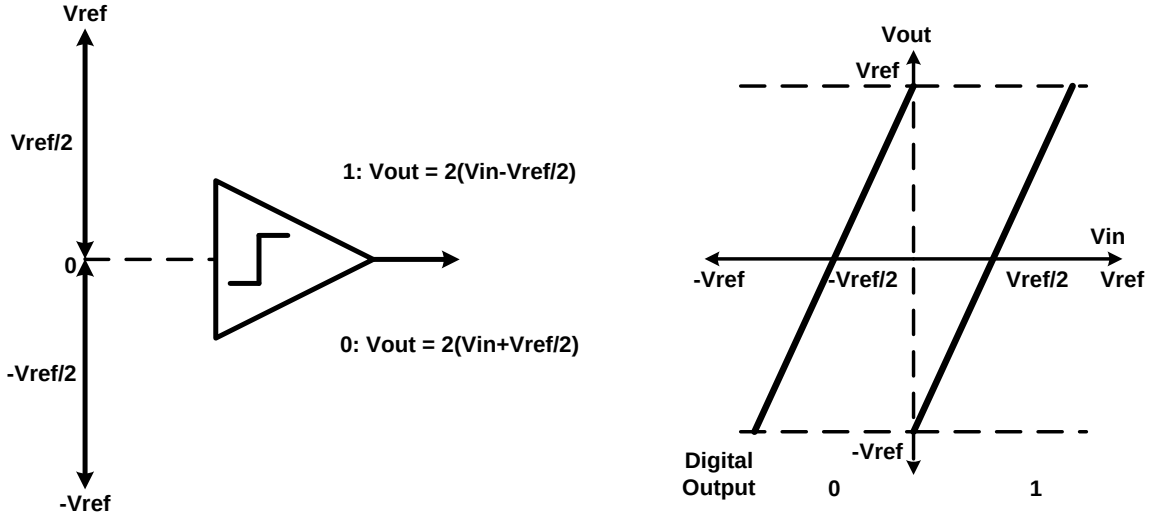


FIGURE 2.5: 1bit/stage - Coarse ADC and transfer function

is then amplified by a gain of 2, bringing the residue back to full-scale swing of ±Vref. This configuration calls for highly precise comparators, as any input offset would generate a residue with a dynamic range greater than full-scale. This causes an overrange error, while also saturating the amplifier, as shown in fig 2.6. The following stage cannot convert the out-of-range signal properly, hence producing a wrong code.

To relax the accuracy requirements on the comparator, redundancy is added to the stage with an extra subrange between ±Vref/2 by using an additional comparator in the coarse ADC, as shown in fig 2.7. The sub-DAC reference level corresponding to the extra subrange is placed at the centre at 0V, and thresholds for the two comparators are placed symmetrically around 0V at ±Vref/4. Hence, the residue is generated from the input signal by subtracting Vref/2, 0 or -Vref/2, for a coarse ADC output of 10, 01 or 00, respectively. The residue in the middle range is limited to ±Vref/2, leaving an overrange of ±Vref/2 at the output. Hence, due to a gain of 2, the maximum error in the comparator thresholds that
can be tolerated by the stage is ±Vref/4. Since the number of comparators used is between 1bit and 2bit resolution, this stage is referred to as 1.5b/stage. As the effective resolution of the stage is 1bit, a 12bit ADC can be realised using ten

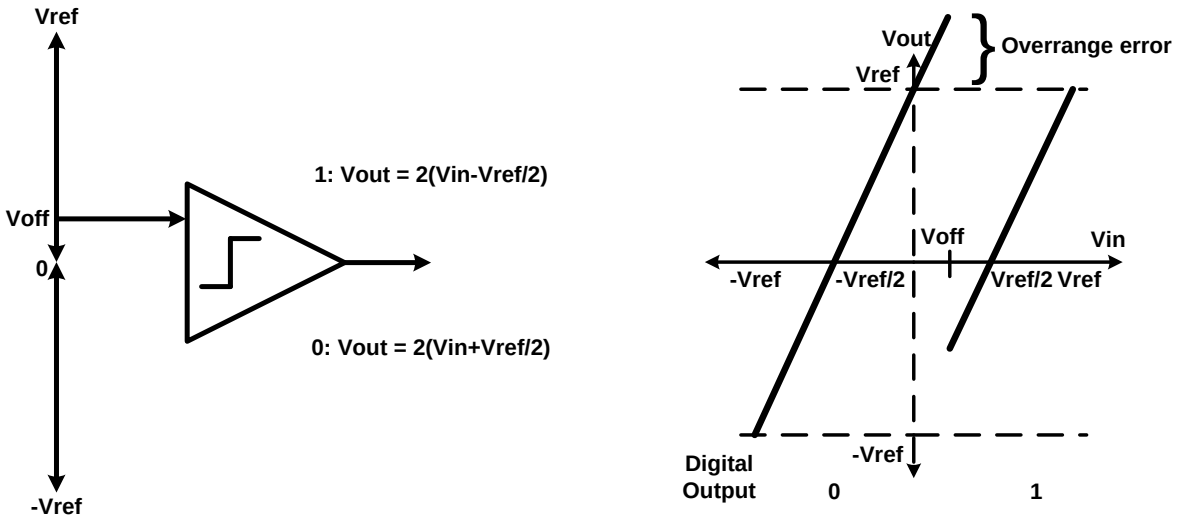


FIGURE 2.6: 1b/stage - Coarse ADC with offset, and transfer function

1.5bit stages followed by a 2-bit flash. Because the gain of the stage amplifier is 2, the final output code can be obtained by shifting bits from each stage by 1 position and adding them, as shown in an example in fig 2.8.

While error correction using 1.5b/stage relaxes the accuracy requirements on the comparator, it requires an extra comparator and additional digital complexity.

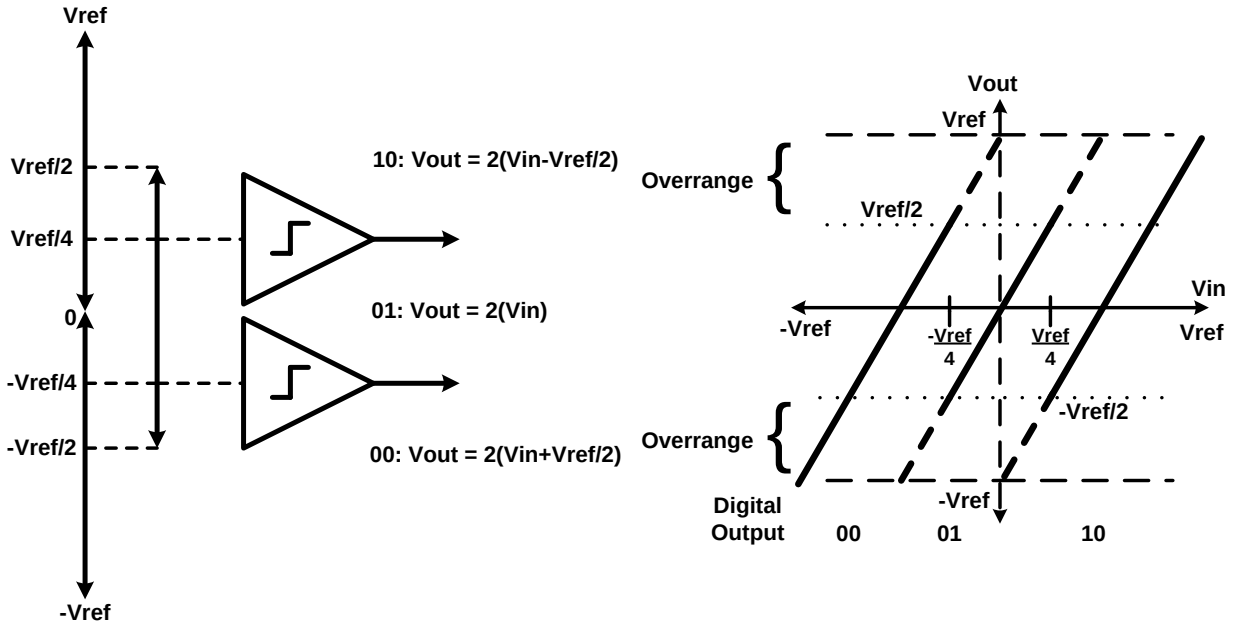


FIGURE 2.7: 1.5b/stage - Coarse ADC and transfer function

Stage	Output Code	
1	0 0	
2	1 0	
3	0 1	
4	0 1	
5	1 0	
6	1 1	
7	1 1	
8	0 1	
9	1 1	
10	0 0	
Flash	1 0	
Total	0 1 1 0 1 0 1 0 0 1 1 0	

FIGURE 2.8: Calculation of output code for 1.5b/stage

Also, errors caused by sub-DAC and amplifier are not compensated by this architecture, and require separate digital calibration techniques.

2.3 Summary

In this chapter, a review of some of the important metrics used to describe the ADC performance was presented. A system-level introduction to pipeline ADC was given. ADC non-idealities, such as comparator offset, have an adverse affect on ADC transfer characteristics. The errors introduced by these non-idealities were briefly illustrated and error correction through the use of digital redundancy in 1.5b/stage topology was explained.

Chapter 3

ADC Design Requirements

This chapter discusses the key building blocks for the pipeline ADC, and analyses some of the design requirements and issues associated with them.

3.1 Multiplying digital-to-analog converter (MDAC)

As discussed in section 2.2.1, every stage in a pipeline ADC consists of a S/H, coarse ADC, sub-DAC, subtractor and a stage amplifier. Out of these functions, sampling, DAC, subtraction and amplification can be combined into a single switched-capacitor circuit referred to as the multiplying DAC (MDAC), shown in fig 3.1 [14]. The circuit operation is divided into two clock phases, $\phi 1$ and $\phi 2$. In $\phi 1$, the input signal is sampled on the sampling cap, Cs, while the op-amp is in reset mode with its inputs and outputs shorted to ground. The charge on the two capacitors is given by -

$$Q_{Cs} = CsVin, Q_{Cf} = CfVin \tag{3.1}$$

At the beginning of $\phi 2$, the output code of the coarse ADC is available to the sub-DAC, and appropriate reference levels are connected to the input of Cs accordingly.

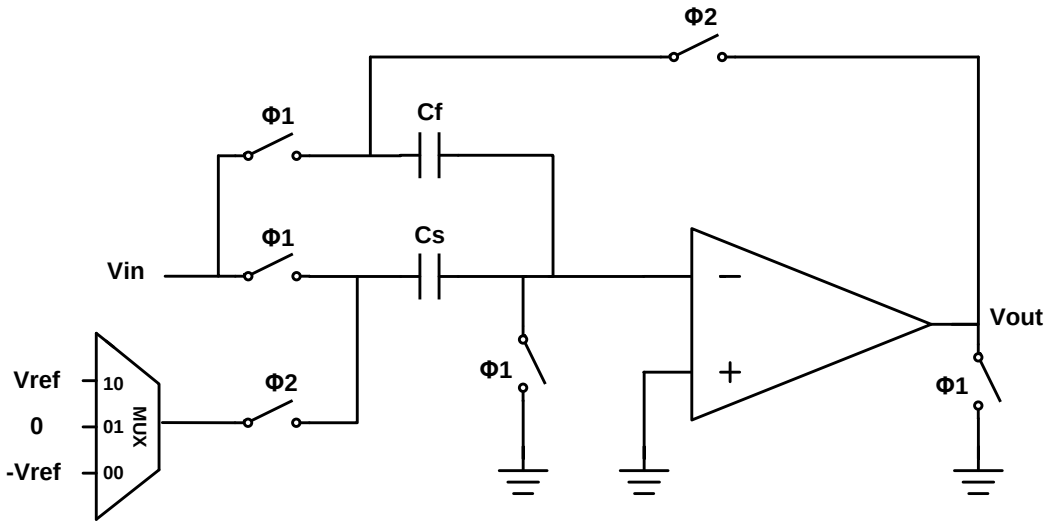


FIGURE 3.1: MDAC

In this phase, the feedback capacitor, Cf, is flipped around and connected in feedback across the op-amp, and the difference between the input signal and the DAC output is amplified through charge transfer between Cs and Cf. The three possible cases are -

Case I 00: -Vref is selected

$Q_{Cs} = -CsVref,\ Q_{Cf} = CfVout$

Applying charge conservation: $CfVout - CsVref = CsVin + CfVin$

$$Vout = \frac{(Cs + Cf)}{Cf}Vin + \frac{Cs}{Cf}Vref \tag{3.2}$$

In 1.5bit/stage, Cs = Cf. Therefore -

$$Vout = 2Vin + Vref = 2(Vin + \frac{Vref}{2}) \tag{3.3}$$

Case II 01: 0 is selected

$Q_{Cs} = 0,\ Q_{Cf} = CfVout$

Hence, through charge conservation: CfVout = CsVin + CfVin

Thus, Vout = 2Vin

Case III 10: Vref is selected
Q_{Cs} = CsVref, Q_{Cf} = CfVout

Applying charge conservation: CfVout + CsVref = CsVin + CfVin

$$\text{Vout} = \frac{(\text{Cs} + \text{Cf})}{\text{Cf}}\text{Vin} - \frac{\text{Cs}}{\text{Cf}}\text{Vref} \tag{3.4}$$

For Cs = Cf,

$$\text{Vout} = 2\text{Vin} - \text{Vref} = 2(\text{Vin} - \frac{\text{Vref}}{2}) \tag{3.5}$$

This implementation of the MDAC is based on a charge amplifier. The difference lies in the fact that in the MDAC, the feedback capacitor is also used for sampling the input signal in $\phi 1$, and is connected in feedback only during $\phi 2$. This lowers the feedback factor of the amplifier in phase 2, making it faster. This architecture is called flip-around MDAC.

To reduce the effect of charge injection from the switches, bottom-plate sampling is implemented by turning off the switches connected at the inputs of the op-amp early. This almost entirely eliminates the signal dependent offset and the independent component can be cancelled by a differential implementation.

3.2 MDAC Design considerations

The MDAC plays a decisive role in determining the overall pipeline ADC performance. Hence, it needs to be designed according to certain requirements in order for the ADC to achieve the desired performance. This section derives the specifications of the MDAC building blocks and discusses some of their design issues.

3.2.1 Op-amp gain and bandwidth

When an ideal opamp is connected in feedback, the overall gain is determined simply by the feedback network. However, due to the finite gain and bandwidth of the opamp, there will be a gain error in the MDAC. Consider an opamp with gain A connected in negative feedback with a feedback factor of β. The overall transfer function is given by -

$$\mathrm{H} = \frac{-\mathrm{A}}{1 + \mathrm{A}\beta} \tag{3.6}$$

for A $\rightarrow \infty$, H=$-1/\beta$.Thus the relative gain error, Δ, can be expressed as -

$$\Delta = \frac{\frac{1}{\beta} - \frac{\mathrm{A}}{1 + \mathrm{A}\beta}}{\frac{1}{\beta}} = \frac{1}{1 + \mathrm{A}\beta} \tag{3.7}$$

Hence, the minimum gain required for a gain error Δ is -

$$\mathrm{A} > \frac{1}{\Delta\beta} - \frac{1}{\beta} \approx \frac{1}{\Delta\beta} \tag{3.8}$$

For 1.5bit/stage, the flip-around MDAC has a feedback factor of 0.5. Hence, in order to keep the error below half an LSB for a 12-bit resolution without calibration, A $> (2 \times 4096 \times 2) \approx$ 84dB.

Bandwidth Along with sufficient gain, the op amp also needs to have a certain bandwidth in order to achieve a minimum amount of settling accuracy. As discussed in the previous section, MDAC amplifies the signal in $\phi 2$, giving the opamp half a clock cycle to settle. If the opamp is modeled as a single pole system, its step response can be expressed as [18]-

$$h(t) = h_o(1 - e^{-t/\tau}) \tag{3.9}$$

where h_o is the transfer function of the amplifier for $t \to \infty$, given by $1/\beta$ (assuming sufficiently high DC gain) and τ is the time constant, given by $1/\omega_{3\text{dB}}$, $\omega_{3\text{dB}}$ being the 3dB bandwidth of the amplifier.

If the op-amp needs to settle to within N-bit accuracy,

$$e^{-t/\tau} = 2^{-N} \tag{3.10}$$

or,

$$t = N\tau \ln 2 = \frac{N \ln 2}{\omega_{3\text{dB}}} \tag{3.11}$$

$\omega_{3\text{dB}}$ can be written as $\beta\omega_u$, and since the opamp has half a clock cycle to finish settling -

$$\frac{1}{2fs} = \frac{N \ln 2}{\beta\omega_u} = \frac{N \ln 2}{\beta 2\pi f_u} \tag{3.12}$$

or,

$$f_u = \frac{f_s N \ln 2}{\pi\beta} \tag{3.13}$$

where f_u is the unity gain bandwidth of the opamp, and f_s is the sampling frequency of the ADC.

The above calculation implies that for a given accuracy, the settling time increases linearly with inverse of unity gain bandwidth. Unity gain bandwidth of an opamp

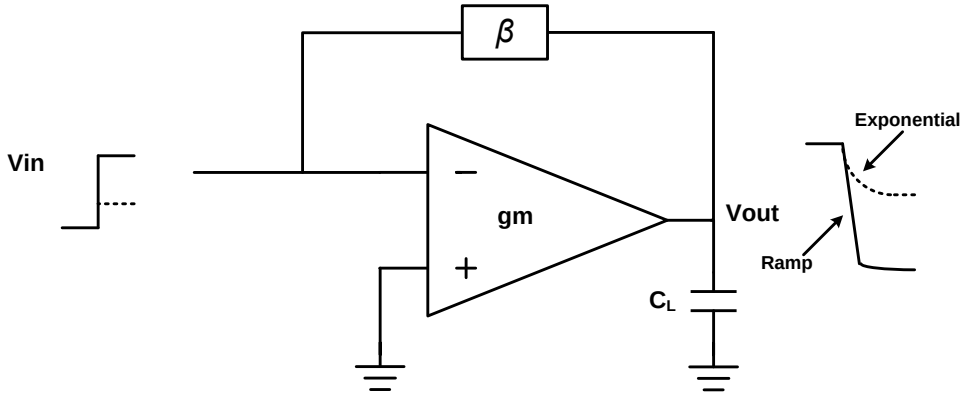


FIGURE 3.2: Slewing in an opamp

is the ratio of gm to the load capacitance. Since the load capacitance is determined by the noise budget, gm is also relatively fixed. But the unity gain bandwidth can be scaled down if the accuracy to which the opamp must settle is relaxed through digital calibration.

Slew rate As can be inferred from eqn 3.10, for an ideal single pole system, the slope of the step response is proportional to the final value of the output. This means that for a larger input step, the output would rise accordingly. In case of an opamp, this would mean supplying an ever larger current to the load. However, at maximum current, the slope becomes fixed and the output begins to change at a constant rate.

So for a small input step *Vin*, the amplifier shown in fig 3.2, provides current $gmVin$ to drive the load C_L according to the following expression -

$$\frac{dVout}{dt} = -\frac{Iout}{C_L} = -\frac{gmVin}{C_L} \tag{3.14}$$

As *Vin* increases, the current at the output also increases till it reaches its maximum value, *Imax*. For a differential pair, this current is equal to the tail current.

At this input, the output slope can be written as -

$$\frac{dVout}{dt} = -\frac{Imax}{C_L} \tag{3.15}$$

The maximum rate at which the opamp can change is called the slew rate. Opamp slewing is a large-signal effect that results in signal-dependent settling causing distortion. In order to avoid slewing, either the maximum step applied to the input should be limited, or sufficiently large bias current be provided to the opamp, to make sure that the rate of change of output voltage is determined by time constant rather than slew rate.

3.2.2 Thermal Noise

Thermal noise is one of the most important design parameters of ADC design. Due to its stochastic nature, noise is the only non-ideality that cannot be calibrated and hence, needs to be designed for carefully. In an MDAC, thermal noise can be analysed in the two clock phases, as shown in fig 3.3. In the sampling phase, the opamp inputs and outputs are grounded. Hence, the only noise generated comes from the sampling switches, which gets stored on the respective capacitors. In the amplification phase, noise from the sub-DAC and Cs gets transferred to the output through charge transfer. The noise of the opamp also gets added to the total noise. The total noise power at the output can be written as -

$$V_{nout}^2 = \left(\frac{Cs}{Cf}\right)^2 \left(\frac{kT}{Cs} + V_{nDAC}^2\right) + \frac{kT}{Cf} + \left(\frac{Cs+Cf}{Cf}\right)^2 V_{namp}^2 \tag{3.16}$$

where V_{namp} is the input-referred noise voltage of the opamp and V_{nDAC} is the output-referred noise of the sub-DAC. This expression describes the output noise for a single-ended MDAC. For a differential implementation, the noise power due to the switches and sub-DAC in the two branches are uncorrelated to each other and hence, will get added.

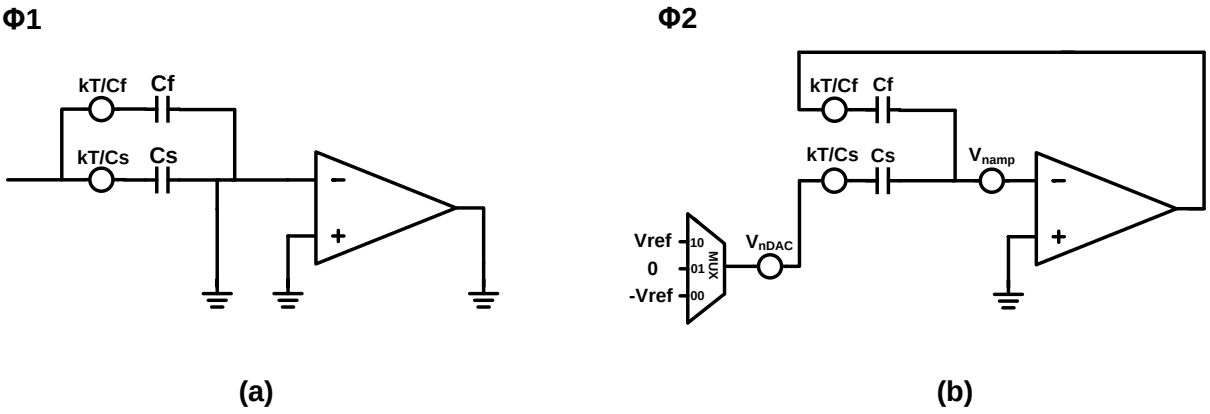


FIGURE 3.3: Noise Analysis for MDAC

ADC Noise Budget In a pipeline ADC, the overall input-referred noise budget for a given resolution can be calculated as -

$$V_{ntot,in}^2 = \left(\frac{V_{FS,diff}}{2^{N_{therm}}}\right)^2 /12 \tag{3.17}$$

where N_{therm} is the target resolution for thermal noise, in terms of number of bits, and $V_{FS,diff}$ is the full-scale signal swing at the input.

This noise represents the noise contributions of all the stages of the pipeline ADC. Since there is gain of 2x in the pipeline chain for a 1.5b/stage, the noise power generated by each stage will get successively divided by a factor of 4 when referred to the input. If stage scaling is implemented as discussed in section 2.2.1, the noise generated by each stage gets doubled as the stage capacitance is scaled by one-half. Hence, a reasonable partition of the ADC noise could be - 50% for SHA, 25% for first stage and 25% for rest of the stages. It is evident that a considerable amount of power and area dedicated to the SHA could be saved by eliminating it, as it dominates the SNR of the ADC without contributing anything towards digitization of the signal. However, there are many other issues in SHA-less architectures, which will be covered in later chapters.

3.2.3 Switches

Switches play a decisive role in deciding the bandwidth and linearity of the sampling network of the MDAC. As all switch implementations have a finite ON resistance, they should be sized large enough in order to maintain a sufficiently small time constant. The ratio of this time constant to the sampling phase determines the accuracy to which the input has been sampled on the capacitors. The ON-resistance of a MOSFET switch is given by -

$$r_{ON} = \mu C_{ox} W L^{-1} V_{gt} \tag{3.18}$$

where Vgt is the overdrive voltage, defined as $Vgs - Vt$. Hence, the width of the MOS switch can be increased to achieve lower resistance. It can be seen that r_{ON} varies with input signal, and hence leads to signal-dependent settling, in turn leading to distortion. This, however, is a problem only while sampling a continuous time signal, requiring special techniques like bootstrapping [2] or clock-boosting[5]. When sampling a discrete-time signal, simple MOS switches work fine as long as the worst-case time constant is sufficient for the sampling speed and accuracy required.

Apart from the series resistance, the parasitic capacitance of the switch also affects the performance of the switched-capacitor circuit in three major ways. Firstly, the source- and drain-to-ground caps slow down the sampling network. Secondly, the overlap caps between gate and source & drain cause clock feedthrough, where artefacts from the clock leak into the signal path adding tones in the output. Finally the charge in its inversion layer gets dumped on the switch terminals when the switch is turned off. This effect is called charge injection and causes small voltage spikes towards the end of each phase. Though it can be cancelled to a large extent by bottom-plate sampling (as explained in last section) the switch size should be kept small to minimize charge injection and other effects.

3.2.4 Capacitor matching

As the gain of the MDAC stage is determined by the ratio of two capacitors, the process variations in these caps directly affect the gain of the stage. For a gain accurate up to 12-bit resolution, the mismatch in the capacitors for the first stage should be less than 0.025%. Metal-Insulator-Metal (MIM) capacitors can attain a matching accuracy of up to 0.01% through proper optimization of process steps and layout [9]. However, they require extra masking steps and hence are not always available. They also have a relatively low capacitance density ranging from 1-5fF/μm^2, and do not scale with process techonology

Metal-metal finger capacitors consist of interdigitated parallel metal wires stacked over several metal layers, and derive their capacitance from vertical and horizontal fields on a given metal layer and between layers. Finger caps scale with technology and can achieve a capacitance density of close to 10fF/μm^2 for a feature size of 0.08μm and 6 metal layers. In 65nm process, the capacitor matching that can be achieved for finger caps is limited to 0.05-0.1%. Since this falls short for applications requiring an ENOB above 10-bit, digital calibration techniques are often used to correct for the gain errors caused by capacitor mismatch.

Apart from mismatch, voltage dependence of capacitors is also a problem in SC circuits. The capacitance of a voltage-dependent capacitor can be expressed as [23] -

$$C(V) = C_o(1 + \alpha_1 V + \alpha_2 V^2 + \ldots) \tag{3.19}$$

where α_1 andα_2 are the capacitor's first- and second-order voltage coefficients, respectively. This voltage dependence of the capacitors can introduce harmonic distortion and hence, should be as small as possible. MOS capacitors provide the highest capacitance density amongst all monolithic capacitors, but have very high voltage and temperature coefficients. Hence, their use is limited to decoupling capacitors and finger caps are almost always used for sampling and feedback

capacitors.

3.3 Comparators

Comparators form the core of all A/D converters, as they carry out the essential function of quantization. Hence, their characteristics, especially speed, offset, area and power consumption, affect the overall performance of the ADC. It is basically used to compare the input signal with a reference and generate a binary output. For applications in high-speed, high-resolution ADCs, the comparator needs to amplify a small difference between the input and the reference to a rail-to-rail swing in a very small amount of time. Hence, high gain and wide bandwidth are two important requirements for the comparator.

Another important design criterion used to measure the performance of the comparator is called bit-error rate (BER), which describes the probability of an incorrect quantization event. This results from the inability of the comparator to resolve a small differential input to a valid output decision within a certain time. This phenomenon, when the comparator output is neither 1 or 0, is called metastability, which is a source of BER. BER is an important figure in digital communication applications and most applications require a BER ranging from 10^{-9}, i.e. 1 error in a billion bits, to 10^{-15}.

The desired high-gain can be implemented by using an open loop opamp. However, as the gain-bandwidth product is fixed, it is very difficult to achieve both high gain and high bandwidth at the same time. This trade-off can be relaxed by using a cascade of amplifiers, with smaller gain and high bandwidth. For 12-bit accuracy and 1V full-scale, the comparator needs to amplify 1 LSB voltage or roughly 0.25mV, to 1V, translating into 72dB, within a certain amount of time. In practice, this gain needs to be much higher in order to have a low BER. As the time available for a comparator to make a decision is often very small, the requirements from the opamp become virtually impractical.

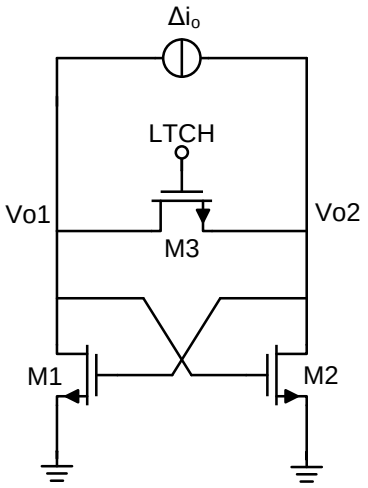


FIGURE 3.4: A Latch-type comparator

The required high-gain can also be achieved with the help of positive feedback. This is done by using a latch, as shown in fig 3.4. M1 and M2 are two common-source amplifiers connected back-to-back in positive feedback. When the LTCH signal is high, the latch outputs are shorted to each other. As soon as LTCH goes low, the swtich releases the latch to regenerate any imbalance seen by it. If an initial voltage difference, ΔV_0, is applied at the beginning of the latch phase, the settling behaviour of the latch can be described as [16] -

$$\Delta V = \Delta V_0 e^{t/\tau} \tag{3.20}$$

where ΔV is the differential output voltage. The time constant τ can be written as-

$$\tau \approx \frac{C_L}{gm} \tag{3.21}$$

where gm is the transconductance of each transistor, and C_L is the load capacitance seen at the output.

The time required by the latch to generate a voltage difference ΔV_{logic} that can

be recognized by the digital logic can be expressed as -

$$T_{LTCH} = \tau \ln \left(\frac{\Delta V_{logic}}{\Delta V_0} \right) \tag{3.22}$$

For a small enough value of ΔV_0, the comparator would display metastability, since T_{LTCH} is normally fixed by the ADC timing scheme.

Another important aspect of comparators that has a significant impact on the ADC accuracy is input-referred offset. The offset of a comparator directly creates DNL errors and hence should be made as small as possible. Latch-based comparators can have high offsets because of the unbalanced common-mode kicks due to mismatch. Often, a preamplifier is used to amplify the differential input voltage and hence reduce the input-referred offset of the latch. However, the preamplifier output should be available to the latch before the beginning of the latch phase, so that the latch begins to regenerate in the right direction. While the use of the preamplifier reduces the input-referred offset, it also adds a delay to the comparator, which should also be taken into account in the timing scheme. As discussed in previous chapter, the use of overrange greatly relaxes the offset requirements from the comparator, as offsets as high as $\pm Vref/4$ can be tolerated. The preamplifier also isolates the input and the reference from the large kickback charge generated by the latch to some extent, and hence is used in most comparator designs.

3.4 Summary

This chapter discussed some of the important buillding blocks for a pipeline ADC. Circuit-level implementation and design-related issues were presented for MDAC and comparators. Gain and bandwidth requirements were derived for the MDAC opamps for a given resolution and sampling frequency. ADC accuracy limitations due to thermal noise and capacitor mismatch were analysed. Latch-based comparators were described and their design issues were briefly examined.

Chapter 4

MDAC Design

This chapter presents the design of the first stage MDAC for the 12-bit, 500MSps pipeline "split-ADC". A number of opamp topologies suitable for low voltage implementation are surveyed and out of them, the current-mirror architecture was identified as the most optimum one and chosen for implementation. Differential gain-boosting stages are used to increase the DC gain. The design is completed by using high-swing cascode biasing and SC common-mode feedback (CMFB). The overall differential MDAC along with the switching network is presented and the design is validated through simulations.

4.1 Opamp Design

The opamp is the most power hungry block of the ADC and decides to a large extent the power consumption and the SNDR of the ADC. Hence, a majority of calibration algorithms are aimed at relaxing the requirements on the opamp, in order to lower their power consumption. Since the ADC is aimed at being a platform for testing calibration techniques, the opamp needs to possess a good degree of scalability in terms of performance and power consumption. Hence, apart from the specifications arising from the desired ADC performance, a major

design requirement from the opamp was the ablity to operate over a large range of bias current, hence being extremely power scalable.

4.1.1 Review of Opamp topologies

As the opamp was the most important block for this ADC, a major part of the design time and effort was spent on the opamp in this dissertation. A number of opamp topologies were reviewed and tested before selecting the final topology. This section presents a survey of all the topologies studied -

(A) Telescopic Opamp In a telescopic opamp, the differential pair and the active load, both use cascode devices to increase the gain, as shown in fig 4.1. As the second pole is due to the parasitic capacitance from the cascode transistors, which is relatively small, this opamp is generally the fastest amongst all architectures. And as the number of current sources, apart from the tail current source, is minimum, it has the highest gain and SNR. The gain of the telescopic opamp can be written as -

$$A = gm_1\{(gm_3ro_3ro_1)||(gm_5ro_5ro_7)\} \tag{4.1}$$

However, the major drawback of telescopic opamp is that its swing is severly limited due to 5 transistors stacked from rail-to-rail, and as a low swing places stringent requirements on thermal noise, it is not suitable for low voltage applications. Another weakness is the inability for the inputs and outputs to be shorted. This limits their application as unity-gain buffers or in switch-cap circuits with reset mechanism where the input and output are shorted to each other.

The swing limitation in a telescopic opamp can be alleviated by cascading it with a second stage. As the second stage can be optimized for high swing, a two-stage configuration can result in high-gain, high-swing opamps. However, using a second

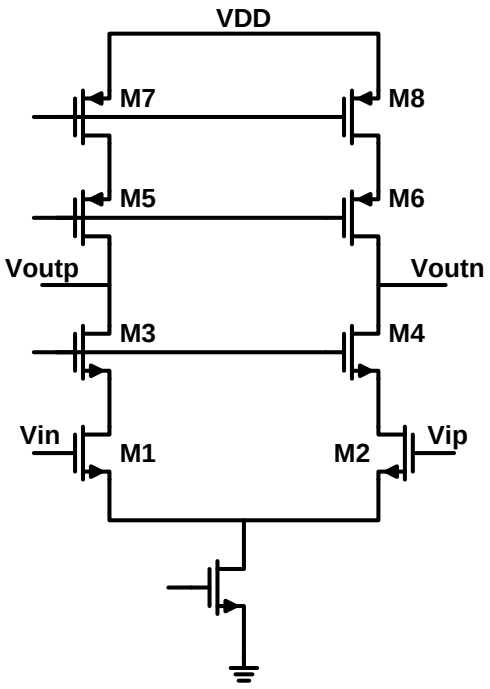


FIGURE 4.1: Telescopic Opamp

stage adds another pole in the opamp transfer function and reduces phase margin. Hence, two-stage opamps almost always need frequency compensation to stablize them, at the expense of unity-gain bandwidth. The second stage also consumes a lot of power in order to drive the load capacitance. The common-mode feedback for a two-stage opamp is also not that straightforward due to the presence of two high-impedance nodes.

The common-mode problem can be solved by using a pseudo-differential topology, where two single-ended opamps are used. This, however, comes at the cost of extra noise and power consumption, and hence was not considered for implementation.

(B) Folded-Cascode opamp The folded cascode opamp is the most popular and widely used single-stage architecture. In this topology, shown in fig 4.2, the small signal current generated from the input transistor is folded across to another path using a current source. The folding idea avoids stacking of cascode transistors on top of input transistors, hence increasing headroom and leading to larger swing. It also allows a lot more freedom in choosing the input and output common mode

levels. The folded cascode does relatively well in terms of speed, as the poles due to the current source and the cascode device in the output branch are quite far off. All the above mentioned advantages are at the expense of extra power, as nearly twice the current is required now for the same gm. Also, since there are two extra current sources, their noise contribution has a significant impact on the overall SNR. Noise of the folded cascode opamp, ignoring the contribution of the cascode devices, can be expressed as [23]-

$$V_{n,in}^2 = \frac{8kT\gamma}{gm_{1,2}} \left\{ 1 + \frac{gm_{3,4}}{gm_{1,2}} + \frac{gm_{5,6}}{gm_{1,2}} \right\} \tag{4.2}$$

where γ is a technology dependent coefficient.

There is another drawback in folded cascode opamp which begins to hurt significantly in smaller technology nodes. The gain of the folded cascode opamp can be expressed as -

$$A = gm_1\{(gm_7 ro_7 (ro_1||ro_3)||(gm_9 ro_9 ro_5)\} \tag{4.3}$$

As the output resistance of a transistor is directly proportional to its length, in deep submicron, the intrinsic gain reduces a lot. For instance, in 65nm, the gain of a single transistor can be as low as 7-8x. In a folded cascode, the gain from the input pair is reduced due to the presence of the folding current sources M3,4, whose output impedance comes in parallel to that of the input transistor. And since they carry the currents of both the input device and the output branch, the gain drops by 2-3x. Due to the already low intrinsic gain in nanoscale technologies, this much loss becomes very significant. A very low gain from the input pair results in less suppression of noise from other transistors and a relatively higher input-referred noise. Hence the folded cascode was not found to be the optimum topology for the given application in 65nm CMOS.

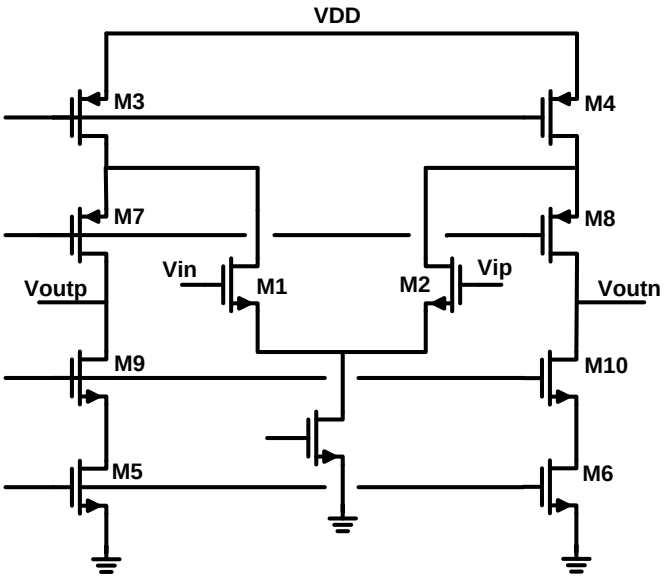


FIGURE 4.2: Folded Cascode Opamp

4.1.2 Current-mirror architecture

Apart from folding, there is another way to transfer the signal from the input pair to the output branch without stacking - mirroring. The resulting architecture is shown in fig 4.3. The differential current generated from the input pair is copied to the output branch through a cascode current mirror. Though two phase inversions take place in the signal path, it is a single-stage topology as the output is the only high impedance node in the signal path.
The gain of this opamp if given by -

$$A = Kgm_1\{(gm_9ro_9ro_5)||(gm_{11}ro_{11}ro_7)\} \tag{4.4}$$

where gm_1 is the input transconductance of the opamp, and K is the current mirror ratio.

This topology achieves a good gain, comparable to that of telescopic opamp. Since input gm gets directly multiplied by K, it can be increased to achieve the same

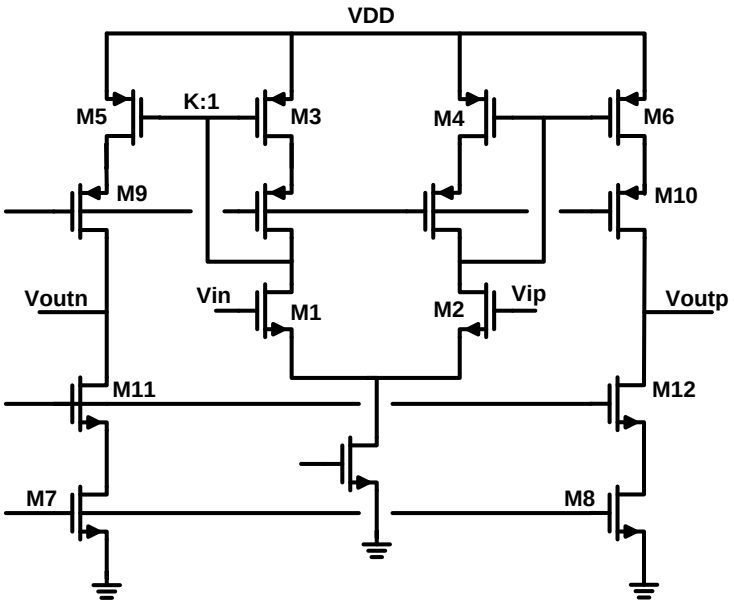


FIGURE 4.3: Current mirror architecture

unity gain bandwidth with a better current efficiency. A comparison of the current-to-gm efficiency is given in table 4.1.

For noise calculations, it can be assumed that the noise contribution of the cascode transistors is very small and hence can be ignored. Hence the overall output referred noise can be calculated as-

$$V_{n,out}^2 = 2(Av_{1,2}^2 V_{n1,2}^2 + Av_{3,4}^2 V_{n3,4}^2 + Av_{5,6}^2 V_{n5,6}^2 + Av_{7,8}^2 V_{n7,8}^2) \tag{4.5}$$

$$V_{n,out}^2 = 2\{(Kgm_{1,2}rout)^2 V_{n1,2}^2 + (Kgm_{3,4}rout)^2 V_{n3,4}^2 + (gm_{5,6}rout)^2 V_{n5,6}^2 + (gm_{7,8}rout)^2 V_{n7,8}^2\} \tag{4.6}$$

Input referred noise can be calculated by dividing the output-referred noise power

	Telescopic	Folded Cascode	Two-stage	Current Mirror		
				K=1	K=2	K=3
Current required for a unit gm	I	2I		2I	1.5I	1.33I

TABLE 4.1: Comparison of current efficiency for opamp topologies

by $Av_{1,2}^2$ -

$$V_{n,in}^2 = 2\left\{V_{n1,2}^2 + \frac{(Kgm_{3,4}rout)^2 V_{n3,4}^2}{(Kgm_{1,2}rout)^2} + \frac{(gm_{5,6}rout)^2}{(Kgm_{1,2}rout)^2}V_{n5,6}^2 + \frac{(gm_{7,8}rout)^2}{(Kgm_{1,2}rout)^2}V_{n7,8}^2\right\} \tag{4.7}$$

$$V_{n,in}^2 = 2\left\{V_{n1,2}^2 + \frac{gm_{3,4}^2}{gm_{1,2}^2}V_{n3,4}^2 + \frac{gm_{5,6}^2}{K^2gm_{1,2}^2}V_{n5,6}^2 + \frac{gm_{7,8}^2}{K^2gm_{1,2}^2}V_{n7,8}^2\right\} \tag{4.8}$$

where $V_{n,i}^2 = 4kT\gamma/gm_i$. In long channel devices, γ is derived to be equal to 2/3, but in sub-micron technologies, it is much higher [1].

This results in -

$$V_{n,in}^2 = \frac{8kT\gamma}{gm_{1,2}}\left\{1 + \frac{gm_{3,4}}{gm_{1,2}} + \frac{gm_{5,6}}{K^2gm_{1,2}} + \frac{gm_{7,8}}{K^2gm_{1,2}}\right\} \tag{4.9}$$

For $K = 1$,the noise performance is the same as the folded cascode, but for larger values of K and the same unity gain bandwidth, the gm of the input pair reduces. So while the input-referred noise power of transistors in the output branch remains the same, the noise from the input pair increases.

Another drawback of the current mirror architecture is that current mirror introduces mirror poles originating from the parasitic gate-to-source capacitances of the mirror transistors M3 and M4. They normally cause a significant drop in the opamp phase margin. But due to small transistor sizes in 65nm CMOS, the degradation in phase margin is not that large. The parasitic capacitance coupled with the large-signal square law characteristics of MOS transistors also introduces harmonic distortion. However, for discrete-time applications, settling accuracy is the most important factor and harmonic distortion is relatively less important. Hence, the current mirror architecture was found to be a good choice for applications in switch-cap circuits in deepsubmicron technologies, and was chosen for this design. The choice for the value of K involves a trade-off and was kept at 2. Higher values

of K would have achieved a better current-efficiency, but at the cost of phase margin and noise. An NMOS differential pair was chosen for its higher gm, and was biased at a common-mode voltage of 0.75V. The output common-mode voltage was kept at 0.5V in order to maximise voltage swing.

4.1.3 Gain-Boosting

As discussed in section 3.2.1, a large amount of DC gain is required to achieve

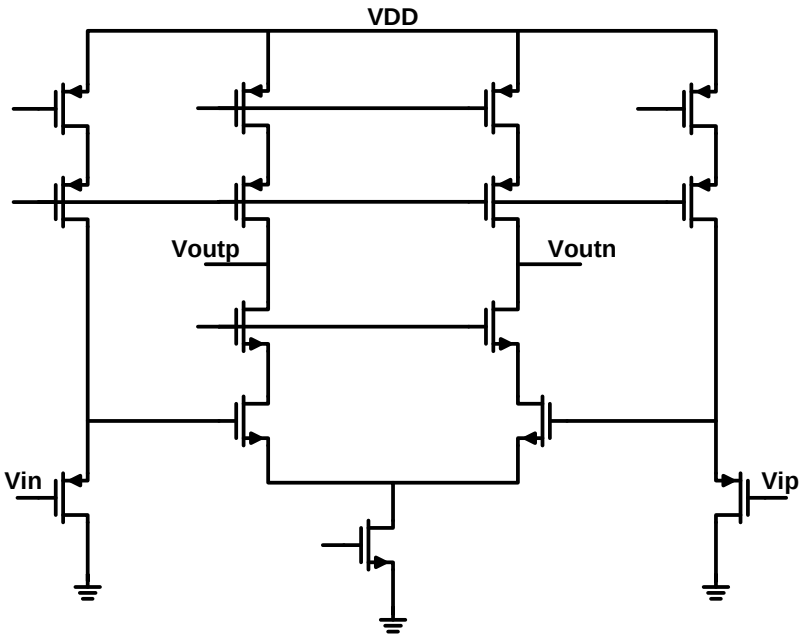


FIGURE 4.4: NMOS Gain boosting amplifier

12-bit accuracy. Gain-boosting was used to increase the gain of the opamp while still using a single-stage architecture [12]. Since the gain-boosting amplifiers don't require a large output swing, fully differential telescopic opamp were used for gain-boosting in this design. Due to low supply voltage of 1V and restrictions placed by telescopic opamp on its bias levels, source followers were used as level shifters, as shown in fig 4.4 and 4.5. Assuming the gain of the level shifters to be close to 1, the gain of the amplifier is given by eqn 4.1.

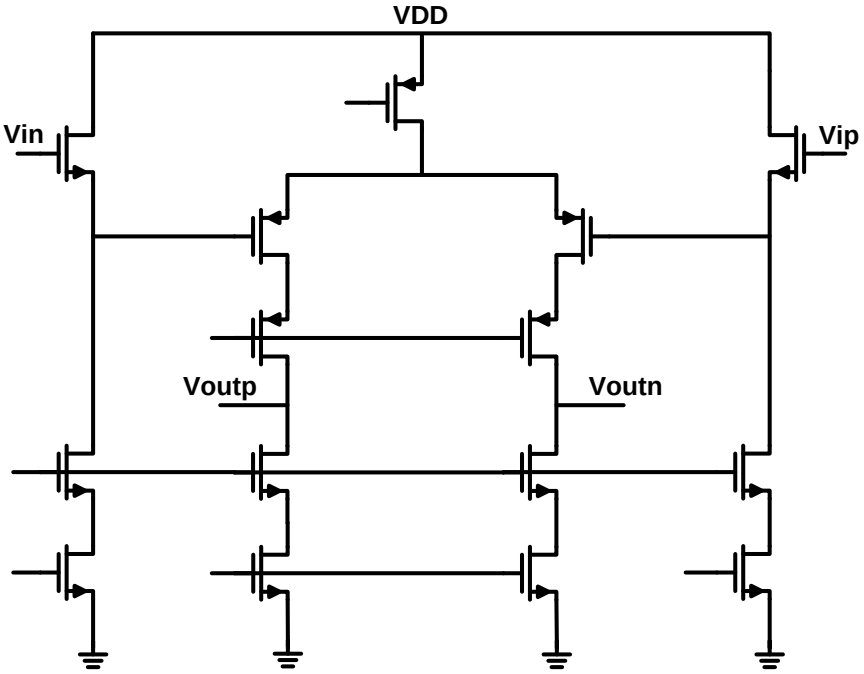


FIGURE 4.5: PMOS Gain boosting amplifier

4.1.4 Biasing

A local biasing block is used to generate the DC bias voltages for the transistors in the opamp in every pipeline stage, and is shared by the opamps in both the half ADCs. The bias block of every stage is controlled by a master current which is supplied by a global biasing. The master current is copied and distributed locally using a series of cascode current mirrors. The voltage for the cascode current mirrors is generated with the help of resistors with $Vds = Vgs - I_{bc}R$. The bias voltages for the opamp are generated by using a high swing cascode arrangement as shown in fig 4.6. For maximum swing, Vb2 should be biased just above Vgs2 + (Vgs1 - Vth1). This is done by using another diode connected transistor M3, with a (W/L) of 1/4 times of that of M1 and M2. Hence,

$$Vb2 = Vgs3 = \sqrt{\frac{I}{K3}} + Vth3 = 2\sqrt{\frac{I}{K}} + Vth3 \tag{4.10}$$

$$\sqrt{\frac{I}{K}} = Vgs1 - Vth1 = Vgs2 - Vth2 \tag{4.11}$$

$$Vb2 = (Vgs1 - Vth1) + (Vgs2 - Vth2) + Vth3 \tag{4.12}$$

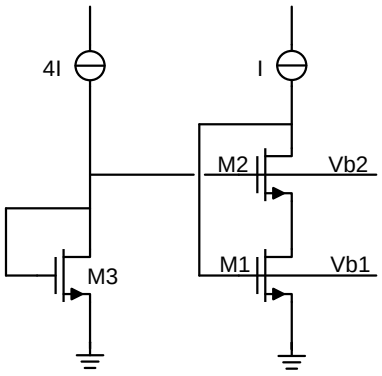


FIGURE 4.6: High swing cascode biasing

Hence, M2 and M3 should have equal lengths in order for Vth2 and Vth3 to match. There will be some inaccuracy as M2 suffers from body effect and hence its Vth would be slightly different from Vth3. Also M1 and M2 are not biased at equal Vgts. Since the noise contribution of the M1 is much higher, it is biased at higher Vgt, in the range of 150-200mV, to make its gm smaller for the given current. The noise contribution of the cascode device is pretty low, so its Vgt is made small to the tune of 50mV, to reduce its headroom consumption, by increasing its number of fingers. For all transistors, a Vds-Vgt margin of atleast 50mV is maintained in order to account for any variations due to PVT corners.

As the telescopic opamps used for gain-boosting have different input and output common-mode levels than the main amplifier, its biasing voltages are generated separately using similar cascode bias topology. The ratio of gm of biasing block to that of the opamp is not made too low, in order to allow for a quick recovery from any kicks generated by the opamp.

4.1.5 Layout

For a fully differential opamp, it is very important to have a good symmetry and matching in the layout, in order to balance out all parasitics, such as IR drop, wire capacitances, etc. Any mismatch would result in an offset. It is also important

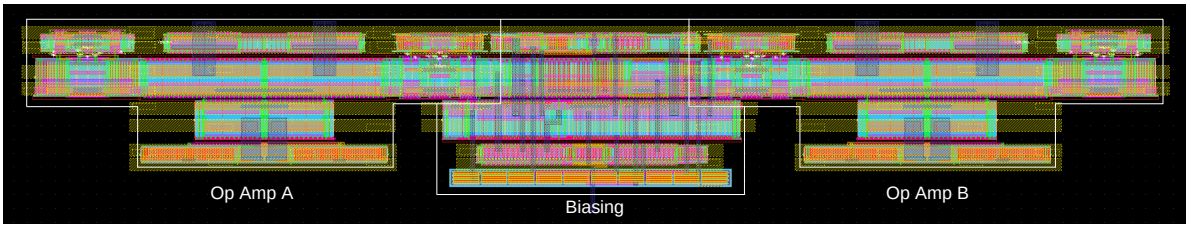


FIGURE 4.7: Layout of first stage MDAC opamp for pipeline split-ADC

to keep the diode-connected biasing transistor in the same strip as the opamp transistors it biases, in order to match their threshold voltages. The layout of the opamps for first stage MDAC for the two half ADCs is shown in fig 4.7. The opamps share their biasing network in order to match their DC operating point. The signal direction is kept the same through the MDAC floorplan, in order to simplify the alignment for the MDACs in all the stages. Power supplies are provided by using a grid formed from the two thick metal layers available, M6 and M7. The metal lines are made wide enough to satisfy electromigration rules in 65nm technology.

The sampling capacitance was laid out using metal-metal finger capacitance structure, as shown in fig 4.8. Metal wires were stacked from Metal 2 to Metal 6, with Metal 1 and 7 used as shields. The wires connected to one of the terminals are completely enclosed between those connected to the other, in order to shield the terminal connected to the opamp input to avoid any stray capacitance at that node. The capacitor-array was punctuated by dummy capacitors at the two ends. An N-well was placed under the finger capacitor-array to reduce noise from the substrate. The capacitance value was estimated by using Magma QuickCap tool.

4.1.6 Common-mode feedback (CMFB)

As the output nodes of the opamp are high-impedance, the output common-mode level is very sensitive to any mismatch in the p- and n- type current sources due to process variations. Since the input common-mode gain is suppressed due to

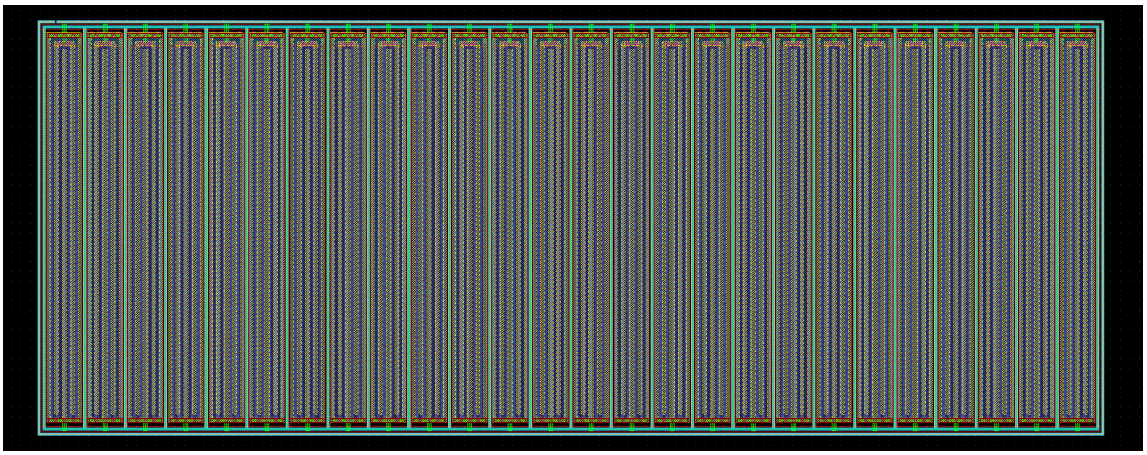


FIGURE 4.8: Finger Capacitance Layout

common-mode rejection of the differential pair, the loop gain for the common-mode feedback loop would be small and it would exert less control on the CM output voltage. Hence, a different feedback loop with high loop gain is used to control the output common-mode.

A common-mode feedback circuit is used to detect the common-mode voltage at the outputs, compare them with a reference and bring the output common-mode voltage to that reference through negative feedback. Broadly speaking, there are two ways of doing this, continuous-time and switch-capacitor technique. In the first approach, the output swing of the opamp is limited by the input signal range of the common-mode detector. Also, continuous-time CMFB loop has its own set of poles and needs to be compensated as well in order to ensure stablity. That, coupled with linearity limitations and extra power consumption, make its design non-trivial. The switch-capacitor approach, on the other hand, faces none of these problems, and being discrete-time, is perfect for SC circuits.

The SC CMFB used in this design is shown in fig 4.9 [10]. The network is operated in two non-overlapping clock phases, $\phi 1$ and $\phi 2$. This circuit acts as a simple SC low pass filter. In $\phi 2$, Ccms charges to Voref-Vbref, where Voref is the reference defining the desired output common-mode voltage, and Vbref is the bias reference for the current sources used in the CMFB loop. Since Ccm is always connected between Vout and Vbcm, which is the gate voltage of the current source, its charged

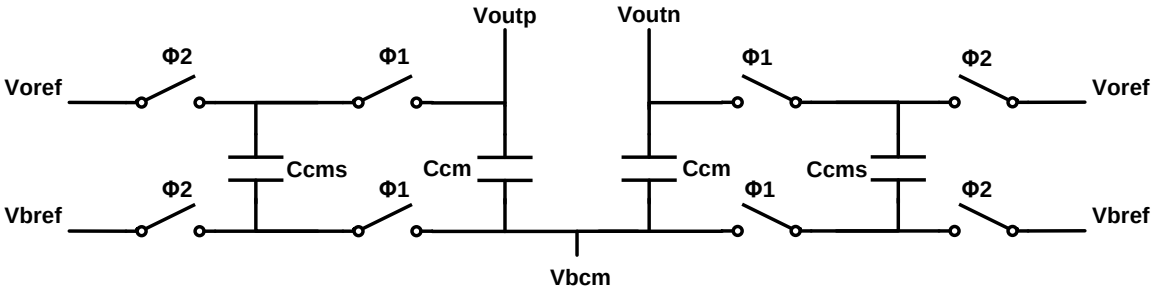


FIGURE 4.9: Switched-cap CMFB

to Voutp,n-Vbcm. During $\phi 1$, Ccm and Ccms are connected in parallel and charge redistribution occurs.

In order to not limit the output swing of the opamp, clock-boosted NMOS switches were used as switches. The ratio of Ccm to the parasitic gate capacitance decides the feedback factor which should be made atleast 1/2. The bandwidth of the CMFB is decided by the transconductance of the current sources. One of the drawbacks of SC CMFB is that Ccm directly loads the op amp, slowing it down marginally. Also charge injection and clock feedthrough from the switches add an offset to the output common-mode voltage.

A common-mode half circuit of the current mirror opamp along with the SC CMFB has two feedback loops, as shown in fig 4.10. Loop1 is the CMFB loop consisting of the SC CMFB circuit and the NMOS current sources. This loop is a negative feedback loop and its gain is given by -

$$Acm_{loop1} = \alpha gm_7 Rout \tag{4.13}$$

where α is the feedback factor of the CMFB. For low frequencies, the equivalent resistance of switched-capacitor $Ccms$, will dominate and hence α will be equal to 1. For higher frequencies, Ccm will take over and α will become $Ccm/(Cp+Ccm)$, where Cp is the parasitic gate capacitance of M7.

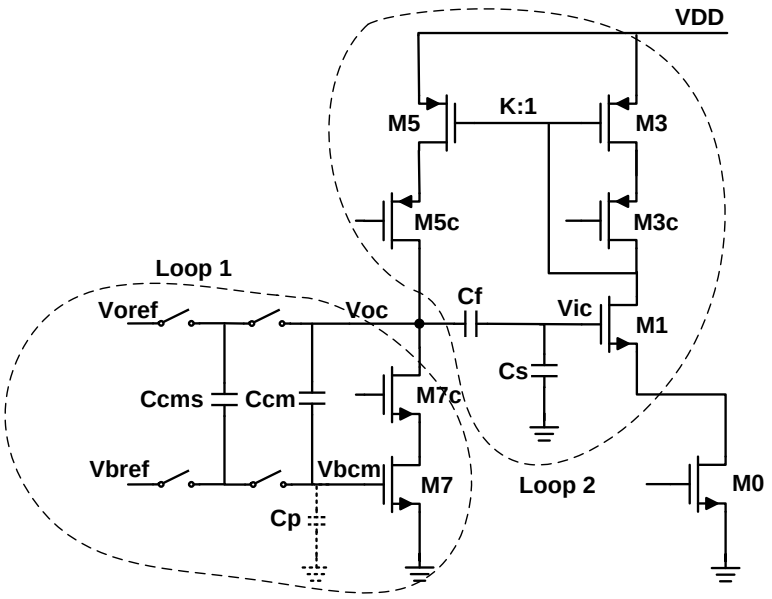


FIGURE 4.10: Common-mode half-circuit of current mirror opamp

The second loop, shown as loop 2 in fig. is due to the capacitive feedback consisting of Cs and Cf, and goes from input to the output of the opamp. As there are two phase inversions in this path, loop 2 is a positive feedback loop. The gain of loop 2 can be written as -

$$Acm_{loop2} = K\frac{gm1}{1+gm1ro_0}Rout\frac{Cf}{Cs+Cf} \tag{4.14}$$

where ro_0 is the output resistance of the tail current source and Rout is the resistance seen at the output of the opamp. When there are no loops connected, at low frequencies *Rout* is simply the resistance of the two cascode current sources in parallel -

$$Rout = (ro_7 gm_{7c} ro_{7c})||(ro_5 gm_{5c} ro_{5c}) \tag{4.15}$$

Naturally, *Rout* is designed to be pretty high, especially when gain-boosting is used. The action of the two feedback loops is analysed in terms of their effect on the output common-mode impedance. If *Rout* was the impedance seen at the

output when the two loops are disconnected, then loop 1 will change it to -

$$Rout_{loop1} = \frac{Rout}{1 + Acm_{loop1}} \tag{4.16}$$

and loop 2 will make it -

$$Rout_{loop2} = \frac{Rout}{1 - Acm_{loop2}} \tag{4.17}$$

Routeff can be expressed as parallel combination of $Rout_{loop1}$and $Rout_{loop2}$. Hence,

$$Rout_{eff} = Rout_{loop1}||Rout_{loop2} = \frac{Rout}{2 + Acm_{loop1} - Acm_{loop2}} \tag{4.18}$$

For $Rout_{eff}$ to be low and positive, Acm_{loop1} should be greater than Acm_{loop2} for all frequencies. This means -

$$Acm_{loop1} > Acm_{loop2} \tag{4.19}$$

From eqns 4.13 and 4.14 -

$$\alpha gm_7 Rout = K\frac{gm1}{1 + gm1ro_0}Rout\frac{Cf}{Cs + Cf} \tag{4.20}$$

For a similar capacitive ratio in both loops and a high ro_0, this can be approximated as -

$$gm_7 \approx \frac{K}{ro_0} \tag{4.21}$$

As ro_0 scales with K, this effectively means that the common-mode loop around the opamp is stable as long as the intrinsic gain of the transistor is higher than 1. In order to have sufficient margin for common-mode stability, the common-mode rejection of the differential pair should be further increased by increasing the length of the tail current source, thereby reducing the input common-mode

gm by atleast an order.

4.1.7 Simulation Results

Table 4.2 summarizes the simulation results for the first stage MDAC opamp at schematic and layout level. There is a slight drop in unity gain bandwidth, phase and gain margin due to extra wiring parasitics.

	Schematic	Layout
VDD	1V	1V
DC Loop Gain	56dB	55.6dB
Loop Unity Gain Bandwidth	834MHz	763MHz
Phase Margin	74.1°	71.9°
Gain Margin	25.2dB	23.5dB
Power Consumption	22.44mW	22.4mW

TABLE 4.2: Simulation results for the gain-boosted current mirror opamp

The opamp performance was also simulated over PVT corners. The maximum and minimum values for each specification are shown in Table 4.3.

Fig 4.11 shows the variation in settling behaviour with bias current. As the settling

	Maximum	Minimum
VDD	1.1V	0.9V
Temperature	125°C	-40°C
DC Loop Gain	60.5dB	42.5dB
Loop Unity Gain Bandwidth	1.19GHz	640MHz
Phase Margin	75.9°	71.9°
Gain Margin	25.8dB	25.1dB
Power Consumption	29mW	16.3mW

TABLE 4.3: Simulation results for the gain-boosted current mirror opamp over corners

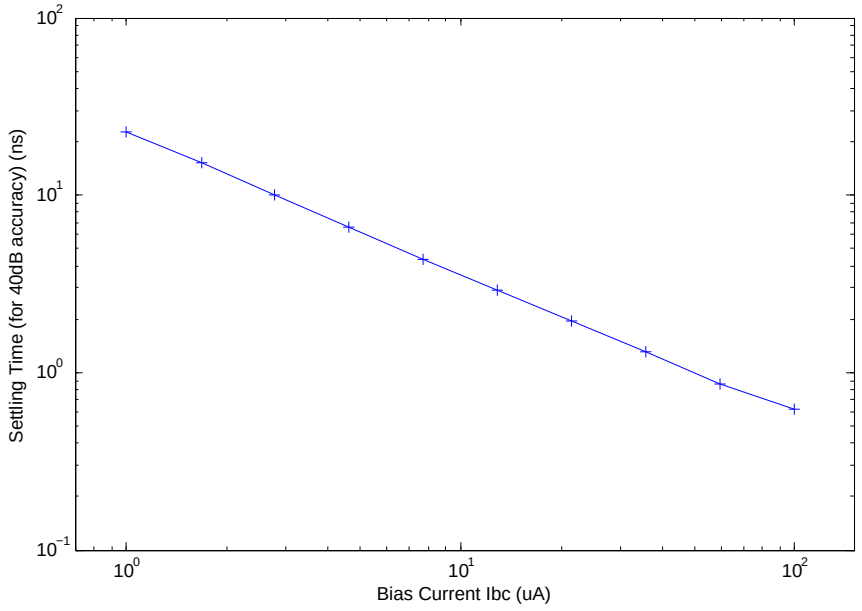


FIGURE 4.11: Settling time variation wrt Bias current

time varies almost linearly with the bias current, the opamp works over a wide range of bias current and hence is extremely power scalable.

4.2 MDAC

The fully differential MDAC is shown in the fig 4.12. While it is essentially the same flip-around topology described in the previous chapter, an extra switch is used to short the input terminals of the opamp during $\phi 1e$. As this switch is connected in parallel to the bottom plate switches in the sampling phase, it reduces the ON resistance of the sampling path. This allows a reduction in the bottom-plate switch sizes, hence reducing the common-mode jump due to their charge injection.

Simple NMOS switches were used everywhere, except in the reference ladder, with clock boosting in order to increase their ON conductance and linearity. The clock boosting scheme used is described in the next chapter. Since the control signals

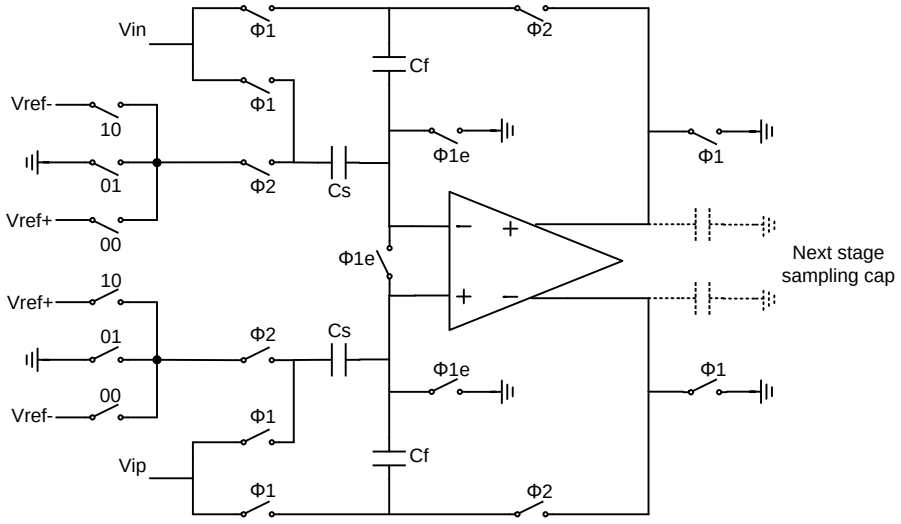


FIGURE 4.12: Fully differential MDAC implementation

for the reference ladder switches are generated by the coarse ADC, a PMOS switch is used to connect Vref+ and NMOS switches for Vref- and input common-mode.

4.2.1 Simulation Results

The simulation results for the first stage MDAC for the pipeline split-ADC are summarized in Table 4.4. The simulations were performed over a typical corner at a temperature of 27°.

Sampling Freq	500MS/s
Swing	0.8Vp-pdiff
THD (fin = 4MHz)	66.5dB
THD (fin = 234MHz)	66dB
IM3 (low freq)	75dB
IM3 (high freq)	73.1dB
Input-referred noise (differential) (100KHz to 100GHz)	76.56μVrms

TABLE 4.4: Simulation results for first stage differential MDAC

The 3-dB bandwidth of the input sampling network for the first stage MDAC was also simulated, and was found to be 395MHz for a source impedance of 50Ω.

4.3 Summary

In this chapter, the design of the MDAC for the pipeline ADC was discussed. A review of commonly used opamp topologies was conducted, and due to its relative strengths for this application, the current mirror architecture was chosen. The complete implementation with layout and simulation results is presented for the first stage opamp. Some common-mode feedback issues in current mirror architecture were discussed and an SC-CMFB implementation is presented. The chapter concludes with a discussion on the implementation and simulation results for the first stage MDAC of pipeline split-ADC.

Chapter 5

Pipeline ADC Design

This chapter describes the design of the other blocks required for pipeline ADC. The top-level implementation and the techniques applied in order to save power are also discussed. Comparators designed for the pipeline stages and the backend flash ADC are presented in detail. The chapter concludes with the simulation results of the entire pipeline split-ADC.

5.1 ADC architecture

The overall pipeline "split-ADC" architecture is shown in fig 5.1. 9 stages with 1.5b/ stage resolution are used followed by a 5bit back-end flash ADC. The extra 2 bits are added in order to compensate for the dynamic range lost due to the gain of residue amplifiers being smaller than 2 and to improve the accuracy in error estimation by reducing the quantization noise.

5.1.1 Power saving techniques

In order to reduce the power consumption of the pipeline ADC, a couple of power saving features were implemented, and are described in this section.

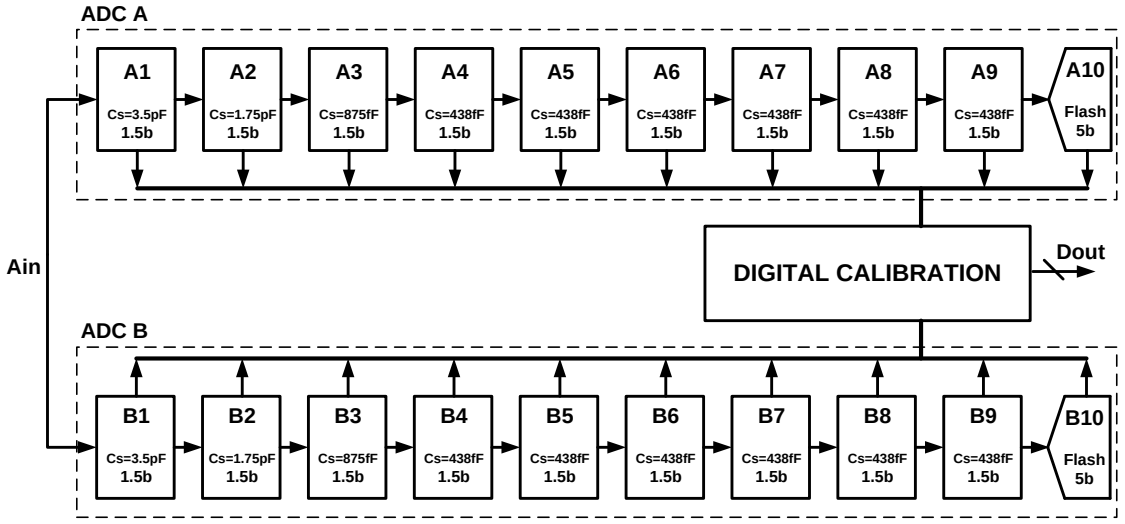


FIGURE 5.1: ADC architecture

5.1.1.1 SHA-less architecture

A Sample-and-hold amplifier (SHA) is normally used at the input of an ADC and accounts for a major portion of the power budget of the ADC. Since its noise and distortion are not attenuated by any preceeding gain, the SHA ultimately puts a limit on the overall ADC performance. The SHA doesn't perform any digitization, and is used only to provide a stable input voltage to the first stage of the ADC. This ensures that the signal sampled by the MDAC and the coarse ADC in the first stage, is the same. Any mismatch in the two inputs would result in an error showing up as comparator offset. This is illustrated in fig 5.2.

During $\phi 1$, both the MDAC and the coarse ADC are sampling the input signal. Normally the sampling circuits and the delay for these two are different. While the MDAC sampling network is purely passive, the CADC sampling path quite often involves a preamplifier in the comparator. Hence, it can be seen that in the absence of a SHA, if a continuous-time signal is applied directly at the input of the pipeline stage, the two networks will sample at different moments, resulting in a mismatch in the voltages. While the comparators will make a decision based on the input signal V1, the MDAC will produce a residue from V2, resulting in an error.

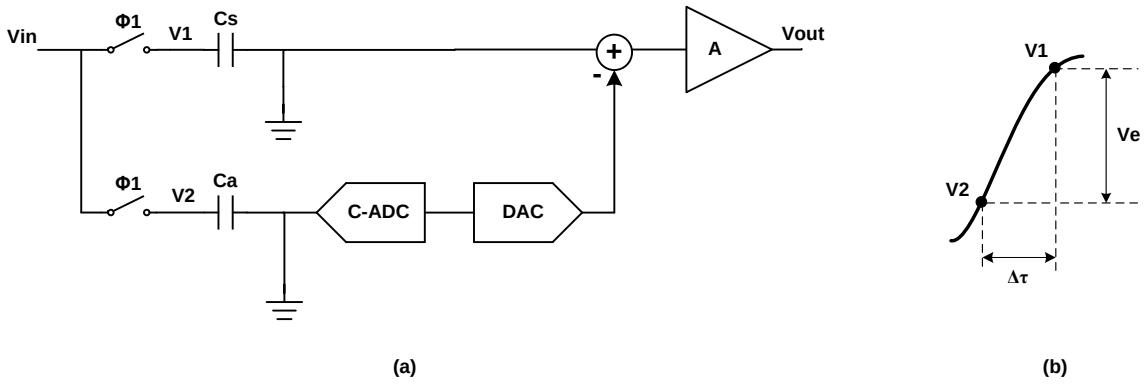


FIGURE 5.2: Effect of mismatch between MDAC and Coarse ADC sampling networks

The magnitude of this error depends on the input frequency and amplitude of the input signal. If a sinusoidal wave, $Vin = V_o \sin(2\pi f_{in} t)$, is applied at the input, the worst-case error would occur at its maximum slope which is at the zero-crossing points. Hence,

$$\frac{dVin}{dt}_{max} = V_o 2\pi f_{in} \tag{5.1}$$

For a mismatch between time constants of the two paths, $\Delta\tau$, the error between the two sampled voltages can be expressed as -

$$V_e = V_o 2\pi f_{in} \Delta\tau \tag{5.2}$$

This error is called aperture error and appears as comparator offset and hence, needs to be smaller than the overrange. 1.5b/stage has the advantage of having a relatively large overrange of $\pm Vref/4$. So assuming ideal comparators, the maximum skew that can be tolerated by the stage at a certain input frequency, can be expressed as -

$$\Delta\tau = \frac{1}{8\pi f_{in}} \tag{5.3}$$

For an input frequency of 250MHz, this translates into a maximum tolerable skew of 160ps. In practice, the skew should be designed to be much smaller in order to take other non-ideal effects into account which also consume overrange such as comparator offset. Hence, efforts need to be made to reduce the aperture error.

Several approaches towards removing the SHA have been published in the literature [3, 20]. [20] uses a dedicated input sampling capacitor for the MDAC along with a separate set of caps for reference sampling. This results in a large reduction in the feedback factor and hence, the bandwidth of the residue amplifier. To further reduce the mismatch, [20] attempts to match the sampling networks for the MDAC and the coarse ADC. However, while the matching is helped by employing a shared input sampling switch, accurate matching between the bottom plate switch resistance and the closed loop impedance of the preamplifier, given by the inverse of its input transconductance, is difficult over PVT corners and other mismatch effects, hence resulting in a significant aperture error at high frequencies. The timing scheme used in [20] also results in a reduced amplification time, as the latch decision is available somewhere in the middle of $\phi 2$, hence negating some of the power benefits derived from removing the SHA.

In this ADC, the first stage and timing structure similar to the one proposed in [3] is implemented. The input sampling networks of MDAC and CADC are completely decoupled, which allows the MDAC to use the same capacitance for sampling the input and the references, resulting in a larger feedback factor compared to [20]. The decision time for the comparator is derived from the sampling phase instead as its easier to increase the bandwidth of the sampling network compared to the amplifier. A simple comparator without a preamplifier is used in order to reduce the decision time, as the degree of coupling of kickback noise from the latch to the MDAC is reduced by using separate input switches.

The time constants of the two sampling paths need to be matched closely, as described in [3]. This is done by designing the input sampling network of the

CADC as a scaled replica of the MDAC network. The input common-mode levels of the opamp and the comparator are also made identical. Further care needs to be taken during layout to match them as much as possible by placing the switches close by. The parasitic capacitances at the input nodes of the opamp and the comparator also play a role and hence should be taken into account.

5.1.1.2 Stage scaling

Since residue amplification is performed at the end of each stage, the input-referred noise of successive stages gets attenuated as we go further down the pipeline chain. Hence, this gain in the pipeline chain can be exploited by reducing the SNR requirements from later stages. Since 1.5b/stage architecture employs a gain of 2, using identical stages results in very high power consumption, while the input-referred noise is largely dominated by the first stage. On the other hand, scaling the sampling capacitance by 4x for every stage results in an equal noise contribution from all stages, while reducing the power consumption and chip area drastically. To optimize this trade-off, the optimum capacitance scaling factor needs to be calculated taking into account the per-stage resolution, the conversion speed, circuit topolgy and the technology used. [6] carries out an analysis and determines the optimum scaling factor to be approximately the interstage gain. Hence, in this design, stage-scaling by a factor of 2 is applied twice, due to limited design and layout time.

5.2 Comparator Design

5.2.1 Stage Comparator

As discussed in the previous section, the input signal sampling paths should match for the MDAC and the coarse ADC. This implies that the input signal cannot be sampled at the input of the latch through a preamplifier, but needs to be sampled on a capacitor. The timing scheme also puts a constraint on the decision

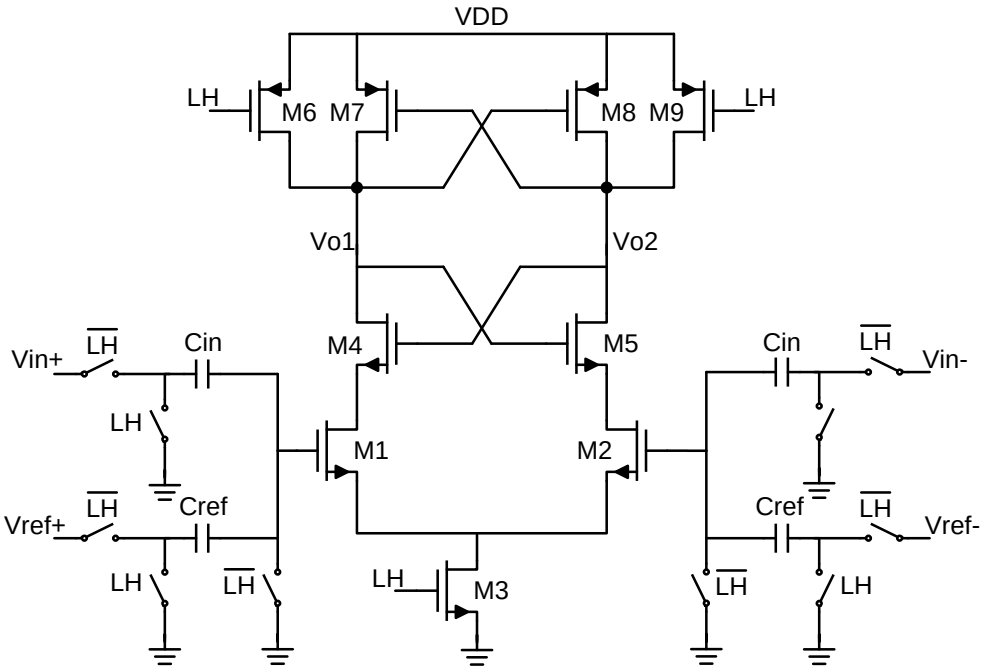


FIGURE 5.3: Charge distribution comparator [13]

time available to the comparator. Though a preamplifier would reduce the input-referred offset of the latch, it also adds extra delay, greatly increasing the chances of metastability. Hence, the charge sharing dynamic comparator [13] shown in fig 5.3 was used as the starting point.

This comparator works in two phases. When the latch signal, LH, is low, the comparator is in reset phase and the outputs, Vo1 and Vo2, are shorted to the supply through PMOS switches, M6 and M9. The dynamic tail current source M3 is switched off making the comparator core inactive. The charge at the input of the M1 and M2 can be written as -

$$Q_{M1}(\overline{LH}) = Cin(0-Vin_{+})+Cref(0-Vref_{-}),\ Q_{M2}(\overline{LH}) = Cin(0-Vin_{-})+Cref(0-Vref_{+}) \tag{5.4}$$

In the latch phase, LH goes high and the switches release the latch and the differential pair becomes active. The charge at the input of M1 and M2 can be written

as -

$$Q_{M1}(LH) = Cin(V_{M1}-0)+Cref(V_{M1}-0),\ Q_{M2}(LH) = Cin(V_{M2}-0)+Cref(V_{M2}-0) \tag{5.5}$$

applying charge conservation,

$$V_{M1} = \frac{CinVin_+ + CrefVref_-}{Cin + Cref},\ V_{M2} = \frac{CinVin_- + CrefVref_+}{Cin + Cref} \tag{5.6}$$

Comparator threshold can be defined as the point where $V_{M1} = V_{M2}$-

$$CinVin_+ + CrefVref_- = CinVin_- + CrefVref_+ \tag{5.7}$$

or

$$Vin_+ - Vin_- = \frac{Cref}{Cin}(Vref_+ - Vref_-) \tag{5.8}$$

The offset of this comparator depends on the mismatch between the capacitors and the latch and differential pair. Since the imbalance is inserted in the latch through the source terminals of M4 and M5, parasitics at the latch outputs are minimum, hence making the latch offset low and the overall offset for this comparator is relatively low. This low offset comes at the cost of speed, as now the Vgts for the latch transistors are reduced due to the headroom consumed by the differential pair in latch phase. This reduces the gain of the latch, making the overall comparator slower.

One way to solve this is to provide the output of the differential pair directly to the latch outputs, making M4 and M5 free to be connected to ground. This makes the latch much faster, but the offset increases due to the extra parasitics seen at the output. So the latch in fig 5.3 was modified by adding two NMOS switches driven by a slightly delayed LH signal, LH_d, as shown in fig 5.4. The delay allows the input difference to propogate through the differential pair and reach the latch. And as the latch begins to regenerate the input signal, the switches connect the

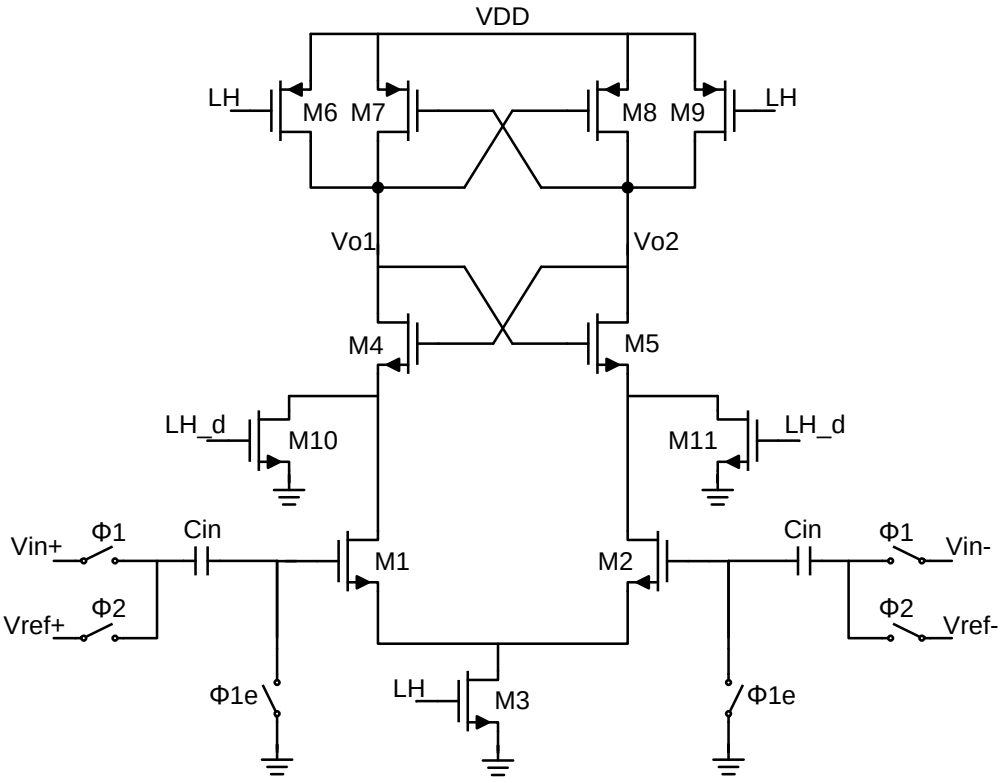


FIGURE 5.4: Modified Comparator

latch to the ground, giving it maximum headroom, and hence making it fast. The delay in LH_d should be sufficiently long for the differential input signal to reach the latch, in order to contain the offset. For very small delay values, the offset of the latch increases, as shown in fig 5.5.

As there is hardly a significant change in offset for delay value greater than 25ps, a delay of 50ps is chosen. Adding these switches also helps in reducing kickback noise, as they produce a common-mode kick at the beginning of LH_d, which is much less serious than differential kickback. Another advantage of this architecture is that by sampling the input signal and reference voltages in different phases, only one capacitor is required. This eliminates the attenuation caused by the capacitive division and the effect of capacitive mismatch, hence improving the offset by atleast a factor of 2. Fig 5.6 shows monte carlo analysis of the proposed comparator. The comparator was found to have an offset variation of 11.41mV over 200 runs, meaning a 3σ offset of 34.2mV. It also achieves a bit error rate of 10^{-12}

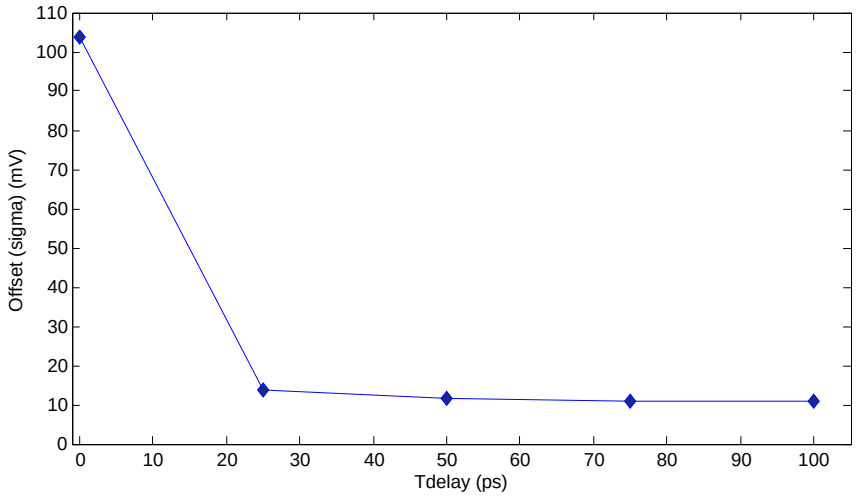


FIGURE 5.5: Variation in offset with LH_d

within a decision time of 300ps.

The comparator can be further improved in terms of speed and offset by using a different reset mechanism. Instead of the supply rail, the latch outputs can be shorted to each other during the reset phase. The output levels during reset would now be determined by the operating point of the two inverters. Due to this, when the latch signal arrives, there is no common-mode transition at the latch outputs, thereby greatly reducing the dynamic offset. The decision time is also reduced because the comparator can now start the evaluation at an earlier moment. However, these improvements come at the cost of static power dissipation during the reset phase. As the comparator shown in fig 5.4 already met the specifications, this reset mechanism was not adopted.

5.2.2 Backend Flash ADC

Since no residue amplification is required at the end of the pipeline chain, a simple 5b flash ADC is used as the last stage. The LSB for the flash ADC translates to 25mV($0.8V/2^5$). As no overrange is used for the flash ADC, the comparator

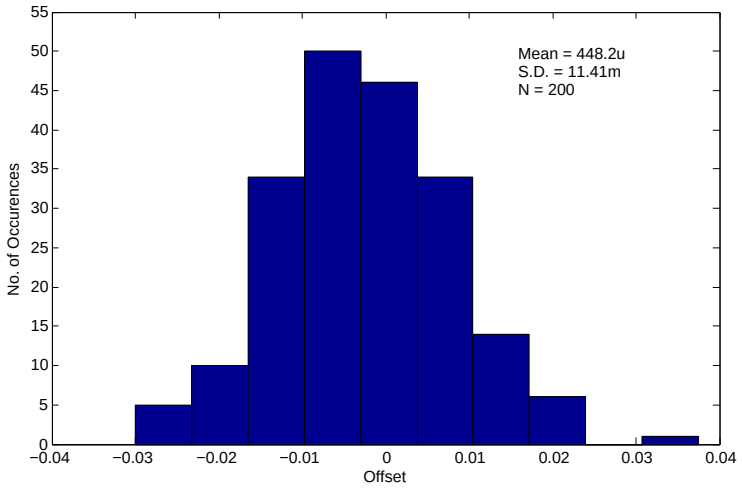


FIGURE 5.6: Monte Carlo simulation of modified comparator

offset should only be a fraction of the LSB in order to have a low INL. The offset cannot be reduced by simply sizing up the comparator as a higher resolution also increases the number of comparators and hence the load capacitance of the previous stage. The comparator offset can be decreased by using a preamplifier in front of it. The preamplifier typically has a low gain and high bandwdith in order to introduce minimum delay. A simple NMOS differential pair with resistive load was used as the preamplifier. The preamplifier attenuated the comparator offset by a gain of around 6. But now the overall offset was dominated by the offset of the preamplifier.

The preamplifier offset can be removed by using an offset-cancellation technique called auto-zeroing. In this technique, the offset of the preamplifier is first stored over a capacitor and then applied along with the input in the next phase to achieve cancellation. Fig 5.7 shows the autozeroing technique for single-ended preamplifier.

During phase 1, the preamplifier is connected in unity gain feedback and the offset is stored on the sampling capacitor -

$$Vout = Vc = -A(Vc - Vos) \tag{5.9}$$

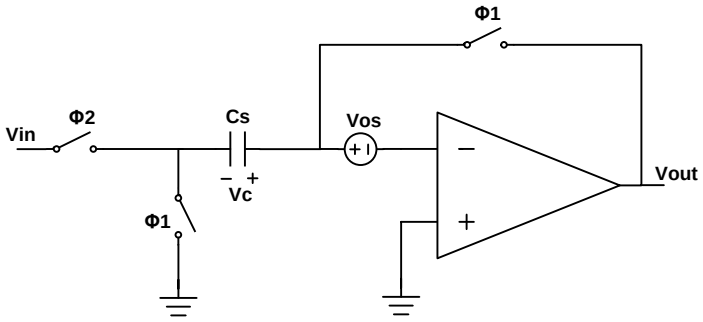


FIGURE 5.7: Offset cancellation through autozeroing

$$Vc = Vos\left(\frac{A}{A+1}\right) \tag{5.10}$$

where Vc is the voltage stored on the capacitor, and A is the gain of the preamplifier.

During phase 2, the loop is broken and the input signal is applied to the preamplifier through the sampling capacitor,

$$Vout = -A(Vin + Vc - Vos) \tag{5.11}$$

$$= -A\left(Vin - \frac{Vos}{A+1}\right) \tag{5.12}$$

Hence, the offset is reduced by A+1 times. The switch connecting the feedback loop also contributes to offset through charge injection. So for the offset for the overall autozeroed comparator can be written as [18] -

$$Vos = \frac{Vos_1}{A+1} + \frac{\Delta Q}{Cs} + \frac{Vos_2}{A} \tag{5.13}$$

where Vos_1 and Vos_2 are the preamplifier and latch offsets, and ΔQ is the charge injection from the switch. For a high resolution flash, the offset term arising from charge injection should be kept low by increasing the sampling capacitance.

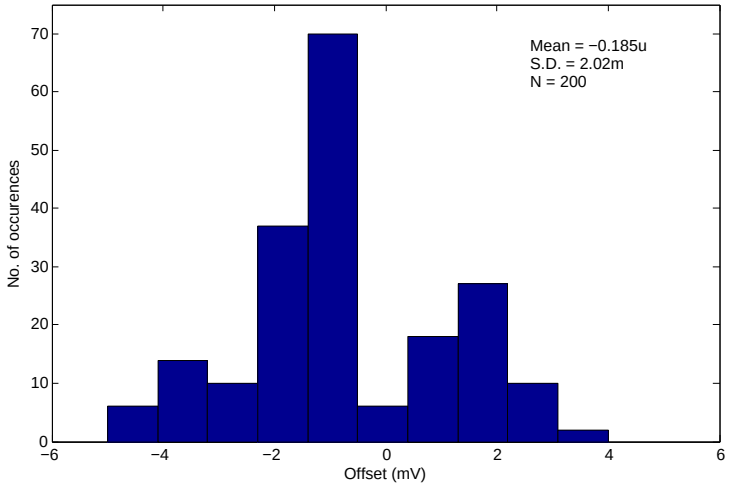


FIGURE 5.8: Monte Carlo simulation of autozeroed comparator

In this autozeroing scheme, the offset is stored on the input capacitance by connecting the preamp in unity feedback. Another way of storing the offset is to short the inputs and store the offset at the output capacitace. Though the offset of the preamplifier is completely cancelled in this technique, the input to the comparator is DC coupled, limiting the input common-mode range. And since the overall comparator offset is dominated by that of the latch, input offset storage was used for this design.

By using autozeroing, the preamplifier offset was also attenuated by its gain, and the overall offset variation was found to be 2mV over 200 runs, meaning a 3σ offset of 6mV as shown in fig 5.8.

5.3 Clock Boosting

The linearity of a switch is determined by the variation in its ON resistance. For low voltage supplies, the gate-to-source voltage becomes very small and the ON-resistance varies significantly with the input signal. This degrades the linearity with which the signal is sampled and hence limits the linearity of the entire ADC itself. This problem can be be avoided by using thick-oxide option for switches in the input stage. However, high voltage clocks are not suitable for high speed

designs because of their large rise and fall times. Another way is to use bootstrapping [2] which maintains a fixed gate-to-source voltage across the switch, making it more linear. To ensure device reliability, any excessive gate-dielectric stress can be avoided by limiting the maximum clock voltage to 1.1V. However, a signal amplitude of 0.7V and clock voltage of 1.1V translates into a very low Vgs of only 400mV, which is insufficient for this sampling frequency. Hence, clock boosting scheme shown in fig 5.9 is used, where the clock signal is raised by a fixed voltage of 0.3V. An inverter with greater than minimum length is used with a supply of 1.2V as an interface between the clock generator and clock boosting, resulting in final clock levels from 0.3V to 1.5V. The maximum gate-to-substrate voltage for the

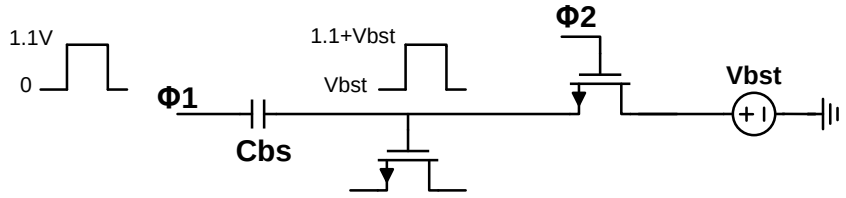
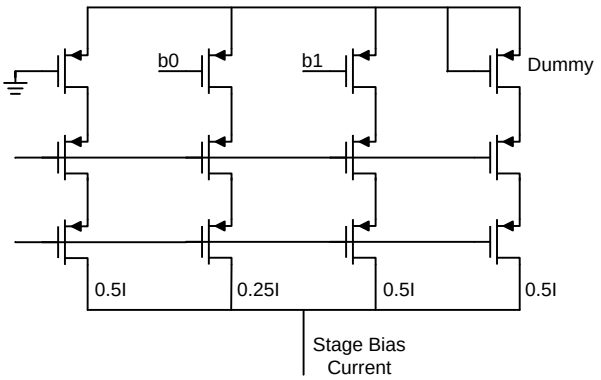


FIGURE 5.9: Clock boosting

switches can be reduced by connecting the bulk terminal to source, using a deep N-well. While this scheme may have reliability issues, since the design is being aimed as a test chip, long term reliability is not a strict constraint.

5.4 Bias current distribution

Apart from the local biasing for each stage, a more global block is required which can be used to control the bias point of each stage through a single external reference. This is done by distributing scaled copies of an external current source through all the pipeline stages, because current distribution is immune to IR drop over wire resistances. As shown in fig 5.10, the current mirror is made programmable in such a way that the bias current for each stage can be controlled



b1	b0	Bias Current
0	0	1.25I
0	1	I
1	0	0.75I
1	1	0.5I

FIGURE 5.10: Programmable stage bias current

independently. A dummy current source is also included as an extra safety margin which could be used by making changes just on the metal layer.

5.5 Simulation Results

The simulation results for each of the pipeline half-ADCs are presented in table 5.1. Since the two half-ADCs digitize the same input signal, an extra 3dB SNR is be achieved by averaging their outputs. Hence, an overall SNR of 71.3dB is achieved by the pipeline split-ADC.

Technology	65nm CMOS
VDD	1V
Sampling Freq	500MS/s
Resolution	12 bits
Full scale input	0.8Vp-pdiff
SNR	68.3dB
Power Consumption (analog core)	77.3mW

TABLE 5.1: Simulation results for the pipeline half-ADC

The THD achieved from the split-ADC for different sampling frequencies is shown in fig 5.11. At 500MS/s the THD is limited to 50dB due to incomplete settling in the stage MDACs. As the sampling frequency is reduced, the THD increases and

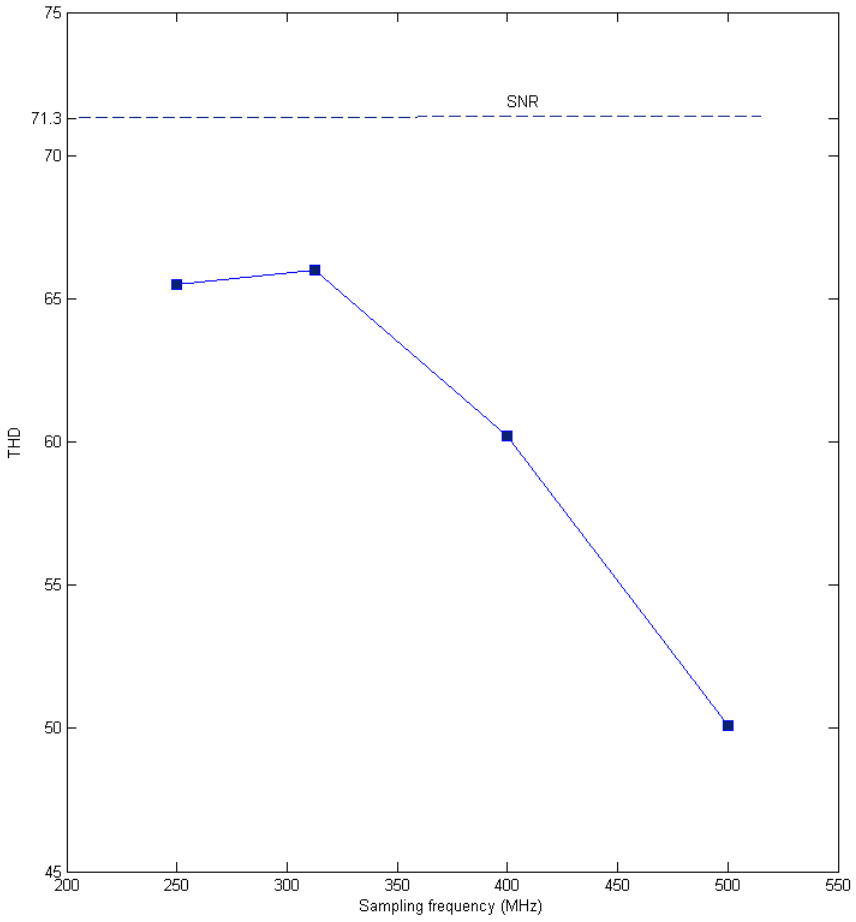


FIGURE 5.11: THD versus Sampling frequency

settles down at 66dB.

5.5.1 Comparison

The split-ADC designed in this thesis is compared to recently published high-speed ADCs (>100MS/s), in terms of energy efficiency in fig 5.12 [21]. The ADC achieves a peak figure of merit of 0.3pJ/conversion at a sampling frequency of 312.5MS/s without using digital calibration or opamp sharing. Since the figure of merit does not scale linearly with speed, the ADC performance is also judged with respect to speed-resolution product, as shown in fig 5.13 [21]. The ADC

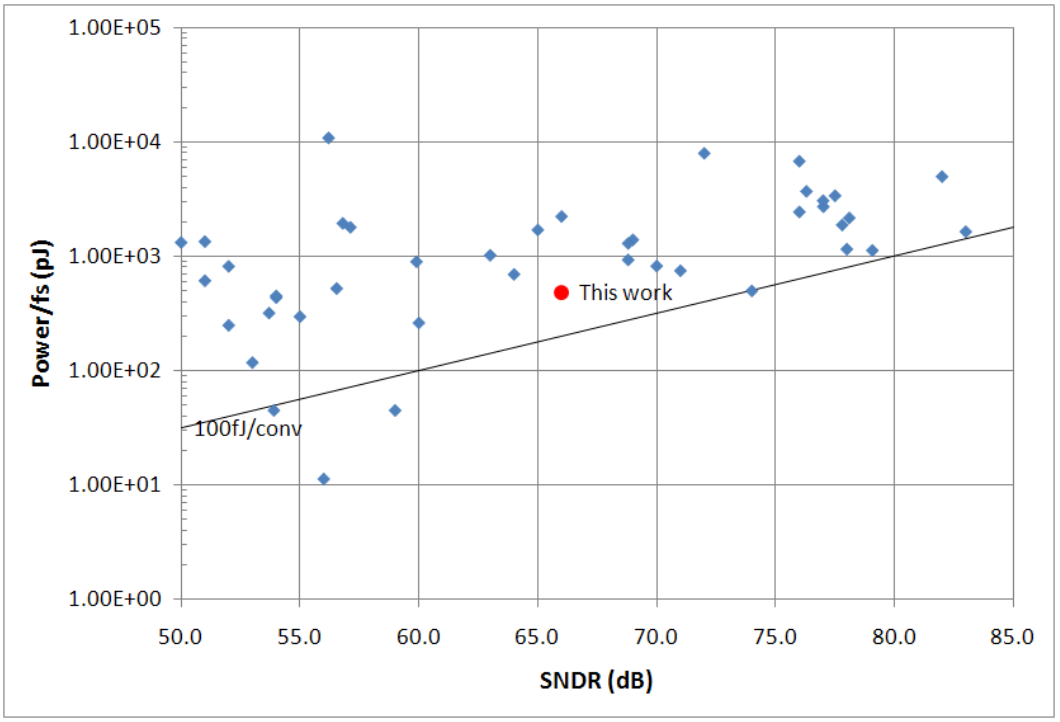


FIGURE 5.12: Comparison of ADC energy efficiency with recently publications

performs quite well in both charts and compares with the state-of-the-art. Since the ADC SNDR is currently limited by THD and the spurious tones caused by insufficient settling can be corrected by digital calibration, the split-ADC serves as an excellent starting point for testing calibration algorithms.

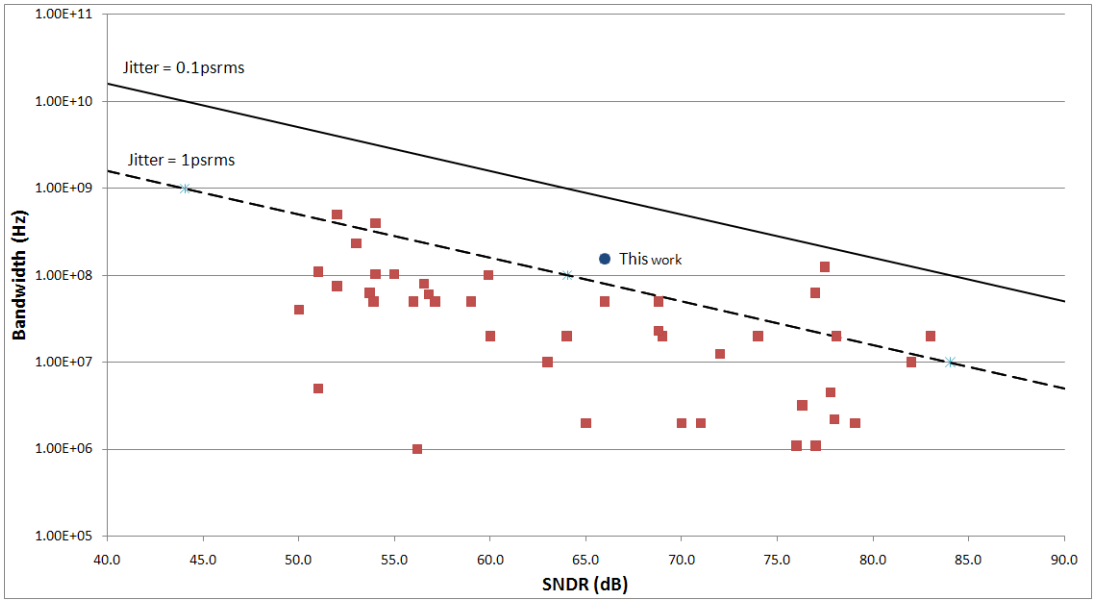


FIGURE 5.13: Comparison of ADC speed-resolution product with recently publications

5.6 Summary

This chapter presented the implementation of the pipeline ADC. An SHA-less architecture was used in order to save power. The problems arising from not using an SHA and the techniques employed to solve them were discussed. The design details for comparators used in the coarse ADC and the back-end flash were presented. The clock-boosting scheme used to improve the linearity of the switches was also described. The chapter concludes with some of the simulation results for the pipeline split-ADC

Chapter 6

Conclusion

6.1 Summary

In this dissertation, a fully differential 12-bit pipeline "split-ADC" sampling at 500MS/s was designed in TSMC 65nm CMOS technology. The pipeline ADC was designed to be programmable in terms of power consumption and stage amplifier settling, allowing it to be used to test the efficiency and power savings achieved from calibration algorithms based on split-ADC architecture.

Apart from the error correction, efforts were made to make the ADC more power efficient. Detailed analysis and comparison of opamp topologies and their performance in 65nm technology was performed and the current mirror architecture was found to be the most optimum topology. By using a current-mirror ratio of 2, roughly 50% of opamp power was saved with respect to folded cascode topology, while a 10dB higher gain was achieved.

Power consumption was further reduced by removing the sample-and-hold as the front-end of the ADC, and sampling the input signal directly at the first stage. This results in an aperture error due to the mismatch between the sampling network of the MDAC and the coarse ADC (CADC). In order to limit the aperture

error, the CADC sampling network was designed as a scaled replica of that of the MDAC. 1.5b/stage architecture was utilised to provide a large overrange to deal with aperture error. Also, a modified timing scheme, as proposed in [3] was implemented to preserve the amplification time of the MDAC. Stage scaling was also used to benefit from the stage gain.

A modified version of the comparator proposed in [13], displaying reasonable offset and good speed, was used for the CADCs due to the extra overrange available from 1.5b/stage. However, the resolution of the backend-flash was increased in order to increase the dynamic range available for the calibration algorithm for error estimation. An autozeroed preamplifier was used to reduce the offset of the comparator. Due to the low supply voltage, clock boosting was used to provide sufficient linearity to the switches. A programmable current mirror was used for bias distribution so that the bias current for each stage could be programmed independently.

The overall pipeline split-ADC was simulated and showed an SNR of 71.3dB at 0.8V full-scale input, after averaging the two half-ADC outputs. The analog core of each half-ADC consumed 77.3mW, resulting in an overall power consumption of 154.6mW. The ADC displayed a THD of 50dB at 500MS/s clock frequency and a maximum THD of 66dB at 312.5MS/s, translating into a peak FoM of 0.3pJ/conv. Since the ADC performance is limited by THD due to incomplete settling in the MDAC, the SNDR and energy efficiency are expected to improve after digital calibration. This makes the pipeline split-ADC an excellent starting point for testing calibration algorithms.

6.2 Design Recommendations

The design and simulation results presented in this thesis are the first steps in realizing the desired pipeline split-ADC. Apart from the layout of the rest of the

ADC, due to time limitations, certain blocks still need to be implemented or could be improved in the following ways -

- An ideal clock generator with buffers was used in this dissertation. The actual clock generator should be designed with a sufficient degree of flexibility, as programmable delay cells. This would be useful for certain ADC blocks. For example, a significant correlation between the delay between LH and LH_d and offset was shown in fig 5.5, and this delay should be adjustable during testing to take into account any parasitic effects which might increase the offset. In general, some amount of programmability should be added in all blocks in order to make debugging easier during measurements.

- When the input signal is fed to the chip, there will be ringing due to parasitic inductive coupling from the bondwires. Hence, an interface is required to drive the on-chip ADC inputs. This interface could be designed using either passive or active realization. While an active buffer could be used to provide gain and present a low impedance to the sampling network, it would consume considerable amount of power, while adding noise and distortion. A passive RC low pass filter could also be used as an interface. Since the signal source is a part of a controlled test set-up, signal attenuation is not an issue.

- Because of the low supply voltages, clock boosting was used to improve the linearity of the switches. The clock boosting scheme used in this design is very simple as it raises the clock signal by a fixed DC voltage. However, bootstrapping could be used to maintain a fixed voltage across the gate-source/drain terminals. While this configuration is more complex, it would improve the switch linearity with relatively lower reliability issues.

- As this ADC was designed primarily for calibration testing purposes, not much attention was paid to optimize the per stage resolution. A 1.5b/stage architecture was used for all stages because of their design simplicity and large overrange, resulting in a relatively large number of stages. Higher resolution could be used in the first few stages to reduce the number of

stages. Less stages, along with other power optimizing techniques such as opamp sharing, could result in a more energy efficient ADC.

- The limitations on how far the amplifier settling can be reduced after using calibration, need to be studied. On one hand, reduced settling requirements lower the closed-loop bandwidth of the amplifier, which allows for a reduction of the ADC power consumption. However, the inherent reduction in the MDAC gain results in a loss of dynamic range and hence the effective resolution of the ADC. A lower gain also results in lesser suppresion of thermal noise from subsequent stages, causing a reduction in the SNR. The harmonic distortion of the opamp would also become more prominant as the settling accuracy is reduced, and may limit the THD of the ADC. Hence, the variation in the THD of the ADC with bias current should also be simulated and taken into account. All these factors point towards an optimum settling accuracy and further research is needed to find this optimum.

Appendix A

Simulation Plots

The relevant plots for all the simulation results quoted in the previous chapters are presented in this appendix.

A.1 Opamp Simulations

Fig A.1 shows the magnitude and phase of the loop gain of the first stage MDAC opamp with frequency.

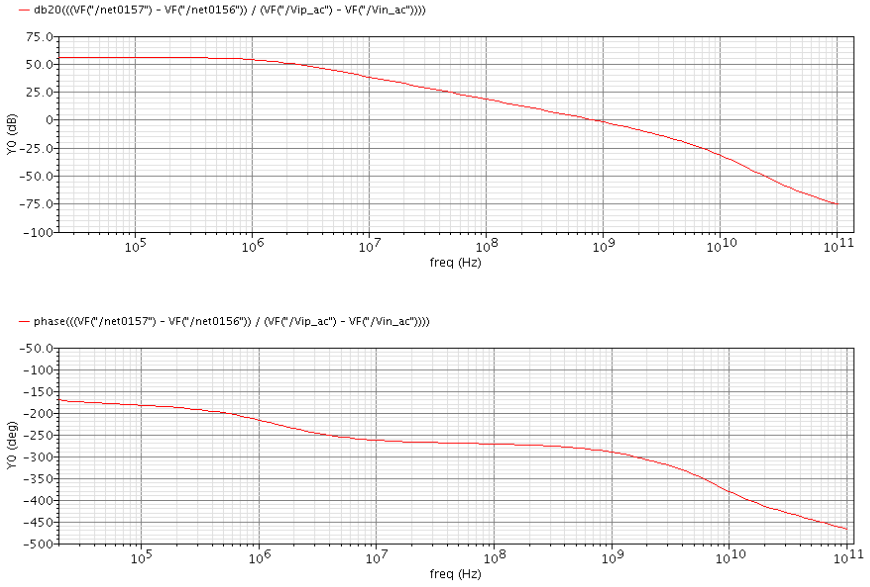


FIGURE A.1: AC Magnitude and Phase Response

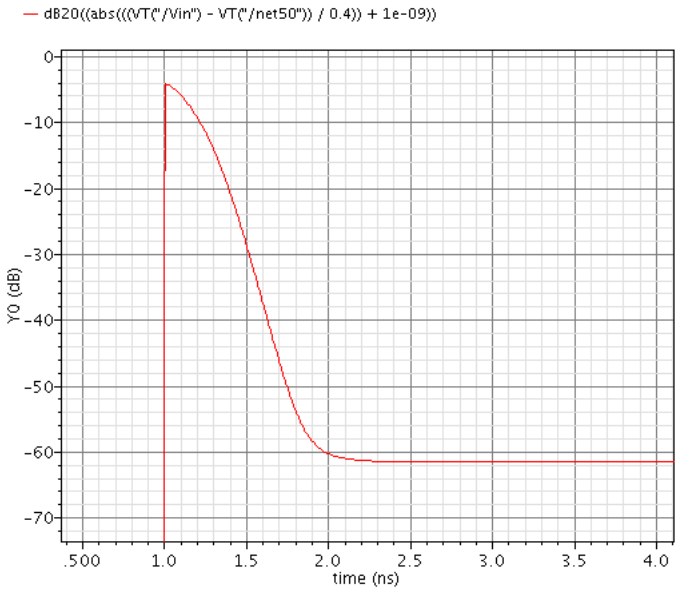


FIGURE A.2: Transient settling response for step input

The transient settling response of the opamp is shown in fig A.2. The plot represents the settling behaviour of the opamp inputs as they recover from the input step and settle towards virtual ground.

A.1.1 Common-mode stability

As discussed in section 4.1.6, the closed-loop input common-mode gain decides the common-mode stability of the opamp and was analytically proved to be lower than 1. The AC response of this gain is plotted in fig A.3 and is clearly below 1 by some margin for all frequencies.

A.1.2 Corner simulations

The opamp performance was evaluated over process (fast, typical, slow), supply (1.1V, 1V, 0.9V) and temperature ($-40°$C, 75°C and 125°C) corners by simulating its AC response and transient settling behaviour, as shown in figs A.4 and A.5.

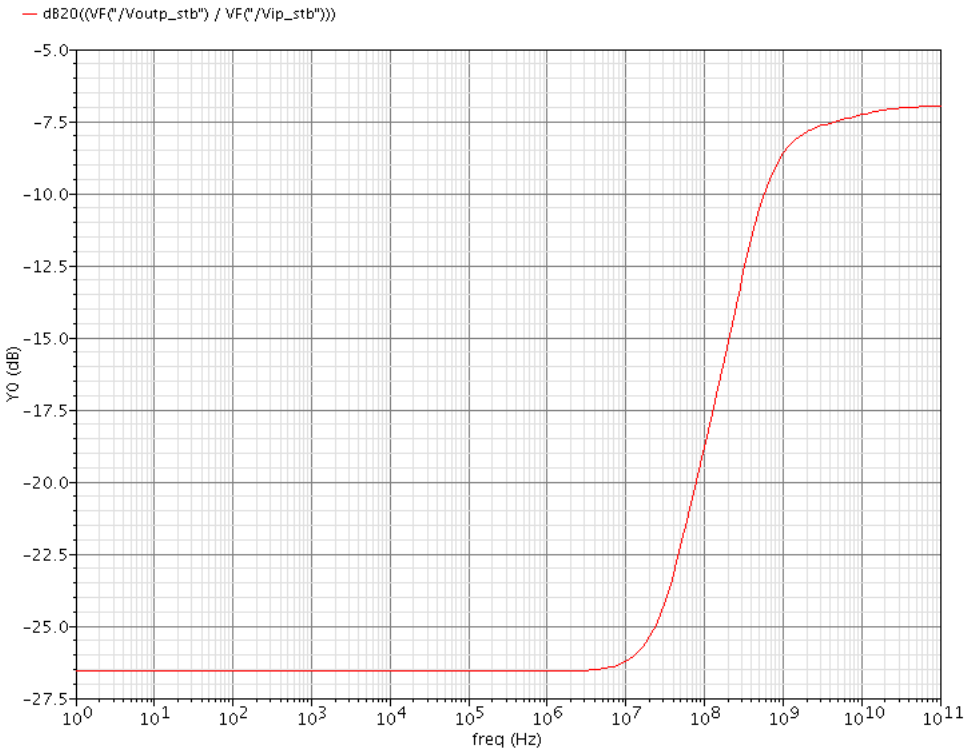


FIGURE A.3: AC response of closed-loop input common-mode gain

A.1.3 Post-layout simulations

The layout of the opamp shown in fig 4.7 was evaluated by running RC-extracted simulations. The AC response and transient settling response for the extracted simulations are shown in fig A.6 and A.7. It can be seen that the results from the extracted simulations match with the schematic level results to a good degree.

A.2 MDAC simulations

The simulation plots for the first stage MDAC of one of the half-ADCs are presented in this section.

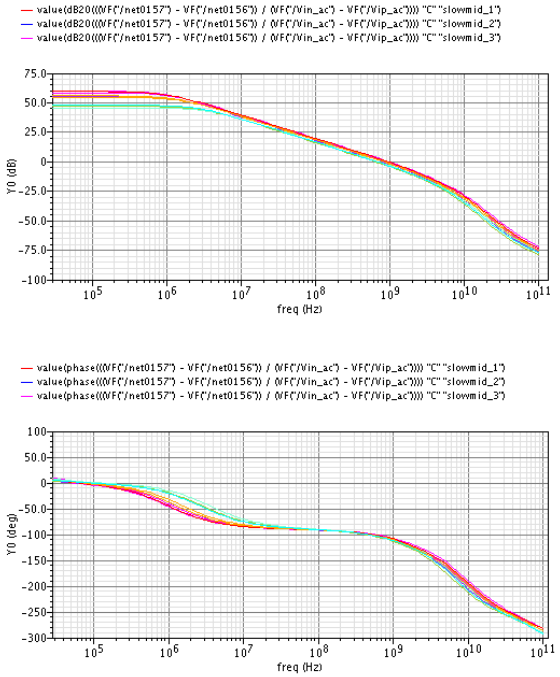


FIGURE A.4: AC response over corners

A.2.1 Input sampling bandwidth

Since the input signal is directly fed to the MDAC, the bandwidth of its sampling network should be higher than Nyquist frequency. Fig A.8 shows the AC Response of input sampling network with 50Ω source impedance.

A.2.2 Dynamic Performance

FFT plots of the MDAC output spectrum are presented for full input signal at different frequencies. Figs A.9 and A.10 show the FFT of the MDAC for a single-tone input at frequencies 3.90625MHz and 246.09375MHz, respectively.

Figs A.11 and A.12 show the FFT of the MDAC for a two-tone input at frequencies 3.90625MHz & 7.8125MHz and 238.28125MHz & 242.1875MHz, respectively.

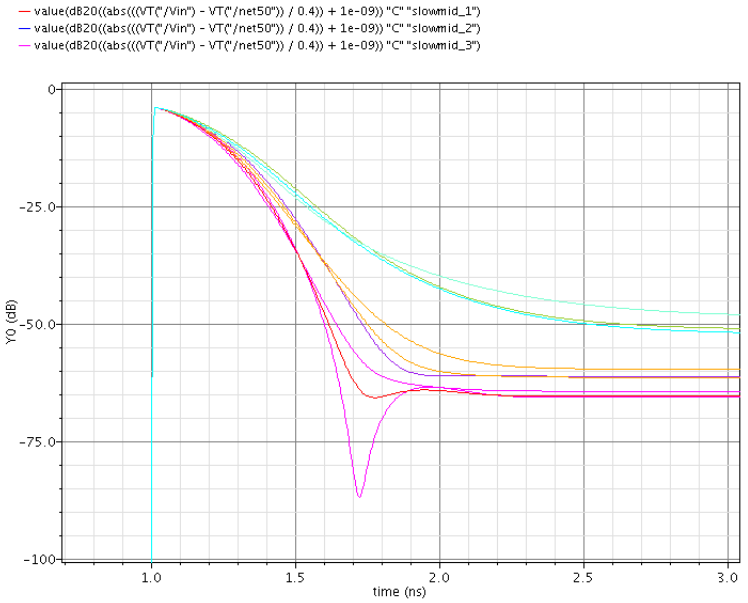


FIGURE A.5: Transient settling response over corners

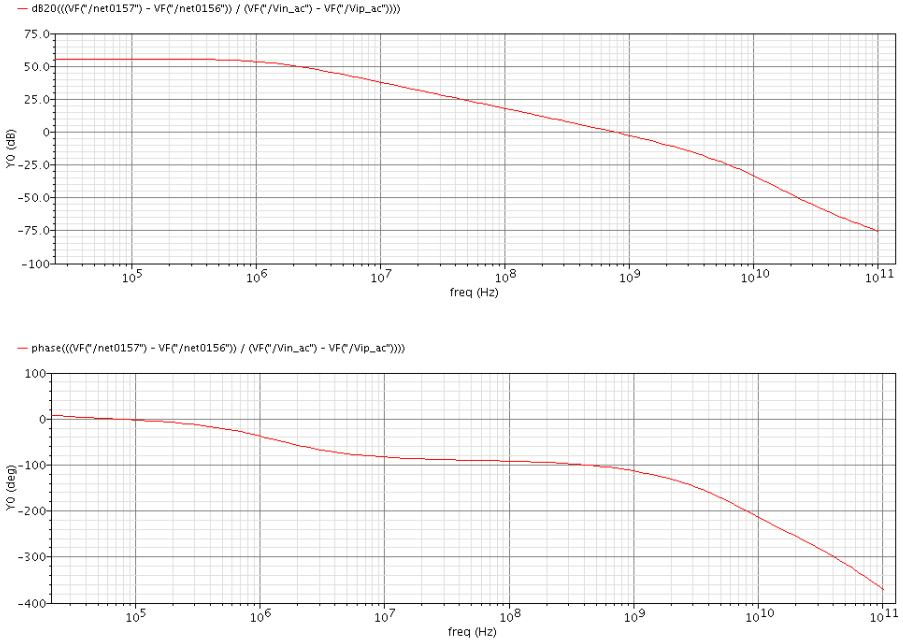


FIGURE A.6: Post layout simulation - AC response

A.3 Comparator BER simulation

The speed of a comparator is measured in terms of bit error rate, which represents the smallest differential input that can be resolved by the comparator in a given decision time. Fig **??** shows the bit error rate simulation of the comparator in

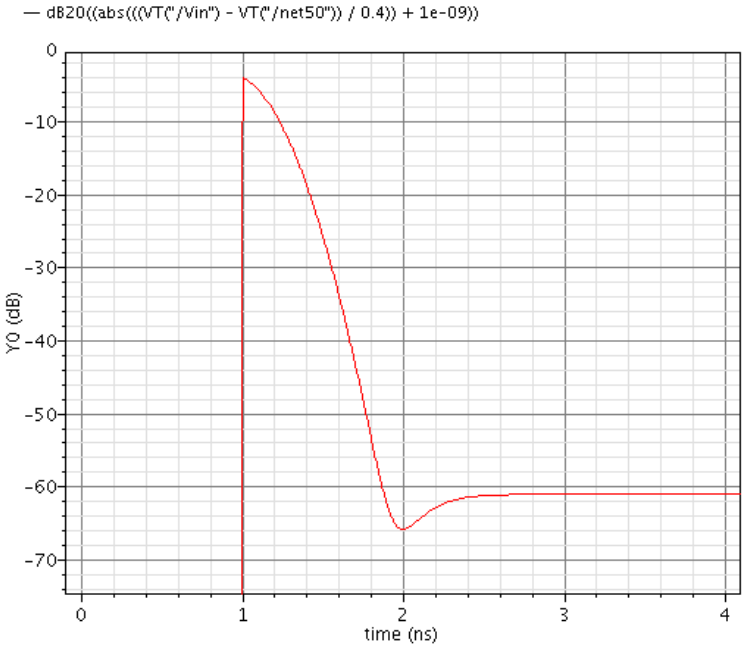


FIGURE A.7: Post layout simulation - transient step response

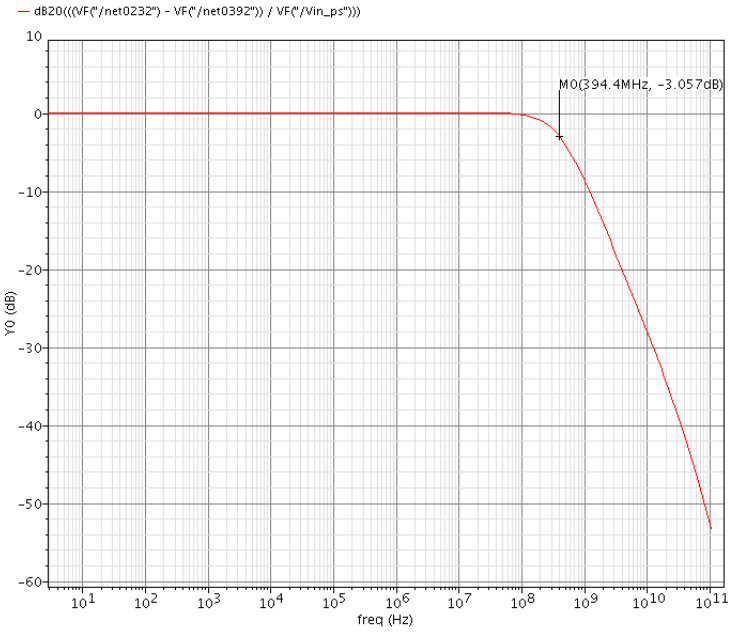


FIGURE A.8: AC Response of input sampling network

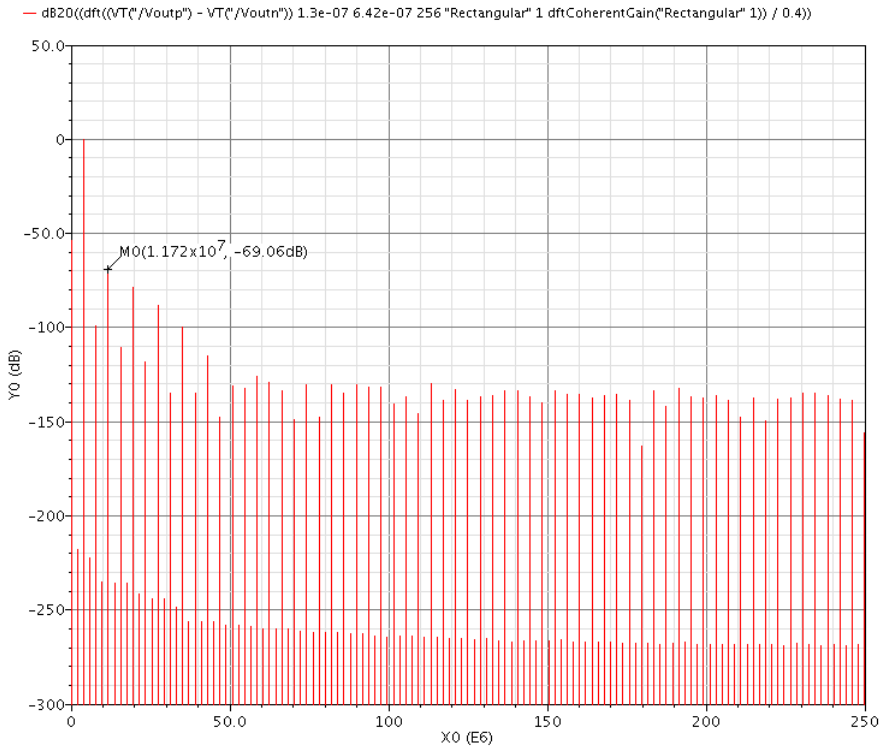


FIGURE A.9: 256-point FFT for input frequency=3.9MHz

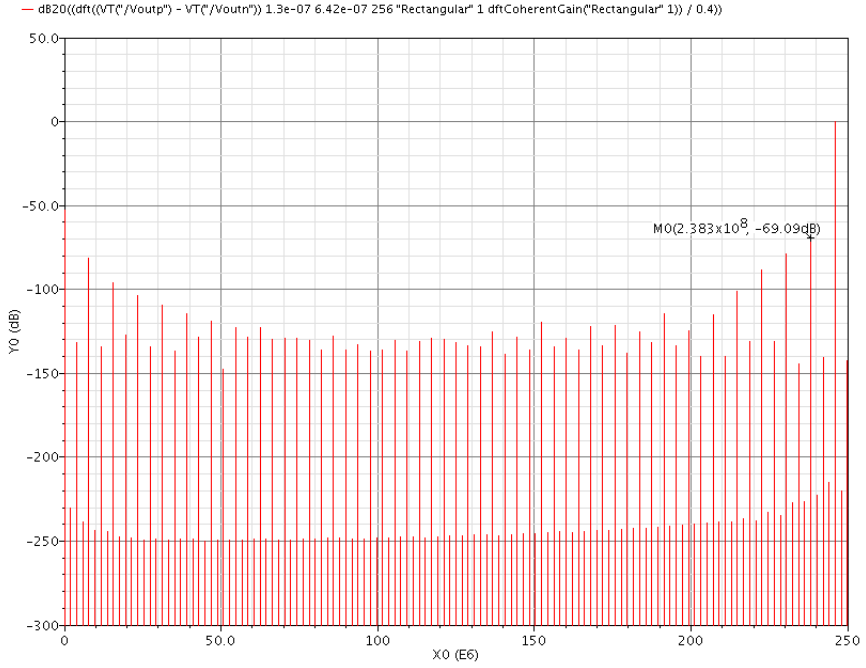


FIGURE A.10: 256-point FFT for input frequency=246MHz

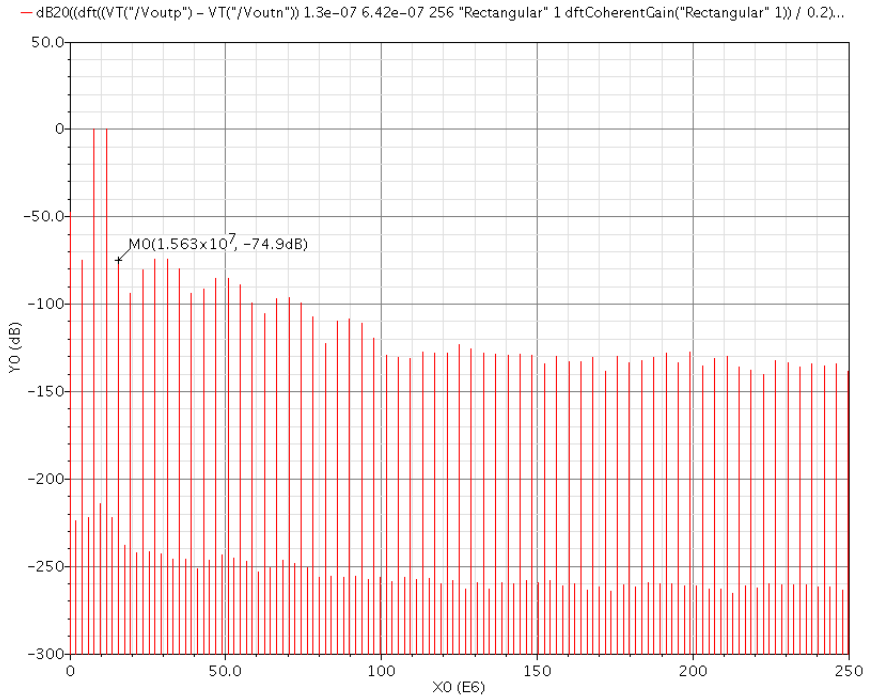


FIGURE A.11: 256-point FFT for input frequencies=3.9MHz and 7.81MHz

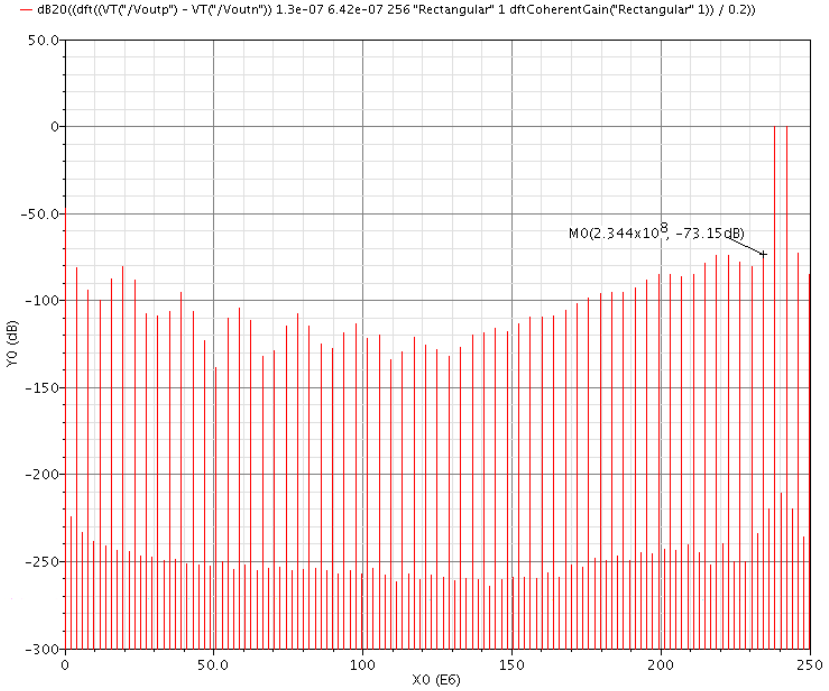


FIGURE A.12: 256-point FFT for input frequencies=238.3MHz and 242.2MHz

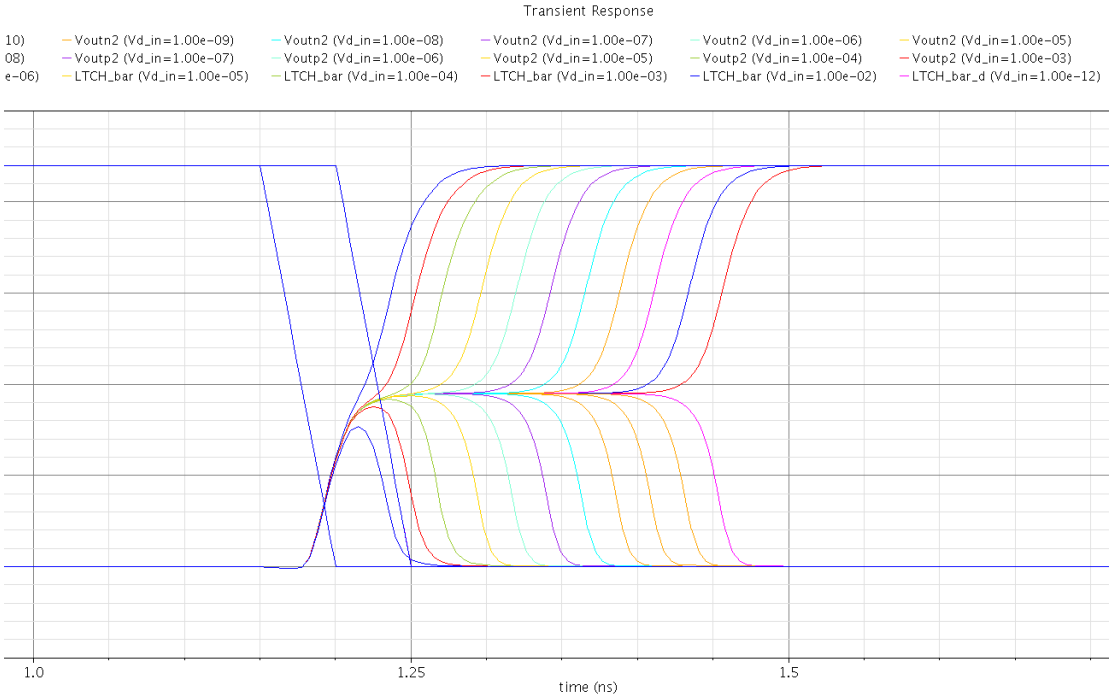


FIGURE A.13: BER simulation

fig 5.4. The comparator achieves a BER of 10^{-12} within a decision time of 300ps, with a time interval for every order being 22.5ps.

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