A Mixed-Signal Multiplexing System for Cable-Count Reduction in Ultrasound Probes

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EEMCS

A Mixed-Signal Multiplexing System for Cable-Count Reduction in Ultrasound Probes

By

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The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled

A MIXED-SIGNAL MULTIPLEXING SYSTEM FOR CABLE-COUNT REDUCTION IN ULTRASOUND PROBES

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QILONG LIU

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MASTER OF SCIENCE MICROELECTRONICS

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Chapter 1 Introduction

1.1 Background

The advance of modern society sees more need for health care. Among the causes of death, cardiovascular disease has been the number one killer according to a report from the World Health Organization (WHO) in 2013 [1.1]. In order to diagnose and heal it sufficiently, imaging technologies such as magnetic resonance imaging (MRI), positron emission tomography (PET) and echocardiography, have been developed. Among them, echocardiography shows its advantages of being low cost, body friendly and capable of providing good imaging quality. For imaging of the heart, transesophageal echocardiography (TEE) has been developed by using the esophagus as an acoustic imaging window. When applying this imaging technique, patients swallow a small probing tube that is positioned in the esophagus close to the heart, where it transmits ultrasonic pulses and receives the resulting reflections. After having been transmitted back to the mainframe and properly processed, the signals collected by the probe can be converted into an image of a heart. A TEE probe is shown in Fig. 1-1.

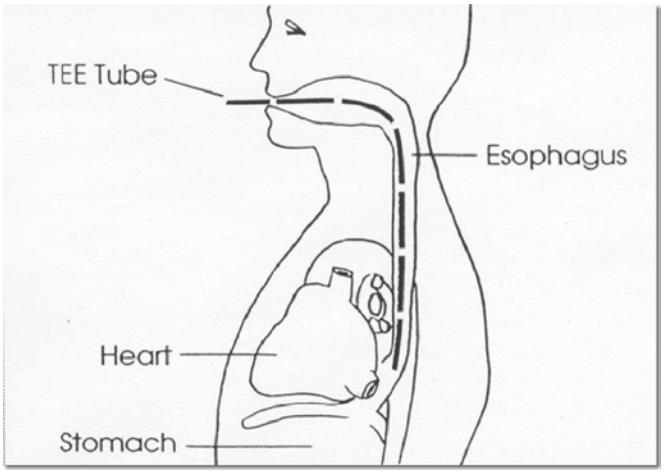


Figure 1-1 TEE diagram [1.2]

In the market there are already medical imaging instruments based on 2D or 3D TEE. For 2D imaging, an 1D transducer array is installed in the probe tip and in one imaging process only a cross-sectional image of the heart can be acquired. As such, the simplicity of the imaging process leads to the complexity of dependence on the physicians' experience. In order to address this issue and to provide better imaging quality, 3D TEE imaging probes are being developed.

In a 3D TEE probing system, a 2D transducer matrix is assembled in the probe tip. In the previous work [1.4], a 45*45 2D TEE rectangular array was proposed, where an analog front end (AFE), as shown in Fig. 1-2 is attached to each transducer element. These AFEs are integrated in a chip that in mounted in the probe tip directly underneath the transducer array. In order to scan the tissue volume of interest, signals reflected arriving at a specific angle are strengthened by the AFE. This is done by delaying the signals arriving at each transducer element in order to emulate a simultaneous receiving from the target point to the whole 2D array. Then the received signals can be summed up in order to enhance SNR. This delay-and-sum technique is referred to as beamforming, which is widely used in a radar systems [1.3].

In the implementation of [1.4], the AFE is composed of a low noise amplifier (LNA), a time-gain-compensation (TGC) amplifier and an analog micro-beamformer (μBF), as shown in Fig. 1.4. After the received signal passes through the transducer for acoustic-electric conversion, it goes through an LNA to maintain the SNR deriving from the transducer in the following stages. Then the TGC compensates for the signal propagation attenuation via amplification with the programmable gains. After that a μBF, which combines signals from a 3*3 subarray, implements the delay-and-sum function as mentioned above. Here the prefix “micro” means the beamformer here can only handle a partial delay-and-sum function which is applied only to a subarray. The complete beamforming of the whole 2D array it is carried out in the mainframe.

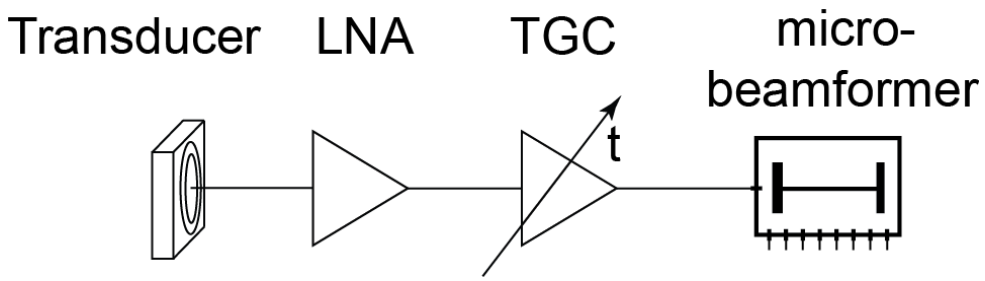


Figure 1-2 Analog front end (AFE) with a transducer element

One benefit that a μBF brings about is the reduction of cable count. Since the 9 transducer elements share one common μBF and generate one output, the overall 45*45 chip-mainframe interconnections are reduced by 9 times, which results in only 225 cables needed for wiring.

However, the size of the interconnection bundle of 225 cables is still very challenging for an endoscope-based application. So a further output stage that can combine outputs from multiple μBFs is necessary, which forms the main goal of the thesis project. As the first trial, 4 μBFs are combined and sent to one output stage so that the total cable count can be less than 60, which more comfortably satisfies the geometry constraint.

In order to accomplish this, we should start from the design requirements, which are illustrated in the next section.

1.2 Design Considerations

1.2.1 Signal Properties

In order to adapt to the µBF of the previous project [1.4], the proposed output stage should be compatible with the signal properties of the µBF's output, which are listed in Table 1-1.

Table 1-1 Signal property of µBF's output

Property	Value	Description
Signal frequency	6 MHz	Gaussian wave, with 50% bandwidth
Signal amplitude	200 mV peak-to-peak	sampled-and-held output
Sampling frequency	25 MHz	-
Dynamic range	40 dB	output of µBF

Besides that, two more requirements are added to clarify the design boundary, as listed in Table 1-2.

Table 1-2 Added requirements on the output stage's output

Requirements	Value	Description
Distortion (THD)	-40 dB	Derived from dynamic range
Crosstalk (µBF to µBF)	-40 dB	Derived from dynamic range

Here both the distortion and crosstalk requirements are derived from the dynamic range at the µBF's output. By doing this the above non-idealities can be of the same level as the noise.

Besides the requirements set by the conveyed signal, the cable as a loading gives another boundary to the design of output stage.

1.2.2 Cable Property

In order to carry the signal produced by the chip at the tip of the endoscopic probe to the mainframe, 3-meter-long micro-coaxial cables manufactured by SUMITOMO [1.5] are used. Being different from on-chip capacitive loading, the long cable exhibits a complicated impedance to the output stage. The accompanied noise, transmission line effects, crosstalk and the finite bandwidth together set new

requirements for the output stage and furthermore for the whole system. In Chapter 2 the details of the cable characterization is given.

1.2.3 Power and Area Restrictions

Since the TEE probe is of endoscopic type, power and chip area are the critical limitations that should be designed with much emphasis. As a rough restriction, the power and the area of the proposed output stage should not exceed those consumed by the µBFs which share it. Based on the implementation in [1.4], one output driver should consume less than 9mW and occupy less than $2mm^2$, when the technology migration from 0.35 µm to 0.18 µm is taken into account.

1.3 Solutions

1.3.1 Possibilities and Limitations

In order to realize the challenges of the thesis project, first, the possible solutions and existing limitations are briefly discussed.

For the signal form to be transmitted, given the aforementioned required signal quality, it may seem more reasonable to convert the signals into digital domain for its robustness against distortion, noise and interference. However, analog to digital conversion using conventional design approaches would likely lead to a significant increase in complexity and power consumption. While with appropriate improvements in ADC design a digital solution might become realistic, it is considered outside the scope of this project. Here, instead, we will investigate the option of transmitting multiple analog signal through a single cable.

Nevertheless, there are also some techniques that we can leverage from digital wireline communication. In order to transmits signal from several µBFs via a shared cable, multiplexing schemes—such as time-division multiplexing (TDM) and frequency-division multiplexing (FDM), and code-division multiplexing (CDM), could be used in order to reduce the cable count.

Last but not least, power and area budgets assigned to the output stage lay the ultimate obstacle of the multiplexing and transmission system.

1.3.2 Introduction to the Thesis Work

In the thesis work, to tackle with the aforementioned challenges, an analog time-multiplexing system is proposed and implemented, as shown in Fig. 1-3.

The whole system consists an low-power current-mode multiplexer as the output stage to transmit signals from multiple µBFs into one coaxial cable. At the other end of the cable, a transimpedance amplifier (TIA) followed by an extra gain stage (EA) is designed to boost the signal to a level suitable for digitization. And then an equalization algorithm takes over the digitized signals in order to repair the non-ideal effects from the cable and to resolve signals from different µBFs. In the end signals are de-multiplexed to their corresponding channels, and signal transmission ends.

To make terminology clear and consistent in the thesis (see labels in Fig. 1-3), term “driver” is used to refer to the individual driving unit with input sampling circuit, which is connected with an µBF (including 3*3 LNAs and TGCs). “Transmitter” (TX) refers to the combination of four drivers and the current-mode multiplexer. “Channel” refers to the transmission media, which is the cable in our case. Sometimes it also refers to the whole signal chain from TX to RX when it does not cause ambiguity in the context. “Receiver” (RX) is used to specify the unit composed of the TIA and the EA in the other end of the cable. *fs* indicates the sampling clock for each µBF, which is 25 MHz in the project. “User” refers to the equalized and demultiplexed result corresponding to separate µBF.

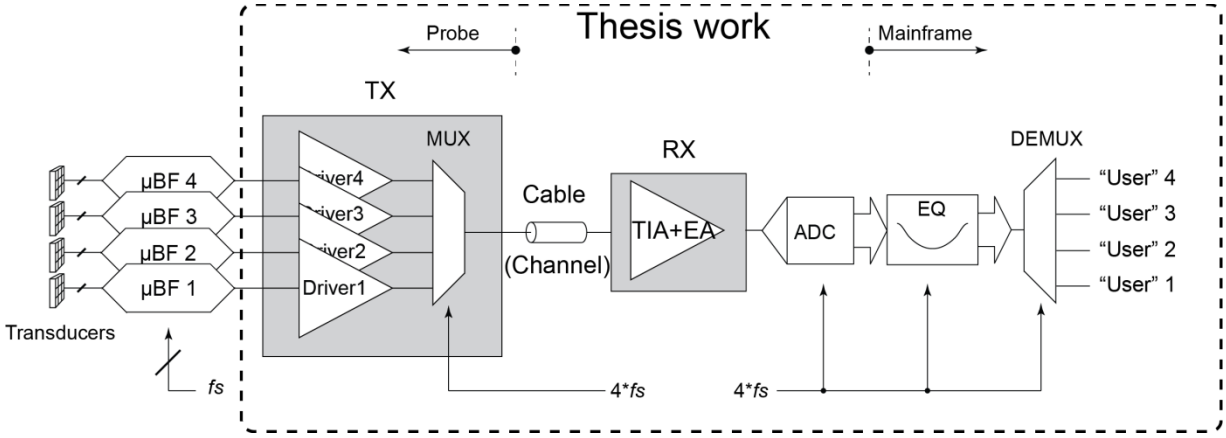


Figure 1-3 Building blocks of the thesis project

1.4 Summary

In this chapter the background of the thesis work has been introduced. With an emphasis on the cable characteristics and the power/area budget, the basic design considerations are explained. In the last part, an overview of the thesis work has been given. In the following chapters, Chapter 2 is dedicated to the comparison of multiplexing schemes and the exhibition of transmission line effect after cable characterization. Chapter 3 mainly deals with equalization algorithms which are proposed to cancel

the non-idealities associated with transmission line effect. A system-level design and optimization are given is Chapter 4, where the specifications of all the building blocks are determined and optimized in SNR and residual crosstalk points of view. In Chapter 5 the transistor-level TX design is given. Measurement results are given in Chapter 6, with a discussion about the discrepancies between modelling and measurement. In the last chapter of the thesis a summary of the project work is provided, including both contributions and potential improvements.

1.5 References

[1.1] “Cardiovascular diseases.” http://www.who.int/mediacentre/factsheets/fs317/en/, January 2015.

[1.2] “Transesophageal echo.” http://www.umanitoba.ca/medicine/units/cardiac_sciences/teeinfo.htm, January 2015.

[1.3] “Beamforming.” http://en.wikipedia.org/wiki/Beamforming, February 2015.

[1.4] Z. Yu, *Low-Power Receive-Electronics for a Miniature 3D Ultrasound Probe*, Ph.D. Thesis, Delft University of Technology, Delft, the Netherlands, 2012.

[1.5] Micro flex coaxial cable (MFCX) datasheet:
http://www.sei.co.jp/ewp/J/products/detail/pdf/6_02.pdf

Chapter 2 Multiplexing and Cable Modelling

In this chapter, the question of how to squeeze signals from multiple micro-beamformers (µBF) into one cable will be answered. First, several multiplexing schemes are proposed and after comparison time-multiplexing is selected. Next, the cable characterization and modelling are carried out in order to well fit time-multiplexing into the project. During this process we find a distributed model of the cable – transmission-line modelling is inevitable to be used in the frequency of interest. In the last part of this chapter, the non-idealities of the cable are pointed out and explained in detail, as a preparation for the system solution proposed in the following chapters.

2.1 Comparison between Multiplexing Schemes

As mentioned in Chapter 1, cable count reduction is the main target of the project. As the first trial, the output signals from 4 µBFs are designed to be transmitted via a shared cable in order to achieve the required reduction in cable count. To achieve this, a multiplexing scheme becomes necessary to be implemented with focus on minimizing the power consumption on the probe side of the cable. In the following discussion, several common schemes, such as frequency-division multiplexing (FDM), code-division multiplexing (CDM) and time-division multiplexing (TDM) are analysed.

FDM

In FDM, signals from each µBF are modulated by a sinusoidal carrier into a separate frequency range [2.1][2.2]. In order to fit FDM into the frame of our application, the sinusoidal carrier should be modified by simpler implementation. Here, square-wave signals with different fundamentals are used as carriers, as shown in Fig. 2-1, enabling implementation using simple chopper switches. Furthermore, I/Q modulation can be also used to improve the frequency band utilization. On the receiver side, coherent demodulation can be applied as a replacement of sinusoidal demodulation and low-pass filtering.

CDM

In CDM, signals from different drivers are coded by different series of pseudo random numbers [2.1][2.3]. Due to the orthogonality of those random series, at the receiver side signals from one driver will only be recognized by its corresponding receiver via the unique decoding series.

In the frequency domain, CDM is a spread-spectrum technique. It means that during transmission, signal power spectrum density (PSD) is wide spread and even hidden below the noise floor of the

physical channel, which is illustrated in Fig. 2-2. After being reconstructed at the corresponding receivers, the noise and interference during transmission are randomized and can be filtered out.

TDM

In TDM, or equivalently time-multiplexing, signals share one physical channel by time-interleaving [2.1][2.4]. In one multiplexing cycle, fs, the whole period is uniformly divided into several slots, and signals from drivers are assigned into the slots sequentially. The TDM control are plotted in Fig. 2-3, where “1” means the corresponding drivers are activated and “0” means being idle.

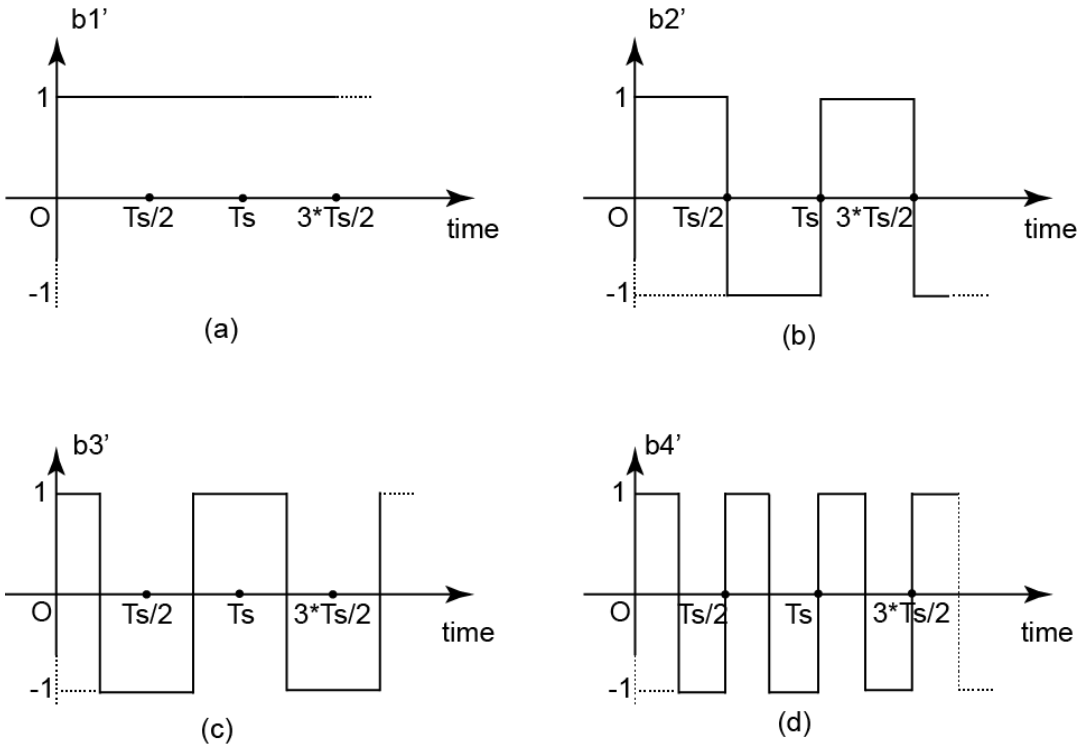
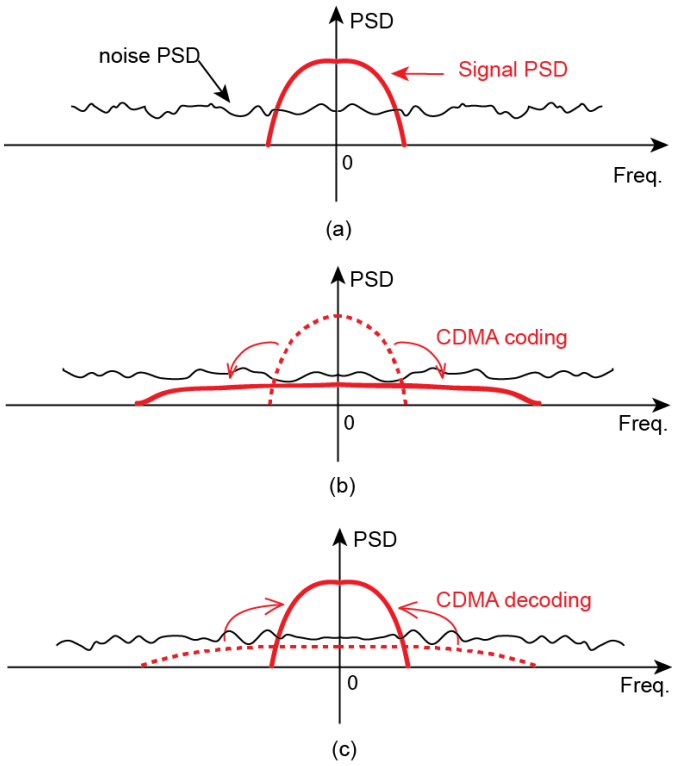


Figure 2-1 Square-wave modulation carriers for different drivers in the modified FDM scheme



(a) PSD at TX (b) PSD after CDM coding

(c) PSD after decoding at RX

Figure 2-2 Spectrum spreading character of CDM

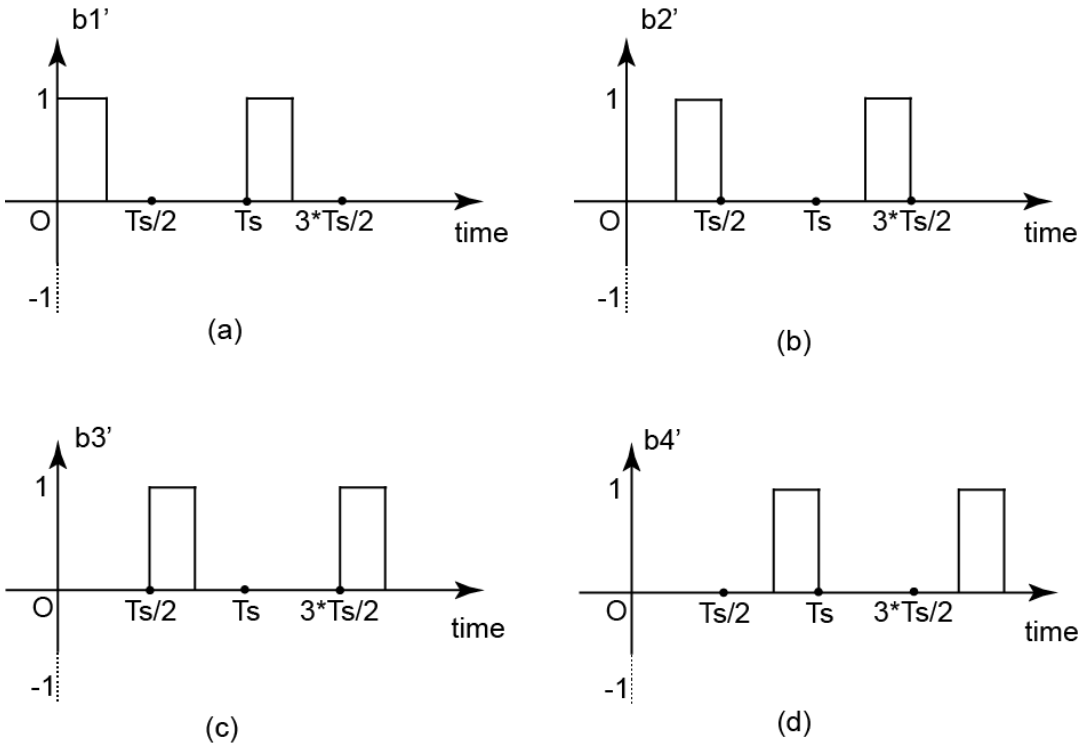


Figure 2-3 TDM control

As a summary, a comparison is made between different multiplexing schemes, which is tabulated in Tab. 2-1.

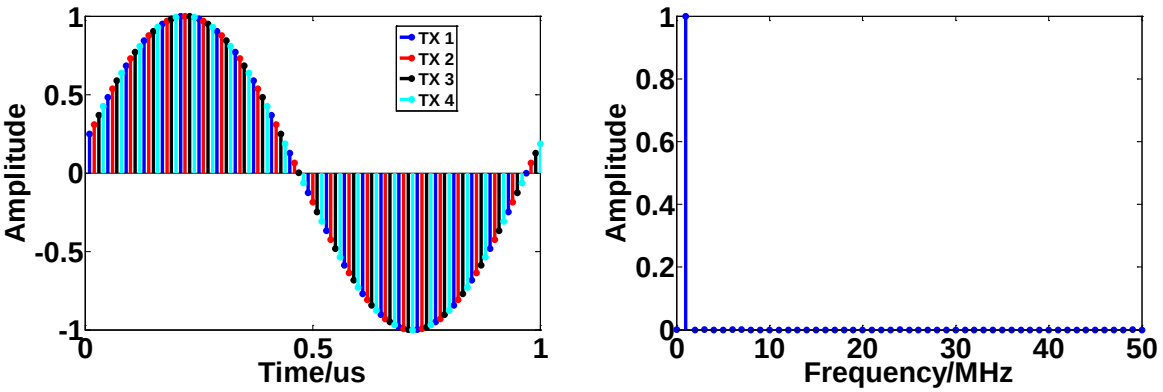
Table 2-1 Comparison between different multiplexing schemes

Schemes	Implementation	Characteristics
FDM	Chopper, clocks with multiple frequencies and I/Q phases	1. All the drivers are on all the time, but their bandwidths can be lower than those in TDM for looser settling requirements. 2. Different modulation frequencies indicate the complexity of digital control, along with topology asymmetry among the drivers. 3. Phase misalignment between I/Q paths will cause spectrum leakage to other signal bands.
CDM	Chopper, random-number-generator, timing control on both RX and TX	1. Drivers are on all the time. 2. Orthogonal coding requires extra coder at TX side, which increase the complexity of TX design. 3. Better interference immunity during transmission compared to FDM and CDM.
TDM	Multiplexing control, clock with identical frequency and multiple phases	1. Drivers can be off when they are idle. 2. Simpler timing control compared to FDM and CDM 3. Lighter design burden due to the uniform settling requirement for all the drivers compared to FDM.

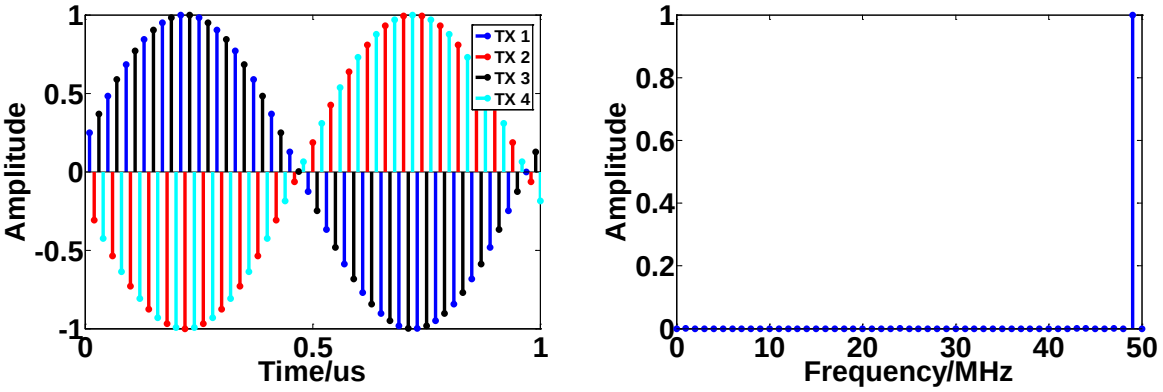
From the comparison in Tab. 2-1, we find TDM shows its advantage over the other two by simpler implementation in both digital control and driver design. More specifically, when the number of μBFs shared by one cable increases, the asymmetry between the different drivers and their controls becomes more obvious in the case of FDM, which lays heavier burden on the multiplexer design. Accordingly TDM, is chosen as the multiplexing scheme for the target of cable count reduction in our application. Next we start to analyse the spectral characteristics of time-multiplexed signals.

2.2 Spectral Characteristics of Time-multiplexing

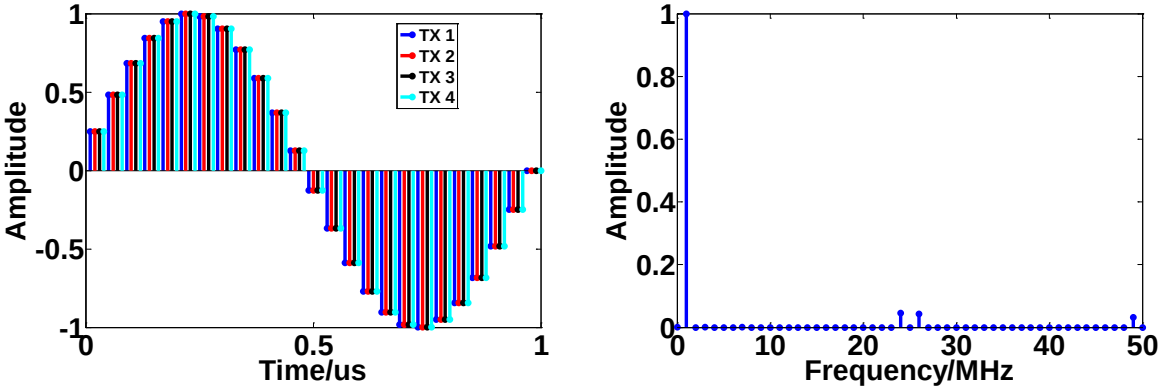
Even though time-multiplexing show its advantage from the implementation point of view, it does not provide better spectrum utilization than its competitors. To explain this, an example of TDM in both time and frequency domain is given in this section. In Fig 2-4 four 1 MHz signals with different phases are sampled at 25 MS/s and are then time-multiplexed. The FFTs of the resulting output signals are also shown in Figure 2-4.



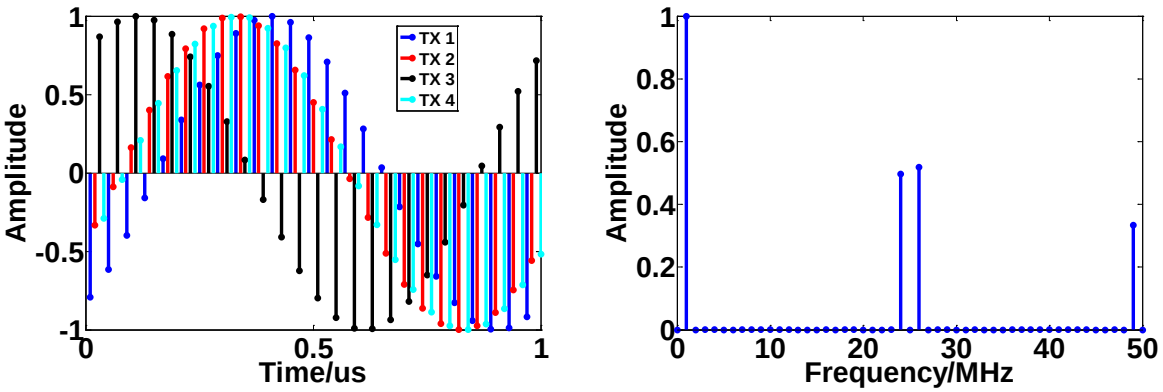
(a) In phase



(b) Out of phase



(c) “Staircase”



(d) Random phase

Figure 2-4 Time and frequency domain of multiplexed signals

From Fig. 2-4 it can be found that:

- The global sampling frequency observed from the multiplexed signal is N times larger than the individual sampling frequency, where N is the number of drivers which share the cable.
- The spectrum of multiplexed signals are in the form of several tones within the Nyquist interval, and each tone contains partial information from all the drivers. It indicates that signal from an individual driver cannot be filtered out by a single band-pass filter.
- The amplitudes of the tones are associated with the relative phase shifts between the signals. However, later it will be shown that the whole signal chain (from TX to RX) shows a non-uniform frequency response in the Nyquist interval, which makes the SNR at the output of RX hard to be estimated. This will be shown in Chapter 6.

As explained above, the signal spectrum after multiplexing is expanded as compared to the case in an individual driver. This makes the cable's high-frequency behaviour critical to the system design. Allowing for this, in the next section, cable modelling will be given in detail.

2.3 Cable Modelling

2.3.1 Cable Characterization

In order to efficiently apply the time-multiplexing in the project, the cable should be characterized to clarify its high-frequency behaviour. Normally, a cable is described using four basic electrical parameters: shunt conductance (G), shunt capacitance (C), series resistance (R) and series inductance (L), all of which are specified by unit length [2.5]. Fig. 2-5 gives a lumped model of a unity-length cable with these parameters. From the cable specifications provided by Oldelft [2.6], the values of R, L, C, G are tabulated in Tab. 2-2. They can be also be obtained by S-parameter measurement via a

vector network analyzer (VNA) [2.7][2.8], of which the result is shown Fig. 2-6. As for the details of VNA measurement please refer to Appendix A.

Table 2-1 Cable specifications [2.6][1]

Parameter	Value	Unit
Series resistance (R)	Max. 22	Ω/m
Shunt resistance (G^{-1})	Min. 1524	MΩ/km
Shunt capacitance (C)	120±10 (1KHz)	pF/m
Series inductance (L)	300 (10MHz)	nH/m

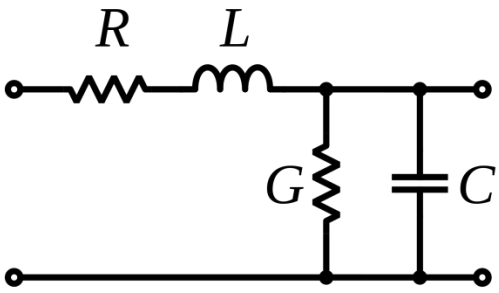


Figure 2-5 Lumped model of a unity-length micro-coaxial cable[2]

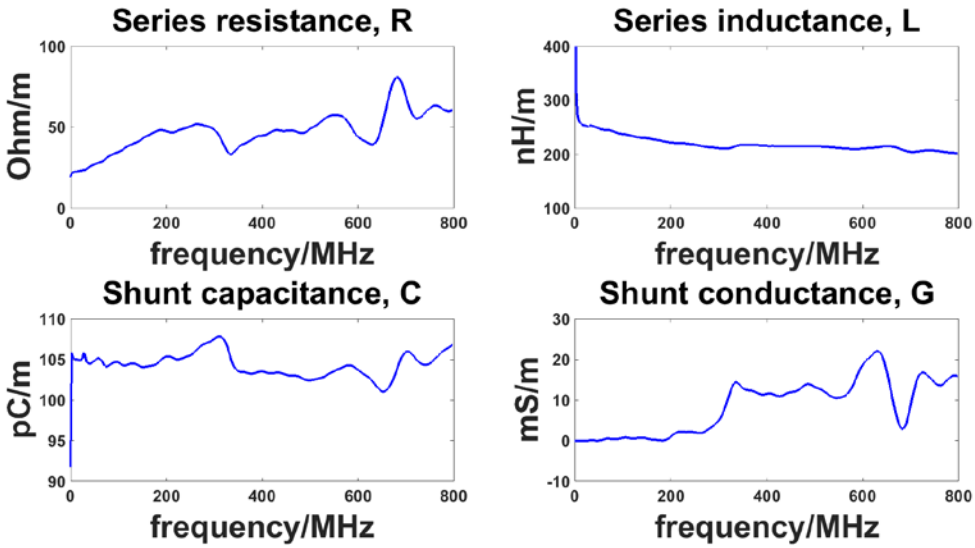


Figure 2-6 Extracted R, L, C, G from VNA measurement

[1] Here the shunt resistance is the value given in the specifications without any converting.
[2] Here the series resistance (R) and the series inductance (L) includes the contribution from both the core and the shield.

Fig. 2-6 shows a good agreement in *L* and *C* between the cable specifications and measurement, while *R* and *G* exhibit frequency-dependent effect. The frequency-dependent *R* it is due to the skin-effect [2.5], and frequency-dependent *G* is caused by dielectric relaxation [2.9][3].

In order to accurately model the cable with the above parameters, one thing that should be examined is the necessity to use a transmission line model in the thesis project. To verify this, we first check whether *L* or *C* is notable in the frequency of interest. By calculation we can get the critical frequency above which *L* becomes dominant to *R*:

$$f_{L,dom} = \frac{l \cdot R}{2\pi(l \cdot L)} = 10.6MHz \qquad (2-1)$$

where *l* is the cable length. And the critical frequency of *C* is

$$f_{C,dom} = \frac{1}{2\pi(l \cdot R)(l \cdot L)} = 6.7MHz \qquad (2-2)$$

Since $f_{L,dom}$ and $f_{C,dom}$ are within the signal band (6MHz~44MHz), both *L* and *C* are indispensable in the cable model. Next we will check if the cable is a distributed model in the signal band. As a rule of thumb in radio-frequency IC design [2.10], a cable or trace is modelled as a distributed model when its physical length is shorter than 1/10 of the wavelength of signal-carrying electromagnetic (EM) wave. Judging from the calculated wavelength shown in Fig. 2-7, it suffices to claim that a distributed model, namely transmission line effect should be taken into account in the signal frequency of interest. From the next section we will elaborate it in our application.

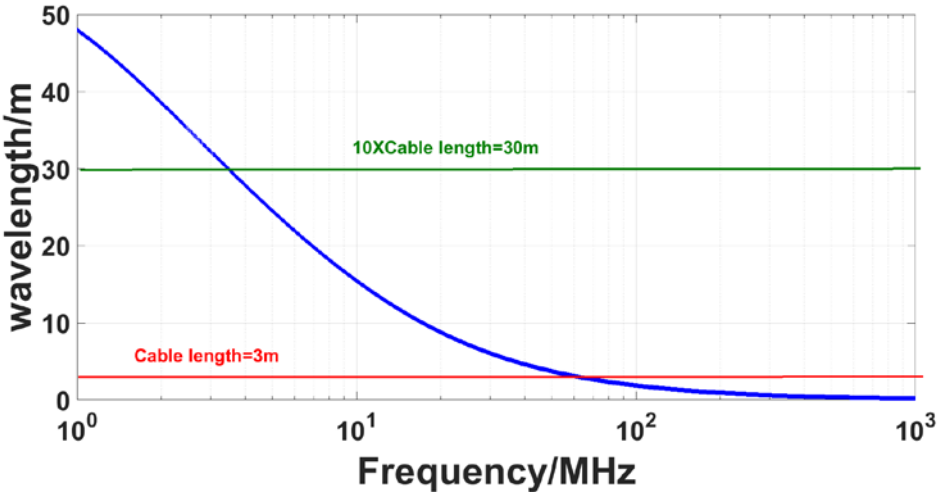


Figure 2-7 Wavelength of EM wave in the micro-coaxial cable

[3] For convenience in the following time domain simulation the parameters are interpolated linearly within the frequency of our interest (DC-200MHz) instead of using the extracted ones.

2.3.2 Transmission Line Effect of a Micro-Coaxial Cable

Pulse Response of Transmission Line

Due to the sampled-and-held nature of the input signal, the time-multiplexed signals on the cable will have the form of amplitude-modulated pulses. So it is important to interpret the cable's pulse response in the context of transmission line effects.[4] In the simulation configuration shown in Fig. 2-7, a pulse mode voltage source with certain output impedance Z_S is connected to the cable, and at the other end a load impedance Z_L is used to sense the output voltage. To make the simulation close to the real application, the pulse duration is chosen equal to the time slot used for single driver transmission (10ns). Fig. 2-8 gives the simulation result of the pulse response in the single-ended matching case, where the cable is loaded by its characteristic impedance. From Fig. 2-8 several key phenomena are observed, which will be explained in detail as follows.

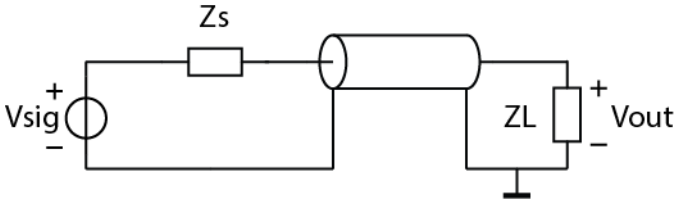


Figure 2-8 Configuration of voltage mode transmission

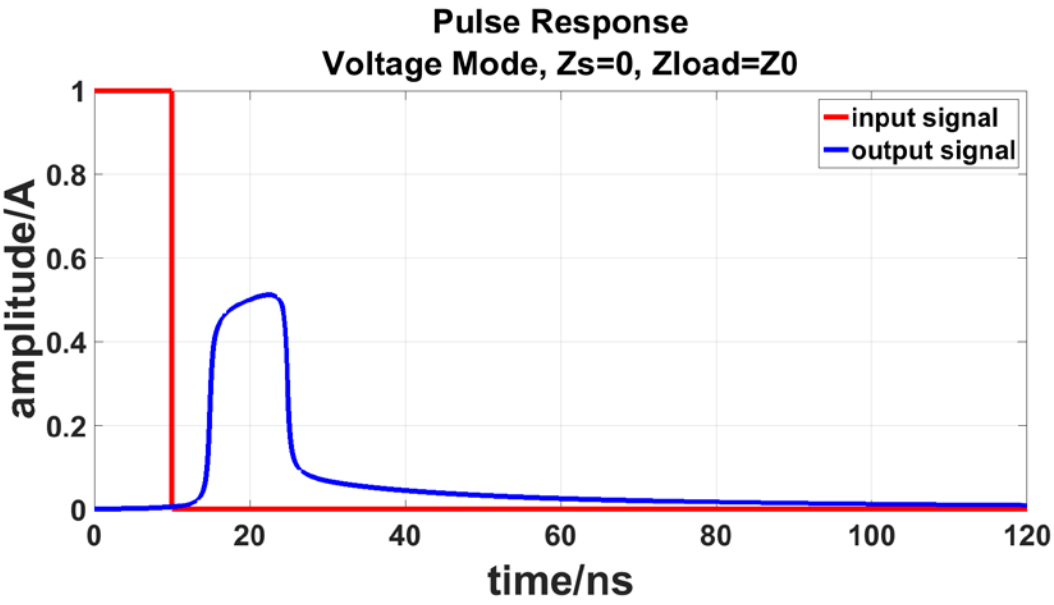


Figure 2-9 Pulse response in a single-ended matching voltage mode transmission

[4] In the following simulations the electrical parameters are interpolated from the measurement data. As for the details of time domain simulation, please refer to [2.11].

Attenuation

From Fig. 2-9 it can be observed that the peak of the output signal is around a half of the input, which shows obvious attenuation. This is due to the cable's intrinsic loss which dissipates the signal amplitude during propagation. As a result such an inevitable effect will lead to reduced output amplitude compared to that at the input port, which also gives the difficultly of SNR estimation at RX side. However, the cable-induced attenuation can be compensated by choosing an unmatched load which boosts the received amplitude via reflection. But extra penalty will paid as well, which will be explained later.

Dispersion

Dispersion in a lossy transmission line can also be observed in Fig. 2-8. Compared with attenuation, dispersion is more serious because it can cause obvious crosstalk between signals from different drivers during multiplexing.

Essentially speaking, dispersion is due to the non-uniform propagation velocity across frequency which distorts the shape of the signals. As shown in Fig. 2-10, low frequency components propagate slower than those with high frequencies. Since a pulse spans a wide frequency range, the velocity difference appears in the form of a sharp rising edge for the high frequency components, and a long tail for the low frequency parts.

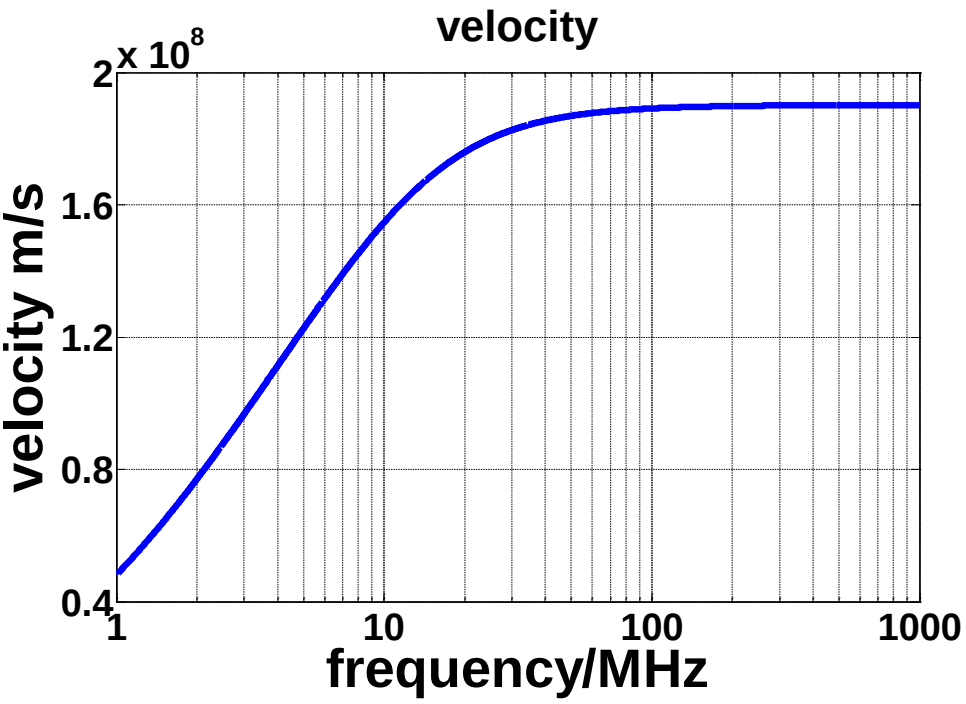


Figure 2-10 Propagation velocity Vs. frequency

Reflection

If Z_S or Z_L is not well matched with the characteristic impedance (plotted in Fig. 2-11), reflection will occur at the source or the load, which can change the received voltage amplitude and generate multiple reflections spaced by certain propagation delays. In the simulation result shown in Fig. 2-12, a loading condition of Z_S=0 Ω, Z_L=100 kΩ is chosen to illustrate such an issue. It can be observed in Fig. 2-12, that at the output there is a pulse with negative polarity arriving 30 ns later than the first received pulse. It is due to reflection caused be the unmatched terminations at both ends of the cable.

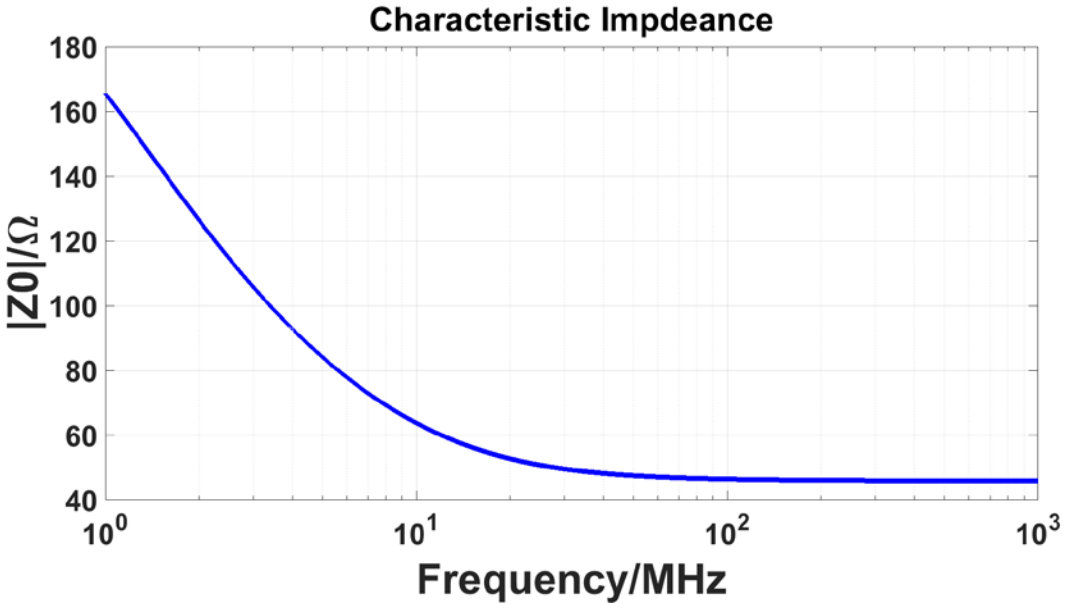


Figure 2-11 Characteristic impedance of the micro-coaxial cable

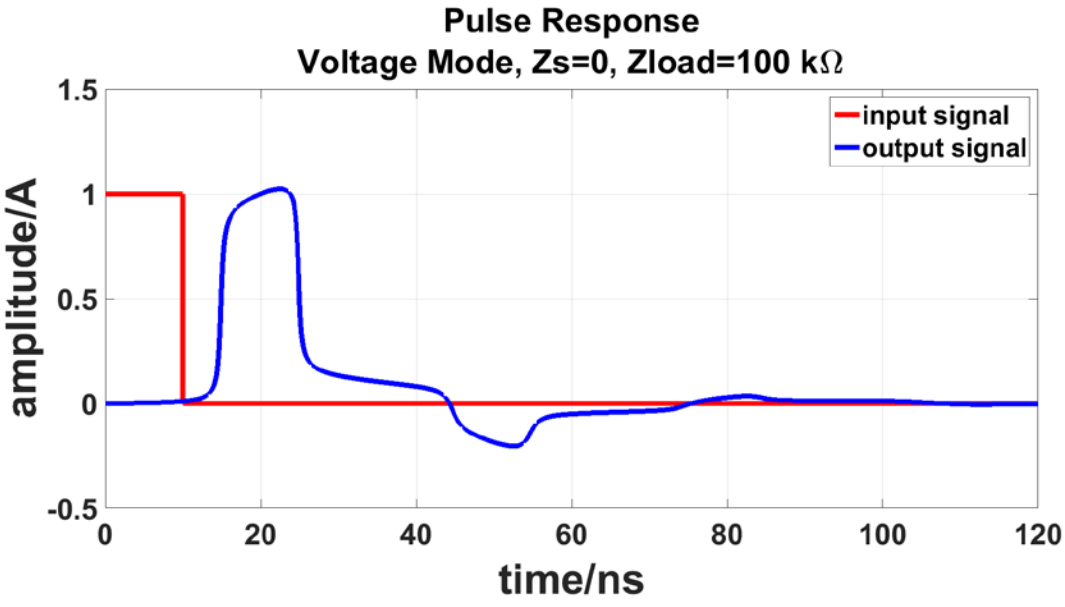


Figure 2-12 Pulse response of a double-ended unmatched transmission line

As mentioned in the above discussion, an unmatched loading can actually help to compensate the propagation attenuation, which can be observed by the comparison between Fig. 2-9 and Fig. 2-12. But the companied reflections present extra difficulty of cancelling the crosstalk between the multiplexed signals.

Allowing for the aforementioned phenomena presented by using pulse response, the conventional matching condition used in digital wireline system design might be abandoned [2.12][2.13]. From the comparison between Fig. 2-9 and Fig. 2-12 it can be found that in time domain the reflections are located in the long tail caused by the dispersion, which means from the crosstalk point of view, the loss of the cable might be the main concern compared with an unmatched termination. From the SNR point of view, an unmatched load can actually help to boost the received signal without any active components. Last but not least, the implementation will be more straightforward if we give up to realize an varying impedance across the signal frequency range (after multiplexing) in order to match the cable's characteristic impedance. In Chapter 4 a quantitative analysis of the above insight will be carried out.

Noise Performance of the Micro-Coaxial Cable

Besides the transmission line effects shown in the time-domain simulation, the cable's distributed character also affects its noise performance. To illustrate this, we first introduce the concept of a 2-port network [2.5][2.14]. A 2-port network is composed of 4 terminals which forms two pairs. Each terminal pair is called as a port if the following condition is satisfied: the current entering one terminal should equal that coming out of the other one. From the above definition we identify that a cable is a 2-port network, since the above condition is automatically satisfied due to Kirchhoff's law.

Noise in a 2-port network can be modelled using two equivalent noise sources: noise voltage v_n and noise current i_n, as labelled in Fig. 2-13.

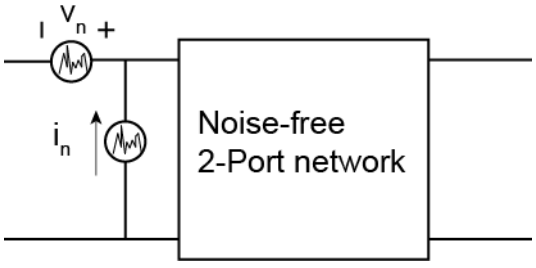


Figure 2-13 Noise parameters in the 2-port network

Normally there is partial correlation between v_n and i_n. In time domain their correlation can be expressed as

$$i_n(t) = Y_{cor}(t) \cdot v_n(t) + i_u(t) \qquad (2-3)$$

where i_n is the input-referred noise current and v_n is the input-referred noise voltage as labelled in Fig. 2-13. Y_{cor} denotes the correlation coefficient between i_n and v_n. i_u stands for the uncorrelated noise current, which is due to the different transfer functions that an independent voltage source in the network experiences when it is referred back to the input port. To illustrate this we decompose a 2-port network into two separate parts, in either of which there is only an independent voltage source, as shown in Fig. 2-14.

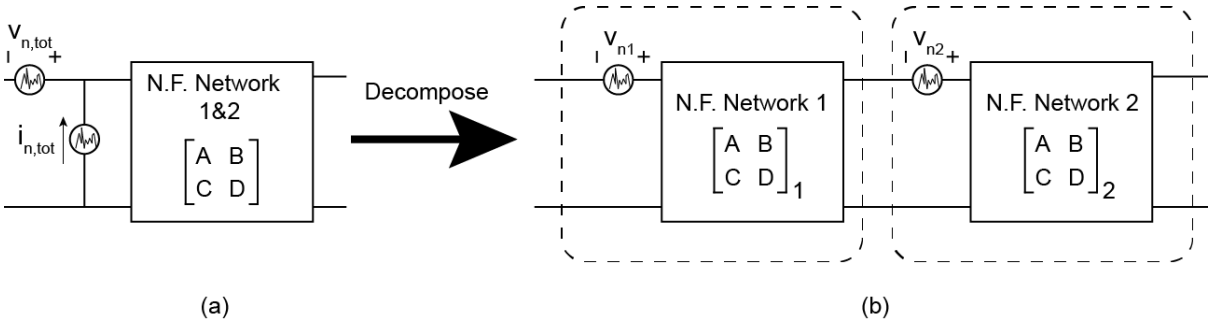


Figure 2-14 Decomposition of a 2-port network based on the noise source separation

By using v_{n1} and v_{n2}, $v_{n,tot}$ and $i_{n,tot}$ can be expressed as follows,

$$v_{n,tot} = A_1 \cdot v_{n2} + v_{n1} \qquad (2-4a)$$

$$i_{n,tot} = C_1 \cdot v_{n2} = \frac{C_1}{A_1} \cdot v_{n,tot} - \frac{C_1}{A_1} \cdot v_{n1} \qquad (2-4b)$$

where A_1, C_1 are the hybrid parameters of Network 1, as labelled in Fig. 2-14(b). If we take $v_{n,tot}$ and v_{n1} as two independent noise sources, then $i_{n,tot}$ is found to be composed of two parts contributed by $v_{n,tot}$ and v_{n1}, where the latter gives an uncorrelated noise current besides that from $v_{n,tot}$:

$$i_{n,tot} = \frac{C_1}{A_1} \cdot v_{n,tot} + i_{u,tot} \qquad (2-5)$$

where

$$i_{u,tot} = -\frac{C_1}{A_1} \cdot v_{n1} \qquad (2-6)$$

Now it has been found that an uncorrelated noise current does exist due to the different transfer functions of the independent noise sources.

In frequency domain, the power spectrum densities (PSD) of i_n, v_n and i_u of a 2-port network can be expressed in the form of the noise equivalent transconductance and resistance expressed as follows,

$$S(i_n) = 4kT \cdot G_n \qquad (2-7a)$$

$$S(v_n) = 4kT \cdot R_n \qquad (2-7b)$$

$$S(i_u) = 4kT \cdot G_u \qquad (2-7c)$$

where G_n, R_n and G_u are the fictitious terms only used to specify the noise performance. For the cable used in the project, G_n, R_n and G_u can be easily calculated based on the extracted electrical parameters shown in Fig. 2-6 [2.15]. In [2.15], the relation between them is also given,

$$G_n = |Y_{cor}|^2 \cdot R_n + G_u \qquad (2-8)$$

By expression $(2-8)$ we can separately calculate the noise contributions in G_n due to R_n and G_u, which are plotted in Fig. 2-15.

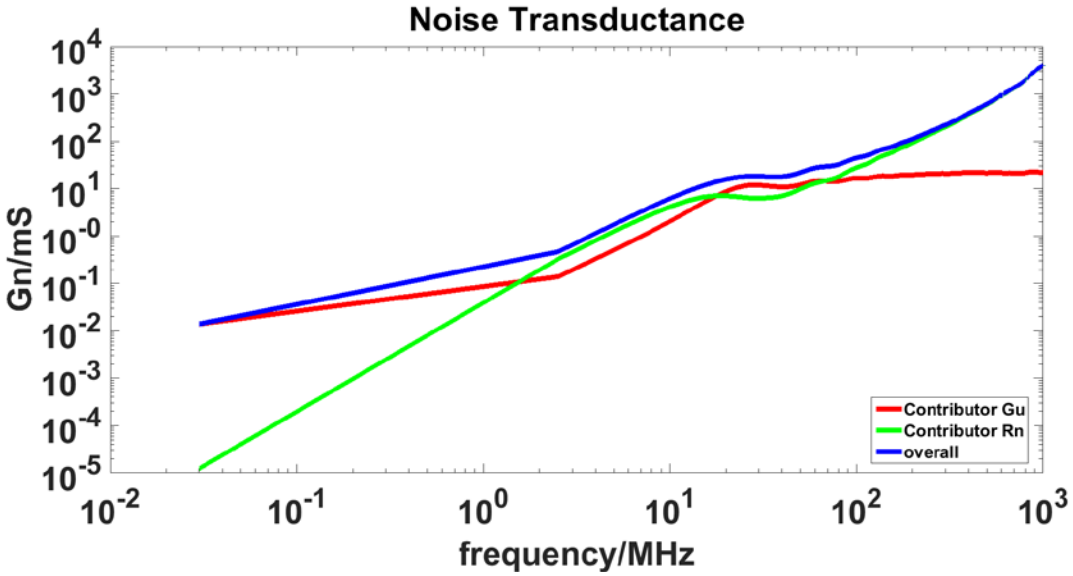


Figure 2-15 Noise contributors in G_n

From Fig. 2-15 we find:

1) Fig. 2-15 shows that G_n increases with frequency. To explained this, we can chop the cable into several identical segments, with each of them treated as lumped 2-port model at the specific frequency. For simplicity it is further assumed that in each segment noise only comes from the series

resistance, R. Then we can refer the noise voltage in each segment back to the input port via different hybrid parameters as shown in Fig. 2-14. However, when frequency increases those parameters exhibit higher attenuation. As a result, the input-referred noise generally becomes larger.

2) Among the two contributors of G_n shown in Fig. 2-15, it can be found that at low frequencies (DC-1MHz), the independent current noise, G_u, dominates the overall noise performance, and that at high frequencies (1MHz to 1GHz), the correlated voltage noise, R_n, plays an more important role. This behaviour can be also explained in a similar way as above. At low-frequencies, for a single noise voltage source in the aforementioned segment, the conversion ratio between the input-referred voltage and current differs obviously along the whole cable. However, at high-frequencies, the high attenuation of cable makes the aforementioned conversion ratio differs little among the segments at far end. And besides, the higher the frequency goes, the larger the number of those segments take up the cable. Allowing for this, the correlated noise originating from R_n starts to dominate the noise contribution over R_n. The insight can be verified by the calculated Y_{cor} shown in Fig. 2-16, where Y_{cor} shows increasing tendency as frequency goes up.

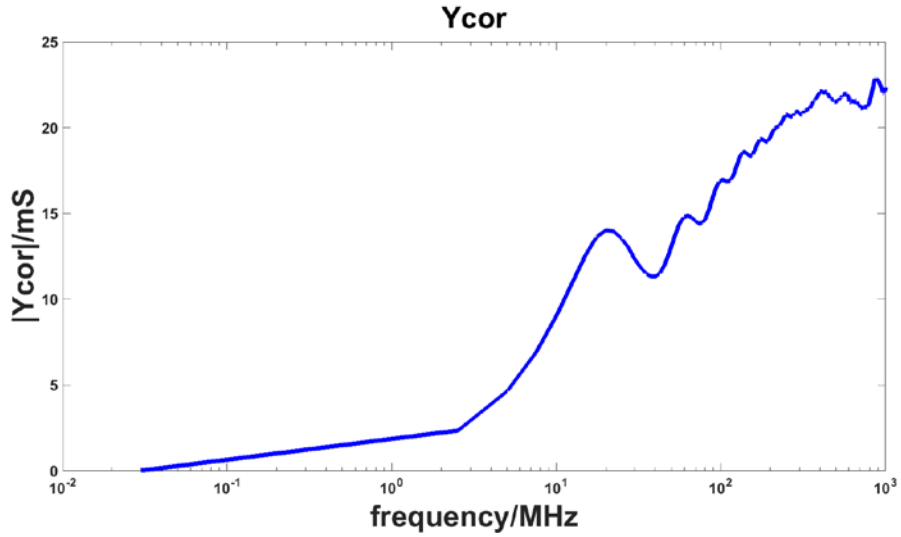


Figure 2-16 Correlation coefficient, Y_{cor}, obtained from VNA measurement

3) When frequency goes higher than 50MHz, the contribution of R_n continues to increase. This is due to the skin-effect of the cable, which leads the series resistance R (and the resulted loss) to grow with frequency.

In this section it is found that the distributed model of the micro-coaxial indeed brings out the problems when time-multiplexing is chosen as the multiplexing scheme. To tackle with those problems, equalization, for time domain non-idealities, and a dedicated SNR model, for the complicated noise performance, are proposed and discussed in detail in the following two chapters.

2.4 Summary

In this chapter we have first investigated several multiplexing schemes in order to investigate their feasibility in our application. After a comparison, time-multiplexing has been chosen for its implementation simplicity and the potential of low power consumption. After that, the spectral characteristics of time-multiplexing have been investigated, from which we conclude that the time-multiplexing actually expands the signal bandwidth and calls for accurate modelling of the behaviour of the cable at higher frequencies. Verified by the time domain simulations and an analysis of the cable's noise performance, the transmission line model has shown to be needed in the cable modelling and does present difficulties in the system level solution that will be addressed in the following chapters.

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Chapter 3 Equalization

As shown in Chapter 2, the loss of the transmission line will introduce crosstalk between signals from different drivers. In order to resolve signals clearly, the finite bandwidth of the channel should be repaired before de-multiplexing. This process is called equalization (EQ). In this chapter several common equalization schemes will be introduced. After comparison the conclusion will be drawn that ADC-based equalization is more suitable in our application. In the last part of this chapter the detailed algorithms of ADC-based equalization will be covered.

3.1 Basics of Equalization

3.1.1 Location of the Equalizer

There are two options for the location of an equalizer: TX or RX. In the case of TX EQ, the high-frequency components of the signal will be pre-emphasized before transmission. This approach potentially leads to SNR reduction, since the low-frequency components will be partly suppressed to allow emphasizing the high-frequency components within the swing limitation set by the power supply. Another disadvantage of TX EQ is that the EQ coefficient adjustment calls for an extra feedback loop from RX to TX, which is against the target of cable and power reduction in the project. Moreover, TX EQ increases complexity on the TX side, which is also not desirable.

In RX EQ, the non-ideal channel response is repaired on the RX side. Due to the more relaxed power and complexity requirements on the RX side, the EQ effort spent on this side is relatively more tolerable. Therefore, equalization at RX is chosen in the project.

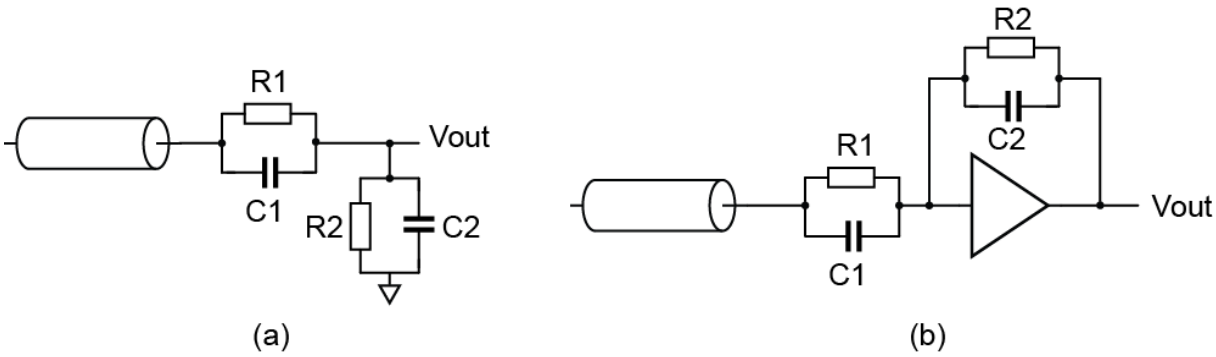
3.1.2 Continuous-Time and Discrete-Time Equalization

From a signal-processing point of view, channel equalization can be categorized as continuous-time EQ and discrete-time EQ. In continuous-time EQ, a passive or active network is connected to the cable in order to boost the overall channel bandwidth, as shown in Fig. 3-1. For a passive network, EQ is realized by attenuating the low-frequency components and retaining the high-frequency ones. Fig. 3-2 shows the simulated output signal for the case of current-mode transmission, with and without passive continuous-time EQ [3.1][3.2][3.3]. With EQ, the load current has a sharper falling edge compared with the characteristic impedance load. However, it can also be observed that the peak of the pulse response is degraded due to the low-frequency suppression. This can be understood with more ease in the frequency response, as is shown in Fig. 3-3.

As a consequence of that, the passive equalization scheme is more sensitive to the noise of the following stages since no gain is provided due to the nature of the passive network. This issue can be

addressed by active EQ [3.4][3.5], where not only the gain can be designed, but also the readout mode can be altered. These advantages come at the cost of additional power consumption of active devices.

Besides these differences between passive EQ and active EQ, a common disadvantage of continuous-time EQ lies in that only a limited number of poles and zeros can be flattened, complicating the implementation of a high-order equalizer .This implies that it is may not be sufficient to implement only continuous-time EQ in applications requiring high accuracy, such as this thesis project. In such applications, it may be combined with discrete-time EQ to yield better performance.



(a) passive EQ (b) active EQ

Figure 3-1 Continuous-time EQ

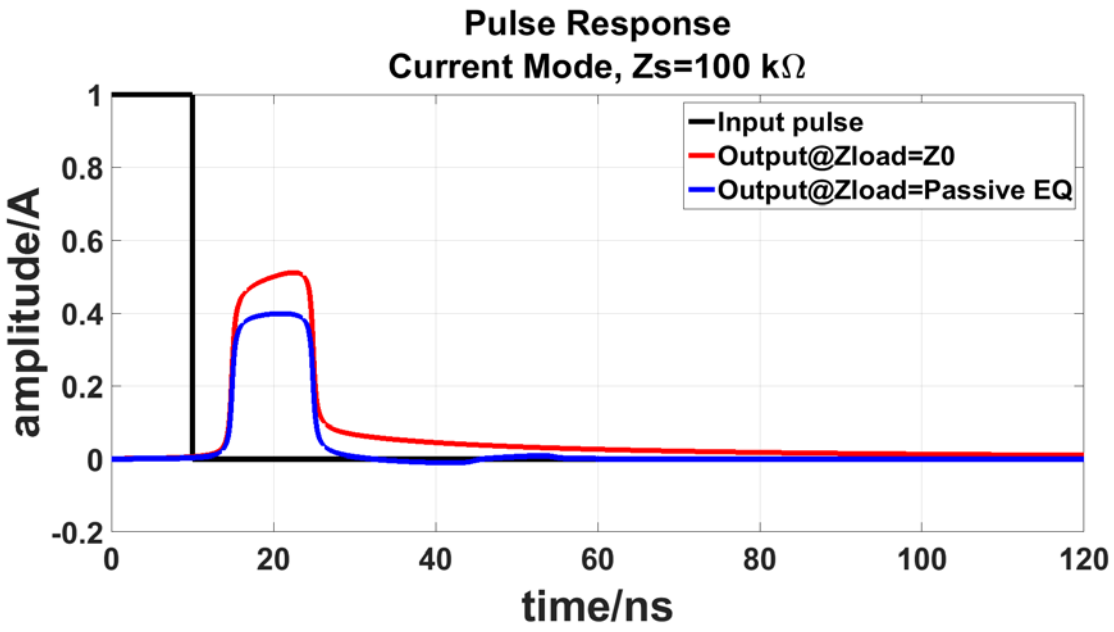


Figure 3-2 pulse response of current mode transmission[1]

[1] Figure can be obtained using the derivation described in [3.1]

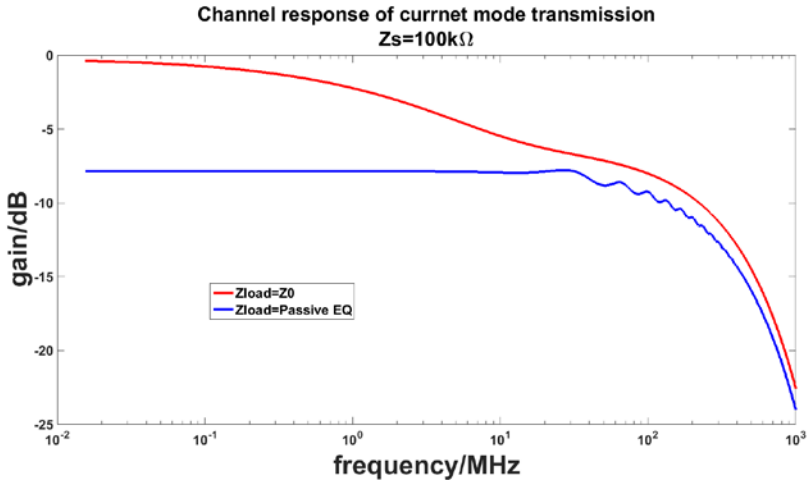


Figure 3-3 Frequency response of current mode transmission with different loads

Usually continuous-time EQ is installed as the first stage of a receiver, which relaxes the requirements on the following discrete-time EQ [3.5].

In a discrete-time EQ, the pulse response of the channel is sampled and then equalized in the discrete-time domain. By employing criteria to reduce the residual error between the equalized response and the ideal one, a set of equalization coefficients can be obtained. This can be either a finite impulse response (FIR) or an infinite impulse response (IIR) description of the EQ impulse response. After convolution of the channel output with this EQ impulse response, the input pulse can be reconstructed as one impulse with other elements approximately being zero, as shown in Fig. 3-4 [3.4].

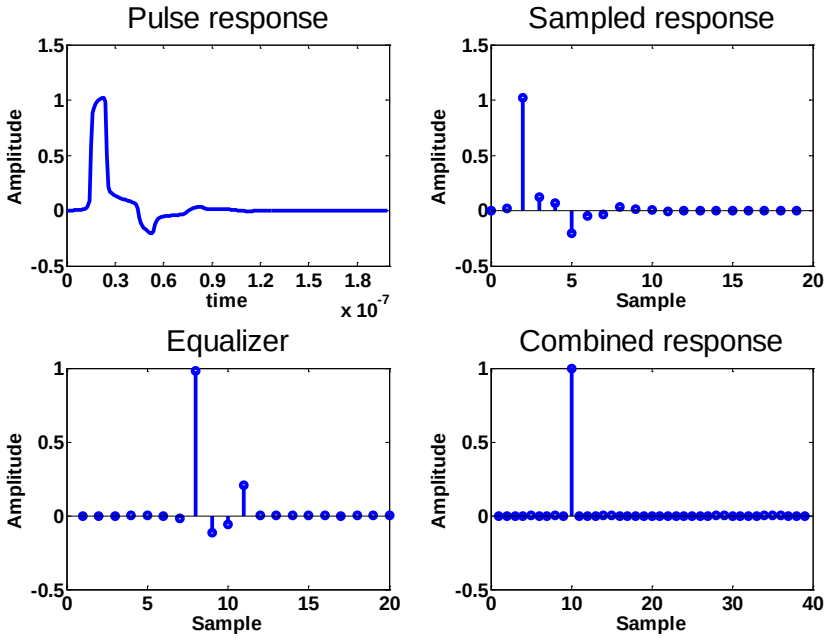


Figure 3-4 One example of discrete-time equalization

In the sampled response as shown in Fig. 3-4, there are usually a main impulse of which the amplitude is larger than that of other samples. Usually the main impulse is called main cursor, and the nonzero samples appearing before the main cursor are called precursors and those after the main cursor are called postcursors.

In high-speed digital links, FIR/IIR EQ is usually implemented in the analog domain, which makes the whole EQ loop compact and fast [3.6]. However, if higher precision with lower transmission speed is required in the application, more stress should be put on the accuracy than the speed, and such an analog-intensive way of equalization should be modified accordingly.

3.1.3 ADC-Based Equalization

Besides the EQs discussed above, one promising solution to our application is ADC-based EQ. As shown in Fig. 3-5, in such a scheme the output signal at RX is sampled and digitized first, and then it is sent to the digital signal processing (DSP) unit where EQ is done in the digital domain. Moreover, an ADC and DSP are typically already present in ultrasound systems, and equalization is expected to be a relatively simple task compared to the signal processing already taking place. Since the power and complexity at RX are less critical in our application, such a scheme is finally chosen and applied in the project.

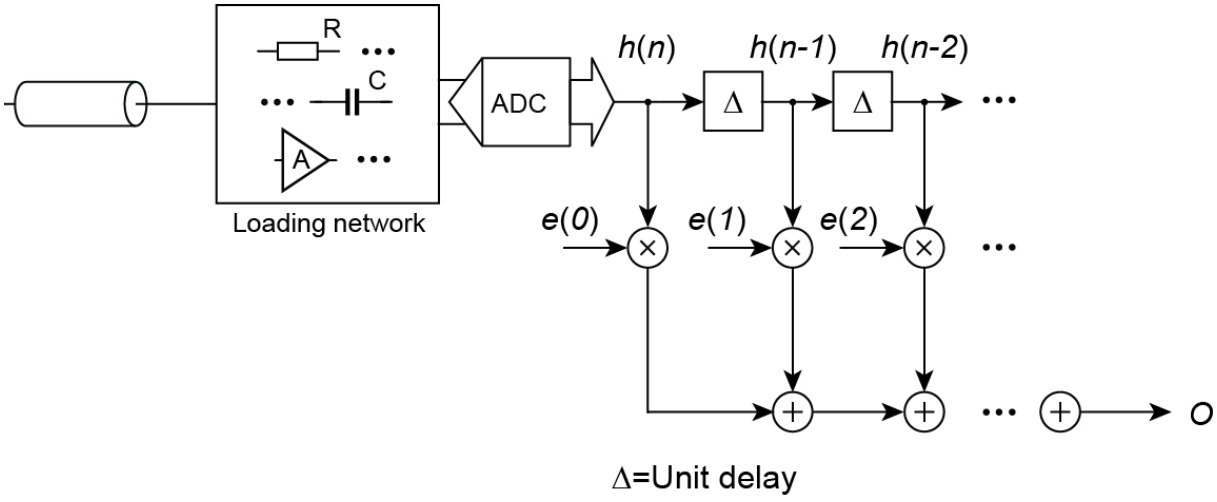


Figure 3-5 ADC-based equalization

Compared with the aforementioned analog-intensive implementations, another advantage of ADC-based EQ is that both the algorithm and the coefficients can be adjusted with more flexibly. This property will benefit the case where the channel response varies with the cable length, layout and wiring situation. However, due to the good shielding of the micro-coaxial cable used in our

application, the cable's electrical character is found to be quite stable with cable bending and twisting. Therefore, the one-time calculated EQ coefficients can be stored in hardware and used for a long time, which saves the effort of adjustment.

In this section, different aspects of equalization have been introduced, with the proposal of ADC-based EQ in our application. The details of the EQ algorithm will be discussed in the next section.

3.2 Equalization Algorithms

Based on the information of the channel response, an equalizer should be designed in order to cancel all the pre-/post cursors. Mathematically, the algorithm can be expressed as

$$E * H * C = C \tag{3-1}$$

where H is the pulse (not impulse!) response of the whole channel, E are the coefficients of the equalizer, and C denotes the input signal series. Here the symbol "$*$" represents convolution instead of simple dot multiplication. Since C stays on both sides of the equal sign, after simplification C can be removed and E, H can be combined as an overall operator applying on the input signal:

$$E * H = U \tag{3-2}$$

where U is the sampled pulse response of an ideal channel, which contains one impulse and other samples being zero. This implies that E should be the inverse of H. However, due to the finite storage space, the recorded H is of finite length. In consequence, an error between the combined response and the ideal one has to be tolerated. Based on the understanding of this error, two main algorithms for finding E, zero-forcing (ZF) and minimum-mean-square-error (MMSE) are studied and employed in the project [3.7].

3.2.1 Zero-Forcing Equalization (ZFE)

In zero-forcing equalization, the channel response is assumed to be accessible and noise-free. Based on this assumption, ZFE is designed to suppress residual pre-/postcursors after equalization to the largest extent. Mathematically, a quantity to measure the effect of the residual cursors is defined as peak distortion (PD) [3.7], which is the ratio between the summations of all the remaining pre-/postcursors and the main cursor,

$$PD(O) = \frac{\sum_{k=1,k\neq k_0}^{N+L-1} |O(k)|}{|O(k_0)|} \tag{3-3}$$

where O is the combined response of the finite-length E and H,

$$O = E * H \tag{3-4}$$

and k_0 is the location of the main cursor. L is the length of H and N is the length of E.

However, there is no guarantee that $PD(O)$ can always be minimized. In the special case that the PD of the pulse response itself is less than unity, there will be solution towards goal of the PD minimization [3.7]. This statement can be expressed as

$$PD(H) = \frac{\sum_{k=1,k\neq k_1}^{L} |h(k)|}{|h(k_1)|} < 1 \tag{3-5}$$

where $h(k)$ is the element of H and $h(k_1)$ is the main cursor. Then the E towards the minimum $PD(O)$ can be calculated by solving the following matrix equation[2]:

$$H_{ZFE} \cdot E = U ==> E = {H_{N\times N}}^{-1} \cdot U \tag{3-6}$$

where H_{ZFE} a matrix composed of sampled pulse responses with different time delays,

$$H_{ZFE} = \left[H_{k_1}, H_{k_1-1}, H_{k_1-2}, .., H_{k_1-N+1}\right] \tag{3-7}$$

where H_k is denoted by

$$H_k = [h(k), h(k+1), h(k+2), .., h(k+N-1)]^T \tag{3-8}$$

If some elements in H_k are not recorded in the implementation, they should be replaced by zero. U is the desired ideal response, which means there should be only one impulse in it.

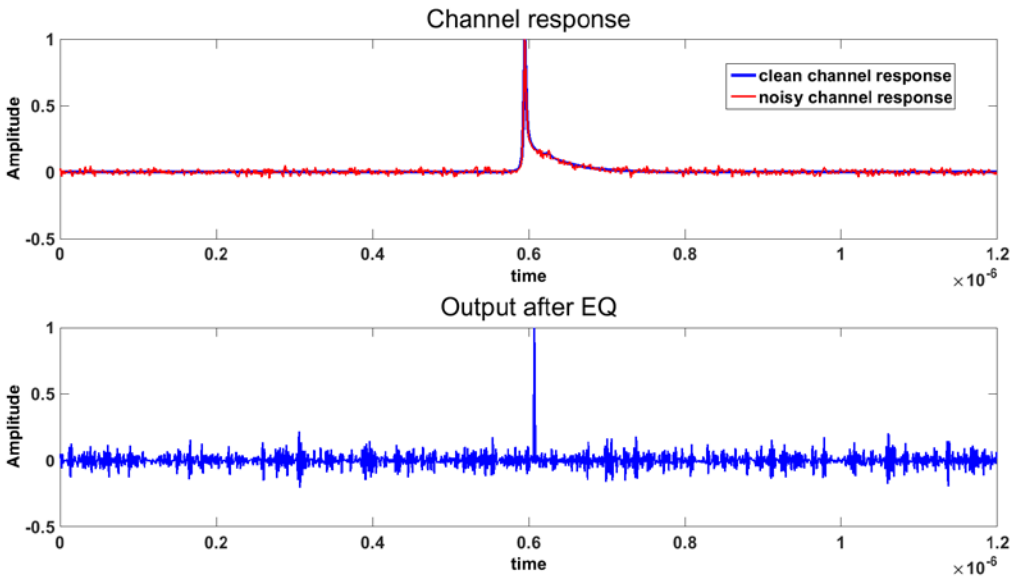
$$U = [0,0,0, \dots ,0,0,1,0,0, \dots ,0,0,0]^T \tag{3-9}$$

Even though ZFE can effectively flatten the channel response, there are some drawbacks of this algorithm. First, the assumption of a noise-free channel response is not justified. In order to capture the channel response cleanly, the noisy channel response should be sampled repeatedly and averaged. In some time-varying or always-on channels where averaging is not possible, such an algorithm exhibits limited functionality in equalization. In our application, the signal is transmitted and processed in real time, and therefore on-line averaging may not be preferred.

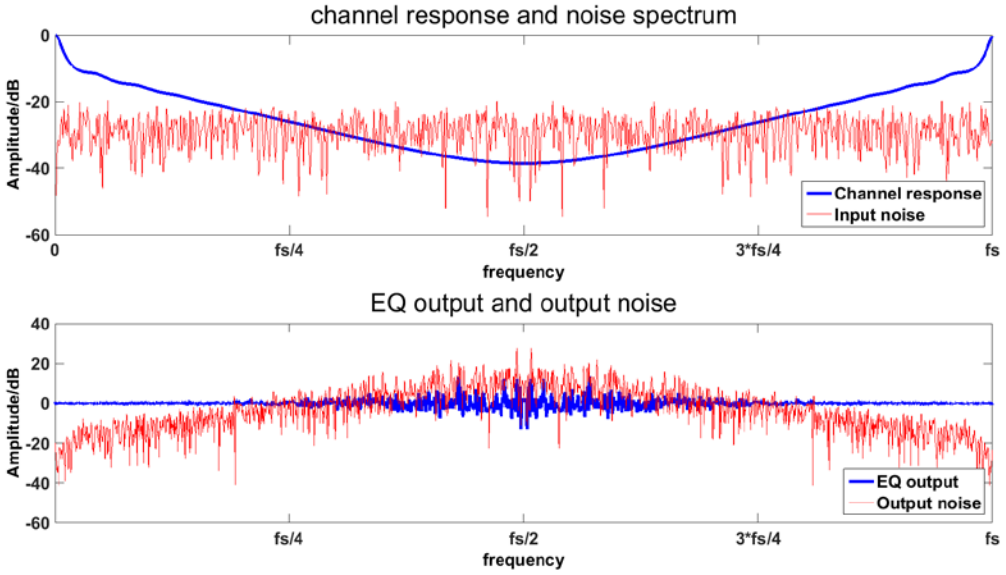
Another drawback is that noise is enhanced. Since ZFE is aimed at completely flattening the low-pass channel response, any high-frequency noise added before the equalizer will be boosted due to the

[2] From Expression (3-6) we may find the first and the last several terms of *O* might be still nonzero and cause the crosstalk to the signal from other AFEs. But as has been proved [3.7], by using such a set of coefficients as a N-element equalizer, $PD(O)$ is minimized.

inverse response of the equalization. To verify this, a simulation has been carried out, in which the cable is modelled with a severer skin effect than that in our application, a pulse current is fed into the cable and read out from a 100 Ω load resistor. White Gaussian noise is plugged into the channel response to emulate the added noise through signal transmission. In Fig. 3.6 the channel response and the ZFE output are shown, where the equalizer's length is chosen to be long enough to avoid the noticeable truncation error due to the FIR limitation. In equalization a low-noise channel response is obtained by averaging several noisy responses. By comparison of the noise level in both time domain (Fig. 3.6 (a)) and frequency domain (Fig. 3.6 (b)), it can be found that the high-frequency noise is actually boosted. On the other hand, in Fig. 3.6 (a) it can be also found the long tail in the channel response is effectively cut out during ZFE, with a single pulse at the equalizer's output. Together with the frequency domain result shown in Fig. 3.6 (b), it verifies the property of complete channel flattening in ZFE.



(a) Noise enhancement of ZFE in time domain



(b) Noise enhancement of ZFE in frequency domain

Figure 3-6 Noise enhancement of ZFE

In ADC-based equalization, quantization noise is one of the noise sources that is enhanced. So in order to achieve the target resolution after equalization, the resolution of the ADC should be carefully considered. This will be discussed in the next chapter.

In order to avoided the drawbacks of ZF equalization, another equalization called minimum-mean-squared-error (MMSE) equalization can be employed.

3.2.2 MMSE Equalization

In MMSE equalization, the channel is equalized in the presence of noise in the channel response[3.7]. The optimization criteria of MMSE EQ is to get the best trade-off between the preventing noise enhancement and reducing pre-/postcursors after equalization. Suppose H' is the sampled channel pulse response with additive noise, n, then we have

$$H' = H + n \tag{3-10}$$

After equalization and comparison with the ideal combined response, U, there will be an error that consists of both residual pre-/postcursors and noise, which is

$$err = H' * E - U = (H * E - U) + n * E \tag{3-11}$$

Reducing the term in brackets is the optimization goal for ZFE. For MMSE, the optimization goal is minimizing (3-11) as a whole,

$$||err||^2 = \overline{\sum_{k=1}^{N+L-1} |err(k)|^2} \qquad (3-12)$$

where N, L are the same as defined in ZFE. Operator "$\bar{}$" means taking average of the several batches of errs. Minimization of $||err||^2$ can be achieved by setting the partial derivative with respect to $e(k)$ to zero,

$$\frac{\partial ||err||^2}{\partial e(k)} = 0, k = 1,2, \dots, N \qquad (3-13)$$

where $e(k)$ are the coefficients of the equalizer:

$$E = \begin{bmatrix} e(1) \\ e(2) \\ \vdots \\ e(N) \end{bmatrix}, \qquad (3-14)$$

The solution of E can be expressed in the matrix form, which is

$$E_{MMSE} = \overline{(H_{MMSE}{}^T \cdot H_{MMSE})^{-1}} \cdot \overline{H_{MMSE}{}^T U} \qquad (3-15)$$

of which H_{MMSE} is the matrix composed of sampled pulse response with different time delays,

$$H_{MMSE} = \left[H'_{l_0}, H'_{l_0-1}, H'_{l_0-2}, \dots, H'_{l_0-N+1}\right] \qquad (3-16)$$

where l_0 is the starting position of H' used in MMSE. H'_k is denoted by

$$H'_k = [h(k), h(k+1), h(k+2), .., h(k+N+L-2)]^T + [n(k), n(k+1), n(k+2), .., n(k+N+L-2)]^T \qquad (3-17)$$

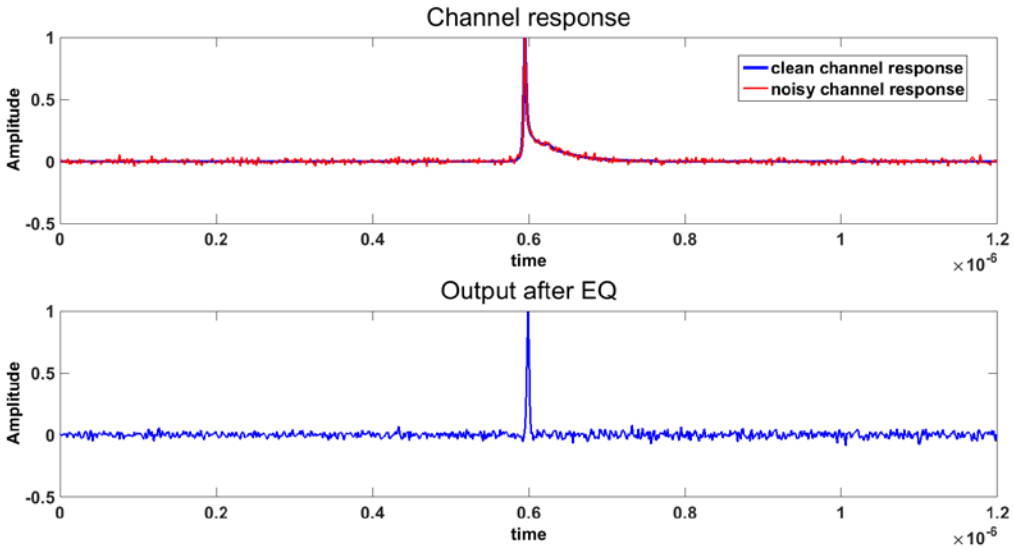
Then the error can be expressed as

$$||err_{MMSE}||^2 = \overline{(H_{MMSE} \cdot E_{MMSE} - U)^T \cdot (H_{MMSE} \cdot E_{MMSE} - U)} \qquad (3-18)$$

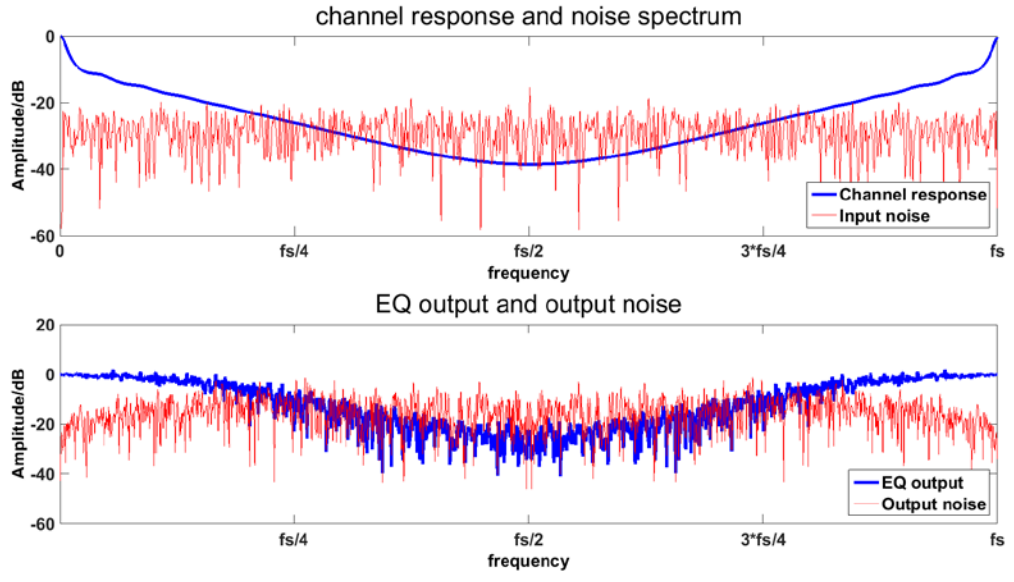
Compared with ZFE, MMSE equalization takes the overall error with noise as the optimization goal, and thus the noise enhancement effect becomes less obvious compared with ZFE, but at a cost of less complete channel equalization. To verify this, a simulation with the same configuration as that in ZFE has been run. The results in both time and frequency domain are plotted in Fig. 3.7. In comparison with the ZFE results shown in Fig. 3.6, the noise is less heavily levelled up in MMSE. However, the pulse is partially recovered, with several remaining pre-/postcursors compared with the result in ZFE,

as the penalty explained above. These effects can also be observed in the frequency domain shown in Fig. 3.7(b), where the EQ output spectrum (blue curve) is still of the low-pass form and the output noise spectrum is less enhanced.

In comparison with ZFE, it can be found that averaging is also carried out for obtaining the mean-square error. So from the point of view of real-time operation point of view, both algorithms are equally feasible.



(a) MMSE equalization in Time domain



(b) MMSE equalization in frequency domain

Figure 3-7 MMSE equalization

The aforementioned property of partial channel recovery in MMSE makes it suitable for highly noisy applications. However, if the SNR at the input of equalizer is high enough, the difference between ZFE and MMSE is small since in both cases the main effort will be paid on reducing the residual pre-/postcursors other than noise [3.8]. In this project, both algorithms have been implemented for comparison.

So far, the basics of equalization have been introduced. The application details in our project, such as the dependency of the equalizer's length on the loading condition and cable length, and the optimization of the equalizer's length, are explained in detail in Chapter 4. Besides that, in order to apply the algorithms to the time-multiplexing system, the difference between drivers should be taken into account, which turns the system, that has so far been assumed to be a single-input-single-output system, into a multiple-input-multiple-output (MIMO) system [3.9][3.10]. In consequence, one set of equalizer coefficients can only correspond to one driver. An equalization algorithm for the MIMO system is elaborated in Appendix B.

3.3 Summary

In this chapter, channel equalization has been introduced. By comparing with common equalization algorithms used in digital links, we propose an ADC-based scheme which is well matched to the requirements of our ultrasound system. Several equalization algorithms have been discussed, with an emphasis of pros and cons in our application.

3.4 References

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Chapter 4 System Design and Optimization

In this chapter the system design and optimization is carried out. The discussion starts from the determination of the signal transmission mode, which affects the design of the on-chip TX circuit. Next, the topology of the bulling blocks on the RX side, including a trans-impedance amplifier (TIA), extra gain stage and ADC, are introduced. Next the system-level modelling and optimization are made in order to provide accurate specifications for these building blocks. Finally, a summary of the whole system is given, as a starting point for circuit design and PCB design in the following chapters.

4.1 Topology Selection of Driver

4.1.2 Current Mode or Voltage Mode

For the driver, in the circuit topology point of view, there are two alternatives, current mode and voltage mode regardless the termination conditions [4.1]. Due to transmission line effect, the input impedance as shown in Fig. 4-1 is [4.2]

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} \qquad (4-1)$$

where Z_L is the load impedance at the output port of the cable. Other parameters in expression (4-1) have been described in Chapter 2.

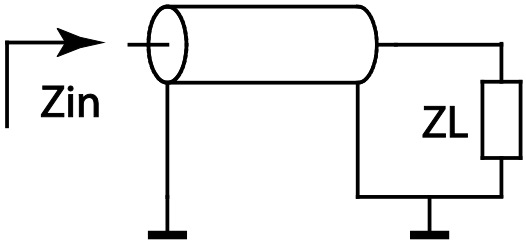


Figure 4-1 Input impedance seen from the output of a driver

From the input impedance vs. load impedance plot shown Fig. 4-2, Z_{in} is below 100 Ω in the frequency range of interest with different loads ranging from 0.1 Ω to 10 kΩ. This is because the loss in the cable screens the load and only the impedance close to Z_0 can be seen at the input port. Such a low Z_{in} gives us the preference to using current-mode transmission, since a high Z_L does not help to build a high Z_{in} in order to utilize the advantage of light loading in voltage-mode transmission. A detailed analysis on the driving power in Appendix C shows that if the transconductance of a current-

mode driver, G_m, can be less than 10 mS to fulfil other specifications, then current-mode transmission will be more power efficient than its counterpart.

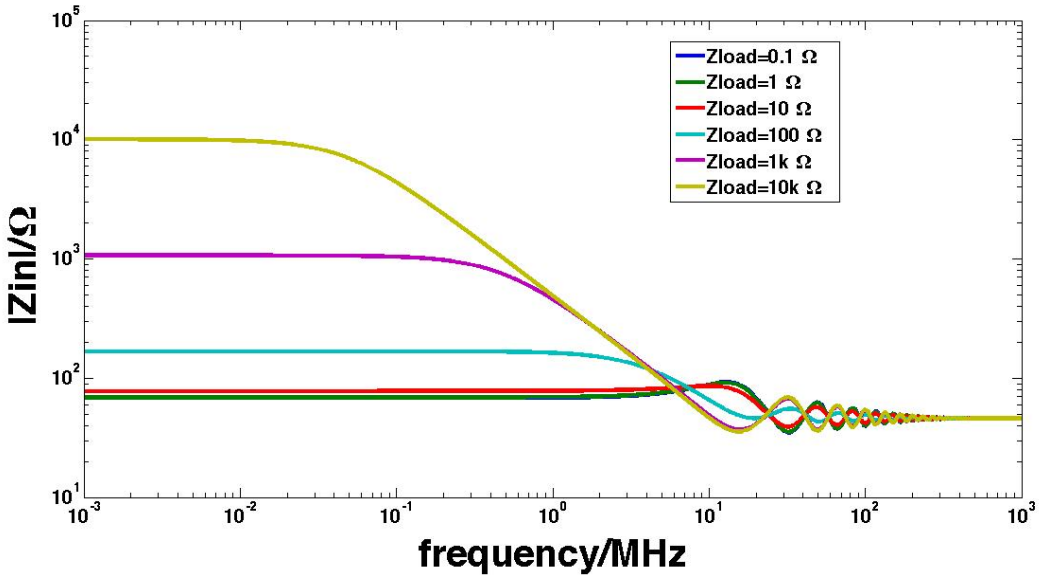


Figure 4-2 Input impedance versus frequency

Another advantage of current-mode transmission is the good crosstalk immunity. Analysis shows that a current-mode transmission is better at reducing crosstalk between drives with a common ground. For details please refer to [4.1].

In conclusion, a current-mode driver is preferred when driving a low-impedance cable in a low-power design. In the project a transconductor-based driver is proposed.

4.1.3 Single-Ended or Differential

A transconductor can be designed in either single-ended or differential form. Two simple common-source transconductors in the single-ended and the differential implementations are used for comparison, as shown in Fig. 4-3. The final decision will be made based on the power-limiting factors in the design, which are usually noise and speed.

From noise point of view, the differential transconductor in Fig. 4-3 (b) introduces doubled input-referred noise from the two loading cables compared with the single-ended version shown in Fig. 4-3 (a). In order to fight against the excess noise the output current of a differential transconductor should be multiplied by $\sqrt{2}$ to maintain the same SNR (suppose the transconductor is noise-free). Allowing for the fixed cable count in the project, the number of differential transconductors should be half of

that in the single-ended condition. If the input swing for both cases is identical, we can conclude that the total power in the differential driving system to be higher than that consumed in its single-ended counterpart.

Furthermore, from speed point of view, extra penalty comes with the fact that a differential transconductor has to run doubly faster than a single-ended one in order to keep the same throughput. Accordingly the power would be higher compared to the single-ended situation.

Besides the comparison focus on the power consumption, there is additional benefit by adopting the single-ended scheme, which is the convenience of accommodating with the singe-ended preceding stage, and the succeeding micro-coaxial cable. Therefore, a single-ended transconductor is chosen in the project. For the poor power-supply-rejection-ratio (PSRR) associated with the single-ended implementation, it will be discussed in Chapter 5.

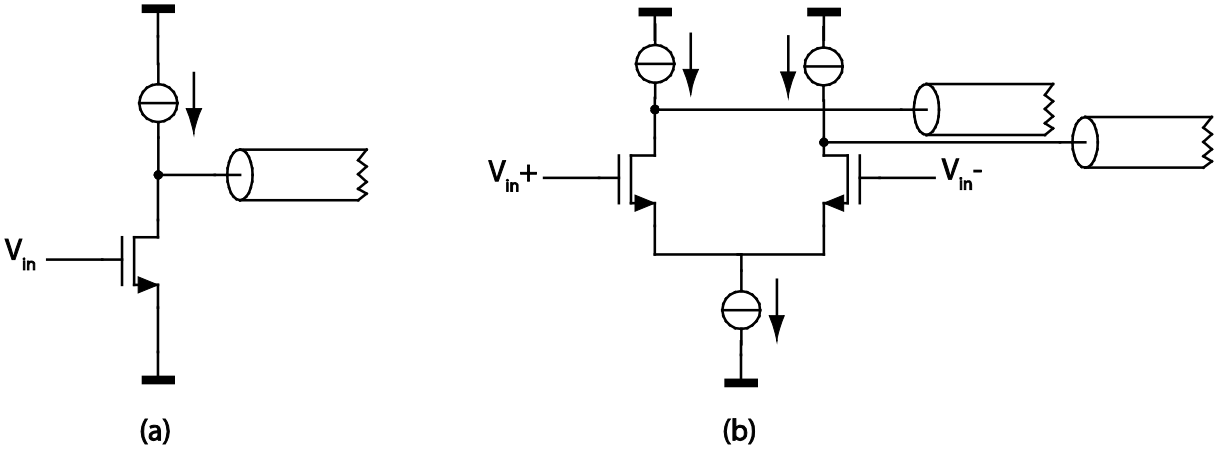


Figure 4-3 Single-ended and differential current-mode transconductors

4.2 Topology Selection of RX

Current-Mode Receiver

To match with the current-mode TX, on RX side a corresponding current-mode readout circuit should be designed. For this purpose, a trans-impedance amplifier (TIA) shown in Fig. 4-4 can be leveraged, which is commonly used in fiber-optic communication where current mode readout is also required [4.3]. The advantage of TIA is that it can accomplish current-voltage conversion and maintain a low input-referred noise current at the same time.

However, compared with the simple resistive termination followed by a fixed-gain amplifier, the topology of TIA indicates relatively higher power consumption. This is because that in the frequency of interest, the amplifier used in TIA must provide higher bandwidth to achieve sufficiently low input

impedance. But, since the power on RX side is not critical in the project, such a power penalty is tolerable as long as a commercial amplifier with sufficient gain-bandwidth (GBW) can be found.

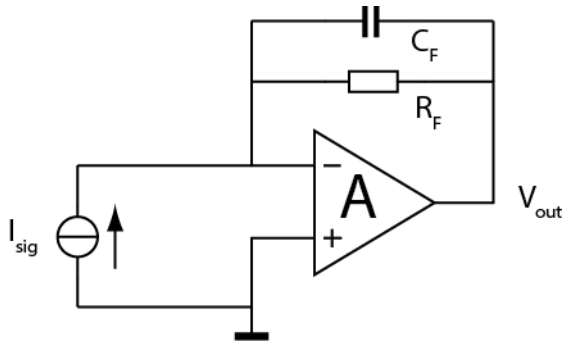


Figure 4-4 TIA as the first stage on RX side

For a TIA design, a common issue is the potential instability caused by the input parasitic capacitance. As shown in [4.4][4.5], the large capacitance at the input of TIA can cause the feedback factor to drop while the amplifier's frequency response is also rolling-off. The pole in the feedback makes the whole feedback loop a two-pole system, then instability might appear. To solve this problem a feedback capacitor C_F can be placed in parallel with the feedback resistance R_F, as shown in Fig. 4-4, to limit the first-order rolling-up of the feedback factor [4.4][4.5]. One extra benefit by introducing C_F is that the noise from both the input and feedback resistance can be further low-pass filtered. As for the penalty, the signal bandwidth might be also cut down due to the low-pass character.

Extra Gain Stage

In order to get the enough output swing to adapt with the input range of RX ADC, one extra gain stage is inserted between a TIA and an ADC to save the effort paid by the TIA. In this unit a possible continuous-time-linear-equalizer (CTLE) can be used to boost the signal bandwidth [4.6].

ADC

As discussed in Chapter 2, the actual sampling frequency for the multiplexed signal is 100 MHz, which is should be the minimum ADC sampling frequency. Since the overall SNR should be higher 40dB, the resolution of chosen ADC should be higher than 7-bit. Later we will see the noise enhancement effect due to equalization, which indicates that an ADC with higher than 8-bit resolution is more reasonable.

4.3 System Modelling and Optimization

4.3.1 Noise Analysis

As explained in Chapter 2, there are two noise parameters associated with the two-port cable. Since the driver on TX side is to be designed in current mode, it is necessary to combine the two noise sources into one in the current domain. Suppose the termination impedance on the TX side is denoted Z_{TX} as labelled in Fig. 4-5. Then the input-referred current noise can be written as [4.7]:

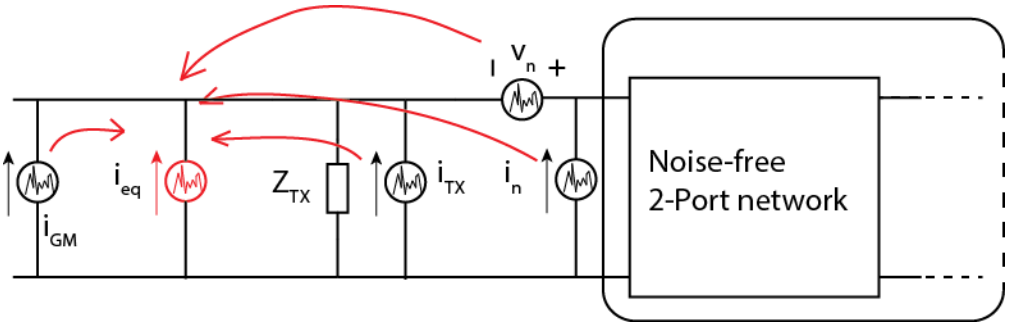


Figure 4-5 Calculation of the equivalent noise current from a 2-port network

$$S(i_{eq}) = S(i_{Gm}) + 4kT \cdot \left(Re[\frac{1}{Z_{TX}}] + R_n \cdot \left| Y_{cor} + \frac{1}{Z_{TX}} \right|^2 + G_u \right) \qquad (4-2)$$

where the first term, i_{Gm}, represents the noise current from transconductor's output signal. The second term denotes the noise from the TX termination impedance Z_{TX}, and the noise of the cable with load. Operator "$Re[]$" means to obtain the real part of the variable in the bracket, which is to calculate the conductance of Z_{TX} in our case. R_n and G_u are the uncorrelated noise equivalent resistance and conductance of the cable respectively, as explained in Chapter 2. Y_{cor} is the correlation admittance between v_n and i_n. Expression $(4-2)$ indicates that a high Z_{TX} helps to both suppress the noise from the cable and lower the current noise generated by itself. Such a condition is natural to be achieved by implementing a transconductor without explicit termination[5]. Then the second term in $(4-2)$ can be further approximated as

$$S(i_{TL+Load}) \approx 4kT \cdot (R_n \cdot |Y_{cor}|^2 + G_u) = 4kT * G_n \qquad (4-3)$$

where G_n is the total noise equivalent transconductance from the cable,

$$G_n = R_n \cdot |Y_{cor}|^2 + G_u \qquad (4-4)$$

[5] Actually in the microwave circuit design, noise from R_n can be further minimized by designing Z_{TX} to be $-1/Y_{cor}$. However, since the real part of Y_{cor} from a lossy device is positive, Z_{TX} should be designed as negative resistance in order to achieve the lowest noise, which might cause instability and design complexity. Therefore in the project the final strategy for a low-noise design is to make Z_{TX} as high as possible.

To improve noise performance, equation $(4-2)$ and $(4-3)$ give us a hint that efforts should be paid on lowering both G_n and i_{Gm}. Among them G_n is contributed by the noise from the cable and the load, Z_L.By using the input-referring scheme shown in Fig. 4-6, a description of the frequency-dependent G_n associated with different resistive loads is given in Fig. 4-7. From it we find that in the frequency range of interest, G_n is almost independent of Z_L when the latter is chosen to be higher than 1 kΩ. This gives us a guideline of choosing R_F in the TIA, that it should be higher than 1 kΩ if the noise from RX is not intended to dominate the overall noise.

As for the noise consideration from the transconductor, i_{Gm}, it will be discussed in the following subsection.

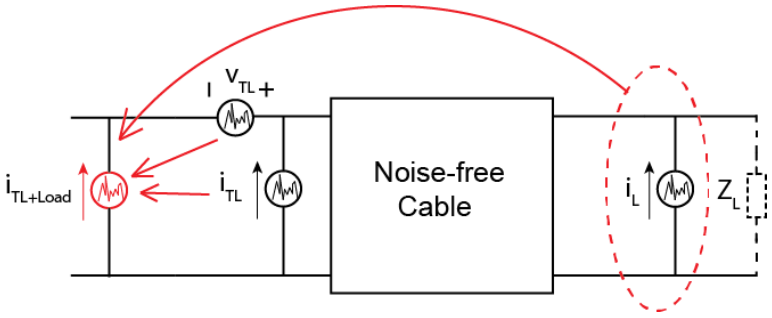


Figure 4-6 Calculation of the equivalent noise current of a 2-port network with load

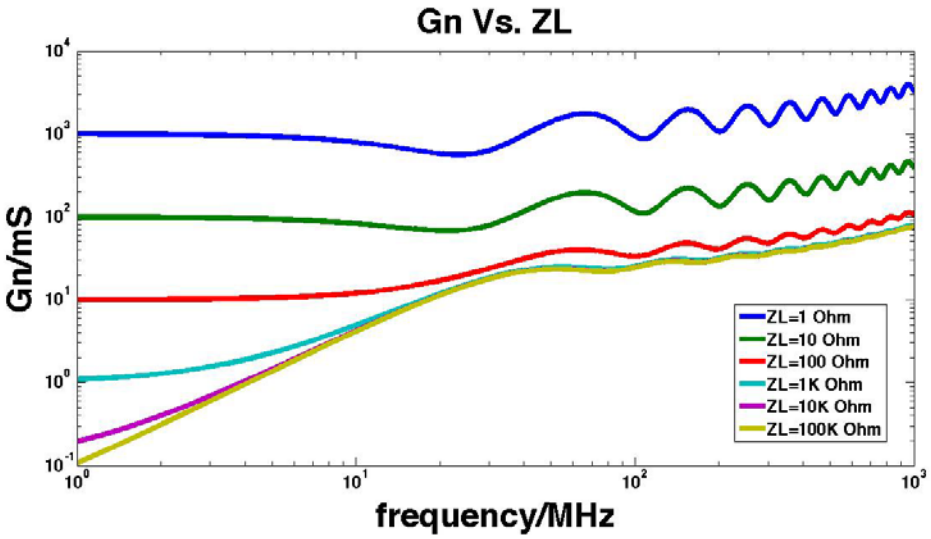


Figure 4-7 Equivalent noise transconductance G_n for different resistive Z_L's

4.3.2 Determination of Transconductance

The transconductance required by the TX transconductor is determined by the SNR specification. To get a rough estimate of it, we can make a simple calculation with some assumptions made beforehand:

The overall transfer function (from a transconductor to RX output) exhibits a first-order low-pass character with a cut-off frequency around 50MHz, which is the bandwidth of the multiplexed signals.

Signal current from the transconductor is assumed to be noise-free, namely a zero i_{Gm} in expression (4-2). Later in this subsection the validation of this assumption will be shown.

Output impedance of the transconductor and R_F of TIA are chosen properly so that only the cable's noise is dominant.

For calculation convenience, the transconductor's output current waveform is approximated as sinusoidal instead of sampled-and-held.

With these assumptions, then the equivalent input-referred noise current is

$$\overline{i_{eq}} = \sqrt{4kT \cdot G_n \cdot NBW} = 0.18\ \mu A \qquad (4-5)$$

where NBW is equivalent noise bandwidth, which, in a first-order system, equals $\pi/2f_c$, where f_c is the cut-off frequency. G_n is chosen to be a constant of 24 mS within the signal band, which is the value calculated at 50 MHz with the load resistance larger than 1 kΩ, as shown in Fig. 4-7.

Since the SNR requirement is 40 dB, the amplitude of the signal current from the transoncudotr should be

$$i_{Gm,out} = \sqrt{2} \cdot 10^{\frac{40}{20}} \cdot i_{eq} = 25.4\ \mu A \qquad (4-6)$$

As mentioned in Chpater 1, the input voltage amplitude of the transconductor is 100 mV. Then the transconductance G_m should be

$$G_m = \frac{i_{TX,out}}{v_{signal}} = 0.25\ mS \qquad (4-7)$$

By comparing G_m and G_n we find that the required G_m is much smaller than G_n. Normally the noise current PSD from the transconductor is several times of $4kTG_m$. From the huge difference between G_m and G_n it can be found that the noise of the whole system is mainly dominated by the cable other than the transconductor. This insight verifies the assumption made before, which also leaves us the convenience of transconductor design.

However, there are deficiencies in such a rough calculation. As shown in Fig. 4-7, $G_n$is not as flat-band as thermal noise, and the overall transfer function does not exactly exhibit first order roll-off character due to the transmission line effect. Therefore, in order to determine a more accurate G_m to meet the SNR specification, a fine SNR model is built in the following section.

4.3.3 Fine Model for SNR Calculation

In the fine model of SNR calculation, all the devices in the signal chain are included, which consists of a transconductor, a cable, a TIA, one extra gain stage, an ADC and one equalizer, which are depicted in Fig. 4-8. Tab. 4-1 gives a list of the configuration details of the building blocks. In the model the noise from the transconductor is composed of excess noise besides G_m[2] and termination impedance. In the cable two independent noise parameters, R_n and G_u, are included. In the TIA noise from the feedback resistance is considered, with the amplifier noise ignored for the device dependency. Similarly, noise in the extra gain stage is ignored in the model. In ADC the quantization noise is taken into account. Last but not least, zero-forcing equalization is used as the equalization algorithm.

SNR calculation is carried out by sweeping the resistive Z_{TX} and resistive input impedance of TIA, $Z_{in,TIA}$. Calculation results on Matlab are plotted in Fig. 4-9(a) and (b), which show the SNR's before A-D conversion and that after equalization, respectively.

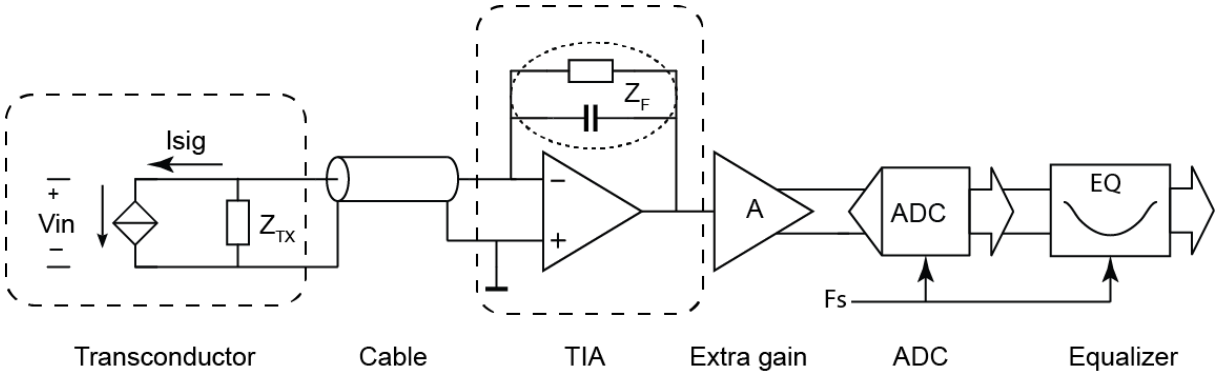
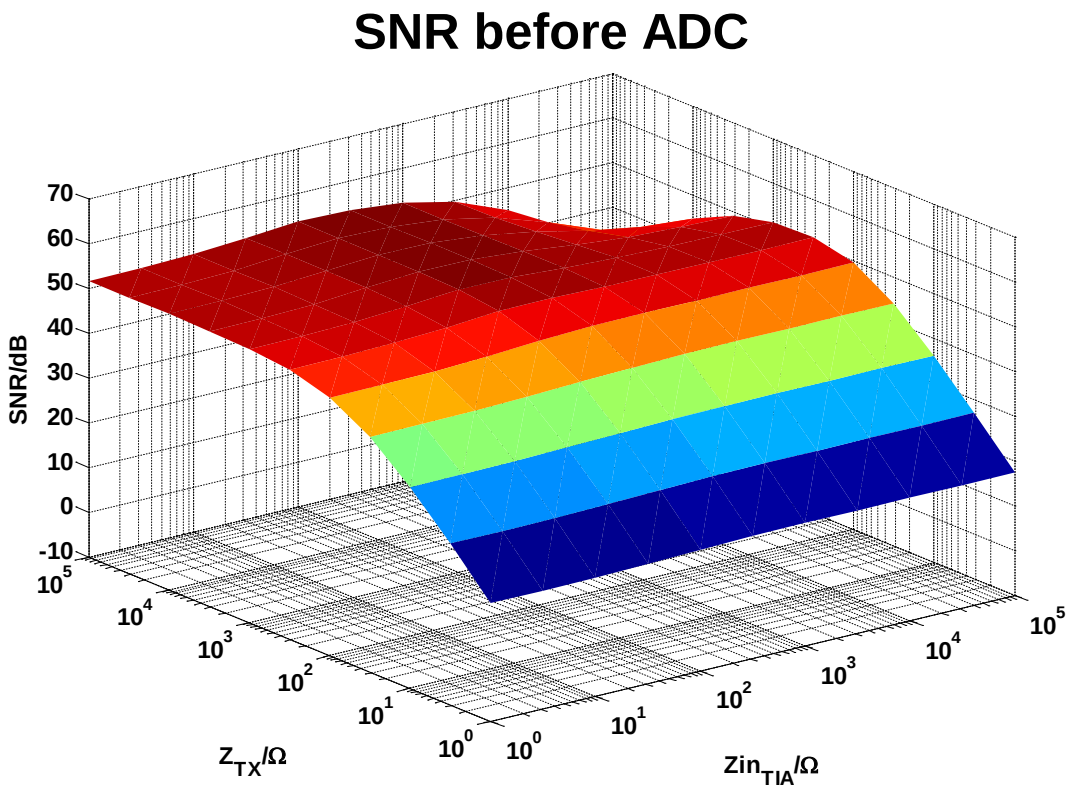


Figure 4-8 Signal chain used in the fine SNR model

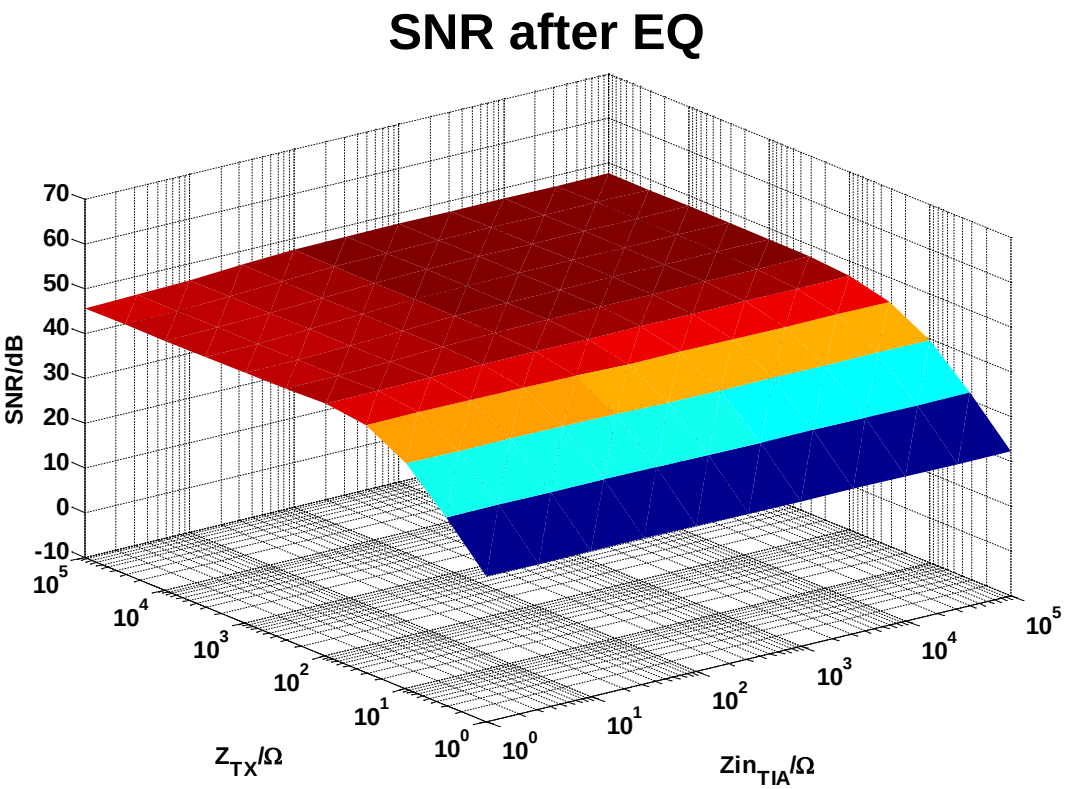
Table 4-1 Configuration details

Configuration details	Description
G_m	1mS for SNR consideration
Amplifier in TIA	Capable to provide its output swing to be the same as the system's input.
$Z_F$in TIA	R-C in parallel to maintain the stability and to filter the out-of-band noise
Extra gain stage	To amplify the output of TIA to accommodate with commercial ADC input range.
ADC	8-bit, 100Ms/S Nyquist ADC for SNR and cost consideration.

[2] Excess noise factor has been defined in the project as the ratio between the equivalent noise transconductance and the driving transconductance, for the purpose of estimating the excess noise in a transconductor.



(a) SNR before A-D conversion



(b) SNR after equalization

Figure 4-9 SNR versus different Z_{TX}'s and $Z_{in,TIA}$'s

Fig 4.9(a) shows that the SNR before A-D conversion exhibits tendency as discussed in the previous section. Some key observations are made below:

- At the region with low Z_{TX}, noise from TX termination impedance degrades the SNR as shown in expression (4-2), which indicates that the impedance matching at TX side is not preferred in the SNR perspective.

- When Z_{TX} is chosen to be higher than 100 Ω, SNR reaches a plateau as $Z_{in,TIA}$ goes below 100 Ω. That is because that in this configuration the overall transfer function is extended to be flat in the signal bandwidth. Since the signal is well seated in this flat band, it makes little difference between choosing $Z_{in,TIA}$ to be 1 Ω and 100 Ω.

- A SNR drop appears when both Z_{TX} and $Z_{in,TIA}$ are chosen to be high. This is because the high Z_L causes the charge injected in the current mode transmission to wander along the cable for a long time before neutralization, which makes the system bandwidth narrow. Then the signal level is degraded while the low-frequency noise current can still creep into the TIA, which causes incorrect emphasis on noise other than signal. These two factors together cause SNR to drop.

Fig. 4-9(b) shows the SNR after equalization. Similarly some facts can be found also as follows,

- There is no obvious SNR profile change before and after equalization as long as Z_{TX} is chosen to be high and $Z_{in,TIA}$ to be low.

- The SNR drop at "high Z_{TX}, high $Z_{in,TIA}$" region is found to be almost recovered after equalization. That is because the loss of in-band signals and the improper emphasis of the low-frequency noise are repaired by equalization. Therefore the dominant noise from the cable would not change with the different RX terminations, which makes the SNR independent of $Z_{in,TIA}$.

- The overall SNR drops after ADC and equalization. That is partly because of the quantization noise of ADC, and partly due to the noise enhancement effect associated with a zero-forcing equalizer, which has been explained in detail in Chapter 3.

By far combining the results in section 4.3.2 and 4.3.3, we can conclude that from the target SNR point of view, the "comfort zone" for Z_S, Z_F, $Z_{in,TIA}$ should be

$$\begin{cases} Z_{TX} \geq 100\ \Omega \\ Z_F \geq 1\ k\Omega \\ Z_{in,TIA} \leq 100\ \Omega \end{cases} \qquad (4-8)$$

In the next section a further analysis in the perspective of equalization is carried out, in the hope of narrowing the constraint shown in the above expression.

4.3.4 Equalizer Length Estimation

As mentioned in Chapter 2 and 3, the improper selection of Z_{TX} or $Z_{in,TIA}$ might leads to impedance mismatch with the cable's characteristic impedance. As a result the equalization effort will also be affected. To clarify such an effect, equalizer length estimation is carried out. To do this a simple termination model is built as shown in Fig. 4-10, where Z_S and Z_L are used to emulate Z_{TX} and $Z_{in,TIA}$ separately. After signal transmission, the current flowing through Z_L, I_{out}, is sampled and quantized for the following digital domain equalizer. Zero-forcing equalization (ZFE) is used for its advantage of good crosstalk cancellation, as explained in Chapter 3.

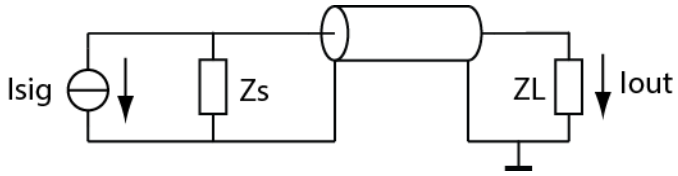


Figure 4-10 Simple current mode transmission for equalization model

In order to quantify the crosstalk, the pre-defined peak distortion (PD) in Chapter 3 is used as a measure of residual crosstalk after equalization. In calculation two different cable losses (1 Ω/m and 24 Ω/m) are used for comparison, where the higher loss is extracted from the cable used in the project. Fig 4.11 shows calculated shortest equalizer length with different $Z_{in,TIA}$'s and cable losses in order to keep PD less than -40 dB.

Fig. 4-11 shows that:

- In the high loss situation (R_0> 10 Ω/m), the shortest equalizer length is almost independent of $Z_L$when Z_L is less than 100 Ω. This is because that the high loss in the cable attenuates reflections caused by the impedance mismatch. To the ZF equalizer in this situation, the cancellation of reflections is less critical than the repair of the poorly shaped bandwidth. Therefore the equalizer length is insensitive to Z_L.

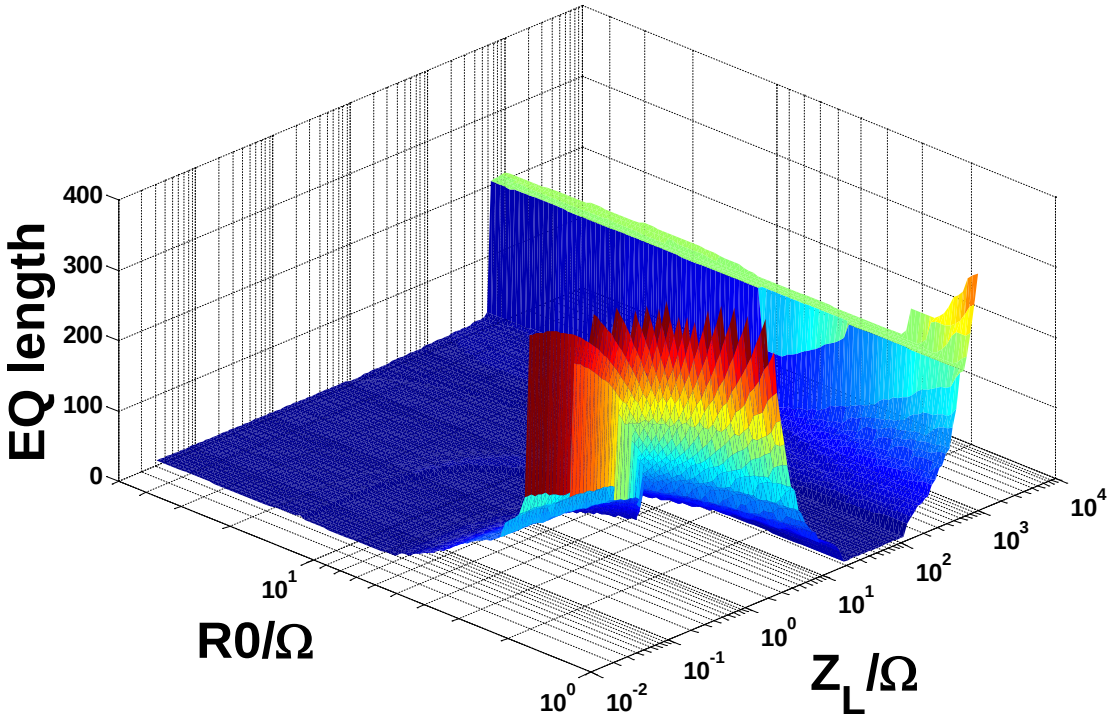


Figure 4-11 Simulated shortest equalizer length needed to obtain -40dB PD,

as a function of Z_L and cable loss

- In contrast, in the low loss situation (R_0<10 Ω/m), the shortest equalizer length is strongly dependent on Z_L when Z_L is chosen to be low. This goes with the intuition that the reflection requires more effort for the equalizer to cancel it than in the high loss situation. As Z_L approaches the cable's characteristic impedance, the equalizer length reaches the minima due to minimized reflections.

- In whatever situation, the shortest equalizer length increases when Z_L is chosen to be high. In this case the bandwidth of the overall transfer function became narrower and difficult to be equalized.

In our application, the cable used in the project owns the loss of 24 Ω/m, which falls into the high loss region as shown in Fig. 4- 11. Furthermore in expression (4-8) $Z_{in,TIA}$ is chosen to be less than 100 Ω for SNR consideration, which also meets the requirement of keeping the equalizer length as short as possible. Therefore, in the equalization point of view, the predefined constraint in expression (4-8) needs no more refinement.

4.4 Summary

In this chapter, specifications for the TX transconductor and RX circuits (TIA, extra gain stage and ADC) have been derived with the emphasis on the SNR and effort of equalization. As a summary, the specifications are tabulated in Tab. 4-2.

Table 4-2 Specifications of all the building blocks in the system

Specifications of building blocks	Value	Motivation
G_m	1 mS	To satisfy the SNR target
Z_{TX}	>=100 Ω in the signal band	To lower the noise from Z_{TX}
Excess noise factor of a transconductor	Not critical	Overall noise is dominated by the cable.
R_F of TIA	>=1 kΩ	To lower the noise from R_F
Gain-bandwidth of TIA	≈4 GHz	To provide less than 100Ω input impedance in the signal bandwidth, given the R_F determined above.
Gain of the extra gain stage	5V/V in the signal band	To make its output adapt to the input range of RX ADC
Sampling speed of RX ADC	100 Ms/S	To satisfy Nyquist sampling theorem and to lower the cost
Resolution of RX ADC	8 bit	To satisfy the SNR specification

Based on these determined parameters, transistor-level and PCB-level designs will be carried out, which are the main contents of the next two chapters separately.

4.5 References

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Chapter 5 Circuit Implementation

In this chapter, the details of the circuit design are given. In the beginning, two multiplexing configurations are analysed and compared. Next, the sampling capacitor array is introduced to accomplish the signal receiving and input multiplexing. After that, the design of the main part of the TX chip, a novel transconductor, is described to achieve low power in the TX part of the system. This is followed by the description of the overall timing control, which is critical to accomplish multiplexing and auto-zeroing. After that, an active output biasing circuit is introduced, for the goal of eliminating undesired DC voltage drop due to the finite DC loss of the cable. Then the test features of the chip are described. The end of this chapter is dedicated to the chip layout.

5.1 Multiplexing Configuration

It is important to identify the location where multiplexing happens: at the input or the output of the TX driver (Fig. 5-1).

5.1.2 Input Multiplexing

In the input multiplexing shown in Fig. 5-1 (a), switches are inserted before the TX drivers, so as to interleave the sampled signals from the four inputs, with transmission duration of $T_s/4$. However, there are several problems with this implementation:

- High bandwidth is required by the TX driver, since the transmission duration of each sample is shrunk into only a quarter of the input sampling period, which is $T_s/4$.
- Finite resistance of the multiplexing switches, together with the sampling capacitors, causes finite-time settling at TX driver's input, which will be completely transmitted onto the cable and recorded by the RX ADC. And this settling error is hard to be calibrated due to the associated non-linearity.
- The parasitic capacitance at the common-connection node, as shown in Fig. 5-2, can cause crosstalk among input signals.

5.1.3 Output Multiplexing

As the counterpart, in an output-multiplexing system, the multiplexing switches are configured after the TX driver, as shown in Fig. 5-1 (b). In this configuration, more time can be allocated to each driver for settling, thus allowing a reduction of power per driver. However, since four drivers have to operate at the same time, there is no obvious power-consumption advantage compared to the output-

multiplexing case. However, an advantage of output multiplexing is its better crosstalk immunity. Based on this the output multiplexing is chosen in the project. The solutions related to the implementation issues will be introduced in section 5.5.1.

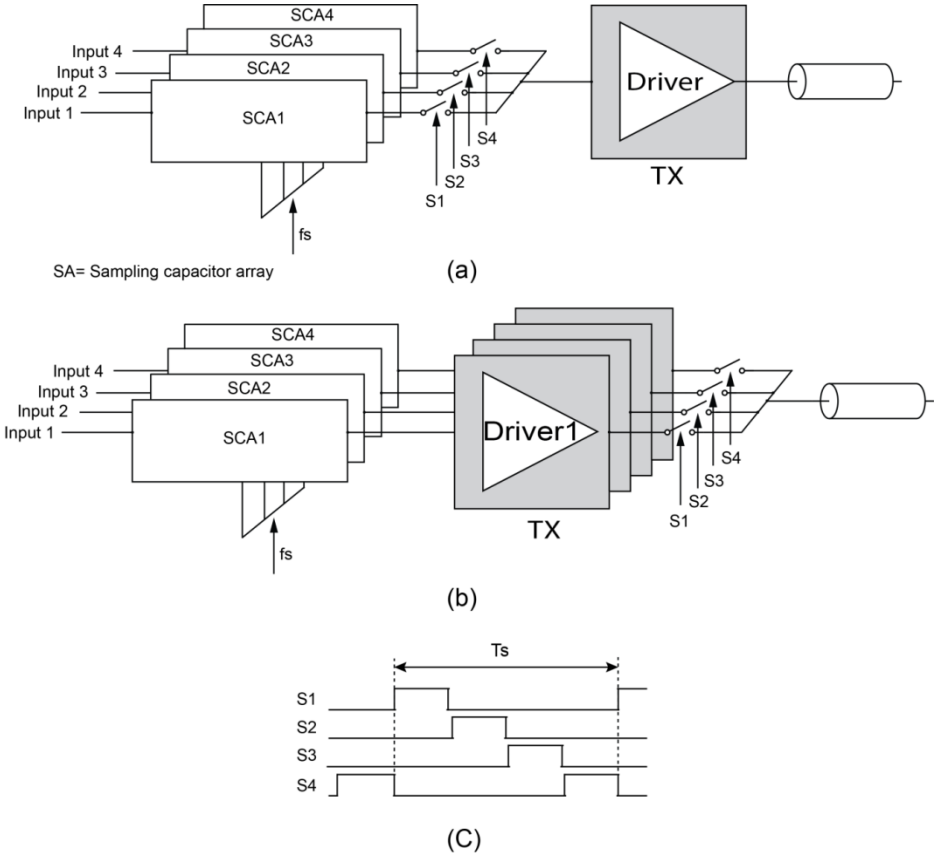


Figure 5-1 Two configurations of a multiplexing system

(a: input multiplexing, b: output multiplexing, c: timing of multiplexing switches)

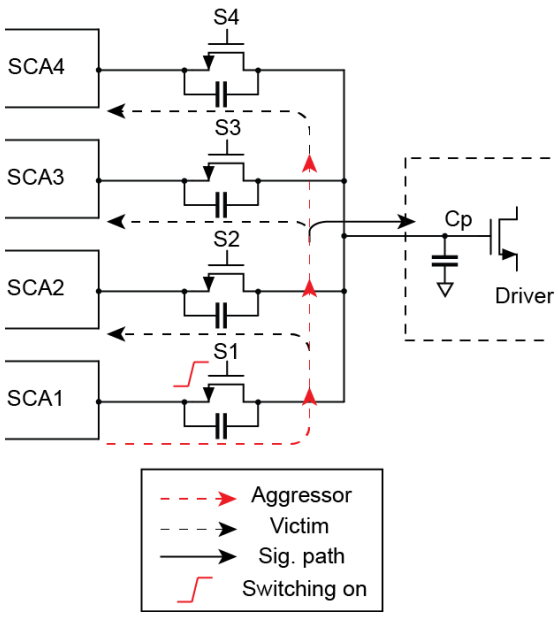


Figure 5-2 Crosstalk in input multiplexing

5.2 Sampling Capacitor Array

As mentioned in Chapter 1, the micro-beamformer(μBF) produces synchronously sampled-and-held signals. These signals are re-sampled by an array of sample-and-hold stages in order to create proper time shift for multiplexing. Fig. 5-3 gives a timing description of the 4 sampling capacitor arrays.

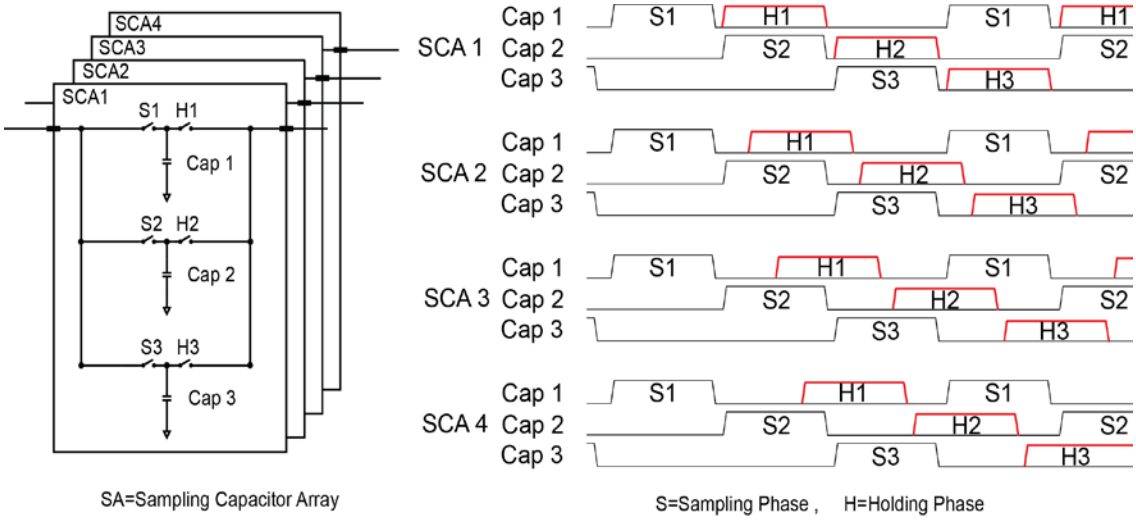


Figure 5-3 Timing of 4-input sampling capacitor arrays

(left: sampling capacitor arrays, right: the companied timing)

As shown in Fig. 5-3, each sampling capacitor array is connected to one driver, and there are 3 sampling capacitors circularly running to sample the input. The sampling switches of all the 4 arrays are closed simultaneously, which guarantees the synchronous sampling from the preceding stage. The holding switches of the 4 arrays are closed successively in order to provide time-shifting outputs to their corresponding drivers.

In implementation, the top-plate sampling circuit in Fig. 5-3 is changed into bottom-plate sampling, as is shown in Fig. 5-4. This makes the sampling circuit insensitive to stray capacitances [5.1]. Besides that, the early switching-off of switch MS2 prevents the charge injection from MS1 from changing the charge held on C_s, which helps to decrease the nonlinearity caused by MS1's signal-dependent charge injection. All the switches in the sampling capacitor arrays are NMOS transistors in deep-nwell for its low on-resistance compared to the normal NMOS switches. The designed resistance for any sampling switch is around 650 Ω, and the sampling capacitor is designed as 1 pF for 60 dB SNR for input sampling.

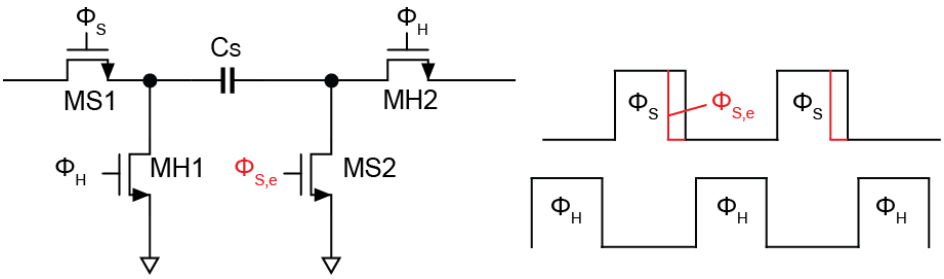


Figure 5-4 Stray-insensitive bottom-plate sampling

(left: circuit implementation, right: timing)

5.3 Transconductor Design

To design the (current-mode) TX driver, an appropriate transconductor has to be selected. Low power consumption is the key requirement is our application. Therefore, a factor called current efficiency (CE) is hereby leveraged [5.2], which specifies the ratio between the transconductance and the total current consumption:

$$CE = \frac{G_m}{I_{tot}} \qquad (5-1)$$

where G_m is the transconductance and I_{tot} is the total current a transconductor consumes.

5.3.1 Source-Degeneration Topology

The simplest transconductor with well-defined transconductance is the degenerated common-source topology shown in Fig. 5-5.

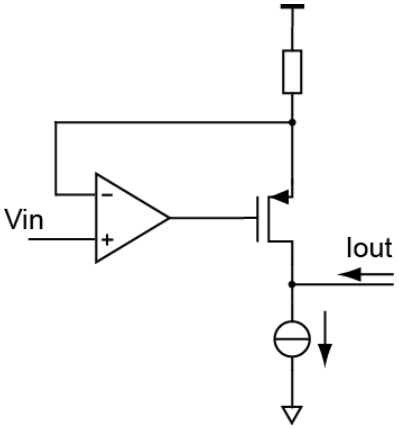


Figure 5-5 Amplifier-assisted source-degenerated transconductor

However, in this topology, the transconductance is defined by resistor R:

$$G_m \approx \frac{1}{R} \qquad (5-2)$$

provided the transconductance g_m of transistor M1 is substantially larger than 1/R. This makes this topology rather power hungry. A good solution to address the above issue is the use of a helper amplifier around the source and gate of the source-degenerated transistor, as shown in Fig. 5-6. By driving the source-degenerated transistor with a current-efficient amplifier, the overall current efficiency can be improved. To explain this we write the G_m of the above circuit as

$$G_m = \frac{Ag_m}{Ag_mR + 1} \qquad (5-3)$$

where A is the open-loop gain of the amplifier. Now to make the approximation in Exp. (5-2) valid, only the condition

$$Ag_m >> 1/R \qquad (5-4)$$

should be satisfied. This will lead to higher current efficiency for the source-degenerated transistor.

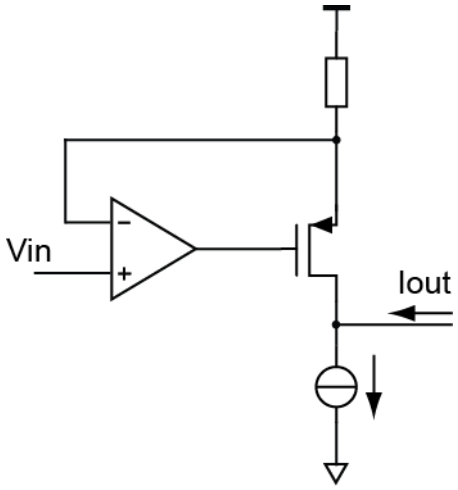


Figure 5-6 Amplifier-assisted source-degenerated transconductor

Current efficiency can also be increased by placing the helper amplifier around the drain and source of the source-degenerated transistor, as shown in Fig. 5-7(a). However, the drawback of this topology is that the output current cannot be read out directly as in the topology in Fig. 5-6. Here a current mirror is necessary to import or amplify the signal current, as shown in Fig. 5-7 (b). The linearity will be limited by the open-loop operation of the added branch, which makes it less attractive compared with the source-degeneration topology.

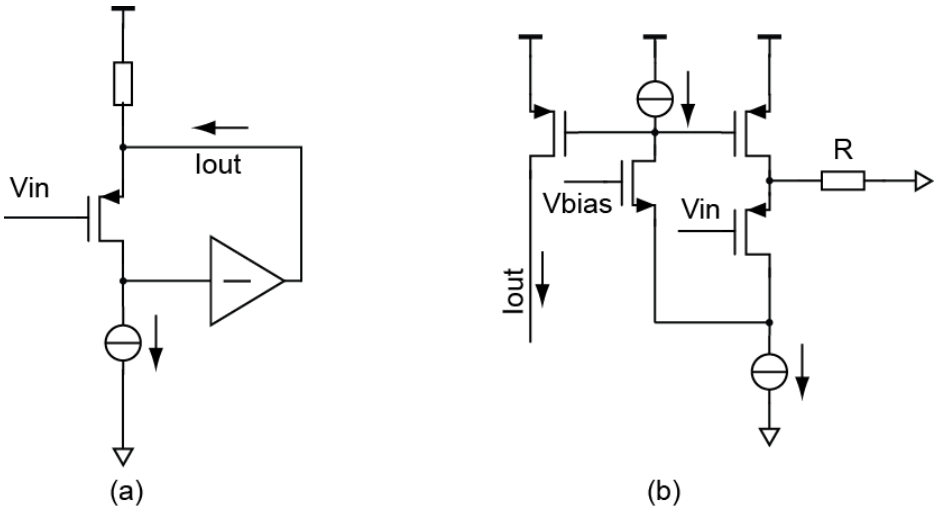


Figure 5-7 Other amplifier-assisted source-degenerated transconductors [5.3][5.4]

Therefore after comparison, the amplifier-assisted source-degeneration transconductor is selected in our project.

5.3.2 Implementation of the Helper Amplifier

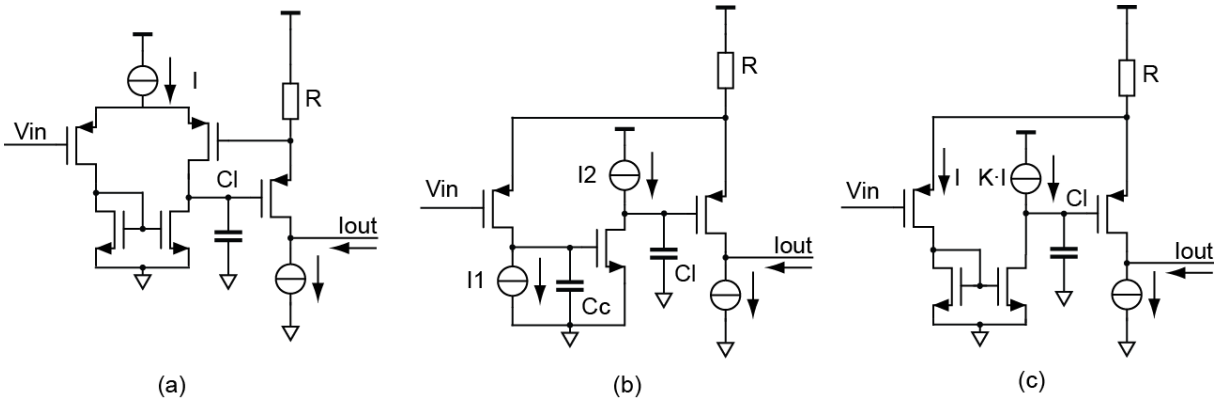


Figure 5-8 Candidates for current-efficient helper amplifiers

Fig. 5-8 shows several possible implementations of the helper amplifier. Fig. 5-10(a) shows a simple differential pair with active load; (b) shows a two-stage single-ended amplifier where C_c is added for frequency compensation. In (c) a new single-stage single-ended amplifier is proposed, where a current mirror with 1:K size ratio is inserted as the inverting stage. As explained in Appendix D, from the power-consumption point of view, (c) can be designed with higher power efficiency than the others in

either noise-limited or speed-limited situation. Therefore the circuit in Fig. 5-8(c) is chosen in the project. As illustrated in Chapter 4, in the context of the project, the noise from the transconductor does not dominate the overall noise performance, and thus K can be chosen as a larger value as in the speed-limited case.

5.3.3 Transconductor Implementation

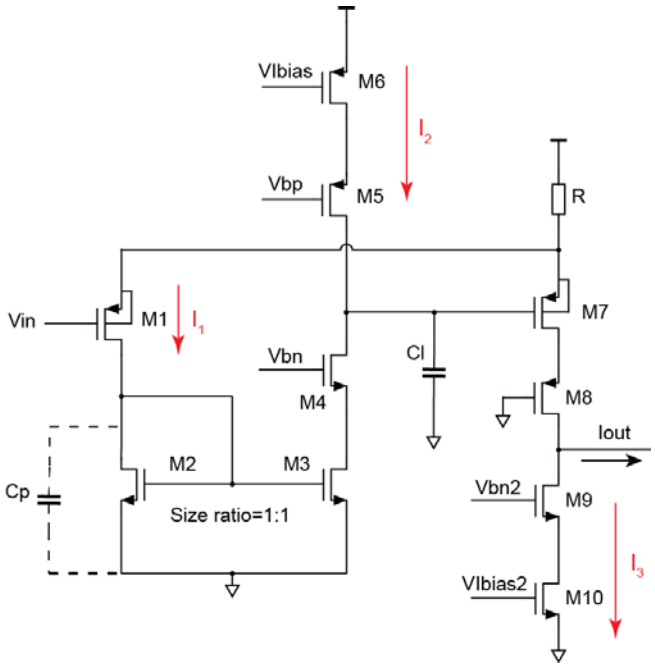


Figure 5-9 Implementation of the proposed transconductor

The final implementation of the transconductor is shown in Fig. 5-9. A PMOS input stage in chosen for two reasons. First such a selection makes source-body connection of the input transistor possible, reducing nonlinearity due to M1's body effect. Another reason is that the following NMOS current mirror composed of M2 and M3 can exhibit less parasitic capacitance C_p than a PMOS counterpart, so stability can be guaranteed without burning more power. Similarly, the PMOS source-degenerated transistor, M7 is also source-body connected for minimizing nonlinearity.

Besides the normal biasing transistors M6 and M10, cascode transistors M4 and M5 are inserted to increase low-frequency close-loop gain. M8 and M9 serve as current-steering switches, as will be explained in section 5.5.

The current assignments of the three branches are as follows, the current in the output branch, I3, has a minimum value for 100uA for class-A operation. In implementation 150uA is assigned to it for

enough margin. The current ratio in the helper amplifier is determined by the size ratio of the current mirror, M2 and M3. Here a 1:1 ratio is chosen to make in input transistor M1 have enough driving ability to push C_p away as a secondary pole. Finally, I1 and I2 are assigned with the same current of 30uA. The simulated unity-gain frequency of the loop gain is around 100 MHz over corners.

5.3.4 Biasing System

In order to reduce the layout complexity, the biasing system is separated into two parts. First an off-chip current is fed into the chip and copied with a 10:1 ratio into separate branches to provide biasing to the four drivers, as shown in Fig. 5-10. The off-chip current is generated using a tuneable resistor R_{bias} with a decoupling capacitor, C_{dcpl}, as also shown in Fig. 5-10.

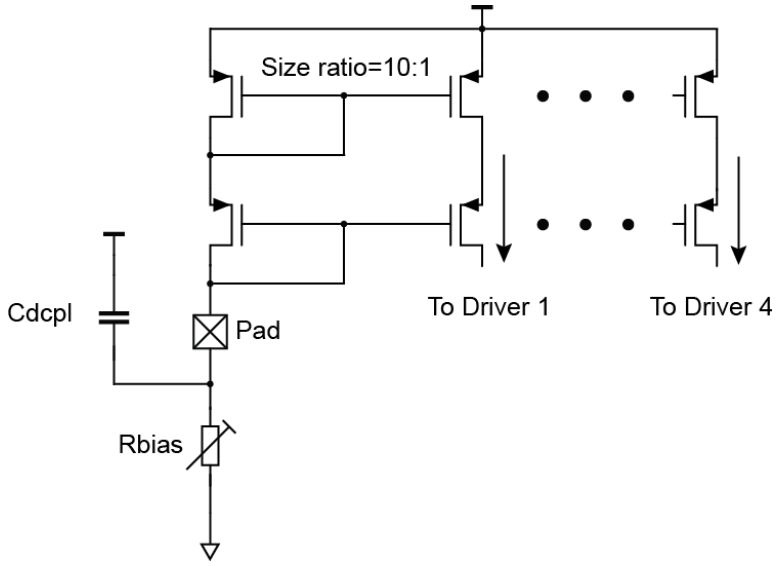


Figure 5-10 Global biasing circuit

Another part is the local basing unit, which is laid-out together with the corresponding transconductor, as shown in Fig. 5-11.

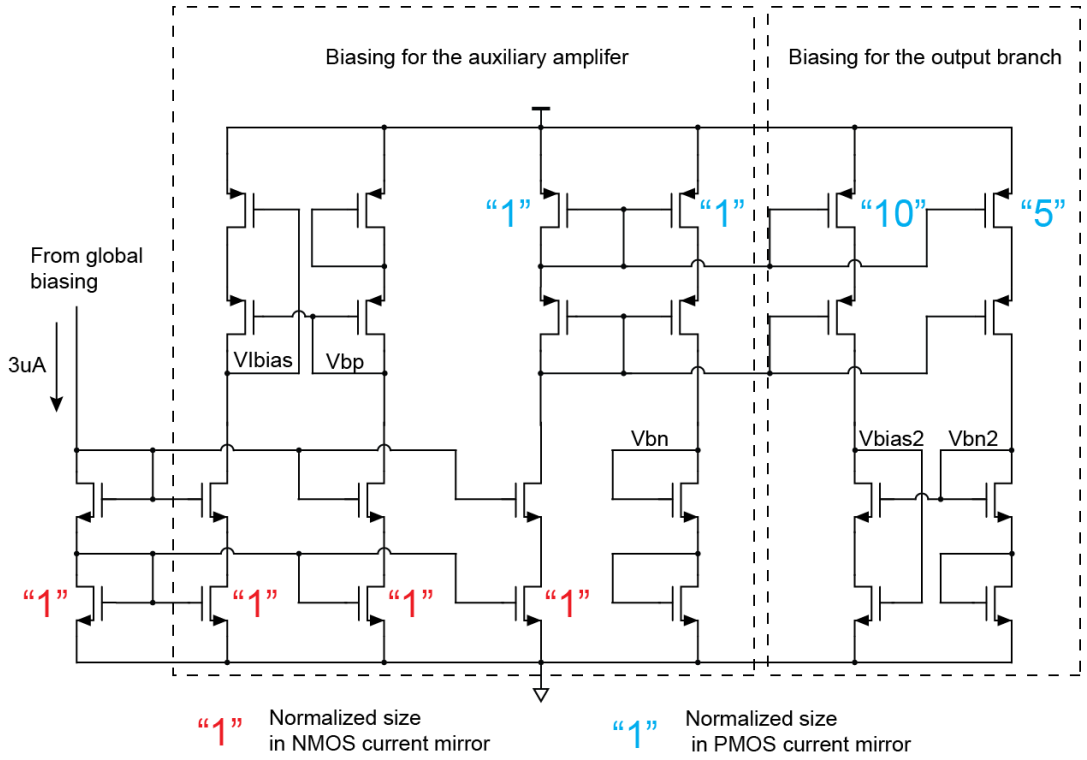


Figure 5-11 Local biasing circuit

In the global biasing unit a current of 52 μA is drawn from the supply, and each the local biasing unit consumes 57 μA current.

5.4 Auto-Zeroing

To define the DC biasing at the input of the transconductor, two approaches can be taken: replica biasing and auto-zeroing.

In replica basing, a circuit with similar or identical topology as the main transconductor is designed to provide an appropriate DC input level, which is DC coupled to the inputs of the transconductors, while the input signals are AC coupled. . In this solution a careful layout should be made to achieve a good matching between the replica biasing and the main driver, so as to suppress output DC current. In Chapter 6 it will be explained that the excessive DC current harms the dynamic range of RX.

In an auto-zeroing circuit, the main transconductors themselves will be configured as in unity-gain feedback during an auto-zeroing phase so that the resulting input voltage can be sampled and stored on a capacitor at the input. During the driving phase, the auto-zeroing capacitor is placed in series with the input source, as shown in Fig. 5-12.

One thing that should be pointed out is that the auto-zeroing switch, S_{AZ} is designed to be switched on earlier but switched off later than $S_{AZ.e}$, in order to avoid the instability caused by the light loading of the buffer-configured driver, which inherently is a two-pole system. Another observation on the timing in Fig. 5-12 is that the auto-zeroing switch S_{AZ} also serves as a reset switch for the preceding sampling period, which removes the signal stored on sampling capacitor used in the previous holding phase as shown in Fig. 5-3.

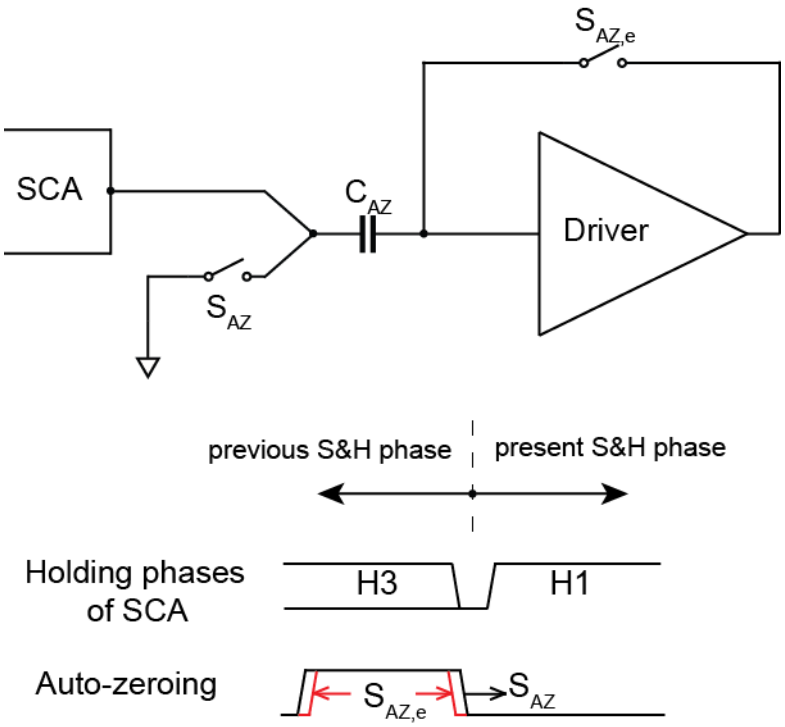


Figure 5-12 Auto-zeroing circuit implemented in the project

There are pros and cons associated with auto-zeroing. The key advantage is that, the residual output DC current can be minimized since DC output current due to mismatch will be compensated for by the auto-zeroing operation. Besides, the low-frequency flicker noise can be partially cancelled [5.5], but the wideband white noise will fold back to the Nyquist band, which may degrade the noise performance. Another advantage lies in the better power-supply-rejection-ratio (PSRR) compared to the replica biasing, but a wide-bandwidth PSRR means to use a small C_{AZ}, which might causes instability during auto-zeroing.

In the implementation, C_{AZ} is chosen as 1.5 pF for both stability and noise requirement. S_{AZ} is implemented as a deep-nwell NMOS also for the consideration of stability[1]. A dummy switch is also

[1] A deep-n-well NMOS is used to lower S_{AZ}'s on-resistance, of which a high value will lead to insufficient phase margin for the unity-gain-configured transconductor during auto-zeroing.

included to absorb the charge injected by S_{AZ}. Switch $S_{AZ,e}$ is implemented in a complementary form to lower its on-resistance and to obtain a first-order compensation of the channel charge, when both NMOS and PMOS transistors are switched off.

5.5 Design of Multiplexing Switch

5.5.1 Current-Steering Multiplexing Switch

Even though the output-multiplexing scheme shows good immunity to crosstalk, as explained in section 5.1, the output-multiplexing circuit in Fig. 5-1 exhibits several drawbacks:

- Charge injection causes excessive current spikes. As explained in Chapter 2, the cable exhibits low impedance during multiplexing. During the fast switching-off transition the channel charge of the multiplexing switches flows into the cable rather than into the high-output-impedance transconductors. Simulations show that the current spikes due to this effect have a higher amplitude than the transmitted signal, and thus increase the required dynamic range of the RX.

- At high frequencies, the cable impedance is much smaller than the on-resistance of the switch. This will lead to significant deviation from the model built in Chapter 3, which calls for an extra iteration for the system optimization.

Therefore, a gentle switching scheme should be designed in output multiplexing in order to minimize the resulting spikes. This is achieved by embedding the switches in the signal path, as shown in Fig. 5-13. Here PMOS switches are used on the signal side and NMOS switches on the biasing side. The current steering NMOS switches are switched to an appropriate biasing voltage instead of the supply voltage to operate them as cascodes and thus obtain higher output impedance. We will refer to this switching scheme as current-steering, which is commonly used in the current mode digital-to-analog converters (DAC) [5.6].

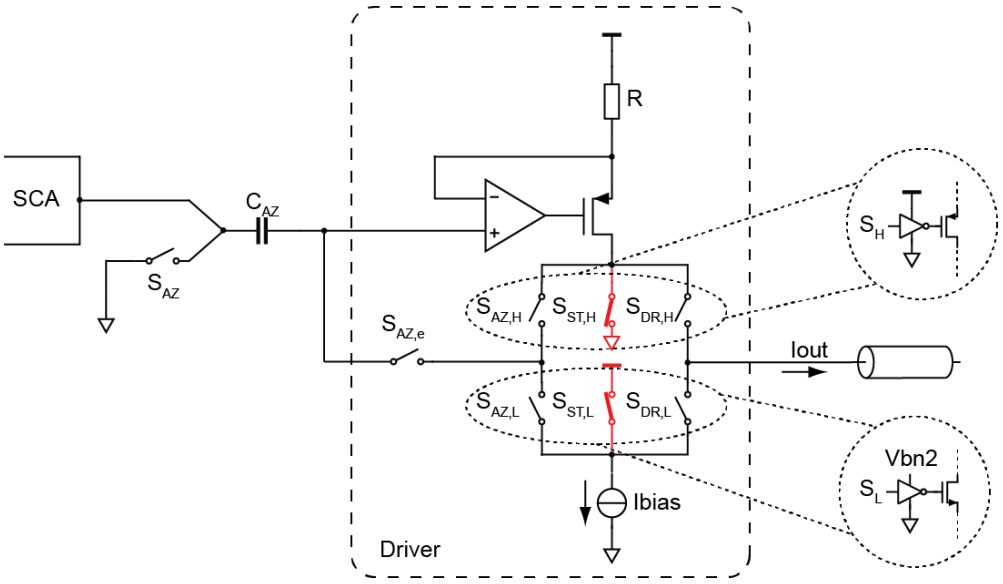


Figure 5-13 Multi-phase operation of a transconductor (red: settling phase active)

5.5.2 Timing of the Multiplexing Switch

Another important aspect in the design of the multiplexing switches is timing control.

In output multiplexing, the holding phase of the sampling capacitor array occupies a time slot of T_s but the transconductor only drives the cable during a time slot of $T_s/4$. To allow its output to settle before it is connected to the cable, a settling phase is inserted between the auto-zeroing phase and the driving phase, as shown in Fig. 5-13. During this phase, the input signal is connected to the transconductor, but no output signal is transmitted onto the cable. By doing this the signal's settling transient will not be seen by the cable, which shows the advantage of output multiplexing over its counterpart as mentioned in section 5.1.

Furthermore, to prevent current spikes at the outputs of the transconductors, the transitions between the 3 phases shown in Fig. 5-13 should be overlapping, as shown in Fig. 5-14. In contrast, non-overlapping timing is required between transition of the early released auto-zeroing switch, $S_{AZ.e}$, and the current steering switches, $S_{ST.H}/S_{ST.L}$. This is because an overlapped transition between auto-zeroing phase and settling phase will cause charge leakage from the auto-zeroing capacitor, C_{AZ}, which eventually affect the accuracy of the input biasing.

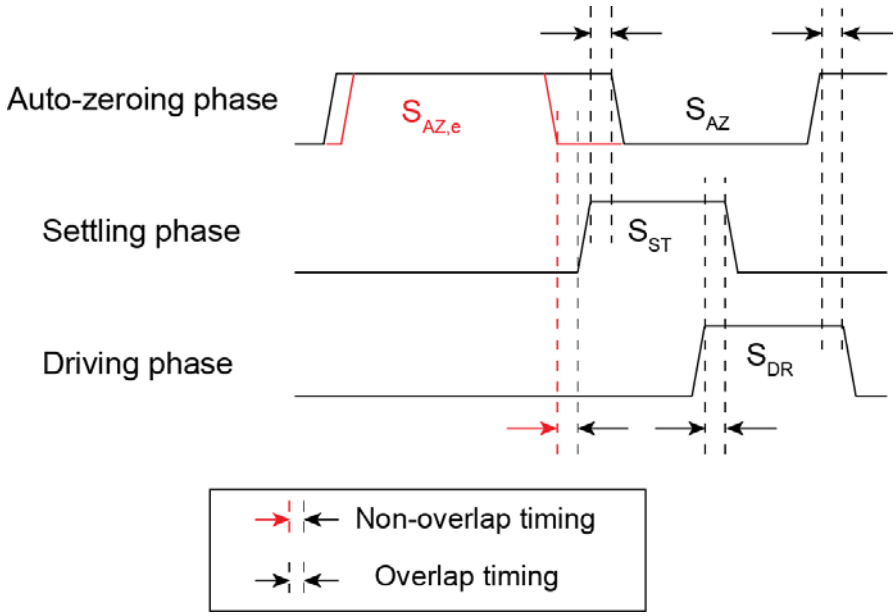


Figure 5-14 Timing of the current steering in output multiplexing

Besides the timing requirement within a single driver, driver-to-driver timing constraints are also necessary. As shown in Fig. 5-15, non-overlapping timing is required during phase transition so as to avoid crosstalk between drivers at the output.

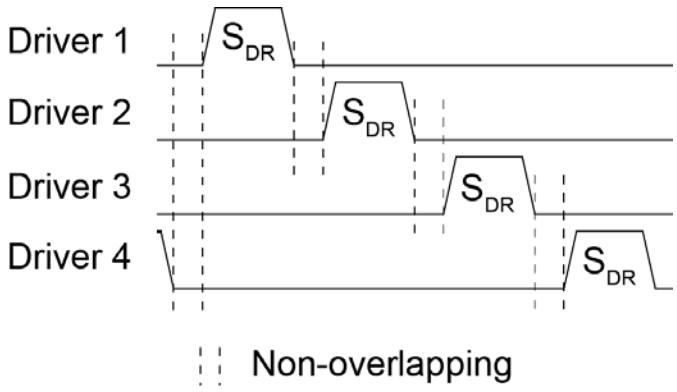


Figure 5-15 Non-overlapping timing during driver switching

The auto-zeroing phase is assigned around 20 ns and the settling and the driving phases are assigned around 10 ns separately. The longer time allocated to the auto-zeroing phase accommodates the lower closed-loop bandwidth in auto-zeroing phase, during which the primary pole of the helper amplifier becomes secondary.

In the implementation, the timing control is separated into two parts for wiring convenience. As shown in Fig. 5-16, at the input of the global control unit one 100MHz clock with reset control is fed into the chip, where the high-frequency clock is divided by 4 to generate 4 non-overlapping 25 MHz clocks for the local control in each driver. This makes the timing control insensitive to the duty cycle of the external clock.

In each local control unit, the 25 MHz clock first passes through a set of delay cells to generate the delays needed for the overlapping/non-overlapping timing. Some of the delayed clocks are sent to the sampling capacitor array, while the rest are used to generate the control for the current-steering switches, where the various overlapping/non-overlapping controls are ensured by using S-R latches driven by appropriately chosen delayed clocks.

The power consumption in the global unit is about 0.36 mW, while the power consumed by the local control (in total) is about 0.9 mW[2]. In both parts most power is consumed by S-R latches and D flip-flops.

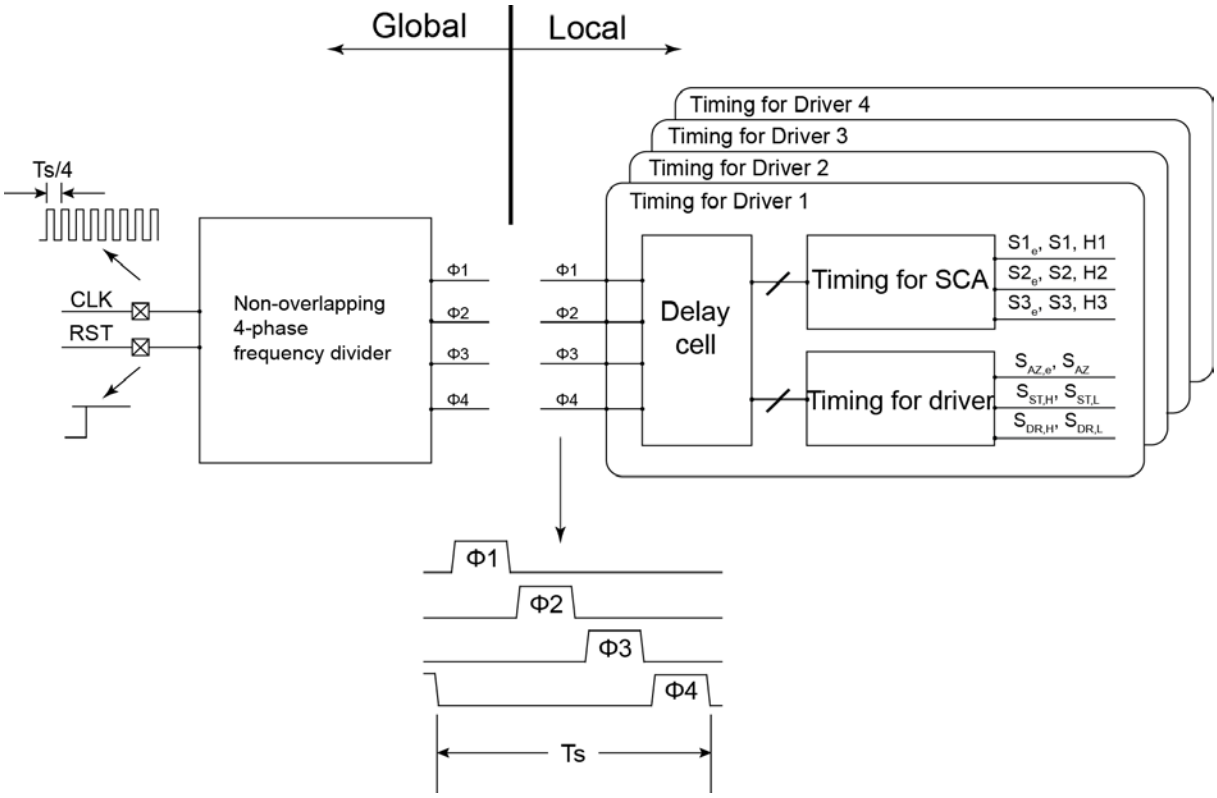


Figure 5-16 Organization of the timing control

[2] The measured power consumption is obviously lower than the pre-layout simulation, but close to the post-layout simulation. This is because in the TSMC digital circuit library, the schematic models exhibit larger parasitics than the corresponding layout. In post-layout simulation, the parasitics are extracted correctly.

5.6 Active Biasing

Due to the DC resistance of the cable, any DC current that leaks into the cable will pull down the driver's output voltage and reduce the headroom of the transconductor's output current biasing branch. This problem can be solved by AC-coupling the cable on TX side. However, due to the low cable impedance at high frequencies, the size of the AC-coupling capacitor would be intolerably large.

Another solution is to AC couple the cable on RX side, and at the same time to provide bias voltage at the input of the cable, as shown in Fig. 5-17. However, if a poorly defined bias voltage is provided via resistive biasing as shown in Fig. 5-17 (a), a current spike will appear during driver switching and eventually harm the dynamic range of the RX. Besides that, extra on-chip reference should be designed as well, which increases the circuit complexity.

To solve this problem, a buffer-configured replica driver is designed as an active biasing solution, as shown in Fig. 5-17 (b). By proper scaling the replica driver, a low DC but high AC output impedance is achieved at the same time, without any penalty of providing the excessive output noise current to the cable.

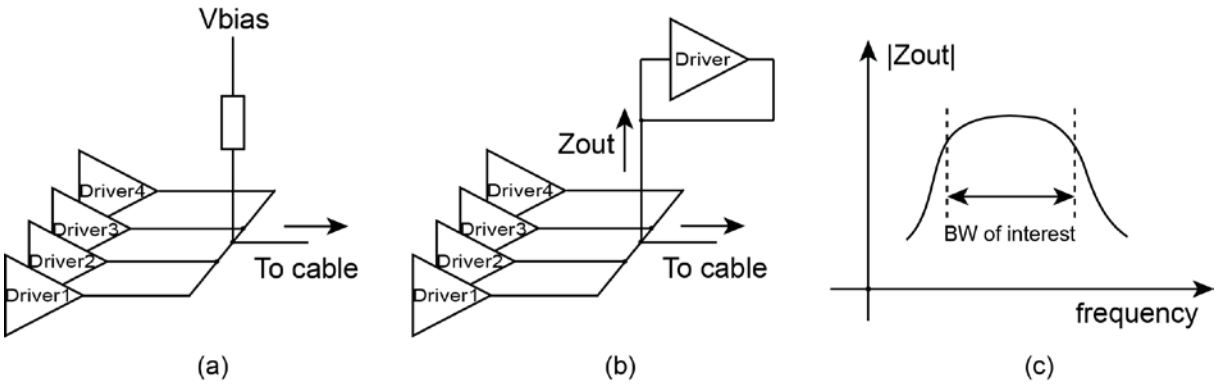


Figure 5-17 Cable biasing

(a: resistive biasing, b: active biasing, c: output impedance of the active biasing versus frequency)

5.7 Testability Design

5.7.1 MUX for Monitoring Node Selection

In order to test the function of the multiplexer, four identical monitoring nodes are chosen in all the four drivers, which is located at the output of the helper amplifier for its parasitic insensitivity. All the

monitoring nodes are connected to a unique PMOS source follower via a driver selection mux, as shown in Fig. 5-18. One isolation switch S_{iso} is also connected at the gate of the source follower, which will be closed when no monitoring is needed so to avoid capacitive coupling between drivers through the selection mux. The control of the selection mux is handled by a test-use shift register. The bias current of the source follower is provided off chip.

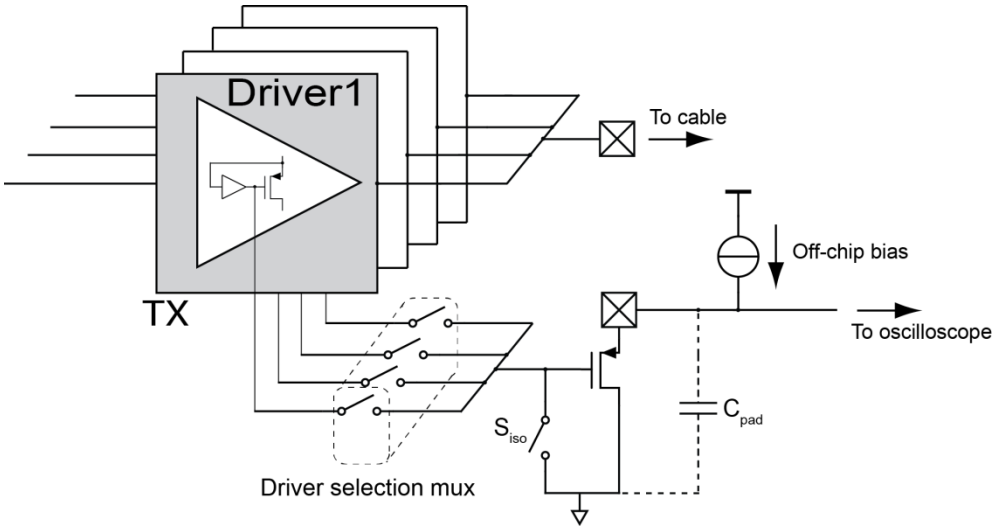


Figure 5-18 Driver selection MUX

5.7.2 High-Transconductance Mode

In order to explore the operation limit of the multiplexer, a high transconductance mode is designed by paralleling a resistor of the same value to the existed source-degeneration resistor in each driver. This mode is enabled by a PMOS switch S_{HGm}, as shown in Fig. 5-19.

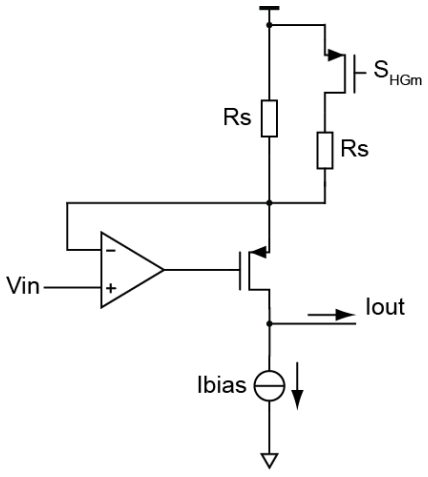


Figure 5-19 High transconductance mode

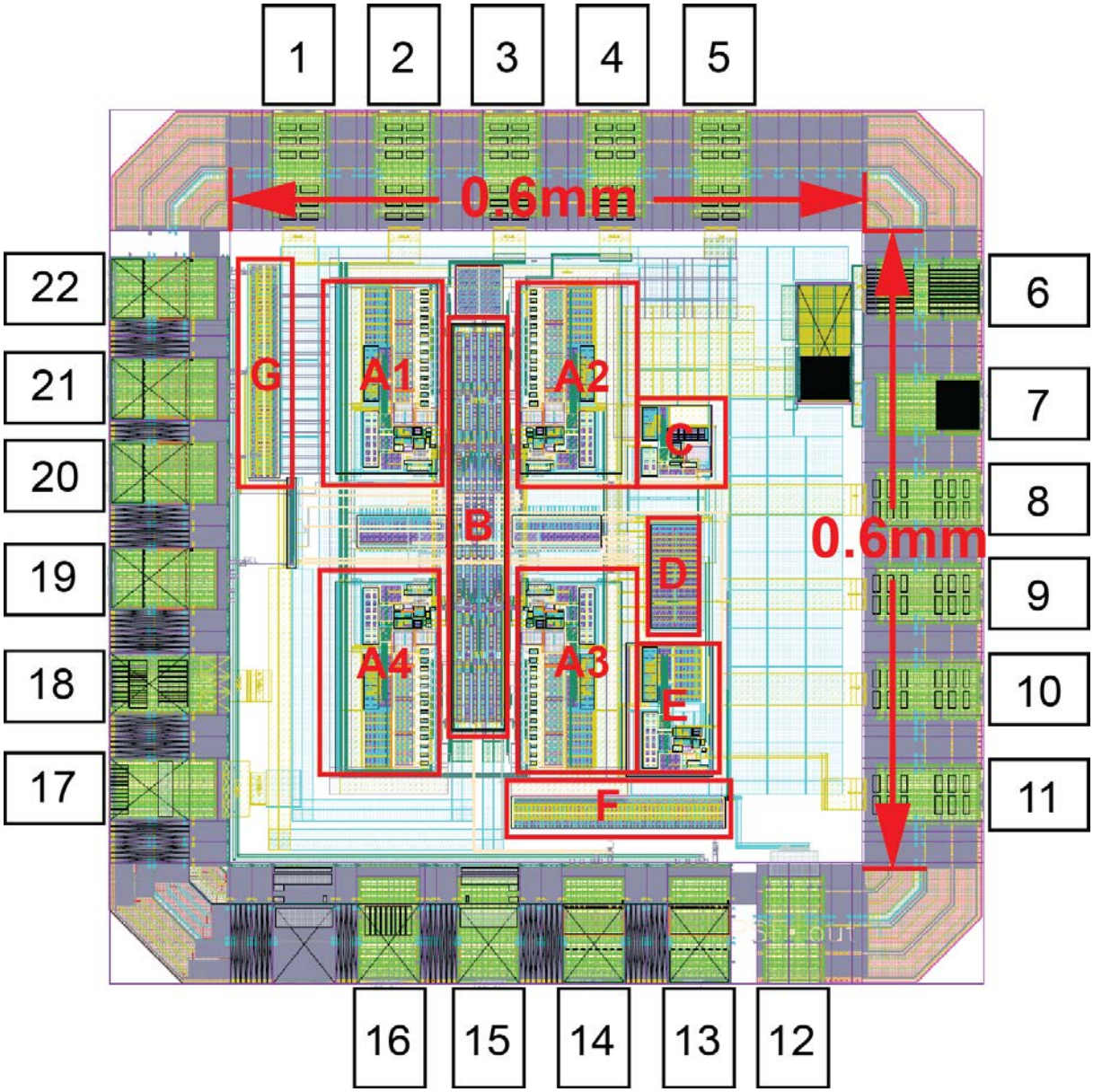
5.7.3 Test Transconductor

In order to test the function of a single driver, one extra transconductor is included for test use, of which the output is directly connected to an on-board TIA.

5.8 Layout Overview

Fig. 5-20 shows the layout of the TX chip with a description of the main building blocks. The four drivers are laid out in a common-centroid form to improve matching. Another benefit of this arrangement is that the multiplexing control (global and local) can be laid out in the centre of the chip and connected to the drivers in a H-tree form, which is good for minimizing the delay difference between drivers. In each driver, most of the area is occupied by the capacitor arrays and local biasing circuits.

The active area is 0.64 mm^2 (width: 0.8 mm, length: 0.8 mm). The chip uses 22 I/O pins which are connected to 12 analog and 11 digital bondpads separately. Among all the bondpads there is an ESD-free one in analog domain (Pin 12) in order to reduce capacitive loading to the test source follower described in section 5.7.1. Tab 5-1 gives the details of all the I/O's.



A1~A4: multiplexing drivers **B**: digital control **C**: replica biasing **D**: current source

E: test-use transconductor **F**: source follower **G**: shift register for test mode

Figure 5-20 Layout of the current mode analog multiplexer

in TSMC 0.18um mixed-signal/RF technology

Table 5-1 Pin assignments

Pin number	I/O	Function
1~4	AI	4 inputs of the multiplexer
5	AI	Reference voltage
6	AIO	Analog ground
7	AIO	Analog supply
8	AO	Multiplexer output
9	AI	Input of current source
10	AI	Input of the test-use driver
11	AO	Output of the test-use driver
12	AO	Source follower output
13	DI	Reset input
14	DI	Clock input
15	DIO	Padring supply
16	DIO	Padring ground
17	DIO	Digital supply
18	DIO	Digital ground
19	DI	High-gm selection
20	DI[3]	Indicator of test mode
21	DI	Reset of the shift register
22	DI	Trigger of the shift register

AI: analog input, AO: analog output, AIO: bi-directional analog pin

DI: digital input, DO: digital output, DIO: bi-directional digital pin

5.9 Summary

In this chapter the chip design has been elaborated. A novel transconductor has been proposed, which is suitable for a speed-limited low-power design as required in the project. Later by embedding the multiplexing switch into the transconductor in a current steering form, disadvantages of output multiplexing have been avoided. The test features of the chip and a layout overview have been included for quick reference.

[3] A wrong pin assignment was made by taking the digital output as an input.

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Chapter 6 Measurement

6.1 Measurement Setup

The measurement setup consists of the following parts:

- Printed circuit boards (PCBs): { Transmitter PCB / Receiver PCB / Cable adapter
- ADC: emulated using an oscilloscope
- Control and algorithms: { FPGA (Altera Cyclone II) / Algorithm on Matlab
- Sources and supplies: { Signal sources (Aliglent 33522A) / Supplies

An overview of the whole system is shown in Fig. 6-1.

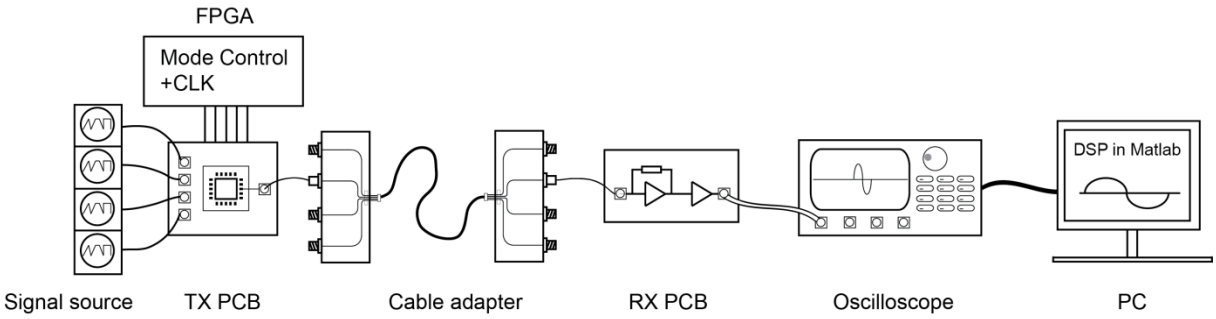


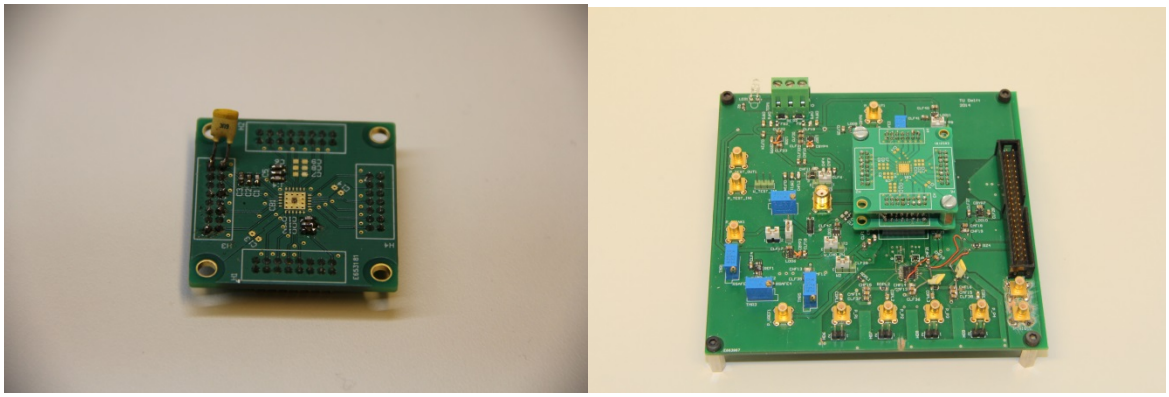
Figure 6-1 Overview of the whole system

Transmitter PCB

The transmitter PCB is composed of two separate boards: a daughterboard and a motherboard. The former is used to load the chip and is mounted onto the latter, as shown in Fig. 6-2. This chip-on-board assembly is used, rather than conventional packaging, to minimize parasitic capacitances, which may limit the signal bandwidth.

The motherboard contains:

- Mode selection MUXes at the input of the chip
- Digital buffers for the control signals from FPGA to PCB
- TIA and source follower for the on-chip test-use driver
- Current source, reference and power supplies



(a) Daughterboard (b) Motherboard

Figure 6-2 Transmitter PCB

The mode selection MUXes are critical to the system. Using these MUXes, three operation modes can be selected: DC mode, pulse generation mode and normal mode (Fig. 6-3). In DC mode, a reference voltage is sampled and multiplexed by the TX. By doing this, the periodic output pattern due to clock feedthrough can be recorded, which will be recorded and subtracted to get a clean pulse response during equalization. In pulse generation mode, a voltage pulse of 100 mV amplitude is generated and fed into the chip. This is done by switching one of the chip's inputs to a voltage V_{pulse} of 100mV higher than the reference voltage, as shown in Fig. 6-3. By doing this, we can measure the pulse response of the whole system and then equalize the signal chain. In normal mode, ac-coupled signals from 4 signal sources are fed to the inputs of the chip, and multiplexed in the form of sample and hold.

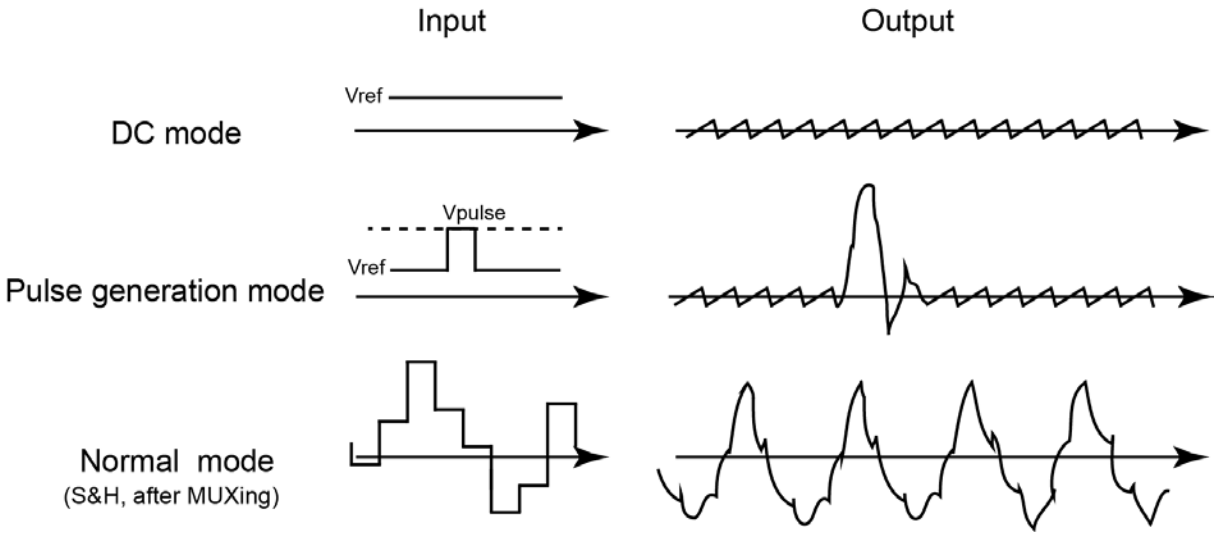


Figure 6-3 Operation modes of the TX PCB

The switching between these modes is done by 2 stages of off-chip MUXes, as shown in Fig. 6-4. The first MUX is responsible for the switching between normal mode and the other two modes. The second MUX takes care of switching between DC mode and pulse generation mode. The truth table of the two mode selection control is shown in Tab. 6-1.

Table 6-1 Truth table of the mode selection control

MUX1	MUX2	Mode
H	H	Pulse generation mode
H	L	DC mode
L	L	Normal mode

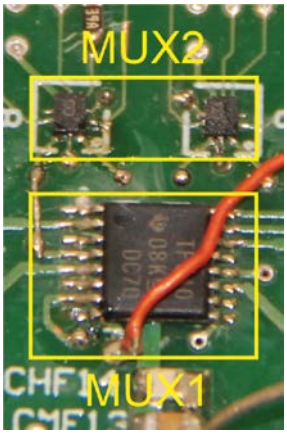


Figure 6-4 Mode selection MUXes

Receiver PCB

As introduced in Chapter 1 and 4, there are two stages designed on the receiver PCB, a TIA and an extra gain stage. Fig. 6-5 gives the schematic of receiver PCB. As is shown in Fig. 6-5, current signals from the cable are fed into a TIA by AC coupling. The TIA's output voltage is sent to the extra gain stage in order to adapt to the following ADC (emulated by an oscilloscope in this case). In order to reduce the parasitic to the largest extent, active and passive devices are mounted back-to-back on both sides of the board, as shown in Fig. 6-6.

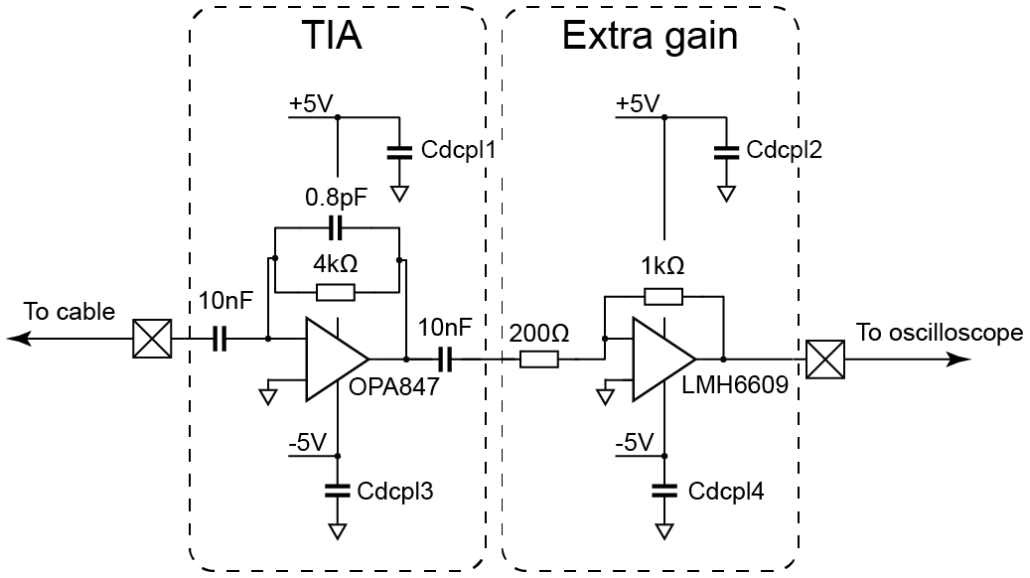
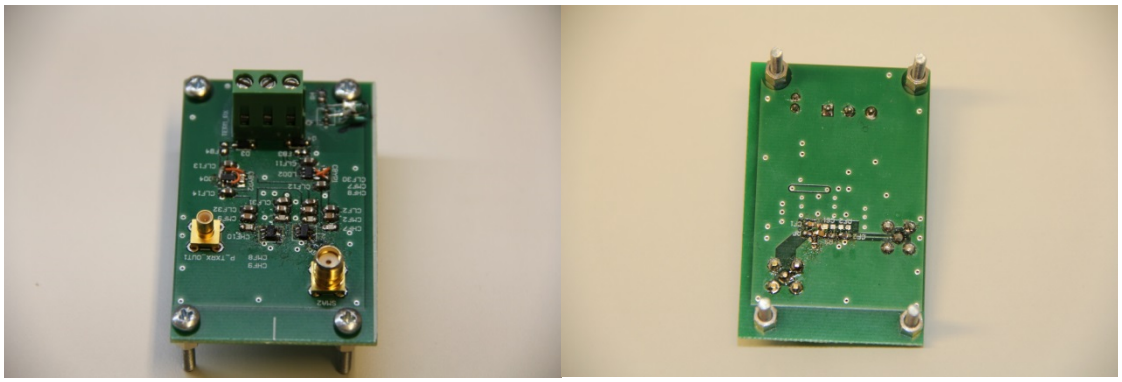


Figure 6-5 Schematic of RX PCB



(a) topside (b) backside

Figure 6-6 Receiver PCB

Cable adapter

The cable adapter is composed of two PCBs on which several cables are mounted, as shown in Fig. 6-7. The adapter has been used for both cable characterization as introduced in Chapter 2, and for system measurement as described in this chapter. This arrangement provides the option to test more cable samples.

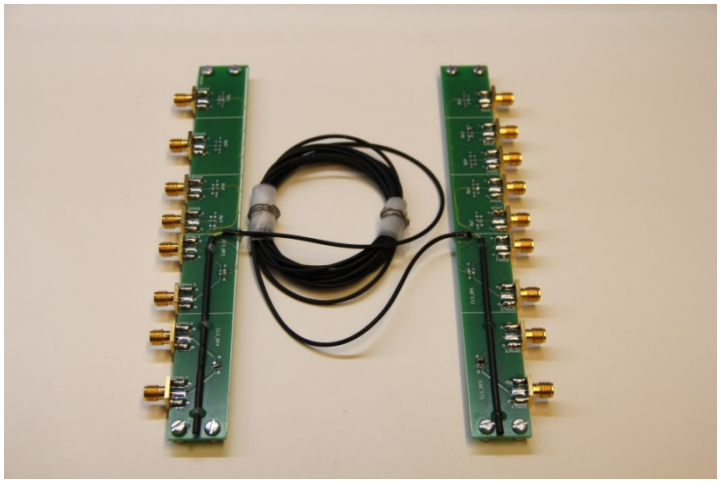


Figure 6-7 Cable adapter

ADC emulation

A digital oscilloscope (YOKOGAWA DL9710L) is used to emulate an ADC for simplicity. A challenge associated with this is that the sampling clock of the oscilloscope is not synchronized with the clock of the TX chip. To address this issue, the chip's clock is sent to the oscilloscope and its zero-crossing points are interpolated and recorded by the oversampling nature of the oscilloscope, as illustrated in Fig. 6-8. By using these zero-crossing points as the sampling moments, the signals sampled by the oscilloscope can be resampled at the chip's clock frequency. Before resampling, a digital anti-aliasing filter is inserted in order to suppress the out-of-band noise from the oscilloscope's sampler.

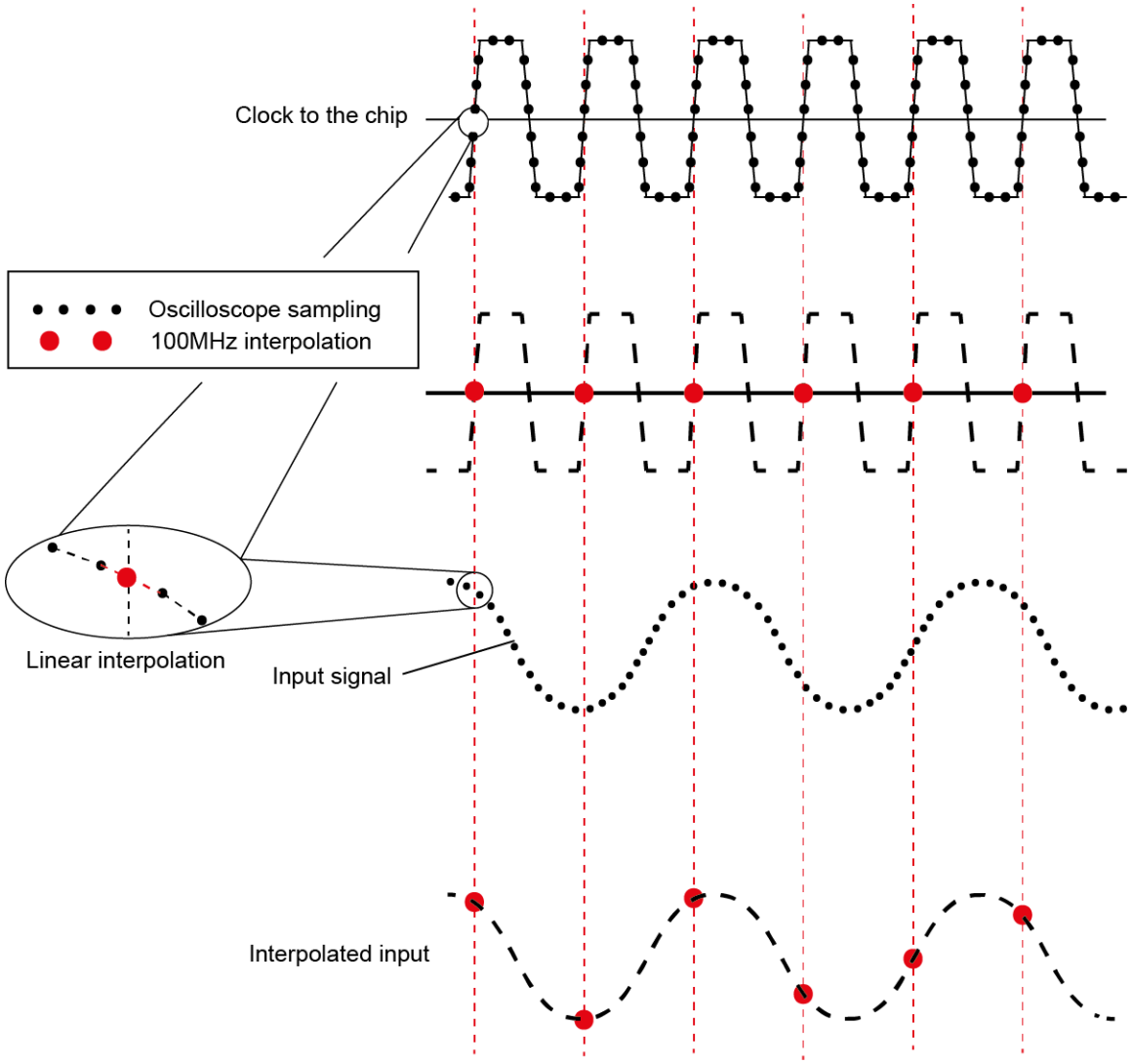


Figure 6-8 Zero-crossing interpolation

FPGA control and algorithms

An FPGA evaluation board of Altera Cyclone II is used to control the whole system. Its main tasks include

- Clock generation
- Mode selection control
- Synchronous pulse generation
- Periodic trigger generation

The synchronous pulse generation is used in the pulse generation mode as discussed in Section 1.1. Since the pulses generated at the inputs of the TX chip should be synchronized with the on-chip

sampling clocks, a replica of the on-chip digital logic is implemented on the FPGA and driven at the same clock frequency to generate the control signals for the pulse generation. However, due to the switch-on time of the on-board MUX and the propagation delay between the FPGA evaluation board and the chip, an incorrectly-timed pulse may appear at the input of TX, as shown is Fig. 6-9. This will cause the pulse to be sampled by more than one on-chip sampling capacitor. To prevent this, the phase delay between the two aforementioned clocks has been made tuneable. The correct timing of pulse generation control is shown in Fig. 6-10.

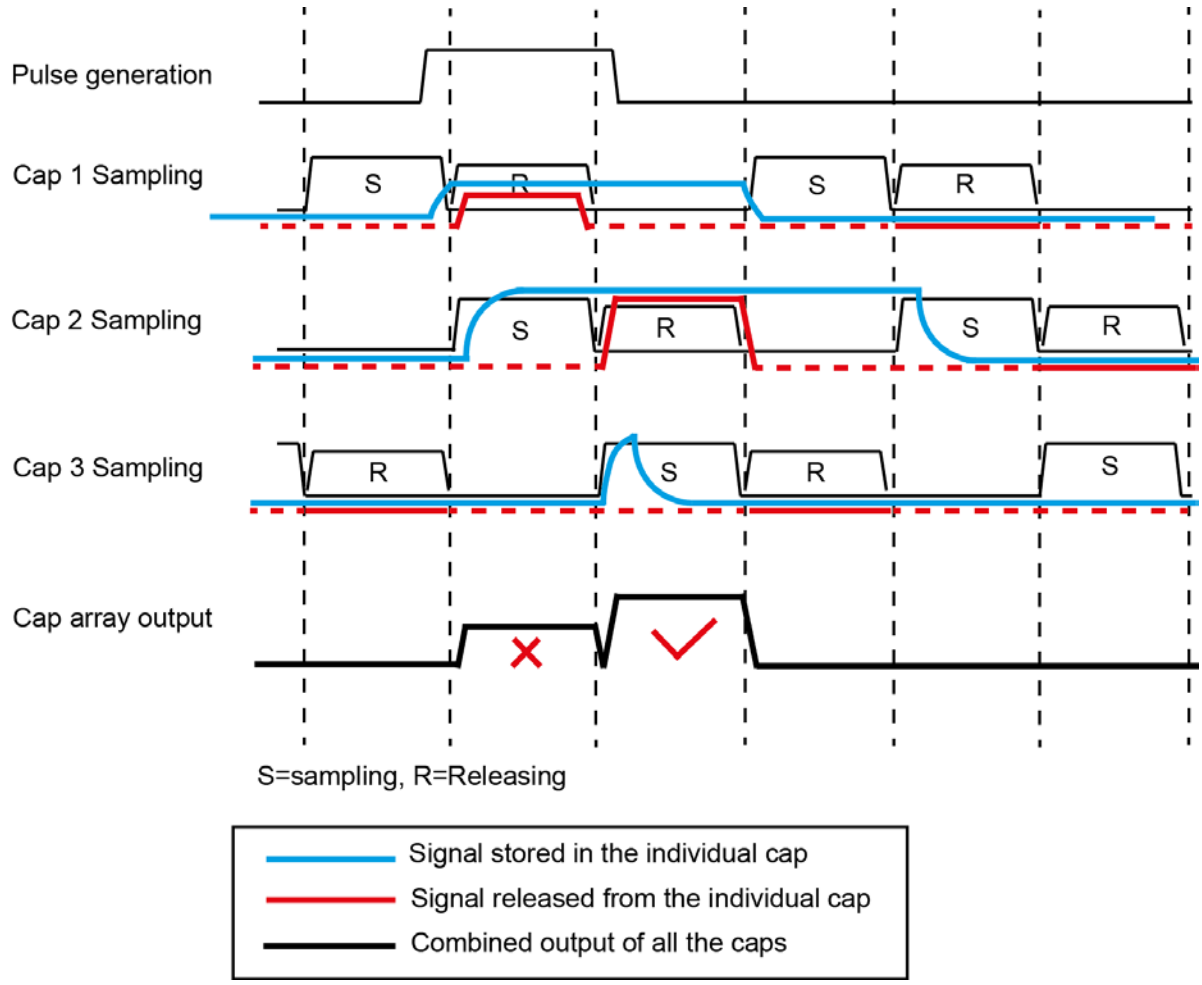


Figure 6-9 Wrong timing of pulse generation control without phase tuning

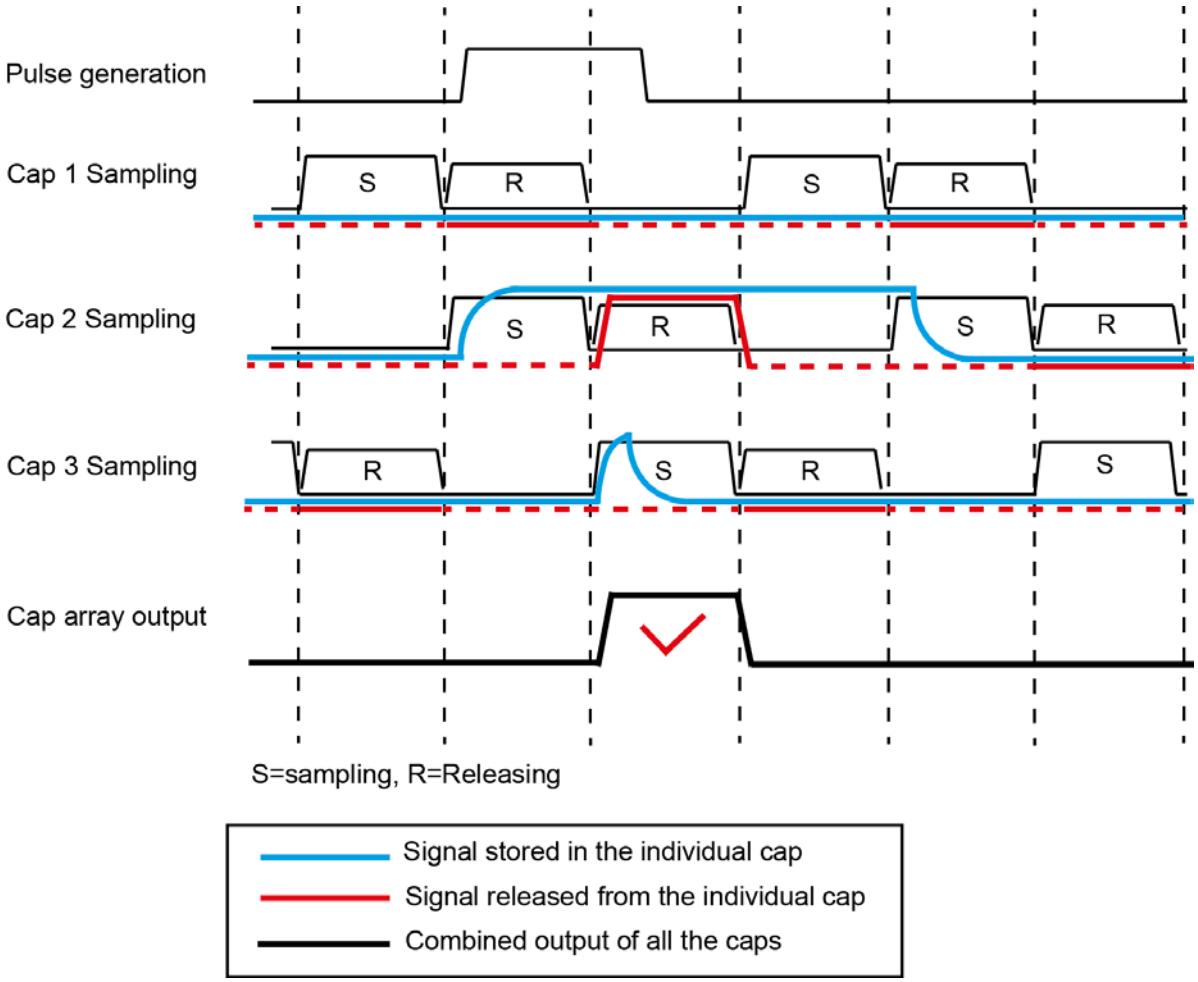


Figure 6-10 Correct timing of pulse generation control obtained by phase tuning

Besides controlling the pulse generation, the FPGA also provides periodic triggers for the oscilloscope to catch the background pattern and the system's pulse response. Thus, we can record the channel responses associated with different drivers or even with different sampling capacitors. After comparison we can judge the necessity of adopting the more complicated equalization algorithms such as MIMO equalization.

The equalization algorithms are implemented in Matlab. As a first trial ZFE is used in the measurement for simplicity. But the migration to MMSE equalization can also be easily accomplished.

Sources and supplies

During measurements, input signals are provided by two Agilent 33522A waveform generators. Power supplies are connected directly to the receiver PCB and then wired to the transmitter PCB. Such a configuration is made to approximate the real application environment, where supplies can

only be provided from the mainframe and fed into the probe. However multiple ground connections to the various instruments will introduce ground loops [6.1][6.2]. To minimize such loops, both PCBs and the FPGA are supplied by batteries[6]. To read out the output of the receiver PCB, an active differential probe is used to connect with the oscilloscope, which can provide enough CMRR against the ground bounce[6.3].

6.2 Measurement Results

The measurements have been carried out in the following 2 parts. First, the system's performance before equalization has been characterized, which includes

- TX driver measurement
- Cable propagation delay measurement
- SNR and THD before equalization

Second, measurements with equalization have been carried out. We start from the characterization of a single driver in order to verify basic performance of the system. It is followed by the two-driver test, which aims to clarify origin of the over-large crosstalk. Finally a full-driver test is done to completely verify the function of the whole system.

6.2.1 Measurement without Equalization

TX Transconductor Measurement

To characterize the performance of the drivers on the TX chip, the on-chip test-use transconductor is directly connected to the test-use TIA without cable connection. The configuration of this TIA is the same as that of the one used in receiver PCB, as shown in the previous section. The input signal is a 6MHz sinusoidal signal with 200 mV peak-to-peak amplitude, generated by an Agilent 33522A waveform generator. The outputs of both the signal source and the test-use TIA are first sampled by the oscilloscope, and then proper filtering is applied to the outputs to obtain the band-limited noise and distortions. All the results are calculated based on the FFT spectrum. Tab. 6-2 shows the comparison between the input and the TIA's output.

[6] The control codes are programmed into the EEPROM chip on the FPGA evaluation board, which avoids the FPGA-PC connection. By far there have been two ground connections in the system. One is the FPGA-oscilloscope ground connection, which is intentionally the only ground-defining point. Another is the signal source-ground connection, which is due to the low impedance between the signal source's floating chassis and ground. The latter is difficult to eliminate.

Table 6-2 Signal property comparison

between the input of test-use transconductor and the output of TIA

Condition	Signal source[3]	Signal source +test-use driver +test-use TIA
SNR/dB (0-100MHz)	43.54	38.81
THD/dB (to 7th order distortion)	47.68	55.48

From Tab.6-2 we find

- SNR decreases after the signal passes the transconductor and the test-use TIA. This 5 dB drop is mainly caused by the slight peaking at 40MHz in TIA's transfer function, as shown in Fig. 6-11. This peaking is due to parasitic capacitance at the TIA's input, which causes low phase margin of TIA's loop gain. In the following measurements with cable connected, the peaking is found to be alleviated by RX TIA's resistive input loading caused by the cable's transmission line effect.
- THD increases after the signal goes through the transconductor and the test-use TIA. By comparing the spectrum of input and output signal, the 3rd and 7th order distortions are suppressed. By far there has not been a reasonable explanation to this phenomenon.

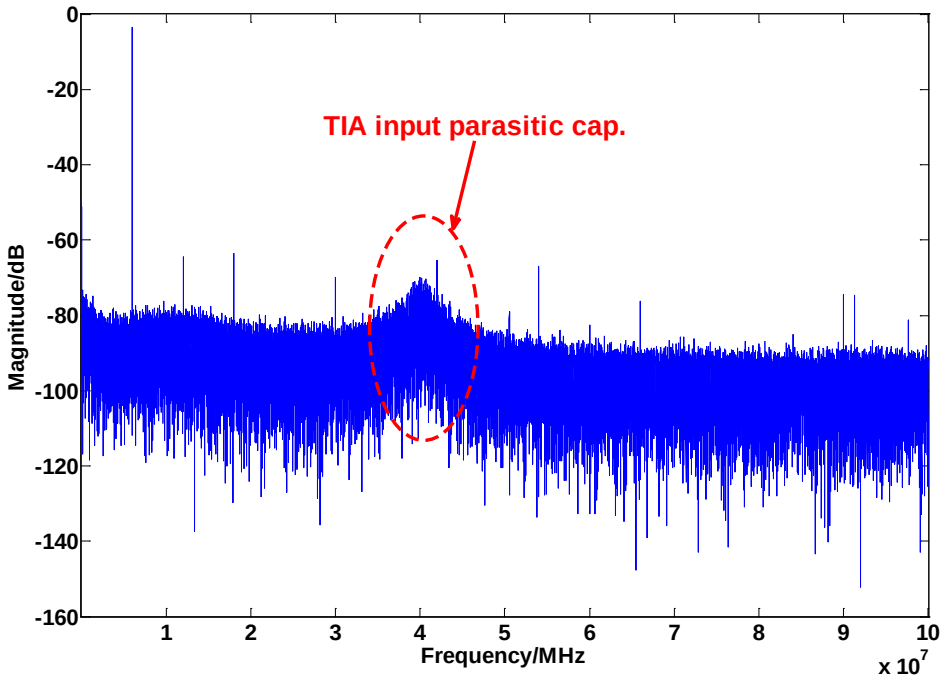


Figure 6-11 Spectrum of the TIA's output in TX driver test

[3] For the signal source measurement, SNR is limited by the oscilloscope [6.4], while THD is limited by the signal source [6.5].

Propagation Delay Measurement

To order to verify the cable model presented in Chapter 2 in a simple way, the propagation delay and attenuation have been measured. A 6 MHz sinusoidal signal is generated with the same equipment as described in Section 2.1.1. The cable adapter is connected to the signal source and an oscilloscope directly, with 50 Ω termination at both ports. Fig. 6-12 and Fig. 6-13 show, respectively, the measured and calculated propagation delay/attenuation when signal passes through the cable adapter. The measured attenuation is in good agreement with the calculation. There is 2.3ns delay difference, which can be attributed to the adapter-oscilloscope connection.

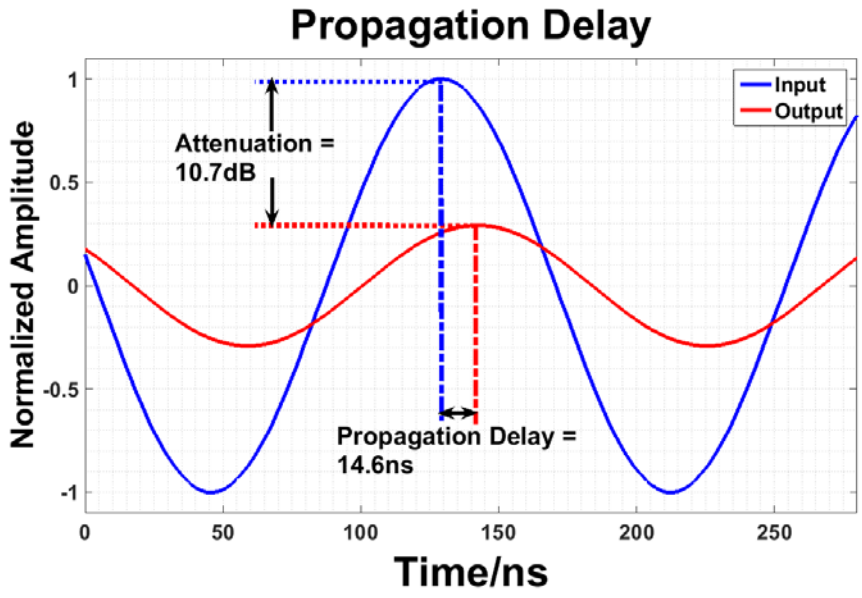


Figure 6-12 Measured propagation delay and attenuation of the cable

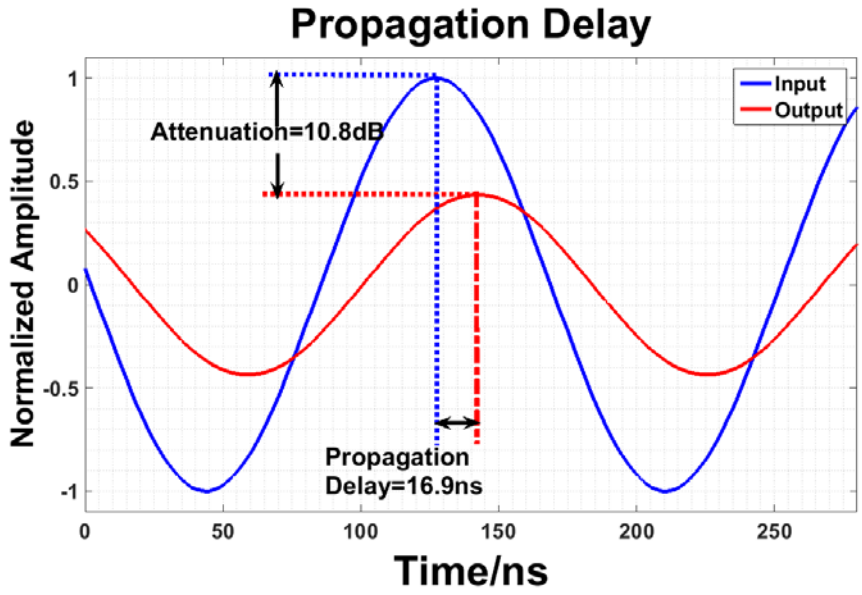


Figure 6-13 Calculated propagation delay and delay of the cable

SNR and THD without equalization

In order to determine SNR and THD without equalization, the TX is switched to normal mode, input signals are fed to the four TX drivers and the TIA's output is sampled by the oscilloscope. Note that the signal power should be integrated within the first Nyquist band of the sampling frequency, which is DC to 50MHz in our case. As discussed in Chapter 2, there will be 4 tones in the output spectrum--even for only one input signal, as shown in Fig. 6-14, since each driver in the TX runs at a sampling frequency of 25 MHz.

Also as has been explained in Chapter 2, depending on the phases of the 4 input signals, some of the tones may shrink or even vanish, which is observed in the measurement shown in Fig. 6-15. This makes it difficult to define the SNR/THD of the system. To makes things clear, we show the SNR and THD in several special cases in Fig. 6-15.

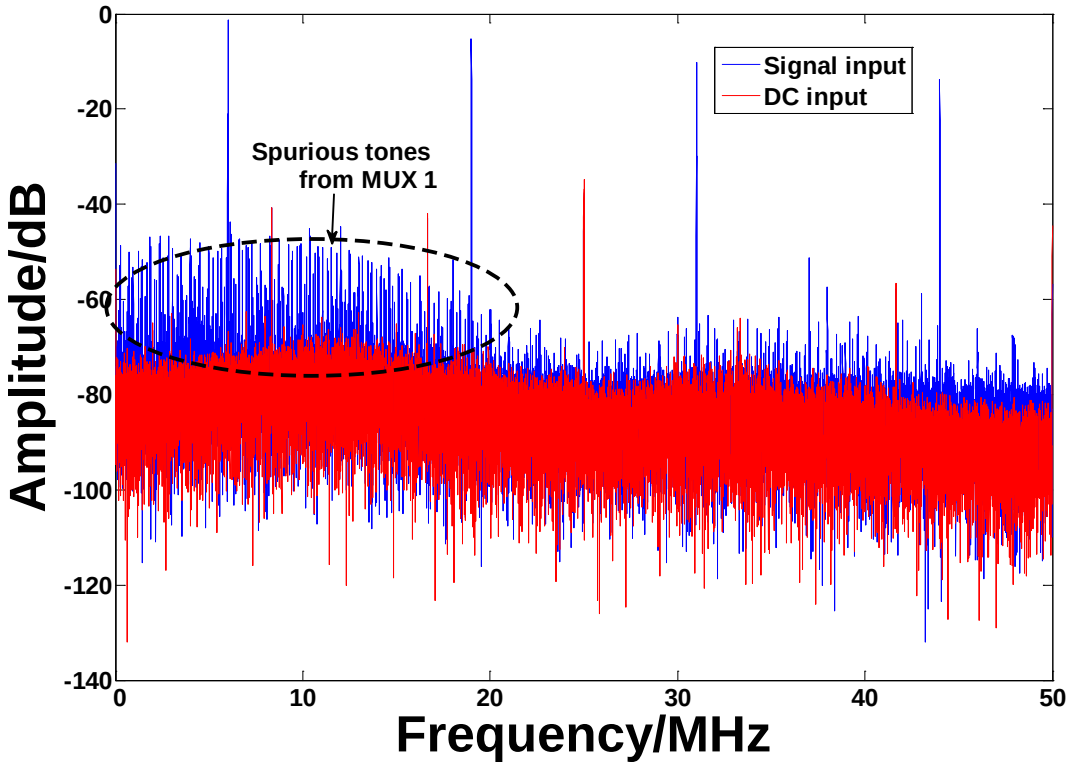


Figure 6-14 Signal spectrum without equalization (one input case)

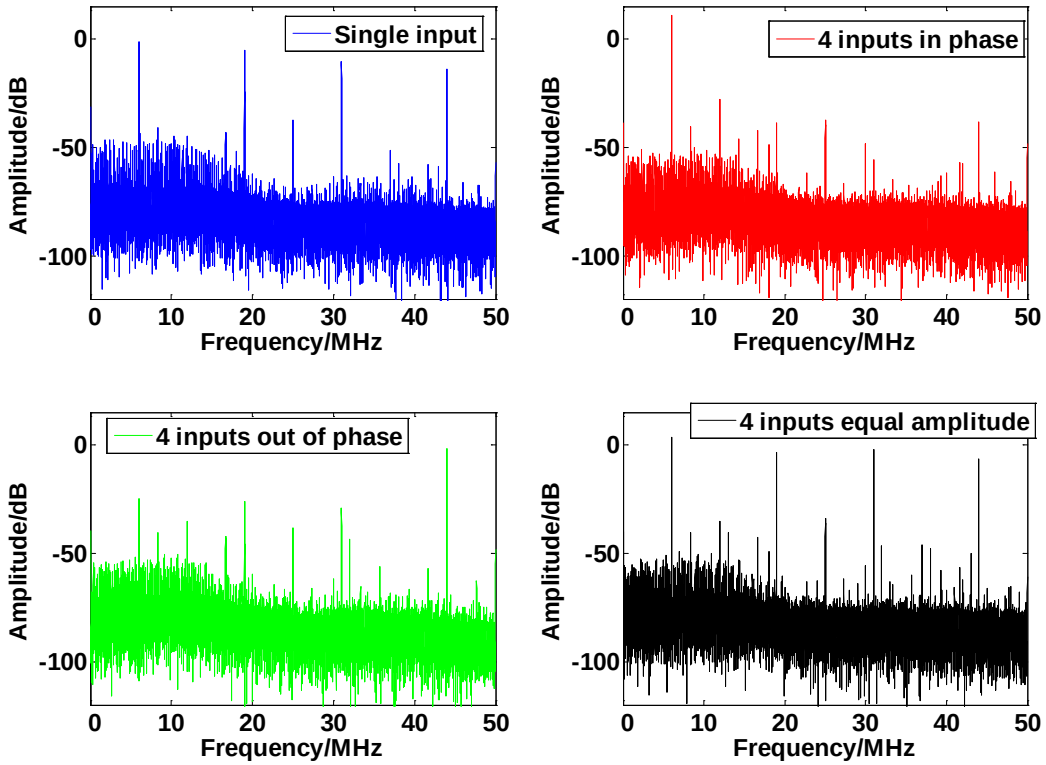


Figure 6-15 Output spectrum with different phase combinations[4]

i SNR Calculation

Before calculation some unwanted tones should be clarified and removed. Some unwanted spurious tones appear at low frequencies, as is shown in the blue curve in Fig. 6-14. The possible reason for this is that these tones are introduced by MUX 1, since they disappear in DC mode in which only MUX2 is active. Since MUX 1 is always active in normal mode, the spurious tones cannot be avoided during equalization, which limits the characterization of the system. Besides those tones, in the spectrum of Fig. 6-14 there are also clock-related tones, which can be removed before carrying out SNR calculation.

In order to investigate the system's noise performance in the presence of these unwanted tones, SNR is calculated in two ways. One way is by integrating noise PSD in normal mode, from DC to 50MHz. Then the resulted SNR is termed as $SNR_{normal\ mode}$:

[4] In the fourth subplot, "equal amplitude" means the efforts are paid to make 4 tones on the spectrum own the equal amplitude. One example of such an arrangement is to try to achieve 0, 0, $\pi/4$ and $3\pi/4$ relative phase delay at the signal generators.

$$SNR_{normal\ mode} = \frac{Signal\ power\ in\ normal\ mode}{Noise\ power\ in\ normal\ mode} \qquad (6-1)$$

Another way of noise power calculation is by integrating noise PSD obtained in DC mode, while signal power is still obtained from the result in normal mode. This method defines $SNR_{DC\ mode}$ as

$$SNR_{\ DC\ mode} = \frac{Signal\ power\ in\ normal\ mode}{Noise\ power\ in\ DC\ mode} \qquad (6-2)$$

By a comparison between $SNR_{normal\ mode}$ and $SNR_{DC\ mode}$, we can have estimation about the impact of the spurious tones. The result is shown in Tab. 6-3. From it we find the spurious tones cause about 5~10dB SNR degradation in different cases, which indicates that those tones indeed negatively affect the system's performance.

Table 6-3 SNR measurement

Case	SNR in Normal mode/dB	SNR in DC mode/dB
Single input	29.3	38.0
"in phase"	42.6	48.2
"out of phase"	30.8	35.6
"equal amplitude"	37.4	42.8

ii THD Calculation

Distortion can originate from the both TX and RX.

If distortion occurs in the TX, due to its sample and hold nature, there will be several images extending within the RX's Nyquist interval, as shown in Fig. 6-16. In the THD calculation, all these distortions are taken into account.

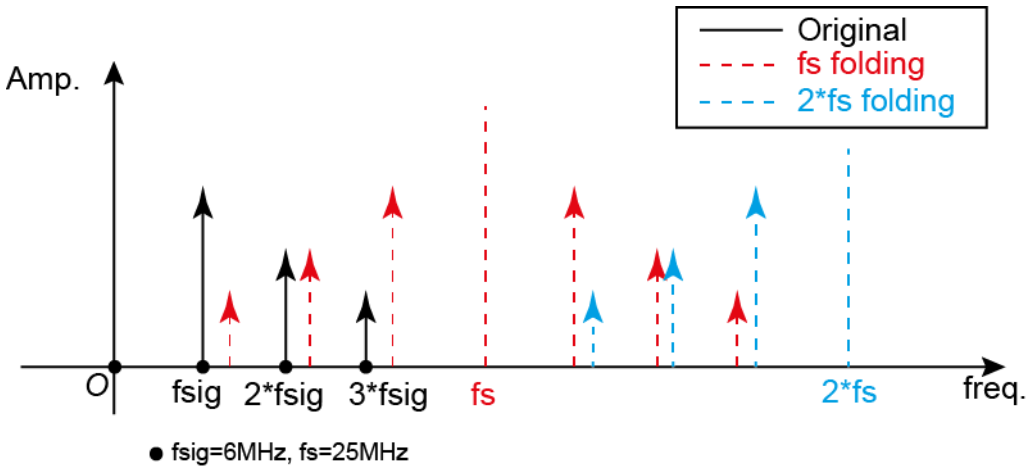


Figure 6-16 TX distortion

At the same time, the RX circuitry (TIA and extra gain stage) also contributes nonlinearity, which we will refer to as RX distortion. It means that even if there is no TX distortion, the four signal tones in the RX's Nyquist interval still introduce distortion at the output of the RX, as shown in Fig. 6-17. In RX distortion the mapping between the fundamental tones and distortions are tabulated in Tab. 6-4.

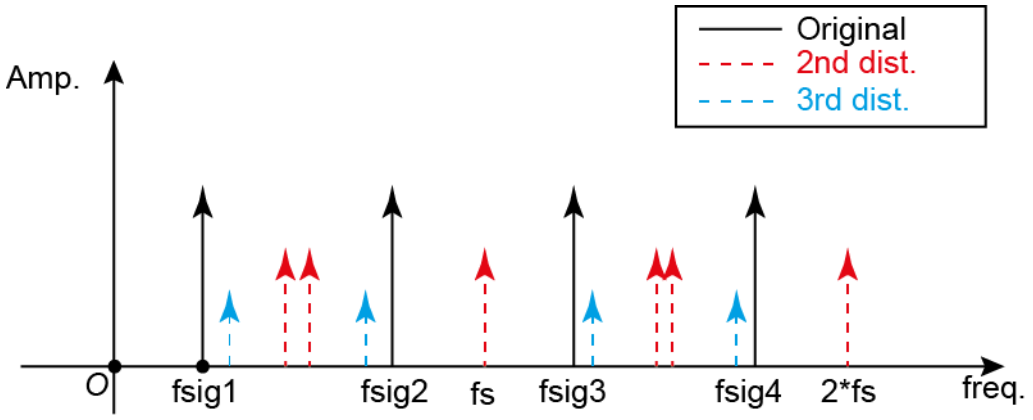


Figure 6-17 RX distortion

Table 6-4 RX distortion look-up table

RX distortion		Tones in Nyquist band (MHz)	
Fundamental tones	*fsig1*	6	
	fsig2	19	
	fsig3	31	
	fsig4	44	
2^{nd} order distortion	2**fsig1*	12	
	2**fsig2*	38	
	2**fsig3*	12	
	2**fsig4*	12	
	fsig1± *fsig2*	25	13

	fsig1± *fsig3*	37	25
	fsig1± *fsig4*	38	50
	fsig2± *fsig3*	50	12
	fsig2± *fsig4*	13	25
	fsig3± *fsig4*	25	13
3rd order distortion	3* *fsig1*	18	
	3* *fsig2*	7	
	3* *fsig3*	43	
	3* *fsig4*	32	
	2* *fsig1*± *fsig2*	7	31
	2* *fsig1*± *fsig3*	43	19
	2* *fsig1*± *fsig4*	6	32
	2* *fsig2*± *fsig1*	32	44
	2* *fsig2*± *fsig3*	7	19
	2* *fsig2*± *fsig4*	6	32
	2* *fsig3*± *fsig1*	6	18
	2* *fsig3*± *fsig2*	31	43
	2* *fsig3*± *fsig4*	6	18
	2* *fsig4*± *fsig1*	6	32
	2* *fsig4*± *fsig2*	7	19
	2* *fsig4*± *fsig3*	7	19

There is a difference between TX and RX distortion. TX distortion is brought about by the nonlinearity of the TX drivers. If the channel is assumed to be linear, then after equalization, those distortions can only be observed at the corresponding equalized and demultiplexed output, without any crosstalk to other users. RX distortion, in contrast, is equivalent to a non-linear channel. Even an input signal or a TX driver is distortion-free, distortions will be observed at the corresponding equalized and demultiplexed output. Moreover, since the employed equalization algorithm is only aimed at cancelling the linear error such as finite bandwidth and nonuniform phase delay, the crosstalk caused by nonlinearity will still stay in the final output.

Tab. 6-5 summarizes the measured distortion in the difference cases shown in Fig. 6-15. These results contain both TX and RX distortion. This difference between TX and RX distortion will become obvious in the measurement results presented in the following measurement.

Table 6-5 Distortion measurement

THD/dB (to 3rd dist.)	Normal mode
Single input	40.7
“in phase”	39.0
“out of phase”	33.0
“equal amplitude”	38.8

6.2.2 Measurements with Equalization

In order to characterize the system's performance with equalization, the measurement flow shown in Fig. 6-18 is adopted, with step-by-step results shown in the following subsections.

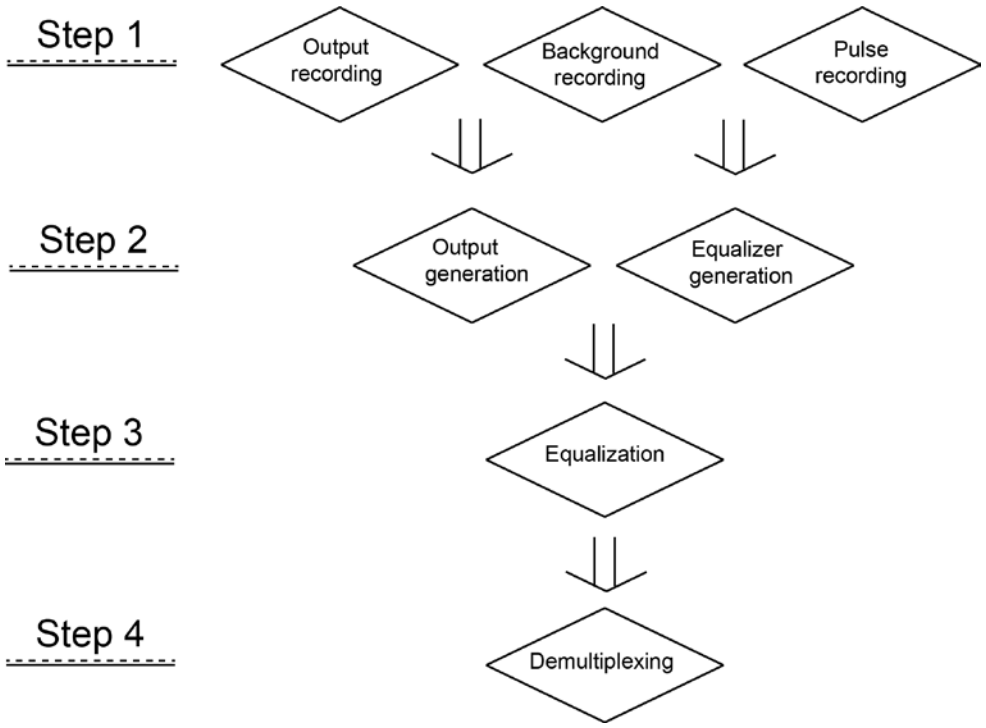


Figure 6-18 Measurement flow with equalization

Background Pattern

As shown in Chapter 5, there will be current spikes at the TX output during driver switching, which appear with a frequency of $4*f_s$. However, due to the variation of clock dividing control and transconductance mismatch in different drivers, the spikes will exhibit a pattern at with lower frequency f_s, namely the cycling speed of four drivers in TX. Besides that, the mismatch between 3 sampling capacitors, and the periodic timing control of the sampling moments also contributes to repeated spike variation, of which the frequency is $f_s/3$. The effects of all these spike variation sources can be observed in the measurement results shown in Fig. 6-19. This background pattern is recorded and subtracted from the subsequent measurements to reduce its impact on equalization.

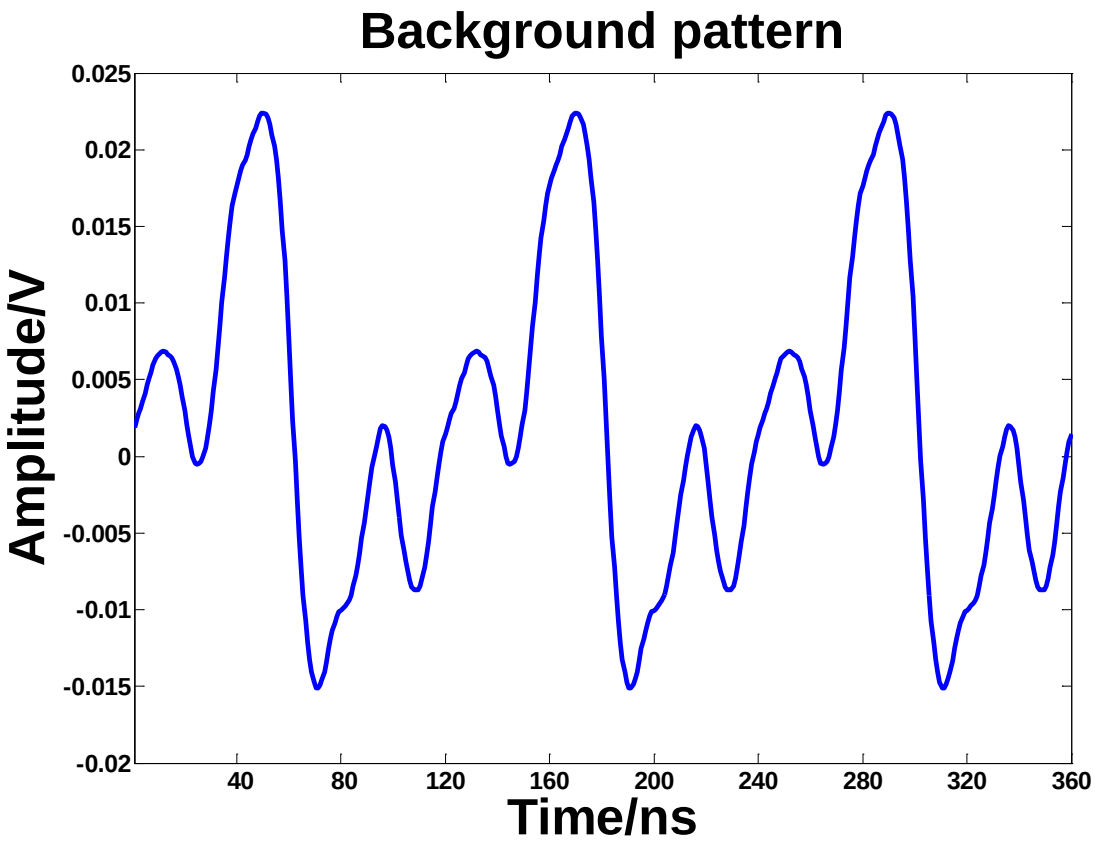


Figure 6-19 Background pattern

(sampled at 1.25GS/s with 1024-cycle averaging)

Channel Response

In order to obtain the equalizer's coefficients, the pulse generation mode is activated to generate a pulse of 10ns and thus the channel's transient pulse response is captured by using the oscilloscope. For comparison, the measured and calculated responses are both plotted in Fig. 6-20. From it we find that the measurement result agrees well with the calculated response, which validates both the cable modelling and the system modelling, as described in Chapter 2 and 4.

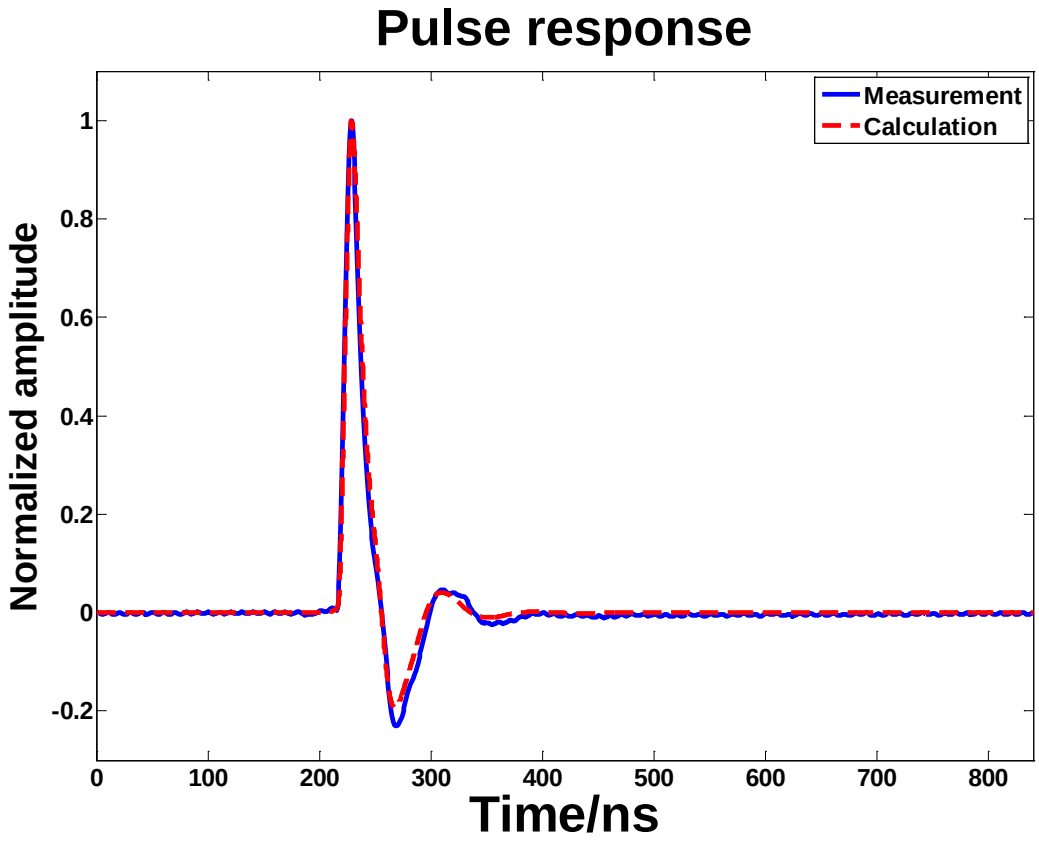


Figure 6-20 Measured and calculated pulse response

(sampled at 1.25GS/s with 1024 cycles averaging)

A side product of pulse response measurement is that the channel can be characterized in the frequency domain as well. Suppose a train of periodic pulses is fed into one TX driver, then, in the frequency domain, the output of the RX can be translated as pulse sampling of the channel response. Such a result is shown in Fig. 6-21.

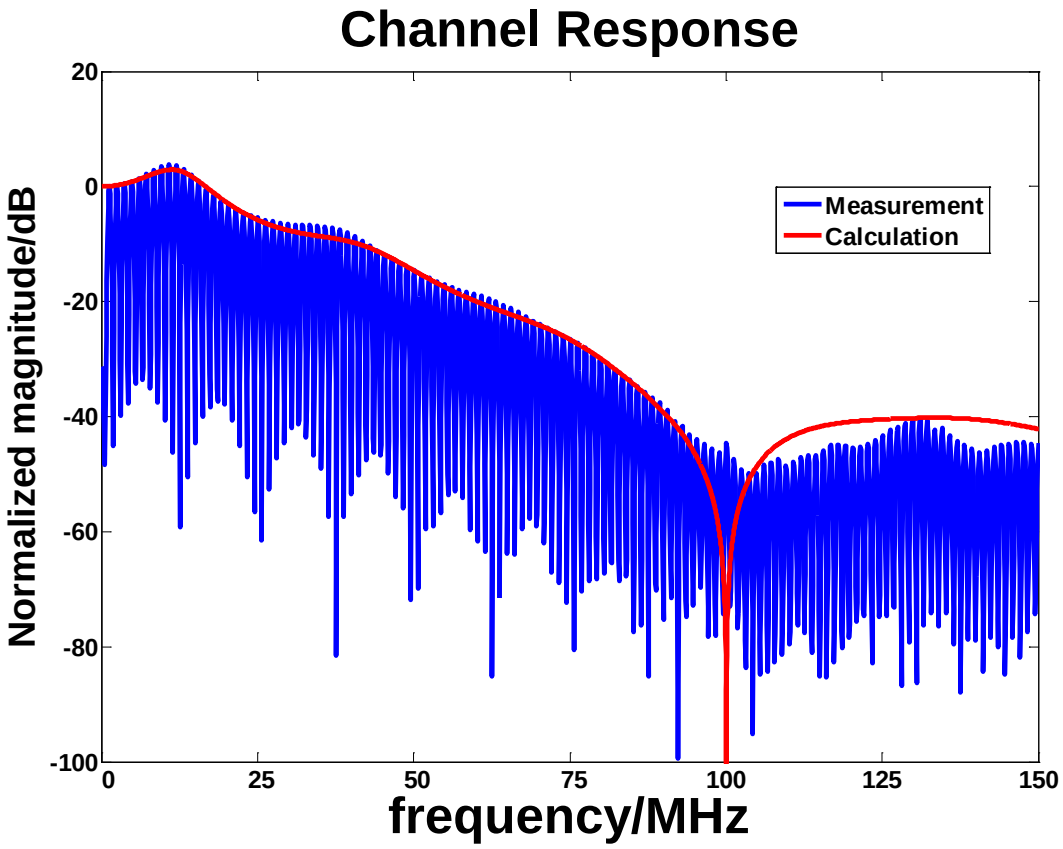


Figure 6-21 Channel characterization in frequency domain

(from the TX output to the RX output,

1024-cycle averaging with high-resolution mode off)

From Fig. 6-21 again we find a good agreement between measurement and calculation. However, in measurement the notch around 100MHz is blurred compared with the calculation result. This may be attributed to the following reasons:

- The width of TX output pulse is slightly differs from 1/(4*fs).
- The notch is shifted due to the channel's nonlinearity.

Both of these effects can contribute to unwanted crosstalk between different output channels. For details please refer to Appendix E.

Equalizer's Coefficients

With the background pattern and the pulse response captured, all the ingredients for equalization are ready. Fig. 6-22 shows the sampled pulse response, in which the input pulse is fed onto a fixed sampling capacitor in one driver.

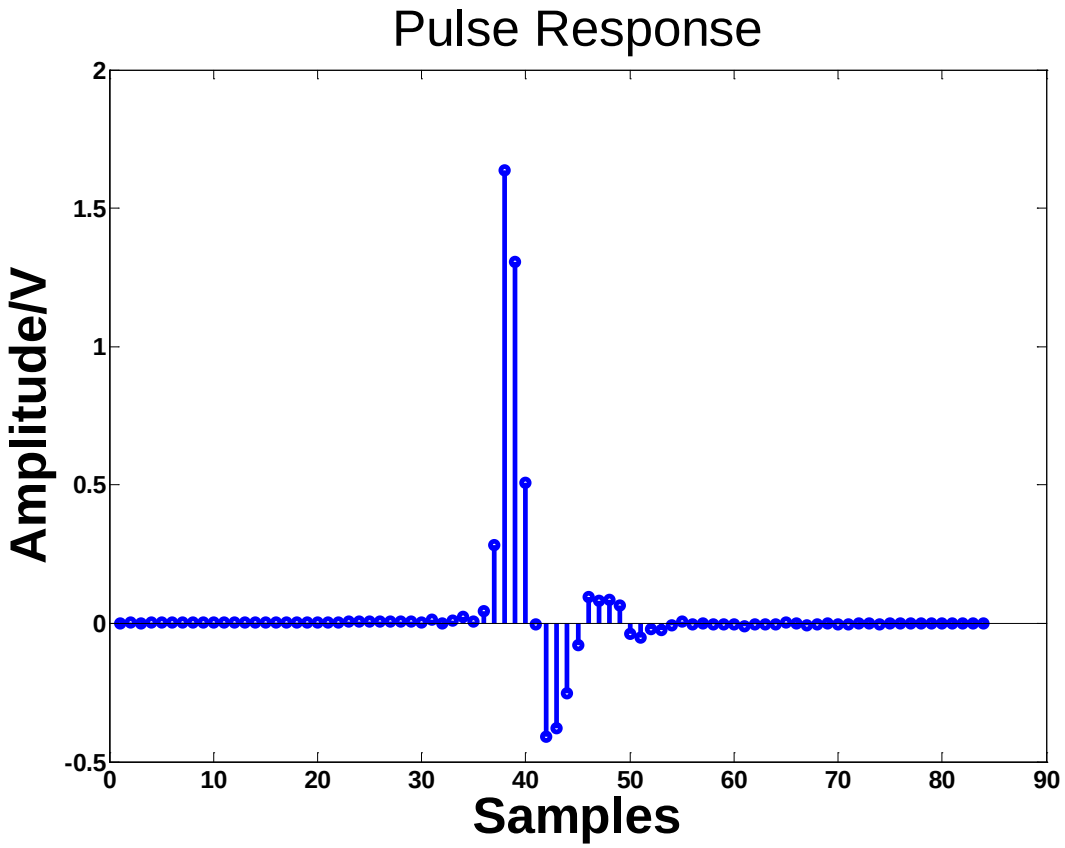


Figure 6-22 Sampled pulse response

(sampled at 100MS/s after 1024-cycle averaging and 100MHz sinc filtering)

Fig. 6-23 shows the calculated zero-forcing equalizer's coefficients. Fig. 6-24 shows the combined response, where non-zero terms are forced to zero with only one impulse left.

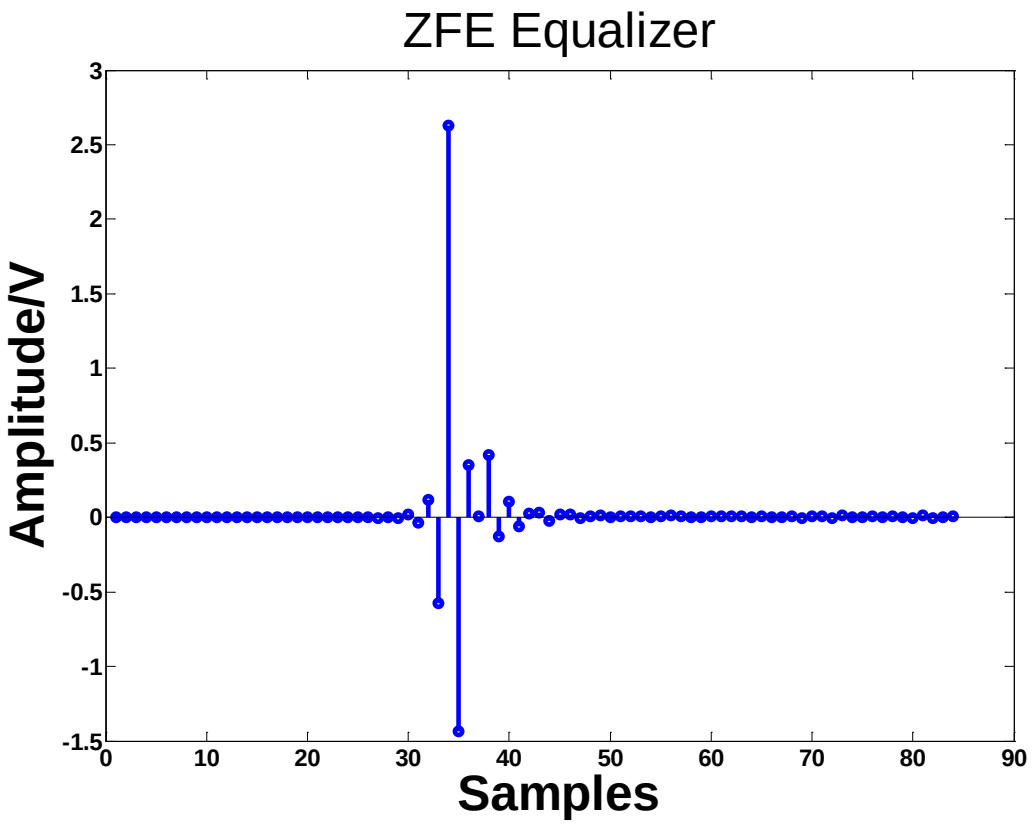


Figure 6-23 ZFE equalization

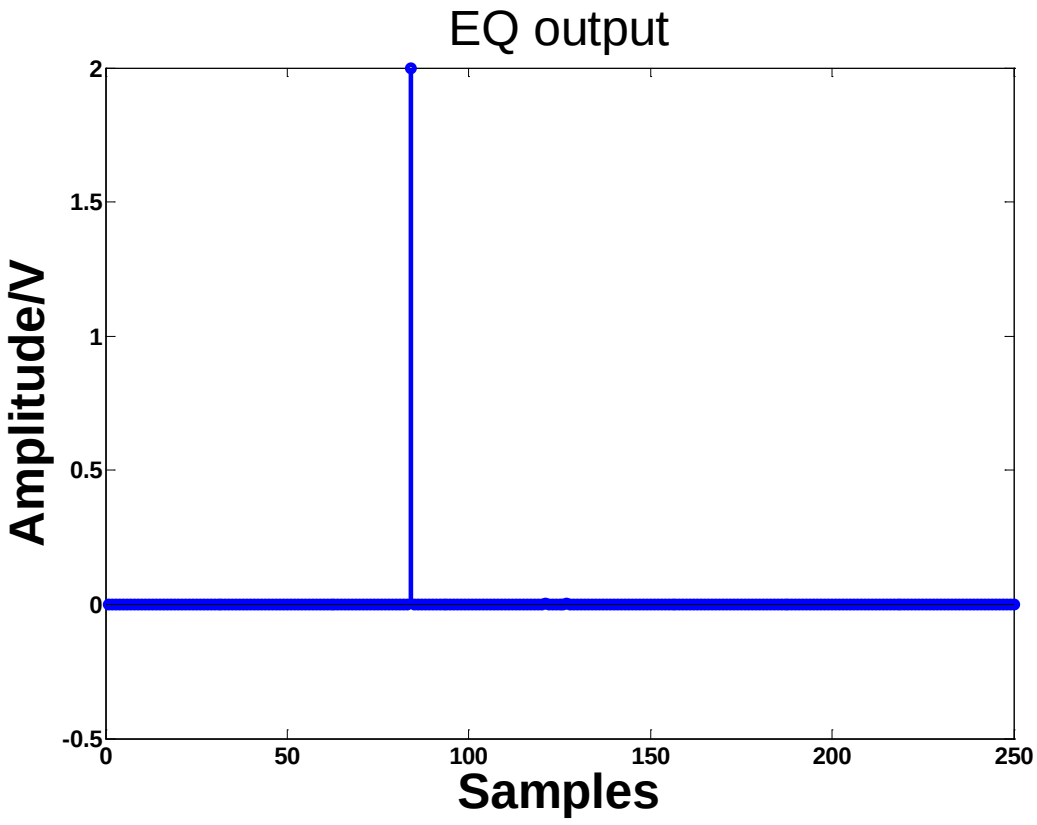


Figure 6-24 Combined response

Single-Driver Equalization

As the first measurement with equalization employed, a 6MHz sinusoidal input signal is fed into only one driver in TX. The sampled outputs of RX, which are the inputs to the equalizer, are plotted in Fig. 6-25. Not surprisingly, if this output is demultiplexed directly, the crosstalk between the different receivers is obvious, as shown in Fig. 6-26.

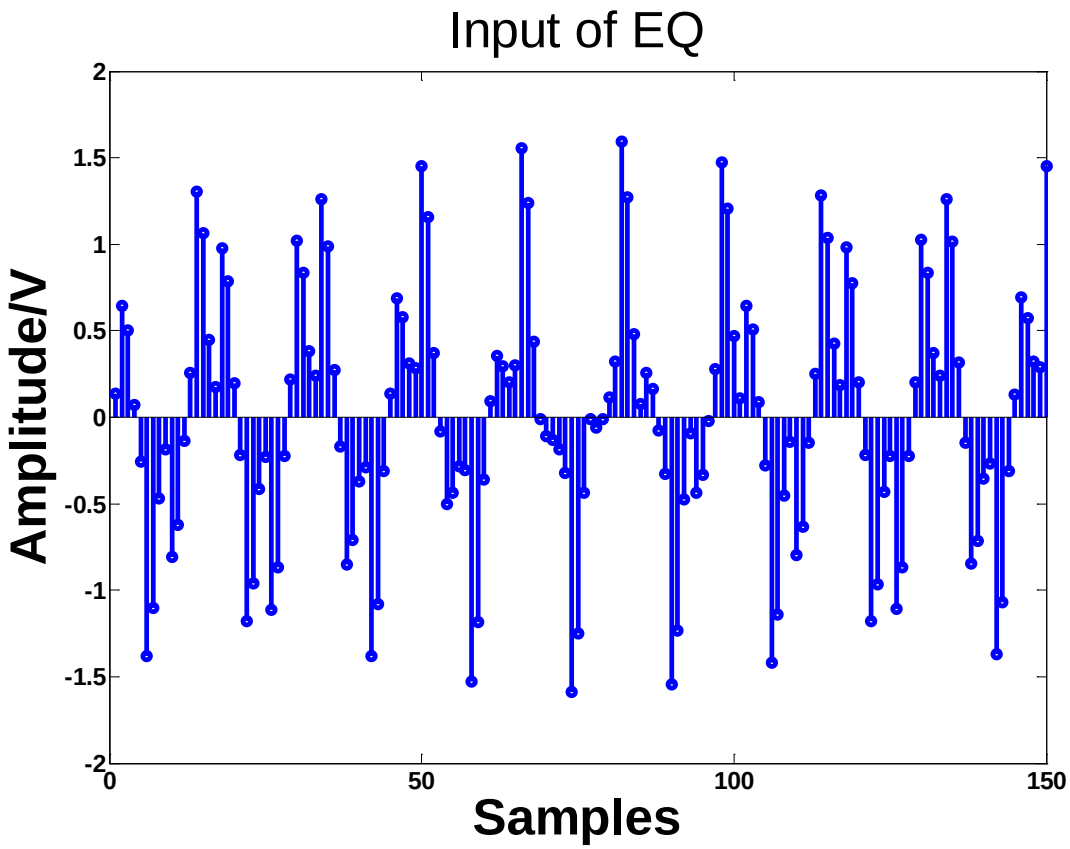


Figure 6-25 Input of equalizer

(100Ms/S sampling with 100MHz sinc filtering)

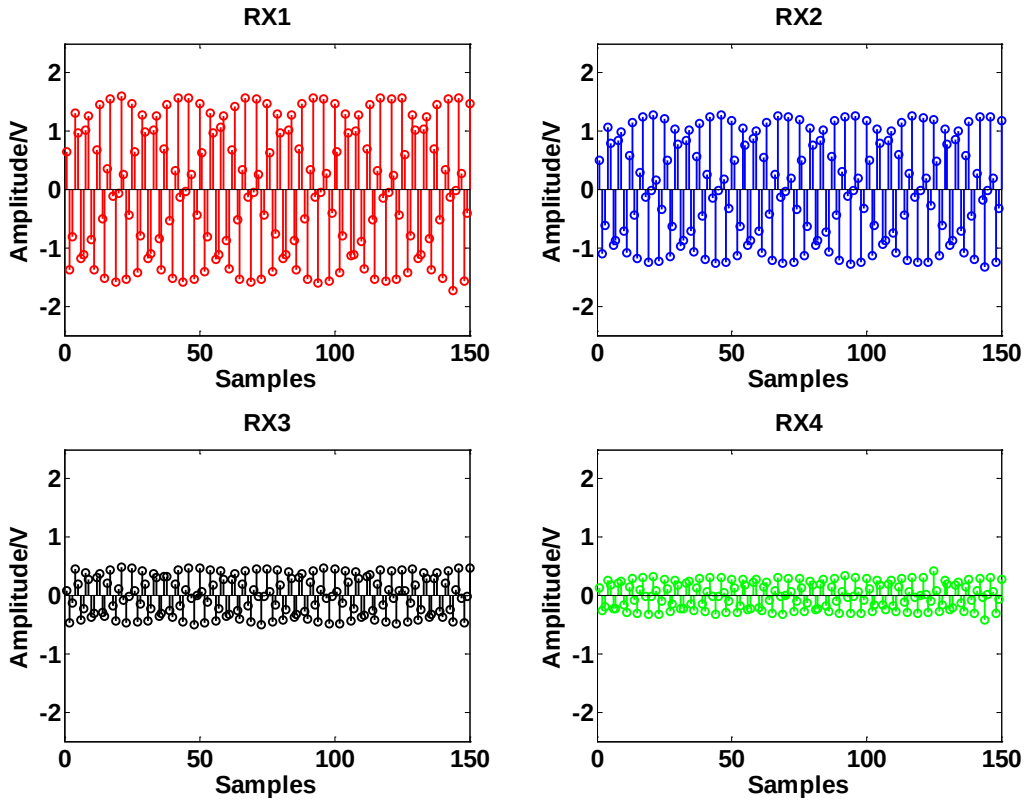


Figure 6-26 Demultiplexed output without equalization

Fig. 6-27 shows the demultiplexed result after equalization. Compared with Fig. 6-26, the signal from one driver is clearly resolved and delivered to one output. The FFTs of signals delivered to all the outputs are plotted in Fig. 6-28, where 2nd distortion and 3rd distortion are located at 12MHz, 7MHz, respectively. Besides these two, there are also several other tones, which are listed in Table 6.6 with descriptions.

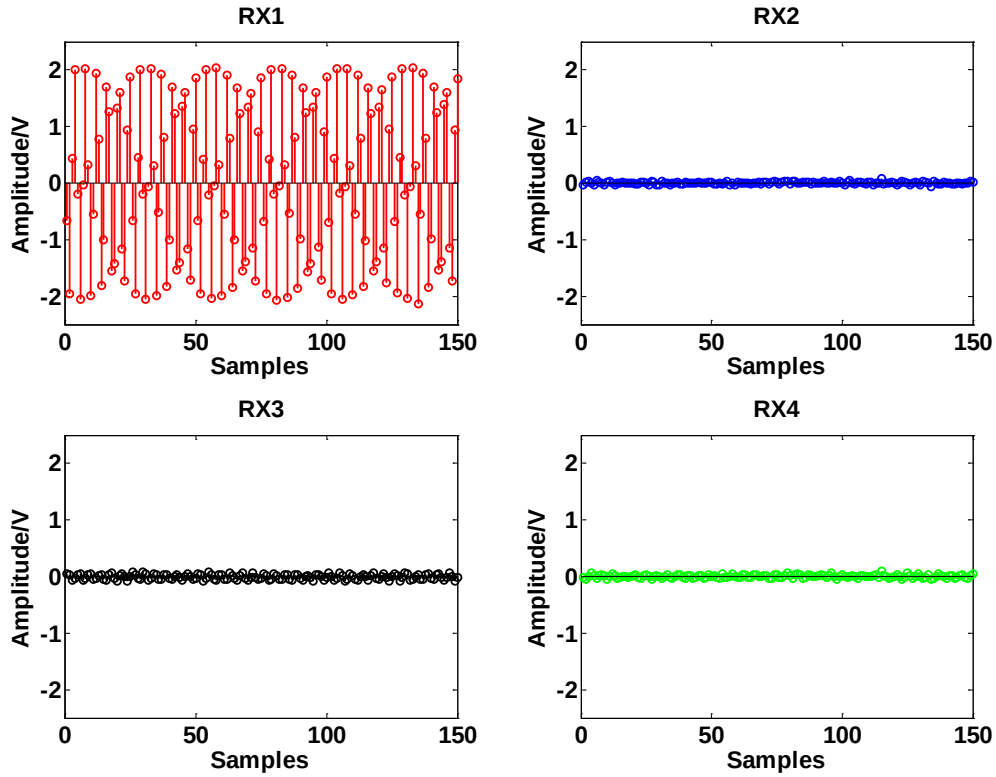


Figure 6-27 Demultiplexing after equalization

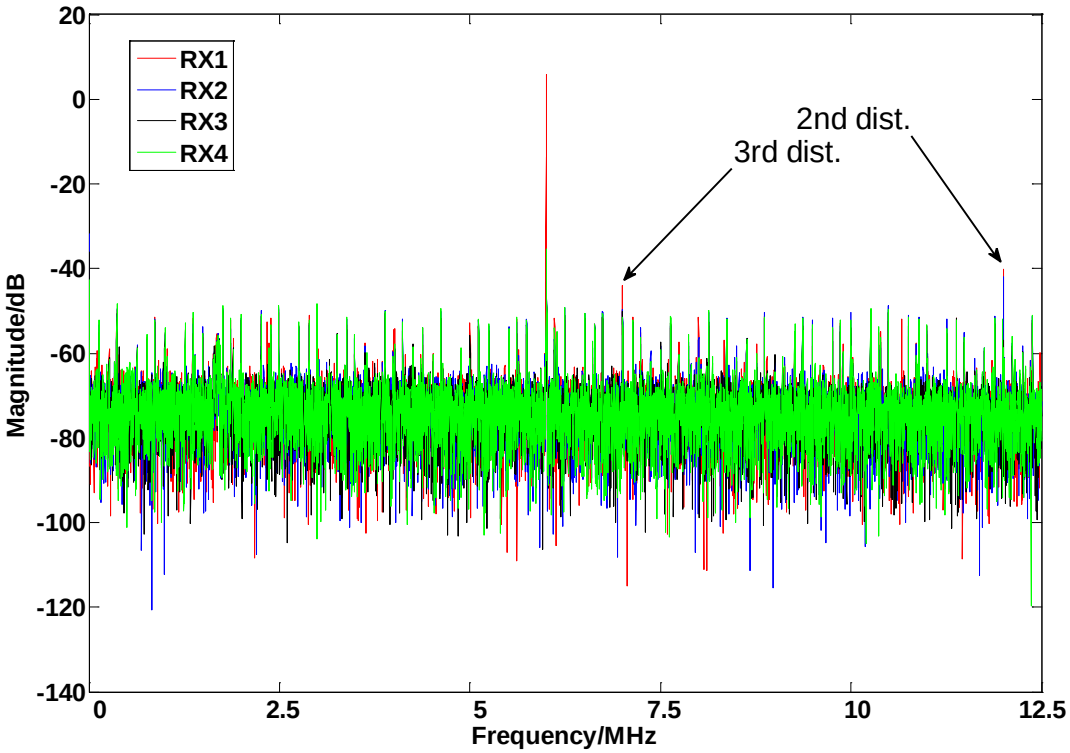


Figure 6-28 FFT of demultiplexed signal after equalization

Table 6-6 Tones in the FFT of each receiver's output

Tones (MHz)	Descriptions
12	2nd distortion
7	3rd distortion
8.3	Sampling control (=*fs*/3)
2.3	Capacitor mismatch induced (=*fs*/3-*fsig*)
10.6	Capacitor mismatch induced (=2**fs*/3-*fsig*)

i Crosstalk Evaluation

Also from Fig. 6-28 we can analyse the crosstalk after equalization. From the combined response after EQ we can calculate that the crosstalk between "users" is expected to be at most -51dB (Appendix E). However, Fig. 6-25 and the zoom-in figure, Fig. 6-29, show the crosstalk which is much higher than this value. Such a deviation might be caused by the following:

- Mismatch between the on-chip resistors that define the transconductances of the drivers.
- In pulse generation mode, residual pulses are generated at the input of multiple drivers other than the target one.
- In normal mode, signals are carried by the pulses of different widths than those in pulse generation mode.
- RX distortion makes the pulse nonlinear in pulse generation mode, which forms a nonlinear "ruler" during equalization.

The first possibility can be easily excluded by the mismatch measurement result shown in Appendix F. As for the rest, all of them can be supported by the simulation and partial measurement results. Among them the RX distortion is the major suspect. The details of this analysis are included in Appendix E.

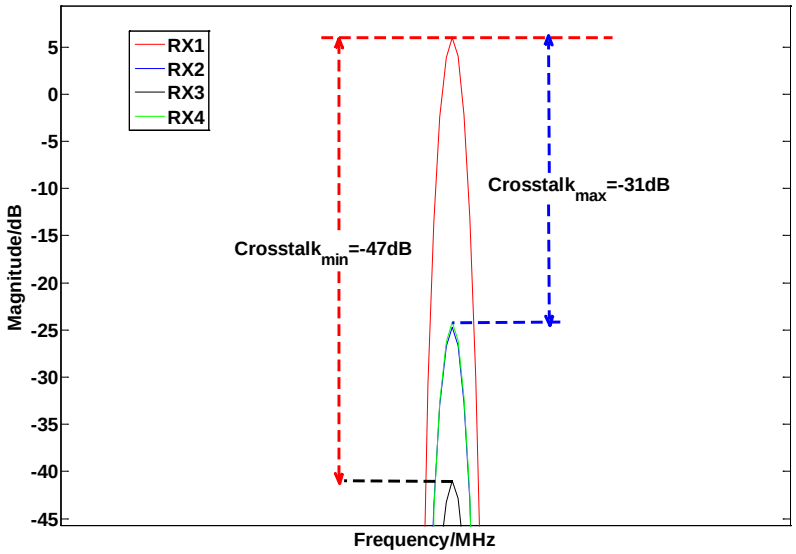


Figure 6-29 Zoom-in of Fig. 6-25 showing crosstalk at the signal frequency

ii SNR and THD Evaluation

The SNR results before and after equalization are tabulated in Tab. 6-7.

Table 6-7 SNR before and after equalization

(single-driver test, noise integrated between DC to 50MHz)

	Normal mode, before EQ	Measurement, after EQ
SNR/dB	29.3	31.1

From this we find SNR after EQ increases by about 2dB compared with SNR before EQ, which seems to be against the basic principle of ZF equalization described in Chapter 4. This abnormal behaviour can be explained by the fact that, by the use of equalization, the weight of the low local SNR region (the low-frequency region with spurious tones in Fig. 6-14) is suppressed, and that of the high SNR region (the high-frequency region with clean noise floor) is emphasised.

Tab. 6.8 shows a comparison of linearity before and after equalization.

Table 6-8 THD before and after equalization

THD/dB (to 3rd dist.)	Normal mode, before EQ	Measurement, after EQ
Single input	40.7	42.3

Tab. 6.8 shows that the THD is improved after equalization, which can also be explained by the high-frequency signal enhancement due to equalization as explained above. However, due to the difference between TX and RX distortion explained in section 3.3b, the TX distortion associated with a particular TX driver will be recollected at the corresponding output of the demultiplexer, while the RX distortion spreads among all the outputs. The THD result in Tab.6.8 does not only include all the TX distortions from its corresponding driver, but also partial contributions made by RX distortion (Appendix F). If the latter becomes dominant, the THD after equalization becomes difficult to predict.

Two-driver Equalization

In this measurement, two sinusoidal signals with 5.8MHz and 6MHz are separately sent to two TX drivers. In the implementation of the equalization algorithm, the transconductance and capacitance mismatch are ignored for simplicity at the moment. Fig. 6-30 shows the result of demultiplexing without equalization, and Fig. 6-31 shows the result with equalization.

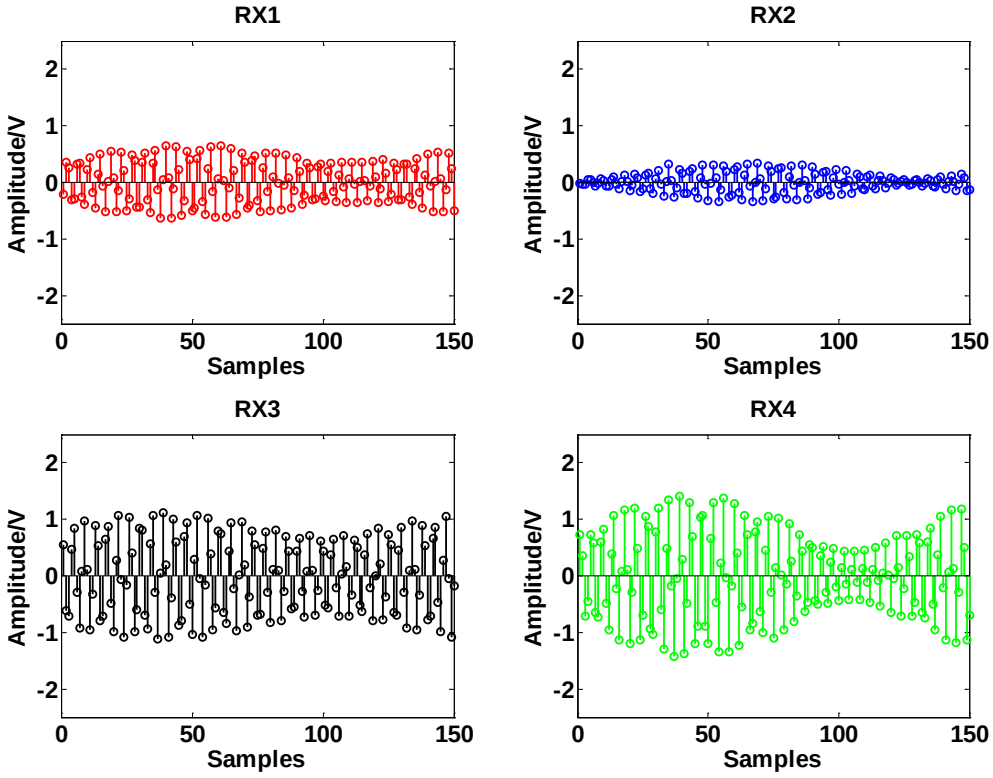


Figure 6-30 Demultiplexed output without equalization

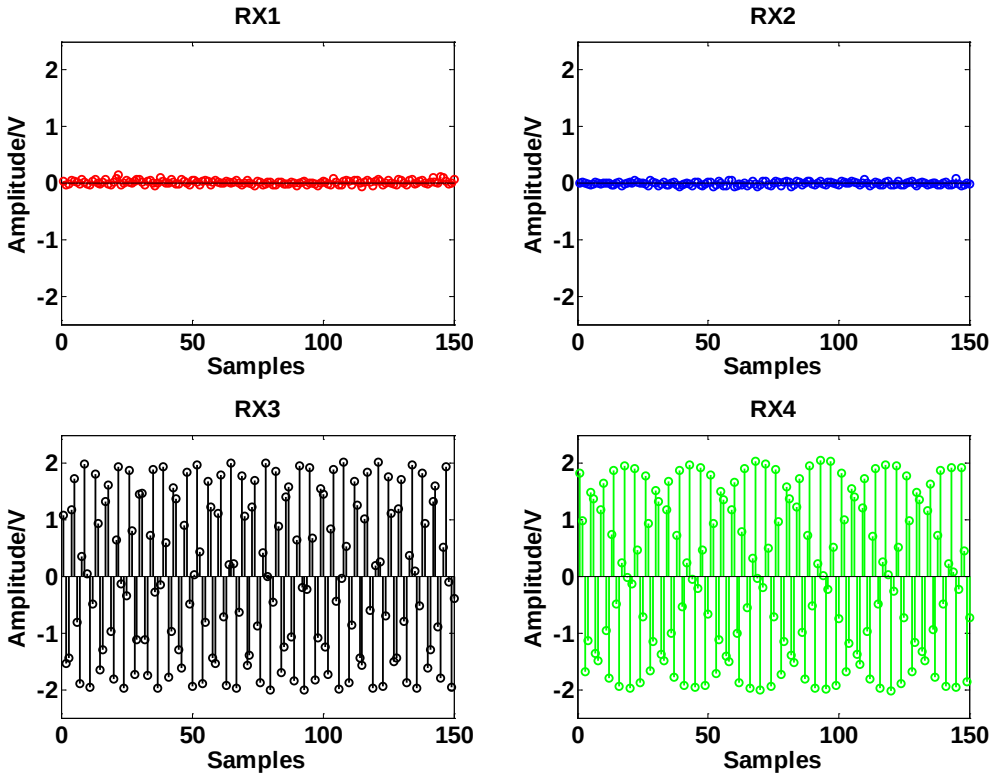


Figure 6-31 Demultiplexing after equalization

Fig.6.32 shows FFTs of the demultiplexed results after equalization. Here we can clearly see intermodulation distortion tones located at 0.2MHz(=6M-5.8M Hz) and 11.6 MHz (=6M+5.8M Hz), which reflect RX distortion. From the common relationship between 2nd order intermodulation distortion (IMD2) and 2nd order harmonic distortion (HD2) [6.6],

$$IM2 = 2 \cdot HD2 \qquad (6-3)$$

We can get a rough estimation of 2nd order harmonic distortion of at the RX side, which is -54dB at 6MHz.

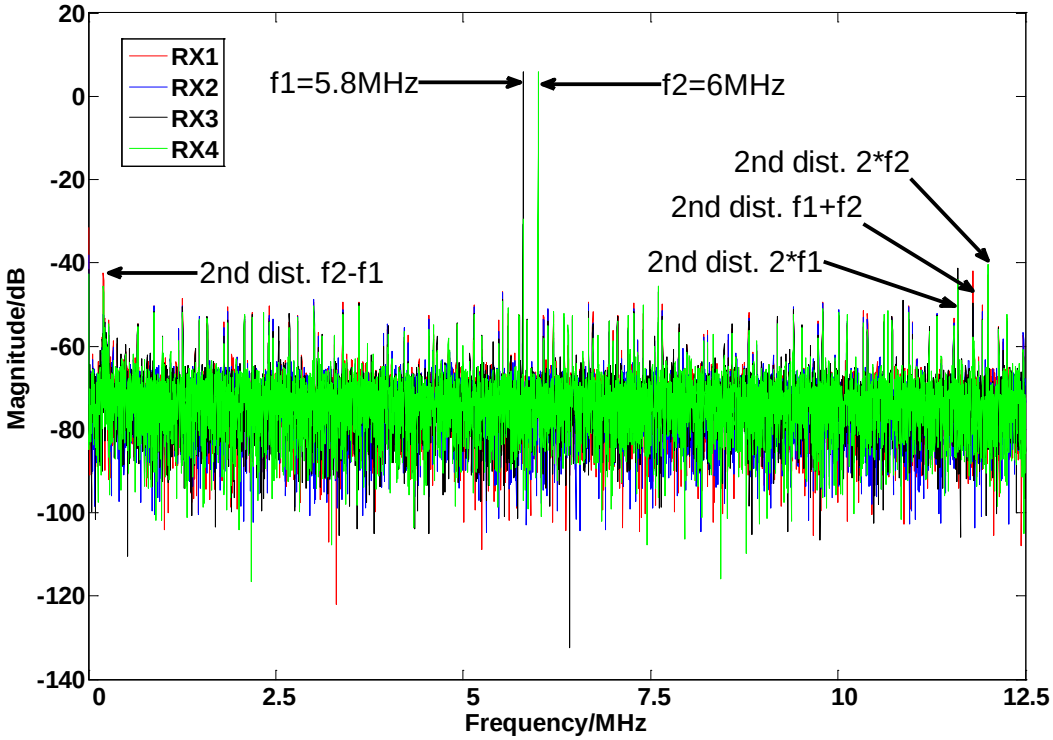


Figure 6-32 FFT of demultiplexed result after equalization

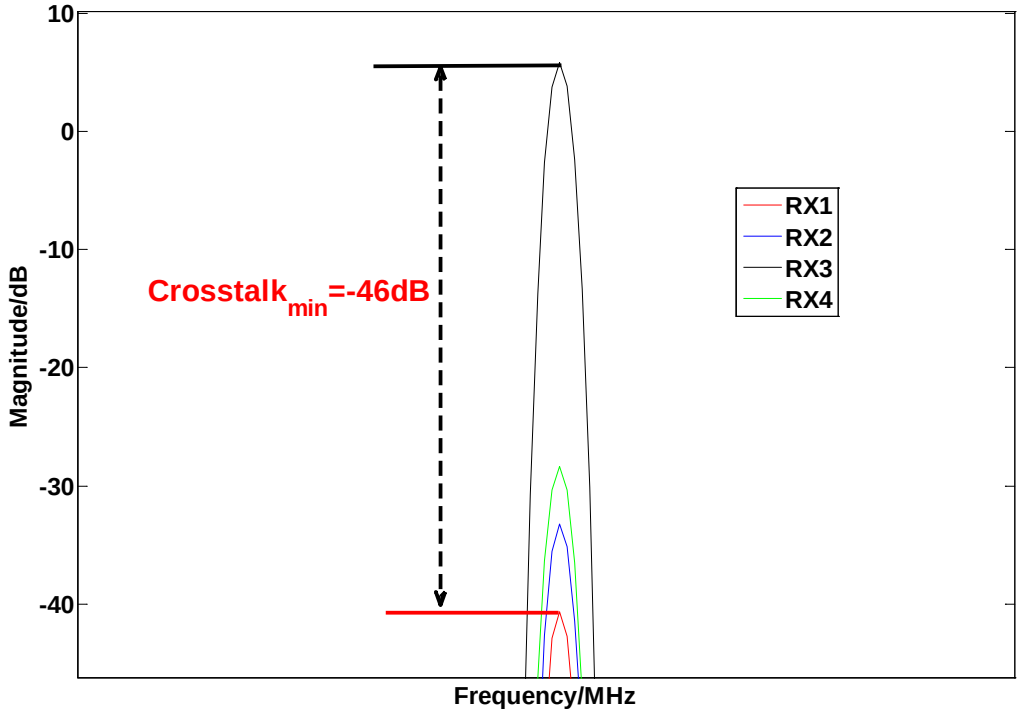


Figure 6-33 Crosstalk measurement in two-driver test

From the minimum crosstalk shown in Fig.6-33, we find it does sit below the upper limit set by the transconductance mismatch, which is described in Appendix F.

All-driver Equalization

i Test with Different Signals

In order to completely test the system's functionality, 4 different signals are fed into the all the four drivers in TX separately. The mapping between signal sources and drivers is listed in Tab. 6-9.

Table 6-9 Different signals used in all-driver test

Driver	Description	properties
1	Gaussian	1MHz period, 200mV peak-to-peak
2	Sinusoidal	
3	Rectangular pulse	
4	Exponential rising	

Fig. 6-34 shows a demultiplexed result without equalization. Its counterpart, the result after equalization, is plotted in Fig. 6-35. For fair comparison an equalized result with the identical signal individually fed to all drivers is also shown as black dotted line in the same figure, which can be considered as the best performance that the system can achieve. By the comparison we find the differences between simultaneous and individual feeding-in are very small.

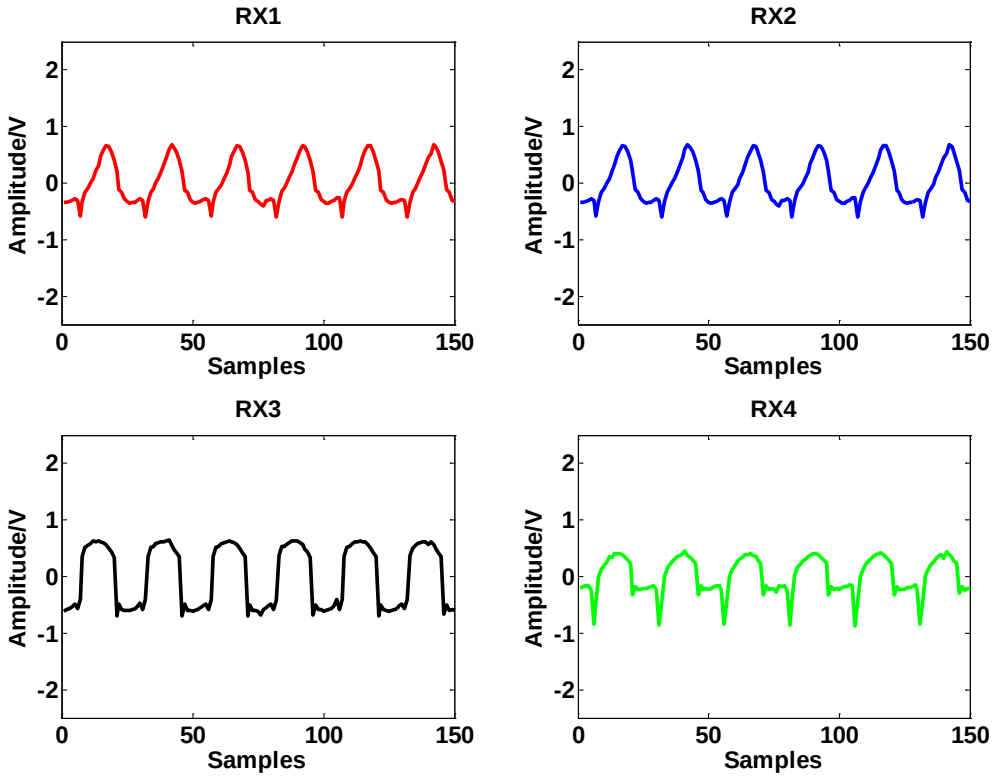


Figure 6-34 Demultiplexed output without equalization

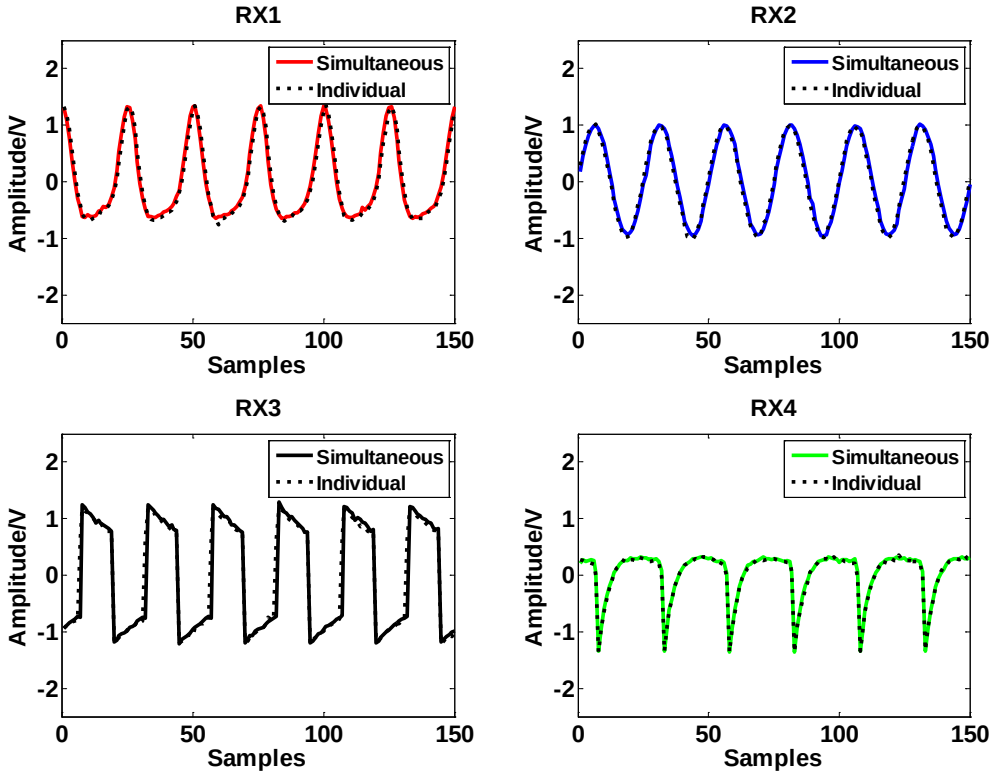


Figure 6-35 Demultiplexed output after equalization

ii Test with Identical Signals

In order to test the system's performance, four 6MHz, 200mV peak-to-peak sinusoidal signals are used for test. Tab. 6-10 and 6-11 give the summaries of noise and linearity performance. From them we find in all-driver test, SNR and THD are close to the specification defined in Chapter 1.

Table 6-10 SNR comparison in all-driver test with identical signals

Input configuration		SNR before equalization	SNR after equalization
Single input		29.3	31.1
4 inputs	"in phase"	42.6	38.4
	"out of phase"	30.8	40.7
	"equal amplitude"	37.4	39.0

Table 6-11 THD comparison in all-driver test with identical signals

THD/dB (to 3rd dist.)		THD after equalization	THD after equalization
Single input		40.7	42.0
4 inputs	"in phase"	39.0	40.8
	"out of phase"	33.0	43.2
	"equal amplitude"	38.8	40.8

6.3 References

[6.1] Texas Instruments, "High-Speed Layout Guidelines," Application report, November 2006.

[6.2] W. Kester and J. Bryant, *Grounding in High Speed Systems*, High Speed Design Techniques, Analog Devices, 1996, Chapter 7,p. 7-27.

[6.3] *User's manual of Model 701923 PBD2000 Differential Probe*, 3rd edition. Yokogawa Electric Corporation, Nov. 2005.

[6.4] *DL9040/DL9140/DL9240 Series Digital Oscilloscope User's Manual*, 8th edition. Yokogawa Meters & Instruments Corporation, April 2009.

[6.5] *Agilent 33500 Series 30 MHz Function / Arbitrary Waveform Generator User's Guide*, 3rd edition. Agilent Technologies, Dec. 2010.

[6.6] L. de Vreede, ET 4294, Microwave Circuit lecture notes, Delft University of Technology, 2012.

[6.7] *Cyclone II FPGA Starter Development Board Reference Manual*, 1st version. Altera, Oct. 2006.

Chapter 7 Conclusion

7.1 Thesis Contributions

In this thesis, several contributions have been made in the area of the probe-mainframe signal transmission in the TEE ultrasound probing system. Some of the main contributions are listed below.

- A novel low-power current-mode multiplexer has been designed to achieve cable count reduction.

As the main goal of the thesis project, power consumption on the cable drivers is the key specification. In order to achieve a low power on-chip design, different multiplexing schemes and cable driving schemes have been analysed. Based on conclusions on these aspects, a current-mode time-multiplexing scheme has been proposed to achieve low power consumption and cable-count reduction at the same time. To further reduce the power consumed by the multiplexer, a novel transconductor has been designed which shows its advantages in our application over several common candidates after comparison. Measurement results show good functionality of the proposed multiplexer, which gives 4 times cable count reduction.

- A mixed-mode RX has been designed to cancel the non-idealities of the cable-based transmission.

Different from the on-chip transmission, the 3-m micro-coaxial cable used in the project exhibits obvious transmission line effect. According to cable characterization and modelling, an ADC-based equalization scheme is determined to cancel the non-idealities during transmission, which also accommodates well with the mainframe of the TEE probing system. Afterward based on the modelling of SNR and equalizer length, a TIA with extra gain stage has been designed as the first stage of RX, which gives an optimized performance for low noise and light equalization burden.

- Equalization algorithms have been successively implemented.

In order to resolve signals from different drivers and verify the feasibility of the whole system, two different equalization algorithms, zero-forcing and minimum-mean-square-error equalizations have been proposed, both of which are applicable in the thesis application with different emphases. Furthermore, multiple-input-multiple-out (MIMO) equalization has also been provided, which aims at cancel the mismatches of the signal transmission between different drivers. Measures results exhibit proves the feasibility of the algorithms.

The main contributions listed above indicate that the proposed scheme is a promising candidate for a low-power cable-count reduction TEE probing system.

7.2 Potential Improvements

The proposed system bridges the gap between the receive ASIC in the TEE probe and the mainframe where signal post processing is carried out. In order to make the proposed scheme more applicable, some improvements can be made, as suggested below.

- SNR can be improved by an on-chip mode-selection MUXes.

As shown in the measurement, the SNR after A-D conversion is less than the target value. This is due to the spurious tones associated with the on-board mode selection MUXes. This can be improved by an on-chip design.

- Crosstalk can be reduced by a more custom design.

As illustrated in Chapter 6, the measured crosstalk does not fall into the desired range. From Appendix E, we know that it might be due to the non-linearity of the RX TIA, or the crosstalk existing in the on-board mode-selection MUXes. Even though the crosstalk can be calibrated out by an equalization algorithm, the power penalty paid on the DSP might be excessively large. However, both suspicious cases can be avoided by a custom circuit design. For the non-linearity of the RX TIA, its effects can be co-simulated with the TX circuitry and examined more easily. For the crosstalk in the on-board mode-selection multiplexer, it can be neatly avoided by an on-chip design for the less parasitics.

- Timing control between RX and TX should be included in system.

As described in Chapter 6, the synchronization between the RX and TX clocks is based on offline clock-phase tuning. This is inconvenient for the real application. To address this issue a phase-locked-loop (PLL) with proper RX-TX feedback could be designed. For a low-power TX design, a known data pattern can be transmitted at RX side. By comparing the transmitting and receiving timing of this pattern, certain timing-calibration quantity can be derived and used to make the clock phase tuning in order to get the best timing alignment between RX and TX.

- A continuous-time linear equalizer (CTLE) can be used as the extra gain stage at RX to boost the bandwidth.

In Chapter 3 the cable shows obvious attenuation frequency goes above 50MHz. So, if further cable reduction is required in the future implementation, there will be more stress on the TIA and equalization design. To solve the bandwidth-limited issue, one effective way is to replace the extra gain stage in RX by an active CTLE, which can serves as both amplifier and bandwidth booster. However, the SNR drop caused by the limited bandwidth of the cable and the TIA cannot be restored.

Appendix A VNA Measurement

In the cable measurement 3 frequency ranges have been used:

0-1GHz: to get raw data in order to achieve good time-domain simulation in Cadence (in Cadence frequency higher than the measured will be processed by extrapolation, which might even not converge. So higher stop frequency in the measurement can give a better time domain simulation.)

0-200MHz: to seek if there is still any opportunities to use CDMA modulation, since the spectrum of a CDMA signal is about below 200MHz as a rough estimation.

0-25MHz: to get a precise channel condition used for time-interleaving method.

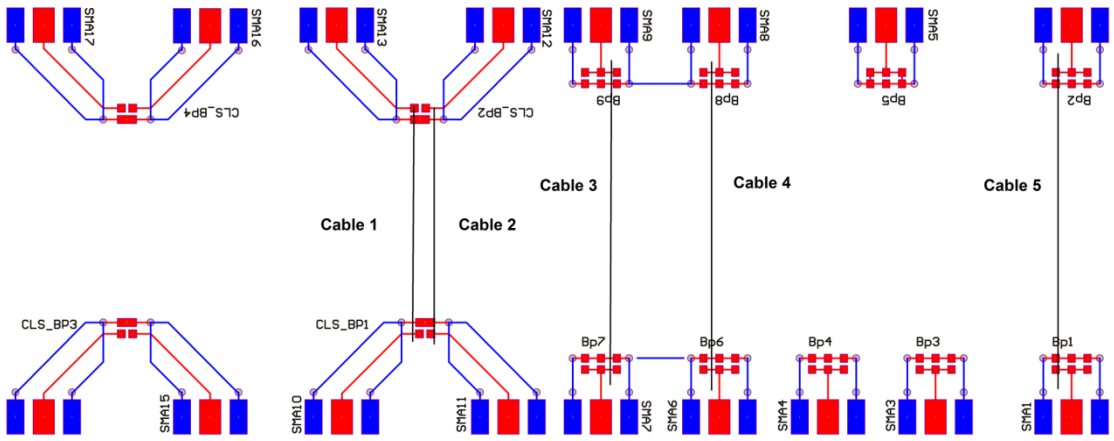
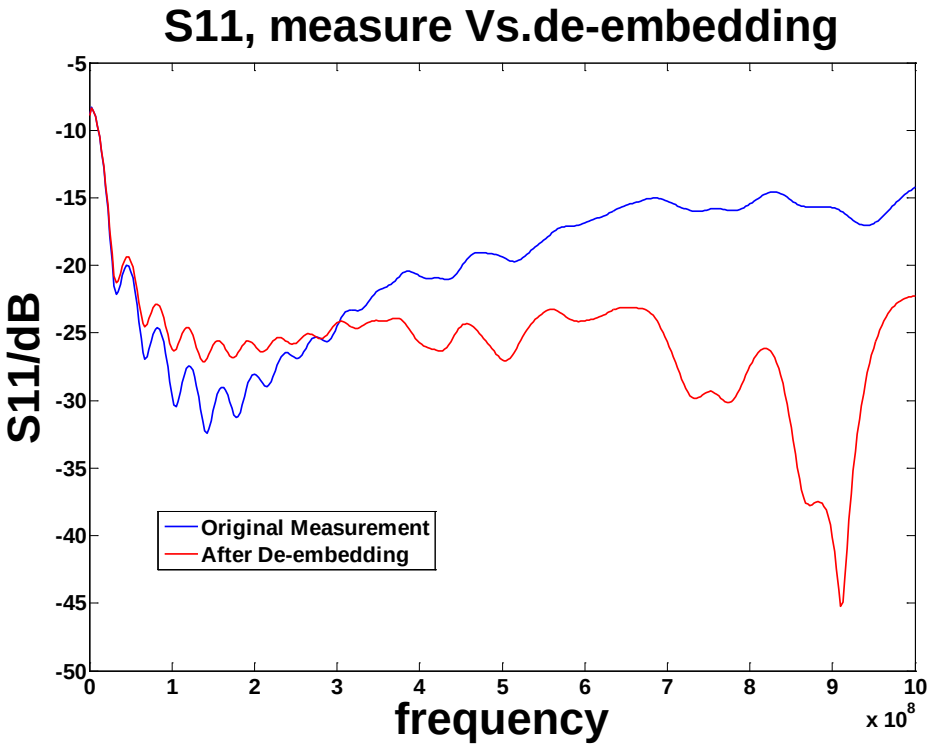


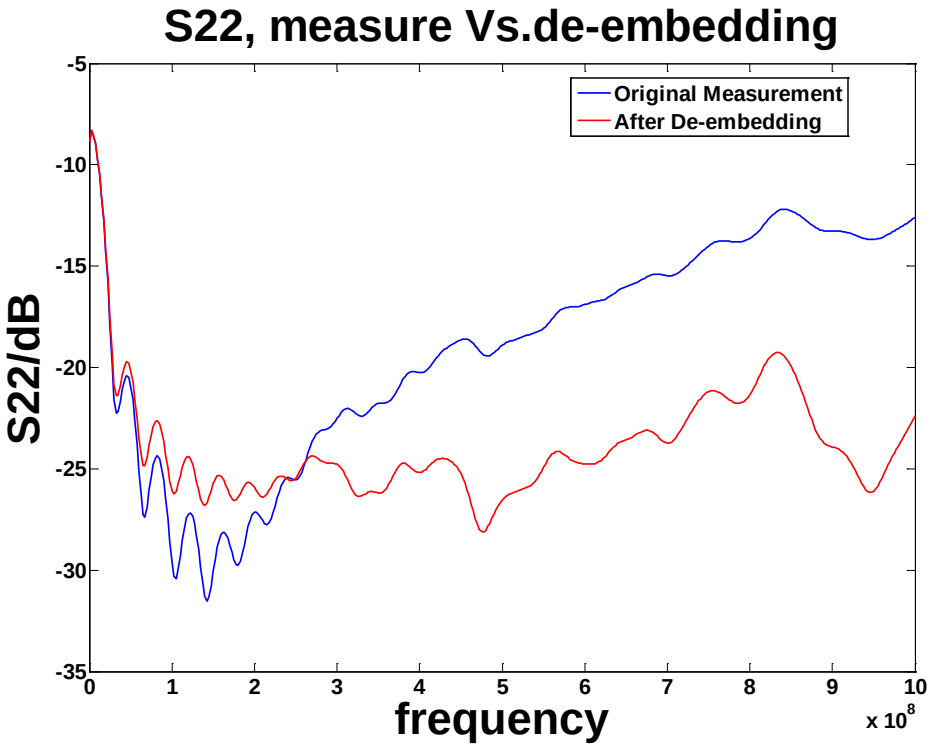
Figure A-1 Cable-board connection

A.1 S-parameter measurement

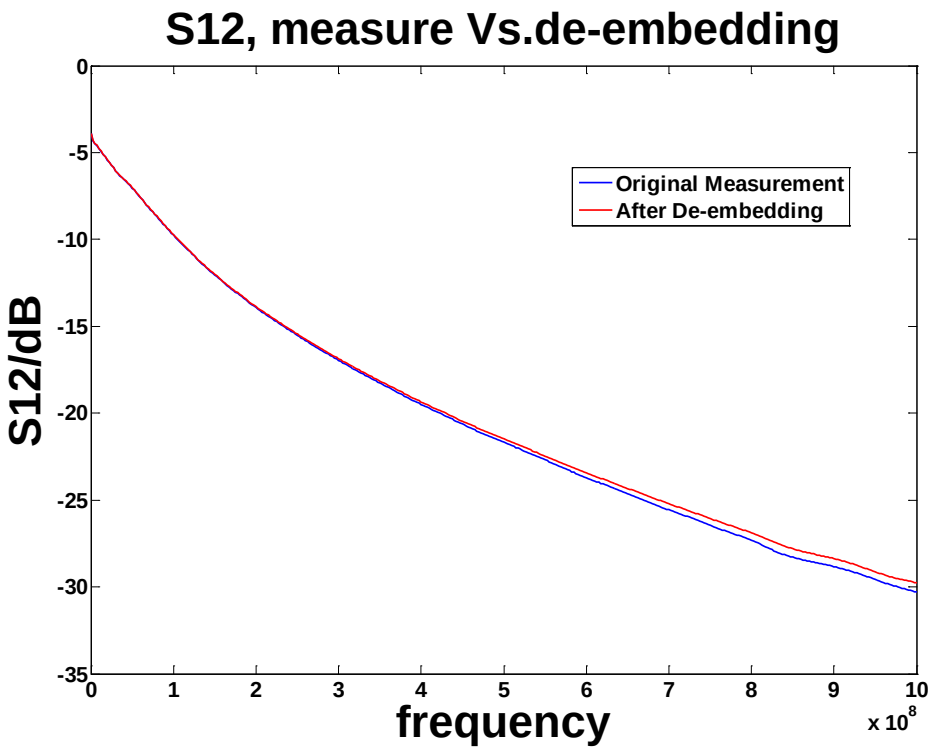
In the following measurement, results with and without connector de-embedding are shown in the same figure for comparison.


S11, measure Vs.de-embedding
S11/dB
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0
1
2
3
4
5
6
7
8
9
10
frequency
x 10^8
Original Measurement
After De-embedding

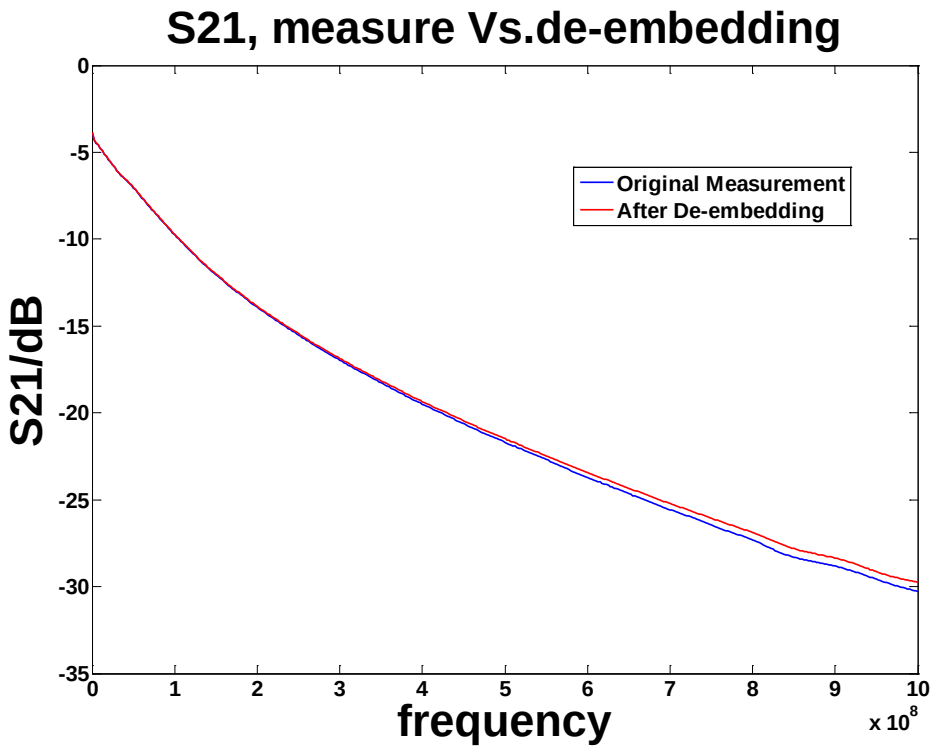
(a)S11


S22, measure Vs.de-embedding
S22/dB
-5
-10
-15
-20
-25
-30
-35
0
1
2
3
4
5
6
7
8
9
10
frequency
x 10^8
Original Measurement
After De-embedding

(b)S22



(c)S12



(d)S21

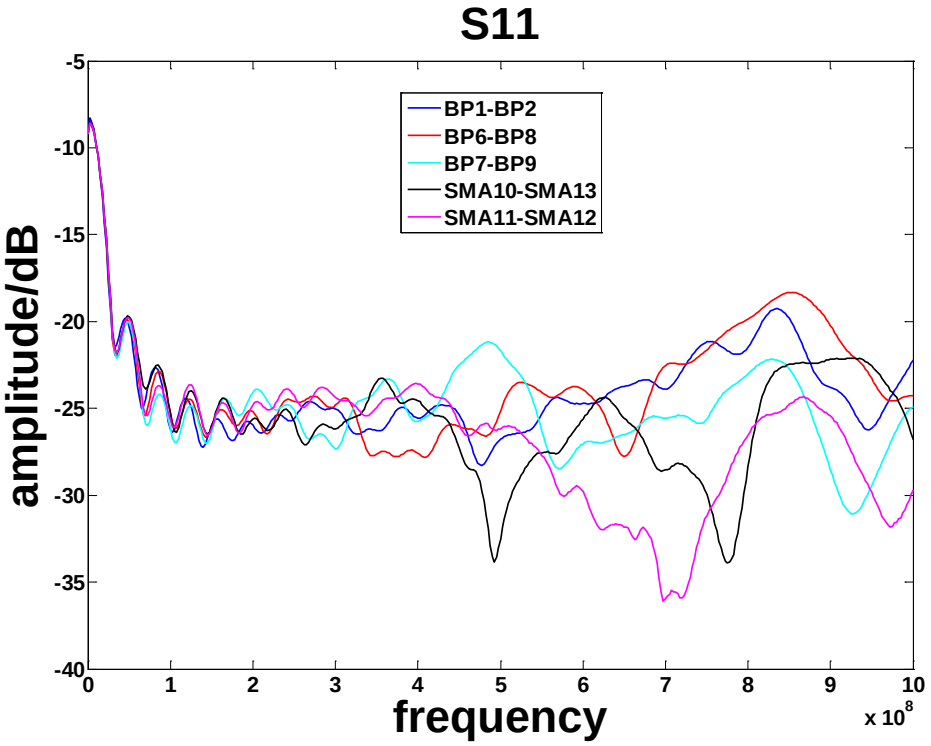
Figure A-2 S-parameter measurement with and without de-embedding

Observations:

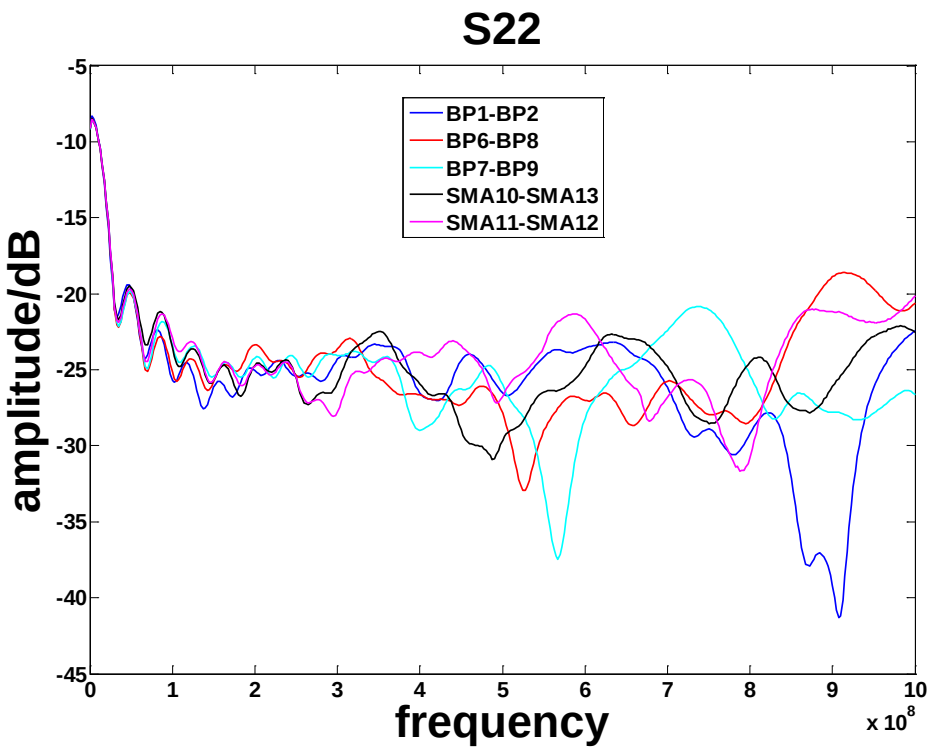
1) The huge difference in S11/S22 between original measurement and de-embedding result are due to the characteristic impedance mismatch between the connector and the transmission line. For S12/S21 it is less sensitive to the mismatch.
2) S12=S21 is the reciprocity of any passive component.
3) S11=S21 is the property of the transmission line.

A.2 Variations among different cables

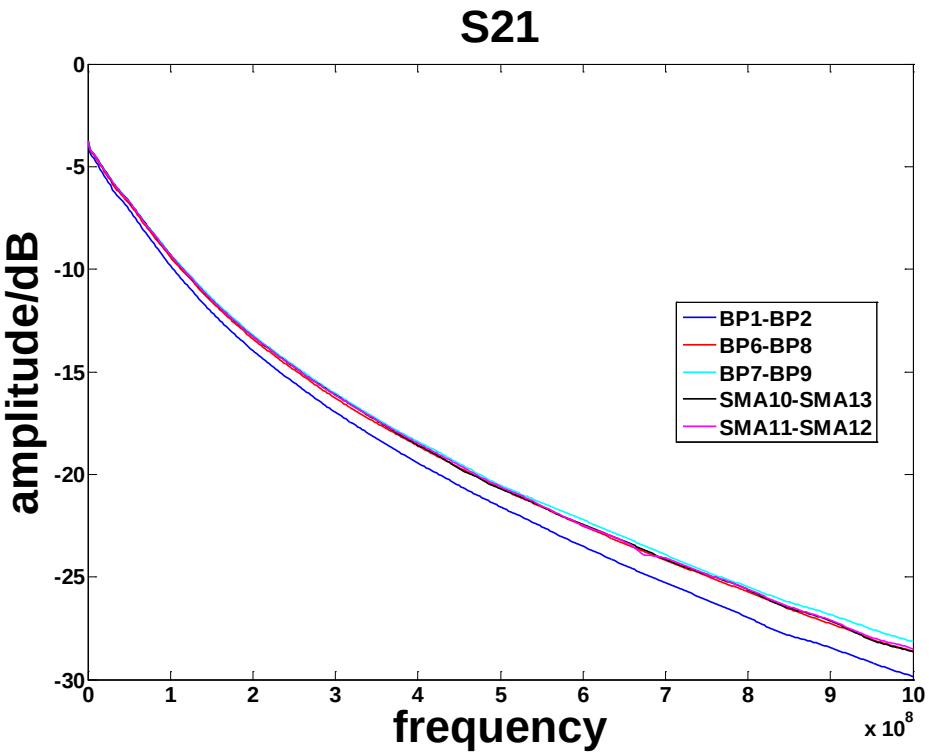
0-1GHz



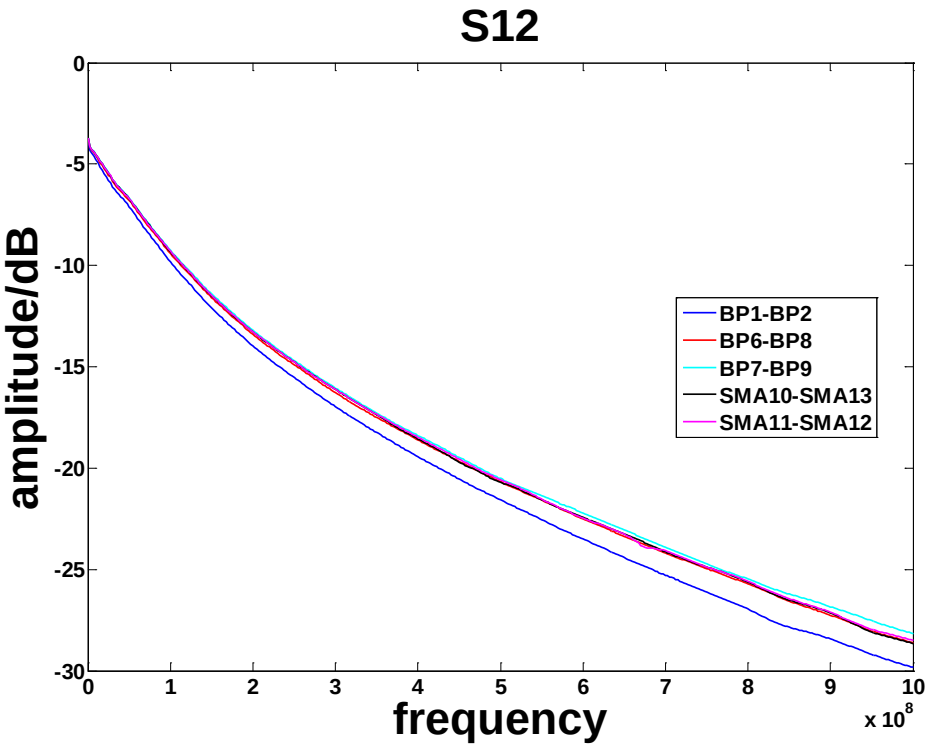
(1) S11


S22
BP1-BP2
BP6-BP8
BP7-BP9
SMA10-SMA13
SMA11-SMA12
amplitude/dB
frequency
x 10^8

(2) S22


S21
BP1-BP2
BP6-BP8
BP7-BP9
SMA10-SMA13
SMA11-SMA12
amplitude/dB
frequency
x 10^8

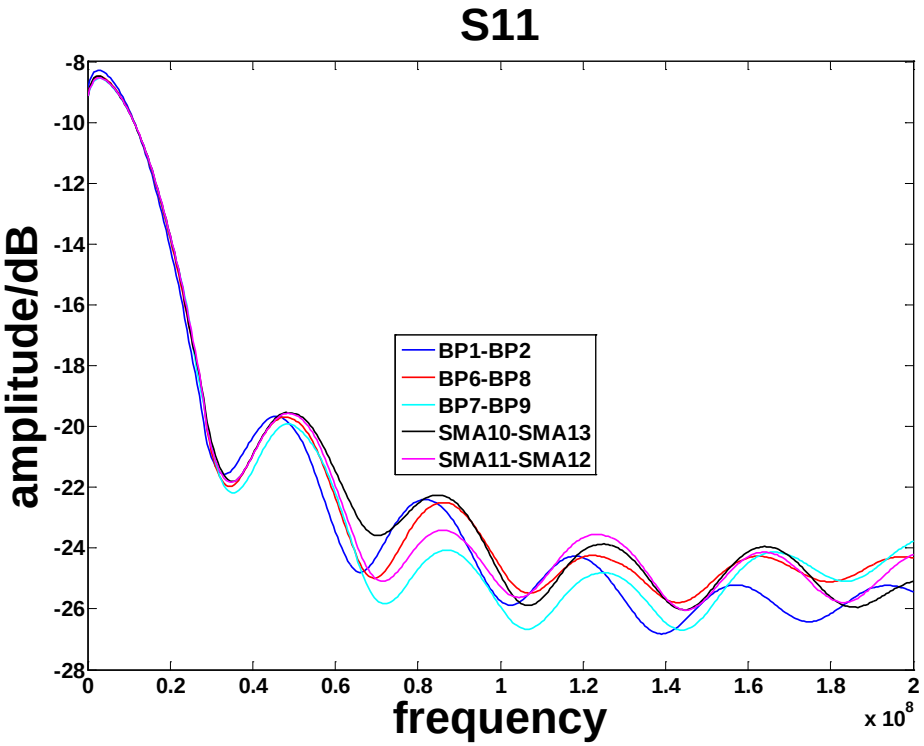
(3) S21



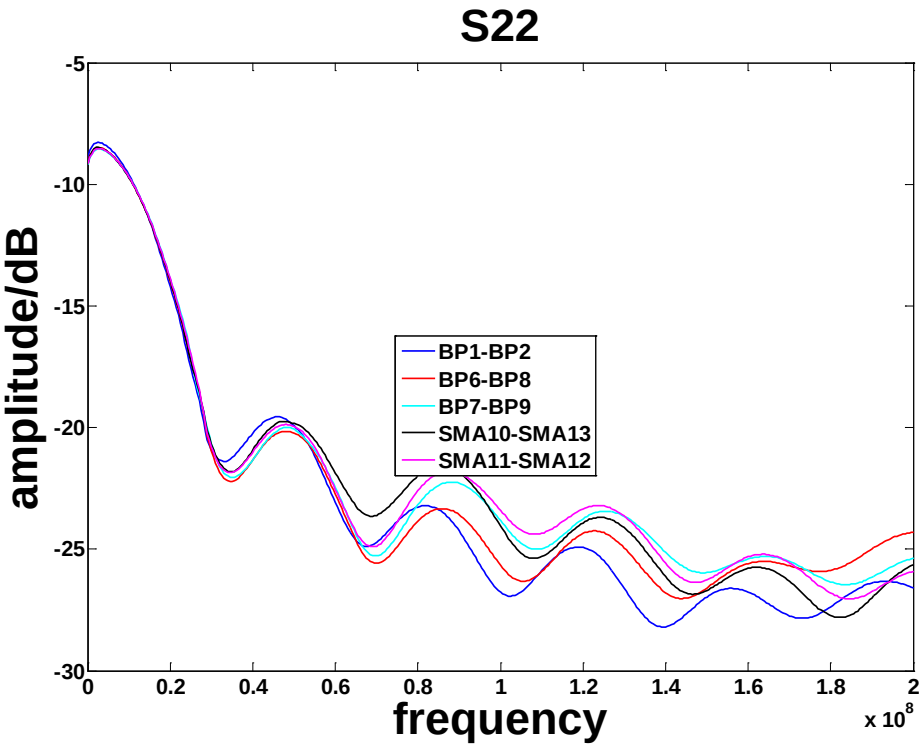
(4) S12

Figure A-3 S-parameter measurement of different cables (0-2GHz)

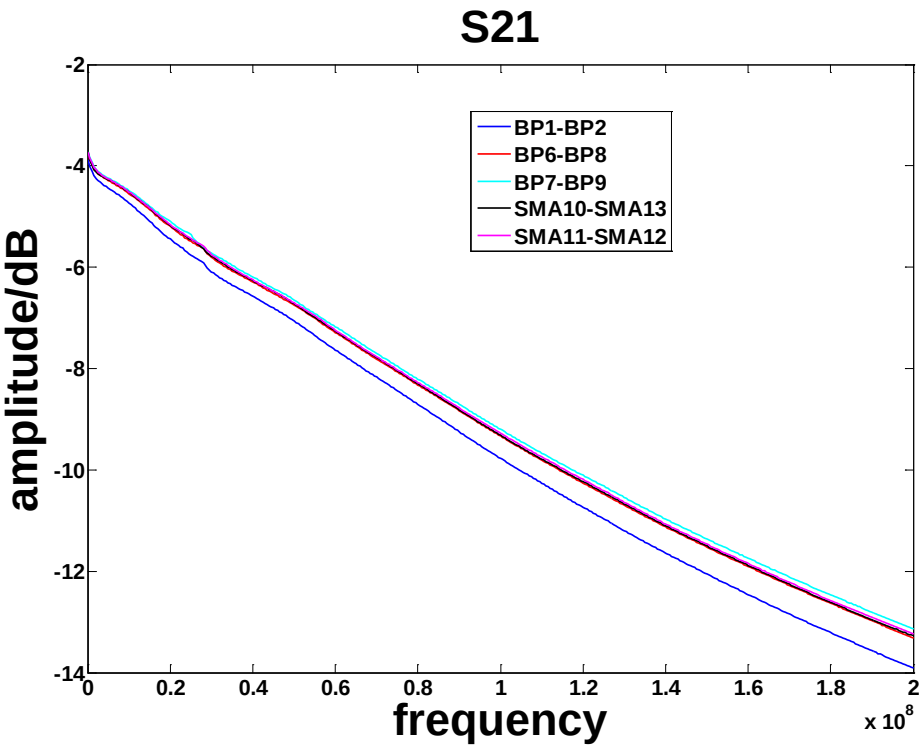
0-200MHz



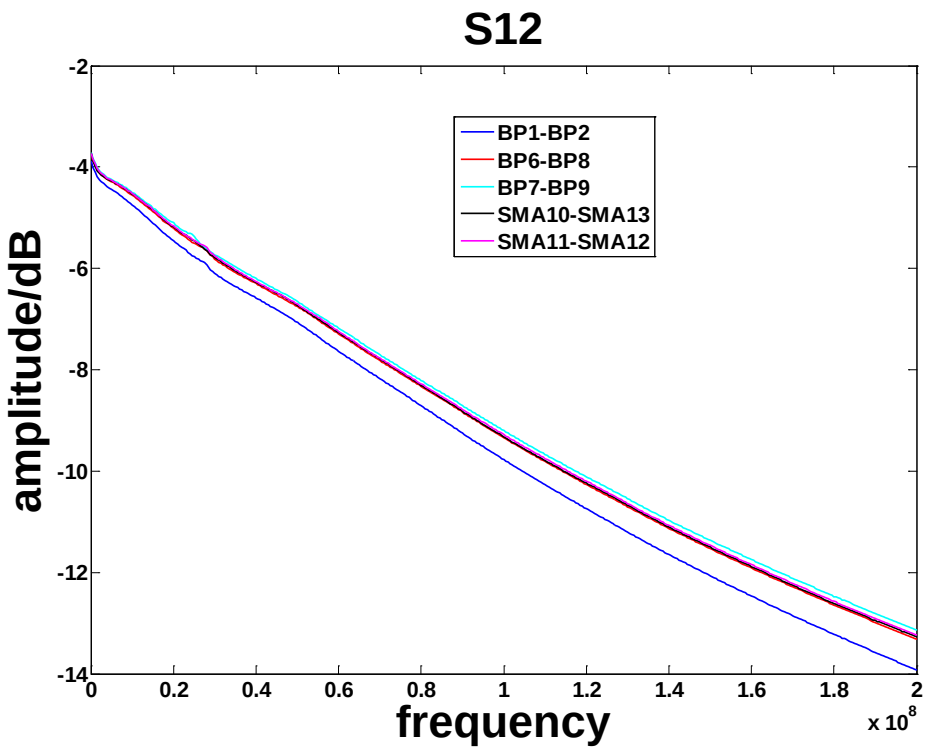
(1) S11


S22
amplitude/dB
frequency
x 10^8
BP1-BP2
BP6-BP8
BP7-BP9
SMA10-SMA13
SMA11-SMA12
-5
-10
-15
-20
-25
-30
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(2) S22


S21
amplitude/dB
frequency
x 10^8
BP1-BP2
BP6-BP8
BP7-BP9
SMA10-SMA13
SMA11-SMA12
-2
-4
-6
-8
-10
-12
-14
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(3) S21



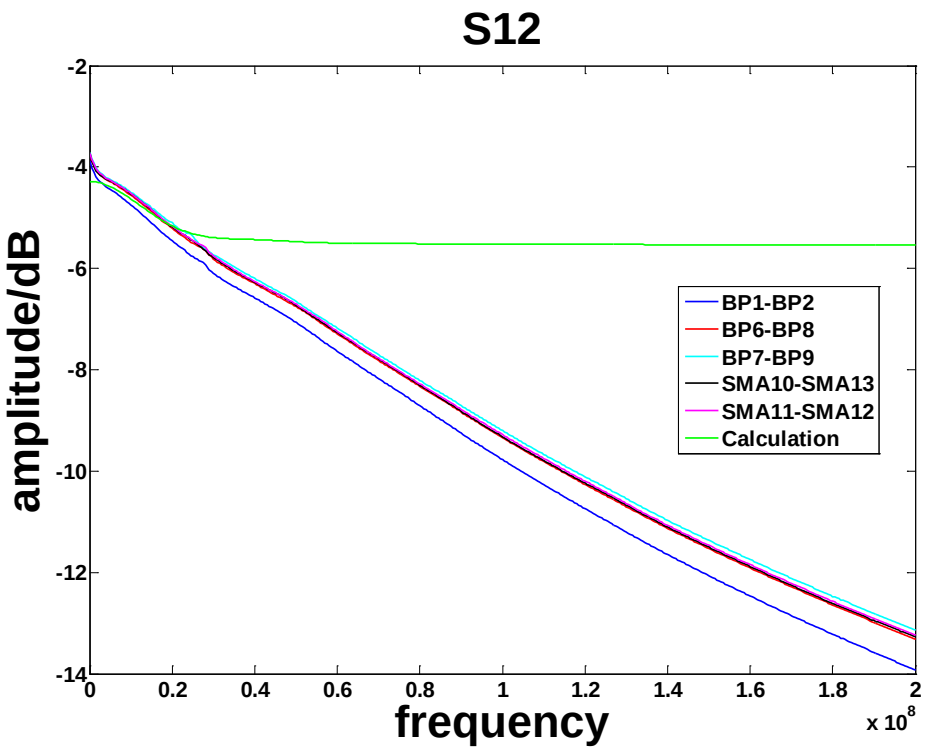
(4) S12

Figure A-4 S-parameter measurement of different cables (0-200MHz)

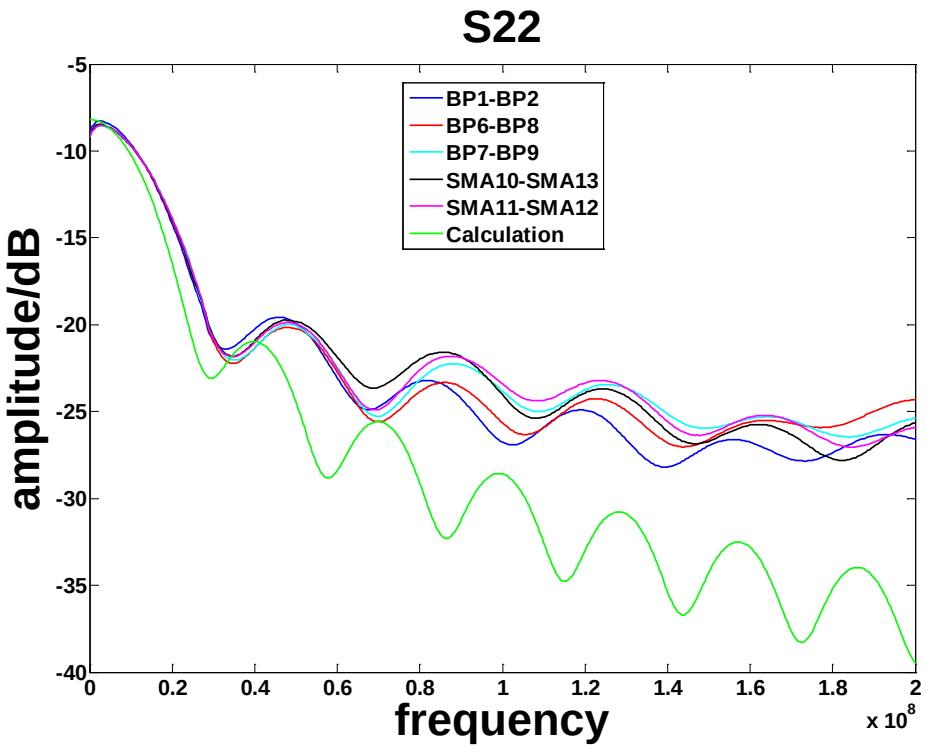
Note:

Cable BP1-BP2 is slightly different from other cables. This can be observed in both 0-200MHz and 0-1GHz measurements. It is due to the length difference between Cable BP1-BP2 and others. In application it is not an issue since the small dimension of the TEE probe cannot induce as much variations as those shown on the test board.

A.3 Measurement Vs. Specifications



(1) S12



(2) S22

Figure A-5 Comparison between measurement and specifications

Reason of the deviation: At higher frequency, skin effect comes into effect, which induces more loss. But at lower frequency the calculation matches the measurement very well. After checking the resistance of the cable, for the core it is about 56 Ohm, and for the shield it is about 2 Ohm (much less loss compared with the core resistance), and the cable length is about 2.6 meter after gluing be Oldelft. In the specification it says the conductor resistance is 22 Ohm/meter, so in theory the total resistance should be 22*2.2=57.2 Ohm, which is quite close to the measured value.

A.4 Crosstalk

In this measurement there are two PCB layout designed. One is BP6-BP8 and BP7-BP9 (Cable 3 and Cable 4 in Fig. A-6), which is mainly used to measure the crosstalk between the cables, and another is SMA10-SMA13 and SMA11-SMA12 (Cable 1 and Cable 2 in A-6), which includes the crosstalk due to the close on-chip bondpads.

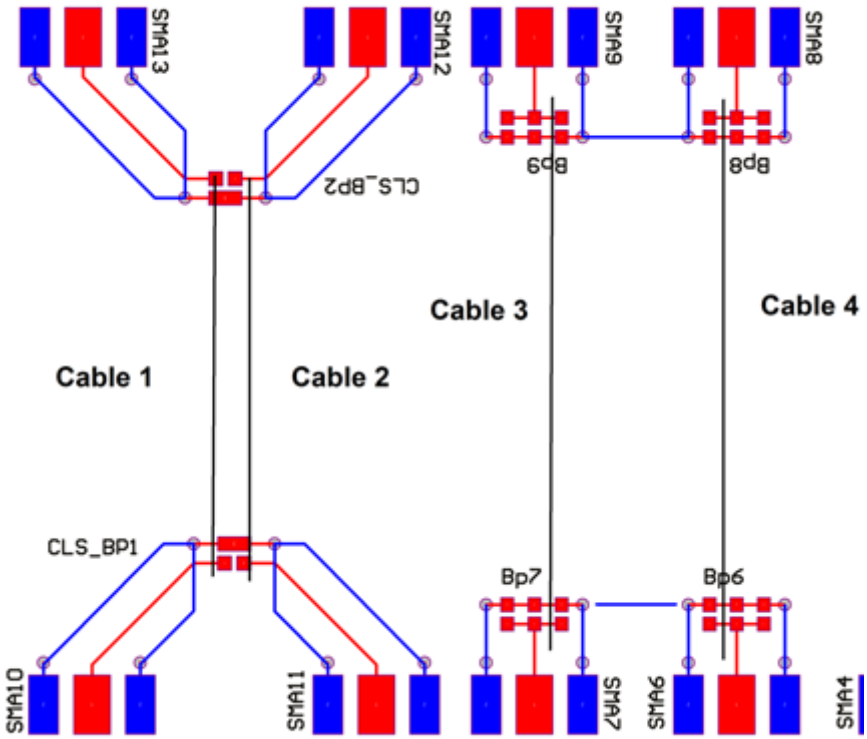


Figure A-6 crosstalk measurement

(Cable 1&2 are for measuring the crosstalk with the close bondpads.

Cable 3&4 are for measuring the crosstalk without the close bondpads)

Taking 0-200MHz as an example:

Far-end cross-talk (FEXT)

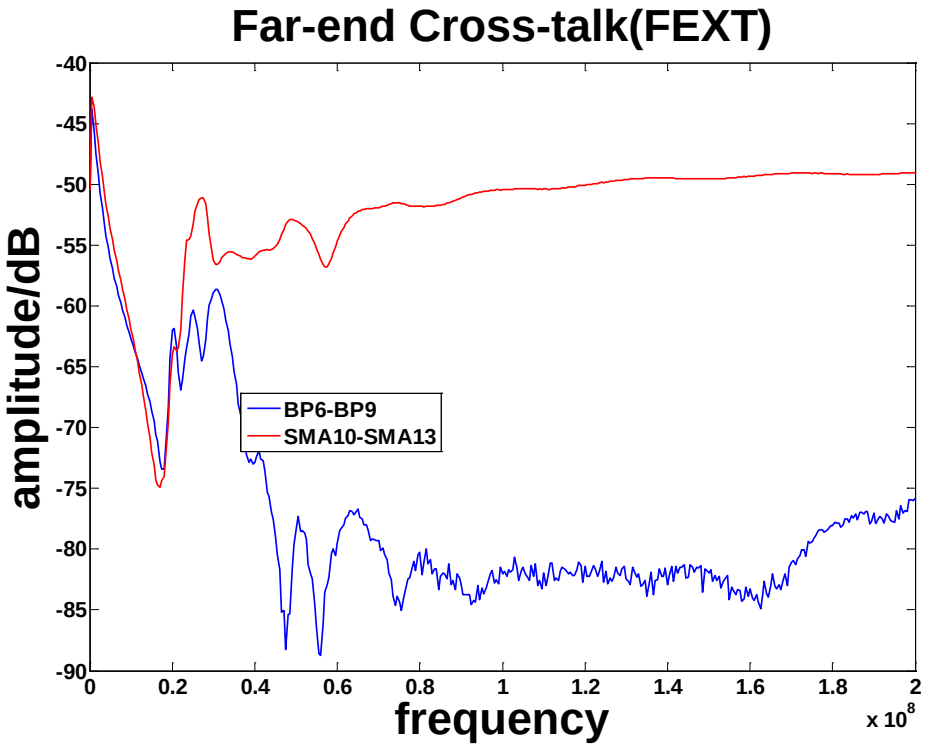


Figure A-7 FEXT (0-200MHz)

Near-end cross-talk (FEXT)

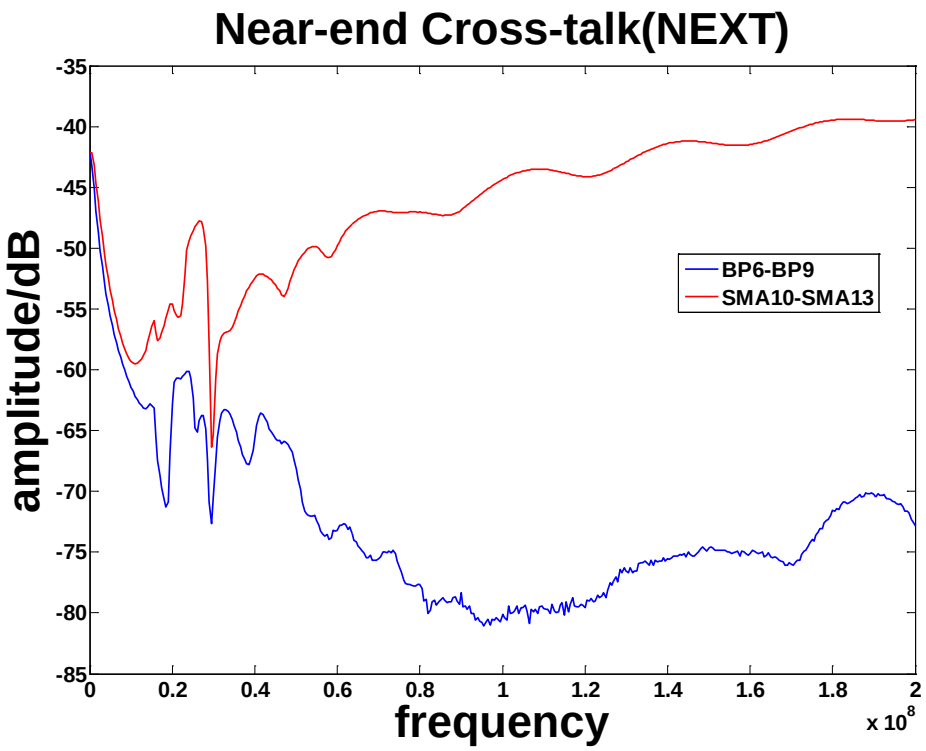


Figure A-8 NEXT (0-200MHz)

Note:

Both measurement are not carried out in the worse cases. That is because that it is hard to check if the selected cables are in the vicinity of each other in the rub tube.

All the plotted data S12's. One port of the network analyzer is connected to one end of a cable, and the other port is connected to one end of the second cable. The remained two ends of the two are cables connected to standard 50Ohm loads.

From the above two figures we find the close bondpads indeed have impact on crosstalk. But it is hard to recognize if the crosstalk is caused by the vicinity of the bondpads, or the glue used to fix the cables.

If the measured crosstalk is acceptable, then one concern encountered in choosing transmission mode in Chapter 2 is alleviated, then we can choose current or voltage mode only based on achieving low power consumption.

A.5 Effects of the cable winding and shaking

In the measurement when the shape of the cable (winding or shaking the cable) is changed, little change can be observed in the recorded data, which indicates good shielding between different cables.

Appendix B Multi-Input-Multi-Output (MIMO) Equalization

On the cable there are signals from 4 drivers. Due to the mismatch between them, such as the mismatches in transconductances and output impedances, the signals actually propagate along different channels, as illustrated in Fig. B-1. Let's take the transconductance mismatch as an example. In our implementation, the transconductance is defined by an on-chip resistor, of which spreads up to 3% [1]. So the unmatched transconductance might cause noticeable crosstalk between the received signals, exceeding the -40dB requirement given in Chapter 1.

At the receiver part, signals are finally delivered to separate outputs, which makes the whole system behave as a multi-input-multi-output (MIMO) system.

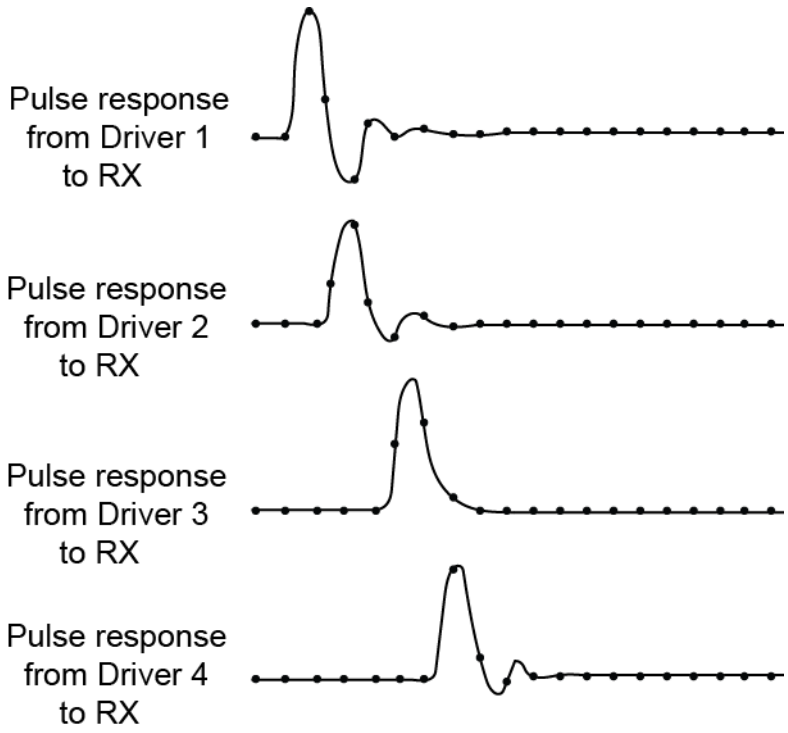


Figure B-1 Reflections showing the different channel responses on the cable.

In order to make the MIMO equalization easy to be understood, the number of channel responses is assumed to be 4, in order to be consistent with the real application. Since the output of the RX will be separated into 4 different "users" (denoted in Chapter 1), in the MIMO model 4 separate sub-receivers, $RX_{sub1..4}$, are assumed to be directly connected at the output of the cable, as shown in Fig. B-2.

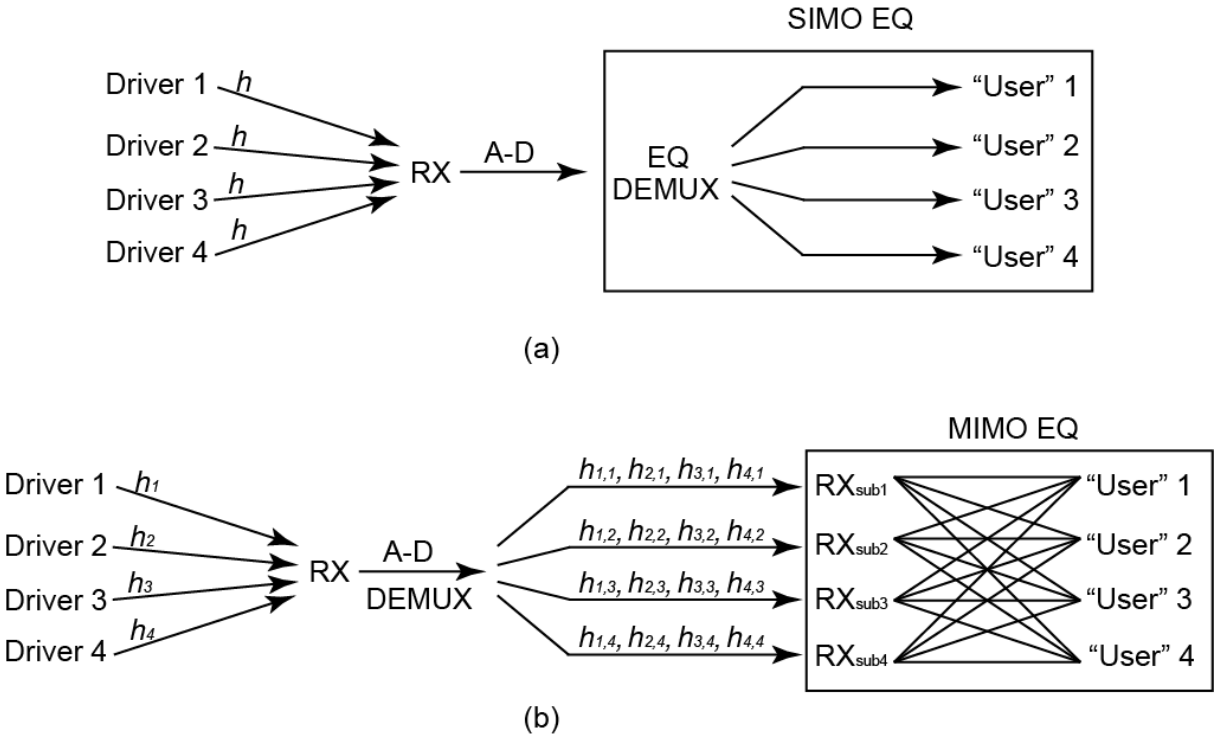


Figure B-2 Decomposition of the SIMO system into a MIMO system

Furthermore, Symbol, $h_{i,j}$, is used to represent the channel response between Driver i and RX_{sub} j. So the complete channel response from the transmitter i, h_i, is distributed among the 4 receivers,

$$h_i: \{h_{i,1}, h_{i,2}, h_{i,3}, h_{i,4}\}, i = 1,2,3,4 \qquad (B-1)$$

where h_i is obtained with a sampling clock of 4*f_s, and h_{ij} are collected at the speed of f_s. So the output from RX_{sub} j, R_j, can be expressed as

$$R_j = \sum_{k=1}^{4} h_{k,j} * S_k \,, j = 1,2,3,4 \qquad (B-2)$$

where $S_k, k = 1,2,3,4$ are the input samples fed into Driver k. From the above expression we find that R_j consists of signals from all Drivers. Equivalently speaking, in order to extract the signal from the target driver, we need the output from all the RXs. This can be expressed as,

$$O_j = \sum_{k=1}^{4} EQ_{k,j} * R_k = \sum_{k=1}^{4} \sum_{i=1}^{4} EQ_{k,j} * h_{i,k} * S_i \qquad (B-3)$$

where O_j is the equalized result collected by User output channel j, and $EQ_{k,j}$ denotes the equalizer from Driver k to RX_{sub} j. Since only the signal from S_j is meaningful to its corresponding user, the corresponding output channel, there should be a further simplification of the above expression.

Only the signal from Transmitter j, S_j, should be left after equalization, which means

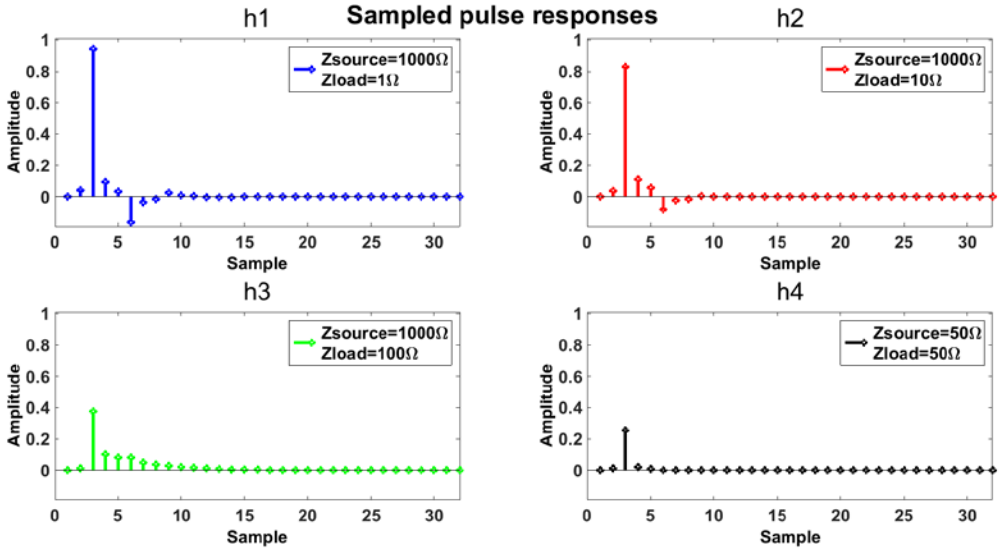
$$\sum_{i=1}^{4} EQ_{k,j} * h_{i,k} = \begin{cases} U_i, i = j \\ O, i \neq j \end{cases} \quad (B-4)$$

As shown in ZFE and MMSE, the convolution can be expressed by matrix multiplication, so it can be expressed as

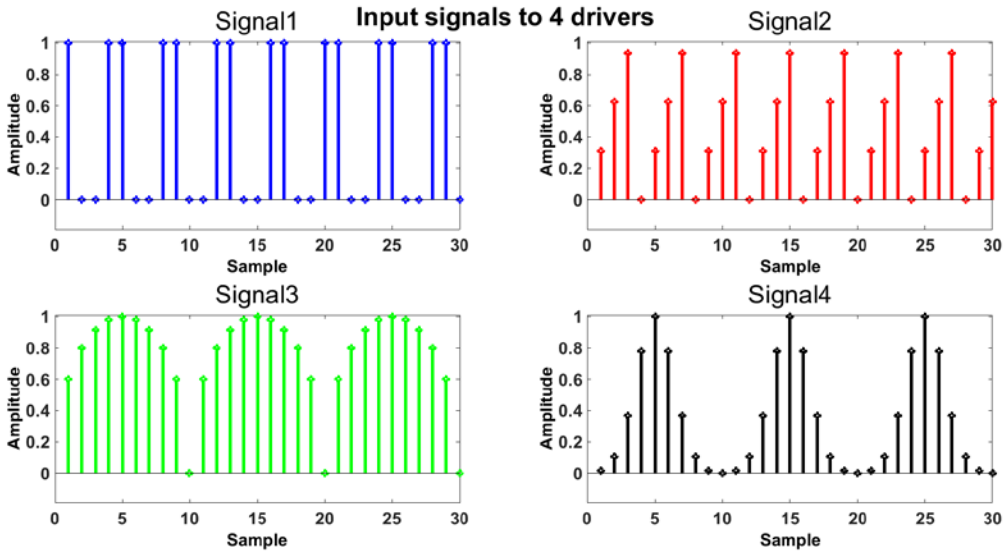
$$\begin{bmatrix} H_{1,1} & H_{1,2} & H_{1,3} & H_{1,4} \\ H_{2,1} & H_{2,2} & H_{2,3} & H_{2,4} \\ H_{3,1} & H_{3,1} & H_{3,3} & H_{3,4} \\ H_{4,1} & H_{4,1} & H_{4,3} & H_{4,4} \end{bmatrix} \begin{bmatrix} EQ_{1,1} & EQ_{1,2} & EQ_{1,3} & EQ_{1,4} \\ EQ_{2,1} & EQ_{2,2} & EQ_{2,3} & EQ_{2,4} \\ EQ_{3,1} & EQ_{3,2} & EQ_{3,3} & EQ_{3,4} \\ EQ_{4,1} & EQ_{4,2} & EQ_{4,3} & EQ_{4,4} \end{bmatrix} = \begin{bmatrix} U_1 & 0 & 0 & 0 \\ 0 & U_2 & 0 & 0 \\ 0 & 0 & U_3 & 0 \\ 0 & 0 & 0 & U_4 \end{bmatrix} \quad (B-5)$$

It can be solved by using either ZFE or MMSE. In Fig. B-3 one an example of MIMO equalization is shown. In the simulation the micro-coaxial cable in the project is used. The terminations of four drivers and four receivers vary as shown in Fig. B-3 (a). This is an exaggerated description of the real application, where load termination keeps unchanged since there is only one RX.

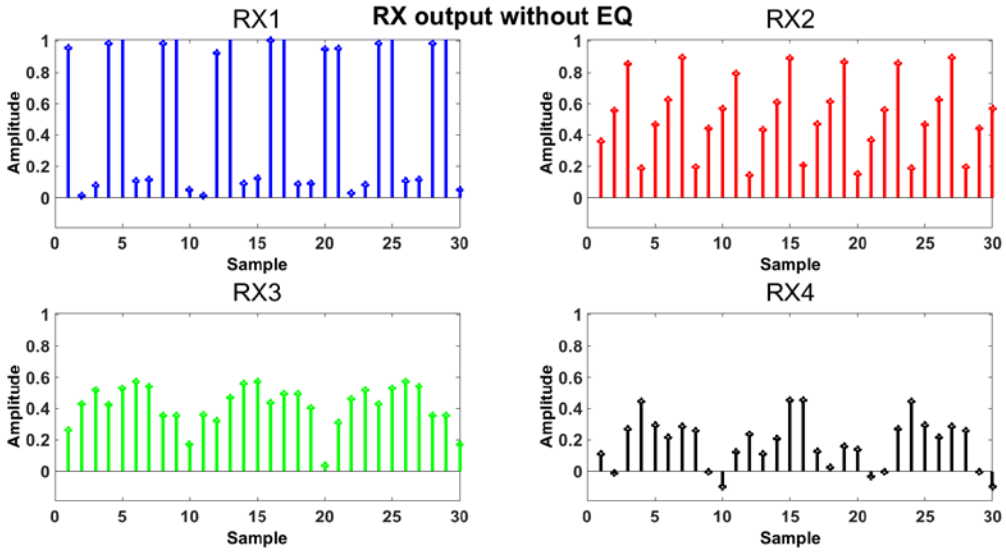
From Fig. B-3 (c) it can be found that signals from different drivers are indeed mixed with each other if no equalization is applied. Comparing Fig. 3-10 (b), (c) and (d), we observe that signals are resolved clearly after MIMO equalization.



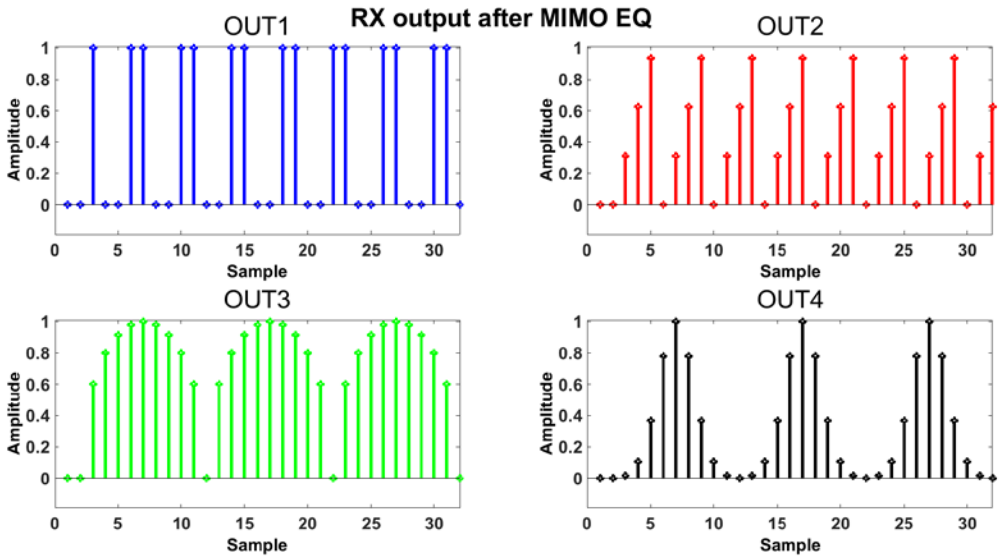
(a) Channel responses



(b) Input signals to 4 drivers



(c) Unequalized results from different RXs



(d) Received signals after MIMO equalization

Figure B-3 One example of MIMO equalization

References

[1] TSMC 0.18 µm mixed-signal/RF spice model document, *version 1.1*. TSMC (Confidential), March 2010

Appendix C Current Mode or Voltage Mode

Since the input of the system is in voltage mode, a transconductor is required to convert the signal into the current domain for a current mode transmission. Assuming the transconductance of the transconductor is G_m, and thus the power transmitted into the cable is

$$P_{cur} = \frac{1}{2} \cdot (V_{in} \cdot G_m)^2 \cdot Z_{in}$$

And if we drive the cable in the voltage mode, the power consumed by driving the cable is

$$P_{vol} = \frac{1}{2} \cdot \frac{{V_{in}}^2}{Z_{in}},$$

where both P_{cur} and P_{vol} are provided by the driver on TX side. With a further assumption that both the voltage TX and current TX operate in Class A mode, the power formulated above can be seen as the lower limit in the power consumption comparison.

Since Z_{in} is of 100 Ω scale in the frequency of interest as shown in Chapter 4, in order to provide the same power onto the cable, G_m of a current-mode driver should be of 10 mS scale. This indicates the current mode TX will be a more power-efficient configuration, if we can drive the cable to meet the specifications with a transconductance smaller than this magnitude. Fortunately the analysis in Chapter 4 gives a positive answer to this assumption.

Appendix D Comparison between Several Trans-conductor Candidates

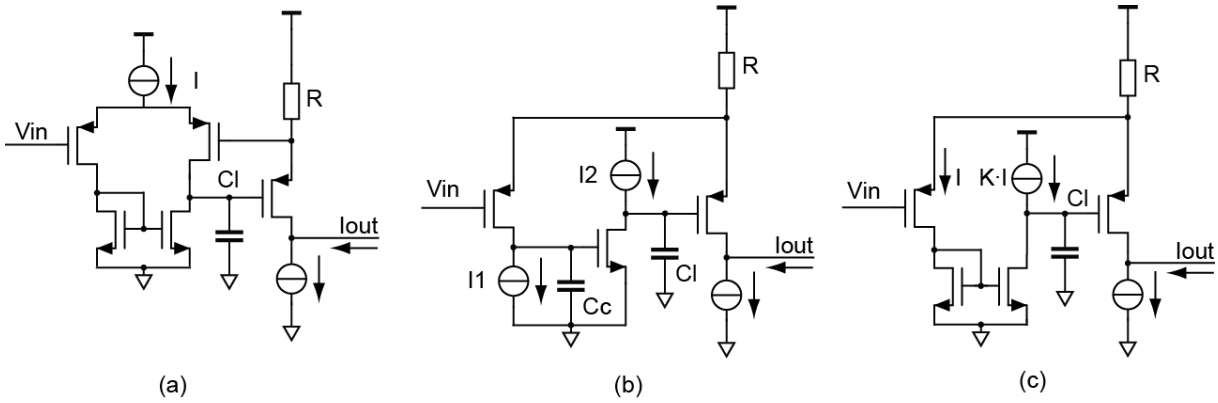


Figure D-1 candidates for current-efficient helper amplifiers

Fig. D-1 shows several possible implementations of the helper amplifier. Fig. D-1 (a) shows a simple differential pair with active load; (b) shows a two-stage single-ended amplifier where C_C is added for frequency compensation. In (c) a new single-stage single-ended amplifier is proposed, where a current mirror with 1:K size ratio is inserted as the inverting stage.

In order to make a clear comparison between the above candidates, several assumptions are made as follows.

1) The main branch, which includes the source-degenerated transistor, degeneration resistor and current source, is designed as identical to all the candidates.

2) All the amplifiers are loaded by a capacitor C_l of the same value to guarantee the stability. C_l is composed of the gate capacitance of the source-degenerated transistor, and a possible explicit capacitor.

3) Input-referred noise from the degeneration resistor is of the same value in all the transconductors, and thus it is ignored in the analysis for simplicity.

4) The current efficiency, g_m/I_d, of the input transistor is deemed as identical to the different topologies.

Based on the above assumptions, the current efficiency analyse can be started from two aspects, gain-bandwidth product (GBW) and input-referred noise power spectrum density (PSD), which are the two dominant factors to determine the power consumption of an amplifier.

1) Gain-bandwidth product

For the amplifier shown in Fig. E-1 (a), GBW is determined by the gm of the input transistor and the load capacitance C_l.

$$GBW_{diff.\ pair} = \frac{1}{2\pi} \cdot \frac{g_m}{C_l} = \frac{1}{2\pi} \cdot \frac{(g_m/I_d)}{C_l} \cdot (I/2) \qquad (E-1)$$

where I is the total current flown through the amplifier. And the current efficiency of the input transistor, g_m/I_d, is considered as a constant.

For the two-stage amplifier in Fig. 10 (b), GBW is can be expressed as

$$GBW_{two-stage} = \frac{1}{2\pi} \cdot \frac{g_m}{C_c} = \frac{1}{2\pi} \cdot \frac{(g_m/I_d)}{C_l} \cdot \frac{C_l}{C_c} \cdot I_1 \qquad (E-2)$$

where C_c is the compensation capacitor at the output of the first stage. And I_1 is the current flown through the first stage. Normally in order to achieve enough phase margin and fast settling at the same time, the secondary pole is chosen as 3 times larger than the dominant pole [Sansen]. And this constraint is interpreted as

$$\left(\frac{g_m}{I_d}\right) \cdot \frac{I_2}{C_l} = 3\left(\frac{g_m}{I_d}\right) \cdot \frac{I_1}{C_c} \qquad (E-3)$$

Then Exp. (5-3) can be reduced to

$$GBW_{two-stage} = \frac{1}{2\pi} \cdot \frac{g_m}{C_c} = \frac{1}{2\pi} \cdot \frac{(g_m/I_d)}{C_l} \cdot \frac{I_2}{3} \qquad (E-4)$$

And for the GBW of the amplifier proposed in Fig. 10 (c), GBW is not only related to the gm of the input transistor, but also to the ratio of the current mirror.

$$GBW_{curr.mirr.} = \frac{1}{2\pi} \cdot \frac{K \cdot g_m}{C_l} = \frac{1}{2\pi} \cdot \frac{(g_m/I_d)}{C_l} \cdot (K \cdot I) \qquad (E-5)$$

where K is ratio of the current mirror, and I is the current flown through the input branch as shown in Fig. 5-10 (c).

In order to make a fair comparison, a current normalized GBW is defined by the ratio of the achieved GBW and total consumed current, which is GBW/I_{tot}. Tab. E-1 shows the results of the above 3 topologies.

Table E-1 CE comparison between candidates in Fig. D-1

	(a)	(b)	(c)
GBW/($\frac{1}{2\pi}\cdot\frac{(g_m/I_d)}{C_l}$)	$\frac{I}{2}$	$\frac{I_2}{3}$	$K\cdot I$
I_{tot}	I	I_1+I_2	$(K+1)\cdot I$
GBW/($\frac{1}{2\pi}\cdot\frac{(g_m/I_d)}{C_l}$)/$I_{tot}$	$\frac{1}{2}$	$\frac{1}{3}\cdot\frac{I_2}{I_1+I_2}$	$\frac{K}{1+K}$

From Tab. 5.1 we find the normalized current efficiency of differential pair and two-stage amplifiers both are not larger than ½. However, as for the proposed amplifier in Fig. D-1, it can achieve a higher efficiency by choosing K to be larger than 1. So if the total consumed current is limited by speed. Therefore the proposed amplifier is a suitable option.

b) Noise

Besides the speed requirement represented by GBW, noise performance of an amplifier also sets another limit to the minimum current consumption. In order to compare the candidates listed above, the input-referred noise voltage PSDs are calculated as follows,

For the noise PSD of differential pair amplifier, it can be expressed as

$$S(f)_{diff-pair}=\frac{4kT\cdot\gamma\cdot I\cdot(gm/I_d)}{[(I/2)\cdot(gm/I_d)]^2}=\frac{4kT\cdot\gamma}{(gm/I_d)}\cdot\frac{4}{I} \qquad (E-6)$$

where γ is the excess noise factor for a signal transistor. For a long-channel device in saturation region, it is 2/3 [1].

The noise PSD of a two-stage amplifier in Fig. D-1 (b), it can be written as

$$S(f)_{two-stage}=\frac{4kT\cdot\gamma\cdot I_1\cdot(gm/I_d)}{[I_1\cdot(gm/I_d)]^2}=\frac{4kT\cdot\gamma}{(gm/I_d)}\cdot\frac{1}{I_1} \qquad (E-7)$$

where the noise from the second stage is assumed to be suppressed by the first stage. So only noise from the input transistor counts in the expression.

As for the noise PSD of the proposed amplifier in Fig. D-1 (c), the noise voltage PSD is expressed as.

$$S(f)_{curr.mirr.}=\frac{4kT\cdot\gamma\cdot I\cdot(gm/I_d)}{[I\cdot(gm/I_d)]^2}=\frac{4kT\cdot\gamma}{(gm/I_d)}\cdot\frac{1}{I} \qquad (E-8)$$

Here the noise from the current mirror is ignored.

And a comparison can also be tabulated as is shown in Tab. D-2, where noise PSD is also normalized by multiplying the total consumed current.

Table E-2 Noise comparison between candidates in Fig. D-1

	(a)	(b)	(c)
Noise PSD/$\frac{4kT\cdot\gamma}{(gm/I_d)}$	$\frac{4}{I}$	$\frac{1}{I_1}$	$\frac{1}{I}$
I_{tot}	I	I_1+I_2	$(1+K)\cdot I$
Noise PSD/$\frac{4kT\cdot\gamma}{(gm/I_d)}\cdot I_{tot}$	4	$1+3\cdot\frac{C_l}{C_c}$	$1+K$

where in the normalized noise PSD of a two-stage amplifier, the approximation of exp.(5-4) is used.

From Tab. D-2 we find noise performances of the differential-pair and the two-stage amplifier are constrained by a fixed values. Take a two-stage amplifier as an example, if the capacitor ratio between C_l and C_c is less than 1, then the higher current-efficiency can be achieved compared with a differential-pair amplifier. However, This ratio will be eventually limited by the transistor parasitic capacitance.

As the counterpart, the proposed amplifier avoids such a problem by the an adjustable current ratio. By tuning the current ratio, K, the normalized noise PSD can be pushed to 1 as close as possible, which indicates higher current efficiency in the noise perspective.

However, a smaller K means lower current efficiency in the bandwidth-limited case, as shown in Tab. D-1. So the advantage of the proposed circuit is also application-dependent. As has been explained in Chapter 3, in the context of the project, the noise from the transconductor does not dominant the overall noise performance. So K can be chosen as a larger value as in the bandwidth-limited case.

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.

Appendix E Possible Reasons for the Overlarge Crosstalk

Due the nature of FIR equalizer, there will be residual cursors in the combined response composed of the channel response and the equalizer. This nature sets an upper limit of crosstalk that the system can achieve, as long as the sampled pulse response in pulse generation mode is identical to the one obtained in normal mode. To detect such a limit a simulation can be done by feeding a series of zero-padded sampled sinusoidal signals into a digital filter, which aims to mimic the signal transmission through the whole system: from TX to equalizer. After demultiplexing, signals delivered to each "user" can be re-measured in frequency domain to calculate the signal leakage from other "users" due to the finite-length equalizer. This calculation result can be considered as the best performance that the system can achieve in the crosstalk point of view. The measurement flow described before is depicted in Fig. E-1.

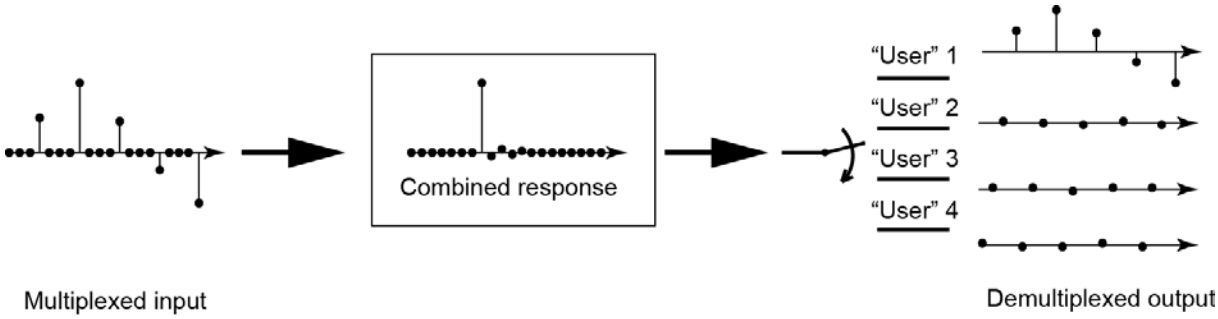


Figure E-1 Measurement for detecting the best performance on crosstalk

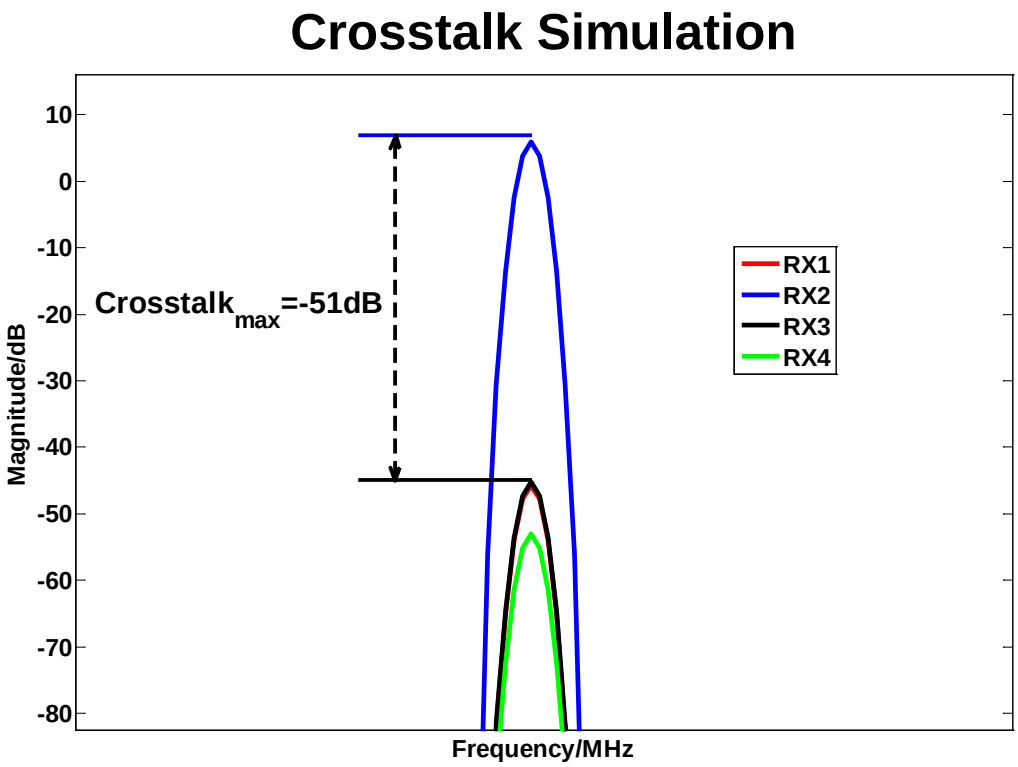


Figure E-2 Calculated the best crosstalk performance that the system can achieve,

only based on the channel response obtained in pulse generation mode

By comparison the measurement results in Chapter 6, it can be found that there is huge gap between the real case and the best performance. To explain this several possible reasons are given as follows.

1) In pulse generation mode, residual pulses are generated at the input of multiple drivers other than the target one.

On TX PCB, pulse generation control to MUX 2 might disturb the reference voltage provided on the PCB, which causes errors to be sampled on the on-chip sampling capacitors in the next clock cycles. As an illustration, Fig. E-3 shows a comparison between the normal pulse (blue) and the pulse with residuals in the next clock cycles (red). Fig. E-4 shows the received pulse responses at RX of the above two cases. From it we find that it is hard to distinguish their difference via time domain result. However, in the frequency domain the maximum residual-pulse-induced crosstalk between different “users” is observable, which is around -30dB, as shown in Fig. E-5.

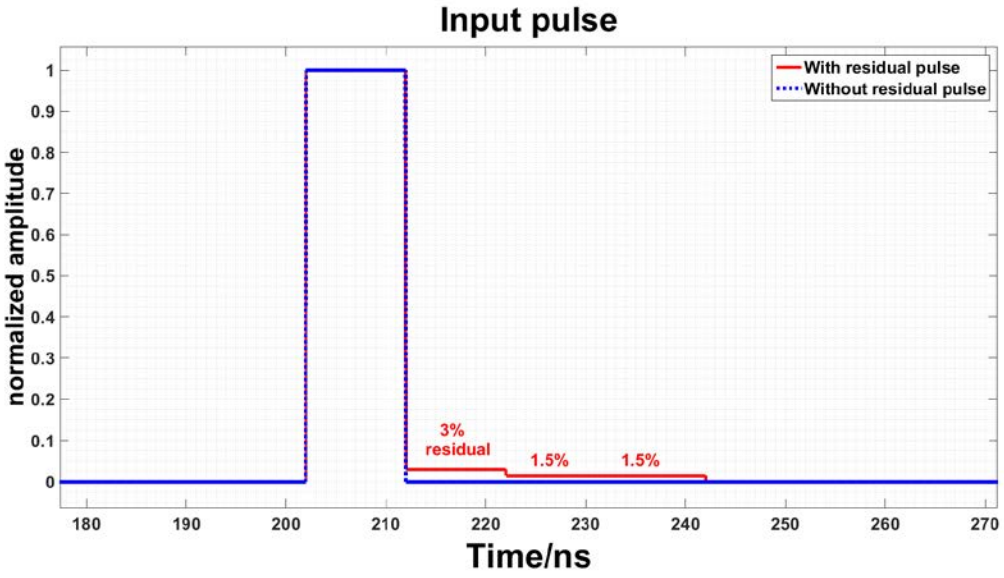


Figure E-3 Input pulses with and without residual pulse

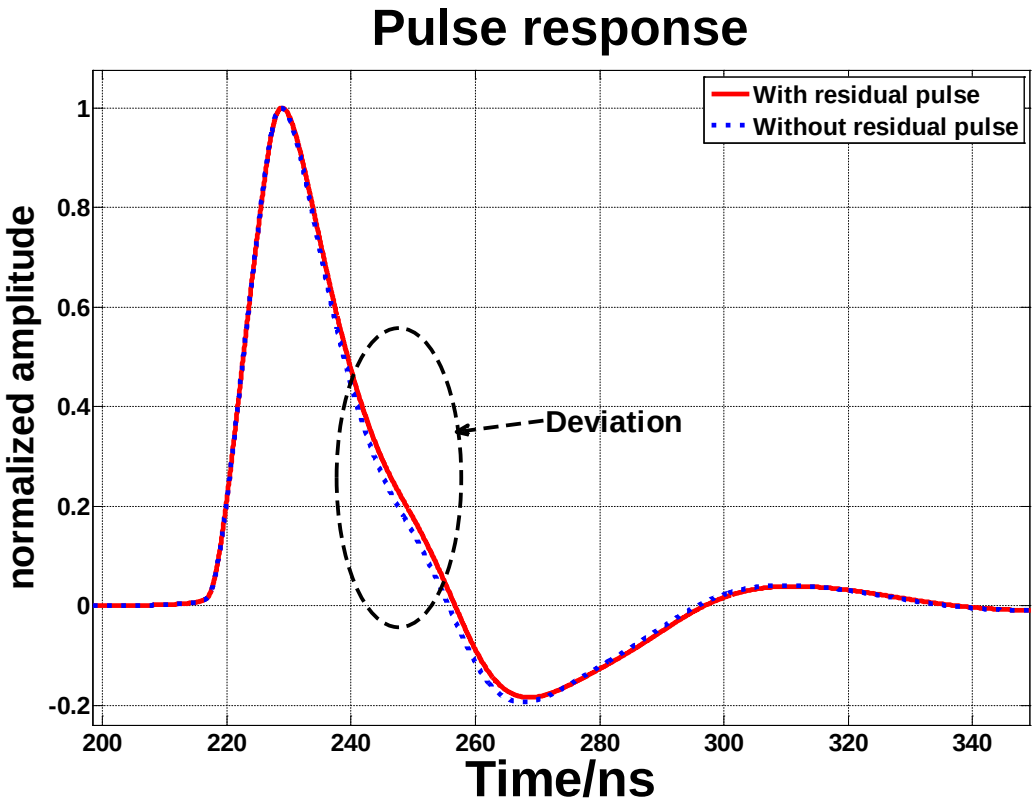


Figure E-4 Pulse responses with/without residual pulses

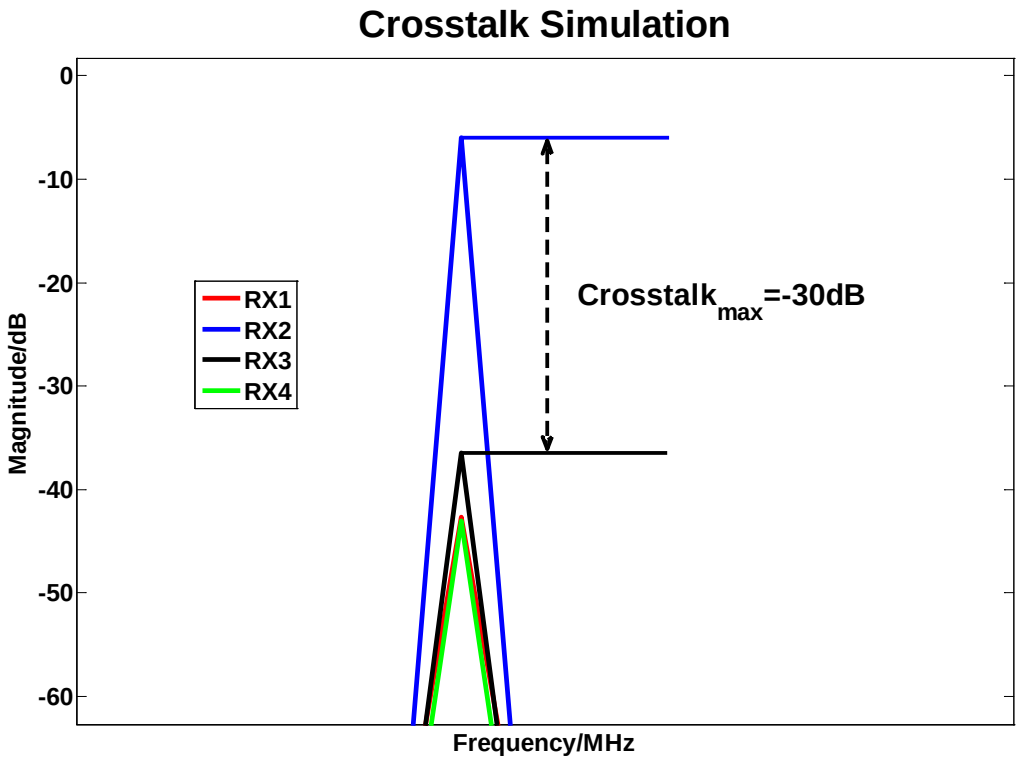


Figure E-5 Crosstalk due to residual pulses

2) In normal mode, signals are carried by the pulse with different width from the one measured in pulse generation mode

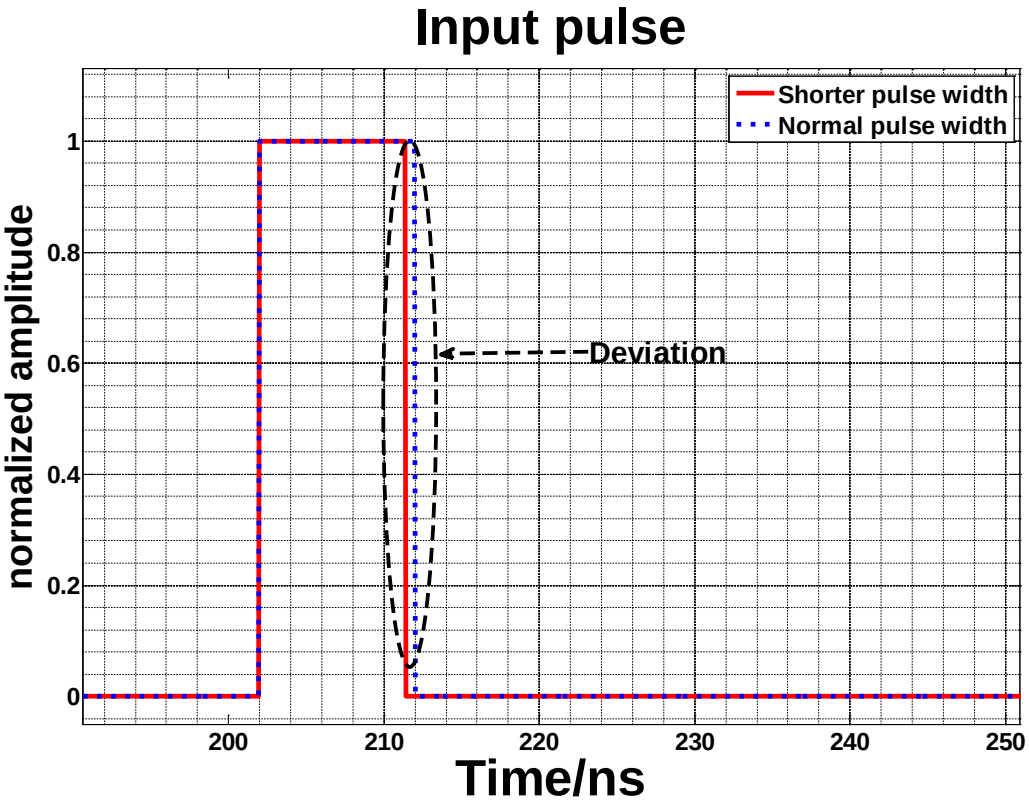


Figure E-6 Input pulses with different widths (red: 9.4ns, blue: 10ns)

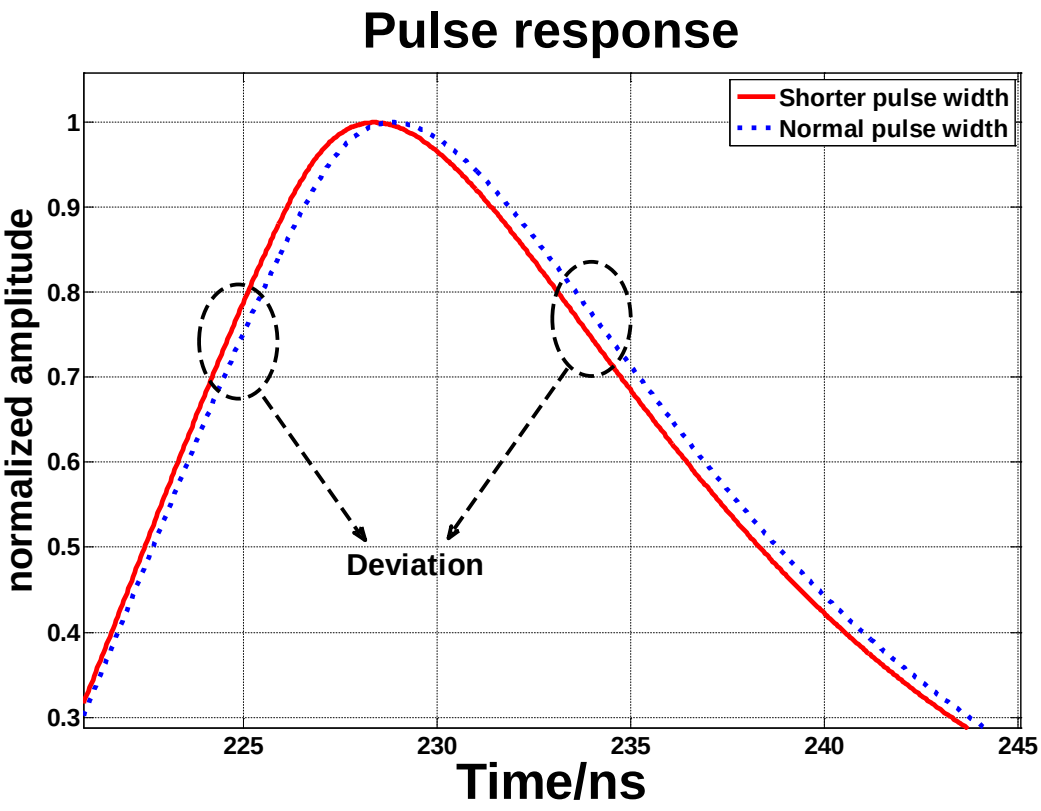


Figure F-7 Pulse responses with different pulse widths

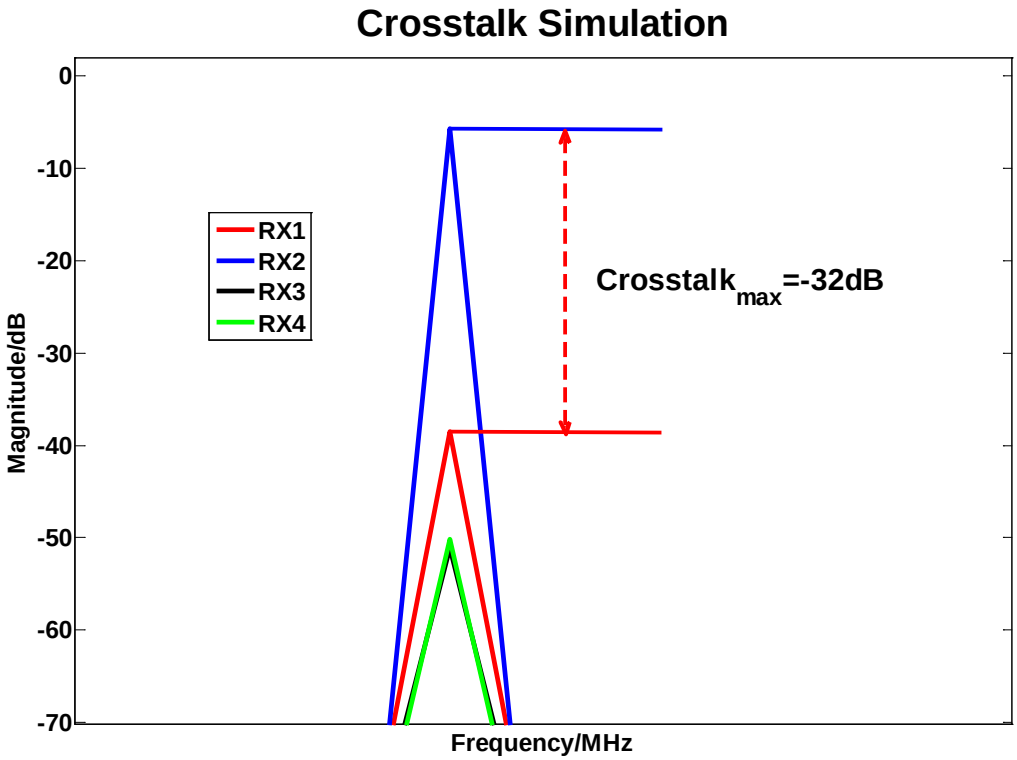


Figure E-8 Pulse responses due to different pulse width

3) RX distortion makes the pulse nonlinear in pulse generation mode, which forms a nonlinear "ruler" during equalization.

If RX distortion is non-dominant, the maximum crosstalk is independent of signal frequency. An easy way to check this assumption is to look at the 2nd order distortion term in one driver test, as shown in Fig. E-9. Here we find the maximum crosstalk at the 2nd order distortion (-2dB) is much larger than that at the signal frequency (about -30dB). And this result indicates that RX nonlinearity comes into effect during equalization.

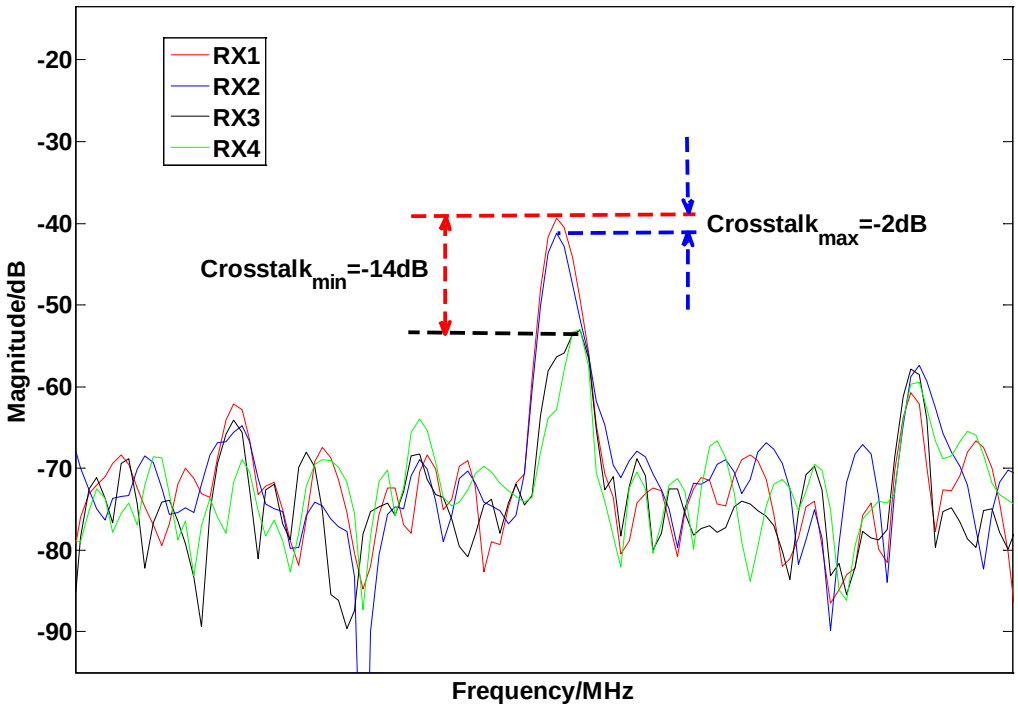


Figure E-9 Zoom-in plot of crosstalk at 2nd harmonic in single-driver test

Fig. E-10 shows a distorted pulse response with -30dB HD2, of which the distortion only comes at the RX. Fig. E-11 shows the calculated crosstalk, which also agrees with the measurement result.

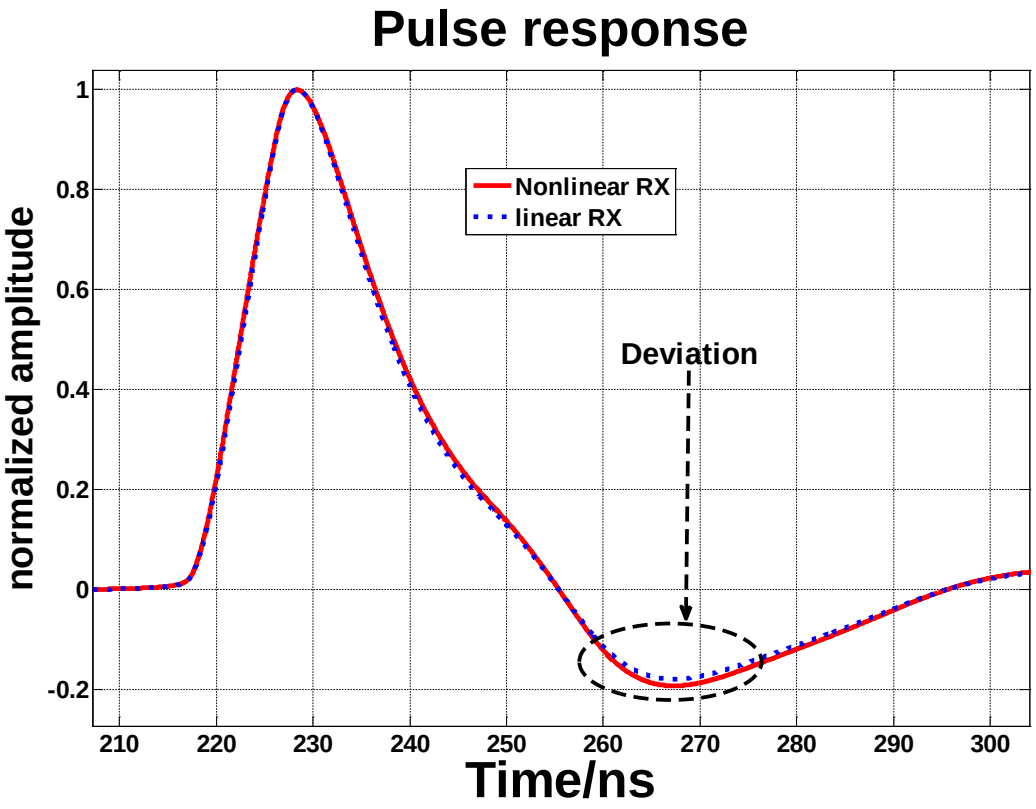


Figure E-10 Pulse responses with/without RX distortion

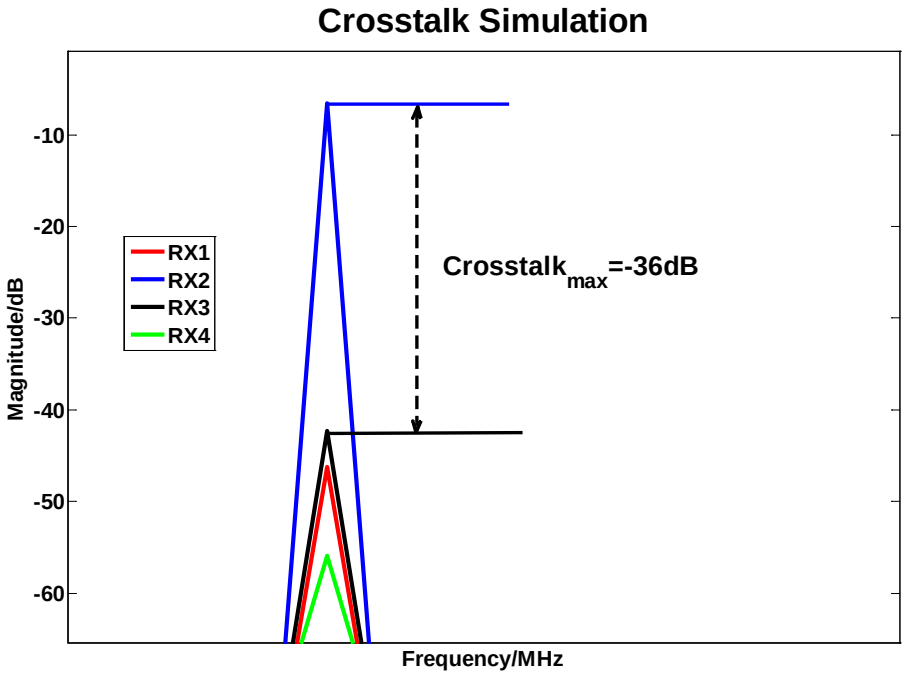
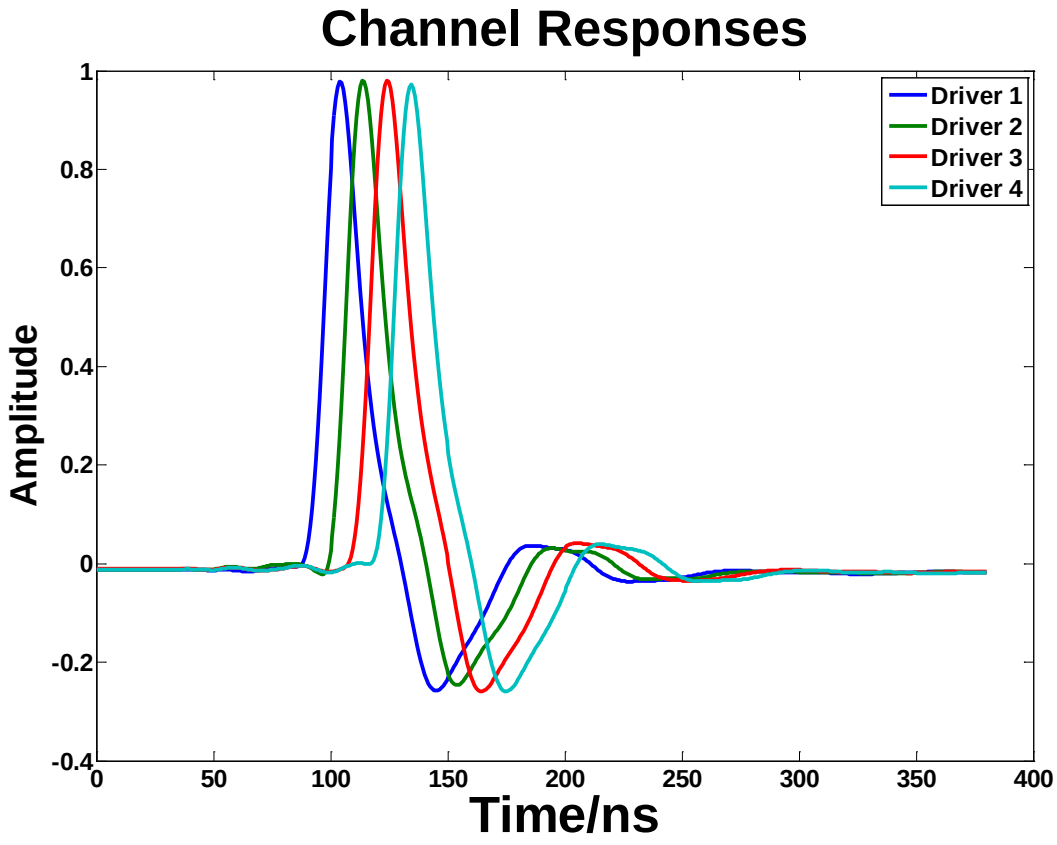


Figure E-11 Crosstalk caused by RX nonlinearity

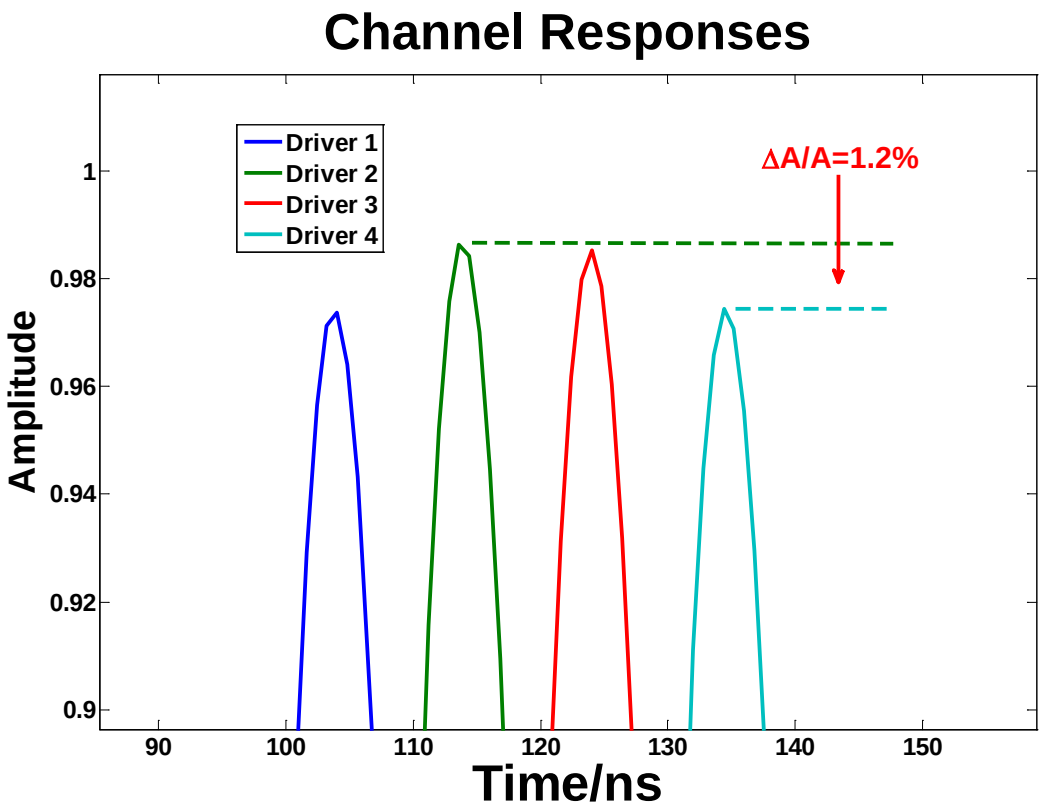
Appendix F Mismatch Analysis

1) Transconductance mismatch

Due to the mismatch between on-chip resistors, the drivers' resistor-defined transconduc-tance also varies. During equalization if all the drivers are taken as identical without considering the 1.2% mismatch shown in Fig. F-1, then after equalization there will be a maximum of -38 dB crosstalk among different receivers (corresponding 1.2% mismatch). And this number forms an upper limit in the crosstalk measurement.



(a) zoom-out plot



(b) zoom-in plot

Figure F-1 Transconductance mismatch between different drivers

2) Cap-to-cap mismatch

Being similar with the mismatch between different drivers, there exist mismatch between different sampling capacitors in one driver. Fig. F-2 shows the channel responses between 3 capacitors in one driver. From it can be found that the cap-to-cap mismatch is better than that between drivers. From this comparison we conclude that the crosstalk is more likely limited by driver-to-driver mismatch, and during equalization cap-to-cap mismatch is omitted for simplicity.

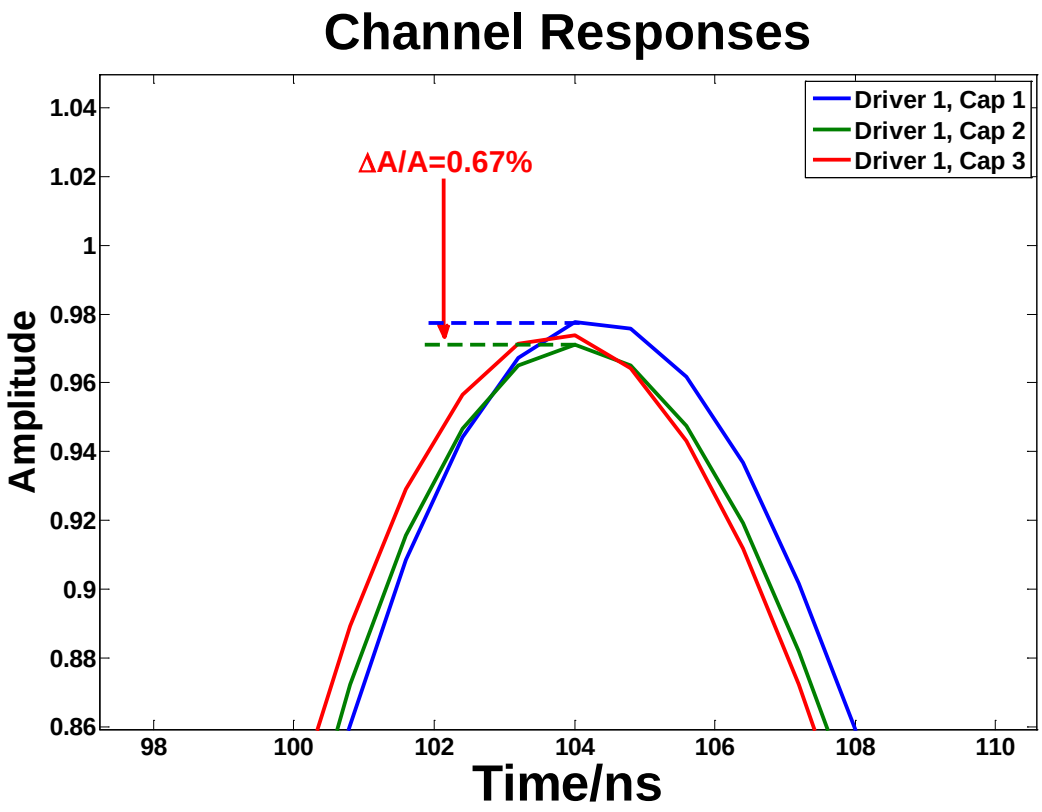


Figure F-2 Mismatch between different sampling capacitors in one driver