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The growth of carbon nanotubes on electrically conductive ZrN support layers for through-silicon vias

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ABSTRACT

State-of-the-art Cu-based through-silicon vias (TSVs) suffer from filling difficulties and reliability concerns. Carbon nanotubes (CNTs) are an attractive alternative filler material for TSV due to their high aspect ratio, attractive mechanical and thermal properties and high current carrying capability. However, so far tall enough CNT could only be grown on electrically insulating layers, limiting their electrical applications. In this work we demonstrate and investigate the growth of CNT with aspect ratios up to 30 on electrically conductive ZrN layers. This was used to fabricate the first CNT TSV devices which are contacted on both sides of the bundle by metal thin-films, instead of probe needles, which were subsequently electrically characterised.

1. Introduction

Three-dimensional (3D) integration has been suggested as a technique to reduce the delay and power losses of interconnects in very large-scale integration by allowing shorter wires to be routed between logic cells. Furthermore, this technique can be used to integrate different semiconductor technologies into a single package, for instance combining sensors and their read-out electronics fabricated in two different active layers [1,2]. Through-silicon vias (TSVs) are an essential component for 3D integration using die or wafer stacking [3]. With traditional wire bonding the number of connections between two stacked dies is limited to the periphery, while TSV can be used to connect the different active layers virtually anywhere over the die. TSV technology recently led to commercial applications in, for instance, stacked memory cells for large-scale computing [4].

Current TSV technology uses electroplated Cu as metal filler in combination with deep reactive ion etching (DRIE) to fabricate the through-silicon holes. In a conventional CMOS process the TSVs are fabricated after the logic circuits. This means that, in order to reach the back-side of the wafer or die, the holes have to be etched through the layer containing the active devices. Due to the limited aspect ratio (AR) of DRIE, and especially to ensure void-free Cu electroplating, much of the device area is lost to reserve space for these Cu TSV. This issue is partly resolved by wafer thinning to allow for smaller vias, however, this results in fragile wafers which complicate handling. Another issue with Cu as filler metal is the mismatch in the thermal expansion coefficient with Si which gives rise to stress. This introduces additional failure mechanisms in the back-end metal stack and influences the performance of nearby transistors, thus requiring a large exclusion zone [5]. Finally, Cu is a contaminant for the front-end and, therefore, requires effective diffusion barriers around the TSV in order to prevent contamination of the electronic devices on the chip.

Carbon nanotubes (CNTs) are an attractive candidate for replacing Cu for TSV. Due to their bottom-up nature in fabrication much higher aspect ratios are envisioned [6]. Moreover, CNT bundles have been shown to have sponge-like mechanical behaviour [7], have a low thermal expansion coefficient [8], current carrying capacity up to 10^9 A/cm^2 [9], and high thermal conductivity up to 3500 W/mK [10]. Finally, according to recent models [11,12], CNT can outperform Cu in terms of electrical performance for TSV applications. High aspect ratio CNT on electrically conductive substrates are also of interest for microelectromechanical systems [13] and super-capacitors [14,15].

In order to grow CNT, chemical vapour deposition is performed in combination with a nm-thin metal catalyst which breaks up into small nanoparticles upon heating. In order for this catalyst layer to successfully break-up into nanoparticles, and prevent diffusion into the Si, a support layer is required. An issue with current CNT TSV is that as support material only Al_2O_3 [6,16,17] or SiO_2 [18] has been used. Both are electrical insulators. While it has been demonstrated that it is possible to contact the CNT through <2 nm Al_2O_3 layers [19], this will result in a relatively high ohmic contact to the CNT as tunnelling will be the electrical

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transport mechanism. Although growth on metal support layers like TiN [20,21] or $CoSi_2$ [22] has been demonstrated, to the best of our knowledge, no CNT growth over 100 μm on conductive layers has been reported. Generally, the growth stops after several tens of μm. Thi is likely due to catalyst poisoning or encapsulation which stops the catalytic reaction [23].

In this work, we present a new electrically conductive ZrN support layer for the growth of CNT bundles with lengths well over 300 μm and with an AR up to 30. Raman spectroscopy, SEM, and TEM were used for analyses of the as-grown CNT. This support layer was then used to fabricate the first CNT TSV test structures using ZrN as the support layer, which were subsequently electrically characterised.

2. Materials and methods

The support layer consists of 30 nm of ZrN, which is reactively sputtered using an SPTS Sigma magnetron sputter coater from a pure Zr target using a gas mixture of Ar and N_2 at a substrate temperature of 350 °C. The resistivity of this ZrN layer is 5.5 mΩ-cm as determined by sheet resistance measurements. While CNT can be grown on ZrN layers as thin as 10 nm, 30 nm was used throughout this work. CNT are grown with 0.8 nm of Fe as the catalyst in an AIXTRON BlackMagic Pro CVD reactor with a specially optimized recipe in order to prevent the micro-loading effects reported before [24,25]. The recipe consists of a 5 min pre-anneal at 400 °C, followed by CNT growth for 255 s at 650 °C using 320/40 sccm of H_2/C_2H_2 at 80 mbar in order to reach a height of ~300 μm.

For the fabrication of CNT TSV test structures, a pair of wafers is prepared and bonded together using Si–Si direct bonding, see also Fig. 1. The bottom wafers contains a patterned 30 nm ZrN layer deposited in 120 nm deep windows etched into the Si wafer. On top of this, a 0.8 nm Fe layer is deposited using e-beam evaporation, and patterned using lithography and wet etching for 5 min in 10% HNO_3 at 50 °C. The top wafer of 300 μm thickness contains through-silicon holes with different diameters down to 25 μm, etched using DRIE with a PECVD SiO_2 hard-mask. Subsequently, the hard mask is removed and the wafers are oxidized using thermal oxidation to obtain a 700 nm SiO_2 isolation layer for the electrical isolation of the side walls of the opening. The SiO_2 of the bonding face of the wafer is removed using a combination of dry etching and BHF wet etching, after which the wafers are aligned and bonded at 3 kN and 300 °C under vacuum. Finally, CNTs are grown with a length similar to the top wafer thickness and the wafer is metallized using 100 nm of Ti and 3 μm of Al without breaking the vacuum. The Al is subsequently patterned in order to obtain 4-point probe measurement structures.

Measurements on the CNT were performed using a FEI XL50 SEM, FEI Tecnai G2 TEM, and Renishaw's inVia Raman spectroscope with 514 nm laser. For the static sessile drop test used to inspect the ZrN layer a Dataphysics OCA-20 contact angle setup was used with DI water, diiodomethane, ethylene glycol, and a mixture of 1:1 water and ethylene glycol as testing liquids. Electrical measurements were performed using a probe-station and Agilent 4156C parameter analyser.

3. Results and discussion

Carbon nanotubes bundles could be grown on top of ZrN using patterned Fe with AR well over 30, as is shown in Fig. 2a which displays a 10 μm and approximately 340 μm long CNT bundle. This is much higher than the future maximum required AR of 20 for TSV as stated in the latest ITRS roadmap [26]. Slight bending of the bundles with these aspect ratios has been observed, but it is expected that when the bundle is grown into a through-silicon opening the support from the sides will prevent this. Due to the limitations of the used DRIE, the maximum AR observed for CNT grown into through-silicon holes was 15 (total length of ~340 μm, Fig. 2b). The growth speed is 1.18 μm/s at 650 °C, which is much faster than regular Cu electroplating. The density of the bundle is estimated to be $4 \cdot 10^{10}$ tubes/cm^2, as observed by counting from Fig. 2c. By tuning the growth time the CNT could be grown with the same length as the 300 μm thick top wafer (Fig. 2d).

We postulate that the ZrN layer works as a good support layer due to its low surface energy, which according to Zhang et al. [22] aids in the dewetting (i.e. breaking up) of the catalyst thin-film into metal nanoparticles. To estimate the surface energy the static sessile drop technique was used with four different test liquids. From the average contact angle between the test liquids, the surface energy can be calculated using the different models available in the literature. Three different models were used to determine the surface energy, which were available in the SCA-21 software of the instrument: the Owens,

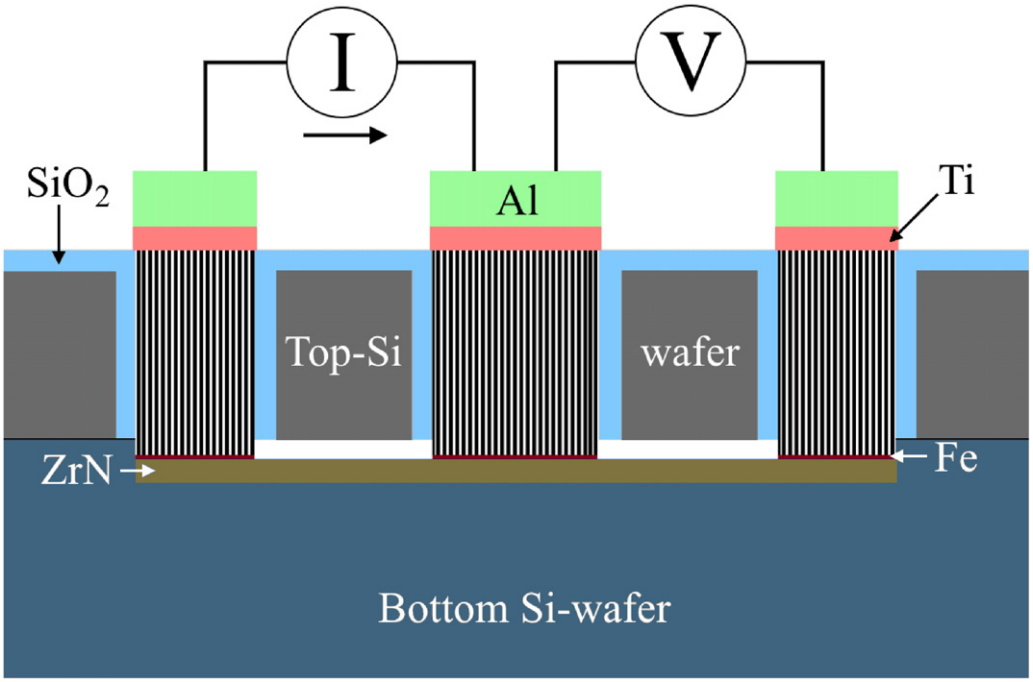

Fig. 1. Schematic cross-section of the 4-point probe measurement structure fabricated using the described method.

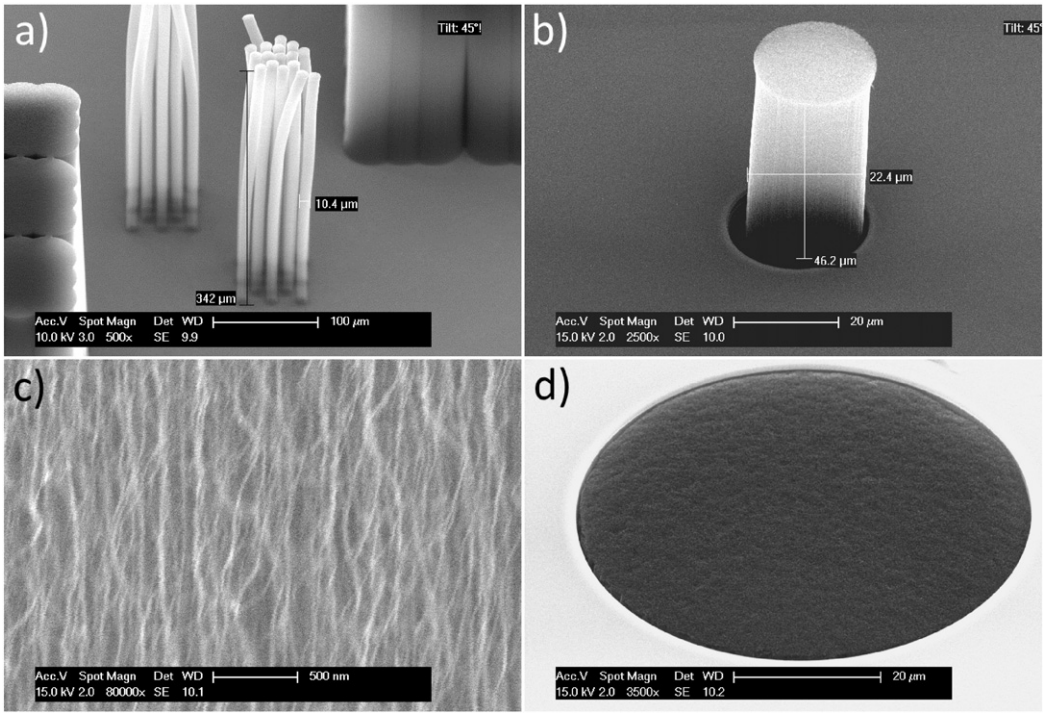

Fig. 2. SEM images of CNT grown on ZrN using 0.8 nm of Fe: a) high-aspect ratio bundles; b) bundle with AR 15 inside TSV opening; c) close-up of CNT bundles indicating alignment and density; d) 60 µm CNT bundle grown inside a 300 µm deep through-silicon hole.

Wendt, Rabel and Kaelble method (OWRK), Wu method, and Equation of State (EOS), of which the details can be found elsewhere [27]. The results calculated using the software are shown in Table 1. The surface energies are close to each other for the different materials. Compared to the surface energy of Fe (2.22 N/m = J/m^2 [22]) the measured surface energy of all these support layers are substantially lower, which should result in a good de-wetting of the catalyst. During the course of the research, other conductive ceramics like MoN and MoO_3 were also investigated and found to give no CNT nucleation. Indeed, when the contact angle of these layers was probed complete wetting of all test liquids was observed (0° contact angle). This indicates a high surface energy.

Fig. 3 displays a TEM image of CNT grown using the growth recipe mentioned in the previous section. As can be observed the sample contains both double-walled and multi-walled tubes. The average diameter was found to be 7 nm. Some kinks are observed, indicating defects are present in the CNT. Using Raman spectroscopy, the crystallinity (or quality) of the CNT can be investigated in more detail [31]. The obtained Raman spectrum can be found in Fig. 4. The ratio between the D and G-band intensities ($I_{D/G}$ = 0.54) can be related to the in-plane ordering length (L_a) of the graphene sheets in the CNT, which for these samples is ~8 nm [32]. The crystallinity of these CNTs is better than that of CNT grown on Al_2O_3 or SiO_2 at similar temperature [7,18], which reported $I_{D/G}$ ratios of 1.1 and 0.7, respectively. We found that it is possible to further improve the L_a to 50 nm ($I_{D/G}$ of 0.1) by tuning the recipe. Unfortunately, this resulted in short CNT growth when the catalyst was patterned due to micro-loading effects [25].

Table 1
Surface energies (in mN/m or mJ/m^2) determined using sessile drop technique for the different models compared with the literature.

Material	OWRK	Wu	EOS	Literature
TiN	53.9	61.0	49.3	41–63 [28], 47 [29]
SiO_2	62.3	68.5	54.7	43–106 [22]
Al_2O_3	38.9	44.1	38.5	62–100 [22]
ZrN	55.3	61.3	50.2	36–43 [28], 47.7 [30]

Using four-point probe structures (Fig. 1) electrical measurements were performed on a CNT TSV structures as shown in Fig. 1. Fig. 5 displays the I–V characteristics of bundles with a diameter of 60 µm and 75 µm, and length of 300 µm. The response is linear, which indicates that the CNT-ZrN and CNT-Ti contacts are ohmic. The resistivity of the 60 µm and 75 µm vias, including the contact resistances, are 431 mΩ-cm and 1455 mΩ-cm, respectively. This is a factor 10 higher than results from the literature [18,17]. However, those results omitted the contact resistance by using bundles of different lengths and were fabricated at 700 °C. The exact cause of the large spread in resistance is unclear. As the length of the bundles is similar and the structures were relative close to each-other, we suspect that there are large variations in the contact resistance. As the top metal contact are sputtered, a bundle that has a slight mismatch in height compared to the top wafer can have poor conformal coating of the metal. Chemical mechanical polishing can aid in reducing these height differences. However, this will require improved mechanical support of the CNT in order to prevent the polishing action from removing the CNT from the holes

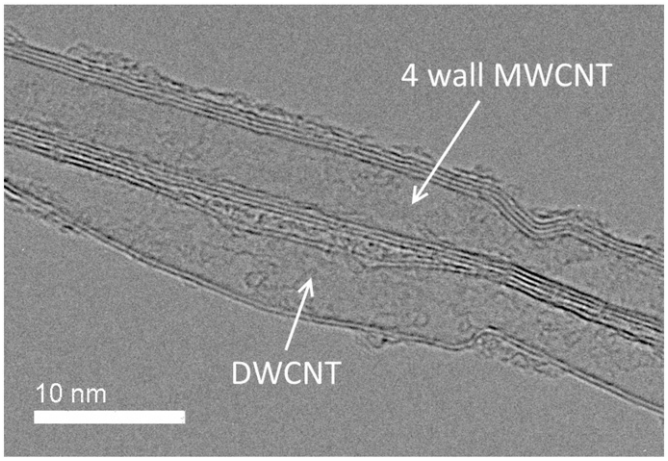

Fig. 3. Typical TEM image of CNT grown on ZrN using the growth recipe used in this work.

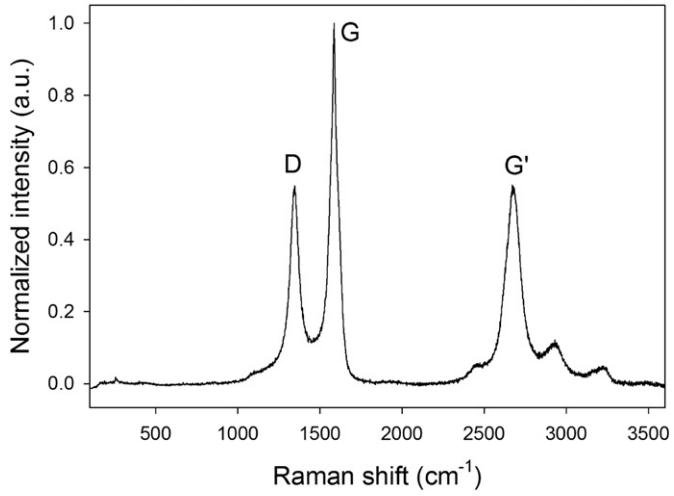

Fig. 4. Raman spectrum of CNT grown on test samples using the same growth recipe. The intensity is normalized to the G-band.

altogether [33]. This can, for instance, be done using spin-on-glass or plasma-enhanced CVD SiO_2 [34,35]. Further measurements on CNT TSV with different lengths are required to extract the contact resistance and determine the resistivity of the CNT bundle in these structures.

To the best of our knowledge, these are the first CNT TSV where both ends of the CNT bundle are directly contacted using metal thin-films, instead of probe-station tips as used in the literature [18,17,6]. This results in more accurate measurements under conditions more close to that of actual TSV. Moreover, the aspect ratios of the CNT bundles obtained here are significantly higher than the previously reported AR of 10 [6]. The direct growth of CNT on electrically conductive layers is an important step towards realizing CNT TSV.

4. Conclusion

In this work, we demonstrate ZrN as a novel electrically conductive catalyst support layer for the growth of long CNT bundles, as opposed to the generally used non-conductive support layers. We obtained aspect ratios up to 30 for free-standing CNT bundles and up to 15 for CNT bundles inside through-silicon openings. Using this material the first CNT TSVs that on both sides are contacted by metal thin-films were fabricated. The resistivity of the lowest resistance CNT TSV was found to be 431 mΩ-cm, which includes the contact resistance to the CNT bundle. Further investigation is required to determine if this high resistivity is due to the contact resistance, or if an even higher CNT density and crystallinity are required. The latter can be achieved by recipe tuning. Growth on electrically conductive layers is an important step forward in the realization of CNT TSV and can be used for other applications in which high aspect ratio CNT requires electrical contact.

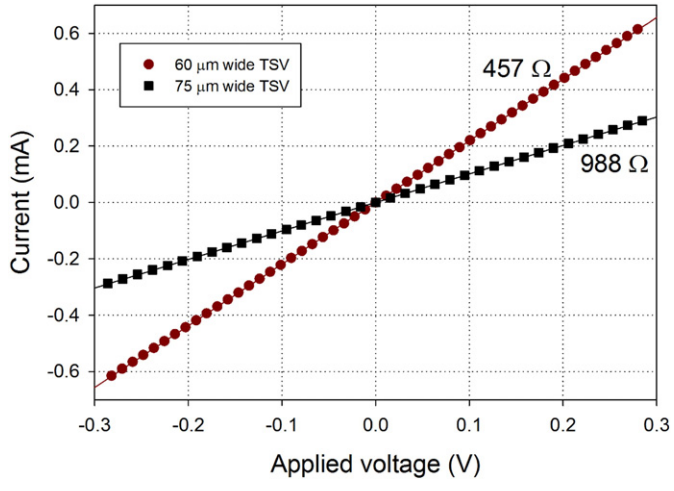

Fig. 5. I–V characteristics of CNT TSVs with diameters of 60 µm and 75 µm, and length of 300 µm (AR 5 and 4, respectively), measured using 4-point probe structures.

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